EE360R — Midterm 2.a

Spring 2003

Name:

- Max marks = 50, Time = 50 mins
- Open book, open notes
- Write your answers on the exam
- Show your work and give explanations

1. Latches and clocking

   (a) Explain why the setup time of the latch below is the time taken for the output Q to switch from 0 to $V_{\mathrm{DD}}/2$ when the data input D steps from 0 to V_{DD}. (Assume the rise and fall times are symmetric throughout.)

5 marks

   (b) What is the **single greatest** advantage of 2-phase clocking over single phase clocking for positive level sensitive latch-based designs?

   (Warning—you could spend 50 minutes giving a detailed answer with figures, numbers, etc.; I only want a short answer that's to the point.)

5 marks

2. PLAs

A PLA can implement two-level (AND-OR) logic using INV-NOR-NOR-INV, with pseudo-NMOS implementations of NOR.

(a) What is the primary **disdvantage** with such an implementation?

(b) How can dynamic logic be used to overcome this problem?

10 marks

3. Timing

(a) Design a static CMOS gate implementing the function

$$((X' + Y') \cdot (Z' + W' + U') + V') \cdot S'$$

(b) Size the devices so that the output resistance is that of an inverter whose NMOS has $W/L = 2$ and PMOS has $W/L = 6$.

15 marks

4. Adders

Figure **A** below shows a schematic of a circuit called the "conditional adder cell" (CAC).

(a) What Boolean functions of the inputs are the four outputs S^0, S^1, C^0, C^1 computing?

(b) Based on the above explain how the schematic in Figure **B** below implements an adder.

15 marks