EE 360R — Computer-aided IC Design | Fall 2007
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Office Hours: TuTh 11:00-12:00 | Lecture: TuTh 9:30-11:00, ENS 302

Description:

We aim to study the process of implementing a digital system as a CMOS integrated circuit.

The course will begin with a review of the basics of CMOS transistor operation and the manufacturing process for CMOS VLSI chips.

We will then study in detail the problem of implementing logic gates in CMOS. Specifically, we will cover layout, design rules, and circuit families.

Afterwards, we will examine techniques for analysing and optimizing timing and power at the circuit level. We will study sequential elements—latches and flops—and clocking. This will be followed by an overview of datapath design: detection logic, shifters, comparators, adders, and multipliers. We will also study memories, specifically the workhorse 6-T SRAM cell as well as peripheral decode logic.

The course will conclude with a survey level treatment of various topics, including advanced circuit design techniques, clock tree design, functional verification, test, design-for-test, electrical effects, packaging, and future trends.

Prerequisites:

This course is intended for ECE undergraduate students. A knowledge of digital logic design (EE316 or its equivalent), and Computer Architecture (EE360N, or its equivalent) is required.

Recommended text:

- Principles of CMOS VLSI Design. N. Weste and D. Harris. *3rd Edition*, 2005. Addison-Wesley.

Web site: All material related to the course is available at `www.ece.utexas.edu/~adnan`

Format/Evaluation:

I will assign approximately 6 written homeworks, which will consist of questions from the book, and will be worth 5% of your grade. There will be two in-class midterms and a final exam, collectively worth 65% of your grade. Three major design projects will make up the remainder of your grade.

Outline

Week	Material
	Preliminaries
Aug 30	Introduction, history
Sep 4	MOS transistor theory
Sep 6	MOS transistor theory, Lab 1 presentation
Sep 11	CMOS processing
Sep 13	Circuit characterization
	CMOS circuit and logic design
Sep 18	Basic logic gate design
Sep 20	Lab 1 & Basic physical design
Sep 25	Basic physical design
Sep 27	Circuit families
Oct 2	Circuit families (by David Pan), Lab 2 presentation
Oct 4	Latch design (by David Pan)
Oct 9	Clocking-1
Oct 11	Midterm 1
Oct 16	Lab 2& Clocking-2
	Datapath and memories
Oct 18	Datapath—adders
Oct 23	Datapath—multipliers
Oct 25	MOS memory arrays—1
Oct 30	MOS memory arrays—2
	Timing optimization
Nov 1	Timing analysis, Lab 3 presentation
Nov 6	Timing optimization
Nov 8	Lab 3 & RTL Synthesis
Nov 13	Midterm 2
	Topics
Nov 15	Verification
Nov 20	Testing
Nov 27	DFT
Nov 29	Clock trees, PLLs
	Conclusion
Nov 29	I/O
Dec 4	Scaling-1
Dec 6	Scaling-2

NOTE: All departmental, college and university regulations concerning drops will be followed. The University of Texas at Austin provides upon request appropriate academic adjustments for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, 471-4241 TDD.