Current Mirror

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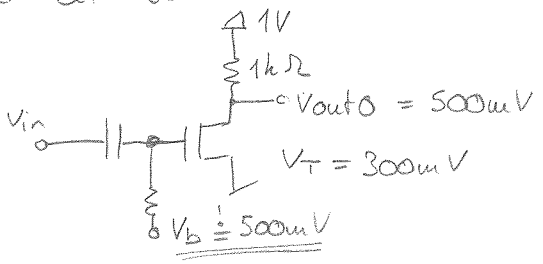
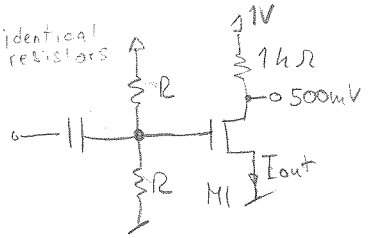
2/15/07

Motivation

- The following transistor in common source configuration needs to have its gate biased at 500mV



Solution #1 : Voltage bias



Q: what happens if V_T is 50mV smaller? (Process, Temp. variation)

A:

Equations: $I_{out} = \frac{0.5V}{1000\Omega} = 500\mu A$

$$\begin{cases} 500\mu A = \frac{\beta}{2}(500mV - 300mV)^2 \\ I_{out2} = \frac{\beta}{2}(500mV - 250mV)^2 \end{cases}$$

$$\frac{I_{out2}}{500\mu A} = \frac{(250mV)^2}{(200mV)^2}$$

$$I_{out2} = 500\mu A \frac{0,0625}{0,04} = 500\mu A \cdot 1,5625 \approx 781\mu A$$

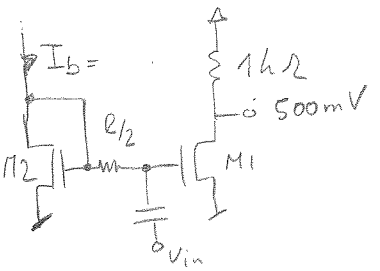
$$\Rightarrow V_{out0} = 1V - 781\mu A \cdot 1k\Omega = 219mV$$

because $V_{out0} < V_{GS} - V_T$ (219mV < 250mV)

M1 is no more working in saturation!

Bad Bias Technique

Solution #2 : current bias



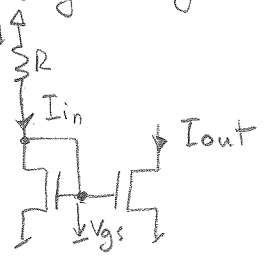
Q: what happens if V_T is 50mV smaller?

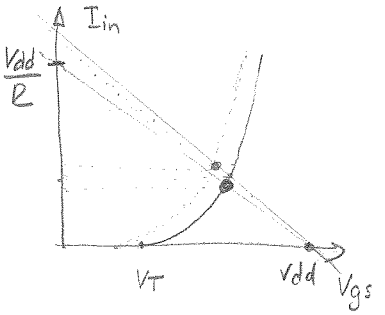
A: assuming $r_{o1}, r_{o2} = \infty$, M1, M2 are identical and $I_b = 500\mu A$, the output voltage will remain unchanged and the circuit will keep working.

Good bias technique

⚠ CMOS transistors are always biased using currents! Do never use absolute voltages, even when you are "playing" with simulator

Example of an easy way to generate a reference current:





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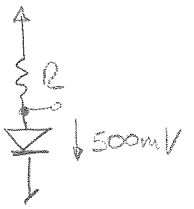


Finding R:

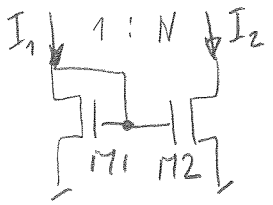
- I_{in} is known
- $\beta = \chi' \frac{W}{L}$ is also known
- $v_{gs} = \sqrt{\frac{2I_{in}}{\beta}} + V_T$

$$\Rightarrow \boxed{R = \frac{V_{dd} - v_{gs}}{I_{in}} = \frac{V_{dd} - V_T - \sqrt{\frac{2I_{in}}{\beta}}}{I_{in}}}$$

The resistor is usually off-chip so that one can tweak it to change the bias current.

- In real products better stability and supply voltage independency are required. A bandgap based reference generator is used.

Principle



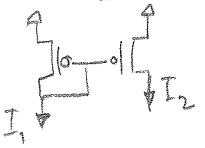
$$\begin{cases} I_1 = \frac{\chi'}{2} \frac{W_1}{L_1} (V_{GS1} - V_T)^2 (1 + \lambda_1 V_{GS1}) \\ I_2 = \frac{\chi'}{2} \frac{W_2}{L_2} (V_{GS1} - V_T)^2 (1 + \lambda_2 V_{DS2}) \end{cases}$$

← Note that M1 is always in saturation because $V_{DS1} = V_{GS1} > V_{GS1} - V_T$

$$\frac{I_1}{I_2} = \frac{\frac{\chi'}{2} \frac{W_1}{L_1} (V_{GS1} - V_T)^2 (1 + \lambda_1 V_{GS1})}{\frac{\chi'}{2} \frac{W_2}{L_1} (V_{GS1} - V_T)^2 (1 + \lambda_2 V_{DS2})}$$

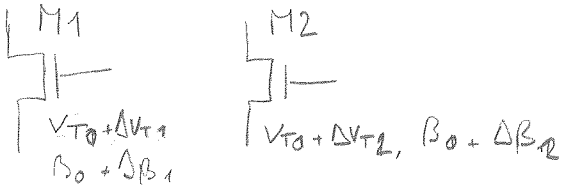
$$\boxed{\frac{I_1}{I_2} = \frac{W_1}{W_2} \frac{1 + \lambda_1 V_{GS1}}{1 + \lambda_2 V_{DS2}}}$$

- If the output impedance is ∞, i.e., $\lambda_1 = \lambda_2 = 0$ then the current ratio is $\boxed{N = \frac{W_2}{W_1}}$
- Big N's ($N = 10 \ldots 20$) are used to reduce the bias current I_1 assuming the operating current I_2 is fixed
- the NMOS mirror is called current sink. The PMOS mirror is called current source



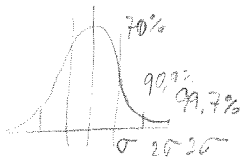
(2A) Transistor ~~Current~~ Mismatch ~~in a Current Mirror~~

- Two real transistors are never identical



$$\begin{cases} \sigma_{\Delta V_T} = \dfrac{A_{VT}}{\sqrt{WL}} \\ \dfrac{\sigma_{\Delta\beta}}{\beta_0} = \dfrac{A_\beta}{\sqrt{WL}} \end{cases}$$

- A_{VT} and A_K are two empirically measured constants
- σ_T, σ_β are the standard deviations of corresponding random variables that are assumed to have a Gaussian distribution
- ΔV_T and $\Delta\beta$ are random variables like noise therefore they add in rms way



- The correlation between V_T and β is very low therefore their effect adds in rms way, as well

- Note that usually $\sigma_{\Delta V_T}$ and $\frac{\sigma_{\Delta\beta}}{\beta}$ are given as the σ between two devices. Therefore the σ of a single device from its nominal value is $\times\sqrt{2}$ smaller

$$\sigma^2_{\Delta V_T} = \sigma^2_{V_{T1},abs} + \sigma^2_{V_{T2},abs}$$

$$= 2\,\sigma^2_{V_T,abs} \quad \text{[if devices have the same size]}$$

$$\boxed{\sigma_{V_T,abs} = \frac{\sigma_{\Delta V_T}}{\sqrt{2}}}$$

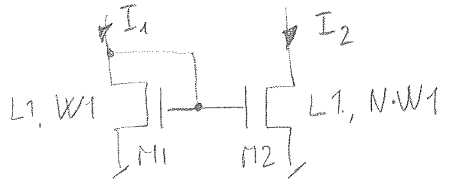
- The way two transistors are laid out can affect their matching factors. The more symmetric they are the better they match

- $\boxed{\sigma_{\Delta V_T} \approx 3\text{-}5\,mV}$ for a deep sub-micron technology

Current Mismatch in a Mirror

- Due to transistor mismatch, the current will never be the same in a mirror, even if $V_{DS1} = V_{DS2} = V_{GS1}$.

- Current mismatch calculation:



$$\begin{cases} \sigma^2_{V_{GS1}} = \sigma^2_{VT1} + \left(\frac{\sigma_{\beta 1}}{\beta_1}\right)^2 \cdot (V_{GS1} - V_T)^2 \\ \sigma^2_{V_{GS2}} = \sigma^2_{VT2} + \left(\frac{\sigma_{\beta 2}}{\beta_1}\right)^2 \cdot (V_{GS2} - V_T)^2 \end{cases}$$

$V_{GS2} = V_{GS1}$
$L_2 = L_1$
$W_2 = N W_1$

$$\sigma^2_{\Delta I} = \left(V^2_{GS1} + V^2_{GS2}\right) g^2_{m2} =$$

$$= g^2_{m2} \cdot \left[\sigma^2_{VT1} + \sigma^2_{VT2} + \left(\frac{\sigma_{\beta 1}}{\beta_1}\right)^2 (V_{GS1} - V_T)^2 + \left(\frac{\sigma_{\beta 2}}{\beta_2}\right)^2 (V_{GS1} - V_T)^2 \right]$$

$$= 2 I \frac{\chi' N W_1}{L_1} \left[\frac{A^2_{\Delta VT}}{2 W_1 L_1} + \frac{A^2_{\Delta VT}}{2 N W_1 L_1} + \left(\frac{A^2_\beta}{2 W_1 L_1} + \frac{A^2_\beta}{2 N W_1 L_1} \right) (V_{GS1} - V_T)^2 \right]$$

$$= \frac{I \chi' N}{L_1^2} A^2_{\Delta V_T} \left(1 + \frac{1}{N}\right) + \frac{I \chi' N A^2_\beta}{L_1^2} (V_{GS1} - V_T)^2 \left(1 + \frac{1}{N}\right)$$

$$= \boxed{\frac{I \chi' N}{L_1^2} \left(1 + \frac{1}{N}\right) \left[A^2_{\Delta V_T} + A^2_\beta (V_{GS} - V_T)^2 \right]}$$

$$\Rightarrow \boxed{\left(\frac{\sigma_{\Delta I_2}}{I_2}\right)^2 = \frac{\chi'}{L_1^2} \left(1 + \frac{1}{N}\right) \left[A^2_{\Delta V_T} + A^2_\beta (V_{GS} - V_T)^2 \right]}$$

- matching improves $L_1 \uparrow$
- matching gets worse when $\sqrt{N} \uparrow$
- the second term in the brackets is usually negligible for normal $V_{GS} - V_T$, however it can contribute if $V_{GS} - V_T$ is big.
- if more mirrors are connected to the chain, the current errors will sum in an rms way.

Mismatch due to voltage unsymmetry

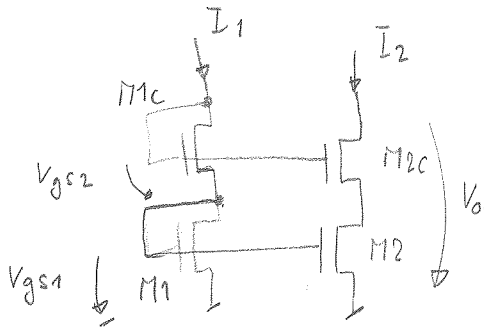
- As we have seen before, if the transistor $\lambda_1 \cdot \lambda_2 \neq 0$ and $V_{gs1} \neq V_{ds2}$ there is a deterministic mismatch of the mirror currents. → maximize r_o !

$$\frac{I_1}{I_2} = \frac{1 + \lambda_1 V_{GS1}}{1 + \lambda_2 V_{DS2}}$$

Cascode Current Mirrors

- In the last class we showed that the cascode structure can boost the transistor impedance

Cascode Mirror #1

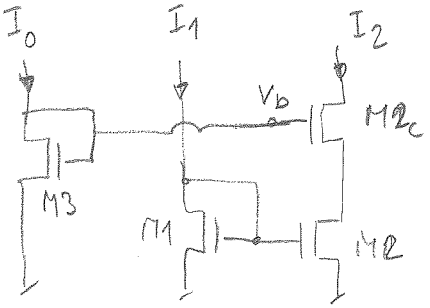


+ : λ is reduced by a factor $\approx g_{m2} r_{o2c}$

- : large minimum V_{out} to keep M2, M2c in saturation

→ $V_{out,min} = V_{gs1} + V_{gs2} - V_{T2} = V_{DSat1} + V_{DSat2} + V_{T1}$

Cascode Mirror #2



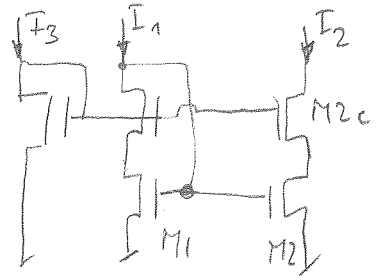
+ : V_b can be selected such that $V_{out,min} = V_{DSat2} + V_{DSat2c}$ → $V_{out,min}$ is small

+ : High output impedance → I_2 is insensitive to variations of V_{out}

- : not precise because λ_1 is still high

- : needs an additional bias current

Cascode Mirror #3



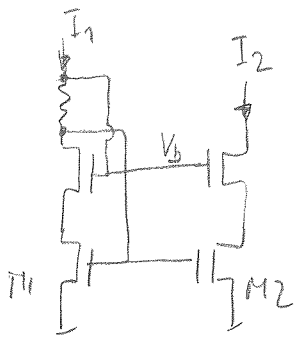
→ Most widely used

\+ : both sides of the mirror are high impedance

\+ : min $V_{out,min} = V_{DSat_2} + V_{DSat_{2c}}$ can be obtained

\- : needs an additional bias current

Cascode Mirror #4



\+ : both sides are high imp.

\+ : min $V_{out,min}$

\+ : no additional bias current needed

\- : V_b does not alway track process / temp variations, $V_{out,min}$ is not always optimum