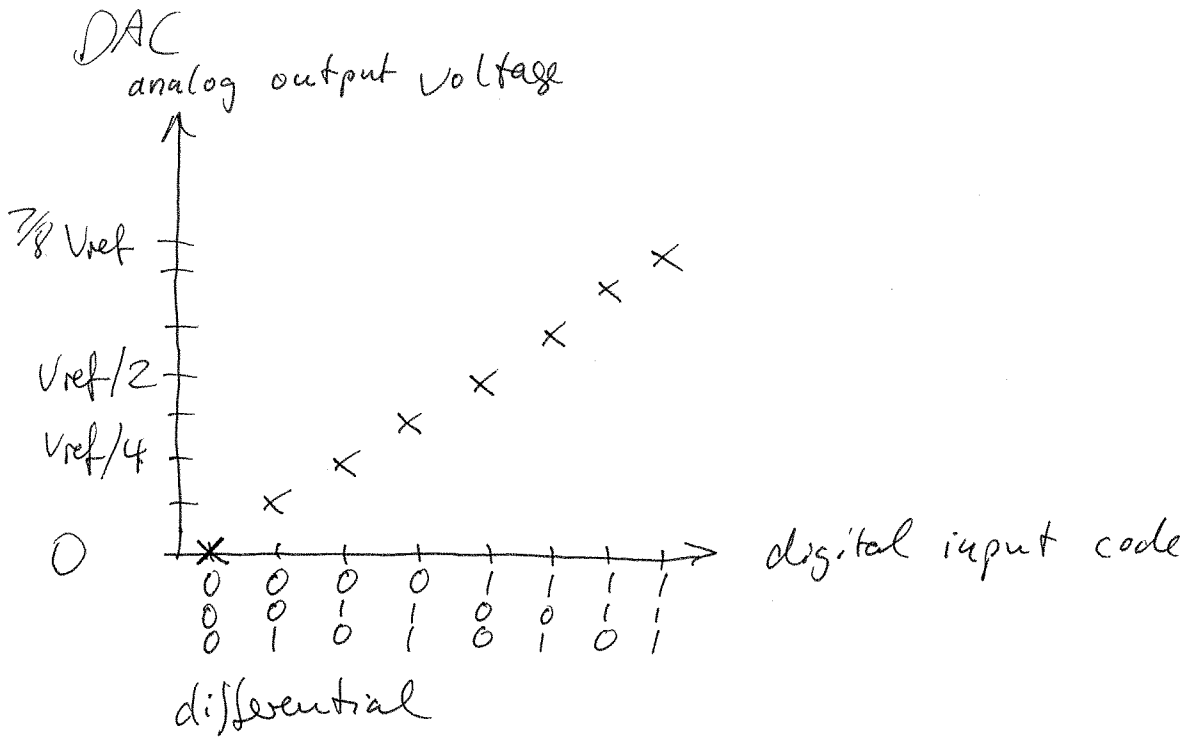
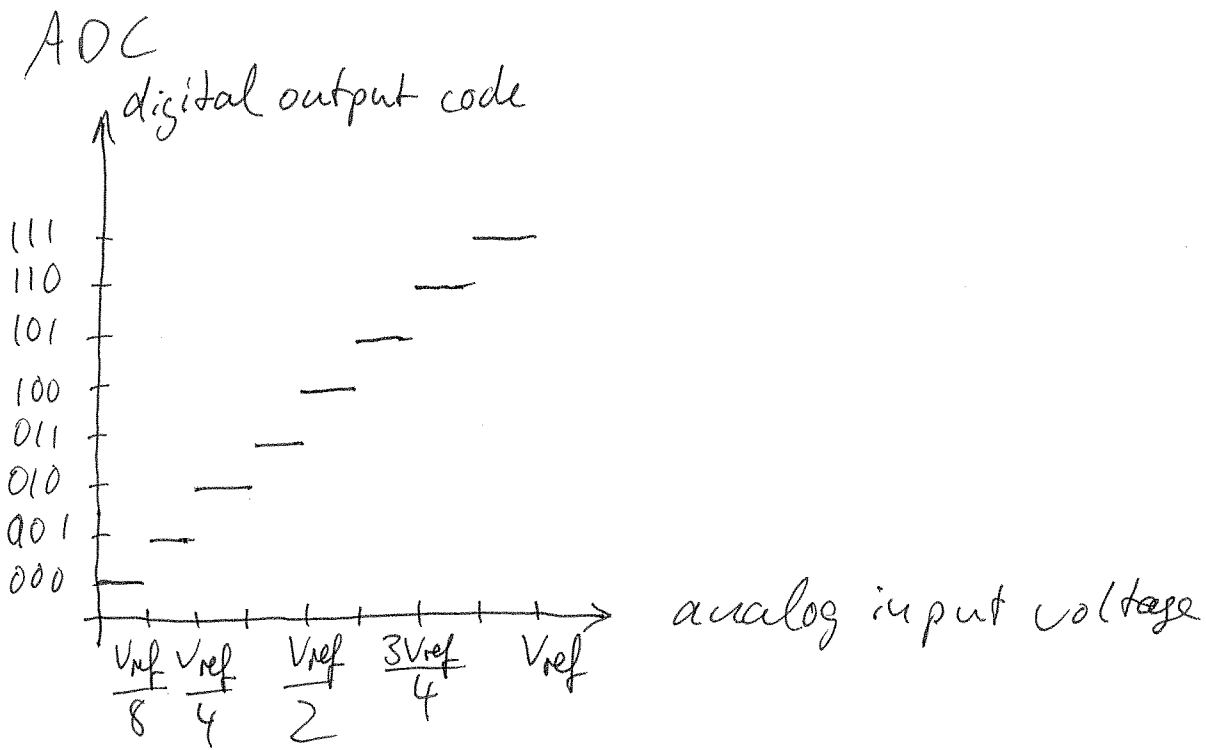
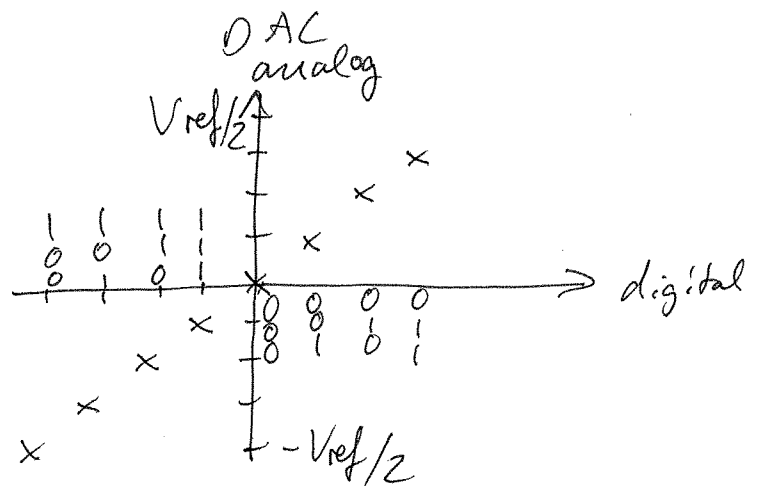
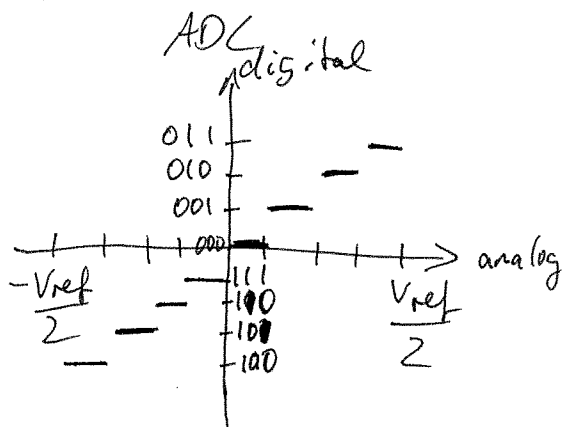
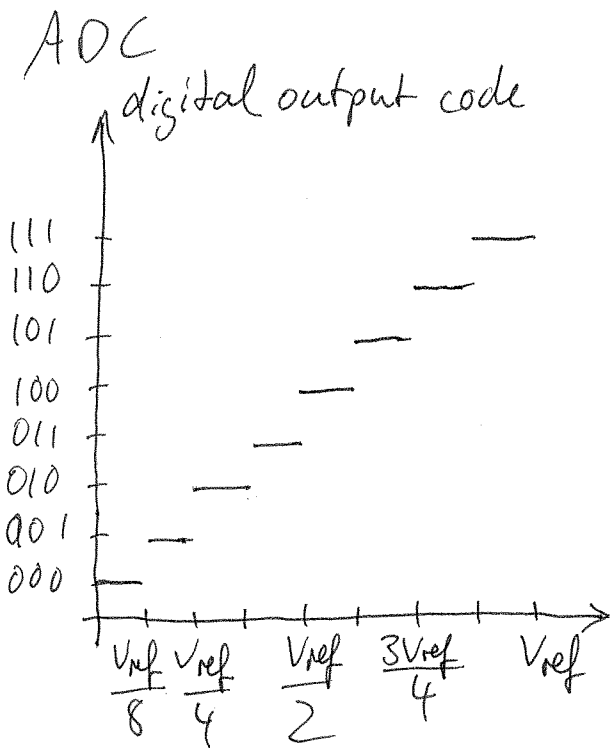




differential

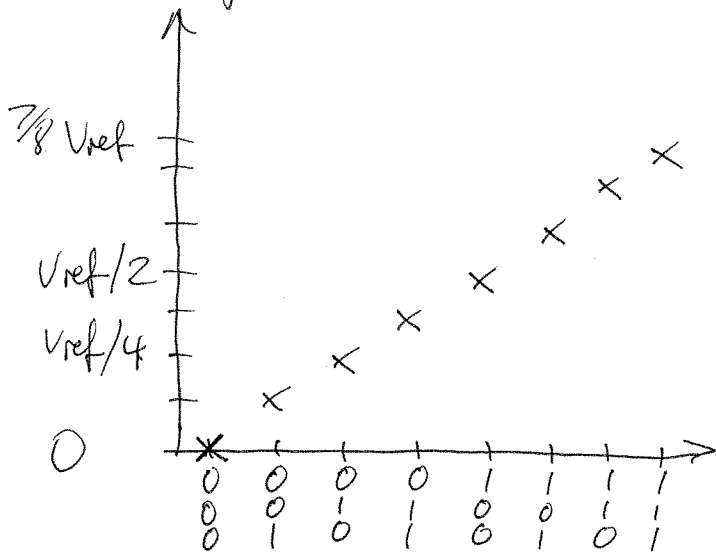




analog input voltage

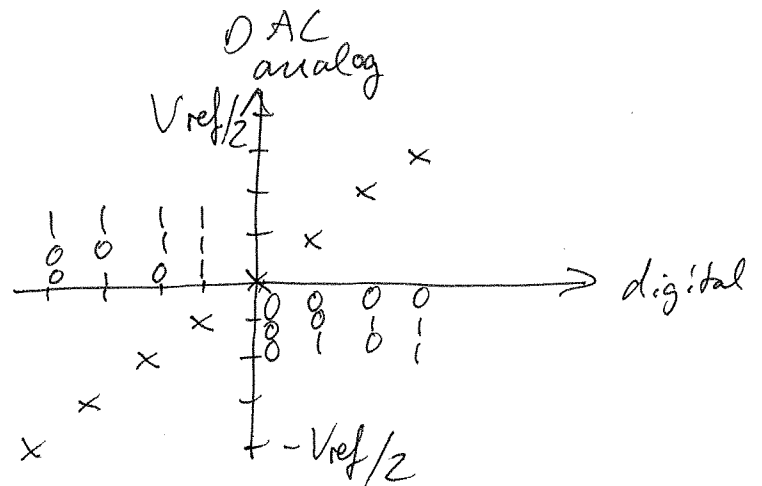
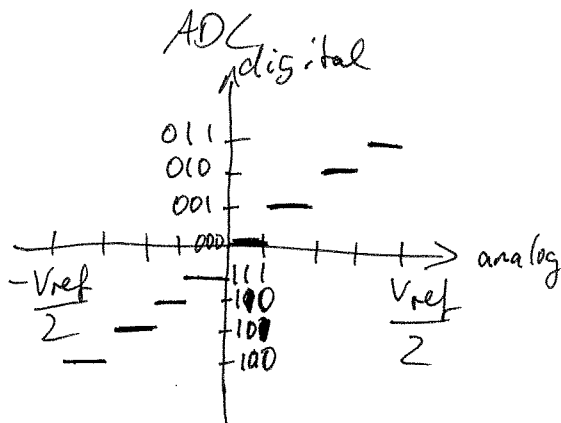
### DAC

analog output voltage

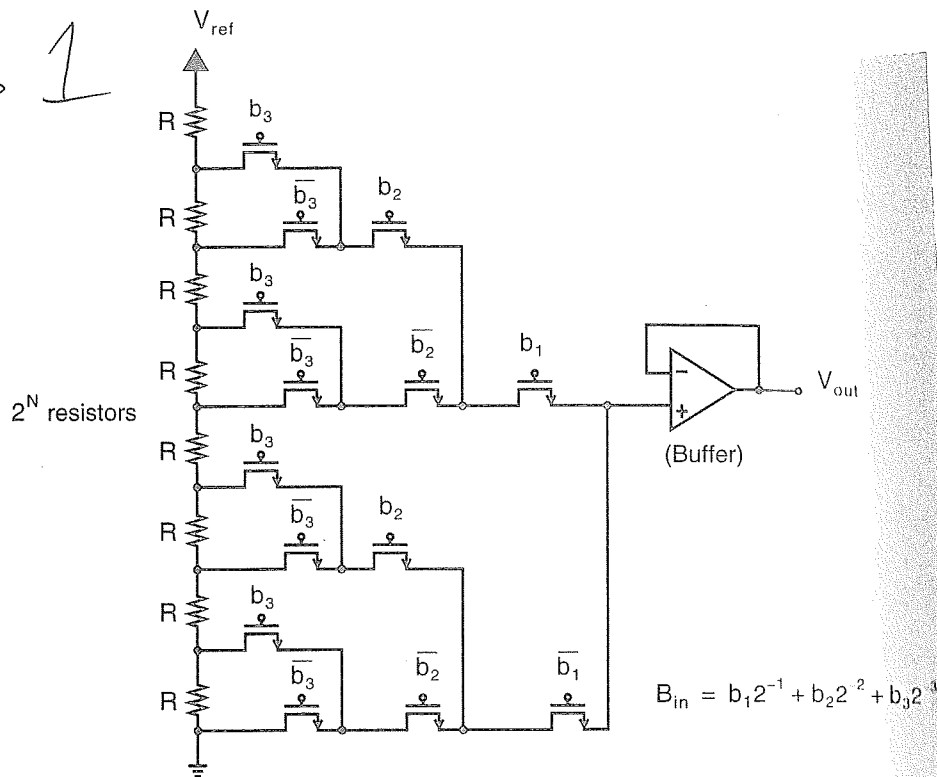


digital input code

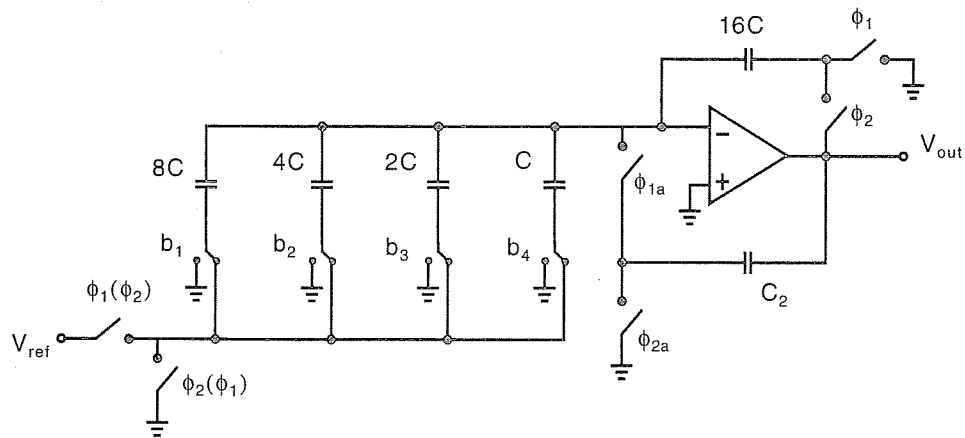
differential



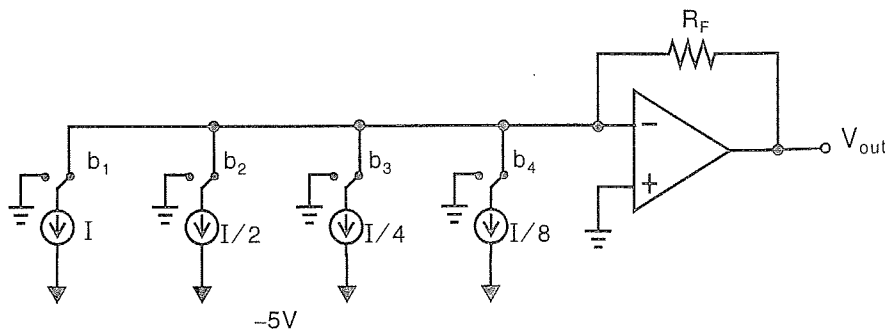
# DACs 1



**Fig. 12.1** Resistor-string 3-bit D/A converter with a transmission-gate, tree-like decoder.



**Fig. 12.12** Binary-array charge-redistribution D/A converter.



**Fig. 12.13** Binary-weighted current-mode D/A converter.

ADCs 1

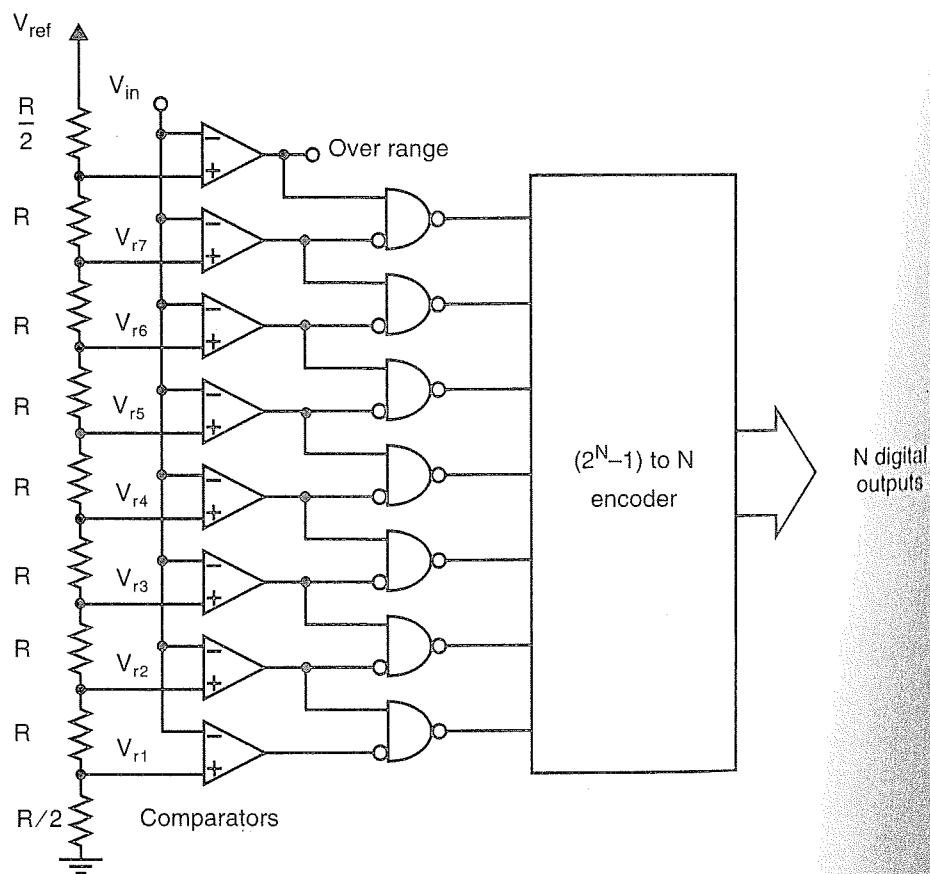


Fig. 13.16 A 3-bit flash A/D converter.

DACs 2

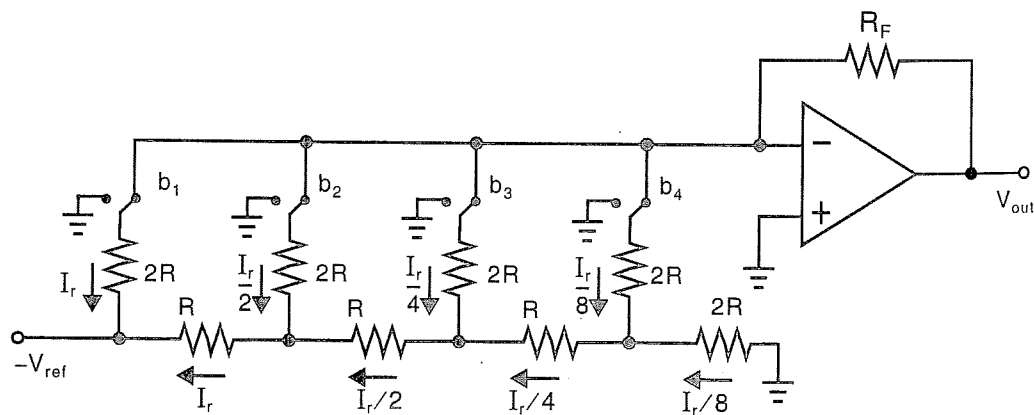
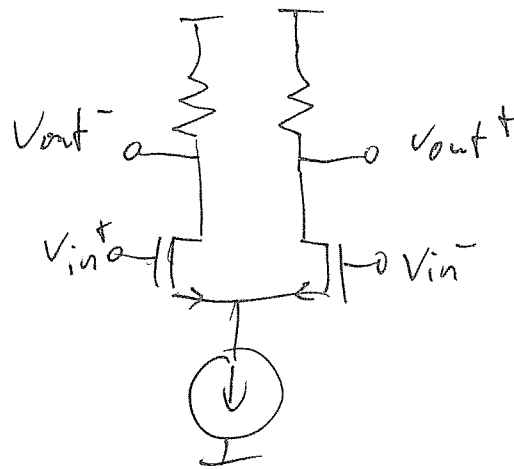


Fig. 12.10 4-bit R-2R based D/A converter.

# Comparator



Preamplifier

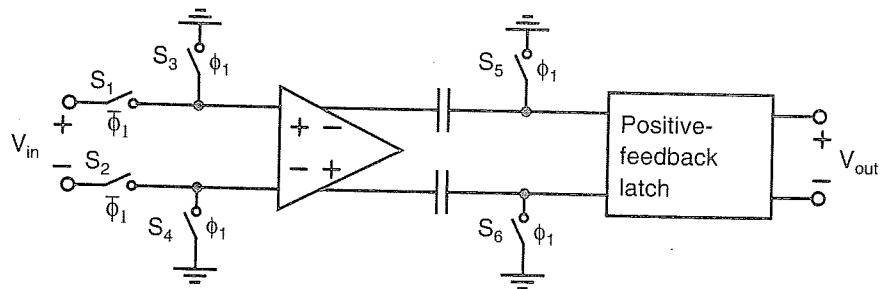


Fig. 7.20 A simplified schematic of the comparator described in [Razavi, 1992].

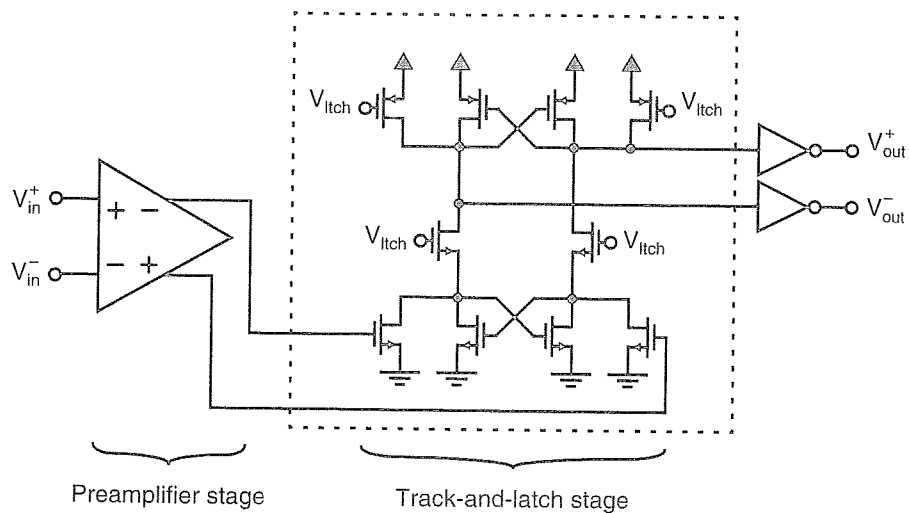


Fig. 7.13 A typical architecture for a high-speed comparator.

AOCs 2

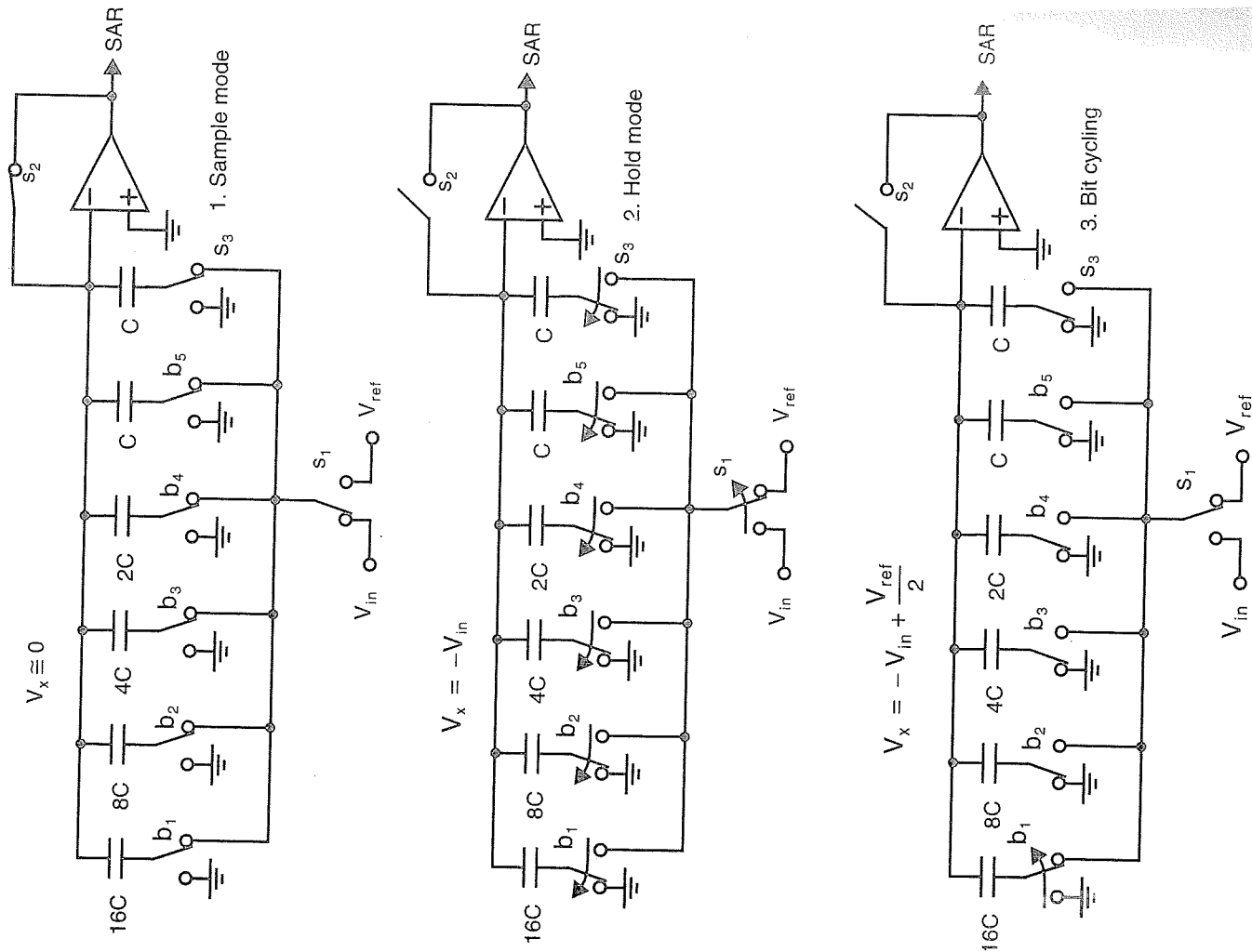


Fig. 13.7 A 5-bit unipolar charge-redistribution A/D converter.

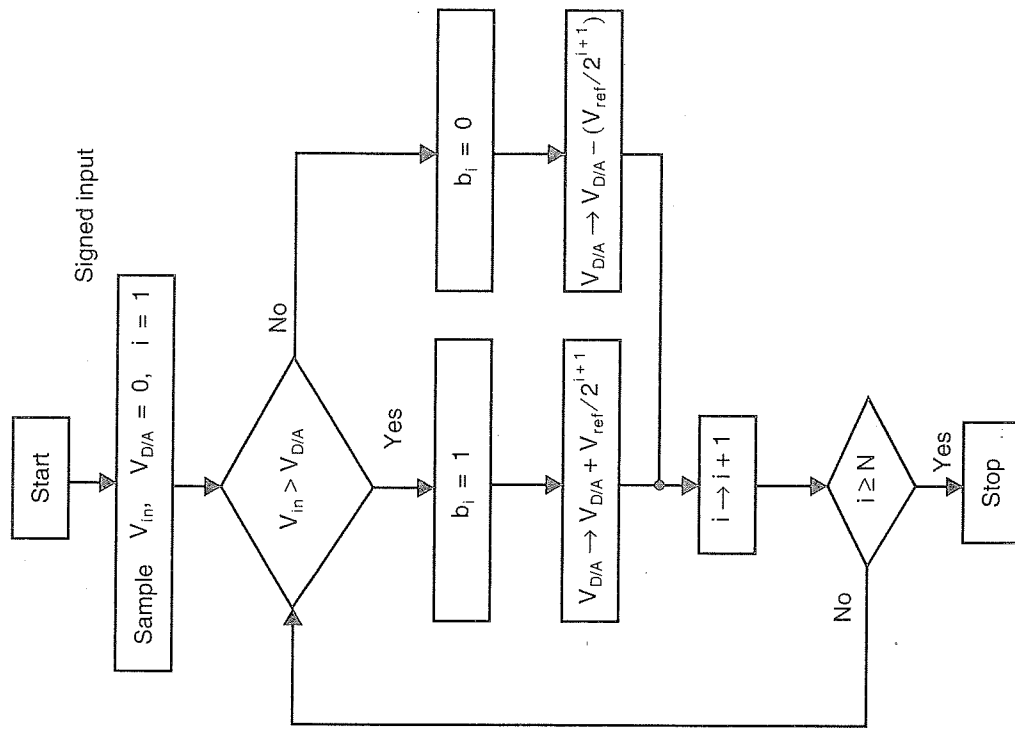


Fig. 13.4 Flow graph for the successive-approximation approach.

[illegible]

The diagram shows a two-stage CMOS operational amplifier. The first stage, labeled 'Cmp', has two inputs:  $V_{i-1}$  and  $b_i$ . Its output is connected to the input of the second stage, labeled '2'. The second stage also receives a feedback signal from its output  $V_i$  through a summing junction (indicated by a circle with a plus sign). The summing junction also receives a signal from the first stage. The output of the second stage is  $V_i$ .

```
graph TD
    Start([Start]) --> Init[Sample V = V_in, i = 1]
    Init --> Dec1{V > 0}
    Dec1 -- Yes --> Set1[b_i = 1]
    Set1 --> Calc1["V → 2(V - V_ref/4)"]
    Dec1 -- No --> Set0[b_i = 0]
    Set0 --> Calc2["V → 2(V + V_ref/4)"]
    Calc1 --> Inc1[i → i + 1]
    Calc2 --> Inc1
    Inc1 --> Dec2{i > N}
    Dec2 -- Yes --> Stop([Stop])
    Dec2 -- No --> Dec1
```

The flowchart illustrates the SAR algorithm for a signed input. It begins with a 'Start' block, followed by an initialization step: 'Sample  $V = V_{in}$ ,  $i = 1$ '. A decision diamond asks if  $V > 0$ . If 'Yes', it sets  $b_i = 1$  and calculates  $V \rightarrow 2(V - V_{ref}/4)$ . If 'No', it sets  $b_i = 0$  and calculates  $V \rightarrow 2(V + V_{ref}/4)$ . Both paths lead to an increment step:  $i \rightarrow i + 1$ . A second decision diamond asks if  $i > N$ . If 'Yes', it reaches the 'Stop' block. If 'No', it loops back to the  $V > 0$  decision.

The diagram shows a feedback loop starting from an input  $V_{in}$  which is connected to the non-inverting input of a 'Gain amp'. The Gain amp has two internal blocks: a multiplier 'X2' and a switch 'S/H'. The output of the Gain amp is connected to the inverting input of a 'Cmp' (comparator). The comparator's output is connected to a 'Shift register', which has a feedback path to the 'S/H' block in the Gain amp. Additionally, the comparator's output is connected to a switch that selects between  $V_{ref}/4$  and  $-V_{ref}/4$ , which are then fed into the summing junction (+) of the Gain amp.

Fig. 13.14 Algorithmic converter.