Homework 4 EE 338L Due 4/5/07

Design a single stage opamp to the specs shown below
Settles a 1V step to 99.99% accuracy in 50ns
Cin=1pF, Cfb=3pF, Cl=1pF
Input at 1.5V+-0.1V
Output at 0.5V to 2.5V where VDD=3V
Input referred noise density better than 12nV/sqrt(Hz)

Calculate W/L and Id for every device in the circuit.
Calculate the unity gain bandwidth and the phase margin.

Handcalculation model as derived before:
.model pfet pmos level=1 vto=-.9 kp=60e-6 lambda=0.003
.model nfet nmos level=1 vto=.7 kp=150e-6 lambda=0.002

Draw up the bias circuit for the opamp starting with a 10uA current source.