EE338L Homework 5 Live 4/26
Design a two stage opamp to the same specs as shown in homework 4.
Settles a 1V step to 99.99% accuracy in 50ns
Cin=1pF, Cfb=3pF, Cl=1pF
Input range 1.5V+/-0.1V
Output range 0.5V-2.5V with Vdd=3V
Input referred noise density lower than 12nV/rtHz
Calculate the Id and W/L for every device in the circuit.

EE338L Lab4

Due 5/3

Enter your circuit design for HW4 in cadence and demonstrate that you meet the specs. Use the testbenches developed in lab 3.

If you had trouble with the design, use the design shown on the website.

EE338L Lab5

Due 5/3

Enter your circuit design for HW5 in cadence and demonstrate that you meet the specs. Use the testbenches developed in lab 3.

If you had trouble with the design, use the design shown on the website.\*\*

\* available by 4/12