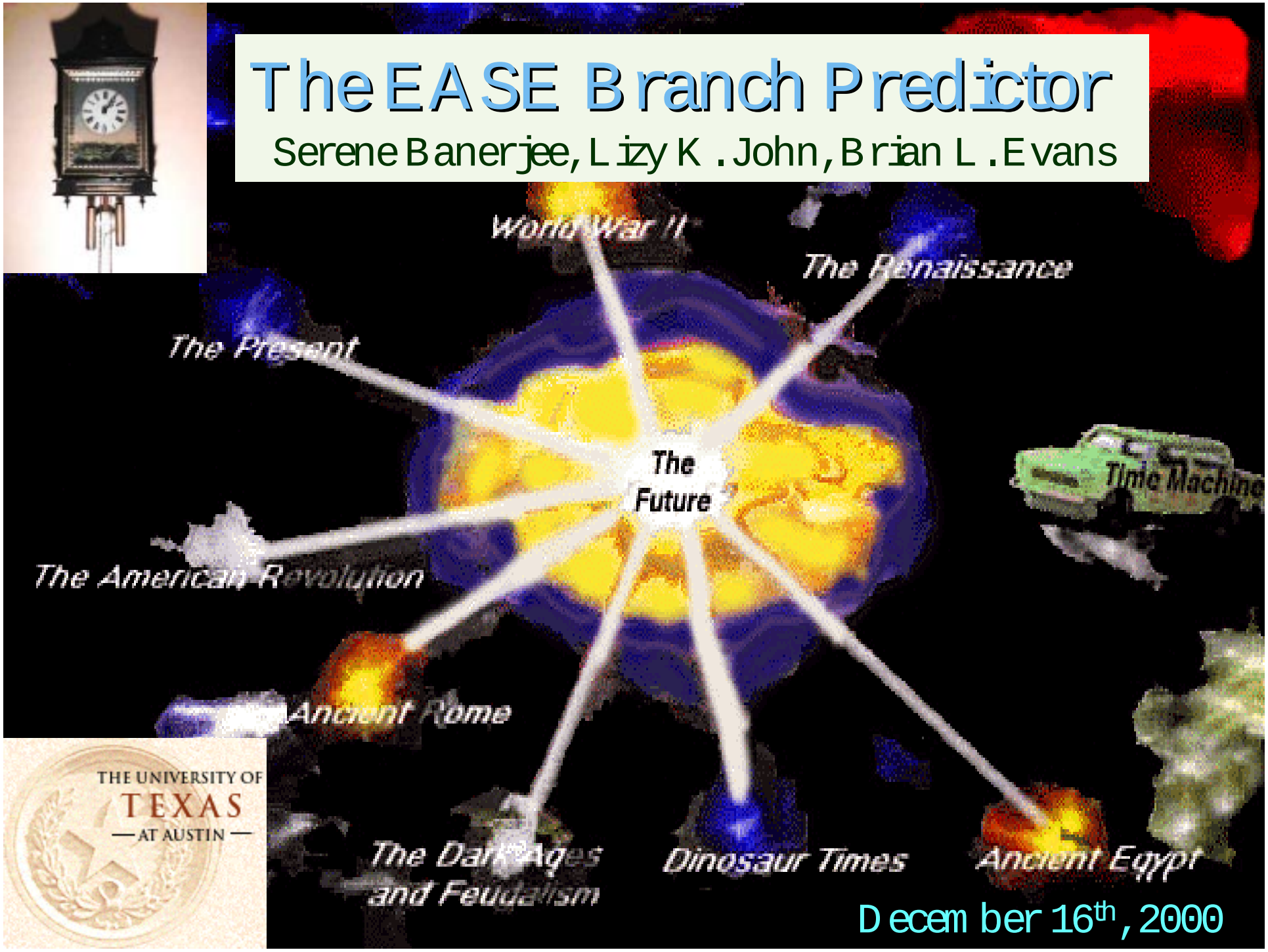
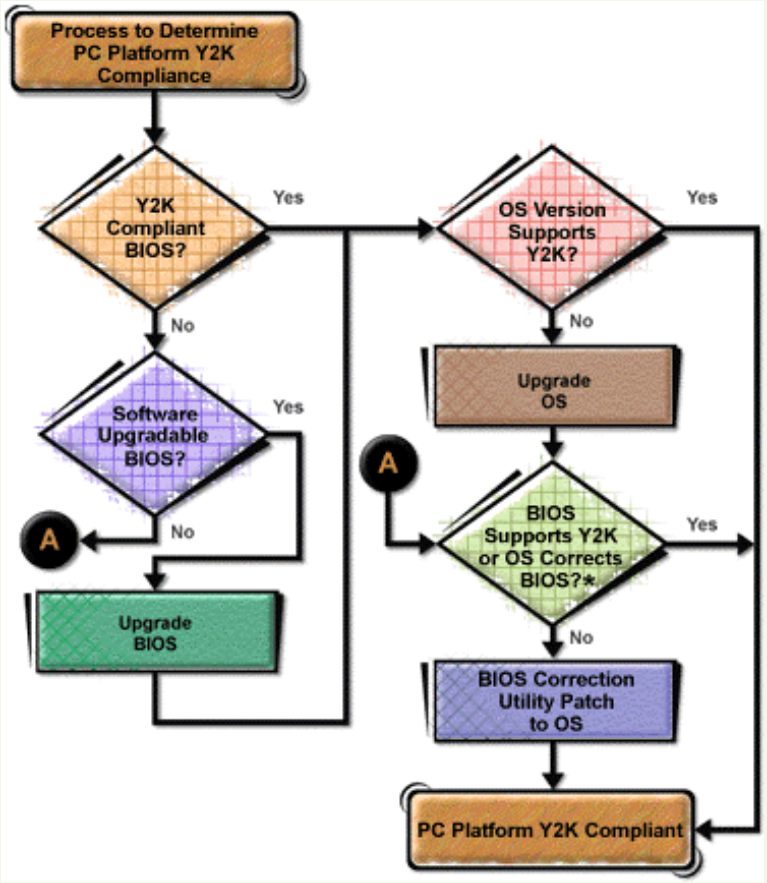
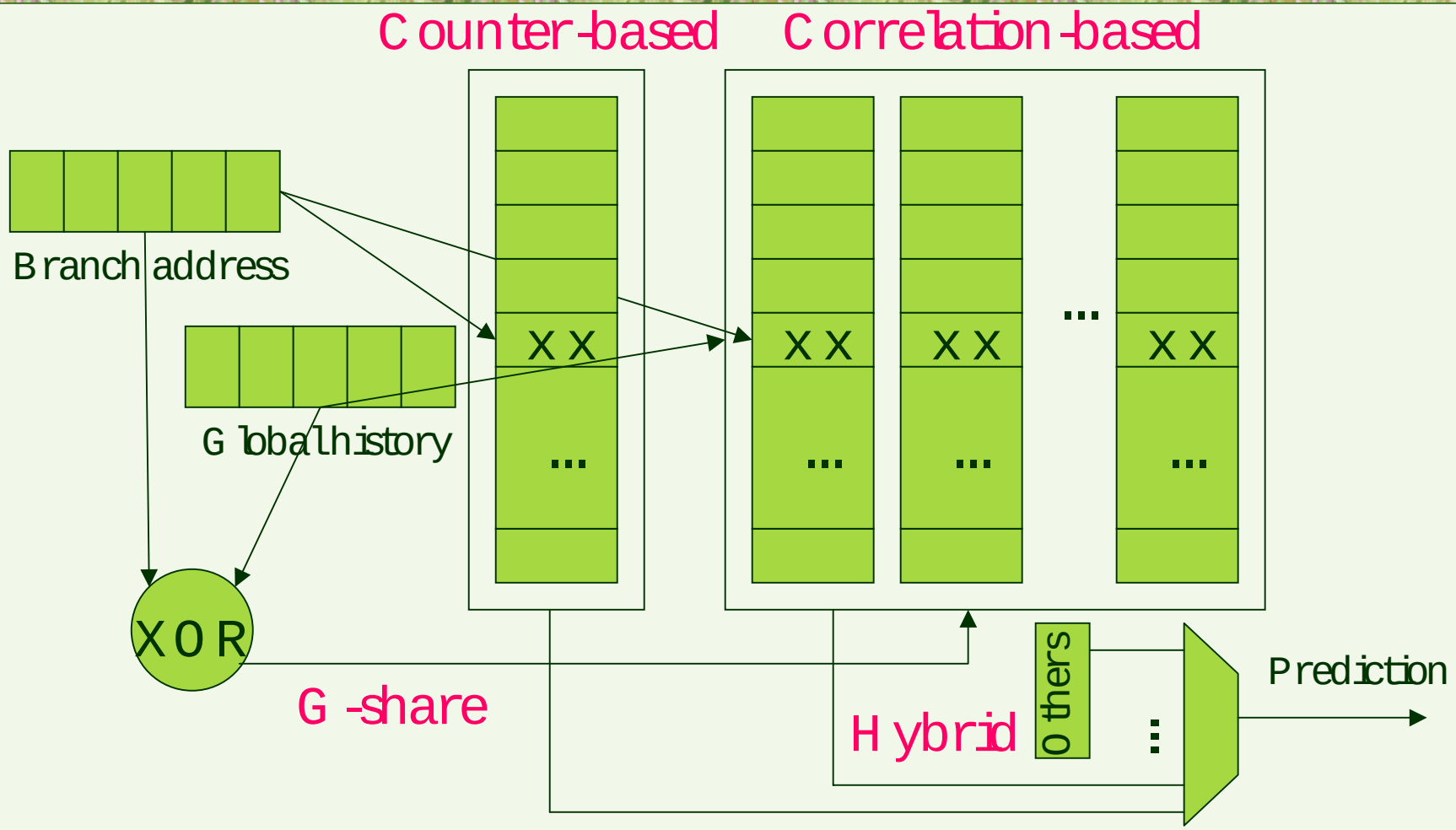

The EASE Branch Predictor
Serene Banerjee, Lizy K. John, Brian L. Evans
World War II
The Renaissance
The Present
The Future
Time Machine
The American Revolution
Ancient Rome
The Dark Ages and Feudalism
Dinosaur Times
Ancient Egypt
THE UNIVERSITY OF TEXAS AT AUSTIN
December 16th, 2000

Motivation

- Superscalar processor
  - 10-12 pipeline stages
  - 64-way issue
- Instructions repeat
- Increase performance
  - Predict branch occurrence
  - Predict branch address
- Missed speculations decrease throughput



Branch Predictors

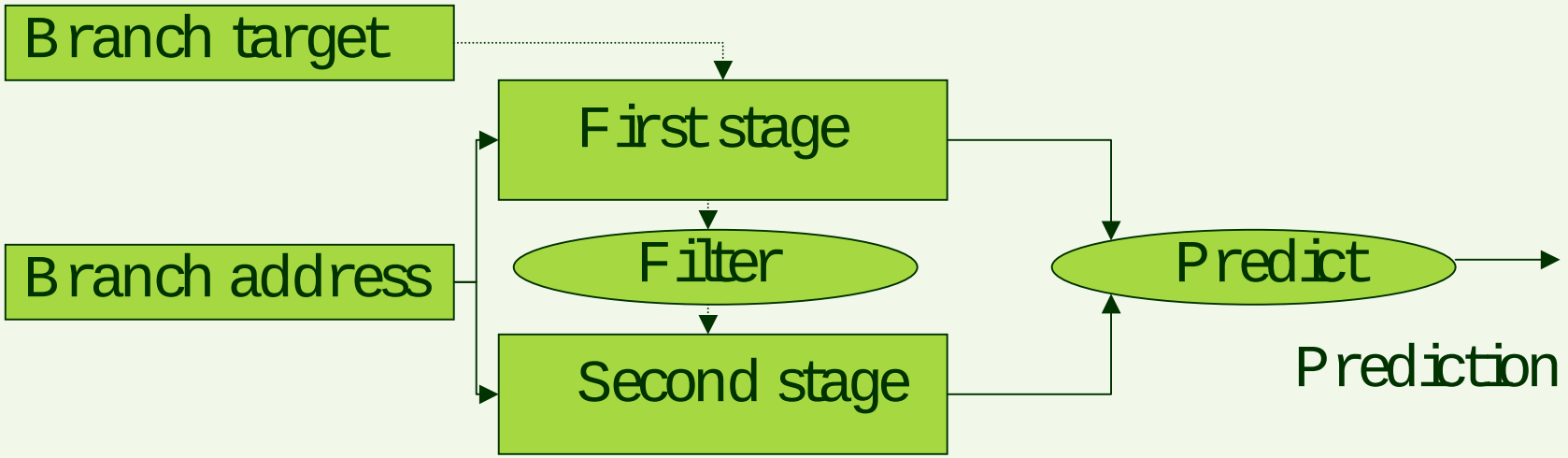


Branch Predictors

- Counter-based [Madeswaran, Mathialagan, 1990]
  - Table of counters indexed with instruction address
  - One-level predictor
- Correlation-based [Yeh, Patt, 1991]
  - Table of counters indexed with instruction address and global counter storing branch prediction history
  - Two-level predictor
- G-share [McFarling, 1993]
  - XOR address and history to randomize prediction

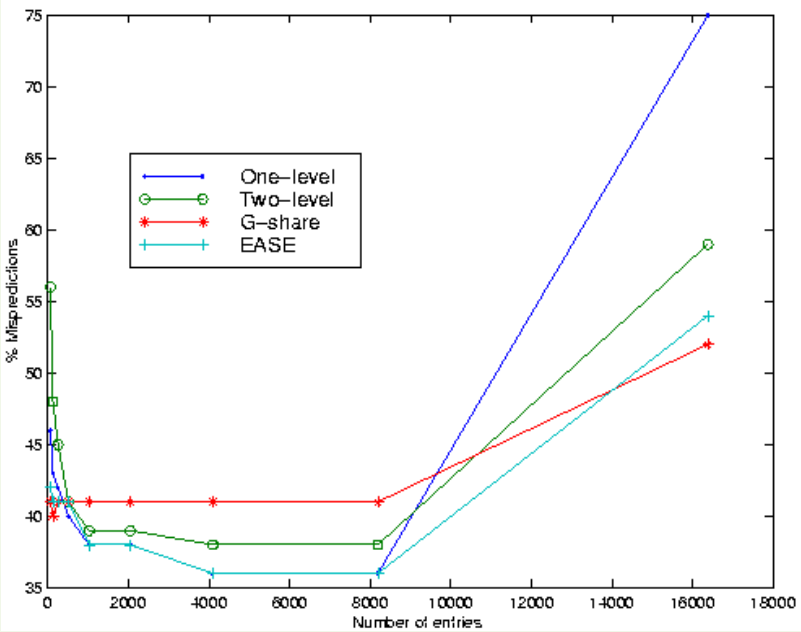
Hybrid Predictors

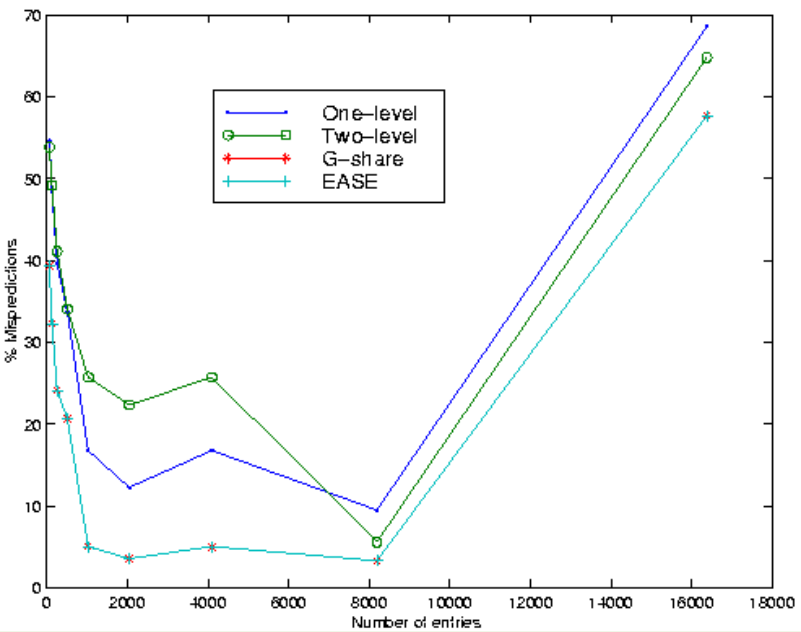
- Cascaded predictor [Driesen, Holzle; 1998]
  - Filter rule: Add new entry if first stage is incorrect
  - Predict rule: Use second stage if there is no table miss
- Performance-dependent switching [Patil, Emer; 1999]



Branch Predictor Results

- 100 instructions program : one-level is better
- 10,000 instructions program : G-share is better



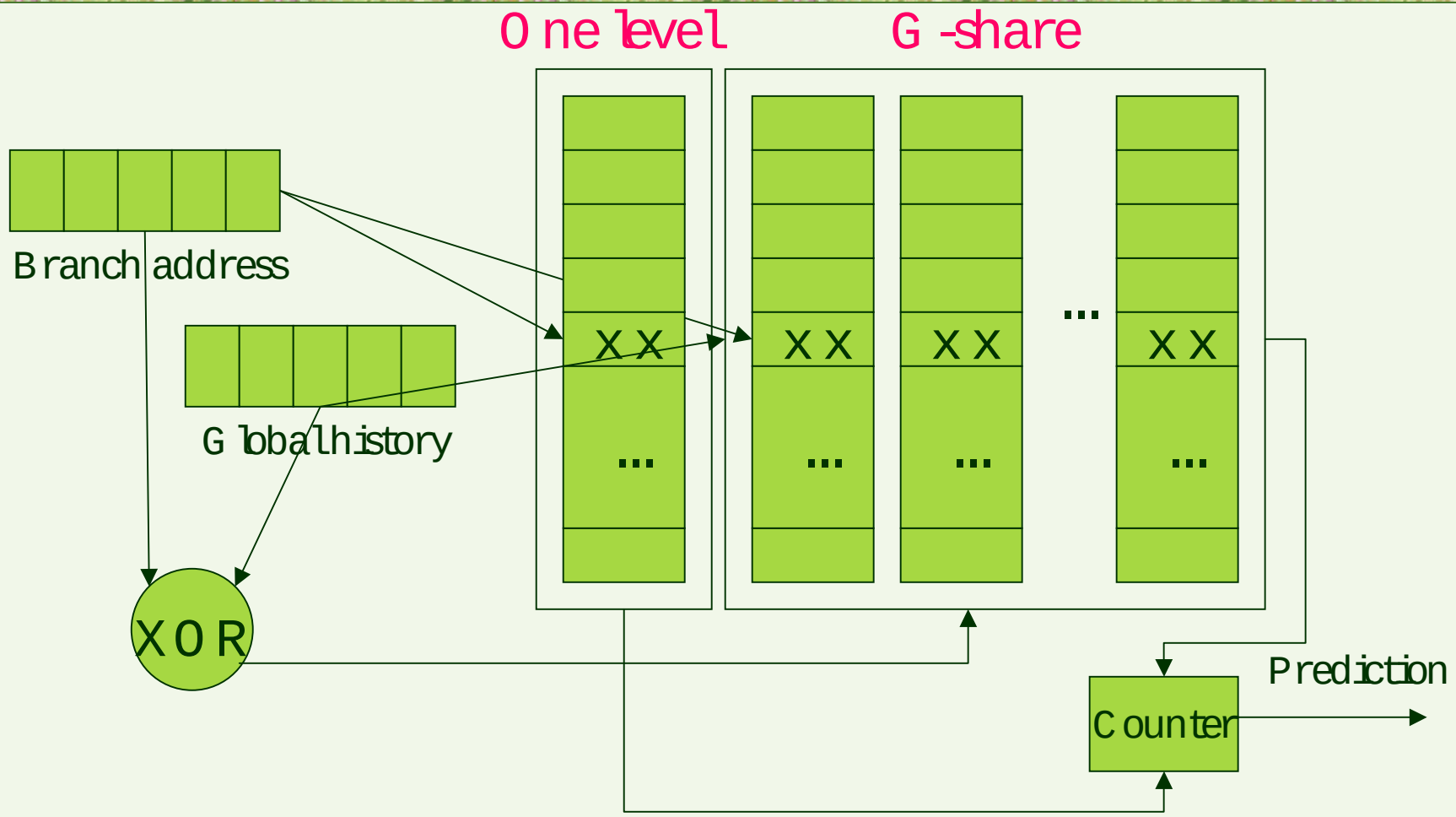


EASE Predictor

- G-share has more cold start misses than one-level
- Embed smaller one-level predictor into G-share
- Switch permanently to G-share after certain time

G-share predictor	One-level predictor
64 entries	16 entries
128 entries	16 entries
256 entries	16 entries
512 entries	128 entries
1024 entries	256 entries
2048 entries	512 entries
8192 entries	512 entries

EASE Predictor

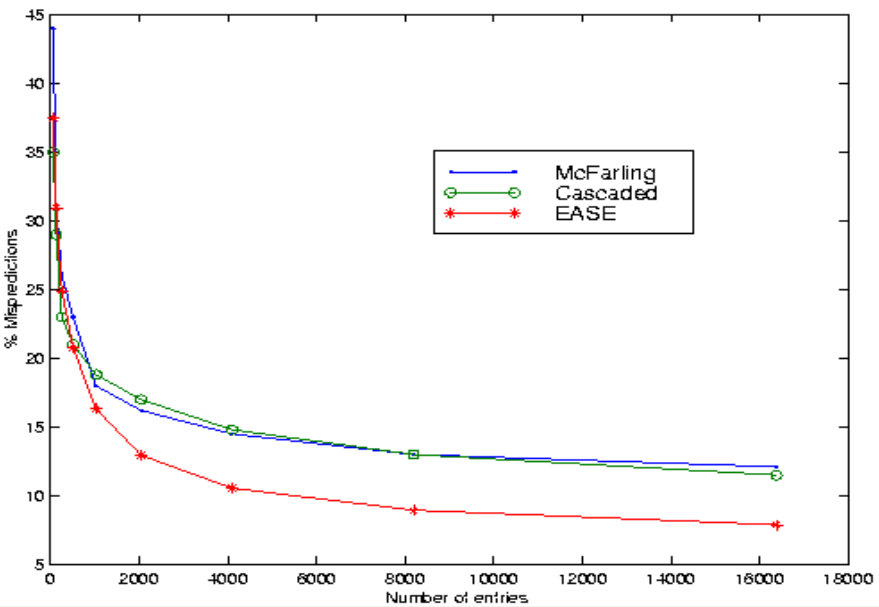


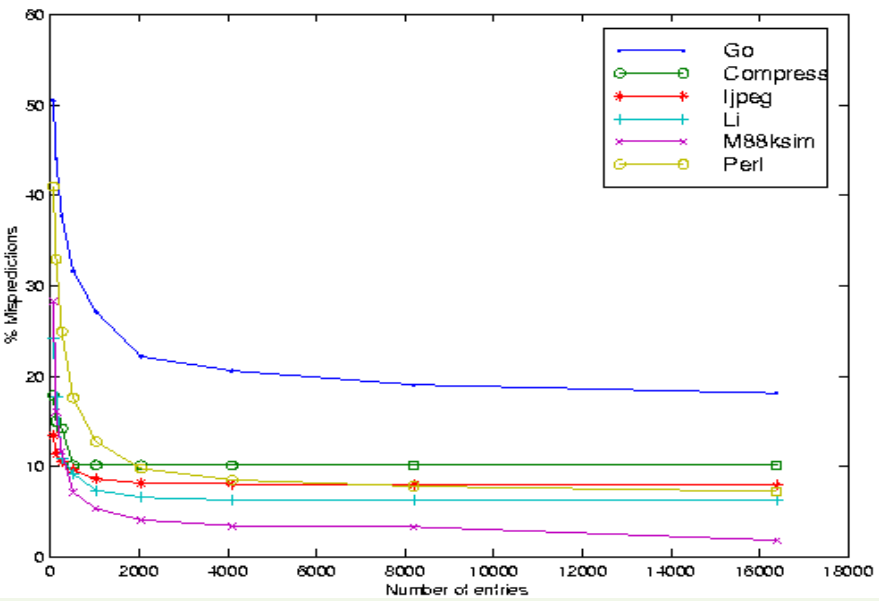
Simulations

- Shade http://www.simplescalar.org [Austin, Burger, 1997]
  - Tracer for SPARC applications
- SPEC 95 benchmarks
  - Gcc, Go, Compress, Ijpeg, Li, M88ksim, Perl
- Measuring prediction accuracy
  - Predict branch outcome and branch target address
  - If branch is predicted taken and actually taken, prediction is correct if branch target buffer matches
  - If predicted not taken and actually not taken, prediction is correct

Results

- EASE has comparable prediction results for SPEC95 benchmarks to a hybrid predictor
- EASE outperforms hybrid predictors for gcc





Conclusions

- More efficient VLSI implementation for EASE
  - Has fewer counters than one-level predictor
  - Needs no decision circuit as does hybrid predictor
- Outperforms hybrid and cascaded predictor for gcc benchmark: 8% vs. 10-14% misprediction
- Comparable results for SPEC95 benchmarks
  - Prevalent predictors: 1-14% misprediction
  - EASE predictor: 2-18% misprediction

http://www.ece.utexas.edu/~serene/software/ease