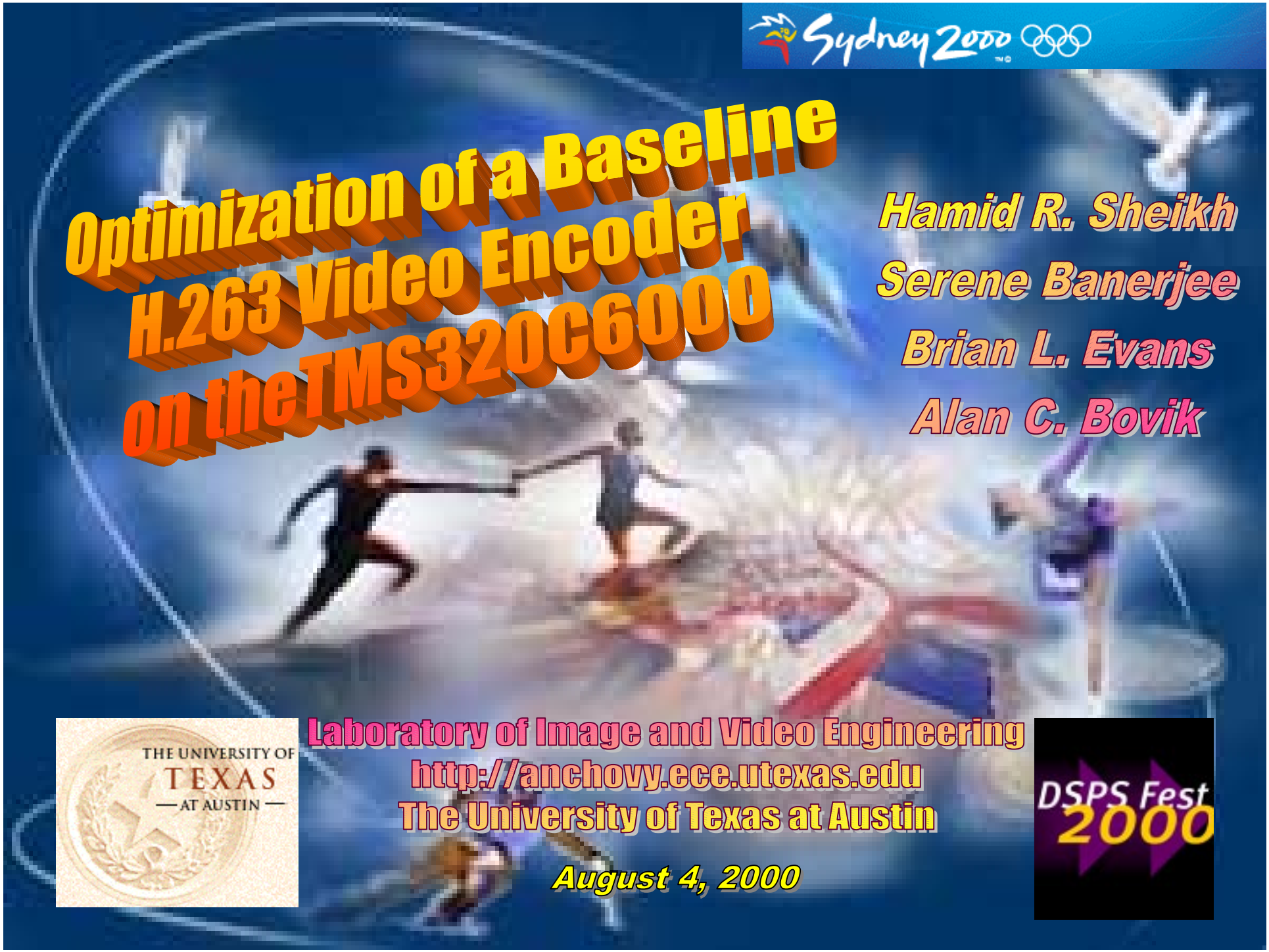
Sydney 2000
Optimization of a Baseline H.263 Video Encoder on the TMS320C6000
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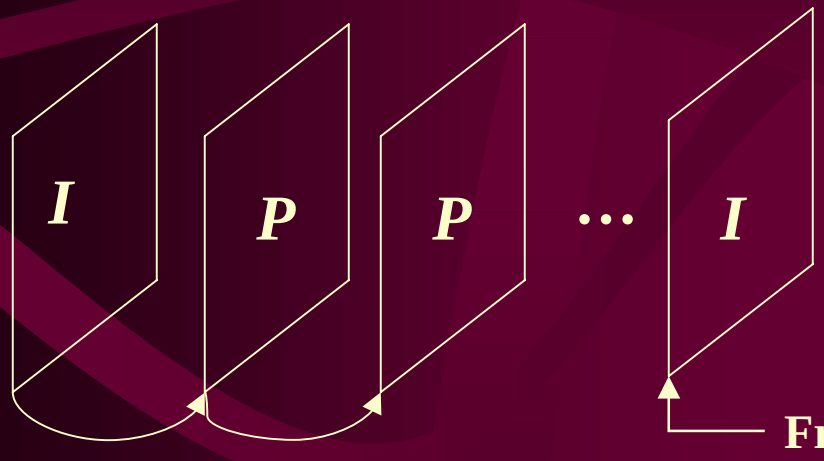
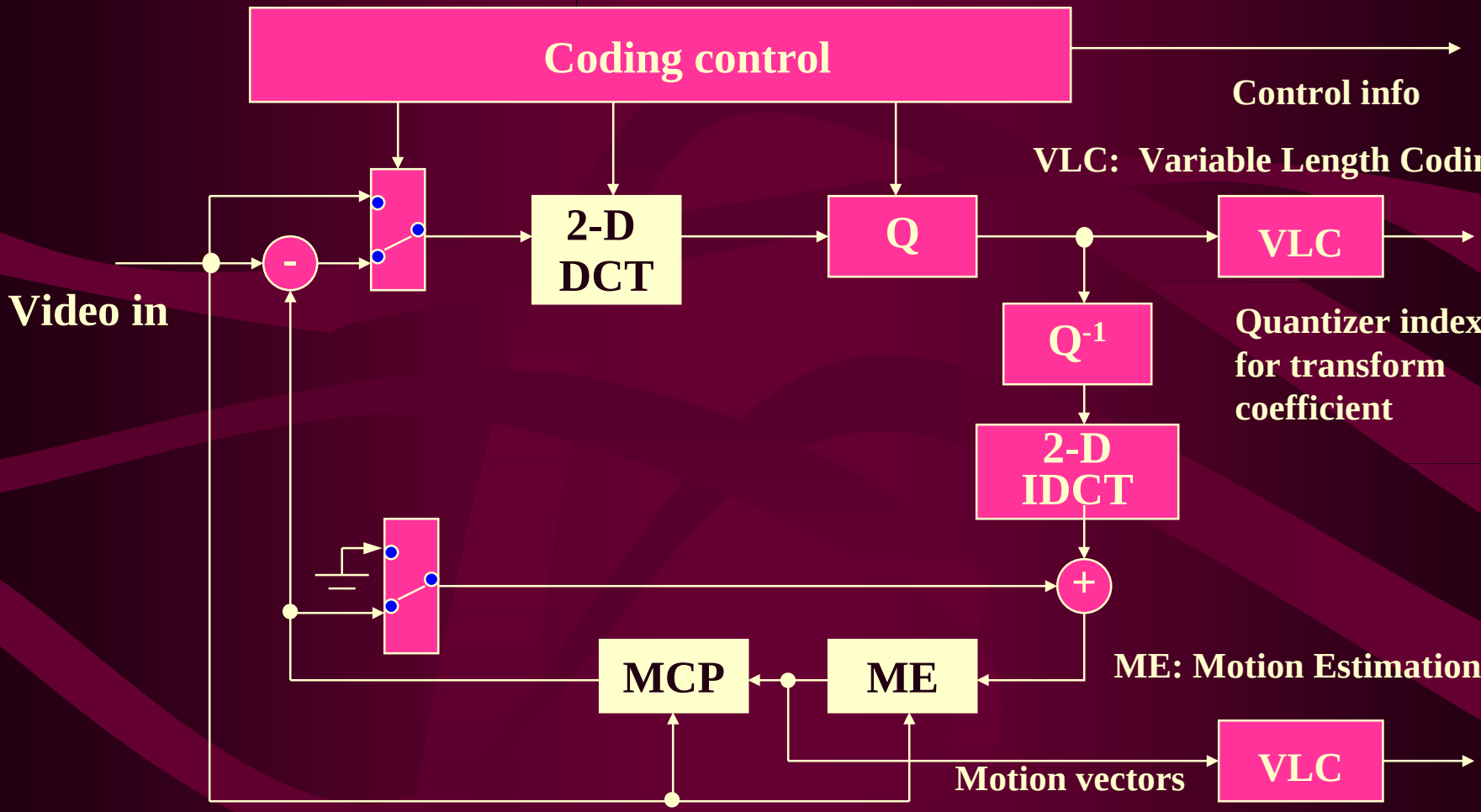
Baseline H.263 Video Encoding



I: Intra frame: ***Discrete Cosine Transform (DCT) is used to reduce spatial redundancy within a frame.***

P: Predicted frame: ***Motion compensated prediction (MCP) used to reduce temporal redundancy. DCT is used to reduce spatial redundancy in the prediction error.***

Baseline H.263 Encoder



TMS320C6000 Processor

- **Data path:** two 32-bit data paths, each having
  - Sixteen 32-bit registers
  - Four 32-bit RISC functional units (load/store architecture)
- **Instructions:** 256-bit words
  - Up to eight 32-bit instructions processed each cycle
  - 11-17 stage pipeline, depending on instruction
- **On-chip memory**
  - Separate program and data memory
  - Internal memory can act as either as cache or addressable RAM
  - Limited in size but 5x - 10x faster than external RAM
- **Clock speed:** 150 - 300 MHz

TMS320C6701 EVM

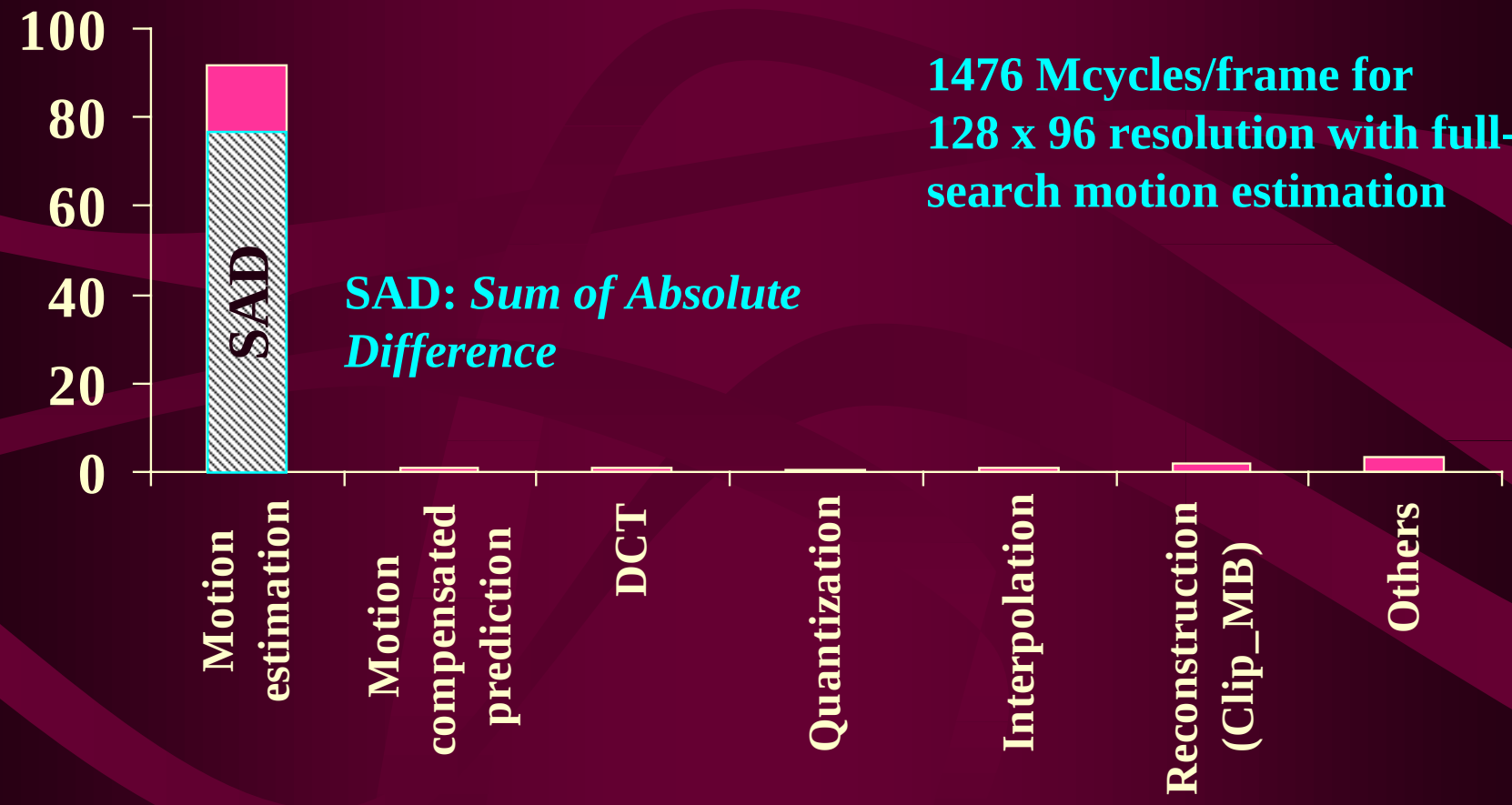
- **TMS320C6701 floating-point processor**
  - **64 kbytes of program and data memory each**
- **External memory**
  - **8 Mbytes of *100 MHz* SDRAM in two banks**
  - **256 kbytes of fast SRAM**
- **100 MHz clock speed due to SDRAM**
- **Development environment**
  - **Code Composer: interactive real-time debugging**
  - **Simulator: does not report pipeline stalls**

H.263 Encoder on C6700

- **University of British Columbia (UBC) H.263 Version 2 (H.263+) video codec**
  - **By Prof. Faouzi Kossentini's group: http://spmg.ece.ubc.ca**
  - **23000 lines (720 kbytes) of C code**
  - **Baseline H.263 and many optional H.263+ modes**
  - **Irregular use of floating-point variables and arithmetic**
  - **Primarily for research purposes**
- **Optimization goals: baseline H.263 only**
  - **Manage internal/external program and data memory**
  - **Write C-callable assembly routines and add compiler intrinsics**

Encoder Profile

(with -o2 optimization only)



SAD: *Sum of Absolute Difference*

1476 Mcycles/frame for 128 x 96 resolution with full-search motion estimation

Memory Optimizations

- **Internal program memory holds**
  - **Computationally intensive routines**
  - **Commonly used runtime support functions from TI libraries**
    - **memcpy(), memcmp() and memset()**
- **Internal data memory holds**
  - **Macroblocks and search area for motion estimation**
  - **Manually caching macroblocks for DCT, quantization, coding and reconstruction**
  - **Local data for computationally intensive routines**
  - **Stack**
- **Speedup: 29 times over -o2 optimization alone**

Code Optimization Techniques

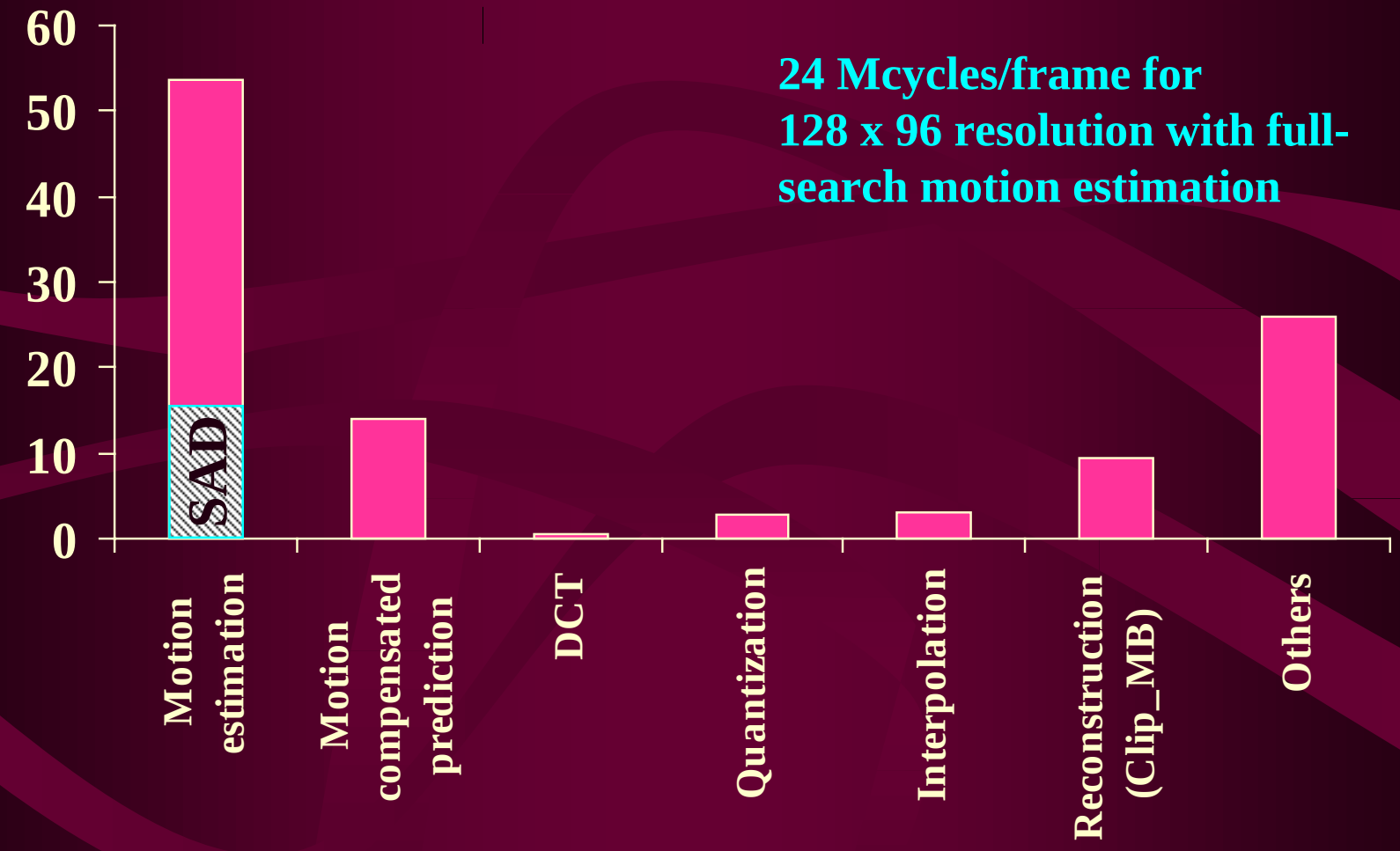
- **Compiler intrinsics gave little improvement**
- **Wrote assembly routines**
  - **Parallel assembly: SAD, Clip_MB (clips overflowing values)**
  - **Linear assembly: Interpolate, FillMBData (packed copy of pixel data into macroblock structures)**
- **Optimization techniques**
  - **Unroll loops and pipeline computations**
  - **Use packed data access to slow external RAM**
  - **Avoid pipeline stalls due to memory bank conflicts**
- **Speedup: 4 times over -o2 optimization alone**

Summary of Optimized Routines
(assembly routines only)

Name	Speedup after Memory Optimizations	Speedup after Code Optimizations	Overall Speedup
SAD	54 x	4 x	264 x
Clip_MB	7.5 x	13 x	228 x
DCT (from TI)	26 x	3 x	138 x
Interpolate	4 x	8 x	22 x
FillMBData	7 x	8 x	22 x

Encoder Profile

after all optimizations



24 Mcycles/frame for 128 x 96 resolution with full-search motion estimation

Comparisons

- **Frame resolution: 128 x 96 (Sub-QCIF)**
- **Full search motion estimation**
- **Clock speed: 100 MHz**

	-o2 optimizations only	-o2 and memory optimizations	-o2 and code optimizations only	All optimizations
Cycle counts per frame	1476 M	51 M	374 M	24 M
Frames per second	0.07	2	0.27	4.1
Speedup	-	29	4	61

Conclusions

- **Coding hints**
  - **External memory access is the key bottleneck**
  - **Perform code optimizations after memory optimizations**
  - **Best to write C code from scratch with embedded application constraints in mind and then optimize**
- **Results for baseline H.263 encoder on C6000**
  - **Computationally intensive components fit into internal program memory**
  - **Memory and hand coded optimizations result in an overall speedup of 61x**
  - **Code available at http://www.ece.utexas.edu/~sheikh/h263**

References

- **ITU Telecom Standardization Sector, "Video Coding for Low Bit Rate Communication", *Draft ITU-T Recommendation H.263 Version 2*, Sept. 1997.**
- **G. Côte, B. Erol, M. Gallant, and F. Kossentini, "H.263+: Video Coding at Low Bit Rates", *IEEE Trans on Circuits and Systems for Video Technology*, vol. 8, no. 7, pp. 849-866, Nov. 1998.**
- **B. Erol, F. Kossentini, and H. Alnuweiri, "Implementation of a Fast H.263+ Encoder/Decoder", *Proc. IEEE Asilomar Conf. on Signals, Systems & Computers*, vol. 1, pp. 462-466, 1998.**
- **TMS320C6000 CPU and Instruction Set, in *Digital Signal Processing Solutions 2000, Texas Instruments, Inc.*, http://www.ti.com, no. SPRU189E, Jan. 2000.**
- **Texas Instruments Inc. TMS320C6x Assembly Benchmarks, *http://www.ti.com/sc/docs/products/dsp/c6000/62bench.htm***
- **S. Sriram and C.-Y. Hung, "MPEG-2 Video Decoding on the TMS320C6x DSP Architecture", *Proc. IEEE Asilomar Conf. On Signals, Systems & Computers*, vol. 2. pp. 1735-1739, 1998.**