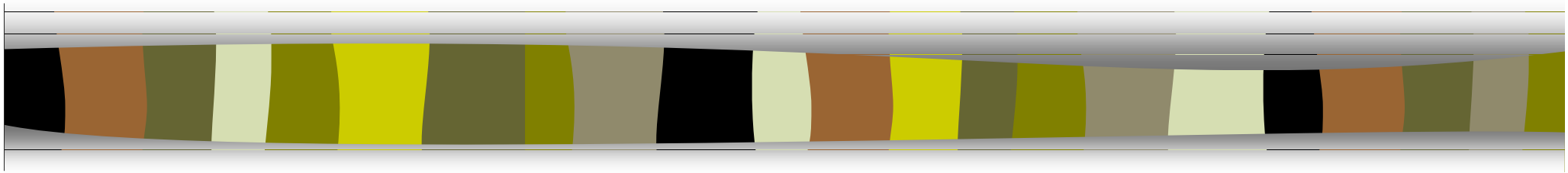
Vertical and Horizontal Beamforming Kernels with AltiVec Technology



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Real-time 3-D Digital Sonar Beamformer

- Signal processing requirements match what is possible on a commodity workstation

Computation	**4-10 GFLOPS**
Memory	**1-2 GB**
Input	**100-200 MB/s**
Output	**50-100 MB/s**

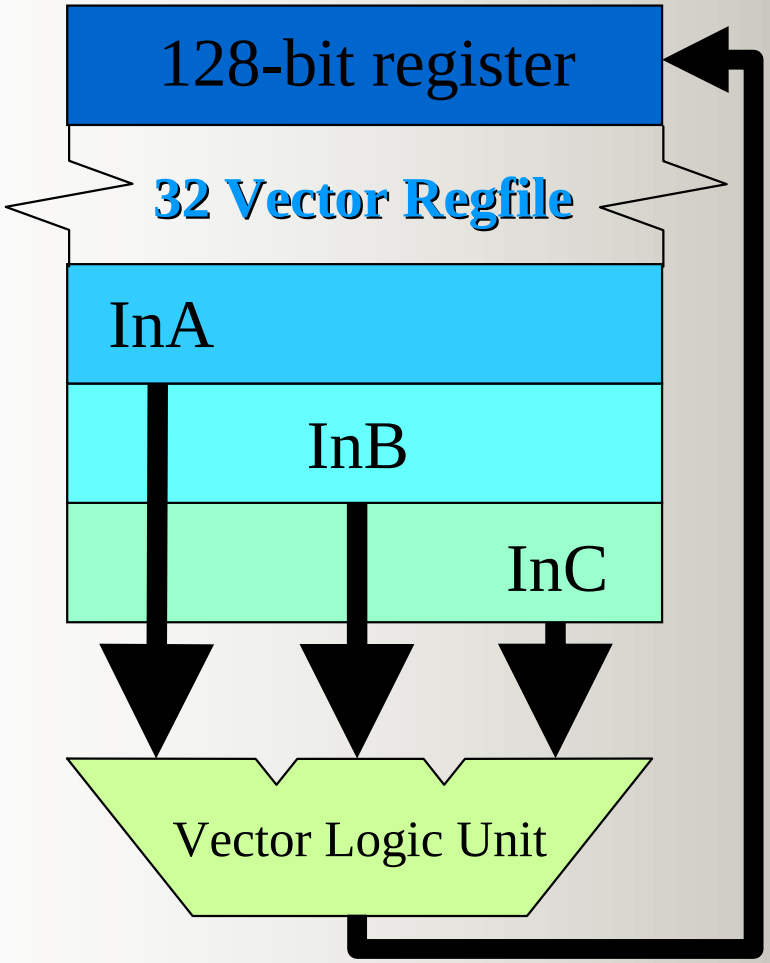
- Data acquisition through custom network interface

Beamformer Platforms

	Custom Hardware	*Embedded COTS (1990s)*	*Commodity Workstation (experimental)*
Cost/unit	**$2,000K**	**$500K**	**$100K**
Development Time	**24 months**	**12 months**	**6 months**
Size/unit (m^3)	**0.067**	**0.067**	**0.089**
Reconfigurability	**Low**	**Medium**	**High**
Software Portability	**Low**	**Medium**	**High**
Hardware Upgrades	**Low**	**Medium**	**High**

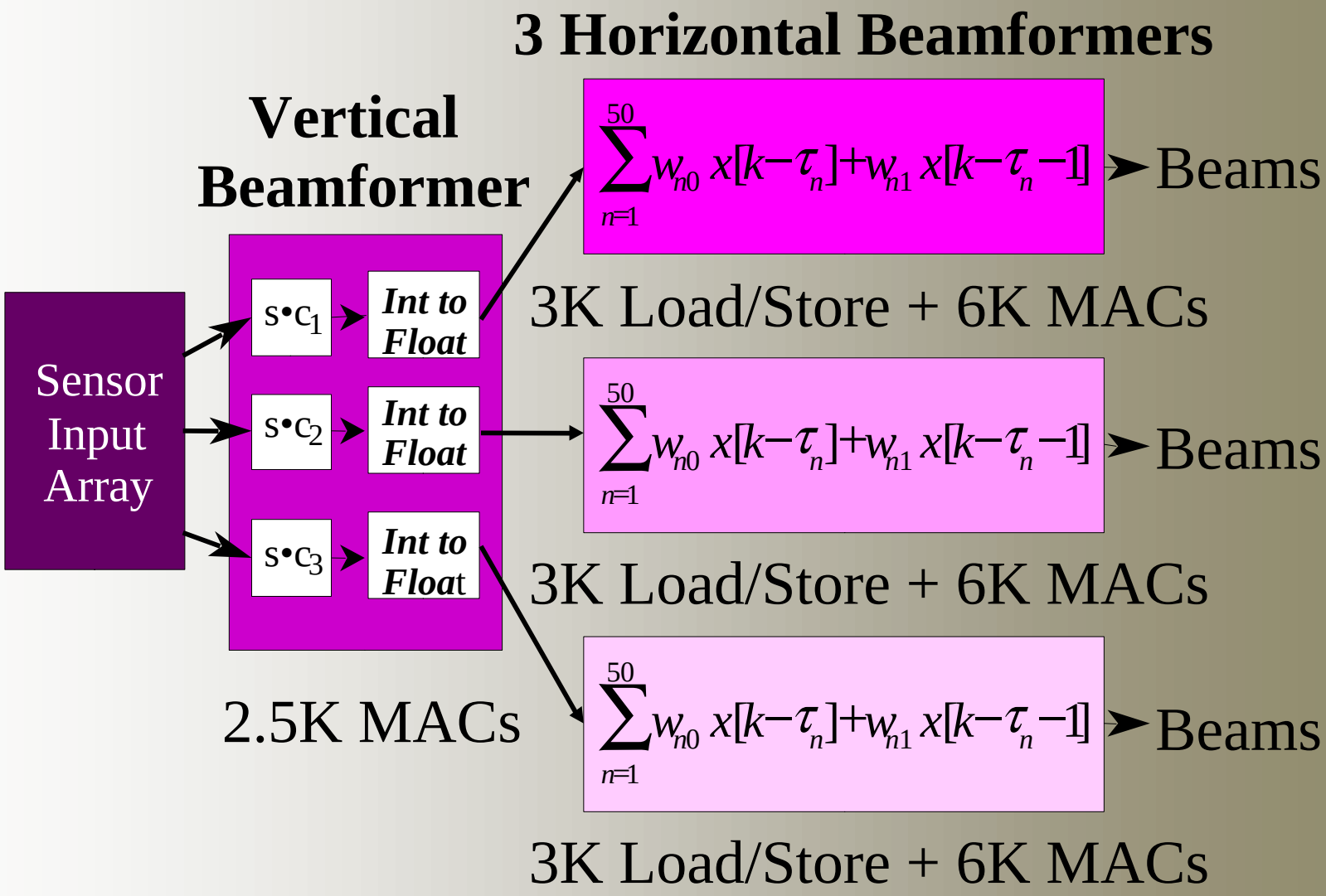
** Table extracted from G.E. Allen and B. L. Evans, "Real-Time Sonar Beamforming on Workstations Using Process Networks and POSIX Threads." IEEE Trans. On Signal Processing, vol. 48, no. 3, pp. 921-926, March 2000.*

PowerPC G4 – AltiVec Unit



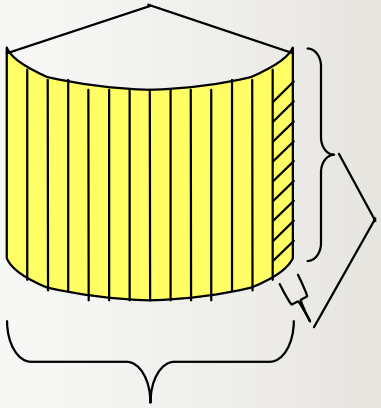
- 32 by 128-bit register file
- 400-550 MHz clock speed
- MAC ops/cyc
  - 4x32-bit FP
  - 8x16-bit INT
- Permutation Unit

3-D Sonar Beamforming



3-D Sonar Beamforming

Sensor Array Model

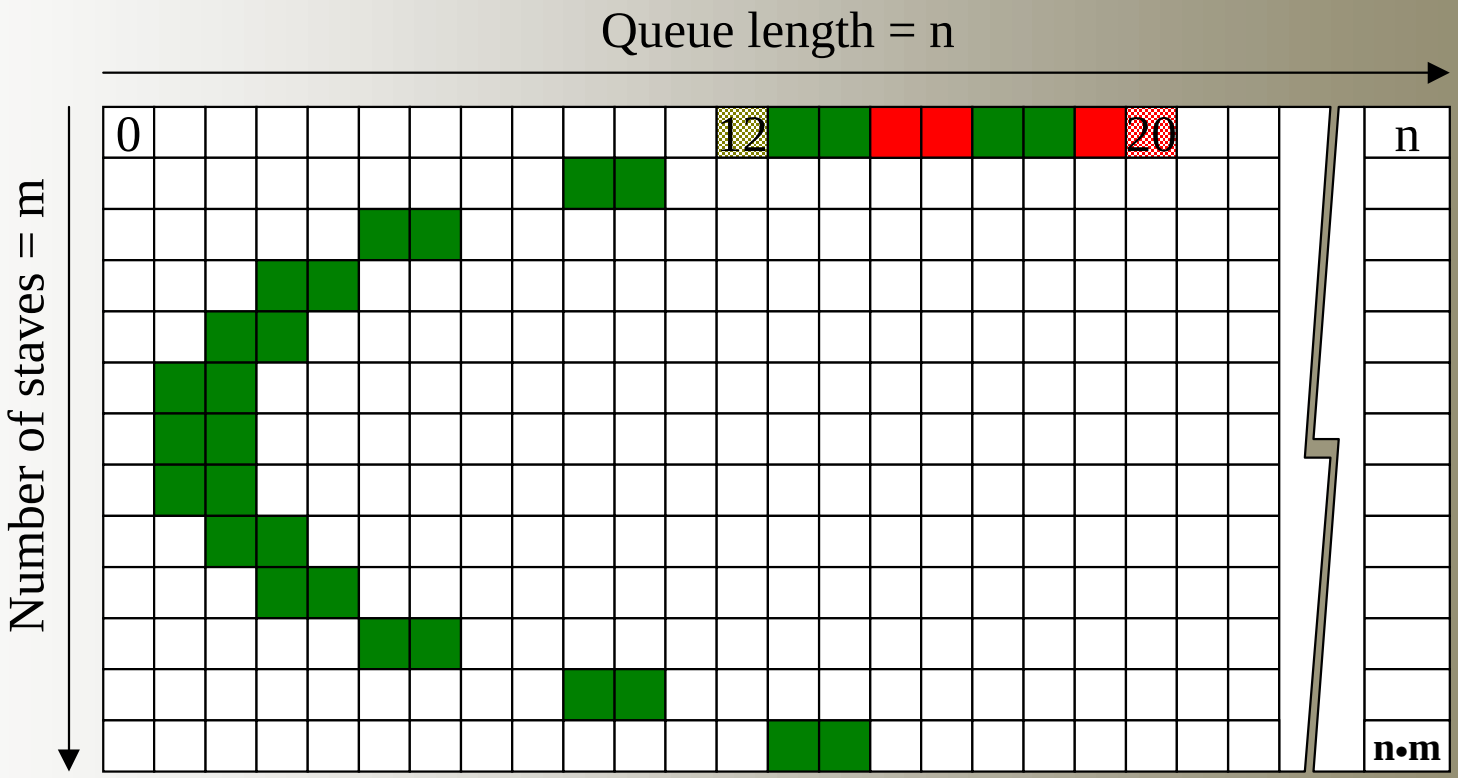


- Vertical Beamformer
  - Input from ten vertical transducers (staves)
  - Computes three dot products
- Horizontal Beamformer
  - $b[k] = \sum_{n=1}^{50} w_{n0}\, x[k - \tau_n] + w_{n1}\, x[k - \tau_n - 1]$
  - Weights w_{n0}, w_{n1} and time delay, τ_n

Vertical Beamformer

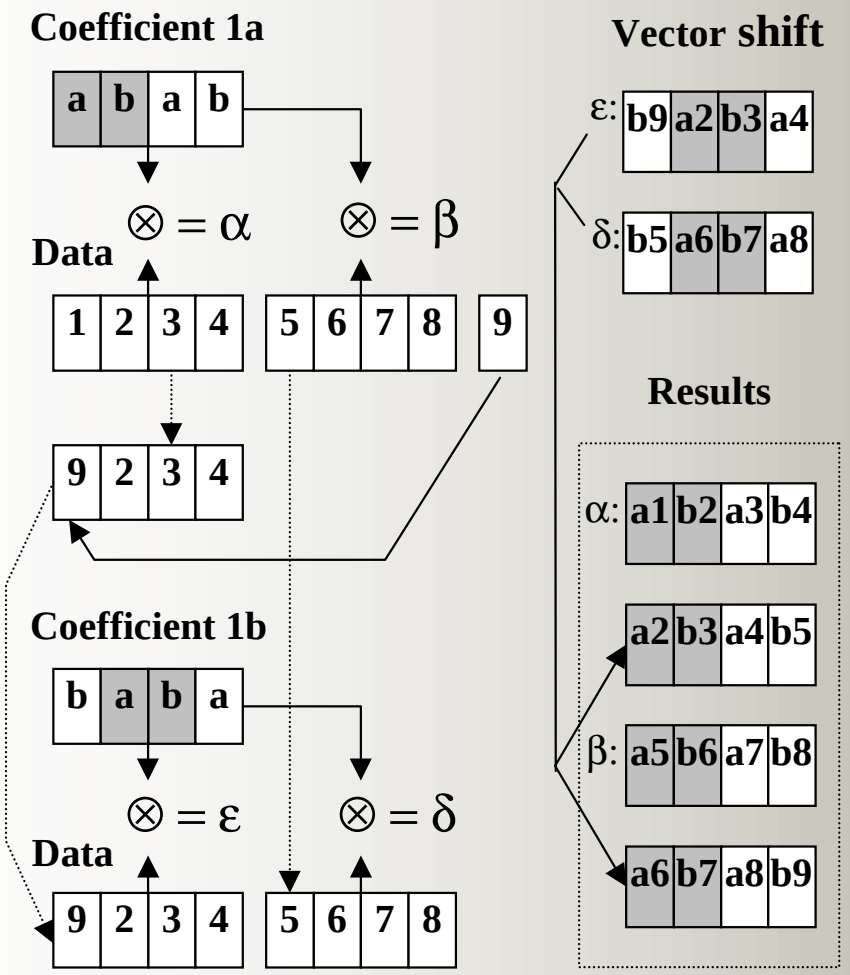
- Permute 16-bit data in a 2-D array
  - 16 byte alignment for SIMD
- Loop unrolled multiply and add
  - Eight 16-bit integer multiply and add
  - Four 32-bit integer results
  - Optimal iterations of loop unrolling
- Integer to floating-point casting
- Transpose resulting matrix
  - Corner turned for horizontal kernel

Horizontal Beamfomer



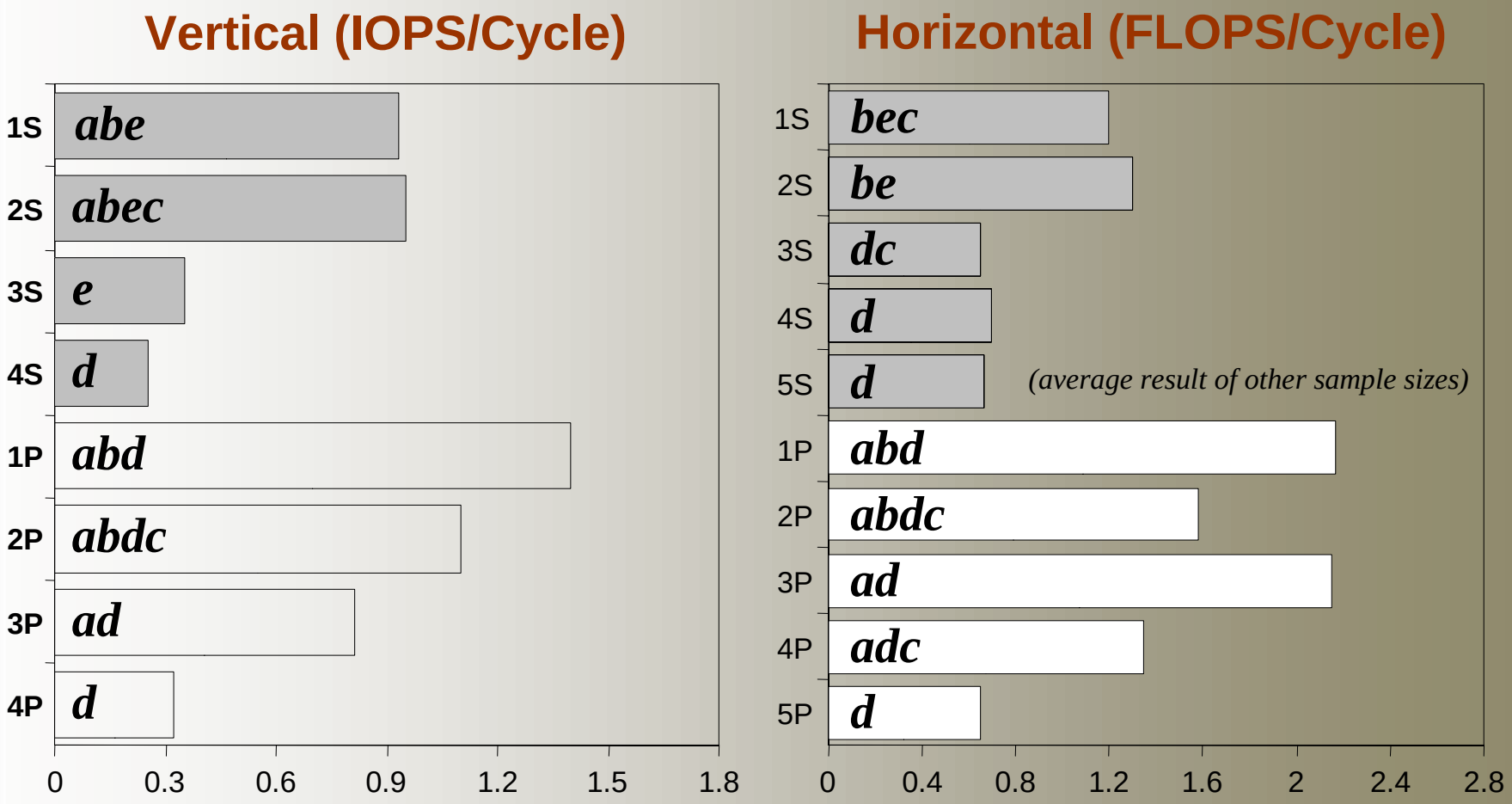
Corner turned floating-point data block

Horizontal Beamformer



- Permutation of 32-bit floating-point
  - 16 byte alignment for SIMD word
  - Minimize permutation
- Loop unrolled two-point interpolation
  - Four 32-bit floating-point multiply and add
  - Optimal iterations of loop unrolling

Performance



UltraSPARC II *PowerPC G4*

(a) NSP Enabled *(b) Data Prefetch* *(c) 64K Data Alignment* *(d) GNU C* *(e) SunCC*

Conclusion

- PowerPC AltiVec (Linux 2.1 & GCC) versus UltraSPARC VIS (Solaris 2.6 & SunCC)
  - SunCC optimization is more efficient than GCC
  - AltiVec out-performs VIS in both kernels
    - Vertical beamformer: 1.56 times faster in ops/cycle
    - Horizontal beamformer: 1.83 times faster in ops/cycle
- Current and future implementation
  - 4-GFLOP beamformer possible on five to six 450-MHz PowerPC G4 processors
  - Goal is to implement on Quad-PowerPC G4 SMP
  - Further optimization opportunities

Conclusion

- Software release plan
  - Computational Process Networks 1.0 with UltraSPARC-II sonar beamforming kernels

    `http://www.ece.utexas.edu/~allen/CPNSourceCode/`
  - Next release to include PowerPC G4 sonar beamforming kernels is planned for December 2000