A Mostly-Digital PWM-Based $\Delta\Sigma$ ADC with an Inherently Matched Multi-bit Quantizer/DAC

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***Abstract*—A mostly-digital PWM-based delta-sigma ($\Delta\Sigma$) ADC is proposed. This system takes advantage of the duration of pulses, rather than voltage or current, as the analog operand used in its closed-loop operation. Therefore, circuits that process the pulses are digital in nature and improve with scaling. Furthermore, the architecture allows inherently matched multi-bit quantizer/DAC blocks by taking advantage of delay lines reusable in both quantization and DAC operation. A second novelty of this architecture is the modualtor's adapative excess delay, that synchronizes the asynchronous loop with an external reference clock. This mitigates the problems associated with non-uniform sampling. A first order 3-bit prototype of this architecture is presented. The core occupies an area of 0.0275 mm^2 in 0.18 μm CMOS process, consumes 2.7 mW, and measures 45.1 dB SNR over a 2 MHz bandwidth.**

***Index Terms*—Analog-to-digital converter, delta-sigma modulation, time-to-digital converter, pulse-width modulation, digital-to-time converter**

I. Introduction

ANALOG-to-Digital Converters (ADCs) have undergone several architectural changes in recent years, to accommodate digital-friendly, but analog-hostile advanced CMOS process nodes. It is widely known that most analog circuit blocks that represent information in voltage (or current) suffer from scaling [1]. The performance impediments originate from a variety of sources, such as reduced supply voltages, and short-channel effects. Conventional voltage-based ADCs are therefore no exception and their performance, *e.g.* SNR, THD, and SFDR, are degraded through scaling.

In recent years, two classes of ADC architectures are explored: time-based [2] and voltage-controlled oscillator-based ADCs [3]. These architectures employ a *minimalistic analog design scheme* [4] that replaces high-accuracy or high-linearity circuits with those of adequate performance, and correct for these inaccuracies in the digital domain. This approach creates opportunities for new architectures that benefit from scaling. In time-based ADCs, analog information is represented with a time-based quantity such as pulse width. This kind of analog processing can enjoy the benefits of scaling due to the inherently higher resolution in time in state-of-the-art CMOS process nodes [2]. Similarly, VCO-based ADCs improve with scaling due to the increase in speed of its mostly digital architecture.

A time-domain ADC architecture that implements pulse-width modulator (PWM) and time-to-digital converter (TDC) in feedback loop is presented [5]. This architecture improves the linearity of PWM. However, major analog blocks (integrator and filter) are required for the noise shaping. Alternative time-domain ADC architecture uses voltage-controlled oscillator (VCO) and phase differentiator. This architecture provides inherent noise-shaping properties and can operate at low supply voltages and high sampling rates. However, VCO-based ADCs suffer from the nonlinear voltage-to-phase (V-to-P) transfer characteristics. To compensate the nonlinearity, either some form of background calibration or digital post-correciton is necessary [6], [3], or the nonlinearity needs to be tuned out [7].

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Manuscript received March 24, 2014.

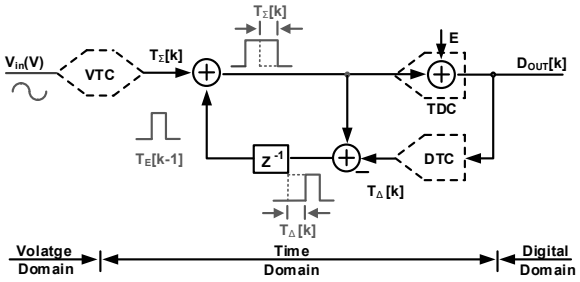

Fig. 1. $\Delta\Sigma$ modulator model showing boundaries of voltage/time/digital domain processing. VTC = voltage-to-time converter, TDC = time-to-digital converter, DTC = digital-to-time converter

In this paper, we present a mostly-digital PWM-based $\Delta\Sigma$ ADC. In this system, an input voltage is converted to pulse width and is subsequently processed in an all-digital $\Delta\Sigma$ modulator that processes pulse width. The advantages of this architecture are: (1) its matched multibit quantizer and feedback DAC through a reusable delay line structure, and (2) adaptive excess loop delay to lock to an external reference clock.

The remainder of this paper is organized as follows. The architecture of the proposed ADC is described in section II. Next the circuit implementations of the main blocks are presented in section III. Finally, measurements are presented in section IV and conclusions are drawn in section V.

II. PWM-Based $\Delta\Sigma$ Modulator Architecture

This section describes the operation principle of the proposed $\Delta\Sigma$ ADC, whose model is shown in Fig. 1. First, the concept of information encoding using pseudo-differential pulses is described. Then pulse width addition and subtraction in the time domain is introduced. Finally, the modulator topology of the proposed ADC is presented.

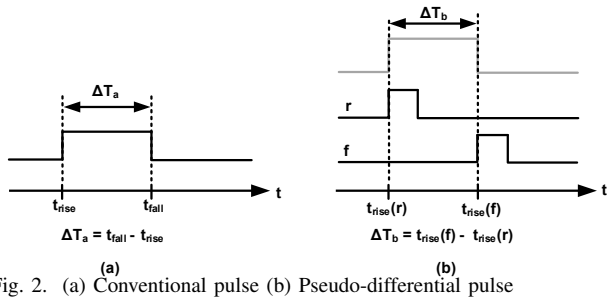

Fig. 2. (a) Conventional pulse (b) Pseudo-differential pulse

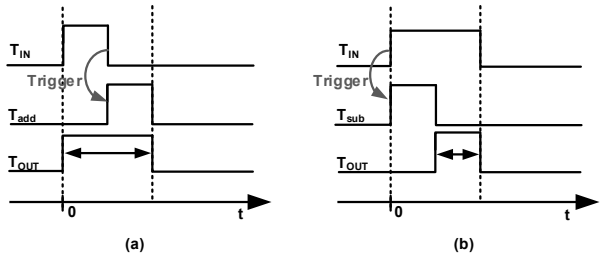

Fig. 3. (a) Addition and (b) subtraction in time-domain using pulse widths

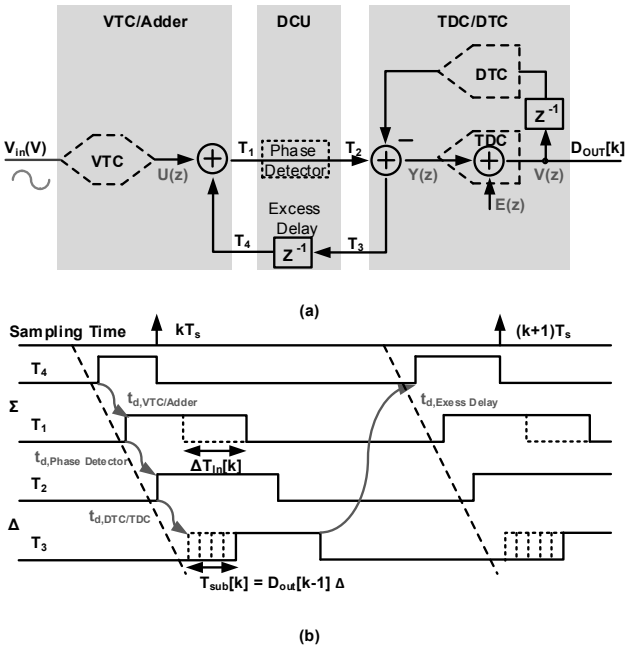

Fig. 4. (a) Architecture and (b) timing diagram of the PWM-based $\Delta\Sigma$ ADC.

A. Pulse Width Information Encoding

In the proposed ADC, analog information is encoded in the form of "pulse width." A conventional digital pulse, shown in Fig. 2(a), consists of a signal that is either low (0 V) or high (V_{DD}). The *pulse width* is defined as the duration of time in which the pulse is high. Conceptually, this definition is simple to understand, however, for both accuracy and robustness, pseudo-differential pulses are often preferred. A pseudo-differential pair of pulses (r, f) as shown in Fig. 2(b), encode pulse width in the time duration between the rise transition of r and that of f. The advantages of pseudo-differential pulses for encoding analog quantities are twofold: (1) By encoding information in the rise-to-rise delay rather than rise-to-fall delay, errors due to skewed low-to-high vs. high-to-low propagation delays are eliminated, and (2) this encoding removes the restriction on minimum pulse widths due to vanishing pulses. Every circuit in the proposed ADC operates using pseudo-differential pulses, even though some of the timing diagrams in this paper illustrate the conventional pulse (for simplicity).

B. Addition and Subtraction in the Time-Domain

Analog time-domain processing using pulse width as the analog quantity is shown in Fig. 3. To add two pulses, say T_{in} and T_{add}, as depicted in Fig. 3(a), we align the start of T_{add} to the end of T_{in}. Then the sum of the pulse widths is simply the pulse T_{out} that begins with T_{in} and ends with T_{add}. Subtraction, depicted in Fig. 3(b), requires aligning the start of T_{sub} with that of T_{in}. The result of subtraction is the pulse T_{out} which begins when T_{sub} ends, and ends when T_{in} ends. Aligning pulses in the manner described requires a triggering mechanism (and asynchronous digital circuits).

With respect to pseudo-differential pulses, it is clear how pulse widths can be added and subtracted. If two pulses are appropriately aligned, adding a pulse to another is achieved by simply delaying the f pulse of the output. Similarly, to subtract two pulses aligned with their r pulses, only the output r pulse needs to be delayed. This method of pulse arithmetic has the advantage of simple implementation using digital logic gates. It also has the complexity of dealing with the alignment of pulses. In the next section, it shall become clear that using an error feedback structure, where the order of addition and subtraction is reversed (relative to conventional first-order $\Delta\Sigma$ modulators) resolves the pulse alignment problem.

C. Modulator Topology

The proposed PWM-based $\Delta\Sigma$ ADC architecture is shown in Fig. 4(a). It comprises three major blocks: 1) VTC/Adder, 2) Delay Control Unit (DCU), and 3) Time-to-Digital Converter/Digital-to-Time Converter. The conceptual timing digram depicted in Fig. 4(b) shows conventional pulses for brevity, however, pseudo-differential pulses are used throughout the rest of this paper. The topology of the modulator is first order error feedback. The system equations are the following:

$$\begin{aligned} V(z) &= Y(z) + E(z) && (1)\\ &= \big(U(z) + z^{-1}Y(z) - z^{-1}V(z)\big) + E(z) && (2)\\ &= U(z) + E(z) - z^{-1}\left(V(z) - Y(z)\right) && (3)\\ V(z) &= U(z) + (1 - z^{-1})E(z) && (4) \end{aligned}$$

III. Circuit Implementation

This section describes the following subsystems in the proposed ADC: (1) Voltage-to-Time Converter/Adder, (2) Digital-to-Time Converter/Time-to-Digital Converter, and (3) Delay Control Unit.

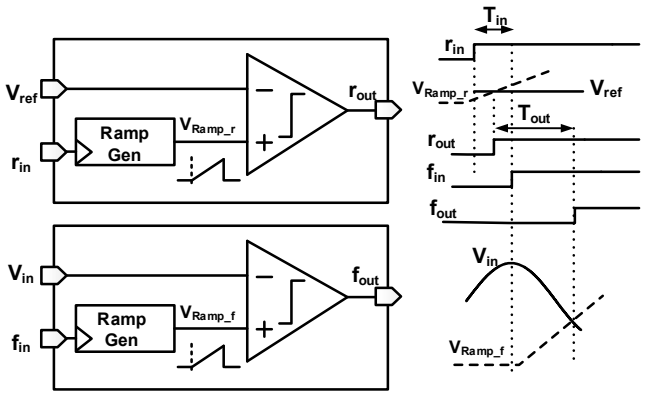

Fig. 5. Functional block diagram and timing diagram of the VTC/Adder. As shown r_{in} triggers V_{Ramp_r} which causes r_{out} to transition high when V_{Ramp_r} crosses V_{ref}. Similary, f_{in} triggers V_{Ramp_f} which causes f_{out} to transition high when V_{Ramp_f} crosses V_{in}. It is clear that $T_{out} = T_{in} + k(V_{in} - V_{ref})$ where k is the inverse slope of the ramp signal.

A. Voltage-to-Time Converter (VTC)/Adder

The addition as well as the preceding voltage-to-time conversion operation shown in Fig. 4 is performed by the VTC/Adder block. At every cycle, the VTC/Adder conceptually adds to its input pulse T_4, a pulse width proportional to $V_{in} - V_{ref}$, and T_1 results (T_4 and T_1 are the input and output pulses of the VTC/Adder, as shown in Fig. 4). Both the input and output pulses are pseudo-differential pulses (r_{in}, f_{in}) and (r_{out}, f_{out}). To implement the voltage-to-time conversion and addition, two identical half-circuits are used as shown in Fig. 5. The identical circuits have a ramp generator and a continuous-time comparator.

With the rise of r_{in}, the first ramp generator is triggered. Once its output ramp crosses the reference voltage (V_{ref}), the comparator outputs a pulse on r_{out}. Naturally, there is some delay associated with each operation ($t_{d,\mathrm{VTC/Adder}}$). Next, with the rise of f_{in}, the second ramp generator is triggered. The resulting ramp is now compared with the instantaneous value of the input voltage (V_{in}). Larger values of V_{in} result in larger delay from ramp triggering (f_{in}) to comparator output (f_{out}). This delay should be linearly proportional to V_{in} in addition to some fixed delay. Given the pseudo-differential architecture, the common-mode delay ($t_{d,\mathrm{VTC/Adder}}$) is canceled and thus the output pulse width $[t_{\mathrm{rise}}(f_{out}) - t_{\mathrm{rise}}(r_{out})]$ is the sum of input pulse width $[t_{\mathrm{rise}}(f_{in}) - t_{\mathrm{rise}}(r_{in})]$ and a pulse width proportional to $V_{in} - V_{ref}$. Note how V_{ref} sets a minimum on pulse width, which is greater than or equal to zero in this design.

The circuit topology of the VTC/Adder is shown in Fig. 6. The ramp generator consists of a wide-swing current source ($I_B = 200\mu$A), an integrating capacitance ($C_I = 110$fF), and digital switches to create a 0 to 640ps full scale $T_\Sigma[k]$ corresponding to a (0.28V-0.68V) linear range of V_{in} with V_{ref} = 0.28V. The continuous-time comparator is a PMOS-input folded-cascode differential amplifier with a buffered output stage. The fixed overall latency is 2.10 ns ($t_{d,\mathrm{VTC/Adder}}$).

The output of the VTC/Adder (T_1) passes through the phase detector block of the Delay Control Unit (T_2) without modification, except for delay $t_{d,\mathrm{Phase\ Detector}}$ applied to both rise and fall pulses. It is then processed by the DTC/TDC block described next.

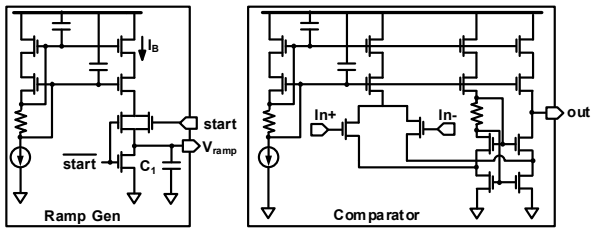

Fig. 6. VTC/Adder circuit showing ramp generator and comparator

B. Digital-to-Time/Time-to-Digital Converter

The DTC/TDC block performs the functions of both the ADC and the DAC in the first-order $\Delta\Sigma$ error feedback only structure shown in Fig. 4. Multi-bit $\Delta\Sigma$ is sensitive to mismatch between the ADC and the DAC in regular (voltage-based) ADCs. The unit delay array (with fixed time interval) is the common block both the ADC and the DAC in time-domain. If the operation of these functions can be performed sequentially, then those blocks may be shared. Thus, a reusable structure of multi-bit subtraction and quantization can save area and reduce the effects of mismatch. This novel merged ADC/DAC is possible thanks to time-domain processing, not possible in voltage-domain processing.

The DTC/TDC operates in two phases. In phase 0 (DTC), the block performs time-based subtraction by delaying the r pulse by a number of LSB time-units ($D_{out}[k-1]$ from the phase 1 output of the previous cycle). The f pulse is passed through a replica structure that has fixed delay. The resulting pseudo-differential pulse (T_3) is output to the excess delay block and also recirculates through the DTC/TDC for phase 1 (TDC phase). The same unit delay elements are used in conjunction with flip-flops and thermometer-to-binary logic that implement the time-based quantizer shown in Fig. 8. This structure resembles a flash TDC which uses (inverting) delay lines and flip-flops to quantize a pulse to a number of unit delays (LSB).

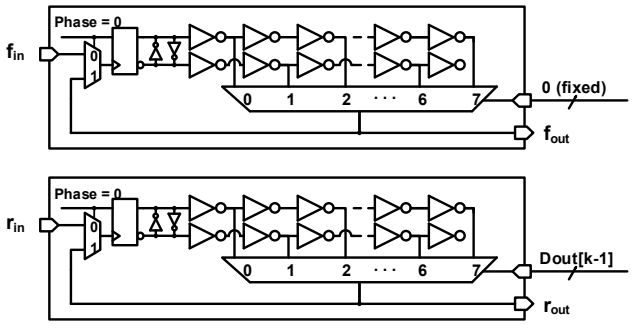

Fig. 7. Digital-to-time converter (DTC) phase (phase 0) of the DTC/TDC circuit. Output pulse is recirculated through the block a second time for the TDC operation (phase 1).

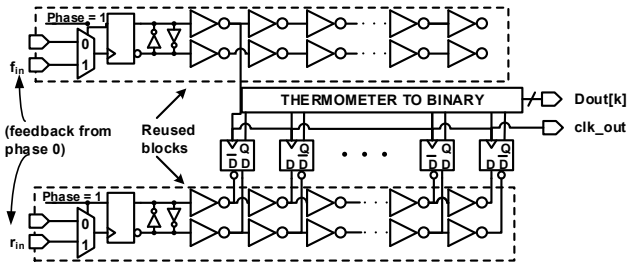

Fig. 8. Time-to-digital converter (TDC) phase (phase 1) of the DTC/TDC circuit. Note the reuse of the unit delay elements from the previous phase (DTC).

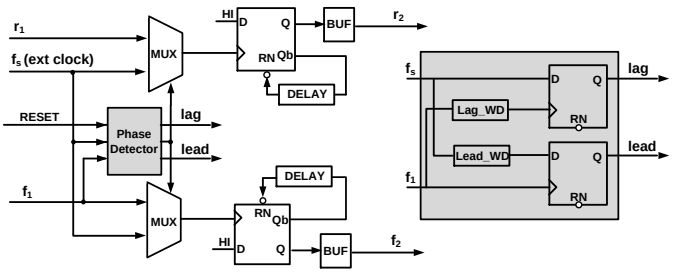

Fig. 9. Delay Control Unit, including phase detector. Intially, after reset, the external clock (f_s) is fed in the loop (as r_2 and f_2) as a zero width pulse. The phase detector signals a *lag* event if f_1 transitions high later than *Lag_WD* after the rising edge of f_s. Similarly, *lead* is signal if f_1 is more than *Lead_WD* earlier than the rise of f_s.

Both the DTC and the TDC are 3-bits in this implementation, with a unit delay (LSB) of 80 ps.

C. Delay Control Unit (DCU)

The main responsibilities of the DCU are to properly startup the loop after global reset and also prevent unwanted pulse drifts through dynamically adjusting the excess loop delay.

At each cycle, pulse addition in the VTC/Adder and pulse subtraction in the DTC, create varying loop delay. Larger input signals create a larger loop delay (and vice versa). This causes the sampling interval (equivalent to the distance between the fall of T_4 in two consecutive cycles in Fig. 4) to vary from cycle to cycle in an input dependent manner. This nonuniform sampling poses a challenge, which is remedied by the Delay Control Unit.

Since sampling in the VTC/Adder is triggered by the f pulse, for a uniform sampling period of T_s, the phase detector (shown in Fig. 9) compares the f pulses at each cycle with the rising edge of a clock with frequency $f_s = 1/T_s$. This activates either a lead or lag signal that is then applied to the excess delay block of the modulator to increase or decrease the loop delay of both r and f pulses through the excess delay block. Referring to Fig. 4, ideally in each cycle, the DCU should adjust the delay of the excess delay to ensure:

$$T_s = t_{d,\text{VTC/Adder}} + t_{d,\text{Phase Detector}} + t_{d,\text{DTC}} + t_{d,\text{Excess Delay}} \quad (5)$$

With just two bits (lead, and lag) the DCU adjusts the excess delay by ±400ps in each cycle. This is in addition to a programmable fixed delay for a wide tuning range of f_s. By using this approach, one can ensure that the average oversampling frequency is always locked to an external f_s clk which is 144 MHz in the prototype implementation (∼7 ns average loop delay). It is important to recognize that the fluctuation in the sampling time of this PWM-based ADC does create errors that are similar in nature to noise artifacts generated by noisy clocks. After releasing the global reset signal, the DCU provides an initial zero-width pseudo-differential pulse to startup the circuit. In normal mode, DCU passes through the input pulse to the output with a constant amount of delay ($t_{d,\text{Phase Detector}}$) in Fig. 4.

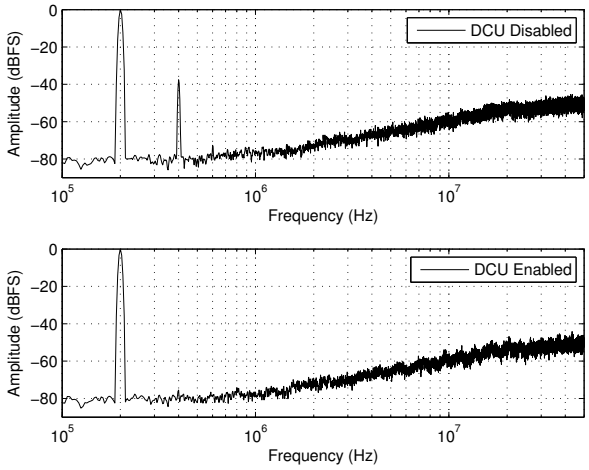

Fig. 10. Simulated output spectrum with Delay Control Unit (DCU) disabled and enabled. The effect of nonuniform sampling is seen as third harmonic, which is removed when the DCU is enabled.

A Simulink model of the proposed ADC architecture, shows the effect of nonuniform sampling in creating dominant third harmonic (Fig. 10). The proposed DCU creates the conditions for uniform sampling, and mitigates this impairment.

IV. Measurement Results

A prototype of the proposed structure was fabricated in a 0.18 μm CMOS process (1.8V, 6M, 1P) in a total area of 110 μm x 250 μm = 0.0275mm^2. The chip micrograph in Fig. 12 outlines the floorplan including the various blocks. The total power consumption is 2.7 mW using a 1.8V supply, where 2.52 mW is consumed by the VTC/Adder and the rest of the digital core consumes merely 180 μW.

Fig. 13 shows the measured output spectrum of the ADC for a 400 mV pk-pk (0 dBFS) and 146.1 kHz sinusoidal input converted with an oversampling frequency of f_s = 144 MHz. FFT length of 128K is used to generate the plot with a 7-term Blackman-Harris window. With OSR = 36, and BW = 2 MHz, SNR and SNDR were measured to be 45.1 dB and 34.6 dB, respectively.

The source of the excessive distortion of this prototype was later found and attributed to the element mismatch in the DTC

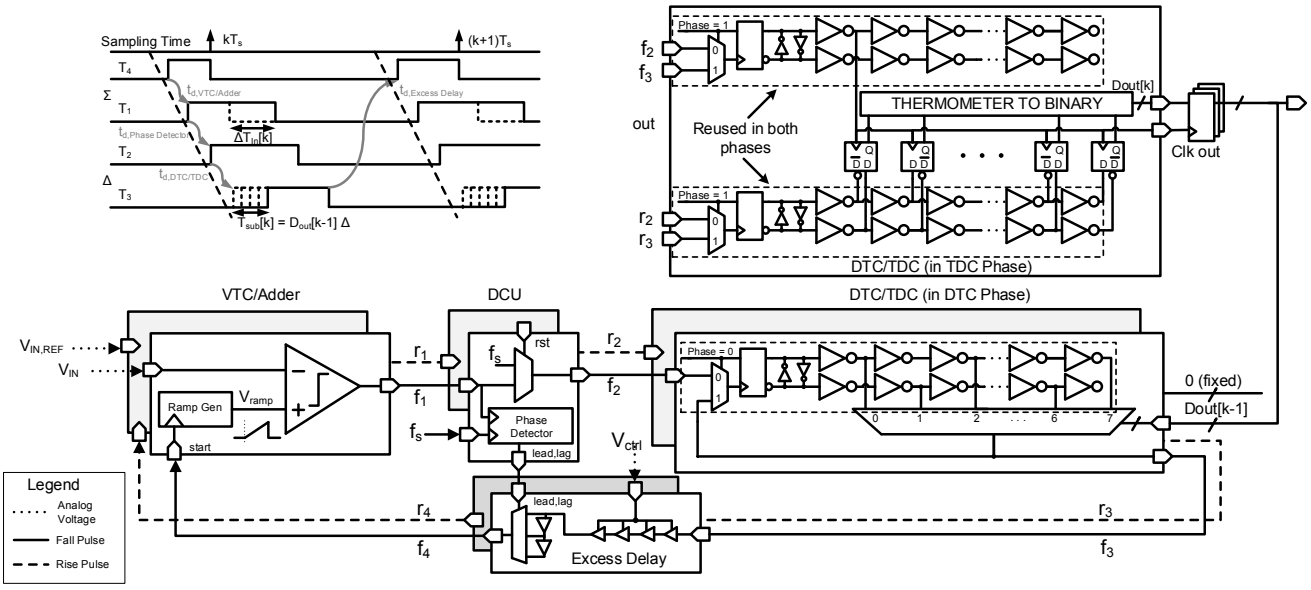

Fig. 11. Complete PWM-based $\Delta\Sigma$ ADC System

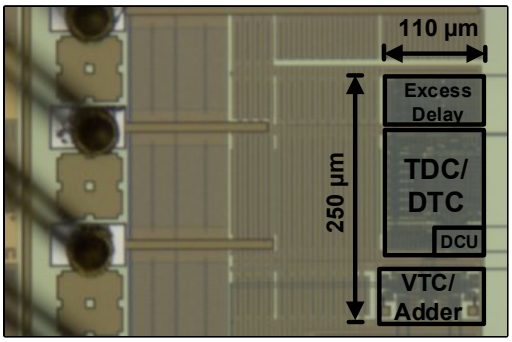

Fig. 12. Die photo

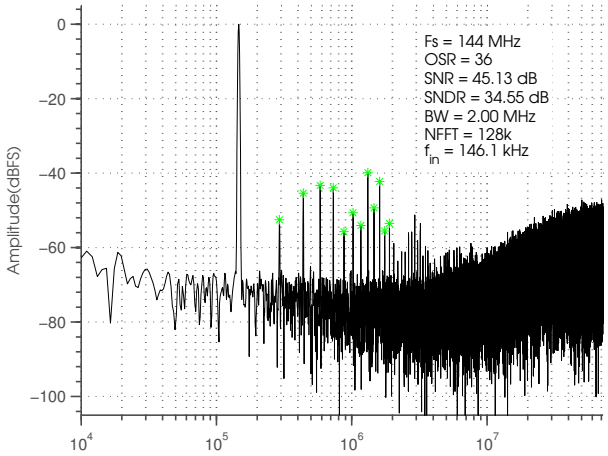

Fig. 13. Magnitude FFT spectrum of a 146.1 kHz sinusoid sampled with F_s = 144 MHz, OSR = 36.

(and also TDC). The use of inverting stages in the DTC/TDC, while having the advantage of better timing resoultion, leads to poor DNL (mismatched odd/even codes) due to the inherent mistmatch between PMOS and NMOS drive strength. A better choice for linearity would be to use noninverting delay stages.

V. Summary and Conclusion

The PWM-based $\Delta\Sigma$ ADC was proposed and a test chip fabricated. The results show a promising architecture that can take advantage of the increasingly higher timing resolution in nanometer scale process nodes. Advantages of this architecture are its simplicity, inherent multibit error matching between ADC/DAC, and small area. The challenge of pulse drift and input-dependent loop delay was mitigated using an adaptive control loop that synchronizes the asynchronous loop with an external frequency reference. The proposed delay control unit and variable excess loop delay, greatly mitigate the nonuniform sampling problem and create conditions for near-uniform sampling period. The bottlenecks of linearity in the proposed ADC are (1) DTC linearity, and (2) the VTC/Adder These may be improved using inverting delay stages in the DTC/TDC, using static nonlinearity calibration, and/or using a mismatch shaper.

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