The Embedded Signal Processing Laboratory

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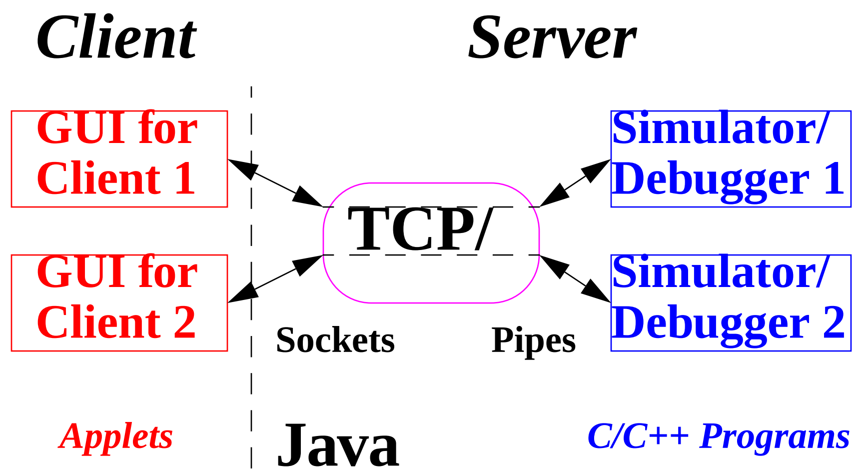
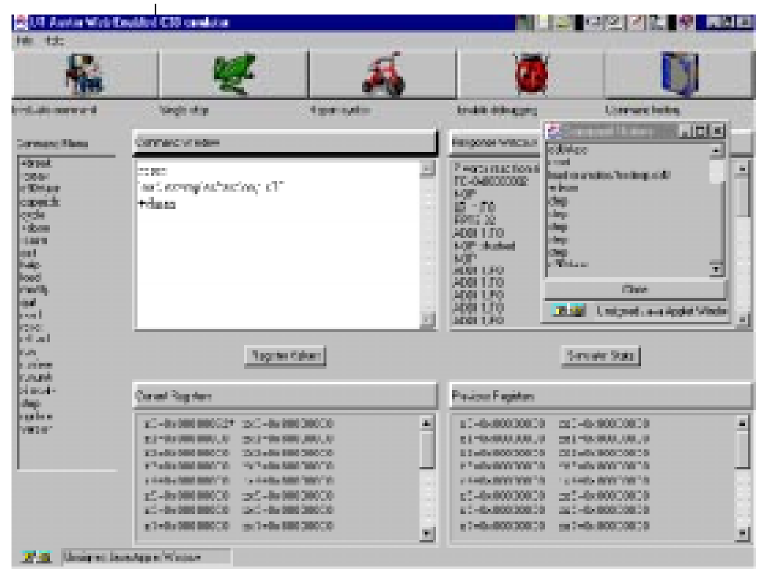
Overview

- **System-Level CAD Tools**
  - Web-enabled simulation of embedded software on microcontrollers and DSPs
  - Cosimulation/cosynthesis of hybrid neural network/signal processing systems
- **Wireline Systems**
  - ITU-compliant DTMF detectors: speaker phone (μcontroller), T1 line (DSP)
  - HDSL2 modem design and implementation in software
- **Wireless Systems**
  - Smart antennas using the constant modulus algorithm
  - Analog phase-locked loop design and implementation (beyond 1 GHz)
- **Filter Design**
  - Multi-criteria optimization for analog IIR filters
  - Minimum phase digital FIR design for real and complex, 1-D and m-D filters
- **Image and Video Processing Systems**
  - Fast image halftoning and inverse halftoning algorithms
  - Hardware/software codesign for MPEG-4 video codecs

Web-Enabled Simulation

- *Problem:* Fast system simulation technology at low cost
- *Goal*: Provide immediate access to new simulation technology without having to purchase and maintain resource-intensive tools
- *Solution*: WEDS
  - *configurable*: GUI configures itself
  - *portable*: multi-platform
  - *extensible*: easy to add new tools
  - *freely distributable*: all source code
- Simulators/Debuggers/Boards
  - Motorola MC68HC11 μcontroller
  - Motorola MC56800 DSP
  - Texas Instruments TMS320C30 DSP



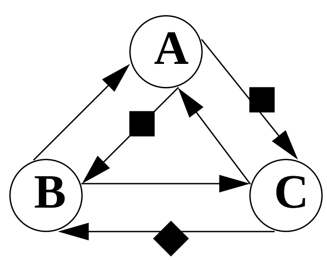


http://anchovy.ece.utexas.edu/~arifler/wetics

Dogu Arifler and Srikanth Gummadi

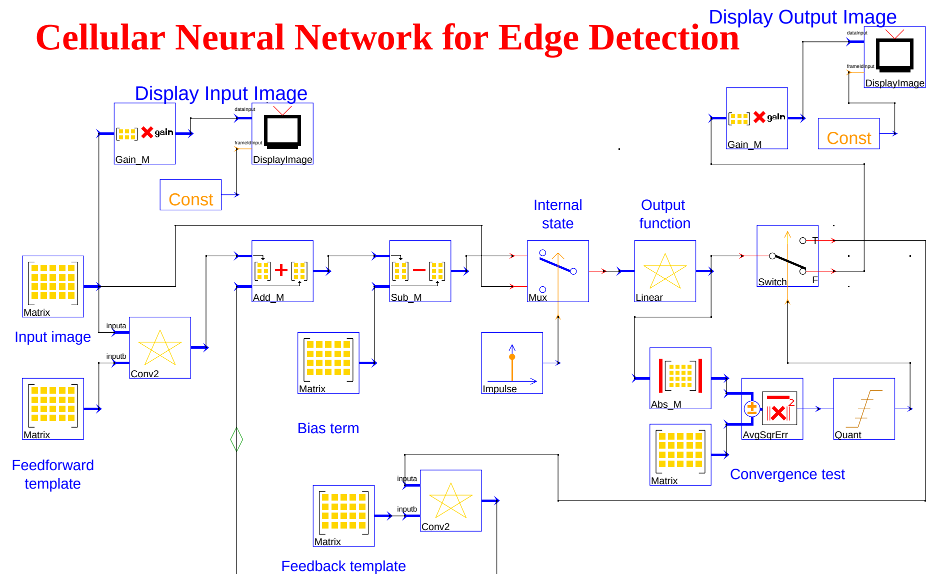
Hybrid Neural Network and Signal Processing Systems

- ***Problem*: Develop a unified model of computation for mixed artificial neural network (ANN)/signal processing systems**
  - **Gamma Memory Model (add FIR filters on the inputs of the neurons)**
  - **Cellular Neural Network (CNN) detects impulsive noise in images which is removed by a median filter**
- ***Goal*: Find a unified model for simulation and synthesis**
- ***Solution*: Use dataflow models that support static schedules**
  - **ANNs during classification: Homogeneous Synchronous Dataflow (HSDF), except CNNs require BDF models (w/ static schedules)**
  - **ANNs during training: Boolean dataflow (BDF)**



HSDF Hopfield ANN

Demonstration in Ptolemy 0.7.1



Biao Lu

Single-Channel ITU-Compliant DTMF Detection

- ***Problem***: **Design of low-cost single-channel ITU-compliant dual-tone multi-frequency touchtone signal detection**
- ***Goal***: **Develop/implement algorithm on one microcontroller for speakerphones**
- ***Solution***:
  - **Frequency estimation by zero crossing and zero crossing using a Friedman interpolator**
  - **Technique developed at Crystal Semiconductor**
- **DTMF Signals**
  - **Sum of two sinusoids: one from a low-frequency group and one from a high-frequency group**

	1209 Hz	1336 Hz	1477 Hz	1633 Hz
697 Hz	1	2	3	A
770 Hz	4	5	6	B
852 Hz	7	8	9	C
941 Hz	*	0	#	D

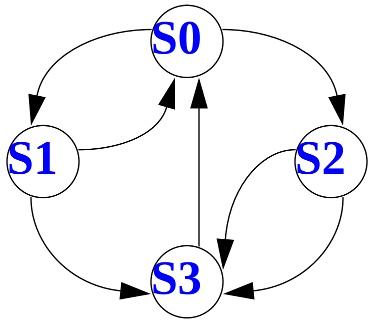
ITU DTMF Specifications

Frequency Tolerance	Low Group	<=1.5%
	High Group	>=3.5%
Signal Duration	Operation	40ms min
	Non-operation	23ms max
Signal Exceptions	Pause Duration	40ms max
	Signal Interruption	10ms min
Twist	Forward	8 dB
	Reverse	4 dB

Amey Deosthali

Multi-Channel ITU-Compliant DTMF Detection

- ***Problem*: Design of low-cost multi-channel ITU-compliant dual-tone multi-frequency (DTMF) touchtone detector**
- ***Goal*: Develop/implement first ITU-compliant detector on a single digital signal processor to perform DTMF detection on a T1 telecommunications line**
- ***Solution*:**
  - **Two sliding windows of lengths 106 and 212 samples to meet both frequency and timing specifications (106 samples = 13.3 ms)**
  - **Signal analysis to provide power level and talk-off checks**
  - **Finite state machine (FSM) to enforce ITU specifications**
  - **Detector requires 24 DSP MIPS, 800 words of data memory, and 1000 words of program memory to decode the 24 telephone channels of a T1 line**
  - **UT Austin filed a patent application on April 3, 1998, on the detector, which includes 30 claims**



FSM

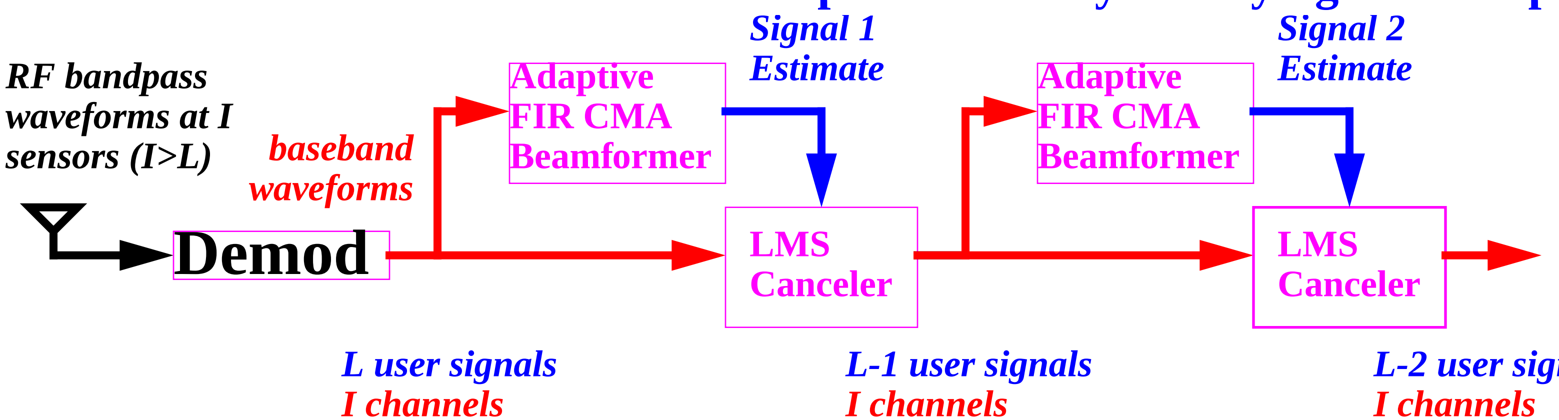
Guner Arslan, Matthew Felder, and James Mason

HDSL2 Modem in Software

- **HDSL2 requires about 1.2 billion MACs**
- **Viterbi decoder takes about**
  - **87% of processing power**
  - **91% of memory**
- **Aim: Implement HDSL2 modem using**
  - **high-end DSP processors**
  - **coprocessors**
- **Optimization**
  - **Design transmit and receive filters to have dyadic coefficients**
  - **Replace Euclidean distance in Viterbi decoder with absolute differences**
- **Current work on HDSL2 modems**
  - **Develop minimum phase transmit and receive filters**
  - **Embedded implementation of Viterbi decoder on DSP processors**
  - **Efficient implementation of echo cancelers and other filters**
  - **Replacing DSP processors with microcontrollers to reduce cost**

Smart Antennas Using the Constant Modulus Algorithm

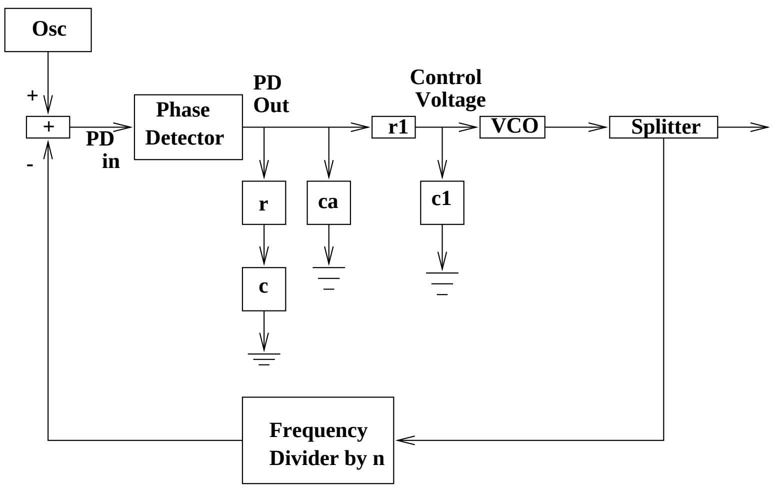
- ***Problem***: Design receivers to overcome interference and fading in wireless communications systems
- ***Goal***: Enhance signals that suffer from multipath, fading, and inter-symbol interference effects
- ***Solution***: Constant Modulus Beamformer Plus Canceler
  - Use *I* sensors to track *L* users sending CM signals (QPSK, FSK) where *I* > *L*
  - Receive narrowband (IS-95, GSM) waveforms from users in the far-field
  - Channel model includes Rayleigh fading; SNR > 10 dB at receiver output
  - Blind equalization, real-time, robust, and overcomes small frequency offsets
  - Make CMA insensitive to channel phase shifts by modifying decision process



Srikanth Gummadi

Analog Phase-Locked Loop Design and Implementation

- *Problem*: Design, prototype, and manufacture higher-order phase-locked loops (PLLs)
- *Goal*: Derive closed-form optimum design formulas for macrocomponent values in terms of system parameters
- *Solution*: Apply symbolic mathematics tools.
  - Motorola Application Note AN1253 "An Improved PLL Design Method Without ωn and ζ" derives formulas for r and c for a second-order loop as a function of charge pump gain, VCO gain, channel spacing, switching time, overshoot, loop bandwidth, VCO modulation bandwidth



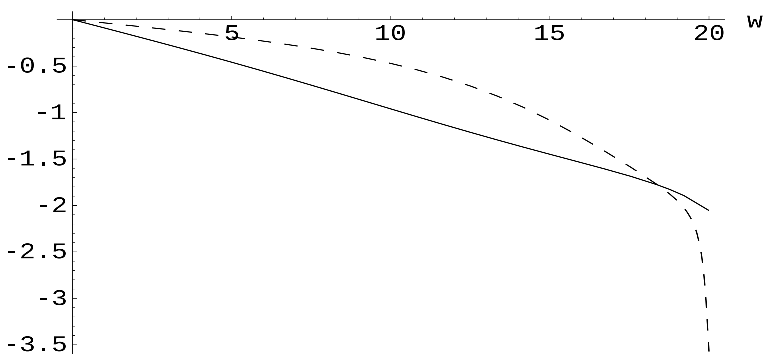
Fifth-Order Phase-Locked Loop

- Current work
  - Derive formulas for higher-order PLLs
  - Perform sensitivity analysis given tolerance of components
  - Automate the design and implementation of higher-order PLLs

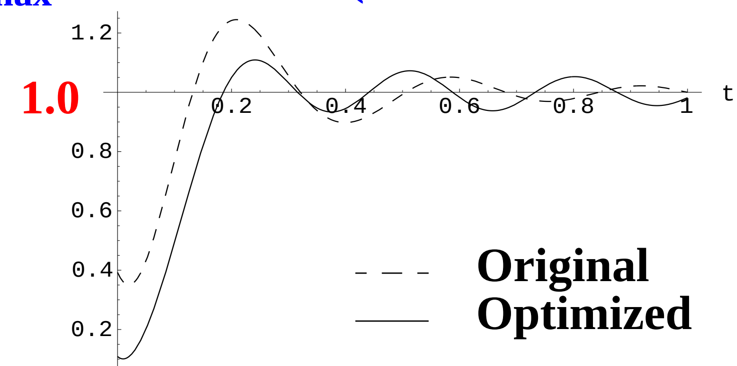
Niranjan Damera-Venkata

Multi-Criteria Analog IIR Filter Design

- ***Problem*: Optimize multiple analog filter behavioral and implementation characteristics at the same time**
- ***Goal*: Develop an extensible, automated framework**
- ***Solution*: Filter Optimization Packages for Mathematica**
  - **Constrained non-linear optimization as Sequential Quadratic Programming: converges to global optimum & robust when closed-form gradients provided.**
  - **Program Mathematica to derive formulas for cost function, constraints, and gradients, and convert the formulas to Matlab programs to run optimization.**
  - **Example: linearize phase and minimize peak overshoot of an elliptic filter; constraining Q_{max} to 10 reduced Q_{max} from 61 to 10 (filter easier to build)**



Linearized phase in passband

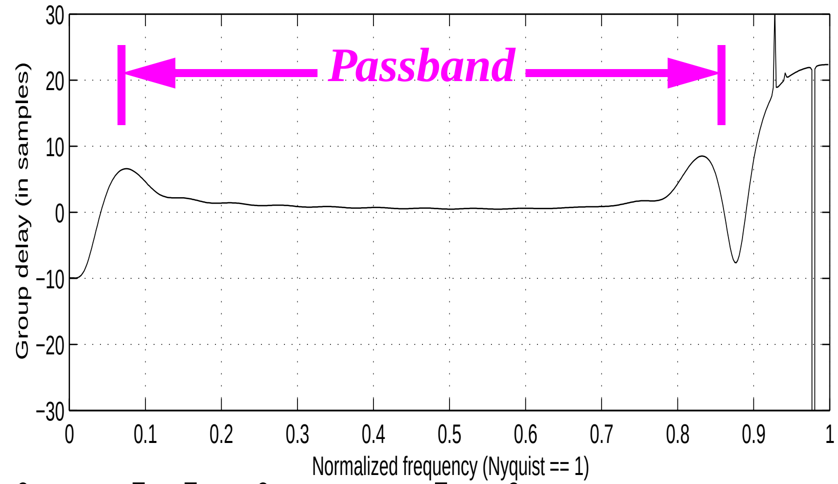


Minimized peak overshoot

http://www.ece.utexas.edu/~bevans/projects/syn_filter_software.html

Minimum Phase Digital FIR Filter Design

- ***Problem***: **Design optimal minimum phase digital FIR filters**
- ***Goal***: **Develop an algorithm that designs real and complex minimum phase digital FIR filters**
- ***Solution***: **Use the Discrete Hilbert Transform**
  - **Use the generalized Hilbert Transform relation to compute the *unique* minimum phase response from the given magnitude response**
  - **Reconstruct the minimum phase polynomial sampling the magnitude and phase response and use the inverse FFT (*the FFT length controls coefficient accuracy*)**
  - **Example: group delay of a 65-tap minimum phase approximation for a telephone channel: group delay reduced from 33 samples to nearly 0 samples in passband**

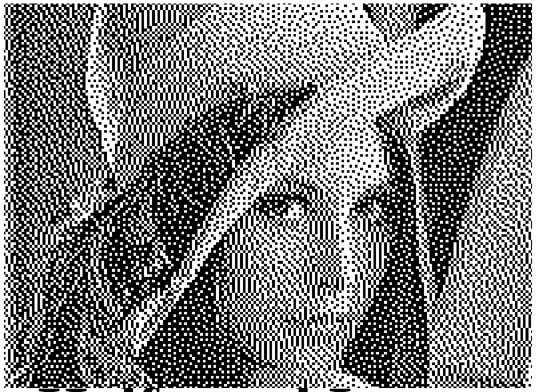


- **For improvements to conventional design techniques:**

ftp://pepperoni.ece.utexas.edu/pub/minphase/mccaslin/minphase.m

Fast Image Halftoning & Inverse Halftoning Algorithms

- *Problem*: Fast high-quality algorithms for halftoning for printers and inverse halftoning for scanned images
- *Goal*: Develop scalable algorithms that deliver high subjective image quality
- *Solution*: Model halftoning as 2-D delta-sigma modulation
  - Noise-shaped feedback coder (Δ-Σ) has signal and noise transfer functions
  - Objective measures of edge sharpening (proportional to quantizer gain) and shaped noise (noise transfer function) in halftoned images
  - Objective measures of blurring and spatially-varying noise in inverse halftoned images



Halftoned Image

Original Image

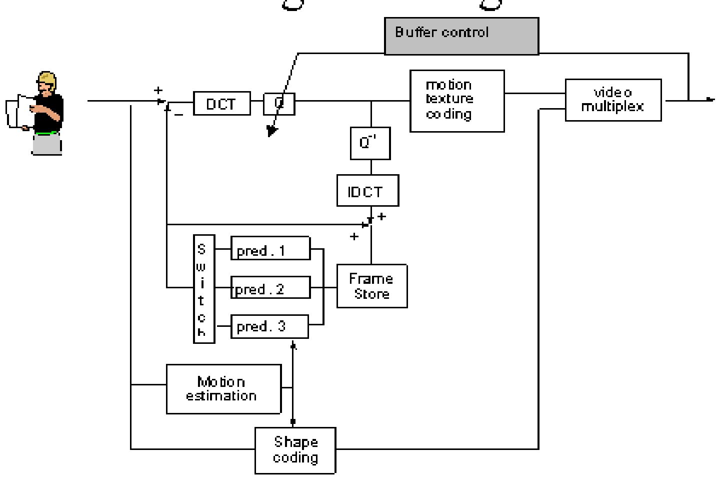
Inverse Halftone

Thomas Kite and Niranjan Damera-Venkata

Hardware/Software Codesign for MPEG-4 Video Codecs

- *Problem*: **Rapid prototyping of audio/video codecs as a new standard being adopted each year since 1992, e.g.**
  - **MPEG-2: (1994): scalable (1-4 Mbps), surround sound, multiplexing**
  - **MPEG-4 (1998): scalable (0.01-4 Mbps), interactive, content-based**
- *Goal*: **Develop a formal system-level design methodology that includes H.261, H.263, H.263+, and MPEG 1, 2, and 4.**
- *Solution*: **Hierarchically combine multiple models of computation for reuse, fast cosimulation, and cosynthesis**

Video/Image Coding Scheme



Structure of Tools