High-Speed Digital Subscriber Line Generation 2 (HDSL2) Modem

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Outline

- Need for high bandwidth
- Digital Subscriber Line (DSL) standards
- Top-level block diagram of HDSL2 modem
- Estimate of implementation cost of a soft HDSL2 modem
- Summary

Need for High Bandwidth

- **Small Office / Home Office**
  - Small business run out of home: 20 million small businesses in the US
- **Internet Access**
  - Internet users: 28 million, growing by 2x every year
- **Internet Service**
  - Web sites: 230,000, growing by 2x every 6 months
- **Telecommuting**
  - Work at home: 5-10 million telecommuters in the US
- **Video-conferencing**

Communication bandwidth between the computers has not kept up with advances in computing power, system memory size, and storage capacity

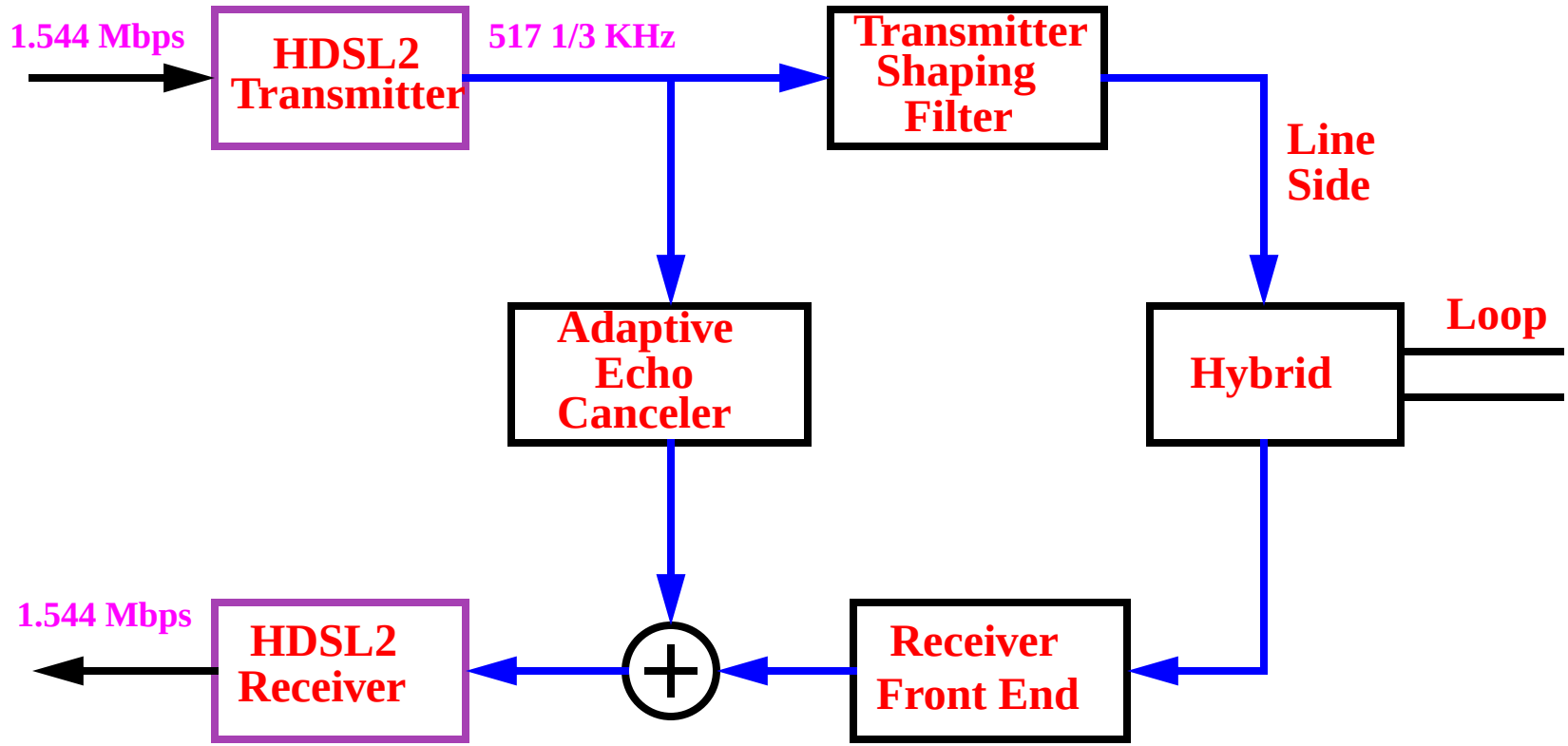
March 9, 1998: Motorola sends samples of CopperGold ADSL solution to customers
Nov. 19,1997: Texas Instruments purchases Amati for its ADSL and VDSL technology ($395 million)

Existing and Proposed DSL Standards

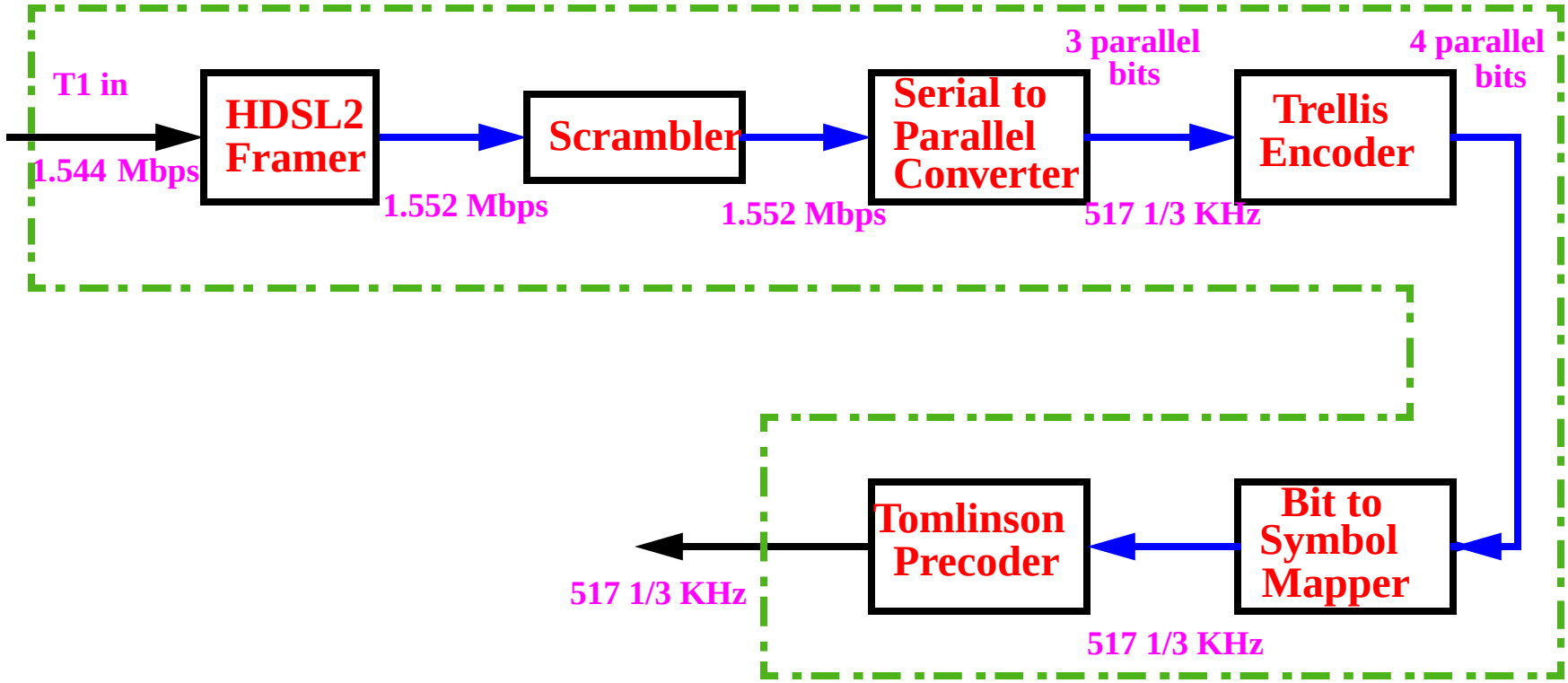
Standard	Meaning	Data Rate	Mode	Applications
V.34	*Voice Band Modem*	*33.6 Kbps*	*Symmetric*	*Internet Access*
V.PCM	*Voice Band Modem*	*56 Kbps* *33.6 Kbps*	*Down* *Up*	*Internet Access*
ISDN	Integrated Services Digital Network	144 Kbps	Symmetric	Internet Access, Pair Gain (2 channels)
T1	T - Carrier One (requires two pairs)	1.544 Mbps	Symmetric	Enterprise, Expansion, Internet Service
HDSL	High Speed Digital Subscriber Line (requires two pairs)	1.544 Mbps	Symmetric	Pair Gain (12 channels) Internet Access, T1/E1 replacement
HDSL2	Single Line HDSL	1.544 Mbps	Symmetric	Pair Gain (24 channels)
ADSL	Asymmetric Digital Subscriber Line	1.5 - 9 Mbps 16-640 Kbps	Down Up	Internet Access, Digital Video
VDSL	Very High Speed DSL	13 - 52 Mbps 1.5-2.3 Mbps	Down Up	Internet Access, Digital Video

(Courtesy of Cicada Semiconductor, Austin, TX)

Top-level Block Diagram of HDSL2 Modem



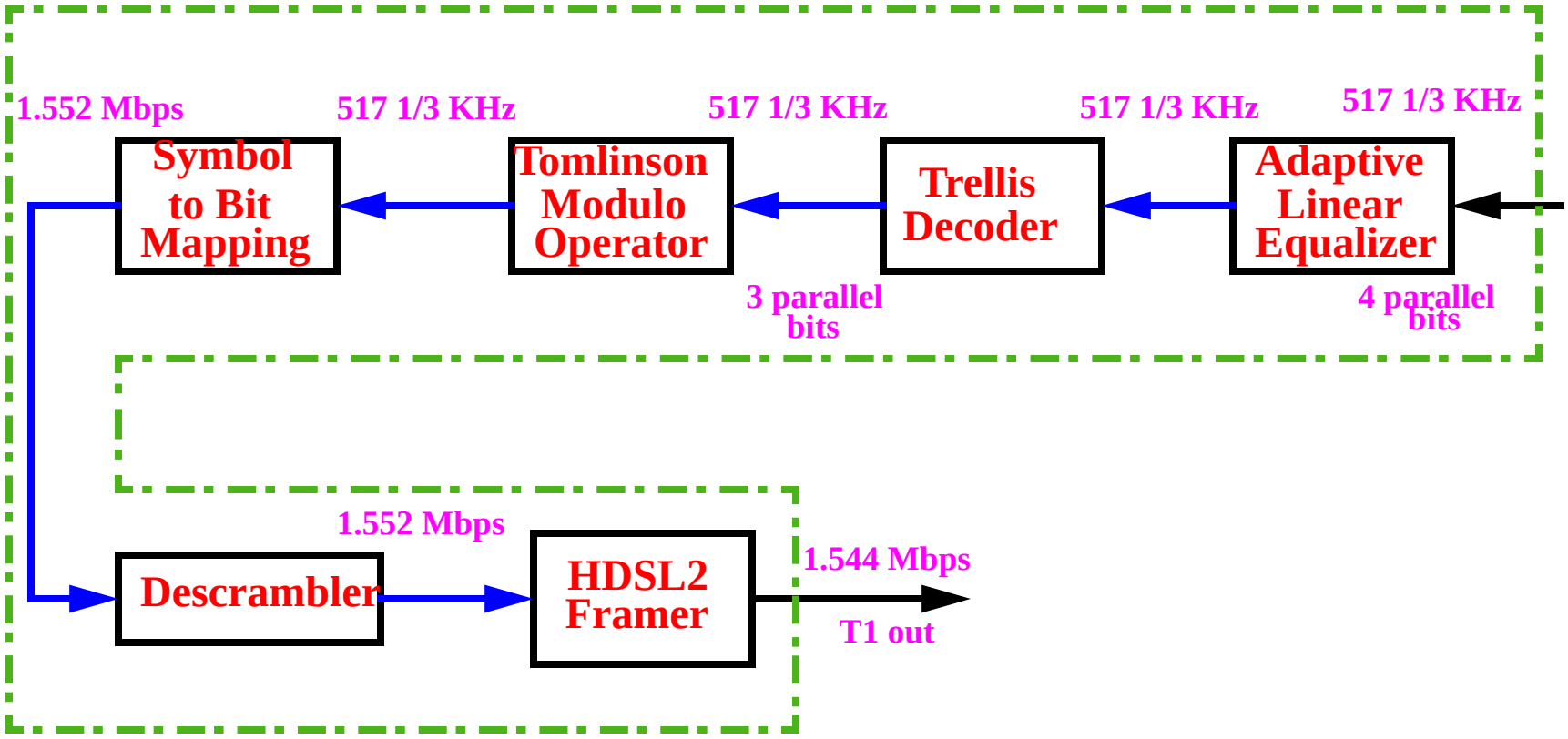
Block Diagram of HDSL2 Transmitter



HDSL2 Transmitter (as approved by T1E1.4 subcommittee)

December 9, 1997

Block Diagram of HDSL2 Receiver



HDSL2 Receiver (as approved by T1E1.4 subcommittee)

December 9, 1997

Estimate of Processing Power and Memory

Module	Multiplications (in millions/sec)	Additions (in millions/sec)	Memory (bits)
Framer	*none*	1.544	*FrameSize*
Scrambler	*none*	3 x 1.552	24 x 16 x 2
Trellis encoder	*none*	9 x 1.552	10 x 16
Bits to Symbol	*none*	*none*	2 x 16 x 16
Tomlinson precoder	100 x 1.552/3 + *update*	100 x 1.552/3 + *update*	100 x 16
Transmit filter	50 x 1.552/3	50 x 1.552 /3	50 x 16
Echo canceler	100 x 1.552/3 + *update*	100 x 1.552/3 + *update*	100 x 16
Receiver filter	50 x 1.552/3	50 x 1.552/3	50 x 16
Trellis decoder	**512 x 2 x 2 x 1.552/3 = 2048 x 1.552/3**	**512 x 2 x 1.552/3**	**80 x 1024**
Symbol to bits	*none*	*none*	2 x 16 x 16
Descrambler	*none*	3 x 1.552	24 x 16 x 16
Framer	*none*	1.554	*FrameSize*
TOTAL	**1214.7 + 2 x *update***	**711.34 + 2 x *update***	**89,440**

Summary

- HDSL2 requires about 1.2 billion MACs
- Viterbi decoder takes about
  - 87% of processing power
  - 91% of memory
- Aim: Implement HDSL2 modem using
  - high-end DSP processors
  - coprocessors
- Optimization
  - Design transmit and receive filters to have dyadic coefficients
  - Replace Euclidean distance in Viterbi decoder with absolute differences
- Current work on HDSL2 modem design
  - Develop minimum phase transmit and receive filters
  - Embedded implementation of Viterbi decoder on DSP processors
  - Efficient implementation of echo cancelers and other filters
  - Replacing DSP processors with microcontrollers to reduce cost