DIANA MARCULESCU

The University of Texas at Austin
Dept. of ECE, 2501 Speedway
Austin, TX 78712

Phone: (512) 471-6179, (512) 232-8118
E-mail: dianam@utexas.edu
URL: http://users.ece.utexas.edu/~dianam

Department Chair, Cockrell Family Chair for Engineering Leadership #5
Professor, Motorola Regents Chair in Electrical and Computer Engineering #2

RESEARCH INTERESTS

Sustainability- and energy-aware computer system modeling and optimization

Energy- and hardware-aware machine learning; Fast and accurate power modeling, estimation, optimization for multi-core systems; Modeling and optimization for sustainability in computing and renewable energy

Reliability- and variability-aware system design

Modeling, analysis, and optimization of soft-error rate in large digital circuits; Microarchitecture to system level design variability modeling and mitigation; 3D integration and impact of process variations

Discrete modeling and analysis of non-silicon networks

Logical models and hardware emulation for efficient nonlinear system analysis; Efficient models for computational biology; Electronic textiles and smart fabrics

EDUCATION

Ph.D. in Computer Engineering, University of Southern California - August 1998
Dissertation: *Information-theoretic and Probabilistic Measures for Power Analysis of Digital Circuits*
Advisor: *Prof. Massoud Pedram*

B.S./M.S. in Computer Science (Eng. Dipl.), Polytechnic Institute of Bucharest, Romania - June 1991
Dissertation: *Fault-tolerant Database System Design*
Advisor: *Prof. Irina Athanasiu*

PROFESSIONAL EXPERIENCE

Department Chair and Cockrell Family Chair for Engineering Leadership #5, Dept. of Electrical and Computer Engineering, University of Texas at Austin, Dec. 2019 – present

Currently leading the Department of Electrical Engineering of more than 1590 undergraduate students, 650 graduate students, and 62 tenured and tenure-track faculty; and overseeing an annual research expenditure budget of more than $23M.

Professor and Motorola Regents Chair in Electrical and Computer Engineering #2, Dept. of Electrical and Computer Engineering, University of Texas at Austin, Dec. 2019 – present

Currently conducting research and leading a group of graduate, undergraduate, and postdoctoral researchers in the area of energy aware and sustainable computing, and hardware aware machine learning. Top ten researcher in energy aware computing, design automation (according to Google Scholar). Recipient of multiple international awards and honors. Principal and co-principal investigator on projects from government and industry, and in collaboration with faculty and researchers from Electrical and Computer Engineering (UT Austin, Carnegie Mellon University), Qualcomm, Microsoft, Google, Arm, and Facebook.

David Edward Schramm Professor, Dept. of ECE, Carnegie Mellon University, Oct. 2016 – Nov. 2019

Professor, Dept. of ECE, Carnegie Mellon University, July 2009 – Nov. 2019

Conducted research, teaching, and led a group of graduate, undergraduate, and postdoctoral researchers in the area of energy aware and sustainable computing, and computing for sustainability. Top ten researcher in energy aware computing, design automation and top woman researcher in the same fields (according to Google Scholar). Recipient of multiple international awards and honors. Principal and co-principal investigator on $10.5M total funding from government and industry, and in collaboration with faculty and researchers from Electrical and Computer Engineering (CMU, University of Southern California, and Washington State University), Biology, Machine Learning, Language and Technology, Philosophy (CMU), School of Medicine (University of Pittsburgh), Civil, Architectural and Environmental Engineering (University of Texas at Austin), Energy and Mineral Engineering (Pennsylvania State University), IBM, Samsung, Qualcomm, Microsoft, and Google.

Founding Director, Center for Faculty Success, College of Engineering, Carnegie Mellon University,

Nov. 2014 – November 2019

Founded and led the only CMU center focused on faculty development and support. Developed and ran programs for faculty recruiting, mentoring, development, and diversity/inclusion awareness for over 600 faculty, staff, and students at CMU and other institutions. Led a team of engineering faculty and collaborated with Google researchers and School of Computer Science faculty in developing and deploying the Bias Busters program for increasing awareness and mitigating the effects of unconscious bias both within and outside CMU. Developed programming and support for junior faculty through a new faculty orientation, mentoring, and workshops; Bias Buster sessions for both individual and group settings, such as search committees, promotion and tenure committees, graduate admissions; support for faculty development and leadership training; and programming for academic job interview skill building for future faculty candidates among engineering Ph.D. students and postdoctoral researchers.

Associate Department Head for Academic Affairs, Dept. of ECE, Carnegie Mellon University,

June 2014 – May 2018

Led and managed academic affairs for the Department of Electrical Engineering of more than 500 undergraduate students, 600 graduate students, and 75 core faculty across the Pittsburgh and remote ECE campuses. Led the effort to revamp the ECE curriculum for the new century to focus on flexibility, maker culture, student support, and professional services and in particular, to streamline and revamp our course offerings in areas we aim to be leaders in: Cyberphysical Systems, Data and Network Science, Computer Security, and Wireless Systems, all of which featured as MS degree concentrations. Supported the work of the faculty teams involved in revamping and reassessing our undergraduate introductory and capstone design experience courses and worked with staff in the Offices of Student and Academic Affairs, and Graduate Affairs in their efforts for streamlining processes for teaching assistant training and selection.

Systems Area Leader, Center for Silicon Systems Implementation, Aug. 2008 – Jan. 2015

Led the Systems area within the Center for Silicon System Implementation, including annual research reports and reviews.

Visiting Professor, University Joseph Fourier and CEA/LETI, Grenoble, France, June – July 2010

Hosts: Dr. Ahmed Jerraya and Dr. Fabien Clermidy

Conducted research in the area of variation- and reliability-aware multi-core system design.

Visiting Professor, Technical University Munich, Dept. of ECE, Germany, April – July 2009

Host: Prof. Ulf Schlichtmann

Conducted research in the area of variation- and reliability-aware multi-core system design.

Associate Professor of ECE, Dept. of ECE, Carnegie Mellon University, July 2005 – July 2009

Conducted research, teaching, and led a group of graduate, undergraduate, and postdoctoral researchers in the area of energy aware computing. Recipient of multiple international awards and

honors. Principal and co-principal investigator on $2.3M total funding from government and industry, and in collaboration with faculty and researchers from Electrical and Computer Engineering (CMU).

Assistant Professor of ECE, Dept. of ECE, Carnegie Mellon University, March 2000 – July 2005

Conducted research, teaching, and led a group of graduate, undergraduate, and postdoctoral researchers in the area of energy aware computing. Recipient of multiple international awards and honors. Principal and co-principal investigator on $3M total funding from government and industry, and in collaboration with faculty and researchers from Electrical and Computer Engineering (CMU), Industrial Technology Research Institute (Taiwan).

Assistant Professor of ECE, Dept. of ECE, University of Maryland, Aug. 1998 – Feb. 2000

Conducted research, teaching, and led a group of graduate and undergraduate researchers in the area of CAD for low power design. Principal investigator on $300K total funding from government and industry, and in collaboration with faculty and researchers from Electrical and Computer Engineering (UMD).

Graduate Research Assistant, Dept. of EE-Systems, University of Southern California, Jan.1994 – Aug. 1998

Conducted research in the area of CAD for power modeling and optimization.

Teaching Assistant, Dept. of CS, New York University, Aug. 1993 – Dec. 1993

Assisted with teaching courses in the area of programming languages.

Teaching Assistant, Dept. of CS, "Politehnica" Univ. of Bucharest, Romania, Jan.1992 – Aug.1993

Assisted with teaching courses in the areas of formal languages and compilers, automata theory, system modeling and simulation.

Software Engineer, Research Institute for Building Design, Bucharest, Romania, Sept.1991 – Jan.1992

Developed and maintained codebase for the research division.

AWARDS AND HONORS

THE UNIVERSITY OF TEXAS AT AUSTIN

Fellow, Association for Computing Machinery, 2020 (for contributions to design and optimization of energy-aware computing systems).

CARNEGIE MELLON UNIVERSITY

Best Paper Award, IEEE Trans. on Very Large Scale Integrated Systems, 2018 (one winner selected out of approximately 360 journal articles).

Barbara Lazarus Award, 2018 (given to a faculty member within the Carnegie Mellon University in recognition of outstanding graduate student and junior faculty mentoring).

Carnegie Institute of Technology Outstanding Faculty Mentor Award, 2017 (given to a faculty member within the Carnegie Institute of Technology in recognition of outstanding graduate student and junior faculty mentoring).

Best Paper Award, ACM Great Lakes Symposium on VLSI, 2017 (one winner selected out of 50 accepted papers).

David Edward Schramm Professorship, Department of Electrical and Computer Engineering, 2016.

Fellow, Institute for Electrical and Electronics Engineers, 2015 (for contributions to design and optimization of energy-aware computing systems).

Marie R. Pistilli Women in EDA Achievement Award, ACM/EDAC/IEEE Design Automation Conference, 2014 (recognizes individuals who have visibly helped to advance the profile of women in the EDA industry).

"Future" Fellow, Australian Research Council, 2013-2017 (supports outstanding mid-career researchers to conduct world-class, innovative research in Australia; the only 2013 awardee in the Computer Science area; deferred).

Distinguished Scientist, Association for Computing Machinery, 2011 (recognizes those members with at least 15 years of professional experience who have made significant accomplishments or achieved a significant impact on the computing field).

Best Paper Award, IEEE Trans. on Very Large Scale Integrated Systems, 2011 (one winner selected out of approximately 360 journal articles).

Best Paper Award, IEEE Intl. Symp. on Quality in Electronic Design, 2009 (two winners selected out of 87 accepted papers).

Best Paper Award, IEEE Intl. Conf. on Computer Design, 2008 (one winner selected out of 113 accepted papers).

Best Paper Award, IEEE/ACM Asian-South Pacific Design Automation Conference, 2005 (two winners out of 99 accepted papers).

Carnegie Institute of Technology George Tallman Ladd Research Award, 2004 (given to a faculty member within the Carnegie Institute of Technology in recognition of outstanding research and professional accomplishments and potential).

National Science Foundation Faculty Early Career Development Award, 2000-2004 (National Science Foundation's most prestigious awards in support of junior faculty who exemplify the role of teacher-scholars through outstanding research, excellent education and the integration of education and research within the context of the mission of their organizations).

OTHER HONORS AND PRIZES

CARNEGIE MELLON UNIVERSITY

Carnegie Mellon University Negotiation and Leadership Academy for Women, 2017-2018.

Inspiring Women in STEM award, Insight into Diversity, 2016.

ELATE Fellow, Executive Leadership in Academic Technology and Engineering, 2013-2014.

IT Honor Roll, IT History Society, 2012 (for developing novel power management techniques to improve the performance delivered per unit of energy consumed for computer hardware and software).

Best Paper Award Nomination, IEEE Design, Automation and Test in Europe Conference, 2009 (less than ten papers nominated out of 232 accepted).

Two Best Paper Award Nominations, 45th ACM/IEEE Design Automation Conference, 2008 (ten papers nominated out of 147 accepted).

Best Paper Award Nomination, 44th ACM/IEEE Design Automation Conference, 2007 (eleven papers nominated out of 161 accepted).

Best Paper Award Nomination, IEEE Intl. Symp. on Quality in Electronic Design, 2007 (less than ten papers nominated out of 93 accepted).

Best Paper Award Nomination, IEEE Transactions on VLSI Systems, 2006 (less than ten papers nominated out of 360 journal articles).

Top Cited Papers for 1990-2000, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, for paper "Information theoretic measures for power analysis," 15(6):599-610 (http://tcad.polito.it/editor/top-cited-TCAD.htm).

Best Paper Award Nomination, IEEE Design, Automation and Test in Europe Conference, 2005 (less than ten papers nominated out of 176 accepted).

IEEE-Circuits and Systems Society Distinguished Lecturer, 2004-2005.

UNIVERSITY OF SOUTHERN CALIFORNIA

Best Paper Award Nomination at the 34th ACM/IEEE Design Automation Conferences, 1997 (twelve papers nominated out of 139 accepted).

Best Paper Award Nomination at the 33rd ACM/IEEE Design Automation Conferences, 1996 (twelve papers nominated out of 142 accepted).

Special Mention at the "Traian Lalescu" National Student Contest on Mathematical Sciences, Bucharest, Romania, 1988 (three prizes and two special mentions selected out of approximately 5,000 engineering sophomore students).

First Prize at the "Traian Lalescu" National Student Contest on Mathematical Sciences, Cluj-Napoca, Romania, 1987 (one winner selected out of approximately 5,000 engineering first year students).

SERVICE AWARDS

CARNEGIE MELLON UNIVERSITY

IEEE CEDA Distinguished Service Award, 2016 (for chairing the IEEE/ACM International Conference on Computer Aided Design).

ACM/EDAC/IEEE Design Automation Conference (DAC) Service Award, 2013 (for creating the ACM Student Research Competition at DAC).

ACM-SIGDA Distinguished Service Award, 2010 (given to individuals who have dedicated many years of their career to promoting, leading, or creating ACM/SIGDA programs or events).

Elected Chair, Special Interest Group on Design Automation, Association for Computing Machinery (ACM-SIGDA), 2005 (top number of votes submitted via secret ballot by approximately 1,000 members).

ACM-SIGDA Technical Leadership Award, 2001-2003 (one winner selected from approximately 20 ACM-SIGDA volunteers).

AWARDS AND HONORS - ADVISED STUDENTS

THE UNIVERSITY OF TEXAS AT AUSTIN

Qualcomm Innovation Finalists for CMU Ph.D. students Ting-Wu (Rudy) Chin and Ahmet Inci (2020).

UT Austin Graduate Mentoring Fellowship for UT Ph.D. student Natasha Frumkin (2020).

CARNEGIE MELLON UNIVERSITY

Bob Lee Gregory Fellowship for Ph.D. Student Ahmet Fatih Inci (2019).

Liang Ji-Dian Fellowship for Ph.D. Student Ruizhou Ding (2018).

David Barakat and LaVerne Owen-Barakat Fellowship for Ph.D. student Ting-Wu (Rudy) Chin (2018).

Qualcomm Innovation Fellowship for Ph.D. students Dimitrios Stamoulis and Zhuo Chen (2018).

Siemens Future Makers Challenge, Third Prize for Ph.D. students Ermao Cai, Zhuo Chen, Ting-Wu Chin, Ruizhou Ding (2018).

David Barakat and LaVerne Owen-Barakat Fellowship for Ph.D. student Dimitrios Stamoulis (2017).

Onassis Ph.D Scholarship for Ph.D. student Ifigeneia Apostolopoulou (2016).

Gerondelis Ph.D Scholarship for Ph.D. student Ifigeneia Apostolopoulou (2016).

Gerondelis Ph.D Scholarship for Ph.D. student Dimitrios Stamoulis (2016).

Vlahakis Ph.D. Fellowship for Ph.D. student Ifigeneia Apostolopoulou (2015-2016).

IEEE Rebooting Computing – Low Power Image Recognition Challenge: Ready to Go Award for CMU team: Zhuo Chen, Ermao Cai, Jiyuan Zhang, Zijun Wan, Tong Yu, Yong Zhuang (June 7, 2015, San Francisco, CA).

iGEM East Jamboree: Silver Medal and Best Poster Award for CMU team: Eric Pederson, Evan Starkweather, Ben Beltzer, Andrew Nadig, Kathy Bates (October 4-6, 2013, Toronto, Canada).

iGEM International Jamboree: Best Foundational Advance prize for CMU team: Yang Choo, Eric Pederson, Jesse Salazar, Peter Wei (Nov. 2-5, 2012, Cambridge, MA).

iGEM East Jamboree: First prize, Gold medal and Best BioBrick Measurement Approach prize for CMU team: Yang Choo, Eric Pederson, Jesse Salazar, Peter Wei (Oct. 13-14, 2012, Pittsburgh, PA).

Intel Foundation Ph.D. Fellowship for Ph.D. Student Da-Cheng Juan (2012-2014).

Semiconductor Research Corporation Undergraduate Research Opportunities Fellowship for Niharika Singh (2011-2014).

Lockheed-Martin Eta Kappa Nu Second Prize for Archa Jain, Neereja Sundaresan, "Parameterizable On-Chip Communication Synthesis for Multi-Core Systems" (2011).

Liang Ji-Dian Fellowship for Ph.D. Student Kai-Chiang (Alex) Wu (2011).

Angel G. Jordan Award for Ph.D. Student Siddharth Garg (2010).

Intel Foundation Ph.D. Fellowship for Ph.D. Student Sebastian Herbert (2007-2009).

Lamme-Westinghouse Fellowship for Ph.D. Student Phillip Stanley-Marbell (2005-2006).

Third Prize, Carnegie Institute of Technology "Meeting of the Minds," for Jianjian Sun, "Deployment of Low Power Modes for E-Textile Applications" (2005).

First Prize, Carnegie Institute of Technology "Meeting of the Minds," for Justiin Ang and Shing-Tai Leung, "Energy Aware Computer Arithmetic Modules" (2002).

Lockheed-Martin Eta Kappa Nu Third Prize for Shing-Tai Leung, "A Library of Energy Aware Computing Gates" (2002).

PRESS COVERAGE

"Monitoring tools for small footprint hydroelectric projects," by Mike Keller, Txchnologist, Jan. 2014.

"Variability modeling moves to system level," by Richard Goering, SCDsource Newsletter, March 2008.

"Winners & Losers 2007: Beauty and the Beast - Not Ready to Wear," by Harry Goldstein, IEEE Spectrum, Jan. 2007.

"Electronic Garments Sense Emotion," by Tracy Schrader, Discovery News, Oct. 2006.

"Clothing Goes Hi-Tech," by Nicole McEwen, The Eagle Tribune, Dec. 2005.

"Wearing Wires," by Malcolm Beith, Newsweek International, July 2003.

"The Future of GALS Systems," in Elektroniktidningen (Swedish Electronics Journal), Oct. 2002.

"Tomorrow's technology points to present-day solutions," by Nicholas Mokhoff, EE Times, June 2002.

PUBLICATIONS

BOOKS AND BOOK CHAPTERS

CARNEGIE MELLON UNIVERSITY

[B11] K. Bharadwaj, R. Ding, D. Stamoulis, R. Marculescu, and D. Marculescu, "Computational Approaches for Incorporating Short and Long Term Dynamics in Smart Water Networks," in *Smart Water Grids: A Cyber-Physical Approach*, P. Tsakalides, A. Panousopoulou, G. Tsagkatakis, L. Montestruque (eds.), Taylor and Francis, 2018.

[B10] S. Garg, Y. Turakhia, and D. Marculescu, "Heterogeneous Dark Silicon Chip Multi-Processors: Design and Run-time Management," in *The Dark Side of Silicon (Computing in the Dark Silicon Era)*, A. Jantsch and A. Rahmani (eds.), Springer Verlag, 2017.

[B9] S. Garg, D. Marculescu, and R. Marculescu, "Fundamental Limits on Run-time Power Management Algorithms for MPSoCs," in *Sustainable and Green Computing Systems*, P. Pande (ed.), Springer Verlag, 2013.

[B8] S. Herbert and D. Marculescu, "Variability-Aware Frequency Scaling in Multi-Clock Processors," in *Adaptive and Dynamic Techniques for Processor Optimization: Theory and Practice*, A. Wang and S. Naffzinger (eds.), Springer Verlag, 2008.

[B7] E. Talpes and D. Marculescu, "Low power microarchitecture techniques," in *The VLSI Handbook*, W.-K. Chen (ed.), CRC Book Press, 2006.

[B6] P. Stanley-Marbell, D. Marculescu, R. Marculescu, and P.K. Khosla, "Challenges and Opportunities in Modeling, Analysis and Optimization of Electronic Textiles," in *Low Power Electronics Design*, C. Piguet (ed.), CRC Book Press, 2004.

[B5] P. Stanley-Marbell, N.H. Zamora, D. Marculescu, and R. Marculescu, "Fault-tolerant techniques for ambient intelligent distributed systems," in *Ambient Intelligence: Impact on embedded-system design*, T. Basten, M. Geilen, H. de Groot (eds.), Kluwer Academic Publishers, 2003.

[B4] V.S.P. Rapaka and D. Marculescu, "Efficient power/performance analysis of embedded and general purpose software applications," in *Embedded Software for SoC*, A. Jerraya, S. Yoo, N. Wehn, D. Verkest (eds.), Kluwer Academic Publishers, 2003.

[B3] S.W. Haga, N. Reeves, R. Barua, and D. Marculescu, "Dynamic functional units assignment for low power," in *Embedded Software for SoC*, A. Jerraya, S. Yoo, N. Wehn, D. Verkest (eds.), Kluwer Academic Publishers, 2003.

[B2] D. Marculescu and R. Marculescu, "System and microarchitectural level power modeling, optimization, and their implications in energy aware computing," in *Power Aware Design Methodologies*, M. Pedram, J. Rabaey (eds.), Kluwer Academic Publishers, 2002.

UNIVERSITY OF MARYLAND, COLLEGE PARK

[B1] I. Athanasiu, D. (Raiciu) Marculescu, R. Sion, and I. Mocanu, "Formal Languages – Applications," Computer Science Department, "Politehnica" University of Bucharest Press, December 1999.

ARCHIVAL JOURNAL PUBLICATIONS

THE UNIVERSITY OF TEXAS AT AUSTIN

[J51] A. Inci, M.M. Isgenc, and D. Marculescu, "DeepNVM++: Cross-Layer Modeling and Optimization Framework of Non-Volatile Memories for Deep Learning," submitted to *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Dec. 2020 (under review).

[J50] D. Stamoulis, R. Ding, D. Wang, D. Lymberopoulos, B. Priyantha, J. Liu, D. Marculescu, "Single-Path Mobile AutoML: Efficient ConvNet Design and NAS Hyperparameter Optimization," *IEEE Journal on Selected Topics on Signal Processing, Special Issue on Compact Deep Neural Networks with Industrial Applications* (JSTSP-CDNN), vol. 14, no.4, pp. 609-622, May 2020.

CARNEGIE MELLON UNIVERSITY

[J49] I. Apostolopoulou and D. Marculescu, "Tractable Learning and Inference for Large-Scale Probabilistic Boolean Networks," *IEEE Trans. on Neural Networks and Learning Systems*, vol.30, no.9, pp. 2720 – 2734, Jan. 2019.

[J48] B. Joardar, R. Kim, J.R. Doppa, P. Pande, D. Marculescu, R. Marculescu, "Learning-based Application-Agnostic 3D NoC Design for Heterogeneous Manycore Systems," *IEEE Trans. on Computers*, vol.68, no.6, pp. 852 – 866, June 2019.

[J47] R. Ding, Z. Liu, R.D. Blanton, and D. Marculescu, "Lightening the Load with Highly Accurate Storage-and Energy-Efficient LightNNs," *ACM Transactions on Reconfigurable Technology and Systems*, vol.11, no.3, art.no.17, Dec. 2018.

[J46] Z. Chen, D. Stamoulis, and D. Marculescu, "Profit: Priority and Power/Performance Optimization for Many-core Systems," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol.37, no.10, pp. 2064-2075, Oct. 2018.

[J45] R. Kim, J.R. Doppa, P.P. Pande, D. Marculescu, and R. Marculescu, "Machine Learning and Manycore Systems Design: A Serendipitous Symbiosis," in *IEEE Computer*, vol.51, no.7, pp. 66-77, July 2018.

[J44] W. Choi, K. Duraisamy, R. Kim, J. Doppa, P. Pande, D. Marculescu, and R. Marculescu, "On-Chip Communication Network for Efficient Training of Deep Convolutional Networks on Heterogeneous Manycore Systems," *IEEE Trans. on Computers*, vol.67, no.5, pp.672-686, May 2018.

[J43] E. Cai and D. Marculescu, "Temperature Effect Inversion-Aware Power-Performance Optimization for FinFET-Based Multi-Core Systems," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol.36, no.11, pp. 1897-1910, Nov. 2017.

[J42] W. Choi, R. Kim, Z. Chen, P. Pande, J. Doppa, D. Marculescu, and R. Marculescu, "Imitation Learning for Dynamic VFI Control in Large-Scale Manycore Systems," *IEEE Trans. on Very Large Scale Integrated (VLSI) Circuits*, vol.25, no.9, pp. 2458-2471, Sept. 2017.

[J41] Y. Turakhia, G. Liu, S. Garg, and D. Marculescu, "Thread Progress Equalization: Dynamically Adaptive Power and Performance Optimization of Multi-threaded Applications," *IEEE Trans. on Computers*, vol.66, no.4, pp. 731-744, April 2017.

[J40] E. Cai, D.-C. Juan, S. Garg, J. Park, and D. Marculescu, "Learning-Based Power/Performance Optimization for Many-Core Systems with Extended-Range Voltage/Frequency Scaling," in *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol.35, no.8, pp. 1318–1331, Aug. 2016.

[J39] R. Kim, W. Choi, Z. Chen, P. Pande, D. Marculescu, and R. Marculescu, "Wireless NoC and Dynamic VFI Co-Design: Energy Efficiency without Performance Penalty," in *IEEE Trans. on Very Large Scale Integrated (VLSI) Circuits*, vol.24, no.7, pp. 2488–2501, July 2016. **(Best Paper Award)**

[J38] R. Kim, W. Choi, G. Liu, E. Mohandesi, P. Pande, D. Marculescu, and R. Marculescu, "Wireless NoC for VFI-Enabled Multicore Chip Design: Performance Evaluation and Design Trade-offs," in *IEEE Trans. on Computers*, vol.65, no.4, pp. 1323-1336, April 2016.

[J37] Z. Qian, D.-C. Juan, P. Bogdan, C.-Y. Tsui, D. Marculescu, and R. Marculescu, "A Support Vector Regression (SVR) based Latency Model for Network-on-Chip (NoC) Architectures," in *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol.35, no.3, pp. 471-484, March 2016.

[J36] J. Jiao, D.-C. Juan, D. Marculescu, and Y. Fu, "A two-level approximate model driven framework for characterizing Multi-Cell Upsets impacts on processors," in *Microelectronics Journal*, vol.48, no.2, pp.7-17, Feb.2016.

[J35] G. Liu, J. Park, and D. Marculescu, "Procrustes: Power Constrained Performance Improvement Using Extended Maximize-then-Swap Algorithm," in *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol.34, no.10, pp. 1664-1676, Oct. 2015.

[J34] J. Jiao, D.-C. Juan, D. Marculescu, and Y. Fu, "Exploiting Component Dependency for Accurate and Efficient Soft Error Analysis via Probabilistic Graphical Models," in *Microelectronics Reliability*, vol.55, no.1, pp.251-263, Jan. 2015.

[J33] D.-C. Juan, S. Garg, and D. Marculescu, "Statistical Peak Temperature Prediction and Thermal Yield Improvement for 3D Chip-Multiprocessors," in *ACM Trans. on Design Automation of Electronic Systems,* vol.19, no.4, art.no. 39, Aug. 2014.

[J32] K.-C. Wu and D. Marculescu, "Power-Planning-Aware Soft Error Hardening via Selective Voltage Assignment," in *IEEE Trans. on Very Large Scale Integrated (VLSI) Circuits*, vol.22, no.1, pp.136-145, Jan.2014.

[J31] S. Garg and D. Marculescu, "Mitigating the Impact of Process Variations on the Performance of 3D ICs," in *IEEE Trans. on Very Large Scale Integrated (VLSI) Circuits*, vol.21, no.10, Oct.2013.

[J30] K.-C. Wu and D. Marculescu, "A Low-Cost, Systematic Methodology for Soft Error Robustness of Logic Circuits," in *IEEE Trans. on Very Large Scale Integrated (VLSI) Circuits*, vol.21, no.2, pp. 367-379, Feb. 2013.

[J29] S. Garg and D. Marculescu, "Addressing Process Variations at the Microarchitecture and System Level," *Foundations and Trends in EDA*, vol.6, no.3, pp. 217-291, 2013.

[J28] S. Garg, D. Marculescu, and R. Marculescu, "Technology-driven Limits on Run-time Power Management Algorithms for Multi-processor Systems on Chip," in *ACM Journal on Emerging Technologies in Computing Systems*, vol.8, no.4, art.no.28, Oct. 2012.

[J27] S. Garg and D. Marculescu, "System-Level Leakage Variability Mitigation for MPSoC Platforms Using Body-Bias Islands," in *IEEE Trans. on Very Large Scale Integrated (VLSI) Circuits*, vol.20, no.12, pp.2289-2310, Dec. 2012.

[J26] S. Herbert, S. Garg, and D. Marculescu, "Exploiting Process Variability in Voltage/Frequency Control," in *IEEE Trans. on Very Large Scale Integrated (VLSI) Circuits*, vol.20, no.8, pp.1392-1404, Aug. 2012.

[J25] S. Garg and D. Marculescu, "On the Impact of Manufacturing Process Variations on the Lifetime of Sensor Networks," in *ACM Trans. on Embedded Computing Systems*, vol.11, no.2, article 33, pp.33:1-33:13, July 2012.

[J24] N. Miskov-Zivanov and D. Marculescu, "Multiple Transient Faults in Combinational and Sequential Circuits: A Systematic Approach," *in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol.29, no.10, pp.1614-1627, Oct. 2010.

[J23] S. Herbert and D. Marculescu, "Mitigating the Impact of Variability on Chip-Multiprocessor Power and Performance," in *IEEE Trans. on VLSI Systems*, vol.17, no.10, pp.1520-1533, Oct. 2009.

[J22] U.Y. Ogras, R. Marculescu, and D. Marculescu, E.-G. Jung, "Design and Management of Voltage-Frequency Island Partitioned Networks-on-Chip," in *IEEE Trans. on VLSI Systems*, vol.17, no.3, pp. 330-341, March 2009. (Special Section on Networks-on-Chip; **Best Paper Award)**

[J21] P. Choudhary and D. Marculescu, "Power Management of Voltage/Frequency Island-Based Systems Using Hardware Based Methods," in *IEEE Trans. on VLSI Systems*, vol.17, no.3, pp. 427-438, March 2009.

[J20] S. Garg and D. Marculescu, "System Level Throughput Analysis for Process Variation Adaptive Multiple Voltage-Frequency Island Designs," in *ACM Trans. on Design Automation of Electronic Systems*, vol.13, No.4, pp. 1-25, Sept. 2008.

[J19] N. Miskov-Zivanov and D. Marculescu, "Modeling and Optimization for Soft Error Reliability of Sequential Circuits," in *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol.27, No.5, pp. 803-816, May 2008.

[J18] D. Marculescu and S. Garg, "Process-Driven Variability Analysis for Single and Multiple Voltage-Frequency Island, Latency-Constrained Systems," in *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol.27, No.5, pp. 893-905, May 2008.

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[C40] N. Miskov-Zivanov and D. Marculescu, "MARS-C: Modeling, Analysis and Reduction of Soft Errors in Combinational Circuits," in *Proc. ACM/IEEE Design Automation Conference* (DAC), San Francisco, CA, June 2006.

[C39] C.-H. Chang and D. Marculescu, "Design and Analysis of a Low Power VLIW DSP Core," in *Proc. IEEE Computer Society Annual Symposium on VLSI* (ISVLSI), Karlsruhe, Germany, March 2006.

[C38] K. Niyogi and D. Marculescu, "System Level Power and Performance Modeling of GALS Point-to-point Communication Interfaces," in *Proc. ACM/IEEE Intl. Symposium on Low Power Electronics and Design* (ISLPED), San Diego, CA, Aug. 2005.

[C37] D. Marculescu and E. Talpes, "Variability and Energy Awareness: A Microarchitecture-Level Perspective," in *ACM/IEEE Design Automation Conference* (DAC), Anaheim, CA, June 2005.

[C36] E. Talpes and D. Marculescu, "Increased Scalability and Power Efficiency through Multiple Speed Pipelines," in *Proc. ACM Intl. Symposium on Computer Architecture* (ISCA), Madison, WI, June 2005.

[C35] D. Marculescu, "Energy Bounds for Fault-Tolerant Nanoscale Designs," in *Proc. IEEE Design, Automation and Test in Europe* (DATE), Munich, Germany, March 2005. **(Paper nominated for *Best Paper Award*)**

[C34] K. Niyogi and D. Marculescu, "Speed and Voltage Selection for GALS Systems Based on Voltage/Frequency Islands," in *IEEE/ACM Asian-South Pacific Design Automation Conference* (ASPDAC), Shanghai, China, Jan. 2005. **(*Best Paper Award*)**

[C33] R. Marculescu, D. Marculescu, and L. Pileggi, "Toward an Integrated Design Methodology for Fault-Tolerant, Multiple Clock/Voltage Integrated Systems," in *Proc. IEEE Intl. Conference on Computer Design* (ICCD), San Jose, CA, October 2004. **(Invited paper)**

[C32] D. Marculescu, "Application Adaptive Energy Efficient Clustered Architectures," in *Proc. ACM/IEEE Intl. Symposium on Low Power Electronics and Design* (ISLPED), Newport Beach, CA, Aug. 2004.

[C31] E. Talpes and D. Marculescu, "Impact of Technology Scaling on Energy Aware Execution Cache-based Microarchitectures," in *Proc. ACM/IEEE Intl. Symposium on Low Power Electronics and Design* (ISLPED), Newport Beach, CA, Aug. 2004.

[C30] P. Stanley-Marbell and D. Marculescu, "Local Decisions and Triggering Mechanisms for Adaptive Fault-Tolerance," in *Proc. IEEE Design, Automation and Test in Europe Conf.* (DATE), Paris, France, Feb. 2004.

[C29] V.S.P. Rapaka, E. Talpes, and D. Marculescu, "Mixed-Clock Issue Queue Design for Energy Aware, High-Performance Cores," in *Proc. IEEE/ACM Asian-South Pacific Design Automation Conference* (ASPDAC), Yokohama, Japan, Jan. 2004.

[C28] P. Stanley-Marbell and D. Marculescu, "Dynamic Fault-Tolerance and Metrics for Battery Powered, Failure-Prone Systems," in *Proc. IEEE/ACM Intl. Conference on Computer-Aided Design* (ICCAD), San Jose, CA, Nov. 2003.

[C27] D. Marculescu, N. H. Zamora, P. Stanley-Marbell, and R. Marculescu, "Fault-Tolerant Techniques for Ambient Intelligent Distributed Systems," in *Proc. IEEE/ACM Intl. Conference on Computer-Aided Design* (ICCAD), San Jose, CA, Nov. 2003.

[C26] V.S.P. Rapaka and D. Marculescu, "A Mixed-Clock Issue Queue Design for Globally Asynchronous, Locally Synchronous Processor Cores," in *Proc. ACM/IEEE Intl. Symposium on Low Power Electronics and Design* (ISLPED), Seoul, South Korea, Aug. 2003.

[C25] E. Talpes and D. Marculescu, "A Critical Analysis of Application-Adaptive Multiple Clock Processors," in *Proc. ACM/IEEE Intl. Symposium on Low Power Electronics and Design* (ISLPED), Seoul, South Korea, Aug. 2003.

[C24] M. Lindwer, D. Marculescu, T. Basten, R. Zimmermann, R. Marculescu, S. Jung, and E. Cantatore, "Ambient Intelligence Visions and Achievements: Linking Abstract Ideas to Real-World Concepts," in *IEEE Design, Automation and Test in Europe Conf.* (DATE), Munich, Germany, March 2003. (**Hot topic session**)

[C23] V.S.P. Rapaka and D. Marculescu, "Pre-characterization Free Efficient Power/Performance Analysis of Embedded and General Purpose Software Applications," in *Proc. IEEE Design, Automation and Test in Europe Conf.* (DATE), Munich, Germany, March 2003.

[C22] S.W. Haga, N. Reeves, R. Barua, and D. Marculescu, "Dynamic Functional Unit Assignment for Low Power," in *Proc. IEEE Design, Automation and Test in Europe Conf.* (DATE), Munich, Germany, March 2003.

[C21] A. Iyer and D. Marculescu, "Power Efficiency of Voltage Scaling in Multiple Clock, Multiple Voltage Cores," in *Proc. IEEE/ACM Intl. Conference on Computer Aided Design* (ICCAD), San Jose, CA, Nov. 2002.

[C20] D. Marculescu, R. Marculescu, and P. Khosla, "Challenges and Opportunities in E-textile Analysis, Modeling and Optimization," in *Proc. ACM/IEEE Design Automation Conference* (DAC), Anaheim, CA, June 2002. **(Special session)**

[C19] A. Iyer and D. Marculescu, "Power Performance Evaluation of Globally Asynchronous, Locally Synchronous Processors," in *Proc. IEEE Intl. Symposium on Computer Architecture* (ISCA), Anchorage, AK, May 2002.

[C18] R. Marculescu and D. Marculescu, "Is Q=MC^2? (On the Relationship between the Model of Colloidal Computing and Quality in Electronic Design)," in *Proc. ACM Intl. Symposium on Quality in Electronic Design* (ISQED), March 2002. **(Invited paper)**

[C17] D. Marculescu and A. Iyer, "Application-Driven Processor Design Exploration for Power-Performance Trade-off Analysis," in *Proc. IEEE/ACM Intl. Conference on Computer Aided Design* (ICCAD), November 2001.

[C16] E. Talpes and D. Marculescu, "Power Reduction through Work Reuse," in *Proc. ACM Intl. Symposium on Low Power Electronics and Design* (ISLPED), August 2001.

[C15] A. Iyer and D. Marculescu, "Power Aware Microarchitecture Resource Scaling," in *Proc. of IEEE Design, Automation and Test in Europe Conf.* (DATE), Munich, Germany, March 2001.

[C14] D. Marculescu, "Profile-Driven Code Execution for Low Power Dissipation," in *Proc. ACM Intl. Symp. on Low Power Electronics and Design* (ISLPED), Rapallo/Portofino Coast, Italy, July 2000.

UNIVERSITY OF MARYLAND, COLLEGE PARK

[C13] D. Marculescu and R. Marculescu, "Information-Theoretic Bounds for Switching Activity Analysis in Finite-State Machines under Temporally Correlated Inputs," in *Proc. 33rd Asilomar Conference on Signals, Systems, and Computers* (ASILOMAR), October 1999. **(Invited paper)**

[C12] R. Marculescu, D. Marculescu, and M. Pedram, "Non-Stationary Effects in Trace-Driven Power Analysis," in *Proc. ACM Intl. Symp. on Low Power Electronics and Design* (ISLPED), San Diego, CA, August 1999.

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[C11] D. Marculescu, R. Marculescu, and M. Pedram, "Theoretical Bounds for Switching Activity Analysis in Finite-State Machines," in *Proc. ACM Intl. Symp. on Low Power Electronics and Design* (ISLPED), Monterey, CA, August 1998.

[C10] D. Marculescu, R. Marculescu, and M. Pedram, "Trace-Driven Steady-State Probability Estimation in FSMs with Application to Power Estimation," in *Proc. ACM Design, Automation and Test in Europe Conf.* (DATE), Paris, France, February 1998.

[C9] R Marculescu, D. Marculescu, and M. Pedram, "Block Entropy and High-Order Temporal Effects in Composite Sequence Compaction for Finite-State Machines," in *Proc. ACM Intl. Symp. on Low Power Electronics and Design* (ISLPED), Monterey, CA, August 1997.

[C8] R. Marculescu, D. Marculescu, and M. Pedram, "Hierarchical Sequence Compaction for Power Estimation," in *Proc. ACM/IEEE Design Automation Conf.* (DAC), Anaheim, CA, June 1997. (**Paper nominated for *Best Paper Award***)

[C7] D. Marculescu, R. Marculescu, and M. Pedram, "Sequence Compaction for Probabilistic Analysis of Finite-State Machines," in *Proc. ACM/IEEE Design Automation Conf.* (DAC), Anaheim, CA, June 1997.

[C6] R. Marculescu, D. Marculescu, and M. Pedram, "Adaptive Models for Input Data Compaction for Power Simulators," in *Proc. ACM Asia and South-Pacific Design Automation Conf.* (ASPDAC), Japan, January 1997.

[C5] D. Marculescu, R. Marculescu, and M. Pedram, "Stochastic Sequential Machine Synthesis Targeting Constrained Sequence Generation," in *Proc. ACM/IEEE Design Automation Conf.* (DAC), Las Vegas, NV, June 1996. (**Paper Nominated for *Best Paper Award***)

[C4] C.-Y.Tsui, R. Marculescu, D. Marculescu, and M. Pedram, "Reducing the Run-Time of Simulation-Based Power Estimation by Vector Compaction," in Proc. *ACM/IEEE Design Automation Conf.* (DAC), Las Vegas, NV, June 1996.

[C3] D. Marculescu, R. Marculescu, and M. Pedram, "Information Theoretic Measures for Energy Consumption at Register Transfer Level," in *Proc. ACM Intl. Symposium. on Low Power Design* (ISLPED), Dana Point, CA, April 1995.

[C2] R. Marculescu, D. Marculescu, and M. Pedram, "Efficient Power Estimation for Highly Correlated Input Streams," in *Proc. of ACM/IEEE Design Automation Conf.* (DAC), San Francisco, CA, June 1995.

[C1] R. Marculescu, D. Marculescu, and M. Pedram, "Switching Activity Analysis Considering Spatiotemporal Correlations," in *Proc. IEEE/ACM Intl. Conf. on Computer Aided Design* (ICCAD), San Jose, CA, November 1994.

PEER REVIEWED PAPERS AND PRESENTATIONS WITHOUT PUBLISHED PROCEEDINGS

THE UNIVERSITY OF TEXAS AT AUSTIN

[W29] A. Inci, E. Bolotin, Y. Fu, G. Dalal, S. Mannor, D. Nellans, and D. Marculescu, "The Architectural Implications of Distributed Reinforcement Learning on CPU-GPU Systems," in *6th Workshop on Energy Efficient Machine Learning and Cognitive Computing* (EMC^2), Virtual, Dec. 2020.

[W28] T.-W. Chin, C. Zhang, and D. Marculescu, "Improving the Adversarial Robustness of Transfer Learning via Noisy Feature Distillation," in *Proc. KDD Workshop on Adversarial Learning Methods for Machine Learning and Data Mining* (AdvML), in conjunction with *ACM SIGKDD Conference on Knowledge Discovery and Data Mining* (KDD), Virtual, August 2020.

[W27] T.-W. Chin, A.S. Morcos, D. Marculescu, "PareCO: Pareto-aware Channel Optimization for Slimmable Neural Networks," in *Proc. KDD Workshop on Adversarial Learning Methods for Machine Learning and Data Mining* (AdvML), in conjunction with *ACM SIGKDD Conference on Knowledge Discovery and Data Mining* (KDD), Virtual, August 2020.

[W26] T.-W. Chin, A.S. Morcos, D. Marculescu, "PareCO: Pareto-aware Channel Optimization for Slimmable Neural Networks," in *Proc. ICML Workshop on Challenges in Deploying and Monitoring Machine Learning Systems* (DMMLSys), in conjunction with *International Conference on Machine Learning* (ICML), Virtual (Vienna, Austria), July 2020.

[W25] T.-W. Chin, A.S. Morcos, D. Marculescu, "PareCO: Pareto-aware Channel Optimization for Slimmable Neural Networks," in *Proc. ICML Workshop on Real World Experiment Design and Active Learning* (RealML), in conjunction with *International Conference on Machine Learning* (ICML), Virtual (Vienna, Austria), July 2020.

[W24] T.-W. Chin, R. Ding, C. Zhang, and D. Marculescu, "Towards Efficient Model Compression via Learned Global Ranking," in *Proc. IEEE CVPR Workshop on Fair, Data Efficient and Trusted Computer Vision*, in conjunction with *IEEE Conference on Computer Vision and Pattern Recognition* (CVPR), Virtual (Seattle, WA), June 2020.

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[W23] D. Stamoulis, R. Ding, D. Wang, D. Lymberopoulos, B. Priyantha, J. Liu, D. Marculescu, "Single-Path NAS: Device-Aware Efficient ConvNet Design," in *Proc. Joint Workshop on On-Device Machine Learning and Compact Deep Neural Network Representations for Industrial Applications* (ODML-CDNNRIA) in conjunction with the *International Conference on Machine Learning* (ICML), June 2019. (oral, **Best Paper Award**)

[W22] T.-W. Chin, C. Zhang, D. Marculescu, "Layer-compensated Pruning for Resource-constrained Convolutional Neural Networks," in *Proc. Workshop on Machine Learning on the Phone and other Consumer Devices* (MLPCD^2) in conjunction with the *Conference on Neural Information Processing Systems* (NeurIPS), Dec. 2018.

[W21] R. Ding, Z. Liu, T.-W. Chin, D. Marculescu, S. Blanton, "Differentiable Training for Hardware Efficient LightNNs," in *Proc. Workshop on Compact Deep Neural Networks with Industrial Applications* (CDNNIA) in conjunction with the *Conference on Neural Information Processing Systems* (NeurIPS), Dec. 2018.

[W20] A. Inci, D. Marculescu, "Solving the Non-Volatile Memory Conundrum for Deep Learning Workloads ," in *Proc. Workshop on Architectures and Systems for Big Data* (ASBD) in conjunction with *IEEE/ACM Intl. Symposium on Computer Architecture* (ISCA), Los Angeles, CA, June 2018.

[W19] E. Cai, I. Apostolopoulou, P. Ranjan, P. Pan, M. Wuebbens, and D. Marculescu, "Efficient Data-Driven Model Learning for Dynamical Systems," in *Intelligent Systems for Molecular Biology Conference* (ISMB) *Late Breaking Research*, Orlando, FL, July 2016.

[W18] Y. Turakhia, S. Garg, and D. Marculescu, "Thread Progress Equalization: Dynamically Adaptive Power and Performance Optimization of Multi-threaded Applications," in *IEEE Intl. Conference on Parallel Architectures and Compilation Techniques* (PACT), San Francisco, CA, Oct. 2015.

[W17] J. Jiao, Y. Fu, D.-C. Juan, and D. Marculescu, "Exploiting Component Dependency for Accurate Architectural-Level Soft Error Analysis," in *Work-in Progress, ACM/IEEE Design Automation Conference* (DAC), San Francisco, CA, June 2014.

[W16] N. Miskov-Zivanov, A. Bresticker, D. Krishnaswamy, S. Venkatakrishnan, D. Marculescu, and J. Faeder, "Biological Network Emulation in FPGA," in *Intl. Workshop on Bio-Design Automation* (IWBDA), San Diego, CA, June 2011.

[W15] M.-C. Lee, Y. Shi, Y.-G. Chen, S.-C. Chang, and D. Marculescu, "Efficient Wake-Up Scheduling for Multi-Core Systems," in *ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems* (TAU), Santa Barbara, CA, April 2011.

[W14] N. Miskov-Zivanov, D. Krishnaswamy, S. Venkataraman, A. Bresticker, D. Marculescu, and J.R. Faeder, "Emulation of Biological Networks in Reconfigurable Hardware," in *CSHL*, Computational Biology, Cold Spring Harbor, NY, April 2011.

[W13] P. Stanley-Marbell and D. Marculescu, "A Programming Model and Language Implementation for Concurrent Failure-Prone Hardware," in *Workshop on Programming Models for Ubiquitous Parallelism* (PMUP), in conjunction with *ACM/IEEE Intl. Conf. on Parallel Architectures and Compilation Techniques* (PACT), Oct.2006.

[W12] P. Stanley-Marbell and D. Marculescu, "Full-System Simulation for Sensor Networks," in *ACM Conference on Embedded Networked Sensor Systems* (SenSys), San Diego, Nov. 2005. (demo)

[W11] P. Stanley-Marbell and D. Marculescu, "Cycle-Accurate Full-System Simulation for Sensor Networks," in *Intl. Conference on Mobile Systems, Applications, and Services* (MobiSys), Seattle, June 2005. (demo)

[W10] N. Miskov-Zivanov and D. Marculescu, "Circuit Reliability Analysis Using Symbolic Techniques," in *IEEE/ACM Intl. Workshop on Logic and Synthesis* (IWLS), Lake Arrowhead, CA, June 2005.

[W9] S. Hassoun and D. Marculescu, "Toward GALS Design Methodologies," in *Workshop on Formal Methods for GALS Design* (FMGALS), in conjunction with *Formal Methods in Europe Conference* (FME), Pisa, Italy, Sep. 2003.

[W8] P. Stanley-Marbell and D. Marculescu, "Programming Crystalline Hardware," in *Workshop on Non-Silicon Computing* (NSC), in conjunction with *Intl. Symp. on Computer Architecture* (ISCA), San Diego, June 2003.

[W7] P. Stanley-Marbell and D. Marculescu, "Dynamic Fault-Tolerance Management in Failure-Prone and Battery-Powered Systems," in *IEEE/ACM Intl. Workshop on Logic and Synthesis* (IWLS), Laguna Beach, CA, May 2003.

[W6] N.H. Zamora, P. Stanley-Marbell, R. Marculescu, and D. Marculescu, "PreCopying: An Improved Code Migration Technique for Future Fault-Tolerant Electronic Textiles," in *Proc. Workshop on Modeling, Analysis and Middleware Support for Electronic Textiles* (MAMSET), in conjunction with *ACM Intl. Conference on Architectural Support for Programming Languages and Operating Systems* (ASPLOS), San Jose, CA, Oct. 2002.

[W5] D. Marculescu, R. Marculescu, and P. Khosla, "Challenges and Opportunities in E-textile Analysis, Modeling and Optimization," in *International Conference on Interactive Textiles for the Warrior*, Boston, MA, July 2002. **(Invited poster)**

[W4] A. Iyer and D. Marculescu, "Run-time Scaling of Microarchitecture Resources in a Processor for Energy Savings," in *Proc. KoolChips Workshop* (KOOL), in conjunction with *International Symposium on Microarchitecture* (MICRO), Monterey, Dec. 2000.

[W3] D. Marculescu, "Power Efficient Processors Using Multiple Supply Voltages," in *Proc. Workshop on Compilers and Operating Systems for Low Power* (COLP), in conjunction with *International Conference on Parallel Architectures and Compilation Techniques* (PACT), Philadelphia, Oct. 2000.

[W2] D. Marculescu, "On the Use of Microarchitecture-Driven Dynamic Voltage Scaling," in *Proc. Workshop on Complexity-Effective Design* (WCED), in conjunction with *Intl. Symp. on Computer Architecture* (ISCA), Vancouver, BC, June 2000.

UNIVERSITY OF SOUTHERN CALIFORNIA

[W1] D. Marculescu, R. Marculescu, and M. Pedram, "High-Order Temporal Effects in Finite State Machine Analysis," in *Intl. Workshop. on Logic Synthesis* (IWLS), Lake Tahoe, CA, May 1997.

TECHNICAL REPORTS, PROFESSIONAL MAGAZINES, AND REVIEW ARTICLES

CARNEGIE MELLON UNIVERSITY

[T9] Z. Chen, and D. Marculescu, "Priority-Aware Near-Optimal Scheduling for Heterogeneous Multi-Core Systems with Specialized Accelerators," https://arxiv.org/abs/1712.03246. CoRR 2017.

[T8] Z. Chen, and D. Marculescu, "Task Scheduling for Heterogeneous Multicore Systems," http://arxiv.org/abs/1712.03209. CoRR 2017.

[T7] R.I. Bahar, A.K. Jones, S. Katkoori, P.H. Madden, D. Marculescu, and I. Markov, "Workshops on Extreme Scale Design Automation (ESDA) Challenges and Opportunities for 2025 and Beyond," *Computing Community Consortium* (CCC), 2014.

[T6] D. Marculescu and C. Das, "Editorial to special section on networks on chip: Architecture, tools, and methodologies," in *ACM Transactions on Design Automation of Electronic Systems* (TODAES), vol.18, no.4, art. no. 45, Oct. 2013.

[T5] D. Marculescu and P. Li, "Guest Editorial Special Section on PAR-CAD: Parallel CAD Algorithms and CAD for Parallel Architectures/Systems," in *IEEE Trans. on CAD of Integrated Circuits and Systems* vol.31, no.1, pp.7-8, Jan.2012.

[T4] D. Marculescu and J. Henkel, "Guest Editors' introduction: Special section on low power electronics and design," in *IEEE Trans on VLSI Systems*, 2008.

[T3] D. Marculescu, R. Marculescu, S. Park, and S. Jayaraman, "Ready to Ware," in *IEEE Spectrum*, vol.40, no.10, pp. 28-32, Dec. 2003.

[T2] P. Bose, D.H. Albonesi, and D. Marculescu, "Guest editors' introduction: Power and complexity aware design," in *IEEE Micro*, vol.23, no.5, pp. 8-11, Sept.-Oct. 2003.

[T1] D. Marculescu, "E-textiles: toward computational clothing," in *IEEE Pervasive Computing*, vol.2, no.1, pp. 89-95, Jan-Mar. 2003.

PATENTS

CARNEGIE MELLON UNIVERSITY

[P1] "Flexible, Lightweight Quantized Deep Neural Networks," (with Ruizhou Ding, Zeye Liu, Ting-Wu Chin, R.D. Shawn Blanton), United States Provisional Patent Application No. 62/921,121, filed May 31, 2019.

FUNDED PROPOSALS AND GRANTS (26 as PI; $16.1M total; $13.4M at home institution)

THE UNIVERSITY OF TEXAS AT AUSTIN

[G39] "Efficient Object Detection for Resource-constrained Devices," PI[‡], Facebook Reality Labs, unrestricted gift, $75,000, Dec. 2019.

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[G38] "CSR: Small: ARTEMIS: Algorithm-hardware co-design for efficient machine learning systems," PI[‡], NSF (CNS), $500,000, 2018-2021.

[G37] "SHF: Small: Energy Efficient Learning on Chip with Quantized Representations," PI, NSF (CCF), $450,000, 2018-2021.

[G37] "Qualcomm Innovation Fellowship - Towards Efficient Hardware-Constrained Deep Learning," PI[‡], Qualcomm Technologies, Inc., $100,000, 2018-2019.

[G36] "Remanence Computing - System Development of Remanence Computer," co-PI, College of Engineering Moonshot Project, approx. $240,000, 2017-2019.

[G35] "Energy Efficient Heterogeneous Datacenter-on-Chip for Big Data Computing," co-PI, Army Research Office, $375,000, 2017-2020.

[G34] "NeTS: CSR: Medium: Collaborative Research: Wireless Datacenter-on-Chip (WiDoC): A New Paradigm for Big Data Computing," co-PI, NSF (CNS), $633,974, 2016-2019.

[G33] "SHF: NeTS: Medium: Collaborative Research: The Power of Less Wiring: Wireless NoC-enabled Voltage-Frequency Islands (VFIs) for Energy-Efficient Multicore Platforms," co-PI, NSF (CCF), $454,000, 2015-2018.

[G32] "AIMCancer: Automated Integration of Mechanisms in Cancer," co-PI, DARPA (I2O), $2,421,232, 2014-2017.

[G31] "ARC 'Future' Fellowship: Sustainability in Computing: A Holistic View," PI[‡], Australian Research Council, AU $868,144, 2013-2017 (deferred).

[‡] Sole PI.

[G30] "Collaborative Research: CyberSEES: Type 2: Climate-Aware Renewable Hydropower Generation and Disaster Avoidance," PI, National Science Foundation (CCF), $1,139,920 ($455,953 CMU portion), Sept. 2013-Aug.2016.

[G29] "Efficient Many-Core Reliability Modeling, Analysis, and Optimization," PI‡, Cisco, unrestricted gift, $100,000, Aug.2013-July 2014.

[G28] "SLIC: Statistical Learning in Silicon," Senior Personnel, National Science Foundation (CCF), $2,240,000, July 2013-June 2017.

[G27] "Enabling Extreme Power Efficiency in Multi-Core Systems," PI‡, Samsung, $120,000, Aug.2012-December 2013.

[G26] "Planning Grant: I/UCRC for Nexys: Next Generation Electronic System Design," PI, National Science Foundation, $14,500, April 2011-March 2012.

[G25] "Modeling and Mitigation of Aging-Induced Performance Degradation," PI‡, Cisco, unrestricted gift, $50,000, Nov.2011-Oct.2012.

[G24] "Distributed Control and Coordination for Massively Integrated Multicore Platforms," co-PI, National Science Foundation (CSR), $475,000, Sep.2011-Aug.2014.

[G23] "Advanced Dynamic Performance and Power Management for Many-Core Systems Using Reverse DVFS and Throughput-/Response Time-Constrained Control," PI‡, Intel Corp., unrestricted gift, $195,000, May 2011-April 2014.

[G22] "Soft Error Modeling and Analysis," PI‡, Cisco, unrestricted gift, $20,000, Sept.2010-Oct.2011.

[G21] "Process variation-aware modeling, analysis, and prevention of thermal attacks in many-core systems," PI‡, CyLab, $75,000, Sep.2010-Aug.2011.

[G20] "miliJoules for 1000 Cores: Energy Efficient NoC-Based Systems Using Voltage-Frequency Islands," co-PI, Semiconductor Research Corporation (System Design), $300,000, May 2008 – April 2011.

[G19] "Collaborative research: Cross-System Modeling and Management for Variation-Adaptive Computing," PI, National Science Foundation (CSR-EHS), $100,000, Aug. 2007 – Jul. 2009.

[G18] "Variability-Aware System Level Performance and Power Analysis," PI‡, National Science Foundation (CSR-SMA), $250,000, Sept. 2007 – Aug. 2010.

[G17] "Energy-Variability Interactions at Microarchitecture Level in 2D- and 3D-architectures," PI‡, National Science Foundation (CPA), $225,000, Sept. 2007 – Aug.2010.

[G16] "Malicious Fault-Immune Cryptographic Hardware Implementation," PI‡, CyLab, $75,000, Sep.2006-Aug.2007.

[G15] "High-Level Power Macromodeling and Estimation," PI‡, Intel, $120,000, April 2006 – March 2009, unrestricted gift.

[G14] "SGER: Analysis of Fault-Tolerant Nanoscale Designs," PI‡, National Science Foundation (SGER), $100,000, Sept. 2005 – Aug.2007.

[G13] "Power Analysis and Optimization of Voltage/Frequency-Island Based Designs," PI‡, Semiconductor Research Corporation (System Design), $306,000, May 2005 – April 2008.

[G12] "Fault-Tolerant Communication for Multiple-Clock/Voltage Integrated Systems," PI, Semiconductor Research Corporation (System Design), $646,436, Apr. 2004 – March 2007.

‡ Sole PI.

[G11] "SENSIBLE - Integrating SENSing and ProcessIng in ConformaBLE Substrates for Security Applications," PI‡, CyLab, $150,000, Sep.2004-Aug.2006.

[G10] "Securing Information Exchange within Partitioned Applications in Next Generation VLSI Systems," PI‡, C3S, $75,000, Sep.2003-Aug.2004.

[G9] "ITRI Lab at CMU: Security in Silicon," co-PI, ITRI, $2,000,000 ($280,000 individual portion), March 2003-April 2006.

[G8] "Modeling, Analysis and Self-Management of Electronic Textiles," PI, Semiconductor Research Corporation, CSR program, $40,000, Aug.2002-July 2003.

[G7] "COATNET: Colloidal Computing for Textile-Area Networks," PI, DARPA (ITO), $104,000, June 2002-May 2003.

[G6] "Colloidal-Computing: A New Paradigm for Energy Aware Computing," co-PI, Semiconductor Research Corporation (System Design), $370,624, June 2001-May 2004.

[G5] "Future Microarchitectures of Minimally Clocked Machines," co-PI, IBM Corp., $200,000, July 2001-May 2002.

[G4] "Communication Aware Dynamic Architectures for Computational Fabrics," PI, DARPA (ITO), $285,447, March 2001-April 2002.

[G3] Equipment Grant, Intel Corp., $17,940, Dec. 2000.

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[G2] "Software-Level Power Analysis and Optimization," PI‡, National Science Foundation Early Faculty Career Development Award, $260,000, June 2000-May 2004.

[G1] "Power Analysis and Scheduling for Energy-Efficient Wireless Embedded Systems," PI‡, Minta Martin Fund, University of Maryland, $35,055, Sept. 1998-Aug. 1999.

TUTORIALS, PANELS, TALKS, LECTURES, AND PODCASTS[1]

THE UNIVERSITY OF TEXAS AT AUSTIN

[L93] "Towards Million-fold Efficiency in AI," invited panelist, *6th Workshop on Energy Efficient Machine Learning and Cognitive Computing* (EMC^2), Virtual, December 2020.

[L92] "miliJoules for 1000 Inferences: Machine Learning Systems 'on the Cheap'," invited keynote at *IEEE System on a Chip Conference* (SOCC), Virtual, September 2020.

[L91] "Edge AI: Systems Design and ML for IoT Data Analytics" (with R. Marculescu, Umit Y. Ogras, K. Bhardwaj, D. Stamoulis), half-day tutorial at *ACM International Conference on Knowledge Discovery and Data Mining* (KDD), Virtual (San Diego, CA), August 2020.

[L90] "The Case for Hardware-ML Model Co-design with Diana Marculescu," invited podcast, *This Week in Machine Learning and Artificial Intelligence* (TWiMLAI), July 2020. https://twimlai.com/twiml-talk-391-the-case-for-hardware-ml-model-co-designwith-diana-marculescu/

[L89] "Putting the "Machine" Back in Machine Learning: The Case for Hardware-ML Model Co-design," Distinguished Lecture, Dept. of Electrical and Computer Engineering, Rice University, Virtual (Houston, TX), July 2020.
https://www.youtube.com/watch?v=oeYj1ElvwXU&ab_channel=RiceUECE

‡ Sole PI.

[1] Not including research review talks.

[L88] "When Climate Meets Machine Learning: The Case for Hardware-ML Model Co-design," invited talk, *Microsoft Research Faculty Summit*, Virtual (Seattle, WA), July 2020. https://www.youtube.com/watch?v=Y93_PMAKaxQ&ab_channel=MicrosoftResearch

[L87] "Putting the "Machine" Back in Machine Learning: The Case for Hardware-ML Model Co-design," keynote talk, *Joint Workshop on Efficient Deep Learning in Computer Vision* in conjunction with *IEEE Conference on Computer Vision and Pattern Recognition* (CVPR), Virtual (Seattle, WA), June 2020.

[L86] "Putting the "Machine" Back in Machine Learning: The Case for System Aware ML Design," keynote talk, *Machine Learning for Computer Architecture and Systems Workshop* in conjunction with *ACM International Symposium on Computer Architecture* (ISCA), Virtual, May 2020.

[L85] "Putting the "Machine" Back in Machine Learning: The Case for Hardware-ML Model Co-design," keynote talk, *1st On Device Intelligence Workshop* in conjunction with *3rd Conference on Machine Learning and Systems* (MLSys), Austin, TX, March 2020. https://www.youtube.com/watch?v=B5ftBvZxESU&ab_channel=On-DeviceIntelligenceWorkshop

[L84] "Putting the "Machine" Back in Machine Learning: The Case for Hardware-ML Model Co-design," invited talk, *2nd Workshop on Artificial Intelligence of Things* (AIoT) in conjunction with *34th AAAI Conference on Artificial Intelligence* (AAAI), New York, NY, Feb. 2020.

[L83] "Putting the "Machine" Back in Machine Learning: The Case for Hardware-ML Model Co-design," invited talk, *5th Workshop on Energy Efficient Machine Learning and Cognitive Computing* (EMC^2) in conjunction with *33rd Conference on Neural Information Processing Systems* (NeurIPS), Vancouver, Canada, Dec. 2019.

CARNEGIE MELLON UNIVERSITY

[L82] "Putting the "Machine" Back in Machine Learning: The Case for Hardware-ML Model Co-design," invited talk, Dept. of Electrical and Computer Engineering, Duke University, Durham, NC, September 2019.

[L81] "Hardware-Aware Machine Learning: Modeling and Optimization," special session, *IEEE/ACM Intl. Conference on Computer-Aided Design* (ICCAD), San Diego, CA, Nov. 2018.

[L80] "Hardware-Aware Machine Learning: Modeling and Optimization," speaker, *Machine Learning in Science and Engineering Conference* (MLSE), Pittsburgh, PA, June 2018.

[L79] "LightNN: Filling the Gap between Conventional Deep Neural Networks and Binarized Networks," speaker, *CMU Machine Learning Symposium*, May 10, 2017.

[L78] "Data-Driven Modeling and In Silico Simulation of Cell Signaling Pathways," special session, *Intelligent Systems for Molecular Biology Conference* (ISMB), Orlando, FL, July 2016. https://www.youtube.com/watch?v=7uo6_zmXJEw&ab_channel=ISCB

[L77] "Sustainability in Computing and Beyond: A journey from nature-inspired computing to nature and back," invited presentation for the LEAP@CMU program, June 22, 2016.

[L76] "Balancing the Effects of Process Variations, Aging, and Application Workload in Multi-Core Systems," keynote talk, *Workshop on System-to-Silicon Performance Modeling and Analysis (Power, Temperature and Reliability),* co-located with *ACM/IEEE Design Automation Conference*, Austin, TX, June 2016.

[L75] "The Quest for Energy Aware Computing," IEEE Distinguished Seminar, School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA, April 2016.

[L74] "Performance and Energy: Friends or Foes," invited panelist, *International Conference on Green and Sustainable Computing*, Las Vegas, NV, December 2015.

[L73] "The Quest for Energy Aware Computing," invited talk, *International Conference on Green and Sustainable Computing*, Las Vegas, NV, December 2015.

[L72] "The Quest for Energy Aware Computing," invited seminar, Yale University, Dept. of Electrical Engineering, New Haven, CT, December 2015.

[L71] "The Quest for Energy Aware Computing," invited seminar, New York University, Dept. of Electrical and Computer Engineering, New York, NY, December 2015.

[L70] "Towards A Holistic Modeling of River Networks," special session, in *INFORMS Annual Meeting*, Philadelphia, PA, Nov. 2015**.**

[L69] "The Quest for Energy Aware Computing," invited seminar, Apple Corp., October 2015.

[L68] "Sustainability in Computing and Beyond," invited presentation for the LEAP@CMU program, June 23, 2015.

[L67] "Understanding and Using Heterogeneity for High Performance, Energy Efficient Computing," invited talk, *IEEE Intl. Conference on Control Systems and Computer Science*, Bucharest, Romania, June 2015.

[L66] "The Quest for Energy Aware Computing," DSN-I seminar, Carnegie Mellon University, Pittsburgh, PA, May 2015.

[L65] "Sustainability in Computing and Beyond," keynote talk, *CRA-W/CDC Discipline Specific Workshop on Diversity in Design Automation*, co-located with *ACM/IEEE Design Automation Conference*, San Francisco, CA, June 2014.

[L64] "Implicit and Explicit Heterogeneity in Power Aware High Performance Multi-Core Systems," Intel Corp., Hillsboro, OR, Jan. 2014.

[L63] "Power-Performance Management for Multi-Core Systems," Intel Corp., Austin, TX, June 2013.

[L64] "Achieving Sustainable Computing Through Energy- and Variability-Aware System Design," *Design Automation Summer School*, Austin, TX, June 2013.

[L63] "Power-Performance Management for Multi-Core Systems," Intel Corp., Hillsboro, OR, Jan. 2013.

[L62] "Achieving Sustainable Computing Through Energy- and Reliability-Aware System Design," University of Southern California, Los Angeles, CA, November 2012.

[L61] "Power-aware Performance Increase via Core/Uncore Reverse DVFS Control for Chip-Multiprocessors," Intel Corp., Hillsboro, OR, June 2012.

[L60] "Achieving Sustainability in Electronic System Design and Beyond," Technische Universitaet Muenchen, Germany, May 2012.

[L59] "Energy Aware Computing: Within and Beyond the 'Silicon Box'," Texas Instruments, April 2012.

[L58] "System Level Power Management for Many-Core Systems: Enabling Performance Increase via Variation-aware Reverse DVFS Control," Intel Corp., Hillsboro, OR, April 2012.

[L57] "System Level Power Management for Many-Core Systems: Enabling Performance Increase via Variation-aware Reverse DVFS Control," Intel Corp., Hillsboro, OR, Jan. 2012.

[L56] "Achieving Sustainability Through Energy and Reliability Aware System Design," Columbia University, Dept. of Computer Science, New York, NY, Nov.2011.

[L55] "Achieving Sustainability Through Energy and Reliability Aware System Design," Massachusetts Institute of Technology, Cambridge, MA, Oct.2011.

[L54] "Energy Aware Computing: Beyond the 'Silicon Box'," Bell Labs @ CMU Workshop, Pittsburgh, PA, Sept. 2011.

[L53] "Process Variation Aware Performance Modeling and Dynamic Power Management for Multi-Core Systems," University College Cork, Ireland, July 2011.

[L52] "Symbolic Reliability Modeling, Analysis, and Optimization of Digital Systems," keynote talk, Design Reliability and Variability Workshop (DRVW), in conjunction with *IEEE VLSI Test Symposium* (VTS), Dana Point, CA, June 2011.

[L51] "Cost-Effective, "Just-in-Logic" Aging-Aware Fault Detection, Isolation, and Repair," Cisco, October 2010.

[L50] "Symbolic Reliability Modeling, Analysis, and Optimization of Digital Systems," SanDisk, September 2010.

[L52] "Process Variation-Aware 3D Thermal Modeling and Management for NoC Designs," CEA-LETI, July 2010.

[L51] "Aging Modeling and Optimization in Digital Systems," CEA-LETI, July 2010.

[L51] "Symbolic Reliability Modeling, Analysis, and Optimization of Digital Systems," Universite Joseph Fourier, July 2010.

[L50] "Process Variation Aware Performance Modeling and Dynamic Power Management for Multi-Core Systems," Universite Joseph Fourier, July 2010.

[L49] "Symbolic Reliability Modeling, Analysis, and Optimization of Digital Systems," Cisco, May 2010 and June 2010.

[L48] "Multi-domain Processors: Challenges, Design Methods, and Recent Developments," (with R. Marculescu, R. Ginosar, S. Rusu), half-day tutorial at *ACM International Symposium on Computer Architecture*, St. Malo, France, June 2010.

[L47] "Process Variation-Aware Dynamic Power Management for Multi-Core Systems," Intel Corp., Oct. 2009.

[L46] "System Level Process Variation Modeling and Mitigation," Dept. of Computer Science, Universitat Politècnica de Catalunya, Barcelona, Spain, July 2009.

[L45] "System Level Process Variation Modeling and Mitigation," Technische Universitaet Muenchen, Germany, June 2009.

[L44] "System Level Process Variation Modeling and Mitigation," Dept. of Computer Science, Universidad Complutense de Madrid, Madrid, Spain, April 2009.

[L43] "DFM Revisited: A Comprehensive Analysis of Variability at all Levels of Abstraction," (with Lars Liebman, Praveen Elakkumanan, Puneet Gupta, Dureseti Chidambarrao, Nagesh Tamarapalli), full-day tutorial at *ACM/IEEE Design Automation Conference*, Anaheim, CA, June 2008.

[L42] "Design Variability: Challenges and Solutions at Microarchitecture-Architecture Level," (with Sani Nassif) half-day tutorial at *IEEE/ACM Design, Automation, and Test in Europe Conference*, Munich, Germany, March 2008.

[L41] "System Level Process Variation Modeling and Mitigation," Dept. of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Feb. 2008.

[L40] "Tutorial on The Sunflower Toolsuite," (with Phillip Stanley-Marbell), full-day tutorial at *Intl. Conf. on High Performance Embedded Architectures & Compilers*, Gotteborg, Sweden, Jan. 2008.

[L39] "Power Analysis and Optimization of Voltage-Frequency Island Based Designs," Technology Transfer E-Workshop, Semiconductor Research Corporation, Jan. 2007.

[L38] "Circuit and Fabrication Issues for Computer Architects (Traveling from Kansas to Oz)," panelist at the CRA-W/CDC Computer Architecture Workshop, Princeton University, Princeton, NJ, July 2006.

[L37] "Analysis and Optimization of Voltage/Frequency-Island Based Designs," Texas Instruments, April 2006.

[L36] "High-Level Power Analysis and Optimization," Intel Corp., January 2006.

[L35] "Energy Awareness and Uncertainty in Design at Microarchitecture Level," Intel Labs, Pittsburgh, PA, October 2005.

[L34] "Energy Awareness and Uncertainty in Design at Microarchitecture Level," Dept. of Electrical and Computer Engineering, Delft University, Delft, Netherlands, July 2005.

[L33] "Power Analysis and Optimization of Voltage/Frequency-Island Based Designs," Semiconductor Research Corporation, Integrated Systems Kick-Off Meeting, May 2005.

[L32] "Energy Awareness and Uncertainty in Design at Microarchitecture Level," Dept. of Computer Science, Stanford University, Stanford, CA, May 2005.

[L31] "Energy Awareness and Uncertainty in Design at Microarchitecture Level," Dept. of Electrical and Computer Engineering, University of Texas, Austin, TX, March 2005.

[L30] "Energy Awareness and Uncertainty in Design at Microarchitecture Level," *Austin Conference on Energy Efficient Design* (ACEED), IBM Research, Austin, TX, March 2005.

[L29] "Enabling Energy Awareness in Emerging Platforms," keynote speech at SoC Technology Center, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, Oct. 2004.

[L28] "Energy Modeling and Optimization at Microarchitecture and System Level," tutorial at SoC Technology Center, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, Oct. 2004.

[L27] "Toward an Integrated Design Methodology for Fault-Tolerant, Multiple Clock/Voltage Integrated Systems," *IEEE Intl. Conference on Computer Design* (ICCD), San Jose, CA, Oct. 2004.

[L26] "Dynamic Power and Fault Tolerance for Ambient Intelligent Distributed Systems," Dept. of Computer Science, Karlsruhe University, Karlsruhe, Germany, Apr. 2004.

[L25] "Dynamic Power and Fault Tolerance for Ambient Intelligent Distributed Systems," Dept. of Electrical Engineering, Princeton University, Princeton, NJ, Apr. 2004.

[L24] "Energy Aware Computing: Synchronous vs. Partially Asynchronous Processors," IBM Research T.J. Watson, Apr. 2004.

[L23] "Dynamic Power and Fault Tolerance for Ambient Intelligent Distributed Systems," Electronic System Design Seminar, University of California, Berkeley, CA, Nov. 2003.

[L22] "Dynamic Power and Fault Tolerance for Ambient Intelligent Distributed Systems," Information Sciences and Technology Seminar, California Institute of Technology, Pasadena, CA, Oct. 2003.

[L21] "IEEE Spectrum Panel: Applying Sensor Networks Into Wearable Fabrics," panel at Intel Developer Forum, San Jose, CA, Oct. 2003.

[L20] "Current Trends and Issues in Energy Aware Computing Systems," lecture at European Summer School on Embedded Systems, Vasteras, Sweden, July 2003.

[L19] "Partially asynchronous microprocessor design," (with Dave Albonesi and Pradip Bose), half-day tutorial at *International Symposium on Computer Architecture*, in conjunction with *Federated Computing Research Conference*, (FCRC-ISCA), San Diego, CA, June 2003.

[L18] "Partially asynchronous microprocessor design," (with Dave Albonesi and Pradip Bose), half-day tutorial at *International Symposium on Microarchitecture* (MICRO), Istanbul, Turkey, November 2002.

[L17] "Energy Aware Computing: Synchronous vs. Partially Asynchronous Processors," Intel's Low Power Research Symposium, Sept. 2002.

[L16] "Minimally clocked microprocessor design," (with Dave Albonesi and Pradip Bose), half-day tutorial at *International Conference on Supercomputing*, New York, June 2002.

[L15] "Challenges and Opportunities in E-textile Analysis, Modeling and Optimization," special session at *ACM/IEEE Design Automation Conference* (DAC), Anaheim, CA, June 2002.

[L14] "Power and Performance Evaluation of Globally Asynchronous, Locally Synchronous Processors," Intel Corp., April 2002.

[L13] "High-Level Power Modeling and Optimization," lecture at *ACM-SIGDA Design Automation Summer School*, Cape Cod, MA, May 2001

[L12-10] "Challenges in energy aware computing," Intel's Low Power Research Symposium, Compaq WRL, and HP Labs, November 2000.

[L9] "Power Modeling and Optimization of High-Performance Systems," Carnegie Mellon University, Pittsburgh, PA, Jan. 2000.

UNIVERSITY OF MARYLAND, COLLEGE PARK

[L8] "Information-Theoretic Bounds for Switching Activity Analysis in Finite-State Machines under Temporally Correlated Inputs," 33rd *Asilomar Conference on Signals, Systems, and Computers* (ASILOMAR), October 1999.

[L7] "Power Modeling and Optimization of High-Performance Systems," University of Minnesota, Minneapolis, MN, Dec. 1999.

[L6] "The Synthesis of Power Manageable Hardware: A Case Study," University of Maryland, College Park, MD, March 1999.

[L5] "Power Analysis and Optimization of Digital Circuits," University of Maryland, Computer Engineering Seminar Series, College Park, MD, Dec. 1998.

UNIVERSITY OF SOUTHERN CALIFORNIA

[L4-1] "Power Analysis and Optimization of Digital Circuits," Carnegie Mellon University, Pittsburgh, PA, May 1998 (also at University of Maryland, College Park, MD; University of Rochester, Rochester, NY; Northwestern University, Evanston, IL; Feb.-May 1998).

OUTREACH, MENTORSHIP, AND FACULTY DEVELOPMENT

THE UNIVERSITY OF TEXAS AT AUSTIN

[M118] *DARPA Young Faculty Award Grant Writing Mini-workshop*, organizer, Department of Electrical and Computer Engineering, The University of Texas at Austin, October 23, 2020.

[M117] *NSF CAREER Grant Writing Mini-workshop*, organizer, Department of Electrical and Computer Engineering, The University of Texas at Austin, June 12, 2020.

CARNEGIE MELLON UNIVERSITY

[M116] *Bias Busters Session for Staff (Admissions Office)*, lecturer, Center for Faculty Success, Carnegie Mellon University, Oct. 29, 2019.

[M115-114]

Bias Busters Session for Faculty and Staff, lecturer, Center for Faculty Success, Carnegie Mellon University, Oct.3, 2019 and Oct. 28, 2019.

[M113-112]

Bias Busters Session for Faculty Search and Promotion & Tenure Committees, lecturer, Center for Faculty Success, Carnegie Mellon University, Sept. 18, 2019 and Oct. 7, 2019.

[M111] *5th College of Engineering New Faculty Orientation*, organizer, Center for Faculty Success, Carnegie Mellon University, Aug. 21-22, 2019.

[M110] *NSF CAREER Grant Writing workshop*, organizer, Center for Faculty Success, Carnegie Mellon University, May 29, 2019.

[M109] *Pitch Perfect: How to sell your ideas to industry and funding agencies*, workshop organizer, Center for Faculty Success, Carnegie Mellon University, May 16, 2019.

[M108] *Bias Busters Session for Staff (LEAD Professional Development Program)*, lecturer, Center for Faculty Success, Carnegie Mellon University, May 10, 2019.

[M107] *College of Engineering Junior Faculty Reception*, organizer, Center for Faculty Success, Carnegie Mellon University, April 15, 2019.

[M106] *Future Faculty Program: Choose the Best Offer and Negotiate for Success*, organizer and lecturer, Center for Faculty Success, Carnegie Mellon University, March 20, 2019.

[M105] *College of Engineering Senior Faculty Lunch*, organizer, Center for Faculty Success, Carnegie Mellon University, March 18, 2019.

[M104] *Future Faculty Program: Interview for Success*, organizer and lecturer, Center for Faculty Success, Carnegie Mellon University, Jan.24, 2019.

[M103] *Bias Busters Session for Faculty and Staff*, lecturer, Center for Faculty Success, Carnegie Mellon University, Dec.3, 2018.

[M102] *Future Faculty Program: Apply for Success*, organizer and lecturer, Center for Faculty Success, Carnegie Mellon University, Nov. 26, 2018.

[M101] *Future Faculty Program: Career Goals and Academia*, organizer and lecturer, Center for Faculty Success, Carnegie Mellon University, Nov. 9, 2018.

[M100] *Bias Busters @ ICCAD Workshop*, organizer and lecturer, International Conference on Computer Aided Design, San Diego, CA, Nov. 4, 2018.

[M98-99]

Bias Busters Session for Faculty Search and Promotion & Tenure Committees, lecturer, Center for Faculty Success, Carnegie Mellon University, Sept. 17, 2018 and Oct. 15, 2018.

[M97] *4th College of Engineering New Faculty Orientation*, co-organizer, Center for Faculty Success, Carnegie Mellon University, Aug. 22-23, 2018.

[M96] *Bias Busters @ USC Workshop*, organizer and lecturer, University of Southern California, Los Angeles, CA, June 4, 2018.

[M95] *Bias Busters @ ISCA Workshop*, organizer and lecturer, International Symposium on Computer Architecture, Los Angeles, CA, June 3, 2018.

[M94] *NSF CAREER Grant Writing workshop*, co-organizer, Center for Faculty Success, Carnegie Mellon University, May 17, 2018.

[M93] *CIT Faculty Mixer*, co-organizer, Center for Faculty Success, Carnegie Mellon University, May 15, 2018.

[M92] *Pitch Perfect: How to sell your ideas to industry and funding agencies*, workshop organizer, Center for Faculty Success, Carnegie Mellon University, May 11, 2018.

[M91] "IDEAL-N CMU Progress report," *NSF IDEAL-N Annual Plenary Meeting*, April 6, 2018.

[M90] *College of Engineering Junior Faculty Lunch*, co-organizer, Center for Faculty Success, Carnegie Mellon University, March 22, 2018.

[M89] *College of Engineering Senior Faculty Lunch*, co-organizer, Center for Faculty Success, Carnegie Mellon University, March 19, 2018.

[M88] *Bias Busters Session for Faculty and Staff*, lecturer, Center for Faculty Success, Carnegie Mellon University, Nov. 27, 2017.

[M86-87]

Bias Busters Session for Faculty Search Committees, lecturer, Center for Faculty Success, Carnegie Mellon University, Nov.6, 2017; University of Pittsburgh, Dec. 1, 2017.

[M85] *Bias Busters Session for Faculty Search and Promotion & Tenure Committees*, lecturer, Center for Faculty Success, Carnegie Mellon University, Oct. 12, 2017.

[M84] *DARPA Young Faculty Award Grant Writing workshop*, co-organizer, Center for Faculty Success, Carnegie Mellon University, Sept. 28, 2017.

[M83] *Bias Busters Session for CMU Division of Operations Staff*, lecturer, Center for Faculty Success, Carnegie Mellon University, Sept. 20, 2017.

[M82] *3rd College of Engineering New Faculty Orientation*, co-organizer, Center for Faculty Success, Carnegie Mellon University, Aug.24-25, 2017.

[M81] "External Funding and Grant Writing," panel organizer, *2nd University-wide New Faculty Orientation*, Carnegie Mellon University, Aug.23, 2017.

[M80] "Internal Funding at CMU," panel organizer, *2nd University-wide New Faculty Orientation*, Carnegie Mellon University, Aug.23, 2017.

[M79] *Bias Busters Session for Faculty*, lecturer, *2nd University-wide New Faculty Orientation*, Carnegie Mellon University, Aug.22, 2017.

[M78] *Bias Busters Train-the-Trainer*, facilitator, Center for Faculty Success, Carnegie Mellon University, July 25, 2017.

[M76-77]

Bias Busters Session for CMU Provost Office Staff, lecturer, Center for Faculty Success, Carnegie Mellon University, May 22, June 22 2017.

[M75] *NSF CAREER Grant Writing workshop*, co-organizer, Center for Faculty Success, Carnegie Mellon University, May 10, 2017.

[M74] "IDEAL-N CMU Progress report," *NSF IDEAL-N Annual Plenary Meeting*, April 7, 2017.

[M73] *College of Engineering Senior Faculty Lunch*, co-organizer, Center for Faculty Success, Carnegie Mellon University, March 28, 2017.

[M72] *College of Engineering Junior Faculty reception*, co-organizer, Center for Faculty Success, Carnegie Mellon University, March 23, 2017.

[M71] "ELATE IAP Story: College of Engineering Center for Faculty Success," invited speaker, *ELATE-ELUM Symposium,* University of Pittsburgh, March 9, 2017.

[M70] *Bias Busters Session for Staff Search Committees (CMU Student Affairs),* lecturer, Center for Faculty Success, Carnegie Mellon University, Jan.18, 2017.

[M69] *Bias Busters Session for Faculty and Staff (Information Networking Institute),* lecturer, Center for Faculty Success, Carnegie Mellon University, Jan.11, 2017.

[M68] "What's in An Ad?," invited speaker, *Workshop on Exploring Faculty Position Job Search Process for PhD Women in STEM Disciplines,* Office for Graduate Education, Carnegie Mellon University, Dec. 14, 2016.

[M67] *Bias Busters Session for Graduate Admission Committees,* organizer/lecturer, Center for Faculty Success, Carnegie Mellon University, Nov.10, 2016.

[M66] *Bias Busters Session for Undergraduate Admission Committees*, lecturer, Center for Faculty Success, Carnegie Mellon University, Nov.4, 2016.

[M65] *Bias Busters @ University Train the Trainer Workshop* – A Carnegie Mellon/Google Collaboration to Address Unconscious Bias, workshop co-organizer and speaker, Carnegie Mellon University and Google Pittsburgh, Nov.2, 2016.

[M64] "Building Your Network and Your Life," speaker, *Rising Stars in EECS workshop,* Carnegie Mellon University, Nov.1, 2016.

[M63] "Promotion and Tenure – Advice from Senior Faculty," panel organizer, *Rising Stars in EECS workshop,* Carnegie Mellon University, Nov.1, 2016.

[M62] *Rising Stars in EECS Workshop,* co-organizer, Carnegie Mellon University, Oct.30-Nov.1, 2016.

[M60-61]

Bias Busters Session for Faculty Search Committees, lecturer, Center for Faculty Success, Carnegie Mellon University, Oct. 18 and Oct.27, 2016.

[M58-59]

Bias Busters Session for Graduate Students, organizer/lecturer, Center for Faculty Success, Carnegie Mellon University, Oct.25, Nov.11, 2016.

[M56-57]

Bias Busters Train-the-Trainer, facilitator, Center for Faculty Success, Carnegie Mellon University, Sept.29 and Dec.8, 2016.

[M54] *Bias Busters Session for Faculty*, lecturer, Center for Faculty Success, Carnegie Mellon University, Oct.6, 2016.

[M54] *Bias Busters Session for Faculty Promotion and Tenure Committees*, lecturer, Center for Faculty Success, Carnegie Mellon University, Sept. 30, 2016.

[M53] "Bias Busting @ University Workshop – A Carnegie Mellon/Google Collaboration to Address Unconscious Bias," workshop co-organizer and speaker, *ACM Richard Tapia Celebration of Diversity in Computing,* Austin, TX, Sept. 15, 2016.

[M52] *Bias Busters Session for Faculty*, lecturer, Center for Faculty Success, Carnegie Mellon University, Aug.26, 2016.

[M51] *Second College of Engineering New Faculty Orientation*, co-organizer, Center for Faculty Success, Carnegie Mellon University, Aug.25-26, 2016.

[M50] "External Funding and Grant Writing," panel organizer, *First University-wide New Faculty Orientation*, Carnegie Mellon University, Aug.24, 2016.

[M49] "Internal Funding at CMU," panel organizer, *First University-wide New Faculty Orientation*, Carnegie Mellon University, Aug.24, 2016.

[M48] "Building Your Network and Your Life," speaker, *First University-wide New Faculty Orientation*, Carnegie Mellon University, Aug.22, 2016.

[M47] "Sustainability in Computing and Beyond: A journey from nature-inspired computing to nature and back," invited presentation for the LEAP@CMU program, June 22, 2016.

[M46] "How Academic Culture Fuels Impostor Syndrome in Students and Faculty and Strategies for Addressing It in the Classroom and the Department," workshop co-organizer and speaker, *Women in Engineering Proactive Network* (WEPAN) *Change Leader Forum*, Broomfield, CO, June 14, 2016.

[M45] "Bias Busting @ University Workshop – A Carnegie Mellon/Google Collaboration to Address Unconscious Bias," workshop co-organizer and speaker, *Women in Engineering Proactive Network* (WEPAN) *Change Leader Forum*, Broomfield, CO, June 14, 2016.

[M44] "Getting to Success in Writing Grants and Proposals," invited speaker, *Young Faculty Workshop*, *ACM/IEEE Design Automation Conference*, Austin, TX, June 5, 2016.

[M43] *Pitch Perfect: How to sell your ideas to industry and funding agencies*, workshop organizer, Center for Faculty Success, Carnegie Mellon University, May 9, 2016.

[M42] *NSF CAREER Grant Writing workshop*, co-organizer, Center for Faculty Success, Carnegie Mellon University, May 2, 2016.

[M41] "It's a common lament: there aren't enough hours in the day. And maybe there aren't in a day, but what if we look at a week?," organizer and host, Center for Faculty Success Speaker Series with Laura Vanderkam, Carnegie Mellon University, April 7, 2016.

[M40-36]

Bias Busters Session for Faculty, lecturer, Center for Faculty Success, Carnegie Mellon University, Feb.12, Feb.26, March 9, April 6, April 20, 2016.

[M35-34]

Bias Busters Session for Faculty Search Committees, lecturer, Center for Faculty Success, Carnegie Mellon University, Nov.13, Nov. 18, 2015.

[M33] *Bias Busters Train-the-Trainer*, facilitator, Center for Faculty Success, Carnegie Mellon University, Nov. 17, 2015.

[M32] *Bias Busters Session for Faculty*, lecturer, Center for Faculty Success, Carnegie Mellon University, Oct. 30, 2015.

[M31] *Lead It Yourself (LIY!) Train-the-Trainer Workshop*, UW ADVANCE grant-supported participant representing CMU's Center for Faculty Success, University of Washington, Oct. 26, 2015.

[M30] *First College of Engineering New Faculty Orientation*, organizer and founding chair, Center for Faculty Success, Carnegie Mellon University, Sept. 8-10, 2015.

[M29] "Sustainability in Computing and Beyond," invited presentation for the LEAP@CMU program, June 23, 2015.

[M28] "Still Too Slow: The Advancement of Women," organizer and host, Center for Faculty Success Speaker Series with Virginia Valian, Carnegie Mellon University, May 13, 2015.

[M27] *Workshop for Faculty Members* by Virginia Valian (CUNY), organizer and host, Center for Faculty Success, Carnegie Mellon University, May 12, 2015.

[M26] *Workshop for Faculty Search Committee Members* by Virginia Valian (CUNY), organizer and host, Center for Faculty Success, Carnegie Mellon University, May 13, 2015.

[M25] *Workshop for Department Heads and College Leaders* by Virginia Valian (CUNY), organizer and host, Center for Faculty Success, Carnegie Mellon University, May 13, 2015.

[M24] *Workshop for University Leadership* by Virginia Valian (CUNY), organizer and host, Center for Faculty Success, Carnegie Mellon University, May 12, 2015.

[M23] "Why Smart People (Including Faculty) Suffer from the Imposter Syndrome and how You Can Help Yourself or Others Thrive in Spite of It," organizer and host, Center for Faculty Success Speaker Series with Valerie Young, Carnegie Mellon University, April 12, 2015.

[M22] EnyAC Tour, Presentation, and Demos, *Carnegie Science Center "Tour Your Future"* program for middle- and high-school girls, March 28, 2015.

[M21] Scholar Citizen Panelist, Odyssey program, Carnegie Mellon University, January 9, 2015.

[M20] "Advancing Women in Engineering Retreat," Carnegie Mellon University, organizer, June 17-19, 2014.

[M19] "Conversations on Leadership -- Lessons from ELATE at Drexel," invited panelist, *Women in Engineering Professional Network Conference* (*WEPAN*), Minneapolis, MN, June 11, 2014.

[M18] "Sustainability in Computing and Beyond," keynote talk, *CRA-W/CDC Discipline Specific Workshop on Diversity in Design Automation*, co-located with *ACM/IEEE Design Automation Conference*, San Francisco, CA, June 2014.

[M17] "Small Footprint Hydropower Generation and Monitoring," Project Olympus Spring Carnival Show & Tell, April 10, 2014.

[M16] "Legos and Small Footprint Hydropower Generation and Monitoring," presentation for the *Pittsburgh First Lego League* team, Pittsburgh, PA, Feb. 4, 2014.

[M15] First iGEM CMU Team, project advisor and mentor, April 2012-2015.

[M14] "IC Aging Analysis Using HSPICE," project advisor and mentor for Niharika Singh, CMU ECE student, as part of *Semiconductor Research Corporation Undergraduate Research Opportunities* (*SRC URO*) program for minority and female engineering students, Aug.2011-May 2014.

[M13] *First CRA-W/CDC Workshop on Diversity in Design Automation and Test*, founder and organizer, Pittsburgh, PA, May 23-24, 2011.

[M12] "Being A College Professor: The Good, The Bad, and The Ugly," presenter at the Career Fair, Dorseyville Middle School, Fox Chapel Area School District, Pittsburgh, PA, May 2010.

[M11] "Soft-Error Analysis Using HSPICE," project advisor and mentor for Sunny Atluri, CMU CIT first year student, as part of Intel First Year Research Experience (IFYRE) program for minority and female engineering students, Aug.2006-Aug.2007.

[M10] "About Low Power Research (and not only!)," invited talk at *Women in ECE* (*WinECE*) Fall Dinner, Sept. 2006.

[M9] "Circuit and Fabrication Issues for Computer Architects (Traveling from Kansas to Oz)," panelist at the *CRA-W/CDC Computer Architecture Workshop*, Princeton University, Princeton, NJ, July 2006.

[M8] "Symbolic Analysis of Circuit Reliability," project advisor and mentor for Amanda Rainer (Harvey Mudd College), as part of Distributed Mentorship Program, *Computing Research Association* (*CRA*), May-Aug. 2005.

[M7] "Impact of Variability on Power and Performance," project advisor and mentor for Daisy Lee (U.C. California, Berkeley), as part of the Distributed Mentorship Program, *Computing Research Association* (*CRA*), May-Aug. 2005.

[M6] "EMG Signal Processing," project advisor for CMU's SWE Engineering Your Future, July 2004.

[M5] "Bringing Undergraduates into Your Research Program," panelist at *Computing Research Association Mentorship Workshop*, in conjunction with *Federated Computing Research Conference*, (*FCRC-CRA-W*), San Diego, CA, June 2003.

[M4] "The Two-Body Problem: Applying for Jobs," invited panelist, organized by CMU's Women in SCS, May 2003.

[M3] "The Smart Woman's Job Search in the Academy and Industry," invited talk at CMU's Graduate Women Lunch, March 2003.

[M2] "The Academic Environment at Carnegie Mellon and Challenges for International Women," invited panelist, organized by CMU's Office for International Education, September 2002.

[M1] "Adapting to Advances in Technology: Next Steps Toward Life-Long Learning," panel moderator and organizer, CRA-W Distinguished Lecture Series, CMU, December 2000.

TEACHING

CARNEGIE MELLON UNIVERSITY

Hardware Architectures for Machine Learning, graduate level (*Fall 2018, Spring 2019*)

Newly developed in fall 2018 and taught every spring semester since. Samples of student comments: *"One of the best courses I took at CMU." "Great class!" "The lectures were designed well to allow for good technical discussion in the class. I don't think that I participated in active learning by that degree in any other class I took at CMU."*

Energy Aware Computing, graduate level (*Spring 2005-2006, Fall 2001-2003, Fall 2009-2018*)

Newly developed in 2001 and taught every year since. Samples of student comments*: "Thank you. The class was a LOT of fun (I don't say that frequently)." "Thank you for this semester! I learned quite a bit." "Thanks again for an interesting class!" "Thanks for your excellent teaching. I really learned a lot in my first semester here."*

VLSI CAD: Logic to Layout, graduate level (*Spring 2011-2014*)

Samples of student comments: *"Brilliant course content. Love doing the assignments." "Great course, wonderful material. I'd highly recommend it. Terrific! Thank you very much."*

Fundamentals of Computer Engineering, sophomore level (*Fall 2005, Spring 2008, Spring 2010*)

Samples of student comments: *"Course was great, very good level of difficulty (requires actual work, but not overwhelming)." "My favorite course so far."*

Advanced Computer Architecture, graduate level (*Fall 2007*)

Samples of student comments: *"The course is rather helpful for those wanting to pursue computer architecture as their research field."*

Advanced Digital Design Project, capstone design course (*Fall 2006*)

"I put a lot of time and effort into this course, but never have I been more anxious and willing to do it than for this class. I loved every minute of it!" "I loved this class!"

Verification of Computer Systems[2], senior-level (*Fall 2004*)

Intro to Computer Architecture, junior level (*Fall 2000, Spring 2001-2003*)

UNIVERSITY OF MARYLAND, COLLEGE PARK

VLSI System Design Laboratory, capstone design course (*Fall 1999*)

Advances in Low-Power Design Methodologies, graduate level (*Fall 1998*). Newly developed course.

Computer Engineering curriculum taskforce. Revamped the "Computer-Aided Design of Digital Systems" course (*Spring 1999*).

UNIVERSITY OF SOUTHERN CALIFORNIA

Computer Aided Design of Digital Systems I, graduate level (*Teaching Assistant, Spring 1994*)

NEW YORK UNIVERSITY

Programming Languages, graduate level (*Teaching Assistant, Fall 1993*)

"POLITEHNICA" UNIVERSITY OF BUCHAREST, ROMANIA

Formal Languages and Compiler Design, undergraduate level *(Teaching Assistant, Spring 1993*)

Programming Techniques, undergraduate level *(Teaching Assistant, Spring 1993*)

Data Structures and Algorithms, undergraduate level *(Teaching Assistant, Fall 1992*)

System Modeling and Simulation, undergraduate level *(Teaching Assistant, Spring 1992*)

FACULTY MENTEES

CARNEGIE MELLON UNIVERSITY

[FM4] Jovan Ilic, Assistant Teaching Professor of ECE (2017-2019).

[FM3] Linda Moya, Assistant Teaching Professor of ECE (2017-2019).

[FM2] Carlee Joe-Wong, Assistant Professor of ECE (2016-2019).

[FM1] Gabriela Hug, Assistant Professor of ECE (2009-2015).

PH.D. STUDENTS ADVISED

THE UNIVERSITY OF TEXAS AT AUSTIN

[PH23] Natasha Frumkin[†], "Machine learning and computer systems convergence," The University of Texas at Austin (2020-present).

[2] Student comments not available electronically before 2005.
[†] UT Austin Ph.D. advisee.

CARNEGIE MELLON UNIVERSITY

[PH22] Ahmet Fatih Inci*, "Energy-efficient computing systems for data-intensive applications," Carnegie Mellon University (2017-present).

[PH21] Ting-Wu (Rudy) Chin*, "Width-optimized ConvNets for Efficient Image Classification," Carnegie Mellon University (2017-present).

[PH20] Ruizhou Ding*, "Improving Efficiency and Accuracy for Training and Inference of Hardware-aware Machine Learning Systems," Carnegie Mellon University (2015-2020). First job: Quantitative researcher, Citadel Securities LLC.

[PH19] Dimitrios Stamoulis*, "Hardware-Aware AutoML for Efficient Deep Learning Applications," Carnegie Mellon University (2015-2020). First job: Senior researcher, Microsoft Cloud & AI, Microsoft Corp.

[PH18] Ifigeneia Apostolopoulou*, "Design automation-inspired complex system modeling and simulation for biological applications," Carnegie Mellon University (2015-2017; graduated with a M.S.). Currently Ph.D. student in Machine Learning at CMU.

[PH17] Zhuo Chen*, "Learning for and with efficient computing systems," Carnegie Mellon University (2013-present). First job: Software Engineer at Google.

[PH16] Ermao Cai*, "Power/Performance Modeling and Optimization: Using and Characterizing Machine Learning Applications," Carnegie Mellon University (2013-2018). First job: Software engineer at Jump Trading.

[PH15] Ivan Ukhov, "Uncertainty Quantification for Electronic System Design," visiting scholar from Linkoping University (2015). First job: Data scientist at LeoVegas Group.

[PH14] Jiajia Jiao, "Soft Error Analysis for Many-Core Systems," visiting scholar from Shanghai Jiao Tong University, (2013-2014). First job: Assistant Professor at Maritime University, Shanghai, China.

[PH13] Guangshuo Liu*, "Implicit and Explicit Heterogeneity in Multi-Core Systems," Carnegie Mellon University (2012-2014; graduated with a M.S.). First job: Software engineer at Google/Nest Labs. Currently: Software engineer at Facebook.

[PH12] Da-Cheng Juan*, "A Learning-Based Framework Incorporating Domain Knowledge for Performance Modeling," Carnegie Mellon University (2009-2014). First job: Senior Software Engineer at Google.

[PH11] Jiyuan Zhang*, "Scalable Resource Management for 1000-Core Systems," Carnegie Mellon University (2013-2014, co-advised with Radu Marculescu). First job: Ph.D. student at CMU.

[PH10] Kai-Chiang (Alex) Wu*, "Reliability Aware Circuit Optimization," Carnegie Mellon University (2006-2011). First job: Software Engineer at Intel Corporation. Currently: Associate Professor at National Chiao-Tong University, Taiwan.

[PH9] Ming-Chao Lee, "Design Optimization for Power Gating," visiting scholar from National Tsinghua University, Taiwan, (2010-2011). First job: Global Unichip.

[PH8] Yi-Lin Chuang, "VLSI Placement Considering Routability and Power Consumption," visiting scholar from National Taiwan University, Taiwan, (2010-2011). First job: TSMC.

[PH7] Lavanya Subramanian*, "Providing Quality of Service in Chip-Multiprocessors under Variability," Carnegie Mellon University (2009-2011). First job: Ph.D. student at CMU. Currently: IBM.

* CMU Ph.D. advisees.

[PH6] Wan-Ping Lee, "Voltage Island Aware Physical Design," visiting scholar from National Taiwan University, Taiwan, (2008-2009). First job: Postdoctoral researcher, Boston College, Systems Biology (Marth Lab). Currently: Senior Lead Scientist at Seven Bridges Genomics.

[PH5] Sebastian X. Herbert*, "Modeling, Characterizing, and Mitigating the Impact of Process Variations on the Energy-Efficiency of Chip-Multiprocessors," Carnegie Mellon University (2005-2009). First job: Principal at DC Energy.

[PH4] Siddharth Garg*, "System-Level Modeling and Mitigation of the Impact of Process Variations," Carnegie Mellon University (2005-2009). First job: Assistant Professor at University of Waterloo. Currently: Associate Professor at New York University.

[PH3] Natasa Miskov-Zivanov*, "Probabilistic Modeling and Optimization for Circuit Reliability," Carnegie Mellon University (2003-2008). First job: Research Associate at University of Pittsburgh, Computational and System Biology (Faeder Lab). Currently: Assistant Professor at University of Pittsburgh.

[PH2] Phillip Stanley-Marbell*, "Programming Unreliable Networks of Computation," Carnegie Mellon University (2001-2007). First job: Postdoctoral-researcher at Technical University Eindhoven, Netherlands. Currently: Assistant Professor at Cambridge University.

[PH1] Emil Talpes*, "Flywheel: Enabling Performance Increase and Power Efficiency by Using Multiple Speed Pipelines," Carnegie Mellon University (2000-2004). First job: Software Engineer at Advanced Micro Devices. Currently: Hardware engineer at Tesla.

POSTDOCTORAL RESEARCHERS AND VISITING SCIENTISTS

CARNEGIE MELLON UNIVERSITY

[PD5] Jinpyo Park, Visiting scientist, Principal Engineer, Samsung Corp., 2012-2013.

[PD4] Siddharth Garg, Postdoctoral researcher, 2009-2010. Currently Assistant Professor at New York University.

[PD3] Umit Y. Ogras, Postdoctoral researcher, 2008-2009. Currently Assistant Professor at Arizona State University.

[PD2] Natasa Miskov-Zivanov, Postdoctoral researcher, 2008-2009. Currently Assistant Professor at University of Pittsburgh.

[PD1] Eun-Gu Jung, Visiting postdoctoral scholar, ETRI, South Korea, 2005-2006.

M.S. STUDENTS ADVISED

CARNEGIE MELLON UNIVERSITY

[MS43] Ruitao Yi, "Efficient Neural Architecture Search," 2019.

[MS42] Aman Jain, "A Framework for Neural Architecture-Hardware Co-Design," 2019.

[MS41] Siri Garudanagiri Virupaksha, "A Framework for Neural Architecture-Hardware Co-Design," 2019.

[MS40] Mark Wuebbens, "A Simulator for Autonomous Vehicle Networks," 2017.

[MS39] Anand Krishnan Prakash, "Analyzing Deep Learning on Heterogeneous Computing Systems," 2016-2017. First job: Berkeley Lab.

* CMU Ph.D. advisees.
* CMU Ph.D. advisees.

[MS38] Harsha Ambardekar, “Probing FPGA I/O for Biological Data Visualization,” 2014-2015. First job: Intel Corp.

[MS37] Sumanth Suresh, “Converting Dynamical Systems to Discrete Time Systems,” 2014-2015. First job: Nutanix.

[MS36] Sudhir Vijay, “Biological Systems to Hardware Model Parser,” 2014-2015. First job: Datrium.

[MS35] Aditya Kotwal, “Boolean Models from Time Series,” 2014-2015. First job: VMWare.

[MS34] Samantha Tan, “Digital Display Post-It Note Array,” 2013-2014.First job: Apple Inc.

[MS33] Suvrat Alshi, “Thread Migration Cost Modeling for Many-Core Systems,” 2013-2014. First job: SanDisk.

[MS32] Shraddha Joshi, “Accurate and Efficient Power Macro-models for Many-Core Systems,” 2013-2014. First job: Oracle Corp.

[MS31] Willis Chang, “Inferring Boolean Functions from Time Series by Using SAT Solvers,” 2013-2014. First job: Sterne, Kessler, Goldstein & Fox.

[MS30] Akshita Jain, “Ambient Display Tile / Digital Post-It Note,” 2012-2013. First job: SanDisk.

[MS29] Samyuktha Subramanian, “Heterogeneous multi-core power modeling and optimization,” 2012-2013. First job: VMWare.

[MS28] Ameya Ambardekar, “Chip Multiprocessor Workload Characterization,” 2011-2012. First job: Intel Corp.

[MS27] Ratin Malkud, “Compiling Biological Networks in Hardware,” 2011-2012. First job: Cisco Systems.

[MS26] Aakash Chugh, “Compiling Biological Networks in Hardware,” 2011-2012. First job: Cadence Design Systems.

[MS25] Arnold Pereira, “Chip Multiprocessor Workload Characterization,” 2011-2012. First job: Microsoft Corp.

[MS24] Xianglong Fu, “Dynamic Power Management for CMP Platforms,” 2011-2012. First job: Oracle/Sun Corp.

[MS23] Pinjie Huang, “Dynamic Power Management for CMP Platforms,” 2011-2012. First job: Oracle/Sun Corp.

[MS22] Sundeep Konudula, “Thermal-Aware Floorplanning,” 2011-2012. First job: Nvidia Corp.

[MS21] Kedar Mane, “Technology Trends for SER in Digital Circuits,” 2010-2011. First job: Nvidia Corp.

[MS20] Jagannathan Raman, “Biological Network Simulation Using GPGUs,” 2010-2011. First job: Nvidia Corp.

[MS19] Deepa Krishnaswamy, “Compiling Biological Networks in Hardware,” 2010-2011. First job: University of Pittsburgh.

[MS18] Sreesan Venkatakrishnan, “Compiling Biological Networks in Hardware,” 2010-2011. First job: Oracle/Sun Corp.

[MS17] Prashanth Balasubramanian, “GPGUs for Speeding Up Biological Network Analysis,” 2009-2010. First job: Apple Inc.

[MS16] Prashant Kashinkunti, “Redundant TSV placement for thermal emergency mitigation and yield improvement of 3D Chip-multiprocessor,” 2009-2010. First job: Microsoft Corp.

[MS15] Yu-Chi Chu, 2008-2009.

[MS14] Dhananjay Motwani, “Power Management for Multi-Core Systems,” 2007-2008. First job: Cisco Systems.

[MS13] Anupama Suryanarayanan, “Power Management for Multi-Core Systems,” 2007-2008. First job: Intel Corp.

[MS12] Gaurav Kapoor, “Power Management for Multi-Core Systems,” 2006-2007. First job: Apple Inc.

[MS11] Sebastian X. Herbert, "Variability-Tolerant Chip Multiprocessors," 2005-2007. Continued as a Ph.D. student at Carnegie Mellon University.

[MS10] Puru Choudhary, "Frequency/Voltage Scaling of GALS Systems using Hardware Based Methods," 2005-2007. First job: Marvell Semiconductors.

[MS9] Natasa Miskov-Zivanov, "Symbolic Analysis of Circuit Reliability," 2003-2005. Continued as a Ph.D. student at Carnegie Mellon University.

[MS8] Koushik Niyogi, "Power and Performance Evaluation of GALS Point-to-point Interfaces," 2003-2005. First job: Cadence Design Systems.

[MS7] V.P. Shyam Rapaka, "Mixed-Clock Issue Queue Design for Globally Asynchronous, Locally Synchronous Processor Cores," 2001-2003. First job: Mentor Graphics Corp.

[MS6] Katrina Zwicker, "A Clustered Architecture with a GALS Clocking Scheme," 2001-2003. First job: Lockheed Martin.

[MS5] Anoop Iyer, "Globally Asynchronous, Locally Synchronous Processors," 2000-2002. First job: Advanced Micro Devices.

[MS4] Emil Talpes, "Energy Aware Execution Caches," 2000-2002. Continued as a Ph.D. student at Carnegie Mellon University.

UNIVERSITY OF MARYLAND, COLLEGE PARK

[MS4] Jun Wan, 1998-2001 (co-advised with Prof. Robert Newcomb, UMD).

[MS3] Percy Wadia, 1998-1999. First job: Intel Corp.

[MS2] Karthik Krishnan, 1998-1999. First job: Intel Corp.

[MS1] Doron Shiloach, 1998-1999. First job: IBM T.J. Watson.

UNDERGRADUATE STUDENTS ADVISED

CARNEGIE MELLON UNIVERSITY

[UG40] Thallam, Venkata Vivek, "Designing a Parameterizable Energy-Efficient Reconfigurable Accelerator," 2019.

[UG39] Haochang (Frank), Fang, "Designing Adaptive Neural Networks for Energy-Constrained Image Classification," 2017-2018.

[UG38] Sajja, Sribhuvan, "Designing Adaptive Neural Networks for Energy-Constrained Image Classification," 2017-2018.

[UG37] Bognar, Mitchell, "Duke University Internship: Designing Adaptive Neural Networks for Energy-Constrained Image Classification," 2017-2018.

[UG36] Zhang, Stella, "Hardware Emulation of Nonlinear Dynamical Systems," 2016-2017.

[UG35] Paquette, Lizzie, "Wesleyan University Internship: Multi-Level Logic Modeling of Cell Signaling Networks," 2016-2017.

[UG34] Pan, Paul, "Cell Signaling Emulation in Hardware," 2015-2017.

[UG33] Wuebbens, Mark, "Cell Signaling Emulation in Hardware," 2014-2017.

[UG32] Kim, Jason, "River Network Modeling Using Inferred Models," 2014-2017.

[UG31] Singh, Niharika, "SRC URO: IC Aging Analysis Using HSPICE," 2012-2015.

[UG30] Loh, Clement C. S., "Compiling Biological Network in Hardware," 2013-2014.

[UG29] Turakhia, Yatish, "IIT Bombay Internship: Power Optimization in Dark Silicon Systems," 2012-2014.

[UG28] Rajkumar, Vikram, "Thermal Modeling and Characterization of Chip Multiprocessors," 2012-2013.

[UG27] Ranjan, Pranay, "IIT Bombay Internship: Inferring Boolean Networks for Biological System Characterization," 2012-2013.

[UG26] Sia, Solomon H., "Compiling Biological Network to Hardware," 2012-2013.

[UG25] Jain, Archa, "Creating a Stateflow Router," 2010-2012.

[UG24] Sundaresan, Neereja, "Creating a Stateflow Router," 2010-2012.

[UG23] Bresticker, Andrew, "Hardware Modeling of Biological Signaling Networks," 2010-2012.

[UG22] Coleman, Sean, "Process Variation Modeling and Characterization in Array Structures," 2008-2009.

[UG21] Escalante, Mario, "Large Area Sensing for Security Applications," 2006-2007.

[UG20] Cheah, Chern Yih, "Large Area Sensing for Security Applications," 2004-2007.

[UG19] Padhi, Neha, "Large Area Sensing for Security Applications," 2004-2007.

[UG18] Rosenberg, Stephanie, "Large Area Sensing for Security Applications, 2004-2007.

[UG17] Loo, Brian, "Large Area Sensing for Security Applications," 2004-2005.

[UG16] Sun, Stanley, "Power Management for Sensing Applications," 2003-2005.

[UG15] Cheng, Yong-Khong, "Large Area Sensing for Security Applications," 2003-2004.

[UG14] Jeevan, Prasanth, "Large Area Sensing for Security Applications," 2003-2004.

[UG13] Lim, Han-Chun, "Large Area Sensing for Security Applications," 2003-2004.

[UG12] Li, Yanjing, "Large Area Sensing for Security Applications," 2003-2004

[UG11] Stoler, Adam, "Criticality Based Voltage Scaling," 2002-2004.

[UG10] Cheng, Zaizhi, "Large Area Sensing for Security Applications," 2002-2004.

[UG9] Lee, Shaun, "Large Area Sensing for Security Applications," 2002-2004.

[UG8] Tan, Gregory, "Large Area Sensing for Security Applications," 2002-2004.

[UG7] Hobday, Colin, "Technology Impact on Processor Scalability," 2002-2004.

[UG6] Lim, Kay Chun, "Power Analysis of Branch Prediction Hardware," 2001-2003.

[UG5] Ang, Justiin, "A Testbed for Electronic Textiles," 2001-2003.

[UG4] Ong, Kah Kien, "Simulation Speed-Up Using a Hybrid Simulator," 2000-2002.

[UG3] Furukawa, Junichi, "Low-Power Processing in EPIC Architecture," 2000-2002.

[UG2] Leung, Shing Tai, "Library of Energy Aware Logic Gates," 2000-2002.

[UG1] Chu, Charlene, "FIFO Design for GALS Systems," 2000-2001.

PH.D. THESIS COMMITTEES

CARNEGIE MELLON UNIVERSITY

[PT15] Zeye (Dexter) Liu (Chair: Shawn Blanton), May 2019-March 2020.

[PT14] Soumya Mittal (Chair: Shawn Blanton), Sept. 2018-January 2020.

[PT13] Kartikeya Bhardwaj (Chair: Radu Marculescu), August 2018-August 2019.

[PT12] Chieh Lo (Chair: Radu Marculescu), December 2017-Sept. 2018.

[PT11] Xuanle Ren (Chair: Shawn Blanton), June 2017-Sept. 2018.

[PT10] David Tian (Chair: Rick Carley), July 2015-present.

[PT9] Matthew Beckler (Chair: Shawn Blanton), December 2012-2017.

[PT8] Adam Hartman (Chair: Don Thomas), August 2012-Dec. 2015.

[PT7] Daniel (Guopeng) Wei (Chair: Radu Marculescu), December 2014-August 2015.

[PT6] Paul Bogdan (Chair: Radu Marculescu), Jan. 2011-Dec. 2011.

[PT5] Brett Meyer (Chair: Don Thomas), Aug. 2008-Aug. 2009.
[PT4] Annie Luo (Chair: Dan Siewiorek), Aug.2006-Aug. 2008.
[PT3] Reed Taylor (Chair: Herman Schmit), Aug. 2003-Aug. 2004.
[PT2] Vikas Chandra (Chair: Herman Schmit), Dec. 2003-Dec. 2004.
[PT1] Se-Hyun Yang (Chair: Babak Falsafi), Dec. 2002-Dec. 2003.

PH.D. QUALIFYING EXAM COMMITTEES

CARNEGIE MELLON UNIVERSITY

[PQ39] Chenlei Fang, April 2018.
[PQ38] Qiwan Meng, April 2018.
[PQ37] Zeye Liu, November 2017.
[PQ36] Joseph Sweeney, April 2017.
[PQ35] Ogun Kibar, April 2017.
[PQ34] Xiang Lin, November 2016.
[PQ33] Chieh Lo, November 2016.
[PQ32] Nandita Vijaykumar, November 2015.
[PQ31] Xuanle Ren, November 2014.
[PQ30] Yu Wang, April 2014.
[PQ29] Cheng Xue, January 2013, May 2013.
[PQ28] Rachata Ausavarungnirun, November 2012.
[PQ27] Christos Angelopoulos, April 2012.
[PQ26] Miray Kas, November 2011.
[PQ25] Tao Cui, November 2011.
[PQ24] Qiuling Zhu, April 2011.
[PQ23] Matthew Beckler, April 2011.
[PQ22] Hongfei Wang, April 2011, November 2010.
[PQ21] Wangyang Zhang, November 2010.
[PQ20] Adam Hartman, November 2009.
[PQ19] Xiaochun Yu, April 2008.
[PQ18] Evangelos Vlachos, April 2008.
[PQ17] Kevin Biswas, November 2007.
[PQ16] Raja Sambasivan, November 2007.
[PQ15] Le Xie, April 2007.
[PQ14] Brett Meyer, April 2006.
[PQ13] Eric Chung, April 2006.
[PQ12] Eriko Nurvidathi, November 2005.
[PQ11] Amit Singhee, April 2005.
[PQ10] Kay Yu, April 2005.
[PQ8] Patrick Bourke, November 2004.
[PQ7] Edward Lin, April 2004.
[PQ6] Yaoyao Xhu, November 2003.

[PQ5] Roland Wunderlich, November 2003.

[PQ4] Sooksan Panichpaiboon, April 2003.

[PQ3] Thomas Wenisch, April 2003.

[PQ2] Vikas Chandra, April 2003.

[PQ1] Fang Fang, April 2002.

RESEARCH COMMUNITY SERVICE

EDITORSHIPS

THE UNIVERSITY OF TEXAS AT AUSTIN

Guest Editor, *IEEE Journal on Selected Topics in Signal Processing,* Special Issue on Compact Deep Neural Networks with Industrial Applications, 2018-present.

Associate Editor, *IEEE Transactions on Computer-Aided Design,* 2019-present.

CARNEGIE MELLON UNIVERSITY

Associate Editor, *IEEE Transactions on Computers,* 2015-2019.

Associate Editor, *IEEE Computer Architecture Letters,* 2013-2015.

Associate Editor, *ACM Transactions on Design Automation of Electronic Systems,* 2010-2013.

Guest Editor, *ACM Transactions on Design Automation of Electronic Systems,* Special Section on Networks on Chip, 2013.

Guest Editor, *IEEE Transactions on Computer-Aided Design of Circuits and Systems*, Special Issue on Parallel CAD, 2011.

Associate Editor, *IEEE Transaction on VLSI Systems*, 2005-2011.

Guest Editor, *IEEE Transaction on VLSI Systems*, Special Section on Low Power Electronics and Design, 2007.

Editor-in-Chief, *ACM/SIGDA Newsletter*, 2002-2005.

Guest Editor, *IEEE MICRO Magazine*, Special Issue on Power and Complexity Aware Design, Oct. 2003.

GOVERNING BOARDS

THE UNIVERSITY OF TEXAS AT AUSTIN

Member, External Review Committee for Computer Engineering Department, University of California, Santa Barbara, 2020-present.

Member, Visiting Committee for Department of Electrical and Computer Engineering, Boston University, 2020-present.

Member, IEEE Fellow Selection Committee, 2019-present.

Member, ACM SIGARCH CARES Committee, 2019-present.

CARNEGIE MELLON UNIVERSITY

Member, IEEE Fellow Selection Committee, 2016-2019.

Member, ACM SIGARCH CARES Committee, 2019.

Member, IEEE Technical Activities Board Committee on Diversity and Inclusion, 2017-2019.

Chair, IEEE Transactions on Computers, Editorial Pick of the Year Committee (EPYC), 2016-2017.

Co-chair, IEEE Technical Activities Board Ad-Hoc Committee on Women and Underrepresented Minorities, 2016-2017.

Member, IEEE Computer Society Fellow Selection Committee, 2016.

Member, IEEE Computer Society Technical Achievement Award Committee, 2015.

Member, Marie R. Pistilli Women in EDA Achievement Award Selection Committee, 2015-present.

Awards Chair/Past Chair, Special Interest Group on Design Automation, Association for Computing Machinery (ACM-SIGDA), 2009-2012.

Chair, Special Interest Group on Design Automation, Association for Computing Machinery (ACM-SIGDA), 2005-2009.

Secretary, Executive Committee of the SIG Governing Board (SGB) of the Association for Computing Machinery (ACM), 2007-2010.

Vice-Chair for Special Interest Group (SIG) Development, Executive Committee of the SIG Governing Board (SGB) of the Association for Computing Machinery (ACM), 2006-2007.

Member, ACM Awards Committee (Outstanding Contributions to ACM Award Subcommittee), 2007-2010.

CONFERENCE COMMITTEES, BOARDS, AND PANEL REVIEWS

THE UNIVERSITY OF TEXAS AT AUSTIN

General Chair, *HiPEAC Conference*, 2020-2021.

National Science Foundation Panel Reviewer, 2019-present.

CARNEGIE MELLON UNIVERSITY

National Science Foundation Panel Reviewer, 2000-2019.

Past Chair, *IEEE/ACM Intl. Conference on Computer-Aided Design*, 2016.

General Chair, *IEEE/ACM Intl. Conference on Computer-Aided Design*, 2015.

General Chair *IEEE/ACM Intl. Symposium on Networks-on-Chip*, 2015.

Program Chair, *IEEE/ACM Intl. Conference on Computer-Aided Design*, 2014.

Vice Program Chair, *IEEE/ACM Intl. Conference on Computer-Aided Design*, 2013.

Technical Program Chair, *IEEE/ACM Intl. Symposium on Networks-on-Chip*, 2012.

Tutorial Chair, *IEEE/ACM Intl. Conference on Computer-Aided Design*, 2012.

Founder and Chair, *First CRA-W/CDC Workshop on Diversity in Design Automation and Test*, 2011.

Finance Chair, *IEEE/ACM Intl. Symposium on Networks-on-Chip,* 2011.

ACM/SIGDA Founding Chair, *ACM Student Research Competition at DAC,* 2010-2012.

ACM/SIGDA Representative, *IEEE/ACM Design, Automation, and Test in Europe Conference*, 2009-2012.

ACM/SIGDA Representative, *ACM/IEEE Design Automation Conference,* 2005-2009.

General Chair, *ACM/IEEE International Symposium on Low Power Electronics and Design,* 2007.

Technical Program Chair, *ACM/IEEE International Symposium on Low Power Electronics and Design,* 2006.

Exhibits Chair, *ACM/IEEE International Symposium on Low Power Electronics and Design,* 2001-2005.

Technical Program Chair, *ACM/IEEE International Workshop on Logic and Synthesis,* 2004.

General Chair, *ACM/IEEE International Workshop on Logic and Synthesis,* 2003.

Chair, Organizing Committee, *SIGDA Ph.D. Forum at Design Automation Conference,* 2002-2003.

Panel Chair, *ACM/IEEE International Workshop on Logic and Synthesis*, 2001-2002.

Panel Chair, *IEEE Computer Society Intl. Symposium on VLSI*, 2002-2004.

Publicity Chair, *IEEE Computer Society Annual Workshop on VLSI*, 2001.

TECHNICAL PROGRAM COMMITTEES – CONFERENCES AND SYMPOSIA

THE UNIVERSITY OF TEXAS AT AUSTIN

Member, Technical Program Committee, *Systems and Machine Learning Conference* (MLSys), 2020.

CARNEGIE MELLON UNIVERSITY

Member, Technical Program Committee, *ACM Intl. Symposium on Computer Architecture*, 2019, 2009, 2004.

Member, Technical Program Committee, *IEEE Design, Automation and Test in Europe Conference,* 2015-2016, 2012-2013, 2010, 2001-2003.

Member, Technical Program Committee, *IEEE/ACM Intl. Symposium on Networks on Chip*, 2010-2013.

Member, Technical Program Committee, *ACM/IEEE Intl. Symposium on Low Power Electronics and Design*, 2011-2012, 2002-2005.

Member, Technical Program Committee, *ACM/IEEE Intl. Conference on Computer-Aided Design,* 2011, 2007-2008 and 2001-2003.

Member, Technical Program Committee, *ACM/IEEE Design Automation Conference*, 2005-2008.

Member, Technical Program Committee, *ACM/IEEE Intl. Symp. on Microarchitecture*, 2006, 2008.

Member, Technical Program Committee, *IEEE Asian-South Pacific Design Automation Conference*, 2006-2007.

Member, Technical Program Committee, *Intl. Symposium on Asynchronous Circuits and Systems*, 2007, 2004-2005.

Member, Technical Program Committee, *Intl. Symp. on High Performance Computer Architecture,* 2005.

Member, Technical Program Committee, *Intl. Symposium on Circuits and Systems*, 2004.

Member, Technical Program Committee, *IEEE Intl. Conference on Computer Design*, 2002-2003.

Member, Technical Program Committee, *SIGDA Ph.D. Forum at Design Automation Conference,* 2001-2003.

WORKSHOP COMMITTEES AND BOARDS

THE UNIVERSITY OF TEXAS AT AUSTIN

Member, Steering Committee, *EMC^2 Workshop*, 2020-present.

CARNEGIE MELLON UNIVERSITY

Chair and Founder, *CRA-W/CDC Workshop on Diversity in Design Automation and Test*, 2011.

Technical Program Co-Chair, *Workshop on Micro Power Management for Macro Systems on Chip*, in conjunction with *Design, Automation and Test in Europe Conference*, 2011.

Technical Program Co-Chair, *Workshop on Complexity Effective Design,* in conjunction with *International Symposium on Computer Architecture*, 2002-2006.

Member, Organizing Committee, *Ph.D. Forum, Grace Hopper Celebration of Women in Computing,* 2004.

Technical Program Co-Chair, *Workshop on Compilers and Operating Systems on Low Power*, in conjunction with *IEEE Conference on Parallel Architectures and Compiling Technologies*, 2002-2003.

Technical Program Co-Chair, *Workshop on Modeling, Analysis and Middleware Support for Electronic Textiles,* in conjunction with *International Conference on Architectural Support for Programming Languages and Operating Systems,* 2002.

TECHNICAL PROGRAM COMMITTEES – WORKSHOPS

CARNEGIE MELLON UNIVERSITY

Member, Technical Program Committee of *ACM/IEEE International Workshop on Logic Synthesis,* 1999-2006.

Member, Technical Program Committee of the *Power Aware Computer Systems Workshop (in conjunction with ASPLOS or MICRO),* 2000, 2003-2004.

Member, Technical Program Committee of the *Formal Methods for GALS Systems Workshop (in conjunction with FME),* 2003.

Member, Technical Program Committee, *Workshop on Compilers and Operating Systems on Low Power,* in conjunction with *IEEE Conference on Parallel Architectures and Compiling Technologies,* 2001.

REVIEWING ACTIVITIES

IEEE Trans. on Computer-Aided Design of Integrated Circuits
*IEEE Trans. on Computer*s
IEEE Trans. on VLSI Systems
IEEE Trans. on Circuits and Systems II
IEEE MICRO
ACM Trans. on Design Automation of Electronic Systems
ACM Trans. on Embedded Computing Systems
ACM Journal of Emerging Technologies
Foundations and Trends in EDA
Journal of System Architecture
ACM/IEEE Design Automation Conference
IEEE/ACM International Conference on Computer-Aided Design
IEEE/ACM Design, Automation, and Test in Europe Conference
ACM/IEEE International Symposium on Computer Architecture
IEEE/ACM International Symposium on Microarchitecture
IEEE International Symposium on High Performance Computer Architecture
ACM/IEEE Embedded Systems Week – CODES/ISSS
ACM/IEEE International Symposium on Low-Power Electronics and Design
IEEE/ACM International Symposium on NoC Systems
IEEE International Symposium on Asynchronous Circuits and Systems
IEEE International Symposium on Circuits and Systems
IEEE International Conference on Computer Design
ACM/IEEE International Workshop on Logic Synthesis

TECHNICAL SOCIETIES

Fellow (2019) and Member (1997-present), *Association for Computing Machinery*

Fellow (2014) and Member (1994-present), *Institute of Electrical and Electronics Engineers*

Member of *American Association for the Advancement of Science* (2012-present)

Member of *IEEE-Circuits and Systems* Society and *IEEE-Computer* Society (since 1994)

Member of *ACM-Special Interest Group on Design Automation* (since 1997)

Member of *ACM-Special Interest Group on Computer Architecture* (since 2001)

Member of *ACM-Special Interest Group on Microarchitecture* (since 2005)

UNIVERSITY SERVICE AND ADMINISTRATION

THE UNIVERSITY OF TEXAS AT AUSTIN

Department Chair, Electrical and Computer Engineering, 2019-present.

CARNEGIE MELLON UNIVERSITY

Vice Co-Chair, Task Force on CMU Experience, CMU, 2018-2019.

Chair, CMU Faculty Affairs Council, 2018-2019.

Member, CMU Faculty Senate Executive Committee, 2018-2019.

Member, Department of ECE Outreach, Inclusion, and Diversity Committee, 2017-2019.

Member, Department of ECE Faculty Search Committee, 2015-2019.

Founding Director, Center for Faculty Success, College of Engineering, CMU, 2014-2019.

Co-Chair, CMU Faculty Diversity, Inclusion, and Development Committee, 2015-2019.

Member, CyLab Director Search Committee, 2018.

Member, CMU Provost Search Committee, 2018.

Associate Department Head for Academic Affairs, CMU ECE, 2014-2018.

Member, CMU Faculty Affairs Council, 2017-2018.

Member, CMU Semiconductor Research Corporation Undergraduate Research Opportunities Selection Committee, 2009-2017.

Member, CMU Faculty Review Committee, 2011-2016.

Member, CMU Strategic Planning Diversity Horizontal, 2015.

Member, CMU Research Review Committee, 2013-2015.

Member, CMU Faculty Senate Nominating Committee, 2010-2014.

Chair, Department of ECE Graduate Studies Committee, 2011-2014.

Member, Department of ECE Head Search Committee, 2013.

Member, CMU College-level Ad-Hoc Promotion and Tenure Committee, 2011-2012.

Member, CMU University-level Non-Tenure Promotions Committee, 2009-2011.

Member, CMU Faculty Senate, 2007-2011.

Member, Department of ECE Graduate Studies Committee, 2005-2011

Member, Department of ECE Head Search Committee, 2004-2005.

Member, Department of ECE Undergraduate Advising Committee, 2004-2005.

Member, Department of ECE Undergraduate Studies Committee, 2003-2004.

Member, Department of ECE Seminar Committee, 2001-2003.