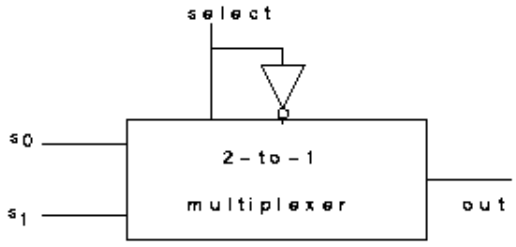
EE382M-7 VLSI I
Spring 2009 (Prof. David Pan)

Homework #1: Assigned Jan. 27, due Feb. 3

1. Minimize the following Boolean equations to eliminate redundancy (a' means the complement of a).
   a) ac + bdc + ca'
   b) (x+y)(x+z)
   c) a(b+c+d) + b(c+d+a) + c(d+a+b) + d(a+b+c)

2. Sketch the transistor-level schematic for a single-stage CMOS logic gate for the function, Y = (AB + C.(A + B))'

3. This problem relates to the design of circuits using multiplexer modules. A 2-to-1 multiplexer module is shown below (the transistor circuit for this was discussed in class). Three of these modules can be combined to produce a 4-to-1 multiplexer. Any 2-input logic function can be implemented using this 4-to-1 multiplexer with the two inputs fed to the select line and the truth table entries appropriately fed to the input lines. However, a 4-to-1 multiplexer can also implement a 3-input logic function if the complement of one of the inputs is also available.
   You are to implement the logic function given below using three of the 2-to-1 multiplexer modules.



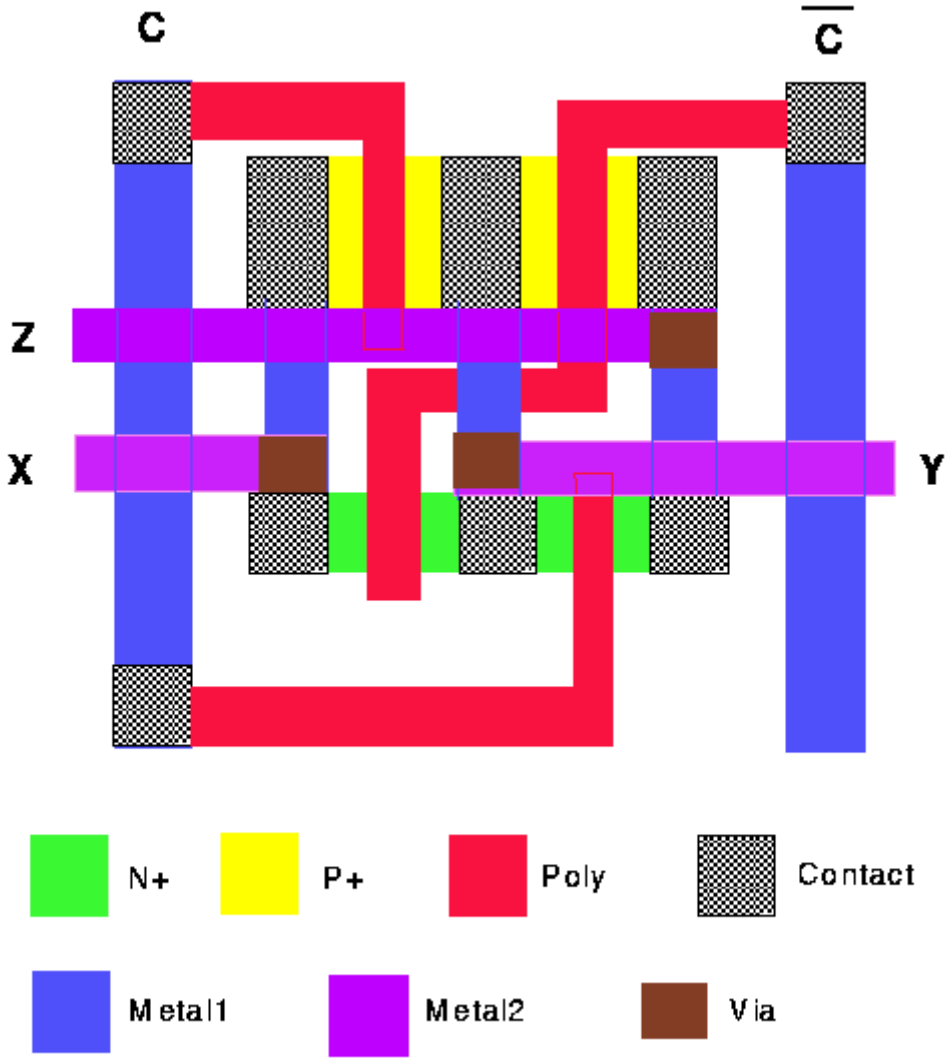
select	out
0	s_0
1	s_1

a	b	c	z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

   (a) Design a gate-level implementation of the above function using multiplexer modules made of NAND/NOR gates.

(b) How many transistors are needed for the gate level implementation?
(c) If the same function is implemented using multiplexers with transmission gates, what would be the number of transistors needed for this implementation?

4. Draw the transistor schematic representing the circuit below. Can you describe the function of the circuit?



Is this cell easy to "tile" in the vertical direction? The horizontal direction? Explain.

5. Problem 1.3 from the Exercises for Chapter 1.

6. Problem 1.8 from the Exercises for Chapter 1.