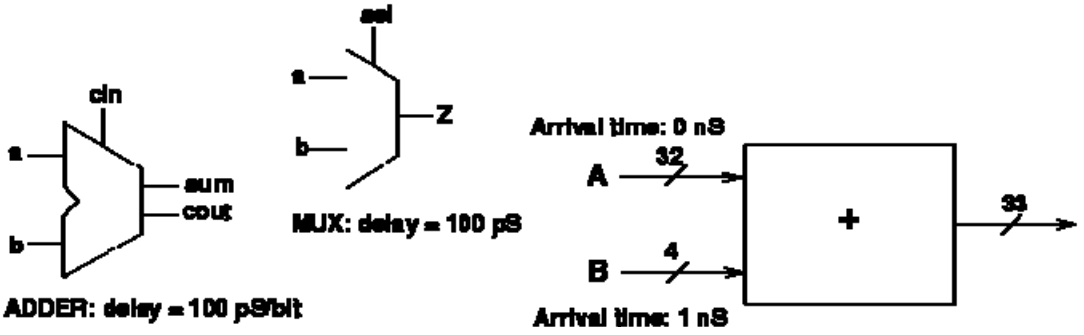
VLSI I

Spring 2009 (Prof. David Pan)

Homework #4: Assigned Feb. 17, due Feb 24

1. Problem 4.19 from the Exercises for Chapter 4.
2. Problem 4.24 from the Exercises for Chapter 4.
3. Problem 4.28 from the Exercises for Chapter 4.
4. Problem 6.10 from the Exercises for Chapter 6.
5. Problem 6.12 from the Exercises for Chapter 6.
6. Problem 10.2 from the Exercises for Chapter 10. Please pay attention to the Errata: Change last sentence to "… function of the most significant bits of the two inputs and the output." (DH) http://www.cmosvlsi.com/errata.pdf
7. Problem 10.3 from the Exercises for Chapter 10. Please pay attention to the Errata: Change last sentence to "…function of the sub signal and the most significant bits of the two inputs and the output." (DH)
8. This problem is to design a fast **addition circuit (+)** to add a 32-bit number with a 4-bit number (to produce a 33-bit number). The circuit should be designed with two macros (shown below): an adder macro (adds numbers of a specified bit-width) which produces an adder with a delay of 100 pS/bit, and a multiplexer (which selects from inputs of specified bit width) which has a delay of 100 pS (independent of the size). The arrival times of the input signals to the circuit are also shown below.



Design the circuits for the following specifications, and show the interconnection of the modules below to meet the specs. Make sure that the you show the appropriate bits for the inputs to the modules. (You may not need to use all the modules for a solution, or you may need to add additional modules. Do NOT add any other logic other than the two modules.)

(a) Design a circuit to complete the addition in <= 3 nS.

(b) Design a circuit to complete the addition in <= 2 nS.