# VLSI I

## Spring 2009 (Prof. David Pan)

## Homework #5: Assigned Feb. 26, due Mar 5

1. Problem 7.1 from the Exercises for Chapter 7.

2. Problem 7.2 from the Exercises for Chapter 7.

3. Problem 7.3 from the Exercises for Chapter 7.

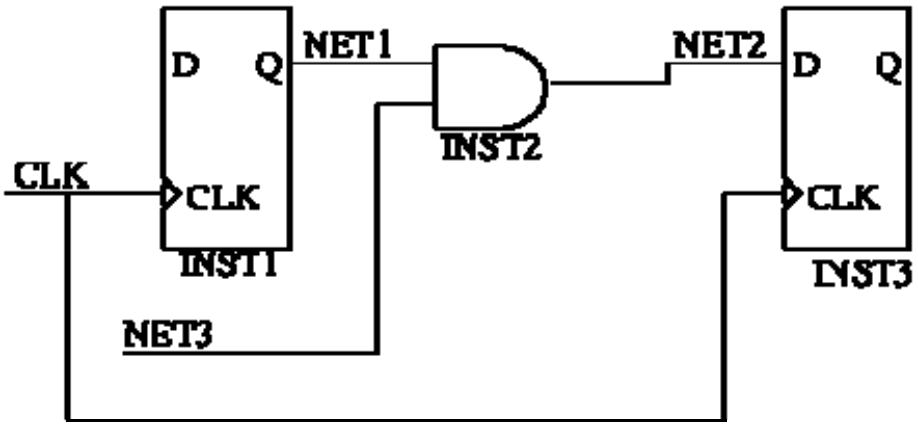
4. Problem 7.4 from the Exercises for Chapter 7.

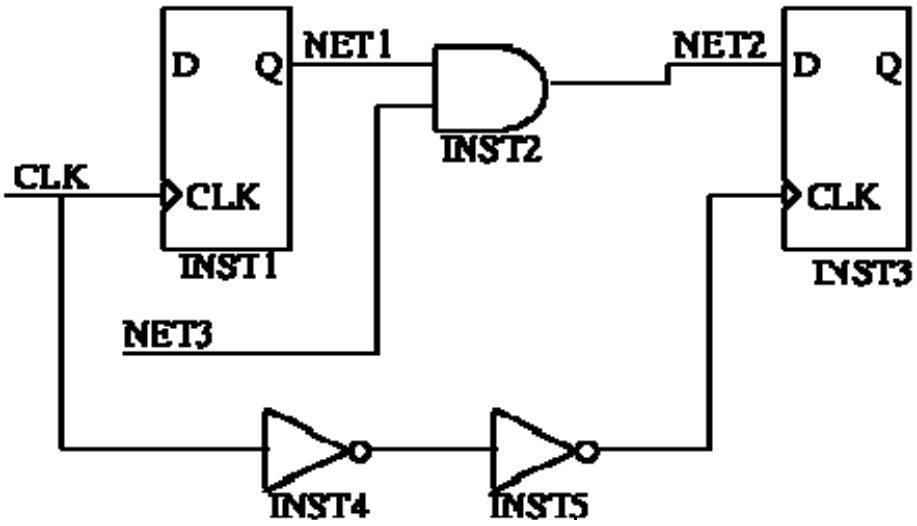
5. Problem 7.5 from the Exercises for Chapter 7.

6. Problem 7.6 from the Exercises for Chapter 7.

7. Identify if there are any hold time problems from INST1 to INST3 in the following two circuits. If there are any, indicate by how much the hold time is violated. Indicate a solution to any hold-time violation.

| | Rise | Fall |
|---|---|---|
| CLK -> Q | 500ps | 500ps |
| Flop Hold Time | 750ps | 750ps |
| And Gate | 300ps | 200ps |
| Inverter Gate | 50ps | 20ps |






8. The flip-flop in the figure below has the delays of the various components labeled (delay of the NAND gate is G1, etc.) Find the approximate **setup time**, **hold time** and **clock-to-QB delay** in terms of the delays of the basic gates and inverters (example, delay = G1 + I2). Use the single value of delay (I3 and I4) for the dynamic and clocked inverters shown at the transistor level.