VLSI I

Spring 2009 (Prof. David Pan)

Homework #6: Assigned Mar. 26, due April 2

1. Problem 6.27 from the Exercises for Chapter 6.

2. Problem 6.31 from the Exercises for Chapter 6.

3. Problem 6.32 from the Exercises for Chapter 6.

4. Problem 6.33 from the Exercises for Chapter 6.

5. Design the carry function for a full adder (C = AB + AC + BC) using standard **Domino CMOS Logic**, with the restriction that there are only three transistors (including clocking transistors) from any output node to ground.