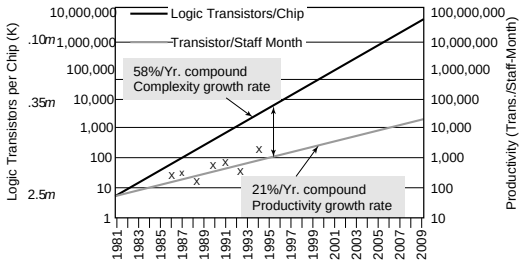
12. Design Styles

- Last module:
  - Floorplanning
  - Sequential circuit design
  - Clock skew
- This module
  - Custom and semi-custom design
  - Array-based implementations

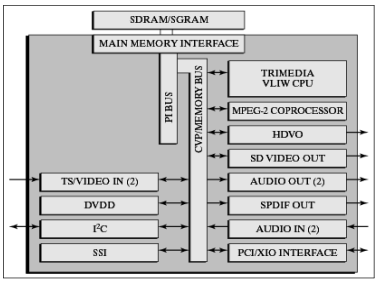
The Design Productivity Challenge



A growing gap between design complexity and design productivity

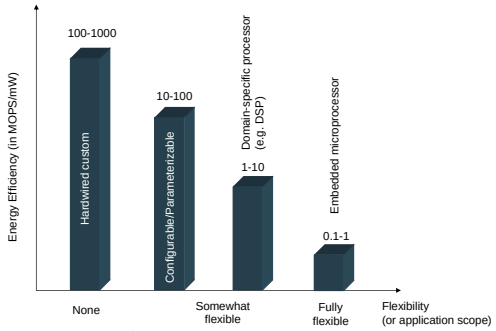
Source: sematech97

A System-on-a-Chip: Example

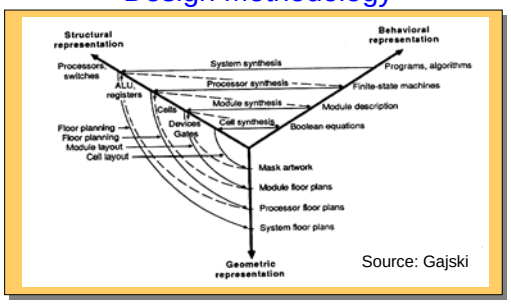


Courtesy: Philips

Impact of Implementation Choices

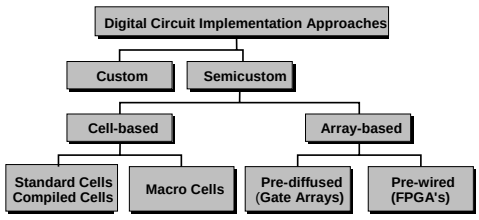


Design Methodology

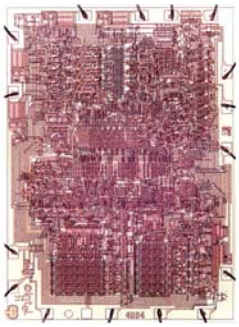


- Design process traverses iteratively between three abstractions: behavior, structure, and geometry
- More and more automation for each of these steps

Implementation Choices



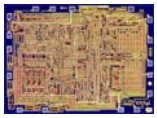
The Custom Approach



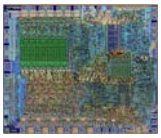
Intel 4004

Courtesy Intel

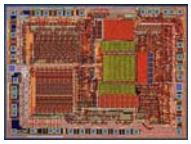
Transition to Automation and Regular Structures



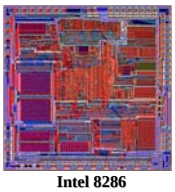
Intel 4004 ('71)



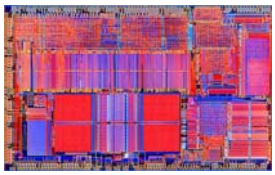
Intel 8080



Intel 8085



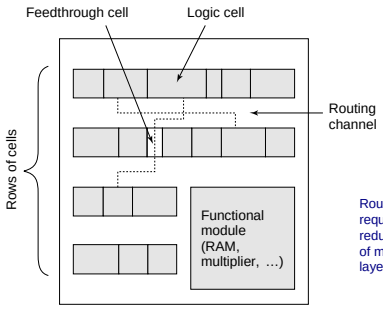
Intel 8286



Courtesy Intel

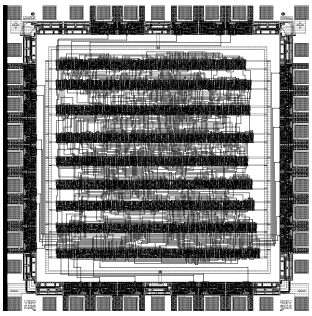
Intel 8486

Cell-based Design (or standard cells)



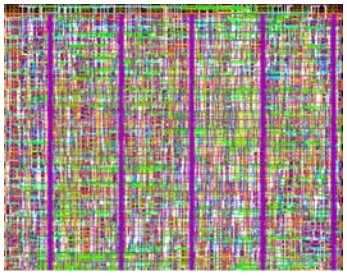
Routing channel requirements are reduced by presence of more interconnect layers

Standard Cell — Example



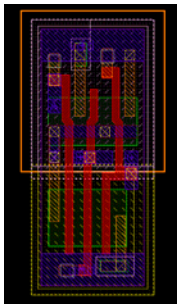
[Brodersen92]

Standard Cell – The New Generation



Cell-structure hidden under interconnect layers

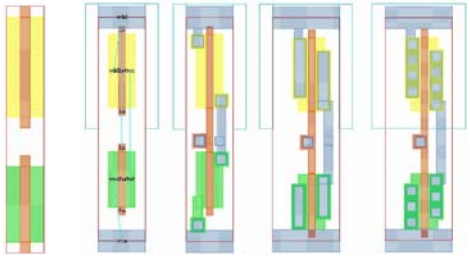
Standard Cell - Example



Path	1.2V - 125°C	1.6V - 40°C
$In1—t_{pLH}$	0.073+7.98C+0.317T	0.020+2.73C+0.253T
$In1—t_{pHL}$	0.069+8.43C+0.364T	0.018+2.14C+0.292T
$In2—t_{pLH}$	0.101+7.97C+0.318T	0.026+2.38C+0.255T
$In2—t_{pHL}$	0.097+8.42C+0.325T	0.023+2.14C+0.269T
$In3—t_{pLH}$	0.120+8.00C+0.318T	0.031+2.37C+0.258T
$In3—t_{pHL}$	0.110+8.41C+0.280T	0.027+2.15C+0.223T

3-input NAND cell
(from ST Microelectronics):
C = Load capacitance
T = input rise/fall time

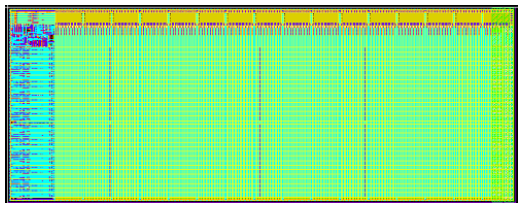
Automatic Cell Generation



Initial transistor geometries | Placed transistors | Routed cell | Compacted cell | Finished cell

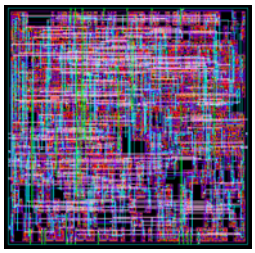
Courtesy Cadabra

MacroModules



256×32 (or 8192 bit) SRAM
Generated by hard-macro module generator

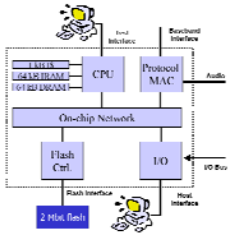
"Soft" MacroModules

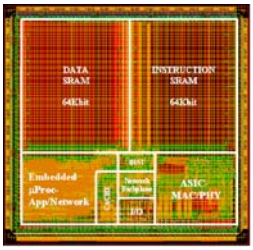


```
string mat = "booth";
directive (multtype = mat);
output signed [16] Z = A * B;
```

Synopsys DesignCompiler

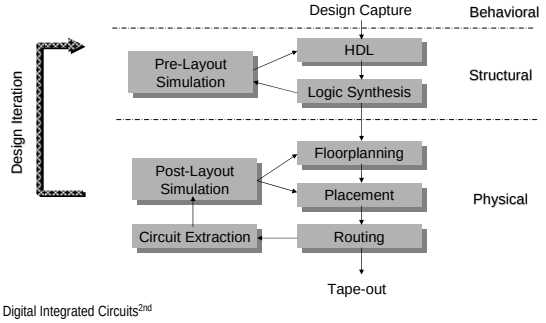
"Intellectual Property" (IP) Cores



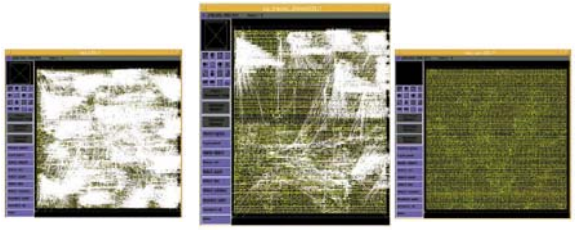


A Protocol Processor for Wireless

Semicustom Design Flow



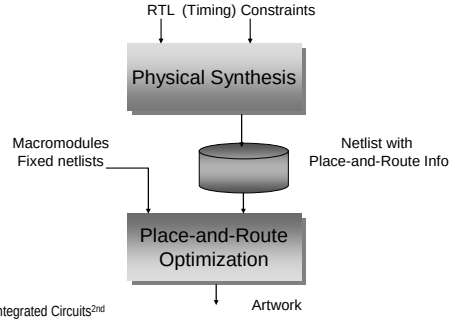
The "Design Closure" Problem



Iterative Removal of Timing Violations (white lines)

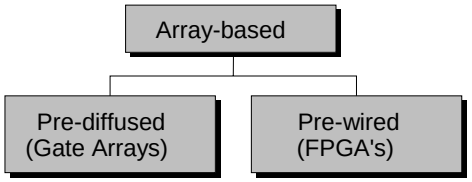
Courtesy Synopsys

Integrating Synthesis with Physical Design



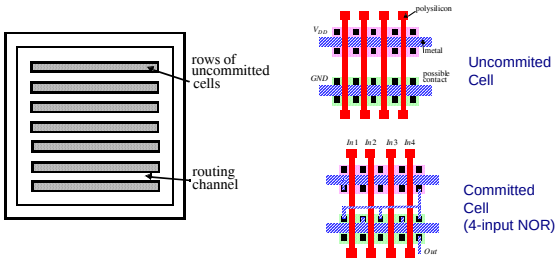
D. Z. Pan 12. Design Styles 19

Late-Binding Implementation



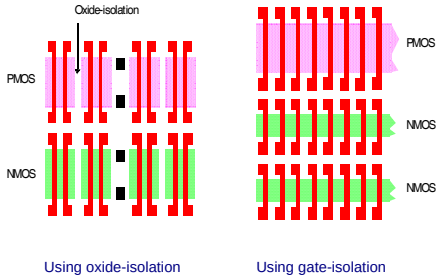
D. Z. Pan 12. Design Styles 20

Gate Array — Sea-of-gates



D. Z. Pan 12. Design Styles 21

Sea-of-gate Primitive Cells



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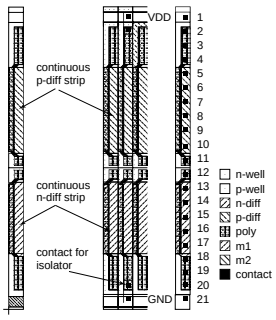
Example: Base Cell of Gate-Isolated GA



From Smith97

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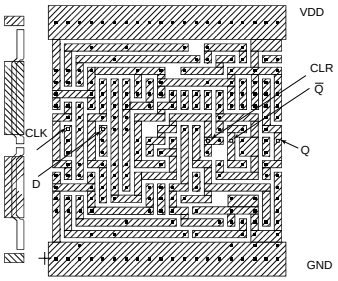
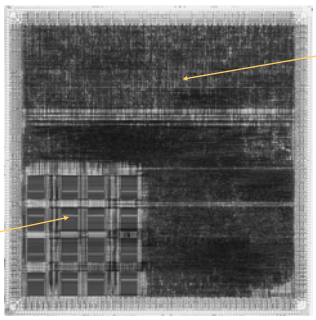
Example: Flip-Flop in Gate-Isolated GA



From Smith97

D. Z. Pan 12. Design Styles 24

Sea-of-gates



LSI Logic LEA300K (0.6 μm CMOS)

Courtesy LSI Logic

Prewired Arrays

Classification of prewired arrays (or field-programmable devices):

- Based on Programming Technique
  - Fuse-based (program-once)
  - Non-volatile EPROM based
  - RAM based
- Programmable Logic Style
  - Array-Based
  - Look-up Table
- Programmable Interconnect Style
  - Channel-routing
  - Mesh networks