16. Deep Submicron (DSM) Issues

- Last module:
  - Pass transistor logic
  - Pseudo nMOS logic
  - Dynamic logic
  - Domino circuits
- This module
  - Transistor I-V Review
  - Nonideal Transistor Behavior
  - Process and Environmental Variations

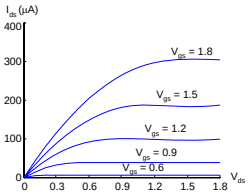
Ideal Transistor I-V

- *Shockley* 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

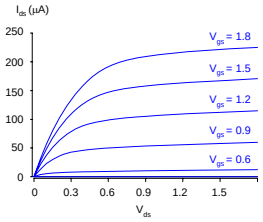
Ideal nMOS I-V Plot

- 180 nm TSMC process
- Ideal Models
  - β = 155(W/L) μA/V²
  - V_t = 0.4 V
  - V_{DD} = 1.8 V



Simulated nMOS I-V Plot

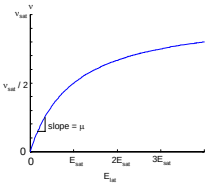
- 180 nm TSMC process
- BSIM 3v3 SPICE models
- What differs?
  - Less ON current
  - No square law
  - Current increases in saturation



Velocity Saturation

- We assumed carrier velocity ∝ E-field
  - $v = \mu E_{lat} = \mu V_{ds}/L$
- At high fields, this ceases to be true
  - Carriers scatter off atoms
  - Velocity reaches v_{sat}
    - Electrons: 6-10 x 10^6 cm/s
    - Holes: 4-8 x 10^6 cm/s
  - Better model

$$v = \frac{\mu E_{lat}}{1 + \frac{E_{lat}}{E_{sat}}} \Rightarrow v_{sat} = \mu E_{sat}$$



Velocity Saturation I-V Effects

- Ideal transistor ON current increases with V_{DD}^2

$$I_{ds} = \mu C_{ox}\frac{W}{L}\frac{\left(V_{gs} - V_t\right)^2}{2} = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

- Velocity-saturated ON current increases with V_{DD}

$$I_{ds} = C_{ox} W \left(V_{gs} - V_t\right) v_{max}$$

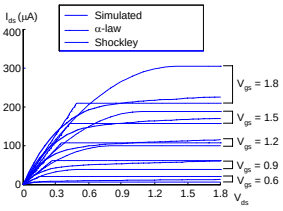
- Real transistors are partially velocity saturated
  - Approximate with α-power law model
  - $I_{ds} \propto V_{DD}^{\alpha}$
  - $1 < \alpha < 2$ determined empirically

α-Power Model

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ I_{dsat}\dfrac{V_{ds}}{V_{dsat}} & V_{ds} < V_{dsat} \quad \text{linear} \\ I_{dsat} & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

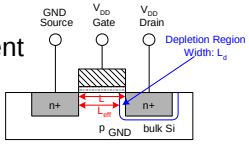
$$I_{dsat} = P_c \frac{\beta}{2}\left(V_{gs} - V_t\right)^{\alpha}$$

$$V_{dsat} = P_v \left(V_{gs} - V_t\right)^{\alpha/2}$$



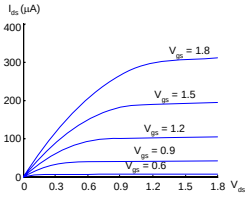
Channel Length Modulation

- Reverse-biased p-n junctions form a *depletion region*
  - Region between n and p with no carriers
  - Width of depletion L_d region grows with reverse bias
  - $L_{eff} = L - L_d$
- Shorter L_{eff} = more current
  - I_{ds} increases with V_{ds}
  - Even in saturation



Channel Length Modulation I-V

$$I_{ds} = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2\left(1 + \lambda V_{ds}\right)$$



- λ = *channel length modulation coefficient*
  - not feature size
  - Empirically fit to I-V characteristics

Body Effect

- Body is an implicit fourth terminal
- V_t: gate voltage necessary to invert channel
- The potential difference V_{sb} between the source and body affects V_t
- Increase in V_t with V_{sb} is called the *body effect*
- Body bias is a post-silicon tuning technique

Body Effect Model

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

- ϕ_s = *surface potential* at threshold

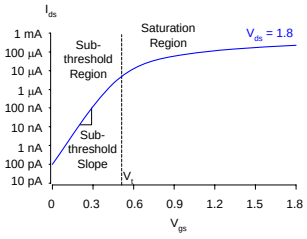
$$\phi_s = 2v_T \ln\frac{N_A}{n_i}$$

  - Depends on doping level N_A
  - And intrinsic carrier concentration n_i
- γ = *body effect coefficient*

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si}N_A} = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

OFF Transistor Behavior

- What about current in cutoff?
- Simulated results
- What differs?
  - Current doesn't go to 0 in cutoff



Leakage Sources

- Subthreshold conduction
  - Transistors can't abruptly turn ON or OFF
- Junction leakage
  - Reverse-biased PN junction diode current
- Gate leakage
  - Tunneling through ultra-thin gate dielectric
- Subthreshold leakage is the biggest source in modern transistors

Subthreshold Leakage

- Subthreshold leakage exponential with V_{gs}

$$I_{ds} = I_{ds0} e^{\frac{V_{gs}-V_t}{nv_T}} \left(1 - e^{\frac{-V_{ds}}{v_T}}\right) \quad I_{ds0} = \beta v_T^2 e^{1.8}$$

- n is process dependent, typically 1.4-1.5

DIBL

- Drain-Induced Barrier Lowering
  - Drain voltage also affect V_t

$$V_t' = V_t - \eta V_{ds}$$

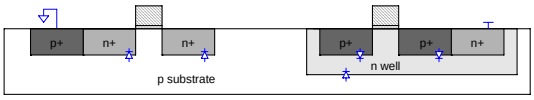
  - High drain voltage causes subthreshold leakage to increase
  - Effect is especially pronounced in short-channel transistors

Junction Leakage

- Reverse-biased p-n junctions have some leakage

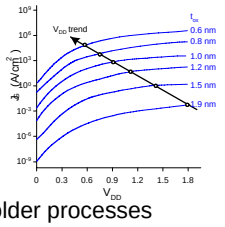
$$I_D = I_S \left(e^{\frac{V_D}{v_T}} - 1\right)$$

- I_s depends on doping levels
  - And area and perimeter of diffusion regions
  - Typically < 1 fA/μm²



Gate Tunneling Leakage

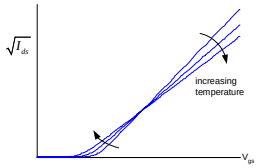
- Carriers may tunnel thorough very thin gate oxides
- Predicted tunneling current (from [Song01])



- Negligible for older processes
- May soon be critically important
  - Intel/IBM high-K dielectric material news 02/07

Temperature Sensitivity

- Increasing temperature
  - Reduces mobility
  - Reduces V_t
- I_{ON} decreases with temperature
- I_{OFF} increases with temperature

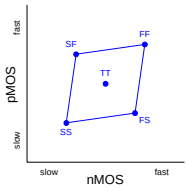


So What?

- So what if transistors are not ideal?
  - They still behave like switches.
- But these effects matter for…
  - Supply voltage choice
  - Logical effort
  - Quiescent/leakage power consumption
  - Pass transistors
  - Temperature of operation

Parameter Variation

- Transistors have uncertainty in parameters
  - Process: L_{eff}, V_t, t_{ox} of nMOS and pMOS
  - Vary around typical (T) values
- Fast (F)
  - L_{eff}: short
  - V_t: low
  - t_{ox}: thin
- Slow (S): opposite



- Not all parameters are independent for nMOS and pMOS

Environmental Variation

- V_{DD} and Temp also vary in time and space
- Fast:
  - V_{DD}: high
  - Temp: low

Corner	Voltage	Temperature
F (fast)	1.98	0 C
T (typical)	1.8	70 C
S (slow)	1.62	125 C

Process Corners

- Process corners describe worst case variations
  - If a design works in all corners, it will probably work for any variation.
- Describe corner with letters (T, F, S)
  - nMOS speed
  - pMOS speed
  - Voltage
  - Temperature

Important Corners

- Some critical simulation corners include

Purpose	nMOS	pMOS	V_{DD}	Temp
Cycle time	S	S	S	S
Power	F	F	F	F
Subthreshold leakage	F	F	F	S
Pseudo-nMOS	S	F	?	?