UT Austin, ECE Department

VLSI Design

2. CMOS Fabrication, Layout Rules

2. CMOS Fabrication, Layout, Design Rules

- Last module:
  - Introduction to the course
  - How a transistor works
  - CMOS transistors

This module:
  - CMOS Fabrication
  - Design Rules

CMOS Fabrication

- CMOS transistors are fabricated on silicon wafers
- Lithography process has been the mainstream chip manufacturing process
  - Similar to printing press
  - See Chris Mack's page for a nice litho tutorial
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

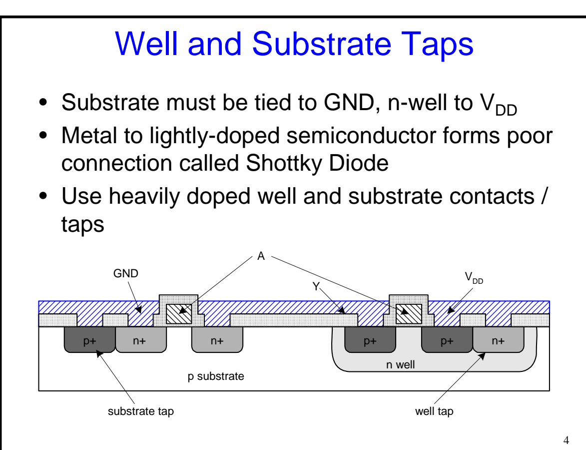
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors

GND
A
Y
V_{DD}
n+
n+
p+
p+
p substrate
n well
nMOS transistor
pMOS transistor
SiO_2
n+ diffusion
p+ diffusion
polysilicon
metal1

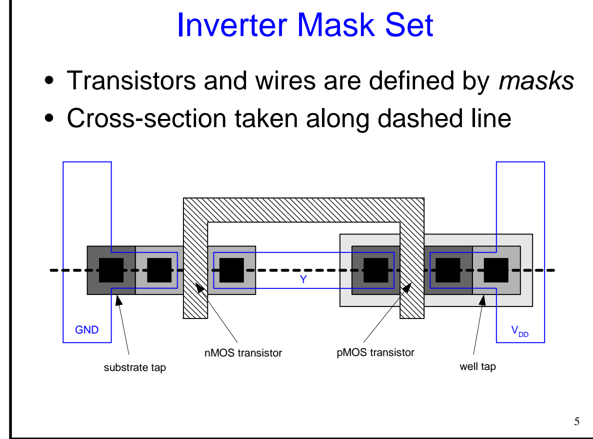
Well and Substrate Taps

- Substrate must be tied to GND, n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



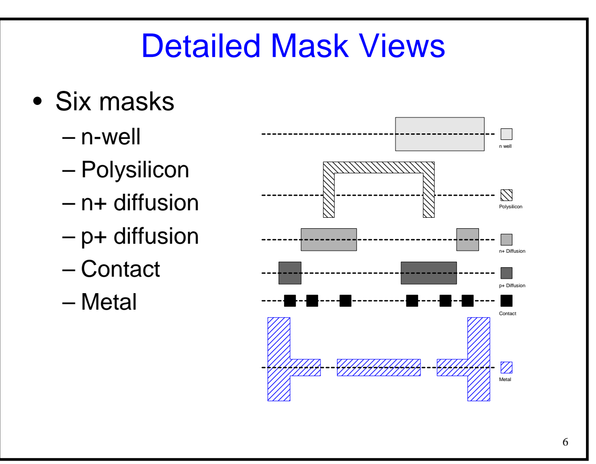
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal



Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

p substrate

7

Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 C with H_2O or O_2 in oxidation furnace

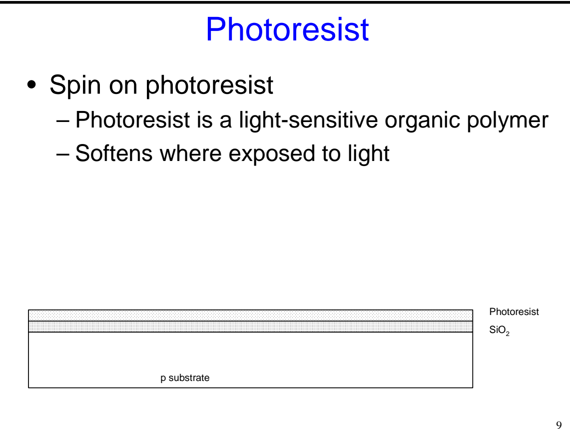
SiO_2

p substrate

8

Photoresist

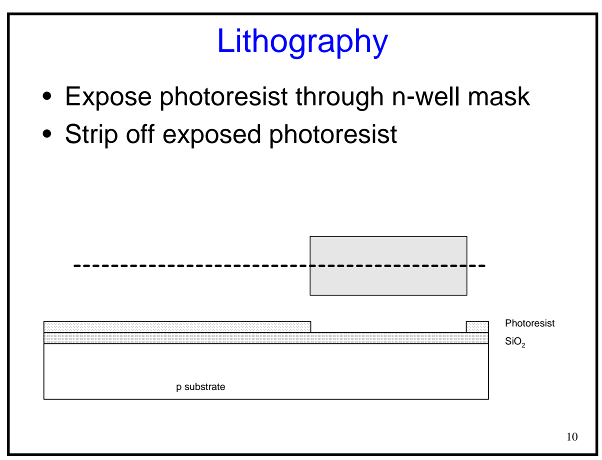
- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



9

Lithography

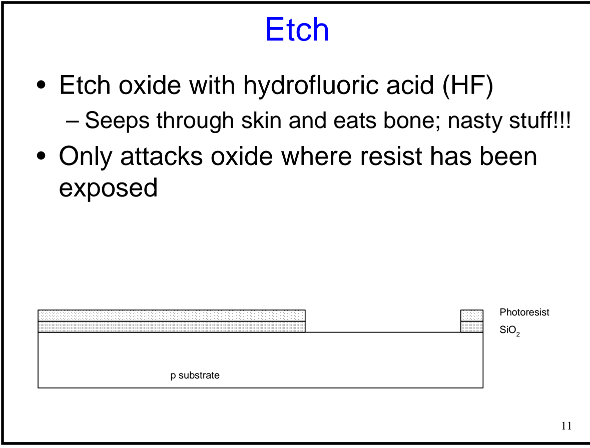
- Expose photoresist through n-well mask
- Strip off exposed photoresist



10

Etch

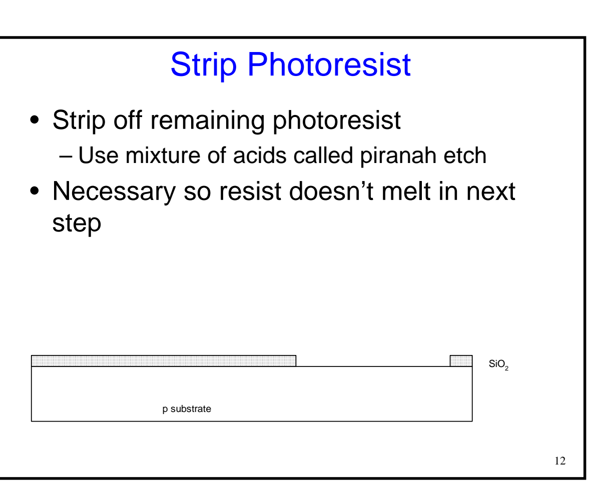
- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed



11

Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn’t melt in next step



12

n-Well

- n-well formed with diffusion or ion implant
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si

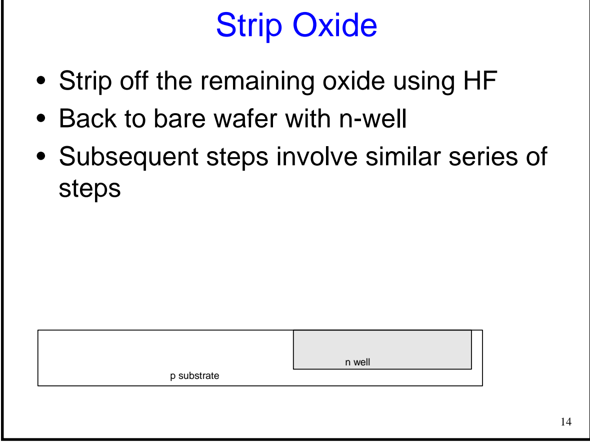
SiO_2

n well

13

Strip Oxide

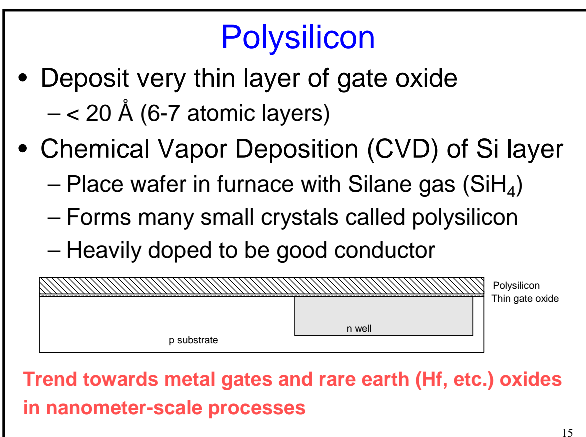
- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps



14

Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of Si layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor

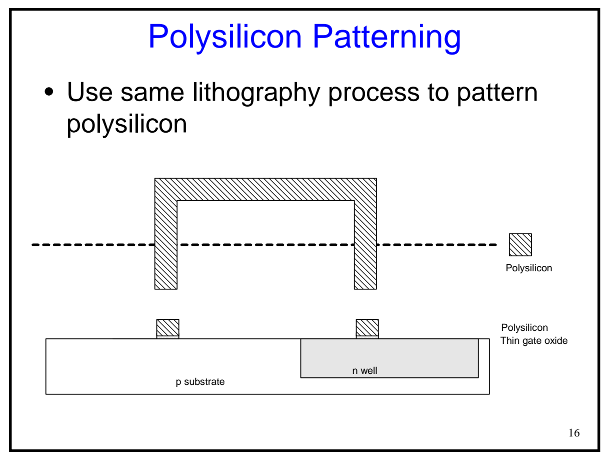


Trend towards metal gates and rare earth (Hf, etc.) oxides in nanometer-scale processes

15

Polysilicon Patterning

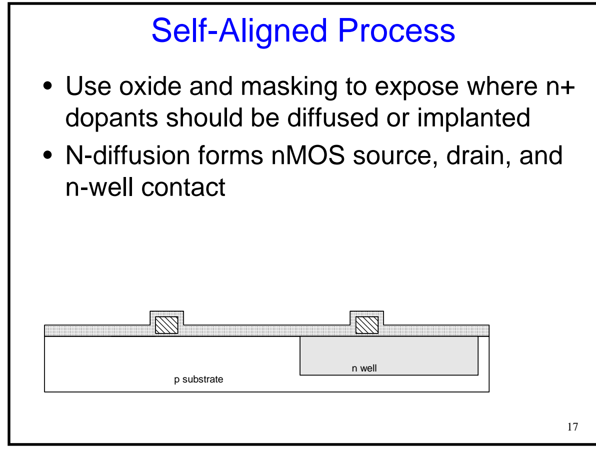
- Use same lithography process to pattern polysilicon



16

Self-Aligned Process

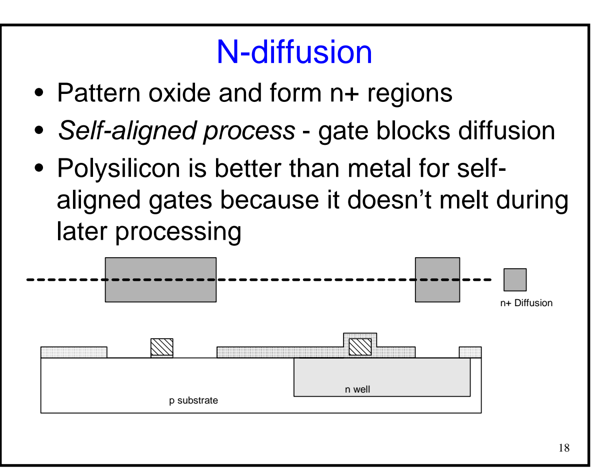
- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



17

N-diffusion

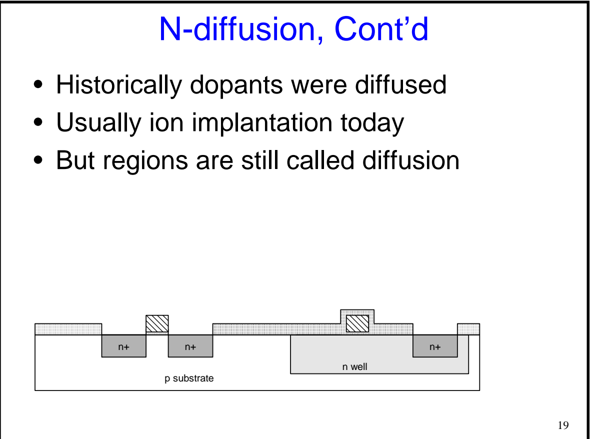
- Pattern oxide and form n+ regions
- *Self-aligned process* - gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



18

N-diffusion, Cont'd

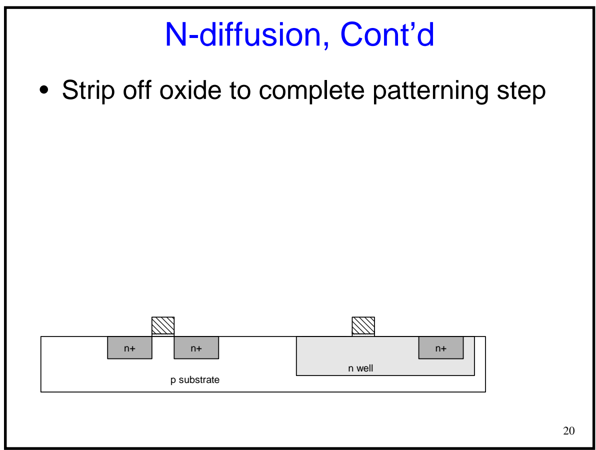
- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



19

N-diffusion, Cont'd

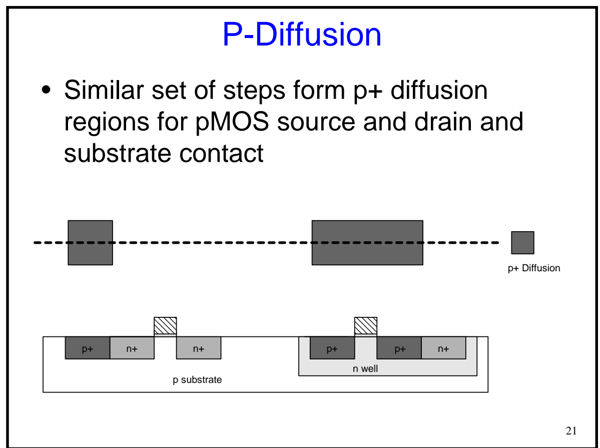
- Strip off oxide to complete patterning step



20

P-Diffusion

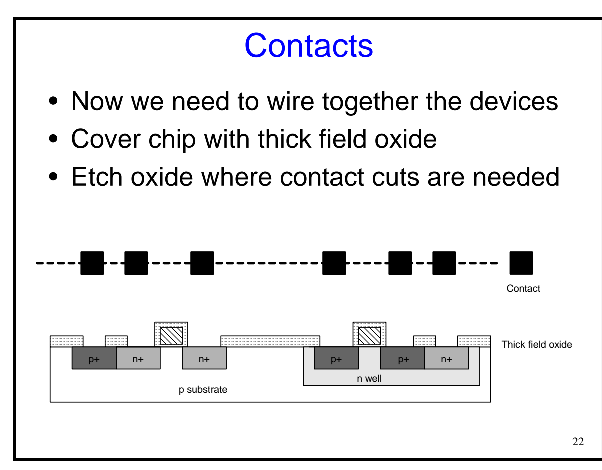
- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



21

Contacts

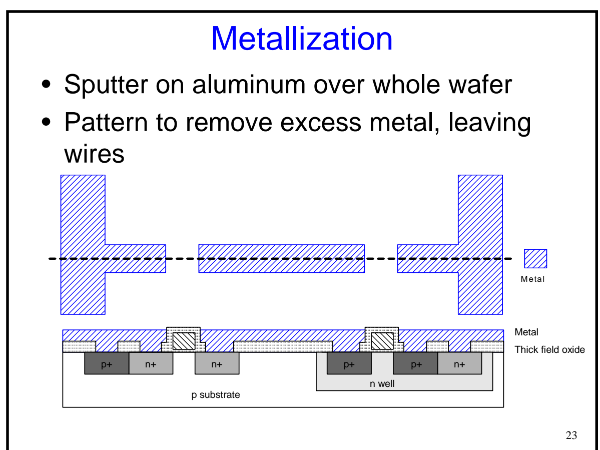
- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



22

Metallization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires



23

Layout

- Describes actual layers and geometry on the silicon substrate to implement a function
- Need to define transistors, interconnection
  - Transistor widths (for performance)
  - Spacing, interconnect widths, to reduce defects, satisfy power requirements
  - Contacts (between poly or active and metal), and vias (between metal layers)
  - Wells and their contacts (to power or ground)
- Layout of lower-level cells constrained by higher-level requirements: "**floorplanning**"
  - "**design iteration**"

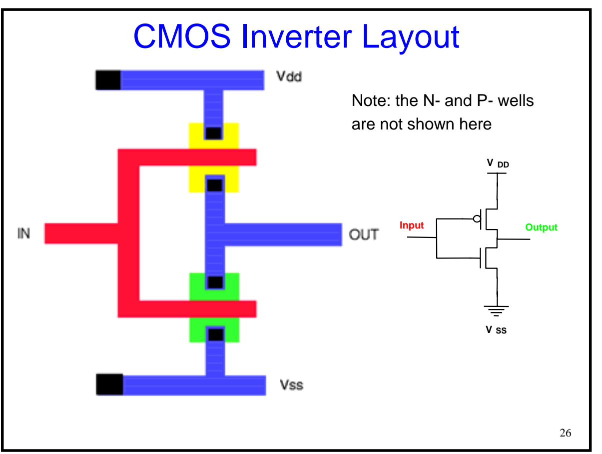
24

Layout, Cont'd

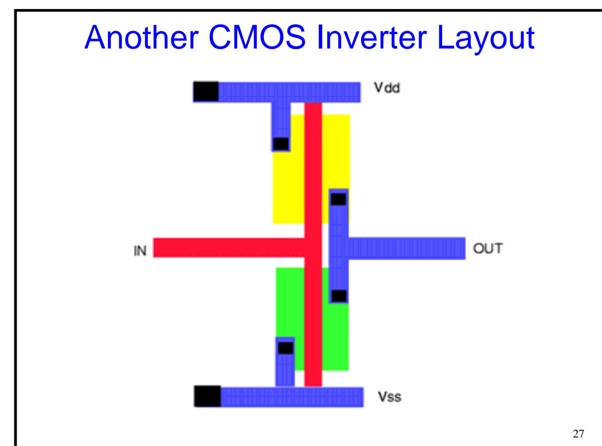
- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size f = distance between source and drain
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. $\lambda = 0.3\ \mu m$ in $0.6\ \mu m$ process

25

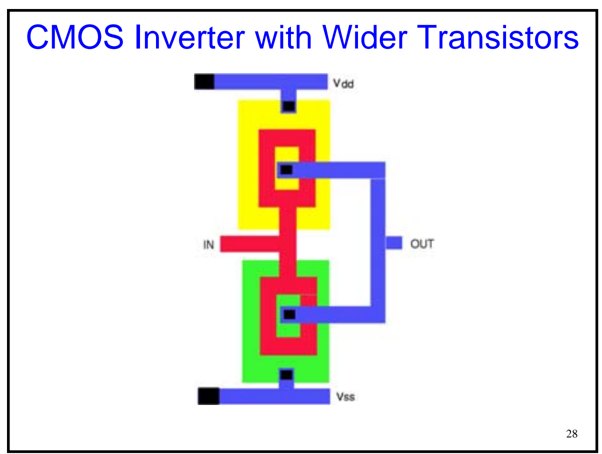
CMOS Inverter Layout



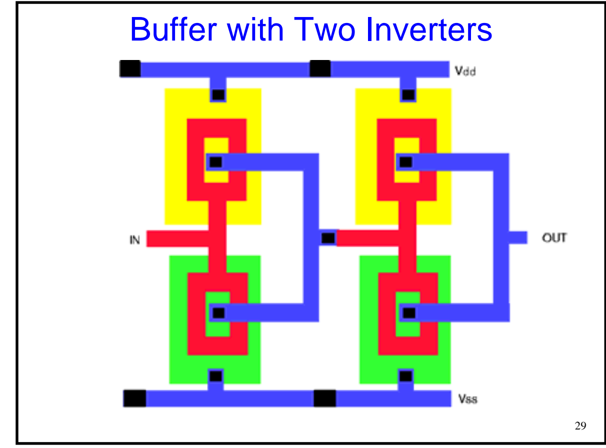
Another CMOS Inverter Layout



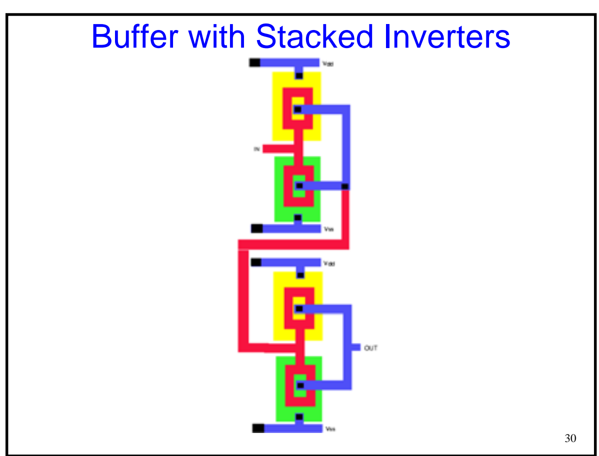
CMOS Inverter with Wider Transistors



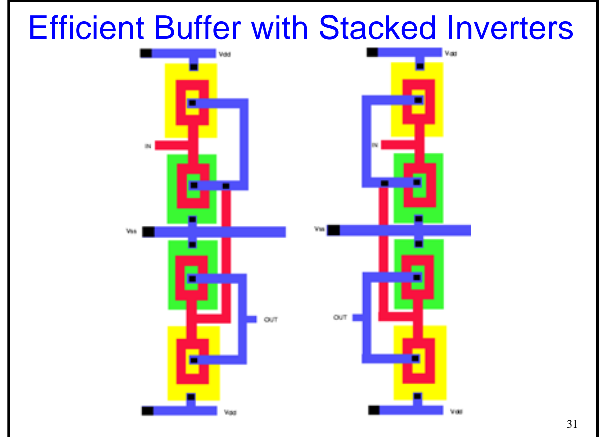
Buffer with Two Inverters



Buffer with Stacked Inverters

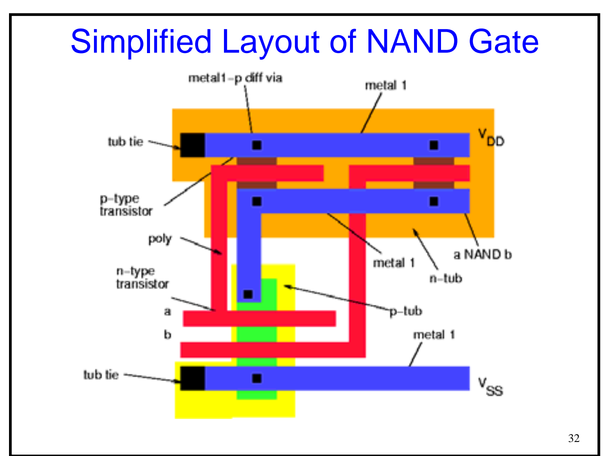


Efficient Buffer with Stacked Inverters



31

Simplified Layout of NAND Gate



32

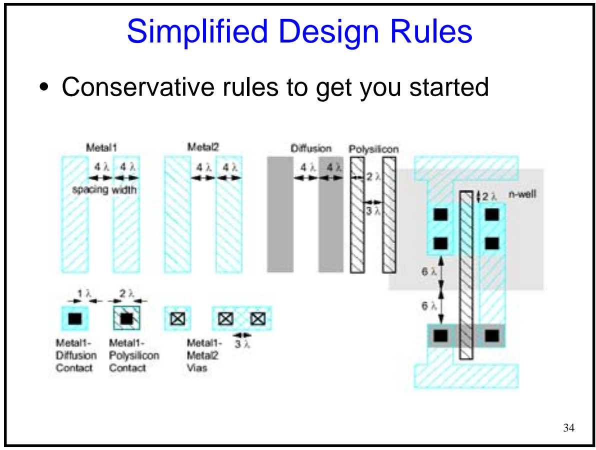
"Stick" Diagram for NAND Gate

- Identifies actual layers, can be annotated with transistor sizes

33

Simplified Design Rules

- Conservative rules to get you started



34

Inverter Layout

- Transistor dimensions specified as Width / Length
  - Minimum size 4λ / 2λ, sometimes called 1 unit
  - In f = 0.6 μm process, this is 1.2 μm wide, 0.6 μm long

V_{DD} A Y GND

8/2 4/2

2 1

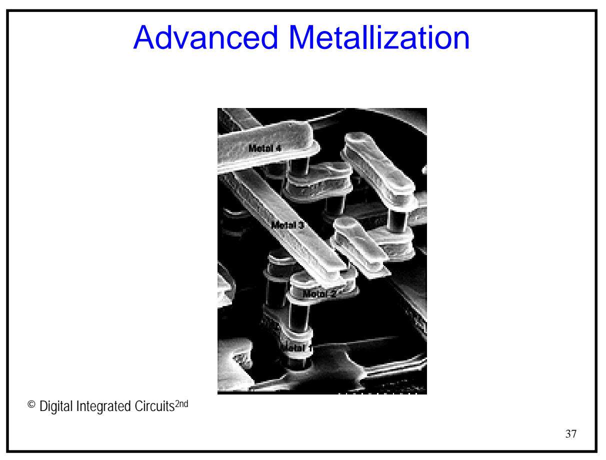
35

The MOSIS Scalable CMOS Rules

- λ-based rules
- Designs using these rules are fabricated by a variety of companies
- Multiple designs are put on a single die
  - Each chip wired to a particular design
- Support for submicron digital CMOS, analog (buried poly layer for capacitor), micromachines, etc.

- www.mosis.org/Technical/Designrules/scmos/

36


Advanced Metallization
Metal 4
Metal 3
Metal 2
Metal 1
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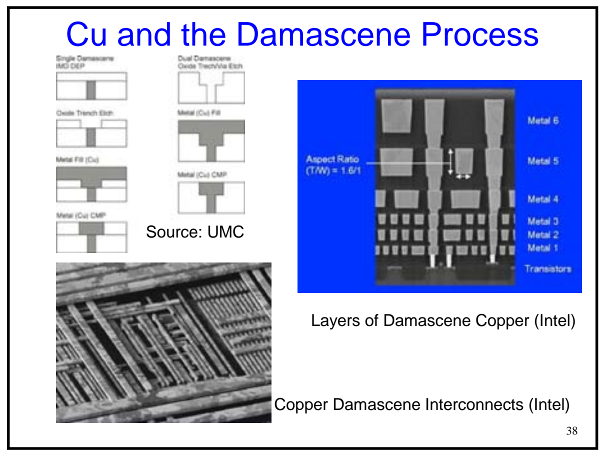
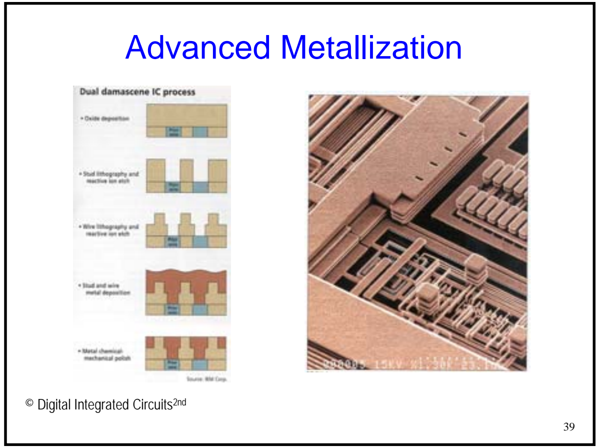
37


Cu and the Damascene Process
Source: UMC
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Transistors
Layers of Damascene Copper (Intel)
Copper Damascene Interconnects (Intel)
38


Advanced Metallization
Dual damascene IC process
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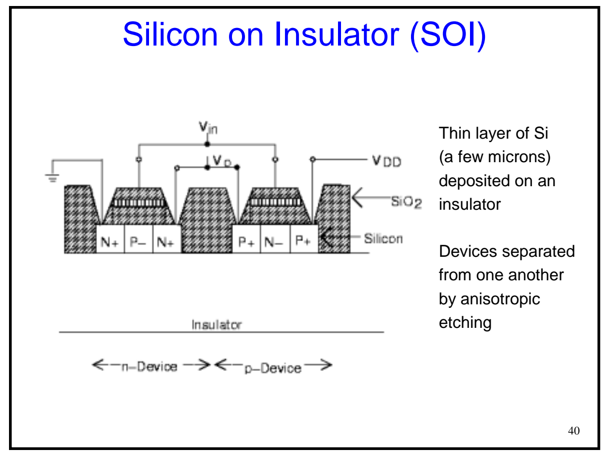
39


Silicon on Insulator (SOI)
Vin
VDD
SiO2
Silicon
Insulator
n–Device
p–Device
Thin layer of Si (a few microns) deposited on an insulator
Devices separated from one another by anisotropic etching
40