## 20. Packaging and I/O

- Previous Unit:
  - Introduction to design testing/verification
- This Unit:
  - Packaging
  - I/O



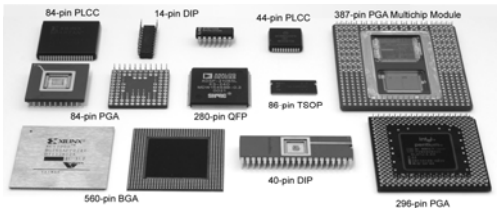
## Packages

- Package functions
  - Electrical connection of signals and power from chip to board
  - Little delay or distortion
  - Mechanical connection of chip to board
  - Removes heat produced on chip
  - Protects chip from mechanical damage
  - Compatible with thermal expansion
  - Inexpensive to manufacture and test



## Package Types

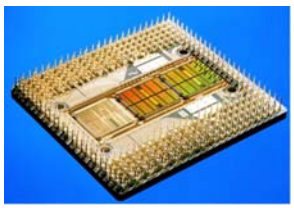
- Through-hole vs. surface mount






## Multichip Modules

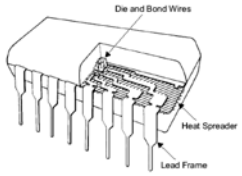
- Pentium Pro MCM
  - Fast connection of CPU to cache
  - Expensive, requires known good dice





## Chip-to-Package Bonding

- Traditionally, chip surrounded by *pad frame*
  - Metal pads on 100 – 200 μm pitch
  - Gold *bond wires* attach pads to package
  - *Lead frame* distributes signals in package
  - Metal *heat spreader* helps with cooling



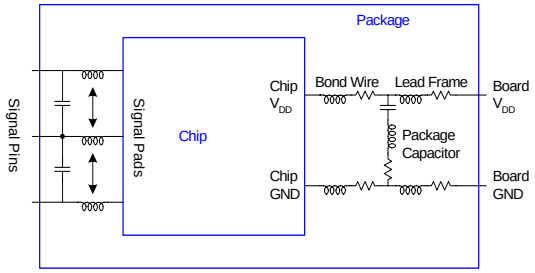



## Advanced Packages

- Bond wires contribute parasitic inductance
- Fancy packages have many signal, power layers
  - Like tiny printed circuit boards
- *Flip-chip* places connections across surface of die rather than around periphery
  - Top level metal pads covered with solder balls
  - Chip flips upside down
  - Carefully aligned to package (done blind!)
  - Heated to melt balls
  - Also called *C4* (Controlled Collapse Chip Connection)

## Package Parasitics

- Use many $V_{DD}$, GND in parallel
  - Inductance, $I_{DD}$






## Heat Dissipation

- 60 W light bulb has surface area of 120 $cm^2$
- Itanium 2 die dissipates 130 W over 4 $cm^2$
  - Chips have enormous power densities
  - Cooling is a serious challenge
- Package spreads heat to larger surface area
  - Heat sinks may increase surface area further
  - Fans increase airflow rate over surface area
  - Liquid cooling used in extreme cases ($$$)



## Thermal Resistance

- $\Delta T = \theta_{ja} P$
  - $\Delta T$: temperature rise on chip
  - $\theta_{ja}$: thermal resistance of chip junction to ambient
  - P: power dissipation on chip
- Thermal resistances combine like resistors
  - Series and parallel
- $\theta_{ja} = \theta_{jp} + \theta_{pa}$
  - Series combination



## Example

- Your chip has a heat sink with a thermal resistance to the package of 4.0° C/W.
- The resistance from chip to package is 1° C/W.
- The system box ambient temperature may reach 55° C.
- The chip temperature must not exceed 100° C.
- What is the maximum chip power dissipation?

- (100-55 C) / (4 + 1 C/W) = 9 W



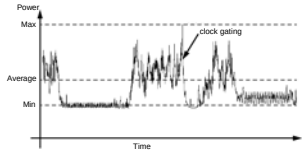
## Power Distribution

- Power Distribution Network functions
  - Carry current from pads to transistors on chip
  - Maintain stable voltage with low noise
  - Provide average and peak power demands
  - Provide current return paths for signals
  - Avoid electromigration & self-heating wearout
  - Consume little chip area and wire
  - Easy to lay out



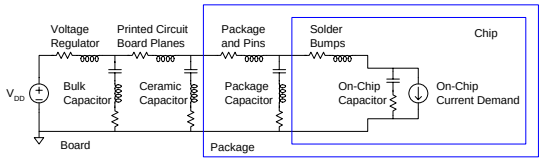
## Power Requirements

- $V_{DD} = V_{DDnominal} - V_{droop}$
- Want $V_{droop}$ < +/- 10% of $V_{DD}$
- Sources of $V_{droop}$
  - IR drops (static)
  - L di/dt noise (dynamic)
- $I_{DD}$ changes on many time scales



## Power System Model

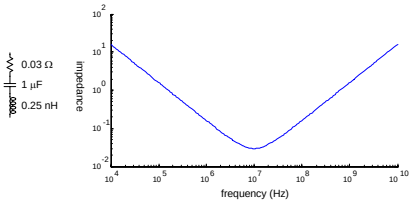
- Power comes from regulator on system board
  - Board and package add parasitic R and L
  - Bypass capacitors help stabilize supply voltage
  - But capacitors also have parasitic R and L
- Simulate system for time and frequency responses






## Bypass Capacitors

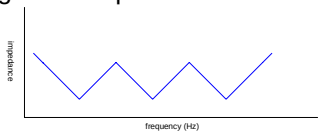
- Need low supply impedance at all frequencies
- Ideal capacitors have impedance decreasing with $\omega$
- Real capacitors have parasitic R and L
  - Leads to resonant frequency of capacitor






## Frequency Response

- Use multiple capacitors in parallel
  - Large capacitor near regulator has low impedance at low frequencies
  - But also has a low self-resonant frequency
  - Small capacitors near chip and on chip have low impedance at high frequencies
- Choose caps to get low impedance at all frequencies






## Input / Output

- Input/Output System functions
  - Communicate between chip and external world
  - Drive large capacitance off chip
  - Operate at compatible voltage levels
  - Provide adequate bandwidth
  - Limit slew rates to control di/dt noise
  - Protect chip against electrostatic discharge
  - Use small number of pins (low cost)



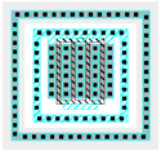
## I/O Pad Design

- Pad types
  - $V_{DD}$ / GND
  - Output
  - Input
  - Bidirectional
  - Analog



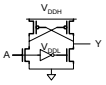
## Output Pads

- Drive large off-chip loads (2 – 50 pF)
  - With suitable rise/fall times
  - Requires chain of successively larger buffers
- Guard rings to protect against latchup
  - Noise below GND injects charge into substrate
  - Large nMOS output transistor
  - p+ inner guard ring
  - n+ outer guard ring
    - In n-well

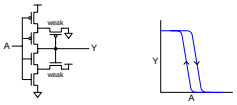


## Input Pads

- Level conversion
  - Higher or lower off-chip V
  - May need thick oxide gates




- Noise filtering
  - Schmitt trigger
  - Hysteresis changes $V_{IH}$, $V_{IL}$

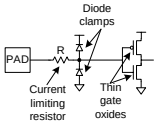


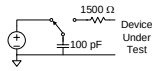

- Protection against electrostatic discharge



## ESD Protection

- Static electricity builds up on your body
  - Shock delivered to a chip can fry thin gates
  - Must dissipate this energy in protection circuits before it reaches the gates
- ESD protection circuits
  - Current limiting resistor
  - Diode clamps
- ESD testing
  - Human body model
  - Views human as charged capacitor

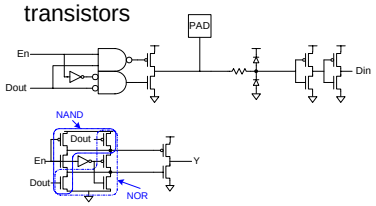




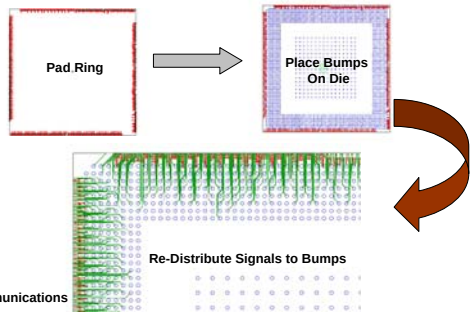

## Bidirectional Pads

- Combine input and output pad
- Need tristate driver on output
  - Use enable signal to set direction
  - Optimized tristate avoids huge series transistors






## Package Design Steps

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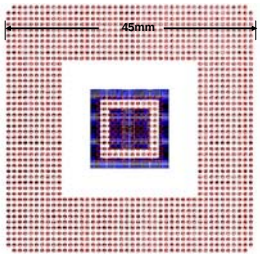
## Flip the Chip and Place on Substrate

- ❑ Substrate has two usable layers for signal routing
- ❑ Two layers are dedicated for various split planes

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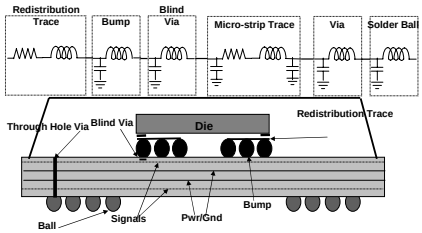
## Electrical Model for the Package




Distributed Parasitics Must be Extracted for >5GHz

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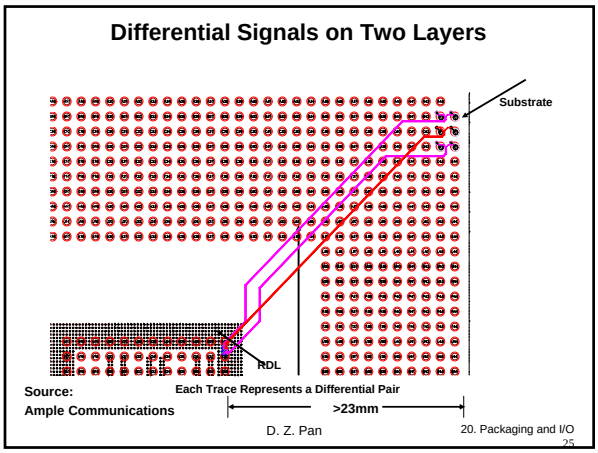
Differential Signals on Two Layers
Substrate
RDL
Each Trace Represents a Differential Pair
>23mm
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25