23. Design for Low Power

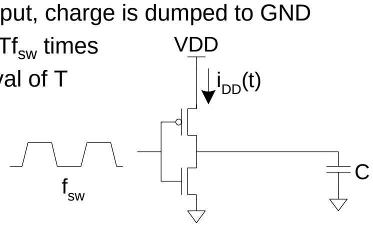
- Previous Unit:
  - Circuit optimization overview
- This Unit
  - Power and Energy
  - Dynamic Power
  - Static Power
  - Low Power Design

Power and Energy

- Power is drawn from a voltage source attached to the V_{DD} pin(s)
- Instantaneous Power: $P(t) = i_{DD}(t) V_{DD}$
- Energy: $E = \int_0^T P(t)dt = \int_0^T i_{DD}(t) V_{DD} dt$
- Average Power: $P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T i_{DD}(t) V_{DD} dt$

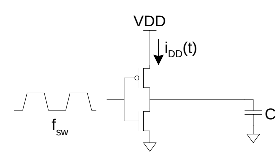
Dynamic Power

- Dynamic power required to charge and discharge load capacitances when transistors switch
- One cycle involves a rising and falling output
- On rising output, charge $Q = CV_{DD}$ is required
- On falling output, charge is dumped to GND
- This repeats Tf_{sw} times over an interval of T



Dynamic Power Cont.

$$P_{dynamic} = \frac{1}{T}\int_0^T i_{DD}(t) V_{DD} dt$$
$$= \frac{V_{DD}}{T}\int_0^T i_{DD}(t) dt$$
$$= \frac{V_{DD}}{T}[Tf_{sw} C V_{DD}]$$
$$= C V_{DD}^2 f_{sw}$$



Activity Factor

- Suppose the system clock frequency = f
- Let $f_{sw} = \alpha f$, where α = activity factor
  - If the signal is a clock, $\alpha = 1$
  - If the signal switches once per cycle, $\alpha = ½$
  - Dynamic gates:
    - Switch either 0 or 2 times per cycle, $\alpha = ½$
  - Static gates:
    - Depends on design, but typically $\alpha = 0.1$
- Dynamic power: $P_{dynamic} = \alpha C V_{DD}^2 f$

Short Circuit Current

- When transistors switch, both nMOS and pMOS networks may be momentarily ON for a short period of time
- Leads to a blip of "short circuit" current.
- < 10% of dynamic power if rise/fall times are comparable for input and output

Example

- 200M transistor chip
  - 20M logic transistors
    - Average width: 12 λ
  - 180M memory transistors
    - Average width: 4 λ
  - 1.2 V 100 nm process
  - C_g = 2 fF/μm

Dynamic Power Example

- Static CMOS logic gates: activity factor = 0.1
- Memory arrays: activity factor = 0.05 (many banks!)
- Estimate dynamic power consumption per MHz (neglect wire capacitance)

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$$C_{\text{logic}} = \left(20\times10^6\right)\left(12\lambda\right)\left(0.05\mu m/\lambda\right)\left(2\,fF/\mu m\right) = 24nF$$

$$C_{\text{mem}} = \left(180\times10^6\right)\left(4\lambda\right)\left(0.05\mu m/\lambda\right)\left(2\,fF/\mu m\right) = 72nF$$

$$P_{\text{dynamic}} = \left[0.1C_{\text{logic}} + 0.05C_{\text{mem}}\right]\left(1.2\right)^2 f = 8.6\text{ mW/MHz}$$

Static Power

- Static power is consumed even when chip is quiescent.
  - Ratioed circuits burn power in fight between ON transistors
  - Leakage draws power from nominally OFF devices

$$I_{ds} = I_{ds0} e^{\frac{V_{gs}-V_t}{nv_T}} \left[1 - e^{\frac{-V_{ds}}{v_T}}\right]$$

$$V_t = V_{t0} - \eta V_{ds} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

Ratio Example

- The chip contains a 32 word x 48 bit ROM
  - Uses pseudo-nMOS decoder and bitline pullups
  - On average, one wordline and 24 bitlines are high
- Find static power drawn by the ROM
  - β = 75 μA/V²
  - V_{tp} = -0.4V

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  - V_{tp} = -0.4V
- Solution:

$$I_{\text{pull-up}} = \beta\frac{\left(V_{DD} - \left|V_{tp}\right|\right)^2}{2} = 24\mu\text{A}$$

$$P_{\text{pull-up}} = V_{DD} I_{\text{pull-up}} = 29\mu\text{W}$$

$$P_{\text{static}} = (31 + 24) P_{\text{pull-up}} = 1.6\text{ mW}$$

Leakage Example

- Process has two threshold voltages and two oxide thicknesses
- Subthreshold leakage:
  - 20 nA/μm for low V_t
  - 0.02 nA/μm for high V_t
- Gate leakage:
  - 3 nA/μm for thin oxide
  - 0.002 nA/μm for thick oxide
- Memories use low-leakage transistors everywhere
- Gates use low-leakage transistors on 80% of logic

Leakage Example Cont.

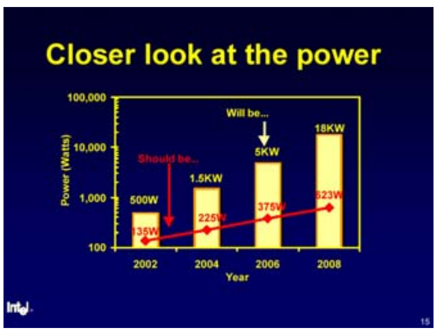
- Estimate static power:
  - High leakage: $(20\times10^6)(0.2)(12\lambda)(0.05\mu m/\lambda)=2.4\times10^6\,\mu m$
  - Low leakage: $(20\times10^6)(0.8)(12\lambda)(0.05\mu m/\lambda)+$ $(180\times10^6)(4\lambda)(0.05\mu m/\lambda)=45.6\times10^6\,\mu m$

$$I_{static}=(2.4\times10^6\,\mu m)[(20nA/\mu m)/2+(3nA/\mu m)]+(45.6\times10^6\,\mu m)[(0.02nA/\mu m)/2+(0.002nA/\mu m)]=32mA$$

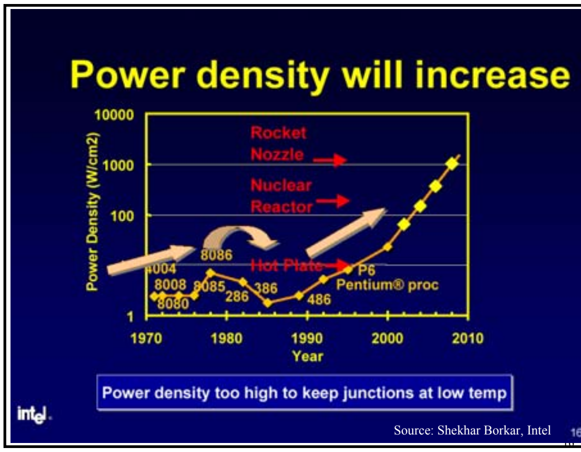
$$P_{static}=I_{static}V_{DD}=38mW$$

- If no low leakage devices, P_{static} = 749 mW

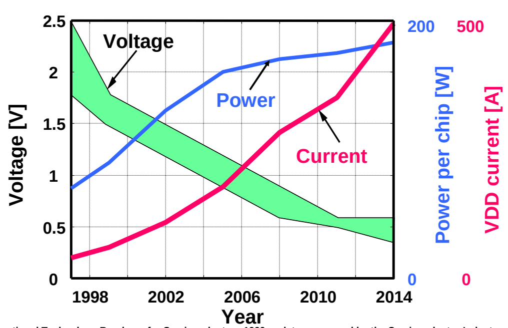
Gloom and Doom predictions



Source: Shekhar Borkar, Intel

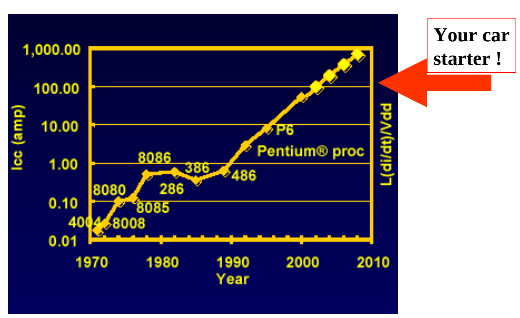


VDD, Power and Current Trend



International Technology Roadmap for Semiconductors 1999 update sponsored by the Semiconductor Industry Association in cooperation with European Electronic Component Association (EECA), Electronic Industries Association of Japan (EIAJ), Korea Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA) (* Taken from Sakurai's ISSCC 2001 presentation)

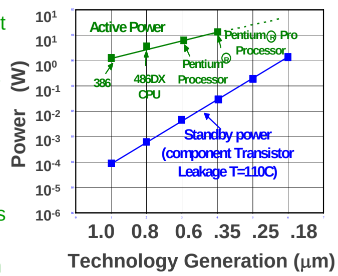
Power Delivery Problem (not just California)



Source: Shekhar Borkar, Intel

Why is Excessive Leakage an Issue?

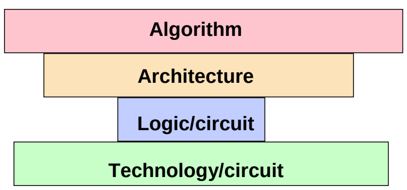
- Leakage component to active power becomes significant % of total power
- Approaching ~10% in 0.18 µm technology
- Acceptable limit less than ~10%, implies serious challenge in V_T scaling!



Low Power Design

- Reduce dynamic power
  - α: clock gating, sleep mode
  - C: small transistors (esp. on clock), short wires
  - V_{DD}: lowest suitable voltage
  - f: lowest suitable frequency
- Reduce static power
  - Selectively use ratioed circuits
  - Selectively use low V_t devices
  - Leakage reduction:
    stacked devices, body bias, low temperature

Low Power Design Techniques



- Need combination of techniques at all levels