THE UNIVERSITY OF TEXAS AT AUSTIN
Cockrell School of Engineering

FULL NAME: David Z. Pan

TITLE: Professor, Silicon Laboratories Endowed Chair in Electrical Engineering

DEPARTMENT: Electrical and Computer Engineering, The University of Texas at Austin

EDUCATION:

University of California, Los Angeles	Computer Science	Ph.D.	Fall 2000
University of California, Los Angeles	Computer Science	M.S.	Fall 1998
University of California, Los Angeles	Atmospheric Sciences	M.S.	Fall 1994
Peking University, China	Physics	B.S.	Spring 1992

CURRENT AND PREVIOUS ACADEMIC POSITIONS:

The University of Texas at Austin	Professor, Silicon Labs Endowed Chair in Electrical Engineering	09/2020 –
The University of Texas at Austin	Professor, Engineering Foundation Endowed Professorship #1	09/2014 – 08/2020
Massachusetts Institute of Technology	Visiting Professor, Dept. of Electrical Engineering and Computer Science; Visiting Scientist, Microsystems Technology Laboratories	06/2019 – 12/2019
The University of Texas at Austin	Professor, Brasfield Endowed Faculty Fellow	09/2013 – 08/2014
The University of Texas at Austin	Associate Professor	09/2008 – 08/2013
The University of Texas at Austin	Assistant Professor	09/2003 – 08/2008

OTHER PROFESSIONAL EXPERIENCES:

IBM T. J. Watson Research Center	Research Staff Member	10/2000 – 08/2003

CONSULTING:

Hogan Lovells US LLP	Expert Consultant	2020-
Cooley LLP	Consultant	2013-2014
Tabula, Inc.	Advisor and Consultant	2012-2015
Pyxis Technology Inc. (Acquired by Mentor Graphics in 2011)	Member of Technical Advisory Board	2005 - 2011
Cadence Design Systems	Consultant	2008
Fish & Richardson, P.C.	Consultant	2006 - 2007

HONORS AND AWARDS (SELECTED):

General Awards/Honors:

- 2014 **IEEE Fellow**, for contributions to design for manufacturability in integrated circuits
- 2017 **SPIE Fellow**, for achievements in IC design for manufacturing with advanced lithography
- 2013 **SRC Technical Excellence Award**, for "Nanometer IC Design for Manufacturability" with the citation "In recognition of your key contributions to technology that have significantly enhanced the productivity of the semiconductor industry"

- 2020- **Silicon Laboratories Endowed Chair in Electrical Engineering,** UT Austin
- 2020 **IEEE CEDA Outstanding Service Recognition**, "for outstanding service to the EDA community as ICCAD General Chair in 2019"
- 2014-2020 **Engineering Foundation Endowed Professorship #1**, UT Austin
- 2019 **Cadence Academic Collaboration Award**, "for contributions to design for manufacturing and physical design of integrated circuits and systems, and educating a diverse body of outstanding EDA professionals to industry"
- 2013-2014 Earl N. & Margaret Brasfield Endowed Faculty Fellowship in Engineering, UT Austin
- 2019-2020 IEEE Council on Electronic Design Automation (CEDA) **Distinguished Lecturer**
- 2014 **RAISE Faculty Excellence Award** -- Recognizing Asian & Asian American Faculty & Staff Instilling Strength and Excellence, The University of Texas at Austin
- 2011 Overseas and Hong Kong/Macau Scholars Collaborative Research Award (a.k.a. Overseas Distinguished Young Scholar) by National Natural Science Foundation of China (NSFC)
- 2010, 2006, 2005, 2004 **IBM Faculty Award**
- 2009 UCLA School of Engineering and Applied Science, **Distinguished Young Alumnus Award** (a.k.a. Rising Professional Achievement Award), which honors the early career achievements of alumni who are under the age of 40
- 2008-2009 IEEE Circuits & Systems (CAS) Society **Distinguished Lecturer**
- 2008, 2000 Semiconductor Research Corporation (SRC) Inventor Recognition Award
- 2008 Association for Computing Machinery (ACM) Recognition of Service Award
- 2007 National Science Foundation (NSF), **Faculty Early Career Development (CAREER) Award**
- 2007 Association for Computing Machinery (ACM) Recognition of Service Award
- 2005 **ACM/SIGDA Outstanding New Faculty Award**
- 2003 IBM Research Bravo Award
- 2001 **Outstanding Ph.D. Award**, UCLA Computer Science Department
- 2000 Dimitris Chorafas Foundation Award
- 1999-2000 IBM Research Fellowship

Best Paper Awards, Prolific Author Awards, etc.:

- 2020 **Best Poster Award**, NSF Workshop on Machine Learning Hardware (Student: Jiaqi Gu)
- 2020 **Best Paper Award**, ACM International Symposium on Physical Design (ISPD)
- 2020 **Best Paper Award**, ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC)
- 2020 **ASP-DAC Prolific Author Award** - for having published 25 or more papers at the 25th Asian and South Pacific Design Automation Conference (ASP-DAC) – I have published 44 papers as of 2020 in ASP-DAC, which is ranked #3 in the world in ASP-DAC history
- 2020 ASP-DAC 10-Year Retrospective Most Influential Paper Award Finalist
- 2019 **Best Paper Award**, ACM/IEEE Design Automation Conference (DAC)
- 2018 **Best Paper Award**, ACM Great Lakes Symposium on VLSI (GLSVLSI)
- 2018 **Best Paper Award**, Integration – the VLSI Journal
- 2017 **Best Paper Award**, IEEE International Symposium on Hardware Oriented Security and Trust (HOST)
- 2016 SPIE Advanced Lithography Franco Cerrina Memorial **Best Student Paper Award**
- 2015 **Best Paper in Session Award**, SRC Techcon Conference
- 2015 Asian and South Pacific Design Automation Conference (**ASP-DAC**) **Frequently Cited Author Award** (given to the top 3 cited authors in ASP-DAC's 20-year history)
- 2015 ASP-DAC 10-Year Retrospective Most Influential Paper Award Finalist
- 2014 **Best Paper Award**, ACM International Symposium on Physical Design (ISPD)
- 2014 Communications of the ACM (CACM) **Research Highlights**, for "Full-Chip Mechanical Reliability Analysis and Optimization for 3D ICs"
- 2013 IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), **Keynote Paper** for "Design for Manufacturing with Emerging Nanolithography"

- 2013 **William J. MacCalla Best Paper Award**, IEEE/ACM International Conference on Computer Aided Design (ICCAD)
- 2013 **DAC Top 10 Author in Fifth Decade**, for being one of the top 10 most prolific authors in DAC's fifth decade
- 2013 **DAC Prolific Author Award** - DAC 25 Club, for having published 25 or more papers at the Design Automation Conference
- 2012 **Best Paper in Session Award**, SRC Techcon Conference
- 2012 **Best Paper Award**, ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC)
- 2011 **Best Paper Award**, ACM International Symposium on Physical Design (ISPD)
- 2010 IBM Research **Pat Goldberg Memorial Best Paper Award** in Computer Science, Electrical Engineering and Math (4 awardees across all fields of CS, EE, and Math among all papers published/co-authored by IBM Research)
- 2010 **Best Paper Award**, ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC)
- 2009 **Best Student Paper Award**, IEEE International Conference on IC Design and Technology
- 2009 **Best Paper (IP) Award**, IEEE/ACM Design Automation & Test in Europe (DATE)
- 2007 **Best Paper in Session Award**, SRC Techcon Conference
- 1998 **Best Paper in Session Award**, SRC Techcon Conference
- **16 additional Best Paper Award Finalists/Nominations**: DAC 2020, ASP-DAC 2020, DAC'19, ISPD'19, DATE'19, DAC'14, ASP-DAC'13, DAC'12, ISPD'12, ICCAD'11, DAC'11, ISPD'10, ICCAD'08, ASP-DAC'08, DAC'06, ASP-DAC'06

Contest and Student Awards:

- 2017 ACM International Symposium on Physical Design **(ISPD) Contest: 1st Place**
- 2016 ACM International Symposium on Physical Design **(ISPD) Contest: 1st Place**
- 2013 ICCAD CAD Contest Award (the 2nd Place) in "Mask Optimization"
- 2012 ICCAD CAD Contest Award in "Fuzzy Pattern Matching for Physical Verification", 2nd Place
- 2009 **Grand Prize ($25,000), eASIC Placement Worldwide Contest**
- 2007 IEEE CEDA Award for the Open Source BoxRouter 2.0
- 2007 ACM International Symposium on Physical Design (ISPD) Routing Contest Awards: the 2nd place in 3D and the 3rd place in 2D

- 2020 Honor for PhD Student Jiaqi Gui: ACM/SIGDA Student Research Competition **Gold Medal** (Graduate Category) at ICCAD 2020
- 2019 Honor for PhD Student Meng Li: Margarida Jacome Dissertation Prize from UT-ECE
- 2019 Honor for PhD Student Meng Li: European Design and Automation Association (EDAA) **Outstanding Dissertation Award**
- 2018 Honor for PhD Student Wuxi Li: ACM/SIGDA Student Research Competition Silver Medal (Graduate Category) at ICCAD 2018
- 2018 Honor for PhD Student Meng Li: **First Place, ACM Student Research Competition Grand Finals** (Graduate Category) – the award was presented at the Turing Award banquet
- 2018 Honor for PhD Student Xiaoqing Xu: **ACM Outstanding PhD Dissertation Award in EDA**
- 2017 Honor for PhD Student Meng Li: ACM/SIGDA Student Research Competition **Gold Medal** (Graduate Category) at ICCAD 2017
- 2016 Honor for PhD Student Xiaoqing Xu: ACM/SIGDA Student Research Competition **Gold Medal** (Graduate Category) at ICCAD 2016
- 2015 Honor for PhD Student Bei Yu: European Design and Automation Association (EDAA) **Outstanding Dissertation Award**
- 2013 Honor for PhD Student Bei Yu: ACM/SIGDA Student Research Competition Silver Medal (Graduate Track) at ICCAD 2013
- 2013 Honor for PhD Student Duo Ding: **ACM Outstanding PhD Dissertation Award in EDA**
- 2012 Fall UT-ECE Senior Design Open House, the 1st Place Winning Team, Faculty Mentor

MEMBERSHIPS IN PROFESSIONAL AND HONORARY SOCIETIES:

Fellow, IEEE (Institute of Electrical and Electronics Engineers), class of 2014
Fellow, SPIE (International Society for Optical Engineering), class of 2017
Member, ACM (Association for Computing Machinery) and ACM/SIGDA

UNIVERSITY COMMITTEE ASSIGNMENTS:

Departmental-	Member, ECE Faculty Search Committee	2012-present
	Member, ECE Faculty Peer Review Committee	2013-
	Member, ECE Faculty Awards Committee	2014
	Member, ECE Department Colloquium Committee	2011-2018
	Member, ECE Benchmarking/Directions Committee	2014
	Coordinator, ECE Department, Integrated Circuits & Systems Area Graduate Admissions Committee	2009-present
	Member, ECE Department, Integrated Circuits & Systems Area Graduate Admissions Committee	2005-present
	Member, Integrated Circuits & Systems Curriculum Committee	2005-present
	Member, Computer Science Department, Graduate Studies Committee	2004-present
	Co-founder/Co-organizer, VLSI Seminar Series (renamed to Integrated Circuits & Systems Seminar Series in Spring 2010)	2003-present
	Member, Computer Engineering Curriculum Committee	2003-2005
	Member, ECE Department, Graduate Studies Committee	2003-present
	Member, Undergraduate Student Appeals Committee	2003-present
	Member, ECE Department Faculty Search Committee	2020-2021
	Member, ECE Department Faculty Review Committee	2010; 2020
College-	*ad hoc* COVID-19 Cockrell School of Engineering (CSE) Planning Committee for International Students	2020
	CSE Faculty Research Assignment Review Committee	2020
University-	Faculty Co-Chair, Asian/Asian American Faculty and Staff Association (AAAFSA), UT Austin	2012-2014
	AAAFSA RAISE Award Committee	2015
	Heman Sweatt Nominations Committee	2013, 2014
	Faculty Mentor Program	2005-present
	AAAFSA Undergraduate Scholarship Committee	2013, 2014
	Graduate School Outstanding Dissertation Selection Committee	2011, 2020

PROFESSIONAL SOCIETY AND MAJOR GOVERNMENTAL COMMITTEES:

Editorship

- Senior Associate Editor, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2014-present
- Subject Editor, Physical Synthesis and Design for Manufacturing, Elsevier Integration – The VLSI Journal, 2020-present
- Associate Editor, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), 2006-2011, 2018-present
- Associate Editor, IEEE Design & Test, 2016-present
- Associate Editor, IET Computers & Digital Techniques, 2014-present
- Associate Editor, Science China Information Sciences, 2013-present

- Subject Area Editor (in VLSI Design), Journal of Computer Science and Technology (JCST), 2010-present
- Associate Editor, Journal of Microelectronic Manufacturing (JoMM), 2019-
- Associate Editor, IEEE Circuits and Systems Society (CASS) Newsletters, 2007-2016
- Associate Editor, IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2007-2014
- Associate Editor, IEEE Transactions on Circuits and Systems, I: Regular Papers (TCAS-I), 2008-2009
- Guest Editor, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), Special Section of International Symposium on Physical Design, 2007 and 2008
- Associate Editor, IEEE Transactions on Circuits and Systems, II: Express Briefs (TCAS-II), 2006-2007

Service to Professional Society and Government/Agencies

- IEEE Computer Society Fellow Evaluation Committee, 2021
- ACM/SIGDA Executive Committee (Award Chair), 2018-present
- IEEE Electron Devices Society (EDS) Representative to IEEE Council on Electronic Design Automation (CEDA), 2016-present
- IEEE Council on Electronic Design Automation (CEDA) Fellow Evaluation Committee, 2017
- IEEE Council on Electronic Design Automation (CEDA), Distinguished Lecturer Program Committee, 2016-present
- EDAA Outstanding Dissertation Award Jury Member, 2019, 2020
- ACM/SIGDA Outstanding New Faculty Award Committee, 2017
- ACM/TODAES Best Paper Award Committee, 2016, 2017, 2019
- ACM/SIGDA Outstanding PhD Dissertation Award Committee, 2014
- Advisor Board, Chinese American Semiconductor Professional Association (华美半导体协会), Austin Chapter, 2013 -
- IEEE Council on Electronic Design Automation (CEDA), Publicity Committee, 2012-present
- IEEE Admission & Advancement Committee Senior Member Review Panel, Feb. 2013
- ACM/SIGDA Technical Committee on Physical Design, Chair, 2009-2015
- Semiconductor Industry Association, International Technology Roadmap for Semiconductors (ITRS), Design Technology Working Group, 2004-2015
- ACM/SIGDA Outstanding PhD Dissertation Award Committee, 2012
- IEEE Computer-Aided Network Design (CANDE) Committee: Past Chair, 2010; Chair, 2009; Secretary, 2008
- IEEE Council on EDA (CEDA) Working Group for Educational Certification Program in China, 2007
- IEEE Guillemin-Cauer and Darlington Best Paper Awards Nomination Committee, 2007
- IEEE TCAS-II EDICS Committee, 2006
- NYSTAR (New York State) Microelectronics Design Center (MDC) Industrial Liaison, 2002-2003
- Semiconductor Research Corporation (SRC) Industrial Liaison, 2001-2003

Services to Professional Conferences

Various Chair/Leadership/Advisory Positions

- Advisory Chair, ICICM-International Conference on Integrated Circuits and Microsystems, 2020
- Past Chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2020
- **General Chair**, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2019

- Advisory Board, IEEE International Conference on Omni-layer Intelligent Systems (COINS), Barcelona, Spain, 2020
- Advisory Board, The First IEEE International Conference on Omni-layer Intelligent Systems (COINS), Greece, 2019
- **Program Chair**, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2018
- Subcommittee Chair for "Physical Design and Verification, Lithography and DFM", Design Automation Conference (DAC), 2020
- Subcommittee Chair for "Physical Design and Verification, Lithography and DFM", Design Automation Conference (DAC), 2020
- CAD Track Chair, International Symposium on Low Power Electronics & Design (ISLPED), 2018
- Vice Program Chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2017
- **Technical Program Chair**, ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2017
- Executive Committee Member and Special Session/Tutorial Chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2016
- International Advisory Committee Co-Chair, IEEE International Conference on Ubiquitous Wireless Broadband (ICUWB), Oct. 16-19, 2016
- Subcommittee Chair for "Physical Verification, Lithography and DFM", Design Automation Conference (DAC), 2016
- **Steering Committee Member**, ACM International Symposium on Physical Design (ISPD), 2016, 2017, 2018, 2019, 2020
- Technical Program Committee Vice Chair, ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2016
- Executive Committee Member and Workshop Chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2015
- **Executive Committee Member and Tutorial Chair**, ACM/IEEE Design Automation Conference (DAC), 2014
- **Organizing Committee Chair**, IEEE Texas Workshop on Integrated Systems Exploration (TexasWISE), 2014
- Co-Chair, IEEE/ACM Workshop on Variability Modeling and Characterization (VMC), 2013, 2014 (co-located with ICCAD)
- **Co-Chair**, NSF/SRC/DFG Cross Domain Resilience Workshop, Austin, July 11-12, 2013
- Technical Program Co-Chair, the 1st IEEE International High Speed Interconnect Symposium (From Silicon to Systems), Dallas, April 30, 2013
- Organizing Committee, the 1st IEEE Texas Workshop on Integrated Systems Exploration (TexasWISE), 2013
- **Conference Co-Chair**, 13th International CAD/Graphics Conference, 2013
- EDA Track Co-Chair, 31st IEEE International Conference on Computer Design (ICCD), 2013
- ASP-DAC 10-Year Retrospective Most Influential Paper Award Committee Member, 2013
- Technical Advisory Board Member, International System-on-Chip (SoC) Conference & Exhibit, 2007-present
- Design for Manufacturability Track Chair, International Conference on Computer Aided Design (ICCAD), 2012
- CAD and Design Tools Track Chair, International Symposium on Low Power Electronics & Design (ISLPED), 2012, 2013, 2014
- Design for Manufacturability Subcommittee Chair, Design Automation Conference (DAC), 2012
- DFM and Statistical Design, Subcommittee Chair, Asian and South Pacific Design Automation Conference (ASP-DAC), 2012, 2013
- EDA Subcommittee Chair, International Symposium on VLSI Design, Automation & Test (VLSI-DAT), 2010, 2011, 2012, 2013, 2014

- EDA Subcommittee Co-Chair, IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), 2012, 2013, 2014
- Award Chair, IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), 2009-2012
- Biological, Nanoscale and Post-CMOS Systems, Subcommittee Chair, International Conference on Computer-Aided Design (ICCAD), 2011
- Physical Design & Manufacturability Subcommittee Chair, Design Automation Conference (DAC), 2011
- Physical Design Track Chair, Asian and South Pacific Design Automation Conference (ASP-DAC), 2011
- Exhibits Chair, International Symposium on Low Power Electronics & Design (ISLPED), 2010
- Best Paper Award Committee Member, IEEE/ACM International Symposium on Networks-on-Chip (NOCS), 2009
- Steering Committee Chair, ACM International Symposium on Physical Design (ISPD), 2009
- DFM Track Chair, Asian and South Pacific Design Automation Conference (ASP-DAC), 2009
- General Co-Chair, Austin Conference on Integrated Systems and Circuits (ACISC), 2009
- Chair for Electronic Design Automation (EDA) track, First Asian Symposium on Quality Electronic Design (ASQED), 2009
- **General Chair**, ACM International Symposium on Physical Design (ISPD), 2008
- Program Co-Chair, Austin Conference on Integrated Systems and Circuits (ACISC), 2008
- Publication Chair, SLIP Workshop, 2008
- Co-Chair for Design of Reliable Circuits and Systems (DFR) track, International Symposium on Quality Electronic Design (ISQED), 2007 and 2008
- Local Arrangement Chair/Steering Committee Member, IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), 2007
- **Program Chair**, ACM International Symposium on Physical Design (ISPD), 2007
- IEEE CANDE Workshop Chair, 2007
- CAD track Co-Chair, International Symposium on Circuits and Systems (ISCAS), 2006, 2007
- Invited Speakers/Panel Chair, Austin Conference on Integrated Systems and Circuits (ACISC), 2006, 2007
- Publication Chair, ACM International Symposium on Physical Design (ISPD), 2006
- Publicity Chair, ACM International Symposium on Physical Design (ISPD), 2005
- Publicity Co-Chair, SLIP Workshop, 2003
- Local Arrangement Chair, Great Lakes Symposium on VLSI (GLSVLSI), 2002
- Session Chair for DAC, ICCAD, ISPD, ASP-DAC, ISQED, SLIP, ICICDT, ICSICT, etc.

Program Committee Member

- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), 2020
- SPIE Advanced Lithography Symposium – DFM Conference Committee, 2012-present
- SPIE Photonics West – Optoelectronic Interconnect XII Conference Committee, 2012
- ACM/IEEE International Symposium on Low Power Electronics & Design (ISLPED), 2011-present
- IEEE International Conference on Computer Design (ICCD), 2011-present
- ACM/SIGDA Student Research Competition at ICCAD 2013, 2014
- ACM/IEEE Design Automation Conference (DAC), 2009-2012
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2003-2005, 2009-2012
- ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC), 2003-2005, 2007, 2009-2013, 2015
- IEEE International Symposium on VLSI Design, Automation & Test (VLSI-DAT), 2008-present
- IEEE International Workshop on Design for Manufacturability & Yield (DFM&Y), 2007-present
- IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), 2005-present

- ACM International Workshop on System Level Interconnect Prediction (SLIP), 2003-2011
- SASIMI Workshop, 2009-2010
- IEEE International Symposium on Quality Electronic Design (ISQED), 2006-2009
- Austin Conference on Integrated Systems and Circuits (ACISC), 2006-2008
- International Semiconductor Technology Conference, 2008
- IEEE/ACM International Conference on VLSI Design (VLSID), 2008
- IEEE/ACM Design, Automation and Test in Europe (DATE), 2006, 2007
- International Symposium on Circuits and Systems (ISCAS), 2004-2007
- ACM International Symposium on Physical Design (ISPD), 2004-2007
- ACM Great Lakes Symposium on VLSI (GLSVLSI), 2002-2006

Proposal Review Panels

- National Science Foundation (NSF) Panelist
- Germany DFG Panelist
- External reviewer for California MICRO Program
- External reviewer for Louisiana Board of Regents
- External reviewer for University of Missouri Research Board
- External reviewer for Austrian Science Fund (FWF)
- External reviewer for Research Grants Council, Hong Kong
- External reviewer for Qatar National Research Fund

PUBLICATIONS:

Google citation page http://scholar.google.com/citations?user=3aLIroEAAAAJ
Citations 10,256, h-index 53, i-10 index 222, as of January 26, 2021

A. Refereed Journal Articles

[J1] Yibai Meng, Wuxi Li, Yibo Lin, and David Z. Pan, "elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2021 (accepted)

[J2] Xiyuan Tang, Xiangxing Yang, Wenda Zhao, Chen-Kai Hsu, Jiaxin Liu, Linxiao Shen, Abhishek Mukherjee, Wei Shi, Shaolan Li, David Z. Pan, and Nan Sun, "A 13.5-ENOB, 107-μW Noise-Shaping SAR ADC with PVT-Robust Closed-Loop Dynamic Amplifier," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 55, No. 12, pp. 3248-3259, Dec. 2020. https://doi.org/10.1109/JSSC.2020.3020194

[J3] Hao Chen*, Mingjie Liu*, Biying Xu*, Keren Zhu*, Xiyuan Tang, Shaolan Li, Yibo Lin, Nan Sun and David Z. Pan, "MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII," *IEEE Design & Test*, 2020 (accepted) (* indicates equal contributions in alphabetical order) https://doi.org/10.1109/MDAT.2020.3024153

[J4] Chenghao Feng, Zhoufeng Ying, Zheng Zhao, Jiaqi Gu, David Z. Pan, and Ray T. Chen, "Wavelength-division-multiplexing (WDM)-based integrated electronic–photonic switching network (EPSN) for high-speed data processing and transportation," *Nanophotonics,* Vol. 9, No. 15, Sept. 2020. https://doi.org/10.1515/nanoph-2020-0356

[J5] Yibo Lin, Zixuan Jiang, Jiaqi Gu, Wuxi Li, Shounak Dhar, Haoxing Ren, Brucek Khailany, and David Z. Pan, "DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2020. https://doi.org/10.1109/TCAD.2020.3003843

[J6] Junzhe Cai, Changhao Yan, Yudong Tao, Yibo Lin, Shengguo Wang, David Z. Pan, and Xuan Zeng, "A Novel and Unified Full-chip CMP Model Aware Dummy Fill Insertion Framework with SQP-Based Optimization Method," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2020. 10.1109/TCAD.2020.3001380

[J7] Xiyuan Tang, Shaolan Li, Xiangxing Yang, Linxiao Shen, Wenda Zhao, Randall P. Williams, Jiaxin Liu, Zhichao Tan, Neal A. Hall, David Z. Pan, and Nan Sun, "An Energy-Efficient Time-

Domain Incremental Zoom Capacitance-to-Digital Converter," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 55, No. 11, pp. 3064-3075, 2020. https://doi.org/10.1109/JSSC.2020.3005812

[J8] Jing Chen, Mohamed Baker Alawieh, Yibo Lin, Maolin Zhang, Jun Zhang, Yufeng Guo, and David Z. Pan, "Automatic Selection of Structure Parameters of Silicon on Insulator Lateral Power Device Using Bayesian Optimization," *IEEE Electron Device Letters*, vol. 41, no. 9, pp. 1288-1291, Sept. 2020. https://doi.org/10.1109/LED.2020.3013571

[J9] Mohamed Baker Alawieh, Yibo Lin, Zaiwei Zhang, Meng Li, Qixing Huang, and David Z. Pan, "GAN-SRAF: Sub-Resolution Assist Feature Generation using Generative Adversarial Networks," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2020. https://doi.org/10.1109/TCAD.2020.2995338

[J10] Shaolan Li, David Z. Pan, and Nan Sun, "An OTA-Less Second-Order VCO-Based CT ΔΣ Modulator Using an Inherent Passive Integrator and Capacitive Feedback," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 55, No. 5, pp. 1337-1350, May 2020. https://doi.org/10.1109/JSSC.2019.2941007

[J11] Zhoufeng Ying, Chenghao Feng, Zheng Zhao, Shounak Dhar, Hamed Dalir, Jiaqi Gu, Yue Cheng, Richard Soref, David Z. Pan and Ray T. Chen, "Electronic-photonic arithmetic logic unit for high-speed computing," *Nature Communications,* Vol. 11, 2154, May 2020. https://doi.org/10.1038/s41467-020-16057-3

[J12] Yibo Lin, Wuxi Li, Jiaqi Gu, Haoxing Ren, Brucek Khailany, "ABCDPlace: Accelerated Batch-based Concurrent Detailed Placement on Multi-threaded CPUs and GPUs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2020. https://doi.org/10.1109/TCAD.2020.2971531

[J13] Chenghao Feng, Zhoufeng Ying, Zheng Zhao, Rohan Mital, David Z. Pan, and Ray T. Chen, "Analysis of Microresonator-Based Logic Gate for High-Speed Optical Computing in Integrated Photonics," *IEEE Journal of Selected Topics in Quantum Electronics,* Vol. 26, No. 2, March-April 2020, https://doi.org/10.1109/JSTQE.2019.2960949

[J14] Jing Chen, Mohamed Baker Alawieh, Yibo Lin, Maolin Zhang, Jun Zhang, Yufeng Guo, and David Z. Pan, "PowerNet: SOI Lateral Power Device Breakdown Prediction With Deep Neural Networks," *IEEE Access*, Feb. 2020. https://doi.org/10.1109/ACCESS.2020.2970966

[J15] David Z. Pan, "Report on the 38th ACM/IEEE International Conference on Computer-Aided Design (ICCAD 2019)**,"** *IEEE Design & Test*, 2020, https://doi.org/10.1109/MDAT.2020.2964756

[J16] Taehyun Kwon, Muhammad Imran, David Z. Pan, and Joon-Sung Yang, "Virtual Tile Based Flip-flop Alignment Methodology for Clock Network Power Optimization," *IEEE Transactions on VLSI Systems (TVLSI)*, Vol. 28, no. 5, May 2020. https://doi.org/10.1109/TVLSI.2020.2966912

[J17] Xiyuan Tang, Linxiao Shen, Begum Kasap, Xiangxing Yang, Wei Shi, Abhishek Mukherjee, David Z. Pan, and Nan Sun, "An Energy-Efficient Comparator with Dynamic Floating Inverter Amplifier," *IEEE Journal of Solid-State Circuits (JSSC)*, Jan. 2020. https://doi.org/10.1109/JSSC.2019.2960485

[J18] Mohamed Baker Alawieh, Yibo Lin, Wei Ye, and David Z. Pan, "Generative Learning in VLSI Design for Manufacturability: Current Status and Future Directions," *Journal of Microelectronic Manufacturing*, Vol. 2, No. 4, Dec. 2019, (**Invited Paper**) https://doi.org/10.33079/jomm.19020401

[J19] Wenda Zhao, Shaolan Li, Biying Xu, Xiangxing Yang, Xiyuan Tang, Linxiao Shen, Nanshu Lu, David Z. Pan, and Nan Sun, "A 0.025-mm² 0.8-V 78.5-dB SNDR VCO-Based Sensor Readout Circuit in a Hybrid PLL-Δ ΣM Structure," *IEEE Journal of Solid-State Circuits (JSSC)*, Dec., 2019, https://doi.org/10.1109/JSSC.2019.2959479

[J20] Ying Chen, Yibo Lin, Lisong Dong, Tianyang Gai, Rui Chen, Yajuan Su, Yayi Wei and David Z. Pan, "SoulNet: Ultrafast Optical Source Optimization Utilizing Generative Neural Networks for Advanced Lithography," *Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)*, 18(4), 043506, Nov. 2019. https://doi.org/10.1117/1.JMM.18.4.043506

[J21] Wuxi Li and David Z. Pan, "A New Paradigm for FPGA Placement without Explicit Packing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 38, No. 1, Nov. 2019. https://doi.org/10.1109/TCAD.2018.2877017

[J22] Yibo Lin, Meng Li, Yuki Watanabe, Taiki Kimura, Tetsuaki Matsunawa, Shigeki Nojima, and David Z. Pan, "Data Efficient Lithography Modeling with Transfer Learning and Active Data Selection,"

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct. 2019. https://doi.org/10.1109/TCAD.2018.2864251

[J23] Meng Li, Bei Yu, Yibo Lin, Xiaoqing Xu, Wuxi Li, and David Z. Pan, "A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Sept. 2019. https://doi.org/10.1109/TCAD.2018.2859402

[J24] Kaveh Shamsi, Meng Li, Kenneth Plaks, Saverio Fazzari, David Z. Pan, and Yier Jin, "IP Protection and Supply Chain Security through Logic Obfuscation: A Systematic Overview," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Sept. 2019. https://doi.org/10.1145/3342099

[J25] Meng Li, Kaveh Shamsi, Travis Meade, Zheng Zhao, Bei Yu, Yier Jin, and David. Z. Pan, "Provably Secure Camouflaging Strategy for IC Protection," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vo. 38, No. 8, pp. 1399-1412, August 2019 https://doi.org/10.1109/TCAD.2017.2750088

[J26] Derong Liu, Bei Yu, Vinicius Livramento, Salim Chowdhury, Duo Ding, Huy Vo, Akshay Sharma, and David Z. Pan, "Synergistic Topology Generation and Route Synthesis for On-Chip Performance-Critical Signal Groups," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 38, no. 6, June 2019. https://doi.org/10.1109/TCAD.2018.2834424

[J27] Abhishek Mukherjee, Miguel Gandara, Biying Xu, Shaolan Li, Linxiao Shen, Xiyuan Tang, David Z. Pan, and Nan Sun, "A 1-GS/s 20 MHz-BW Capacitive-Input Continuous-Time ΔΣ ADC Using a Novel Parasitic Pole-Mitigated Fully Differential VCO," *IEEE Solid-State Letters*, April 2019. https://doi.org/10.1109/LSSC.2019.2911874

[J28] Ying Chen, Yibo Lin, Tianyang Gai, Yajuan Su, Yayi Wei, and David Z. Pan, "Semi-Supervised Hotspot Detection with Self-Paced Multi-Task Learning," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, April 2019 https://doi.org/10.1109/TCAD.2019.2912948

[J29] Jing Chen, Yibo Lin, Yufeng Guo, Maolin Zhang, Mohamed B. Alawieh, and David Z. Pan, "Lithography Hotspot Detection Using a Double Inception Module Architecture," *Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)*, 18(1), 013507, 2019 https://doi.org/10.1117/1.JMM.18.1.013507

[J30] Shaolan Li, Qiao Bo, Miguel Gandara, David Z. Pan, and Nan Sun, "A 13-ENOB Second-Order Noise-Shaping SAR ADC Realizing Optimized NTF Zeros Using the Error-Feedback Structure," *IEEE Journal of Solid-State Circuits (JSSC)*, Oct. 2018. https://doi.org/10.1109/JSSC.2018.2871081

[J31] Xinquan Li, Bei Yu, Jiaojiao Ou, Jianli Chen, David Z. Pan, and Wenxin Zhu, "Graph Based Redundant Via Insertion and Guiding Template Assignment for DSA-MP," *IEEE Transactions on VLSI Systems (TVLSI)*, July 2018 https://doi.org/10.1109/TVLSI.2018.2850044

[J32] Kaveh Shamsi, Meng Li, David Z. Pan, and Yier Jin, "On the Approximation Resiliency of Logic Locking and IC Camouflaging Schemes," *IEEE Transactions on Information Forensics & Security (TIFS)*, Vol. 14, no. 2, pp. 347-359, June 2018. https://doi.org/10.1109/TIFS.2018.2850319

[J33] Hao Zhou, Hengliang Zhu, Tao Cui, David Z. Pan, Dian Zhou, and Xuan Zeng, "An Improved Domain Decomposition Method for Drop Impact Reliability Analysis of 3D ICs," *IEEE Transactions on Components, Packaging and Manufacturing Technology (TCPMT)*, Vol. 8, no. 10, pp. 1788-1799, Oct. 2018 https://doi.org/10.1109/TCPMT.2018.2853157

[J34] Zhoufeng Ying, Shounak Dhar, Zheng Zhao, David Z. Pan, Richard Soref, and Ray T. Chen, "Electro-Optic Ripple-Carry Adder in Integrated Silicon Photonics for Optical Computing," *IEEE Journal of Selected Topics in Quantum Electronics (JSTQE)*, Vol. 24, No. 6, Nov.-Dec. 2018. https://doi.org/10.1109/JSTQE.2018.2836955

[J35] Zhoufeng Ying, Zheng Zhao, Chenghao Feng, Rohan Mital, Shounak Dhar, David Z. Pan, Richard Soref, and Ray T. Chen, "Automated logic synthesis for electro-optic logic-based integrated optical computing," *Optics Express*, 26, no. 21, Oct. 15, 2018.

[J36] David Z. Pan, "Directed self-assembly for advanced chips," ***Nature Electronics***, Vol. 1, no. 10, pp. 530-531, Oct. 2018. https://doi.org/10.1038/s41928-018-0152-7

[J37] Hao Zhou, Hengliang Zhu, Tao Cui, David Z. Pan, Dian Zhou, and Xuan Zeng, "Thermal Stress and Reliability Analysis of TSV-Based 3-D ICs With a Novel Adaptive Strategy Finite Element

Method," *IEEE Transactions on VLSI Systems (TVLSI)*, Vol. 26, No. 7, pp. 1312-1325, July 2018. https://doi.org/10.1109/TVLSI.2018.2811417

[J38] Jun Zhang, Yufeng Guo, David Z. Pan, Kemeng Yang, Xiaojuan Lian, Jiafei Yao, and Man Li, "A New Physical Insight for the 3-D-Layout-Induced Cylindrical Breakdown in Lateral Power Devices on SOI Substrate," *IEEE Transactions on Electron Devices*, Vol. 65, No. 5, pp. 1843-1848, May 2018.

[J39] Ye Zhang, Wenlong Lv, Wai-Shing Luk, Fan Yang, Hai Zhou, Dian Zhou, David Z. Pan, and Xuan Zeng, "Cut Redistribution and Insertion for Advanced 1D Layout Design via Network Flow Optimization," *IEEE Transactions on VLSI Systems (TVLSI)*, 2018 https://doi.org/10.1109/TVLSI.2018.2828603

[J40] Wuxi Li, Yibo Lin, Meng Li, Shounak Dhar and David Z. Pan, "UTPlaceF 2.0: A High-Performance Clock-Aware FPGA Placement Engine," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 23, no. 4, July 2018 https://doi.org/10.1145/3174849

[J41] Zhoufeng Ying, Zheng Wang, Zheng Zhao, Shounak Dhar, David Z. Pan, Richard Soref, and Ray T. Chen, "Silicon microdisk-based full adders for optical computing," *Optics Letters*, Vol. 43, issue 5, pp. 983-986, (2018), https://doi.org/10.1364/OL.43.000983

[J42] Kemeng Yang, Yufeng Guo, David Z. Pan, Jun Zhang, Man Li, Yi Tong, Lin He, and Jiafei Yao, "A Novel Variation of Lateral Doping Technique in SOI LDMOS With Circular Layout," *IEEE Transactions on Electron Devices* (TED), Vol. 65, no. 4, pp. 1447-1452, April 2018 https://doi.org/10.1109/TED.2018.2808193

[J43] Zhoufeng Ying, Zheng Wang, Zheng Zhao, Shounak Dhar, David Z. Pan, Richard Soref, *and* Ray T. Chen, "Comparison of microrings and microdisks for high-speed optical modulation in silicon photonics, *Applied Physics Letters*, 112, 111108 (2018); https://doi.org/10.1063/1.5019590

[J44] Yibo Lin, Bei Yu, Meng Li, and David Z. Pan, "Layout Synthesis for Topological Quantum Circuits with 1D and 2D Architectures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 38, No. 8, Aug. 2018 https://doi.org/10.1109/TCAD.2017.2760511

[J45] Yibo Lin, Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, Natarajan Viswanathan, Wen-Hao Liu, Zhuo Li, Charles J. Alpert and David Z. Pan, "MrDP: Multiple-row Detailed Placement of Heterogeneous-sized Cells for Advanced Nodes," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 37, No. 6, pp. 1237-1250, June 2018 https://doi.org/10.1109/TCAD.2017.2748025

[J46] Xiaoqing Xu, Yibo Lin, Meng Li, Tetsuaki Matsunawa, Shigeki Nojima, Chikaaki Kodama, Toshiya Kotani, and David Z. Pan, "Sub-Resolution Assist Feature Generation with Supervised Data Learning," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 37, No. 6, pp. 1225-1236, June 2018, https://doi.org/10.1109/TCAD.2017.2748029

[J47] Wuxi Li, Shounak Dhar, and David Z. Pan, "UTPlaceF: A Routability-Driven FPGA Placer with Physical and Congestion Aware Packing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 37, No. 4, pp. 869-882, April 2018, https://doi.org/10.1109/TCAD.2017.2729349

[J48] Hengliang Zhu, Feng Hu, Hao Zhou, Dian Zhou, Xuan Zeng, and David Z. Pan, "Interlayer Cooling Network Design for High-Performance 3D-ICs Using Channel Patterning and Pruning," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 37, No. 4, pp. 770-781, April 2018 https://doi.org/10.1109/TCAD.2017.2731683

[J49] Jun Zhang, Yu-Feng Guo, David Z. Pan, Ke-Meng Yang, Xiao-Juan Lian, and Jia-Fei Yao, "Effective Doping Concentration Theory: A New Physical Insight for the Double-RESURF Lateral Power Devices on SOI Substrate," *IEEE Transactions on Electron Devices (TED)*, Vol. 65, No. 2, pp. 648-654, Feb. 2018

[J50] Taehee Lee, David Z. Pan, and Joon-Sung Yang, "Clock Network Optimization with Multi-bit Flip-flop Generation Considering Multicorner Multimode Timing Constraint," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 37, No. 1, pp. 245-256, Jan. 2018 https://doi.org/10.1109/TCAD.2017.2698025

[J51] Derong Liu, Bei Yu, Salim Chowdhury, and David Z. Pan, "TILA-S: Timing-Driven Incremental Layer Assignment Avoiding Slew Violations," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 37, No. 1, pp. 231-244, Jan 2018 https://doi.org/10.1109/TCAD.2017.2652221

[J52] Yunfeng Yang, Wai-Shing Luk, Hai Zhou, David Z. Pan, Changhao Yan, Dian Zhou, and Xuan Zeng, "An Effective Layout Decomposition Method for DSA with Multiple Patterning in Contact-Hole Generation," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 23, No. 1, Article 11, September 2017 https://doi.org/10.1145/3131847

[J53] Yibo Lin, Bei Yu, and David Z. Pan, "High Performance Dummy Fill Insertion with Coupling and Uniformity Constraints," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 36, No. 9, pp. 1532-1544, Sept. 2017. https://doi.org/10.1109/TCAD.2016.2638452

[J54] Derong Liu, Bei Yu, Salim Chowdhury, and David Z. Pan, "Incremental Layer Assignment for Timing Optimization," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 22, No. 4, Article 75, July 2017 https://doi.org/10.1145/3083727

[J55] Yibo Lin, Bei Yu, Biying Xu, and David Z. Pan, "Triple Patterning Aware Detailed Placement Toward Zero Cross-Row Middle-of-Line Conflict," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 37, Issue 7, pp. 1140-1152, July 2017 https://doi.org/10.1109/TCAD.2017.2648843

[J56] Vinicius Livramento, Derong Liu, Salim Chowdhury, Bei Yu, Xiaoqing Xu, David Z. Pan, Jos´e Lu´ıs G¨untzel, and Luiz C. V. dos Santos, "Incremental Layer Assignment Driven by an External Signoff Timing Engine," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 37, Issue 7, pp. 1126-1139, July 2017 https://doi.org/10.1109/TCAD.2016.2638450

[J57] Xiaoqing Xu, Yibo Lin, Meng Li, Jiaojiao Ou, Brian Cline, and David Z. Pan, "Redundant Local-Loop Insertion for Unidirectional Routing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 37, Issue 7, pp. 1113-1125, July 2017 https://doi.org/10.1109/TCAD.2017.2651811

[J58] Yibo Lin, Bei Yu, Yi Zou, Zhuo Li, Charles J. Alpert, and David Z. Pan**, "**Stitch Aware Detailed Placement for Multiple E-Beam Lithography," *Integration, the VLSI Journal*, vol. 58, pp. 47-54, June 2017 https://doi.org/10.1016/j.vlsi.2017.02.004 **(Best Paper Award)**

[J59] Yibo Lin, Xiaoqing Xu, Bei Yu, Ross Baldick and David Z. Pan, "Triple/Quadruple Patterning Layout Decomposition via Novel Linear Programming and Iterative Rounding," *Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)*, Vol. 16, No. 2, 023507, June 2017 https://doi.org/10.1117/1.JMM.16.2.023507

[J60] Xiaoqing Xu and David Z. Pan, "Toward Unidirectional Routing Closure in Advanced Technology Nodes," *IPSJ Transactions on System LSI Design Methodology*, Vol.10, pp. 2–12, Feb. 2017 **(Invited Paper)** http://doi.org/10.2197/ipsjtsldm.10.2

[J61] Jun Zhang, Yu-Feng Guo, David Z. Pan, and Ke-Meng Yang, "A Novel 3-D Analytical Method for Curvature Effect-Induced Electric Field Crowding in SOI Lateral Power Device," *IEEE Transactions on Electron Devices*, vol. 63, no. 11, pp. 4359 - 4365, Nov. 2016 https://doi.org/10.1109/TED.2016.2609908

[J62] Tetsuaki Matsunawa, Bei Yu, and David Z Pan, "Laplacian Eigenmaps and Bayesian Clustering Based Layout Pattern Sampling and Its Applications to Hotspot Detection and OPC," *Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)*, 15(4), 043504, Oct. 2016. http://dx.doi.org/10.1117/1.JMM.15.4.043504

[J63] Subhendu Roy, Derong Liu, Jagmohan Singh, Junhyung Um, and David. Z. Pan, "OSFA: A New Paradigm of Aging Aware Gate-Sizing for Power/Performance Optimizations under Multiple Operating Conditions," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 35, no. 10, pp. 1618-1629, Oct. 2016. Available at http://dx.doi.org/10.1109/TCAD.2016.2523439

[J64] Yunfeng Yang, Wai-Shing Luk, David Z. Pan, Hai Zhou, Changhao Yan, Dian Zhou, and Xuan Zeng, "Layout Decomposition Co-optimization for Hybrid E-Beam and Multiple Patterning Lithography," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 35, no. 9., September 2016. http://dx.doi.org/10.1109/TCAD.2015.2512903

[J65] Xiaoqing Xu, Bei Yu, Jhih-Rong Gao, Che-Lun Hsu and David Z. Pan, "PARR: Pin Access Planning and Regular Routing for Self-Aligned Double Patterning," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 21, no. 3, July 2016. http://dx.doi.org/10.1145/2842612

[J66] Bei Yu, Xiaoqing Xu, Subhendu Roy, Yibo Lin, Jiaojiao Ou, and David Z. Pan, "Design for Manufacturability and Reliability in Extreme-Scaling VLSI," *Science China Information Sciences (SCIS),* vol.59, June, 061406:2, 2016. (**Invited Paper**) https://doi.org/10.1007/s11432-016-5560-6

[J67] Xiaoqing Xu, Brian Cline, Greg Yeric, Bei Yu and David Z. Pan, "A Systematic Framework for Evaluating Standard Cell Middle-Of-Line (MOL) Robustness for Multiple Patterning Lithography," *Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)*, vol. 15, no. 2, 021202, 2016. Available at http://dx.doi.org/10.1117/1.JMM.15.2.021202

[J68] Tetsuaki Matsunawa, Bei Yu, and David Z Pan, "Optical Proximity Correction with Hierarchical Bayes Model," *Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)*, vol. 15, no. 2, 021009, 2016. Available at http://dx.doi.org/10.1117/1.JMM.15.2.021009

[J69] Subhendu Roy, Mihir Choudhury, Ruchir Puri, and David Z. Pan, "Polynomial Time Algorithm for Area and Power Efficient Adder Synthesis in High-Performance Designs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 35, no. 5, pp. 820-831, May 2016. Available at http://dx.doi.org/10.1109/TCAD.2015.2481794

[J70] Ye Zhang, Wai-Shing Luk, Yunfeng Yang, Hai Zhou, Changhao Yan, David Z. Pan, and Xuan Zeng, "Layout Decomposition with Pairwise Coloring and Adaptive Multi-Start for Triple Patterning Lithography," *ACM Transactions on Design Automation of Electronic Systems*, vol. 21, no. 1, Nov. 2015, Available at http://dx.doi.org/10.1145/2764904

[J71] Jiaojiao Ou, Bei Yu, Jhih-Rong Gao, Moshe Preil, Azat Latypov, and David Z Pan, "Directed Self-Assembly (DSA) Cut Mask Assignment for Unidirectional Design," *The Journal of Microlithography, Microfabrication, and Microsystems (JM3)*, vol. 14, no. 3, 031211, Aug., 2015, Available at http://dx.doi.org/10.1117/1.JMM.14.3.031211

[J72] Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, Yibo Lin, Zhuo Li, Charles Alpert, and David Z. Pan, "Methodology for Standard Cell Compliance and Detailed Placement for Triple Patterning Lithography," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 34, no. 5, pp. 726 – 739, May 2015. Available at http://dx.doi.org/10.1109/TCAD.2015.2401571

[J73] Xiaoqing Xu, Brian Cline, Greg Yeric, Bei Yu, and David Z. Pan, "Self-Aligned Double Patterning Aware Pin Access and Standard Cell Layout Co-Optimization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 34, no. 5, pp. 699-712 May 2015. Available at http://dx.doi.org/10.1109/TCAD.2015.2399439

[J74] Subhendu Roy, Pavlos M. Mattheakis, Laurent Masse-Navette, and David Z. Pan, "Clock Tree Resynthesis for Multi-corner Multi-mode Timing Closure," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 34, no. 4, pp. 589-602, April 2015. Available at http://dx.doi.org/10.1109/TCAD.2015.2394310

[J75] Bei Yu, Kun Yuan, Duo Ding, and David Z. Pan, "Layout Decomposition for Triple Patterning Lithography," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 34, no. 3, pp. 433 – 446, March 2015. Available at http://dx.doi.org/10.1109/TCAD.2014.2387840

[J76] Yongchan Ban and David Z. Pan, "Self-Aligned Double Patterning Layout Decomposition for 2D Random Metals for Sub-10nm Node Design," *SPIE Journal of Microlithography, Microfabrication, and Microsystems (JM3)*, vol. 14, no. 1, pp. 011004, Jan-Mar 2015. Available at http://dx.doi.org/10.1117/1.JMM.14.1.011004

[J77] Bei Yu, Jhih-Rong Gao, Duo Ding, Xuan Zeng, and David Z. Pan, "Accurate Lithography Hotspot Detection based on Principal Component Analysis-Support Vector Machine Classifier with Hierarchical Data Clustering," *SPIE Journal of Microlithography, Microfabrication, and Microsystems (JM3)*, vol. 14, no. 1, pp. 011003, Jan-Mar 2015. Available at http://dx.doi.org/10.1117/1.JMM.14.1.011003

[J78] Bei Yu, Subhendu Roy, Jhih-Rong Gao, and David Z. Pan, "Triple Patterning Lithography Layout Decomposition Using End-cutting," *SPIE Journal of Microlithography, Microfabrication, and Microsystems (JM3)*, vol. 14, no. 1, pp. 011002, Jan-Mar 2015. Available at http://dx.doi.org/10.1117/1.JMM.14.1.011002

[J79] Jiwoo Pak, Sung Kyu Lim, and David Z. Pan, "Electromigration Study for Multi-scale Power/Ground Vias in TSV-based 3D ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 33, no. 12, Dec. 2014. Available at http://dx.doi.org/10.1109/TCAD.2014.2360456

[J80] Subhendu Roy, Mihir Choudhury, Ruchir Puri, and David Z. Pan, "Toward Optimal Performance-Area Trade-Off in Adders by Synthesis of Parallel Prefix Structures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 33, no. 10, pp. 1517—1530, Oct. 2014. Available at http://dx.doi.org/10.1109/TCAD.2014.2341926

[J81] Moongon Jung, Joydeep Mitra, David Z. Pan, and Sung Kyu Lim, "Full-Chip Mechanical Reliability Analysis and Optimization for 3D ICs," *Communications of the ACM* (**Research Highlights**), Vol. 57, No. 1, pp. 107-115, Jan. 2014. Available at http://dx.doi.org/10.1145/2494536

[J82] Runsheng Wang, Xiaobo Jiang, Tao Yu, Jiewen Fan, Jiang Chen, David Z. Pan, and Ru Huang, "Investigations on Line-Edge Roughness (LER) and Line-Width Roughness (LWR) in Nanoscale CMOS Technology: Part II – Experimental Results and Impacts on Device Variability," *IEEE Transactions on Electron Devices*, vol. 60, no. 11, pp. 3676-3682, Nov. 2013. Available at http://dx.doi.org/10.1109/TED.2013.2283517

[J83] Moongon Jung, David Z. Pan, and Sung Kyu Lim, "Chip/Package Mechanical Stress Impact on 3D IC Reliability and Mobility Variations," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 11, Nov. 2013. Available at http://dx.doi.org/10.1109/TCAD.2013.2265372

[J84] David Z. Pan, Bei Yu, and Jhih-Rong Gao, "Design for Manufacturing with Emerging Nanolithography," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 10, pp. 1453 – 1472, Oct. 2013. (**Keynote Paper**) Available at: http://dx.doi.org/10.1109/TCAD.2013.2276751

[J85] Wooyoung Jang and David Z. Pan, "Chemical-Mechanical Polishing Aware Application-Specific 3D NoC Design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 6, pp. 940-951, June 2013. Available at: http://dx.doi.org/10.1109/TCAD.2013.2237771

[J86] Krit Athikulwongse, Jae-Seok Yang, David Z. Pan, and Sung Kyu Lim, "Impact of Mechanical Stress on the Full Chip Timing for TSV-based 3D ICs," *IEEE Transactions on Computer- Aided Design of Integrated Circuits and Systems (TCAD)*. vol. 32, no. 6, pp. 905-917, June 2013. Available at: http://dx.doi.org/10.1109/TCAD.2013.2237770

[J87] Ashutosh Chakraborty and David Z. Pan, "Skew Management of NBTI Impacted Gated Clock Trees," I*EEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 6, pp. 918-927, June 2013. Available at: http://dx.doi.org/10.1109/TCAD.2012.2195002

[J88] Samuel I. Ward, Myung-Chul Kim, Natarajan Viswanathan, Zhuo Li, Charles Alpert, Earl E. Swartzlander Jr., and David Z. Pan, "Structure-Aware Placement Techniques for Designs with Datapath," *IEEE Transactions on Computer- Aided Design of Integrated Circuits and Systems (TCAD)*. vol. 32, no. 2, pp. 228-241, February 2013. Available at: http://dx.doi.org/10.1109/TCAD.2012.2233862

[J89] Moongon Jung, Joydeep Mitra, David Z. Pan, and Sung Kyu Lim, "TSV Stress-aware Full-Chip Mechanical Reliability Analysis and Optimization for 3D IC," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 31, no. 8, pp. 1194-1207, August 2012. Available at: http://dx.doi.org/10.1109/TCAD.2012.2188400

[J90] Wooyoung Jang and David Z. Pan, "A3MAP: Architecture-Aware Analytic Mapping for Networks-on-Chip," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 17, no. 3, June 2012. Available at: http://dx.doi.org/10.1145/2209291.2209299

[J91] Kun Yuan, Bei Yu, and David Z. Pan, "E-Beam Lithography Stencil Planning and Optimization with Overlapped Characters," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 31, no. 2, pp. 167-179, February 2012. Available at: http://dx.doi.org/10.1109/TCAD.2011.2179041

[J92] Duo Ding, J. Andres Torres, and David Z. Pan, "High Performance Lithography Hotspot Detection with Successively Refined Pattern Identifications and Machine Learning," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 30, no. 11, pp. 1621-1634, November 2011. Available at: http://dx.doi.org/10.1109/TCAD.2011.2164537

[J93] Wooyoung Jang and David Z. Pan, "Application-Aware NoC Design for Efficient SDRAM Access," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol.

30, no. 10, pp. 1521-1533, October 2011. Available at: http://dx.doi.org/10.1109/TCAD.2011.2160176

[J94] Wooyoung Jang and David Z. Pan, "A Voltage-Frequency Island Aware Energy Optimization Framework for Networks-on-Chip," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS),* vol. 1, no. 3, pp. 420-432, September 2011. Available at: http://dx.doi.org/10.1109/JETCAS.2011.2165756

[J95] Ou He, Sheqin Dong, Wooyoung Jang, Jinian Bian, and David Z. Pan, "UNISM: Unified Scheduling and Mapping for General Networks on Chip," *IEEE Transactions on VLSI Systems (TVLSI)*, vol. 20, no. 8, pp. 1496-1509, July 2011. Available at: http://dx.doi.org/10.1109/TVLSI.2011.2159280

[J96] Ryan A. Integlia, Lianghong Yin, Duo Ding, David Z. Pan, Douglas M. Gill, and Wei Jiang, "Parallel-Coupled Dual Racetrack Silicon Micro-Resonators for Quadrature Amplitude Modulation," *Optics Express*, vol. 19, no. 16, pp. 14892-14902, August 2011. Available at: http://dx.doi.org/10.1364/OE.19.014892

[J97] Yongchan Ban and David Z. Pan, "Modeling of Layout Aware Line-Edge Roughness and Poly Optimization for Leakage Minimization," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS*), vol. 1, no. 2, pp. 150-159, June 2011. Available at: http://dx.doi.org/10.1109/JETCAS.2011.2159286

[J98] Anand Rajaram and David Z. Pan, "Robust Chip-Level Clock Tree Synthesis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 30, no. 6, pp. 877-890, June 2011. Available at: http://dx.doi.org/10.1109/TCAD.2011.2106852

[J99] Anand Ramalingam, Ashish Kumar Singh, Sani R. Nassif, Gi-Joon Nam, Michael Orshansky, and David Z. Pan, "An Accurate Sparse-Matrix Based Framework for Statistical Static Timing Analysis," *Integration, the VLSI Journal*, March 2011. Available at: http://dx.doi.org/10.1016/j.vlsi.2011.03.002

[J100] Anand Rajaram and David Z. Pan, "MeshWorks: A Comprehensive Framework for Optimized Clock Mesh Network Synthesis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 29, no. 12, pp. 1945-1958, December 2010. Available at: http://dx.doi.org/10.1109/TCAD.2010.2061130

[J101] Yongchan Ban, Savithri Sundareswaran, and David Z. Pan, "Electrical Impact of Line-Edge Roughness on Sub-45nm Node Standard Cells," *SPIE Journal of Microlithography, Microfabrication, and Microsystems (JM3)*, vol. 9, no. 4, pp. 041206, December 2010. Available at: http://dx.doi.org/10.1117/1.3500746

[J102] Yongchan Ban, David Z. Pan, Yuansheng Ma, and Harry J. Levinson, "Modeling and Characterization of Contact-Edge Roughness for Minimizing Design and Manufacturing Variations," *SPIE Journal of Microlithography, Microfabrication, and Microsystems (JM3)*, vol. 9, no. 4, pp. 041211, October 2010. Available at: http://dx.doi.org/10.1117/1.3504697

[J103] Wooyoung Jang and David Z. Pan, "An SDRAM-Aware Router for Networks-on-Chip," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 29, no. 10, pp. 1572-1585, October 2010. Available at: http://dx.doi.org/10.1109/TCAD.2010.2061251

[J104] Ashutosh Chakraborty, Sean X. Shi, and David Z. Pan, "Stress Aware Layout Optimization Leveraging Active Area Dependent Mobility Enhancement," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 29, no. 10, pp. 1533-1545, October 2010. Available at: http://dx.doi.org/10.1109/TCAD.2010.2061173

[J105] Xinyuan Dou, Xiaolong Wang, Xiaohui Lin, Duo Ding, David Z. Pan, and Ray T. Chen, "Highly Flexible Polymeric Optical Waveguide for Out-of-plane Optical Interconnects," *Optics Express*, vol.18, no. 15, pp. 16227-16233, July 2010. Available at: http://dx.doi.org/10.1364/OE.18.016227

[J106] Kun Yuan, Jae-Seok Yang, and David Z. Pan, "Double Patterning Layout Decomposition for Simultaneous Conflict and Stitch Minimization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), vol. 29, no. 2, pp. 185-196, February 2010. Available at: http://dx.doi.org/10.1109/TCAD.2009.2035577

[J107] David Z. Pan, Minsik Cho, and Kun Yuan, "Manufacturability Aware Routing in Nanometer VLSI," *Foundations and Trends in Electronic Design Automation*, vol. 4, no. 1, pp. 1-97, January 2010. Available at: http://dx.doi.org/10.1561/1000000015 **(Invited)**

[J108] Xinyuan Dou, Xiaolong Wang, Haiyu Huang, Xiaohui Lin, Duo Ding, David Z. Pan, and Ray T. Chen, "Polymeric Waveguides with Embedded Micro-mirrors Formed by Metallic Hard Mold,"

Optics Express, vol. 18, no. 1, pp. 378-385, December 2009. Available at: http://dx.doi.org/10.1364/OE.18.000378

[J109] Minsik Cho, Kun Yuan, Yongchan Ban, and David Z. Pan, "ELIAD: Efficient Lithography Aware Detailed Routing Algorithm with Compact and Macro Post-OPC Printability Prediction," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), vol. 28, no. 7, pp. 1006-1016, July 2009. Available at: http://dx.doi.org/10.1109/TCAD.2009.2018876

[J110] Peng Yu and David Z. Pan, "ELIAS: An Accurate and Extensible Lithography Aerial Image Simulator with Improved Numerical Algorithms," *IEEE Transactions on Semiconductor Manufacturing*, vol. 22, no. 2, pp. 276-289, May 2009. Available at: http://dx.doi.org/10.1109/TSM.2009.2017652

[J111] Minsik Cho, Katrina Lu, Kun Yuan, and David Z. Pan, "BoxRouter 2.0: A Hybrid and Robust Global Router with Layer Assignment for Routability," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 14, no. 2, pp. 351-372, March 2009. Available at: http://dx.doi.org/10.1145/1497561.1497575

[J112] David Z. Pan, Peng Yu, Minsik Cho, Anand Ramalingam, Kiwoon Kim, Anand Rajaram, and Sean X. Shi, "Design for Manufacturing Meets Advanced Process Control: A Survey," *Journal of Process Control*, vol. 18, no. 10, pp. 975-984, December 2008. Available at: http://dx.doi.org/10.1016/j.jprocont.2008.04.007

[J113] Tung-Chieh Chen, Minsik Cho, David Z. Pan, and Yao-Wen Chang, "Metal-Density-Driven Placement for CMP Variation and Routability," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), vol. 27, no. 12, pp. 2145-2155, December 2008. Available at: http://dx.doi.org/10.1109/TCAD.2008.2006148

[J114] Minsik Cho and David Z. Pan, "Fast Substrate Noise Aware Floorplanning for Mixed Signal SOC Designs," *IEEE Transactions on VLSI Systems*, vol. 16, no. 12, pp. 1713-1717, December 2008. Available at: http://dx.doi.org/10.1109/TVLSI.2008.2001734

[J115] Peng Yu, Weifeng Qiu, and David Z. Pan, "Fast Lithography Image Simulation By Exploiting Symmetries in Lithography Systems," *IEEE Transactions on Semiconductor Manufacturing*, vol. 21, no. 4, pp. 638-645, November 2008. Available at: http://dx.doi.org/10.1109/TSM.2008.2005380

[J116] Minsik Cho and David Z. Pan, "A High-Performance Droplet Routing Algorithm for Digital Microfluidic Biochips," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 27, no. 10, pp. 1714-1724, October 2008. Available at: http://dx.doi.org/10.1109/TCAD.2008.2003282

[J117] Minsik Cho, Hua Xiang, Ruchir Puri, and David Z. Pan, "Track Routing and Optimization for Yield," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 5, pp. 872-882, May 2008. Available at: http://dx.doi.org/10.1109/TCAD.2008.917589

[J118] Haoxing Ren, David Z. Pan, C. J. Alpert, P. Villarrubia, and Gi-Joon Nam, "Diffusion-Based Placement Migration with Application on Legalization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 12, pp. 2158-2172, December 2007. Available at: http://dx.doi.org/10.1109/TCAD.2007.907005

[J119] Minsik Cho and David Z. Pan, "BoxRouter: A New Global Router Based on Box Expansion and Progressive ILP," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 12, pp. 2130-2143, December 2007. Available at: http://dx.doi.org/10.1109/TCAD.2007.907003

[J120] Peng Yu, Sean X. Shi, and David Z. Pan, "True Process Variation Aware Optical Proximity Correction with Variational Lithography Modeling and Model Calibration," *SPIE Journal of Microlithography, Microfabrication, and Microsystems (JM3)*, *Special Edition of Resolution Enhancement Techniques and Design for Manufacturability*, vol. 6, no. 3, pp. 031004, September 2007. Available at: http://dx.doi.org/10.1117/1.2752814

[J121] Anand Ramalingam, Anirudh Devgan, and David Z. Pan, "Wakeup Scheduling in MTCMOS Circuits Using Successive Relaxation to Minimize Ground Bounce," *ASP Journal of Low Power Electronics (JOLP)*, vol. 3, no. 1, pp. 28-35, April 2007. Available at: http://dx.doi.org/10.1166/jolpe.2007.116

[J122] Haoxing Ren, David Z. Pan, and D. S. Kung, "Sensitivity Guided Net Weighting for Placement-Driven Synthesis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and*

Systems, vol. 24, no. 5, pp. 711-721, May 2005. Available at: http://dx.doi.org/10.1109/TCAD.2005.846367

[J123] Chin-Chih Chang, Jason Cong, David Z. Pan, and Xin Yuan, "Multilevel Global Placement with Congestion Control," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 4, pp. 395-409, April 2003. Available at: http://dx.doi.org/10.1109/TCAD.2003.809661

[J124] Jason Cong and David Z. Pan, "Wire Width Planning for Interconnect Performance Optimization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 21, no. 3, pp. 319-329, March 2002. Available at: http://dx.doi.org/10.1109/43.986425

[J125] Jason Cong, Tianming Kong, and David Z. Pan, "Buffer Block Planning for Interconnect Planning and Prediction," *IEEE Transactions on VLSI Systems (TVLSI)*, vol. 9, no. 6, pp. 929-937, December 2001. Available at: http://dx.doi.org/10.1109/92.974906

[J126] Jason Cong, L. He, Cheng-Kok Koh, and David Z. Pan, "Interconnect Sizing and Spacing with Consideration of Coupling Capacitance," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, no. 9, pp.1164-1169, September 2001. Available at: http://dx.doi.org/10.1109/43.945311

[J127] Jason Cong and David Z. Pan, "Interconnect Performance Estimation Models for Design Planning," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, no. 6, pp. 739-752, June 2001. Available at: http://dx.doi.org/10.1109/43.924827

B. Refereed Conference Proceedings

[C1] Hao Chen*, Mingjie Liu*, Xiyuan Tang*, Keren Zhu*, Abhishek Mukherjee, Nan Sun and David Z. Pan, "MAGICAL 1.0: An Open-Source Fully-Automated AMS Layout Synthesis Framework Verified With a 40-nm 1GS/s ΔΣ ADC," *IEEE Custom Integrated Circuits Conference (CICC),* April 25-31, 2021. (* equal contributions in alphabetic order)

[C2] Jiaqi Gu, Chenghao Feng, Zheng Zhao, Zhoufeng Ying, Ray T. Chen and David Z. Pan, "Efficient On-Chip Learning for Optical Neural Networks Through Power-Aware Sparse Zeroth-Order Optimization," *Association for the Advancement of Artificial Intelligence (AAAI)*, Feb. 2-9, 2021.

[C3] Shubham Rai, Walter Lau Neto, Yukio Miyasaka, Xinpei Zhang, Mingfei Yu, Qingyang Yi Masahiro Fujita, Guilherme B. Manske, Matheus F. Pontes, Leomar S. da Rosa Junior, Marilton S. de Aguiar, Paulo F. Butzen, Po-Chun Chien, Yu-Shan Huang, Hoa-Ren Wang, Jie-Hong R. Jiang, Jiaqi Gu, Zheng Zhao, Zixuan Jiang, David Z. Pan, Brunno A. de Abreu, Isac de Souza Campos, Augusto Berndt, Cristina Meinhardt, Jonata T. Carvalho, Mateus Grellert, Sergio Bampi, Aditya Lohana, Akash Kumar, Wei Zeng, Azadeh Davoodi, Rasit O. Topaloglu, Yuan Zhou, Jordan Dotzel, Yichi Zhang, Hanyu Wang, Zhiru Zhang, Valerio Tenace, Pierre-Emmanuel Gaillardon, Alan Mishchenko and Satrajit Chatterjee, "Logic Synthesis Meets Machine Learning: Trading Exactness for Generalization," *IEEE Design, Automation & Test in Europe (DATE) Conference*, Feb. 1-5, 2021 **(Invited Paper)** https://arxiv.org/pdf/2012.02530.pdf

[C4] Jiaqi Gu, Chenghao Feng, Zheng Zhao, Zhoufeng Ying, Mingjie Liu, Ray T. Chen and David Z. Pan, "SqueezeLight: Towards Scalable Optical Neural Networks with Multi-Operand Ring Resonators," *IEEE Design, Automation & Test in Europe (DATE) Conference*, Feb. 1-5, 2021.

[C5] Jiaqi Gu, Zheng Zhao, Chenghao Feng, Zhoufeng Ying, Ray T. Chen and David Z. Pan, "O2NN: Optical Neural Networks with Differential Detection-Enabled Optical Operands," *IEEE Design, Automation & Test in Europe (DATE) Conference*, Feb. 1-5, 2021.

[C6] Mingjie Liu, Walker Turner, George Kokai, Brucek Khailany, David Z. Pan and Haoxing Ren, "Parasitic-Aware Analog Circuit Sizing with Graph Neural Networks and Bayesian Optimization," *IEEE Design, Automation & Test in Europe (DATE) Conference*, Feb. 1-5, 2021.

[C7] Xiaohan Gao, Chenhui Deng, Mingjie Liu, Zhiru Zhang, David Z. Pan, and Yibo Lin, "Layout Symmetry Annotation for Analog Circuits with Graph Neural Networks," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 18-21, 2021.

[C8] Keren Zhu, Hao Chen, Mingjie Liu, Xiyuan Tang, Nan Sun and David Z. Pan, "Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 02-05, 2020. (**Best Paper Award Nomination from Track)**

[C9] Hao Chen, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun and David Z. Pan, "Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 02-05, 2020.

[C10] Jiaqi Gu, Zixuan Jiang, Yibo Lin and David Z. Pan, "DREAMPlace 3.0: Multi-Electrostatics Based Robust VLSI Placement with Region Constraints," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 02-05, 2020.

[C11] Mohamed Baker Alawieh, Wei Ye, and David Z. Pan, "Re-examining VLSI Manufacturing and Yield through the Lens of Deep Learning," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 02-05, 2020 (**Invited Paper**)

[C12] Rachel Selina Rajarathnam, Yibo Lin, Yier Jin, and David Z. Pan, "ReGDS: A Reverse Engineering Framework from GDSII to Gate-level Netlist," *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, San Jose, Dec. 6-9, 2020

[C13] Zixuan Jiang, Keren Zhu, Mingjie Liu, Jiaqi Gu, and David Z. Pan, "An Efficient Training Framework for Reversible Neural Architectures," *European Conference on Computer Vision (ECCV)*, Aug. 23-28, 2020

[C14] Jiaqi Gu, Zheng Zhao, Chenghao Feng, Wuxi Li, Ray T. Chen and David Z. Pan, "FLOPS: Efficient On-Chip Learning for Optical Neural Networks through Stochastic Zeroth-Order Optimization," *ACM/IEEE Design Automation Conference (DAC)*, July 19-23, 2020. **(Best Paper Candidate;** total 6 best paper candidates, from nearly 1,000 submissions**)**

[C15] Mingjie Liu, Keren Zhu, Xiyuan Tang, Biying Xu, Wei Shi, Nan Sun and David Z. Pan, "Closing the Design Loop: Bayesian Optimization Assisted Hierarchical Analog Layout Synthesis", *ACM/IEEE Design Automation Conference (DAC),* July 19-23, 2020.

[C16] Mohamed Baker Alawieh, Duane Boning and David Z. Pan, "Wafer Map Defect Patterns Classification using Deep Selective Learning," *ACM/IEEE Design Automation Conference (DAC),* July 19-23, 2020.

[C17] Navid Khoshavi, Arman Roohi, Connor Broyles, Saman Sargolzaei, Yu Bi and David Z. Pan, "SHIELDeNN: Online Accelerated Framework for Fault-Tolerant Deep Neural Network Architectures," *ACM/IEEE Design Automation Conference (DAC)*, July 19-23, 2020.

[C18] Chenghao Feng, Zheng Zhao, Zhoufeng Ying, Jiaqi Gu, David Z Pan, and Ray T Chen, "Compact Design of On-chip Elman Optical Recurrent Neural Network," *OSA Conference on Lasers and Electro-Optics (CLEO)*: Applications and Technology, May 10-15, 2020. https://doi.org/10.1364/CLEO_AT.2020.JTh2B.8

[C19] Chenghao Feng, Zhoufeng Ying, Zheng Zhao, Jiaqi Gu, David Z. Pan, and Ray T. Chen, "Integrated WDM-based Optical Comparator for High-speed Computing," *OSA Conference on Lasers and Electro-Optics (CLEO)*: Science and Innovations, pp. SM3O.1. May 10-15, 2020. https://doi.org/10.1364/CLEO_SI.2020.SM3O.1

[C20] Wei Ye, Mohamed Baker Alawieh, Yuki Watanabe, Shigeki Nojima, Yibo Lin and David Z. Pan, "TEMPO: Fast Mask Topography Effect Modeling with Deep Learning," *ACM International Symposium on Physical Design (ISPD),* 2020. **(Best Paper Award)** https://doi.org/10.1145/3372780.3375565

[C21] Mingjie Liu*, Keren Zhu*, Jiaqi Gu, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan, "Towards Decrypting the Art of Analog Layout, Placement Quality Prediction via Transfer Learning," *IEEE Design, Automation & Test in Europe (DATE)*, Mar. 09-13, 2020. (* indicates equal contributions in alphabetical order) https://doi.org/10.23919/DATE48585.2020.9116330

[C22] Jiaqi Gu, Zheng Zhao, Chenghao Feng, Hanqing Zhu, Ray T. Chen, David Z. Pan, "ROQ: A Noise-Aware Quantization Scheme Towards Robust Optical Neural Networks with Low-bit Controls," *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France, Mar. 09-13, 2020

[C23] Chenghao Feng, Zhoufeng Ying, Zheng Zhao, Jiaqi Gu, David Z. Pan, and Ray T. Chen, "Wavelength-division-multiplexing-based electronic-photonic network for high-speed computing," *SPIE OPTO Proceedings Volume 11284, Smart Photonic and Optoelectronic Integrated Circuits XXII;* 112840H, March 9, 2020. https://doi.org/10.1117/12.2551323

[C24] Xiyuan Tang, Xiangxing Yang, Wenda Zhao, Chen-Kai Hsu, Jiaxin Liu, Linxiao Shen, Abhishek Mukherjee, Wei Shi, David Z. Pan and Nan Sun, "A 13.5b-ENOB Second-Order Noise-Shaping SAR with PVT-Robust Closed-Loop Dynamic Amplifier," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, Feb. 16-20, 2020.

[C25] Jiaqi Gu, Zheng Zhao, Chenghao Feng, Mingjie Liu, Ray T. Chen, David Z. Pan, "Towards Area-Efficient Optical Neural Networks: An FFT-based Architecture," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Beijing, China, Jan. 13-16, 2020. **(Best Paper Award)**

[C26] Mingjie Liu, Wuxi Li, Keren Zhu, Biying Xu, Yibo Lin, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan, "S^{3}DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Beijing, China, Jan. 13-16, 2020. **(Best Paper Award Nomination)**

[C27] Mohamed Baker Alawieh, Wuxi Li, Yibo Lin, Love Singhal, Mahesh Iyer and David Z. Pan, "High-Definition Routing Congestion Prediction for Large-Scale FPGAs," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Beijing, China, Jan. 13-16, 2020.

[C28] Biying Xu, Mingjie Liu, Keren Zhu, Yibo Lin, Shaolan Li, Xiyuan Tang, Nan Sun, and David Z. Pan, "MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4-7, 2019 **(Invited Paper)**

[C29] Zheng Zhao, Zhoufeng Ying, Chenghao Feng, Jiaqi Gu, Ray T. Chen, and David Z. Pan, "Design Technology for Scalable and Robust Photonic Integrated Circuits," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4-7, 2019 **(Invited Paper)**

[C30] Keren Zhu, Mingjie Liu, Yibo Lin, Biying Xu, Shaolan Li, Xiyuan Tang, Nan Sun and David Z. Pan, "GeniusRoute: A New Analog Routing Paradigm Using Generative Neural Network Guidance," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4-7, 2019 **(Best Paper Award Nomination from Track)**

[C31] Wuxi Li, Yibo Lin, and David Z. Pan, "elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4-7, 2019

[C32] Chengyue Gong, Zixuan Jiang, Dilin Wang, Yibo Lin, Qiang Liu and David Z. Pan, "Mixed Precision Neural Architecture Search for Energy Efficient Deep Learning," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4-7, 2019

[C33] Kaveh Shamsi, David Z. Pan and Yier Jin, "IcySAT: Improved SAT-based Attacks on Cyclic Locked Circuits," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4-7, 2019

[C34] Shounak Dhar, Love Singhal, Mahesh A. Iyer and David Z. Pan, "FPGA Accelerated Spreading for Global Placement," 23rd *IEEE High Performance Extreme Computing Conference (HPEC)*, Boston, September 24-26, 2019

[C35] Shounak Dhar, Love Singhal, Mahesh A. Iyer and D. Z. Pan, "*FPGA Accelerated FPGA Placement*," 29th International Conference on Field Programmable Logic and Applications (FPL), Barcelona, Spain, September 9-11, 2019

[C36] Yibo Lin, Shounak Dhar, Wuxi Li, Haoxing Ren, Brucek Khailany and David Z. Pan, "DREAMPlace: Deep Learning Toolkit Enabled GPU Acceleration for Modern VLSI Placement," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019. **(Best Paper Award)**

[C37] Wei Ye, Mohamed Baker Alawieh, Yibo Lin, and David Z. Pan, "LithoGAN: End-to-End Lithography Modeling with Generative Adversarial Networks," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019. **(Best Paper Award Candidate)**

[C38] Biying Xu, Yibo Lin, Xiyuan Tang, Shaolan Li, Linxiao Shen, Nan Sun and David Z. Pan, "WellGAN: Generative-Adversarial-Network-Guided Well Generation for Analog/Mixed-Signal Circuit Layout," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019.

[C39] Mohamed Baker Alawieh, Yibo Lin, Zaiwei Zhang, Meng Li, Qixing Huang and David Z. Pan, "GAN-SRAF: Sub-Resolution Assist Feature Generation using Conditional Generative Adversarial Networks," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019.

[C40] Mohamed Baker Alawieh, Sinead Williamson and David Z. Pan, "Rethinking Sparsity in Performance Modeling for Analog and Mixed Circuits using Spike and Slab Models," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019.

[C41] Kaveh Shamsi, David Z. Pan and Yier Jin, "On the Impossibility of Approximation-Resilient Circuit Locking," *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, Tysons Corner, USA, May 6-10, 2019

[C42] Shaolan Li, Wenda Zhao, Biying Xu, Xiangxing Yang, Xiyuan Tang, Linxiao Shen, Nanshu Lu, David Z. Pan and Nan Sun, "A 0.025mm^2 0.8V 78.5dB SNDR VCO-based Sensor Readout Circuit Using a Hybrid PLL-$\Delta\Sigma$ Structure," *IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, Apr. 14-17, 2019.

[C43] Shaolan Li, Biying Xu, David Z. Pan and Nan Sun, "A 60-fJ/step 11-ENOB VCO-based CTDSM Synthesized from Digital Standard Cell Library," *IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, Apr. 14-17, 2019

[C44] Biying Xu, Shaolan Li, Chak-Wa Pui, Derong Liu, Linxiao Shen, Yibo Lin, Nan Sun, and David Z. Pan, "Device Layer-Aware Analytical Placement for Analog Circuits," *ACM International Symposium on Physical Design (ISPD),* San Francisco, CA, April 14-17, 2019. **(Best Paper Award Nomination)**

[C45] Kaveh Shamsi, Meng Li, David Z. Pan and Yier Jin, "KC2: Key-Condition Crunching for Fast Sequential Circuit Deobfuscation," *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Florence, Italy, March 25-29, 2019. **(Best Paper Award Candidate)**

[C46] Wei Ye, Mohamed Baker Alawieh, Meng Li, Yibo Lin, and David Z. Pan, "Litho-GPA: Gaussian Process Assurance for Lithography Hotspot Detection," *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Florence, Italy, March 25-29, 2019.

[C47] Zheng Zhao, Derong Liu, Zhoufeng Ying, Biying Xu, Chenghao Feng, Ray T. Chen. and David Z. Pan, "Exploiting Wavelength Division Multiplexing for Optical Logic Synthesis," *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Florence, Italy, March 25-29, 2019.

[C48] Zhoufeng Ying, Zheng Zhao, Chenghao Feng, Rohan Mital, Shounak Dhar, David Z. Pan, Ray T. Chen, "Automated logic synthesis for electro-optic computing in integrated photonics," *SPIE OPTO Proceedings Volume 10924, Optical Interconnects XIX*; 109240H (March 2019) https://doi.org/10.1117/12.2510363

[C49] Wuxi Li, Mehrdad Eslami Dehkordi, Stephen Yang and David Z. Pan, "Simultaneous Placement and Clock Tree Construction for Modern FPGAs," *ACM International Symposium on Field-Programmable Gate Arrays (FPGA)*, Seaside, CA, February 24 - 26, 2019.

[C50] Wei Ye, Yibo Lin, Meng Li, Qiang Liu, and David Z. Pan, "LithoROC: lithography hotspot detection with explicit ROC optimization," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Jan. 21–24, 2019 **(Invited Paper)**

[C51] Shounak Dhar, Love Singhal, Mahesh A. Iyer and David Z. Pan, "A Shape-Driven Spreading Algorithm Using Linear Programming for Global Placement," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Jan. 21–24, 2019.

[C52] Wei Ye, Mohamed Baker Alawieh, Yibo Lin, and David Z. Pan, "Tackling Signal Electromigration with Learning-Based Detection and Multistage Mitigation," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Jan. 21–24, 2019.

[C53] Ying Chen, Yibo Lin, Tianyang Gai, Yajuan Su, Yayi Wei, and David Z. Pan, "Semi-Supervised Hotspot Detection with Self-Paced Multi-Task Learning," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Jan. 21–24, 2019.

[C54] Mohamed Baker Alawieh, Xiyuan Tang and David Z. Pan, "S^2-PM: Semi-Supervised Learning for Efficient Performance Modeling of Analog and Mixed Signal Circuits," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Jan. 21–24, 2019.

[C55] Zheng Zhao, Derong Liu, Meng Li, Zhoufeng Ying, Biying Xu, Lu Zhang, Bei Yu, Ray T. Chen, and David Z. Pan, "Hardware-software Co-design of Slimmed Optical Neural Networks," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Jan. 21–24, 2019.

[C56] Yibo Lin, Mohamed Baker Alawieh, Wei Ye, and David Z. Pan, "Machine Learning for Yield Learning and Optimization," *IEEE International Test Conference (ITC)*, Oct. 2018 **(Invited Paper)**

[C57] Meng Li, Kaveh Shamsi, Yier Jin, and David Z. Pan, "TimingSAT: Decamouflaging Timing-based Logic Obfuscation," *IEEE International Test Conference (ITC)*, Oct. 2018

[C58] Shounak Dhar and David Z. Pan, "GDP: GPU accelerated Detailed Placement," *IEEE High Performance Extreme Computing Conference (HPEC)*, Boston, Sept. 25-27, 2018

[C59] Derong Liu, Zheng Zhao, Zheng Wang, Zhoufeng Ying, Ray T. Chen, and David Z. Pan, "OPERON: Optical-electrical Power-efficient Route Synthesis for On-chip Signals," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, June 24-28, 2018

[C60] Kaveh Shamsi, Meng Li, David Z. Pan, and Yier Jin, "Cross-Lock: Dense Layout-Level Interconnect Locking using Cross-bar Architectures," *ACM Great Lakes Symposium on VLSI* (*GLSVLSI*), Chicago, Illinois, May 23-25, 2018. **(Best Paper Award)**

[C61] Biying Xu, Bulent Basaran, Ming Su, and David Z. Pan, "Analog Placement Constraint Extraction and Exploration with the Application to Layout Retargeting," *ACM International Symposium on Physical Design (ISPD),* Monterey, CA, Mar. 25-28, 2018.

[C62] Wei Ye, Meng Li, Kai Zhong, Bei Yu, and David Z. Pan, "Power Grid Reduction by Sparse Convex Optimization," *ACM International Symposium on Physical Design (ISPD),* Monterey, CA, Mar. 25-28, 2018.

[C63] Yibo Lin, Yuki Watanabe, Taiki Kimura, Tetsuaki Matsunawa, Shigeki Nojima, Meng Li, and David Z. Pan, "Data Efficient Lithography Modeling with Residual Neural Networks and Transfer Learning," *ACM International Symposium on Physical Design (ISPD),* Monterey, CA, Mar. 25-28, 2018.

[C64] Meng Li, Bei Yu, Yibo Lin, Xiaoqing Xu, Wuxi Li, and David Z. Pan, "A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jeju Island, Korea, Jan. 22-25, 2018.

[C65] Zheng Zhao, Zheng Wang, Zhoufeng Ying, Shounak Dhar, Ray T. Chen, and David Z. Pan, "Logic Synthesis for Energy-Efficient Photonic Integrated Circuits," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Jeju Island, Korea, Jan. 22-25, 2018.

[C66] Che-Lun Hsu, Shaofeng Guo, Yibo Lin, Xiaoqing Xu, Meng Li, Runsheng Wang, Ru Huang, and David Z. Pan, "Layout-Dependent Aging Mitigation for Critical Path Timing," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Jeju Island, Jan. 22-25, 2018.

[C67] Wuxi Li, Meng Li, Jiajun Wang, and David Z. Pan, "UTPlaceF 3.0: A Parallelization Framework for Modern FPGA Global Placement," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Irvine, CA, Nov. 13-16, 2017. **(Invited Paper)**

[C68] Jiaojiao Ou, Xiaoqing Xu, Brian Cline, Greg Yeric, and David Z. Pan, "DTCO for DSA-MP Hybrid Lithography with Double-BCP Materials in Sub-7nm Node," *IEEE International Conference on Computer Design (ICCD)*, Boston, MA, Nov. 5-8, 2017.

[C69] Yibo Lin, Peter Debacker, Darko Trivkovic, Ryoung-han Kim, Praveen Raghavan, and David Z. Pan, "Patterning Aware Design Optimization of Selective Etching in N5 and Beyond," *IEEE International Conference on Computer Design (ICCD)*, Boston, MA, Nov. 5-8, 2017.

[C70] Zheng Zhao, Zheng Wang, Zhoufeng Ying, Shounak Dhar, Ray T. Chen, and David Z. Pan, "Optical Computing on Silicon-on-Insulator-Based Photonic Integrated Circuits," *IEEE International Conference on ASIC (ASICON)*, Guiyang, China, Oct. 25-28, 2017. **(Invited Paper)**

[C71] Zheng Wang, Zhoufeng Ying, Shounak Dhar, Zheng Zhao, David Pan, and Ray T. Chen, "Nanophotonic devices for power-efficient computing and optical interconnects," *In IEEE Photonics Society Summer Topical Meeting Series (SUM), pp. 7-8,* July 2017. **(Invited Paper)**

[C72] Wei Ye, Yibo Lin, Xiaoqing Xu, Wuxi Li, Yiwei Fu, Yongsheng Sun, Canhui Zhan, and David Z. Pan, "Placement Mitigation Techniques for Power Grid Electromigration," *IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, Taipei, July 24-26, 2017.

[C73] Meng Li, Liangzhen Lai, Vikas Chandra, and David Z. Pan, "Cross-level Monte Carlo Framework for System Vulnerability Evaluation against Fault Attack," *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, June 18-22, 2017.

[C74] Biying Xu, Shaolan Li, Nan Sun, and David Z. Pan, "A Scaling Compatible, Synthesis Friendly VCO-based Delta-sigma ADC Design and Synthesis Methodology," *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, June 18-22, 2017.

[C75] Xiaoqing Xu, Yibo Lin, Vinicius Livramento, and David Z. Pan, "Concurrent Pin Access Optimization for Unidirectional Routing," *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, Jun. 18-22, 2017.

[C76] Derong Liu, Vinicius Livramento, Salim Chowdhury, Duo Ding, Huy Vo, Akshay Sharma, and David Z. Pan, "Streak: Synergistic Topology Generation and Route Synthesis for On-Chip

Performance-Critical Signal Groups," *ACM/IEEE Design Automation Conference (DAC),* Austin, TX, June 18-22, 2017.

[C77] Travis Meade, Zheng Zhao, Shaojie Zhang, David Z. Pan, and Yier Jin**, "**Revisit Sequential Logic Obfuscation: Attacks and Defenses," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, MD, USA, May 28-31, 2017 **(Invited Paper)**

[C78] Zheng Wang, Zhoufeng Ying, Shounak Dhar, Zheng Zhao, David Z. Pan, and Ray T. Chen, "Optical Switches Based Carry-Ripple Adder for Future High-Speed and Low-Power Consumption Optical Computing," *In CLEO: Science and Innovations, pp. STh1N-2. Optical Society of America*, May 2017.

[C79] Zhoufeng Ying, Zheng Wang, Shounak Dhar, Zheng Zhao, David Z. Pan, and Ray T. Chen, "On-chip Microring Resonator Based Electro-optic Full Adder for Optical Computing," *In CLEO: QELS_Fundamental Science, pp. JW2A-147. Optical Society of America*, May 2017.

[C80] Kaveh Shamsi, Meng Li, Travis Meade, Zheng Zhao, David Z. Pan and Yier Jin, "Cyclic Obfuscation for Creating SAT-Unresolvable Circuits," *ACM Great Lakes Symposium on VLSI* (*GLSVLSI*), Banff, Alberta, Canada, May 10-12, 2017.

[C81] Kaveh Shamsi, Meng Li, Travis Meade, Zheng Zhao, David Z. Pan, and Yier Jin, "AppSAT: Approximately Deobfuscating Integrated Circuits," *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, McLean, VA, USA, May 1-4, 2017 **(Best Paper Award)**

[C82] Jiaojiao Ou, Bei Yu, Xiaoqing Xu, Joydeep Mitra, Yibo Lin and David Z. Pan. "DSAR: DSA aware Routing with Simultaneous DSA Guiding Pattern and Double Patterning Assignment," *ACM International Symposium on Physical Design (ISPD),* Portland, OR, Mar. 19-22, 2017.

[C83] Biying Xu, Shaolan Li, Xiaoqing Xu, Nan Sun and David Z. Pan, "Hierarchical and Analytical Placement Techniques for High-Performance Analog Circuits," *ACM International Symposium on Physical Design (ISPD),* Portland, OR, Mar. 19-22, 2017.

[C84] Shounak Dhar, Mahesh Iyer, Saurabh Adya, Love Singhal, Nikolay Rubanov and David Pan, "An Effective Timing-Driven Detailed Placement Algorithm for FPGAs," *ACM International Symposium on Physical Design (ISPD)*, Portland, OR, Mar. 19-22, 2017.

[C85] Joydeep Mitra, Andres Torres, and David Z. Pan, "Process, Design Rule, and Layout Co-optimization for DSA Based Patterning of Sub-10nm Finfet Devices," *SPIE Intl. Symp. Advanced Lithography Conference*, San Jose, CA, Feb. 26 - Mar. 2, 2017

[C86] Joydeep Mitra, Andres Torres, and David Z. Pan, "Model Based Guiding Pattern Synthesis for On-target and Robust Assembly of Via and Contact layers using DSA," *SPIE Intl. Symp. Advanced Lithography Conference*, San Jose, CA, Feb. 26 - Mar. 2, 2017.

[C87] Taiki Kimura, Tetsuaki Matsunawa, Chikaaki Kodama, Shigeki Nojima and David Z. Pan, "SOCS-based post-layout optimization for multiple patterns with light interference prediction," *SPIE Intl. Symp. Advanced Lithography Conference*, San Jose, CA, Feb. 26 - Mar. 2, 2017.

[C88] Jiaojiao Ou, Brian Cline, Greg Yeric and David Z. Pan. "Efficient DSA and DP Hybrid Lithography Conflict Detection and Guiding Template Assignment", *SPIE Intl. Symp. Advanced Lithography Conference*, San Jose, CA, Feb. 26 - Mar. 2, 2017.

[C89] Wuxi Li, Shounak Dhah, and David Z. Pan, "UTPlaceF: A Routability-Driven FPGA Placer with Physical and Congestion Aware Packing," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, Nov. 7-10, 2016 (**Invited Paper; 1st Place Winner of ISPD'16 Contest**)

[C90] Yibo Lin, Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, Natarajan Viswanathan, Wen-Hao Liu, Zhuo Li, Charles J. Alpert and David Z. Pan, "MrDP: Multiple-row Detailed Placement of Heterogeneous-sized Cells for Advanced Nodes," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, Nov. 7-10, 2016

[C91] Meng Li, Kaveh Shamsi, Travis Meade, Zheng Zhao, Bei Yu, Yier Jin and David Z. Pan, "Provably Secure Camouflaging Strategy for IC Protection," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, Nov. 7-10, 2016

[C92] Shounak Dhar, Saurabh Adya, Love Singhal, Mahesh A. Iyer and David Z. Pan, "Detailed Placement for Modern FPGAs using 2D Dynamic Programming," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, Nov. 7-10, 2016

[C93] Yudong Tao, Changhao Yan, Yibo Lin, Shengguo Wang, David Z. Pan, and Xuan Zeng, "A Novel Unified Dummy Fill Insertion Framework with SQP-Based Optimization Method," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, Nov. 7-10, 2016

[C94] Travis Meade, Shaojie Zhang, Zheng Zhao, David Z. Pan, and Yier Jin, "Gate-Level Netlist Reverse Engineering Tool Set for Functionality Recovery and Malicious Logic Detection," *International Symposium for Testing and Failure Analysis (ISTFA)*, Fort Worth, Texas, USA, Nov. 6-10, 2016

[C95] Yibo Lin, Bei Yu, and David Z. Pan, "Detailed Placement in Advanced Technology Nodes: A Survey," *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Hangzhou, China, October 25-28, 2016. **(Invited Paper)**

[C96] Derong Liu, Bei Yu, Salim Chowdhury, and David Z. Pan, "Incremental Layer Assignment for Critical Path Timing," *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, June 5-9, 2016

[C97] Meng Li, Jin Miao, Kai Zhong, and David Z. Pan, "Practical Public PUF Enabled by Solving Max-Flow Problem on Chip," *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, June 5-9, 2016

[C98] Jiaojiao Ou, Bei Yu and David Z. Pan, "Concurrent Guiding Template Assignment and Redundant Via Insertion for DSA-MP Hybrid Lithography," *Proceedings ACM International Symposium on Physical Design (ISPD)*, Santa Rosa, CA, April 3-6, 2016

[C99] Xiaoqing Xu, Tetsuaki Matsunawa, Shigeki Nojima, Chikaaki Kodama, Toshiya Kotani and David Pan, "A Machine Learning Based Framework for Sub-Resolution Assist Feature Generation," *Proceedings ACM International Symposium on Physical Design (ISPD)*, Santa Rosa, CA, April 3-6, 2016

[C100] Yibo Lin, Xiaoqing Xu, Bei Yu, Ross Baldick, and David Z. Pan, "Triple/Quadruple Patterning Layout Decomposition via Novel Linear Programming and Iterative Rounding," *Proc. SPIE 9781, Design-Process-Technology Co-optimization for Manufacturability X*, San Jose, CA, Feb. 21-25, 2016 **(Franco Cerrina Memorial Best Student Paper Award)**

[C101] Xiaoqing Xu, Brian Cline, Greg Yeric, and David Z. Pan, "Standard Cell Pin Access and Physical Design in Advanced Lithography," *SPIE Advanced Lithography Conference*, San Jose, CA, Feb. 21-25, 2016 **(Invited Paper)**

[C102] Taiki Kimura, Tetsuaki Matsunawa, Shigeki Nojima, and David Z. Pan, "Hybrid Hotspot Detection using Regression Model and SOCS Kernels," *Proc. SPIE 9781, Design-Process-Technology Co-optimization for Manufacturability X*, San Jose, CA, Feb. 21-25, 2016

[C103] Tetsuaki Matsunawa, Bei Yu, and David Z. Pan, "Laplacian Eigenmaps and Bayesian Clustering Based Layout Pattern Sampling and Its Applications to Hotspot Detection and OPC," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Macau, Jan. 25-28, 2016.

[C104] Yibo Lin, Bei Yu, Yi Zou, Zhuo Li, Charles J. Alpert, and David Z. Pan, "Stitch Aware Detailed Placement for Multiple E-Beam Lithography," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Macau, Jan. 25-28, 2016.

[C105] Pengpeng Ren, Xiaoqing Xu, Peng Hao, Junyao Wang, Runsheng Wang, Ming Li, Jianping Wang, Weihai Bu, Jingang Wu, Walsum Wong, Shaofeng Yu, Hanming Wu, Shiuh-Wuu Lee, David Z. Pan, and Ru Huang, "Adding the Missing Time-Dependent Layout Dependency into Device-Circuit-Layout Co-Optimization -- New Findings on the Layout Dependent Aging Effects," *IEEE International Electron Devices Meeting (IEDM)*, Washington DC, Dec. 7-9, 2015

[C106] Andrew B. Kahng, Mulong Luo, Gi-Joon Nam, Siddhartha Nath, David Z. Pan, and Gabriel Robins, "Toward Metrics of Design Automation Research Impact," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, November 2-6, 2015. (**Invited Paper**)

[C107] Bei Yu, Derong Liu, Salim Chowdhury, and David Z. Pan, "TILA: Timing-Driven Incremental Layer Assignment," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, November 2-6, 2015.

[C108] Yibo Lin, Bei Yu, Biying Xu, and David Z. Pan, "Triple Patterning Aware Detailed Placement Toward Zero Cross-Row Middle-of-Line Conflict," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, November 2-6, 2015.

[C109] Chen-Hsuan Lin, Subhendu Roy, Chun-Yao Wang, David Z. Pan, and Deming Chen, "CSL: Coordinated and Scalable Logic Synthesis Techniques for Effective NBTI Reduction," *IEEE International Conference on Computer Design (ICCD)*, Oct. 18-21, 2015

[C110] David Z. Pan, Lars Liebmann, Bei Yu, Xiaoqing Xu, Yibo Lin, "Pushing Multiple Patterning in Sub-10nm: Are We Ready?" *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, June 7-11, 2015 (**Invited Paper**)

[C111] Xiaoqing Xu, Bei Yu, Jhih-Rong Gao, Che-Lun Hsu, and David Z. Pan, "PARR: Pin Access Planning and Regular Routing for Self-Aligned Double Patterning," *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, June 7-11, 2015

[C112] Yibo Lin, Bei Yu, and David Z. Pan, "High Performance Dummy Fill Insertion with Coupling and Uniformity Constraints," *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, June 7-11, 2015

[C113] Subhendu Roy, Derong Liu, Junhyung Um, and David Z. Pan, "OSFA: A New Paradigm of Gate Sizing for Power/Performance Optimizations under Multiple Operating Conditions," *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, June 7-11, 2015

[C114] Keith Campbell, Pranay Vissa, David Z. Pan, and Deming Chen, "High-Level Synthesis of Error Detecting Cores through Low-Cost Modulo-3 Shadow Datapaths," *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, June 7-11, 2015

[C115] Wei Ye, Bei Yu, Yong-Chan Ban, Lars Liebmann, and David Z. Pan, "Standard Cell Layout Regularity and Pin Access Optimization Considering Middle-of-Line," *ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Pittsburgh, PA, May 20-22, 2015

[C116] Jiaojiao Ou, Bei Yu, Jhih-Rong Gao, Moshe Preil, Azat Latypov, and David Z Pan, "Directed Self-Assembly Based Cut Mask Optimization for Unidirectional Design," *ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Pittsburgh, PA, May 20-22, 2015

[C117] Subhendu Roy, Pavlos M Mattheakis, Peter S Colyer, Laurent Masse-Navette, Pierre-Olivier Ribet, and David Z Pan, "Skew Bounded Buffer Tree Resynthesis for Clock Power Optimization," *ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Pittsburgh, PA, May 20-22, 2015

[C118] Xiaoqing Xu, Brian Cline, Greg Yeric, Bei Yu, and David Z. Pan, "A Systematic Framework for Evaluating Standard Cell Middle-of-Line (MOL) Robustness for Multiple Patterning," *SPIE Intl. Symp. Advanced Lithography - Design-Process-Technology Co-optimization for Manufacturability IX*, San Jose, CA, Feb. 23-27, 2015

[C119] Tetsuaki Matsunawa, Jhih-Rong Gao, Bei Yu, and David Z. Pan, "A New Lithography Hotspot Detection Framework Based on AdaBoost Classifier and Simplified Feature Extraction," *SPIE Intl. Symp. Advanced Lithography - Design-Process-Technology Co-optimization for Manufacturability IX*, San Jose, CA, Feb. 23-27, 2015

[C120] Tetsuaki Matsunawa, Bei Yu, and David Z. Pan, "Optical proximity correction with hierarchical Bayes model," *SPIE Intl. Symp. Advanced Lithography - Optical Microlithography XXVIII*, San Jose, CA, Feb. 23-27, 2015

[C121] Bei Yu, David Z. Pan, Tetsuaki Matsunawa, and Xuan Zeng, "Machine Learning and Pattern Matching in Physical Design," *Proceedings IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Japan, Jan. 19-22, 2015 **(Invited Paper)**

[C122] Jiwoo Pak, Bei Yu, and David Z. Pan, "Electromigration-aware Redundant Via Insertion," *Proceedings IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Japan, Jan. 19-22, 2015

[C123] Subhendu Roy, Mihir Choudhury, Ruchir Puri, and David Z. Pan, "Polynomial Time Algorithm for Area and Power Efficient Adder Synthesis in High-Performance Designs," *Proceedings IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Japan, Jan. 19-22, 2015

[C124] Subhendu Roy, Pavlos Matthaiakis, Pavlos, Laurent Masse-Navette, and David Z. Pan, "Evolving Challenges and Techniques for Nanometer SoC Clock Network Synthesis," *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Guilin, China, October 28-31, 2014. **(Invited Paper)**

[C125] Bei Yu, Gilda Garreton, and David Z. Pan, "Layout Compliance for Triple Patterning Lithography: an Iterative Approach," *SPIE/BACUS Photomask Symposium*, Monterey, CA, September 2014. **(Invited Paper)**

[C126] Jhih-Rong Gao, Xiaoqing Xu, Bei Yu, and David Z. Pan, "MOSAIC: Mask Optimizing Solution With Process Window Aware Inverse Correction," *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, June 1-5, 2014 **(Best Paper Award Nomination)**

[C127] Bei Yu and David Z. Pan, "Layout Decomposition for Quadruple Patterning Lithography and Beyond," *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, June 1-5, 2014
[C128] Moongon Jung, David Z. Pan, and Sung Kyu Lim, "Through-Silicon-Via Material Property Variation Impact on Full-Chip Reliability and Timing," *IEEE International Interconnect Technology Conference (IITC)*, San Jose, CA, May 20-23, 2014
[C129] Xiaoqing Xu, Brian Cline, Greg Yeric, Bei Yu and David Z. Pan, "Self-Aligned Double Patterning Aware Pin Access and Standard Cell Layout Co-Optimization," *Proceedings ACM International Symposium on Physical Design (ISPD)*, Petaluma, CA, March 2014
[C130] Yilin Zhang and David Z. Pan, "Timing-Driven, Over-the-Block Rectilinear Steiner Tree Construction with Pre-Buffering and Slew Constraints," *Proceedings ACM International Symposium on Physical Design (ISPD)*, Petaluma, CA, March 2014
[C131] Subhendu Roy, Pavlos M. Mattheakis, Laurent Masse-Navette, and David. Z. Pan, "Clock Tree Resynthesis for Multi-corner Multi-mode Timing Closure," *Proceedings ACM International Symposium on Physical Design (ISPD)*, Petaluma, CA, March 2014 **(Best Paper Award)**
[C132] Bei Yu, Jhih-Rong Gao, Xiaoqing Xu, and David Z. Pan, "Bridging the Gap from Mask to Physical Design for Multiple Patterning Lithography," *SPIE Intl. Symp. Advanced Lithography - Design-Process-Technology Co-optimization for Manufacturability VIII*, San Jose, CA, Feb. 23-27, 2014 **(Invited Paper)**
[C133] Jhih-Rong Gao, Bei Yu, and David Z. Pan, "Accurate Lithography Hotspot Detection Based on PCA-SVM Classifier with Hierarchical Data Clustering," *SPIE Intl. Symp. Advanced Lithography - Design-Process-Technology Co-optimization for Manufacturability VIII*, San Jose, CA, Feb. 23-27, 2014
[C134] Jhih-Rong Gao, Bei Yu, David Z. Pan, "Self-aligned Double Patterning Layout Decomposition with Complementary E-Beam Lithography," *Proceedings IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Singapore, Jan. 20-23, 2014
[C135] Yilin Zhang, Salim Chowdhury, David Z. Pan, "BOB-Router: A New Buffering-Aware Global Router with Over-the-Block Routing Resources Optimization," *Proceedings IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Singapore, Jan. 20-23, 2014
[C136] Subhendu Roy and David Z. Pan, "Reliability Aware Gate Sizing Combating NBTI and Oxide Breakdown," *Proc. IEEE 27th International Conference on VLSI Design*, Mumbai, India, Jan. 7-9, 2014
[C137] Jiwoo Pak, Sung Kyu Lim and David Z. Pan, "Electromigration Study for Multi-scale Power/Ground Vias in TSV-based 3D ICs," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 18-21, 2013.
[C138] Bei Yu, Xiaoqing Xu, Jhih-Rong Gao and David Z. Pan, "Methodology for Standard Cell Compliance and Detailed Placement for Triple Patterning Lithography," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 18-21, 2013. **(William J. MacCalla Best Paper Award)**
[C139] Bei Yu, Yen-Hung Lin, Gerard Luk-Pat, Duo Ding, Kevin Lucas and David Z. Pan, "A High-Performance Triple Patterning Layout Decomposer with Balanced Density," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 18-21, 2013.
[C140] Samuel I. Ward, Natarajan Viswanathan, Nancy Y. Zhou, Cliff C. N. Sze, Zhuo Li, Charles J. Alpert and David Z. Pan, "Clock Power Minimization using Structured Latch Templates and Decision Tree Induction," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 18-21, 2013
[C141] Jhih-Rong Gao, Bei Yu, Duo Ding, and David Z. Pan, "Lithography Hotspot Detection and Mitigation in Nanometer VLSI," *Proc. The IEEE 10th International Conference on ASIC (ASICON)*, Shenzhen, China, Oct. 28-31, 2013 **(Invited Paper)**
[C142] Subhendu Roy, Mihir Choudhury, Ruchir Puri, and David Z. Pan, "Towards Optimal Performance-Area Trade-off in Adders by Synthesis of Parallel Prefix Structures," *ACM/IEEE Design Automation Conference (DAC),* Austin, TX, June 2-6, 2013.
[C143] Yang Li and David Z. Pan, "An Accurate Semi-Analytical Framework for Full-Chip TSV-induced Stress Modeling," *ACM/IEEE Design Automation Conference (DAC),* Austin, TX, June 2-6, 2013.

[C144] Bei Yu, Kun Yuan, Jhih-Rong Gao, and David Z. Pan, "E-BLOW: E-Beam Lithography Overlapping aware Stencil Planning for MCC System," *ACM/IEEE Design Automation Conference (DAC),* Austin, TX, June 2-6, 2013.

[C145] Bei Yu, Jhih-Rong Gao, and David Z. Pan, "Triple-patterning Lithography (TPL) Layout Decomposition using End Cutting," *SPIE Intl. Symp. Advanced Lithography*, San Jose, CA, Feb. 24-28, 2013.

[C146] Jhih-Rong Gao, Harshdeep Jawandha, Prasad Atkarc, Atul Walimbe, Bikram Baidya, and David Z. Pan, "Self-aligned Double Patterning Compliant Routing with In-design Physical Verification Flow," *SPIE Intl. Symp. Advanced Lithography*, San Jose, CA, Feb. 24-28, 2013.

[C147] Jhih-Rong Gao, Bei Yu, Ru Huang, and David Z. Pan, "Self-aligned Double Patterning Friendly Configuration for Standard Cell Library Considering Placement," *SPIE Intl. Symp. Advanced Lithography*, San Jose, CA, Feb. 24-28, 2013.

[C148] Bei Yu, Jhih-Rong Gao, and David Z. Pan, "L-Shape based Layout Fracturing for E-Beam Lithography," *Proceedings Asian and South Pacific Design Automation Conference (ASP-DAC)*, Yokohama, Japan, January 22- 25, 2013. **(Best Paper Award Nomination)**

[C149] Bei Yu, Jhih-Rong Gao, Duo Ding, Yongchan Ban, Jae-seok Yang, Kun Yuan, Minsik Cho, and David Z. Pan, "Dealing with IC Manufacturability in Extreme Scaling," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 5-8, 2012. (**Embedded Tutorial Paper**)

[C150] Jiwoo Pak, Sung Kyu Lim, and David Z. Pan, "Electromigration-aware Routing for 3D ICs with Stress-aware EM Modeling," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 5-8, 2012.

[C151] Yen-Hung Lin, Bei Yu, David Z. Pan and Yih-Lang Li, "TRIAD: A Triple Patterning Lithography Aware Detailed Router," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 5-8, 2012.

[C152] Yilin Zhang, Ashutosh Chakraborty, Salim Chowdhury, and David Z. Pan, "Reclaiming Over-the-IP-Block Routing Resources With Buffering-Aware Rectilinear Steiner Minimum Tree Construction," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 5-8, 2012.

[C153] Samuel I. Ward, Duo Ding, and David Z. Pan, "PADE: A High-Performance Placer with Automatic Datapath Extraction and Evaluation through High Dimensional Data Learning," *ACM/IEEE Design Automation Conference (DAC)*, pp. 756-761, San Francisco, CA, June 3-6, 2012. Available at: http://dx.doi.org/10.1145/2228360.2228497

[C154] Moongon Jung, David Z. Pan, and Sung Kyu Lim, "Chip/Package Co-Analysis of Thermo-Mechanical Stress and Reliability in TSV-based 3D ICs," *ACM/IEEE Design Automation Conference (DAC)*, pp. 317-326, San Francisco, CA, June 3-6, 2012. **(Nominated for Best Paper Award)** Available at: http://dx.doi.org/10.1145/2228360.2228419

[C155] David Z. Pan, Jhih-Rong Gao, and Bei Yu, "VLSI CAD for Emerging Nanolithography," *IEEE VLSI Design, Automation and Test (VLSI-DAT),* Hsinchu, Taiwan, April 2012. **(Invited Paper)**

[C156] Samuel I. Ward, Myung-Chul Kim, Natarajan Viswanathan, Zhuo Li, Charles Alpert, Earl Swartzlander, and David Z. Pan, "Keep it Straight: Teaching Placement How to Better Handle Designs with Datapaths," *Proceedings ACM International Symposium on Physical Design (ISPD)*, pp. 79-86, Napa Valley, CA, March 25-28, 2012. **(Best Paper Award Candidate)** Available at**:** http://dx.doi.org/10.1145/2160916.2160935

[C157] Jhih-Rong Gao and David Z. Pan, "Flexible Self-aligned Double Patterning Aware Detailed Routing with Prescribed Layout Planning," *Proceedings ACM International Symposium on Physical Design (ISPD)*, pp. 25-32, Napa Valley, CA, March 25-28, 2012. Available at**:** http://dx.doi.org/10.1145/2160916.2160923

[C158] Kevin Lucas, Gerry Luk-Pat, Ben Painter, Chris Cork, Bei Yu, and David Z. Pan, "Implications of Triple Patterning for 14 nm Node Design and Patterning," *SPIE Advanced Lithography Symposium Design for Manufacturability Conference*, vol. 8327, pp. 832703, San Jose, CA, February 12-16, 2012. (**Keynote Presentation and Invited Paper)** Available at: http://dx.doi.org/10.1117/12.920028

[C159] Vijay J. Reddi, David Z. Pan, Sani R. Nassif, and Keith A. Bowman, "Robust and Resilient Designs from the Bottom-Up: Technology, CAD, Circuit, and System Issues," *Proceedings Asian*

and South Pacific Design Automation Conference (ASP-DAC), pp. 7-16, Sydney, Australia, January 30-February 3, 2012. **(Invited Paper)** Available at: http://dx.doi.org/10.1109/ASP-DAC.2012.6165064

[C160] David Z. Pan, Sung Kyu Lim, Krit Athikulwongse, Moongon Jung, Joydeep Mitra, Jiwoo Pak, Mohit Pathak, and Jae-seok Yang, "Design for Manufacturability and Reliability for TSV-based 3D ICs," *Proceedings Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 750-755, Sydney, Australia, January 30-February 3, 2012. **(Invited Paper)** Available at: http://dx.doi.org/10.1109/ASP-DAC.2012.6165055

[C161] Duo Ding, Bei Yu, Joydeep Ghosh, and David Z. Pan, "EPIC: Efficient Prediction of IC Manufacturing Hotspots with a Unified Meta-Classification Formulation," *Proceedings Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 263-270, Sydney, Australia, January 30-February 3, 2012. **(Best Paper Award)** Available at: http://dx.doi.org/10.1109/ASP-DAC.2012.6164956

[C162] Duo Ding, Bei Yu, and David Z. Pan, "GLOW: A Global Router for Low-Power Thermal-reliable Interconnect Synthesis using Photonic Wavelength Multiplexing," *Proceedings Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 621-626, Sydney, Australia, January 30-February 3, 2012. Available at: http://dx.doi.org/10.1109/ASP-DAC.2012.6165031

[C163] Duo Ding and David Z. Pan, "Low-power Integration of On-chip Nanophotonic Interconnect for High-performance Optoelectrical IC," *Proceedings SPIE Optoelectronic Integrated Circuits XIV*, vol. 8267, pp. 82670Z, San Francisco, CA, January 25-26, 2012. **(Invited Paper)** Available at: http://dx.doi.org/10.1117/12.913886

[C164] Ryan A. Integlia, Lianghong Yin, Duo Ding, David Z. Pan, Douglas M. Gill, and Wei Jiang, "Parallel-Coupled Dual Racetrack Silicon Micro-Resonators for Quadrature Amplitude Modulation," *Proceedings SPIE Silicon Photonics VII*, vol. 19, no. 16, pp. 14892-14902, San Francisco, CA, January 22-25, 2012. Available at: http://dx.doi.org/10.1364/OE.19.014892

[C165] Bei Yu, Kun Yuan, Boyang Zhang, Duo Ding, and David Z. Pan, "Layout Decomposition for Triple Patterning Lithography," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 1-8, San Jose, CA, November 7-11, 2011. **(Best Paper Award Candidate)** Available at: http://dx.doi.org/10.1109/ICCAD.2011.6105297

[C166] Yen-Hung Lin, Yong-Chan Ban, David Z. Pan, and Yih-Lang Li, "Doppler: DPL-Aware and OPC-Friendly Gridless Detailed Routing with Mask Density Balancing," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 283-289, San Jose, CA, November 7-11, 2011. Available at: http://dx.doi.org/10.1109/ICCAD.2011.6105343

[C167] Moongon Jung, Xi Liu, Suresh Sitaraman, David Z. Pan, and Sung Kyu Lim, "Full-Chip Through-Silicon-Via Interfacial Crack Analysis and Optimization for 3D IC," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 563-570, San Jose, CA, November 7-11, 2011. Available at: http://dx.doi.org/10.1109/ICCAD.2011.6105386

[C168] Mohit Pathak, Jiwoo Pak, David Z. Pan, and Sung Kyu Lim, "Electromigration Modeling and Full-Chip Reliability Analysis for BEOL Interconnect in TSV-based 3D ICs," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 555-562, San Jose, CA, November 7-11, 2011. Available at: http://dx.doi.org/10.1109/ICCAD.2011.6105385

[C169] Wooyoung Jang, Ou He, Jae-Seok Yang, and David Z. Pan, "Chemical-Mechanical Polishing Aware Application-Specific 3D NoC Design," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 207-212, San Jose, CA, November 7-11, 2011. Available at: http://dx.doi.org/10.1109/ICCAD.2011.6105327

[C170] Duo Ding, Jhih-Rong Gao, Kun Yuan, and David Z. Pan, "AENEID: A Generic Lithography-Friendly Detailed Router Based on Post RET Data Learning and Hotspot Prediction," *ACM/IEEE Design Automation Conference (DAC)*, pp. 795-800, San Diego, CA, June 5-9, 2011. Available at: http://dx.doi.org/10.1145/2024724.2024902

[C171] Moongon Jung, Joydeep Mitra, David Z. Pan, and Sung Kyu Lim, "TSV Stress-Aware Full-Chip Mechanical Reliability Analysis and Optimization for 3D IC," *ACMIEEE Design Automation Conference (DAC)*, pp. 188-193, San Diego, CA, June 5-9, 2011. **(Best Paper Award Candidate)** Available at: http://dx.doi.org/10.1145/2024724.2024767

[C172] Yongchan Ban, Kevin Lucas, and David Z. Pan, "Flexible 2D Layout Decomposition Framework for Spacer-Type Double Pattering Lithography," *ACM/IEEE Design Automation Conference*

(DAC), pp. 789-794, San Diego, CA, June 5-9, 2011. Available at: http://dx.doi.org/10.1145/2024724.2024901

[C173] Jiwoo Pak, Mohit Pathak, Sung Kyu Lim, and David Z. Pan, "Modeling of Electromigration in Through-Silicon-Via Based 3D IC," *IEEE Electronic Components and Technology Conference (ECTC)*, pp. 1420-1427, Lake Buena Vista, FL, May 31-June 3, 2011. Available at: http://dx.doi.org/10.1109/ECTC.2011.5898698

[C174] Joydeep Mitra, Moongon Jung, Suk-Kyu Ryu, Rui Huang, Sung Kyu Lim, and David Z. Pan, "A Fast Simulation Framework for Full-Chip Thermo-Mechanical Stress and Reliability Analysis of Through-Silicon-Via Based 3D ICs," *IEEE Electronic Components and Technology Conference (ECTC)*, pp. 746-753, Lake Buena Vista, FL, May 31-June 3, 2011. Available at: http://dx.doi.org/10.1109/ECTC.2011.5898596

[C175] Kun Yuan and David Z. Pan, "E-Beam Lithography Stencil Planning and Optimization with Overlapped Characters," *ACM International Symposium on Physical Design (ISPD)*, pp. 151-158, Santa Barbara, CA, March 27-30, 2011. **(Best Paper Award)** Available at: http://dx.doi.org/10.1145/1960397.1960433

[C176] Yongchan Ban, David Z. Pan, Alex Miloslavsky, Kevin Lucas, Soo-Han Choi, and Chul-Hong Park, "Layout Decomposition of Self-Aligned Double Patterning for 2D Random Logic Patterning," *International Symposium SPIE Advanced Lithography*, vol. 7974, pp. 79740L, San Jose, CA, February 28-March 2, 2011. Available at: http://dx.doi.org/10.1117/12.879500

[C177] Chul-Hong Park, David Z. Pan, and Kevin Lucas, "Exploration of VLSI CAD Researches for Early Design Rule Evaluation," *Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 405-406, Yokohama, Japan, January 25-28, 2011. **(Invited Paper)** Available at: http://dx.doi.org/10.1109/ASP-DAC.2011.5722223

[C178] Duo Ding, Andres J. Torres, Fedor G. Pikus, and David Z. Pan, "High Performance Lithographic Hotspot Detection using Hierarchically Refined Machine Learning," *Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 775-780, Yokohama, Japan, January 25-28, 2011. Available at: http://dx.doi.org/10.1109/ASP-DAC.2011.5722294

[C179] Jae-Seok Yang, Jiwoo Pak, Xin Zhao, Sung Kyu Lim, and David Z. Pan, "Robust Clock Tree Synthesis with Timing Yield Optimization for 3D-ICs," *Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 621-626, Yokohama, Japan, January 25-28, 2011. Available at: http://dx.doi.org/10.1109/ASP-DAC.2011.5722264

[C180] Shashikanth Bobba, Ashutosh Chakraborty, Olivier Thomas, Perrine Batude, Thomas Ernst, Olivier Faynot, David Z. Pan, and Giovanni De Micheli, "CELONCEL: Effective Design Technique for 3-D Monolithic Integration Targeting High Performance Integrated Circuits," *Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 336-343, Yokohama, Japan, January 25-28, 2011. Available at: http://dx.doi.org/10.1109/ASP-DAC.2011.5722210

[C181] Ashutosh Chakraborty and David Z. Pan, "Controlling NBTI Degradation during Static Burn-in Testing," *Asian and South Pacific Design Automation Conference (ASP-DAC),* pp. 597-602, Yokohama, Japan, January 25-28, 2011. Available at: http://dx.doi.org/10.1109/ASP-DAC.2011.5722259

[C182] Krit Athikulwongse, Ashutosh Chakraborty, Jae-Seok Yang, David Z. Pan, and Sung Kyu Lim, "Stress-Driven 3D-IC Placement with TSV Keep-Out Zone and Regularity Study," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 669-674, San Jose, CA, November 7-11, 2010. Available at: http://dx.doi.org/10.1109/ICCAD.2010.5654245

[C183] Minsik Cho, David Z. Pan, and Ruchir Puri, "Novel Binary Linear Programming for High Performance Clock Mesh Synthesis," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 438-443, San Jose, CA, November 7-11, 2010. Available at: http://dx.doi.org/10.1109/ICCAD.2010.5653737

[C184] Kun Yuan and David Z. Pan, "WISDOM: Wire Spreading Enhanced Decomposition of Masks in Double Patterning Lithography," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 32-38, San Jose, CA, November 7-11, 2010. Available at: http://dx.doi.org/10.1109/ICCAD.2010.5654070

[C185] Ashutosh Chakraborty and David Z. Pan, "PASAP: Power Aware Structured ASIC Placement," *International Symposium on Low Power Electronics Design (ISLPED)*, pp. 395-400, Austin, TX, August 18-20, 2010. Available at: http://dx.doi.org/10.1145/1840845.1840933

[C186] Wooyoung Jang and David Z. Pan, "Voltage and Frequency Island Optimizations for Many-Core/Networks-on-Chip Designs," *The First International Conference on Green Circuits and Systems (ICGCS)*, pp. 217-220, Shanghai, China, June 21-23, 2010. **(Invited Paper)** Available at: http://dx.doi.org/10.1109/ICGCS.2010.5543066

[C187] David Z. Pan, Jae-Seok Yang, Kun Yuan, and Minsik Cho, "CAD for Double Patterning Lithography," *IEEE International Conference on IC Design and Technology (ICICDT)*, pp. 122-125, Grenoble, France, June 2-4, 2010. **(Invited Paper)** Available at: http://dx.doi.org/10.1109/ICICDT.2010.5510279

[C188] Wooyoung Jang and David Z. Pan, "Application-Aware NoC Design for Efficient SDRAM Access," *ACM/IEEE Design Automation Conference (DAC)*, pp. 453-456, Anaheim, CA, June 13-18, 2010. Available at: http://dx.doi.org/10.1145/1837274.1837387

[C189] Yongchan Ban and David Z. Pan, "Compact Modeling and Robust Layout Optimization for Contacts in Deep Sub-Wavelength Lithography," *ACM/IEEE Design Automation Conference (DAC)*, pp. 408-411, Anaheim, CA, June 13-18, 2010. Available at: http://dx.doi.org/10.1145/1837274.1837375

[C190] Jae-Seok Yang, Krit Athikulwongse, Young-Joon Lee, Sung Kyu Lim, and David Z. Pan, "TSV Stress Aware Timing Analysis with Applications to 3D-IC Layout Optimization," *ACM/IEEE Design Automation Conference (DAC)*, pp. 803-806, Anaheim, CA, June 13-18, 2010. Available at: http://dx.doi.org/10.1145/1837274.1837476

[C191] Anurag Kumar, Minsik Cho, and David Z. Pan, "DNA Microarray Placement for Improved Performance and Reliability," *International Symposium on VLSI Design Automation and Test (VLSI-DAT)*, pp. 275-278, Hsinchu, Taiwan, April 26-28, 2010. Available at: http://dx.doi.org/10.1109/VDAT.2010.5496742

[C192] Yongchan Ban, Savithri Sundareswaran, and David Z. Pan, "Total Sensitivity Based DFM Optimization of Standard Library Cells," *International Symposium on Physical Design (ISPD)*, pp. 113-120, San Francisco, CA, March 14-17, 2010. Available at: http://dx.doi.org/10.1145/1735023.1735053

[C193] Ashutosh Chakraborty and David Z. Pan, "Skew Management of NBTI Impacted Gated Clock Trees," *International Symposium on Physical Design (ISPD)*, pp. 127-133, San Francisco, CA, March 14-17, 2010. **(Nominated for Best Paper Award)** Available at: http://dx.doi.org/10.1145/1735023.1735056

[C194] Yongchan Ban, David Z. Pan, Yuansheng Ma, Harry J. Levinson, Yunfei Deng, and Jongwook Kye, "Modeling and Characterization of Contact Edge Roughness for Minimizing Design and Manufacturing Variations in 32-nm Node Standard Cell," *International Symposium SPIE Advanced Lithography*, vol. 7641, pp. 746410D, San Jose, CA, February 2010. Available at: http://dx.doi.org/10.1117/12.846654

[C195] Wooyoung Jang and David Z. Pan, "A3MAP: Architecture-Aware Analytic Mapping for Networks-on-Chip," *Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 523-528, Taipei, Taiwan, January 18-21, 2010. Available at: http://dx.doi.org/10.1109/ASP-DAC.2010.5419827

[C196] Jae-Seok Yang, Katrina Lu, Minsik Cho, Kun Yuan, and David Z. Pan, "A New Graph-Theoretic, Multi-Objective Layout Decomposition Framework for Double Patterning Lithography," *Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 637-644, Taipei, Taiwan, January 18-21, 2010. **(Best Paper Award) (IBM Research Pat Goldberg Memorial Best Paper Award for 2010 in Computer Science, Electrical Engineering and Math)** Available at: http://dx.doi.org/10.1109/ASP-DAC.2010.5419807

[C197] David Z. Pan, Jae-seok Yang, Kun Yuan, Minsik Cho, and Yongchan Ban, "Layout Optimizations for Double Patterning Lithography," *IEEE 8th International Conference on ASIC* (*ASICON*), pp. 726-729, Changsha, China, October 20-23, 2009. **(Invited Paper)** Available at: http://dx.doi.org/10.1109/ASICON.2009.5351308

[C198] Wooyoung Jang and David Z. Pan, "An SDRAM-Aware Router for Networks-on-Chip," *ACM/IEEE Design Automation Conference (DAC)*, pp. 800-805, San Francisco, CA, July 26-31, 2009. Available at: http://dx.doi.org/10.1145/1629911.1630117

[C199] Ashutosh Chakraborty, Anurag Kumar, and David Z. Pan, "RegPlace: A High Quality Open-Source Placement Framework for Structured ASICs," *ACM/IEEE Design Automation Conference*

(DAC), pp. 442-447, San Francisco, CA, July 26-31, 2009. Available at: http://dx.doi.org/10.1145/1629911.1630029

[C200] Kun Yuan, Katrina Lu, and David Z. Pan, "Double Patterning Lithography Friendly Detailed Routing with Redundant Via Consideration," *ACM/IEEE Design Automation Conference (DAC)*, pp. 63-66, San Francisco, CA, July 26-31, 2009. Available at: http://dx.doi.org/10.1145/1629911.1629930

[C201] Duo Ding, Yilin Zhang, Haiyu Huang, Ray T. Chen, and David Z. Pan, "O-Router: An Optical Routing Framework for Low Power On-Chip Silicon Nano-Photonic Integration," *ACM/IEEE Design Automation Conference (DAC)*, pp. 264-269, San Francisco, CA, July 26-31, 2009. Available at: http://dx.doi.org/10.1145/1629911.1629983

[C202] Duo Ding and David Z. Pan, "OIL: A Nano-Photonics Optical Interconnect Library for a New Photonic Networks-on-Chip Architecture," *International Workshop on System Level Interconnect Prediction (SLIP)*, pp. 11-18, San Francisco, CA, July 26-27, 2009. Available at: http://dx.doi.org/10.1145/1572471.1572475

[C203] Katrina Lu and David Z. Pan, "Reliability-Aware Global Routing under Thermal Considerations," *Asia Symposium on Quality Electronic Design (ASQED)*, pp. 313-318, Kuala Lumpur, Malaysia, July 15-16, 2009. Available at: http://dx.doi.org/10.1109/ASQED.2009.5206246

[C204] Duo Ding, Xiang Wu, Joydeep Ghosh, and David Z. Pan, "Machine Learning Based Lithographic Hotspot Detection with Critical-Feature Extraction and Classification," *IEEE International Conference on IC Design and Technology (ICICDT)*, pp. 219-222, Austin, TX, May 18-20, 2009. **(Best Student Paper Award)** Available at: http://dx.doi.org/10.1109/ICICDT.2009.5166300

[C205] Ashutosh Chakraborty, Gokul Ganesan, Anand Rajaram, and David Z. Pan, "Analysis and Optimization of NBTI Induced Clock Skew in Gated Clock Trees," *Design, Automation & Test in Europe (DATE)*, pp. 296-299, Nice, France, April 20-24, 2009. **(Best Paper Award in the IP category)** Available at: http://dl.acm.org/citation.cfm?id=1874620.1874690

[C206] Kun Yuan, Jae-Seok Yang, and David Z. Pan, "Double Patterning Layout Decomposition for Simultaneous Conflict and Stitch Minimization," *ACM International Symposium on Physical Design (ISPD)*, pp. 107-114, San Diego, CA, March 28-April 1, 2009. Available at: http://dx.doi.org/10.1145/1514932.1514958

[C207] Ashutosh Chakraborty and David Z. Pan, "On Stress Aware Active Area Sizing, Gate Sizing, and Repeater Insertion," *International Symposium on Physical Design (ISPD)*, pp. 35-42, San Diego, CA, March 29-April 1, 2009. Available at: http://dx.doi.org/10.1145/1514932.1514941

[C208] Yong-Chan Ban, David Z. Pan, Savithri Sundareswaran, and Rajendran Panda, "Electrical Impact of Line-Edge Roughness on Sub-45nm Node Standard Cell," *International Symposium SPIE Advanced Lithography*, vol. 7275, pp. 727518, San Jose, CA, February 22-27, 2009. Available at: http://dx.doi.org/10.1117/12.814355

[C209] Jae-Seok Yang and David Z. Pan, "Overlay Aware Interconnect and Timing Variation Modeling for Double Patterning Technology," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 488-493, San Jose, CA, November 10-13, 2008. Available at: http://dx.doi.org/10.1109/ICCAD.2008.4681619

[C210] Wooyoung Jang, Duo Ding, and David Z. Pan, "A Voltage-Frequency Island Aware Energy Optimization Framework For Networks-on-Chip," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 264-269, San Jose, CA, November 10-13, 2008. Available at: http://dx.doi.org/10.1109/ICCAD.2008.4681584

[C211] Tao Luo, David A. Papa, Zhuo Li, C. N. Sze, Charles J. Alpert, and David Z. Pan, "Pyramids: An Efficient Computational Geometry-Based Approach for Timing-driven Placement," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 204-211, San Jose, CA, November 10-13, 2008. **(Best Paper Award Candidate)** Available at: http://dx.doi.org/10.1109/ICCAD.2008.4681575

[C212] Minsik Cho, Yongchan Ban, and David Z. Pan, "Double Patterning Technology Friendly Detailed Routing," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 506-511, San Jose, CA, November 10-13, 2008. Available at: http://dx.doi.org/10.1109/ICCAD.2008.4681622

[C213] Peng Yu, Xi Chen, David Z. Pan, and Andrew Ellington, "Synthetic Biology Design and Analysis: a Case Study of Frequency Entrained Biological Clock," *IEEE International Conference on*

Bioinformatics and Biomedicine (BIBM'08), pp. 329-334, Philadelphia, PA, November 3-5, 2008. Available at: http://dx.doi.org/10.1109/BIBM.2008.77

[C214] David Z. Pan, Minsik Cho, Kun Yuan, and Yongchan Ban, "Lithography Friendly Routing: From Construct-by-Correction to Correct-by-Construction," 9th *International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, pp. 2232-2235, Beijing, China, October 20-23, 2008. **(Invited Paper)** Available at: http://dx.doi.org/10.1109/ICSICT.2008.4735031

[C215] Shanhu Shen, Peng Yu, and David Z. Pan, "Enhanced DCT2-Based Inverse Mask Synthesis with Initial SRAF Insertion," *the 28th Annual SPIE/BACUS Photomask Symposium*, vol. 7122, pp. 712241, Monterey, CA, October 6-10, 2008. Available at: http://dx.doi.org/10.1117/12.801409

[C216] Anand Rajaram and David Z. Pan, "Robust Chip-Level Clock Tree Synthesis for SOC Designs," *ACM/IEEE Design Automation Conference (DAC)*, pp. 720-723, Anaheim, CA, June 8-13, 2008. Available at: http://dx.doi.org/10.1145/1391469.1391654

[C217] Tung-Chieh Chen, Ashutosh Chakraborty, and David Z. Pan, "An Integrated Nonlinear Placement Framework with Congestion and Porosity Aware Buffer Planning," *ACM/IEEE Design Automation Conference (DAC)*, pp. 702-707, Anaheim, CA, June 8-13, 2008. Available at: http://dx.doi.org/10.1145/1391469.1391651

[C218] Minsik Cho, Kun Yuan, Yongchan Ban, and David Z. Pan, "ELIAD: Efficient Lithography Aware Detailed Router with Compact Printability Prediction," *ACM/IEEE Design Automation Conference (DAC)*, pp. 504-509, Anaheim, CA, June 8-13, 2008. Available at: http://dx.doi.org/10.1145/1391469.1391598

[C219] Tung-Chieh Chen, Minsik Cho, David Z. Pan, and Yao-Wen Chang, "Metal-Density Driven Placement for CMP Variation and Routability," *International Symposium on Physical Design (ISPD)*, pp. 31-38, Portland, OR, April 13-16, 2008. Available at: http://dx.doi.org/10.1145/1353629.1353638

[C220] Minsik Cho and David Z. Pan, "A High-Performance Droplet Router for Digital Microfluidic Biochips," *International Symposium on Physical Design (ISPD)*, pp. 200-206, Portland OR, April 13-16, 2008. (**Covered by EE Times** on April 22, 2008 in the report "Labs-on-chip design automation takes cue from EDA") Available at: http://dx.doi.org/10.1145/1353629.1353672

[C221] S. X. Shi, A. Ramalingam, Daifeng Wang, and David. Z. Pan, "Latch Modeling for Statistical Timing Analysis," *Design, Automation & Test in Europe, DATE '08*, pp. 1136-1141, Munich, Germany, March 10-14, 2008. Available at: http://dx.doi.org/10.1109/DATE.2008.4484831

[C222] Ashutosh Chakraborty, S. X Shi, and David Z. Pan, "Layout Level Timing Optimization by Leveraging Active Area Dependent Mobility of Strained-Silicon Devices," *Design, Automation & Test in Europe, DATE '08*, pp. 849-855, Munich, Germany, March 10-14, 2008. Available at: http://dx.doi.org/10.1109/DATE.2008.4484780

[C223] David Z. Pan and Minsik Cho, "Synergistic Physical Synthesis for Manufacturability and Variability in 45nm Designs and Beyond," *Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 220-225, Seoul, South Korea, Jan. 21-24, 2008. **(Invited Paper)** Available at: http://dx.doi.org/10.1109/ASP-DAC.2008.4483945

[C224] Tao Luo and David Z. Pan, "DPlace2.0: A Stable and Efficient Analytical Placement Based on Diffusion," *Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 346-351, Seoul, South Korea, Jan. 21-24, 2008. Available at: http://dx.doi.org/10.1109/ASP-DAC.2008.4483972

[C225] Tao Luo, David Newmark, and David Z. Pan, "Total Power Optimization Combining Placement, Sizing and Multi-Vt Through Slack Distribution Management," *Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 352-357, Seoul, South Korea, Jan. 21-24, 2008. Available at: http://dx.doi.org/10.1109/ASP-DAC.2008.4483973

[C226] Anand Rajaram and David Z. Pan, "MeshWorks: An Efficient Framework for Planning, Synthesis and Optimization of Clock Mesh Networks," *Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 250-257, Seoul, South Korea, Jan. 21-24, 2008. **(Best Paper Award Candidate)** Available at: http://dx.doi.org/10.1109/ASP-DAC.2008.4483951

[C227] Peng Yu and David Z. Pan, "TIP-OPC: A New Topological Invariant Paradigm for Pixel Based Optical Proximity Correction," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 847-853, San Jose, CA, November 4-8, 2007. Available at: http://dx.doi.org/10.1109/ICCAD.2007.4397370

[C228] Peng Yu and David Z. Pan, "A Novel Intensity Based Optical Proximity Correction Algorithm with Speedup in Lithography Simulation," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 854-859, San Jose, CA, November 4-8, 2007. Available at: http://dx.doi.org/10.1109/ICCAD.2007.4397371

[C229] Minsik Cho, K. Lu, Kun Yuan, and David Z. Pan, "BoxRouter 2.0: Architecture and Implementation of a Hybrid and Robust Global Router," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 503-508, San Jose, CA, November 4-8, 2007. Available at: http://dx.doi.org/10.1109/ICCAD.2007.4397314

[C230] Anand Ramalingam, Ashish Kumar Singh, Sani R. Nassif, Michael Orshansky, and David Z. Pan, "Accurate Waveform Modeling using Singular Value Decomposition with Applications to Timing Analysis," *ACM/IEEE Design Automation Conference (DAC)*, pp. 148-153, San Diego, CA, June 4-8, 2007. Available at: http://dx.doi.org/10.1145/1278480.1278517

[C231] Minsik Cho, Hua Xiang, Ruchir Puri, and David Z. Pan, "TROY: Track Router with Yield-Driven Wire Planning," *ACM/IEEE Design Automation Conference (DAC)*, pp. 55-58, San Diego, CA, June 4-8, 2007. Available at: http://dx.doi.org/10.1145/1278480.1278495

[C232] Anand Ramalingam, Giri V. Devarayanadurg, and David Z. Pan, "Accurate Power Grid Analysis with Behavioral Transistor Network Modeling," *ACM International Symposium on Physical Design (ISPD)*, pp. 43-50, Austin, TX, March 18-21, 2007. Available at: http://dx.doi.org/10.1145/1231996.1232007

[C233] Gi-Joon Nam, Mehmet Can Yildiz, David Z. Pan, and Patrick H. Madden, "ISPD Placement Contest Updates and ISPD 2007 Global Routing Contest," *ACM International Symposium on Physical Design (ISPD)*, p. 167, Austin, TX, March 18-21, 2007. **(Invited)**. Available at: http://dx.doi.org/10.1145/1231996.1232029

[C234] Joon-Sung Yang, A. Rajaram, N. Shi, J. Chen, and David Z. Pan, "Sensitivity Based Link Insertion for Variation Tolerant Clock Network Synthesis," *International Symposium on Quality Electronic Design (ISQED)*, pp. 398-403, San Jose, CA, March 26-28, 2007. Available at: http://dx.doi.org/10.1109/ISQED.2007.142

[C235] Peng Yu and David Z. Pan, "Fast Predictive Post-OPC Contact/Via Printability Metric and Validation," *Proceedings of SPIE Optical Microlithography XX*, vol. 6520, pp. 652045, March 9, 2007. Available at: http://link.aip.org/link/doi/10.1117/12.717194

[C236] Haoxing Ren, David Z. Pan, C. J. Alpert, Gi-Joon Nam, and P. Villarrubia, "Hippocrates: First-Do-No-Harm Detailed Placement," *Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 141-146, Yokohama, Japan, January 23-26, 2007. Available at: http://dx.doi.org/10.1109/ASP-DAC.2007.357976

[C237] Minsik Cho, David Z. Pan, Hua Xiang, and R. Puri, "Wire Density Driven Global Routing for CMP Variation and Timing," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 487-492, San Jose, CA, November 5-9, 2006. Available at: http://dx.doi.org/10.1109/ICCAD.2006.320162

[C238] S. X. Shi, Peng Yu, and David Z. Pan, "A Unified Non-Rectangular Device and Circuit Simulation Model for Timing and Power," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 423-428, San Jose, CA, November 5-9, 2006. Available at: http://dx.doi.org/10.1109/ICCAD.2006.320151

[C239] A. Ramalingam, A. K. Singh, S. R. Nassif, Gi-Joon Nam, Michael Orshansky, and David Z. Pan, "An Accurate Sparse Matrix Based Framework for Statistical Static Timing Analysis," *Proceedings IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 231-236, San Jose, CA, November 5-9, 2006. Available at: http://dx.doi.org/10.1109/ICCAD.2006.320141

[C240] A. Dutta and David Z. Pan, "Partial Functional Manipulation Based Wirelength Minimization," *IEEE International Conference on Computer Design (ICCD)*, pp. 344-349, San Jose, CA, October 1-4, 2006. Available at: http://dx.doi.org/10.1109/ICCD.2006.4380839

[C241] Peng Yu, S. X. Shi, and David Z. Pan, "Process Variation Aware OPC with Variational Lithography Modeling," *ACM/IEEE Design Automation Conference (DAC)*, pp. 785-790, San Francisco, CA, July 24-28, 2006. Available at: http://dx.doi.org/10.1109/DAC.2006.229324

[C242] Minsik Cho and David Z. Pan, "BoxRouter: A New Global Router Based on Box Expansion and Progressive ILP," *ACM/IEEE Design Automation Conference (DAC)*, pp. 373-378, San Francisco, CA, July 24-28, 2006. **(Best Paper Award Candidate, 12 out of 865 submissions)** Available at: http://dx.doi.org/10.1109/DAC.2006.229299

[C243] Tao Luo, D. Newmark, and David Z. Pan, "A New LP Based Incremental Timing Driven Placement for High Performance Designs," *ACM/IEEE Design Automation Conference (DAC)*, pp. 1115-1120, San Francisco, CA, July 24-28, 2006. Available at: http://dx.doi.org/10.1109/DAC.2006.229407

[C244] Minsik Cho and David Z. Pan, "PEAKASO: Peak-Temperature Aware Scan-Vector Optimization," *VLSI Test Symposium (VTS),* Berkeley, CA, April 30-May 4, 2006. Available at: http://dx.doi.org/10.1109/VTS.2006.56

[C245] Anand Rajaram and David Z. Pan, "Variation Tolerant Buffered Clock Network Synthesis with Cross Links," *ACM International Symposium on Physical Design (ISPD)*, pp. 157-164, San Jose, CA, April 9-12, 2006. (**Covered by EE Times** on April 17, 2006 in the report "Paths to better timing analysis" by Richard Goering) Available at: http://dx.doi.org/10.1145/1123008.1123038

[C246] A. Havlir and David Z. Pan, "Simultaneous Statistical Delay and Slew Optimization for Interconnect Pipelines," *International Symposium on Quality Electronic Design (ISQED)*, pp. 172-178, San Jose, CA, March 27-29, 2006. Available at: http://dx.doi.org/10.1109/ISQED.2006.118

[C247] A. Ramalingam, F. Liu, S. R. Nassif, and David Z. Pan, "Accurate Thermal Analysis Considering Nonlinear Thermal Conductivity," *International Symposium on Quality Electronic Design (ISQED)*, pp. 643-649, San Jose, CA, March 27-29, 2006. Available at: http://dx.doi.org/10.1109/ISQED.2006.20

[C248] A. Rajaram and David Z. Pan, "Fast Incremental Link Insertion in Clock Networks for Skew Variability Reduction," *International Symposium on Quality Electronic Design (ISQED)*, pp. 78-84, San Jose, CA, March 27-29, 2006. Available at: http://dx.doi.org/10.1109/ISQED.2006.66

[C249] Peng Yu, David Z. Pan, and Chris A. Mack, "Fast Lithography Simulation under Focus Variations for OPC and Layout Optimizations," *SPIE Design and Process Integration for Microelectronic Manufacturing IV*, vol. 6156, pp. 397-406, February 2006. Available at: http://dx.doi.org/10.1117/12.658110

[C250] S. X. Shi and David Z. Pan, "Wire Sizing with Scattering Effect for Nanoscale Interconnection," *Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 503-508, Yokohama, Japan, January 24-27, 2006. Available at: http://dx.doi.org/10.1109/ASP-DAC.2006.1594735

[C251] A. Ramalingam, S. V. Kodakar, A. Devgan, and David Z. Pan, "Robust Analytical Gate Delay Modeling for Low Voltage Circuits," *Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 61-66, Yokohama, Japan, January 24-27, 2006. Available at: http://dx.doi.org/10.1109/ASP-DAC.2006.1594646

[C252] Minsik Cho, Hongjoong Shin, and David Z. Pan, "Fast Substrate Noise-Aware Floorplanning with Preference Directed Graph for Mixed-Signal SOCs," *Asian and South Pacific Design Automation Conference (ASP-DAC)*, pp. 765-770, Yokohama, Japan, January 24-27, 2006. **(Best Paper Award Candidate, 8 out of 424 submissions)** Available at: http://dx.doi.org/10.1109/ASP-DAC.2006.1594778

[C253] T. Luo, H. Ren, C. Alpert, and David Z. Pan, "Computational Geometry Based Placement Migration," *Proceedings ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 41-47, San Jose, CA, November 6-10, 2005. Available at: http://dx.doi.org/10.1109/ICCAD.2005.1560038

[C254] Minsik Cho, S. Ahmed, and David Z. Pan, "TACO: Temperature Aware Clock-tree Optimization," *Proceedings ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 582-587, San Jose, CA, November 6-10, 2005. (**Covered by EE Times** on June 19, 2006 in the report "Chip designers feel the heat" by Richard Goering) Available at: http://dx.doi.org/10.1109/ICCAD.2005.1560133

[C255] David Z. Pan, "Lithography Aware Physical Design," *6th International Conference on ASIC (ASICON)*, pp. 1172-1173, Shanghai, China, October 24-27, 2005. **(Invited Paper)** Available at: http://dx.doi.org/10.1109/ICASIC.2005.1611242

[C256] J. Mitra, Peng Yu, and David Z. Pan, "RADAR: RET-Aware Detailed Routing Using Fast Lithography Simulations," *ACM/IEEE Design Automation Conference (DAC)*, pp. 369-372, Anaheim, CA, June 13-17, 2005. Available at: http://dx.doi.org/10.1109/DAC.2005.193836

[C257] Haoxing Ren, David Z. Pan, C. Alpert, and P. Villarrubia, "Diffusion-Based Placement Migration," *Proceedings 42nd ACM/IEEE Design Automation Conference (DAC)*, pp. 515-520, Anaheim, CA, June 13-17, 2005. Available at: http://dx.doi.org/10.1109/DAC.2005.193863

[C258] Anand Rajaram, David Z. Pan, and Jiang Hu, "Improved Algorithms for Link-Based Non-Tree Clock Networks for Skew Variability Reduction," *Proceedings International Symposium on Physical Design (ISPD)*, pp. 55-62, San Francisco, CA, April 3-6, 2005. Available at: http://dx.doi.org/10.1145/1055137.1055150

[C259] David Z. Pan and M. D. F. Wong, "Manufacturability-Aware Physical Layout Optimizations," *International Conference on IC Design and Technology (ICICDT)*, pp. 149-153, Austin, TX, May 9-11, 2005. Available at: http://dx.doi.org/10.1109/ICICDT.2005.1502616

[C260] A. Ramalingam, Bin Zhang, David Z. Pan, and A. Devgan, "Sleep Transistor Sizing Using Timing Criticality and Temporal Currents," *Asia South Pacific Design Automation Conference (ASP-DAC)*, vol. 2, pp. 1094-1097, Shanghai, China, January 18-21, 2005. Available at: http://dx.doi.org/10.1109/ASP-DAC.2005.1466531

[C261] Gang Xu, Ruiqi Tian, David Z. Pan, and M.D.F. Wong, "CMP Aware Shuttle Mask Floorplanning," *Asia South Pacific Design Automation Conference (ASP-DAC)*, vol. 2, pp. 1111-1114, Shanghai, China, January 18-21, 2005. Available at: http://dx.doi.org/10.1109/ASP-DAC.2005.1466535

[C262] Gang Xu, Li-Da Huang, David Z. Pan, and M.D.F. Wong, "Redundant-Via Enhanced Maze Routing for Yield Improvement," *Asia South Pacific Design Automation Conference (ASP-DAC)*, vol. 2, pp. 1148-1151, Shanghai, China, January 18-21, 2005. Available at: http://dx.doi.org/10.1109/ASP-DAC.2005.1466544

[C263] Haoxing Ren, David Z. Pan, and P. G. Villarrubia, "True Crosstalk Aware Incremental Placement with Noise Map," *Proceedings ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 402-409, San Jose, CA, November 7-11, 2004. Available at: http://dx.doi.org/10.1109/ICCAD.2004.1382608

[C264] Gang Xu, R. Tian, David Z. Pan, and Martin D. Wong, "A Multi-Objective Floorplanner for Shuttle Mask Optimization," *Proceedings SPIE International Symposium on Photomask Technology*, vol. 5567, pp. 340-350, Monterey, CA, September 24, 2004. Available at: http://link.aip.org/link/doi/10.1117/12.569345

[C265] Haoxing Ren, David Z. Pan, and David S. Kung, "Sensitivity Guided Net Weighting for Placement Driven Synthesis," *Proceedings International Symposium on Physical Design (ISPD)*, pp. 10-17, Phoenix, AZ, April 18-21, 2004. Available at: http://dx.doi.org/10.1145/981066.981070

[C266] R. Puri, L. Stok, J. Cohn, D. Kung, David Z. Pan, D. Sylvester, A. Srivastava, and S. Kulkarni, "Pushing ASIC Performance in a Power Envelope," *Proceedings 40th ACM/IEEE Design Automation Conference (DAC)*, pp. 788-793, Anaheim, CA, June 2-6, 2003. Available at: http://dx.doi.org/10.1109/DAC.2003.1219126

[C267] Chin-Chih Chang, Jason Cong, and David Z. Pan, "Physical Hierarchy Generation with Routing Congestion Control," *Proceedings International Symposium on Physical Design (ISPD)*, pp. 36-41, San Diego, CA, April 7-10, 2002. Available at: http://dx.doi.org/10.1145/505388.505399

[C268] J. Cong, David Z. Pan, and P. V. Srinivas, "Improved Crosstalk Modeling for Noise Constrained Interconnect Optimization," *Proceedings Asia South Pacific Design Automation Conference (ASP-DAC)*, pp. 373-378, Yokohama, Japan, January 30-February 2, 2001. Available at: http://dx.doi.org/10.1109/ASP-DAC.2001.913335

[C269] J. Cong, Tianming Kong, and David Z. Pan, "Buffer Block Planning for Interconnect-Driven Floorplanning," *Proceedings ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 358-363, San Jose, CA, November 7-11, 1999. Available at: http://dx.doi.org/10.1109/ICCAD.1999.810675

[C270] J. Cong and David Z. Pan, "Interconnect Estimation and Planning for Deep Submicron Designs," *Proceedings ACM/IEEE 36th Design Automation Conference (DAC)*, pp. 507-510, New Orleans, LA, June 1999. Available at: http://dx.doi.org/10.1109/DAC.1999.781368

[C271] J. Cong and David Z. Pan, "Interconnect Delay Estimation Models for Synthesis and Design Planning," *Proceedings Asian and South Pacific Design Automation Conference (ASP-DAC)*, vol. 1, pp. 97-100, Hong Kong, China, January 18-21, 1999. Available at: http://dx.doi.org/10.1109/ASP-DAC.1999.759720

[C272] J. Cong, Lei He, Cheng-Kok Koh, and David Z. Pan, "Global Interconnect Sizing and Spacing with Consideration of Coupling Capacitance," *Proceedings ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 628-633, San Jose, CA, November 9-13, 1997. Available at: http://dx.doi.org/10.1109/ICCAD.1997.643604

[C273] J. Cong, David Z. Pan, Lei He, Cheng-Kok Koh, and Kei-Yong Khoo, "Interconnect Design for Deep Submicron ICs," *Proceedings ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 478-485, San Jose, CA, November 9-13, 1997. Available at: http://dx.doi.org/10.1109/ICCAD.1997.643579

C. Other Refereed Conference/Workshop Papers/Posters (without proceeding) (Partial List)

[W1] Xiaoqing Xu, Bei Yu, Jhih-Rong Gao, Che-Lun Hsu, and David Z. Pan, "PARR: Pin Access Planning and Regular Routing for Self-Aligned Double Patterning," *SRC Techcon Conference*, Austin, TX, September 2015. **(Best Paper in Session Award)**

[W2] Tetsuaki Matsunawa, Jhih-Rong Gao, Bei Yu, and David Z. Pan, "Machine Learning Based High-Accurate Hotspot Detection with Boosting Algorithm," *ACM/IEEE Design Automation Conference (DAC)* Designer Track, 2014 (**Best Designer Track Finalist**)

[W3] Jiwoo Pak, Mohit Pathak, Sung Kyu Lim, David Z. Pan, "Modeling and Prediction of Chip-Level Electromigration for TSV-Based 3D ICs," *SRC Techcon Conference*, Austin, TX, September 2012. **(Best Paper in Session Award)**

[W4] Yen-Hung Lin, Bei Yu, David Z. Pan, and Yih-Lang Li, "TRIAD: Triple Patterning Lithography Aware Detailed Router," *the 6th IEEE International Workshop on Design for Manufacturability and Yield (DFM&Y)*, June 4, 2012

[W5] Bei Yu, Yen-Hung Lin, Gerard Luk-Pat, Kevin Lucas, and David Z. Pan, "A High-Performance Triple Patterning Layout Decomposer," *the 6th IEEE International Workshop on Design for Manufacturability and Yield (DFM&Y)*, June 4, 2012

[W6] T. Luo, D. Newmark, and David Z. Pan, "Effective Power Optimization combining Placement, Sizing and Multi-Vt techniques," *SRC Techcon Conference*, Austin, TX, September 2007. **(Best Paper in Session Award)**

[W7] P. Yu and David Z. Pan, "TIP-OPC: A New Topological Invariant Paradigm for Pixel Based Optical Proximity Correction," *Proceedings SRC Techcon Conference*, Austin, TX, September 2007.

[W8] A. Ramalingam, A. K. Singh, S. R. Nassif, G.-J. Nam, M. Orshansky, and David Z. Pan, "Accurate Waveform Modeling using Singular Value Decomposition with Applications to Timing Analysis," *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, Austin, TX, February 2007.

[W9] J. Cong, David Z. Pan, and P.V. Srinivas, "Improved Crosstalk Modeling for Noise Constrained Interconnect Optimization," *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, Austin, TX, December 2000.

[W10] C.-C. Chang, J. Cong, David Z. Pan, and X. Yuan, "Interconnect-Driven Floorplanning with Fast Global Wiring Planning and Optimization," *Proceedings SRC Techcon Conference*, Phoenix, AZ, September 2000.

[W11] J. Cong, David Z. Pan, and P.V. Srinivas, "Improved Crosstalk Modeling with Applications to Noise Constrained Interconnect Optimization," *Proceedings SRC Techcon Conference*, Phoenix, AZ, September 2000.

[W12] J. Cong and David Z. Pan, "Interconnect Delay and Area Estimation for Multiple-Pin Nets," *Proceedings ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, Monterey, CA, March 1999.

[W13] J. Cong and David Z. Pan, "Interconnect Delay Estimation Models for Logic and High Level Synthesis," *SRC Techcon Conference*, Las Vegas, NV, September 1998. **(Best Paper in Session Award)**

[W14] J. Cong and David Z. Pan, "Interconnect Performance Estimation Models for Synthesis and Design Planning," *ACM/IEEE International Workshop on Logic Synthesis*, Lake Tahoe, CA, June 1998.

D. Books/Book Chapters and Dissertation

[B1] Wei Ye, Mohamed Baker Alawieh, Che-Lun Hsu, Yibo Lin, and David Z. Pan, "Dealing with Aging and Yield in Scaled Technologies," *Dependable Embedded Systems*, edited by Jörg Henkel and Nikil Dutt, Springer, 2020

[B2] Meng Li and David Z. Pan, ***A Synergistic Framework for Hardware IP Privacy and Integrity Protection*****,** Springer, 2020
[B3] Bei Yu and David Z. Pan*,* ***Design for Manufacturability with Advanced Lithography*****,** Springer, 2016
[B4] Yibo Lin and David Z. Pan, "Machine Learning in Physical Verification, Mask Synthesis, and Physical Design," *Machine Learning in VLSI Computer-Aided Design*, edited by Abe Elfedel, Duane Boning and Xin Li, Springer, 2018
[B5] Bei Yu and David Z. Pan, "Layout Decomposition for Triple Patterning," in *Encyclopedia of Algorithms*, edited by M.-Y. Kao, Springer, 2015
[B6] Minsik Cho and David Z. Pan, "Global Routing," in *Encyclopedia of Algorithms*, edited by M.-Y. Kao, Springer, 2015
[B7] M. Cho, J. Mitra, and David Z. Pan, "Manufacturability Aware Routing" in *The Handbook of Algorithms for VLSI Physical Design Automation* (edited by Charles J. Alpert, Dinesh P. Mehta, and Sachin S. Sapatnekar), CRC Press, 2009. (Invited book chapter)
[B8] David Z. Pan, B. Halpin, and H. Ren, "Timing-Driven Placement" in *The Handbook of Algorithms for VLSI Physical Design Automation* (edited by Charles J. Alpert, Dinesh P. Mehta, and Sachin S. Sapatnekar), CRC Press, 2009. (Invited book chapter)
[B9] T. Luo and David Z. Pan, "DPlace: Anchor Cell based Quadratic Placement with Linear Objective" in *Modern Circuit Placement: Best Practices and Results* (edited by Jason Cong and Gi-Joon Nam), Springer, 2007. (Invited book chapter)
[B10] David Z. Pan and M. Stan, "Physical Design and Interaction with Technology" in *CAD Algorithms, Methods and Tools for Low-Power Circuits and Systems* (edited by Enrico Macii), IEEE Technology Survey, 2006
[B11] Zhigang Pan, *Interconnect Synthesis and Planning for High-Performance IC Designs*, PhD Dissertation, University of California at Los Angeles, 2000

PATENTS:

[P1] David Zhigang Pan and Peng Yu, "Method and System for Performing Optical Proximity Correction with Process Variations Considerations." US Patent, No. 7,711,504, Granted May 4, 2010.
[P2] Minsik Cho and David Zhigang Pan, "Method and System for Performing Global Routing on an Integrated Circuit Design." US Patent, No. 7,661,085, Granted on February 9, 2010.
[P3] Anthony Correale, Jr., David S. Kung, Douglas T. Lamb, David Zhigang Pan, Ruchir Puri, and David Wallach, "Multiple Voltage Integrated Circuit and Design Method Therefore." US Patent, No. 7,480,883, Granted on January 20, 2009.
[P4] Anthony Correale, Jr., Rajeev Joshi, David S. Kung, David Zhigang Pan, and Ruchir Puri, "Single Supply Level Converter." US Patent, No. 7,119,578, Granted on October 10, 2006.
[P5] Anthony Correale, Jr., David S. Kung, Douglas T. Lamb, David Zhigang Pan, Ruchir Puri, and David Wallach, "Multiple Voltage Integrated Circuit and Design Method Therefor." US Patent, No. 7,111,266, Granted on September 19, 2006.
[P6] Anthony Correale, Jr., David S. Kung, David Zhigang Pan, and Ruchir Puri, "Method and Program Product of Level Converter Optimization." U.S. Patent, No. 7,089,510, Granted on August 8, 2006.
[P7] Jingsheng Cong, David Zhigang Pan, and P.V. Srinivas, "Method and Apparatus for Calculation of Crosstalk Noise in Integrated Circuits." U.S. Patent, No. 7,013,253, Granted March 2006.
[P8] Jingsheng Cong and David Zhigang Pan, "Wire Width Planning and Performance Optimization for VLSI Interconnects." U.S. Patent No. 6,408,427, Granted June 2002.

ORAL PRESENTATIONS:

<u>Invited Tutorials/Talks, Special Sessions, Panels at Conferences/Workshops</u>

[O1] Panelist, "ML for CAD – Where is the Treasure Hiding?" *the 2nd ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, Nov. 20, 2020

[O2] "Re-examining VLSI Manufacturing and Yield through the Lens of Deep Learning," *ICCAD 2020 Special Session 1D.1*, Nov. 2, 2020
[O3] "AI for IC and IC for AI: Closed-Loop Perspectives and Recent Results," ICCAD Workshop -- ACCAD, Nov. 6, 2020 (through Zoom)
[O4] **Keynote,** "AI for IC and IC for AI: Closed-Loop Perspectives and Recent Results," 2020 IEEE ICICM-International Conference on Integrated Circuits and Microsystems, Oct. 24, 2020 (online)
[O5] **Keynote,** "AI for IC and IC for AI: Closed-Loop Perspectives and Recent Results," CCF Integrated Circuit Design and Automation Conference, Aug. 11, 2020 (online)
[O6] **Keynote,** "AI for IC and IC for AI: A Closed-Loop Perspective," The 20th CASPA Summer Symposium, July 25, 2020 (onine)
[O7] "AI-Enabled Agile IC Physical Design and Manufacturing," ACM SIGDA / IEEE CEDA The First Design Automation WebiNar (DAWN) on Machine Learning for EDA, May 7, 2020 https://www.youtube.com/watch?v=hXWgwXJbxS0
[O8] "AI and Intelligent IC/Accelerator Design: A Synergistic Approach," Future Chip Forum, Beijing, Dec. 16, 2019
[O9] "Artificial Intelligence & Integrated Circuit: A Synergistic Approach," S. T. Yau Science Forum (丘成桐科学论坛), Beijing, Dec. 15, 2019
[O10] "MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence," ICCAD 2019 Special Session, Denver Area, Nov. 6, 2019
[O11] **"**AI-Enabled Agile IC Design and Manufacturing," IEEE Electronic Design Process Symposium (EDPS), Milpitas, CA, Oct. 3-4, 2019
[O12] "Deep Learning for Agile Physical Design and Manufacturing," 1st ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), September 3-4, 2019, Canmore (Banff Area), Canada
[O13] "Machine Learning and Its Applications in IC Physical Design," ACM/SIGDA Seasonal School on Physical Design, Beijing, China, July 28, 2019
[O14] "Deep Learning for Agile Physical Design and Manufacturing," 1st ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), September 3-4, 2019, Canmore, Canada
[O15] Panelist in "How to Build an Impactful Research Group?" ACM/IEEE Design Automation Conference Early Career Workshop, June 2, 2019
[O16] Panelist in "The Future of Interconnect Planning and Prediction (IPP)—Models, Methods, Applications and Topologies," SLIP'19, June 2, 2019
[O17] "Hardware-Software Co-design of Optical Neural Networks," The 5th International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS), Co-located with DATE 2019, Florence, Italy, March 29, 2019
[O18] "MAGICAL: Machine Generated Analog IC Layout," Emerging Technologies in EDA Workshop, Hsinchu, Taiwan, March 21, 2019
[O19] "Provably Secure Camouflaging Strategy for IC Protection," *The First Workshop on **Top Picks** in Hardware and Embedded Security*, San Diego, Nov. 8, 2018
[O20] "Analog Layout Constraint Extraction and Exploration with Application to Layout Retargeting," *International Workshop on Design Automation for Analog and Mixed-Signal Circuit*, San Diego, Nov. 8, 2018
[O21] "Machine Learning for Yield Learning and Optimization," *IEEE International Test Conference (ITC)*, Oct. 31, 2018
[O22] **Keynote** "AI and Intelligent IC Design/Manufacturing," *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Chengdu, China, Oct. 27, 2018
[O23] "Optical Computing on Photonic Integrated Circuits," OPTICS Workshop at MICRO 51, Fukuoka, Japan, Oct. 21, 2018
[O24] **Keynote** "AI and Intelligent IC Design/Manufacturing," IEEE International Test Conference in Asia (ITC-Asia), Harbin, China, Aug. 2018
[O25] "BDD-Based Logic Synthesis for Energy-Efficient Photonic Integrated Circuits," JST CREST International Workshop on Optics for Computing, Tokyo, 7/18/2018
[O26] "Machine Learning for Lithography Modeling, Mask Synthesis and Physical Design," DAC Workshop on Machine Learning in Design Automation (MALENDA), San Francisco, CA, June 24, 2018

[O27] Panelist in "Research Collaboration Panel," *The Second ACSIC Symposium on Frontiers in Computing* (**第二届北美计算机华人学者年会/暨计算技术前沿研讨会)**, Dallas, TX, June 1, 2018

[O28] **Plenary Talk** "AI and Intelligent IC Design/Manufacturing," Duke Kunshan University AI Forum, Kunshan, China, May 22, 2018

[O29] "Optical Computing on Silicon-on-Insulator Based Photonic Integrated Circuits," *North American Workshop on Silicon Photonics for High Performance Computing*, Fort Collins, Colorado, May 17-18, 2018

[O30] "Machine Learning for IC Design & Technology Co-Optimization in Extreme Scaling," *VLSI-DAT/TSA* Joint Special Session, Hsinchu, Taiwan, April 17, 2018

[O31] **Keynote** "Machine Learning for Lithography and Physical Design", China S*emiconductor Technology International Conference (CSTIC) - Symposium II and Symposium XI-DTCO Joint session*, China, March 2018

[O32] **Tutorial** "IC Design and Technology Co-Optimizations (DTCO) in Extreme Scaling," *ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC),* Jan. 22-25, 2018

[O33] "Smarter Design for Manufacturing, Reliability & Security in the IoT Era," 第二届硅谷北京国际物联网高峰论坛, Santa Clara, CA, Jan. 13, 2018

[O34] "AI Applications and Security Panel", *Future Chips Forum,* Tsinghua University, Dec. 18-19, 2017

[O35] "Nanometer IC Design and Technology Co-Optimizations – Challenges and Practices," The 1st West Lake Semiconductor Process Technology Workshop, Hangzhou, Oct. 30, 2017

[O36] "Machine Learning for Mask/Wafer Hotspot Detection and Mask Synthesis," *SPIE Photomask Technology + Extreme Ultraviolet Lithography Conference*, Monterey, CA, Sept. 2017

[O37] Panelist, "Early/Mid-Career Academic Panel," *DAC'17 Early Career Workshop*, Austin, TX, June 18, 2017.

[O38] "Toward Unidirectional Routing Closure in Extreme Scaling," *IEEE/ACM System Level Interconnect Prediction (SLIP) Workshop*, Austin, TX, June 17, 2017.

[O39] Panelist in "Academic/Industry Collaboration Panel," *The First ACSIC Symposium on Frontiers in Computing* (**第一届北美计算机华人学者年会/暨计算技术前沿研讨会)**, Chicago, June 9, 2017

[O40] Panel Moderator, "Panel on IoT and Security", *TexasWISE Workshop*, Dallas, TX, April 21, 2017

[O41] "Toward Synergistic Academic/Industry Collaboration for Future EDA Research and Talent Pipeline," *CDNLive*, April 12, 2017, Santa Clara, CA

[O42] **Vision Talk**, "Bridging Nanometer IC Design and Technology Gaps for Manufacturability, Reliability, and Security", *The First Future Chip Summit*, Beijing, Dec. 13-14, 2016

[O43] Panel Moderator, "The Dawn of EDA R&D in China," *The First Future Chip Summit*, Beijing, Dec. 13-14, 2016

[O44] Panelist, "Industry and Academic Collaboration in EDA," *The First Future Chip Summit*, Beijing, Dec. 13-14, 2016

[O45] **SIGDA Live,** "How to Survive & Thrive in Academia: My Personal Take on Promotion & Tenure," Dec. 8, 2016, https://www.youtube.com/watch?v=NhM4714z1N4

[O46] **Keynote,** "Smarter Manufacturing and Design for Reliable/Secure IC and IoT," *China-US Smart Manufacturing Summit*, Washington DC, Nov. 1, 2016

[O47] Panelist, "Smart Manufacturing and Wireless Factory," *China-US Smart Manufacturing Summit*, Washington DC, Nov. 1, 2016

[O48] **Plenary Talk,** "Bridging Design & Technology Gaps for Future Chips," *16th IEEE International Conference on Ubiquitous Wireless Broadband*, Nanjing, Oct. 17, 2016

[O49] "Bridging Design and Technology Gap for Manufacturability, Reliability, and Security," *The First ShanghaiTech Workshop on Emerging Devices, Circuits and Systems (SWEDCS)*, June 30, 2016

[O50] **Panelist, "**TSVs ARE SO 2010 - THE REALITY OF 3D-IC," *ACM/IEEE Design Automation Conference*, Austin, TX, June 6-9, 2016

[O51] **Visionary Talk,** "DFX: on Deep Nanoscale Design for Manufacturability, Reliability, and Security," *IEEE International Workshop on Design Automation for Cyber-Physical System*s (co-located with DAC), Austin, TX, June 5, 2016 http://www.ieee-cps.org/CPSDA-2016/program.html

[O52] **Keynote**, "Nanolithography and Design Technology Co-optimization in Extreme Scaling," China S*emiconductor Technology International Conference (CSTIC) - Symposium II and Symposium XI-DTCO Joint session*, Shanghai, March 13-14, 2016

[O53] Invited talk, "Standard Cell Pin Access and Physical Design in Advanced Lithography," *SPIE Advanced Lithography Conference*, San Jose, CA, Feb. 21-25, 2016
[O54] Panelist -- "From EDA to DA: Can we evolve beyond our E-roots?" ICCAD, Austin, Nov. 2-6, 2015
[O55] "Toward Cross-Layer Technology, EDA and System Power/Performance/Reliability Optimizations," Samsung Low Power Forum, Austin, TX, Oct. 8, 2015
[O56] "Cross-Layer Reliability in Extreme Scaling & Beyond," Reliability and Design (ZuE) Workshop, Siegen, Germany, September 21-23, 2015
[O57] "Pushing Multiple Patterning in Sub-10nm: Are We Ready?" *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, June 11, 2015. (**Special Session)**
[O58] "Technology, EDA and System Power/Performance/Reliability Optimization with a Cross-Layer Case Study," DAC 2015 SEAK Workshop, June 7, 2015
[O59] "Design for Manufacturing in Extreme Scaling and Beyond," *edaWorkshop*, Dresden, May 21, 2015
[O60] "Design for Manufacturability & Reliability in Extreme Scaling and Beyond," CSTIC, March 16, 2015
[O61] "Machine Learning and Pattern Matching in Physical Design," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Japan, Jan. 19-22, 2015 (**Special Session**)
[O62] IEEE CEDA All Japan Joint Chapter, "My Take on ASP-DAC on its 20th Anniversary," ASP-DAC 2015
[O63] **Keynote**, "CAD Tool and Methodology for Reliable 3D-IC Integration," TwinLab 3DSC Workshop, 11/11/2014
[O64] Invited talk, "Evolving Challenges and Techniques for Nanometer SoC Clock Network Synthesis," IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Oct. 28-31, 2014, Guilin, China
[O65] Invited talk, "Manufacturable and Reliable Interconnect in Extreme Scaling," IEEE SLIP Workshop, June 1, 2014
[O66] Invited talk, "Design for Manufacturability and Reliability in Extreme Scaling and Beyond," *China Semiconductor Technology International Conference (CSTIC)*, Shanghai, March 16, 2014
[O67] **Opening Plenary**, "Mathematical Methods in Nanometer Design for Manufacturability," *International Workshop on Mathematical Methods in Chip Design Automation*, Fuzhou, March 14-16, 2014
[O68] Invited talk, "Bridging the Gap from Mask to Physical Design for Multiple Patterning Lithography," *SPIE International Symposium on Advanced Lithography - Design-Process-Technology Co-optimization for Manufacturability VIII*, San Jose, CA, Feb. 23-27, 2014
[O69] 2013 BIMS 北京微电子国际研讨会特邀讲员，"未来集成电路的智能设计与制造,"Beijing, China, Oct. 31, 2013
[O70] Invited talk, "Lithography Hotspot Detection and Mitigation in Nanometer VLSI," 2013 *IEEE ASICON*, Shenzhen, China, Oct. 29, 2013
[O71] SRC e-Workshop, "CAD Tool and Methodology for Reliable 3D-IC Integration" (jointly presented with Prof. Sung Kyu Lim at Georgia Tech), July 18, 2013
[O72] Invited talk, "VLSI Design and Nanolithography in 14nm and Beyond", 2013 *CMOS Emerging Technologies Research Symposium*, Whistler, Canada, July 17, 2013
[O73] Invited talk, "Cross-Layer Robustness in Extreme Scaling", The first NSF/SRC/DFG International Workshop on Cross-Layer Resilience, Austin, July 11 and 12, 2013
[O74] **Keynote**, "Cross-Layer Resilient Design for Extreme Scaling and Beyond", ACM/IEEE International Workshop on Logic and Synthesis (IWLS), Austin, TX, June 7, 2013
[O75] Roundtable Panelist in "Who Will Pay for Low Power – Chip Manufacturers, Tool Providers or Consumers?" hosted by Ed Sperling of Low Power Engineering, held during DAC, June 5, Austin, TX, 2013
[O76] Invited talk, "Design for Manufacturability and Reliability in TSV-based 3D-IC", ACM/IEEE DFM&Y Workshop, Austin, TX, June 3, 2013
[O77] "CAD in Extreme Scaling and Emerging Technologies", NSF/CCC/SIGDA Workshop, Austin, TX, June 2, 2013

[O78] "Modeling and Layout Optimization for Robust 3D-IC Integration with TSVs", the 1st IEEE International High Speed Interconnect Symposium (From Silicon to Systems), Dallas, April 30, 2013
[O79] "Dealing with IC Manufacturability in Extreme Scaling", ICCAD Embedded Tutorial, Nov. 2012
[O80] "Lithography Aware Physical Design," 2012 Lithography Workshop, Williamsburg, VA, June 2012
[O81] "Reliability Modeling and Design Issues for TSV-based 3D Integration," *4th Design for 3D Silicon Integration Workshop (D43D)*, Lausanne, Switzerland, June 25, 2012
[O82] Panelist on "Future Interconnect Technologies," SLIP 2012, co-located with DAC'12 in San Francisco, CA, June 2012
[O83] Special Session talk on "VLSI CAD for Emerging Nanolithography," VLSI-DAT, Hsinchu, Taiwan, April 2012
[O84] "Design for Manufacturability with Emerging Nanolithography," ASP-DAC 2012 Tutorial, Sydney, Australia, January 2012
[O85] Special Session talk on "Physical CAD for Robust Designs," ASP-DAC 2012, Sydney, Australia, January 2012
[O86] Special Session talk on "Design for Manufacturability & Reliability for TSV-based 3D-ICs," ASP-DAC 2012, Sydney, Australia, January 2012
[O87] "Design for Manufacturability and Reliability in Extreme CMOS Scaling and 3D-IC," Global COE Workshop on "Ambient SoC Education and Research for New Leaders," co-located with ASP-DAC 2012, Sydney, Australia, January 30, 2012 (Invited talk)
[O88] "Robust and Energy Efficient Design-Process Integration in Sub-22nm CMOS and 3D-IC," Pacific Rim Outlook Forum for IC Technology (PROFIT) Workshop, Inner Mongolia, China, August 2011
[O89] "'More Moore' and 'More than Moore', beyond 22nm: Challenges and Opportunities," The 11th Emerging Information & Technology Conference, Chicago, IL, July 28-29, 2011
[O90] "Reliability and Variability in TSV-based 3D-IC Designs," The 3rd Design for 3D Silicon Integration Workshop (D43D), Grenoble, France, June 2011
[O91] **Keynote Speaker,** "Nanolithography and Design-Technology Co-optimization Beyond 22nm," TAU Workshop, Santa Barbara, CA, March 2011
[O92] "Double Patterning Lithography Layout Decomposition and Routing," IEEE Lithography Workshop, Kauai, HI, November 2010
[O93] Invited Tutorial on "Design for Resilience in Beyond-22nm CMOS & 3D-IC," IEEE Dallas CAS Workshop, Dallas, TX, October 18, 2010
[O94] "Design for Manufacturability and Reliability in TSV-based 3D-IC," ASP-DAC TPC Workshop, Seoul, Korea, September 11, 2010
[O95] "Voltage and Frequency Island Optimizations for Many-Core/ Networks-on-Chip Designs," the first International Conference on Green Circuits & Systems (ICGCS), Shanghai, China, June, 2010
[O96] "CAD for Double Patterning Lithography," IEEE ICICDT, Grenoble, France, June 3, 2010
[O97] "Layout Optimizations for Double Patterning Lithograph," IEEE ASICON, Changsha, China, October 23, 2009
[O98] "Nanometer & Emerging Design Automation Research at UTDA," ASP-DAC TPC Workshop, Tokyo, Japan, September 7, 2009
[O99] "More Moore's Law through Computational Scaling - and EDA's Role," invited talk at the **NSF Workshop on the Future of Electronic Design Automation**, Washington DC, July 8, 2009
[O100] Organizer/Presenter, "Nanolithography and CAD Challenges for 32nm/22nm (and Beyond?)," half-day tutorial at ICCAD, San Jose, CA, November 12, 2008
[O101] Invited Talk, "EDA Education and Research at UT Austin," the first EDA Education & Research Workshop, held at ICCAD 2008, San Jose, CA, November 9, 2008
[O102] Invited Talk, "Lithography Friendly Routing: From Construct-by-Correction to Correct-by-Construction," ICSICT, Beijing, China, October 21, 2008
[O103] Invited Tutorial, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," SBCCI, Gramado, Brazil, September 1, 2008
[O104] Invited Talk, "Lithography Friendly Routing: From Construct-by-Correction to Correct-by-Construction," SBCCI, Gramado, Brazil, September 2, 2008

[O105] **Keynote Speaker**, "Design for Manufacturability – Practices and Perspectives for 45/32nm and Beyond," 2008 Freescale Physical Design and Design for Manufacturing (DFM) Conference, Austin, TX, May 13-16, 2008
[O106] Special Session Organizer/Presenter, "Tackling Manufacturability/Variability for 32nm and Below," *ASP-DAC*, Seoul, Korea, January 2008
[O107] Tutorial Organizer/Presenter, "DFM Routing and Clock Distribution," *ICCAD*, San Jose, CA, November 2007
[O108] "Design and CAD for Manufacturability." *ACM/SIGDA Design Automation Summer School*, San Diego, CA, June 2-3, 2007 (held with IEEE/ACM Design Automation Conference)
[O109] "Nanometer Physical Design for Manufacturability and Variability," 3-hour Tutorial at the *VLSI-DAT* Conference, Taiwan, April 27, 2007
[O110] "DFM: Impact of Manufacturing Reality on Design," Half-day Tutorial at ICCAD, San Jose, CA, November 9, 2006
[O111] Panelist – "What Will Make or Break DFM&Y," *The First IEEE Design for Manufacturability & Yield Workshop (DFM&Y)*, San Jose, CA, October 26, 2006
[O112] Tutorial on "Lithography and Design for Variability," *Austin Conference on Integrated Systems and Circuits* (with Dr. Chris Mack), Austin, TX, May 18, 2006
[O113] Panelist – "Design for Manufacturability (DFM)," *SPIE Microlithography, Design and Process Integration Conference*, San Jose, CA, March 4, 2005
[O114] "Lithography and CMP Aware Routing," *IEEE Design for Manufacturability & Yield Workshop (DFM&Y)*, San Jose, CA, October 26, 2006
[O115] "Design for Manufacturability with Deep Sub-wavelength Lithography," *International Center on Design for Nanotechnology (IC-DFN) Workshop*, Hangzhou, China, August 16, 2006
[O116] "Manufacturability Aware Physical Layout Optimizations," *International Conference on IC Design and Technology (ICICDT)*, Austin, TX, May 2005
[O117] "Lithography Aware Physical Design," *IEEE International Conference on ASIC (ASICON)*, Shanghai, China, October 27, 2005
[O118] "Nanometer Physical Design Research at UT Austin," *International Center for System-on-Chip (IC-SOC) Workshop*, Changsha, China, August 6, 2004
[O119] "Diffusion-Based Placement Migration," *IEEE Electronic Design Process Symposium (EDPS)*, Monterey, CA, April 7, 2005
[O120] "Optimizing Power in Performance Constraints," *IEEE International Conference on Integrated Circuit Design and Technology (ICICDT)*, Austin, TX, May 19, 2004

Invited Talks at Various Institutions and Companies

[O121] "AI for IC and IC for AI: Closed-Loop Perspectives and Recent Results," Rutgers ECE Colloquium (online), Dec. 2, 2020
[O122] "MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence," Nvidia Research, Oct. 28, 2020
[O123] "AI for IC and IC for AI: Closed-Loop Perspectives and Recent Results," IEEE CEDA Hong Kong Chapter (online), Sept. 30, 2020
[O124] "AI for IC and IC for AI: Closed-Loop Perspectives and Recent Results," IEEE CASS Rio Grande do Sul Chapter (online), Sept. 11, 2020
[O125] "Machine Learning for Digital/Analog IC and FPGA Physical Design," Xilinx, July 31 (online seminar)
[O126] "AI-Enabled Agile IC Physical Design and Manufacturing," AMD, July 17, 2020 (online seminar)
[O127] "Machine Learning for Physical Design & Manufacturing," Synopsys DG Tech Talk, July 8, 2020 (online)
[O128] "DREAMPlace and Beyond," Google, June 26, 2020 (online)
[O129] "AI for IC and IC for AI: A Closed-Loop Perspective," Austin Big Data Forum, June 25, 2020 (online)
[O130] "MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence," TSMC (online seminar), May 26, 2020
[O131] "Machine Learning for Modern IC Design and Manufacturing," Apple Lonestar Design Center, Feb. 14 2020

[O132] "AI and Intelligent IC/Accelerator Design: A Synergistic Approach," Peking University, CECA Seminar, Beijing, Dec. 18, 2019
[O133] "AI and Intelligent IC/Accelerator Design: A Synergistic Approach," George Washington University, ECE Seminar, Washington DC, Dec. 4, 2019
[O134] "AI and Intelligent IC/Accelerator Design: A Synergistic Approach," Northeastern University, **ECE Distinguished Speaker Series**, Boston, Nov. 13, 2019
[O135] "AI and Intelligent IC/Accelerator Design: A Synergistic Approach," Facebook, Boston, Nov. 1, 2019
[O136] "AI-Enabled Agile IC Design and Manufacturing," MIT Lincoln Lab, Boston, Oct. 30, 2019
[O137] **"**AI-Enabled Agile IC Design and Manufacturing," Cadence AI Forum, San Jose, Oct. 15, 2019
[O138] "AI and Intelligent IC/Accelerator Design: A Synergistic Approach," University of Pennsylvania, ESE Colloquium, Oct. 1, 2019
[O139] "MAGICAL: Machine Generated Analog IC Layout," Silicon Labs, Austin, TX, June 12, 2019
[O140] "AI and Intelligent IC Design: A Synergistic Approach," MIT, Cambridge, MA, May 8, 2019
[O141] "AI and Intelligent IC Design/Manufacturing," TSMC and National Tsinghua University, Hsinchu, Taiwan, March 22, 2019
[O142] "AI and Intelligent IC Design/Manufacturing," Rice University, Houston, August 8, 2018
[O143] "Toward Machine Generated Analog IC Layout", Cirrus Logic Tech Talk, Austin, July 31, 2018
[O144] "AI and Intelligent IC Design/Manufacturing," China-Netherland Forum, Tsinghua University, China, July 11, 2018
[O145] "AI and Intelligent IC Design/Manufacturing," Peking University, China, July 10, 2018
[O146] "AI and Intelligent IC Design/Manufacturing," Shanghai Tech University, China, May 31, 2018
[O147] "AI and Intelligent IC Design/Manufacturing," John Hopcroft Center for Computer Science, Shanghai Jiaotong University, China, May 30, 2018
[O148] "AI and Intelligent IC Design/Manufacturing," Nanjing University, China, May 29, 2018
[O149] "Machine Learning for IC Design & Technology Co-Optimization in Extreme Scaling," TSMC, Silicon Valley, CA, May 4, 2018
[O150] "Intelligent Design and Manufacturing in the Era of Extreme Scaling and Internet of Everything," Peking University Shenzhen Graduate School, Shenzhen, China, March 14, 2018
[O151] "Design for X (DFx) in Extreme Scaling and Emerging Technologies," Peking University, Beijing, China, Dec. 22, 2017
[O152] "Design for X (DFx) in Extreme Scaling and Emerging Technologies," Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China, Dec. 22, 2017
[O153] "Design for X (DFx) in Extreme Scaling and Emerging Technologies," Tsinghua University, Beijing, China, Dec. 21, 2017
[O154] "Machine Learning for VLSI Design and Verification," Cirrus Logic, Austin, TX, Aug. 8, 2017
[O155] "Bridging IC Design & Technology Gaps for Manufacturability, Reliability, and Security," Xi'an Jiaotong University, May 27, 2017
[O156] "Machine Learning for Electronic Design Automation," Fudan University, Shanghai, May 22, 2017
[O157] "Machine Learning for Electronic Design Automation," University of Calgary, Canada, May 9, 2017
[O158] "Bridging IC Design & Technology Gaps for Manufacturability, Reliability, and Security in Extreme Scaling," UC Riverside, April 28, 2017
[O159] **Distinguished Lecture**, "Bridging Design & Technology Gaps for Future Chip Manufacturability, Reliability, and Security," Oklahoma State University, Stillwater, OK, April 20, 2017
[O160] **Distinguished Lecture**, "Bridging Design & Technology Gaps for Future Chip Manufacturability, Reliability, and Security," University of Kansas (KU), Lawrence, KS, April 14, 2017
[O161] **Distinguished Speaker Series**, "Bridging IC Design, Manufacturing and Security Gaps in Extreme Scaling," Cadence, San Jose, CA, April 12, 2017
[O162] "Bridging Design & Technology Gaps for Future Chip Manufacturability, Reliability, and Security," Boston University, March 30, 2017
[O163] "Bridging Design & Technology Gaps for Future IC and Systems," Fudan University, Shanghai, China, Dec. 28, 2016
[O164] "Bridging Design & Technology Gaps for Future Chips," Nantong University, China, Dec. 19, 2016
[O165] "Machine Learning in IC Design for Manufacturability & Security," Peking University, China, Dec. 15, 2016

[O166] "Machine Learning and Pattern Matching in VLSI CAD," Texas State University, San Marcos, Texas, Dec. 2, 2016
[O167] **Distinguished Lecture,** "Bridging IC Design and Technology Gaps for Manufacturability, Reliability, and Security," Michigan Technological University, Oct. 7, 2016
[O168] **Distinguished Lecture,** "Bridging IC Design and Technology Gaps for Manufacturability, Reliability, and Security," Old Dominion University, Sept. 19, 2016
[O169] "Robust Standard Cell Design and Layout Regularity Study with Nanolithography," SRC eWorkshop, August 10, 2016
[O170] "Bridging Design and Technology Gaps for Manufacturability, Reliability, and Security," Univ. of Utah, June 16, 2016
[O171] "Design & Process Technology Co-optimizations in Extreme Scaling," NVIDIA, Austin, June 13, 2016
[O172] "Challenges and Opportunities IC Design and Manufacturing in Deep Nano-Scaling and Beyond," Univ. of Science and Technology of China (USTC), Hefei, China, May 16, 2016
[O173] "Challenges and Opportunities IC Design and Manufacturing in Extreme Scaling and Beyond," Jiangnan University, Wuxi, China, May 10, 2016
[O174] "Challenges and Opportunities of IC Design & Manufacturing in Extreme Scaling and Beyond," Tsinghua University (Institute of Microelectronics), May 5, 2016
[O175] "IC Design and Technology Co-Optimization and Exploration in Extreme Scaling and Beyond," Institute of Microelectronics, Chinese Academy of Science, May 3, 2016
[O176] "Machine Learning and Pattern Matching in VLSI-CAD Applications," Intel Strategic CAD Lab Online Seminar, April 19, 2016
[O177] "Standard Cell Pin Access and Physical Design in Advanced Lithography," Intel Corporation, Hillsboro, Oregon, April 8, 2016
[O178] "Lithography Hotspot Detection and Mask Synthesis in Extreme Scaling," Intel Corporation, Hillsboro, Oregon, April 8, 2016
[O179] "Machine Learning and Pattern Matching in VLSI CAD," Chongqing University, China, March 21, 2016
[O180] "Toward Cross-Layer Power/Performance/Reliability Optimizations," School of Microelectronics, Southeast University, Nanjing, China, March 17, 2016
[O181] "Machine Learning and Pattern Matching in VLSI CAD," School of Computer Science, Southeast University, Nanjing, China, March 17, 2016
[O182] "Toward Cross-Layer Power/Performance/Reliability Optimizations," School of Microelectronics, Fudan University, Shanghai, China, March 15, 2016
[O183] "纳米集成电路设计与制造的挑战、机遇与展望 Nanometer IC Design and Manufacturing: Challenges, Opportunities, and Outlooks," University of Macao, Jan. 28, 2016
[O184] "纳米集成电路设计与制造的挑战、机遇与展望 Nanometer IC Design and Manufacturing: Challenges, Opportunities, and Outlooks," PKU-Shenzhen, China, Jan. 21, 2016
[O185] "Machine Learning and Pattern Matching in VLSI CAD," City University of Hong Kong, Hong Kong, China, Jan. 18, 2016
[O186] "Machine Learning and Pattern Matching in VLSI CAD," Chinese University of Hong Kong, Hong Kong, China, Jan. 18, 2016
[O187] "Pushing Multiple Patterning and Hybrid Lithography in Extreme Scaling," IMEC, Leuven, Belgium, Oct. 5, 2015
[O188] "Nanometer IC Design and Manufacturing Closure in Extreme Scaling and Beyond," TU Eindhoven, Netherlands, Oct. 2, 2015
[O189] "Design for Manufacturability & Reliability in Extreme Scaling and Beyond," KIT, Karlsruhe, Germany, September 28, 2015
[O190] "Multiple Patterning & Physical Design in Extreme Scaling," Univ. of Bonn, Germany, September 24, 2015
[O191] "Design for Manufacturability and Reliability in Nanometer IC and Beyond," SMIC, Shanghai, September 2, 2015
[O192] "Pushing Multiple Patterning and Hybrid Lithography in Extreme Scaling," TSMC, Hsinchu, September 1, 2015

[O193] "Pushing Multiple Patterning and Hybrid Lithography in Sub-10nm: What's the Limit?" National Tsinghua University, Taiwan, September 1, 2015
[O194] "Technology, EDA and System Power/Performance/Reliability Optimization with a Cross-Layer Case Study," Cirrus Logic, Austin, TX, August 4, 2015
[O195] "Design for Reliability in Nanometer IC and Beyond," Infineon, Munich, Germany, July 17, 2015
[O196] "Design for Manufacturability/Reliability Research at UTDA," TU Vienna, Austria, June 23, 2015
[O197] "Design for Manufacturability & Reliability in Extreme Scaling and Beyond," TUM, Munich, Germany, June 2, 2015
[O198] "Nanometer IC Design and Manufacturing: Challenges, Opportunities, and Outlooks," Huazhong University of Science and Technology, March 24, 2015
[O199] "CAD Tool and Methodology for Reliable 3D-IC and Optical Integration," Wuhan University, March 23, 2015
[O200] "Nanometer IC Design, Manufacturing and Applications: Challenges, Opportunities, and Outlooks," Nanjing University of Science and Technology, March 18, 2015
[O201] "Standard Cell Pin Access and Cell Layout Co-Optimizations," Fudan University, March 16, 2015
[O202] "Design for Manufacturability and Reliability in Extreme Scaling and Beyond," CMU ECE Colloquium, Feb. 5, 2015
[O203] "Design for Reliability in Nanometer VLSI," Hisilicon, Jan. 16, 2016
[O204] "Cross-Layer Optimizations for Nanometer VLSI in Extreme Scaling and Beyond," Peking University, Jan. 15, 2015
[O205] "Nanometer IC Design for Manufacturability and Reliability in Extreme Scaling and Beyond," Tsinghua University, EE Dept., Jan. 14, 2015
[O206] "Machine Learning and Pattern Matching in VLSI Design and Verification," HK PolyU, Jan. 8, 2015
[O207] "Cross-Layer Design for Manufacturability and Reliability in Extreme Scaling and Beyond," Chinese University of Hong Kong, Jan. 8, 2015
[O208] "Mask Synthesis and Physical Design for Nanolithography," GlobalFoundries, Dec. 12, 2014
[O209] "Mask Synthesis and Physical Design for Nanolithography," ASML, Nov. 6, 2014
[O210] "Nanometer IC Design and Manufacturing: Challenges, Opportunities, and Outlooks," Nanjing University of Posts & Telecommunications, Oct. 27, 2014
[O211] 'Design Techniques for Monolithic 3D Integration," IBM, Webinar, Oct. 3, 2014
[O212] "Mask and Physical Design Optimizations for Multiple Patterning Lithography," Samsung Electronics Future Technology Seminar, Seoul, S. Korea, Aug. 22, 2014
[O213] "Nanometer IC Design Challenges & Opportunities in Extreme Scaling and Beyond," LG Electronics, Seoul, S. Korea, Aug. 22, 2014
[O214] "Nanometer IC Design and Manufacturing in Extreme Scaling and Beyond," Shanghai Jiaotong University, Shanghai, China, July 23, 2014
[O215] "Physical Design and Manufacturing Closure for 22nm/14nm IC and Beyond," Nanjing University of Posts & Telecommunications, July 10, 2014
[O216] Design for Manufacturability & Reliability in Extreme Scaling and Beyond, Southeast University, Nanjing, China, July 8, 2014
[O217] "Physical Design and Manufacturing Closure for 22nm/14nm IC and Beyond," Nanjing University of Science and Technology, July 8, 2014
[O218] "Reclaiming Over-the-IP-Block Routing Resources for Routability and Timing," IBM EDA Seminar, Austin, TX, June 10, 2014
[O219] "Design for Manufacturability and Reliability in Extreme Scaling and Beyond," Harvard University, May 5, 2014
[O220] "Design for Manufacturability and Reliability in Extreme Scaling and Beyond," MIT, May 2, 2014
[O221] "Physical Design and Manufacturing Closure for Nanometer VLSI," Cirrus Logic, Austin, TX, April 17, 2014
[O222] "New Trends in Physical Design for Nanoscale, 3D, and Optical Integration," Fudan University, China, Jan. 10, 2014
[O223] "Intelligent Design and Manufacturing of Future Integrated Circuits," Nanjing University of Science and Technology, China, Jan. 7, 2014
[O224] "Nanometer IC Design for Manufacturability and Reliability in Extreme Scaling and Beyond," Zhejiang University, China, Jan. 6, 2014

[O225] "Design and Manufacturing Closure for Nanometer VLSI," Broadcom, Sunnyvale, Dec. 12, 2013
[O226] "Nanometer IC Design for Manufacturability and Reliability in Extreme Scaling and Beyond," IEEE CEDA Central Texas Chapter, Nov. 12, 2013
[O227] "Nanometer IC Design for Manufacturability and Reliability in Extreme Scaling and Beyond," Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China, Oct. 31, 2013
[O228] "Design for Manufacturability and Reliability in Extreme CMOS Scaling and Beyond," IEEE CAS Victoria Chapter, Univ. of Victoria, July 22, 2013
[O229] "Design for Manufacturability and Reliability in Extreme CMOS Scaling and Beyond," IEEE CAS Vancouver Chapter, UBC, July 15, 2013
[O230] "Cross-Layer Resilient Design for Extreme Scaling and Beyond," Qualcomm, San Diego, CA, July 8, 2013
[O231] "CAD for Nanolithography," School of Microelectronics, Fudan University, China, June 24, 2013
[O232] "Cross-Layer Resilient Design for Extreme Scaling and Beyond," Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China, June 20, 2013
[O233] "Physical Design and Manufacturability/Reliability in Extreme Scaling and Beyond," Huada Empyrean Software Co., Beijing, China, June 20, 2013
[O234] "Cross-Layer Resilient Design for Extreme Scaling and Beyond," Peking University, Beijing, China, June 18, 2013
[O235] "Cross-Layer Resilient Design for Extreme Scaling and Beyond," Fudan University, Shanghai, China, June 13, 2013
[O236] "Design Technologies for Extreme Scaling and Beyond," Texas Instruments, Dallas, Texas, April 29, 2013
[O237] "Design and Manufacturing Closure for Next-Generation Microprocessors," Oracle Labs Tea Talk, Redwood City, CA, April 24, 2013
[O238] "Design for Robustness in Extreme Scaling and 3D-IC," Princeton University – EE Department, March 13, 2013
[O239] "Design for Robustness in Extreme Scaling and 3D-IC," Columbia University - EE, New York, March 12, 2013
[O240] "Dealing with IC Manufacturability and Design Enablement in Extreme Scaling and Beyond," IBM Research Design Automation PIC Seminar, Yorktown Heights, March 11, 2013
[O241] "Dealing with IC Manufacturability in Extreme Scaling," Toshiba, Japan, Jan. 21, 2013
[O242] "Next Generation VLSI CAD for "More Moore" and "More than Moore," Globalfoundries, San Jose, CA, Nov. 8, 2012
[O243] "Design Technologies for "More Moore" and "More than Moore"," Oracle, Santa Clara, CA, Nov. 7, 2012
[O244] "Next Generation VLSI CAD for "More Moore" and "More than Moore," Mentor Graphics, San Jose, CA, Nov. 6, 2012
[O245] "The 'Moore', The Merrier!" Peking University, China, August 21, 2012
[O246] "The 'Moore', The Merrier!" National Taiwan University, Taipei, Taiwan, July 27, 2012
[O247] "Synergistic Design & Technology Co-Optimization for 'More Moore' and 'More than Moore'," National Tsing Hua University, Hsinchu, Taiwan, July 26, 2012
[O248] "Nanolithography and CAD Challenges beyond 14nm," Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, July 25, 2012
[O249] "Nanolithography and CAD Challenges beyond 14nm," Yuan Ze University, Taoyuan, Taiwan, July 25, 2012
[O250] "Nanolithography and CAD Challenges beyond 14nm", EPFL EE Summer Research Institute, Lausanne, Switzerland, June 22, 2012
[O251] "Physical Design in Extreme Scaling/3D Integration and Datapath-Aware Placement," Tabula, Santa Clara, CA, June 7, 2012
[O252] "Challenges and Opportunities for Physical Design in 14nm and Beyond," Samsung Austin Research Center (SARC), Austin, TX, May 29, 2012
[O253] "Design for Manufacturability/Reliability in beyond-14nm/3D-IC Integration and Datapath-aware Placement," IBM Austin Research Lab, Austin, TX, May 11, 2012
[O254] "Nanolithography and CAD Challenges beyond 14nm," National Cheng Kung University, Tainan City, Taiwan, April 26, 2012

[O255] "Design for Manufacturability & Reliability in TSV-based 3D-IC," National Cheng Kung University, Tainan City, Taiwan, April 26, 2012
[O256] "High-Performance VLSI Placement with Automatic Datapath Extraction and Evaluation," National Tsing Hua University and National Chiao Tung University, Hsinchu, Taiwan, April 23, 2012
[O257] "Design for Manufacturability and Reliability in Extreme CMOS Scaling and 3D-IC Integration," Department of Electrical Engineering, University of Southern California, Los Angeles, CA, April 13, 2012
[O258] "Resilient Design in Extremely-Scaled CMOS and 3D-IC Integration," ARM Inc., Austin, TX, April 11, 2012
[O259] "Design for Manufacturability and Reliability in Beyond-14nm Lithography and 3D-IC Integration," Fudan University, Shanghai, China, Jan. 10 2012
[O260] 'More Moore' and 'More than Moore' in Sub-20nm CMOS and 3D-IC," Peking University, Beijing, China, December 30, 2011
[O261] "'More Moore' and 'More than Moore' in Sub-20nm CMOS and 3D-IC," Tsinghua University, Beijing, China, December 29, 2011
[O262] "Resilient Design in Nanoscale CMOS and 3D-IC," Globalfoundries, Sunnyvale, CA, November 11, 2011
[O263] "Resilient Design Closure in Nanoscale CMOS and 3D-IC," Oracle, Sunnyvale, CA, November 9, 2011
[O264] "Resilient Design Closure in Nanoscale CMOS and 3D-IC," ARM, San Jose, CA, November 8, 2011
[O265] "Resilient Design Closure in Nanometer CMOS and 3D-IC," Freescale, Austin, TX, October 19, 2011
[O266] "'More Moore' and 'More than Moore' in Nanometer CMOS and 3D-IC," Shangdong University, Shangdong, China, July 19, 2011
[O267] "'More Moore' and 'More than Moore' in sub-22nm CMOS and 3D-IC," Zhejiang University, Zhejiang, China, July 12, 2011
[O268] "Physical Design and DFM in Sub-22nm and 3D," Politecnico di Torino, Torino, Italy, July 1, 2011
[O269] "Design and Technology Integration in beyond-22nm CMOS and 3D-IC," IMEC, Leuven, Belgium, June 27, 2011
[O270] "'More Moore' and 'More than Moore' beyond 22nm: Challenges and Opportunities," Katholieke Universiteit Leuven, Leuven, Belgium, June 27, 2011
[O271] "Recent Results in Nanometer Physical CAD," AMD, Austin, TX, May 19, 2011
[O272] "Nanometer Physical Design and Technology Co-optimization: A Synergistic Perspective," Samsung Austin Research Center, Austin, TX, May 5, 2011
[O273] "Design and Technology Co-optimization in beyond-22nm CMOS and 3D-IC Integration," Qualcomm, San Diego, CA, April 1, 2011
[O274] "Design and Technology Integration in beyond-22nm CMOS and 3D-IC," Globalfoundries, Sunnyvale, CA, February 4, 2011
[O275] "Design for Manufacturability and Reliability in beyond-22nm CMOS and 3D-IC Integration," Fujitsu Labs, Kawasaki, Japan, January 26, 2011
[O276] "Design for Resilience in Beyond-22nm CMOS and 3D-IC," UIUC ECE Colloquium, Urbana Champaign, IL, September 30, 2010
[O277] "Design for Resilience in Nanometer CMOS and 3D-IC," Samsung, Korea, September 9, 2010
[O278] "Design for Resilience in Nanometer CMOS and 3D-IC," Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, September 8, 2010
[O279] "Design for Resilience in Nanometer CMOS and 3D-IC," Design Automation PIC Seminar Series, IBM T. J. Watson Research Center, Yorktown Heights, NY, July 22, 2010
[O280] "Challenges and Opportunities in Nanometer VLSI and 3D-IC," Fuzhou University, Fuzhou, China, July 4, 2010
[O281] "Design for Manufacturability and Resilience in Nanometer CMOS and 3D-IC," TSMC, Hsinchu, Taiwan, April 28, 2010
[O282] "Design for Resilience in Nanometer CMOS and 3D-IC," at Springsoft, National Chiao Tung University, April 29; at Fudan University and Shanghai Jiaotong University, June 25; at Peking University and Tsinghua University, June 29; at Institute of Computing Technology, Chinese Academy of Sciences, June 30, 2010

[O283] "Design for Manufacturability and Robustness in Nanometer CMOS, 3D-IC, and Emerging Technologies," ITRI, Hsinchu, Taiwan, April 28, 2010
[O284] "Recent Results in Design for Manufacturing and Robustness," Freescale, Austin, TX, April 9, 2010
[O285] "Low Power Design and Challenges in Nanometer Multicore Era," IEEE CAS Melbourne and Victoria University, Melbourne, Australia, August 20, 2009
[O286] **IEEE Distinguished Lecture**, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," IEEE CAS Melbourne, Melbourne, Australia, August 20, 2009
[O287] **IEEE Distinguished Lecture**, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," IEEE CAS Sydney, Sydney, Australia, August 14, 2009
[O288] "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," Institute of Microelectronics, Singapore, July 14, 2009
[O289] **IEEE Distinguished Lecture**, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," IEEE CAS Singapore Chapter, Singapore, July 13, 2009
[O290] "Unified Analysis, Characterization and Optimization of Systematic and Random Variations with Variational Litho-Modeling," SRC e-Workshop, Austin, TX, April 22, 2009
[O291] "On Clock Mesh Design," Sun Microsystems, Austin, TX, March 9, 2009
[O292] "On Graduate Research and Education in US," Zhejiang University, Hangzhou, China, January 12, 2009
[O293] "Synergistic Modeling and Optimization for Nanometer IC Design & Manufacturing Closure," Tsinghua University, Beijing, China, October 24, 2008
[O294] **IEEE Distinguished Lecture**, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," IEEE CAS Taiwan, Kaohsiung, Taiwan, September 10 and 11, 2008
[O295] "Nanometer Physical Design and DFM," SpringSoft, Hsinchu, Taiwan, September 9, 2008
[O296] "On Nanometer VLSI Physical Design and Manufacturing Closure: What, Why, and How?," UFRGS, Porto Alegre, Brazil, August 13, 2008
[O297] "Physical Design Issues in Microfluidic Biochips," Technical University of Dresden, Germany, July 4, 2008
[O298] **IEEE Distinguished Lecture**, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," IEEE Los Angeles Council, Los Angeles, CA, June 9, 2008
[O299] "New Faculty Seminar on NSF CAREER," FIC, Cockrell School of Engineering, UT Austin, Austin, TX, May 21, 2008
[O300] "Modeling and Optimization for Nanometer IC Design and Manufacturing Integration," AMD, Austin, TX, March 28, 2008
[O301] "Synergistic Modeling and Optimization for Nanometer Design for Manufacturing," Texas Instruments, Dallas, TX, February 15, 2008
[O302] "Synergistic Modeling and Optimization for Physical and Electrical DFM," UT Dallas, Dallas, TX, February 14, 2008
[O303] "Synergistic Modeling and Optimization for Physical and Electrical DFM," UC Santa Barbara, CA, February 8, 2008
[O304] "Synergistic Modeling and Optimization for Physical and Electrical DFM," Seoul National University LSI Workshop, Seoul, Korea, January 25, 2008
[O305] "Synergistic Modeling and Optimization for Physical and Electrical DFM," Samsung Electronics, Seoul, Korea, January 21, 2008
[O306] "Synergistic Modeling and Optimization for Physical and Electrical DFM," Stanford University, Stanford, CA, November 30, 2007
[O307] "Synergistic Modeling and Optimization for Physical and Electrical DFM," University of California at Berkeley, CA, November 30, 2007
[O308] "Synergistic Modeling and Optimization for Physical and Electrical DFM," Mentor Graphics, San Jose, CA, November 29, 2007
[O309] "Challenges and Opportunities for Nanometer VLSI Design and Manufacturability," Tongji University, Shanghai, China, August 23, 2007
[O310] "Synergistic Modeling and Optimization for Physical and Electrical DFM," Tsinghua University and Peking University, Beijing, China, August 22, 2007

[O311] "Challenges and Opportunities for Nanometer IC Design and Manufacturability," Shangdong University, Jinan, China, August 20, 2007
[O312] "Challenges and Opportunities for Nanometer IC Design and Manufacturability," Southeast University, Nanjing, China, August 10, 2007
[O313] "Recent Results and Physical and Electrical DFM," Qualcomm, San Diego, CA, July 11, 2007
[O314] "Synergistic Modeling and Optimization for Physical and Electrical DFM," **Cadence Distinguished Seminar Series**, San Jose, CA, July 11, 2007
[O315] "Recent Research Highlights at UTDA," Cadence Berkeley Lab, Berkeley, CA, July 11, 2007
[O316] "DFM and Physical CAD Research at UTDA," Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, April 25, 2007
[O317] "Modeling & Optimization for Physical and Electrical DFM," National Tsing-hua University, Hsinchu, Taiwan, April 24, 2007
[O318] "Modeling & Optimization for Physical and Electrical DFM," National Taiwan University, Taipei, Taiwan, April 23, 2007
[O319] "Tackling Design for Manufacturability/Variability from Root Causes," Intel Corporation, Santa Clara, CA, February 28, 2007
[O320] "Recent Research on Physical CAD and DFM at UT Design Automation (UTDA) Lab," System LSI Design Workshop, Fukuoka, Japan, September 9, 2006
[O321] "Modeling and Optimization for Nanometer Physical Design and Manufacturability," Fudan University, Shanghai, China, August 24, 2006
[O322] "Physical Design and Manufacturability Closure for Nanometer VLSI/SOC," 6th Emerging Information Technology Conference (EITC), Dallas, TX, August 10, 2006
[O323] "Modeling and Optimization for Nanometer Physical Design and Manufacturability," IBM T. J. Watson Research Center, Yorktown Heights, NY, July 21, 2006
[O324] "The Real DFM - Physical Design for Manufacturability/Variability," Freescale Seminar, Austin, TX, July 13, 2006
[O325] "The True DFM - Physical Design For Manufacturability" (part two), IBM EDA Seminar Series, Fishkill, NY, May 2, 2006 (given through conference call & online)
[O326] "The True DFM - Physical Design For Manufacturability" (part one), IBM EDA Seminar Series, Fishkill, NY, April 25, 2006 (given through conference call & online)
[O327] "New Ideas in Nanometer Physical CAD & DFM," Intel, Santa Clara, CA, February 24, 2006
[O328] "A New LP Based Incremental Timing Driven Placement for High Performance Designs," IBM Austin CAS Conference, Austin, TX, February 17, 2006
[O329] "Nanometer Physical Design for Manufacturability," STARC, Kawasaki, Japan, January 25, 2006
[O330] "Physical Design for Manufacturability," Fujitsu Corporation, Kawasaki, Japan, January 23, 2006
[O331] "New Ideas in Nanometer Physical CAD & Manufacturability," Tsinghua University, Beijing, China, October 28, 2005
[O332] "Challenges and Opportunities in Nanometer VLSI Physical Design & Manufacturing Closure," Peking University, Beijing, China, October 28, 2005
[O333] "Physical Design for Manufacturability," Zhejiang University, Hanzhou, China, October 24, 2005
[O334] "New Ideas in Nanometer Physical Synthesis & DFM," IBM T. J. Watson Research Center, Yorktown Heights, NY, August 8, 2005
[O335] "Litho-Aware Routing & Diffusion-Based Placement," Cadence, San Jose, CA, July 28, 2005
[O336] "New Ideas in Nanometer Physical CAD," Sun Microsystems, Austin, TX, July 21, 2005
[O337] "New Ideas in Placement & Variation-Tolerant Clock Designs," Intel Strategic CAD Lab, Hillsboro, OR, July 8, 2005
[O338] "New Ideas in Placement & DFM," Synopsys Advanced Technology Group, Hillsboro, OR, July 7, 2005
[O339] "True Manufacturability Aware Physical Design," Freescale, Austin, TX, May 27, 2005
[O340] "Physical CAD Research on Nanometer Design and Manufacturing Closure," Texas Instruments, Dallas, TX, March 18, 2005
[O341] "Diffusion-Based Placement Migration," IBM Austin CAS Conference, Austin, TX, February 25, 2005
[O342] "Nanometer Physical Synthesis for Multi-Objective Design Closure and Manufacturability," Magma Design Automation, Santa Clara, CA, November 5, 2004

[O343] "Nanometer Physical Synthesis for Multi-Objective Design Closure and Manufacturability," Cadence Berkeley Lab, Berkeley, CA, November 5, 2004
[O344] "Nanometer Physical Synthesis for VLSI Design Closure," University of Maryland at College Park, MD, October 22, 2004
[O345] "Recent Results of Physical Synthesis with Nanometer Effects," IBM Austin Research Lab Seminar, Austin, TX, October 8, 2004
[O346] "Holistic Approaches for Multi-Objective Design Closure with Nanometer Effects," AMD, Austin, TX, October 5, 2004
[O347] "Nanometer Physical Synthesis for Timing, Signal Integrity, and Low Power Optimizations," Synopsys Advanced Technology Group, Hillsboro, OR, October 1, 2004
[O348] "Nanometer Physical Synthesis for Timing, Signal Integrity, and Low Power Optimizations," Intel Strategic CAD Lab, Hillsboro, OR, September 30, 2004
[O349] "Integrated Placement with Nanometer Timing and Signal Integrity Closure," Electrical Engineering Department, Texas A&M University, College Station, TX, September 28, 2004
[O350] "Recent Results of Physical Synthesis with Nanometer Effects," Intel, Austin, TX, September 9, 2004
[O351] "Nanometer VLSI Designs: Challenges, Opportunities and Optimizations," Shanghai Jiaotong University, Shanghai, China, August 17, 2004
[O352] "Holistic Approaches of Next-Generation Physical Design to Cope with Nanometer Effects," Fudan University, Shanghai, China, August 17, 2004
[O353] "Physical Synthesis in Nanometer VLSI Designs," Tsinghua University, China, August 12, 2004
[O354] "Physical Design with Integrity." Agere Systems, Allentown, PA, July 27, 2004
[O355] "Recent Results of Physical Synthesis with Nanometer Effects," IBM T. J. Watson Research Center, Design Automation PIC Seminar, Yorktown Heights, NY, July 26, 2004
[O356] "Nanometer Physical Synthesis for Performance, Power and Predictability," AMD, Austin, TX, March 4, 2004
[O357] "Physical Synthesis for Nanometer Designs," IEEE CAS/SSC Joint Chapter Meeting, Austin, TX, February 26, 2004
[O358] "Physical Synthesis for Nanometer Designs," Motorola SPS (Freescale), Austin, TX, February 19, 2004
[O359] "Interconnect-Centric Design Closure for High Performance and Low Power VLSI," ECE Department, Yale University, New Haven, CT, May 12, 2003
[O360] "Interconnect-Centric Design Closure for High Performance and Low Power VLSI," ECE Department, University of Wisconsin at Madison, Madison, WI, May 1, 2003
[O361] "Physical Design Closure for High Performance and Low Power VLSI," ECE Seminar, Purdue University, West Lafayette, IN, April 17, 2003
[O362] "Physical Design Closure for High Performance and Low Power VLSI," EE-Systems, University of Southern California, Los Angeles, CA, April 14, 2003
[O363] "Physical Design Closure for High Performance and Low Power VLSI," Department of Electrical and Computer Engineering, UT Austin, Austin, TX, April 7, 2003
[O364] "Physical Design Closure for High Performance and Low Power VLSI," Division of Engineering, Brown University, Providence, RI, April 2, 2003
[O365] "Challenges and Opportunities for Nanometer Design Closure," VLSI Seminar Series, University of Michigan, Ann Arbor, MI, October 28, 2002
[O366] "Interconnect Prediction and Planning for Design Closure," EE Seminar, Fudan University, Shanghai, China, November 26, 2001

MEDIA COVERAGE:

- MIT Technology Review - DeepTech 深科技, April 12, 2020, "谷歌又一野心浮现：用 AI"反哺"芯片设计," https://mp.weixin.qq.com/s/B-71EH6aOqWl9zZI8SgA0Q
- EE Times, April 6, 2017, "ISPD Predicts Chip Futures," http://www.eetimes.com/document.asp?doc_id=1331563 (covered my UT group as the "ISPD'17 Clock-aware FPGA Placement Contest" 1st Place Winner)

- Semiconductor Engineering, September 7, 2016, "Joint R&D Has Its Ups and Downs," http://semiengineering.com/joint-rd-has-its-ups-and-downs/
- EE Times, April 8, 2016, "Machine Learning Routes Chips," http://www.eetimes.com/document.asp?doc_id=1329391 (covered my students and I as the ISPD'16 FPGA Placement Contest 1st Place Winners)
- EE Times, April 9, 2014,"ISPD-14 Focuses on FinFETs, Security, Supply Chain," http://www.eetimes.com/document.asp?doc_id=1321843 (covered our ISPD'14 Best Paper)
- SRC Press Release, "2013 Technical Excellence Award Presented to David Pan from UT/Austin" http://www.src.org/award/tech-excellence/2013/
- Stanford and UT Austin Professors to Be Honored for Advancing Chip Research at Annual SRC TECHCON Event
  - http://www.src.org/newsroom/press-release/2013/499/
  - Business Wire Article: http://www.businesswire.com/news/home/20130905005318/en/Stanford-UT-Austin-Professors-Honored-Advancing-Chip
  - + other media coverage (Yahoo Finance, Market Watch, etc.)
- June 2013, DAC Roundtable "Experts at the Table: Who Pays for Low Power?" hosted by System-Level Design Editor-in-Chief Ed Sperling http://lp-hp.com/blog/2013/07/11/experts-at-the-table-who-pays-for-low-power/
- Synopsys Conversation Central, "CAD Research and Education in Extreme Scaling and Beyond," hosted by Karen Bartleson, June 2013 (Synopsys web site, YouTube, Podcast)
  - Show Notes page: http://bit.ly/13jZHFb
  - YouTube Video: http://youtu.be/06mz2HLkWpk
  - iTunes Page: http://bit.ly/QPtlHr
- EE Times, April 13, 2011: "ISPD spots 3-D, maskless-lithography trends," http://www.eetimes.com/electronics-news/4215124/ISPD-reveals-3-D--maskless-lithography-trends-
- March 20, 2010: Interview by Prof. Patrick Madden, ACM/SIGDA Chair, on the ASP-DAC 2010 Best Paper on *"A Multi-Objective Min-Cut Based Layout Decomposition Framework for Double Patterning Lithography,"* http://www.youtube.com/watch?v=N76t3YNQoPc
- May 19, 2009: "The IEEE CANDE Committee Elects Officers", Reuters, Yahoo Finance, etc. http://www.reuters.com/article/pressRelease/idUS155240+19-May-2009+BW20090519
- EE Times, April 21, 2008, "Lab-on-chip design automation takes cue from EDA," http://www.eetimes.com/electronics-news/4076826/Lab-on-chip-design-automation-takes-cue-from-EDA
- EE Times, April 17, 2008, "Future of chip design revealed at ISPD," http://www.eetimes.com/showArticle.jhtml?articleID=207400313
- EE Times (China/Taiwan), April 30, 2007, "VLSI-DAT 盛况空前，业界专家布道前瞻新技术" (in Chinese), http://www.eetchina.com/ART_8800462927_480401_NT_0f306e22.HTM
- EE Times, April 2, 2007, "Rethinking statistical timing analysis," http://eetimes.com/news/design/showArticle.jhtml?articleID=198700121
- EE Times, March 22, 2007, "IC routing contest boosts CAD research," http://eetimes.com/news/design/showArticle.jhtml?articleID=198500084
- EE Times, June 19, 2006, "Chip designers feel the heat - Accurate thermal analysis cools the effects of sub-90-nm design," http://www.eetimes.com/news/design/showArticle.jhtml?articleID=189400781
- EE Times, April 17, 2006, "Paths to better timing analysis," http://www.eet.com/news/latest/showArticle.jhtml?articleID=185302541
- EE Times, October 28, 2005, "EDA startup forms technical advisory board," http://www.eetimes.com/news/design/showArticle.jhtml?articleID=172901367
- EE Times, July 11, 2005, "Shift to 65 nm has its costs," http://www.eetimes.com/news/latest/showArticle.jhtml?articleID=165701002

CURRENT PHD/MS STUDENTS, POST-DOCs AND VISITING SCHOLARS:

- **Students admitted to Ph.D. candidacy**:
  -
- **Post M.S. students preparing to take Ph.D. qualifying exam**:
  - Chenghao Feng (co-supervised with Prof. Ray Chen)
  - Jiaqi Gu (co-supervised by Prof. Ray Chen)
  - Zixuan Jiang
  - Mingjie Liu
  - Rachel Selina Rajarathnam
  - Keren Zhu
- **M.S. in progress:**
  - Ahmet F. Budak (co-supervised by Prof. Nan Sun)
  - Hao Chen
  - Hanqing Zhu
- **Post-docs:**
  - Xiyuan Tang
- **Visiting Scholars:**

PH.D. SUPERVISIONS COMPLETED:

Name	PhD Dissertation	Semester	First job after PhD and current position (with selected awards)
1. Haoxing Ren	Incremental Placement for Modern VLSI Design Closure	Spring 2006	Research Staff Member, IBM T. J. Watson Research; now Principal Research Scientist, NVIDIA
2. Gang Xu	Layout Optimization Algorithms for VLSI Design and Manufacturing	Summer 2007	R&D Engineer, Mentor Graphics; now Software Engineer, Google
3. Tao Luo	Nanometer VLSI Placement and Optimization for Multi-Objective Design Closure	Fall 2007	Sr. MTS, Magma; now Sr. Software Engineer, Uber (2007 SRC Techcon Best Paper in Session)
4. Anand Ramalingam	Analysis Techniques for Nanometer Digital Integrated Circuits	Fall 2007	Member of Consulting Staff, Magma DA; now Staff Engineer at Synopsys
5. Minsik Cho	Physical Synthesis for Nanometer VLSI and Emerging Technologies	Summer 2008	Research Staff Member, IBM T. J. Watson Research Center; now Program Director/Master Inventor at IBM Systems (ISPD'13 Best Paper Award; IBM Research 2010 Pat Goldberg Memorial Best Paper Award; 2008 SRC Inventor Recognition Award; 2007 IBM PhD Scholarship; ISPD'07 Global Routing Contest Awards)
6. Anand Rajaram	Synthesis of Variation Tolerant Clock Distribution Networks	Fall 2008	Member of Consulting Staff, Magma DA; now Sr. Staff R&D Engineer, Synopsys
7. Peng Yu	Fast and Accurate Lithography Simulation and Optical Proximity Correction for Nanometer Design for Manufacturing	Spring 2009	Post-Doc Researcher, Baylor College of Medicine; now Assistant Professor, Texas A&M University (2008-09 UT Graduate School Continuing Fellowship; 2008 SPIE Education Scholarship; 2008 SRC Inventor Recognition Award)

8. Xiaokang (Sean) Shi	Modeling and Optimization to Connect Layout with Silicon for Nanoscale IC	Fall 2009	Sr. Component Engineer, Intel Corporation; now Engineer at Bloomberg (2009 IBM PhD Scholarship)
9. Kun Yuan	VLSI Physical Design Automation for Double Patterning and Emerging Lithography	Fall 2010	Sr. Member of Technical Staff, Cadence; now Sr. Software Engineer at Airbnb (ISPD'11 Best Paper Award; IBM Research 2010 Pat Goldberg Memorial Best Paper Award)
10. Ashutosh Chakraborty	Mechanical Stress and Circuit Aging Aware VLSI CAD	Fall 2010	Senior Hardware Engineer, Oracle; now Software Engineer at Google (2009 DATE Best Paper/IP Award; 2009-10 UT Graduate School Continuing Fellowship; 2009 eASIC Placement Contest 1st Prize)
11. Jae-Seok Yang	Nanometer VLSI Design-Manufacturing Interface for Large Scale Integration	Spring 2011	Senior Engineer, Samsung; now Principal Engineer, Samsung (2010 ASP-DAC Best Paper Award; IBM Research 2010 Pat Goldberg Memorial Best Paper Award)
12. Wooyoung Jang	Architecture and Physical Design for Advanced Networks-on-Chip	Spring 2011	Senior Engineer, Samsung; now Assistant Professor, Dankook University, S. Korea (2006-2011 Samsung Scholarship)
13. Yongchan (James) Ban	Lithography Variability Driven Cell Characterization and Layout Optimization for Manufacturability	Spring 2011	Senior Engineer, Intel; now MTS, Synopsys (2010 SPIE Education Scholarship)
14. Duo Ding	CAD for Nanolithography and Nanophotonics	Summer 2011	Senior Hardware Engineer, Oracle; now Senior Staff Software Engineer at Samsung Electronics (2013 ACM Outstanding PhD Dissertation Award in EDA; 2012 ASP-DAC Best Paper Award; 2009 ICICDT Best Student Paper Award)
15. Samuel Ward	Physical Design Automation of Structured High-Performance Integrated Circuits	Fall 2013	Data Scientist/Fraud Manager, Apple Inc. (IBM Master Inventor in 2011)
16. Jhih-Rong (Jerrica) Gao	Lithography Aware Physical Design and Layout Optimization for Manufacturability	Spring 2014	Senior Member of Technical Staff, Cadence; now Principal Software Engineer at Cadence (ICCAD'13 Best Paper Award, ICCAD'12 and ICCAD'13 CAD Contest Awards, SPIE 2013 Scholarship)
17. Jiwoo Pak	Electromigration Modeling and Layout Optimization for Advanced VLSI	Spring 2014	Senior Member of Technical Staff, Cadence; now Principal Software Engineer at Cadence (SRC Techcon 2012 Best in Session Award, 2013 Grace Hopper Celebration Scholarship)

18. Bei Yu	Design for Manufacturing with Advanced Lithography	Summer 2014	Post-doc Researcher, UT Austin; now Assistant Professor at Chinese University of Hong Kong (EDAA Outstanding Dissertation Award, ICCAD'13 Best Paper Award, ASP-DAC'12 Best Paper Award, 2013 Chinese Government Award for Outstanding Self-Financed Students Abroad, 2013/2012 ICCAD CAD Contest 2nd Place Awards, Silver Medal in ACM Student Research Contest, SPIE Optics and Photonics Education Scholarship, 2012 IBM Ph.D. Scholarship)
19. Yilin Zhang	Interconnect Optimizations for Nanometer VLSI Design	Summer 2014	Software Scientist, Rocket Fuel Inc., now Software Engineer, Google
20. Subhendu Roy	Logic and Clock Network Optimization in Nanometer VLSI Circuits	Summer 2015	Principal Software Engineer, Cadence; now Intel (ISPD 2014 Best Paper Award; TexasWISE 2014 Best Student Poster Award)
21. Xiaoqing Xu	Standard Cell Optimization and Physical Design in Advanced Technology Nodes	Spring 2017	Senior Research Engineer, ARM Research (Gold Medal at Design Automation Student Research Competition by ACM SIGDA 2016; Best in Session Award at SRC Techcon 2015)
22. Yibo Lin	Bridging Design and Manufacturing Gap through Machine Learning and Machine-Generated Layout	Spring 2018	Post-doc Researcher, UT Austin; Assistant Professor at Peking University (DAC'19 Best Paper Award; Integration – the VLSI Journal Best Paper Award 2018; UT Graduate Continuing Fellowship 2017; SPIE'16 Franco Cerrina Memorial Best Student Paper Award)
23. Jiaojiao Ou	Design for Manufacturing with Directed Self-Assembly Lithography	Spring 2018	Senior R&D Engineer, Synopsys (2017 SPIE BACUS Scholarship)
24. Derong Liu	Layer Assignment and Routing Optimization for Advanced Technologies	Summer 2018	Lead Software Engineer, Cadence (ISPD'18 Best Paper Award)
25. Meng Li	A Synergistic Framework for Hardware IP Privacy and Integrity Protection	Summer 2018	Research Scientist, Facebook Reality Lab (First Place of ACM Student Research Competition Grand Finals 2018; EDAA Outstanding Dissertation Award 2018; GLSVLSI'18 Best Paper Award; Gold Medal of ACM/SIGDA Student Research Competition 2017; HOST'17 Best Paper Award)
26. Biying Xu	Layout Automation for Analog and Mixed-Signal Integrated Circuits	Spring 2019	Lead Software Engineer, Cadence (Cadence Women in Technology Scholarship 2018)
27. Joydeep Mitra	Mask Synthesis Techniques for Directed Self-Assembly	Spring 2019	Senior Software Architect, Cadence

28. Wuxi Li	Placement Algorithms for Large-Scale Heterogeneous FPGAs	Summer 2019	Staff Software Engineer, Xilinx (DAC'19 Best Paper Award, ISPD 2017 and 2016 Contests First Place)
29. Shounak Dhar	Modern FPGA Placement Techniques with Hardware Acceleration	Summer 2019	SoC Design Engineer, Intel (DAC'19 Best Paper Award, ISPD 2016 Contest First Place)
30. Zhoufeng Ying (co-supervised with Prof. Ray Chen)	Monolithic and Hybrid Nanophotonic Chips for High-speed and Power-Efficient Optical Computing and Interconnects	Spring 2020	Senior Silicon Photonics Designer, Alpine Optoelectronics
31. Zheng Zhao (co-supervised by Prof Ray Chen)	Design Automation for Optical Computing: Boolean Logic and Neural Networks	Spring 2020	Senior Software Engineer, Synopsys (Cadence Women in Technology Scholarship in 2019)
32. Wei Ye	Design for Manufacturability and Reliability through Learning and Optimization	Spring 2020	Research Scientist, Facebook On-Device AI (ISPD 2020 Best Paper Award, Cadence Women in Technology Scholarship in 2018)
33. Mohamed Baker Alawieh	Machine Learning for VLSI Computer Aided Design	Fall 2020	Senior R&D Engineer, Synopsys (ISPD 2020 Best Paper Award)

POST-DOC SUPERVISIONS COMPLETED:

1. Arman Roohi (postdoc 08/2019 - 07/2020), Assistant Professor at Department of Computer Science and Engineering, University of Nebraska - Lincoln
2. Shaolan Li (postdoc 06/2018 - 07/2019), Assistant Professor at Department of Electrical and Computer Engineering, Georgia Institute of Technology
3. Yibo Lin (postdoc 06/2018 - 06/2019), Assistant Professor at Department of Computer Science and Center for Energy-Efficient Computing and Applications (CECA), Peking University
4. Bei Yu (postdoc 08/2014 - 07/2015), Assistant Professor at Department of Computer Science and Engineering, Chinese University of Hong Kong

M.S. SUPERVISIONS COMPLETED (with Thesis or Report):

1. Jun Liu, August 2005
2. Andy Havlir, December 2005
3. Emiliano Lozano, May 2008
4. Varsha Dadlani, May 2008
5. Duo Ding, May 2008
6. Ashutosh Chakraborty, May 2008
7. Sean Xiaokang Shi, December 2008
8. Katrina Lu, December 2008
9. Tony Quan, August 2009
10. Anurag Kumar, December 2009
11. Boyang Zhang, May 2012
12. Wen Zhang, August 2012
13. Jagmohan Singh, August 2013

BS and REU Alumni:

- Joshua Gnanayutham
- Saanika Kenkare

- Rohan Tanna
- Miranda M. Pacheco
- August Shi
- Michael Booker
- Doug Ilijev
- Marc Anthony Gonzalez (B.S. 2011)
- Dhruv Mehrotra (B.S. in Jan. 2004)

Visiting Scholars/Students Alumni:

- Tung-Chieh Chen (National Taiwan University, Taiwan), Jan. – Dec. 2007
- Shanhu Shen (Zhejiang University, China), Sept. 2007 to Aug. 2008
- Ou He (Tsinghua University, China), October 2009 – October 2010
- Yen-Hung Lin (National Chiao Tung University, Taiwan), Mar. to Dec. 2011 (now TSMC)
- Prof. Weifeng Lv (Hangzhou Dianzi University, China), Sept. 2013 – Feb. 2014
- Dr. Junhyung Um (Samsung Electronics Principal Engineer), Jan. to Dec. 2014
- Wei Ye (Zhejiang University), Internship, July to Dec. 2014
- Dr. Tetsuaki Matsunawa (Toshiba), Oct. 2013 – April, 2015
- Vinícius dos Santos Livramento (Federal University of Santa Catarina, Brazil), Jan. 2016 – June 2016
- Taiki Kimura (Toshiba, Japan), May 2015 – October 2016
- Prof. Ronghua Jiang (Sichuan University, China), March 2016 – March 2017
- Zhijian Pan (Tsinghua University), Oct. 2016 - April 2017
- Prof. Jun Liu (Hefei University of Technology), Sept. 2016 – Aug. 2017
- Jun Zhang (Nanjing University of Posts & Telecommunications), Nov. 2016 - Oct. 2017
- Prof. Peiyong Zhang (Zhejiang University), Dec. 2016-Dec. 2017
- Prof. Hui Xu (Anhui University of Science & Technology), Oct. 2017 – Sept. 2018
- Prof. Zhiguo Yu (Jiangnan University), Dec. 2017 – Dec. 2018
- Meng Liu (Institute of Automation, Chinese Academy of Sciences), Feb. 2018-Nov. 2018
- Ying Chen (Institute of Microelectronics, Chinese Academy of Sciences), Oct. 2017 – March 2019
- Prof. Kun Ren, Hangzhou Dianzi University, Oct. 2018 to Sept. 2019
- Prof. Wei Hu, Xidian University, Dec. 2018 to Dec. 2019
- Prof. Wooyoung Jang, Dankook University, Jan. 2019 to Feb. 2020
- Jing Chen (NJUPT), July 2018 – September 2020
- Prof. Jae-Joon Kim, Pohang University of Science and Technology, Sept. 2019 to Aug. 2020

David Z. Pan's IEEE Biography:

David Z. Pan (S'97–M'00–SM'06–F'14) received his B.S. degree from Peking University, and his M.S. and Ph.D. degrees from University of California, Los Angeles (UCLA). From 2000 to 2003, he was a Research Staff Member with IBM T. J. Watson Research Center. He is currently a Professor and holder of the Silicon Laboratories Endowed Chair in Electrical Engineering at The University of Texas at Austin. His research interests include electronic design automation, design for manufacturing, machine learning and hardware acceleration, design/CAD for analog/mixed signal designs and emerging technologies. He has published over 400 journal articles and refereed conference papers, and is the holder of 8 U.S. patents. He has graduated 37 PhD/postdocs who are holding key academic and industry positions.

He has served as a Senior Associate Editor for ACM Transactions on Design Automation of Electronic Systems (TODAES), an Associate Editor for IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), IEEE Transactions on Very Large Scale Integration Systems (TVLSI), IEEE Transactions on Circuits and Systems PART I (TCAS-I), IEEE Transactions on Circuits and Systems PART II (TCAS-II), IEEE Design & Test, Science China Information Sciences, Journal of Computer Science and Technology, IEEE CAS Society Newsletter, etc. He has served in the Executive and Program Committees

of many major conferences. He is the ISPD 2008 General Chair, DAC 2014 Tutorial Chair, ASP-DAC 2017 Program Chair, ICCAD 2018 Program Chair, and ICCAD 2019 General Chair.

He has received a number of prestigious awards for his research contributions, including the SRC Technical Excellence Award in 2013, DAC Top 10 Author in Fifth Decade, DAC Prolific Author Award, ASP-DAC Frequently Cited Author Award, ASP-DAC Prolific Author Award, 19 Best Paper Awards at premier venues (ISPD 2020, ASP-DAC 2020, DAC 2019, GLSVLSI 2018, VLSI Integration 2018, HOST 2017, SPIE 2016, ISPD 2014, ICCAD 2013, ASP-DAC 2012, ISPD 2011, IBM Research 2010 Pat Goldberg Memorial Best Paper Award, ASP-DAC 2010, DATE 2009, ICICDT 2009, SRC Techcon in 1998, 2007, 2012 and 2015) and 16 additional Best Paper Award finalists, Communications of the ACM Research Highlights (2014), ACM/SIGDA Outstanding New Faculty Award (2005), NSF CAREER Award (2007), SRC Inventor Recognition Award three times, IBM Faculty Award four times, UCLA Engineering Distinguished Young Alumnus Award (2009), UT Austin RAISE Faculty Excellence Award (2014), Cadence Academic Collaboration Award (2019), and many international CAD contest awards, among others. His students have also won many awards, including the First Place of ACM Student Research Competition Grand Finals in 2018, ACM/SIGDA Student Research Competition Gold Medal (thrice), ACM Outstanding PhD Dissertation in EDA (twice), EDAA Outstanding Dissertation Award (twice), and so on. He is a Fellow of IEEE and SPIE.