IP-Camera

Product Requirements Strawman Design & Development Plan

[Draft Version 0.1]

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1. Overview

1.1 SCOPE

This document serves two purposes:

- To outline the requirements for an IP-based network camera that can provide surveillance functions with audio/video streaming capabilities over the Internet.
- To provide a Strawman design for the IP-camera under discussion with a draft development plan that can be used to materialize the project and assess the scope of the effort.

1.2 Acronyms & Definitions

1xEV-DO	1xEvolution-Data Only
1xRTT	1xRadio Telephone Technology
3xRTT	3xRadio Telephone Technology
AAC	Advanced Audio Coding
AGC	Automatic Gain Control
AMR	Adaptive Multi Rate
ARP	Address Resolution Protocol
BOOTP	Bootstrap Protocol
CCD	Charge-Coupled Device
CDMA	Code Division Multiple Access
CELP	Code Excited Linear Prediction voice compression
CHAP	Challenge-Handshake Authentication Protocol
CIF	CIF Resolution = 352x288
CMOS	Complementary Metal-Oxide Semiconductor
DHCP	Dynamic Host Configuration Protocol
EDGE	Enhanced Data Rates for GSM Evolution
EFR	Enhanced Full Rate = ACELP 12.2 Kbps
EVRC	Enhanced Variable Rate Codec
FDD	Frequency Division Duplex
FR	Full Rate = RPE-LTP 13 Kbps
FTP	File Transfer Protocol
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
HR	Half Rate = VSELP 5.6 kbps
HSCSD	High Speed Circuit Switched Data
HTTP	HyperText Transfer Protocol
IP	Internet Protocol
IS-95-A	CDMAOne System
IS-95-B	CDMAOne System
ISDN	Integrated Services Digital Network
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PPP	Point-to-Point Protocol
QCIF	Quarter CIF Resolution = 176x144
QQCIF	Quarter QCIF Resolution = 88x72
QQQVGA	Quarter QQVGA Resolution = 80x60
QQVGA	Quarter VGA Resolution = 160x120
QSIF	Quarter SIF Resolution = 176x120
QSVGA	Quarter SVGA Resolution = 400x300
QVGA	QVGA Resolution = 320x240

RTCP	Real Time Control Protocol
RTP	Real Time Protocol
RTSP	Real Time Streaming Protocol
SDP	Session Description Protocol
SIF	Source Input Format Resolution = 352x240
SMTP	Simple Mail Transfer Protocol
SQCIF	Sub-QCIF Resolution = 176x144
SVGA	Super VGA Resolution = 800x600
SXGA	Super XGA Resolution = 1280x1024
TCP	Transmission Control Protocol
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division Synchronous CDMA
UDP	User Datagram Protocol
UXGA	Ultra XGA Resolution = 1600x1200
VGA	VGA Resolution = 640x480
W-CDMA	Wideband CDMA
XGA	XGA Resolution = 1024x768

2. Product Concept & Requirements

2.1 Product Concept – The Big Picture

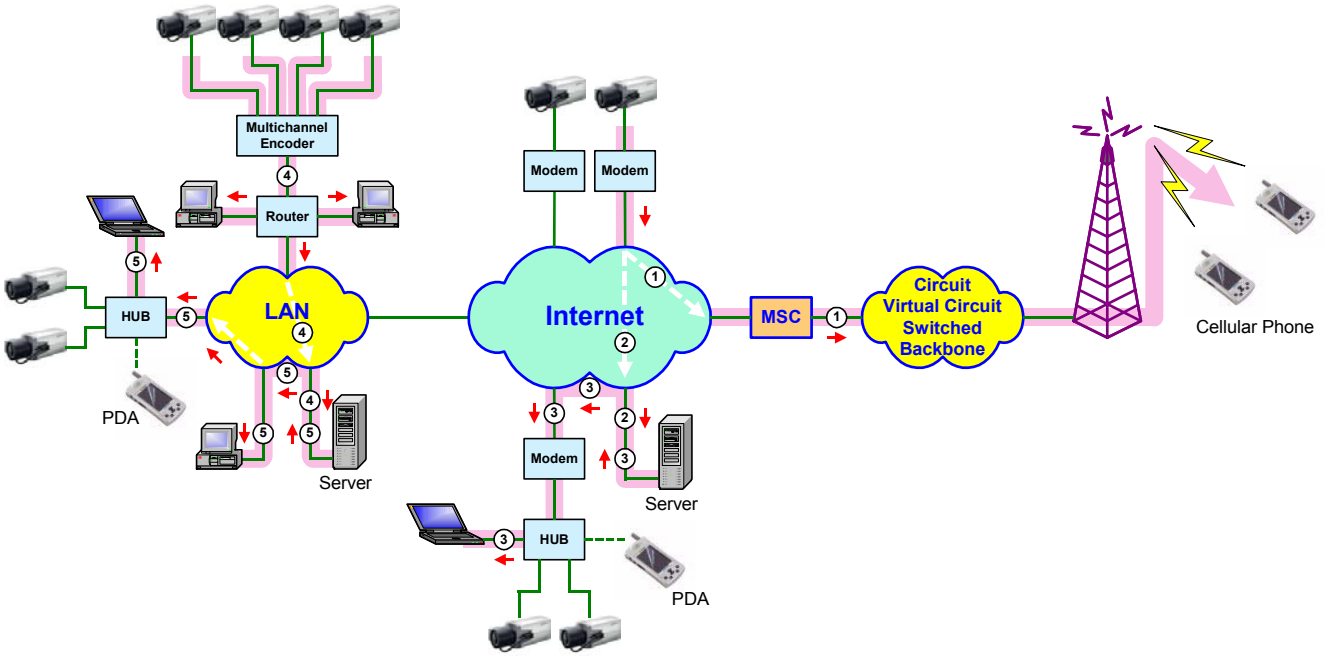


Figure 1 Product Concept – The Big Picture

Examples of the data flow:

Scenario ① An IP-Camera captures real-time video and sends it to a cellular phone via the Internet and the cellular wireless network after an event-triggered alarm message was sent. Note that the available video transmission bandwidth for the wireless network is limited and is technology dependent. See Appenidx A for the limitation.

Scenario ② An IP-Camera captures real-time video and stores it to a remote video server via the Internet.

Scenario ③ A remote laptop computer retrieves the video from the video server via the Internet.

Scenario ④ Multiple IP-cameras are capturing muiple real-time video streams through a multichannel video encoder. Two computers (shown as in Figure 1) are monitoring the videos simultaneously. The coded video streams are stored to a remote video server via the Internet.

Scenario ⑤ Two remote computers (shown as in Figure 1) later retrieve the videos from the video server via the Internet.

2.2 Summary

This section summarizes the general requirement for the IP-camera and its major functionalities. Target applications and competitions will also be mentioned briefly.

General Requirements:

- Initial product is IP-based digital video surveillance camera.
- Follow-on product to include remote wireless, mobile and wearable video variants with additional features such as license plate recognition and object tracking.
- A rapid follow-on to support 802.11 a/b/g.
- Support of a 10/100 Base-T wired Ethernet interface.
- Target unit cost (BOM) < $150.
- Real-time, full-rate (up to 30 fps) network streaming of MPEG-4 compressed video up to D1 resolutions (720x480) with migration to highend H.264 video encode.
- CMOS sensors to reduce cost.
- For surveillance market, where image clarity and detail are typically more critical than frame rate, use CCD sensors at reduced frame rates.
- Surveillance specific capabilities including: user access control, encryption, configurable motion detection, external alarm triggers, pan-tilt-zoom control (up/down/left/right), pre-event video capture, and remote A/V codec configuration.
- A comprehensive well documented API and reliance upon industry standard formats and protocols to simplify third-party and OEM integrations.
- Support for remote software updates and system management.
- Embedded OS.
- Multi-voice speech encodes.

Client SW Support:

- Video Monitoring & Recording.

Configuration & Control

- Add new camera(s).
- Auto connect/Record/De-blocking/De-ringing.
- Encoder frame rate/bitrate configuration.
- Pre-recording
- Channel enable/disable
- Camera configuration setup
- Remote firmware upgrade
- Remote status monitoring
- Address book function
- Dynamic IP setup (DDNS & MAC address)
- Video buffering
- Motion area control
- Auto detection control
- Camera light control
- Sensor control
- Transmission mode control
- Camera speed control

Pan/Tilt/Zoom Control

- Remote control

Variable Backup & Player Control

- Remote control

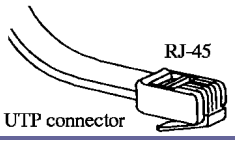
Target Applications:

- Digital video surveillance.
- Video streaming encode and transcode tasks.
- Remote site monitoring (e.g., oil field equipment, water supplies, electricity distribution stations, etc.)
- Mobile monitoring (cell-modem based).
- Video recording of public and commercial transportation.
- Wearable cameras with wireless streaming to monitor stations
- Counting applications (people entering a mall, for example).

2.3 Feature Requirements Details

This section outlines the desired product features and requirements details.

Table 1 Feature Requirements Details

Feature	Requirements	Remarks
Image Sensor	- 2/5" or better CMOS Sensor, e.g., OmniVision OV8610, Fujitsu MB86S10	
Resolution	- Up to SVGA resolution (800x600) - Digital Zoom	See Appendix B for the Encoder Requirement Analysis.
Exposure	- Backlight compensation - Automatic AGC - White Balance: Automatic and preset to Fixed Indoor, Fixed Fluorescent, Fixed Outdoor, and Hold - Shortest exposure time: 1/30, 000 s - Longest exposure time: 0.7 s	
Sensitivity	- Max illumination: 10,000 LUX - Min illumination: 3 LUX	
Image/Video	- Max frame rate = 30 fps - JPEG still images - MJPEG video encode - MPEG-4 video encode (Low-end) - H.264 video encode (High-end) - 5-level compression: High, Medium, Low, Lowest, None	
Audio (8 KHz, mono)	- G.726 (16/32 Kbps) - G.729 (8 Kbps) - G.723 (5.3/6.3 Kbps) - MPEG AAC (Variable rate)	
Microcontroller SOC	TI OMAP1612	- ARM926 CPU core at 204 MHz - TMS320C55x DSP core at 204 MHz - Built-in security - USB 1.1 host/client - 100 MHz memory interface - Support of 128-256 MB DDR SDRAM - Support of.128-256 MB SDR SDRAM
Media Processor (High-end)	TI DM642	- DSP core at 480 MHz or 4800 MIPS.
Memory	- 16 MBytes SDRAM - 8/16 MBytes Flash	
Network I/F (One or two)	10/100 Base T Ethernet port	Unshielded Twisted Pair (UTP) cable via a RJ45 connector. 
Network Protocols	Supports TCP/IP, HTTP, FTP, SMTP, NTP, PPP, ARP, BOOTP, CHAP, PAP, Telnet	- All transportation of data is done through HTTP, RTP (based on UDP), or FTP. - Alerts can be sent as an e-mail using SMTP. - Telnet can be used for remote terminal debug.

Feature	Requirements	Remarks
Streaming Protocols	RTP, RTCP, RTSP, SDP	-
Serial Port	9-pin serial port	- Connect a modem or ISDN terminal adaptors to allow the camera to be accessed via a PPP dial-up connection to an ISP over a modem link. - RS-232 modem connector for dial-up use. - Support of most V90 modems.
I/O connector		Four-pole terminal block provides 24-volt power supply to drive other devices through a relay and digital input/output connectors, which allow external switches to be connected for event-driven applications (such as a door sensor with a solenoid, event triggered remote image storage via e-mail and FTP, sending an e-mail in case of an alert.).
Power Supply	External power unit supply	12V AC included. Consumes max 7W.
OS	Embedded Linux with TCP/IP, UDP, FTP, Telnet, and Web Server	Advantages running Linux: - Well-known, well-documented, and reliable. - Easy to employ new developers. - Small footprint, take less flash or RAM memory. - Decentralized, many companies can benefit from. - Much functionality available for free. - Source code freely available to everyone. - Developed under the GNU General Public License. - Faster and easier development for future OEMs.
Web Server	Built-in Web server (Internet Explorer 4.x, 5.x, 6.x, or Netscape Navigator 4.x on the client side)	- Use camera's URL to access the images. - A snapshot or video stream is triggered by the request from the browser (using camera's URL). - For motion video, use the "server push" technology, which is only available in Netscape. (To be validated.) - For MS IE, use the ActiveX component that is packaged in the product. (To be validated.) - Secured like any other Internet host.
Built-in FTP server.		
Built-in FTP client.		
Built-in e-mail client.		On the client side.
Needs an IP address		- Searches the network for "Sequent" MAC address. - Assigns a chosen IP address to the camera. - Camera then can be accessed directly using a standard Web browser. - Support of DHCP.
Streaming video		
Motion detection	Image Recognition or Ultrasound	
Alarm inputs/outputs		
Relay output		

Feature	Requirements	Remarks
Analog video output	PAL, NTSC	
e-mail support		

3. A Strawman Design

3.1 System Architecture Block Diagram – Low End

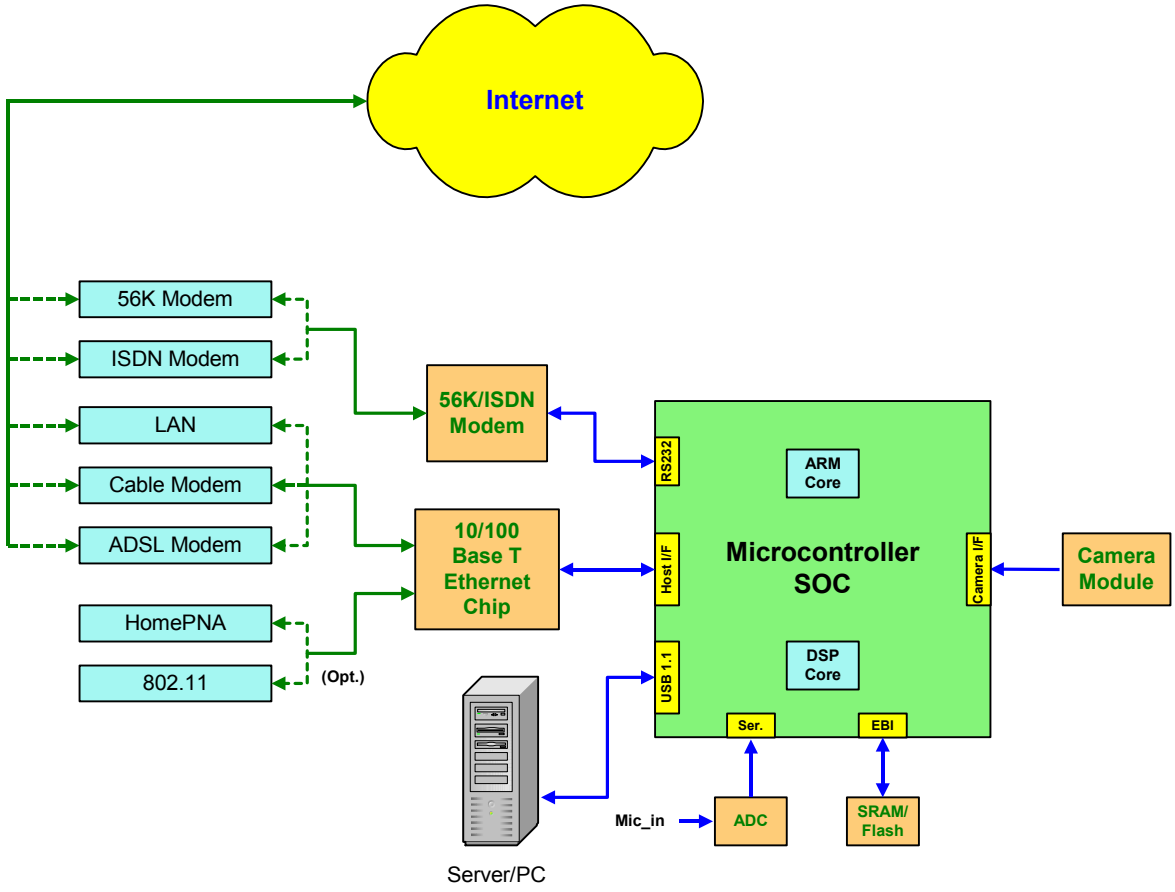


Figure 2 System Architecture Block Diagram – Low End

3.2 System Architecture Block Diagram – High End

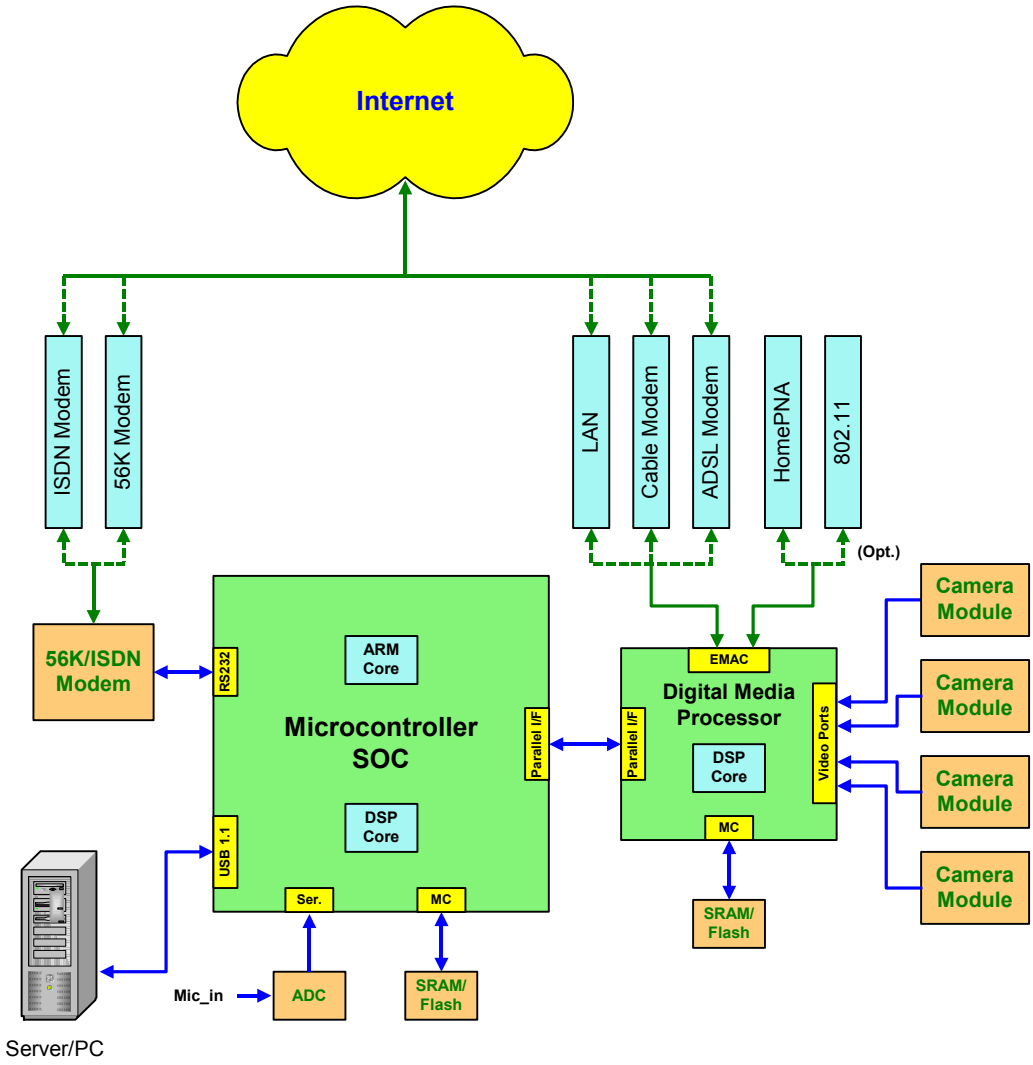


Figure 3 System Architecture Block Diagram – High End

3.3 Software Architecture Block Diagram

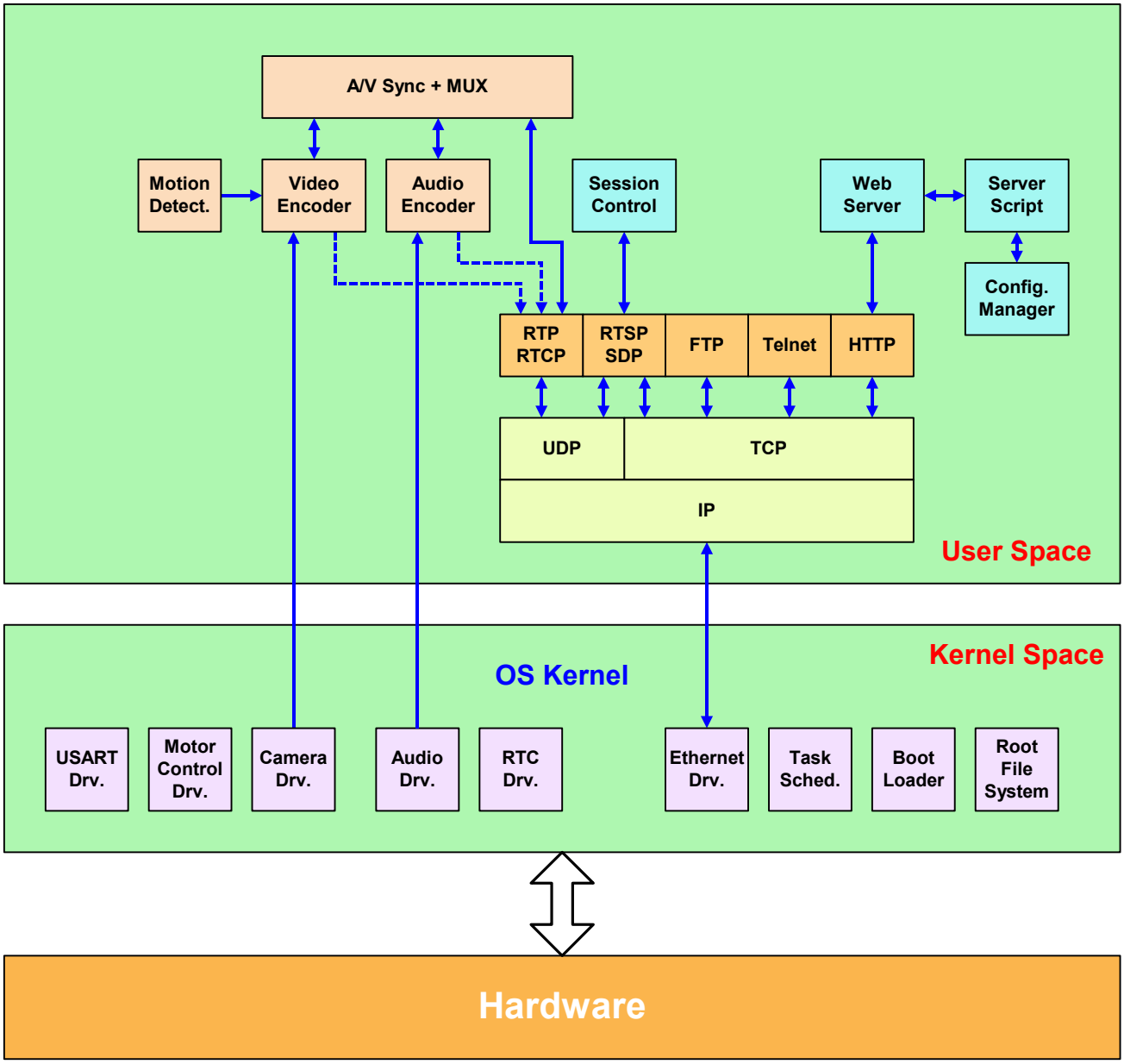


Figure 4 Software Architecture Block Diagram

4. Software Tasks

4.1 Software System Tasks

Table 2 Software System Tasks

Component	Description	Target Platform	Development Effort Estimation
Embedded OS	Embedded Linux Supporting Networking Protocol Stacks	ARM926	Free
System Utilities	Timers, Monitors, Powers	ARM926	Linux Built-in
Streaming Protocols	• RTP • RTCP • RTSP • SDP • Session Control	ARM926	Supported by Business Partner
IRQ Service	Interrupt Service Routines	ARM926	Internal Development
Video/Image Encoder	• MJPEG • MPEG-4 Simple Profile • H.264 • JPEG	• ARM926 (Low-End) • DM642 (High-End)	• No HW Acceleration • MPEG-4 & H.264: To be Supported by Business Partner • MJPEG: Internal Development
Audio Encoder	• G.726 (16/32 Kbps) • G.729 (8 Kbps) • G.723 (5.3/6.3 Kbps) • AAC	OMPA1612 DSP	Internal Development
Video System Module	System-Level Elementary Video Bitstream	• ARM926 (Low-End) • DM642 (High-End)	Supported by Business Partner or Internal Development
Audio System Module	System-Level Elementary Audio Bitstream	ARM926	Internal Development
A/V Sync + Mux	Audio/Video Combination and Synchronization.	ARM926	Internal Development
Motion Detection	Image Recognition or Ultrasound	ARM926	Internal Development
Drivers	See Section 4.2		Internal Development

4.2 Driver Tasks

4.2.1 Low-End Solution (MC/DSP)

Table 3 Low-End Diver Tasks

Drivers	Description	Target Platform	Development Effort Estimation (Low/Medium/High)
Camera Interface	Controls the operation for camera interface.	MC/DSP (ARM926 Based)	Low
Camera	Controls operation of a CMOS or CCD camera.	MC/DSP (ARM926 Based)	Medium
I^2C	Required for I^2C based camera.	MC/DSP (ARM926 Based)	Low. Need to customize a reference SW for SW based solution.
DMA	Controls the operations of DMA channels.	MC/DSP (ARM926 Based)	Medium
GPIO	Controls the operation of GPIO.	MC/DSP (ARM926 Based)	Low
Ethernet	Controls the operation of Ethernet chip.	MC/DSP (ARM926 Based)	Medium to High
Timer	Controls the operation of timer.	MC/DSP (ARM926 Based)	Low
RTC	Controls the operation of RTC.	MC/DSP (ARM926 Based)	Low
UART	Controls the operation of serial port.	MC/DSP (ARM926 Based)	Medium
USB	Controls the operation of USB.	MC/DSP (ARM926 Based)	High
Flash Memory	Controls the operation of flash file system.	MC/DSP (ARM926 Based)	Medium to High
Motor	Controls the operation of camera motor	MC/DSP (ARM926 Based)	Medium (Zero, if 3rd party code available)
Modem	Controls the operation of modem if supported.	MC/DSP (ARM926 Based)	Zero to Low

4.2.2 High-End Solution (MC+DSP+MP)

Table 4 High-End Driver Tasks

Drivers	Description	Target Platform	Development Effort Estimation (Low/Medium/High)
Camera	Controls operation of a CMOS or CCD camera.	MP	Medium
I^2C	Required for I^2C based camera.	MC/DSP (ARM926 Based)	Low. Need to customize a reference SW for SW based solution.
DMA	Controls the operations of DMA channels.	MP + MC/DSP (ARM926 Based)	Medium
GPIO	Controls the operation of GPIO.	MC and DSP if available.	Low
Ethernet	Controls the operation of Ethernet Port.	MP	Medium to High
Timer	Controls the operation of timer	MP + MC/DSP (ARM926 Based)	Low
RTC	Controls the operation of RTC.	MC/DSP (ARM926 Based)	Low
Serial Port	Controls the operation of serial port.	MP + MC/DSP (ARM926 Based)	Medium
Video port	Controls the operation of video I/O port.	MP	Medium
Audio Port	Controls the operation of audio port.	MC/DSP (ARM926 Based)	Medium
Flash Memory	Controls the operation of flash file system.	MP + MC/DSP (ARM926 Based)	Medium to High
Motor	Controls the operation of camera motor	MC/DSP (ARM926 Based)	Medium (Zero, if 3rd party code available)
Modem	Controls the operation of modem if supported.	MC/DSP (ARM926 Based)	Zero to Low

4.3 Applications

4.3.1 Embedded Network Camera Applications

Table 5 Embedded IP Camera Applications

Applications	Description	Target Platform	Development Effort Estimation
Basic Web Server	• Access control. • Camera configuration and control. • Video/image/audio encoding configuration and control. • Streaming.	MC/DSP (ARM926 Based)	Streaming protocols should be easy with reference SW available from internet. Never worked on server before. Reference SW might be available on the internet.
Video/Image Encoder	• Running MPEG/H26X encoder. • Running MJPEG/JPEG encoder.	MP – Highend MC/DSP - Lowend (ARM926 Based)	A lot of re-architect/optimization might be required even if a reference SW is available from the internet or MediaExcel.
Audio encoder	Running an audio encoder	MC/DSP (ARM926 Based)	A lot of re-architect/optimization might be required even if a reference SW is available from the internet or MediaExcel.
Video/Audio Mux	Multiplex encoded audio/video stream.	MC/DSP (ARM926 Based)	Depends on what kind of MUX to use. For video clips, we can use MP4. Some customization of reference SW is required.
Enhanced Web Server	Single/Multicasting.	MC/DSP (ARM926 Based)	
Web Client	FTP client.	MC/DSP (ARM926 Based)	

4.3.2 PC Client Applications

Table 6 PC Client Applications

Applications	Description	Target Platform	Development Effort
IE	Internet Explorer	PC	None
Decoder Plugin.	Required if the decoder is not supported by Windows Media Player or RealPlayer.	Laptop/Desktop PC	

4.4 Software Tools

"Code Composer Studio™ IDE" available from TI for the OMAP platform is required for this project. Code Composer Studio™ (CCStudio) Development Tools provide a fully integrated development environment (IDE) supporting Texas Instruments industry-leading TMS320™ DSP platforms. Code Composer Studio IDE is the first intelligent development environment to offer TMS320C2000, TMS320C5000, TMS320C6000, and OMAP application development for multi-processor, multi-user and multi-site projects.

CCStudio integrates all host and target tools in a unified environment -- including TI's DSP/BIOS™ kernel, code-generation tools, fast simulators, debugger, and Real-Time Data Exchange (RTDX) technology -- to simplify DSP system configuration and application design. CCStudio also has an open architecture that allows TI and third parties to extend the IDEs functionality by seamlessly plugging-in additional specialized tools.

Table 7 Code Composer Studio(TM) IDE for OMAP ™ Platform

Tool Name	Part Number	OS	Platform	Price
OMAP Code Composer Studio bundled with Annual Subscription	TMDSCCSOMAP-1	Win98/2000/XP/NT	OMAP™ Platform	$5400.35
OMAP Code Composer Studio Annual Subscription	TMDSSUBOMAP		OMAP™ Platform	$900.06

Table 7 lists the available OMAP CCStudio subscription information. For details, see the following website:

http://focus.ti.com/omap/docs/omapgenpage.tsp?navigationId=9306&templateId=5663&path=templatedata/cm/omaptools/data/ccs

For the high-end DM642-based product, the "C6000 Code Composer Studio™" software tool is also required.

5. Hardware System Tasks

5.1 System Development

Use the "Innovator™ Development Kit for the OMAP Platform" from TI for the code development and all necessary system level testing and verification. For a jump-start, the Innovator development system can be used as is initially. The camera module then needs to be replaced by the one that is planed for use by this project.

For the high-end DM642-based product, the Network Video Developer's Kit (NVDK) for developing video and imaging applications with required network connectivity is required.

5.2 Reference Board

Details to be provided later. The reference board will result in a prototype machine that is to be delivered with all the software components.

5.3 System Integration & Verification

This effort includes the system integration on the development system as well as on the prototype machine. A detailed document shall be provided to guide the entire effort.

5.4 Hardware Tool – The Innovator™ Development Kit

Features and Benefits:

- Handheld, battery-operated small form factor for a compelling demonstration platform.
- Single development platform supporting multiple operating systems; support for the following operating systems is planned: Linux®, Microsoft® Windows® CE, Palm OS™, Symbian OS™, Java™ and others.
- Includes OMAP1510 processor for maximum performance and power efficiency. Also supports development for the OMAP5910 and OMAP710 processors.
- Expansion boards are planned to support multiple wireless standards including GSM/GPRS, 802.11 and Bluetooth™.
- Modular hardware approach for maximum design flexibility: user interface module, processor module, and expansion module.

Table 8 Innovator™ Development Kit Specification

Module Name	Specification
Hardware: User Interface Module	• LCD/Touch screen/CCFL front light • 4-wire touch screen controller • Dual RS232 port interfaces • Voice connectors, stereo amplifier, and dual speakers • Power and up/down/select buttons • USB host and client ports • Two serial ports
Hardware: Processor Module	• OMAP1510 processor • 32MB SDRAM • 32MB Flash • SD/MMC expansion slot • JTAG accessible
Hardware: Expansion Module	• IRDA • Stereo inpu
Hardware: Break-out Board	• 10 Mb Ethernet • PS2 keyboard port • PS2 mouse port
Hardware: Enclosure	• with 1100mAH battery and charger
Software:	• Operating system options • Startup diagnostic application
Documentation:	• User Guide • Software documentation
Accessories: (included)	• Serial port dongle

Module Name	Specification
	• Stereo headphones • Earpiece/microphone • 2 Stylus • Plexiglas stand • Ethernet cable • PS2 touch pad mouse/keyboard • Digital camera

6. Summary of Required Tools from TI

6.1 OMAP Tools

Hardware Tools:

The Innovator™ Development Kit for OMAP
- Required for system emulation, software development, and early demo.

XDS560 Emulator
- Required for real-time hardware/software debugging through JTAG.
- Used for prototype development, driver development, and system integration.

Software Tools:

TI C55X DSP – Code Composer Studio™
- With C Compiler, Assembler, Linker, Debugger, and IDE (Integrated Development Environment).

ARM926EJ -
- With GNU C Compiler and Debugger.

Operating System:

GNU Linux Version 2.4
- With Debugger, Trace Tools, and Compilers.
- MontaVista Linux Tools

6.2 DM642 Tools

Hardware Tools:

DM642 Emulation Module
XDS560 Emulator
Network Video Developer's Kit (NVDK)

Software Tools:

C6000 Code Composer Studio™

Operating System:

DSP/BIOS

7. Development Plan

7.1 Resource Requirements

Table 9 Resource Requirements & Major Responsibilities

Type	Number	Major Responsibilities
Project Lead	1	• Lead the entire design. • Provide technical guidance to the design team. • Monitor the milestones and the project progress. • Provide resource management. • Provide consultation to the management. • Perform the operation on the day-to-day basis. • Deliver the product in time.
Hardware Engineer	1	• Lead all the hardware design activities. • Perform system integration at the hardware level. • Take the initiative in directing the hardware design. • Proactively involved in solving engineering issues. • Provide assistance to other teammates. • Provide necessary documentation.
System Software Engineer	1	• Lead all the system software design activities. • Perform system integration at the software level. • Take the initiative in directing the software design. • Proactively involved in solving engineering issues. • Provide assistance to other teammates. • Provide necessary documentation.
Application Software Engineer	2	• Lead all the application software design activities. • Perform system integration at the application level. • Take the initiative in directing the application design. • Proactively involved in solving engineering issues. • Provide assistance to other teammates. • Provide necessary documentation.
Total	5	

7.2 Product Development Phases

7.2.1 Product Concept and Study Phase

A product concept for the IP-camera is to be created during this phase. Aspects in regarding to market demand, competition, resource constraints, time-to-market, and leverageable in-housed solutions need to be factored into the design consideration.

7.2.2 Specification Phase

Design specifications and other documentations need to be generated at the early stage of the product development cycle. They need to be maintained and updated as the project moves forward. Tools acquition should also be initiated during this phase. Table 10 summarizes those major documents that need to be created immediately. Design/Implementation specifications are not listed in Table 10. However, they need to be included in the master schedule once the project is kicked off.

Table 10 Major Documentations

Name	Description
Project Schedule	A detailed development schedule lists all the tasks, which cover the start dates, completion dates, and the inter-depencies among all the tasks. Milestones and checkpoints need to be identified in this document.
Hardware Architecture Specification	This document outlines the components/parts, suppliers, pricing, designs, integration, testing, and verification strategies.
System Architecture Specification	This document specifies the system architecture at the block level. All necessary data flow paths (e.g., audio/video) should be addressed. Necessary performance analysis, memory/bandwidth analysis should also be provided.
Software Architecture Specification	This document defines the overall software architecture including system controls, operating modes, OS specific functional operation, software components/modules, and application scenarios.
Driver Architecture Specification	This document defines the driver architecture inline with the underlying OS. Code portability for platform migration needs to be considered when defining the architecture.
Camera API Specification	Camera API needs to be defined to be compatible with the industry standard. The interface will not only be used for in-house test application development but also be used by 3rd party vendors for system integration.
A/V Codec API Specification	A/V Codec API needs to be defined to be compatible with the industry standard. The interface will not only be used for in-house test application development but also be used by 3rd party vendors for system integration.

7.2.3 Hardware Design Phase

Major tasks encompass the validation of the TI develompent kit, components investigation/acquisition, reference prototype board design, …, etc.

7.2.4 Code Development Phase

All code development will be executed during this phase. Code design and peer-reviews will also be conducted. Typical code development methodology will be enforced to ensure the quality of the code.

7.2.5 Integration & Verification Phase

Integrate all high-level software components on TI evaluation platform to demonstrate the capabilities of the IP-Camera system. Resolve all issues related to the system design and software implementations.

7.2.6 Product Prototyp Phase

Following actions will be conducted during this phase:

- Debug the prototype board (the evaluation system) to make sure all hardware devices are functioning as desired.
- Port Embedded Lynux to the prototype board and make sure the OS can be brought up properly.
- Debug all the device drivers and resolve any issues occurred during the debugging.
- Integrate all high-level software components and demonstrate the capabilities of the IP-Camera on the prototype board.
- Conduct thorough functional verifications and reliabilities tests.

7.2.7 End-Product Form Factor Dseign

(Out source)

7.3 Tentative Schedule

Table 11 Tentative Schedule

Phase	Man-Month (MM)
Product Concept and Study Phase	2 MM (Started already)
Specification Phase	2 MM
Hardware Design Phase	2 MM
Code Development Phase	20 MM
Integration & Verification Phase	20 MM
Product Prototype Phase	16 MM
End-product form factor dseign	(Out source)

8. Critical Success Factors

Table 12 Critical Success Factors

Area of Dependency	Description	Risk Factor (Low/Medium/High)
Tools Support	Support required from TI, camera vendors (such as OmniVision etc.), and other chip vendors	High
Parts, Supplies, Boards	All hardware components and the board layout etc.	Medium
OS System Support	Embedded Linux	Low
Codec Optimization	Codecs from business partners may not be optimized to our platforms.	Low
Network/Streaming Protocols	Support of Network/Streaming Protocols from business partner(s) or suppliers (such as TI) may need to be modified and optimized for our design.	Medium
New Development Tools	Learning curve involved.	Low

Appendix

A Wireless Technologies

This Appendix is for information only. To support video streaming to a wireless cellular handset, the available data rate is severely limited by the underlying carrier. See following subsections for the comparison.

A.1 Bitrates for Various Wireless Technologies

Table 13 Bitrates for Various Wireless Technologies

Technology Name	Year of Introduction	Access Technology	Speech Codec	Maximum Data Rate	Switching Technology
GSM	1992	TDMA	FR, EFR, HR	9.6 Kbps (14.4 Kbps option)	Circuit Switched
GPRS	2001-2002	TDMA	Not Applicable	Depends on Coding Scheme (CS) and # of Timeslots Used (1 up to 8 Slots): CS1: 9.05 Kbps/TS[1] CS2: 13.4 Kbps/TS CS3: 15.6 Kbps/TS CS4: 21.6 Kbps/TS	Packet Switched
HSCSD	2000	TDMA	Not Applicable	Depends on # of Timeslots Used (1 up to 8 Slots): 9.6 Kbps or 14.4 Kbps per Timeslot	Circuit Switched
EDGE	2001-2002	TDMA	Not Applicable	Up to 384 Kbps	Circuit Switched & Packet Switched for EGPRS
IS-95-A	1995-1997	CDMA	8 Kbps var. rate CELP; or 13 Kbps var. rate CELP; or 8 Kbps var. rate EVRC	9.6 Kbps or 14.4 Kbps	Circuit Switched
IS-95-B	1995-1997	CDMA	8 Kbps var. rate CELP; or 13 Kbps var. rate CELP; or 8 Kbps var. rate EVRC	Up to 64 Kbps	Circuit Switched & Packet Switched
CDMA2000 (1xRTT)	Mar. 2001 (Korea First, Then USA &	CDMA	8 Kbps var. rate CELP; or 13 Kbps var. rate	Up to 307.2 Kbps	Circuit Switched & Packet

[1] TS = Timeslot

Technology Name	Year of Introduction	Access Technology	Speech Codec	Maximum Data Rate	Switching Technology
	Japan)		CELP; or 8 Kbps var. rate EVRC		Switched
1xEV-DO	2001-2002	CDMA	Not Applicable	Up to 2.5 Mbps Downlink; Up to 307 Kbps Uplink	Packet Switched
CDMA2000 (3xRTT)	(No Plan Yet)	CDMA	8 Kbps var. rate CELP; or 13 Kbps var. rate CELP; or 8 Kbps var. rate EVRC	Up to 1 Mbps (Up to 2 Mbps Indoor)	Circuit Switched & Packet Switched
W-CDMA (FDD)	2001 (Early Trial Systems)	CDMA	AMR	Up to 384 Kbps (Up to 2 Mbps Indoor)	Circuit Switched & Packet Switched
W-CDMA (TDD)	2003 or Later	TDMA/ CDMA	AMR	Up to 384 Kbps (Up to 2 Mbps Indoor)	Circuit Switched & Packet Switched
W-CDMA (Low Chip Rate[2] TDD)	2003 or Later	TDMA/ CDMA	AMR	Up to 384 Kbps	Circuit Switched & Packet Switched
TD-SCDMA	2003 or Later	TDMA/ CDMA	EFR	Up to 384 Kbps (Phase 1) 2 Mbps (Phase 2)	Circuit Switched & Packet Switched

[2] 1.28 Mcps

A.2 GPRS Multislot Classes

Multislot classes are product dependant, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as (for example) 3+1 or 2+2, the first number indicates the amount of downlink timeslots (what the mobile phone is able to receive from the network). The second number indicates the amount of uplink timeslots (how many timeslots the mobile phone is able to transmit). The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

Table 14 GPRS MultiClasses

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5

A.3 GPRS Multislot Class Examples

Table 15 GPRS Multislot Class Examples

GPRS Class	Downlink		Uplink		Vendors
	# Slots	Bitrate	# Slots	Bitrate	
Class 2	2	16-24 Kbps	1	8-12Kbps	Mororola Accompli A008 Trium Mondo, Sirius
Class 4	3	24-36Kbps	1	8-12Kbps	Motorola TimeportT260
Class 6	3	24-36Kbps	2	16-24Kbps	Nokia 6310, 6510, 8310
	2	16-24Kbps	3	24-36Kbps	
Class 8	4	32-48Kbps	1	8-12Kbps	Ericsson T39, R520 Motorola v60i, v66i Samsung Q200, S100 Siemens S45, ME45, M50 Trium Eclipse
Class 10	4	32-48Kbps	1	8-12Kbps	Philips Fisio 820
	3	24-36Kbps	2	16-24Kbps	
Class 12	4	32-48Kbps	1	8-12Kbps	Sierra Wireless Aircard 750 GSM/GPRS PC Card
	3	24-36Kbps	2	16-24Kbps	
	2	16-24Kbps	3	24-36Kbps	
	1	8-12Kbps	4	32-48Kbps	

B Encoder Requirement Analysis

B.1 ARM926 Only Solution

Typically, it takes an average of 4.5 MCycles to encode a P frame (QCIF size) with HW motion estimation for an ARM926 with a 16K I-Cache and a 16K D-Cache. If motion estimation is done in SW using 3-step search, it takes an average of 5.4 MCycles to do motion estimation for a single QCIF frame based on some prior estimation. Therefore, a total of 9.9 M cycles will be required to encode a QCIF frame, or 0.1 MCycles to encode a 16x16 Macroblock.

Based upon the 0.1M cycles/macroblock cycle count estimate, we can figure out the "estimated" maximum resolution that can be supported by a typical MPEG-4 encoder for a given frame rate on a 204MHz ARM926.

Table 16 Estimated Maximum Resolutions for ARM926 Only Solution

Frame Rate	Max Macroblocks /frame	Maximum frame size for 4:3 aspect ratio (except D1)
1.5	1350	720x480 (D1)
1.7	1200	640x480
10	204	264x198
15	136	216x162
20	102	186x140 (Close to QCIF)
30	68	152x114
60	34	108x81

As an illustration for the estimation: when the frame rate is at 10, each frame takes 20.4 Mcycles/s (204/10). So the maximum allowed MB per frame will be 20.4/0.1 = 204. 204 macroblocks for a 4:3 aspect ratio frames give us a frame size of 264x198.

B.2 C55X Only solution

Based on the benchmark result provided by TI's OMAP white paper SWPY006, the C55X DSP requires only 36% cycles of that required for ARM for encoding. Based on that assumption, we can figure out the "estimated" maximum resolution that can be supported by a typical MPEG-4 encoder for a given frame rate on a 204MHz ARM926.

Table 17 Estimated Maximum Resolutions for C55X Only Solution

Frame Rate	Max Macroblocks /frame	Maximum frame size for 4:3 aspect ratio (except D1)
4.2	1350	720x480 (D1)
4.7	1200	640x480
10	566	440x330
15	378	360x270(Close to CIF)
20	284	310x232
30	188	252x190
60	94	180x136

B.3 ARM926 + C55X Based Solution (OMAP)

Since C55X DSP requires only 36% cycles of that required by the ARM, a 204Mhz ARM core is equivalent to a 73MHz CX55 core (= 204x36%) for the encoding. So the total processing power normalized to CX55 is 277. Based on that assumption, we can figure out the maximum resolution that can be supported by encoder for a given frame rate on the OMAP.

Table 18 Estimated Maximum Resolutions for ARM926 + C55X Based Solution

Frame Rate	Max Macroblocks /frame	Maximum frame size for 4:3 aspect ratio (except D1)
5.6	1350	720x480 (D1)
6.3	1200	640x480
10	760	510x382
15	508	418x312
20	382	360x270(Close to CIF)
30	252	292x220
60	126	208x158

B.4 DM642 Based Solution

Based on TI's white paper on H.263 profile 3 (which is very close to MPEG-4 simple profile) implementation on C6000 (SPRA018), 205 CIF frames can be encoded in one second on C6415 at 600Mhz. Since DM642 and C6415 use the same CPU core, the encoding cycle counts on DM642 and C6415 should be very close to each other.

Table 19 Estimated Maximum Resolutions for DM642 Based Solution

Frame Rate	Max Macroblocks /frame	Maximum frame size for 4:3 aspect ratio (except D1)
60	1350	720x480
67	1200	640x480
10	8118	1664x1248
15	5412	1360x1020
20	4059	1176x882
30	2706	962x722
205	396	352x288
820	99	176x144

As an illustration for the estimation: a CIF frame has 396 MBs, so DM642 can decoder 81180 (396x205) macroblocks per second. For D1 resolution, this is equivalent to 60 frames per second (81180/1350).

C CMOS Imagers

C.1 CMOS Imagers Comparison

Table 20 CMOS Imagers Comparison

Camera Vendor	Model	Max Resol. / Max FPS	Supported Resolutions	JPEG Encode	Interface
Agilent	ADCM-2650/2670 (Module)	VGA / 31	VGA, CIF, QVGA, QCIF, QQVGA, QQCIF, Any < VGA	Yes	CCIR656 UART (2670) / Parallel (2650) for JPEG
	ADCM-1700 (Module)	CIF/ Prog.	CIF, QVGA, QCIF, QQVGA, QQCIF, QQQVGA	No	CCIR656
	ADCM-1650 (Module)	CIF / 15	CIF, QVGA, QCIF, QQVGA, QQCIF, any ≤ 352x352	Yes	CCIR656, Serial/Parallel for JPEG
	HDCP-2010 (Image Processor)	VGA / 30 CIF / 80		Yes	YUV 4:4:4, 4:2:2 Serial/Parallel for JPEG
	HDCS-1020 (Sensor)	CIF / 30		No	Internal
	HDCS-2020 (Sensor)	VGA / 15		No	Internal
Core Logic	CLC340 (Image Processor) supported sensors: Hynix HV7121CP1, OmniVision OV6645/6630	CIF / 30	CIF, QCIF	Yes	CCIR 601 UART for JPEG (Max 230.4 Kbps)
Fujitsu	MB86S10	SXGA / ?	SXGA ~ QQCIF	No	8-bit YCbCr 4:2:2 8-bit YUV 4:2:2 16-bit RGB 5:6:5
Hitachi	HAM49001 (Module)	CIF / 15	Programmable	No	YUV 4:2:2
Hynix	HV7121GP (Integrated[3])	CIF /30	CIF, QCIF, QVGA, QQVGA	No	YcbCr 4:2:2 YcbCr 4:4:4 RGB 4:4:4 Bayer
	HV7131GP (Integrated)	VGA / 30	VGA, QVGA, QQVGA	No	YcbCr 4:2:2 YcbCr 4:4:4 RGB 4:4:4 Bayer

[3] Sensor and image processor are combined in a single chip.

Camera Vendor	Model	Max Resol. / Max FPS	Supported Resolutions	JPEG Encode	Interface
	HV7141D (Sensor)	SVGA / Prog.	Programmable	No	Internal
	HV7131D (Sensor)	VGA / Prog.	Programmable	No	Internal
	HV7121D (Sensor)	CIF / Prog.	Programmable	No	Internal
Kodak	KAC-1310 (Sensor)	SXGA / 15	Programmable	No	Internal
	KAC-0311 (Sensor)	VGA / 30	Programmable	No	Internal
Micron Micron	MT9M413 (Sensor)	SXGA / 500	Programmable	No	Internal
	MT9M001 (Sensor)	SXGA / 30	Programmable	No	Internal
	MT9V403 (Sensor)	VGA / 200	Programmable	No	Internal
	MT9V043 (Sensor)	VGA / 30	Programmable	No	Internal
	MT9V143 (Integrated)	VGA / 30	VGA, QVGA, QQVGA, CIF, QCIF	No	CCIR 656 RGB 5:6:5
	MI0133 (Sensor)	CIF / 30	Programmable	No	Internal
	MI-SOC-0133 (Integrated)	CIF / 30	CIF	No	CCIR 656
OmniVision	OV2610 (Integrated)	UXGA / 10	UXGA, SVGA	No	CCIR 601/656 Raw RGB
	OV9630/9620 (Integrated)	SXGA/ 15	SXGA, VGA	No	CCIR 601/656 Raw RGB
	OV8610 (Integrated)	SVGA / 15	SVGA, VGA, QSVGA	No	CCIR 601/656 YcrCb 4:2:2 GRB 4:2:2 Raw RGB
	OV7648/7640/7635 (Integrated)	VGA / 30	VGA, QVGA	No	CCIR 601/656 YcrCb 4:2:2 GRB 4:2:2 Raw RGB
	OV6645/6630/6620 (Integrated)	CIF / 30	CIF, QCIF	No	CCIR 601/656 GRB 4:2:2 Raw RGB
	OV7648FS (Module)	VGA / 30	VGA, QVGA	No	CCIR 601/656 Raw RGB
Pictos (Conexant)	CX11646-21/22 (Image Processor)	VGA / 30	VGA, QVGA, CIF, QCIF	Yes	CCIR 656 Proprietary for JPEG
	CX20490 (Sensor)	VGA / 30	Programmable	No	Internal
	CN1024 (Sensor)	XGA / 25	Programmable	No	Internal
Sanyo	IGT99264-SSC01 (Module)	VGA /15	VGA	No	YUV 4:2:2 RGB 5:6:5
Sharp	LZ0P3916 (Module)	VGA / 30	VGA, QVGA, CIF, QCIF,	No	CCIR 656

Camera Vendor	Model	Max Resol. / Max FPS	Supported Resolutions	JPEG Encode	Interface
	LZ0P390E (Module)	CIF / 15	CIF, QCIF, QQCIF, QVGA, QQVGA	No	CCIR 656
Sony	ICX284AQ/434AQ (Sensor)	UXGA / 30	Programmable	No	Internal
ST	STV0674 (Image Processor)	VGA / 30	VGA, QVGA, CIF	Yes	M-JPEG via USB
	STV0676 (Image Processor)	VGA / 30	VGA, QVGA, CIF	Yes	YCrCb 4:2:2 M-JPEG via USB
	VV6600C001 (Sensor)	SXGA / 15	SXGA, VGA	No	Internal
	VV6501 (Sensor)	VGA / 30	VGA	No	Internal
	VV6411 (Sensor)	CIF /30	CIF, QCIF	No	Internal
Toshiba	TCM8210MD (A) (Module)	VGA / 30	VGA, QVGA, QQVGA, CIF, QCIF, SQCIF	No	YUV 4:2:2 RGB 5:6:5
TransChip	TC5640 (Single-Chip Module w/ Lens)	CIF / 30	CIF, QCIF, QVGA, QQVGA	Yes	CCIR 656 YUV RGB 4:4:4 RGB 5:6:5 RGB 6:6:6 RGB 8:8:8 Parallel/Serial for JPEG
	TC5740 (Single-Chip Module w/ Lens)	VGA / 20	VGA, QVGA, CIF, QCIF, QVGA, QQVGA	Yes	CCIR 656 YUV RGB 4:4:4 RGB 5:6:5 RGB 6:6:6 RGB 8:8:8 Parallel/Serial for JPEG
	TC6000 (Single-Chip Module w/ Lens) Note: With **MPEG4 Capture**. Contact info: rutie@transchip.com	SXGA	SXGA and smaller	Yes	CCIR 656 YUV RGB 4:4:4 RGB 5:6:5 RGB 6:6:6 RGB 8:8:8 Parallel/Serial for JPEG and MPEG4

C.2 Major Suppliers of CMOS Imagers

Table 21 Major Suppliers of CMOS Imagers

Names	Names
Agilent	National Semiconductor
Atmel Corporation, Thomson-CSF	Integrated Vision Products AB
C-Cam	Kodak
Chrontel	Lucent Technologies
Conexant (Pictos)	Matsushita*
CSEM	Micron
Dalsa	Mitsubishi
Eastmann-Kodak	Motorola
FillFactory	National Semiconductor
Foveon	Neuricam
Fujitsu	OmniVision Technologies, Inc.
IC Media Corp.	Philips
IMS Stuttgart	Photon Vision Systems
Infineon	Polaroid
(Intel)	Sarnoff Corporation
FHG Duisburg	Sharp*
Hamamatsu	Siemens
Hyundai Electronics	Sony*
Integrated Vision Products AB	SMaL Camera
Kodak	STMicroelectronics - VVL
Lucent Technologies	Suni Imaging Microsystems
Matsushita*	Texas Instruments
Micron	Toshiba
Mitsubishi	Y Media
Motorola	Zoran, PixelCam Inc