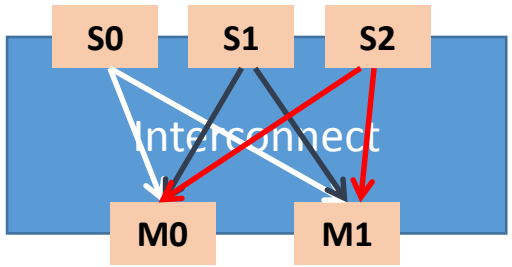
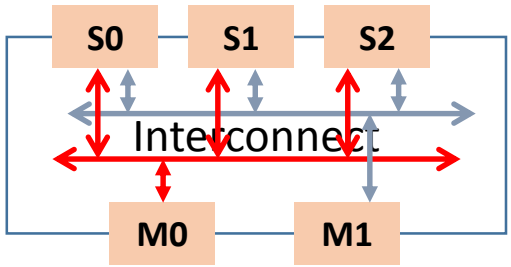
Arteris FlexNoC Resilience Package

Wooseok Lee

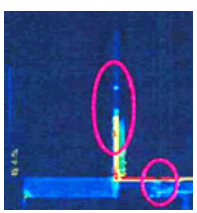
Why NoC?

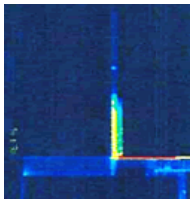
- Why Network on Chip Technology?
  - Commonly called “a front-end solution to a back-end problem”
  - Many of today’s systems-on-chip are too complex to utilize a traditional hierarchal bus or crossbar interconnect approach.
  - As semiconductor transistor dimensions shrink and increasing amounts of IP block functions are added to a chip
  - Physical infrastructure that carries data on the chip and guarantees quality of service begins to crumble



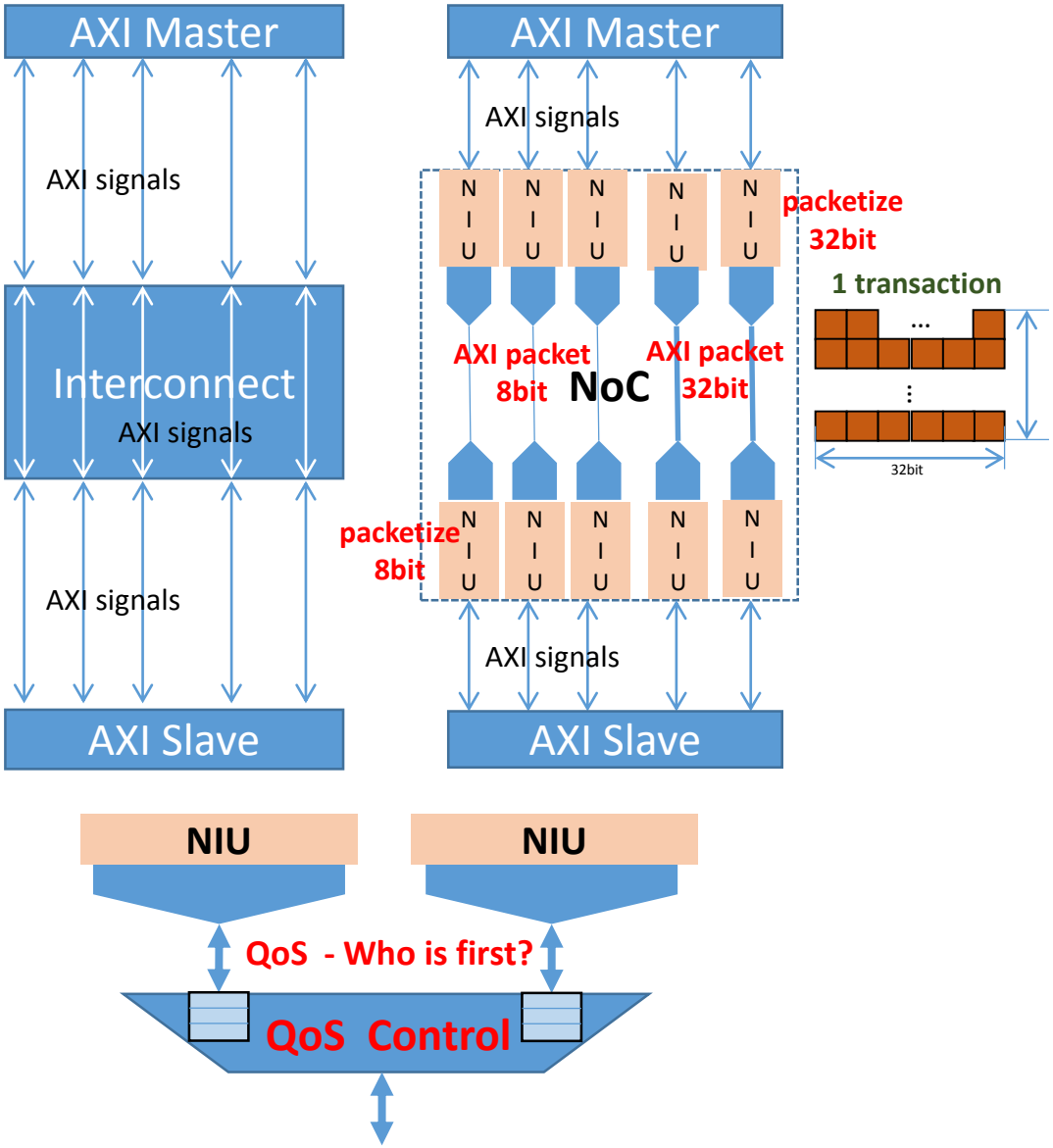


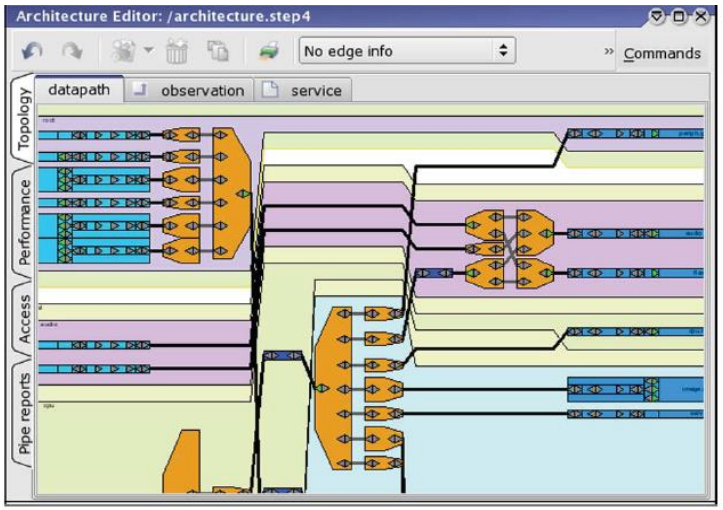
- Major reasons why SoC need a NoC IP interconnect fabric
  - Reduce Wire Routing Congestion
  - Ease Timing Closure
  - Higher Operating Frequency
  - Change IP Easily
  - Heterogeneous Traffic Types - QoS
    - CPU/Video Display/Imaging System/Background

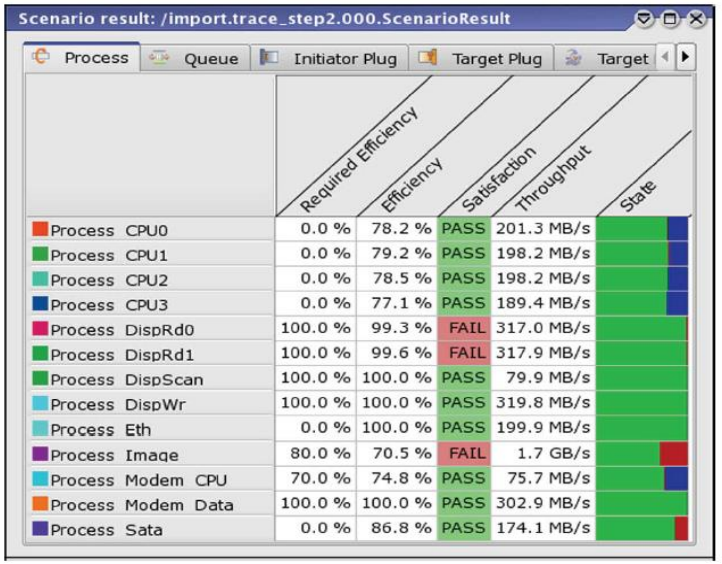




Packetization / TLM

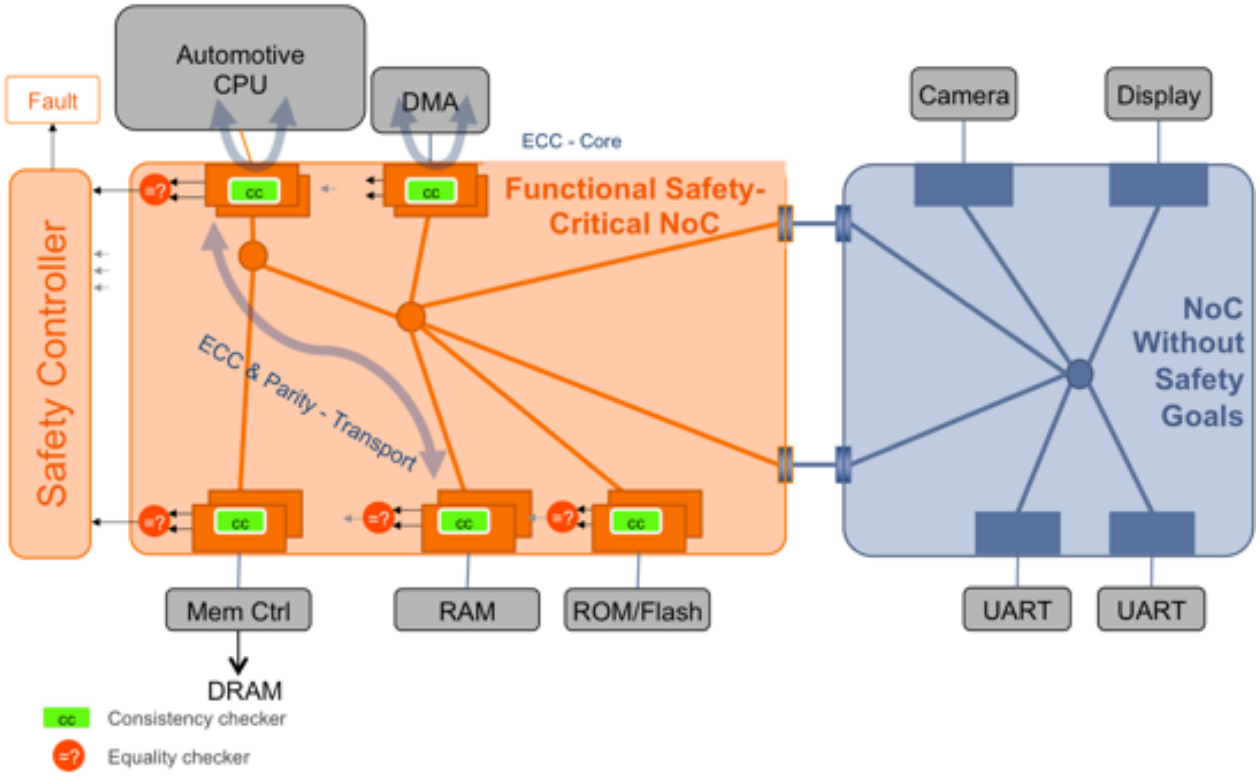






FlexNoC Resilience Package

- Protecting memory with ECC but leaving the rest of an SoC uncovered is non-sense.
- Without end-to-end protection of the cores, memory, peripherals, and interconnect, faults can and will put the entire system at risk.



Reference

[1] http://www.arteris.com/flexnoc-resilience-package

[2] http://cdn2.hubspot.net/hub/48858/file-1735393975-pdf/docs/flexnoc-resilience-package-datasheet.pdf

[3] J. Probell and B. d. Lescure, “SoC Reliability Features in the FlexNoC Resilience Package,” Arteris Tech Paper.

[4] https://www.semiwiki.com/forum/content/3917-noc-resilience-protects-end-end.html