

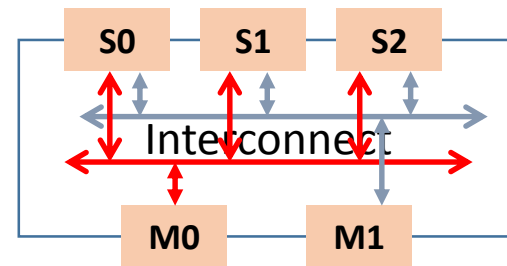
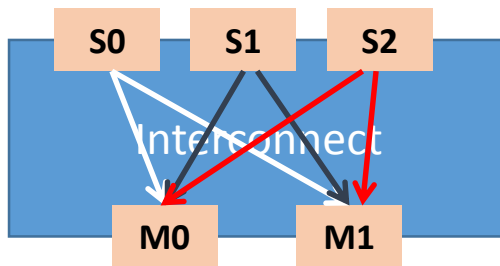
Arteris FlexNoC Resilience Package

Wooseok Lee

Why NoC?

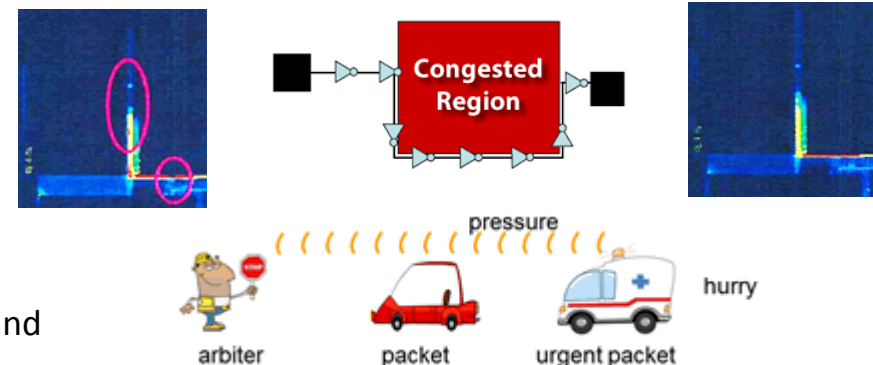
- Why Network on Chip Technology?

- Commonly called “a front-end solution to a back-end problem”
- Many of today’s systems-on-chip are too complex to utilize a traditional hierarchal bus or crossbar interconnect approach.
- As semiconductor transistor dimensions shrink and increasing amounts of IP block functions are added to a chip
- Physical infrastructure that carries data on the chip and guarantees quality of service begins to crumble

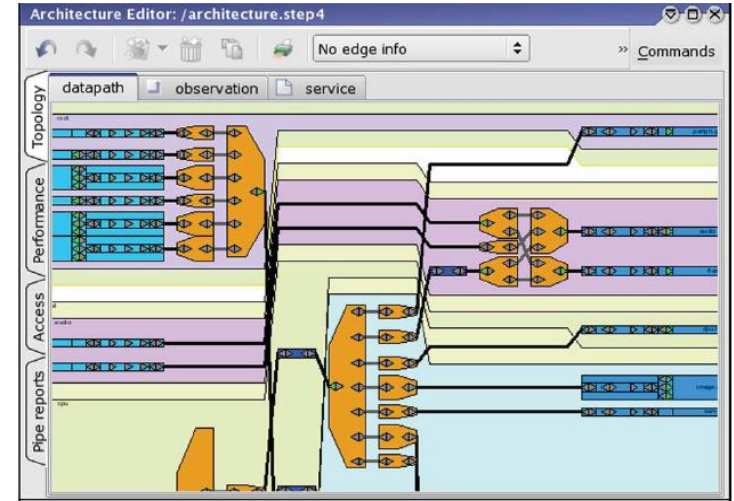
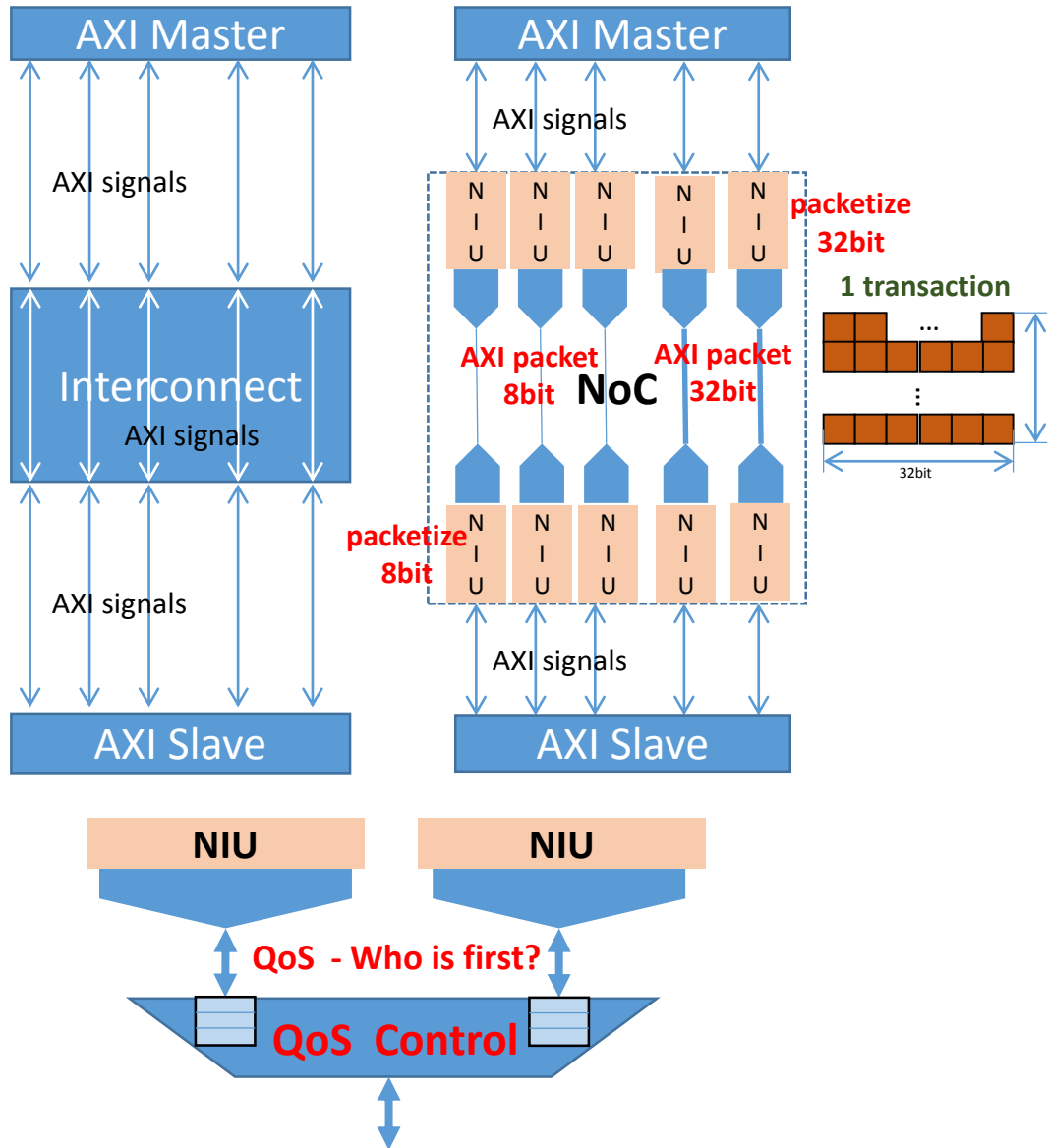


- Major reasons why SoC need a NoC IP interconnect fabric



























- Reduce Wire Routing Congestion
- Ease Timing Closure
- Higher Operating Frequency
- Change IP Easily
- Heterogeneous Traffic Types - QoS
 - CPU/Video Display/Imaging System/Background



Packetization / TLM

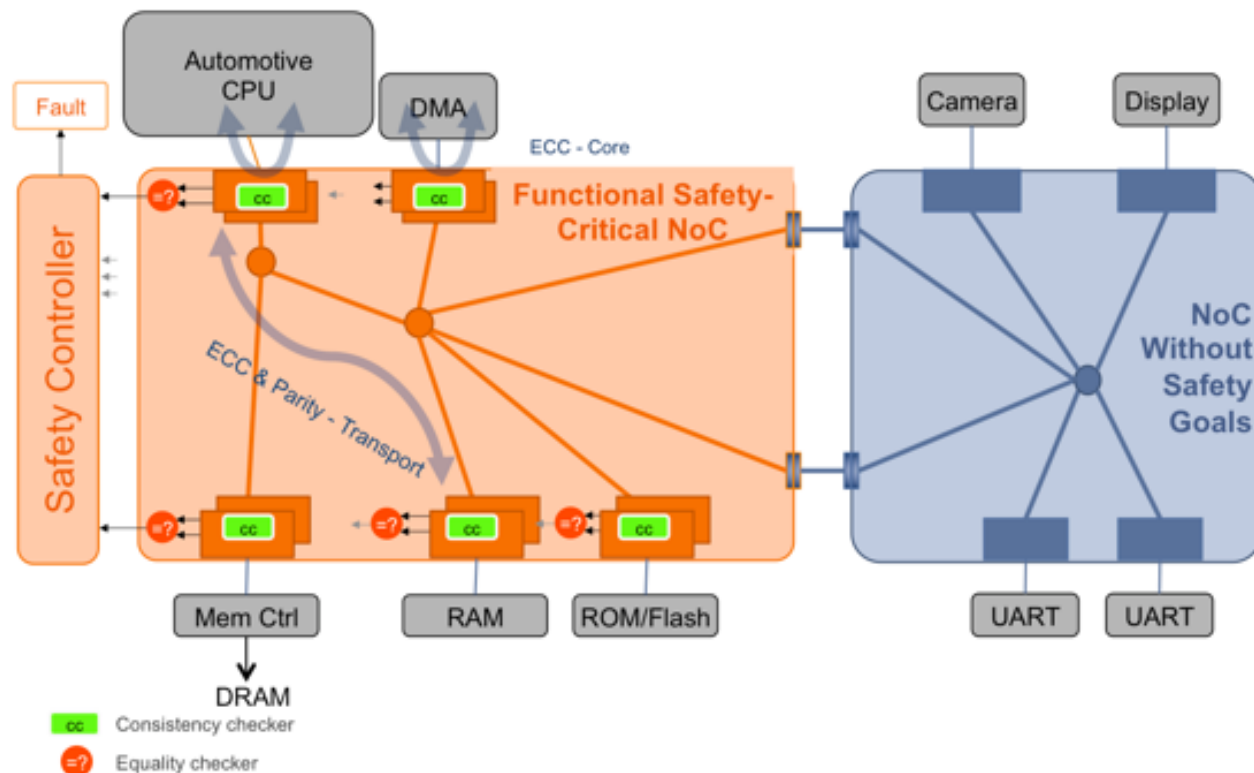


Scenario result: /import.trace_step2.000.ScenarioResult

Process		Queue	Initiator Plug	Target Plug	Target					
						Required Efficiency	Efficiency	Satisfaction	Throughput	State
	Process CPU0					0.0 %	78.2 %	PASS	201.3 MB/s	
	Process CPU1					0.0 %	79.2 %	PASS	198.2 MB/s	
	Process CPU2					0.0 %	78.5 %	PASS	198.2 MB/s	
	Process CPU3					0.0 %	77.1 %	PASS	189.4 MB/s	
	Process DispRd0					100.0 %	99.3 %	FAIL	317.0 MB/s	
	Process DispRd1					100.0 %	99.6 %	FAIL	317.9 MB/s	
	Process DispScan					100.0 %	100.0 %	PASS	79.9 MB/s	
	Process DispWr					100.0 %	100.0 %	PASS	319.8 MB/s	
	Process Eth					0.0 %	100.0 %	PASS	199.9 MB/s	
	Process Image					80.0 %	70.5 %	FAIL	1.7 GB/s	
	Process Modem CPU					70.0 %	74.8 %	PASS	75.7 MB/s	
	Process Modem Data					100.0 %	100.0 %	PASS	302.9 MB/s	
	Process Sata					0.0 %	86.8 %	PASS	174.1 MB/s	

FlexNoC Resilience Package

- Protecting memory with ECC but leaving the rest of an SoC uncovered is non-sense.
- Without end-to-end protection of the cores, memory, peripherals, and interconnect, faults can and will put the entire system at risk.



Reference

[1] <http://www.artemis.com/flexnoc-resilience-package>

[2] <http://cdn2.hubspot.net/hub/48858/file-1735393975-pdf/docs/flexnoc-resilience-package-datasheet.pdf>

[3] J. Probell and B. d. Lescure, “SoC Reliability Features in the FlexNoC Resilience Package,” Arteris Tech Paper.

[4] <https://www.semiwiki.com/forum/content/3917-noc-resilience-protects-end-end.html>