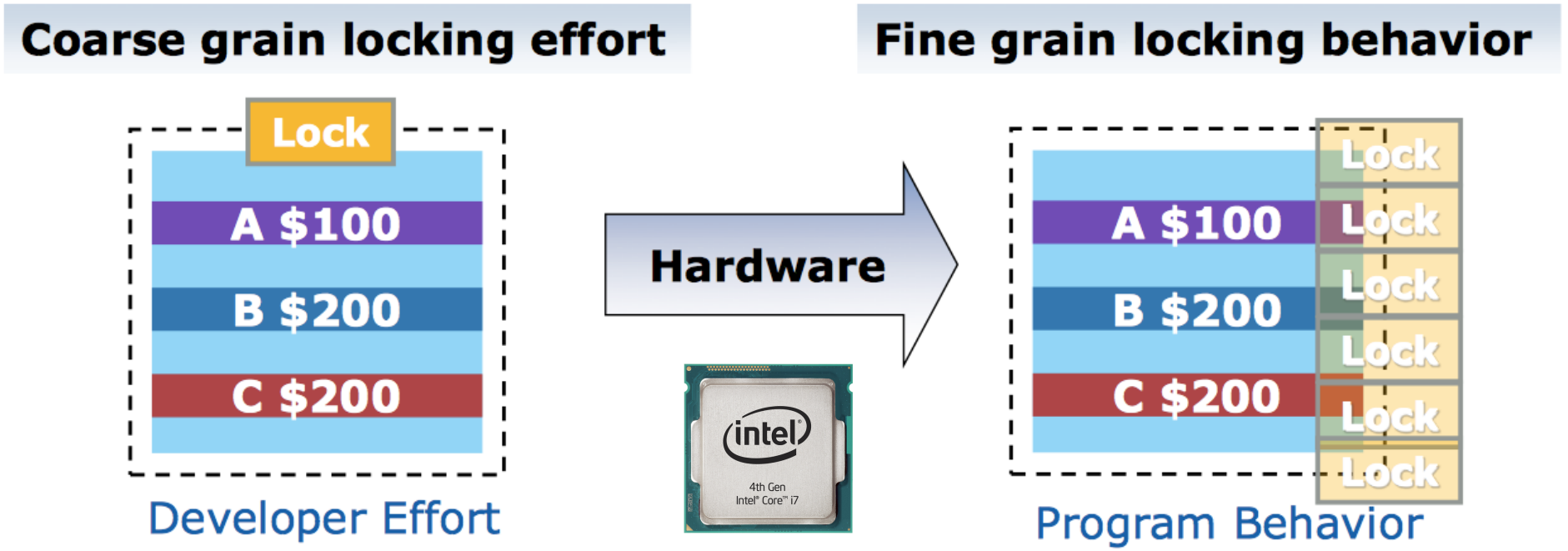
Intel TSX Erratum

- Transaction Synchronization Extensions (TSX)
  - Allows traditionally locked instruction in a multithreaded environment to execute without locks using LOCK ELISION
  - If instructions end up violating each others shared data, progress is backtracked and the tradition locked route is taken
- Introduced originally for a database/server environment
- read-sets and write-sets at the granularity of an L1 cache line
- data conflicts are detected through the cache coherence protocol.



Intel TSX Erratum

- Bug caused by a complex set of internal timing and system events
- Results in "unpredictable system behavior"
- Found in Current Haswell and future Broadwell Chips
- Microcode update turns off TSX altogether

Intel's Official Errata Document
http://www.intel.com/content/dam/www/public/us/en/documents/specification-updates/xeon-e3-1200v3-spec-update.pdf

HSW136. Software Using Intel® TSX May Result in Unpredictable System Behavior

Problem:	Under a complex set of internal timing conditions and system events, software using the Intel TSX (Transactional Synchronization Extensions) instructions may result in unpredictable system behavior.
Implication:	This erratum may result in unpredictable system behavior.
Workaround:	It is possible for the BIOS to contain a workaround for this erratum.
Status:	For the steppings affected, see the *Summary Table of Changes*.

Sources:

- Ravi Rajwar, CPU Architect, Intel Martin Dixon, Principal Engineer, Intel, "Intel® Transactional Synchronization Extensions", https://software.intel.com/sites/default/files/managed/68/10/sf12-arcs004-100.pdf
- Ian Cutress, "Intel Disables TSX Instructions: Erratum Found in Haswell, Haswell-E/EP, Broadwell-Y", http://www.anandtech.com/show/8376/intel-disables-tsx-instructions-erratum-found-in-haswell-haswelleep-broadwelly
- Transactional Synchronization Extensions, http://en.wikipedia.org/wiki/Transactional_Synchronization_Extensions