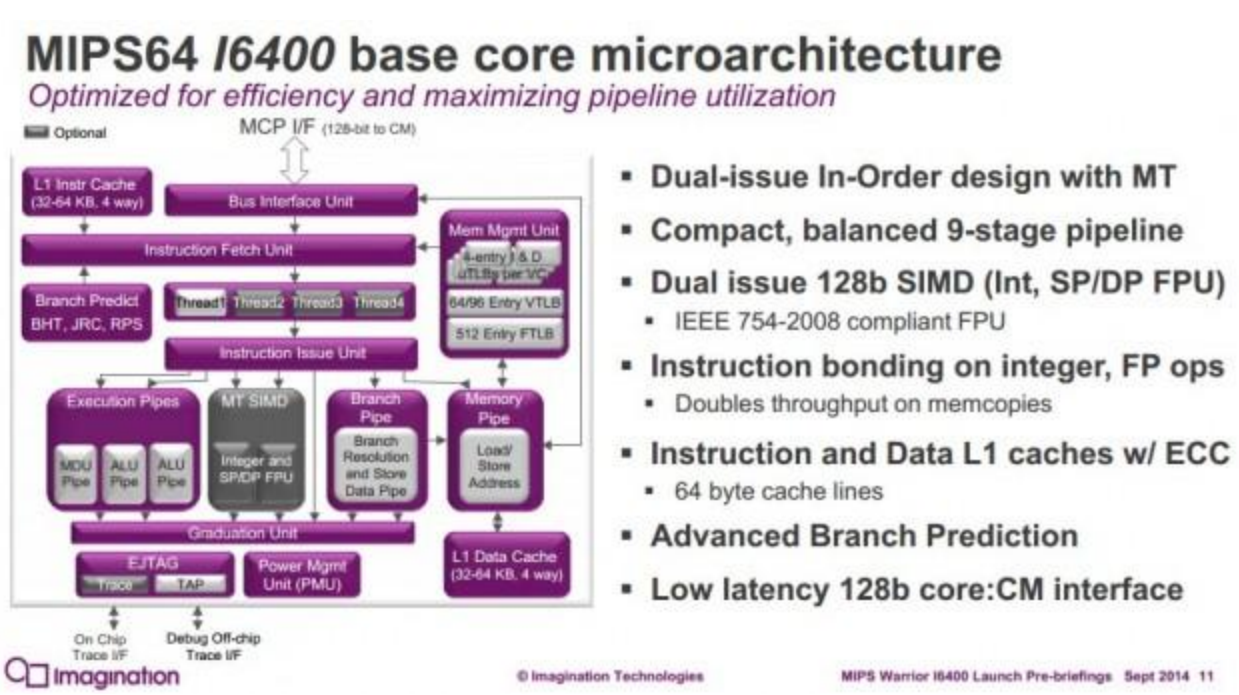
MIPS Returns

- One of the early RISC ISAs
  - MIPS stands for “Microprocessor without interlocking pipeline stages”, basically no hardware insertion of pipeline bubbles, compiler takes care of this (used to).
  - Load/Store, Register centric, simple fixed length instructions, emphasized simple hardware
- Used in many introductory Comp Arch courses (most notably in H&P textbook) and digital design courses
- Popularity has waned in industry, still found in embedded space
- Architecture recently purchased by Imagination Technologies whose known for their PowerVR graphics IPs (seen in iPad, iPhone, Atom SoCs, Android Tablets, etc…)



Warrior I6400 Core

- Implements new MIPS3264 version of MIPS ISA (32 and 64 bit coexists, no mode switching such as in IA32/AMD64)
- Targets embedded and mobile segments currently dominated by ARM, comparable to the Cortex-A53 (ARM's reference lower-end 64 bit design)
- Can be configured as multithread (up to 4 threads with 2 scheduled) or 2-wide superscalar for a single thread. SMT designs are fairly new to the (non-DSP) embedded space
- "Instruction bonding", loads/stores of equal sizes to adjacent memory addresses can be dynamically fused into a single instruction up to 128-bits to increase the performance of memory copies/moves

I6400 vs. Cortex-A53

	MIPS I6400	ARM Cortex-A53
CPU Codename	Warrior	Apollo
ISA	MIPS3264 Release 6	ARMv8-A (32/64-bit)
Cores in an SMP Cluster	1-6	1-4
Thread Width	1-4	1
Issue Width	2 micro-ops	2 micro-ops
Reorder Buffer Size	None: In-Order	None: In-Order
Pipeline Depth (stages)	9	8 (Int) 10 (FP)
Integer ALUs	2	2
Load/Store Units	1 (2 with bonding)	1
Load Latency	3 cycles	3 cycles
Branch Units	1	1
FP/NEON ALUs	2	2
Coherency	Directory	Snoop + Filter
L1 Cache	32 or 64KB I$ + 32 or 64KB D$	8 to 64KB I$ + 8 to 64KB D$
L2 Cache	0.5 to 8MB	0.5 to 2MB

Sources

1. http://www.theverge.com/2012/11/7/3611972/imagination-buys-mips-arm-gets-patents
2. http://www.anandtech.com/show/8457/mips-strikes-back-64bit-warrior-i6400-architecture-arrives
3. http://www.extremetech.com/computing/189190-imaginations-warrior-cpu-breathes-new-life-into-mips-will-attack-arm-on-multiple-fronts