

Open ISA

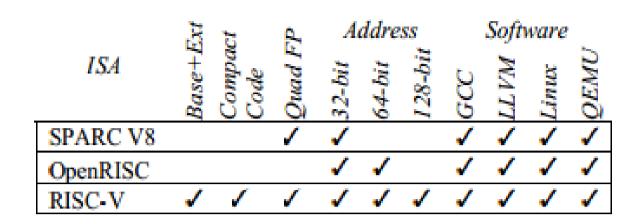
- Big Companies = Time & Money
 - → Negotiations
 - → Patents
- Many already have the ISA experience needed
- Open = Longevity
 - → Company that dies takes its ISA with it

<u>Learning from</u> <u>mistakes</u>

Example: uArch affecting the ISA (a.k.a.

"over-architecting")

ISA	Width (bits)	Frequency (GHz)	Dhrystone Performance (DMIPS/MHz)	Area mm2 (no caches)	Area mm2 (16 KB caches)	Area Efficiency (DMIPS/MHz/mm2)	Dynamic Power (mW/MHz)
ARM	32	>1	1.57	0.27	0.53	3.0	< 0.080
RISC-V	64	>1	1.72	0.14	0.39	4.4	0.034
R/A	2	1	1.1	0.5	0.7	1.5	≥0.4



Base + extension:

- core set of instructions that compilers depend upon
- optional extensions for common ISA additions
- space for new opcodes for application-specific accelerators.

Warehouse computer optimizations

- Quadruple-precision (QP) as well as SP and DP floating point.
- 128 bit address space

Variable length extension available (similar to Thumb ISA)

Sources:

- http://www.extremetech.com/computing/188405-risc-ridesagain-new-risc-v-architecture-hopes-to-battle-arm-and-x86-bybeing-totally-open-source
- http://www.eecs.berkeley.edu/Pubs/TechRpts/2014/EECS-2014-146.pdf
- http://www.eecs.berkeley.edu/~waterman/papers/msthesis.pdf
- http://riscv.org/