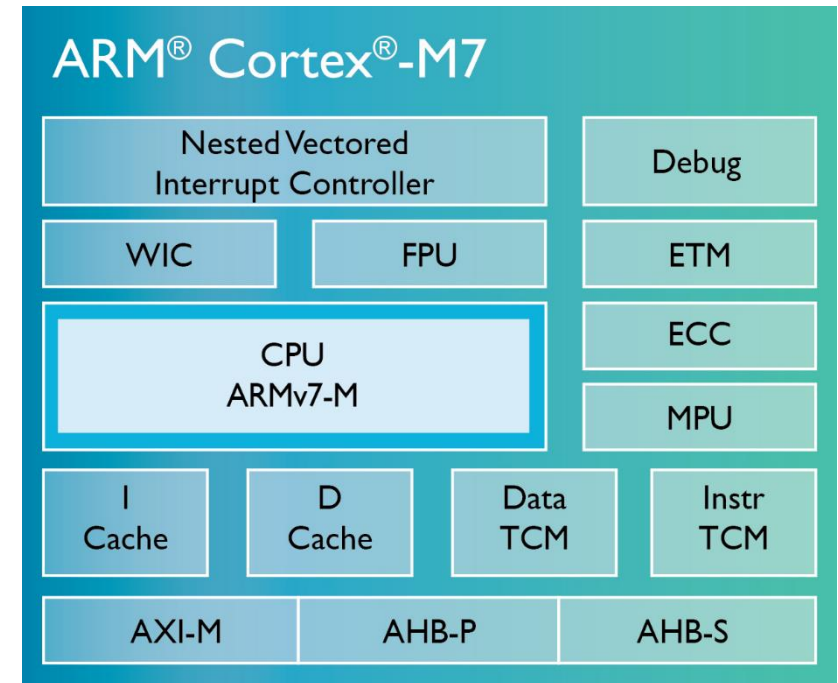


ARM Cortex-M7 Launches: Bring Intelligence to IoT

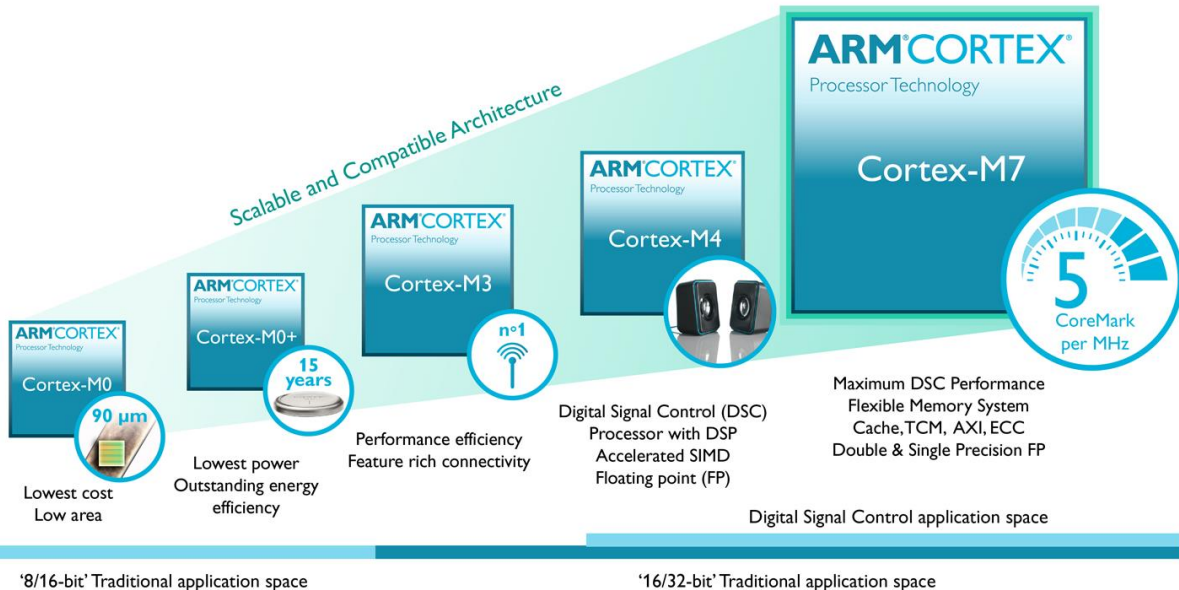


ARM

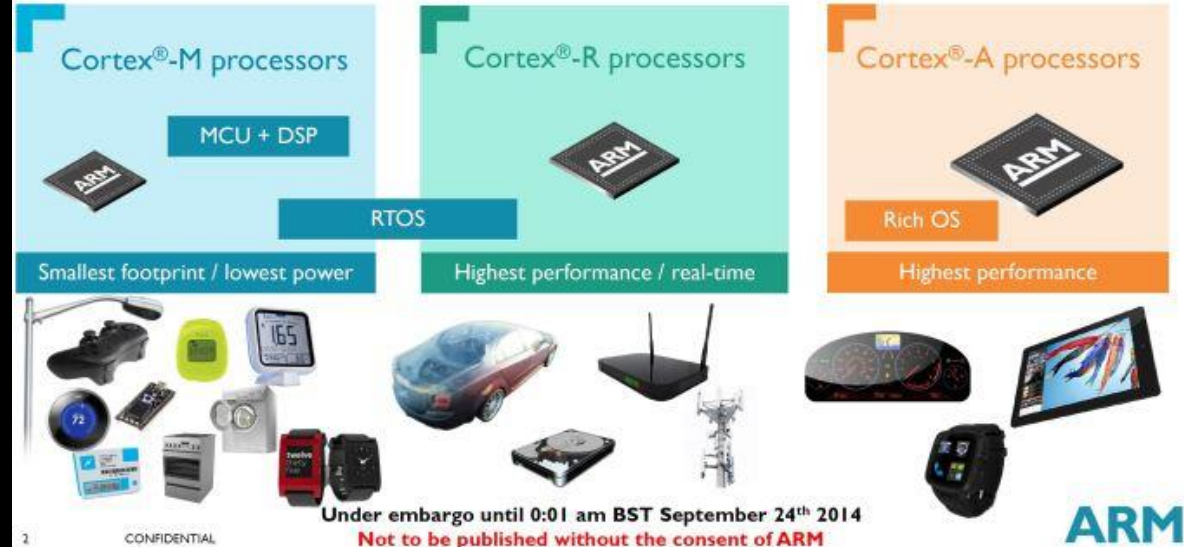
Cortex-M Series

(Advanced low power optimization)

Scalable and Compatible Architecture

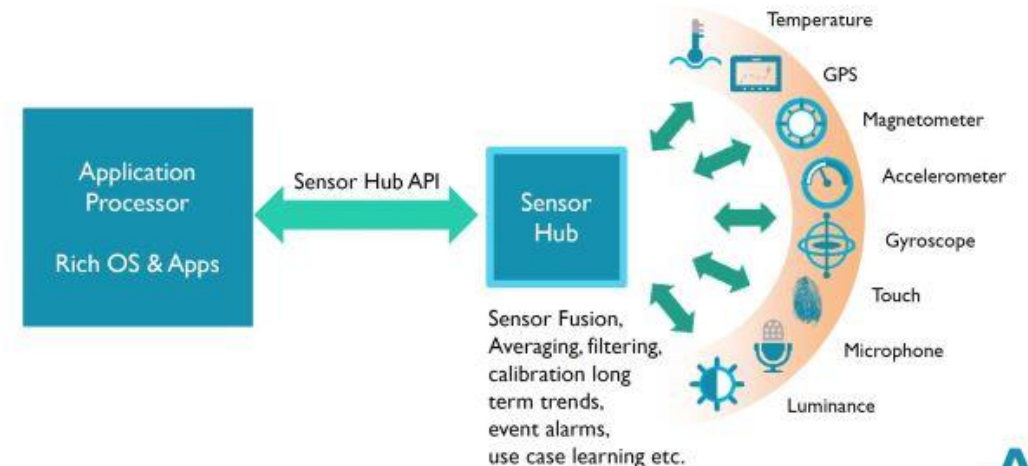


ARM® Cortex® Processors across the Embedded Market



'Always-on, Always-Aware' Architecture key for Sensors

Sensor Hub brings contextual awareness tracking even when the Apps Processor is in standby



Cortex-M7 vs. Cortex-M4

	ARM Cortex-M7	ARM Cortex-M4
ISA Support	ARMv7-M	Thumb® / Thumb-2
Floating Point Unit	Single and double precision floating point unit	Single precision floating point unit
Pipeline	6-stage superscalar + branch prediction	3-stage + branch speculation
Performance Efficiency	5.04 CoreMark/MHz*	3.40 CoreMark/MHz*
Performance Efficiency	2.14 / 2.55 / 3.23 DMIPS/MHz**	1.25 / 1.52 / 1.91 DMIPS/MHz ** (With FPU: 1.27 / 1.55 / 1.95 DMIPS/MHz)
Interconnect	64-bit AMBA4 AXI, AHB peripheral port (64MB to 512MB)	
Instruction cache	0 to 64kB, 2-way associative with optional ECC	
Data cache	0 to 64kB, 4-way associative with optional ECC	
Instruction TCM	0 to 16MB with optional ECC	
Data TCM	0 to 16MB with optional ECC	

* CoreMark: One of the benchmarks of EEMBC (comprise of commonly used algorithms)

** Dhrystone: abides by all “ground rules” / permits inlining of functions / permits simultaneous compilation

References

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- <http://www.arm.com/products/processors/cortex-m/cortex-m7-processor.php>
- <http://www.arm.com/products/processors/cortex-m/cortex-m4-processor.php>