Pentium Pro

- 1995
- First out of order, 3 wide

Pentium

- First superscalar from intel
- In-order, 2 wide
- simple instructions may be paired

uops
ex : ADD[EBX + EAX], ECX

decompose

1. MR1 <- EBX + EAX; effective address
2. MR2 <- Mem[MR1]; load
3. Flags, MR3 <- MR2 + ECX; add
4. Mem[MR1] <- MR3; result store

CISC with uop -> more RISC like

Performance Monitoring on PentiumPro

- 2 counters
- 100s of metrics
- Free running cycle counter
- Counters controlled with even select register
    - Certain counters only have access to certain metrics

Performance metric with numerator and denominator events displayed in table in PentiumPro paper

Concepts for understanding

- Dynamic execution
- Dataflow order
- Reservation station – hold instructions for dependency
- ROB – re-order results to in order, Read Order Buffer
- MOB – ROB for memory instructions, Memory Order Buffer
- Register renaming – hide register names to clarify dependencies
- Non-blocking cache – allows other accesses to continue when handling a miss

PentiumPro pipeline

- 8-3-3 length
- 3 width
- 20 RS entries
- 40 ROB entries

Latencies/throughput
Add 1/1

FPADD 3/1
FPMUL 5/0.5
IMUL 4/1
LD 3 for L1 hit
FDIV 17/32/37 single/double/extended

MPKI-miss per kilo instruction
-good metric for judging memory use

SPEC
FP better i-cache behavior than INT

- Fewer branches
- FP have big data structures with loops

FP worse LID-cache and L2-cache

- Bigger data sets

Speculative execution factor

- Small but non-zero number desired
- Accurate speculation desired

PentiumPro

- Feature size 0.6u
- INT – 0.01 to 0.9 MPKI
- FP – 0.01 to 0.05 MPKI
- Memory transaction / ki
    - INT – 1 to 10
    - FP – 1 to 70

In out of order processor, not always possible to find cause and effect relations
CPI most correlated with L2 misses