EE 382N-4 Embedded System Architecture
HW #1

Assigned: Jan 15th, 2011 Due: Feb 14th, 2011 (ICS Program)
Assigned: Jan 24th, 2011 Due Feb 21st, 2011 (Regular Program)

Problem 1 (100 pts)

Design the assembly language instructions needed to implement a Matrix Multiplication if you were building a specialized machine using a **Two (2) address machine**. NOTE: you need to use primitive instructions, i.e., logical, arithmetic, moves, stores, branches, etc.

Assumptions:

a) The datapath has one 32-bit ALU, one 32-bit shifter and one 32x32 multiplier. The multiplier generates a 64-bit result and stores the results in two consecutive memory locations.
b) The instructions are fixed width. You will need to specify the width. The maximum amount of addressable memory in this machine is 4096 bytes.
c) The data width is 32 bits. Hint: Need to worry about overflow and condition code bits, etc.

Deliverables

1) Describe your new instruction set.

2) Write the pseudo assembly language routine using the new instructions showing the multiplication of a 3x3 array below:

$$A \cdot B = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} \begin{bmatrix} b_{11} & b_{12} & b_{13} \\ b_{21} & b_{22} & b_{23} \\ b_{31} & b_{32} & b_{33} \end{bmatrix} = \begin{bmatrix} \sum_i a_{1i} b_{i1} & .. & .. \\ .. & .. & \sum_i a_{2i} b_{i3} \\ .. & .. & .. \end{bmatrix}$$

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