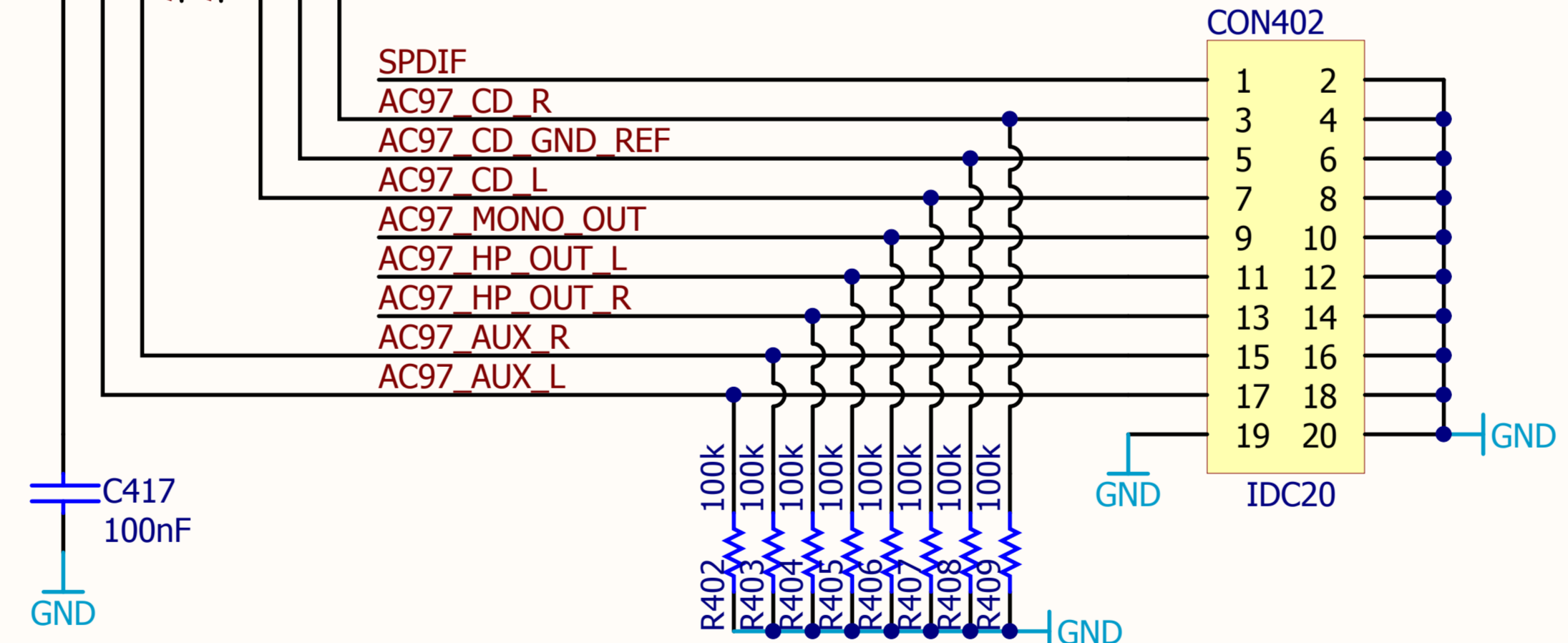
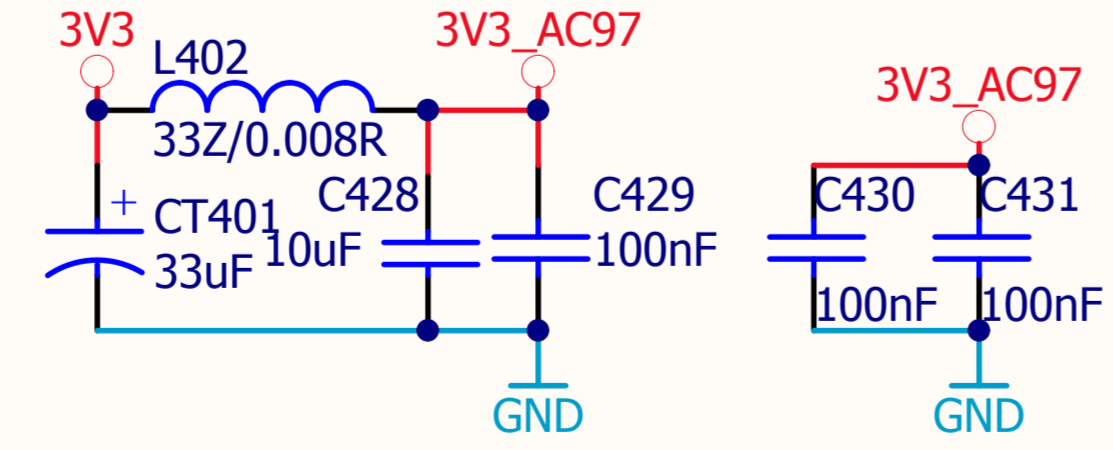
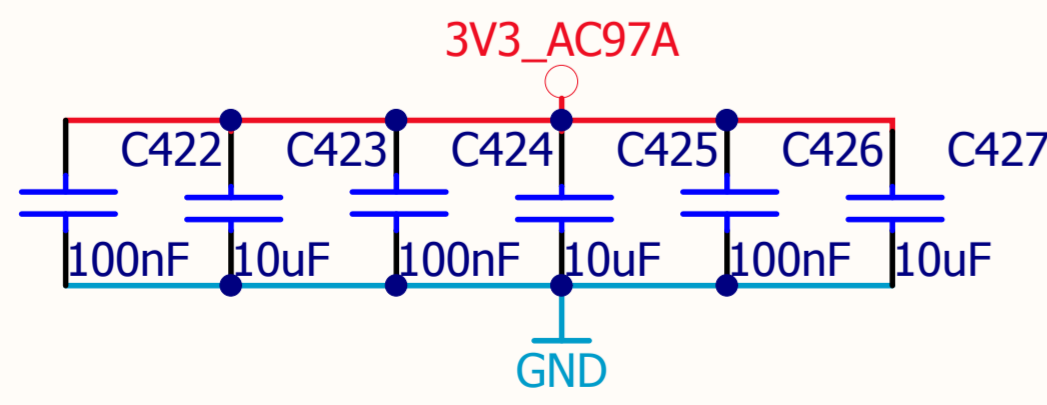
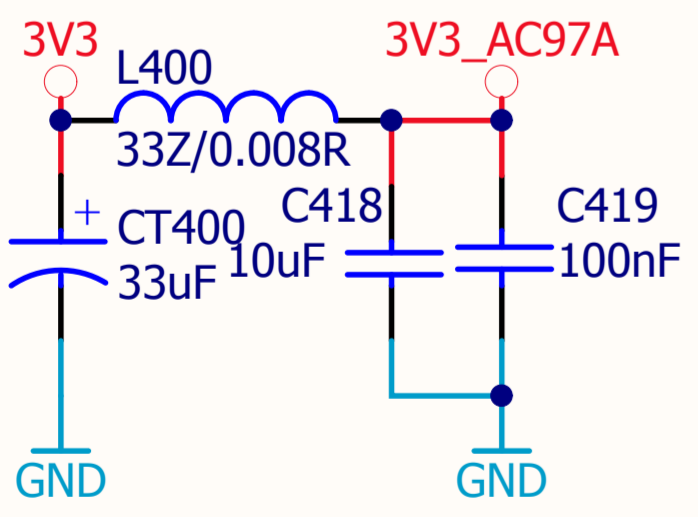
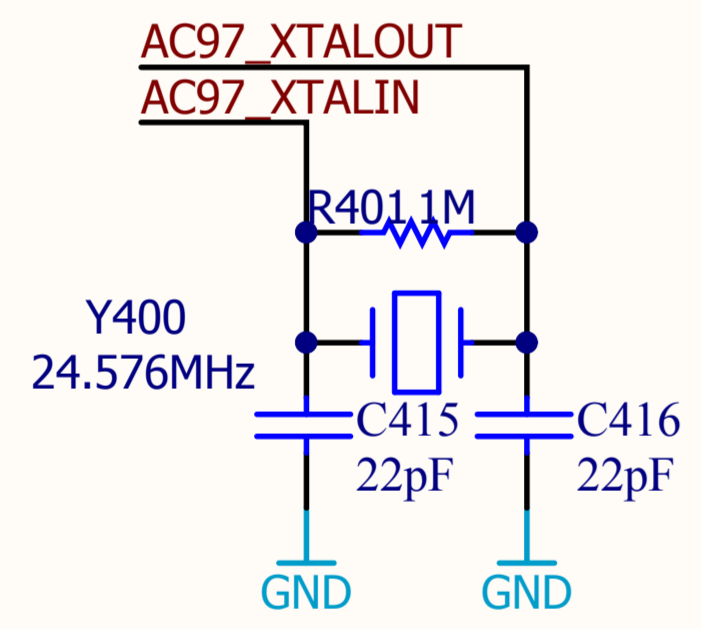
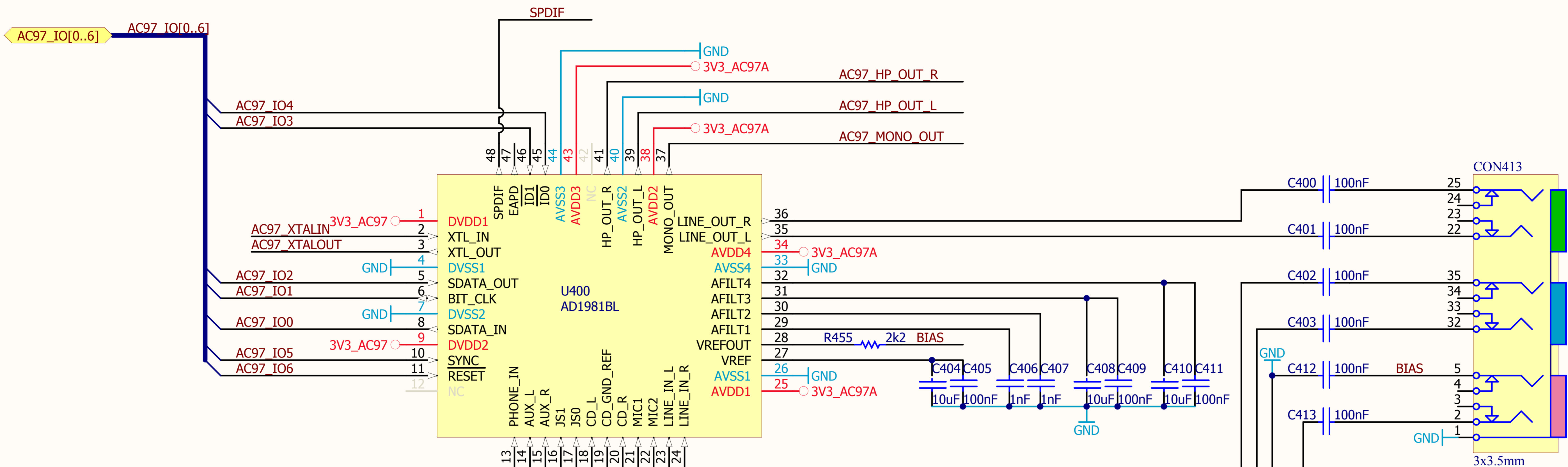


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Novi Sad Institute of Information Technology					
Accessory Connector					
Size	Number	Revision			
A3	P005_24	R002			
Date:	25.1.2007	Sheet 9 of	27		
File:	D:\Working\...Accessory Connector_1_1500	Drawn By:	Ivan Resetar		



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Title		LL5000 Audio Codec		
Size A4	Number P005_21	Revision R002		
Date:	25.1.2007	Sheet 2 of	27	
File:	D:\Working\..\AudioCodec_1_1.SchDoc	Drawn By:	Ivan Resetar	

A

A

B

B

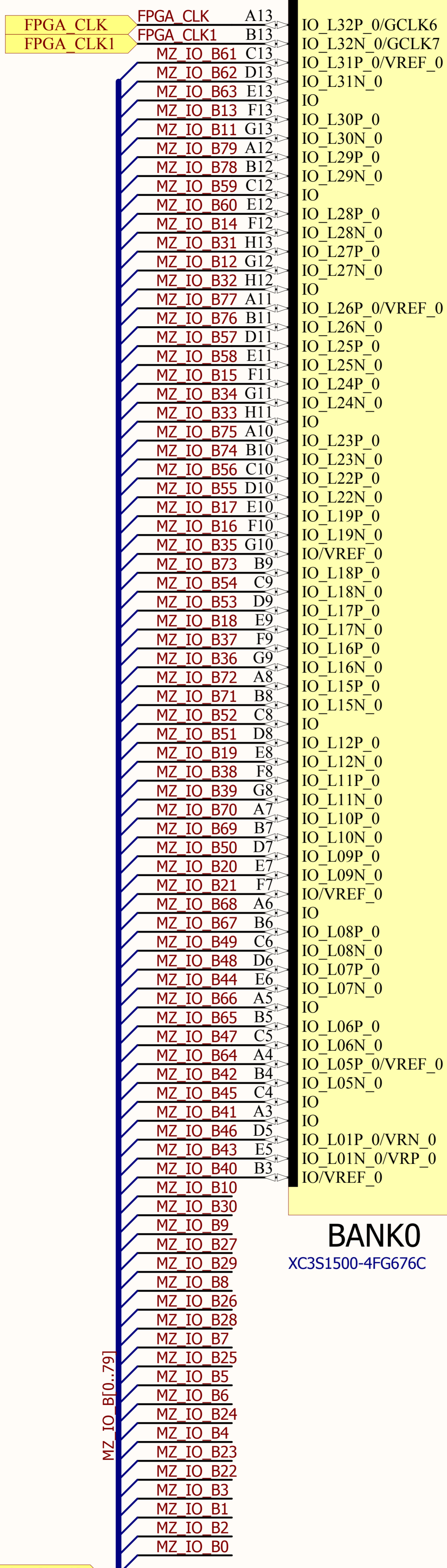
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C

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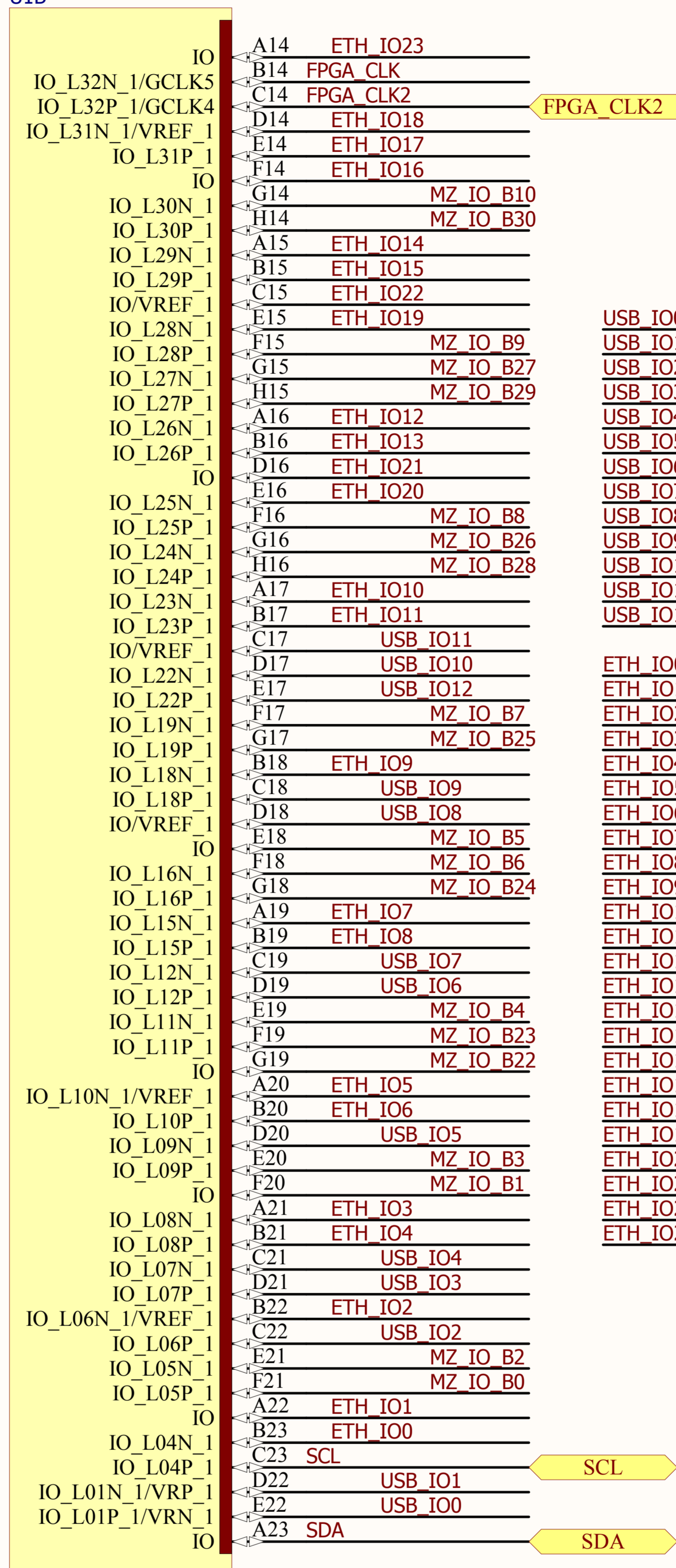
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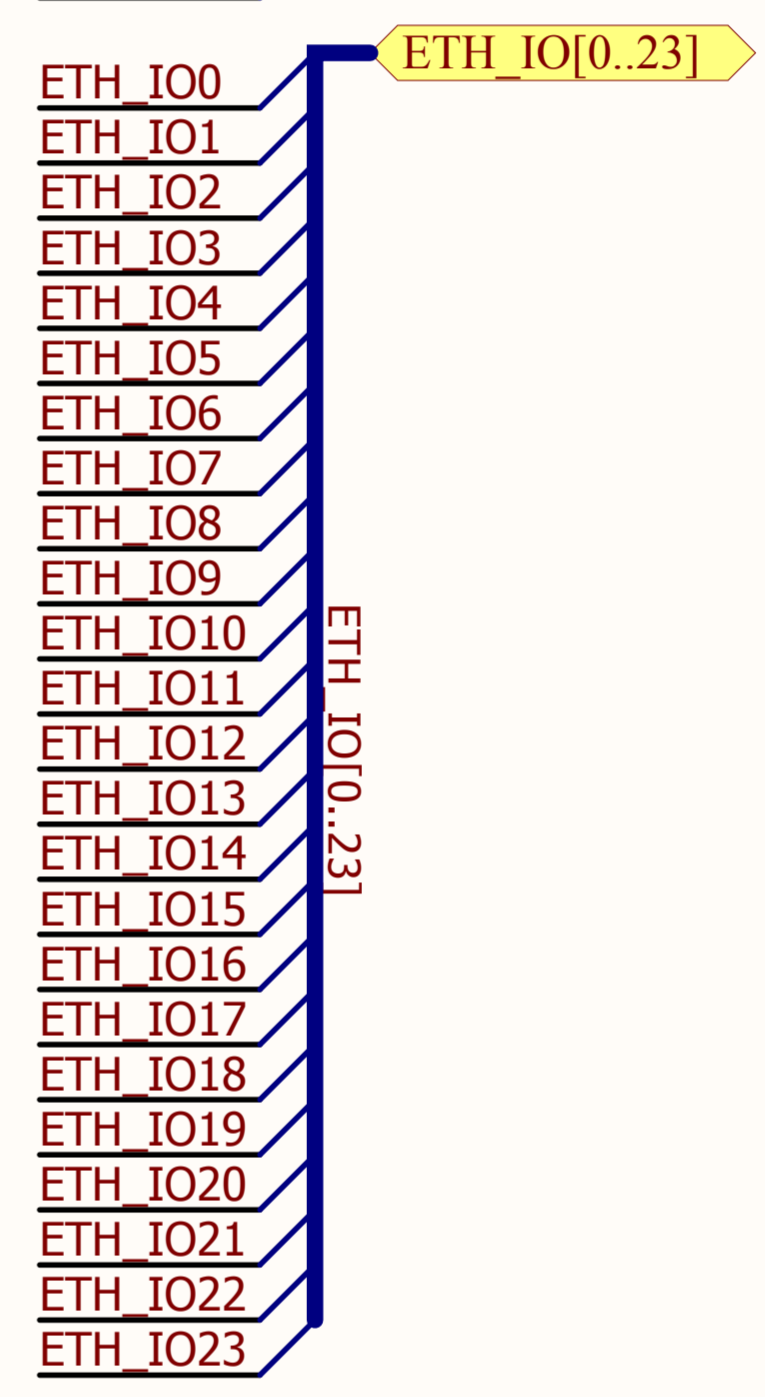
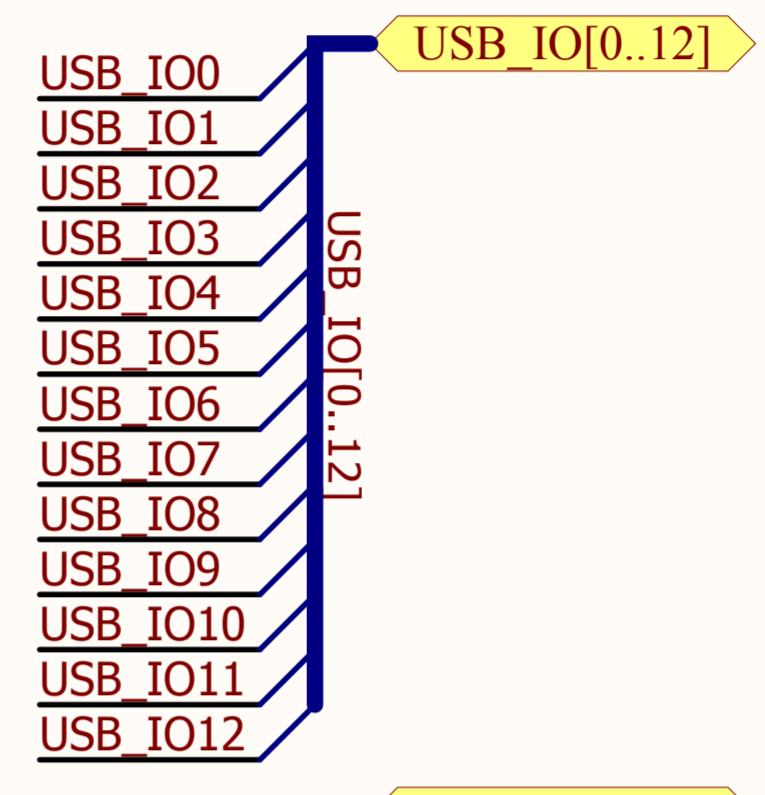


BANK0
XC3S1500-4FG676C

U1B



BANK1
XC3S1500-4FG676C

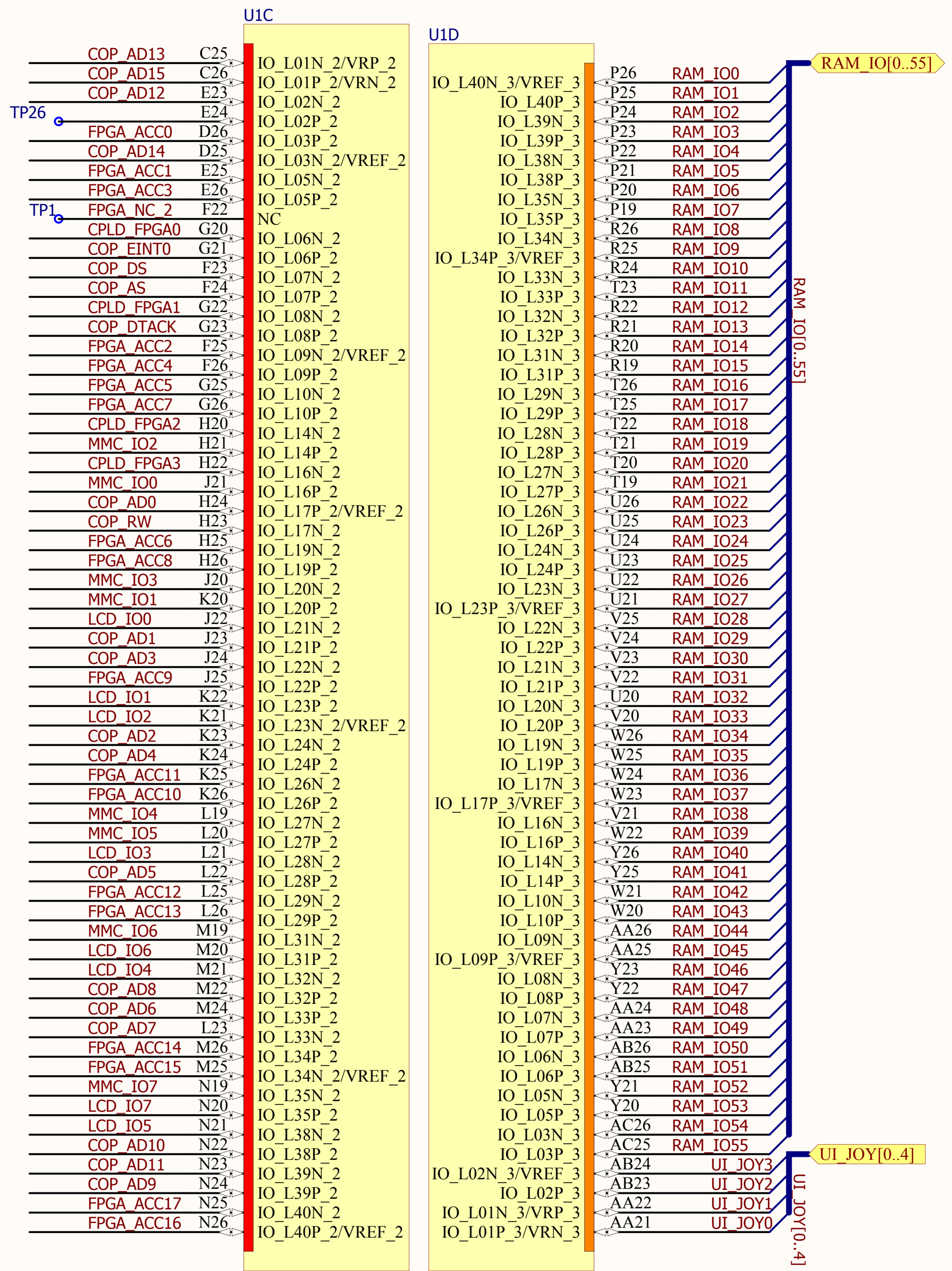


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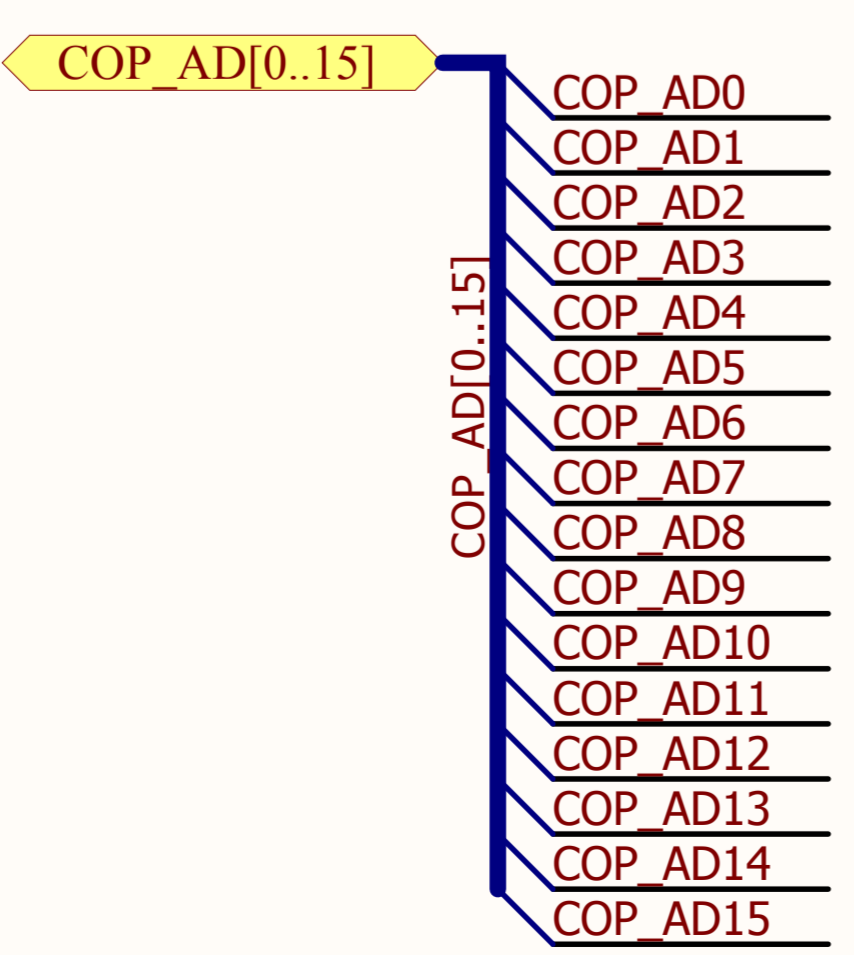
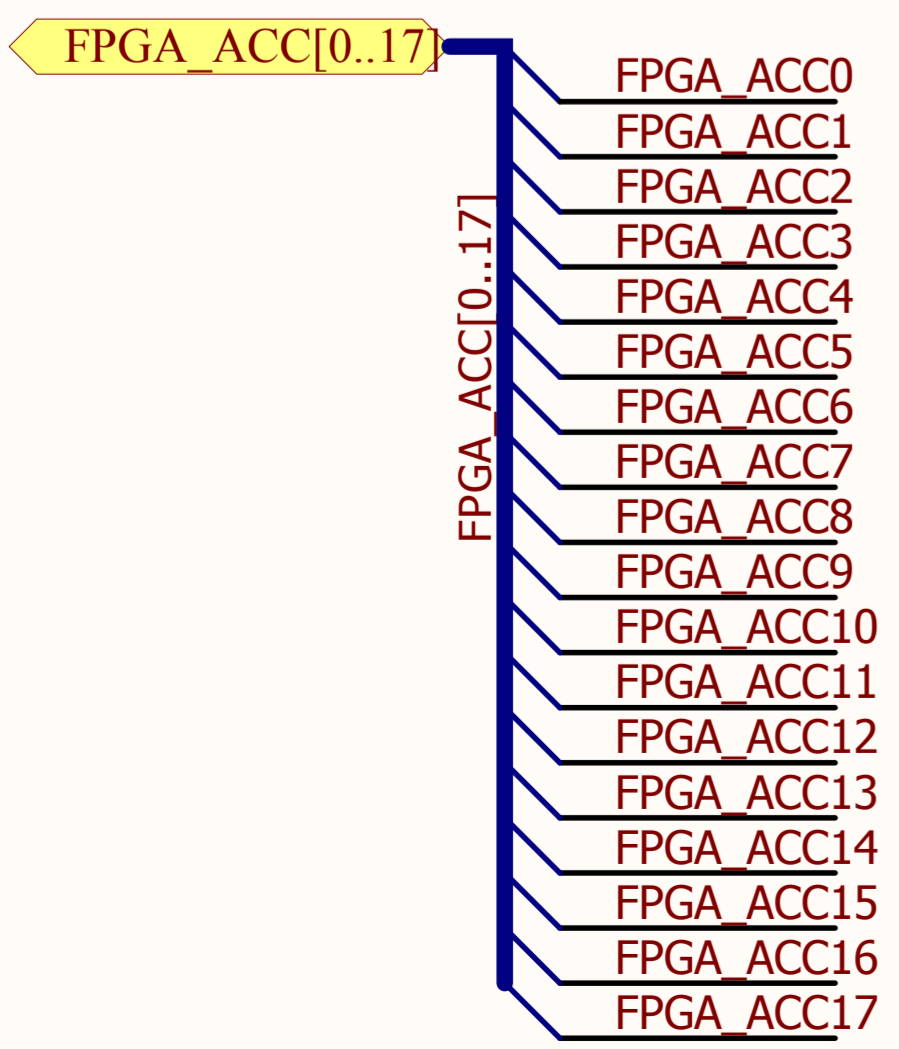
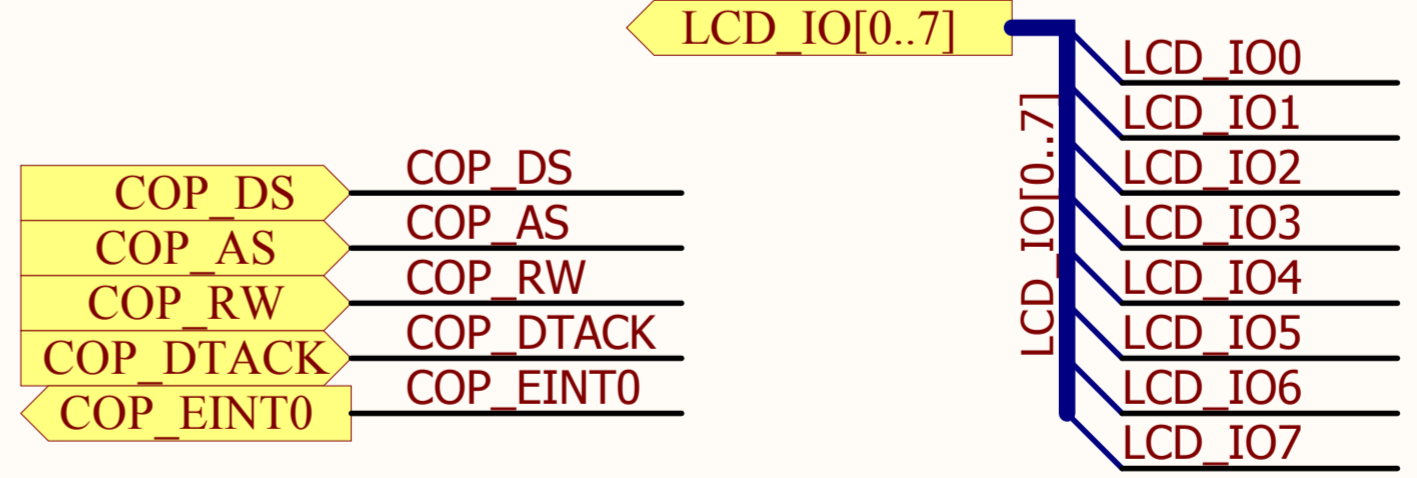
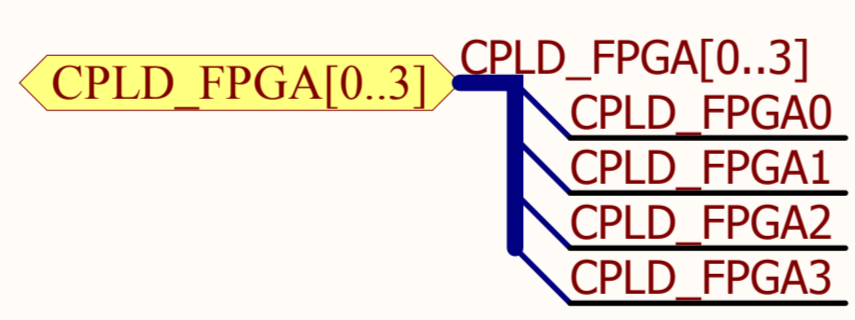
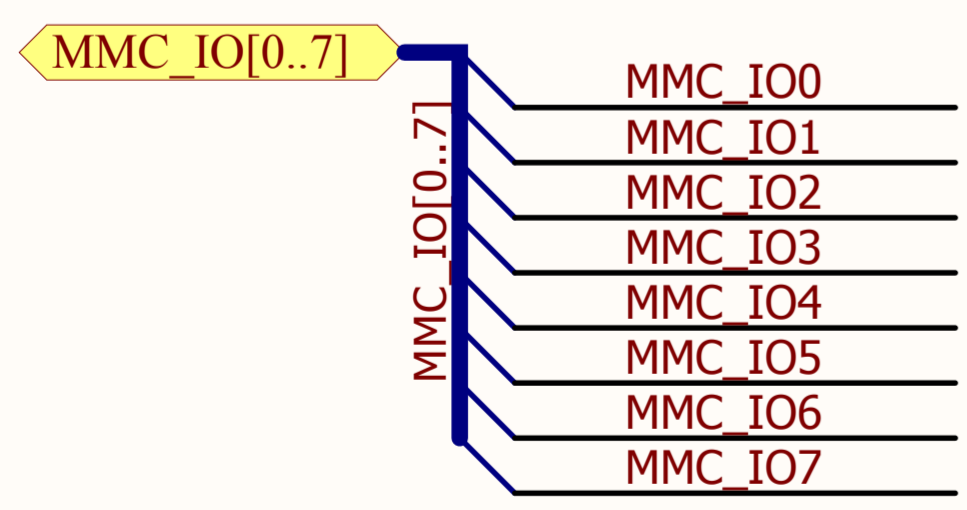
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Title TLL5000 Bank0/1 Connections		
Size A4	Number P005_2	Revision R002
Date: 25.1.2007	Sheet 2 of 27	Drawn By: Zoltan Pele
File: D:\Working\...\Bank0_1_1_1.SchDoc		



BANK2
XC3S1500-4FG676C

BANK3
XC3S1500-4FG676C



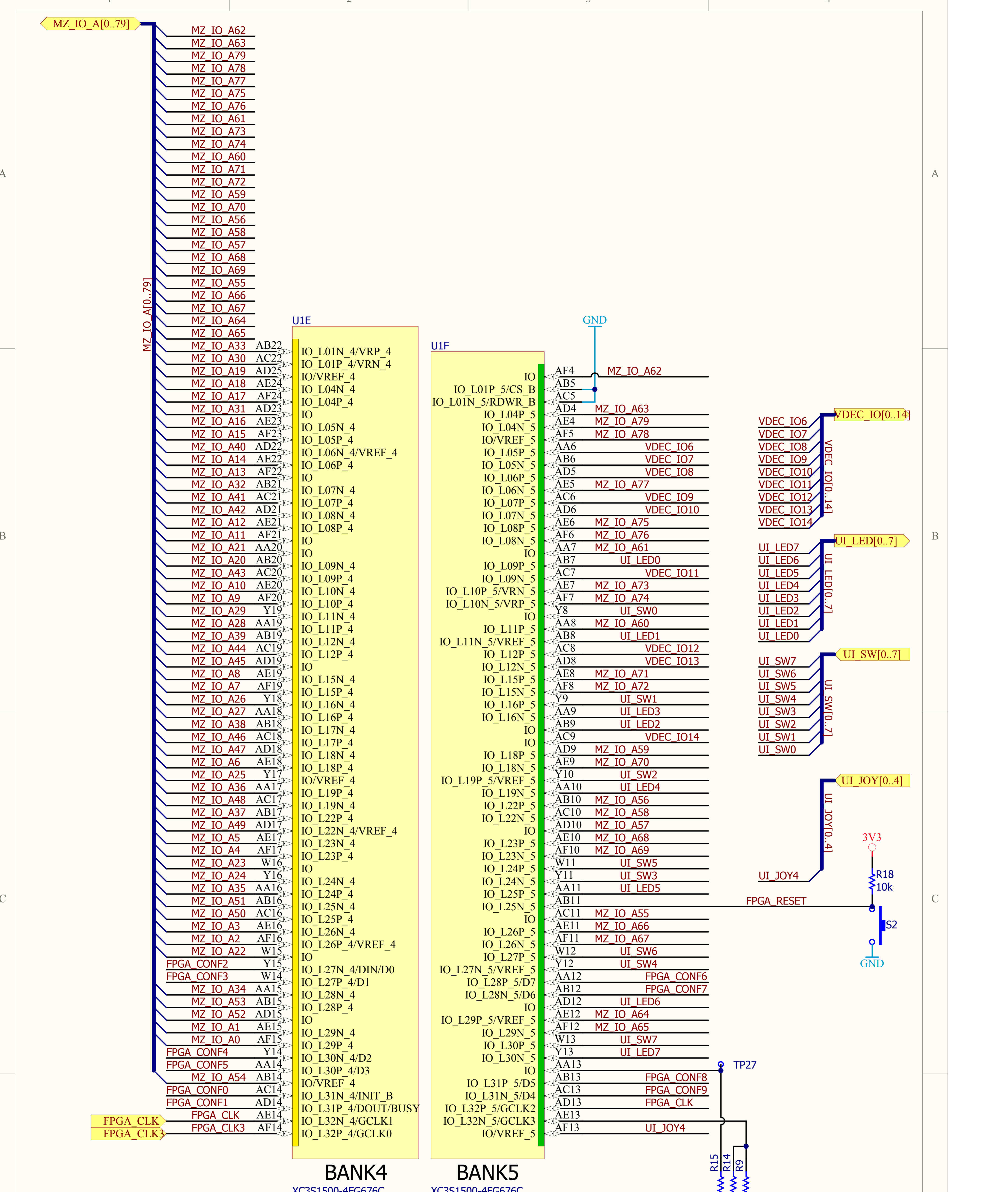


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Title		
TLL5000 FPGA Bank 2/3 Connection		
Size	Number	Revision
A4	P005_3	R002
Date:	25.1.2007	Sheet 3of 27
File:	D:\Working\...\Bank2_3_1_1.SchDoc	Drawn By: Zoltan Pele



FPGA_CONF0[0..9]


- FPGA_CONF0
- FPGA_CONF1
- FPGA_CONF2
- FPGA_CONF3
- FPGA_CONF4
- FPGA_CONF5
- FPGA_CONF6
- FPGA_CONF7
- FPGA_CONF8
- FPGA_CONF9

BANK4
XC3S1500-4FG676C

BANK5
XC3S1500-4FG676C

VENC_CLK VENC_CLK

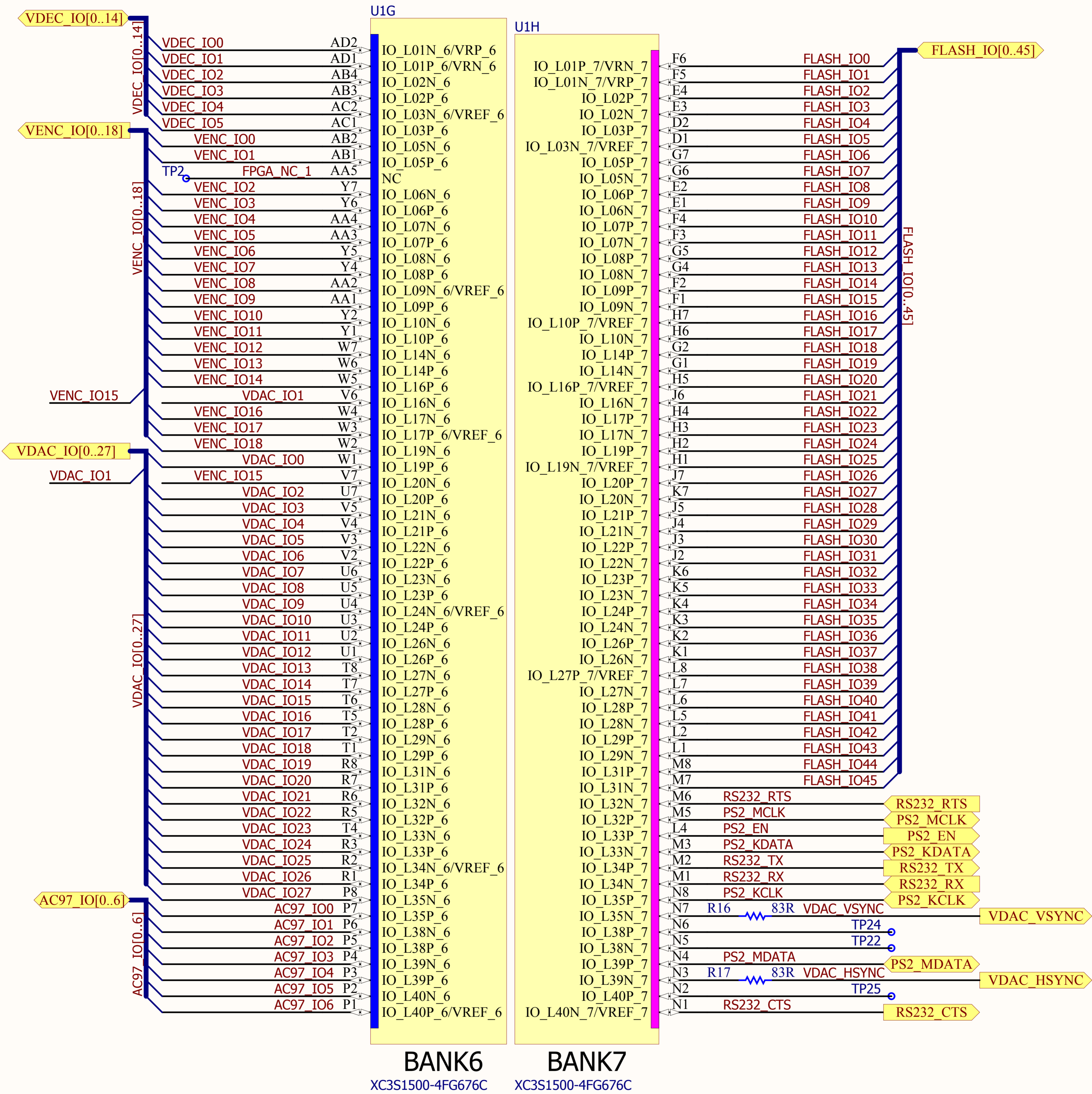
FPGA_CLK4 FPGA_CLK4



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Title: TLL5000 FPGA Bank4/5 Connection			
Size: A4	Number: P005_4	Revision: R002	
Date: 25.1.2007	Sheet 4of 27	Drawn By: Zoltan Pele	
File: D:\Working\...\Bank4_5_1_1.SchDoc			



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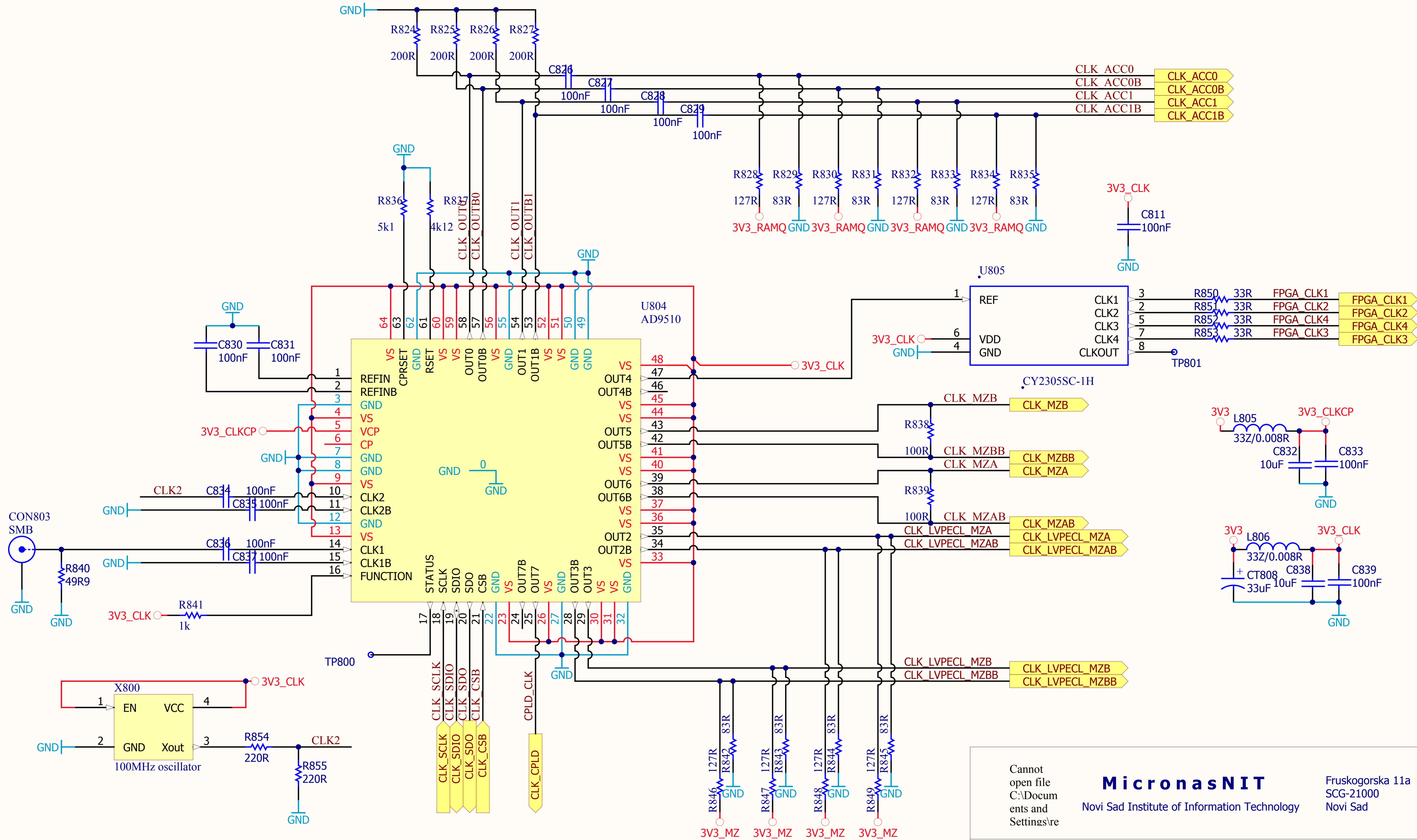
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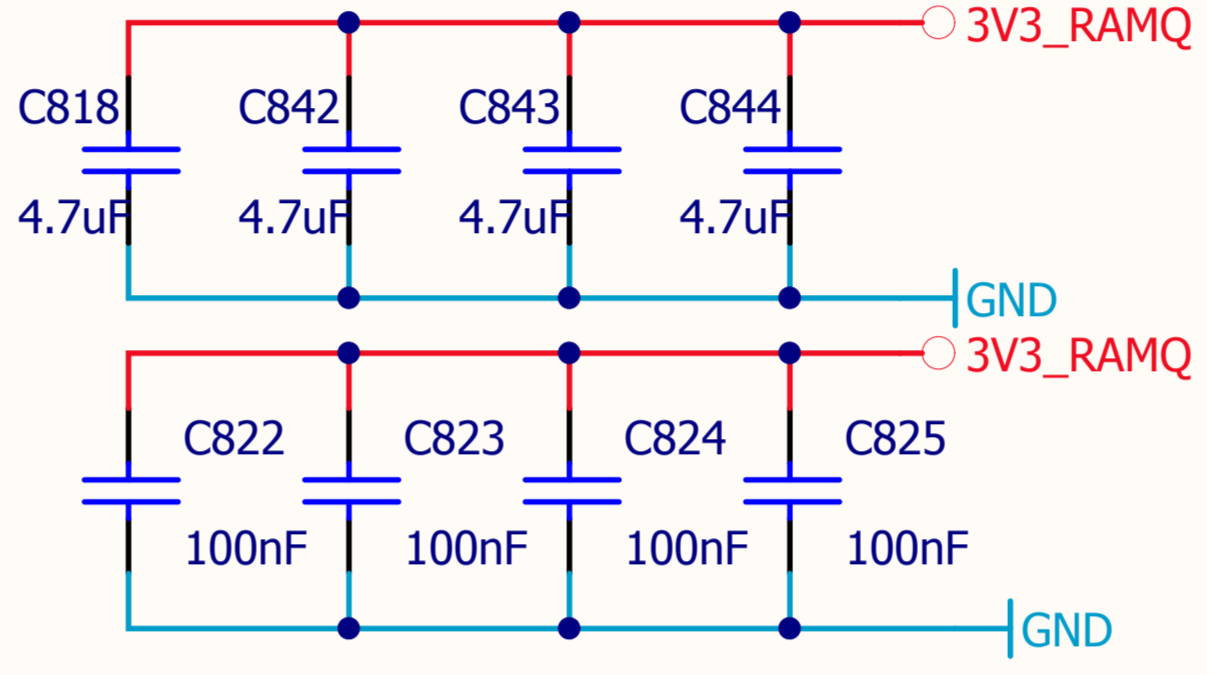
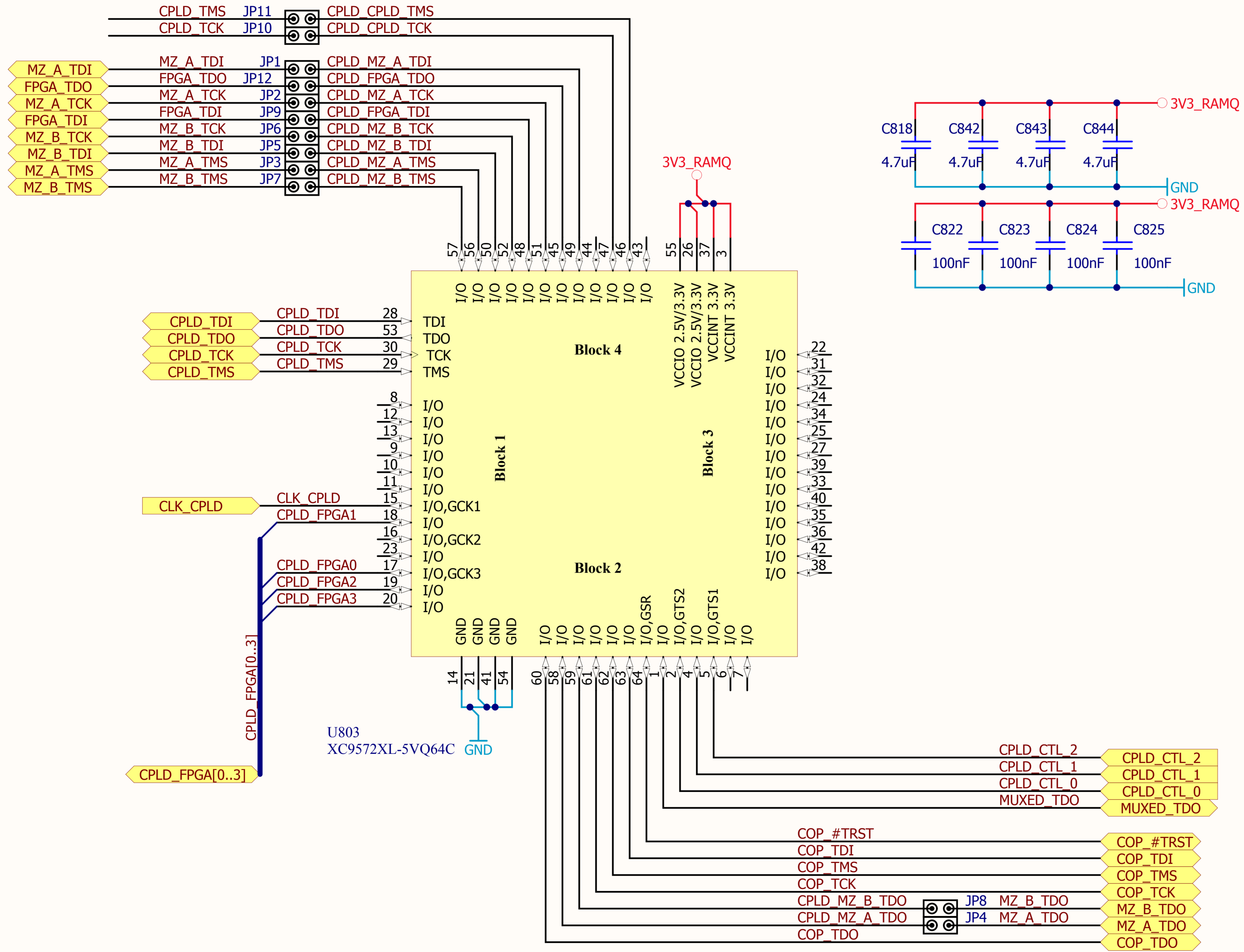
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Size A4	Number P005_5	Revision R002
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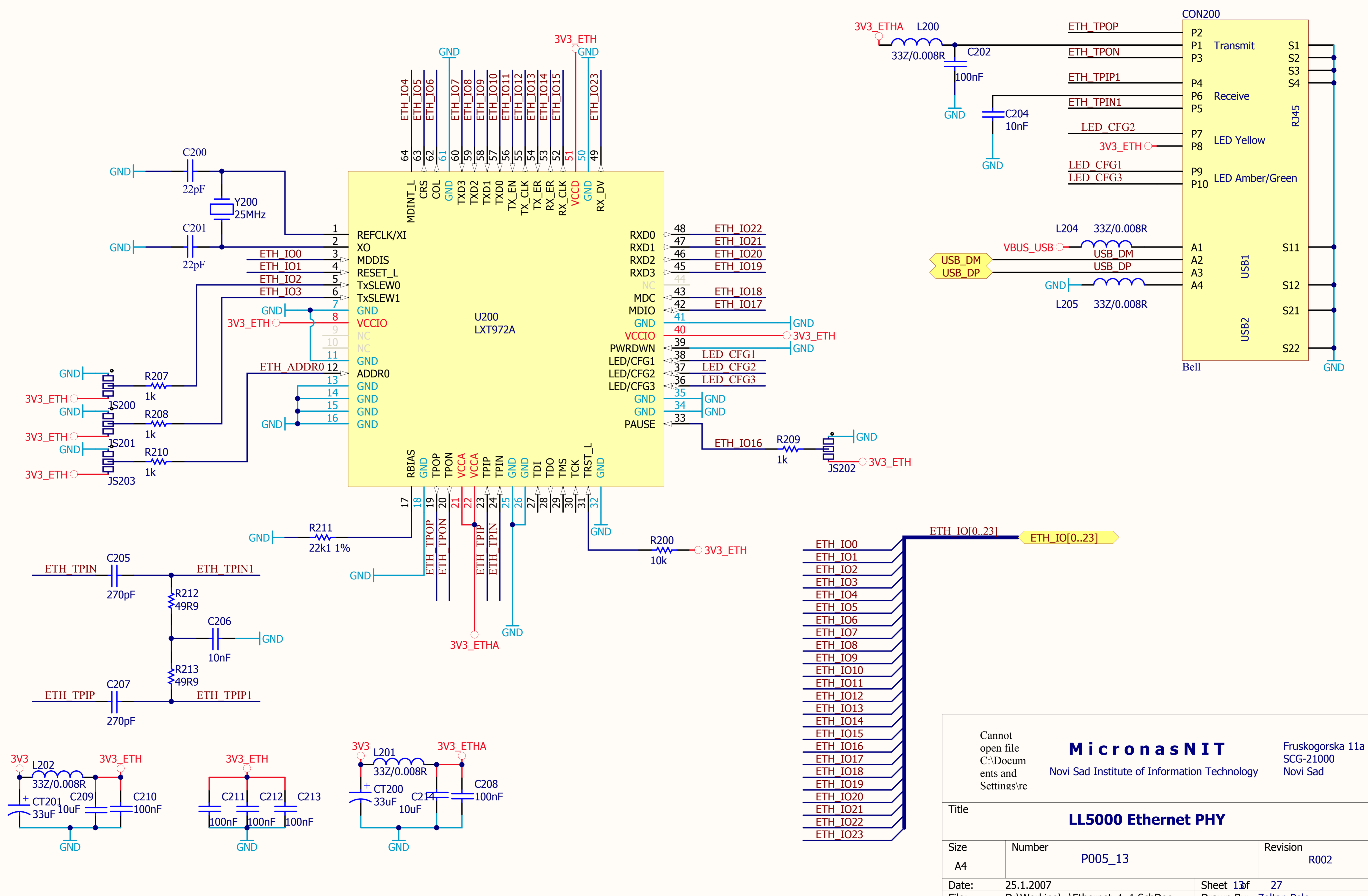
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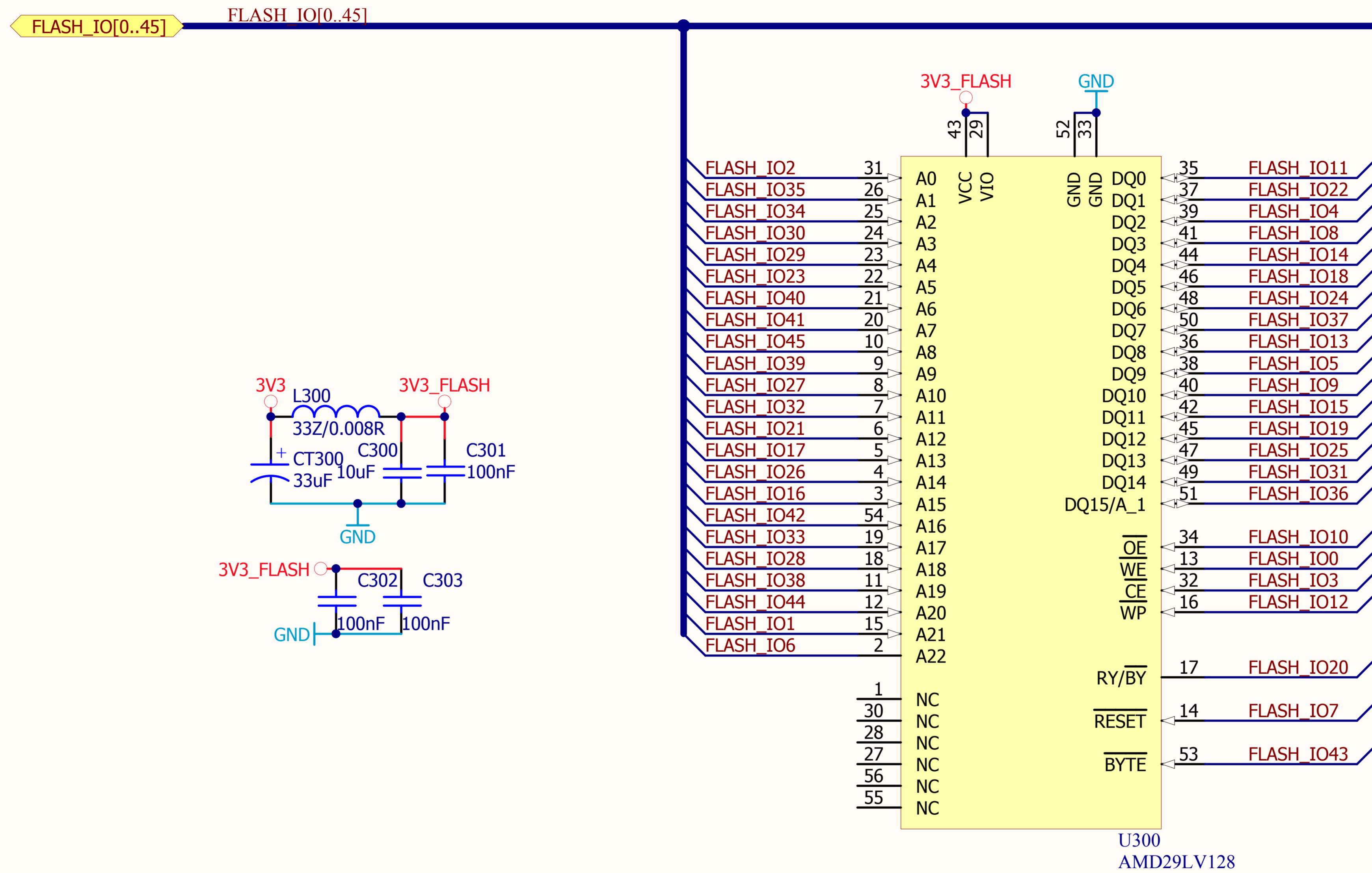
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Title LL5000 Clock Generator			
Size A4	Number P005_23	Revision R002	
Date:	25.1.2007	Sheet 23 of	27
File:	D:\Working\..\ClockGenerator_1_1.SchDoc Drawn By: Ivan Resetar		



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Title		CPLD	
Size A4	Number P005_9	Revision R002	
Date: 25.1.2007	Sheet 9 of 27	Drawn By: Ivan Resetar	
File: D:\Working\..\CPLD_1_1.SchDoc			



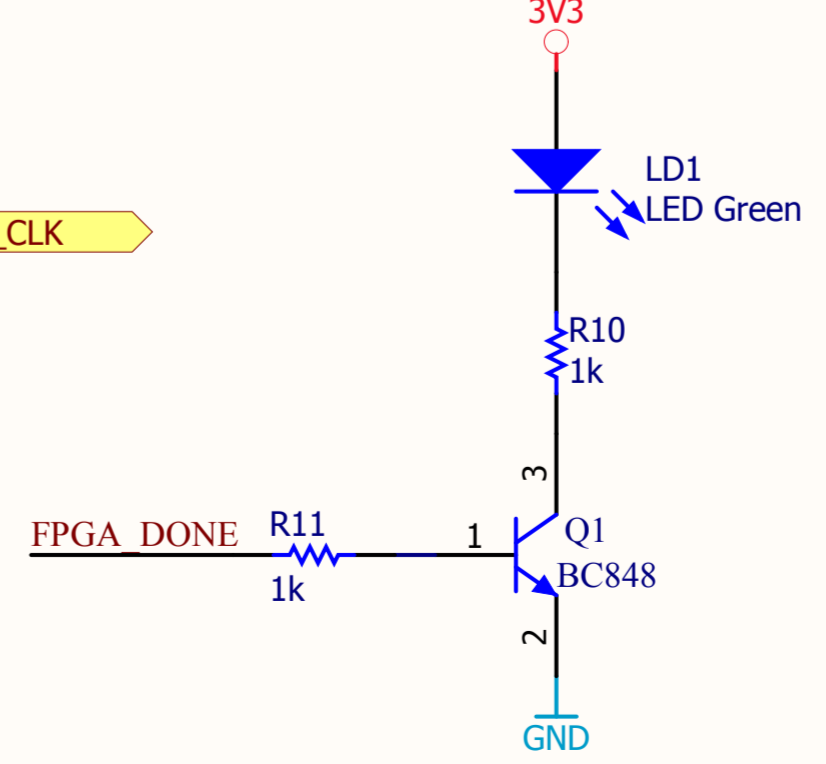
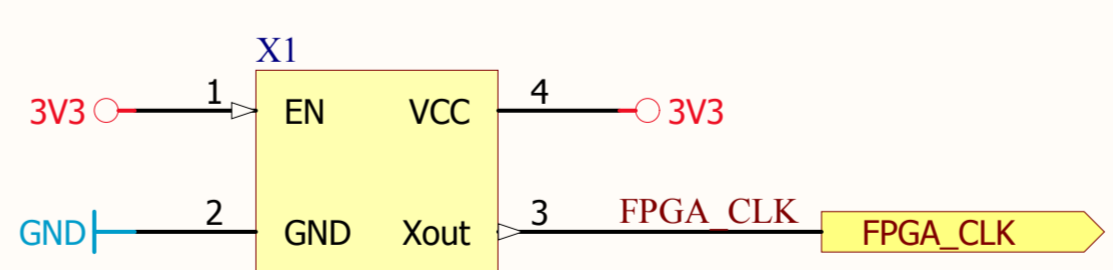
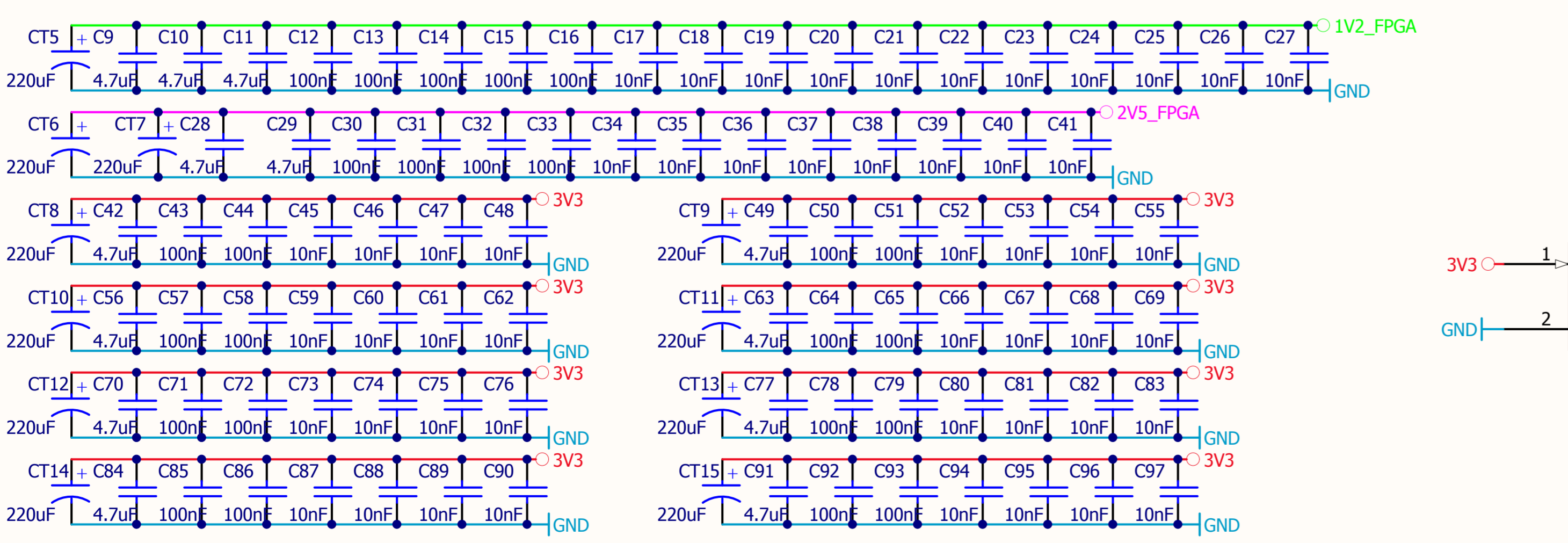
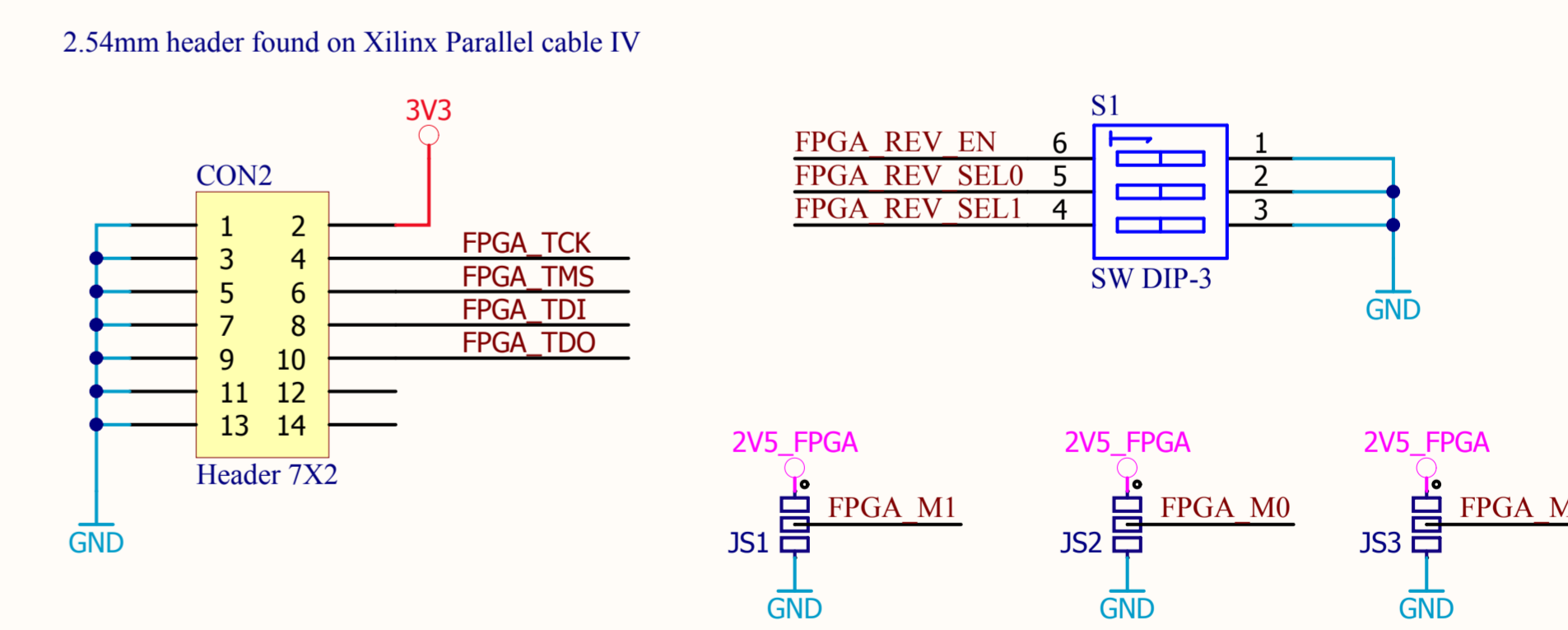
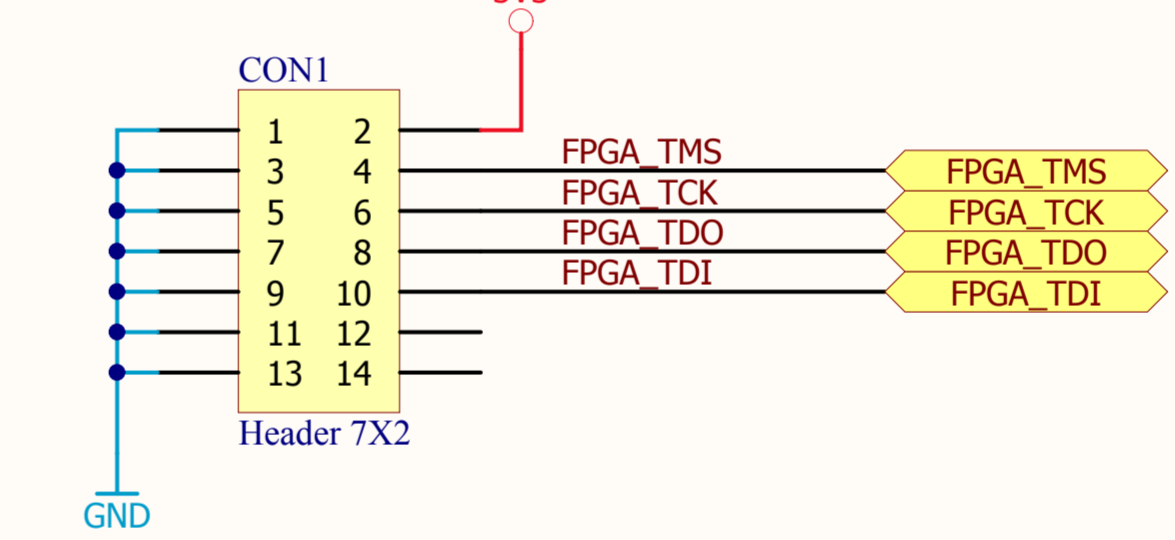
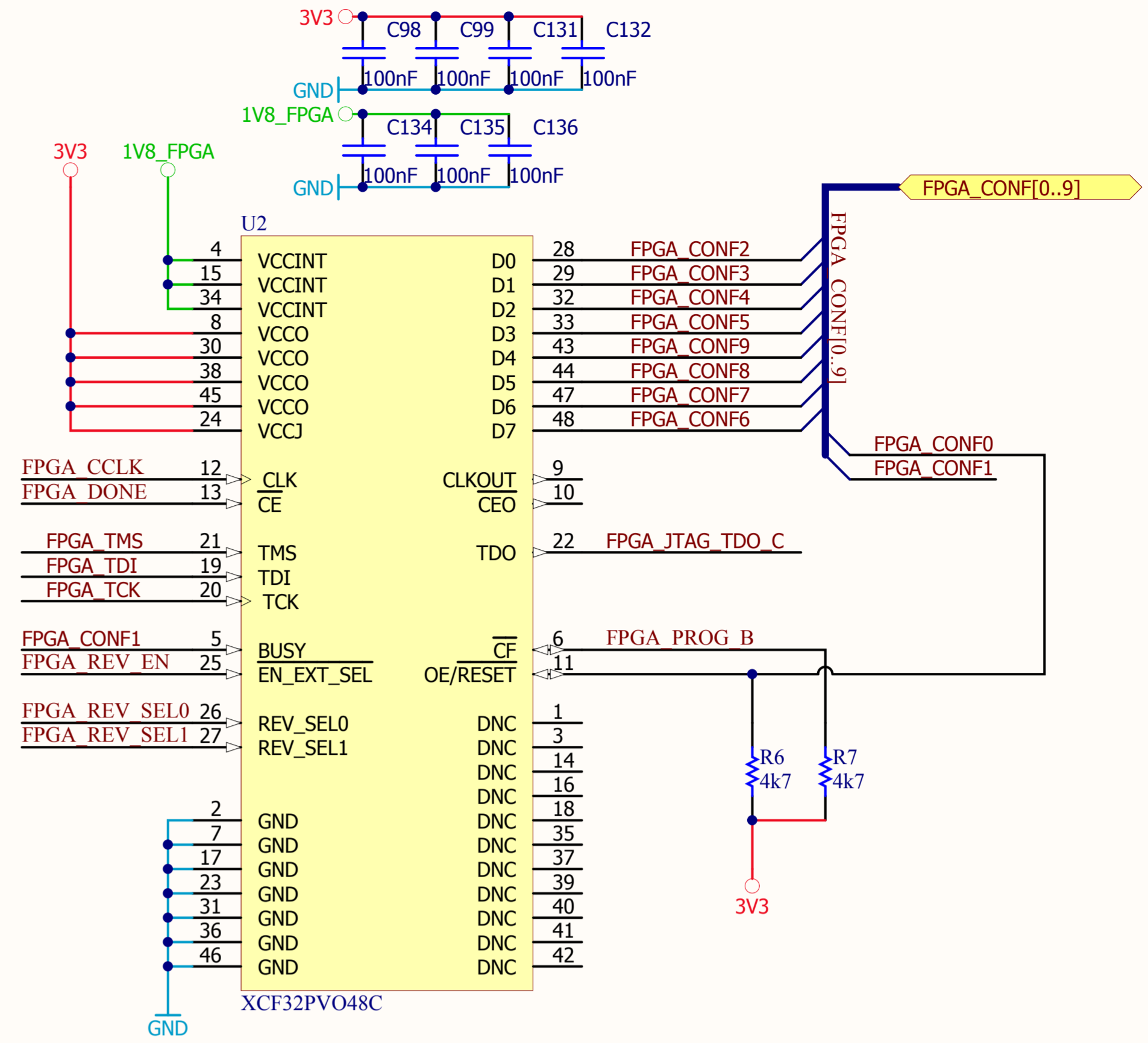
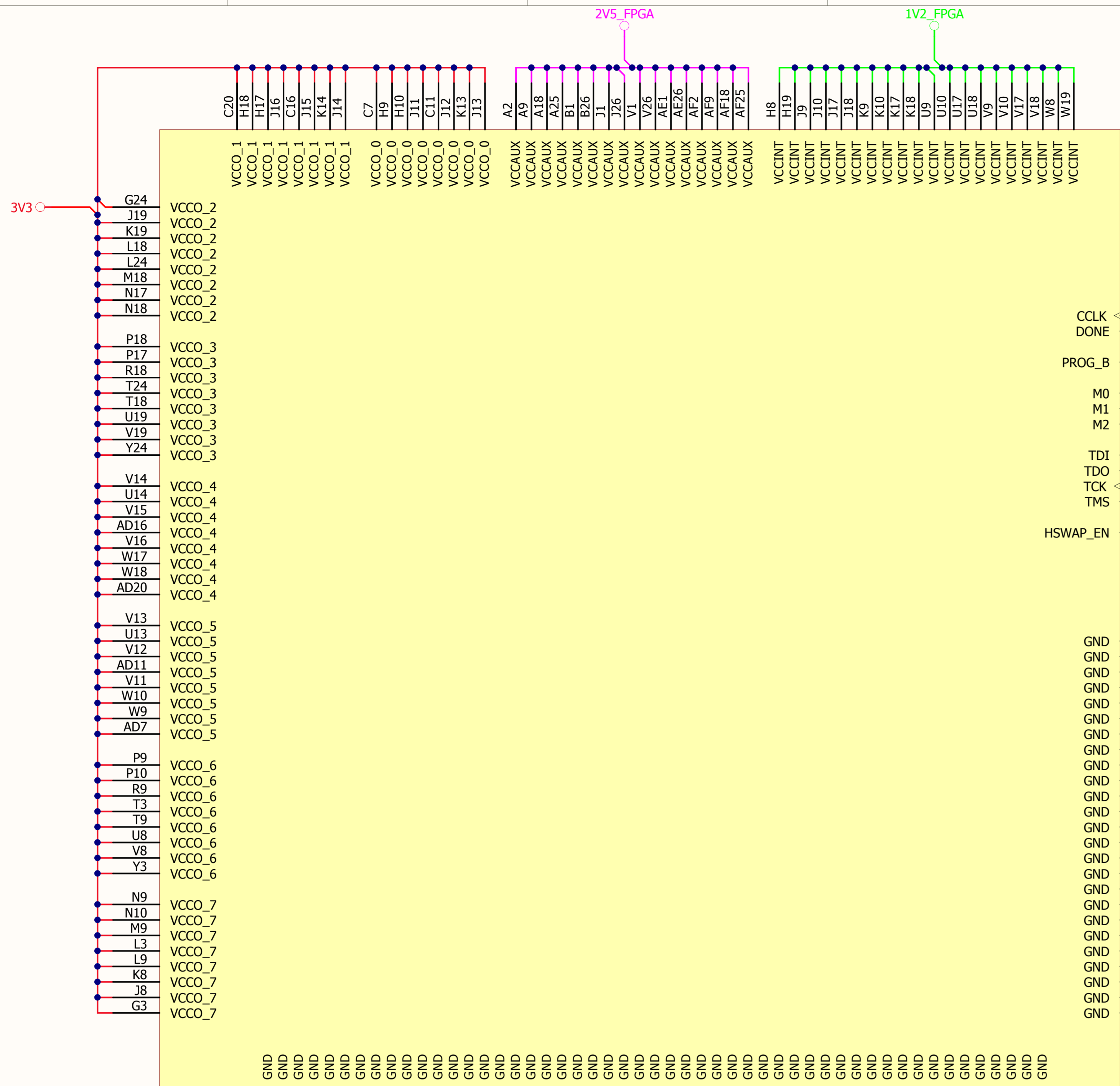
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Title		LL5000 Ethernet PHY	
Size A4	Number P005_13	Revision R002	
Date:	25.1.2007	Sheet 1 of 27	
File:	D:\Working\..\Ethernet_1_1.SchDoc	Drawn By:	Zoltan Pele



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Title			Intel Flash 28F128		
Size	Number	Revision			
A4	P005_15	R002			
Date:	25.1.2007	Sheet 15 of 27			
File:	D:\Working\..\FLASH_1_1.SCHDOC	Drawn By:	Zoltan Pele		



Cannot open file C:\Documents and Settings\ire		MicronasNIT		Fruskogorska 11a SCG-21000 Novi Sad	
Novi Sad Institute of Information Technology					
Title FPGA power supply and JTAG					
Size	A3	Number	P005_6	Revision	R002
Date:	25.1.2007		Sheet 6 of 27		
File:	D:\Working\...\FPGA GND_1.1.SchDoc		Drawn By: Zoltan Pele		

Video Encoder

FPGA BALL	Schematic Net Name	Interface Signal Name
AB2	VENC_IO0	P1
AB1	VENC_IO1	P2
Y7	VENC_IO2	TTX
Y6	VENC_IO3	#CSO/#HSO
AA4	VENC_IO4	P0
AA3	VENC_IO5	#VSO
Y5	VENC_IO6	FIELD/#VSYNC
Y4	VENC_IO7	#RESET
AA2	VENC_IO8	P3
AA1	VENC_IO9	P4
Y2	VENC_IO10	P5
Y1	VENC_IO11	P6
W7	VENC_IO12	TTXREQ
W6	VENC_IO13	#HSYNC
W5	VENC_IO14	#BLANK
V7	VENC_IO15	SCRESET/RTC
W4	VENC_IO16	PAL/#NTSC
W3	VENC_IO17	CLAMP
W2	VENC_IO18	P7

Video Decoder

FPGA BALL	Schematic Net Name	Interface Signal Name
AD2	VDEC_IO0	#RESET
AD1	VDEC_IO1	P1
AB4	VDEC_IO2	P2
AB3	VDEC_IO3	LCC
AC2	VDEC_IO4	P0
AC1	VDEC_IO5	#PWRDWN
AA6	VDEC_IO6	P3
AB6	VDEC_IO7	P4
AD5	VDEC_IO8	P5
AC6	VDEC_IO9	P6
AD6	VDEC_IO10	P7
AC7	VDEC_IO11	SFL
AC8	VDEC_IO12	HS
AD8	VDEC_IO13	#INTRQ
AC9	VDEC_IO14	VS/FIELD

Audio Codec

FPGA BALL	Schematic Net Name	Interface Signal Name
P7	AC97_IO0	SDATA_IN
P6	AC97_IO1	BIT_CLK
P5	AC97_IO2	SDATA_OUT
P4	AC97_IO3	#ID_1
P3	AC97_IO4	#ID_0
P2	AC97_IO5	SYNC
P1	AC97_IO6	#RESET

Video DAC

FPGA BALL	Schematic Net Name	Interface Signal Name
W1	VDAC_IO0	B1
V6	VDAC_IO1	#SYNC
U7	VDAC_IO2	#BLANK
V5	VDAC_IO3	G0
V4	VDAC_IO4	R6
V3	VDAC_IO5	R5
V2	VDAC_IO6	B2
U6	VDAC_IO7	G2
U5	VDAC_IO8	G1
U4	VDAC_IO9	R4
U3	VDAC_IO10	R3
U2	VDAC_IO11	B3
U1	VDAC_IO12	B4
T8	VDAC_IO13	G6
T7	VDAC_IO14	G7
T6	VDAC_IO15	G3
T5	VDAC_IO16	R1
T2	VDAC_IO17	B5
T1	VDAC_IO18	B6
R8	VDAC_IO19	G5
R7	VDAC_IO20	R7
R6	VDAC_IO21	G4
R5	VDAC_IO22	#PSAVE
T4	VDAC_IO23	R2
R3	VDAC_IO24	R0
R2	VDAC_IO25	B7
R1	VDAC_IO26	CLOCK
P8	VDAC_IO27	B0



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Title **TLL5000 FPGA AV Connection List**

Size A4	Number P005_B	Revision R002
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Date: 25.1.2007 Sheet 6 of 27
File: D:\Working\..FPGA_AudioVideo_Connections\By_Ivan_Pesetar

User Interface

FPGA BALL	Schematic Net Name	Interface Signal Name
Y8	UI_SW0	UI_SW0
Y9	UI_SW1	UI_SW1
Y10	UI_SW2	UI_SW2
Y11	UI_SW3	UI_SW3
Y12	UI_SW4	UI_SW4
W11	UI_SW5	UI_SW5
W12	UI_SW6	UI_SW6
W13	UI_SW7	UI_SW7
AB7	UI_LED0	UI_LED0
AB8	UI_LED1	UI_LED1
AB9	UI_LED2	UI_LED2
AA9	UI_LED3	UI_LED3
AA10	UI_LED4	UI_LED4
AA11	UI_LED5	UI_LED5
AD12	UI_LED6	UI_LED6
Y13	UI_LED7	UI_LED7
J22	LCD_IO0	LCD_D3
K22	LCD_IO1	LCD_D2
K21	LCD_IO2	LCD_D1
L21	LCD_IO3	LCD_D0
M21	LCD_IO4	LCD_EN
N21	LCD_IO5	LCD_R/#W
M20	LCD_IO6	LCD_RS
N20	LCD_IO7	LCD_L+
AA21	UI_JOY0	UI_JOY0
AA22	UI_JOY1	UI_JOY1
AB23	UI_JOY2	UI_JOY2
AB24	UI_JOY3	UI_JOY3
AF13	UI_JOY4	UI_JOY4

USB

FPGA BALL	Schematic Net Name	Interface Signal Name
E22	USB_IO0	DATA0
D22	USB_IO1	DATA1
C22	USB_IO2	DATA2
D21	USB_IO3	DATA3
C21	USB_IO4	DATA4
D20	USB_IO5	DATA5
D19	USB_IO6	DATA6
C19	USB_IO7	DATA7
D18	USB_IO8	CLOCKOUT
C18	USB_IO9	STP
D17	USB_IO10	DIR
C17	USB_IO11	NXT
E17	USB_IO12	RESET

Serial Interface

FPGA BALL	Schematic Net Name	Interface Signal Name
N8	PS2_KCLK	PS2_KCLK
M5	PS2_MCLK	PS2_MCLK
N4	PS2_MDATA	PS2_MDATA
M3	PS2_KDATA	PS2_KDATA
L4	PS2_EN	PS2_EN
M2	RS232_TX	RS232_TX
M1	RS232_RX	RS232_RX
N1	RS232_CTS	RS232_CTS
M6	RS232_RTS	RS232_RTS

Ethernet

FPGA BALL	Schematic Net Name	Interface Signal Name
B23	ETH_IO0	MDDIS
A22	ETH_IO1	RESET
B22	ETH_IO2	TxSLEW0
A21	ETH_IO3	TxSLEW1
B21	ETH_IO4	MDINT_L
A20	ETH_IO5	CRS
B20	ETH_IO6	COL
A19	ETH_IO7	TXD3
B19	ETH_IO8	TXD2
B18	ETH_IO9	TXD1
A17	ETH_IO10	TXD0
B17	ETH_IO11	TX_EN
A16	ETH_IO12	TX_CLK
B16	ETH_IO13	TX_ER
A15	ETH_IO14	RX_ER
B15	ETH_IO15	RX_CLK
F14	ETH_IO16	PAUSE
E14	ETH_IO17	MDIO
D14	ETH_IO18	MDC
E15	ETH_IO19	RXD3
E16	ETH_IO20	RXD2
D16	ETH_IO21	RXD1
C15	ETH_IO22	RXD0
A14	ETH_IO23	RX_DV



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Title **TLL5000 FPGA Communication Connection List**

Size A4	Number P005_C	Revision R002
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Date: 25.1.2007 Sheet Of 27
File: D:\Working\...FPGA_Communication_Connection_List_1.1_SchResetar

SDRAM

FPGA BALL	Schematic Net Name	Interface Signal Name
P26	RAM_IO0	DQ1
P25	RAM_IO1	DQ0
P24	RAM_IO2	DQ13
P23	RAM_IO3	DQ12
P22	RAM_IO4	DQ14
P21	RAM_IO5	DQ15
P20	RAM_IO6	DQ2
P19	RAM_IO7	CLK
R26	RAM_IO8	DQ4
R25	RAM_IO9	DQ3
R24	RAM_IO10	DQ11
T23	RAM_IO11	DQ9
R22	RAM_IO12	DQ10
R21	RAM_IO13	DQ5
R20	RAM_IO14	A8
R19	RAM_IO15	CKE
T26	RAM_IO16	DQ7
T25	RAM_IO17	DQ6
T22	RAM_IO18	RAS#
T21	RAM_IO19	DQM0
T20	RAM_IO20	A7
T19	RAM_IO21	A9
U26	RAM_IO22	CAS#
U25	RAM_IO23	WE#
U24	RAM_IO24	DQ8
U23	RAM_IO25	DQM1
U22	RAM_IO26	BA0
U21	RAM_IO27	A5
V25	RAM_IO28	CS#
V24	RAM_IO29	DQ29
V23	RAM_IO30	DQ28
V22	RAM_IO31	A0
U20	RAM_IO32	A6
V20	RAM_IO33	DQM3
W26	RAM_IO34	BA1
W25	RAM_IO35	A11
W24	RAM_IO36	DQ27
W23	RAM_IO37	DQ26
V21	RAM_IO38	A4
W22	RAM_IO39	DQM2
Y26	RAM_IO40	A1
Y25	RAM_IO41	A10
W21	RAM_IO42	A3
W20	RAM_IO43	DQ31
AA26	RAM_IO44	DQ16
AA25	RAM_IO45	A2
Y23	RAM_IO46	DQ25
Y22	RAM_IO47	DQ18
AA24	RAM_IO48	DQ24
AA23	RAM_IO49	DQ23
AB26	RAM_IO50	DQ19
AB25	RAM_IO51	DQ17
Y21	RAM_IO52	DQ21
Y20	RAM_IO53	DQ30
AC26	RAM_IO54	DQ22
AC25	RAM_IO55	DQ20

SD/MMC

FPGA BALL	Schematic Net Name	Interface Signal Name
J21	MMC_IO0	DI/CD/CMD
K20	MMC_IO1	SW_CI
H21	MMC_IO2	CD/DAT3
J20	MMC_IO3	DAT2
L19	MMC_IO4	Do/DAT0
L20	MMC_IO5	CLK
M19	MMC_IO6	DAT1
N19	MMC_IO7	SW_WP

FLASH

FPGA BALL	Schematic Net Name	Interface Signal Name
F6	FLASH_IO0	WE#
F5	FLASH_IO1	A21
E4	FLASH_IO2	A0
E3	FLASH_IO3	CE#
D2	FLASH_IO4	DQ2
D1	FLASH_IO5	DQ9
G7	FLASH_IO6	A22
G6	FLASH_IO7	RESET#
E2	FLASH_IO8	DQ3
E1	FLASH_IO9	DQ10
F4	FLASH_IO10	OE#
F3	FLASH_IO11	DQ0
G5	FLASH_IO12	WP#
G4	FLASH_IO13	DQ8
F2	FLASH_IO14	DQ4
F1	FLASH_IO15	DQ11
H7	FLASH_IO16	A15
H6	FLASH_IO17	A13
G2	FLASH_IO18	DQ5
G1	FLASH_IO19	DQ12
H5	FLASH_IO20	RY/BY#
J6	FLASH_IO21	A12
H4	FLASH_IO22	DQ1
H3	FLASH_IO23	A5
H2	FLASH_IO24	DQ6
H1	FLASH_IO25	DQ13
J7	FLASH_IO26	A14
K7	FLASH_IO27	A10
J5	FLASH_IO28	A18
J4	FLASH_IO29	A4
J3	FLASH_IO30	A3
J2	FLASH_IO31	DQ14
K6	FLASH_IO32	A11
K5	FLASH_IO33	A17
K4	FLASH_IO34	A2
K3	FLASH_IO35	A1
K2	FLASH_IO36	DQ15/A_1
K1	FLASH_IO37	DQ7
L8	FLASH_IO38	A19
L7	FLASH_IO39	A9
L6	FLASH_IO40	A6
L5	FLASH_IO41	A7
L2	FLASH_IO42	A16
L1	FLASH_IO43	BYTE#
M8	FLASH_IO44	A20
M7	FLASH_IO45	A8



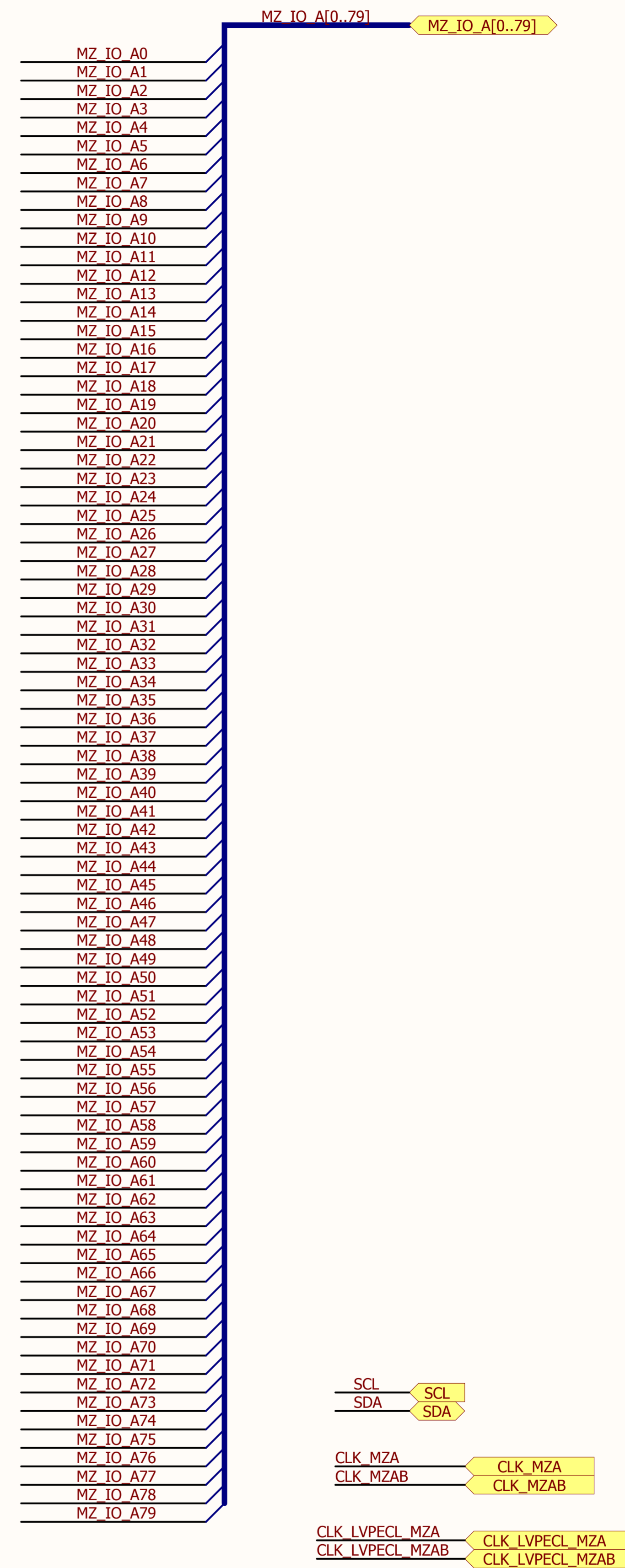
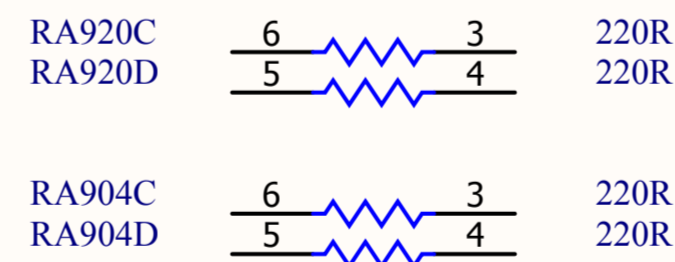
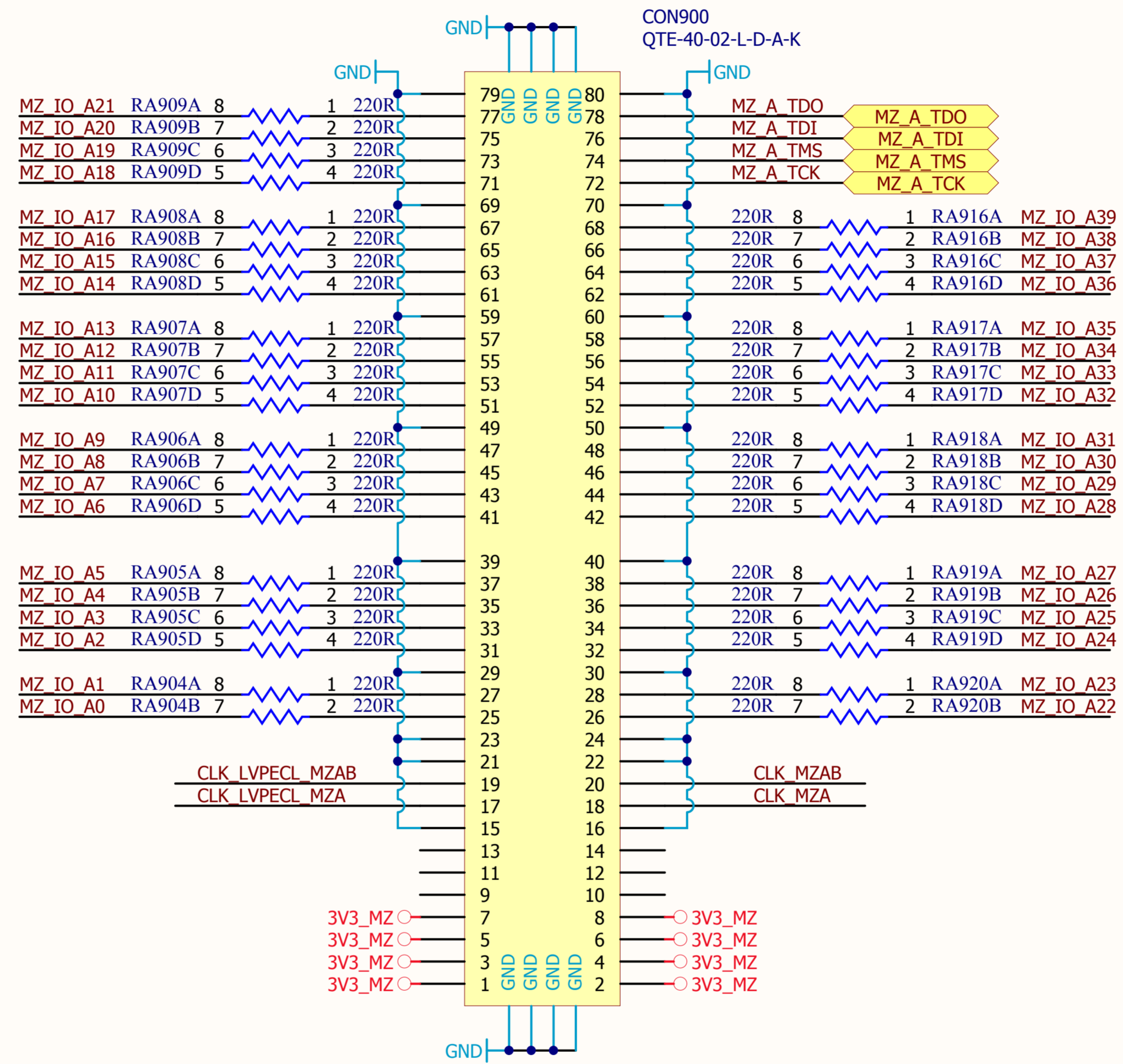
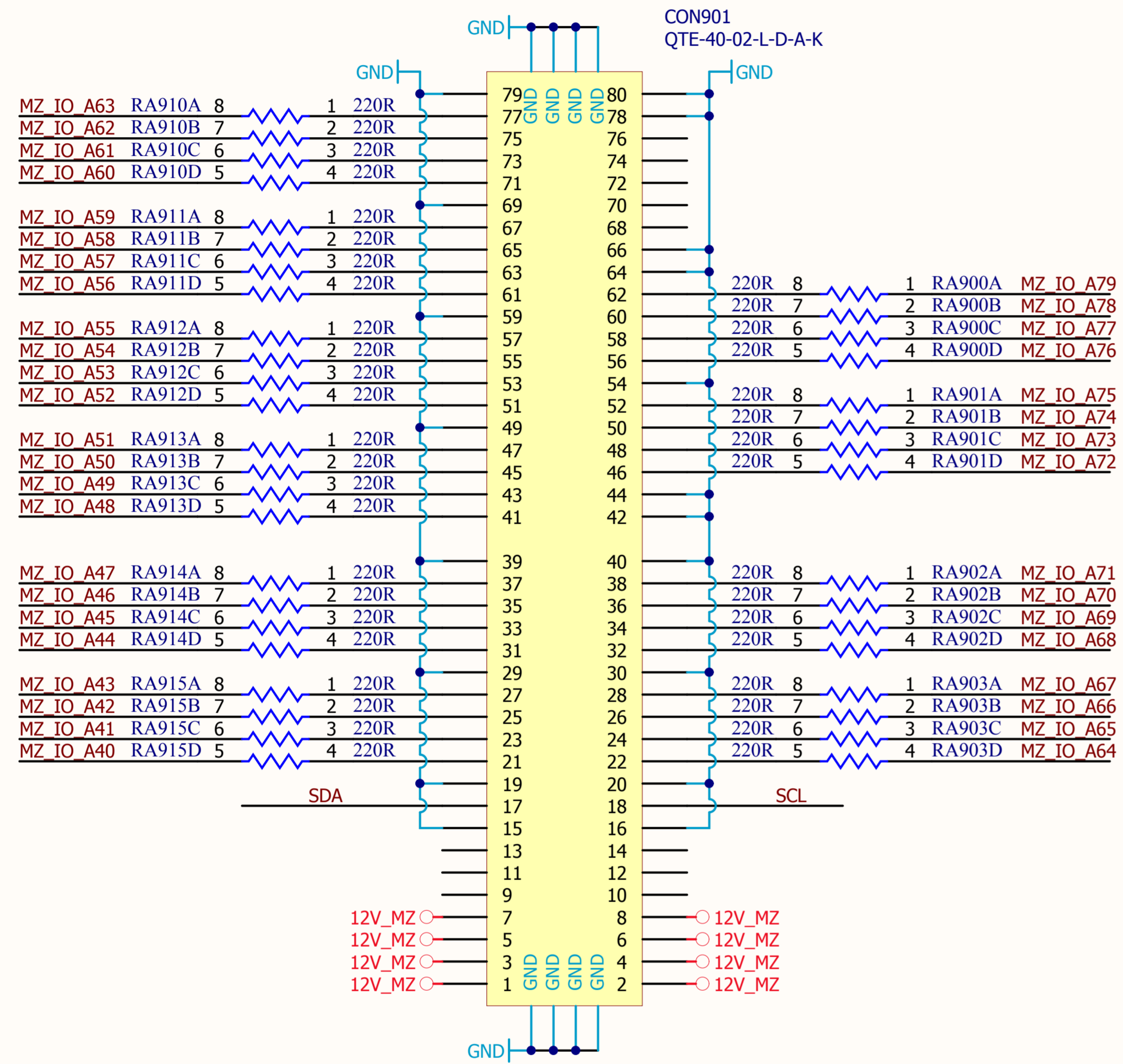
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Novi Sad
SRB-21000

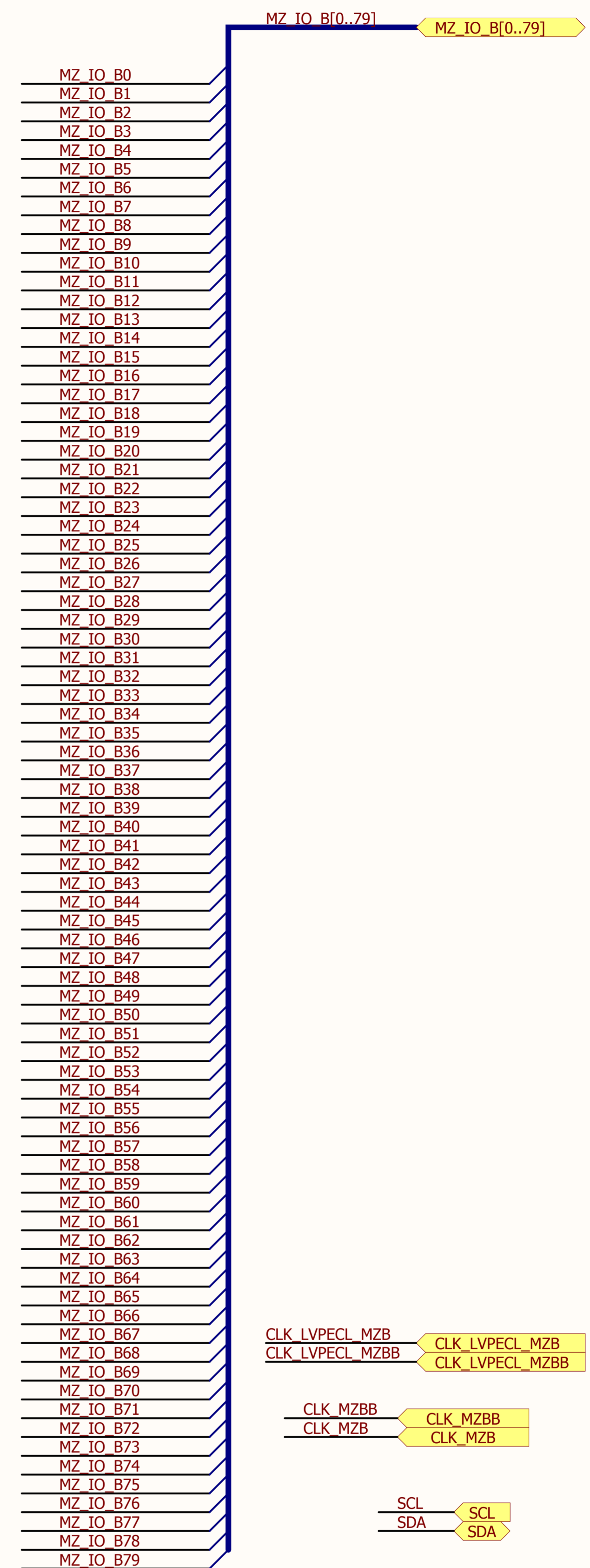
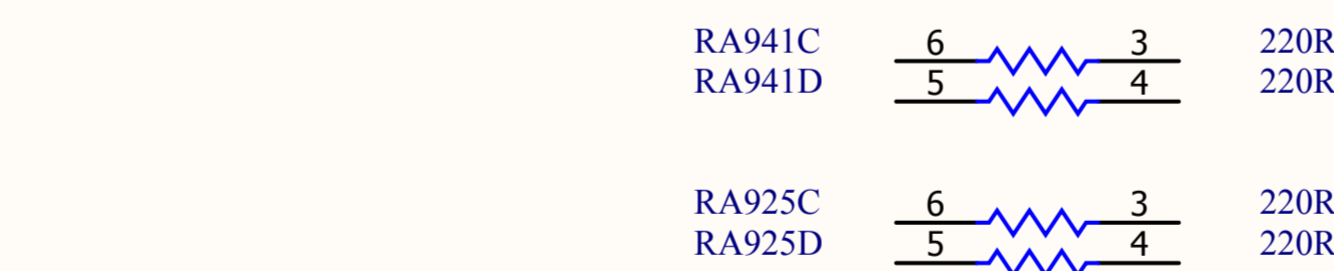
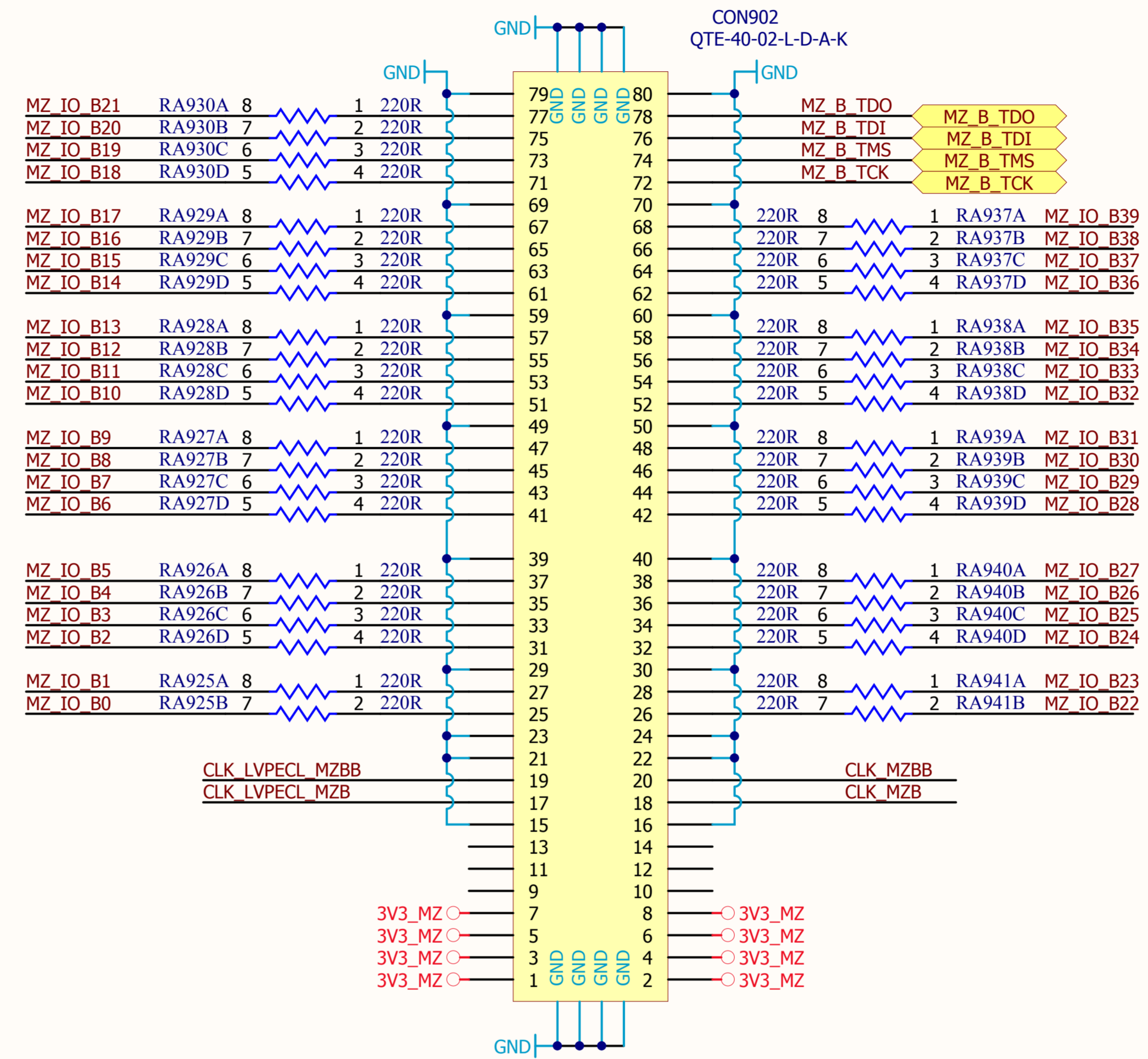
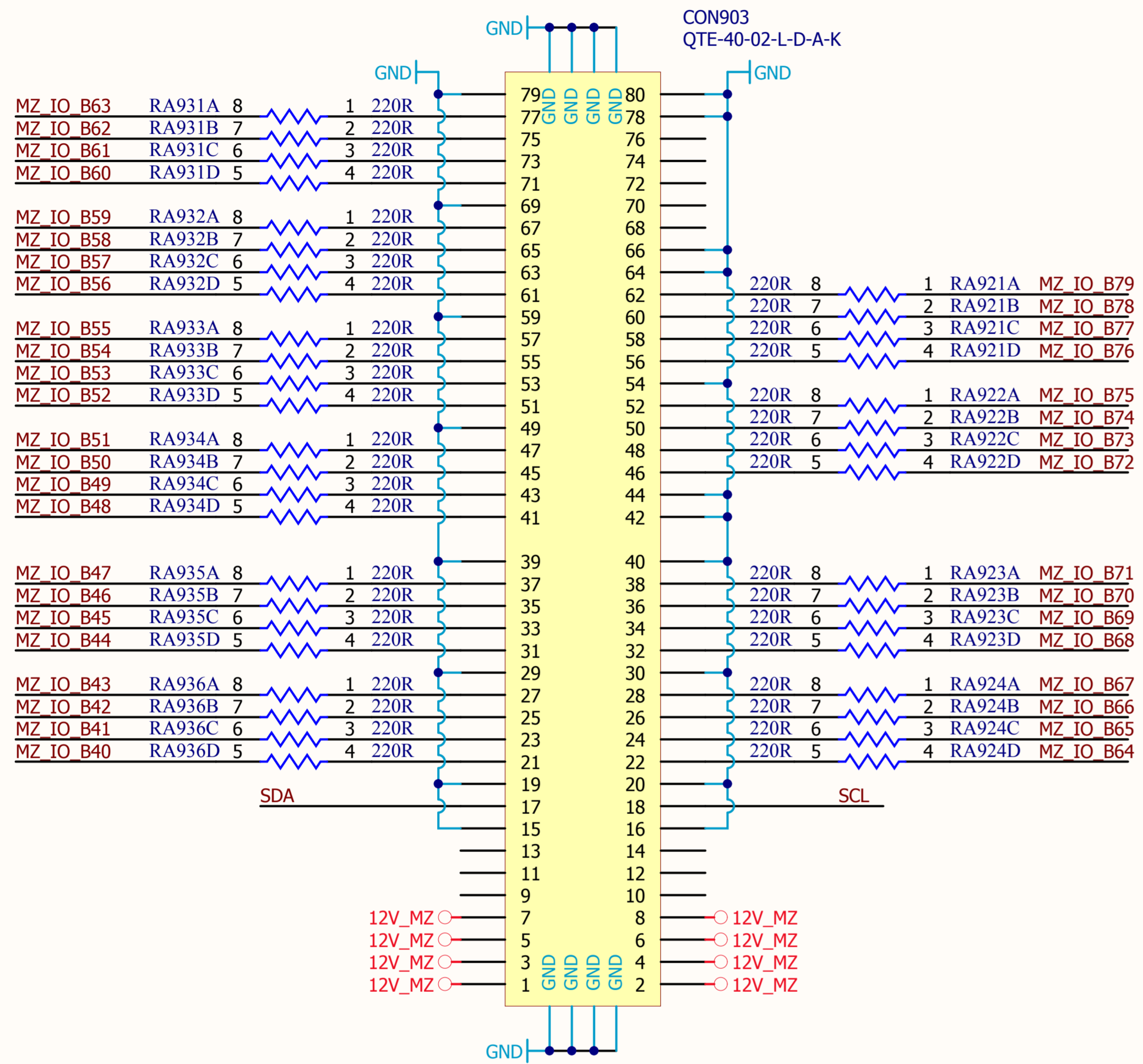
Title **TLL5000 FPGA Memory Connection List**

Size A4	Number P005_D	Revision R002
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Date: 25.1.2007 Sheet Df 27
File: D:\Working\..FPGA_Memory_Connection_List\Drawn By: S. N. Reseter



Cannot open file C:\Docum ents and Settings\re		MicronasNIT Novi Sad Institute of Information Technology		Fruskogorska 11a SCG-21000 Novi Sad	
Title Mezzanine A board conenctors					
Size A3	Number P005_11	Revision R002			
Date:	25.1.2007	Sheet 1bf	27		
File:	D:\Working\...\Mezzanine A conn_1.1.Sch		Drawn By:	Zoltan Pele	



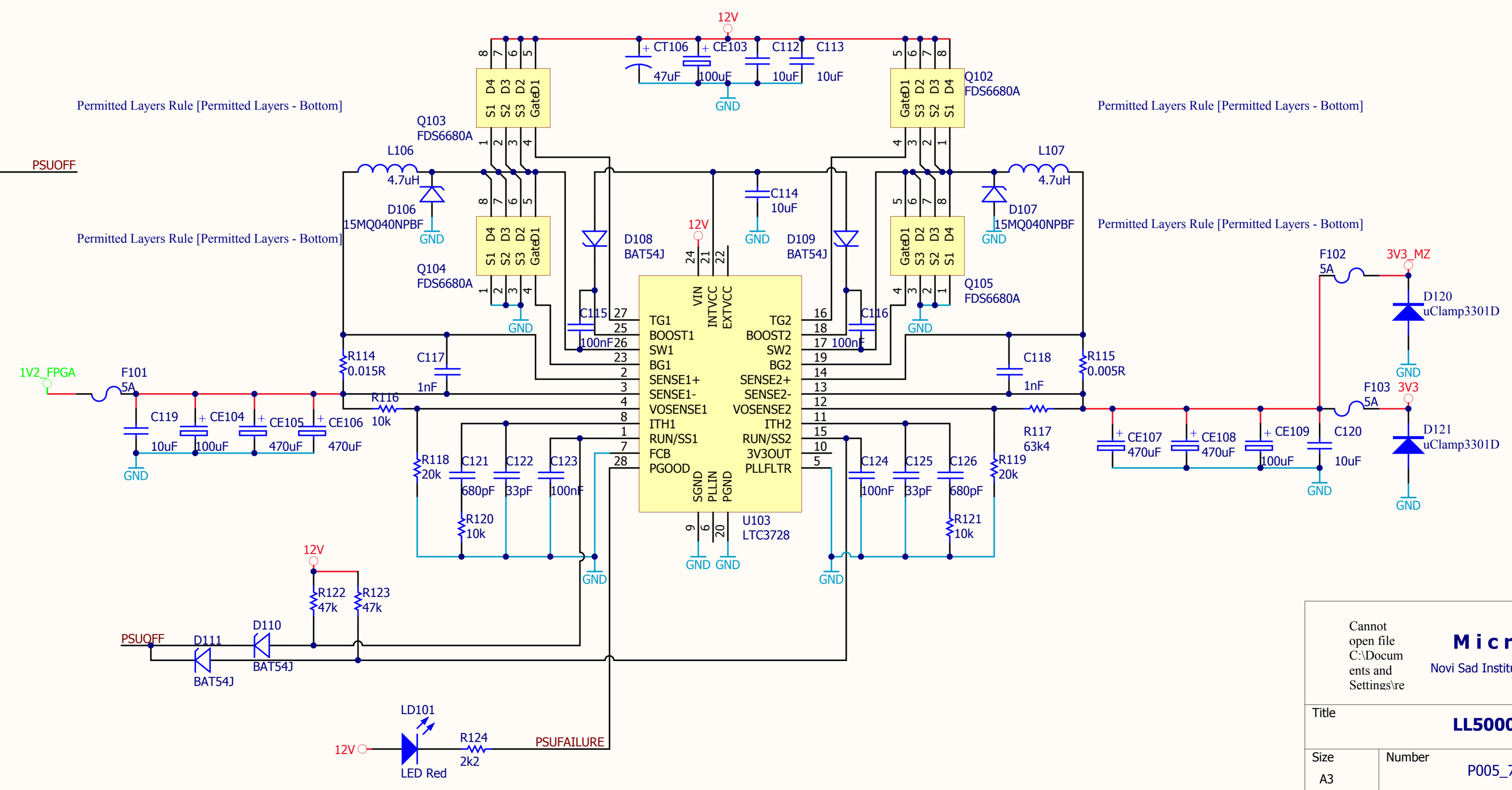
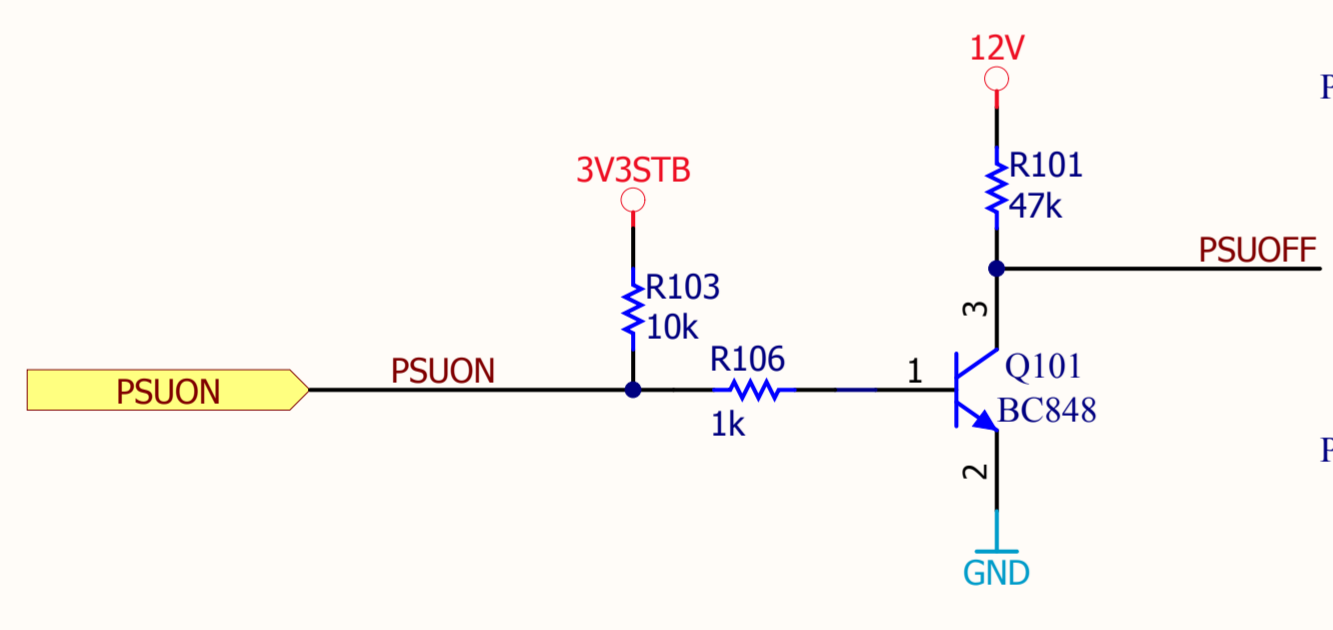
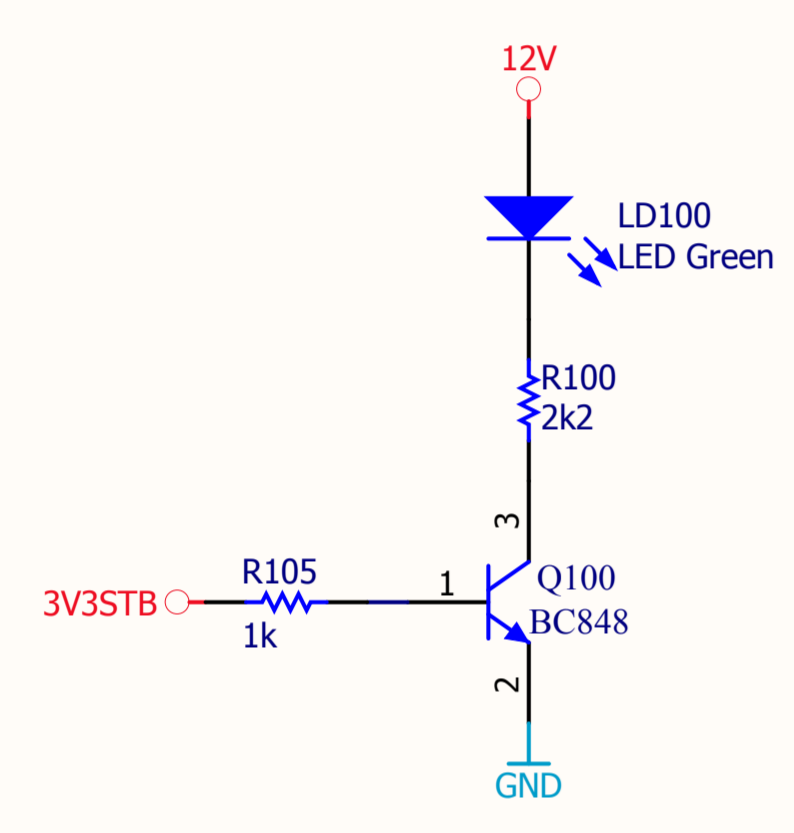
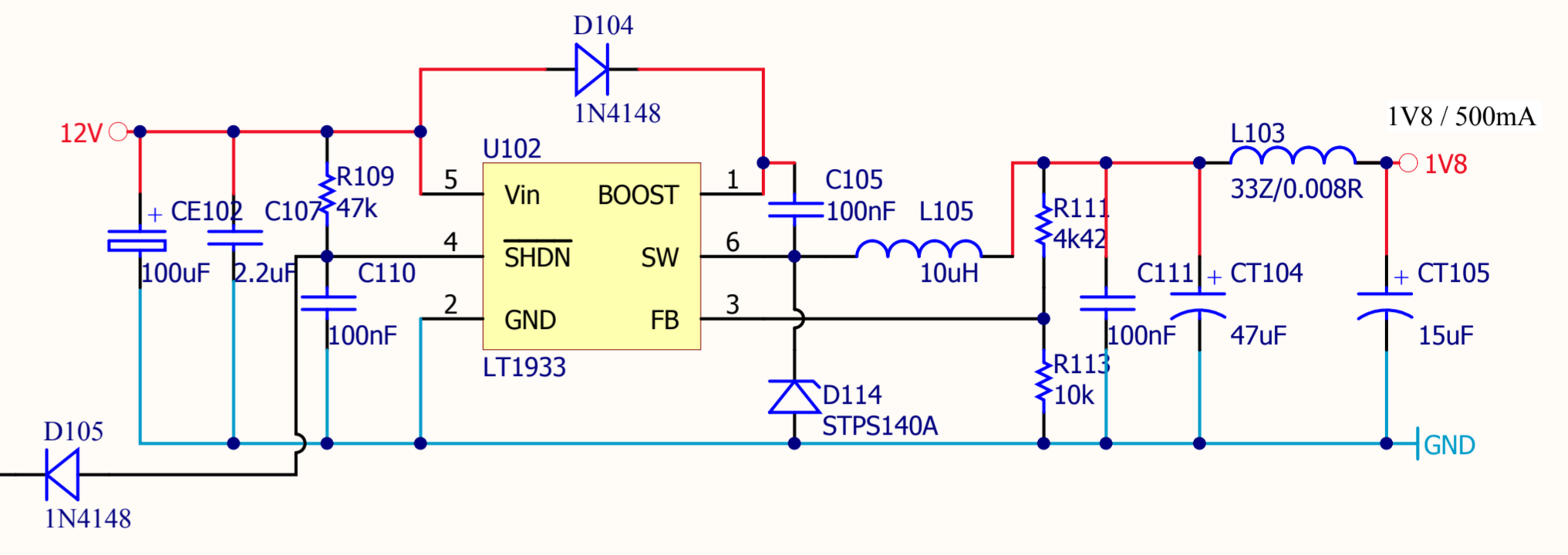
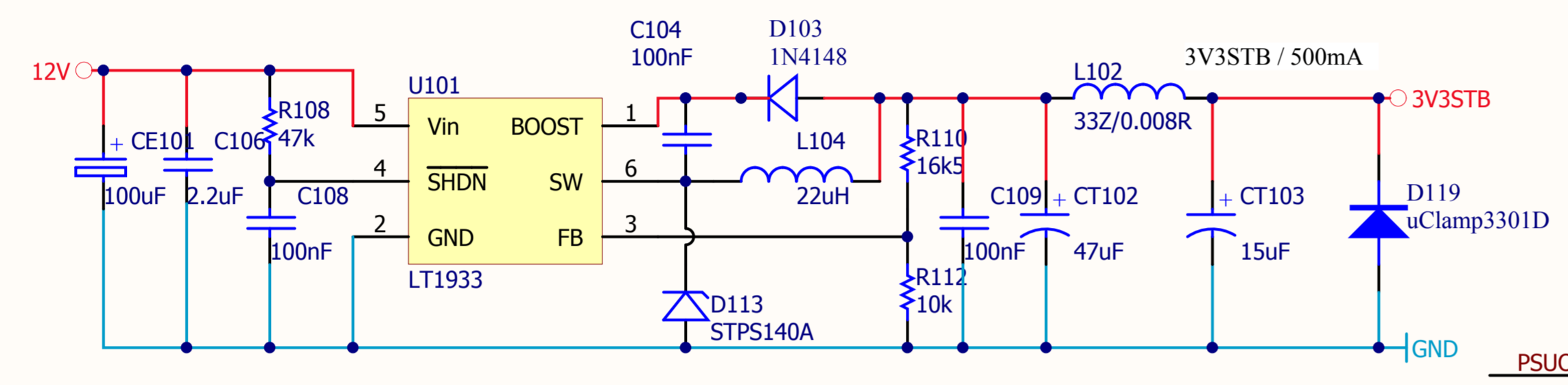
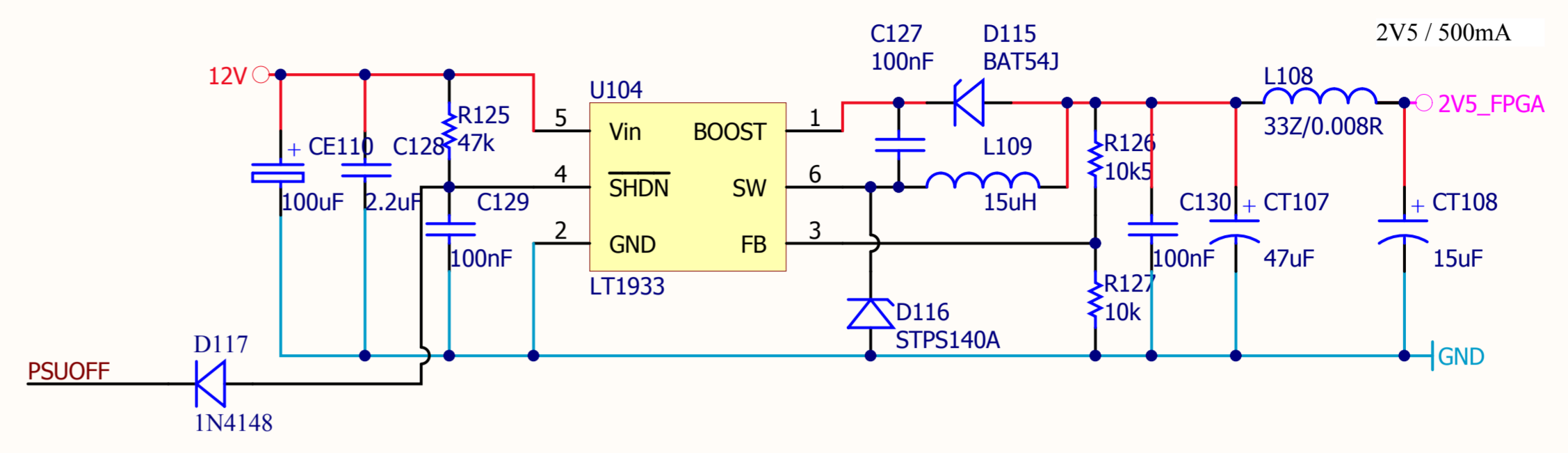
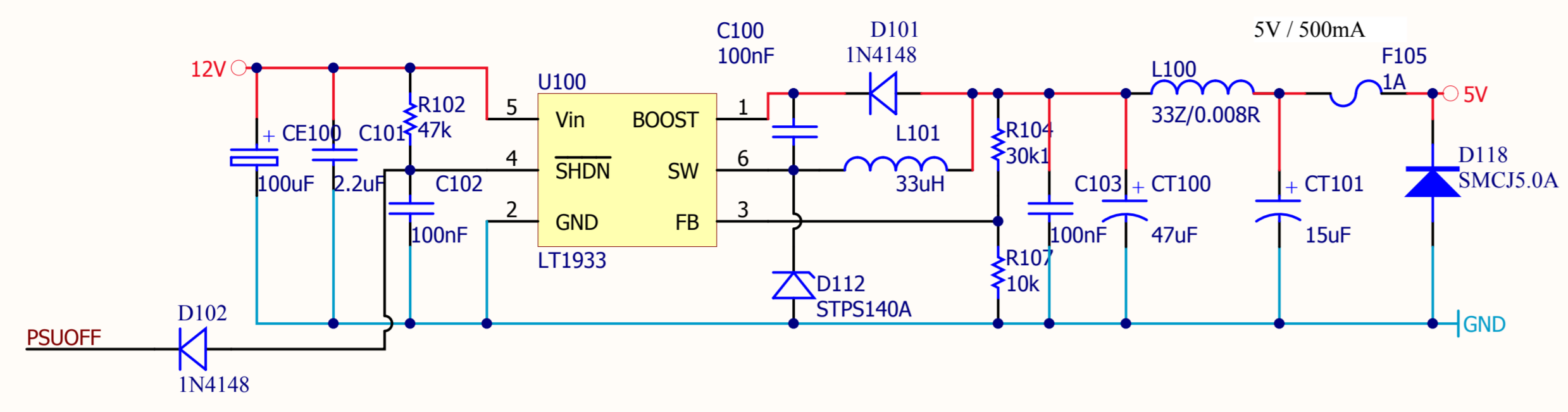
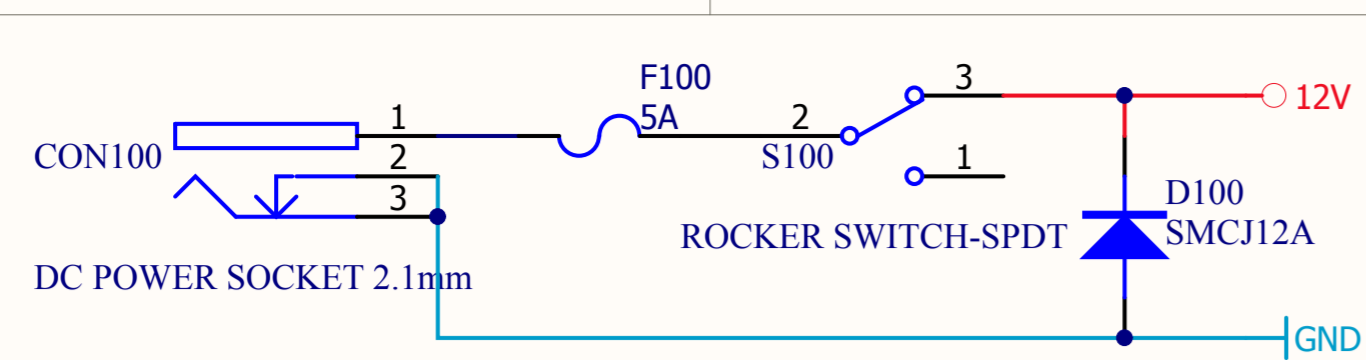
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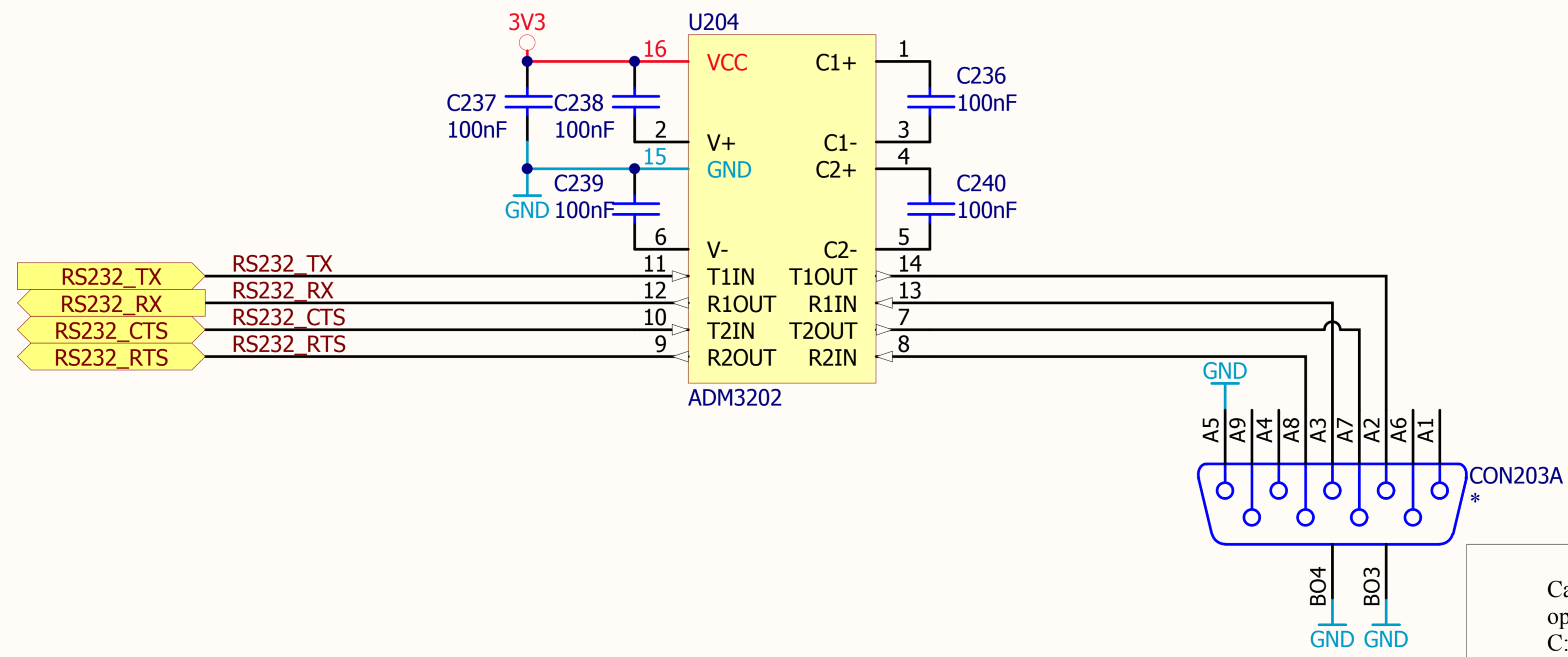
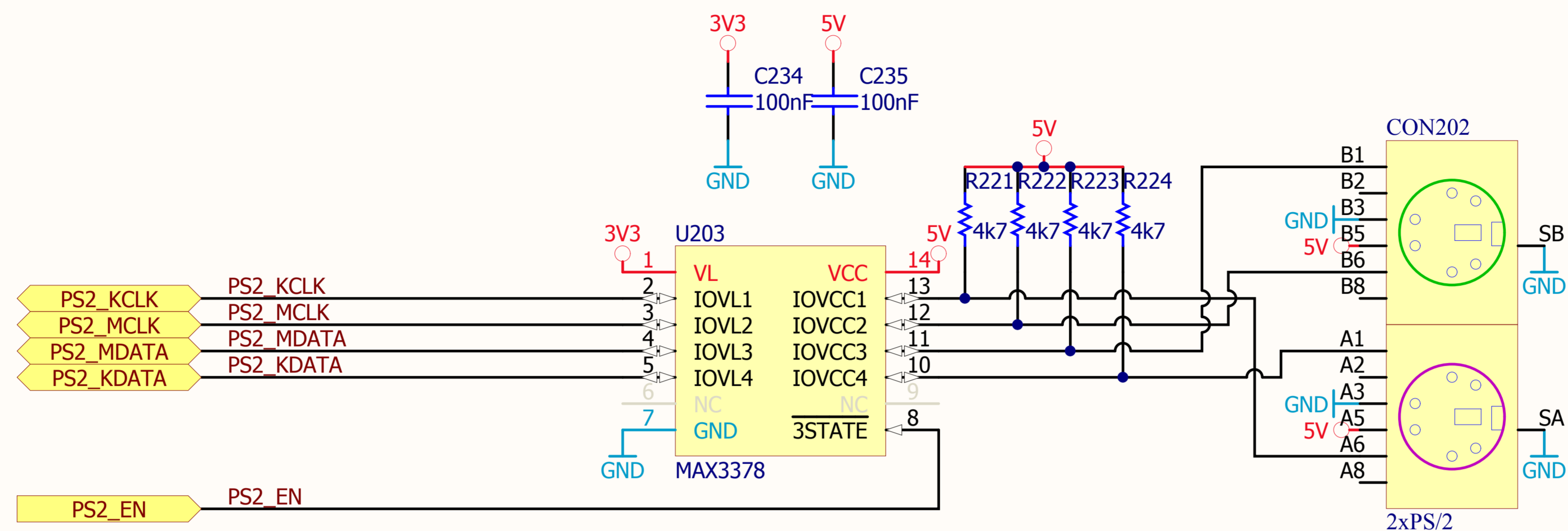
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Title: **Mezzanine B board connectors**

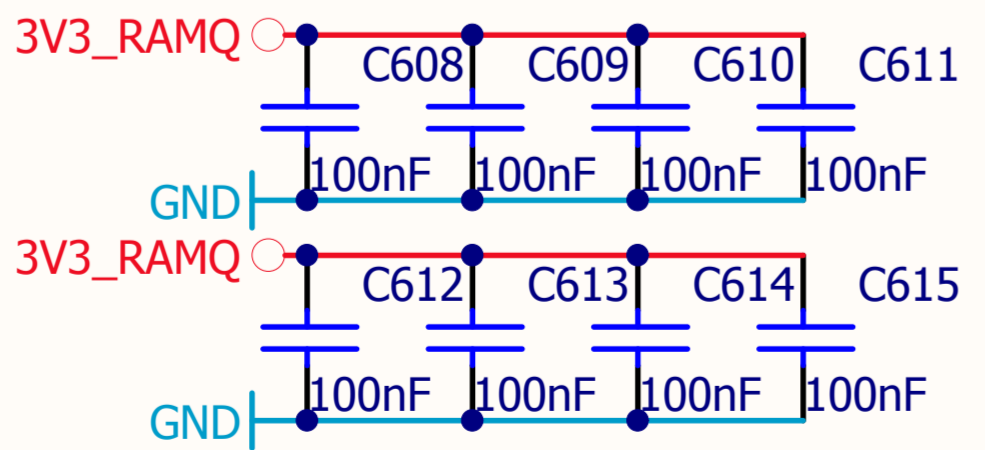
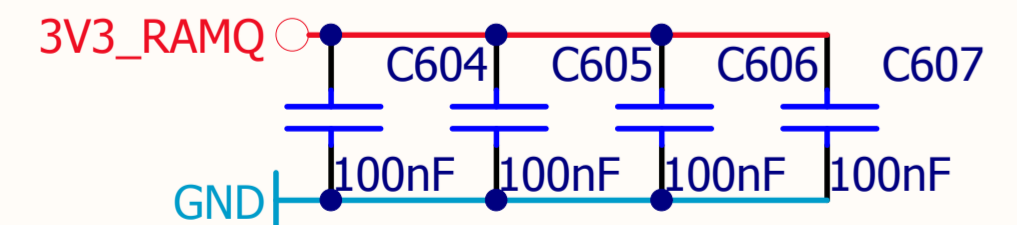
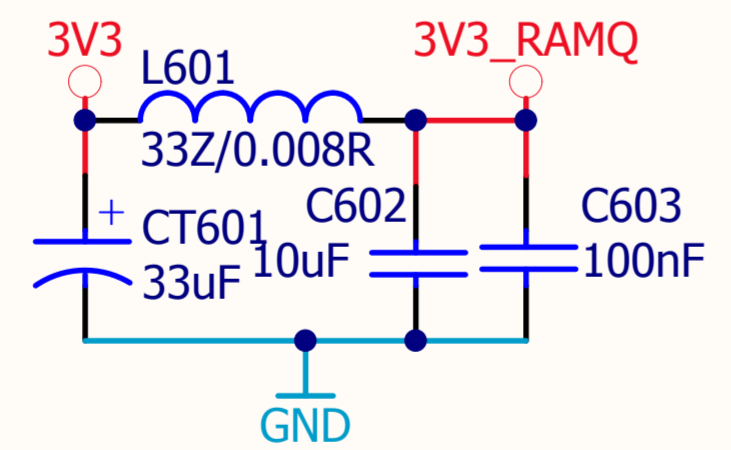
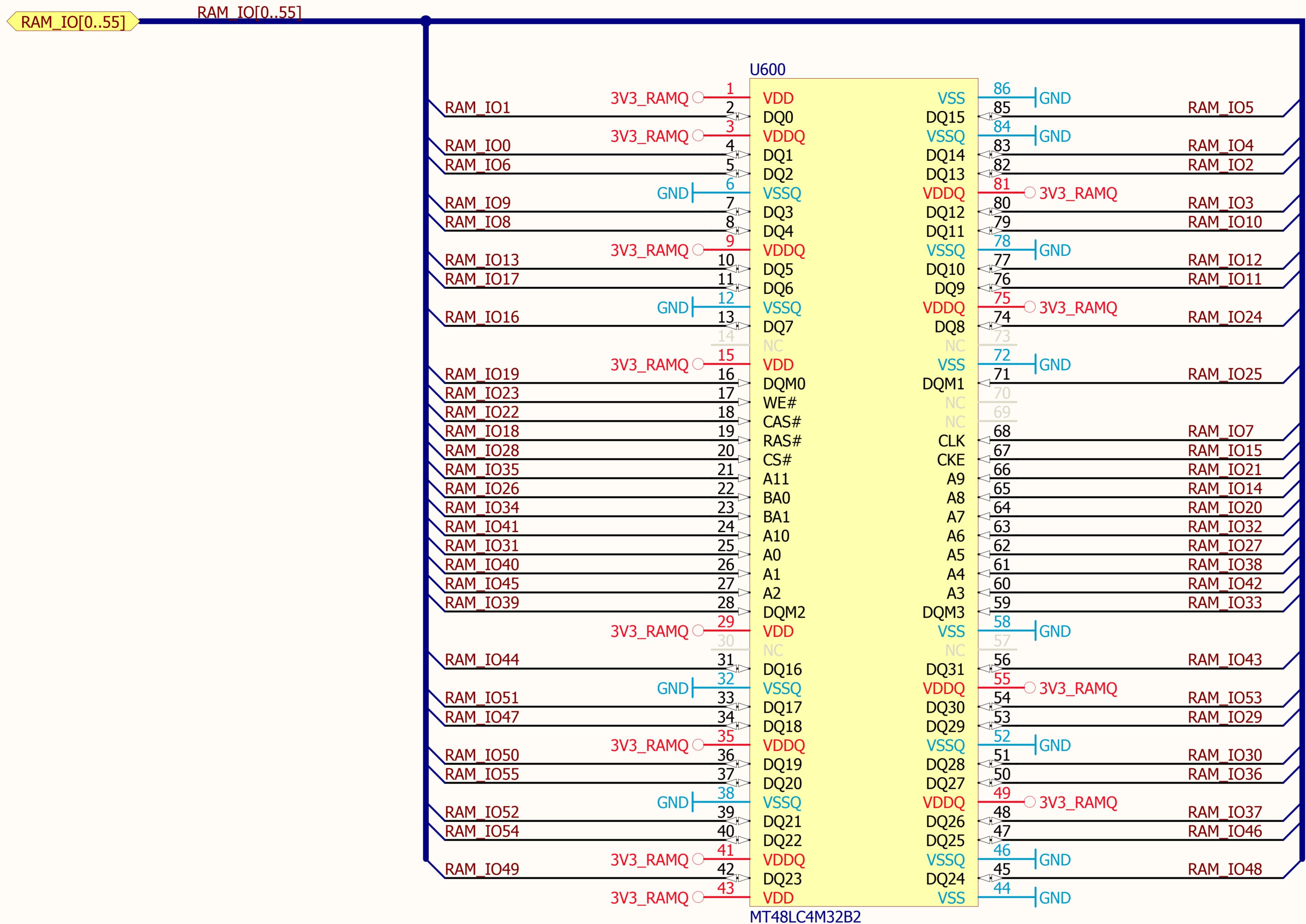
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Date: 25.1.2007	Sheet 1 of 27	Drawn By: Zoltan Pele
File: D:\Working\...\Mezzanine B conn_1.1.Sch		



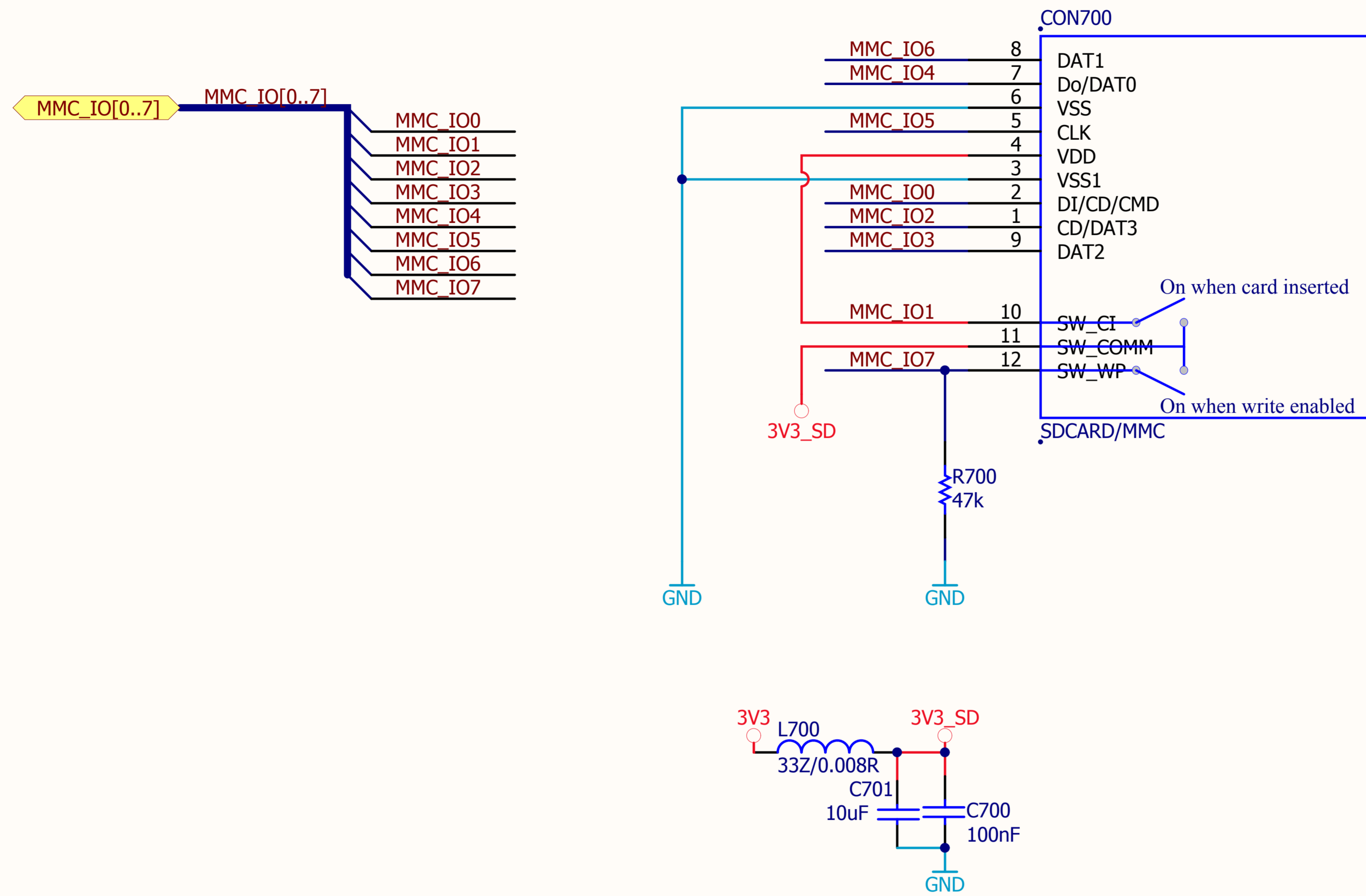
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LL5000 Power Supply					
Size	A3	Number	P005_7	Revision	R002
Date:	25.1.2007		Sheet 7 of	27	
File:	D:\Working\...\PowerSupply_1_1.SchDoc		Drawn By:	Ivan Resetar	



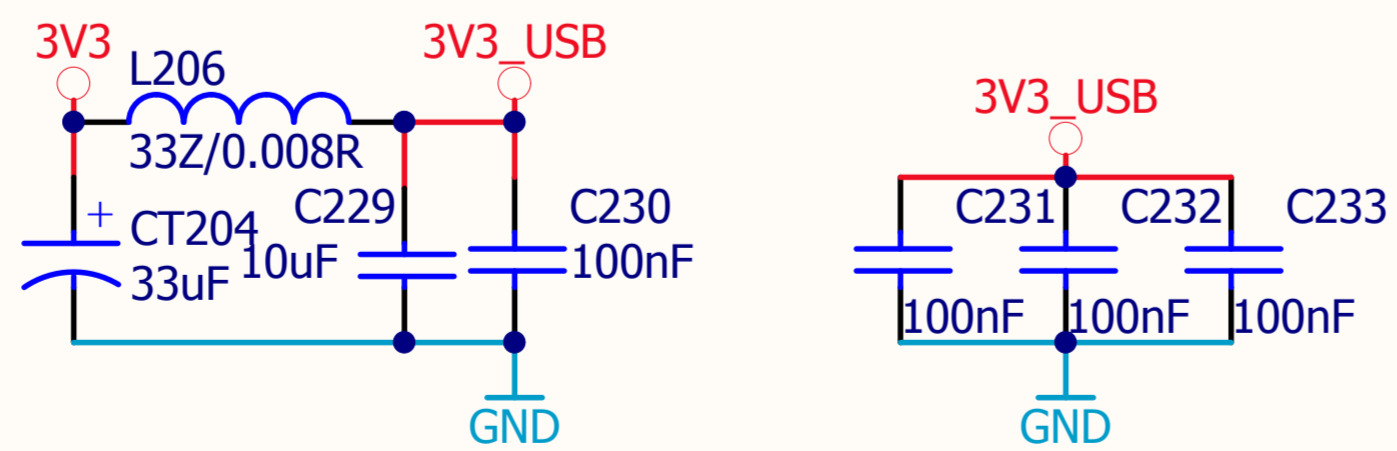
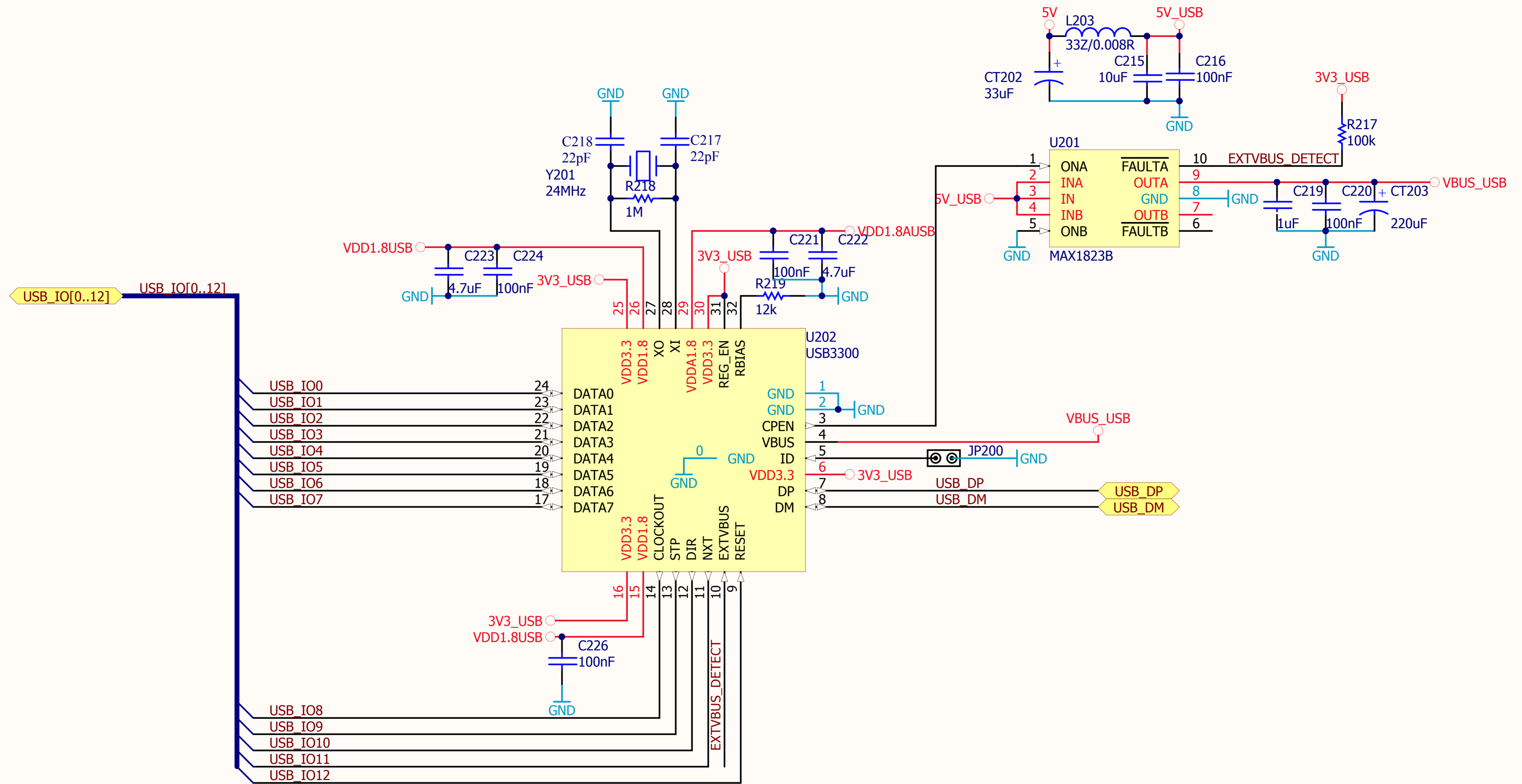
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Novi Sad Institute of Information Technology				
Title LL5000 PS/2 Mouse + Keyboard, RS232				
Size A4	Number P005_17	Revision R002		
Date:	25.1.2007	Sheet 1 of	27	
File:	D:\Working\..\PS2RS232_1_1.SchDoc	Drawn By:	Ivan Resetar	



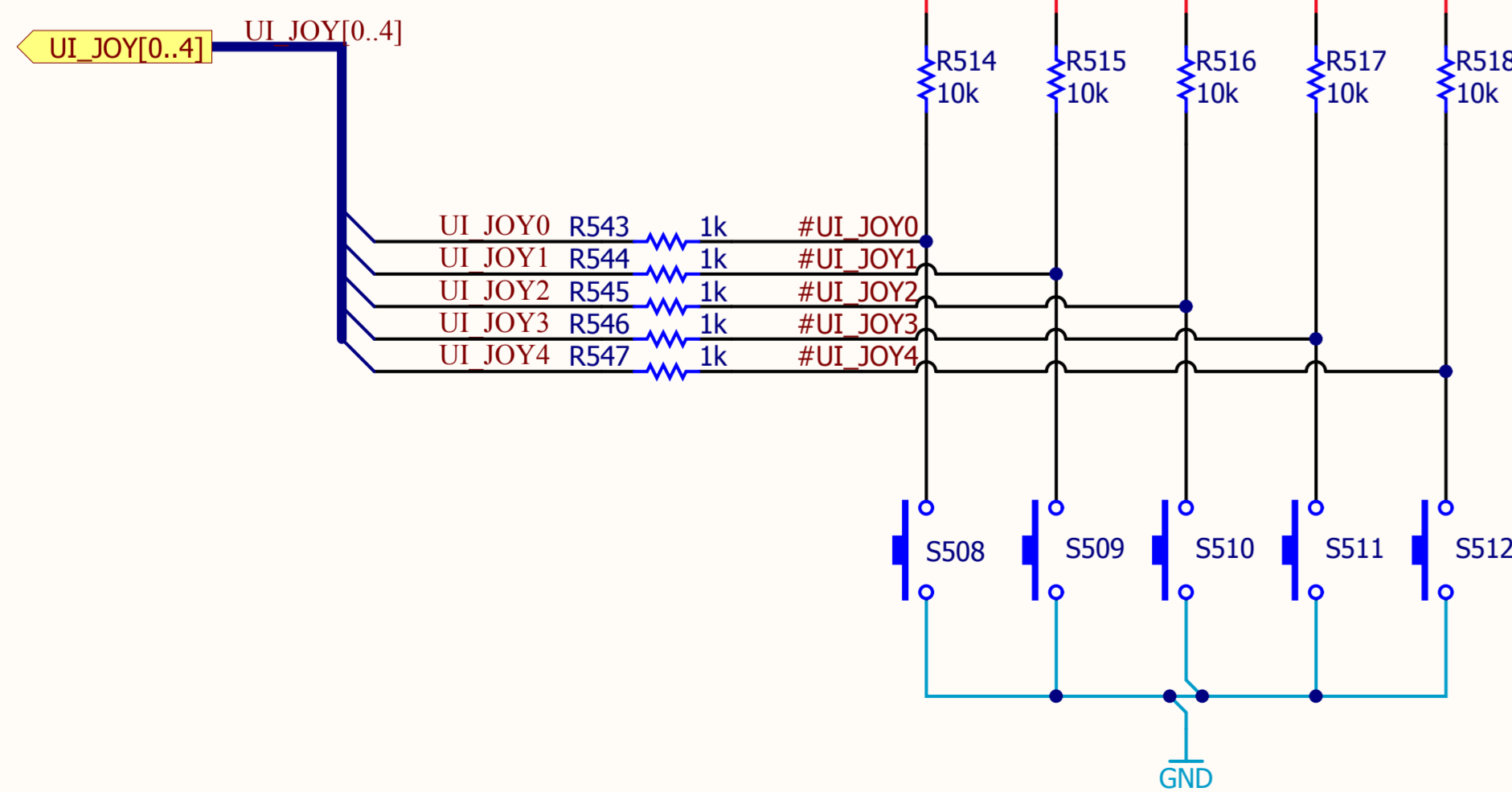
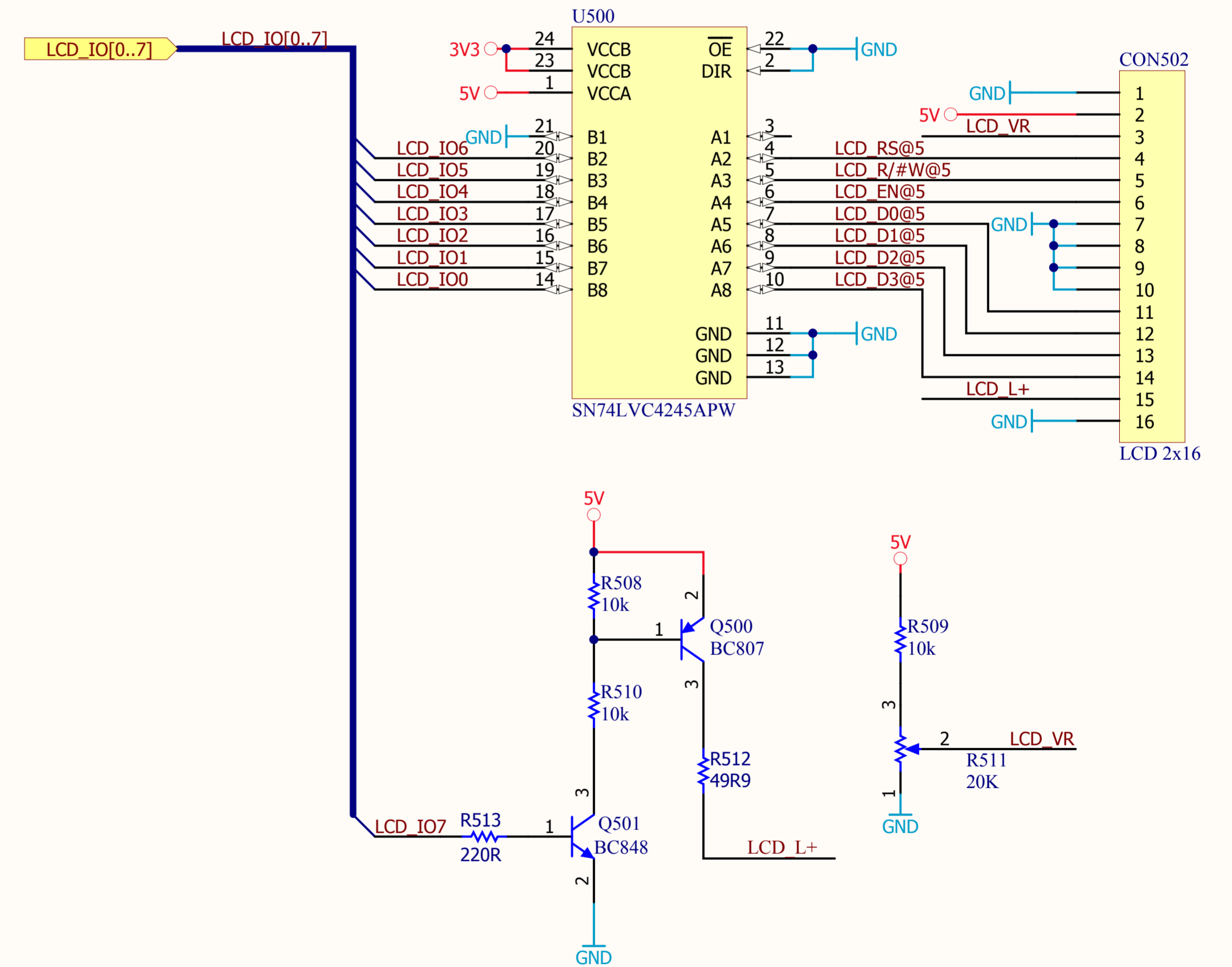
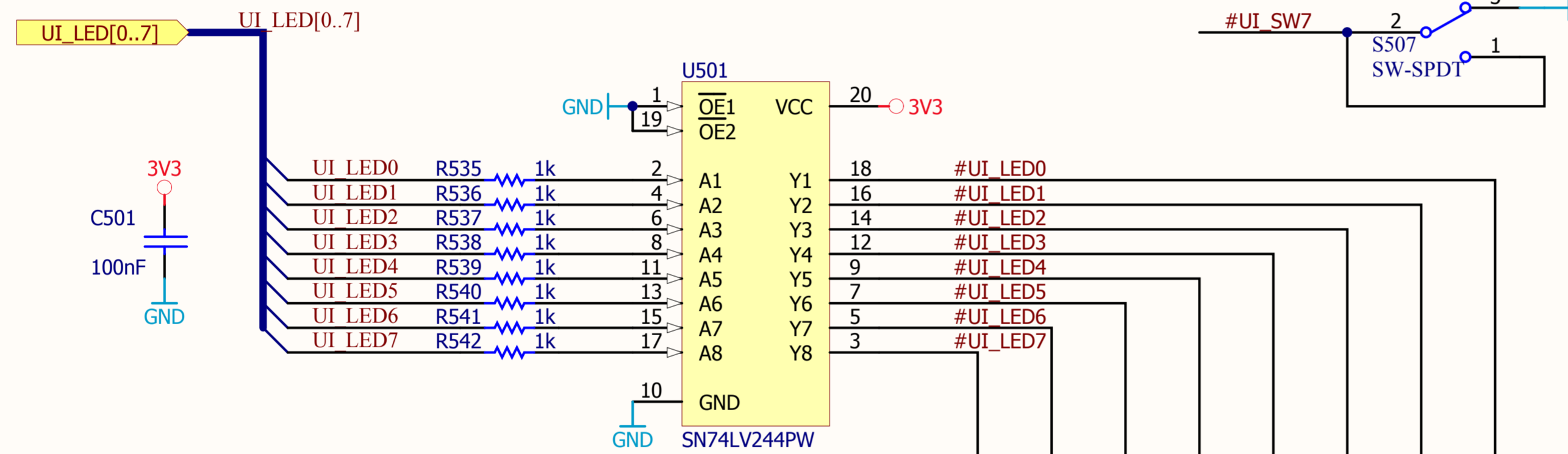
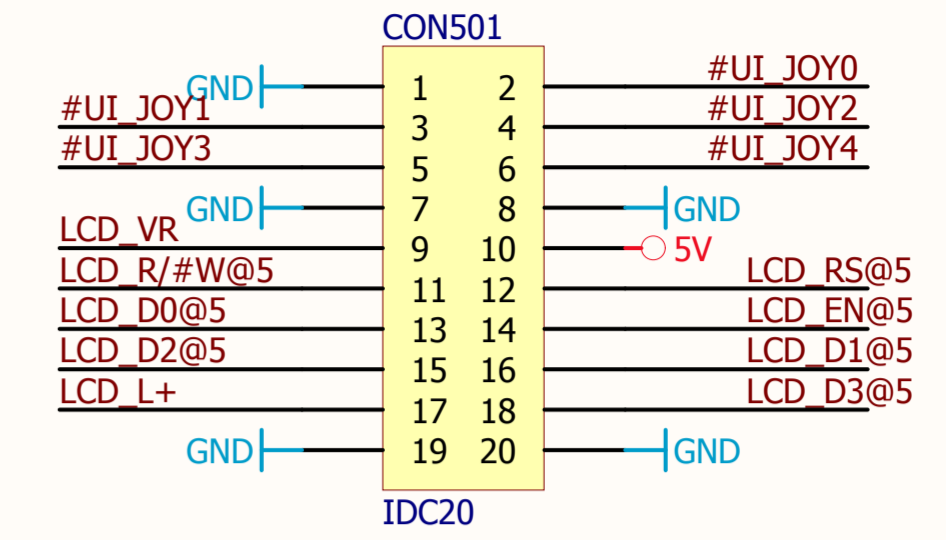
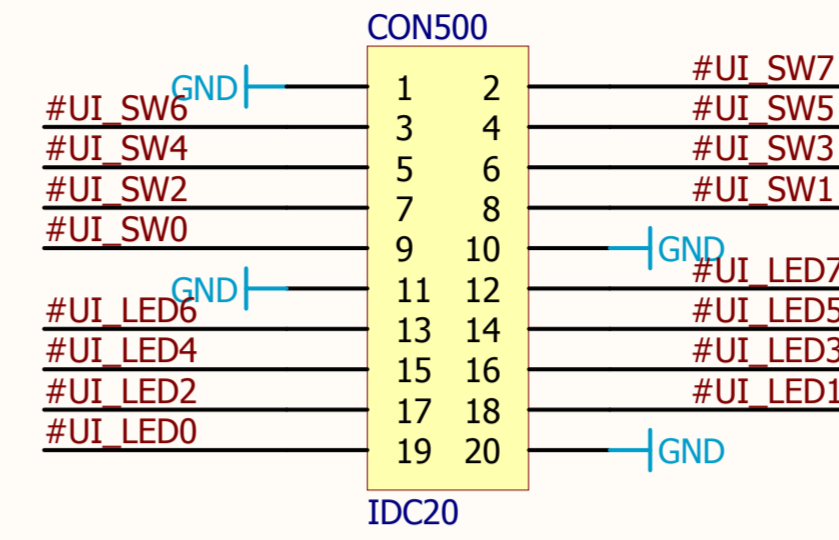
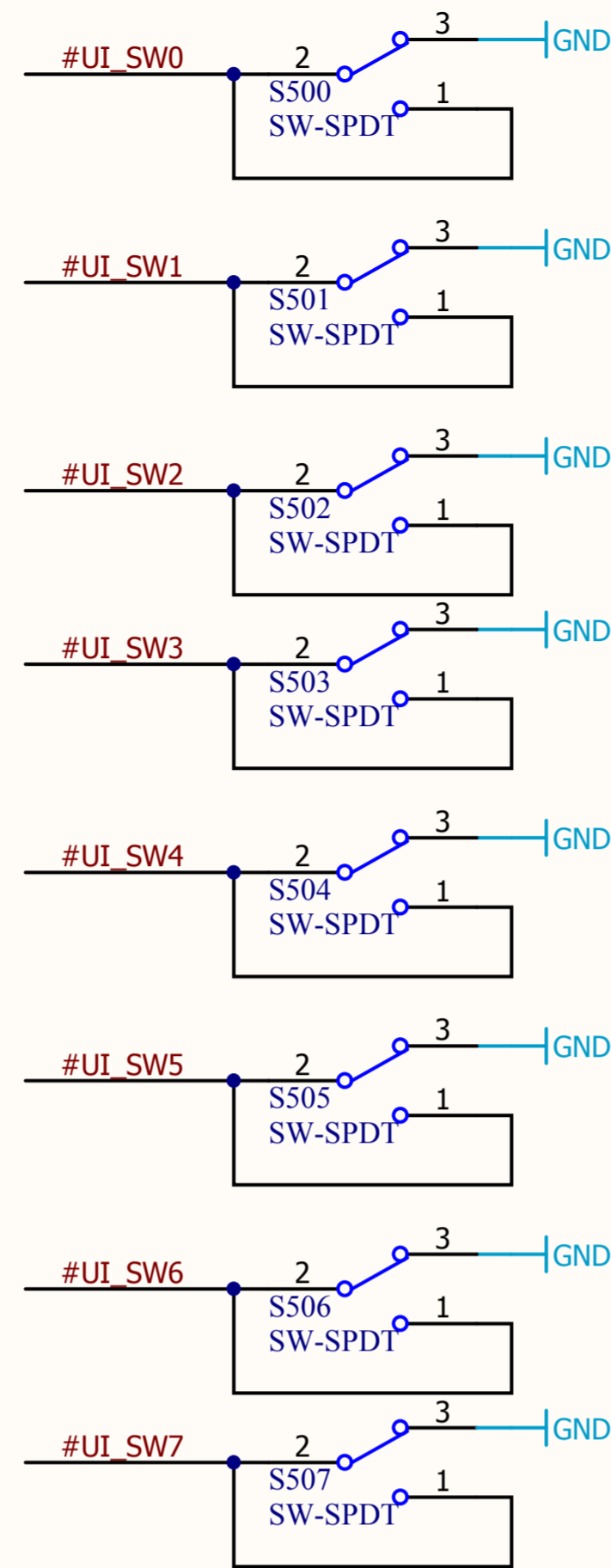
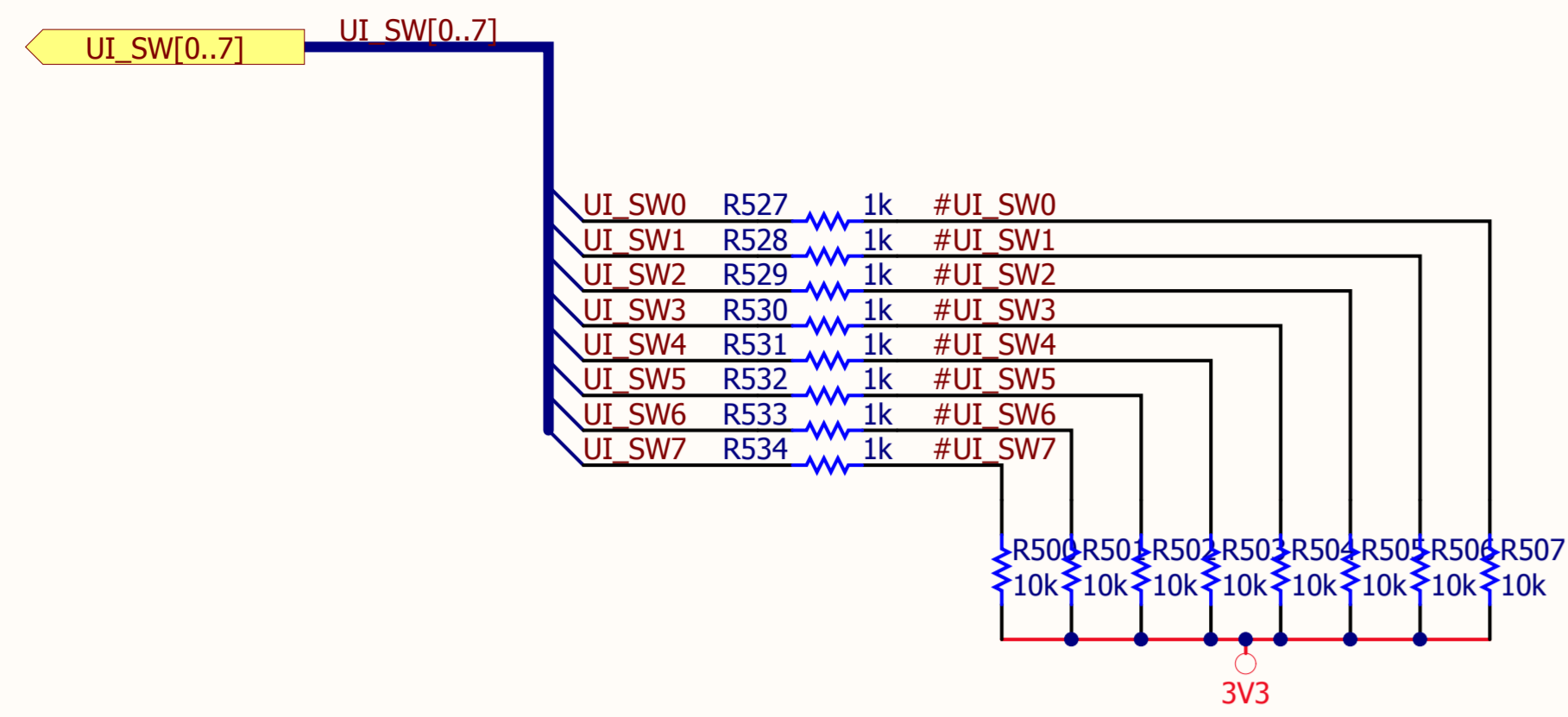
Cannot open file C:\Docum ents and Settings\re		Micronas NIT		Fruskogorska 11a SCG-21000 Novi Sad
Novi Sad Institute of Information Technology				
Title				
LL5000 SDRAM				
Size A4	Number P005_14			Revision R002
Date:	25.1.2007	Sheet 1 of	27	
File:	D:\Working\..\SDRAM_1_1.SchDoc	Drawn By:	Ivan Resetar	



Cannot open file C:\Docum ents and Settings\re		Micronas NIT	Fruskogorska 11a SCG-21000 Novi Sad
Title: LL5000 Secure Digital card Interface			
Size: A4	Number: P005_16	Revision: R002	
Date: 25.1.2007	Sheet 16 of 27	Drawn By: Ivan Resetar	
File: D:\Working\..\sd_header_1_1.SchDoc			



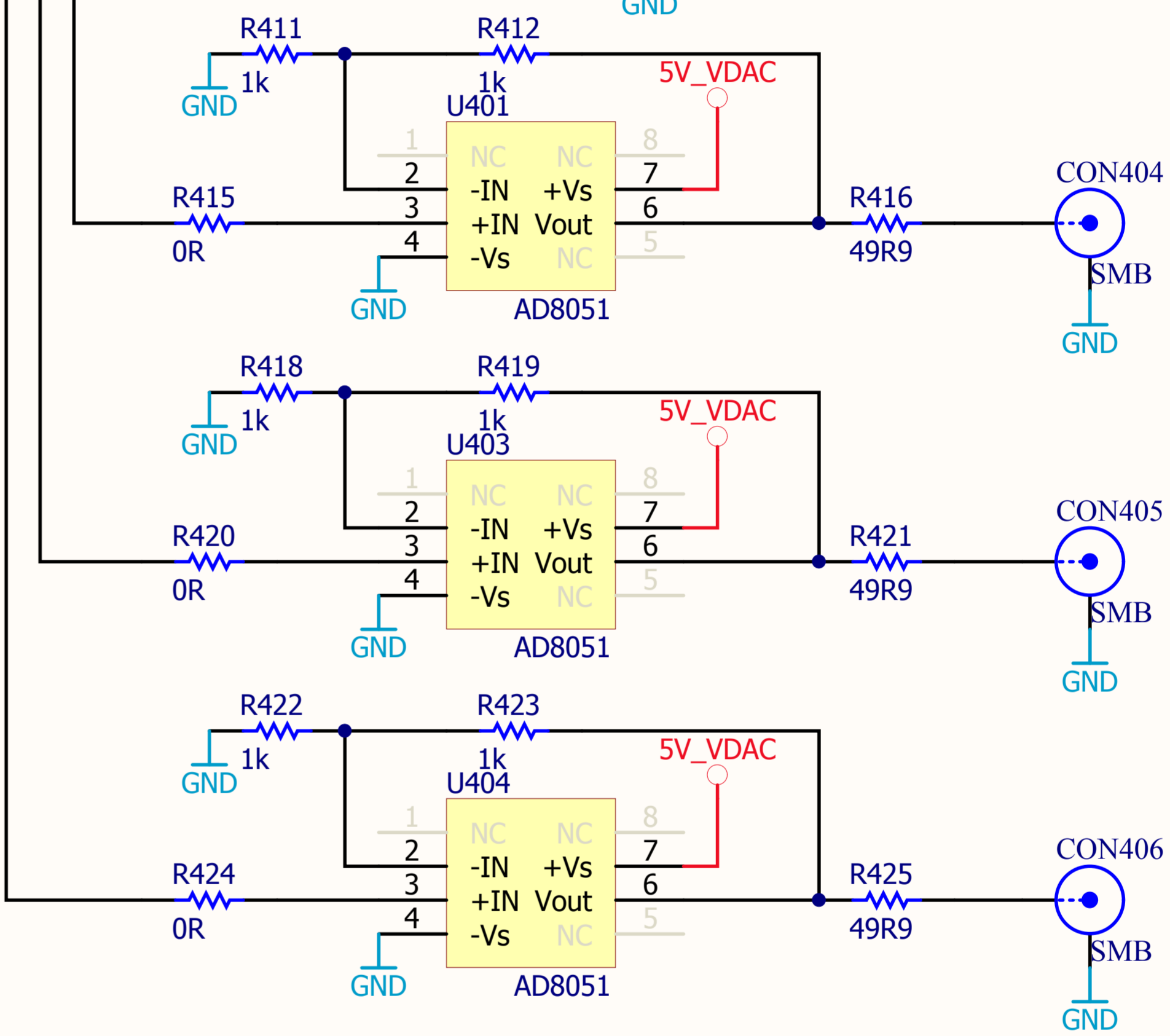
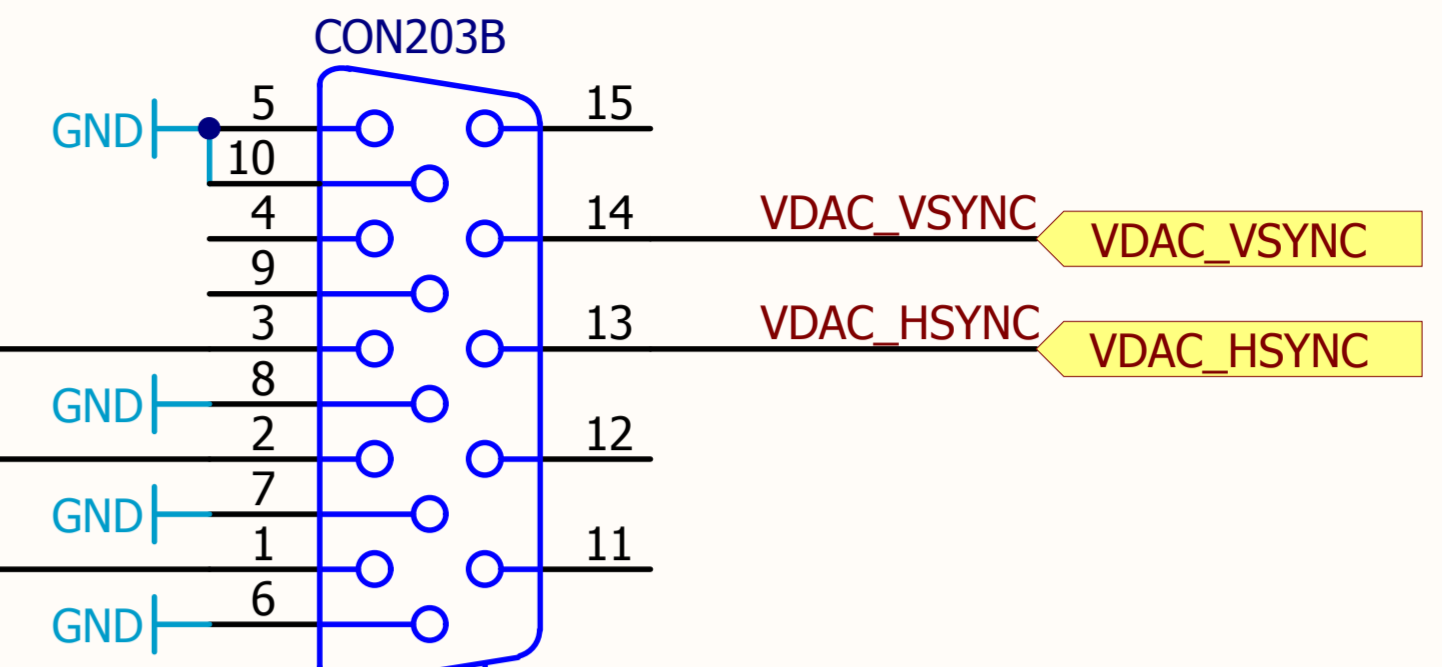
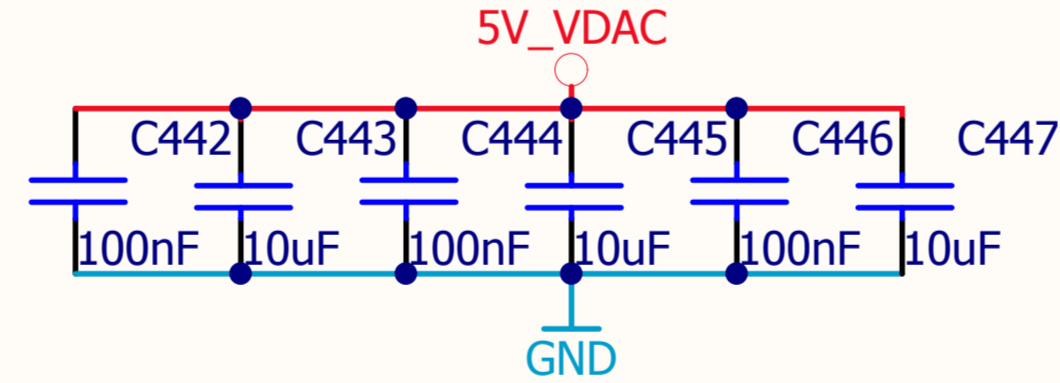
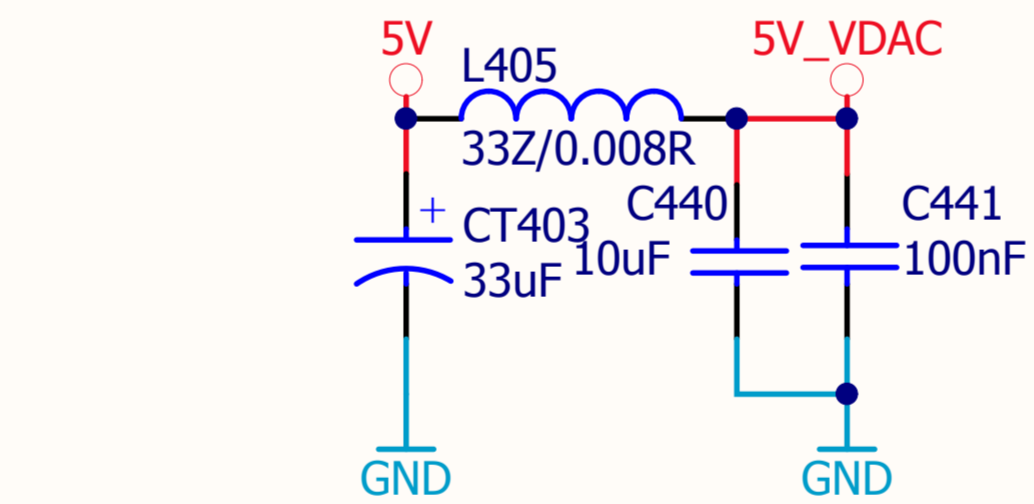
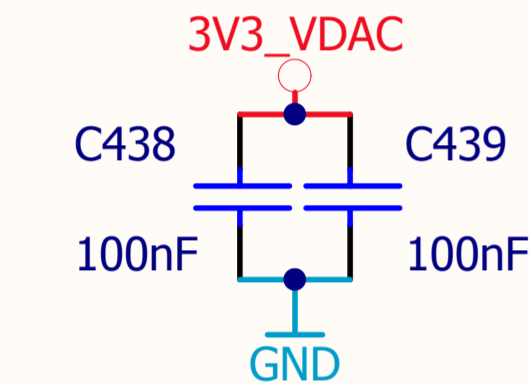
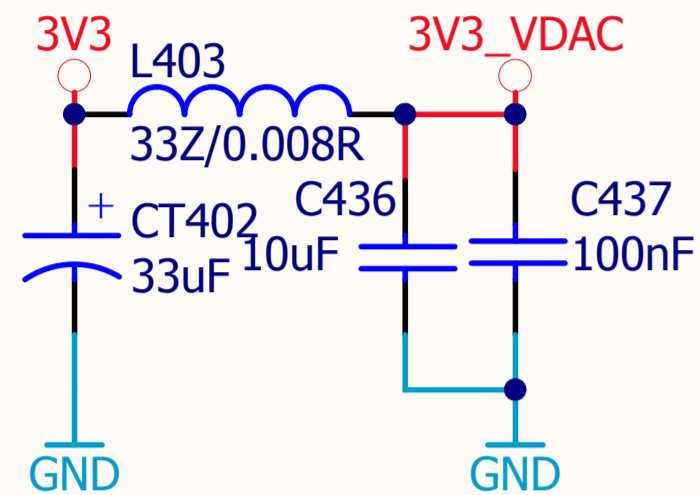
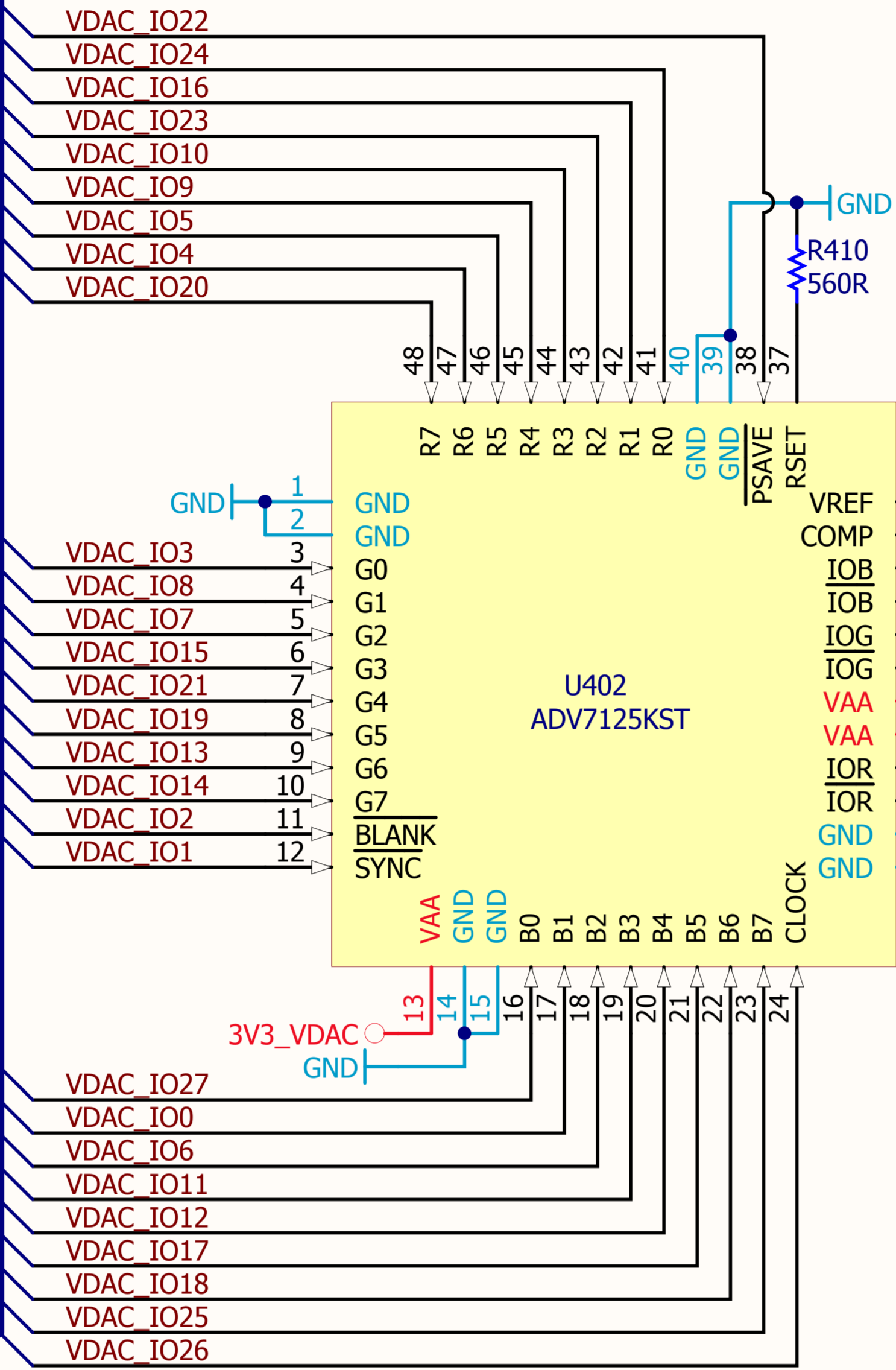
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LL5000 USB 2.0 PHY					
Size A4	Number P005_12			Revision R002	
Date:	25.1.2007		Sheet 1 of	27	
File:	D:\Working\..\USB_1_1.SchDoc		Drawn By:	Ivan Resetar	



Place these pushbuttons in a diamond-shape area

Cannot open file C:\Documents and Settings\ire		MicronasNIT		Fruskogorska 11a SCG-21000 Novi Sad	
LL5000 User Interface					
Title	Number				Revision
A3	P005_22				R002
Date:	25.1.2007	Sheet 22 of	27		
File:	D:\Working\...\UserInterface_1_1.SchDoc		Drawn By:	Ivan Resetar	

VDAC_IO[0..27]



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Title		LL5000 Video DAC		
Size A4	Number P005_18	Revision R002		
Date:	25.1.2007	Sheet 1 of 27		
File:	D:\Working\...\VideoDAC_1_1.SchDoc	Drawn By:	Ivan Resetar	

A

A

B

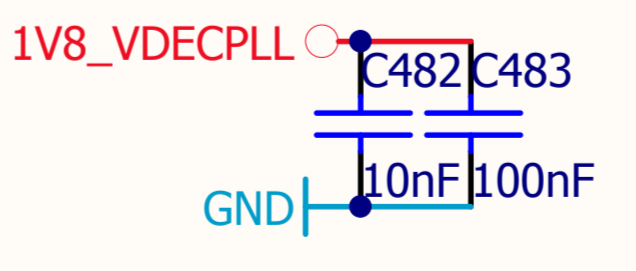
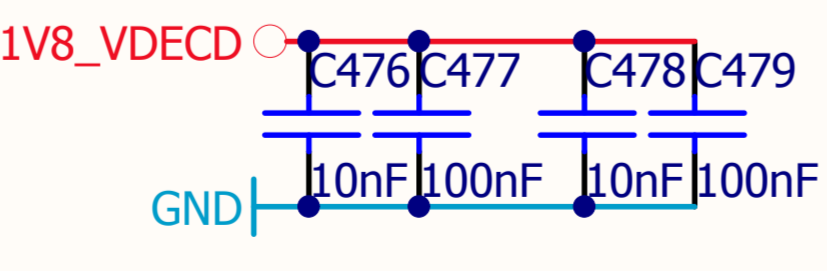
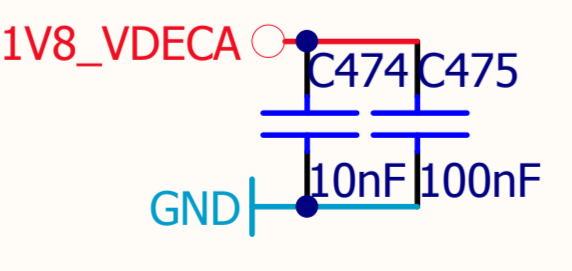
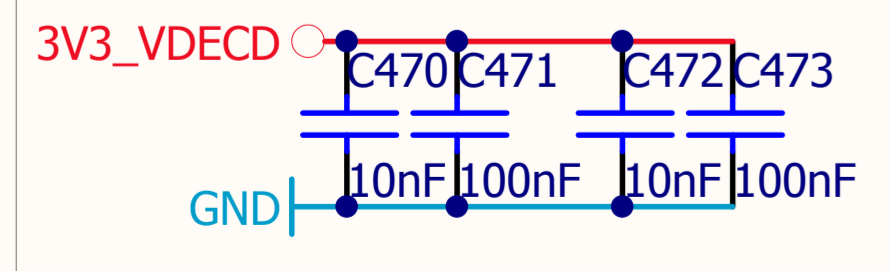
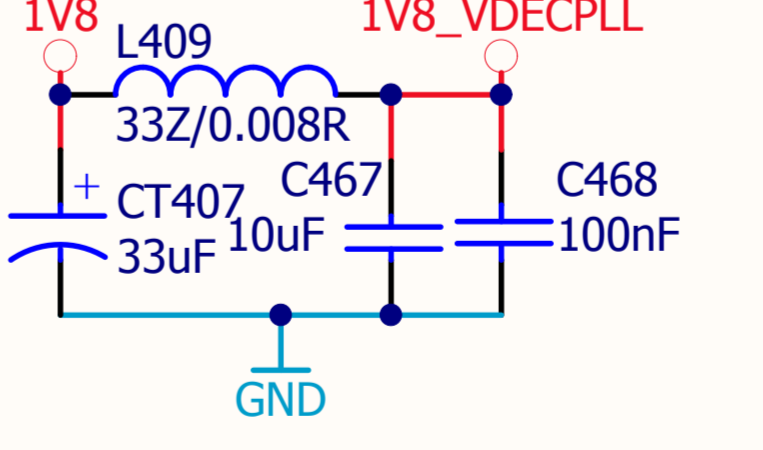
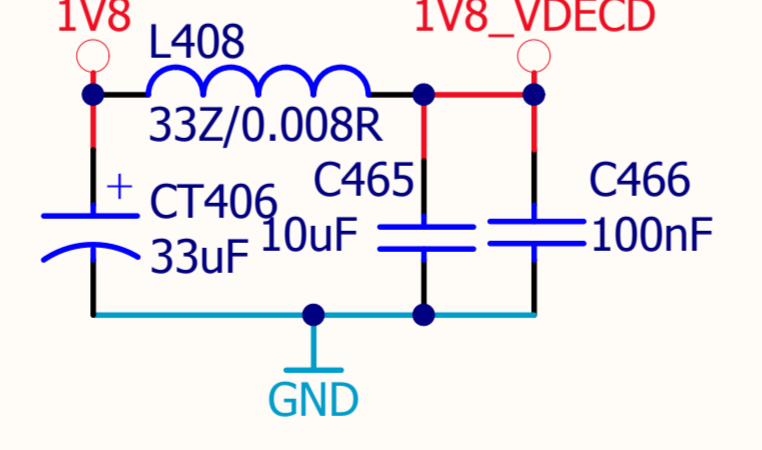
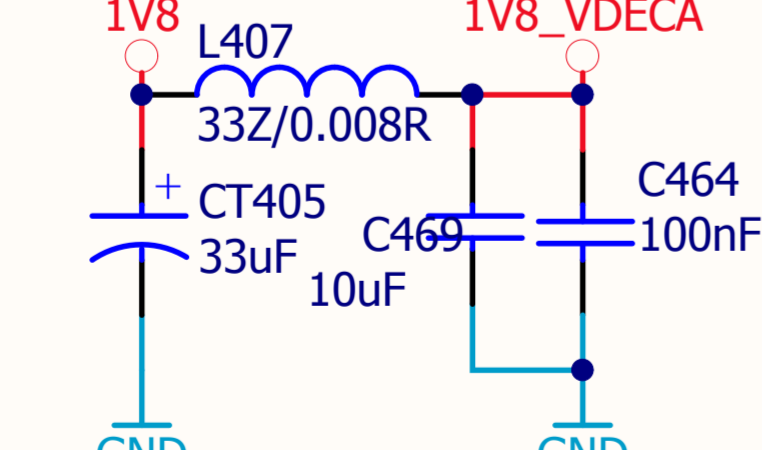
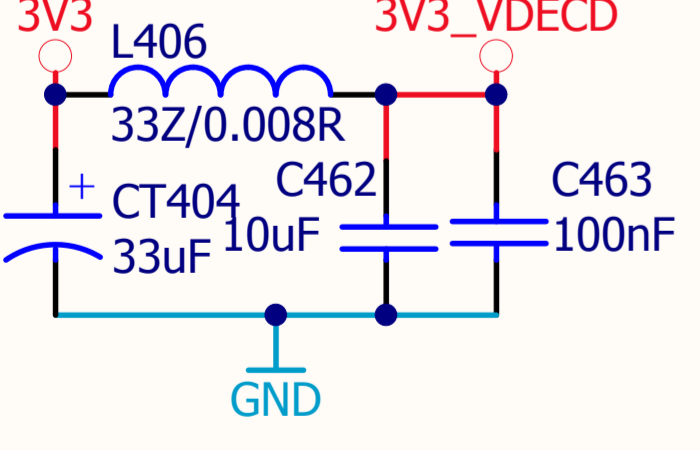
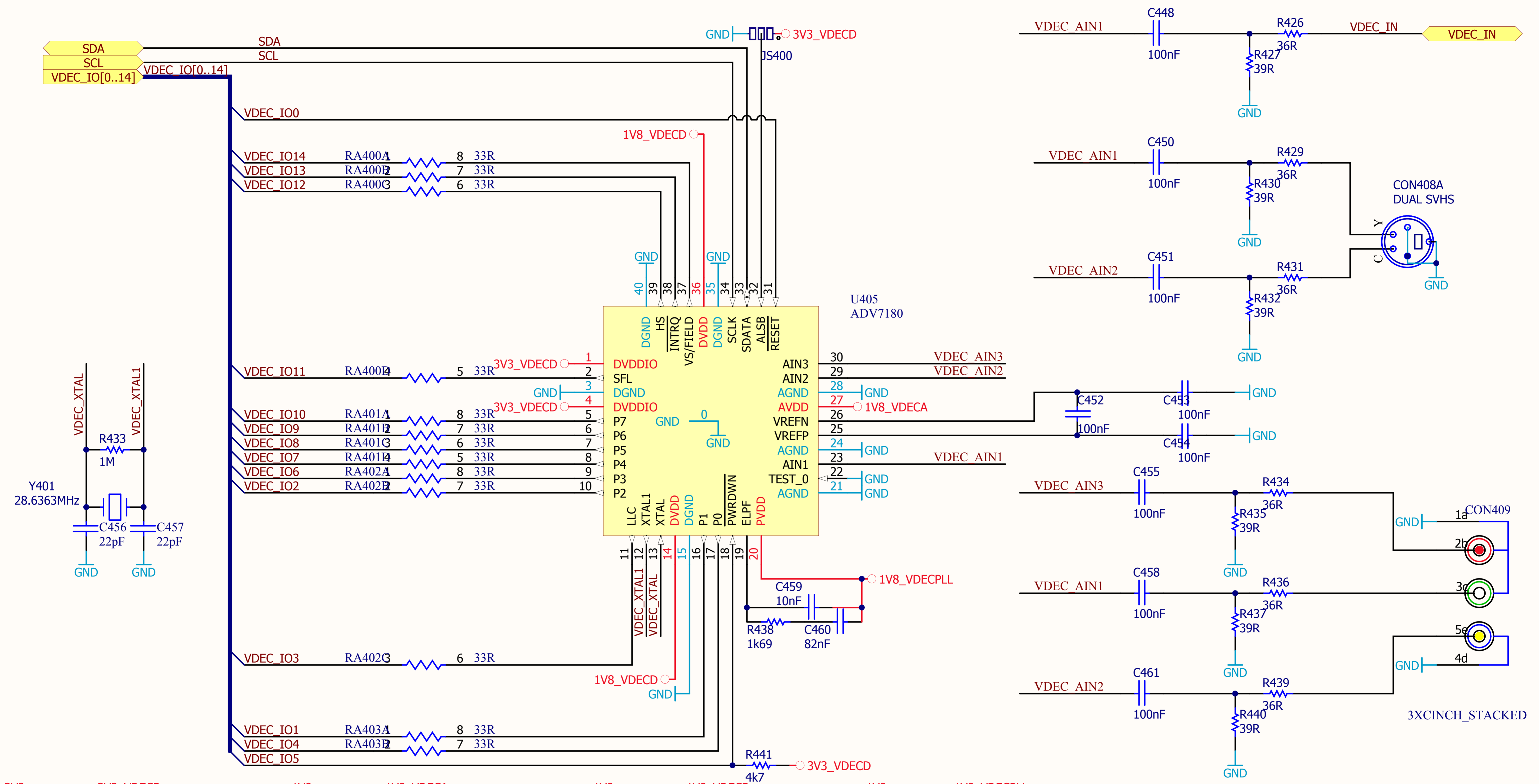
B

C

C

D

D



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Title			LL5000 Video Decoder		
Size	Number	Revision			
A4	P005_19	R002			
Date:	25.1.2007	Sheet 19 of	27		
File:	D:\Working\..\VideoDecoder_1_1.SchDoc		Drawn By:	Ivan Resetar	

