OS and Libraries Document Collection

Summary

The Software Development Kit (SDK) provides a variety of Xilinx® software packages, including drivers, libraries, board support packages, and complete operating systems to help you develop a software platform. This document collection provides information on these. Complete documentation for other operating systems can be found in the their respective reference guides. Device drivers are documented along with the corresponding peripheral documentation. The documentation is listed in the following table; click the name to open the document.

Table 1-1: **OS and Libraries Document Collection Contents**

Document ID	Document Name	Summary
UG645	LibXil Standard C Libraries	Describes the software libraries available for the embedded processors.
UG647	Standalone (v 6.1)	Describes the Standalone platform, a single-threaded, simple operating system (OS) platform that provides the lowest layer of software modules used to access processor-specific functions. Some typical functions offered by the Standalone platform include setting up the interrupts and exceptions systems, configuring caches, and other hardware specific functions. The Hardware Abstraction Layer (HAL) is described in this document.
UG646	Xilkernel (v6.4)	Describes the Xilkernel, a simple embedded processor kernel that can be customized to a large degree for a given system. Xilkernel has the key features of an embedded kernel such as multi-tasking, priority-driven preemptive scheduling, inter-process communication, synchronization facilities, and interrupt handling. Xilkernel is small, modular, user-customizable, and can be used in different system configurations. Applications link statically with the kernel to form a single executable.
UG649	LibXil Memory File System (MFS) (v2.2)	Describes a simple, memory-based file system that can reside in RAM, ROM, or Flash memory.
UG650	lwIP 1.4.1 Library (v1.7)	Describes the SDK port of the third party networking library, Light Weight IP (lwIP) for embedded processors.
UG651	LibXil Flash (v4.2)	Describes the functionality provided in the flash programming library. This library provides access to flash memory devices that conform to the Common Flash Interface (CFI) standard. Intel and AMD CFI devices for some specific part layouts are currently supported.
UG652	LibXil Isf (v5.7)	Describes the In System Flash hardware library, which enables higher-layer software (such as an application) to communicate with the Isf. LibXil Isf supports the Xilinx In-System Flash and external Serial Flash memories from Atmel (AT45XXXD), Spansion(S25FLXX), Winbond W25QXX, and Micron N25QXX.

Table 1-1: **OS and Libraries Document Collection Contents *(Cont'd)***

Document ID	Document Name	Summary
UG1032	LibXil FFS (v3.5)	Xilffs is a generic FAT file system that is primarily added for use with SD/eMMC driver. The file system is open source and a glue layer is implemented to link it to the SD/eMMC driver. A link to the source of file system is provided in the PDF where the file system description can be found.
UG1190	LibXil RSA for Zynq-7000 AP SoC Devices (v1.2)	The LibXil RSA library provides APIs to use RSA encryption and decryption algorithms and SHA algorithms.
UG1191	LibXil SKey for Zynq-7000 UltraScale and Zynq UltraScale+ MPSoC AP SoC Devices (v6.1)	The LibXil SKey library provides a programming mechanism for user-defined eFUSE bits and for programming the KEY into battery-backed RAM (BBRAM) of Zynq® SoC, provides programming mechanisms for eFUSE bits of UltraScale™ devices. The library also provides programming mechanisms for eFUSE bits and BBRAM key of the Zynq® UltraScale+™ MPSoC devices.
UG1189	Library XilSecure for Zynq UltraScale MPSoC (v1.2)	The LibXilSecure library provides APIs to access secure hardware on the Zynq® UltraScale+™ MPSoC devices.
UG1199	Power Management Framework for Zynq UltraScale+ MPSoC Devices	The Zynq UltraScale+ MPSoC power management framework is a set of power management options, based upon an implementation of the extensible energy management interface (EEMI). The power management framework allows software components running across different processing units (PUs) on a chip or device to issue or respond to requests for power management.

About the Libraries

The Standard C support library consists of the `newlib`, `libc`, which contains the standard C functions such as `stdio`, `stdlib`, and `string` routines. The math library is an enhancement over the `newlib` math library, `libm`, and provides the standard math routines.

The LibXil libraries consist of the following:

- LibXil Driver (Xilinx device drivers)
- LibXil MFS (Xilinx memory file system)
- LibXil Flash (a parallel flash programming library)
- LibXil Isf (a serial flash programming library)

There are two operating system options provided in the Xilinx software package: the Standalone Platform and Xilkernel.

The Hardware Abstraction Layer (HAL) provides common functions related to register IO, exception, and cache. These common functions are uniform across MicroBlaze™ and Cortex A9 processors. The Standalone platform document provides some processor specific functions and macros for accessing the processor-specific features.

Most routines in the library are written in C and can be ported to any platform.

User applications must include appropriate headers and link with required libraries for proper compilation and inclusion of required functionality. These libraries and their corresponding `include` files are created in the processor `\lib` and `\include` directories, under the current project, respectively. The **-I** and **-L** options of the compiler being used should be leveraged to add these directories to the search paths.

Library Organization

The organization of the libraries is illustrated in the figure below. As shown, your application can interface with the components in a variety of ways. The libraries are independent of each other, with the exception of some interactions. For example, Xilkernel uses the Standalone platform internally. The LibXil Drivers and the Standalone form the lowermost hardware abstraction layer. The library and OS components rely on standard C library components. The math library, `libm.a` is also available for linking with the user applications.

Note: "LibXil Drivers" are the device drivers included in the software platform to provide an interface to the peripherals in the system. These drivers are provided along with SDK and are configured by Libgen. This document collection contains a section that briefly discusses the concept of device drivers and the way they integrate with the board support package in SDK.

Taking into account some restrictions and implications, which are described in the reference guides for each component, you can mix and match the component libraries.

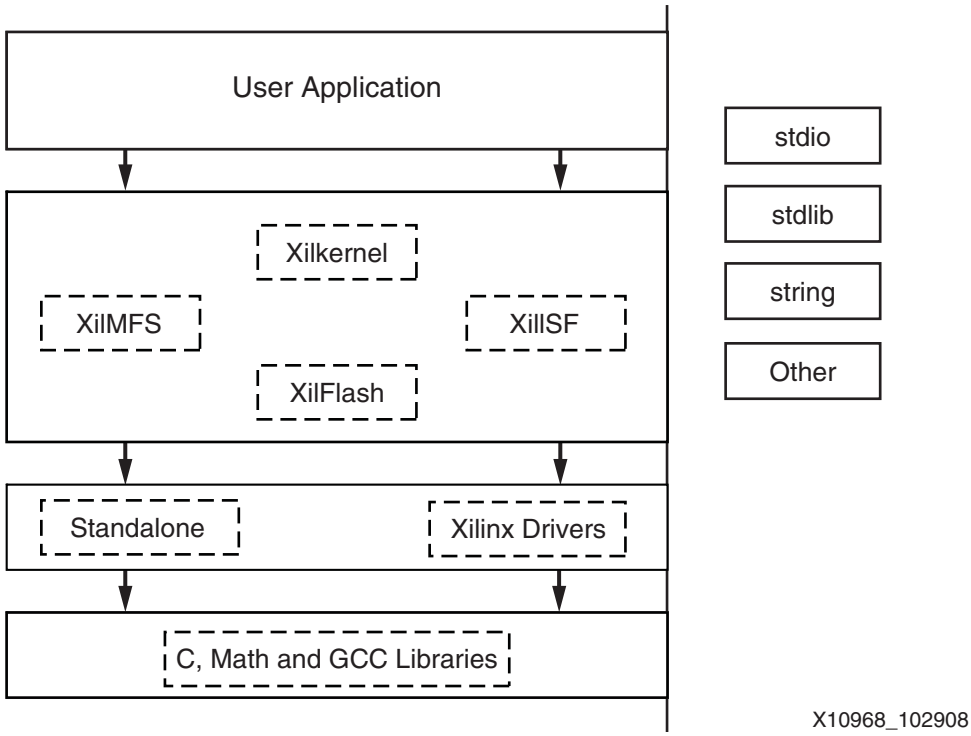

Figure 1: **Library Organization**

Additional Resources

Xilinx Documentation

For more Xilinx documentation, including Vivado® and Zynq® documentation, see the following resources:

- *MicroBlaze Processor Reference Guide* (UG081)
- *Zynq-7000 All Programmable SoC Software Developers Guide* (UG821)
- *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing* (UG973)
- Vivado Design Suite Documentation

Revision History

The following table lists the revision history of the OS and Libraries Document Collection

Date	Version	Revision
11/30/2016	2016.4	• New version of Standalone (v6.1) • New version of lwIP 1.4.1 Library (v1.7) • New version of LibXil FFS (v3.5) • New version of LibXil SKey for Zynq-7000 UltraScale and Zynq UltraScale+ MPSoC AP SoC Devices (v6.1) • New version of LibXil MFS(v2.2)
10/05/2016	2016.3	• New version of Standalone (v6.0) • New version of lwIP 1.4.1 Library (v1.6) • New version of LibXil FFS (v3.4) • New version of LibXil Isf (v5.7) • New version of Library XilSecure for Zynq UltraScale MPSoC (v1.2) • New version of LibXil SKey for Zynq-7000 UltraScale and Zynq UltraScale+ MPSoC AP SoC Devices (v6.0)
06/08/2016	2016.2	• New version of Standalone (v.5.5) • New version of lwIP 1.4.1 Library (v1.5) • New version of LibXil FFS (v3.3) • New version of LibXil Isf (v5.6)
04/06/2016	2016.1	• New version of Standalone (v5.4) • New version of LibXil FFS (v3.2) • New version of LibXil Flash (v4.2) • New version of LibXil Isf (v5.5) • New version of Library XilSecure for Zynq UltraScale MPSoC (v1.1) • New version of LibXil SKey for Zynq-7000 UltraScale and Zynq UltraScale+ MPSoC AP SoC Devices (v5.0) • New version of LibXil RSA for Zynq-7000 AP SoC Devices (v1.2) • New version of IwIP 1.4.1 Library (v1.4) • New version of Xilkernel (v6.3)

UG645 March 20, 2013

LibXil Standard C Libraries

Overview

The Xilinx® Software Development Kit (SDK) libraries and device drivers provide standard C library functions, as well as functions to access peripherals. The SDK libraries are automatically configured based on the Microprocessor Software Specification (MSS) file. These libraries and include files are saved in the current project `lib` and `include` directories, respectively. The **-I** and **-L** options of `mb-gcc` are used to add these directories to its library search paths.

Additional Resources

- *MicroBlaze Processor Reference Guide* (UG081)
- *Embedded System Tools Reference Manual* (UG1043)

Standard C Library (libc.a)

The standard C library, `libc.a`, contains the standard C functions compiled for the MicroBlaze™ processor or the Cortex A9 processor. You can find the header files corresponding to these C standard functions in <*XILINX_SDK*>/gnu/<*processor*>/<*platform*>/<*processor-lib*>/include, where:

- <*XILINX_SDK*> is the <*Installation directory*>
- <*processor*> is `arm` or `microblaze`
- <*platform*> is `sol`, `nt`, or `lin`
- <*processor-lib*> is `arm-xilinx-eabi` or `microblaze-xilinx-elf`

The `lib.c` directories and functions are:

_ansi.h	fastmath.h	machine/	reent.h	stdlib.h	utime.h
_syslist.h	fcntl.h	malloc.h	regdef.h	string.h	utmp.h
ar.h	float.h	math.h	setjmp.h	sys/	
assert.h	grp.h	paths.h	signal.h	termios.h	
ctype.h	ieeefp.h	process.h	stdarg.h	time.h	
dirent.h	limits.h	pthread.h	stddef.h	unctrl.h	
errno.h	locale.h	pwd.h	stdio.h	unistd.h	

Programs accessing standard C library functions must be compiled as follows:

For MicroBlaze processors:

```
mb-gcc <C files>
```

For Cortex A9 processors:

```
arm-xilinx-eabi-gcc <C files>
```

The `libc` library is included automatically.

For programs that access `libm` math functions, specify the **`-lm`** option.

Refer to the "MicroBlaze Application Binary Interface (ABI)" section in the *MicroBlaze Processor Reference Guide (UG081)* for information on the C Runtime Library. "Additional Resources," page 1 contains a link to the document.

Xilinx C Library (libxil.a)

The Xilinx® C library, `libxil.a`, contains the following object files for the MicroBlaze™ processor embedded processor:

```
_exception_handler.o
_interrupt_handler.o
_program_clean.o
_program_init.o
```

Default exception and interrupt handlers are provided. The `libxil.a` library is included automatically.

Programs accessing Xilinx C library functions must be compiled as follows:

```
mb-gcc <C files>
```

Input/Output Functions

The SDK libraries contains standard C functions for I/O, such as `printf` and `scanf`. These functions are large and might not be suitable for embedded processors.

The prototypes for these functions are in `stdio.h`.

Note: The C standard I/O routines such as printf, scanf, vfprintf are, by default, line buffered. To change the buffering scheme to no buffering, you must call setvbuf appropriately. For example:

```
setvbuf (stdout, NULL, _IONBF, 0);
```

These Input/Output routines require that a newline is terminated with both a CR and LF. Ensure that your terminal CR/LF behavior corresponds to this requirement.

Refer to the "Microprocessor Software Specification (MSS)" chapter in the *Embedded System Tools Reference Manual (UG1043)* for information on setting the standard input and standard output devices for a system. "Additional Resources," page 1 contains a link to the document.

In addition to the standard C functions, the SDK processors library provides the following smaller I/O functions:

`void` **`print`** `(char *)`

This function prints a string to the peripheral designated as standard output in the Microprocessor Software Specification (MSS) file. This function outputs the passed string as is and there is no interpretation of the string passed. For example, a `"\n"` passed is interpreted as a new line character and not as a carriage return and a new line as is the case with ANSI C printf function.

`void` **`putnum`** `(int)`

This function converts an integer to a hexadecimal string and prints it to the peripheral designated as standard output in the MSS file.

`void` **`xil_printf`** `(const *char ctrl1,...)`

`xil_printf` is a light-weight implementation of `printf`. It is much smaller in size (only 1 kB). It does not have support for floating point numbers. `xil_printf` also does not support printing of long (such as 64-bit) numbers.

Note: About Format String Support:

The format string is composed of zero or more directives: ordinary characters (not %), which are copied unchanged to the output stream; and conversion specifications, each of which results in fetching zero or more subsequent arguments. Each conversion specification is introduced by the character %, and ends with a conversion specifier.

In between there can be (in order) zero or more flags, an optional minimum field width and an optional precision. Supported flag characters are:

The character % is followed by zero or more of the following flags:

- `0` The value should be zero padded. For `d`, x conversions, the converted value is padded on the left with zeros rather than blanks.
  If the 0 and - flags both appear, the 0 flag is ignored.
- `-` The converted value is to be left adjusted on the field boundary.
  (The default is right justification.) Except for n conversions, the converted value is padded on the right with blanks, rather than on the left with blanks or zeros. A - overrides a 0 if both are given.

Note: About Supported Field Widths:

Field widths are represented with an optional decimal digit string (with a nonzero in the first digit) specifying a minimum field width. If the converted value has fewer characters than the field width, it is padded with spaces on the left (or right, if the left-adjustment flag has been given). The supported conversion specifiers are:

- `d` The `int` argument is converted to signed decimal notation.
- `l` The `int` argument is converted to a signed long notation.
- `x` The `unsigned int` argument is converted to unsigned hexadecimal notation. The letters `abcdef` are used for x conversions.
- c The int argument is converted to an unsigned char, and the resulting character is written.
- s The `const char*` argument is expected to be a pointer to an array of character type (pointer to a string).
  Characters from the array are written up to (but not including) a terminating `NULL` character; if a precision is specified, no more than the number specified are written. If a precision s given, no null character need be present; if the precision is not specified, or is greater than the size of the array, the array must contain a terminating `NULL` character.

Memory Management Functions

The MicroBlaze processor and Cortex A9 processor C libraries support the standard memory management functions such as `malloc( )`, `calloc( )`, and `free( )`. Dynamic memory allocation provides memory from the program heap. The heap pointer starts at low memory and grows toward high memory. The size of the heap cannot be increased at runtime. Therefore an appropriate value must be provided for the heap size at compile time. The `malloc( )` function requires the heap to be at least 128 bytes in size to be able to allocate memory dynamically (even if the dynamic requirement is less than 128 bytes). The return value of `malloc` must always be checked to ensure that it could actually allocate the memory requested .

Arithmetic Operations

Software implementations of integer and floating point arithmetic is available as library routines in `libgcc.a` for both processors. The compiler for both the processors inserts calls to these routines in the code produced, in case the hardware does not support the arithmetic primitive with an instruction.

MicroBlaze Processor

Integer Arithmetic

By default, integer multiplication is done in software using the library function `__mulsi3`. Integer multiplication is done in hardware if the mb-gcc option, `-mno-xl-soft-mul`, is specified.

Integer divide and mod operations are done in software using the library functions `__divsi3` and `__modsi3`. The MicroBlaze processor can also be customized to use a hard divider, in which case the div instruction is used in place of the `__divsi3` library routine.

Double precision multiplication, division and mod functions are carried out by the library functions `__muldi3`, `__divdi3`, and `__moddi3`, respectively.

The unsigned version of these operations correspond to the signed versions described above, but are prefixed with an `__u` instead of __.

Floating Point Arithmetic

All floating point addition, subtraction, multiplication, division, and conversions are implemented using software functions in the C library.

Thread Safety

The standard C library provided with SDK is not built for a multi-threaded environment. STDIO functions like `printf()`, `scanf()` and memory management functions like `malloc()` and `free()` are common examples of functions that are not thread-safe. When using the C library in a multi-threaded environment, proper mutual exclusion techniques must be used to protect thread unsafe functions.

UG647 November 30, 2016

Standalone (v 6.1)

Summary

Standalone is the lowest layer of software modules used to access processor specific functions. Standalone is used when an application accesses board/processor features directly and is below the operating system layer.

This document contains the following sections:

- MicroBlaze Processor API
- Cortex A9 Processor API
- Cortex R5 Processor API
- Cortex A53 Processor API
- Xilinx Hardware Abstraction Layer
- Program Profiling
- Configuring the Standalone OS
- MicroBlaze MMU Example

MicroBlaze Processor API

The following list is a summary of the MicroBlaze™ processor API sections. You can click on a link to go directly to the function section.

- MicroBlaze Processor Interrupt Handling
- MicroBlaze Processor Exception Handling
- MicroBlaze Processor Instruction Cache Handling
- MicroBlaze Processor Data Cache Handling
- MicroBlaze Processor Fast Simplex Link (FSL) Interface Macros
- MicroBlaze Processor FSL Macro Flags
- MicroBlaze Processor Pseudo-asm Macro Summary
- MicroBlaze Processor Version Register (PVR) Access Routine and Macros
- MicroBlaze Processor File Handling
- MicroBlaze Processor Errno

MicroBlaze Processor Interrupt Handling

The interrupt handling functions help manage interrupt handling on MicroBlaze processor devices. To use these functions, include the header file `mb_interface.h` in your source code.

MicroBlaze Processor Interrupt Handling Function Descriptions

---

`void` **`microblaze_enable_interrupts`**`(void)`

Enable interrupts on the MicroBlaze processor. When the MicroBlaze processor starts up, interrupts are disabled. Interrupts must be explicitly turned on using this function.

`void` **`microblaze_disable_interrupts`**`(void)`

Disable interrupts on the MicroBlaze processor. This function can be called when entering a critical section of code where a context switch is undesirable.

`void` **`microblaze_register_handler`**`(XInterruptHandler` *`Handler`*`, void` *`*DataPtr`*`)`

Register the interrupt handler for the MicroBlaze processor. This handler is invoked in turn, by the first level interrupt handler that is present in Standalone.

The first level interrupt handler saves and restores registers, as necessary for interrupt handling, so that the function you register with this handler can be dedicated to the other aspects of interrupt handling, without the overhead of saving and restoring registers.

MicroBlaze Processor Exception Handling

This section describes the exception handling functionality available on the MicroBlaze processor. This feature and the corresponding interfaces are not available on versions of the MicroBlaze processor older than v3.00.a.

Note: These functions work correctly only when the parameters that determine hardware exception handling are configured appropriately in the MicroBlaze Microprocessor Hardware Specification (MHS) hardware block. For example, you can register a handler for divide by zero exceptions only if hardware divide by zero exceptions are enabled on the MicroBlaze processor. Refer to the *MicroBlaze Processor Reference Guide (UG081)* for information on how to configure these cache parameters. A link to that document can be found in "MicroBlaze Processor API," page 1.

MicroBlaze Processor Exception Handler Function Descriptions

The following functions help manage exceptions on the MicroBlaze processor. You must include the `mb_interface.h` header file in your source code to use these functions.

`void` **`microblaze_disable_exceptions`**`(void)`

Disable hardware exceptions from the MicroBlaze processor. This routine clears the appropriate "exceptions enable" bit in the model-specific register (MSR) of the processor.

`void` **`microblaze_enable_exceptions`**`(void)`

Enable hardware exceptions from the MicroBlaze processor. This routine sets the appropriate "exceptions enable" bit in the MSR of the processor.

`void` **`microblaze_register_exception_handler`**`(u8` *`ExceptionId`*`, XExceptionHandler` *`Handler`*`, void` *`*DataPtr`*`)`

Register a handler for the specified exception type. *`Handler`* is the function that handles the specified exception.
`DataPtr` is a callback data value that is passed to the exception handler at run-time. By default the exception ID of the corresponding exception is passed to the handler.

Table 1 describes the valid exception IDs, which are defined in the `microblaze_exceptions_i.h` file.

Table 1: **Valid Exception IDs**

Exception ID	Value	Description
`XEXC_ID_FSL`	0	FSL bus exceptions.
`XEXC_ID_UNALIGNED_ACCESS`	1	Unaligned access exceptions.
`XEXC_ID_ILLEGAL_OPCODE`	2	Exception due to an attempt to execute an illegal opcode.
`XEXC_ID_M_AXI_I_EXCEPTION(1)`	3	Exception due to a timeout from the Instruction side system bus.
`XEXC_ID_M_AXI_D_EXCEPTION(1)`	4	Exception due to a timeout on the Data side system bus.
`XEXC_ID_DIV_BY_ZERO`	5	Divide by zero exceptions from the hardware divide.
`XEXC_ID_FPU`	6	Exceptions from the floating point unit on the MicroBlaze processor. ***Note:*** This exception is valid only on v4.0 and later versions of the MicroBlaze processor.
`XEXC_ID_MMU`	7	Exceptions from the MicroBlaze processor MMU. All possible MMU exceptions are vectored to the same handler. ***Note:*** This exception is valid only on v7.00.a and later versions of the MicroBlaze processor.

By default, Standalone provides empty, no-op handlers for all the exceptions *except* unaligned exceptions. A default, fast, unaligned access exception handler is provided by Standalone.

An unaligned exception can be handled by making the corresponding aligned access to the appropriate bytes in memory. Unaligned access is transparently handled by the default handler. However, software that makes a significant amount of unaligned accesses will see the performance effects of this at run-time. This is because the software exception handler takes much longer to satisfy the unaligned access request as compared to an aligned access.

In some cases you might want to use the provision for unaligned exceptions to just trap the exception, and to be aware of what software is causing the exception. In this case, you should set breakpoints at the unaligned exception handler, to trap the dynamic occurrence of such an exception or register your own custom handler for unaligned exceptions.

Note: The lowest layer of exception handling, always provided by Standalone, stores volatile and temporary registers on the stack; consequently, your custom handlers for exceptions must take into consideration that the first level exception handler will have saved some state on the stack, before invoking your handler.

Nested exceptions are allowed by the MicroBlaze processor. The exception handler, in its prologue, re-enables exceptions. Thus, exceptions within exception handlers are allowed and handled. When the `predecode_fpu_exceptions` parameter is set to `true`, it causes the low-level exception handler to:

- Decode the faulting floating point instruction
- Determine the operand registers
- Store their values into two global variables

You can register a handler for floating point exceptions and retrieve the values of the operands from the global variables. You can use the `microblaze_getfpex_operand_a()` and `microblaze_getfpex_operand_b()` macros.

Note: These macros return the operand values of the last floating point (FP) exception. If there are nested exceptions, you cannot retrieve the values of outer exceptions. An FP instruction might have one of the source registers being the same as the destination operand. In this case, the faulting instruction overwrites the input operand value and it is again irrecoverable.

MicroBlaze Processor Instruction Cache Handling

The following functions help manage instruction caches on the MicroBlaze processor. You must include the `xil_cache.h` header file in your source code to use these functions.

Note: These functions work correctly only when the parameters that determine the caching system are configured appropriately in the MicroBlaze Microprocessor Hardware Specification (MHS) hardware block. Refer to the *MicroBlaze Reference Guide (UG081)* for information on how to configure these cache parameters. "MicroBlaze Processor API," page 1 contains a link to this document.

MicroBlaze Processor Instruction Cache Handling Function Descriptions

---

`void` **`Xil_ICacheEnable`**`(void)`

Enable the instruction cache on the MicroBlaze processor. When the MicroBlaze processor starts up, the instruction cache is disabled. The instruction cache must be explicitly turned on using this function.

`void` **`Xil_ICacheDisable`**`(void)`

Disable the instruction cache on the MicroBlaze processor.

`void` **`Xil_ICacheInvalidate`**`()`

Invalidate the instruction icache.

Note: For MicroBlaze processors prior to version v7.20.a, the cache and interrupts are disabled before invalidation starts and restored to their previous state after invalidation.

`void` **`Xil_ICacheInvalidateRange`**`(unsigned int` *`cache_addr`*`, unsigned int` *`cache_size`*`)`

Invalidate the specified range in the instruction icache. This function can be used for invalidating all or part of the instruction icache.

The parameter `cache_addr` indicates the beginning of the cache location to be invalidated. The `cache_size` represents the number of bytes from the `cache_addr` to invalidate.

Note that *cache lines* are invalidated starting from the cache line to which cache_addr belongs and ending at the cache line containing the address (`cache_addr` + `cache_size` - 1).

For example, `Xil_ICacheInvalidateRange` (0x00000300, 0x100) invalidates the instruction cache region from 0x300 to 0x3ff (0x100 bytes of cache memory is cleared starting from 0x300).

If the L2 cache system (system cache) is present in the hardware system, this function invalidates relevant cache lines in the L2 cache as well. The invalidation starts with the L2 cache and moves to the L1 cache.

Note: For MicroBlaze processors prior to version v7.20.a: The cache and interrupts are disabled before invalidation starts and restored to their previous state after invalidation.

MicroBlaze Processor Data Cache Handling

The following functions help manage data caches on the MicroBlaze processor. You must include the header file `xil_cache.h` in your source code to use these functions.

Note: These functions work correctly only when the parameters that determine the caching system are configured appropriately in the MicroBlaze MHS hardware block. Refer to the *MicroBlaze Processor Reference Guide (UG081)* for information on how to configure these cache parameters. "MicroBlaze Processor API," page 1 contains a link to this document.

Data Cache Handling Functions

`void` **`Xil_DCacheEnable`**`(void)`

Enable the data cache on the MicroBlaze processor. When the MicroBlaze processor starts up, the data cache is disabled. The data cache must be explicitly turned on using this function.

`void` **`Xil_DCache_Disable`**`(void)`

Disable the data cache on the MicroBlaze processor. If writeback caches are enabled in the MicroBlaze processor hardware, this function also flushes the dirty data in the cache back to external memory and invalidates the cache. For write through caches, this function does not do any extra processing other than disabling the cache.

If the L2 cache system is present in the hardware, this function flushes the L2 cache before disabling the DCache.

`void` **`Xil_DCacheFlush`**`()`

Flush the entire data cache. This function can be used when write-back caches are turned on in the MicroBlaze processor hardware. Executing this function ensures that the dirty data in the cache is written back to external memory and the contents invalidated.

If the L2 cache system is present in the hardware, this function flushes the L2 cache first, before flushing the L1 cache.

`void` **`Xil_DCacheFlushRange`**`(unsigned int` *`cache_addr`*`, unsigned int` *`cache_len`*`)`

Flush the specified data cache range. This function can be used when write-back caches are enabled in the MicroBlaze processor hardware. Executing this function ensures that the dirty data in the cache range is written back to external memory and the contents of the cache range are invalidated. Note that *cache lines* will be flushed starting from the cache line to which cache_addr belongs and ending at the cache line containing the address (*`cache_addr`* + *`cache_size`* - 1).

If the L2 cache system is present in the hardware, this function flushes the relevant L2 cache range first, before flushing the L1 cache range.

For example, `Xil_DCacheFlushRange (0x00000300, 0x100)` flushes the data cache region from 0x300 to 0x3ff (0x100 bytes of cache memory is flushed starting from 0x300).

void **Xil_DCacheInvalidate**()

Invalidate the data cache.

If the L2 cache system is present in the hardware, this function invalidates the L2 cache first, before invalidating the L1 cache.

Note: For MicroBlaze processors prior to version v7.20.a, the cache and interrupts are disabled before invalidation starts and restored to their previous state after invalidation.

---

void **Xil_DCacheInvalidateRange**(unsigned int *cache_addr*, unsigned int *cache_size*

Invalidate the data cache. This function can be used for invalidating all or part of the data cache. The parameter *cache_addr* indicates the beginning of the cache location and *cache_size* represents the size from *cache_addr* to invalidate.

Note that *cache lines* will be invalidated starting from the cache line to which *cache_addr* belongs and ending at the cache line containing the address (*cache_addr* + *cache_size* - 1).

If the L2 cache system is present in the hardware, this function invalidates the relevant L2 cache range first, before invalidating the L1 cache range.

Note: For MicroBlaze processors prior to version v7.20.a, the cache and interrupts are disabled before invalidation starts and restored to their previous state after invalidation.

For example, `Xil_DCacheInvalidateRange` (0x00000300, 0x100) invalidates the data cache region from 0x300 to 0x3ff (0x100 bytes of cache memory is cleared starting from 0x300).

Software Sequence for Initializing Instruction and Data Caches

Typically, before using the cache, your program must perform a particular sequence of cache operations to ensure that invalid/dirty data in the cache is not being used by the processor. This would typically happen during repeated program downloads and executions.

The following example snippets show the necessary software sequence for initializing instruction and data caches in your program.

```
/* Initialize ICache *//
Xil_ICacheInvalidate ();
Xil_ICacheEnable ();

/* Initialize DCache */
Xil_DCacheInvalidate ();
Xil_DCacheEnable ();
```

At the end of your program, you should also put in a sequence similar to the example snippet below. This ensures that the cache and external memory are left in a valid and clean state.

```
/* Clean up DCache. For writeback caches, the disable_dcache routine
   internally does the flush and invalidate. For write through caches,
    an explicit invalidation must be performed on the entire cache. */

#if XPAR_MICROBLAZE_DCACHE_USE_WRITEBACK == 0
Xil_DCacheInvalidate ();
#endif

Xil_DCacheDisable ();

/* Clean up ICache */
Xil_ICacheInvalidate ();
Xil_ICacheDisable ();
```

MicroBlaze Processor Fast Simplex Link (FSL) Interface Macros

Standalone includes macros to provide convenient access to accelerators connected to the MicroBlaze Fast Simplex Link (FSL) Interfaces.

MicroBlaze Processor Fast Simplex Link (FSL) Interface Macro Summary

The following is a list of the available macros. Click on a macro name to go to the description of the active macros.

getfslx(val,id,flags)
putfslx(val,id,flags)
tgetfslx(val,id,flags)
getd fslx(val,id,flags)
putdfslx(val,id,flags)
tgetdfslx(val,id,flags)
tputdfslx(val,id,flags)
fsl_isinvalid(invalid)
fsl_iserror(error)

MicroBlaze Processor FSL Macro Descriptions

The following macros provide access to all of the functionality of the MicroBlaze FSL feature in one simple and parameterized interface. Some capabilities are available on MicroBlaze v7.00.a and later only, as noted in the descriptions.

In the macro descriptions, *val* refers to a variable in your program that can be the source or sink of the FSL operation.

Note: *id* must be an integer *literal* in the basic versions of the macro (`getfslx, putfslx, tgetfslx, tputfslx`) and can be an integer literal or an integer variable in the dynamic versions of the macros (`getdfslx, putdfslx, tgetdfslx, tputdfslx.`)

You must include `fsl.h` in your source files to make these macros available.

`getfslx(`*`val,id,flags`*`)`

Performs a get function on an input FSL of the MicroBlaze processor; id is the FSL identifier and is a literal in the range of 0 to 7 (0 to 15 for MicroBlaze v7.00.a and later). The semantics of the instruction is determined by the valid FSL macro flags, which are listed in Table 2, page 9.

`putfslx(`*`val,id,flags`*`)`

Performs a put function on an input FSL of the MicroBlaze processor; id is the FSL identifier and is a literal in the range of 0 to 7 (0 to 15 for MicroBlaze processor v7.00.a and later).

The semantics of the instruction is determined by the valid FSL macro flags, which are listed in Table 2, page 9.

`tgetfslx(`*`val,id,flags`*`)`

Performs a test get function on an input FSL of the MicroBlaze processor; id is the FSL identifier and is a literal in the ranging of 0 to 7 (0 to 15 for MicroBlaze v7.00.a and later). This macro can be used to test reading a single value from the FSL. The semantics of the instruction is determined by the valid FSL macro flags, which are listed in Table 2, page 9.

`tputfslx(`*`val,id,flags`*`)`

Performs a put function on an input FSL of the MicroBlaze processor; id is the FSL identifier and is a literal in the range of 0 to 7 (0 to 15 for MicroBlaze processor v7.00.a and later). This macro can be used to test writing a single value to the FSL.The semantics of the put instruction is determined by the valid FSL macro flags, which are listed in Table 2, page 9.

getd fslx(*val,id,flags*)

Performs a get function on an input FSL of the MicroBlaze processor; id is the FSL identifier and is an integer value or variable in the range of 0 to 15. The semantics of the instruction is determined by the valid FSL macro flags, which are listed in Table 2, page 9. This macro is available on MicroBlaze processor v7.00.a and later only.

---

putdfslx(*val,id,flags*)

Performs a put function on an input FSL of the MicroBlaze processor; id is the FSL identifier and is an integer value or variable in the range of 0 to 15. The semantics of the instruction is determined by the valid FSL macro flags, which are listed in Table 2, page 9. This macro is available on MicroBlaze processor v7.00.a and later only.

---

tgetdfslx(*val,id,flags*)

Performs a test get function on an input FSL of the MicroBlaze processor; id is the FSL identifier and is an integer or variable in the range of 0 to 15. This macro can be used to test reading a single value from the FSL. The semantics of the instruction is determined by the valid FSL macro flags, listed in Table 2, page 9. This macro is available on MicroBlaze processor v7.00.a and later only.

---

tputdfslx(*val,id,flags*)

Performs a put function on an input FSL of the MicroBlaze processor; id is the FSL identifier and is an integer or variable in the range of 0 to 15. This macro can be used to test writing a single value to the FSL.The semantics of the instruction is determined by the valid FSL macro flags, listed in Table 2, page 9. This macro is available on MicroBlaze processor v7.00.a and later only.

---

fsl_isinvalid(*invalid*)

Checks if the last FSL operation returned valid data. This macro is applicable after invoking a non-blocking FSL put or get instruction. If there was no data on the FSL channel on a get, or if the FSL channel was full on a put, *invalid* is set to 1; otherwise, it is set to 0.

---

fsl_iserror(*error*)

This macro is used to check if the last FSL operation set an error flag. This macro is applicable after invoking a control FSL put or get instruction. If the control bit was set *error* is set to 1; otherwise, it is set to 0.

MicroBlaze Processor FSL Macro Flags

Table 2 lists the available FSL Macro flags.

Table 2: **FSL Macro Flags**

Flag	Description
FSL_DEFAULT	Blocking semantics (on MicroBlaze processor v7.00.a and later this mode is interruptible).
FSL_NONBLOCKING	Non-blocking semantics.[1]
FSL_EXCEPTION	Generate exceptions on control bit mismatch.[2]
FSL_CONTROL	Control semantics.
FSL_ATOMIC	Atomic semantics. A sequence of FSL instructions cannot be interrupted.
FSL_NONBLOCKING_EXCEPTION	Combines non-blocking and exception semantics.
FSL_NONBLOCKING_CONTROL	Combines non-blocking and control semantics.
FSL_NONBLOCKING_ATOMIC	Combines non-blocking and atomic semantics.
FSL_EXCEPTION_CONTROL	Combines exception and control semantics.
FSL_EXCEPTION_ATOMIC	Combines exception and atomic semantics.
FSL_CONTROL_ATOMIC	Combines control and atomic semantics.
FSL_NONBLOCKING_EXCEPTION_CONTROL	Combines non-blocking, exception, and control semantics.[2]
FSL_NONBLOCKING_EXCEPTION_ATOMIC	Combines non-blocking, exception, and atomic semantics.
FSL_NONBLOCKING_CONTROL_ATOMIC	Combines non-blocking, atomic, and control semantics.
FSL_EXCEPTION_CONTROL_ATOMIC	Combines exception, atomic, and control semantics.
FSL_NONBLOCKING_EXCEPTION_CONTROL_ATOMIC	Combines non-blocking, exception, control, and atomic semantics.

1. When non-blocking semantics are not applied, blocking semantics are implied.
2. This combination of flags is available only on MicroBlaze processor v7.00.a and later versions.

Deprecated MicroBlaze Processor Fast Simplex Link (FSL) Macros

The following macros are deprecated:

`getfsl(val,id)(deprecated)`

Performs a blocking data get function on an input FSL of the MicroBlaze processor; *id* is the FSL identifier in the range of 0 to 7. This macro is uninterruptible.

`putfsl(val,id)(deprecated)`

Performs a blocking data put function on an output FSL of the MicroBlaze processor; *id* is the FSL identifier in the range of 0 to 7. This macro is uninterruptible.

ngetfsl(*val,id*)(deprecated)

Performs a non-blocking data get function on an input FSL of the MicroBlaze processor; *id* is the FSL identifier in the range of 0 to 7.

---

nputfsl(*val,id*)(deprecated)

Performs a non-blocking data put function on an output FSL of the MicroBlaze processor; *id* is the FSL identifier in the range of 0 to 7.

---

cgetfsl(*val, id*)(deprecated)

Performs a blocking control get function on an input FSL of the MicroBlaze processor; *id* is the FSL identifier in the range of 0 to 7. This macro is uninterruptible.

---

cputfsl(*val, id*)(deprecated)

Performs a blocking control put function on an output FSL of the MicroBlaze processor; *id* is the FSL identifier in the range of 0 to 7. This macro is uninterruptible.

---

ncgetfsl(*val, id*)(deprecated)

Performs a non-blocking control get function on an input FSL of the MicroBlaze processor; *id* is the FSL identifier in the range of 0 to 7.

---

ncputfsl(*val, id*)(deprecated)

Performs a non-blocking control put function on an output FSL of the MicroBlaze processor; *id* is the FSL identifier in the range of 0 to 7.

---

getfsl_interruptible(*val, id*)(deprecated)

Performs repeated non-blocking data get operations on an input FSL of the MicroBlaze processor until valid data is actually fetched; *id* is the FSL identifier in the range of 0 to 7. Because the FSL access is non-blocking, interrupts will be serviced by the processor.

---

putfsl_interruptible(*val, id*)(deprecated)

Performs repeated non-blocking data put operations on an output FSL of the MicroBlaze processor until valid data is sent out; *id* is the FSL identifier in the range of 0 to 7. Because the FSL access is non-blocking, interrupts will be serviced by the processor.

cgetfsl_interruptible(*val, id*)(deprecated)

Performs repeated non-blocking control get operations on an input FSL of the MicroBlaze processor until valid data is actually fetched; *id* is the FSL identifier in the range of 0 to 7. Because the FSL access is non-blocking, interrupts are serviced by the processor.

---

cputfsl_interruptible(*val, id*)(deprecated)

Performs repeated non-blocking control put operations on an output FSL of the MicroBlaze processor until valid data is sent out; *id* is the FSL identifier in the range of 0 to 7. Because the FSL access is non-blocking, interrupts are serviced by the processor.

MicroBlaze Processor Pseudo-asm Macros

Standalone includes macros to provide convenient access to various registers in the MicroBlaze processor. Some of these macros are very useful within exception handlers for retrieving information about the exception. To use these macros, you must include the `mb_interface.h` header file in your source code.

MicroBlaze Processor Pseudo-asm Macro Summary

The following is a summary of the MicroBlaze processor pseudo-asm macros. Click on the macro name to go to the description.

mfgpr(rn)
mfmsr( )
mfesr( )
mfear( )
mffsr( )
mtmsr(v)
mtgpr(rn,v)
microblaze_getfpex_operand_a( )
microblaze_getfpex_operand_b( )
clz(v)
mbar(mask)
mb_swapb(v)
mb_swaph(v)
mb_sleep

MicroBlaze Processor Pseudo-asm Macro Descriptions

---

mfgpr(*rn*)

Return value from the general purpose register (GPR) *rn*.

---

mfmsr( )

Return the current value of the MSR.

---

mfesr( )

Return the current value of the Exception Status Register (ESR).

---

mfear( )

Return the current value of the Exception Address Register (EAR).

mffsr( )

Return the current value of the Floating Point Status (FPS).

---

mtmsr(*v*)

Move the value v to MSR.

---

mtgpr(*rn,v*)

Move the value *v* to GPR *rn*.

---

microblaze_getfpex_operand_a( )

Return the saved value of operand A of the last faulting floating point instruction.

---

microblaze_getfpex_operand_b( )

Return the saved value of operand B of the last faulting floating point instruction.

Note: Because of the way some of these macros have been written, they cannot be used as parameters to function calls and other such constructs.

---

clz(v)

Counts the number of leading zeros in the data specified by v

---

mbar(mask)

This instruction ensures that outstanding memory accesses on memory interfaces are completed before any subsequent instructions are executed. mask value of 1 specifies data side barrier, mask value of 2 specifies instruction side barrier and mask value of 16 specifies to put the processor in sleep.

---

mb_swapb(v)

Swaps the bytes in the data specified bv v. This converts the bytes in the data from little endian to big endian or vice versa. So v contains a value of 0x12345678, the macro will return a value of 0x78563412.

---

mb_swaph(v)

Swaps the half words in the data specified bv v. So if v has a value of 0x12345678, the macro will return a value of 0x56781234.

---

mb_sleep

Puts the processor in sleep.

MicroBlaze Processor Version Register (PVR) Access Routine and Macros

MicroBlaze processor v5.00.a and later versions have configurable Processor Version Registers (PVRs). The contents of the PVR are captured using the *pvr_t* data structure, which is defined as an array of 32-bit words, with each word corresponding to a PVR register on hardware. The number of PVR words is determined by the number of PVRs configured in the hardware. You should not attempt to access PVR registers that are not present in hardware, as the *pvr_t* data structure is resized to hold only as many PVRs as are present in hardware.

To access information in the PVR:

1. Use the `microblaze_get_pvr()` function to populate the PVR data into a *pvr_t* data structure.
2. In subsequent steps, you can use any one of the PVR access macros list to get individual data stored in the PVR.

Note: The PVR access macros take a parameter, which must be of type *pvr_t*.

PVR Access Routine

The following routine is used to access the PVR. You must include `pvr.h` file to make this routine available.

`int` **`microblaze_get_pvr`**`(`*`pvr_t *pvr`*`)`

Populate the PVR data structure to which *pvr* points with the values of the hardware PVR registers. This routine populates only as many PVRs as are present in hardware and the rest are zeroed. This routine is not available if `C_PVR` is set to NONE in hardware.

PVR Macros

The following processor macros are used to access the PVR. You must include `pvr.h` file to make these macros available.

Table 3 lists the MicroBlaze processor PVR macros and descriptions.

Table 3: **PVR Access Macros**

Macro	Description
`MICROBLAZE_PVR_IS_FULL(pvr)`	Return non-zero integer if PVR is of type FULL, 0 if basic.
`MICROBLAZE_PVR_USE_BARREL(pvr)`	Return non-zero integer if hardware barrel shifter present.
`MICROBLAZE_PVR_USE_DIV(pvr)`	Return non-zero integer if hardware divider present.
`MICROBLAZE_PVR_USE_HW_MUL(pvr)`	Return non-zero integer if hardware multiplier present.
`MICROBLAZE_PVR_USE_FPU(pvr)`	Return non-zero integer if hardware floating point unit (FPU) present.
`MICROBLAZE_PVR_USE_FPU2(pvr)`	Return non-zero integer if hardware floating point conversion and square root instructions are present.
`MICROBLAZE_PVR_USE_ICACHE(pvr)`	Return non-zero integer if I-cache present.
`MICROBLAZE_PVR_USE_DCACHE(pvr)`	Return non-zero integer if D-cache present.

Table 3: **PVR Access Macros *(Cont'd)***

Macro	Description
`MICROBLAZE_PVR_MICROBLAZE_VERSION (pvr)`	Return MicroBlaze processor version encoding. Refer to the *MicroBlaze Processor Reference Guide (UG081)* for mappings from encodings to actual hardware versions. "MicroBlaze Processor API," page 1 contains a link to this document.
`MICROBLAZE_PVR_USER1(pvr)`	Return the USER1 field stored in the PVR.
`MICROBLAZE_PVR_USER2(pvr)`	Return the USER2 field stored in the PVR.
`MICROBLAZE_PVR_INTERCONNECT(pvr)`	Return non-zero if MicroBlaze processor has PLB interconnect; otherwise return zero.
`MICROBLAZE_PVR_D_PLB(pvr)`	Return non-zero integer if Data Side PLB interface is present.
`MICROBLAZE_PVR_D_OPB(pvr)`	Return non-zero integer if Data Side On-chip Peripheral Bus (OPB) interface present.
`MICROBLAZE_PVR_D_LMB(pvr)`	Return non-zero integer if Data Side Local Memory Bus (LMB) interface present.
`MICROBLAZE_PVR_I_PLB(pvr)`	Return non-zero integer if Instruction Side PLB interface is present.
`MICROBLAZE_PVR_I_OPB(pvr)`	Return non-zero integer if Instruction side OPB interface present.
`MICROBLAZE_PVR_I_LMB(pvr)`	Return non-zero integer if Instruction side LMB interface present.
`MICROBLAZE_PVR_INTERRUPT_IS_EDGE (pvr)`	Return non-zero integer if interrupts are configured as edge-triggered.
`MICROBLAZE_PVR_EDGE_IS_POSITIVE (pvr)`	Return non-zero integer if interrupts are configured as positive edge triggered.
`MICROBLAZE_PVR_USE_MUL64(pvr)`	Return non-zero integer if MicroBlaze processor supports 64-bit products for multiplies.
`MICROBLAZE_PVR_OPCODE_0x0_ILLEGAL (pvr)`	Return non-zero integer if opcode 0x0 is treated as an illegal opcode.
`MICROBLAZE_PVR_UNALIGNED_EXCEPTION (pvr)`	Return non-zero integer if unaligned exceptions are supported.
`MICROBLAZE_PVR_ILL_OPCODE_ EXCEPTION(pvr)`	Return non-zero integer if illegal opcode exceptions are supported.
`MICROBLAZE_PVR_IOPB_EXCEPTION(pvr)`	Return non-zero integer if I-OPB exceptions are supported.
`MICROBLAZE_PVR_DOPB_EXCEPTION(pvr)`	Return non-zero integer if D-OPB exceptions are supported.
`MICROBLAZE_PVR_IPLB_EXCEPTION(pvr)`	Return non-zero integer if I-PLB exceptions are supported.
`MICROBLAZE_PVR_DPLB_EXCEPTION(pvr)`	Return non-zero integer if D-PLB exceptions are supported.
`MICROBLAZE_PVR_DIV_ZERO_EXCEPTION (pvr)`	Return non-zero integer if divide by zero exceptions are supported.

Table 3: **PVR Access Macros *(Cont'd)***

Macro	Description
MICROBLAZE_PVR_FPU_EXCEPTION(pvr)	Return non-zero integer if FPU exceptions are supported.
MICROBLAZE_PVR_FSL_EXCEPTION(pvr)	Return non-zero integer if FSL exceptions are present.
MICROBLAZE_PVR_DEBUG_ENABLED(pvr)	Return non-zero integer if debug is enabled.
MICROBLAZE_PVR_NUM_PC_BRK(pvr)	Return the number of hardware PC breakpoints available.
MICROBLAZE_PVR_NUM_RD_ADDR_BRK (pvr)	Return the number of read address hardware watchpoints supported.
MICROBLAZE_PVR_NUM_WR_ADDR_BRK (pvr)	Return the number of write address hardware watchpoints supported.
MICROBLAZE_PVR_FSL_LINKS(pvr)	Return the number of FSL links present.
MICROBLAZE_PVR_ICACHE_BASEADDR (pvr)	Return the base address of the I-cache.
MICROBLAZE_PVR_ICACHE_HIGHADDR (pvr)	Return the high address of the I-cache.
MICROBLAZE_PVR_ICACHE_ADDR_TAG_ BITS(pvr)	Return the number of address tag bits for the I-cache.
MICROBLAZE_PVR_ICACHE_USE_FSL(pvr)	Return non-zero if I-cache uses FSL links.
MICROBLAZE_PVR_ICACHE_ALLOW_WR (pvr)	Return non-zero if writes to I-caches are allowed.
MICROBLAZE_PVR_ICACHE_LINE_LEN (pvr)	Return the length of each I-cache line in bytes.
MICROBLAZE_PVR_ICACHE_BYTE_SIZE (pvr)	Return the size of the D-cache in bytes.
MICROBLAZE_PVR_DCACHE_BASEADDR (pvr)	Return the base address of the D-cache.
MICROBLAZE_PVR_DCACHE_HIGHADDR (pvr)	Return the high address of the D-cache.
MICROBLAZE_PVR_DCACHE_ADDR_TAG_ BITS(pvr)	Return the number of address tag bits for the D-cache.
MICROBLAZE_PVR_DCACHE_USE_FSL(pvr)	Return non-zero if the D-cache uses FSL links.
MICROBLAZE_PVR_DCACHE_ALLOW_WR (pvr)	Return non-zero if writes to D-cache are allowed.
MICROBLAZE_PVR_DCACHE_LINE_LEN (pvr)	Return the length of each line in the D-cache in bytes.
MICROBLAZE_PVR_DCACHE_BYTE_SIZE (pvr)	Return the size of the D-cache in bytes.
MICROBLAZE_PVR_TARGET_FAMILY(pvr)	Return the encoded target family identifier.

Table 3: **PVR Access Macros *(Cont'd)***

Macro	Description
`MICROBLAZE_PVR_MSR_RESET_VALUE`	Refer to the *MicroBlaze Processor Reference Guide (UG081)* for mappings from encodings to target family name strings. "MicroBlaze Processor API," page 1 contains a link to this document.
`MICROBLAZE_PVR_MMU_TYPE(pvr)`	Returns the value of C_USE_MMU. Refer to the *MicroBlaze Processor Reference Guide (UG081)* for mappings from MMU type values to MMU function. "MicroBlaze Processor API," page 1 contains a link to this document.

MicroBlaze Processor File Handling

The following routine is included for file handling:

`int` **`fcntl`**`(int` *`fd, int cmd, long arg`*`);`

A dummy implementation of `fcntl( )`, which always returns 0, is provided. **`fcntl`** is intended to manipulate file descriptors according to the command specified by *`cmd.`* Because Standalone does not provide a file system, this function is included for completeness only.

MicroBlaze Processor Errno

The following routine provides the error number value:

`int` **`errno`**`( );`

Return the global value of errno as set by the last C library call.

Cortex A9 Processor API

Standalone BSP contains boot code, cache, exception handling, file and memory management, configuration, time and processor-specific include functions. It supports gcc compilers.

The following lists the Cortex A9 Processor API sections.You can click on a link to go directly to the function section.

- Cortex A9 Processor Boot Code
- Cortex A9 Processor Cache Functions
- Cortex A9 Processor Exception Handling
- Cortex A9 Processor File Support
- Cortex A9 gcc Errno Function
- Cortex A9 gcc Memory Management
- Cortex A9 gcc Process Functions
- Cortex A9 Processor-Specific Include Files
- Cortex A9 Time Functions

The following subsections describe the functions by type.

Cortex A9 Processor Boot Code

The boot.S file contains a minimal set of code for transferring control from the processor's reset location to the start of the application. It performs the following tasks.

- Invalidate L1 caches, TLBs, Branch Predictor Array, etc.
- Invalidate L2 caches and initialize L2 Cache Controller
- Enable caches and MMU
- Load MMU translation table base address into the TTB registers
- Enable NEON coprocessor

The boot code also starts the Cycle Counter and initializes the Static Memory Controller.

Cortex A9 Processor Cache Functions

The xil_cache.c file and the corresponding xil_cache.h header file provide access to the following cache and cache-related operations.

Cache Function Summary

The following are links to the function descriptions. Click on the name to go to that function.

void Xil_DCacheEnable(void)

void Xil_DCacheInvalidate(void)

void Xil_DCacheInvalidateLine(unsigned int adr)

void Xil_DCacheInvalidateRange(unsigned int adr, unsigned len)

void Xil_DCacheFlush(void)

void Xil_DCacheFlushLine(unsigned int adr)

void Xil_DCacheFlushRange(unsigned int adr, unsigned len)

void Xil_DCacheStoreLine(unsigned int adr)

void Xil_ICacheEnable(void)

void Xil_ICacheDisable(void)

void Xil_ICacheInvalidate(void)
void Xil_ICacheInvalidateLine(unsigned int adr)
void Xil_ICacheInvalidateRange(unsigned int adr, unsigned len)
void Xil_L1DCacheEnable(void)
void Xil_L1DCacheDisable(void)
void Xil_L1DCacheInvalidate(void)
void Xil_L1DCacheInvalidateLine(unsigned int adr)
void Xil_L2CacheInvalidateRange(unsigned int adr, unsigned len)
void Xil_L1DCacheFlush(void)
void Xil_L1DCacheFlushLine(unsigned int adr)
void Xil_L1DCacheFlushRange(unsigned int adr, unsigned len)
void Xil_L1DCacheStoreLine(unsigned int adr)
void Xil_L1ICacheEnable(void)
void Xil_ICacheDisable(void)
void Xil_ICacheInvalidate(void)
void Xil_L1ICacheInvalidateLine(unsigned int adr)
void Xil_L1ICacheInvalidateRange(unsigned int adr, unsigned len)
void Xil_L2CacheEnable(void)
void Xil_L2CacheDisable(void)
void Xil_L2CacheInvalidate(void)
void Xil_L2CacheInvalidateLine(unsigned int adr)
void Xil_L2CacheInvalidateRange(unsigned int adr, unsigned len)
void Xil_L2CacheFlush(void)
void Xil_L2CacheFlushLine(unsigned int adr)
void Xil_L2CacheFlushRange(unsigned int adr, unsigned len)
void Xil_L2CacheStoreLine(unsigned int adr)

Cache Function Descriptions

`void` **`Xil_DCacheEnable`**`(void)`

Enable the data caches.

`void` **`Xil_DCacheInvalidate`**`(void)`

Invalidate the entire data cache.

`void` **`Xil_DCacheInvalidateLine`**`(unsigned int` *`adr`*`)`

Invalidate a data cache line. If the byte specified by adr is cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the modified contents are lost and are not written to system memory before the line is invalidated. A subsequent data access to this address results in a cache miss and a cache line refill.

void **Xil_DCacheInvalidateRange**(unsigned int *adr*, unsigned *len*)

Invalidates the data cache lines that are described by the address range starting from adr and len bytes long. A subsequent data access to any address in this range results in a cache miss and a cache line refill.

---

void **Xil_DCacheFlush**(void)

Flush the entire Data cache.

---

void **Xil_DCacheFlushLine**(unsigned int *adr*)

Flush a Data cache line. If the byte specified by the address (adr) is cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the entire contents of the cacheline are written to system memory before the line is invalidated. A subsequent data access to this address results in a cache miss and a cache line refill.

---

void **Xil_DCacheFlushRange**(unsigned int *adr*, unsigned *len*)

Flushes the data cache lines that are described by the address range starting from adr and len bytes long. A subsequent data access to any address in this range results in a cache miss and a cache line refill.

---

void **Xil_DCacheStoreLine**(unsigned int *adr*)

Store a Data cache line. If the byte specified by the adr is cached by the data cache and the cacheline is modified (dirty), the entire contents of the cacheline are written to system memory. After the store completes, the cacheline is marked as unmodified (not dirty).

---

void **Xil_ICacheEnable**(void)

Enable the instruction caches.

---

void **Xil_ICacheDisable**(void)

Disable the instruction caches.

---

void **Xil_ICacheInvalidate**(void)

Invalidate the entire instruction cache.

---

void **Xil_ICacheInvalidateLine**(unsigned int *adr*)

Invalidate an instruction cache line. If the instruction specified by the parameter adr is cached by the instruction cache, the cacheline containing that instruction is invalidated.

void **Xil_ICacheInvalidateRange**(unsigned int *adr*, unsigned *len*)

Invalidate the instruction cache for the given address range. If the bytes specified by the adr are cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the modified contents are lost and are not written to system memory before the line is invalidated.

---

void **Xil_L1DCacheEnable**(void)

Enable the level 1 data cache.

---

void **Xil_L1DCacheDisable**(void)

Disable the level 1 data cache.

---

void **Xil_L1DCacheInvalidate**(void)

Invalidate the level 1 data cache.

---

void **Xil_L1DCacheInvalidateLine**(unsigned int *adr*)

Invalidate a level 1 data cache line. If the byte specified by the adr is cached by the data cache, the cacheline containing that byte is invalidated.If the cacheline is modified (dirty), the modified contents are lost and are not written to system memory before the line is invalidated.

---

void **Xil_L1DCacheInvalidateRange**(unsigned int *adr*, unsigned *len*)

Invalidate the level 1 data cache for the given address range. If the bytes specified by the adr are cached by the sata cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the modified contents are lost and are not written to system memory before the line is invalidated.

---

void **Xil_L1DCacheFlush**(void)

Flush the level 1 data cache.

---

void **Xil_L1DCacheFlushLine**(unsigned int *adr*)

Flush a level 1 data cache line. If the byte specified by the adr is cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the entire contents of the cacheline are written to system memory before the line is invalidated.

---

void **Xil_L1DCacheFlushRange**(unsigned int *adr*, unsigned *len*)

Flush the level 1 data cache for the given address range. If the bytes specified by the adr are cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the written to system memory first before the before the line is invalidated.

void **Xil_L1DCacheStoreLine**(unsigned int *adr*)

Store a level 1 data cache line. If the byte specified by the adr is cached by the data cache and the cacheline is modified (dirty), the entire contents of the cacheline are written to system memory. After the store completes, the cacheline is marked as unmodified (not dirty).

---

void **Xil_L1ICacheEnable**(void)

Enable the level 1 instruction cache.

---

void **Xil_L1ICacheDisable**(void)

Disable level 1 the instruction cache.

---

void **Xil_L1ICacheInvalidate**(void)

Invalidate the entire level 1 instruction cache.

---

void **Xil_L1ICacheInvalidateLine**(unsigned int *adr*)

Invalidate a level 1 instruction cache line. If the instruction specified by the parameter adr is cached by the instruction cache, the cacheline containing that instruction is invalidated.

---

void **Xil_L1ICacheInvalidateRange**(unsigned int *adr*, unsigned *len*)

Invalidate the level 1 instruction cache for the given address range. If the bytes specified by the adr are cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the modified contents are lost and are not written to system memory before the line is invalidated.

---

void **Xil_L2CacheEnable**(void)

Enable the L2 cache.

---

void **Xil_L2CacheDisable**(void)

Disable the L2 cache.

---

void **Xil_L2CacheInvalidate**(void)

Invalidate the L2 cache. If the byte specified by the adr is cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the modified contents are lost and are not written to system memory before the line is invalidated.

---

void **Xil_L2CacheInvalidateLine**(unsigned int *adr*)

Invalidate a level 2 cache line. If the byte specified by the adr is cached by the Data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the modified contents are lost and are not written to system memory before the line is invalidated.

void **Xil_L2CacheInvalidateRange**(unsigned int *adr*, unsigned *len*)

Invalidate the level 2 cache for the given address range. If the bytes specified by the adr are cached by the data cache, the cacheline containing that byte is invalidated.If the cacheline is modified (dirty), the modified contents are lost and are not written to system memory before the line is invalidated.

---

void **Xil_L2CacheFlush**(void)

Flush the L2 cache. If the byte specified by the adr is cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the entire contents of the cacheline are written to system memory before the line is invalidated.

---

void **Xil_L2CacheFlushLine**(unsigned int *adr*)

Flush a level 1 cache line. If the byte specified by the adr is cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the entire contents of the cacheline are written to system memory before the line is invalidated.

---

void **Xil_L2CacheFlushRange**(unsigned int *adr*, unsigned *len*)

Flush the level 2 cache for the given address range. If the bytes specified by the adr are cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the written to system memory first before the before the line is invalidated.

---

void **Xil_L2CacheStoreLine**(unsigned int *adr*)

Store a level 2 cache line. If the byte specified by the adr is cached by the data cache and the cacheline is modified (dirty), the entire contents of the cacheline are written to system memory. After the store completes, the cacheline is marked as unmodified (not dirty).

---

void **XL2cc_EventCtrInit**(int Event0, int Event1)

This function initializes the event counters in L2 Cache controller with a set of event codes specified by the user. Use the event codes defined by XL2CC_* in xl2cc_counter.h to specify the events Event0 and Event1.

---

void **XL2cc_EventCtrStart**(void)

This function starts the event counters in L2 Cache controller.

---

void **XL2cc_EventCtrStop**(u32 *EveCtr0, u32 *EveCtr1)

This function disables the event counters in L2 Cache controller, saves the

counter values to address pointed to by EveCtr0 and EveCtr1 and resets the counters.

Cortex A9 Processor MMU Handling

The standalone BSP MMU handling API is implemented in file `xil_mmu.c` and the corresponding header `file xil_mmu.h`.

MMU Handling Function Summary

The following function describes the available MMU handling API.

`void` **`Xil_SetTlbAttributes`**`(u32 addr, u32 attrib)`

This function changes the MMU attribute of the 1 MB address range in which the passed memory address "addr" falls.

The new MMU attribute is passed as an argument "attrib" to this API.

This API can be used to change attributes such as cache-ability and share-ability of a specified memory region.

Cortex A9 Processor Exception Handling

The Standalone BSP provides an exception handling API. For details about the exceptions and interrupts on ARM Cortex-A9 processor, refer to "Exceptions" under the chapter "The System Level Programmers' Model" in the ARM Architecture Reference Manual ARMv7-A and ARMv-7R edition.

The exception handling API is implemented in a set of the files - asm_vectors.S, vectors.c, xil_exception.c, and the corresponding header files vectors.h and xil_exception.h.

Exception Handling Function Summary

The following are links to the function descriptions. Click on the name to go to that function.

void Xil_ExceptionInit(void)

void Xil_ExceptionRegisterHandler (u8 ExceptionId, XExceptionHandler Handler, void *DataPtr)

void Xil_ExceptionRemoveHandler (u8 ExceptionId)

void Xil_ExceptionEnableMask(Mask)

void Xil_ExceptionEnable(void)

void Xil_ExceptionDisableMask(Mask)

void Xil_ExceptionDisable(void)

Exception Handling Function Descriptions

`void` **`Xil_ExceptionInit`**`(void)`

Sets up the interrupt vector table and registers a "do nothing" function for each exception. This function has no parameters and does not return a value. This function must be called before registering any exception handlers or enabling any interrupts.

void **Xil_ExceptionRegisterHandler** (u8 ExceptionId, XExceptionHandler Handler, void *DataPtr)

Registers an exception handler for a specific exception; does not return a value. Refer to Table 1, for a list of exception types and their values.

The parameters are:

- **ExceptionId** is of parameter type u8, and is the exception to which this handler should be registered. The type and the values are defined in the xil_exception.h header file.
- **Handler** is an Xil_ExceptionHandler parameter that is the pointer to the exception handling function.

  The function provided as the Handler parameter must have the following function prototype:

  typedef void (*Xil_ExceptionHandler)(void * DataPtr);

  This prototype is declared in the xil_exception.h header file.
- **DataPtr** is of parameter type void * and is the user value to be passed when the Handler is called.

  When this Handler function is called, the parameter DataPtr contains the same value provided, when the Handler was registered.

Table 4: Registered Exception Types and Values

Exception Type	Value
XIL_EXCEPTION_ID_RESET	0
XIL_EXCEPTION_ID_UNDEFINED_INT	1
XIL_EXCEPTION_ID_SWI_INT	2
XIL_EXCEPTION_ID_PREFETCH_ABORT_INT	3
XIL_EXCEPTION_ID_DATA_ABORT_INT	4
XIL_EXCEPTION_ID_IRQ_INT	5
XIL_EXCEPTION_ID_FIQ_INT	6

---

void **Xil_ExceptionRemoveHandler** (u8 ExceptionId)

De-register a handler function for a given exception. For possible values of parameter ExceptionId, refer to Table 1.

---

void **Xil_ExceptionEnableMask**(Mask)

Enable exceptions specified by Mask. The parameter Mask is a bitmask for exceptions to be enabled. The Mask parameter can have the values XIL_EXCEPTION_IRQ, XIL_EXCEPTION_FIQ, or XIL_EXCEPTION_ALL.

---

void **Xil_ExceptionEnable**(void)

Enable the IRQ exception.

These macros must be called after initializing the vector table with function Xil_exceptionInit and registering exception handlers with function Xil_ExceptionRegisterHandler.

void **Xil_ExceptionDisableMask**(Mask)

Disable exceptions specified by Mask. The parameter Mask is a bitmask for exceptions to be disabled. The Mask parameter can have the values XIL_EXCEPTION_IRQ, XIL_EXCEPTION_FIQ, or XIL_EXCEPTION_ALL.

---

void **Xil_ExceptionDisable**(void)

Disable the IRQ exception.

Cortex A9 Processor and pl310 Errata Support

Various ARM errata are handled in the standalone BSP. The implementation for errata handling follows ARM guidelines and is based on the open source Linux support for these errata. The errata conditions handled in the standalone BSP are listed below.

- ARM erratum number 742230 (DMB operation may be faulty)
- ARM erratum number 743622 (Faulty hazard checking in the Store Buffer may lead to data corruption)
- ARM erratum number 775420 (A data cache maintenance operation which aborts, might lead to deadlock)
- ARM erratum number 794073 (Speculative instruction fetches with MMU disabled might not comply with architectural requirements)
- ARM erratum number 588369 (Clean & Invalidate maintenance operations do not invalidate clean lines)
- ARM PL310 erratum number 727915 (Background Clean and Invalidate by Way operation can cause data corruption)
- ARM PL310 erratum number 753970 (Cache sync operation may be faulty)

For further information on these errata items, please refer to the appropriate ARM documentation at ARM the information center.

The BSP file `xil_errata.h` defines macros for these errata. The handling of the errata are enabled by default. To disable handling of all the errata globally, un-define the macro `ENABLE_ARM_ERRATA` in `xil_errata.h`. To disable errata on a per-erratum basis, un-define relevant macros in `xil_errata.h`.

Cortex A9 Processor File Support

The following links take you directly to the `gcc` file support function.

int read(int fd, char *buf, int nbytes)
int write(int fd, char *buf, int nbytes)
int isatty(int fd)
int fcntl (int fd, int cmd, long arg)

File support is limited to the `stdin` and `stdout` streams. Consequently, the following functions are *not* necessary:

gcc

- `open( ) (in gcc/open.c)`
- `close( ) (in gcc/close.c)`
- `fstat( ) (in gcc/fstat.c)`
- `unlink( ) (in gcc/unlink.c)`
- `lseek( ) (in gcc/lseek.c)`

These files are included for completeness and because they are referenced by the C library.

Cortex A9 gcc File Support Function Descriptions

`int read(int fd, char *buf, int nbytes)`

The read( ) function in gcc/read.c reads nbytes bytes from the standard input by calling inbyte( ). It blocks until all characters are available, or the end of line character is read. The read( ) function returns the number of characters read. The fd parameter is ignored.

`int write(int fd, char *buf, int nbytes)`

Writes nbytes bytes to the standard output by calling outbyte( ). It blocks until all characters have been written. The write( ) function returns the number of characters written. The fd parameter is ignored.

`int isatty(int fd)`

Reports if a file is connected to a tty. This function always returns 1, because only the stdin and stdout streams are supported.

`int fcntl (int fd, int cmd, long arg)`

A dummy implementation of fcntl, which always returns 0. fcntl is intended to manipulate file descriptors according to the command specified by cmd. Because Standalone does not provide a file system, this function is not used.

Cortex A9 gcc Errno Function

`int errno( )`

Returns the global value of errno as set by the last C library call.

Cortex A9 gcc Memory Management

`char *sbrk(int nbytes)`

Allocates nbytes of heap and returns a pointer to that piece of memory. This function is called from the memory allocation functions of the C library.

Cortex A9 gcc Process Functions

The functions getpid( ) in getpid.c and kill( ) in kill.c are included for completeness and because they are referenced by the C library.

Cortex A9 Processor-Specific Include Files

The xreg_cortexa9.h include file contains the register numbers and the register bits for the ARM Cortex-A9 processor.

The xpseudo_asm.h include file contains the definitions for the most often used inline assembler instructions, available as macros. These can be very useful for tasks such as setting or getting special purpose registers, synchronization, or cache manipulation. These inline assembler instructions can be used from drivers and user applications written in C.

Cortex A9 Time Functions

The xtime_l.c file and corresponding xtime_l.h include file provide access to the 64-bit Global Counter in the PMU. This counter increases by one at every 2 processor cycles. The sleep.c file and corresponding sleep.h include file implement sleep functions. Sleep functions are implemented as busy loops.

Cortex A9 Time Function Summary

The time functions are summarized below. Click on the function name to go to the description.

typedef unsigned long long XTime
void XTime_SetTime(XTime xtime)
void XTime_GetTime(XTime *xtime)
unsigned int usleep(unsigned int useconds)
unsigned int sleep(unsigned int _seconds)

Cortex A9 Time Function Descriptions

`typedef unsigned long long XTime`

The XTime type in xtime_l.h is a 64-bit value, which represents the Global Counter.

`void` **`XTime_SetTime`**`(XTime xtime)`

Sets the global timer to the value in xtime.

`void` **`XTime_GetTime`**`(XTime *xtime)`

Writes the current value of the Global Timer to variable xtime.

`unsigned int` **`usleep`**`(unsigned int useconds)`

Delays the execution of a program by useconds microseconds. It returns zero if the delay can be achieved or -1 if the delay can't be achieved. This function requires that the processor frequency (in Hz) is defined in xparameters.h.

`unsigned int` **`sleep`**`(unsigned int _seconds)`

Delays the execution of a program by what is specified in seconds. It always returns zero. This function requires that the processor frequency (in Hz) is defined in xparameters.h.

Cortex A9 Event Counters

`xpm_counter.c` and `xpm_counter.h` provide APIs for configuring and controlling the Cortex-A9

Performance Monitor Events. Cortex-A9 Performance Monitor has 6 event counters which can be used to count a variety of events described in Cortex-A9 TRM.

`xpm_counter.h` defines configurations (XPM_CNTRCFGx) which specifies the event counters to count a set of events.

Cortex A9 Event Counters Function Summary

The Event Counters functions are summarized below. Click on the function name to go to the description.

void Xpm_SetEvents(int PmcrCfg)

void Xpm_GetEventCounters(u32 *PmCtrValue)

Cortex A9 Event Counters Function Description

`void` **`Xpm_SetEvents`**`(int PmcrCfg)`

This function configures the Cortex A9 event counters controller, with the event codes, in a configuration selected by the user and enables the counters.

PmcrCfg is configuration value based on which the event counters are configured.

Use XPM_CNTRCFG* values defined in xpm_counter.h to define a configuration which specify the event counters to count a set of events.

`void` **`Xpm_GetEventCounters`**`(u32 *PmCtrValue)`

This function disables the event counters and returns the counter values.

PmCtrValue returns the counter values.

Cortex R5 Processor API

Standalone BSP contains boot code, cache, exception handling, file and memory management, configuration, time and processor-specific include functions. It supports gcc compiler. The following lists the Cortex R5 Processor API sections. You can click on a link to go directly to the function section.

- Cortex R5 Processor Boot Code
- Cortex R5 Processor Cache Functions
- Cortex R5 Processor MPU Handling
- Cortex R5 Processor Exception Handling
- Cortex R5 gcc File Support
- Cortex R5 gcc Errno Functions
- Cortex R5 gcc Memory Management
- Cortex R5 gcc Process Functions
- Cortex R5 Processor-Specific Include Files
- Cortex R5 Time Functions

The following subsections describe the functions by type.

Cortex R5 Processor Boot Code

The boot.S file contains a minimal set of code for transferring control from the processor's reset location to the start of the application. It performs the following tasks.

- Disable branch prediction , MPU, instruction and data caches,
- Initialize stack pointer for IRQ, FIQ, supervisor, abort, undefined and system mode
- Invalidate entire instruction and data caches
- Configure memory attributes for various region using MPU
- Enable branch prediction, data cache, instruction cache and MPU

Cortex R5 Processor Cache Functions

The `xil_cache.c` file and the corresponding `xil_cache.h` header file provide access to the following cache and cache-related operations.

Cache Function Summary

The following are links to the function descriptions. Click on the name to go to that function.

- void Xil_DCacheEnable(void)
- void Xil_DCacheDisable(void)
- void Xil_DCacheInvalidate(void)
- void Xil_DCacheInvalidateLine(INTPTR adr)
- void Xil_DCacheInvalidateRange(INTPTR adr, u32 len)
- void Xil_DCacheFlush(void)
- void Xil_DCacheFlushLine(INTPTR adr)
- void Xil_DCacheFlushRange(INTPTR adr,u32 len)
- void Xil_DCacheStoreLine(INTPTR adr)
- void Xil_ICacheEnable(void)
- void Xil_ICacheDisable(void)
- void Xil_ICacheInvalidate(void)
- void Xil_ICacheInvalidateLine(INTPTR adr)
- void Xil_ICacheInvalidateRange(INTPTR adr, u32 len)

Cache Function Descriptions

`void Xil_DCacheEnable(void)`

Enable the data caches.

`void Xil_DCacheDisable(void)`

Disable the data caches.

`void Xil_DCacheInvalidate(void)`

Invalidate the entire data cache.

void Xil_DCacheInvalidateLine(INTPTR adr)

Invalidate a data cache line. If the byte specified by adr is cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the modified contents are lost and are not written to system memory before the line is invalidated. A subsequent data access to this address results in a cache miss and a cache line refill.

void Xil_DCacheInvalidateRange(INTPTR adr, u32 len)

Invalidates the data cache lines that are described by the address range starting from adr and len bytes long. A subsequent data access to any address in this range results in a cache miss and a cache line refill.

void Xil_DCacheFlush(void)

Flush the entire Data cache.

void Xil_DCacheFlushLine(INTPTR adr)

Flush a Data cache line. If the byte specified by the address (adr) is cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the entire contents of the cacheline are written to system memory before the line is invalidated. A subsequent data access to this address results in a cache miss and a cache line refill.

void Xil_DCacheFlushRange(INTPTR adr,u32 len)

Flush the data cache lines that are described by the address range starting from adr and len bytes long. A subsequent data access to any address in this range results in a cache miss and a cache line refill.

void Xil_DCacheStoreLine(INTPTR adr)

Store a Data cache line. If the byte specified by the adr is cached by the data cache and the cacheline is modified (dirty), the entire contents of the cacheline are written to system memory. After the store completes, the cacheline is marked as unmodified (not dirty).

void Xil_ICacheEnable(void)

Enable the instruction caches.

void Xil_ICacheDisable(void)

Disable the instruction caches.

void Xil_ICacheInvalidate(void)

Invalidate the entire instruction cache.

void Xil_ICacheInvalidateLine(INTPTR adr)

Invalidate an instruction cache line. If the instruction specified by the parameter adr is cached by the instruction cache, the cacheline containing that instruction is invalidated.

void Xil_ICacheInvalidateRange(INTPTR adr, u32 len)

Invalidate the instruction cache for the given address range. If the bytes specified by the adr are cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the modified contents are lost and are not written to system memory before the line is invalidated.

Cortex R5 Processor MPU Handling

The standalone BSP MPU handling API is implemented in file xil_mpu.c and the corresponding header file xil_mpu.h.

MMU Handling Function Summary

The following functions describe the available MMU handling API.

- void Xil_SetMPURegion(INTPTR addr, u64 size, u32 attrib)
- void Xil_SetTlbAttributes(INTPTR addr, u32 attrib)
- void Xil_EnableMPU(void)
- void Xil_DisableMPU(void)

MMU Handling Function Descriptions

void Xil_SetMPURegion(INTPTR addr, u64 size, u32 attrib)

This function changes the memory attributes for a section of memory with starting address given by variable addr of the region size provided by variable size and having attributes specified by variable attrib.

This API can be used to change attributes such as cache-ability and share-ability of a specified memory region, access to a particular region etc.

void Xil_SetTlbAttributes(INTPTR addr, u32 attrib)

It sets the memory attributes for a section of memory with starting address specified by variable addr of the region size 1MB with attributes given by variable attrib. This API is provided for the usage of similar type of API across other platforms/processors.

void Xil_EnableMPU(void)

Enable the MPU

void Xil_DisableMPU(void)

Disable the MPU

Cortex R5 Processor Exception Handling

The Standalone BSP provides an exception handling API. For details about the exceptions and interrupts on ARM Cortex-R5 processor, refer to "Exceptions" under the chapter "The System Level Programmers' Model" in the ARM Architecture Reference Manual ARMv7-A and ARMv-7R edition.

The exception handling API is implemented in a set of the files - asm_vectors.S, vectors.c, xil_exception.c, and the corresponding header files vectors.h and xil_exception.h.

Exception Handling Function Summary

The following are links to the function descriptions. Click on the name to go to that function.

- void Xil_ExceptionInit(void)
- void Xil_ExceptionRegisterHandler (u32 ExceptionId, Xil_ExceptionHandler Handler, void *DataPtr)
- void Xil_ExceptionRemoveHandler (u32 ExceptionId)
- void Xil_ExceptionEnableMask(Mask)
- void Xil_ExceptionEnable(void)
- void Xil_ExceptionDisableMask(Mask)
- void Xil_ExceptionDisable(void)

Exception Handling Function Descriptions

```
void Xil_ExceptionInit(void)
```

Sets up the interrupt vector table and registers a "do nothing" function for each exception. This function has no parameters and does not return a value. This function must be called before registering any exception handlers or enabling any interrupts.

```
void Xil_ExceptionRegisterHandler (u32 ExceptionId,
   Xil_ExceptionHandler Handler, void *DataPtr)
```

Registers an exception handler for a specific exception; does not return a value. Refer to Table the for a list of exception types and their values.

The parameters are:

- **ExceptionId** is of parameter type u8, and is the exception to which this handler should be registered. The type and the values are defined in the xil_exception.h header file. Refer Table 5 for more details.
- **Handler** is an Xil_ExceptionHandler parameter that is the pointer to the exception handling function. The function provided as the Handler parameter must have the following function prototype:

  ```
  typedef void (*Xil_ExceptionHandler)(void * DataPtr);
  ```

  This prototype is declared in the xil_exception.h header file.
- **DataPtr** is of parameter type void * and is the user value to be passed when the Handler is called. When this Handler function is called, the parameter DataPtr contains the same value provided, when the Handler was registered.

Table 5: Registered Exception Types and Values

Exception Type	Value
XIL_EXCEPTION_ID_RESET	0
XIL_EXCEPTION_ID_UNDEFINED_INT	1
XIL_EXCEPTION_ID_SWI_INT	2
XIL_EXCEPTION_ID_PREFETCH_ABORT_INT	3
XIL_EXCEPTION_ID_DATA_ABORT_INT	4
XIL_EXCEPTION_ID_IRQ_INT	5
XIL_EXCEPTION_ID_FIQ_INT	6

`void Xil_ExceptionRemoveHandler (u32 ExceptionId)`

De-register a handler function for a given exception. For possible values of parameter ExceptionId, refer above the table

---

`void Xil_ExceptionEnableMask(Mask)`

Enable exceptions specified by Mask. The parameter Mask is a bitmask for exceptions to be enabled. The Mask parameter can have the values XIL_EXCEPTION_IRQ, XIL_EXCEPTION_FIQ, or XIL_EXCEPTION_ALL.

`void Xil_ExceptionEnable(void)`

Enable the IRQ exception.

These macros must be called after initializing the vector table with function Xil_exceptionInit and registering exception handlers with function Xil_ExceptionRegisterHandler

---

`void Xil_ExceptionDisableMask(Mask)`

Disable exceptions specified by Mask. The parameter Mask is a bitmask for exceptions to be disabled. The Mask parameter can have the values XIL_EXCEPTION_IRQ, XIL_EXCEPTION_FIQ, or XIL_EXCEPTION_ALL.

`void Xil_ExceptionDisable(void)`

Disable the IRQ exception.

Cortex R5 gcc File Support

The following links take you directly to the `gcc` file support function.

- int read(int fd, char *buf, int nbytes)
- int write(int fd, char *buf, int nbytes)
- int isatty(int fd)
- int fcntl (int fd, int cmd, long arg)

File support is limited to the `stdin` and `stdout` streams. Consequently, the following functions are *not* necessary:

gcc

- `open( ) (in gcc/open.c)`
- `close( ) (in gcc/close.c)`
- `fstat( ) (in gcc/fstat.c)`
- `unlink( ) (in gcc/unlink.c)`
- `lseek( ) (in gcc/lseek.c)`

These files are included for completeness and because they are referenced by the C library.

Cortex R5 gcc File Support Function Descriptions

```
int read(int fd, char *buf, int nbytes)
```

The read( ) function in gcc/read.c reads nbytes bytes from the standard input by calling inbyte( ). It blocks until all characters are available, or the end of line character is read. The read( ) function returns the number of characters read. The fd parameter is ignored.

```
int write(int fd, char *buf, int nbytes)
```

Writes nbytes bytes to the standard output by calling outbyte( ). It blocks until all characters have been written. The write( ) function returns the number of characters written. The fd parameter is ignored.

```
int isatty(int fd)
```

Reports if a file is connected to a tty. This function always returns 1, because only the stdin and stdout streams are supported.

```
int fcntl (int fd, int cmd, long arg)
```

A dummy implementation of fcntl, which always returns 0. fcntl is intended to manipulate file descriptors according to the command specified by cmd. Because Standalone does not provide a file system, this function is not used.

Cortex R5 gcc Errno Functions

```
int errno( )
```

Returns the global value of errno as set by the last C library call.

Cortex R5 gcc Memory Management

```
char *sbrk(int nbytes)
```

Allocates nbytes of heap and returns a pointer to that piece of memory. This function is called from the memory allocation functions of the C library.

Cortex R5 gcc Process Functions

The functions getpid( ) in getpid.c and kill( ) in kill.c are included for completeness and because they are referenced by the C library.

Cortex R5 Processor-Specific Include Files

The xreg_cortexr5.h include file contains the register numbers and the register bits for the ARM Cortex-R5 processor.

The xpseudo_asm.h include file contains the definitions for the most often used inline assembler instructions, available as macros. These can be very useful for tasks such as setting or getting special purpose registers, synchronization, or cache manipulation. These inline assembler instructions can be used from drivers and user applications written in C.

Cortex R5 Time Functions

The xtime_l.c file and corresponding xtime_l.h include file provide access to the 32-bit counter in TTC. The sleep.c & usleep.c file and corresponding sleep.h include file implement sleep functions. Sleep functions are implemented as busy loops.

Cortex R5 Time Function Summary

The time functions are summarized below. Click on the function name to go to the description.

- Typedef u32 XTime
- void XTime_StartTimer(void)
- void XTime_SetTime(XTime xtime)
- void XTime_GetTime(XTime *xtime)
- unsigned int usleep(unsigned int useconds)
- unsigned int sleep(unsigned int _seconds)

Cortex R5 Time Function Descriptions

`Typedef u32 XTime`

The XTime type in xtime_l.h is a 32-bit value, which represents the TTC counter value.

`void XTime_StartTimer(void)`

Starts the TTC timer 3 counter 0 if present and if it is not already running with desired parameters for sleep functionalities.

`void XTime_SetTime(XTime xtime)`

The function does not contain anything, as the TTC counter value can not be set. This function is retained to maintain uniformity across platform.

`void XTime_GetTime(XTime *xtime)`

Writes the current value of the TTC counter to variable xtime.

`unsigned int usleep(unsigned int useconds)`

Delays the execution of a program by useconds microseconds. The counts per microseconds are defined in the `xtime_l.h` file.

The **`usleep`** API is implemented using TTC3 counter 0 if present. When TTC3 is absent, **`usleep`** is implemented using set of assembly instructions which is tested with instruction and data caches enabled and is known to provide proper delay. It may give more delay than

expected when caches are disabled. If interrupt comes when **usleep** using assembly instruction is being executed, the delay may be greater than what is expected since once the interrupt is served count resumes from where it was interrupted.

`unsigned int sleep(unsigned int _seconds)`

Delays the execution of a program by what is specified in seconds. The counts per seconds are defined in the `xtime_l.h` file.

The **sleep** API is implemented using TTC3 counter 0 if present. When TTC3 is absent, **sleep** is implemented using set of assembly instructions which is tested with instruction and data caches enabled and is known to provide proper delay. It may give more delay than expected when caches are disabled. If interrupt comes when sleep using assembly instruction is being executed, the delay may be greater than what is expected since once the interrupt is served count resumes from where it was interrupted.

Cortex A53 Processor API

Cortex-A53 standalone BSP contains two separate BSPs for 32bit mode and 64bit mode. The 32bit mode of cortex-A53 is compatible with ARMv7-A architecture whereas 64bit mode of cortex-A53 contains ARMv8-A architecture.

Standalone BSP contains boot code, cache, exception handling, file and memory management, configuration, time and processor-specific include functions. It supports gcc compiler. The following Cortex A53 Processor API subsections describe the functions by type.

- Cortex A53 Processor Boot Code
- Cortex A53 Processor Cache Functions
- Cortex A53 Processor MMU Handling
- Cortex A53 Processor Exception Handling
- Cortex A53 gcc File Support
- Cortex A53 gcc Errno Function
- Cortex A53 gcc Memory Management
- Cortex A53 gcc Process Functions
- Cortex A53 Processor-Specific Include Files
- Cortex A53 Time Functions

Cortex A53 Processor Boot Code

The `boot.S` file contains a minimal set of code for transferring control from the processor's reset location to the start of the application. It performs the following tasks.

- Disable branch prediction, MMU, instruction and data caches
- Initialize stack pointer (for current exception level for 64bit mode and for IRQ, FIQ, supervisor, abort, undefined and system mode for 32bit mode)
- Invalidate TLBs, entire instruction and data caches
- Program MMU
- Enable branch prediction, data cache, instruction cache and MPU

Cortex A53 Processor Cache Functions

The `xil_cache.c` file and the corresponding `xil_cache.h` header file provide access to the following cache and cache-related operations.

Cache Function Summary

The following are links to the function descriptions. Click on the name to go to that function.

- void Xil_DCacheEnable(void)
- void Xil_ DCacheDisable(void)
- void Xil_DCacheInvalidate(void)
- void Xil_DCacheInvalidateLine(INTPTR adr)
- void Xil_DCacheInvalidateRange(INTPTR adr, INTPTR len)
- void Xil_DCacheFlush(void)
- void Xil_DCacheFlushLine(INTPTR adr)
- void Xil_DCacheFlushRange(INTPTR adr, INTPTR len)
- void Xil_ICacheEnable(void)
- void Xil_ICacheDisable(void)
- void Xil_ICacheInvalidate(void)
- void Xil_ICacheInvalidateLine(INTPTR adr)
- void Xil_ICacheInvalidateRange(INTPTR adr, INTPTR len)

Cache Function Descriptions

`void Xil_DCacheEnable(void)`

Enable the data caches.

`void Xil_ DCacheDisable(void)`

Disable the data caches.

`void Xil_DCacheInvalidate(void)`

Clean and invalidate the entire data cache. ARMv8 architectures do not support simply invalidating the cachelines which are present in caches. In case of an environment which supports visualization like Cortex-A53, if simple invalidation functionalities are present, it may lead to loss of essential data in some scenarios. For example, If one OS invalidates a line belonging to another OS, it may crash the other OS due to the loss of essential data. Hence, such operations are prompted to clean and invalidate which avoids data corruption.

`void Xil_DCacheInvalidateLine(INTPTR adr)`

Clean and invalidate a data cache line. ARMv8 architectures does not support simply invalidating the cachelines which are present in caches. In case of an environment which supports visualization like Cortex-A53, if simple invalidation functionalities are present, it may lead to loss of essential data in some scenarios. For example, If one OS invalidates a line belonging to another OS, it may crash the other OS due to the loss of essential data. Hence, such operations are prompted to clean and invalidate which avoids such corruption.

`void Xil_DCacheInvalidateRange(INTPTR adr, INTPTR len)`

Clean and invalidate the data cache lines that are described by the address range starting from adr and len bytes long. ARMv8 architectures does not support simply invalidating the cachelines which are present in caches. In case of an environment which supports visualization

like Cortex-A53, if simple invalidation functionalities are present, it may lead to loss of essential data in some scenarios. For example, If one OS invalidates a line belonging to another OS, it may crash the other OS due to the loss of essential data. Hence, such operations are prompted to clean and invalidate which avoids such corruption.

`void Xil_DCacheFlush(void)`

Flush the entire Data cache.

`void Xil_DCacheFlushLine(INTPTR adr)`

Flush a Data cache line. If the byte specified by the address (adr) is cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the entire contents of the cacheline are written to system memory before the line is invalidated. A subsequent data access to this address results in a cache miss and a cache line refill.

`void Xil_DCacheFlushRange(INTPTR adr, INTPTR len)`

Flush the data cache lines that are described by the address range starting from adr and len bytes long. A subsequent data access to any address in this range results in a cache miss and a cache line refill.

`void Xil_ICacheEnable(void)`

Enable the instruction caches.

`void Xil_ICacheDisable(void)`

Disable the instruction caches.

`void Xil_ICacheInvalidate(void)`

Invalidate the entire instruction cache.

`void Xil_ICacheInvalidateLine(INTPTR adr)`

Invalidate an instruction cache line. If the instruction specified by the parameter adr is cached by the instruction cache, the cacheline containing that instruction is invalidated.

`void Xil_ICacheInvalidateRange(INTPTR adr, INTPTR len)`

Invalidate the instruction cache for the given address range. If the bytes specified by the adr are cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the modified contents are lost and are not written to system memory before the line is invalidated.

Cortex A53 Processor MMU Handling

The standalone BSP MMU handling API is implemented in file `xil_mmu.c` and the corresponding header file `xil_mmu.h`.

MMU Handling Function Summary

The following functions describe the available MMU handling API.

```
void Xil_SetTlbAttributes(INTPTR addr, INTPTR attrib)
```

For 64 bit mode it sets the memory attributes for a section of memory with starting address specified by variable addr of the region size 2MB (if the address is less than 4GB) or 1 GB (if the address is beyond 4GB) with attributes given by variable attrib whereas for 32bit mode it sets the memory attributes for a section of memory with starting address specified by variable addr of the region size 1MB with attributes given by variable attrib. This API can be used to change attributes such as cache-ability and share-ability of a specified memory region, access to a particular region.

Cortex A53 Processor Exception Handling

The Standalone BSP provides an exception handling API. The exception handling API is implemented in a set of the files - asm_vectors.S, vectors.c, xil_exception.c, and the corresponding header files vectors.h and xil_exception.h.

Exception Handling Function Summary

The following are links to the function descriptions. Click on the name to go to that function.

- void Xil_ExceptionInit(void)
- void Xil_ExceptionRegisterHandler (u32 ExceptionId, Xil_ExceptionHandler Handler, void *DataPtr)
- void Xil_ExceptionRemoveHandler (u32 ExceptionId)
- void Xil_ExceptionEnableMask(Mask)
- void Xil_ExceptionEnable(void)
- void Xil_ExceptionDisableMask(Mask)
- void Xil_ExceptionDisable(void)

Exception Handling Function Descriptions

```
void Xil_ExceptionInit(void)
```

Sets up the interrupt vector table and registers a "do nothing" function for each exception. This function has no parameters and does not return a value. This function must be called before registering any exception handlers or enabling any interrupts.

```
void Xil_ExceptionRegisterHandler (u32 ExceptionId,
   Xil_ExceptionHandler Handler, void *DataPtr)
```

Registers an exception handler for a specific exception; does not return a value. Refer to Table for a list of exception types and their values (for 64bit and 32bit mode).

The parameters are:

- **ExceptionId** is of parameter type u8, and is the exception to which this handler should be registered. The type and the values are defined in the `xil_exception.h` header file. Refer Table 6 and Table 7 for more details.
- **Handler** is an `Xil_ExceptionHandler` parameter that is the pointer to the exception handling function. The function provided as the Handler parameter must have the following function prototype:

```
typedef void (*Xil_ExceptionHandler)(void * DataPtr);
```

This prototype is declared in the `xil_exception.h` header file.

- **DataPtr** is of parameter type **`void *`** and is the user value to be passed when the Handler is called. When this Handler function is called, the parameter **`DataPtr`** contains the same value provided, when the Handler was registered.

Table 6: Registered Exception Types and Values for 64bit Mode

Exception Type	Value
`#define XIL_EXCEPTION_ID_SYNC_INT`	1
`#define XIL_EXCEPTION_ID_IRQ_INT`	2
`#define XIL_EXCEPTION_ID_FIQ_INT`	3
`#define XIL_EXCEPTION_ID_SERROR_ABORT_INT`	4

Table 7: Registered Exception Types and Values for 32bit Mode

Exception Type	Value
`XIL_EXCEPTION_ID_RESET`	0
`XIL_EXCEPTION_ID_UNDEFINED_INT`	1
`XIL_EXCEPTION_ID_SWI_INT`	2
`XIL_EXCEPTION_ID_PREFETCH_ABORT_INT`	3
`XIL_EXCEPTION_ID_DATA_ABORT_INT`	4
`XIL_EXCEPTION_ID_IRQ_INT`	5
`XIL_EXCEPTION_ID_FIQ_INT`	6

`void Xil_ExceptionRemoveHandler (u32 ExceptionId)`

De-register a handler function for a given exception. For possible values of parameter ExceptionId, refer above the table

---

`void Xil_ExceptionEnableMask(Mask)`

Enable exceptions specified by Mask. The parameter Mask is a bitmask for exceptions to be enabled. The Mask parameter can have the values XIL_EXCEPTION_IRQ, XIL_EXCEPTION_FIQ, or XIL_EXCEPTION_ALL.

`void Xil_ExceptionEnable(void)`

Enable the IRQ exception.

These macros must be called after initializing the vector table with function Xil_exceptionInit and registering exception handlers with function Xil_ExceptionRegisterHandler

---

`void Xil_ExceptionDisableMask(Mask)`

Disable exceptions specified by Mask. The parameter Mask is a bitmask for exceptions to be disabled. The Mask parameter can have the values XIL_EXCEPTION_IRQ, XIL_EXCEPTION_FIQ, or XIL_EXCEPTION_ALL.

void Xil_ExceptionDisable(void)

Disable the IRQ exception.

Cortex A53 gcc File Support

The following links take you directly to the gcc file support function.

- int read(int fd, char *buf, int nbytes)
- int write(int fd, char *buf, int nbytes)
- int isatty(int fd)
- int fcntl (int fd, int cmd, long arg)

File support is limited to the stdin and stdout streams. Consequently, the following functions are *not* necessary:

gcc

- open( ) (in gcc/open.c)
- close( ) (in gcc/close.c)
- fstat( ) (in gcc/fstat.c)
- unlink( ) (in gcc/unlink.c)
- lseek( ) (in gcc/lseek.c)

These files are included for completeness and because they are referenced by the C library.

Cortex A53 gcc File Support Function Descriptions

int read(int fd, char *buf, int nbytes)

The read( ) function in gcc/read.c reads nbytes bytes from the standard input by calling inbyte( ). It blocks until all characters are available, or the end of line character is read. The read( ) function returns the number of characters read. The fd parameter is ignored.

int write(int fd, char *buf, int nbytes)

Writes nbytes bytes to the standard output by calling outbyte( ). It blocks until all characters have been written. The write( ) function returns the number of characters written. The fd parameter is ignored.

int isatty(int fd)

Reports if a file is connected to a tty. This function always returns 1, because only the stdin and stdout streams are supported.

int fcntl (int fd, int cmd, long arg)

A dummy implementation of fcntl, which always returns 0. fcntl is intended to manipulate file descriptors according to the command specified by cmd. Because Standalone does not provide a file system, this function is not used.

Cortex A53 gcc Errno Function

`int errno( )`

Returns the global value of errno as set by the last C library call.

Cortex A53 gcc Memory Management

`char *sbrk(int nbytes)`

Allocates nbytes of heap and returns a pointer to that piece of memory. This function is called from the memory allocation functions of the C library.

Cortex A53 gcc Process Functions

The functions **`getpid( )`** in `getpid.c` and **`kill( )`** in `kill.c` are included for completeness and because they are referenced by the C library. The function **`initialise_monitor_handles()`** in `initialise_monitor_handles.c` is included for completeness and because they are referenced by the C library for 64bit mode.

Cortex A53 Processor-Specific Include Files

The `xreg_cortexa53.h` include file contains the register numbers and the register bits for the ARM Cortex-A53 processor.

The `xpseudo_asm.h` include file contains the definitions for the most often used inline assembler instructions, available as macros. These can be very useful for tasks such as setting or getting special purpose registers, synchronization, or cache manipulation. These inline assembler instructions can be used from drivers and user applications written in C.

Cortex A53 Time Functions

The `xtime_l.c` file and corresponding `xtime_l.h` include file provide access to the 64-bit generic counter in Cortex-A53. The `sleep.c` & `usleep.c` file and corresponding `sleep.h` include file implement sleep functions. Sleep functions are implemented as busy loops.

Cortex A53 Time Function Summary

The time functions are summarized below.

- typedef u64 XTime
- void XTime_StartTimer(void)
- void XTime_SetTime(XTime xtime)
- void XTime_GetTime(XTime *xtime)
- unsigned int usleep(unsigned int useconds)
- unsigned int sleep(unsigned int _seconds)

Cortex A53 Time Function Descriptions

`typedef u64 XTime`

The XTime type in `xtime_l.h` is a 64-bit value, which represents the Generic counter value.

`void XTime_StartTimer(void)`

Starts the global timer counter.

`void XTime_SetTime(XTime xtime)`

The function does not contain anything, as the generic counter in A53 runs constantly and it does not display actual time. This function is kept for the uniformity across platform.

`void XTime_GetTime(XTime *xtime)`

Writes the current value of the generic counter to variable xtime.

`unsigned int usleep(unsigned int useconds)`

Delays the execution of a program by useconds microseconds. The counts per microseconds are defined in the usleep.c file.

`unsigned int sleep(unsigned int _seconds)`

Delays the execution of a program by what is specified in seconds. The counts per seconds are defined in the xtime_l.h file.

Xilinx Hardware Abstraction Layer

The following sections describe the Xilinx® Hardware Abstraction Layer API. It contains the following sections:

- Types (xil_types)
- Register IO (xil_io)
- Exception (xil_exception)
- Cache (xil_cache)
- Assert (xil_assert)
- Extra Header File
- Test Memory (xil_testmem)
- Test Register IO (xil_testio)
- Test Cache (xil_testcache)
- Hardware Abstraction Layer Migration Tips

Types (xil_types)

Header File

```
#include "xil_types.h"
```

Typedef

```
typedef unsigned char u8
typedef unsigned short u16
typedef unsigned long u32
typedef unsigned long long u64
typedef char s8
typedef short s16
typedef long s32
```

```
typedef long long s64
```

Macros

Macro	Value
#define TRUE	1
#define FALSE	0
#define NULL	0
#define XIL_COMPONENT_IS_READY	0x11111111
#define XIL_COMPONENT_IS_STARTED	0x22222222

Register IO (xil_io)

Header File

```
#include "xil_io.h"
```

Common API

The following is a linked summary of register IO functions. They can run on MicroBlaze and Cortex A9 processors.

u8 Xil_In8(u32 Addr)
u16 Xil_EndianSwap16 (u16 Data)
u16 Xil_Htons(u16 Data)
u16 Xil_In16(u32 Addr)
u16 Xil_In16BE(u32 Addr)
u16 Xil_In16LE(u32 Addr)
u16 Xil_Ntohs(u16 Data)
u32 Xil_EndianSwap32 u32 Data)
u32 Xil_Htonl(u32 Data)
u32 Xil_In32(u32 Addr)
u32 Xil_In32BE(u32 Addr)
u32 Xil_In32LE(u32 Addr)
u32 Xil_Ntohs(u32 Data)
void Xil_Out8(u32 Addr, u8 Value)
void Xil_Out16(u32 Addr, u16 Value)
void Xil_Out16BE(u32 Addr, u16 Value)
void Xil_Out16LE(u32 Addr, u16 Value)
void Xil_Out32(u32 Addr, u32 Value)
void Xil_Out32BE(u32 Addr, u32 Value)
void Xil_Out32LE(u32 Addr, u32 Value)

---

u8 **Xil_In8**(u32 Addr)

Perform an input operation for an 8-bit memory location by reading from the specified address and returning the value read from that address.

Parameters:

`Addr` contains the address at which to perform the input operation.

Returns:

The value read from the specified input address.

u16 **Xil_EndianSwap16** (u16 Data)

Perform a 16-bit endian swapping.

Parameters:

Data contains the value to be swapped.

Returns:

Endian swapped value.

u16 **Xil_Htons**(u16 Data)

Convert a 16-bit number from host byte order to network byte order.

Parameters:

Data the 16-bit number to be converted.

Returns:

The converted 16-bit number in network byte order.

u16 **Xil_In16**(u32 Addr)

Perform an input operation for a 16-bit memory location by reading from the specified address and returning the value read from that address.

Parameters:

Addr contains the address at which to perform the input operation.

Returns:

The value read from the specified input address.

u16 **Xil_In16BE**(u32 Addr)

Perform an big-endian input operation for a 16-bit memory location by reading from the specified address and returning the value read from that address.

Parameters:

Addr contains the address at which to perform the input operation.

Returns:

The value read from the specified input address with the proper endianness. The return value has the same endianness as that of the processor. For example, if the processor is little-endian, the return value is the byte-swapped value read from the address.

u16 **Xil_In16LE**(u32 Addr)

Perform a little-endian input operation for a 16-bit memory location by reading from the specified address and returning the value read from that address.

Parameters:

Addr contains the address at which to perform the input operation.

Returns:

The value read from the specified input address with the proper endianness. The return value has the same endianness as that of the processor. For example, if the processor is big-endian, the return value is the byte-swapped value read from the address.

---

u16 **Xil_Ntohs**(u16 Data)

Convert a 16-bit number from network byte order to host byte order.

Parameters:

Data the 16-bit number to be converted.

Returns:

The converted 16-bit number in host byte order.

---

u32 **Xil_EndianSwap32** (u32 Data)

Perform a 32-bit endian swapping.

Parameters:

Data contains the value to be swapped.

Returns:

Endian swapped value.

---

u32 **Xil_Htonl**(u32 Data)

Convert a 32-bit number from host byte order to network byte order.

Parameters:

Data the 32-bit number to be converted.

Returns:

The converted 32-bit number in network byte order.

---

u32 **Xil_In32**(u32 Addr)

Perform an input operation for a 32-bit memory location by reading from the specified address and returning the value read from that address.

Parameters:

Addr contains the address at which to perform the input operation.

Returns:

The value read from the specified input address.

u32 **Xil_In32BE**(u32 Addr)

Perform a big-endian input operation for a 32-bit memory location by reading from the specified address and returning the value read from that address.

Parameters:

`Addr` contains the address at which to perform the input operation.

Returns:

The value read from the specified input address with the proper endianness. The return value has the same endianness as that of the processor. For example, if the processor is little-endian, the return value is the byte-swapped value read from the address.

u32 **Xil_In32LE**(u32 Addr)

Perform a little-endian input operation for a 32-bit memory location by reading from the specified address and returning the value read from that address.

Parameters:

`Addr` contains the address at which to perform the input operation.

Returns:

The value read from the specified input address with the proper endianness. The return value has the same endianness as that of the processor. For example, if the processor is big-endian, the return value is the byte-swapped value read from the address.

u32 **Xil_Ntohs**(u32 Data)

Convert a 32-bit number from network byte order to host byte order.

Parameters:

Data the 32-bit number to be converted.

Returns:

The converted 32-bit number in host byte order.

void **Xil_Out8**(u32 Addr, u8 Value)

Perform an output operation for an 8-bit memory location by writing the specified value to the specified address.

Parameters:

`Addr` contains the address at which to perform the output operation.

`Value` contains the value to be output at the specified address.

void **Xil_Out16**(u32 Addr, u16 Value)

Perform an output operation for a 16-bit memory location by writing the specified value to the specified address.

Parameters:

`Addr` contains the address at which to perform the output operation.

`Value` contains the value to be output at the specified address.

`void` **`Xil_Out16BE`**`(u32 Addr, u16 Value)`

Perform a big-endian output operation for a 16-bit memory location by writing the specified value to the specified address.

Parameters:

`Addr` contains the address at which to perform the output operation.

`Value` contains the value to be output at the specified address. The value has the same endianness as that of the processor. For example, if the processor is little-endian, the byte-swapped value is written to the address.

`void` **`Xil_Out16LE`**`(u32 Addr, u16 Value)`

Perform a little-endian output operation for a 16-bit memory location by writing the specified value to the specified address.

Parameters:

`Addr` contains the address at which to perform the output operation.

`Value` contains the value to be output at the specified address. The value has the same endianness as that of the processor. For example, if the processor is big-endian, the byte-swapped value is written to the address.

`void` **`Xil_Out32`**`(u32 Addr, u32 Value)`

Perform an output operation for a 32-bit memory location by writing the specified value to the specified address.

Parameters:

`Addr` contains the address at which to perform the output operation.

`Value` contains the value to be output at the specified address.

`void` **`Xil_Out32BE`**`(u32 Addr, u32 Value)`

Perform a big-endian output operation for a 32-bit memory location by writing the specified value to the specified address.

Parameters:

`Addr` contains the address at which to perform the output operation.

`Value` contains the value to be output at the specified address. The value has the same endianness as that of the processor. For example, if the processor is little-endian, the byte-swapped value is written to the address.

`void` **`Xil_Out32LE`**`(u32 Addr, u32 Value)`

Perform a little-endian output operation for a 32-bit memory location by writing the specified value to the specified address.

Parameters:

`Addr` contains the address at which to perform the output operation.

`Value` contains the value to be output at the specified address. The value has the same endianness as that of the processor. For example, if the processor is big-endian, the byte-swapped value is written to the address.

Exception (xil_exception)

Header File

```
#include "xil_exception.h"
```

Typedef

```
typedef void(* Xil_ExceptionHandler)(void *Data)
```

This typedef is the exception handler function pointer.

Common API

The following are exception functions. They can run on MicroBlaze and Cortex A9 processors.

`void` **`Xil_ExceptionDisable`**`()`

Disable Exceptions.

`void` **`Xil_ExceptionEnable`**`()`

Enable Exceptions.

`void` **`Xil_ExceptionInit`**`()`

Initialize exception handling for the processor. The exception vector table is set up with the stub handler for all exceptions.

`void` **`Xil_ExceptionRegisterHandler`**`(u32 Id, Xil_ExceptionHandler Handler, void *Data)`

Make the connection between the ID of the exception source and the associated handler that runs when the exception is recognized. `Data` is used as the argument when the handler is called.

Parameters:

`Id` contains the identifier (ID) of the exception source. This should be `XIL_EXCEPTION_INT` or be in the range of `0` to `XIL_EXCEPTION_LAST`. Refer to the `xil_exception.h` file for further information.

`Handler` is the handler for that exception.

`Data` is a reference to data that will be passed to the handler when it is called.

`void` **`Xil_ExceptionRemoveHandler`**`(u32 Id)`

Remove the handler for a specific exception ID. The stub handler is then registered for this exception ID.

Parameters:

`Id` contains the ID of the exception source. It should be `XIL_EXCEPTION_INT` or in the range of `0` to `XIL_EXCEPTION_LAST`. Refer to the `xil_exception.h` file for further information.

Common Macro

The common macro is:

```
#define XIL_EXCEPTION_ID_INT
```

This macro is defined for all processors and used to set the exception handler that corresponds to the interrupt controller handler. The value is processor-dependent. For example:

```
Xil_ExceptionRegisterHandler(XIL_EXCEPTION_ID_INT,
(XilExceptionHandler)IntcHandler, IntcData)
```

MicroBlaze Processor-Specific Macros

Macro	Value
#define XIL_EXCEPTION_ID_FIRST	0
#define XIL_EXCEPTION_ID_FSL	0
#define XIL_EXCEPTION_ID_UNALIGNED_ACCESS	1
#define XIL_EXCEPTION_ID_ILLEGAL_OPCODE	2
#define XIL_EXCEPTION_ID_IOPB_EXCEPTION	3
#define XIL_EXCEPTION_ID_IPLB_EXCEPTION	3
#define XIL_EXCEPTION_ID_DOPB_EXCEPTION	4
#define XIL_EXCEPTION_ID_DPLB_EXCEPTION	4
#define XIL_EXCEPTION_ID_DIV_BY_ZERO	5
#define XIL_EXCEPTION_ID_FPU	6
#define XIL_EXCEPTION_ID_MMU	7
#define XIL_EXCEPTION_ID_LAST	XIL_EXCEPTION_ID_MMU

Cache (xil_cache)

Header File

```
#include "xil_cache.h"
```

Common API

The functions listed in this sub-section can be executed on all processors.

`void` **`Xil_DCacheDisable`**`()`

Disable the data cache.

`void` **`Xil_DCacheEnable`**`()`

Enable the data cache.

`void` **`Xil_DCacheFlush`**`()`

Flush the entire data cache. If any cacheline is dirty (has been modified), it is written to system memory. The entire data cache will be invalidated.

void **Xil_DCacheFlushRange**(u32 Addr, u32 Len)

Flush the data cache for the given address range. If any memory in the address range (identified as Addr) has been modified (and are dirty), the modified cache memory will be written back to system memory. The cacheline will also be invalidated.

Parameters:

Addr is the starting address of the range to be flushed.

Len is the length, in bytes, to be flushed.

void **Xil_DCacheInvalidate**()

Invalidate the entire data cache. If any cacheline is dirty (has been modified), the modified contents are lost.

void **Xil_DCacheInvalidateRange**(u32 Addr, u32 Len)

Invalidate the data cache for the given address range. If the bytes specified by the address (Addr) are cached by the data cache, the cacheline containing that byte is invalidated. If the cacheline is modified (dirty), the modified contents are lost.

Parameters:

Addr is address of range to be invalidated.

Len is the length in bytes to be invalidated.

void **Xil_ICacheDisable**()

Disable the instruction cache.

void **Xil_ICacheEnable**()

On MicroBlaze processors, enable the instruction cache.

void **Xil_ICacheInvalidate**()

Invalidate the entire instruction cache.

void **Xil_ICacheInvalidateRange**(u32 Addr, u32 Len)

Invalidate the instruction cache for the given address range.

Parameters:

Addr is address of range to be invalidated.

Len is the length in bytes to be invalidated.

Assert (xil_assert)

Header File

```
#include "xil_assert.h"
```

Typedef

```
typedef void(* Xil_AssertCallback)(char *Filename, int Line)
```

Common API

The functions listed in this sub-section can be executed on all processors.

`void` **`Xil_Assert`**`(char *File, int Line)`

Implement `assert`. Currently, it calls a user-defined callback function if one has been set. Then, potentially enters an infinite loop depending on the value of the `Xil_AssertWait` variable.

Parameters:

`File` is the name of the filename of the source.

`Line` is the line number within File.

`void` **`Xil_AssertSetCallbac`**`k(xil_AssertCallback Routine)`

Set up a callback function to be invoked when an assert occurs. If there was already a callback installed, then it is replaced.

Parameters:

`Routine` is the callback to be invoked when an assert is taken.

`#define` **`Xil_AssertVoid`**`(Expression)`

This assert macro is to be used for functions that do not return anything (void). This can be used in conjunction with the `Xil_AssertWait` boolean to accommodate tests so that asserts that fail still allow execution to continue.

Parameters:

`Expression` is the expression to evaluate. If it evaluates to false, the assert occurs.

`#define` **`Xil_AssertNonvoid`**`(Expression)`

This assert macro is to be used for functions that return a value. This can be used in conjunction with the `Xil_AssertWait` boolean to accommodate tests so that asserts that fail still allow execution to continue.

Parameters:

`Expression` is the expression to evaluate. If it evaluates to false, the assert occurs.

Returns:

Returns 0 unless the `Xil_AssertWait` variable is true, in which case no return is made and an infinite loop is entered.

#define Xil_AssertVoidAlways()

Always assert. This assert macro is to be used for functions that do not return anything (void). Use for instances where an assert should always occur.

Returns:

Returns void unless the `Xil_AssertWait` variable is true, in which case no return is made and an infinite loop is entered.

#define Xil_AssertNonvoidAlways()

Always assert. This assert macro is to be used for functions that return a value. Use for instances where an assert should always occur.

Returns:

Returns void unless the `xil_AssertWait` variable is true, in which case no return is made and an infinite loop is entered.

Extra Header File

The `xil_hal.h` header file is provided as a convenience. It includes all the header files related to the Hardware Abstraction Layer. The contents of this header file are as follows:

```
#ifndef XIL_HAL_H
#define XIL_HAL_H

#include "xil_assert.h"
#include "xil_exception.h"
#include "xil_cache.h"
#include "xil_io.h"
#include "xil_types.h"

#endif
```

Test Memory (xil_testmem)

Description

A subset of the memory tests can be selected or all of the tests can be run in order. If there is an error detected by a subtest, the test stops and the failure code is returned. Further tests are not run even if all of the tests are selected.

Subtest Descriptions

XIL_TESTMEM_ALLMEMTESTS

Runs all of the subtests.

XIL_TESTMEM_INCREMENT

Incrementing Value test.

This test starts at `XIL_TESTMEM_MEMTEST_INIT_VALUE` and uses the incrementing value as the test value for memory.

XIL_TESTMEM_WALKONES

Walking Ones test.

This test uses a walking “1“ as the test value for memory.

```
location 1 = 0x00000001
location 2 = 0x00000002
...
```

XIL_TESTMEM_WALKZEROS

Walking Zeros test.

This test uses the inverse value of the walking ones test as the test value for memory.

```
location 1 = 0xFFFFFFFE
location 2 = 0xFFFFFFFD
...
```

XIL_TESTMEM_INVERSEADDR

Inverse Address test.

This test uses the inverse of the address of the location under test as the test value for memory.

XIL_TESTMEM_FIXEDPATTERN

Fixed Pattern test.

This test uses the provided patterns as the test value for memory.

If zero is provided as the pattern, the test uses `0xDEADBEEF`.

> ***Caution!*** The tests are DESTRUCTIVE. Run them before any initialized memory spaces have been set up. The address provided to the memory tests is not checked for validity, except for the case where the value is NULL. It is possible to provide a code-space pointer for this test to start with and ultimately destroy executable code causing random failures.

Note: This test is used for spaces where the address range of the region is smaller than the data width. If the memory range is greater than 2 to the power of width, the patterns used in `XIL_TESTMEM_WALKONES` and `XIL_TESTMEM_WALKZEROS` will repeat on a boundary of a power of two, making it more difficult to detect addressing errors. The `XIL_TESTMEM_INCREMENT` and `XIL_TESTMEM_INVERSEADDR` tests suffer the same problem. If you need to test large blocks of memory, it is recommended that you break them up into smaller regions of memory to allow the test patterns used not to repeat over the region tested.

Header File

```
#include "xil_testmem.h"
```

Common API

`int` **`Xil_Testmem8`**`(u8 *Addr, u32 Words, u8 Pattern, u8 Subtest)`

Perform a destructive 8-bit wide memory test.

Parameters:

`Addr` is a pointer to the region of memory to be tested.

`Words` is the length of the block.

`Pattern` is the constant used for the constant pattern test, if 0, 0xDEADBEEF is used.

`Subtest` is the test selected. See `xil_testmem.h` for possible values.

Returns:

-1 is returned for a failure

0 is returned for a pass

Note: Used for spaces where the address range of the region is smaller than the data width. If the memory range is greater than 2 to the power of width, the patterns used in `XIL_TESTMEM_WALKONES` and `XIL_TESTMEM_WALKZEROS` repeat on a boundary of a power of two, which makes detecting addressing errors more difficult. This is true of `XIL_TESTMEM_INCREMENT` and `XIL_TESTMEM_INVERSEADDR` tests also. If you need to test large blocks of memory, it is recommended that you break them up into smaller regions of memory to allow the test patterns used not to repeat over the region tested.

`int` **`Xil_Testmem16`**`(u16 *Addr, u32 Words, u16 Pattern, u8 Subtest)`

Perform a destructive 16-bit wide memory test.

Parameters:

`Addr` is a pointer to the region of memory to be tested.

`Words` is the length of the block.

`Pattern` is the constant used for the constant pattern test, if 0, 0xDEADBEEF is used.

`Subtest` is the test selected. See `xil_testmem.h` for possible values.

Returns:

-1 is returned for a failure.

0 is returned for a pass.

Note: Used for spaces where the address range of the region is smaller than the data width. If the memory range is greater than 2 to the power of width, the patterns used in `XIL_TESTMEM_WALKONES` and `XIL_TESTMEM_WALKZEROS` repeat on a boundary of a power of two, making detecting addressing errors more difficult.

This is true of `XIL_TESTMEM_INCREMENT` and `XIL_TESTMEM_INVERSEADDR` tests also. If you need to test large blocks of memory, it is recommended that you break them up into smaller regions of memory to allow the test patterns used not to repeat over the region tested.

`int` **`Xil_Testmem32`** `(u32 *Addr, u32 Words, u32 pattern, u8 Subtest)`

Perform a destructive 32-bit wide memory test.

Parameters:

`Addr` is a pointer to the region of memory to be tested.

`Words` is the length of the block.

`Pattern` is the constant used for the constant pattern test, if 0, 0xDEADBEEF is used.

`Subtest` is the test selected. See xil_testmem.h for possible values.

Returns:

0 is returned for a pass.

-1 is returned for a failure.

Note: This test is used for spaces where the address range of the region is smaller than the data width. If the memory range is greater than 2 to the power of width, the patterns used in `XIL_TESTMEM_WALKONES` and `XIL_TESTMEM_WALKZEROS` repeat on a boundary of a power of two, making detecting addressing errors more difficult. This is true of the `XIL_TESTMEM_INCREMENT` and `XIL_TESTMEM_INVERSEADDR` tests also. If you need to test large blocks of memory, it is recommended that you break them up into smaller regions of memory to allow the test patterns used not to repeat over the region tested.

Test Register IO (xil_testio)

This file contains utility functions to teach endian-related memory I/O functions.

Header File

```
#include "xil_testio.h"
```

Common API

`int` **`Xil_TestIO8`**`(u8 *Addr, int Len, u8 Value)`

Perform a destructive 8-bit wide register IO test where the register is accessed using `Xil_Out8` and `Xil_In8`. the `Xil_TestI08` function compares the read and write values.

Parameters:

`Addr` is a pointer to the region of memory to be tested.

`Len` is the length of the block.

`Value` is the constant used for writing the memory.

Returns:

0 is returned for a pass.

-1 is returned for a failure.

int **Xil_TestIO16**(u8 *Addr, int Len, u16 Value, int Kind, int Swap)

Perform a destructive 16-bit wide register IO test. Each location is tested by sequentially writing a 16-bit wide register, reading the register, and comparing value. This function tests three kinds of register IO functions, normal register IO, little-endian register IO, and big-endian register IO. When testing little/big-endian IO, the function performs the following sequence:

Xil_Out16LE/Xil_Out16BE, Xil_In16, Compare In-Out values, Xil_Out16, Xil_In16LE/Xil_In16BE, Compare In-Out values. Whether to swap the read-in value before comparing is controlled by the 5th argument.

Parameters:

`Addr` is a pointer to the region of memory to be tested.

`Len` is the length of the block.

`Value` is the constant used for writing the memory.

`Kind` is the test kind. Acceptable values are: `XIL_TESTIO_DEFAULT`, `XIL_TESTIO_LE`, `XIL_TESTIO_BE`.

`Swap` indicates whether to byte swap the read-in value.

Returns:

0 is returned for a pass.

-1 is returned for a failure.

---

int **Xil_TestIO32**(u8 *Addr, int Len, u32 Value, int Kind, int Swap)

Perform a destructive 32-bit wide register IO test. Each location is tested by sequentially writing a 32-bit wide register, reading the register, and comparing value. This function tests three kinds of register IO functions, normal register IO, little-endian register IO, and big-endian register IO. When testing little/big-endian IO, the function performs the following sequence: Xil_Out32LE/Xil_Out32BE, Xil_In32, Compare In-Out values, Xil_Out32, Xil_In32LE/Xil_In32BE, Compare In-Out values. Whether to swap the read-in value before comparing is controlled by the 5th argument.

Parameters:

`Addr` is a pointer to the region of memory to be tested.

`Len` is the length of the block.

`Value` is the constant used for writing the memory.

`Kind` is the test kind. Acceptable values are: `XIL_TESTIO_DEFAULT`, `XIL_TESTIO_LE`, `XIL_TESTIO_BE`.

`Swap` indicates whether to byte swap the read-in value.

Returns:

0 is returned for a pass.

-1 is returned for a failure.

Test Cache (xil_testcache)

This file contains utility functions to test the cache.

Header File

```
#include "xil_testcache.h"
```

Common API

---

int Xil_TestDCacheAll()

Tests the DCache related functions on all related API tests such as `Xil_DCacheFlush` and `Xil_DCacheInvalidate`. This test function writes a constant value to the data array, flushes the DCache, writes a new value, and then invalidates the DCache.

Returns:

0 is returned for a pass.

-1 is returned for a failure.

---

int Xil_TestDCacheRange()

Tests the DCache range-related functions on a range of related API tests such as `Xil_DCacheFlushRange` and `Xil_DCacheInvalidate_range`. This test function writes a constant value to the data array, flushes the range, writes a new value, and then invalidates the corresponding range.

Returns:

0 is returned for a pass.

-1 is returned for a failure.

---

int Xil_TestICacheAll()

Perform `xil_icache_invalidate()`.

Returns:

0 is returned for a pass. The function will hang if it fails.

---

int Xil_TestICacheRange()

Perform `Xil_ICacheInvalidateRange()` on a few function pointers.

Returns:

0 is returned for a pass. The function will hang if it fails.

Hardware Abstraction Layer Migration Tips

Mapping Header Files to HAL Header Files

You should map the old header files to the new HAL header files as listed in Table 8.

Table 8: **HAL Header File Mapping**

Area	Old Header File	New Header File
Register IO	“xio.h“	“xil_io.h”
Exception	“xexception_l.h” “mb_interface.h”	“xil_exception.h”
Cache	“xcache.h” “mb_interface.h”	“xil_cache.h”
Interrupt	“xexception_l.h” “mb_interface.h”	“xil_exception.h”
Typedef u8 u16 u32	“xbasic_types.h”	“xil_types.h”
Typedef of Xuint32 Xfloat32 ...	“xbasic_types.h”	Deprecated. Do not use.
Assert	“xbasic_types.h”	“xil_assert.h”
Test Memory	“xutil.h”	“xil_testmem.h”
Test Register IO	None	“xil_testio.h”
Test Cache	None	“xil_testcache.h”
XTRUE, XFALSE, XNULL definitions	“xbasic_types.h”	Deprecated. Use TRUE, FALSE, NULL defined in xil_types.h

Mapping Functions to HAL Functions

You should map old functions to the new HAL functions as follows.

Table 9: **I/O Function Mapping**

Old xio	New xil_io
#include “xio.h”	#include “xil_io.h”
XIo_In8	Xil_In8
XIo_Out8	Xil_Out8
XIo_In16	Xil_In16
XIo_Out16	Xil_Out16
XIo_In32	Xil_In32
XIo_Out32	Xil_Out32

Table 10: **Exception Function Mapping**

Old xexception	New Xil_exception
#include “xexception_l.h” #include “mb_interface.h”	#include “xil_exception.h”
XExc_Init	Xil_ExceptionInit
XExc_mEnableException microblaze_enable_exceptions	For all processors: Xil_ExceptionEnable(void)

Table 10: **Exception Function Mapping *(Cont'd)***

Old xexception	New Xil_exception
XExc_registerHandler microblaze_register_exception_handler	Xil_ExceptionRegisterHandler
XExc_RemoveHandler	Xil_ExceptionRemoveHandler
XExc_mDisableExceptions microblaze_disable_exceptions	Xil_ExceptionDisable

Table 11: **Interrupt Function Mapping**

Old Interrupt	New Xil_interrupt
#include "xexception_l.h"	#include "xil_exception.h"
XExc_RegisterHandler(XEXC_ID_NON_CRITICAL, handler) microblaze_register_handler(handler)	Xil_ExceptionRegisterHandler(XIL_EXCEPTION_ID_INT, handler)

Table 12: **Cache Function Mapping**

Old xcache	New xil_cache
#include "Xcache_l.h" #include "mb_interface.h"	#include "xil_cache.h"
XCache_EnableDCache microblaze_enable_dcache	For all processors: Xil_DCacheEnable(void)
XCache_DisableDCache microblaze_disable_dcache	Xil_DCacheDisable
XCache_InvalidateDCacheRange microblaze_invalidate_dcache_range	Xil_DCacheInvalidateRange
microblaze_invalidate_dcache	Xil_DCacheInvalidate
XCache_FlushDCacheRange microblaze_flush_dcache_range	Xil_DCacheFlushRange
microblaze_flush_dcache	Xil_DCacheFlush
XCache_EnableICache microblaze_enable_icache	For all processors: Xil_ICacheEnable(void)
XCache_DisableICache microblaze_disable_icache	Xil_ICacheDisable
XCache_InvalidateICacheRange microblaze_invalidate_icache_Range	Xil_ICacheInvalidateRange
microblaze_invalidate_icache	Xil_ICacheInvalidate

Table 13: **Assert Function Mapping**

Old ASSERT	New xil_assert
#include "xbasic_types.h"	#include "xil_assert.h"
XAssert	Xil_Assert
XASSERT_VOID	Xil_AssertVoid
XASSERT_NONVOID	Xil_AssertNonvoid
XASSERT_VOID_ALWAYS	Xil_AssertVoidAlways

Table 13: **Assert Function Mapping *(Cont'd)***

Old ASSERT	New xil_assert
XASSERT_NONVOID_ALWAYS	Xil_AssertNonvoidAlways
XAssertSetCallback	Xil_AssertSetCallback

Table 14: **Memory Test Function Mapping**

Old XUtil_Memtest	New xil_testmem
#include "xutil.h"	#include "xil_testmem.h"
XUtil_MemoryTest32	Xil_Testmem32
XUtil_MemoryTest16	Xil_Testmem16
XUtil_MemoryTest8	Xil_Testmem8

Program Profiling

The Standalone OS supports program profiling in conjunction with the GNU compiler tools and the Xilinx Microprocessor Debugger (XMD).

Note: XMD has been deprecated and will be removed in future versions of the Xilinx Software Development Kit (SDK). XSDB replaces XMD and provides additional functionality. We recommend you switch to XSDB for command-line debugging.

Profiling a program running on a hardware (board) provides insight into program execution and identifies where execution time is spent. The interaction of the program with memory and other peripherals can be more accurately captured.

Program running on hardware target is profiled using *software intrusive* method. In this method, the profiling software code is instrumented in the user program. The profiling software code is a part of the `libxil.a` library and is generated when software intrusive profiling is enabled in Standalone. For more details on about profiling, refer to the "Profile Overview" section of the *SDK Help.*

When the **`-pg`** profile option is specified to the compiler (`mb-gcc`), the profiling functions are linked with the application to profile automatically. The generated executable file contains code to generate profile information.

Upon program execution, this instrumented profiling function stores information on the hardware. The profile information can be read by the GNU gprof tool. The program functionality remains unchanged but it slows down the execution.

Note: The profiling functions do not have any explicit application API. The library is linked due to profile calls (`_mcount`) introduced by GCC for profiling.

Profiling Requirements

- Software intrusive profiling requires memory for storing profile information. You can use any memory in the system for profiling.
- A timer is required for sampling instruction address. The `axi_timer` is the supported profile timer for MicroBlaze processors. The Global Timer is used as the profile timer for Cortex A9 processors.

Profiling Functions

`_profile_init`

Called before the application `main( )` function. Initializes the profile timer routine and registers timer handler accordingly, based on the timer used, connects to the processor, and

starts the timer. The Tcl routine of Standalone library determines the timer type and the connection to processor, then generates the #defines in the `profile_config.h` file.

Refer to the "Microprocessor Library Definition (MLD)" chapter in the *Embedded System Tools Reference Manual (UG111)*, which is available in the installation directory. A link to this document is also provided in "MicroBlaze Processor API," page 1.

_mcount

Called by the `_mcount` function, which is inserted at every function start by `gcc`. Records the *caller* and *callee* information (Instruction address), which is used to generate call graph information.

_profile_intr_handler

The interrupt handler for the profiling timer. The timer is set to sample the executing application for PC values at fixed intervals and increment the Bin count. This function is used to generate the histogram information.

Configuring the Standalone OS

You can configure the Standalone OS using the Board Support Package Settings dialog box in SDK.

Table 15 lists the configurable parameters for the Standalone OS.

Table 15: **Configuration Parameters**

Parameter	Type	Default Value	Description
`enable_sw_intrusive_profiling`	Bool	false	Enable software intrusive profiling functionality. Select **`true`** to enable.
`profile_timer`	Peripheral Instance	none	Specify the timer to use for profiling. Select an **axi_timer** from the list of displayed instances. For Cortex A9, the ARM Cortex-A9 Private timer is used.
`stdin`	Peripheral Instance	none	Specify the **STDIN** peripheral from the drop down list
`stdout`	Peripheral Instance	none	Specify the **STDOUT** peripheral from the drop down list.
`predecode_fpu_exception`	Bool	false	This parameter is valid only for MicroBlaze processor when FPU exceptions are enabled in the hardware. Setting this to **`true`** will include extra code that decodes and stores the faulting FP instruction operands in global variables.

MicroBlaze MMU Example

The `tlb_add` function adds a single TLB entry. The parameters are:

tlbindex	The index of the TLB entry to be updated.
tlbhi	The value of the TLBHI field.
tlblo	The value of the TLBLO field.

```
static inline void tlb_add(int tlbindex, unsigned int tlbhi, unsigned int
tlblo)
{
    __asm__ __volatile__ ("mts rtlbx,  %2 \n\t"
                          "mts rtlbhi, %0 \n\t"
                          "mts rtlblo, %1 \n\t"
                          :: "r" (tlbhi),
                          "r" (tlblo),
                          "r" (tlbindex));

    tlbentry[tlbindex].tlbhi = tlbhi;
    tlbentry[tlbindex].tlblo = tlblo;
}
```

Given a base and high address, the tlb_add_entries function figures the minimum number page mappings/TLB entries required to cover the area. This function uses recursion to figure the entire range of mappings.

Parameters:

base	The base address of the region of memory
high	The high address of the region of memory
tlbaccess	The type of access required for this region of memory. It can be a logical or -ing of the following flags: 0 indicates read-only access TLB_ACCESS_EXECUTABLE means the region is executable TLB_ACCESS_WRITABLE means the region is writable

Returns: 1 on success and 0 on failure

```
static int tlb_add_entries (unsigned int base, unsigned int high, unsigned
int tlbaccess)
{
    int sizeindex, tlbsizemask;
    unsigned int tlbhi, tlblo;
    unsigned int area_base, area_high, area_size;
    static int tlbindex = 0;

    // Align base and high to 1KB boundaries
    base = base & 0xfffffc00;
   high = (high >= 0xfffffc00) ? 0xffffffff : ((high + 0x400) & 0xfffffc00)
- 1;

    // Start trying to allocate pages from 16 MB granularity down to 1 KB
    area_size   = 0x1000000;            // 16 MB
    tlbsizemask = 0x380;                // TLBHI[SIZE] = 7 (16 MB)

    for (sizeindex = 7; sizeindex >= 0; sizeindex--) {
        area_base = base & sizemask[sizeindex];
        area_high = area_base + (area_size - 1);

        // if (area_base <= (0xffffffff - (area_size - 1))) {

        if ((area_base >= base) && (area_high <= high)) {

            if (tlbindex < TLBSIZE) {
           tlbhi = (base & sizemask[sizeindex]) | tlbsizemask | 0x40;
// TLBHI: TAG, SIZE, V
            tlblo = (base & sizemask[sizeindex]) | tlbaccess | 0x8;
// TLBLO: RPN, EX, WR, W
                tlb_add (tlbindex, tlbhi, tlblo);
```

```
                    tlbindex++;
                } else {
                    // We only handle the 64 entry UTLB management for now
                    return 0;
                }

                // Recursively add entries for lower area
                if (area_base > base)
                    if (!tlb_add_entries (base, area_base - 1, tlbaccess))
                        return 0;
    // Recursively add entries for higher area
                if (area_high < high)
                    if (!tlb_add_entries(area_high + 1, high, tlbaccess))
                        return 0;

                break;
            }
            // else, we try the next lower page size
            area_size   = area_size >> 2;
            tlbsizemask = tlbsizemask - 0x80;
        }
        return 1;
    }
```

For a complete example, refer to:
`$XILINX_SDK/data/embeddedsw/lib/bsp/xilkernel_v6_1/src/src/arch/microblaze/mpu.c`.

LibXil Flash (v4.2)

Overview

The XilFlash library provides read/write/erase/lock/unlock features to access a parallel flash device. Flash device family specific functionality are also supported by the library. This library requires the underlying hardware platform to contain the following:

- axi_emc or similar core for accessing the flash.

This library implements the functionality for flash memory devices that conform to the "Common Flash Interface" (CFI) standard. CFI allows a single flash library to be used for an entire family of parts.This library supports Intel and AMD CFI compliant flash memory devices. Refer Table 1 for a list of supported flash devices.

All the calls in the library are blocking in nature in that the control is returned back to user only after the current operation is completed successfully or an error is reported.

The following common APIs are supported for all flash devices:

- Initialize
- Read
- Write
- Erase
- Lock
- UnLock
- IsReady
- Reset
- Device specific control

You must call the "int XFlash_Initialize (XFlash *InstancePtr, u32 BaseAddress, u8 BusWidth)" API before calling any other API in this library.

Supported Devices

Table 1 lists the supported CFI compliant flash memory devices.

Table 1: Flash Devices Supported by Xilflash Library

Flash Device	Manufacturer
MT28F320J	Micron
JS28F256	Intel
ST M29DW323DT	Micron
T28F128J3D075	Micron
PC28F512M29EW	Micron
S29GL128S	Spansion
PC28F00AP30TF	Micron

XilFlash Library APIs

This section provides a linked summary and detailed descriptions of the LibXil Flash library APIs.

API Summary

The following is a summary list of APIs provided by the LibXil Flash library. The list is linked to the API description. Click on the API name to go to the description.

int XFlash_Initialize (XFlash *InstancePtr, u32 BaseAddress, u8 BusWidth)
int XFlash_Reset (XFlash *InstancePtr)
int XFlash_Read (XFlash *InstancePtr, u32 Offset, u32 Bytes, void *DestPtr)
int XFlash_Write (XFlash *InstancePtr, u32 Offset, u32Bytes, void *SrcPtr)
int XFlash_Erase (XFlash *InstancePtr, u32 Offset, u32 Bytes)
int XFlash_Lock (XFlash *InstancePtr, u32 Offset, u32 Bytes)
int XFlash_UnLock (XFlash *InstancePtr, u32 Offset, u32 Bytes)
int XFlash_DeviceControl (XFlash *InstancePtr, u32 Command, DeviceControl *Parameters)
int XFlash_IsReady (XFlash *InstancePtr)

XilFlash Library API Descriptions

`int` **`XFlash_Initialize`** `(XFlash` ***`*InstancePtr, u32 BaseAddress, u8 BusWidth`***`)`

Parameters

`InstancePtr` is a pointer to XFlash Instance.

`BaseAddress` is the base address of the Flash memory.

`BusWidth` is the total width of the Flash memory, in bytes.

Returns

`XST_SUCCESS` if successful.

`XFLASH_PART_NOT_SUPPORTED` if the command set algorithm or the layout is not supported by any flash family compiled into the system.

`XFLASH_CFI_QUERY_ERROR` if the device would not enter the CFI query mode. Either device doesn't support CFI or unsupported part layout exists or a hardware problem exists.

Description

Initializes a specific XFlash Instance.

The initialization entails:

- Issuing the CFI query command
- Identifying the Flash family and layout from CFI data
- Setting the default options for the instance
- Setting up the VTable
- Initialize the Xilinx Platform Flash XL to Async mode if the user selects to use the Platform Flash XL. The Platform Flash XL is an Intel CFI complaint device.

Includes

xilflash.h

xilflash_cfi.h

xilflash_intel.h

xilflash_amd.h

`int` **`XFlash_Reset`** `(XFlash` ***`*InstancePtr`***`)`

Parameters

`InstancePtr` is a pointer to XFlash Instance.

Returns

XST_SUCCESS if Successful.

XFLASH_BUSY if the flash devices were in the middle of an operation and could not be reset.

XFLASH_ERROR if the device has experienced an internal error during the operation. XFlash_DeviceControl() must be used to access the cause of the device specific error condition.

Description

Resets the flash device and places it in read mode.

Includes

`xilflash.h`

`xilflash_cfi.h`

`xilflash_intel.h`

`xilflash_amd.h`

`int` **`XFlash_Read`** `(XFlash` ***`*InstancePtr`***`, u32` ***`Offset`***`, u32`

Bytes, void **DestPtr*)

Parameters	*InstancePtr* is a pointer to XFlash Instance. *Offset* is the offset into the devices address space from which to read. *Bytes* is the number of bytes to read. *DestPtr* is the destination Address to copy data to.
Returns	XST_SUCCESS if successful. XFLASH_ADDRESS_ERROR if the source address did not start within the addressable areas of the device.
Description	This API reads the data from the flash device and copies it into the specified user buffer. The source and destination addresses can be on any alignment supported by the processor.
Includes	xilflash.h xilflash_cfi.h xilflash_intel.h xilflash_amd.h

---

int **XFlash_Write** (XFlash **InstancePtr*, u32 *Offset*, u32*Bytes*, void **SrcPtr*)

Parameters	*InstancePtr* is a pointer to XFlash Instance. *Offset* is the offset into the devices address space from which to begin programming. *Bytes* is the number of bytes to Program. *SrcPtr* is the Source Address containing data to be programmed.
Returns	XST_SUCCESS if successful. XFLASH_ERROR if a write error has occurred. The error is usually device specific. Use XFlash_DeviceControl() to retrieve specific error conditions. When this error is returned, it is possible that the target address range was only partially programmed.
Description	Programs the flash device with the data specified in the user buffer. The source and destination addresses must be aligned to the width of the flash data bus. If the processor supports unaligned access, then the source address does not need to be aligned to the flash width; however, this library is generic, and because some processors (such as MicroBlaze™ processors) do not support unaligned access, this API requires that the source address be aligned.
Includes	xilflash.h xilflash_cfi.h xilflash_intel.h xilflash_amd.h

int **XFlash_Erase** (XFlash **InstancePtr*, u32 *Offset*, u32

Bytes)

Parameters	*InstancePtr* is a pointer to XFlash Instance. *Offset* is the offset into the devices address space from which to begin erasure. *Bytes* is the number of bytes to Erase.
Returns	XST_SUCCESS if successful. XFLASH_ADDRESS_ERROR if the destination address range is not completely within the addressable areas of the device.
Description	This API erases the specified address range in the flash device. The number of bytes to erase can be any number as long as it is within the bounds of the devices.
Includes	xilflash.h xilflash_cfi.h xilflash_intel.h xilflash_amd.h

---

int **XFlash_Lock** (XFlash **InstancePtr*, u32 *Offset*, u32 *Bytes*)

Parameters	*InstancePtr* is a pointer to XFlash instance. *Offset* is the offset of the block address into the devices address space which need to be locked. *Bytes* is the number of bytes to be locked.
Returns	XST_SUCCESS if successful. XFLASH_ADDRESS_ERROR if the destination address range is not completely within the addressable areas of the device.
Description	Locks a block in the flash device.
Includes	xilflash.h xilflash_cfi.h xilflash_intel.h xilflash_amd.h

`int` **`XFlash_UnLock`** `(XFlash *InstancePtr, u32 Offset, u32 Bytes)`

Parameters	*InstancePtr* is a pointer to XFlash Instance. *Offset* is the offset of the block address into the devices address space which need to be unlocked. *Bytes* is the number of bytes to be unlocked.
Returns	XST_SUCCESS if successful. XFLASH_ADDRESS_ERROR if the destination address range is not completely within the addressable areas of the device.
Description	Unlocks previously locked blocks that are locked.
Includes	xilflash.h xilflash_cfi.h xilflash_intel.h xilflash_amd.h

---

`int` **`XFlash_DeviceControl`** `(XFlash *InstancePtr, u32 Command, DeviceControl *Parameters)`

Parameters	*InstancePtr* is a pointer to XFlash Instance. *Command* is the device specific command to issue. *Parameters* specifies the arguments passed to the device control function.
Returns	XST_SUCCESS if successful. XFLASH_NOT_SUPPORTED if the command is not supported by the device.
Description	Executes device specific commands.
Includes	xilflash.h xilflash_cfi.h xilflash_intel.h xilflash_amd.h

---

`int` **`XFlash_IsReady`** `(XFlash *InstancePtr)`

Parameters	*InstancePtr* is a pointer to XFlash instance.
Returns	TRUE if the device has been initialized; otherwise, FALSE.
Description	Checks the device readiness, signifying successful initialization.
Includes	xilflash.h xilflash_cfi.h xilflash_intel.h xilflash_amd.h

Libgen Customization

XilFlash Library can be integrated with a system using the following snippet in the Microprocessor Software Specification (MSS) file:

```
BEGIN LIBRARY
PARAMETER LIBRARY_NAME = xilflash
PARAMETER LIBRARY_VER = 4.2
PARAMETER PROC_INSTANCE = microblaze_0
PARAMETER ENABLE_INTEL = true
PARAMETER ENABLE_AMD = false
END
```

Where:

- `LIBRARY_NAME`—Is the library name (`xilflash`).
- `LIBRARY_VER`—Is the library version (`4.2`).
- `PROC_INSTANCE`—Is the processor name (`microblaze_0`).
- `ENABLE_INTEL`—Enables or disables the Intel flash device family (`true` | `false`).
- `ENABLE_AMD`—Enables or disables the AMD flash device family (`true` | `false`).

Xilkernel (v6.4)

Overview

Xilkernel is a small, robust, and modular kernel. It is a free software library that you receive with the Xilinx® Software Development Kit (SDK). Xilkernel:

- Allows a high degree of customization, letting you tailor the kernel to an optimal level both in terms of size and functionality.
- Supports the core features required in a lightweight embedded kernel, with a POSIX API.
- Works on MicroBlaze™ processors.

Xilkernel IPC services can be used to implement higher level services (such as networking, video, and audio) and subsequently run applications using these services.

Why Use a Kernel?

The following are a few of the deciding factors that can influence your choice of using a kernel as the software platform for your next application project:

- Typical embedded control applications comprise various *tasks* that need to be performed in a particular sequence or schedule. As the number of control tasks involved grows, it becomes difficult to organize the sub-tasks manually, and to time-share the required work. The responsiveness and the capability of such an application decreases dramatically when the complexity is increased.
- Breaking down tasks as individual applications and implementing them on an operating system (OS) is much more intuitive.
- A kernel enables the you to write code at an abstract level, instead of at a small, micro-controller-level standalone code.
- Many common and legacy applications rely on OS services such as file systems, time management, and so forth. Xilkernel is a thin library that provides these essential services. Porting or using common and open source libraries (such as graphics or network protocols) might require some form of these OS services also.

Key Features

Xilkernel includes the following key features:

- High scalability into a given system through the inclusion or exclusion of functionality as required.
- Complete kernel configuration and deployment within minutes from inside of SDK.
- Robustness of the kernel: system calls protected by parameter validity checks and proper return of POSIX error codes.
- A POSIX API targeting embedded kernels, win core kernel features such as:
  - Threads with round-robin or strict priority scheduling.
  - Synchronization services: semaphores and mutex locks.
  - IPC services: message queues and shared memory.
  - Dynamic buffer pool memory allocation.
  - Software timers.
  - User-level interrupt handling.
- Static thread creation that startup with the kernel.

- System call interface to the kernel.
- Exception handling for the MicroBlaze processor.
- Memory protection using MicroBlaze Memory Management (Protection) Unit (MMU) features when available.

Xilkernel Organization

The kernel is highly modular in design. You can select and customize the kernel modules that are needed for the application at hand. Customizing the kernel is discussed in detail in "Kernel Customization," page 43[1]. Figure 1 shows the various modules of Xilkernel:

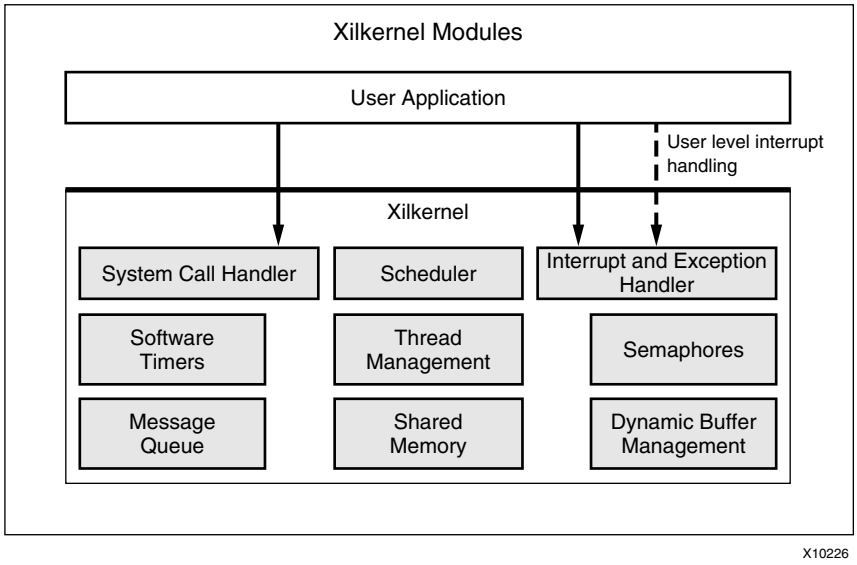

Figure 1: **Xilkernel Modules**

Building Xilkernel Applications

Xilkernel is organized in the form of a library of kernel functions. This leads to a simple model of kernel linkage. To build Xilkernel, you must include Xilkernel in your software platform, configure it appropriately, and run Libgen to generate the Xilkernel library. Your application sources can be edited and developed separately. After you have developed your application, you must link with the Xilkernel library, thus pulling in all the kernel functionality to build the final kernel image. The Xilkernel library is generated as `libxilkernel.a`. Figure 2, page 3 shows this development flow.

Internally, Xilkernel also supports the much more powerful, traditional OS-like method of linkage and separate executables. Conventional operating systems have the kernel image as a separate file and each application that executes on the kernel as a separate file. However, Xilinx recommends that you use the more simple and more elegant library linkage mode. This mode provides maximum ease of use. It is also the preferred mode for debugging, downloading, and bootloading. The separate executable mode is required only by those who have advanced requirements in the form of separate executables. The separate executable mode and its caveats are documented in "Deprecated Features," page 51.

The following are the steps for the kernel linkage mode of application development:

1. Application source C files should include the file `xmk.h` as the first file among others. For example, defining the `includexmk.h` flag makes available certain definitions and declarations from the GNU include files that are required by Xilkernel and applications.

1. Some of these features might not be fully supported in a given release of Xilkernel.

2. Your application software project links with the library `libxil.a`. This library contains the actual kernel functions generated. Your application links with this and forms the final kernel and application image.
3. Xilkernel is responsible for all first level interrupt and exception handling on both the MicroBlaze and PowerPC processors. Therefore, you should not directly attempt to use any of the methods of handling interrupts documented for standalone programs. Instead refer to the section on interrupt handling for how to handle user level interrupts and exceptions.
4. You can control the memory map of the kernel by using the linker script feature of the final software application project that links with the kernel. Automatic linker script generation helps you here.
5. Your application must provide a `main( )` which is the starting point of execution for your kernel image. Inside your `main( )`, you can do any initialization and setup that you need to do. The kernel remains unstarted and dormant. At the point where your application setup is complete and you want the kernel to start, you must invoke `xilkernel_main( )` that starts off the kernel, enables interrupts, and transfers control to your application processes, as configured. Some system-level features may need to be enabled before invoking `xilkernel_main( )`. These are typically machine-state features such as cache enablement, hardware exception enablement which must be “always ON” even when context switching from application to application. Make sure that you setup such system state before invoking `xilkernel_main( )`. Also, you must not arbitrarily modify such system-state in your application threads. If a context switch occurs when the system state is modified, it could lead to subsequent threads executing without that state being enabled; consequently, you must lock out context switches and interrupts before you modify such a state.

Note: Your linker script must be aware of the requirements for the kernel.

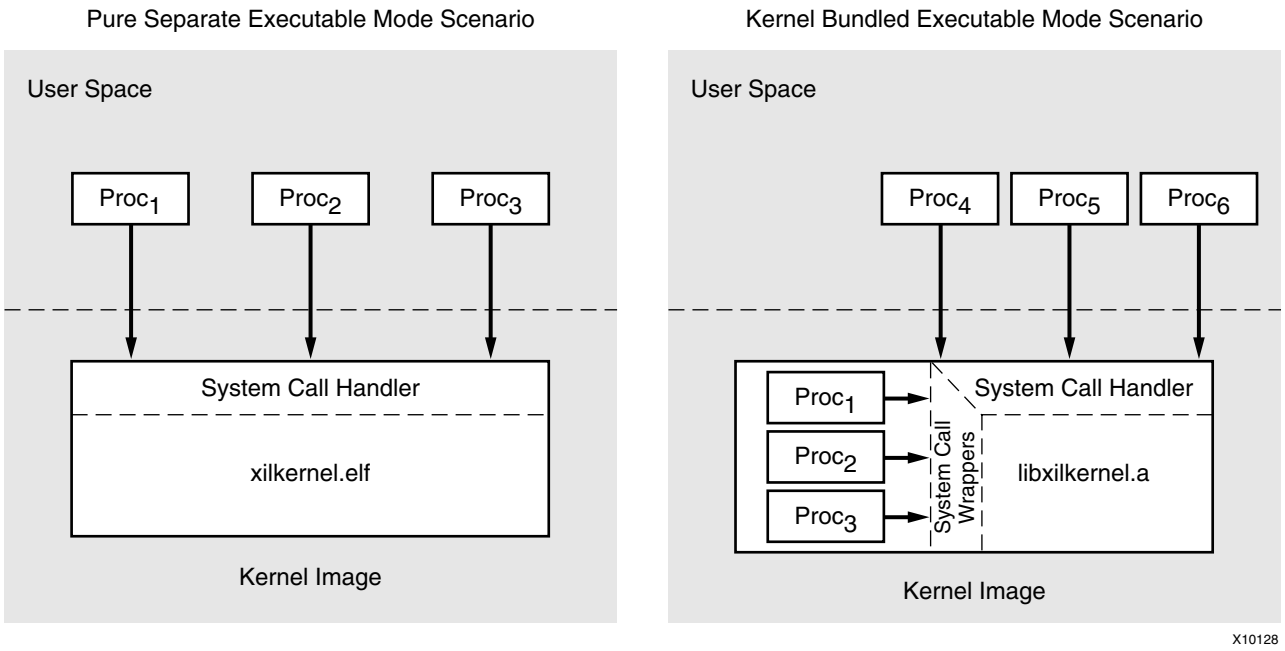

Figure 2: **Xilkernel Development Flow**

Xilkernel Process Model

The units of execution within Xilkernel are called *process contexts*. Scheduling is done at the process context level. There is no concept of thread groups combining to form, what is conventionally called a process. Instead, all the threads are peers and compete equally for resources. The POSIX threads API is the primary user-visible interface to these process contexts. There are a few other useful additional interfaces provided, that are not a part of POSIX. The interfaces allow creating, destroying, and manipulating created application threads. The actual interfaces are described in detail in "Xilkernel API," page 6. Threads are manipulated with thread identifiers. The underlying process context is identified with a process identifier *pid_t*.

Xilkernel Scheduling Model

Xilkernel supports either priority-driven, preemptive scheduling with time slicing (`SCHED_PRIO`) or simple round-robin scheduling (`SCHED_RR`). This is a global scheduling policy and cannot be changed on a per-thread basis. This must be configured statically at kernel generation time.

In `SCHED_RR`, there is a single ready queue and each process context executes for a configured time slice before yielding execution to the next process context in the queue.

In `SCHED_PRIO` there are as many ready queues as there are priority levels. Priority 0 is the highest priority in the system and higher values mean lower priority.

As shown in the following figure, the process that is at the head of the highest priority ready queue is always scheduled to execute next. Within the same priority level, scheduling is round-robin and time-sliced. If a ready queue level is empty, it is skipped and the next ready queue level examined for schedulable processes. Blocked processes are off their ready queues and in their appropriate wait queues. The number of priority levels can be configured for `SCHED_PRIO`.

For both the scheduling models, the length of the ready queue can also be configured. If there are wait queues inside the kernel (in semaphores, message queues), they are configured as priority queues if scheduling mode is `SCHED_PRIO`. Otherwise, they are configured as simple first-in-first-out (FIFO) queues.

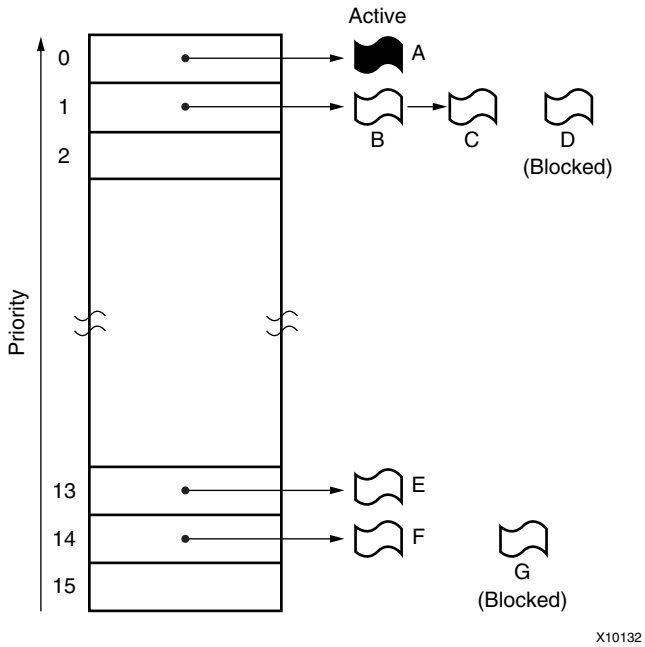

Figure 3: **Priority-Driven Scheduling**

Each process context is in any of the following six states:

- `PROC_NEW` - A newly created process.
- `PROC_READY` - A process ready to execute.
- `PROC_RUN` - A process that is running.
- `PROC_WAIT` - A process that is blocked on a resource.
- `PROC_DELAY` - A process that is waiting for a timeout.
- `PROC_TIMED_WAIT` - A process that is blocked on a resource and has an associated timeout.

When a process terminates, it enters a dead state called `PROC_DEAD`. The process context state diagram is shown in the following figure.

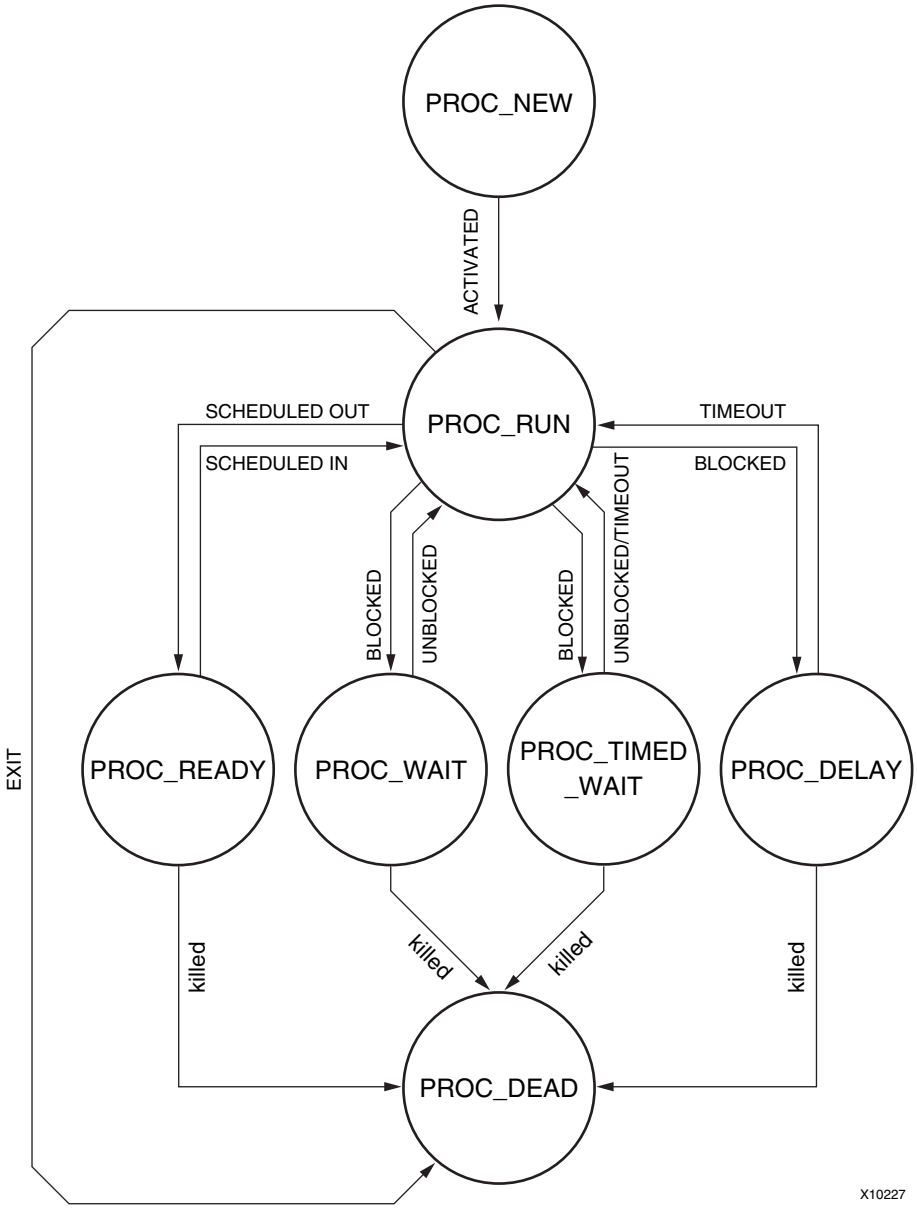

Figure 4: **Process Context States**

POSIX Interface

Xilkernel provides a POSIX interface to the kernel. Not all the concepts and interfaces defined by POSIX are available. A subset covering the most useful interfaces and concepts are implemented. Xilkernel programs can run almost equivalently on your desktop OS, like Linux or SunOS. This makes for easy application development, portability and legacy software support. The programming model appeals to those who have worked on equivalent POSIX interfaces on traditional operating systems. For those interfaces that have been provided, POSIX is rigorously adhered to in almost all cases. For cases that do differ, the differences are clearly specified. Refer to "Xilkernel API", for the actual interfaces and their descriptions.

Xilkernel Functions

Click an item below view function summaries and descriptions for:

- Thread Management
- Semaphores
- Message Queues
- Shared Memory
- Mutex Locks
- Dynamic Buffer Memory Management
- Software Timers
- Memory Protection Overview

Xilkernel API

Thread Management

Xilkernel supports the basic POSIX threads API. Thread creation and manipulation is done in standard POSIX notation. Threads are identified by a unique thread identifier. The thread identifier is of type `pthread_t`. This thread identifier uniquely identifies a thread for an operation. Threads created in the system have a kernel wrapper to which they return control to when they terminate. So, a specific exit function is not required at the end of the thread's code.

Thread stack is allocated automatically on behalf of the thread from a pool of Block Starting Symbol (BSS) memory that is statically allocated based upon the maximum number of system threads. You can also assign a custom piece of memory as the stack for each thread to create dynamically.

The entire thread module is optional and can be configured in or out as a part of the software specification. See "Configuring Thread Management," page 45 for more details on customizing this module.

Thread Management Function Summary

The following list is a linked summary of the thread management functions in Xilkernel. Click on a function to view a detailed description.

int pthread_create(pthread_t thread, pthread_attr_t* att, void*(*start_func)(void*),void* param)
void pthread_exit(void *value_ptr)
int pthread_join(pthread_t thread, void **value_ptr)
int pthread_detach(pthread_t target)
int pthread_equal(pthread_t t1, pthread_t t2)
int pthread_getschedparam(pthread_t thread, int *policy, struct sched_param *param)
int pthread_setschedparam(pthread_t thread, int policy, const struct sched_param *param)
int pthread_attr_init(pthread_attr_t* attr)
int pthread_attr_destroy (pthread_attr_t* attr)
int pthread_attr_setdetachstate(pthread_attr_t* attr, int dstate)
int pthread_attr_getdetachstate(pthread_attr_t* attr, int *dstate)
int pthread_attr_setschedparam(pthread_attr_t* attr, struct sched_param *schedpar)
int pthread_attr_getschedparam(pthread_attr_t* attr, struct sched_param* schedpar)
int pthread_attr_setstack(const pthread_attr_t *attr, void *stackaddr, size_t stacksize)
int pthread_attr_getstack(const pthread_attr_t *attr, void **stackaddr, size_t *stacksize)
pid_t get_currentPID(void)
int kill(pid_tpid)
int process_status(pid_t pid, p_stat *ps)
int xmk_add_static_thread(void* (*start_routine)(void *), int sched_priority)
int yield(void)

Thread Management Function Descriptions

The following descriptions are the thread management interface identifiers.

`int` **`pthread_create`**`(pthread_t` *`thread`*`, pthread_attr_t*` *`att`*`, void*(*`*`start_func`*`)(void*),void*` *`param`*`)`

Parameters	*`thread`* is the location at which to store the created thread's identifier. *`attr`* is the pointer to thread creation attributes structure. *`start_func`* is the start address of the function from which the thread needs to execute. *`param`* is the pointer argument to the thread function.
Returns	0 and thread identifier of the created thread in *`thread`*, on success. -1 if *`thread`* refers to an invalid location. `EINVAL` if *`attr`* refers to invalid attributes. `EAGAIN` if resources unavailable to create the thread.
Description	`pthread_create( )` creates a new thread, with attributes specified by *`attr`*, within a process. If *`attr`* is `NULL`, the default attributes are used. If the attributes specified by *`attr`* are modified later, the thread's attributes are not affected. Upon successful completion, `pthread_create( )` stores the ID of the created thread in the location referenced by thread. The thread is created executing *`start_routine`* with `arg` as its sole argument. If the *`start_routine`* returns, the effect is as if there was an implicit call to `pthread_exit( )` using the return value of *`start_routine`* as the exit status. This is explained in the *`pthread_exit`* description. You can control various attributes of a thread during its creation. See the *`pthread_attr`* routines for a description of the kinds of thread creation attributes that you can control.
Includes	`xmk.h, pthread.h`

`void` **`pthread_exit`**`(void` *`*value_ptr`*`)`

Parameters	*`value_ptr`* is a pointer to the return value of the thread.
Returns	None.
Description	The `pthread_exit( )` function terminates the calling thread and makes the value *`value_ptr`* available to any successful join with the terminating thread. Thread termination releases process context resources including, but not limited to, memory and attributes. An implicit call to `pthread_exit( )` is made when a thread returns from the creating start routine. The return value of the function serves as the thread's exit status. Therefore no explicit `pthread_exit( )` is required at the end of a thread.
Includes	`xmk.h, pthread.h`

`int` **`pthread_join`**`(pthread_t` *`thread`*`, void **`*`value_ptr`*`)`

Parameters	*`value_ptr`* is a pointer to the return value of the thread.
Returns	0 on success. `ESRCH` if the target thread is not in a joinable state or is an invalid thread. `EINVAL` if the target thread already has someone waiting to join with it.
Description	The `pthread_join( )` function suspends execution of the calling thread until the *`pthread_t`* (target thread) terminates, unless the target thread has already terminated.Upon return from a successful `pthread_join( )` call with a non-`NULL` *`value_ptr`* argument, the value passed to the `pthread_exit( )` function by the terminating thread is made available in the location referenced by *`value_ptr`*. When a `pthread_join( )` returns successfully, the target thread has been terminated. The results of multiple simultaneous calls to `pthread_join( )` specifying the same target thread are that only one thread succeeds and the others fail with `EINVAL`. ***Note:*** No deadlock detection is provided.
Includes	`xmk.h, pthread.h`

`pthread_t` **`pthread_self`**`(void)`

Parameters	None.
Returns	On success, returns thread identifier of current thread. Error behavior not defined.
Description	The `pthread_self( )` function returns the thread ID of the calling thread.
Includes	`xmk.h, pthread.h`

`int` **`pthread_detach`**`(pthread_t` *`target`*`)`

Parameters	*`target`* is the target thread to detach.
Returns	0 on success. `ESRCH` if target thread cannot be found.
Description	The `pthread_detach( )` function indicates to the implementation that storage for the *`thread`* can be reclaimed when that thread terminates. If thread has not terminated, `pthread_detach( )` does not cause it to terminate. The effect of multiple `pthread_detach( )` calls on the same target thread is unspecified.
Includes	`xmk.h, pthread.h`

`int` **`pthread_equal`**`(pthread_t` *`t1`*`, pthread_t` *`t2`*`)`

Parameters	*`t1`* and *`t2`* are the two thread identifiers to compare.
Returns	1 if *`t1`* and *`t2`* refer to threads that are equal. 0 otherwise.
Description	The `pthread_equal( )` function returns a non-zero value if *`t1`* and *`t2`* are equal; otherwise, zero is returned. If either *`t1`* or *`t2`* are not valid thread IDs, zero is returned.
Includes	`xmk.h, pthread.h`

`int` **`pthread_getschedparam`**`(pthread_t` *`thread`*`, int` *`*policy`*`, struct sched_param` *`*param`*`)`

Parameters	*`thread`* is the identifier of the thread on which to perform the operation. *`policy`* is a pointer to the location where the global scheduling policy is stored. *`param`* is a pointer to the scheduling parameters structure.
Returns	0 on success. `ESRCH` if the value specified by thread does not refer to an existing thread. `EINVAL` if param or policy refer to invalid memory.
Description	The `pthread_getschedparam( )` function gets the scheduling policy and parameters of an individual thread. For `SCHED_RR` there are no scheduling parameters; consequently, this routine is not defined for `SCHED_RR`. For `SCHED_PRIO`, the only required member of the sched_param structure is the priority *`sched_priority`*. The returned priority value is the value specified by the most recent `pthread_getschedparam( )` or `pthread_create( )` call affecting the target thread. It does not reflect any temporary adjustments to its priority as a result of any priority inheritance or ceiling functions. This routine is defined only if scheduling type is `SCHED_PRIO`.
Returns	`xmk.h, pthread.h`

`int` **`pthread_setschedparam`**`(pthread_t` *`thread,`* `int` *`policy`*`, const struct sched_param` *`*param)`*

Parameters	*`thread`* is the identifier of the thread on which to perform the operation. *`policy`* is ignored. *`param`* is a pointer to the scheduling parameters structure.
Returns	0 on success. `ESRCH` if *`thread`* does not refer to a valid thread. `EINVAL` if the scheduling parameters are invalid.
Description	The `pthread_setschedparam( )` function sets the scheduling policy and parameters of individual threads to be retrieved. For `SCHED_RR` there are no scheduling parameters; consequently this routine is not defined for `SCHED_RR`. For `SCHED_PRIO`, the only required member of the sched_param structure is the priority *`sched_priority`*. The priority value must be a valid value as configured in the scheduling parameters of the kernel. The policy parameter is ignored. ***Note:*** This routine is defined only if scheduling type is `SCHED_PRIO`.
Includes	`xmk.h, pthread.h`

`int` **`pthread_attr_init`**`(pthread_attr_t*` ***`attr`***`)`

Parameters	***`attr`*** is a pointer to the attribute structure to be initialized.
Returns	0 on success. 1 on failure. `EINVAL` on invalid ***`attr`*** parameter.
Description	The `pthread_attr_init( )` function initializes a thread attributes object ***`attr`*** with the default value for all of the individual attributes used by a given implementation. The function contents are defined in the `sys/types.h` header. ***Note:*** This function does not make a call to the kernel.
Includes	`xmk.h, pthread.h`

`int` **`pthread_attr_destroy`** `(pthread_attr_t*` ***`attr`***`)`

Parameters	***`attr`*** is a pointer to the thread attributes that must be destroyed.
Returns	0 on success. `EINVAL` on errors.
Description	The `pthread_attr_destroy( )` function destroys a thread attributes object and sets ***`attr`*** to an implementation-defined invalid value. Re-initialize a destroyed ***`attr`*** attributes object with `pthread_attr_init( )`; the results of otherwise referencing the object after it is destroyed are undefined. ***Note:*** This function does not make a call to the kernel.
Includes	`xmk.h, pthread.h`

`int` **`pthread_attr_setdetachstate`**`(pthread_attr_t*` ***`attr`***`, int` ***`dstate`***`)`

Parameters	***`attr`*** is the attribute structure on which the operation is to be performed. ***`dstate`*** is the detachstate required.
Returns	0 on success. `EINVAL` on invalid parameters.
Description	The detachstate attribute controls whether the thread is created in a detached state. If the thread is created detached, then when the thread exits, the thread's resources are detached without requiring a `pthread_join( )` or a call `pthread_detach( )`.The application can set detachstate to either `PTHREAD_CREATE_DETACHED` or `PTHREAD_CREATE_JOINABLE`. ***Note:*** This does not make a call into the kernel.
Includes	`xmk.h, pthread.h`

`int` **`pthread_attr_getdetachstate`**`(pthread_attr_t*` ***`attr`***`, int *`***`dstate`**`)`

Parameters	***`attr`*** is the attribute structure on which the operation is to be performed. ***`dstate`*** is the location in which to store the detachstate.
Returns	0 on success. `EINVAL` on invalid parameters.
Description	The implementation stores either `PTHREAD_CREATE_DETACHED` or `PTHREAD_CREATE_JOINABLE` in dstate, if the value of detachstate was valid in ***`attr`***. ***Note:*** This does not make a call into the kernel.
Includes	`xmk.h, pthread.h`

`int` **`pthread_attr_setschedparam`**`(pthread_attr_t*` ***`attr`***`, struct sched_param *`***`schedpar`**`)`

Parameters	***`attr`*** is the attribute structure on which the operation is to be performed. ***`schedpar`*** is the location of the structure that contains the scheduling parameters.
Returns	0 on success. `EINVAL` on invalid parameters. `ENOTSUP` for invalid scheduling parameters.
Description	The `pthread_attr_setschedparam( )` function sets the scheduling parameter attributes in the ***`attr`*** argument. The contents of the ***`sched_param`*** structure are defined in the `sched.h` header. ***Note:*** This does not make a call into the kernel.
Includes	`xmk.h, pthread.h`

`int` **`pthread_attr_getschedparam`**`(pthread_attr_t*` ***`attr`***`, struct sched_param*` ***`schedpar`***`)`

Parameters	***`attr`*** is the attribute structure on which the operation is to be performed. ***`schedpar`*** is the location at which to store the ***`sched_param`*** structure.
Returns	0 on success. `EINVAL` on invalid parameters.
Description	The `pthread_attr_getschedparam( )` gets the scheduling parameter attributes in the ***`attr`*** argument. The contents of the `param` structure are defined in the `sched.h` header. ***Note:*** This does not make a call to the kernel.
Includes	`xmk.h, pthread.h`

`int` **`pthread_attr_setstack`**`(const pthread_attr_t *attr, void *stackaddr, size_t stacksize)`

Parameters	*attr* is the attributes structure on which to perform the operation. *stackaddr* is base address of the stack memory. *stacksize* is the size of the memory block in bytes.
Returns	0 on success. EINVAL if the *attr* param is invalid or if *stackaddr* is not aligned appropriately.
Description	The pthread_attr_setstack( ) function shall set the thread creation stack attributes *stackaddr* and *stacksize* in the *attr* object. The stack attributes specify the area of storage to be used for the created thread's stack. The base (lowest addressable byte) of the storage is *stackaddr*, and the size of the storage is *stacksize* bytes. The *stackaddr* must be aligned appropriately according to the processor EABI, to be used as a stack; for example, pthread_attr_setstack( ) might fail with EINVAL if (*stackaddr* and 0x3) is not 0. ***Note:*** For the MicroBlaze processor, the alignment required is 4 bytes.
Includes	xmk.h, pthread.h

`int` **`pthread_attr_getstack`**`(const pthread_attr_t *attr, void **stackaddr, size_t *stacksize)`

Parameters	*attr* is the attributes structure on which to perform the operation. *stackaddr* is the location at which to store the base address of the stack memory. *stacksize* is the location at which to store the size of the memory block in bytes.
Returns	0 on success. EINVAL on invalid *attr.*
Description	The pthread_attr_getstack( ) function retrieves the thread creation attributes related to stack of the specified attributes structure and stores it in stackaddr and stacksize.
Includes	xmk.h, pthread.h

`pid_t` **`get_currentPID`**`(void)`

Parameters	None.
Returns	The process identifier associated with the current thread or elf process.
Description	Gets the underlying process identifier of the process context that is executing currently. The process identifier is needed to perform certain operations like kill( ) on both processes and threads.
Includes	xmk.h, sys/process.h

`int` **`kill`**`(pid_t`*`pid`*`)`

Parameters	*pid* is the PID of the process.
Returns	0 on success. -1 on failure.
Description	Removes the process context specified by *pid* from the system. If *pid* refers to the current executing process context, then it is equivalent to the current process context terminating. A kill can be invoked on processes that are suspended on wait queues or on a timeout. No indication is given to other processes that are dependant on this process context. ***Note:*** This function is defined only if `CONFIG_KILL` is true. This can be configured in with the enhanced features category of the kernel.
Includes	`xmk.h, sys/process.h`

`int` **`process_status`**`(pid_t` *`pid`*`, p_stat *`*`ps`*`)`

Parameters	*pid* is the PID of process. *ps* is the buffer where the process status is returned.
Returns	Process status in `ps` on success. `NULL` in *ps* on failure.
Description	Get the status of the process or thread, whose pid is *pid*. The status is returned in structure p_stat which has the following fields: • *pid* is the process ID. • *state* is the current scheduling state of the process. The contents of `p_stat` are defined in the `sys/ktypes.h` header.
Includes	`xmk.h, sys/process.h`

`int` **`xmk_add_static_thread`**`(void* (*`*`start_routine`*`)(void *), int` *`sched_priority`*`)`

Parameters	*start_routine* is the thread start routine. *sched_priority* is the priority of the thread when the kernel is configured for priority scheduling.
Returns	0 on success and -1 on failure.
Description	This function provides the ability to add a thread to the list of startup or static threads that run on kernel start, via C code. This function must be used prior to xilkernel_main() being invoked.
Includes	`xmk.h, sys/init.h`

`int yield(void)`

Parameters	None.
Returns	None.
Description	Yields the processor to the next process context that is ready to execute. The current process is put back in the appropriate ready queue. ***Note:*** This function is optional and included only if `CONFIG_YIELD` is defined. This can be configured in with the enhanced features category of the kernel.
Includes	`xmk.h, sys/process.h`

Semaphores

Xilkernel supports kernel-allocated POSIX semaphores that can be used for synchronization. POSIX semaphores are counting semaphores that also count below zero (a negative value indicates the number of processes blocked on the semaphore). Xilkernel also supports a few interfaces for working with named semaphores. The number of semaphores allocated in the kernel and the length of semaphore wait queues can be configured during system initialization. Refer to "Configuring Semaphores," page 46 for more details. The semaphore module is optional and can be configured in or out during system initialization. The message queue module, described later on in this document, uses semaphores. This module must be included if you are to use message queues.

Semaphore Function Summary

The following list provides a linked summary of the semaphore functions in Xilkernel. You can click on a function to go to the description.

int sem_init(sem_t *sem, int pshared, unsigned value)
int sem_destroy(sem_t* sem)
int sem_getvalue(sem_t* sem, int* value)
int sem_wait(sem_t* sem)
int sem_trywait(sem_t* sem)
int sem_timedwait(sem_t* sem, unsigned_ms)
sem_t* sem_open(const char* name, int oflag,...)
int sem_close(sem_t* sem)
int sem_post(sem_t* sem)
int sem_unlink(const char* name)

Semaphore Function Descriptions

The following are descriptions of the Xilkernel semaphore functions:

`int` **`sem_init`**`(sem_t *sem, int pshared, unsigned value)`

Parameters	*sem* is the location at which to store the created semaphore's identifier. *pshared* indicates sharing status of the semaphore, between processes. *value* is the initial count of the semaphore. ***Note:*** *pshared* is unused currently.
Returns	0 on success. -1 on failure and sets errno appropriately. The errno is set to ENOSPC if no more semaphore resources are available in the system.
Description	The sem_init( ) function initializes the unnamed semaphore referred to by *sem*. The value of the initialized semaphore is *value*. Following a successful call to sem_init( ), the semaphore can be used in subsequent calls to sem_wait( ), sem_trywait( ), sem_post( ), and sem_destroy( ). This semaphore remains usable until the semaphore is destroyed. Only sem itself can be used for performing synchronization. The result of referring to copies of sem in calls to sem_wait( ), sem_trywait( ), sem_post( ), and sem_destroy( ) is undefined. Attempting to initialize an already initialized semaphore results in undefined behavior.
Includes	xmk.h, semaphore.h

`int` **`sem_destroy`**`(sem_t* sem)`

Parameters	*sem* is the semaphore to be destroyed.
Returns	0 on success. -1 on failure and sets errno appropriately. The errno can be set to: • EINVAL if the semaphore identifier does not refer to a valid semaphore. • EBUSY if the semaphore is currently locked, and processes are blocked on it.
Description	The sem_destroy( ) function destroys the unnamed semaphore indicated by sem. Only a semaphore that was created using sem_init( ) can be destroyed using sem_destroy( ); the effect of calling sem_destroy( ) with a named semaphore is undefined. The effect of subsequent use of the semaphore *sem* is undefined until *sem* is re-initialized by another call to sem_init( ).
Includes	xmk.h, semaphore.h

`int` **`sem_getvalue`**`(sem_t*` *`sem`*`, int*` *`value`*`)`

Parameters	*sem* is the semaphore identifier. *value* is the location where the semaphore value is stored.
Returns	0 on success and *value* appropriately filled in. -1 on failure and sets `errno` appropriately.The `errno` can be set to `EINVAL` if the semaphore identifier refers to an invalid semaphore.
Description	The `sem_getvalue( )` function updates the location referenced by the *sval* argument to have the value of the semaphore referenced by sem without affecting the state of the semaphore. The updated value represents an actual semaphore value that occurred at some unspecified time during the call, but it need not be the actual value of the semaphore when it is returned to the calling process. If sem is locked, then the object to which *sval* points is set to a negative number whose absolute value represents the number of processes waiting for the semaphore at some unspecified time during the call.
Includes	`xmk.h, semaphore.h`

`int` **`sem_wait`**`(sem_t*` *`sem`*`)`

Parameters	*sem* is the semaphore identifier.
Returns	0 on success and the semaphore in a locked state. -1 on failure and `errno` is set appropriately. The `errno` can be set to: • `EINVAL` if the semaphore identifier is invalid. • `EIDRM` if the semaphore was forcibly removed.
Description	The `sem_wait( )` function locks the semaphore referenced by *sem* by performing a semaphore lock operation on that semaphore. If the semaphore value is currently zero, then the calling thread does not return from the call to `sem_wait( )` until it either locks the semaphore or the semaphore is forcibly destroyed. Upon successful return, the state of the semaphore is locked and remains locked until the `sem_post( )` function is executed and returns successfully. ***Note:*** When a process is unblocked within the `sem_wait` call, where it blocked due to unavailability of the semaphore, the semaphore might have been destroyed forcibly. In such a case, -1 is returned. Semaphores might be forcibly destroyed due to destroying message queues that use semaphores internally. No deadlock detection is provided.
Includes	`xmk.h, semaphore.h`

`int` **`sem_trywait`**`(sem_t*` *`sem`*`)`

Parameters	*sem* is the semaphore identifier.
Returns	0 on success. -1 on failure and *errno* is set appropriately. The *errno* can be set to: • `EINVAL` if the semaphore identifier is invalid. • `EAGAIN` if the semaphore could not be locked immediately.
Description	The `sem_trywait( )` function locks the semaphore referenced by *sem* only if the semaphore is currently not locked; that is, if the semaphore value is currently positive. Otherwise, it does not lock the semaphore and returns -1.
Includes	`xmk.h, semaphore.h`

`int` **`sem_timedwait`**`(sem_t*` *`sem`*`, unsigned` *`ms`*`)`

Parameters

`sem` is the semaphore identifier.

Returns

0 on success and the semaphore in a locked state.

-1 on failure and *`errno`* is set appropriately. The *`errno`* can be set to:

- `EINVAL` - If the semaphore identifier does not refer to a valid semaphore.
- `ETIMEDOUT` - The semaphore could not be locked before the specified timeout expired.
- `EIDRM` - If the semaphore was forcibly removed from the system.

Description

The `sem_timedwait( )` function locks the semaphore referenced by *`sem`* by performing a semaphore lock operation on that semaphore. If the semaphore value is currently zero, then the calling thread does not return from the call to `sem_timedwait( )` until one of the following conditions occurs:

- It locks the semaphore.
- The semaphore is forcibly destroyed.
- The timeout specified has elapsed.

Upon successful return, the state of the semaphore is locked and remains locked until the `sem_post( )` function is executed and returns successfully.

Note: When a process is unblocked within the `sem_wait` call, where it blocked due to unavailability of the semaphore, the semaphore might have been destroyed forcibly. In such a case, -1 is returned. Semaphores maybe forcibly destroyed due to destroying message queues which internally use semaphores. No deadlock detection is provided.

Note: This routine depends on software timers support being present in the kernel and is defined only if `CONFIG_TIME` is true.

Note: This routine is slightly different from the POSIX equivalent. The POSIX version specifies the timeout as absolute wall-clock time. Because there is no concept of absolute time in Xilkernel, we use relative time specified in milliseconds.

Includes

`xmk.h, semaphore.h`

`sem_t* sem_open(const char* name, int oflag,...)`

Parameters

name points to a string naming a semaphore object.

oflag is the flag that controls the semaphore creation.

Returns

A pointer to the created/existing semaphore identifier.

SEM_FAILED on failures and when *errno* is set appropriately. The *errno* can be set to:

- ENOSPC - If the system is out of resources to create a new semaphore (or mapping).
- EEXIST - if O_EXCL has been requested and the named semaphore already exists.
- EINVAL - if the parameters are invalid.

Description

The sem_open( ) function establishes a connection between a named semaphore and a process. Following a call to sem_open( ) with semaphore *name*, the process can reference the semaphore associated with name using the address returned from the call. This semaphore can be used in subsequent calls to sem_wait( ), sem_trywait( ), sem_post( ), and sem_close( ). The semaphore remains usable by this process until the semaphore is closed by a successful call to sem_close( ). The *oflag* argument controls whether the semaphore is created or merely accessed by the call to sem_open( ). The bits that can be set in *oflag* are:

- O_CREAT
  Used to create a semaphore if it does not already exist. If O_CREAT is set and the semaphore already exists, then O_CREAT has no effect, except as noted under O_EXCL. Otherwise, sem_open( ) creates a named semaphore. O_CREAT requires a third and a fourth argument: *mode*, which is of type mode_t, and *value*, which is of type unsigned.
- O_EXCL
  If O_EXCL and O_CREAT are set, sem_open( ) fails if the semaphore name exists. The check for the existence of the semaphore and the creation of the semaphore if it does not exist are atomic with respect to other processes executing sem_open( ) with O_EXCL and O_CREAT set. If O_EXCL is set and O_CREAT is not set, the effect is undefined.

Note: The *mode* argument is unused currently. This interface is optional and is defined only if CONFIG_NAMED_SEMA is set to TRUE.

Note: If flags other than O_CREAT and O_EXCL are specified in the *oflag* parameter, an error is signalled.

The semaphore is created with an initial value of *value*.

After the *name* semaphore has been created by sem_open( ) with the O_CREAT flag, other processes can connect to the semaphore by calling sem_open( ) with the same value of *name*.

If a process makes multiple successful calls to sem_open( ) with the same value for name, the same semaphore address is returned for each such successful call, assuming that there have been no calls to sem_unlink( ) for this semaphore.

Includes

xmk.h, semaphore.h

`int sem_close(sem_t* sem)`

Parameters

sem is the semaphore identifier.

Returns

0 on success.

-1 on failure and sets *errno* appropriately. The *errno* can be set to:

- EINVAL - If the semaphore identifier is invalid.
- ENOTSUP - If the semaphore is currently locked and/or processes are blocked on the semaphore.

Description	The `sem_close( )` function indicates that the calling process is finished using the named semaphore *sem*. The `sem_close( )` function deallocates (that is, make available for reuse by a subsequent `sem_open( )` by this process) any system resources allocated by the system for use by this process for this semaphore. The effect of subsequent use of the semaphore indicated by *sem* by this process is undefined. The name mapping for this named semaphore is also destroyed. The call fails if the semaphore is currently locked. ***Note:*** This interface is optional and is defined only if `CONFIG_NAMED_SEMA` is true.
Includes	`xmk.h, semaphore.h`

`int` **`sem_post`**`(sem_t*` *`sem`*`)`

Parameters	*sem* is the semaphore identifier.
Returns	0 on success. -1 on failure and sets *errno* appropriately. The `errno` can be set to `EINVAL` if the semaphore identifier is invalid.
Description	The `sem_post( )` function performs an unlock operation on the semaphore referenced by the *sem* identifier. If the semaphore value resulting from this operation is positive, then no threads were blocked waiting for the semaphore to become unlocked and the semaphore value is incremented. If the value of the semaphore resulting from this operation is zero or negative, then one of the threads blocked waiting for the semaphore is allowed to return successfully from its call to `sem_wait( )`. This is either the first thread on the queue, if scheduling mode is `SCHED_RR` or, it is the highest priority thread in the queue, if scheduling mode is `SCHED_PRIO`. ***Note:*** If an unlink operation was requested on the semaphore, the post operation performs an unlink when no more processes are waiting on the semaphore.
Includes	`xmk.h, semaphore.h`

`int` **`sem_unlink`**`(const char*` *`name`*`)`

Parameters	*name* is the name that refers to the semaphore.
Returns	0 on success. -1 on failure and *errno* is set appropriately. *errno* can be set to `ENOENT` - If an entry for name cannot be located.
Description	The `sem_unlink( )` function removes the semaphore named by the string name. If the semaphore named by *name* has processes blocked on it, then `sem_unlink( )` has no immediate effect on the state of the semaphore. The destruction of the semaphore is postponed until all blocked and locking processes relinquish the semaphore. Calls to `sem_open( )` to recreate or reconnect to the semaphore refer to a new semaphore after `sem_unlink( )` is called. The `sem_unlink( )` call does not block until all references relinquish the semaphore; it returns immediately. ***Note:*** If an unlink operation had been requested on the semaphore, the unlink is performed on a post operation that sees that no more processes waiting on the semaphore. This interface is optional and is defined only if `CONFIG_NAMED_SEMA` is true.
Includes	`xmk.h, semaphore.h`

Message Queues

Xilkernel supports kernel allocated X/Open System Interface (XSI) message queues. XSI is a set of optional interfaces under POSIX. Message queues can be used as an IPC mechanism. The message queues can take in arbitrary sized messages. However, buffer memory allocation must be configured appropriately for the memory blocks required for the messages, as a part of system buffer memory allocation initialization.The number of message queue structures allocated in the kernel and the length of the message queues can be also be configured during system initialization. The message queue module is optional and can be configured in/out. Refer to "Configuring Message Queues," page 46 for more details. This module depends on the semaphore module and the dynamic buffer memory allocation module being present in the system. There is also a larger, but more powerful message queue functionality that can be configured if required. When the enhanced message queue interface is chosen, then *`malloc`* and *`free`* are used to allocate and free space for the messages. Therefore, arbitrary sized messages can be passed around without having to make sure that buffer memory allocation APIs can handle requests for arbitrary size.

Note: When using the enhanced message queue feature, you must choose your global heap size carefully, such that requests for heap memory from the message queue interfaces are satisfied without errors. You must also be aware of thread-safety issues when using `malloc( ), free ( )` in your own code. You must disable interrupts and context switches before invoking the dynamic memory allocation routines. You must follow the same rules when using any other library routines that may internally use dynamic memory allocation.

Message Queue Function Summary

The following list provides a linked summary of the message queues in Xilkernel. You can click on a function to go to the description.

int msgget(key_t key, int msgflg)
int msgctl(int msqid, int cmd, struct msqid_ds* buf)
int msgsnd(int msqid, const void *msgp, size_t msgsz, int msgflg)
ssize_t msgrcv(int msqid, void *msgp, size_t nbytes, long msgtyp, int msgflg)

Message Queue Function Descriptions

The Xilkernel message queue function descriptions are as follows:

`int` **`msgget`**`(key_t` *`key`*`, int` *`msgflg`*`)`

Parameters

`key` is a unique identifier for referring to the message queue.

`msgflg` specifies the message queue creation options.

Returns

A unique non-negative integer message queue identifier.

-1 on failure and sets *`errno`* appropriately; `errno` can be set to:

- `EEXIST` - If a message queue identifier exists for the argument key but ((`msgflg` and `IPC_CREAT`) and `msgflg & IPC_EXCL`) is non-zero.
- `ENOENT` - A message queue identifier does not exist for the argument key and (`msgflg` & `IPC_CREAT`) is 0.
- `ENOSPC` - If the message queue resources are exhausted.

Description

The `msgget( )` function returns the message queue identifier associated with the argument key. A message queue identifier, associated message queue, and data structure (see `sys/kmsg.h`), are created for the argument key if the argument key does not already have a message queue identifier associated with it, and (*`msgflg`* and `IPC_CREAT`) is non-zero.

Upon creation, the data structure associated with the new message queue identifier is initialized as follows:

- `msg_qnum, msg_lspid, msg_lrpid` are set equal to 0.
- `msg_qbytes` is set equal to the system limit (`MSGQ_MAX_BYTES`).

The `msgget( )` function fails if a message queue identifier exists for the argument key but ((*`msgflg`* and `IPC_CREAT`) and (*`msgflg`* & `IPC_EXCL`)) is non-zero.

`IPC_PRIVATE` is not supported. Also, messages in the message queue are not required to be of the form shown below. There is no support for message type based message receives and sends in this implementation.

The following is an example code snippet:

```
struct mymsg {
  long mtype; /* Message type. */
  char mtext[some_size]; /* Message text. */
  }
```

Includes

`xmk.h, sys/msg.h, sys/ipc.h`

`int` **`msgctl`**`(int` *`msqid`*`, int` *`cmd`*`, struct msqid_ds*` *`buf`*`)`

Parameters	*`msqid`* is the message queue identifier. *`cmd`* is the command. *`buf`* is the data buffer
Returns	0 on success. Status is returned in *`buf`* for `IPC_STAT`. -1 on failure and sets `errno` appropriately. The *`errno`* can be set to `EINVAL` if any of the following conditions occur: • *`msgid`* parameter refers to an invalid message queue. • *`cmd`* is invalid. • *`buf`* contains invalid parameters.
Description	The `msgctl( )` function provides message control operations as specified by *`cmd`*. The values for *`cmd`*, and the message control operations they specify, are: • `IPC_STAT` **-** Places the current value of each member of the msqid_ds data structure associated with msqid into the structure pointed to by `buf`. The contents of this structure are defined in `sys/msg.h`. • `IPC_SET` - Unsupported. • `IPC_RMID` - Removes the message queue identifier specified by *`msqid`* from the system and destroys the message queue and associated `msqid_ds` data structure. The remove operation forcibly destroys the semaphores used internally and unblocks processes that are blocked on the semaphore. It also deallocates memory allocated for the messages in the queue.
Includes	`xmk.h, sys/msg.h, sys/ipc.h`

`int` **`msgsnd`**`(int` *`msqid`*`, const void *`*`msgp`*`, size_t` *`msgsz`*`, int` *`msgflg`*`)`

Parameters	*`msqid`* is the message queue identifier. *`msgp`* is a pointer to the message buffer. *`msgsz`* is the size of the message. *`msgflg`* is used to specify message send options.
Returns	0 on success. -1 on failure and sets *`errno`* appropriately. The *`errno`* can be set to: • `EINVAL` - The value of msgid is not a valid message queue identifier. • `ENOSPC` - The system could not allocate space for the message. • `EIDRM` - The message queue was removed from the system during the send operation.

Description	The `msgsnd( )` function sends a message to the queue associated with the message queue identifier specified by `msqid`.
	The argument *`msgflg`* specifies the action to be taken if the message queue is full:
	If (*`msgflg`* and `IPC_NOWAIT`) is non-zero, the message is not sent and the calling thread returns immediately.
	If (*`msgflg`* and `IPC_NOWAIT`) is 0, the calling thread suspends execution until one of the following occurs:
	• The condition responsible for the suspension no longer exists, in which case the message is sent.
	• The message queue identifier msqid is removed from the system; when this occurs a -1 is returned.
	The send fails if it is unable to allocate memory to store the message inside the kernel. On a successful send operation, the *`msg_lspid`* and *`msg_qnum`* members of the message queues are appropriately set.

Includes	`xmk.h, sys/msg.h, sys/ipc.h`

`ssize_t` **`msgrcv`**`(int` *`msqid`*`, void *`*`msgp`*`, size_t` *`nbytes`*`, long` *`msgtyp`*`, int` *`msgflg`*`)`

Parameters

`msqid` is the message queue identifier.

`msgp` is the buffer where the received message is to be copied.

`nbytes` specifies the size of the message that the buffer can hold.

`msgtyp` is currently unsupported.

`msgflg` is used to control the message receive operation.

Returns

On success, stores received message in user buffer and returns number of bytes of data received.

-1 on failure and sets *`errno`* appropriately. The *`errno`* can be set to:

- `EINVAL` - If msgid is not a valid message queue identifier.
- `EIDRM` - If the message queue was removed from the system.
- `ENOMSG` - `msgsz` is smaller than the size of the message in the queue.

Description

The `msgrcv( )` function reads a message from the queue associated with the message queue identifier specified by *`msqid`* and places it in the user-defined buffer pointed to by *`msgp`*.

The argument *`msgsz`* specifies the size in bytes of the message. The received message is truncated to *`msgsz`* bytes if it is larger than *`msgsz`* and (*`msgflg`* and `MSG_NOERROR`) is non-zero. The truncated part of the message is lost and no indication of the truncation is given to the calling process. If `MSG_NOERROR` is not specified and the received message is larger than *`nbytes`*, then a -1 is returned signalling error.

The argument *`msgflg`* specifies the action to be taken if a message is not on the queue. These are as follows:

- If (*`msgflg`* and `IPC_NOWAIT`) is non-zero, the calling thread returns immediately with a return value of -1.
- If (*`msgflg`* and `IPC_NOWAIT`) is 0, the calling thread suspends execution until one of the following occurs:
  - A message is placed on the queue
  - The message queue identifier *`msqid`* is removed from the system; when this occurs -1 is returned

Upon successful completion, the following actions are taken with respect to the data structure associated with *`msqid`*:

- *`msg_qnum`* is decremented by 1.
- *`msg_lrpid`* is set equal to the process ID of the calling process.

Includes

`xmk.h, sys/msg.h, sys/ipc.h`

Shared Memory

Xilkernel supports kernel-allocated XSI shared memory. XSI is the X/Open System Interface which is a set of optional interfaces under POSIX. Shared memory is a common, low-latency IPC mechanism. Shared memory blocks required during run-time must be identified and specified during the system configuration. From this specification, buffer memory is allocated to each shared memory region. Shared memory is currently not allocated dynamically at run-time. This module is optional and can be configured in or out during system specification. Refer to "Configuring Shared Memory," page 47 for more details.

Shared Memory Function Summary

The following list provides a linked summary of the shared memory functions in Xilkernel. You can click on a function to go to the description.

int shmget(key_t key, size_t size, int shmflg)
int shmctl(int shmid, int cmd, struct shmid_ds *buf)
void* shmat(int shmid, const void *shmaddr, int flag)
int shm_dt(void *shmaddr)

Shared Memory Function Descriptions

The Xilkernel shared memory interface is described below.

> ***Caution!*** The memory buffers allocated by the shared memory API might not be aligned at word boundaries. Therefore, structures should not be arbitrarily mapped to shared memory segments, without checking if alignment requirements are met.

`int` **`shmget`**`(key_t` *`key`*`, size_t` *`size`*`, int` *`shmflg`*`)`

Parameters

`key` is used to uniquely identify the shared memory region.

`size` is the requested size of the shared memory segment.

`shmflg` specifies segment creation options.

Returns

Unique non-negative shared memory identifier on success.

-1 on failure and sets *`errno`* appropriately: *`errno`* can be set to:

- `EEXIST` - A shared memory identifier exists for the argument key but (*`shmflg`* and `IPC_CREAT`) and (*`shmflg`* and `IPC_EXCL`) is non-zero.
- `ENOTSUP` - Unsupported *`shmflg.`*
- `ENOENT` - A shared memory identifier does not exist for the argument key and (*`shmflg`* and `IPC_CREAT`) is 0.

Description

The `shmget( )` function returns the shared memory identifier associated with key. A shared memory identifier, associated data structure, and shared memory segment of at least size bytes (see `sys/shm.h`) are created for key if one of the following is true:

- *`key`* is equal to `IPC_PRIVATE`.
- *`key`* does not already have a shared memory identifier associated with it and (*`shmflg`* and `IPC_CREAT`) is non-zero.

Upon creation, the data structure associated with the new shared memory identifier shall be initialized.The value of *`shm_segsz`* is set equal to the value of size. The values of *`shm_lpid`*, *`shm_nattch`*, *`shm_cpid`* are all initialized appropriately. When the shared memory segment is created, it is initialized with all zero values. At least one of the shared memory segments available in the system must match *exactly* the requested size for the call to succeed. Key `IPC_PRIVATE` is not supported.

Includes

`xmk.h, sys/shm.h, sys/ipc.h`

`int` **`shmctl`**`(int` *`shmid`*`, int` *`cmd`*`, struct shmid_ds *`*`buf`*`)`

Parameters

`shmid` is the shared memory segment identifier.

`cmd` is the command to the control function.

`buf` is the buffer where the status is returned.

Returns

0 on success. Status is returned in buffer for `IPC_STAT`.

-1 on failure and sets *`errno`* appropriately: *`errno`* can be set to EINVAL on the following conditions:

- if *`shmid`* refers to an invalid shared memory segment.
- if *`cmd`* or other params are invalid.

Description

The `shmctl( )` function provides a variety of shared memory control operations as specified by `cmd`. The following values for *`cmd`* are available:

- `IPC_STAT`**:** places the current value of each member of the shmid_ds data structure associated with shmid into the structure pointed to by buf. The contents of the structure are defined in `sys/shm.h`.
- `IPC_SET` is not supported.
- `IPC_RMID`: removes the shared memory identifier specified by *`shmid`* from the system and destroys the shared memory segment and shmid_ds data structure associated with it. No notification is sent to processes still attached to the segment.

Includes

`xmk.h, sys/shm.h, sys/ipc.h`

`void* shmat(int shmid, const void *shmaddr, int flag)`

Parameters	*shmid* is the shared memory segment identifier. *shmaddr* is used to specify the location, to attach shared memory segment. This is currently unused. *flag* is used to specify shared memory (SHM) attach options.
Returns	The start address of the shared memory segment on success. NULL on failure and sets *errno* appropriately. *errno* can be set to EINVAL if *shmid* refers to an invalid shared memory segment
Description	shmat( ) increments the value of *shm_nattch* in the data structure associated with the shared memory ID of the attached shared memory segment and returns the start address of the segment. shm_lpid is also appropriately set. ***Note:*** *shmaddr* and *flag* arguments are not used.
Includes	xmk.h, sys/shm.h, sys/ipc.h

`int shm_dt(void *shmaddr)`

Parameters	*shmaddr* is the shared memory segment address that is to be detached.
Returns	0 on success. -1 on failure and sets errno appropriately. The errno can be set to EINVAL if shmaddr is not within any of the available shared memory segments.
Description	The shmdt( ) function detaches the shared memory segment located at the address specified by *shmaddr* from the address space of the calling process. The value of *shm_nattch* is also decremented. The memory segment is not removed from the system and can be attached to again.
Includes	xmk.h, sys/shm.h, sys/ipc.h

Mutex Locks

Xilkernel provides support for kernel allocated POSIX thread mutex locks. This synchronization mechanism can be used alongside of the *pthread_* API. The number of mutex locks and the length of the mutex lock wait queue can be configured during system specification. PTHREAD_MUTEX_DEFAULT and PTHREAD_MUTEX_RECURSIVE type mutex locks are supported. This module is also optional and can be configured in or out during system specification. Refer to "Configuring Shared Memory," page 47 for more details.

Mutex Lock Function Summary

The following list provides a linked summary of the Mutex locks in Xilkernel. You can click on a function to go to the description.

int pthread_mutex_init(pthread_mutex_t* mutex, const pthread_mutexattr_t* attr)
int pthread_mutex_destroy(pthread_mutex_t* mutex)
int pthread_mutex_lock(pthread_mutex_t* mutex)
int pthread_mutex_trylock(pthread_mutex_t* mutex)
int pthread_mutex_unlock(pthread_mutex_t* mutex)
int pthread_mutexattr_init(pthread_mutexattr_t* attr)
int pthread_mutexattr_destroy(pthread_mutexattr_t* attr)
int pthread_mutexattr_settype(pthread_mutexattr_t* attr, int type)
int pthread_mutexattr_gettype(pthread_mutexattr_t* attr, int *type)

Mutex Lock Function Descriptions

The Mutex lock function descriptions are as follows:

`int` **`pthread_mutex_init`**`(pthread_mutex_t*` ***`mutex`***`, const pthread_mutexattr_t*` ***`attr`***`)`

Parameters	*mutex* is the location where the newly created mutex lock's identifier is to be stored. *attr* is the mutex creation attributes structure.
Returns	0 on success and mutex identifier in **mutex*. EAGAIN if system is out of resources.
Description	The pthread_mutex_init( ) function initializes the mutex referenced by *mutex* with attributes specified by *attr*. If *attr* is NULL, the default mutex attributes are used; the effect is the same as passing the address of a default mutex attributes object. Refer to the pthread_mutexattr_ routines, which are documented starting on page 32 to determine what kind of mutex creation attributes can be changed. Upon successful initialization, the state of the mutex becomes initialized and unlocked. Only the mutex itself can be used for performing synchronization. The result of referring to copies of mutex in calls to pthread_mutex_lock( ), pthread_mutex_trylock( ),pthread_mutex_unlock( ),and pthread_mutex_destroy( ) is undefined. Attempting to initialize an already initialized mutex results in undefined behavior. In cases where default mutex attributes are appropriate, the macro PTHREAD_MUTEX_INITIALIZER can be used to initialize mutexes that are statically allocated. The effect is equivalent to dynamic initialization by a call to pthread_mutex_init( ) with parameter *attr* specified as NULL, with the exception that no error checks are performed. For example: `static pthread_mutex_t foo_mutex = PTHREAD_MUTEX_INITIALIZER;`
Includes	xmk.h, pthread.h

Note: The mutex locks allocated by Xilkernel follow the semantics of PTHREAD_MUTEX_DEFAULT mutex locks by default. The following actions will result in undefined behavior:

- Attempting to recursively lock the mutex.
- Attempting to unlock the mutex if it was not locked by the calling thread.
- Attempting to unlock the mutex if it is not locked.

`int` **`pthread_mutex_destroy`**`(pthread_mutex_t*` ***`mutex`***`)`

Parameters	*`mutex`* is the mutex identifier.
Returns	0 on success. `EINVAL` if *`mutex`* refers to an invalid identifier.
Description	The `pthread_mutex_destroy( )` function destroys the mutex object referenced by *`mutex;`* the mutex object becomes, in effect, uninitialized. A destroyed mutex object can be reinitialized using `pthread_mutex_init( )`; the results of otherwise referencing the object after it has been destroyed are undefined. ***Note:*** Mutex lock/unlock state disregarded during destroy. No consideration is given for waiting processes.
Includes	`xmk.h, pthread.h`

`int` **`pthread_mutex_lock`**`(pthread_mutex_t*` ***`mutex`***`)`

Parameters	*`mutex`* is the mutex identifier.
Returns	0 on success and mutex in a locked state. `EINVAL` on invalid *`mutex`* reference. -1 on unhandled errors.
Description	The mutex object referenced by *`mutex`* is locked by the thread calling `pthread_mutex_lock( )`. If the mutex is already locked, the calling thread blocks until the mutex becomes available. If the mutex type is `PTHREAD_MUTEX_RECURSIVE`, then the mutex maintains the concept of a lock count. When a thread successfully acquires a mutex for the first time, the lock count is set to one. Every time a thread relocks this mutex, the lock count is incremented by one. Each time the thread unlocks the mutex, the lock count is decremented by one. If the mutex type is `PTHREAD_MUTEX_DEFAULT`, attempting to recursively lock the mutex results in undefined behavior. If successful, this operation returns with the mutex object referenced by mutex in the locked state.
Includes	`xmk.h, pthread.h`

int **pthread_mutex_trylock**(pthread_mutex_t* *mutex*)

Parameters	*mutex* is the mutex identifier.
Returns	0 on success. *mutex* in a locked state. EINVAL on invalid *mutex* reference, EBUSY if *mutex* is already locked. -1 on unhandled errors.
Description	The mutex object referenced by *mutex* is locked by the thread calling pthread_mutex_trlock( ). If the mutex is already locked, the calling thread returns immediately with EBUSY. If the mutex type is PTHREAD_MUTEX_RECURSIVE, then the mutex maintains the concept of a lock count. When a thread successfully acquires a mutex for the first time, the lock count is set to one. Every time a thread relocks this mutex, the lock count is incremented by one. Each time the thread unlocks the mutex, the lock count is decremented by one. If the mutex type is PTHREAD_MUTEX_DEFAULT, attempting to recursively lock the mutex results in undefined behavior. If successful, this operation returns with the mutex object referenced by mutex in the locked state.
Includes	xmk.h, pthread.h

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int **pthread_mutex_unlock**(pthread_mutex_t* *mutex*)

Parameters	*mutex* is the mutex identifier.
Returns	0 on success, EINVAL on invalid mutex reference. -1 on undefined errors.
Description	The pthread_mutex_unlock( ) function releases the mutex object referenced by *mutex*. If there are threads blocked on the mutex object referenced by *mutex* when pthread_mutex_unlock( ) is called, resulting in the mutex becoming available, the scheduling policy determines which thread will acquire the mutex. If it is SCHED_RR, then the thread that is at the head of the mutex wait queue is unblocked and allowed to lock the mutex. If the mutex type is PTHREAD_MUTEX_RECURSIVE, the mutex maintains the concept of a lock count. When the lock count reaches zero, the mutex becomes available for other threads to acquire. If a thread attempts to unlock a mutex that it has not locked or a mutex which is unlocked, an error is returned. If the mutex type is PTHREAD_MUTEX_DEFAULT the following actions result in undefined behavior: • Attempting to unlock the mutex if it was not locked by the calling thread. • Attempting to unlock the mutex if it is not locked. If successful, this operation returns with the mutex object referenced by *mutex* in the unlocked state.
Includes	xmk.h, pthread.h

`int` **`pthread_mutexattr_init`**`(pthread_mutexattr_t*` ***`attr`***`)`

Parameters	***`attr`*** is the location of the attributes structure.
Returns	0 on success. `EINVAL` if ***`attr`*** refers to an invalid location.
Description	The `pthread_mutexattr_init( )` function initializes a mutex attributes object ***`attr`*** with the default value for all of the attributes defined by the implementation. Refer to `sys/types.h` for the contents of the `pthread_mutexattr` structure. ***Note:*** This routine does not involve a call into the kernel.
Includes	`xmk.h, pthread.h`

`int` **`pthread_mutexattr_destroy`**`(pthread_mutexattr_t*` ***`attr`***`)`

Parameters	***`attr`*** is the location of the attributes structure.
Returns	0 on success. `EINVAL` if ***`attr`*** refers to an invalid location.
Description	The `pthread_mutexattr_destroy( )` function destroys a mutex attributes object; the object becomes, in effect, uninitialized. ***Note:*** This routine does not involve a call into the kernel.
Includes	`xmk.h, pthread.h`

`int` **`pthread_mutexattr_settype`**`(pthread_mutexattr_t*` ***`attr`***`, int` ***`type`***`)`

Parameters	***`attr`*** is the location of the attributes structure. ***`type`*** is the type to which to set the mutex.
Returns	0 on success. `EINVAL` if ***`attr`*** refers to an invalid location or if ***`type`*** is an unsupported type.
Description	The `pthread_mutexattr_settype( )` function sets the type of a mutex in a mutex attributes structure to the specified type. Only `PTHREAD_MUTEX_DEFAULT` and `PTHREAD_MUTEX_RECURSIVE` are supported. ***Note:*** This routine does not involve a call into the kernel.
Includes	`xmk.h, pthread.h`

`int` **`pthread_mutexattr_gettype`**`(pthread_mutexattr_t*` *`attr`*`, int *`*`type`*`)`

Parameters	*attr* is the location of the attributes structure. *type* is a pointer to the location at which to store the mutex.
Returns	0 on success. EINVAL if *attr* refers to an invalid location.
Description	The pthread_mutexattr_gettype( ) function gets the type of a mutex in a mutex attributes structure and stores it in the location pointed to by *type*.
Includes	xmk.h, pthread.h

Dynamic Buffer Memory Management

The kernel provides a buffer memory allocation scheme, which can be used by applications that need dynamic memory allocation. These interfaces are alternatives to the standard C memory allocation routines - malloc( ), free( ) which are much slower and bigger, though more powerful. The allocation routines hand off pieces of memory from a pool of memory that the user passes to the buffer memory manager.

The buffer memory manager manages the pool of memory. You can dynamically create new pools of memory. You can also statically specify the different memory blocks sizes and number of such memory blocks required for your applications. Refer to "Configuring Buffer Memory Allocation," page 47 for more details. This method of buffer management is relatively simple, small and a fast way of allocating memory. The following are the buffer memory allocation interfaces. This module is optional and can be included during system initialization.

Dynamic Buffer Memory Management Function Summary

The following list provides a linked summary of the dynamic buffer memory management functions in Xilkernel. You can click on a function to go to the description.

int bufcreate(membuf_t *mbuf, void *memptr, int nblks, size_t blksiz)
int bufdestroy(membuf_t mbuf)
void* bufmalloc(membuf_t mbuf, size_t siz)
void buffree(membuf_t mbuf, void* mem)

> ***Caution!*** The buffer memory allocation API internally uses the memory pool handed down the by the user to store a free-list in-place within the memory pool. As a result, only memory sizes greater than or equal to 4 bytes long are supported by the buffer memory allocation APIs. Also, because there is a free-list being built in-place within the memory pool, requests in which memory block sizes are not multiples of 4 bytes cause unalignment at run time. If your software platform can handle unalignment natively or through exceptions then this does not present an issue. The memory buffers allocated and returned by the buffer memory allocation API might also not be aligned at word boundaries. Therefore, your application should not arbitrarily map structures to memory allocated in this way without first checking if alignment and padding requirements are met.

Dynamic Buffer Memory Management Function Descriptions

The dynamic buffer memory management function descriptions are as follows:

`int` **`bufcreate`**`(membuf_t *mbuf, void *memptr, int nblks, size_t blksiz)`

Parameters	*mbuf* is location at which to store the identifier of the memory pool created. *memptr* is the pool of memory to use. *nblks* is the number of memory blocks that this pool should support. *blksiz* is the size of each memory block in bytes.
Returns	0 on success and stores the identifier of the created memory pool in the location pointed to by *mbuf.* -1 on errors.
Description	Creates a memory pool out of the memory block specified in *memptr*. *nblks* number of chunks of memory are defined within the pool, each of size *blksiz*. Therefore, *memptr* must point to at least *(nblks * blksiz)* bytes of memory. *blksiz* must be greater than or equal to 4.
Includes	`xmk.h, sys/bufmalloc.h`

`int` **`bufdestroy`**`(membuf_t mbuf)`

Parameters	*mbuf* is the identifier of the memory pool to destroy.
Returns	0 on success. -1 on errors.
Description	This routine destroys the memory pool identified by *mbuf*.
Includes	`xmk.h, sys/bufmalloc.h`

`void*` **`bufmalloc`**`(membuf_t mbuf, size_t siz)`

Parameters	*mbuf* is the identifier of the memory pool from which to allocate memory. *size* is the size of memory block requested.
Returns	The start address of the memory block on success. `NULL` on failure and sets *errno* appropriately: *errno* is set to: • `EINVAL` if *mbuf* refers to an invalid memory buffer. • `EAGAIN` if the request cannot be satisfied.
Description	Allocate a chunk of memory from the memory pool specified by *mbuf*. If *mbuf* is `MEMBUF_ANY`, then all available memory pools are searched for the request and the first pool that has a free block of size *siz*, is used and allocated from.
Includes	`xmk.h, sys/bufmalloc.h`

`void` **`buffree`**`(membuf_t` *`mbuf`*`, void*` *`mem`*`)`

Parameters	*`mbuf`* is the identifier of the memory pool. *`mem`* is the address of the memory block.
Returns	None.
Description	Frees the memory allocated by a corresponding call to *`bufmalloc`*. If *`mbuf`* is `MEMBUF_ANY`, returns the memory to the pool that satisfied this request. If not, returns the memory to specified pool. Behavior is undefined if arbitrary values are specified for *`mem`*.
Includes	`xmk.h, sys/bufmalloc.h`

Software Timers

Xilkernel provides software timer functionality, for time relating processing. This module is optional and can be configured in or out. Refer to "Configuring Software Timers," page 48 for more information on customizing this module.

The following list provides a linked summary of the interfaces are available with the software timers module. You can click on a function to go to the description.

unsigned int xget_clock_ticks( )

`unsigned int` **`xget_clock_ticks`**`( )`

Parameters	None.
Returns	Number of kernel ticks elapsed since the kernel was started.
Description	A single tick is counted, every time the kernel timer delivers an interrupt. This is stored in a 32-bit integer and eventually overflows. The call to `xget_clock_ticks( )` returns this tick information, without conveying the overflows that have occurred.
Includes	`xmk.h, sys/timer.h`

`time_t` **`time`**`(time_t` *`*timer`*`)`

Parameters	*`timer`* points to the memory location in which to store the requested time information.
Returns	Number of seconds elapsed since the kernel was started.
Description	The routine time elapsed since kernel start in units of seconds. This is also subject to overflow.
Includes	`xmk.h, sys/timer.h`

`unsigned` **`sleep`**`(unsigned int` *`ms`*`)`

Parameters	*ms* is the number of milliseconds to sleep.
Returns	Number of seconds between sleeps. 0 on complete success.
Description	This routine causes the invoking process to enter a sleep state for the specified number of milliseconds.
Includes	`xmk.h, sys/timer.h`

Interrupt Handling

Xilkernel abstracts away primary interrupt handling requirements from the user application. Even though the kernel is functional without any interrupts, the system only makes sense when it is driven by at least one timer interrupt for scheduling. The kernel handles the main timer interrupt, using it as the kernel tick to perform scheduling. The timer interrupt is initialized and tied to the vectoring code during system initialization. This kernel pulse provides software timer facilities and time-related routines also. Additionally, Xilkernel can handle multiple interrupts when connected through an interrupt controller, and works with the `axi_intc` interrupt controller core. The following figure shows a basic interrupt service in Xilkernel.

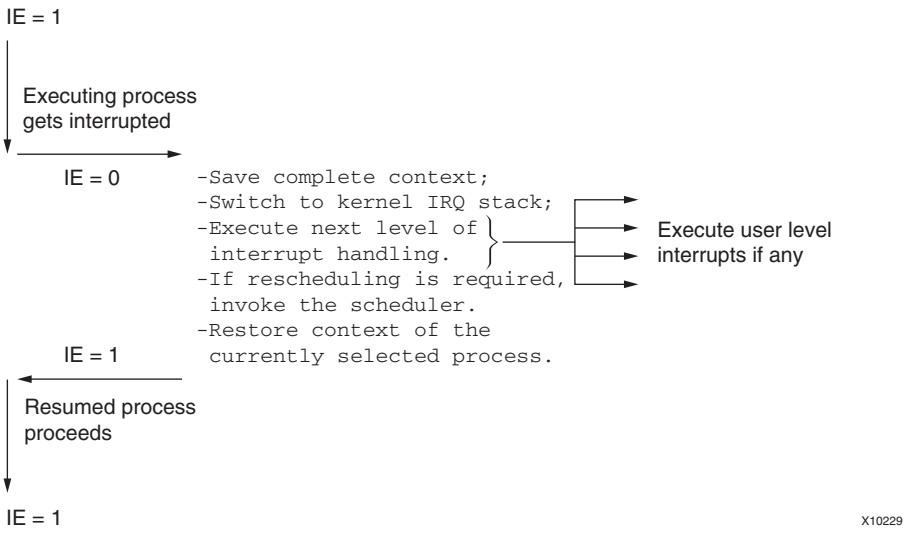

Figure 5: **Basic Interrupt Service in Xilkernel**

The interrupt handling scenario is illustrated in this diagram. Upon an interrupt:

- The context of the currently executing process is saved into the context save area.
- Interrupts are disabled from this point in time onwards, until they are enabled at the end of interrupt handling.
- This alleviates the stack burden of the process, as the execution within interrupt, does not use the user application stack.
- This interrupt context can be thought of as a special kernel thread that executes interrupt handlers in order. This thread starts to use its own separate execution stack space.
- The separate kernel execution stack is at-least 1 KB in size to enable it to handle deep levels of nesting within interrupt handlers. This kernel stack is also automatically configured to use the pthread stack size chosen by the user, if it is larger than 1 KB. If you foresee a large stack usage within your interrupt handlers, you will need to specify a large value for `pthread_stack_size`.

This ends the first level of interrupt handling by the kernel. At this point, the kernel transfers control to the second level interrupt handler. This is the main interrupt handler routine of the

interrupt controller. From this point, the handler for the interrupt controller invokes the user-specified interrupt handlers for the various interrupting peripherals.

In MicroBlaze processor kernels, if the system timer is connected through the interrupt controller, then the kernel invisibly handles the main timer interrupt (kernel tick), by registering itself as the handler for that interrupt.

Interrupt handlers can perform any kind of required interrupt handling action, including making system calls. However, the handlers must never invoke blocking system calls, or the entire kernel is blocked and the system comes to a suspended state. Use handlers wisely to do minimum processing upon interrupts.

> ***Caution!*** User level interrupt handlers must not make blocking system calls. System calls made, if any, should be non-blocking.

After the user-level interrupt handlers are serviced, the first-level interrupt handler in the kernel gets control again. It determines if the preceding interrupt handling caused a rescheduling requirement in the kernel.

If there is such a requirement, it invokes the kernel scheduler and performs the appropriate rescheduling. After the scheduler has determined the next process to execute, the context of the new process is restored and interrupts are enabled again.

When Xilkernel is used with multiple-interrupts in the system, the Xilkernel user-level interrupt handling API becomes available. The following subsection lists user-level interrupt handling APIs.

User-Level Interrupt Handling APIs

User-Level Interrupt Handling APIs Function Summary

The following list provides a linked summary of the user-level interrupt handling APIs in Xilkernel. You can click on a function to go to the description.

unsigned int register_int_handler(int_id_t id, void *handler)(void*), void *callback)
void unregister_int_handler(int_id_t id)
void enable_interrupt(int_id_t id)
void disable_interrupt(int_id_t id)
void acknowledge_interrupt(int_id_t id)

User-Level Interrupt Handling APIs Function Descriptions

The interrupt handlings API descriptions are as follows:

`unsigned int` **`register_int_handler`**`(int_id_t` *`id`*`, void *handler)(void*), void *`*`callback`*`)`

Parameters	*`id`* is the zero-based numeric id of the interrupt. *`handler`* is the user-level handler. *`callback`* is a callback value that can be delivered to the user-level handler.
Returns	`XST_SUCCESS` on success. error codes defined in `xstatus.h`.
Description	The `register_int_handler( )` function registers the specified user level interrupt handler as the handler for a specified interrupt. The user level routine is invoked asynchronously upon being serviced by an interrupt controller in the system. The routine returns an error on MicroBlaze processor systems if *`id`* is the identifier for the system timer interrupt. PowerPC processor systems have a dedicated hardware timer interrupt that exists separately from the other interrupts in the system. Therefore, this check is not performed for a PowerPC processor system.
Includes	`xmk.h, sys/intr.h`

`void` **`unregister_int_handler`**`(int_id_t` *`id`*`)`

Parameters	*`id`* is the zero-based numeric id of the interrupt.
Returns	None.
Description	The `unregister_int_handler( )` function unregisters the registered user-level interrupt handler as the handler for the specified interrupt. The routine does nothing and fails silently on MicroBlaze processor systems if *`id`* is the identifier for the system timer interrupt.
Includes	`xmk.h, sys/intr.h`

`void` **`enable_interrupt`**`(int_id_t` *`id`*`)`

Parameters	*id* is the zero-based numeric id of the interrupt.
Returns	None.
Description	The `enable_interrupt( )` function enables the specified interrupt in the interrupt controller. The routine does nothing and fails silently on MicroBlaze processor systems, if *id* is the identifier for the system timer interrupt.
Includes	`xmk.h, sys/intr.h`

`void` **`disable_interrupt`**`(int_id_t` *`id`*`)`

Parameters	*id* is the zero-based numeric id of the interrupt.
Returns	None.
Description	The `disable_interrupt( )` function disables the specified interrupt in the interrupt controller. The routine does nothing and fails silently on MicroBlaze processor systems if *id* is the identifier for the system timer interrupt.
Includes	`xmk.h, sys/intr.h`

`void` **`acknowledge_interrupt`**`(int_id_t` *`id`*`)`

Parameters	*id* is the zero-based numeric identifier of the interrupt.
Returns	None.
Description	The `acknowledge_interrupt( )` function acknowledges handling the specified interrupt to the interrupt controller. The routine does nothing and fails silently on MicroBlaze processor systems if *id* is the identifier for the system timer interrupt.
Includes	`xmk.h, sys/intr.h`

Exception Handling

Xilkernel handles exceptions for the MicroBlaze processor, treating them as faulting conditions by the executing processes/threads. Xilkernel kills the faulting process and reports using a message to the console (if verbose mode is on) as to the nature of the exception. You cannot register your own handlers for these exceptions and Xilkernel handles them all natively.

Xilkernel does *not* handle exceptions for the PowerPC processor. The exception handling API and model that is available for the Standalone platform is available for Xilkernel. You might want to register handlers or set breakpoints (during debug) for exceptions that are of interest to you.

Memory Protection

Memory protection is an extremely useful feature that can increase the robustness, reliability, and fault tolerance of your Xilkernel-based application. Memory protection requires support from the hardware. Xilkernel is designed to make use of the MicroBlaze Memory Management (Protection) Unit (MMU) features when available. This allows you to build fail-safe applications that each run within the valid sandbox of the system, as determined by the executable file and available I/O devices.

Note: Full virtual memory management is not supported by Xilkernel. Even when a full MMU is available on a MicroBlaze processor, only transparent memory translations are used, and there is no concept of demand paging.

Note: Xilkernel does not support the Memory Protection feature on PowerPC processors.

Memory Protection Overview

When the MicroBlaze parameter C_USE_MMU is set to >=2, the kernel configures in memory protection during startup automatically.

Note: To disable the memory protection in the kernel, add the compiler flag -D XILKERNEL_MB_MPU_DISABLE, to your library and application build.

The kernel identifies three types of protection violations:

1. **Code violation** — occurs when a thread tries to execute from memory that is not defined to contain program instructions.

   Note: Because Xilkernel is a single executable, all threads have access to all program instructions and the kernel cannot trap violations where a thread starts executing the kernel code directly.

2. **Data access violation** — Occurs when a thread tries to read or write data to or from memory that is not defined to be a part of the program data space. Similarly, read-only data segments can be protected by write access by all threads.

   Note: Because Xilkernel is a single executable, all threads have equal access to all data as well as the kernel data structures. The kernel cannot trap violations where a thread accesses data that it is not designated to handle.

3. **I / O violation** — occurs when a thread tries to read or write from memory-mapped peripheral I / O space that is not present in the system.

Xilkernel attempts to determine these three conceptual protection areas in your program and system during system build and kernel boot time automatically. The kernel attempts to identify code and data labels that demarcate code and data sections in your executable ELF file. These labels are typically provided by linker scripts.

For example, MicroBlaze linker scripts use the labels *_ftext* and *_etext* to indicate the beginning and the end of the .text section respectively.

The following table summarizes the logical sections that must be present in the linker script, the requirements on the alignment of each section, and the demarcating labels.

Table 1: **Linker Script Logical Sections**

Section	Start Label	End Label	Description
.text	*_ftext*	*_etext*	Executable instruction sections
.data	*_fdata*	*_edata*	Read-write data sections including small data sections
.rodata	*_frodata*	*_erodata*	Read only data sections including small data sections
.stack	*_stack_end*	*_stack*	Kernel stack with 1 KB guard page above and below
stack guard page (top)	*_fstack_guard_top*	*_estack_guard_top*	Top kernel stack guard page (1 KB)
stack guard page (bottom)	*_fstack_guard_bottom*	*_estack_guard_bottom*	Bottom kernel stack guard page (1 KB)

Each section must be aligned at 1 KB boundary and clearly demarcated by the specified labels. Otherwise, Xilkernel will ignore the missing logical sections with no error or warning message.

> ***Caution!*** This behavior could manifest itself in your software not working as expected, because MPU translation entries will be missing for important ELF sections and the processor will treat valid requests as invalid.

Note: Each section typically has a specific type of data that is expected to be present. If the logic of the data inserted into the sections by your linker script is inappropriate, then the protection offered by the kernel could be incorrect or the level of protection could be diluted.

I/O ranges are automatically enumerated by the library generation tools and provided as a data structure to the kernel. These peripheral I/O ranges will not include read/write memory areas because the access controls for memory are determined automatically from the ELF file. During kernel boot, the enumerated I/O ranges are marked as readable and writable by the threads. Accesses outside of the defined I/O ranges causes a protection fault.

User-specified Protection

In addition to the automatic inference and protection region setup done by the kernel, you can provide your own protection regions by providing the data structures as shown in the following example. If this feature is not required, these data structures can be removed from the application code.

```
#include <mpu.h>

int user_io_nranges = 2;
xilkernel_io_range_t user_io_range[1] = {{0x25004000, 0x25004fff,
MPU_PROT_READWRITE},
                {0x44000000, 0x44001fff, MPU_PROT_NONE}};
```

The `xilkernel_io_ranges_t` type is defined as follows:

```
typedef struct xilkernel_io_range_s {
    unsigned int baseaddr;
    unsigned int highaddr;
    unsigned int flags;
} xilkernel_io_range_t;
```

The following table lists the valid field flags that identify the user-specified access protection options:

Table 2: **Access Protection Field Flags**

Field Flag	Description
`MPU_PROT_EXEC`	Executable program instructions (no read or write permissions)
`MPU_PROT_READWRITE`	Readable and writable data sections (no execute permissions)
`MPU_PROT_READ`	Read-only data sections (no write/execute permissions)
`MPU_PROT_NONE`	(Currently no page can be protected from all three accesses at the same time. This field flag is equivalent to `MPU_PROT_READ`)

Fixed Unified Translation Look-aside Buffer (TLB) Support on the MicroBlaze Processor

The MicroBlaze processor has a fixed 64-entry Unified Translation Look-aside Buffer (TLB). Xilkernel can support up to this maximum number of TLBs only. If the maximum TLBs to enable protection for a given region are exceeded, Xilkernel will report an error during Microprocessor Unit (MPU) initialization and proceed to boot the kernel without memory protection. There is no support for dynamically swapping TLB management to provide an arbitrary number of protection regions.

Other Interfaces

Internally, Xilkernel, depends on the Standalone platform; consequently, the interfaces that the Standalone presents are inherited by Xilkernel. Refer to the “Standalone” document for information on available interfaces.

Hardware Requirements

Xilkernel is completely integrated with the software platform configuration and automatic library generation mechanism. As a result, a software platform based on Xilkernel can be configured and built in a matter of minutes. However, some services in the kernel require support from the hardware. Scheduling and all the dependent features require a periodic kernel tick and typically some kind of timer is used. Xilkernel has been designed to work with the `axi_timer` IP core. By specifying the instance name of the timer device in the software platform configuration, Xilkernel is able to initialize and use the timer cores and timer related services automatically. Refer to “Configuring System Timer,” page 48 for more information on how to specify the timer device.

Xilkernel has also been designed to work in scenarios involving multiple-interrupting peripherals. The `axi_intc` IP core handles the hardware interrupts and feeds a single IRQ line from the controller to the processor. By specifying the name of the interrupt controller peripheral in the software platform configuration, you would be getting kernel awareness of multiple interrupts. Xilkernel would automatically initialize the hardware cores, interrupt system, and the second level of software handlers as a part of its startup. You do not have to do this manually. Xilkernel handles non-cascaded interrupt controllers; cascaded interrupt controllers are not supported.

System Initialization

The entry point for the kernel is the `xilkernel_main( )` routine defined in `main.c`. Any user initialization that must be performed can be done before the call to `xilkernel_main( )`. This includes any system-wide features that might need to be enabled before invoking `xilkernel_main( )`. These are typically machine-state features such as cache enablement or hardware exception enablement that must be "always ON" even when context switching between applications. Make sure to set up such system states before invoking `xilkernel_main( )`. Conceptually, the `xilkernel_main( )` routine does two things: it initializes the kernel via `xilkernel_init( )` and then starts the kernel with `xilkernel_start( )`. The first action performed within `xilkernel_init( )` is kernel-specific hardware initialization. This includes registering the interrupt handlers and configuring the system timer, as well as memory protection initialization. Interrupts/exceptions are not enabled after completing `hw_init( )`. The `sys_init( )` routine is entered next.

The `sys_init( )` routine performs initialization of each module, such as processes and threads, initializing in the following order:

1. Internal process context structures
2. Ready queues
3. pthread module
4. Semaphore module
5. Message queue module
6. Shared memory module
7. Memory allocation module
8. Software timers module
9. Idle task creation
10. Static pthread creation

After these steps, `xilkernel_start( )` is invoked where interrupts and exceptions are enabled. The kernel loops infinitely in the *idle task*, enabling the scheduler to start scheduling processes.

Thread Safety and Re-Entrancy

Xilkernel, by definition, creates a multi-threaded environment. Many library and driver routines might not be written in a thread-safe or re-entrant manner. Examples include the C library routines such as `printf( )`, `sprintf( )`, `malloc( )`, `free( )`. When using any library or driver API that is not a part of Xilkernel, you must make sure to review thread-safety and re-entrancy features of the routine. One common way to prevent incorrect behavior with unsafe routines is to protect entry into the routine with locks or semaphores.

Restrictions

The MicroBlaze processor compiler supports a `-mxl-stack-check` switch, which can be used to catch stack overflows. However, this switch is meant to work only with single-threaded applications, so it cannot be used in Xilkernel.

Kernel Customization

Xilkernel is highly customizable. As described in previous sections, you can change the modules and individual parameters to suit your application. The SDK **Board Support Package Settings** dialog box provides an easy configuration method for Xilkernel parameters. Refer to the “Embedded System and Tools Architecture Overview” chapter in the *Embedded Systems Tools Reference Manual (UG111)* for more details. To customize a module in the kernel, a parameter with the name of the category set to `TRUE` must be defined in the Microprocessor Software Specification (MSS) file. An example for customizing the pthread is shown as follows:

```
parameter config_pthread_support = true
```

If you do not define a configurable *`config_`* parameter for the module, that module is not implemented. You do not have to manually key in these parameters and values. When you input information in the **Board Support Package Settings** dialog box, SDK generates the corresponding Microprocessor Software Specification (MSS) file entries automatically.

The following is an MSS file snippet for configuring OS Xilkernel for a PowerPC processor system. The values in the snippet are sample values that target a hypothetical board:

```
BEGIN OS
PARAMETER OS_NAME = xilkernel
PARAMETER OS_VER = 5.02.a
PARAMETER STDIN = RS232
PARAMETER STDOUT = RS232
PARAMETER proc_instance = microblaze0
PARAMETER config_debug_support = true
PARAMETER verbose = true
PARAMETER systmr_spec = true
PARAMETER systmr_freq = 100000000
PARAMETER systmr_interval = 80
PARAMETER sysintc_spec = system_intc
PARAMETER config_sched = true
PARAMETER sched_type = SCHED_PRIO
PARAMETER n_prio = 6
PARAMETER max_readyq = 10
PARAMETER config_pthread_support = true
PARAMETER max_pthreads = 10
PARAMETER config_sema = true
PARAMETER max_sem = 4
PARAMETER max_sem_waitq = 10
PARAMETER config_msgq = true
PARAMETER num_msgqs = 1
PARAMETER msgq_capacity = 10
PARAMETER config_bufmalloc = true
PARAMETER config_pthread_mutex = true
PARAMETER config_time = true
PARAMETER max_tmrs = 10
PARAMETER enhanced_features = true
PARAMETER config_kill = true
PARAMETER mem_table = ((4,30),(8,20))
PARAMETER static_pthread_table = ((shell_main,1))
END
```

The configuration parameters in the MSS specification impact the memory and code size of the Xilkernel image. Kernel-allocated structures whose count can be configured through the MSS must be reviewed to ensure that your memory and code size is appropriate to your design.

For example, the maximum number of process context structures allocated in the kernel is determined by the sum of two parameters; `max_procs` and `max_pthreads`. If a process context structures occupies *x* bytes of `bss` memory, then the total `bss` memory requirement for process contexts is `(max_pthreads*x)` bytes. Consequently, such parameters must be tuned carefully, and you need to examine the final kernel image with the GNU size utility to ensure that your memory requirements are met. To get an idea the contribution each kernel-allocated structure makes to memory requirements, review the corresponding header file. The specification in the MSS is translated by Libgen and Xilkernel Tcl files into C-language configuration directives in two header files: `os_config.h` and `config_init.h`. Review these two files, which are generated in the main processor include directory, to understand how the specification gets translated.

Configuring STDIN and STDOUT

The standard input and output peripherals can be configured for Xilkernel. Xilkernel can work without a standard input and output also. These peripherals are the targets of input-output APIs like `print`, `outbyte`, and `inbyte`. The following table provides the attribute descriptions, data types, and defaults.

Table 3: **STDIN/STDOUT Configuration Parameters**

Attribute	Description	Type	Defaults
`stdin`	Instance name of stdin peripheral.	string	none
`stdout`	Instance name of stdout peripheral.	string	none

Configuring Scheduling

You can configure the kernel scheduling policy by configuring the parameters shown in the following table.

Table 4: **Scheduling Parameters**

Attribute	Description	Type	Defaults
`config_sched`	Configure scheduler module.	boolean	true
`sched_type`	Type of Scheduler to be used. Allowed values: 2 - `SCHED_RR` 3 - `SCHED_PRIO`	enum	`SCHED_RR`
`n_prio`	Number of priority levels if scheduling is `SCHED_PRIO`.	numeric	32
`max_readyq`	Length of each ready queue. This is the maximum number of processes that can be active in a ready queue at any instant in time.	numeric	10

Configuring Thread Management

Threads are the primary mechanism for creating process contexts. The configurable parameters of the thread module are listed in the following table.

Table 5: **Thread Module Parameters**

Attribute	Description	Type	Defaults
`config_pthread_support`	Need pthread module.	boolean	true
`max_pthreads`	Maximum number of threads that can be allocated at any point in time.	numeric	10
`pthread_stack_size`	Stack size for dynamically created threads (in bytes).	numeric	1000

Table 5: **Thread Module Parameters *(Cont'd)***

Attribute	Description	Type	Defaults
`static_pthread_table`	Statically configure the threads that startup when the kernel is started. This is defined to be an array with each element containing the parameters `pthread_start_addr` and `pthread_prio`. ***Note:*** If you are specifying function names for `pthread_start_addr`, they must be functions in your source code that are compiled with the C dialect. They *`cannot`* be functions compiled with the C++ dialect.	array of 2-tuples	none
`pthread_start_addr`	Thread start address.	Function name (string)	none
`pthread_prio`	Thread priority.	numeric	none

Configuring Semaphores

You can configure the semaphores module, the maximum number of semaphores, and semaphore queue length. The following table shows the parameters used for configuration.

Table 6: **Semaphore Module Parameters**

Attribute	Description	Type	Defaults
`config_sema`	Need Semaphore module.	boolean	false
`max_sem`	Maximum number of Semaphores.	numeric	10
`max_sem_waitq`	Semaphore Wait Queue Length.	numeric	10
`config_named_sema`	Configure named semaphore support in the kernel.	boolean	false

Configuring Message Queues

Optionally, you can configure the message queue module, number of message queues, and the size of each message queue. The message queue module depends on both the semaphore module and the buffer memory allocation module. The following table shows the parameter definitions used for configuration. Memory for messages must be explicitly specified in the *`malloc`* customization or created at run-time.

Table 7: **Message Queue Module Parameters**

Attribute	Description	Type	Defaults
`config_msgq`	Need Message Queue module.	boolean	false
`num_msgqs`	Number of message queues in the system.	numeric	10
`msgq_capacity`	Maximum number of messages in the queue.	numeric	10
`use_malloc`	Provide for more powerful message queues which use *`malloc`* and *`free`* to allocate memory for messages.	boolean	false

Configuring Shared Memory

Optionally, you can configure the shared memory module and the size of each shared memory segment. All the shared memory segments that are needed must be specified in these parameters.The following table shows the parameters used for configuration.

Table 8: **Shared Memory Module Parameters**

Attribute	Description	Type	Defaults
config_shm	Need shared memory module.	boolean	false
shm_table	Shared memory table. Defined as an array with each element having shm_size parameter.	array of 1-tuples	none
shm_size	Shared memory size.	numeric	none
num_shm	Number of shared memories expressed as the shm_table array size.	numeric	none

Configuring Pthread Mutex Locks

Optionally, you can choose to include the pthread mutex module, number of mutex locks, and the size of the wait queue for the mutex locks. The following table shows the parameters used for configuration.

Table 9: **Pthread Mutex Module Parameters**

Attribute	Description	Type	Defaults
config_pthread_mutex	Need pthread mutex module.	boolean	false
max_pthread_mutex	Maximum number of pthread mutex locks available in the system.	numeric	10
max_pthread_mutex_ waitq	Length of each the mutex lock wait queue.	numeric	10

Configuring Buffer Memory Allocation

Optionally, you can configure the dynamic buffer memory management module, size of memory blocks, and number of memory blocks. The following table shows the parameters used for configuration.

Table 10: **Memory Management Module Parameters**

Attribute	Description	Type	Defaults
config_bufmalloc	Need buffer memory management.	boolean	false
max_bufs	Maximum number of buffer pools that can be managed at any time by the kernel.	numeric	10
mem_table	Memory block table. This is defined as an array with each element having mem_bsize, mem_nblks parameters.	array of 2-tuples	none
mem_bsize	Memory block size in bytes.	numeric	none
mem_nblks	Number of memory blocks of a size.	numeric	none

Configuring Software Timers

Optionally, you can configure the software timers module and the maximum number of timers supported. The following table shows the parameters used for configuration.

Table 11: **Software Timers Module Parameters**

Attribute	Description	Type	Defaults
config_time	Need software timers and time management module.	boolean	false
max_tmrs	Maximum number of software timers in the kernel.	numeric	10

Configuring Enhanced Interfaces

Optionally, you can configure some enhanced features/interfaces using the following parameters shown in the following table.

Table 12: **Enhanced Features**

Attribute	Description	Type	Defaults
config_kill	Include the ability to kill a process with the kill( ) function.	boolean	false
config_yield	Include the yield( ) interface.	boolean	false

Configuring System Timer

You can configure the timer device in the system for MicroBlaze processor kernels. Additionally, you can configure the timer interval for PowerPC and PIT timer based MicroBlaze processor systems. The following table shows the available parameters .

Table 13: **Attributes for Copying Kernel Source Files**

Attribute	Description	Type	Defaults
systmr_dev[1]	Instance name of the system timer peripheral.	string	none
systmr_freq	Specify the clock frequency of the system timer device. For the axi_timer, it is the frequency of the AXI bus to which the axi_timer is connected.	numeric	100000000
systmr_interval	Time interval per system timer interrupt.	numeric (milliseconds)	10

1. *MicroBlaze only.*

Configuring Interrupt Handling

You can configure the interrupt controller device in the system kernels. Adding this parameter automatically configures multiple interrupt support and the user-level interrupt handling API in the kernel. This also causes the kernel to automatically initialize the interrupt controller. The following table shows the implemented parameters.

Table 14: **Attributes for Copying Kernel Source Files**

Attribute	Description	Type	Defaults
sysintc_spec	Specify the instance name of the interrupt controller device connected to the external interrupt port.	string	null

Configuring Debug Messages

You can configure that the kernel outputs debug/diagnostic messages through its execution flow. Enabling the parameter in the following table makes the DBG_PRINT macro available, and subsequently its output to the standard output device:

Table 15: **Attribute for Debug Messages**

Attribute	Description	Type	Defaults
debug_mode	Turn on kernel debug messages.	boolean	false

Coping Kernel Source Files

You can copy the configured kernel source files to your repository for further editing and use them for building the kernel. The following table shows the implemented parameters:

Table 16: **Attributes for Copying Kernel Source Files**

Attribute	Description	Type	Defaults
copyoutfiles	Need to copy source files.	boolean	false
copytodir	User repository directory. The path is relative to *project_directory*/*system_name*/libsrc/xilkernel_v6_2/*src_dir*.	path string	"../*copyoflib*"

Debugging Xilkernel

The entire kernel image is a single file that can serve as the target for debugging with the SDK GNU Debugger (GDB) mechanism. User applications and the library must be compiled with a **-g**. Refer to the *Embedded System Tools Reference Manual (UG111)* for documentation on how to debug applications with GDB.

Note: This method of debugging involves great visibility into the kernel and is intrusive. Also, this debugging scheme is *not* kernel-user application aware.

Memory Footprint

The size of Xilkernel depends on the user configuration. It is small in size and can fit in different configurations. The following table shows the memory size output from GNU size utility for the kernel. Xilkernel has been tested with the GNU Compiler Collection (GCC) optimization flag of -O2; the numbers in the table are from the same optimization level.

Table 17: **User Configuration and Xilkernel Size**

Configuration	MicroBlaze (in kb)	PowerPC (in kb)
Basic kernel functionality with multi-threading only.	7	16
Full kernel functionality with round-robin scheduling (no multiple interrupt support and no enhanced features).	16	26
Full kernel functionality with priority scheduling (no multiple interrupt support and no enhanced features).	16.5	26.5
Full kernel functionality with all modules (threads, support for both ELF processes, priority scheduling, IPC, synchronization constructs, buffer malloc, multiple and user level interrupt handling, drivers for interrupt controller and timer, enhanced features).	22	32

Xilkernel File Organization

Xilkernel sources are organized as shown in the table below:

Table 18: **Organization of Xilkernel Sources**

`root/`				Contains the `/data` and the `/src` folders.
	`data/`			Contains Microprocessor Library Definition (MLD) and Tcl files that determine XilKernel configuration.
	`src/`			Contains all the source.
		`include/`		Contains header files organized similar to `/src`.
		`src/`		Non-header source files.
			`arch/`	Architecture-specific sources.
			`sys/`	System-level sources.
			`ipc/`	Sources that implement the IPC functionality.

Modifying Xilkernel

You can further customize Xilkernel by changing the actual code base. To work with a custom copy of Xilkernel, you must first copy the Xilkernel source folder `xilkernel_v6_2` from the SDK installation and place it in a software repository; for example, `<..../mylibraries/bsp/xilkernel_v6_2>`. If the repository path is added to the tools, Libgen picks up the source folder of Xilkernel for compilation.

Refer to "Xilkernel File Organization," page 50 for more information on the organization of the Xilkernel sources. Xilkernel sources have been written in an elementary and intuitive style and include comment blocks above each significant function. Each source file also carries a comment block indicating its role.

Deprecated Features

ELF Process Management (Deprecated)

A deprecated feature of Xilkernel is the support for creating execution contexts out of separate Executable Linked Files (ELFs).

You might do this if you need to create processes out of executable files that lay on a file system (such as XilFATFS or XilMFS). Typically, a loader is required, which Xilkernel does not provide. Assuming that your application does involve a loader, then given a entry point in memory to the executable, Xilkernel can then create a process. The kernel does not allocate a separate stack for such processes; the stack is set up as a part of the CRT of the separate executable.

Note: Such separate executable ELF files, which are designed to run on top of Xilkernel, must be compiled with the compiler flag `-xl-mode-xilkernel` for MicroBlaze processors. For PowerPC processors, you must use a custom linker script, that does not include the `.boot` and the `.vectors` sections in the final ELF image. The reason that these modifications are required is that, by default, any program compiled with the SDK GNU tool flow, could potentially contain sections that overwrite the critical interrupt, exception, and reset vectors section in memory. Xilkernel requires that its own ELF image initialize these sections and that they stay intact. Using these special compile flags and linker scripts, removes these sections from the output image for applications.

The separate executable mode has the following caveats:

- Global pointer optimization is not supported.

  Note: This is supported in the default kernel linkage mode. It is not supported only in this separate executable mode.
- Xilkernel does not feature a loader when creating new processes and threads. It creates process and thread contexts to start of from memory images assumed to be initialized. Therefore, if any ELF file depends on initialized data sections, then the next time the same memory image is used to create a process, the initialized sections are invalid, unless some external mechanism is used to reload the ELF image before creating the process.

Note: This feature is deprecated. Xilinx encourages use of the standard, single executable file application model.

Refer to the "Configuring ELF Process Management (Deprecated)," page 52 for more details. An ELF process is created and handled using the following interfaces.

`int` **`elf_process_create`**`(void* start_addr, int prio)`

Parameters	*start_addr* is the start address of the process. *prio* is the starting priority of the process in the system.
Returns	• The PID of the new process on success. • -1 on failure.
Description	Creates a new process. Allocates a new PID and Process Control Block (PCB) for the process.The process is placed in the appropriate ready queue.
Includes	`xmk.h, sys/process.h`

`int` **`elf_process_exit`**`(void)`

Parameters	None.
Returns	None.
Description	Removes the process from the system. ***Caution!*** Do not use this function to terminate a thread.
Includes	`xmk.h, sys/process.h`

Configuring ELF Process Management (Deprecated)

You can select the maximum number of processes in the system and the different functions needed to handle processes. The processes and threads that are present in the system on system startup can be configured statically. The following table provides a list of available parameters:

Table 19: **Process Management Parameters**

Attribute	Description	Type	Defaults
`config_elf_process`	Need ELF process management. ***Note:*** Using `config_elf_process` requires enhanced_features=true in the kernel configuration.	boolean	true
`max_procs`	Maximum number of processes in the system.	numeric	10
`static_elf_process_table`	Configure startup processes that are separate executable files. This is defined to be an array with each element containing the parameters `process_start` and `process_prio`.	Array of 2-tuples	none
`process_start_addr`	Process start address.	Address	none
`process_prio`	Process priority.	Numeric	none

LibXil Memory File System (MFS) (v2.2)

Overview

The LibXil MFS provides the capability to manage program memory in the form of file handles. You can create directories and have files within each directory. The file system can be accessed from the high-level C language through function calls specific to the file system.

MFS Functions

This section provides a linked summary and descriptions of MFS functions.

MFS Function Summary

The following list is a linked summary of the supported MFS functions. Descriptions of the functions are provided after the summary table. You can click on a function in the summary list to go to the description.

void mfs_init_fs(int_numbytes,_char_*address,_int init_type)
void mfs_init_genimage(int numbytes, char *address, int init_type)
int mfs_change_dir(char_*newdir)
int mfs_create_dir(char *newdir)
int mfs_delete_dir(char *dirname)
int mfs_get_current_dir_name(char *dirname)
int mfs_delete_file(char *filename)
int mfs_rename_file(char *from_file, char *to_file)
int mfs_exists_file(char *filename)
int mfs_get_usage(int *num_blocks_used, int *num_blocks_free)
int mfs_dir_open(char *dirname)
int mfs_dir_close(int fd)
int mfs_dir_read(int fd, char_**filename, int *filesize,int *filetype)
int mfs_file_open(char *filename, int mode)
int mfs_file_write(int fd, char *buf, int buflen)
int mfs_file_close(int fd)
long mfs_file_lseek(int fd, long offset, int whence)

MFS Function Descriptions

`void` **`mfs_init_fs`**`(int` *`numbytes`*`, char` *`*address`*`, int` *`init_type`*`)`

Parameters	*`numbytes`* is the number of bytes of memory available for the file system. *`address`* is the starting(base) address of the file system memory. *`init_type`* is `MFSINIT_NEW`, `MFSINIT_IMAGE`, or `MFSINIT_ROM_IMAGE`.
Description	Initialize the memory file system. This function must be called before any file system operation. Use `mfs_init_genimage` instead of this function if the filesystem is being initialized with an image generated by `mfsgen`. The status/mode parameter determines certain filesystem properties: • `MFSINIT_NEW` creates a new, empty file system for read/write. • `MFSINIT_IMAGE` initializes a filesystem whose data has been previously loaded into memory at the base address. • `MFSINIT_ROM_IMAGE` initializes a Read-Only filesystem whose data has been previously loaded into memory at the base address.
Includes	`xilmfs.h`

`void` **`mfs_init_genimage`**`(int` *`numbytes`*`, char` *`*address`*`, int` *`init_type`*`)`

Parameters	*`numbytes`* is the number of bytes of memory in the image generated by the mfsgen tool. This is equal to the size of the memory available for the file system, plus 4. *`address`* is the starting(base) address of the image. *`init_type`* is either `MFSINIT_IMAGE` or `MFSINIT_ROM_IMAGE`
Description	Initialize the memory file system with an image generated by mfsgen. This function must be called before any file system operation. The status/mode parameter determines certain filesystem properties: • `MFSINIT_IMAGE` initializes a filesystem whose data has been previously loaded into memory at the base address. • `MFSINIT_ROM_IMAGE` initializes a Read-Only filesystem whose data has been previously loaded into memory at the base address.
Includes	`xilmfs.h`

`int` **`mfs_change_dir`**`(char` *`*newdir`*`)`

Parameters	*`newdir`* is the chdir destination.
Returns	1 on success. 0 on failure.
Description	If *`newdir`* exists, make it the current directory of MFS. Current directory is not modified in case of failure.
Includes	`xilmfs.h`

`int` **`mfs_create_dir`**`(char *newdir)`

Parameters	*newdir* is the directory name to be created.
Returns	Index of new directory in the file system on success. 0 on failure.
Description	Create a new empty directory called *newdir* inside the current directory.
Includes	`xilmfs.h`

`int` **`mfs_delete_dir`**`(char *dirname)`

Parameters	*dirname* is the directory to be deleted.
Returns	Index of new directory in the file system on success. 0 on failure.
Description	Delete the directory dirname, if it exists and is empty.
Includes	`xilmfs.h`

`int` **`mfs_get_current_dir_name`**`(char *dirname)`

Parameters	*dirname* is the current directory name.
Returns	1 on success. 0 on failure.
Description	Return the name of the current directory in a preallocated buffer, *dirname,* of at least 16 chars. It does not return the absolute path name of the current directory, but just the name of the current directory.
Includes	`xilmfs.h`

`int` **`mfs_delete_file`**`(char *filename)`

Parameters	*filename* is the file to be deleted.
Returns	1 on success. 0 on failure.
Description	Delete *filename* from the directory.
Includes	`xilmfs.h`

Caution! This function does not completely free up the directory space used by the file. Repeated calls to create and delete files can cause the filesystem to run out of space.

`int` **`mfs_rename_file`**`(char *`*`from_file`*`, char *`*`to_file`*`)`

Parameters	*from_file* is the original filename. *to_file* is the new file name.
Returns	1 on success. 0 on failure.
Description	Rename *from_file* to *to_file*. Rename works for directories as well as files. Function fails if *to_file* already exists.
Includes	xilmfs.h

`int` **`mfs_exists_file`**`(char *`*`filename`*`)`

Parameters	*filename* is the file or directory to be checked for existence.
Returns	0 if *filename* does not exist. 1 if *filename* is a file. 2 if *filename* is a directory.
Description	Check if the file/directory is present in current directory.
Includes	xilmfs.h

`int` **`mfs_get_usage`**`(int *`*`num_blocks_used`*`, int *`*`num_blocks_free`*`)`

Parameters	*num_blocks_used* is the number of blocks used. *num_blocks_free* is the number of free blocks.
Returns	1 on success. 0 on failure.
Description	Get the number of used blocks and the number of free blocks in the file system through pointers.
Includes	xilmfs.h

`int` **`mfs_dir_open`**`(char *`*`dirname`*`)`

Parameters	*dirname* is the directory to be opened for reading.
Returns	The index of dirname in the array of open files on success. -1 on failure.
Description	Open directory dirname for reading. Reading a directory is done using mfs_dir_read( ).
Includes	xilmfs.h

`int` **`mfs_dir_close`**`(int fd)`

Parameters	`fd` is file descriptor return by open.
Returns	`1` on success. `0` on failure.
Description	Close the dir pointed by `fd`. The file system regains the fd and uses it for new files.
Includes	`xilmfs.h`

`int` **`mfs_dir_read`**`(int fd, char **filename, int *filesize,int *filetype)`

Parameters	`fd` is the file descriptor return by open; passed to this function by caller. `filename` is the pointer to file name at the current position in the directory in MFS; this value is filled in by this function. `filesize` is the pointer to a value filled in by this function: Size in bytes of filename, if it is a regular file; Number of directory entries if filename is a directory. `filetype` is the pointer to a value filled in by this function: `MFS_BLOCK_TYPE_FILE` if `filename` is a regular file. `MFS_BLOCK_TYPE_DIR` if `filename` is a directory.
Returns	`1` on success. `0` on failure.
Description	Read the current directory entry and advance the internal pointer to the next directory entry. `filename`, `filetype`, and `filesize` are pointers to values stored in the current directory entry.
Includes	`xilmfs.h`

`int` **`mfs_file_open`**`(char *filename, int mode)`

Parameters	`filename` is the file to be opened. `mode` is Read/Write or Create.
Returns	The index of filename in the array of open files on success. -1 on failure.
Description	Open file filename with given mode. The function should be used for files and not directories: • `MODE_READ`, no error checking is done (if file or directory). • `MODE_CREATE` creates a file and not a directory. • `MODE_WRITE` fails if the specified file is a `DIR`.
Includes	`xilmfs.h`

`int` **`mfs_file_read`**`(int fd, char *buf, int buflen)`

Parameters	*fd* is the file descriptor return by open. *buf* is the destination buffer for the read. *buflen* is the length of the buffer.
Returns	Number of bytes read on success. 0 on failure.
Description	Read *buflen* number bytes and place it in *buf*. *fd* should be a valid index in "open files" array, pointing to a file, not a directory. *buf* should be a pre-allocated buffer of size *buflen* or more. If fewer than *buflen* chars are available then only that many chars are read.
Includes	`xilmfs.h`

`int` **`mfs_file_write`**`(int fd, char *buf, int buflen)`

Parameters	*fd* is the file descriptor return by open. *buf* is the source buffer from where data is read. *buflen* is the length of the buffer.
Returns	1 on success. 0 on failure.
Description	Write *buflen* number of bytes from *buf* to the file. *fd* should be a valid index in open_files array. *buf* should be a pre-allocated buffer of size buflen or more. ***Caution!*** Writing to locations other than the end of the file is not supported. Using `mfs_file_lseek( )` go to some other location in the file then calling `mfs_file_write( )` is not supported
Includes	`xilmfs.h`

`int` **`mfs_file_close`**`(int fd)`

Parameters	*fd* is the file descriptor return by open.
Returns	1 on success. 0 on failure.
Description	Close the file pointed by *fd*. The file system regains the *fd* and uses it for new files.
Includes	`xilmfs.h`

`long` **`mfs_file_lseek`**`(int` *`fd`*`, long` *`offset`*`, int` *`whence`*`)`

Parameters	*`fd`* is the file descriptor return by open. *`offset`* is the number of bytes to seek. *`whence`* is the file system dependent mode: • `MFS_SEEK_END`, then *`offset`* can be either 0 or negative, otherwise *`offset`* is non-negative. • `MFS_SEEK_CURR`, then *`offset`* is calculated from the current location. • `MFS_SEEK_SET`, then *`offset`* is calculated from the start of the file.
Returns	Returns *`offset`* from the beginning of the file to the current location on success. `-1` on failure: the current location is not modified.
Description	Seek to a given *`offset`* within the file at location *`fd`* in open_files array. ***Caution!*** It is an error to seek before beginning of file or after the end of file. ***Caution!*** Writing to locations other than the end of the file is not supported. Using the `mfs_file_lseek( )` function or going to some other location in the file then calling `mfs_file_write( )` is not supported.
Includes	`xilmfs.h`

Utility Functions

The following subsections provide a summary and the descriptions of the utility functions that can be used along with the MFS. These functions are defined in `mfs_filesys_util.c` and are declared in `xilmfs.h`.

Utility Function Summary

The following list is a linked summary of the supported MFS Utility functions. Descriptions of the functions are provided after the summary table. You can click on a function in the summary list to go to the description.

int mfs_ls(void)
int mfs_ls_r(int recurse)
int mfs_cat(char* filename)
int mfs_copy_stdin_to_file(char *filename)
int mfs_file_copy(char *from_file, char *to_file)

Utility Function Descriptions

`int` **`mfs_ls`**`(void)`

Parameters	None.
Returns	`1` on success. `0` on failure.
Description	List contents of current directory on `STDOUT`.
Includes	`xilmfs.h`

`int` **`mfs_ls_r`**`(int` *`recurse`*`)`

Parameters	*`recurse`* controls the amount of recursion: • `0` lists the contents of the current directory and stop. • `> 0` lists the contents of the current directory and any subdirectories up to a depth of *`recurse`*. • `= -1` completes recursive directory listing with no limit on recursion depth.
Returns	1 on success. 0 on failure.
Description	List contents of current directory on `STDOUT`.
Includes	`xilmfs.h`

`int` **`mfs_cat`**`(char*` *`filename`*`)`

Parameters	*`filename`* is the file to be displayed.
Returns	`1` on success. `0` on failure.
Description	Print the file to `STDOUT`.
Includes	`xilmfs.h`

`int` **`mfs_copy_stdin_to_file`**`(char *`*`filename`*`)`

Parameters	*`filename`* is the destination file.
Returns	1 on success. 0 on failure.
Description	Copy from `STDIN` to named file. An end-of-file (EOF) character should be sent from `STDIN` to allow the function to return 1.
Includes	`xilmfs.h`

`int` **`mfs_file_copy`**`(char *`*`from_file`*`, char *`*`to_file`*`)`

Parameters	*from_file* is the source file. *to_file* is the destination file.
Returns	1 on success. 0 on failure.
Description	Copy *from_file* to *to_file*. Copy fails if *to_file* already exists or either from or to location cannot be opened.
Includes	xilmfs.h

Additional Utilities

The mfsgen program is provided along with the MFS library. You can use mfsgen to create an MFS memory image on a host system that can be subsequently downloaded to the embedded system memory. The mfsgen links to LibXil MFS and is compiled to run on the host machine rather than the target MicroBlaze™ or Cortex A9 processor system. Conceptually, this is similar to the familiar zip or tar programs.

An entire directory hierarchy on the host system can be copied to a local MFS file image using mfsgen. This file image can then be downloaded on to the memory of the embedded system for creating a pre-loaded file system.

Test programs are included to illustrate this process. For more information, see the readme.txt file in the utils sub-directory.

Usage: **mfsgen -{c** *filelist*| **t** | **x} vsb** *num_blocks* **f** *mfs_filename*

Specify exactly one of c, t, or x modes

c: creates an mfs file system image using the list of files specified on the command line (directories specified in this list are traversed recursively).

t: lists the files in the mfs file system image

x: extracts the mfs file system from image to host file system

v: is verbose mode

s: switches endianness

b: lists the number of blocks (*num_blocks*) which should be more than 2

- If the b option is specified, the *num_blocks* value should be specified
- If the b option is omitted, the default value of *num_blocks* is 5000
- The b option is meaningful only when used in conjunction with the c option

f: specify the host file name (*mfs_filename*) where the mfs file system image is stored

- If the f option is specified, the mfs filename should be specified
- If the f option is omitted, the default file name is filesystem.mfs

Libgen Customization

A memory file system can be integrated with a system using the following snippet in the Microprocessor Software Specification (MSS) file.

```
BEGIN LIBRARY
  parameter LIBRARY_NAME = xilmfs
  parameter LIBRARY_VER = 2.0
  parameter numbytes= 50000
  parameter base_address = 0xffe00000
  parameter init_type = MFSINIT_NEW
  parameter need_utils = false
END
```

The memory file system must be instantiated with the name **xilmfs**. The following table lists the attributes used by Libgen.

Table 1: **Attributes for Including Memory File System**

Attributes	Description
`numbytes`	Number of bytes allocated for file system.
`base_address`	Starting address for file system memory.
`init_type`	Options are: • `MFSINIT_NEW` (default) creates a new, empty file system. • `MFSINIT_ROM_IMAGE` creates a file system based on a pre-loaded memory image loaded in memory of size *`numbytes`* at starting address *`base_address.`* This memory is considered read-only and modification of the file system is not allowed. • `MFS_INIT_IMAGE` is similar to the previous option except that the file system can be modified, and the memory is readable and writable.
`need_utils`	true or false (default = false) If true, this causes `stdio.h` to be included from `mfs_config.h`. The functions described in "Utility Functions," page 7 require that you have defined `stdin` or `stdout`. Setting the `need_utils` to true causes stdio.h to be included. ***Caution!*** The underlying software and hardware platforms must support `stdin` and `stdout` peripherals for these utility functions to compile and link correctly.

LibXil Isf (v5.7)

LibXil Isf Library Overview

The LibXil Isf library:

- Allows you to Write, Read, and Erase the Serial Flash.
- Allows protection of the data stored in the Serial Flash from unwarranted modification by enabling the Sector Protection feature.
- Supports multiple instances of Serial Flash at a time, provided they are of the same device family (Atmel, Intel, STM, Winbond, SST, or Spansion) as the device family is selected at compile time.
- Allows the user application to perform Control operations on Intel, STM, Winbond, SST, and Spansion Serial Flash.
- Requires the underlying hardware platform to contain the axi_quad_spi, ps7_spi, ps7_qspi, psu_qspi or psu_spi device for accessing the Serial Flash.
- Uses the Xilinx® SPI interface drivers in interrupt-driven mode or polled mode for communicating with the Serial Flash. In interrupt mode, the user application must acknowledge any associated interrupts from the Interrupt Controller.

Additional information:

- In interrupt mode, the application is required to register a callback to the library and the library registers an internal status handler to the selected interface driver.
- When the user application requests a library operation, it is initiated and control is given back to the application. The library tracks the status of the interface transfers, and notifies the user application upon completion of the selected library operation.
- Added support in the library for SPI PS and QSPI PS. You must select one of the interfaces at compile time.
- Added support for QSPIPSU and SPIPS flash interface on Zynq® UltraScale™+ MPSoC.
- When the user application requests selection of QSPIPS interface during compilation, the QSPI PS or QSPI PSU interface, based on the hardware platform, are selected. Similarly, if the SPIPS interface is selected during compilation, SPI PS or SPI PSU interface are selected.

Supported Devices

Table 1 lists the supported Xilinx In-System Flash and external Serial Flash Memories.

Table 1: Xilinx In-System Flash and External Serial Flash Memories

Device Series	Manufacturer
AT45DB011D AT45DB021D AT45DB041D AT45DB081D AT45DB161D AT45DB321D AT45DB642D	Atmel
W25Q16 W25Q32 W25Q64 W25Q80 W25Q128 W25X10 W25X20 W25X40 W25X80 W25X16 W25X32 W25X64	Winbond
S25FL004 S25FL008 S25FL016 S25FL032 S25FL064 S25FL128 S25FL129 S25FL256 S25FL512 S70FL01G	Spansion
SST25WF080	SST
N25Q032 N25Q064 N25Q128 N25Q256 N25Q512 N25Q00AA MT25Q01 MT25Q02	Micron[1]

1. Intel, STM, and Numonyx Serial Flash devices are now a part of Serial Flash devices provided by Micron.

LibXil Isf Library APIs

This section provides a linked summary and detailed descriptions of the LibXil Isf library APIs.

API Summary

The following is a summary list of APIs provided by the LibXil Isf library. The list is linked to the API description. Click the API name to go to the description.

int XIsf_Initialize(XIsf *InstancePtr, XSpi *SpiInstPtr, u32 SlaveSelect, u8 *WritePtr)
int XIsf_GetStatus(XIsf *InstancePtr, u8 *ReadPtr)
int XIsf_GetStatusReg2(XIsf *InstancePtr, u8 *ReadPtr)
int XIsf_GetDeviceInfo(XIsf *InstancePtr, u8 *ReadPtr)
int XIsf_Read(XIsf *InstancePtr, XIsf_ReadOperation Operation, void *OpParamPtr)
int XIsf_Write(XIsf *InstancePtr, XIsf_WriteOperation Operation, void *OpParamPtr)
int XIsf_Erase(XIsf *InstancePtr, XIsf_EraseOperation Operation, u32 Address)
void XIsf_SetStatusHandler(XIsf*InstancePtr, XIsf_Iface *XIfaceInstancePtr XIsf_StatusHandler XilIsf_Handler);
int XIsf_SectorProtect(XIsf *InstancePtr, XIsf_SpOperation Operation, u8 *BufferPtr)
int XIsf_WriteEnable(XIsf *InstancePtr, u8 WriteEnable)
int XIsf_Ioctl (XIsf *InstancePtr, XIsf_IoctlOperation Operation)
int XIsf_SetSpiConfiguration(XIsf *InstancePtr, XIsf_Iface *SpiInstPtr, u32 Options, u8 PreScaler)
inline void XIsf_SetTransferMode(XIsf *InstancePtr, u8 Mode)
int XIsf_MicronFlashEnter4BAddMode(XIsf *InstancePtr)
int XIsf_MicronFlashExit4BAddMode(XIsf *InstancePtr)

LibXil Isf API Descriptions

`int` **`XIsf_Initialize`**`(XIsf *InstancePtr, XSpi *SpiInstPtr, u32 SlaveSelect, u8 *WritePtr)`

Parameters

`InstancePtr` is a pointer to the XIsf instance.

`SpiInstPtr` is a pointer to the XSpi instance to be worked on.

`SlaveSelect` is a 32-bit mask with a 1 in the bit position of the slave being selected. Only one slave can be selected at a time.

`WritePtr` is a pointer to the buffer allocated for use by the In-system and Serial Flash Library to perform any read/write operations on the Serial Flash device.

User applications must initialize the Isf library by passing the address of this buffer to the Initialization API.

For Write operations:

- A minimum of one byte and a maximum of `ISF_PAGE_SIZE` bytes can be written to the Serial Flash, through a single Write operation.
- The buffer size must be equal to the number of bytes to be written to the Serial Flash + `XISF_CMD_MAX_EXTRA_BYTES`, and must be large enough for use across the applications that use a common instance of the Serial Flash.

For Non Write operations:

- The buffer size must be equal to `XISF_CMD_MAX_EXTRA_BYTES`.

Returns

`XST_SUCCESS` upon success.

`XST_DEVICE_IS_STOPPED` if the device must be started before transferring data.

`XST_FAILURE` upon failure.

Description

The geometry of the underlying Serial Flash is determined by reading the Joint Electron Device Engineering Council (JEDEC®) Device Information and the Serial Flash Status Register.

When called, this API initializes the SPI interface with default settings. With custom settings, the user should call `XIsf_SetSpiConfiguration()` before calling this API.

Note: The `XIsf_Initialize()` API is a blocking call (for both polled mode and interrupt mode of the SPI driver). It reads the JEDEC information of the device and waits till the transfer is complete before checking if the information is valid.

Support multiple instances of Serial Flash at a time, provided they are of the same device family (either Atmel, Intel, STM, Winbond, or SST) as the device family is selected at compile time.

Includes

xilisf.h

`int` **`XIsf_GetStatus`**`(XIsf *InstancePtr, u8 *ReadPtr)`

Parameters	*InstancePtr* is a pointer to the XIsf instance. *ReadPtr* is a pointer to the memory where the Status Register content is copied.
Returns	XST_SUCCESS upon success XST_FAILURE upon failure
Description	Reads the Serial Flash Status Register. ***Note:*** The status register content is stored at the second byte pointed by the *ReadPtr*.
Includes	xilisf.h

`int` **`XIsf_GetStatusReg2`**`(XIsf *InstancePtr, u8 *ReadPtr)`

Parameters	*InstancePtr* is a pointer to the XIsf instance. *ReadPtr* is a pointer to the memory where the Status Register content is copied.
Returns	XST_SUCCESS upon success XST_FAILURE upon failure
Description	Reads the Serial Flash Status Register2. this API is valid only for Windbond (W25QXX) flash devices. ***Note:*** The status register content is stored at the second byte pointed by the *ReadPtr*.
Includes	xilisf.h

`int` **`XIsf_GetDeviceInfo`**`(XIsf *InstancePtr, u8 *ReadPtr)`

Parameters	*InstancePtr* is a pointer to the XIsf instance. *ReadPtr* is a pointer to the memory where the Device information is copied.
Returns	XST_SUCCESS upon success. XST_FAILURE upon failure.
Description	Reads the JEDEC information of the Serial Flash. ***Note:*** The Device information is stored at the second byte pointed by the *ReadPtr*.
Includes	xilisf.h

```
int XIsf_Read(XIsf *InstancePtr, XIsf_ReadOperation
   Operation, void *OpParamPtr)
```

Parameters

InstancePtr is a pointer to the XIsf instance.

Operation is the type of the read operation to be performed on the Serial Flash.

The *Operation* options are:

XISF_READ: Normal Read

XISF_FAST_READ: Fast Read

XISF_PAGE_TO_BUF_TRANS: Page to Buffer Transfer

XISF_BUFFER_READ: Buffer Read

XISF_FAST_BUFFER_READ: Fast Buffer Read

XISF_OTP_READ: One Time Programmable Area (OTP) Read.

XISF_DUAL_OP_FAST_READ: Dual Output Fast Read

XISF_DUAL_IO_FAST_READ: Dual Input/Output Fast Read

XISF_QUAD_OP_FAST_READ: Quad Output Fast Read

XISF_QUAD_IO_FAST_READ: Quad Input/Output Fast Read

OpParamPtr is the pointer to structure variable which contains operational parameter of specified Operation. This parameter type is dependent on the type of Operation to be performed.

When specifying Normal Read (XISF_READ), Fast Read (XISF_FAST_READ) and One Time Programmable Area Read(XISF_OTP_READ), Dual Output Fast Read

(XISF_DUAL_OP_FAST_READ), Dual Input/Output Fast Read

(XISF_DUAL_IO_FAST_READ), Quad Output Fast Read

(XISF_QUAD_OP_FAST_READ)and Quad Input/Output Fast Read (XISF_QUAD_IO_FAST_READ):

- *OpParamPtr* must be of type struct *XIsf_ReadParam*.
- *OpParamPtr->Address* is the start address in the Serial Flash.
- *OpParamPtr->ReadPtr* is a pointer to the memory where the data read from the Serial Flash is stored.
- *OpParamPtr->NumBytes* is number of bytes to read.
- *OpParamPtr->NumDummyBytes* is the number of dummy bytes to be transmitted for the Read command. This parameter is only used in case of Dual and Quad reads.

Normal Read and Fast Read operations are supported for Atmel, Intel, STM, Winbond, SST, and Spansion Serial Flash. Dual and quad reads are supported for Winbond (W25QXX),Micron (N25QXX) and Spansion (S25FL129) quad flash. OTP Read operation is only supported in Intel Serial Flash.

When specifying Page To Buffer Transfer (XISF_PAGE_TO_BUF_TRANS):

- *OpParamPtr* must be of type struct *XIsf_FlashToBufTransferParam*.
- *OpParamPtr->BufferNum* specifies the internal SRAM Buffer of the Serial Flash. The valid values are XISF_PAGE_BUFFER1 or XISF_PAGE_BUFFER2. XISF_PAGE_BUFFER2 is not valid in the case of AT45DB011D Flash as it contains a single buffer.
- *OpParamPtr->Address* is start address in the Serial Flash.

This operation is only supported in Atmel Serial Flash.

XIsf_Read (*continued*)

Parameters	When specifying Buffer Read (XISF_BUFFER_READ) and Fast Buffer Read (XISF_FAST_BUFFER_READ): ″ *OpParamPtr* must be of type struct *XIsf_BufferReadParam*. ″ *OpParamPtr->BufferNum* specifies the internal SRAM Buffer of the Serial Flash. The valid values are XISF_PAGE_BUFFER1 or XISF_PAGE_BUFFER2. XISF_PAGE_BUFFER2 is not valid in the case of AT45DB011D Flash as it contains a single buffer. ″ *OpParamPtr->ReadPtr* is pointer to the memory where the data read from the SRAM buffer is to be stored. ″ *OpParamPtr->ByteOffset* is byte offset in the SRAM buffer from where the first byte is read. ″ *OpParamPtr->NumBytes* is the number of bytes to be read from the Buffer. These operations are supported only in Atmel Serial Flash.
Returns	XST_SUCCESS upon success. XST_FAILURE upon failure.
Description	Reads the data from the Serial Flash. ***Note:*** Application must fill the structure elements of the third argument and pass its pointer by type casting it with void pointer. The valid data is available from the fourth location pointed to by the ReadPtr for Normal Read and Buffer Read operations. The valid data is available from the fifth location pointed to by the ReadPtr for Fast Read, Fast Buffer Read, and OTP Read operations. The valid data is available from the (4 + *NumDummyBytes*) location pointed to by ReadPtr for Dual/Quad Read operations.
Includes	xilisf.h

```
int XIsf_Write(XIsf *InstancePtr, XIsf_WriteOperation
   Operation, void *OpParamPtr)
```

Parameters

InstancePtr is a pointer to the XIsf instance.

Operation is the type of write operation to be performed on the Serial Flash.

The *Operation* options are:

- XISF_WRITE: Normal Write
- XISF_DUAL_IP_PAGE_WRITE: Dual Input Fast Program
- XISF_DUAL_IP_EXT_PAGE_WRITE: Dual Input Extended Fast Program
- XISF_QUAD_IP_PAGE_WRITE: Quad Input Fast Program
- XISF_QUAD_IP_EXT_PAGE_WRITE: Quad Input Extended Fast Program
- XISF_AUTO_PAGE_WRITE: Auto Page Write
- XISF_BUFFER_WRITE: Buffer Write
- XISF_BUF_TO_PAGE_WRITE_WITH_ERASE: Buffer to Page Transfer with Erase
- XISF_BUF_TO_PAGE_WRITE_WITHOUT_ERASE: Buffer to Page Transfer without Erase
- XISF_WRITE_STATUS_REG: Status Register Write
- XISF_WRITE_STATUS_REG2: 2 byte Status Register Write
- XISF_OTP_WRITE: OTP Write.

OpParamPtr is the pointer to a structure variable which contains operational parameters of specified operation.

This parameter type is dependant upon the value of first argument (*Operation*).

When specifying Normal Write (XISF_WRITE): Dual Input Fast Program (XISF_DUAL_IP_PAGE_WRITE), Dual Input Extended Fast Program (XISF_DUAL_IP_EXT_PAGE_WRITE), Quad Input Fast Program (XISF_QUAD_IP_PAGE_WRITE), Quad Input Extended Fast Program (XISF_QUAD_IP_EXT_PAGE_WRITE):

- *OpParamPtr* must be of type struct *XIsf_WriteParam*.
- *OpParamPtr->Address* is the start address in the Serial Flash.
- *OpParamPtr->WritePtr* is a pointer to the data to be written to the Serial Flash.
- *OpParamPtr->NumBytes* is the number of bytes to be written to the Serial Flash.

This operation is supported for Atmel, Intel, STM, Winbond, and Spansion Serial Flash.

For SST, only normal write is applicable.

When specifying the Auto Page Write (XISF_AUTO_PAGE_WRITE):

- *OpParamPtr* must be of 32 bit unsigned integer variable. This is the address of page number in the Serial Flash which is to be refreshed.

This operation is only supported in Atmel Serial Flash.

When specifying the Buffer Write (XISF_BUFFER_WRITE):

- *OpParamPtr* must be of type struct *XIsf_BufferWriteParam*.
- *OpParamPtr->BufferNum* specifies the internal SRAM Buffer of the Serial Flash. The valid values are XISF_PAGE_BUFFER1 or XISF_PAGE_BUFFER2. XISF_PAGE_BUFFER2 is not valid in the case of AT45DB011D Flash as it contains a single buffer.
- *OpParamPtr->WritePtr* is a pointer to the data to be written to the Serial Flash SRAM Buffer.
- *OpParamPtr->ByteOffset* is byte offset in the buffer from where the data is to be written.
- *OpParamPtr->NumBytes* is number of bytes to be written to the Buffer.

XIsf_Write (*continued*)

Parameters

This operation is supported only for Atmel Serial Flash.When specifying Buffer To Memory Write With Erase (XISF_BUF_TO_PAGE_WRITE_WITH_ERASE) or Buffer To Memory Write Without Erase (XISF_BUF_TO_PAGE_WRITE_WITHOUT_ERASE):

- *OpParamPtr* must be of type struct *XIsf_BufferToFlashWriteParam*.
- *OpParamPtr->BufferNum* specifies the internal SRAM Buffer of the Serial Flash. The valid values are XISF_PAGE_BUFFER1 or XISF_PAGE_BUFFER2. XISF_PAGE_BUFFER2 is not valid in the case of AT45DB011D Flash as it contains a single buffer.
- *OpParamPtr->Address* is starting address in the Serial Flash memory from where the data is to be written.

These operations are only supported in Atmel Serial Flash.

When specifying Write Status Register (XISF_WRITE_STATUS_REG), the *OpParamPtr* must be an 8-bit unsigned integer variable. This is the value to be written to the Status Register.

This operation is supported in Intel, STM, SST, and Winbond Serial Flash only.

When specifying Write 2 Byte Status Register (XISF_WRITE_STATUS_REG2), the *OpParamPtr* must be of type (u8 *) and should point to two 8 bit unsigned integer values. This is the value to be written to the 16 bit Status Register

Note: This operation is supported only in Winbond (W25QXX) Serial Flash.

When specifying One Time Programmable Area Write (XISF_OTP_WRITE):

- *OpParamPtr* must be of type struct XIsf_WriteParam.
- *OpParamPtr->Address* is the address in the SRAM Buffer of the Serial Flash to which the data is to be written.
- *OpParamPtr->WritePtr* is a pointer to the data to be written to the Serial Flash.
- *OpParamPtr->NumBytes* should be set to 1 when performing OTPWrite operation.

This operation is only supported in Intel Serial Flash.

Returns

XST_SUCCESS upon success.

XST_FAILURE upon failure.

Description

Writes data to the Serial Flash.

Note: Application must fill the structure elements of the third argument and pass its pointer by type casting it with void pointer.

For Intel, STM, Winbond, SST, and Spansion Serial Flash the user application must call the XIsf_WriteEnable() API by passing XISF_WRITE_ENABLE as an argument before calling the XIsf_Write() API.

Includes

xilisf.h

`int` **`XIsf_Erase`**`(XIsf *InstancePtr, XIsf_EraseOperation Operation, u32 Address)`

Parameters	*InstancePtr* is a pointer to the XIsf instance. *Operation* is the type of Erase operation to be performed on the Serial Flash. The different operations are ″ XISF_PAGE_ERASE: Page Erase ″ XISF_BLOCK_ERASE: Block Erase ″ XISF_SECTOR_ERASE: Sector Erase ″ XISF_BULK_ERASE: Bulk Erase ″ XISF_SUB_SECTOR_ERASE: Sub Sector Erase *Address* is the address of the Page/Block/Sector to be erased. The address can be either Page address, Block address or Sector address based on the Erase operation to be performed.
Returns	XST_SUCCESS upon success. XST_FAILURE upon failure.
Description	Erases the contents of the specified memory in the Serial Flash. ***Note:*** The erased bytes will read as 0xFF. For Intel, STM, Winbond, and Spansion Serial Flash the user application must call XIsf_WriteEnable() API by passing XISF_WRITE_ENABLE as an argument before calling the XIsf_Erase() API. Atmel, Intel, STM Winbond, Micron (N25QXX), and Spansion Serial Flash devices support Sector/Block/Bulk Erase operations. SST devices support all Erase/SubSector commands.
Includes	xilisf.h

`void` **`XIsf_SetStatusHandler`**`(XIsf*InstancePtr, XIsf_Iface *XIfaceInstancePtr XIsf_StatusHandler XilIsf_Handler);`

Parameters	*InstancePtr* is a pointer to the XIsf instance. *XIfaceInstancePtr* is a pointer to the XIsf_Iface instance to be worked on. *XilIsf_Handler* is the status handler for the application.
Returns	**None**
Description	Sets the application status handler. The library will register an internal handler to the interface driver.
Includes	xilisf.h

`int` **`XIsf_SectorProtect`**`(XIsf *InstancePtr, XIsf_SpOperation Operation, u8 *BufferPtr)`

Parameters	*InstancePtr* is a pointer to the XIsf instance. *Operation* is the type of Sector Protect operation to be performed on the Serial Flash. The Operation options are ″ XISF_SPR_READ: Read Sector Protection Register ″ XISF_SPR_WRITE: Write Sector Protection Register ″ XISF_SPR_ERASE: Erase Sector Protection Register ″ XISF_SP_ENABLE: Enable Sector Protection ″ XISF_SP_DISABLE: Disable Sector Protection *BufferPtr* is a pointer to the memory where the SPR content is read to/written from. This argument can be NULL if the Operation is SprErase, SpEnable and SpDisable.
Returns	XST_SUCCESS upon success. XST_FAILURE upon failure.
Description	Performs Sector Protect operations. ***Note:*** The SPR content is stored at the fourth location pointed by the BufferPtr when performing XISF_SPR_READ operation. For Intel, STM, Winbond, and Spansion Serial Flash devices the user application must call the XIsf_WriteEnable() API by passing XISF_WRITE_ENABLE as an argument, before calling the XIsf_SectorProtect() API, for Sector Protect Register Write (XISF_SPR_WRITE) operation. Atmel Flash supports all these Sector Protect operations. Intel, STM, Winbond, and Spansion support only Sector Protect Read and Sector Protect Write operations.
Includes	xilisf.h

`int` **`XIsf_WriteEnable`**`(XIsf *InstancePtr, u8 WriteEnable)`

Parameters	*InstancePtr* is a pointer to the XIsf instance. *WriteEnable* specifies whether to enable (XISF_WRITE_ENABLE) or disable (XISF_WRITE_DISABLE) the writes to the Serial Flash.
Returns	XST_SUCCESS upon success. XST_FAILURE upon failure.
Description	Enables/Disables writes to the Intel, STM, Winbond, SST, and Spansion Serial Flash. ***Note:*** If this API is called for Atmel Flash, XST_FAILURE is returned.
Includes	xilisf.h

`int` **`XIsf_Ioctl`** `(XIsf *InstancePtr, XIsf_IoctlOperation Operation)`

Parameters	*InstancePtr* is a pointer to the XIsf instance. *Operation* is the type of Control operation to be performed on the Serial Flash. The control Operations options are: " XISF_RELEASE_DPD: Release from Deep Power Down (DPD) Mode " XISF_ENTER_DPD: Enter DPD Mode " XISF_CLEAR_SR_FAIL_FLAGS: Clear the Status Register Fail Flags.
Returns	XST_SUCCESS upon success. XST_FAILURE upon failure.
Description	This API configures and controls the Intel, STM, Winbond, and Spansion Serial Flash. ***Note:*** Atmel Serial Flash does not support any of these operations. Intel Serial Flash support Enter/Release from DPD Mode and Clear Status Register Fail Flags. STM, Winbond, and Spansion Serial Flash support Enter/Release from DPD Mode. Winbond (W25QXX) supports Enable High performance mode.
Includes	xilisf.h

`int` **`XIsf_SetSpiConfiguration`**`(XIsf *InstancePtr, XIsf_Iface *SpiInstPtr, u32 Options, u8 PreScaler)`

Parameters	*InstancePtr* is a pointer to the XIsf instance. *SpiInstPtr* is a pointer to the XIsf_Iface instance to be worked on. *Options* contains specified options to be set. *PreScaler* is the value of the clock prescaler to set.
Returns	XST_SUCCESS upon success. XST_FAILURE upon failure.
Description	Sets the configuration of SPI. This API can be called before calling XIsf_Initialize() to operate the SPI interface in a mode other than the default options mode. *PreScaler* is only applicable to PS SPI/QSPI.
Includes	xilisf.h

`inline void` **`XIsf_SetTransferMode`**`(XIsf *InstancePtr, u8 Mode)`

Parameters	*InstancePtr* is a pointer to the XIsf instance. *Mode* is the value to be set.
Returns	None.
Description	This API sets the interrupt/polling mode of transfer. By default, the xilisf library is designed to operate in polling mode. User needs to call this API, if operating in Interrupt Mode.

`int` **`XIsf_MicronFlashEnter4BAddMode`**`(XIsf *InstancePtr)`

Parameters	*`InstancePtr`* is a pointer to the XIsf instance.
Returns	XST_SUCCESS upon success. XST_FAILURE upon failure.
Description	By default, flash is in 3B Address mode. User needs to call this API to enter the flash in the 4B Address mode.

`int` **`XIsf_MicronFlashExit4BAddMode`**`(XIsf *InstancePtr)`

Parameters	*`InstancePtr`* is a pointer to the XIsf instance.
Returns	XST_SUCCESS upon success. XST_FAILURE upon failure.
Description	User needs to call this API, if the flash is operating in the 4B address mode. Calling this API exits the flash from the 4B address mode.

Libgen Customization

The LibXil Isf library can be integrated with a system using the following snippet in the Microprocessor Software Specification (MSS) file.

```
BEGIN LIBRARY
  parameter LIBRARY_NAME = xilisf
  parameter LIBRARY_VER = 5.6
  parameter serial_flash_family = 1
  parameter serial_flash_interface = 1
END
```

Where:

- `LIBRARY_NAME`—Is the library name (`xilisf`).
- `LIBRARY_VER`—Is the library version (`5.7`).
- `serial_flash_family`—Is a numerical value representing the serial flash family, where:
  - 1 = Xilinx In-system Flash or Atmel Serial Flash
  - 2 = Intel (Numonyx) S33 Serial Flash[1]
  - 3 = STM (Numonyx) M25PXX/N25QXX Serial Flash[1]
  - 4 = Winbond Serial Flash
  - 5 = Spansion Serial Flash/Micron Serial Flash
  - 6 = SST Serial Flash
- `serial_flash_interface` - Is a numerical value representing the serial flash interface, where:
  - 1 = AXI QSPI Interface
  - 2 = SPI PS Interface
  - 3 = QSPI PS Interface or QSPI PSU Interface

Intel/STM/Numonyx serial flash devices now belong to the Micron family.

Additional Resources

- *Spartan-3AN FPGA In-System Flash User Guide* (UG333): http://www.xilinx.com/support/documentation/user_guides/ug333.pdf
- Atmel Serial Flash Memory website (AT45XXXD): http://www.atmel.com/dyn/products/devices.asp?family_id=616#1802
- Intel (Numonyx) S33 Serial Flash Memory website (S33): http://www.numonyx.com/Documents/Datasheets/314822_S33_Discrete_DS.pdf
- STM (Numonyx) M25PXX Serial Flash Memory website (M25PXX): http://www.numonyx.com/en-US/MemoryProducts/NORserial/Pages/M25PTechnicalDocuments.aspx
- Winbond Serial Flash Page: http://www.winbond-usa.com/hq/enu/ProductAndSales/ProductLines/FlashMemory/SerialFlash/
- Spansion website: http://www.spansion.com/Support/Pages/DatasheetsIndex.aspx
- SST SST25WF080: http://www.sst.com/dotAsset/40369.pdf
- Micron N25Q flash family: http://www.micron.com/products/nor-flash/serial-nor-flash/n25q#/

LibXil FFS (v3.5)

Overview

The LibXil fat file system (FFS) library consists of a file system and a glue layer. This FAT file system can be used with an interface supported in the glue layer.

The file system code is open source and is used as it is. Glue layer implementation supports SD/eMMC interface presently.

Application should make use of APIs provided in ff.h. These file system APIs access the driver functions through the glue layer.

File System Files

Table 1: **File System Files**

File	Description
`ff.c`	Implements all the file system APIs
`ff.h`	File system header
`ffconf.h`	File system configuration header – File system configurations such as READ_ONLY, MINIMAL etc. can be set here. This library uses _FS_MINIMIZE and _FS_TINY and Read/Write (NOT read only)
`Integer.h`	Contains type definitions used by file system

Glue Layer Files

Table 2: **Glue Layer Files**

File	Description
`diskio.c`	Glue layer – implements the function used by file system to call the driver APIs
`diskio.h`	Glue layer header

Choosing a File System with an SD Interface

To choose a file system with an SD interface:

1. In SDK, create a new bsp and select the xilffs library.
2. In xilffs options, set **`fs_interface = 1`** to select **`SD/eMMC`**. This is the default value. When this option is set, make sure there is an SD/eMMC interface available.
3. Build the bsp and application to use the file system with SD/eMMC.
4. SD or eMMC will be recognized by the low level driver.

Library Parameters in MSS File

The MSS file contains the following library parameters:

```
parameter LIBRARY_NAME = xilffs
parameter LIBRARY_VER = 3.4
parameter fs_interface = 1
parameter read_only = false
parameter use_lfn = false
parameter enable_multi_partition = false
parameter num_logical_vol = 2
parameter use_mkfs = true
```

- `LIBRARY_NAME:` Library name (xilffs)
- `LIBRARY_VER:` Library version (3.3)
- `fs_interface:` File system interface. Currently SD/eMMC is the only interface supported.
  - Value: “1” for SD/eMMC
  - Default value is “1”.
- `read_only`: Enables the file system in **`Read Only`** mode, if true. Default is false. Zynq® UltraScale+™ MPSoC **`fsbl`** sets this option as true.
- `use_lfn`: Enables the long file name (LFN) support, if true. Default is false.
- `enable_multi_partition`: Enables the multi partition support, if true. Default is false.
- `num_logical_vol`: Number of volumes (logical drives, from 1 to 10) to be used. Default is 2.
- `use_mkfs`: Enables the mkfs support, if true. Default is true. Zynq UltraScale+ MPSoC fsbl set this option as false.

File System

The file system supports FAT16 and FAT32. The APIs are standard file system APIs. A detailed description can be found at http://elm-chan.org/fsw/ff/00index_e.html.

Revision R0.10b is used in the library.

UG650 November 30, 2016

lwIP 1.4.1 Library (v1.7)

Overview

The lwIP is an open source TCP/IP protocol suite available under the BSD license. The lwIP is a standalone stack; there are no operating systems dependencies, although it can be used along with operating systems. The lwIP provides two A05PIs for use by applications:

- RAW API: Provides access to the core lwIP stack.
- Socket API: Provides a BSD sockets style interface to the stack.

The lwip141_v1_7 is an SDK library that is built on the open source lwIP library version 1.4.1. The lwip141_v1_7 library provides adapters for the Ethernetlite (axi_ethernetlite), the TEMAC (axi_ethernet), and the Gigabit Ethernet controller and MAC (GigE) cores. The library can run on MicroBlaze™, ARM Cortex-A9, ARM Cortex-A53, and ARM Cortex-R5 processors. The Ethernetlite and TEMAC cores apply for MicroBlaze systems. The Gigabit Ethernet controller and MAC (GigE) core is applicable only for ARM Cortex-A9 system (Zynq®-7000 processor devices) and ARM Cortex-A53 & ARM Cortex-R5 system (Zynq® UltraScale™+ MPSoC).

Features

The lwIP provides support for the following protocols:

- Internet Protocol (IP)
- Internet Control Message Protocol (ICMP)
- User Datagram Protocol (UDP)
- TCP (Transmission Control Protocol (TCP)
- Address Resolution Protocol (ARP)
- Dynamic Host Configuration Protocol (DHCP)
- Internet Group Message Protocol (IGMP)

Additional Resources

- lwIP wiki: http://lwip.scribblewiki.com
- Xilinx® lwIP designs and application examples: http://www.xilinx.com/support/documentation/application_notes/xapp1026.pdf
- lwIP examples using RAW and Socket APIs: http://savannah.nongnu.org/projects/lwip/
- FreeRTOS Port for Zynq is available for download from the FreeRTOS website: http://www.freertos.org/Interactive_Frames/Open_Frames.html?http://interactive.freertos.org/forums

Using lwIP

The following sections detail the hardware and software steps for using lwIP for networking. The key steps are:

1. Creating a hardware system containing the processor, ethernet core, and a timer. The timer and ethernet interrupts must be connected to the processor using an interrupt controller.
2. Configuring lwip141_v1_7 to be a part of the software platform. For operating with lwIP socket API, the Xilkernel library or FreeRTOS BSP is a prerequisite. See the Note below.

   Note: The Xilkernel library is available only for MicroBlaze systems. For Cortex-A9 based systems (Zynq) and Cortex-A53 or Cortex-R5 based systems (Zynq® UltraScale™+ MPSoC), there is no support for Xilkernel. Instead, use FreeRTOS. A FreeRTOS BSP is available for Zynq systems and must be included for using lwIP socket API. The FreeRTOS BSP for Zynq is available for download from:
   http://www.freertos.org/Interactive_Frames/Open_Frames.html?http://interactive.freertos.org/forums

Setting up the Hardware System

This section describes the hardware configurations supported by lwIP. The key components of the hardware system include:

- Processor: Either a MicroBlaze or a Cortex-A9 or a Cortex-A53 or a Cortex-R5 processor. The Cortex-A9 processor applies to Zynq systems. The Cortex-A53 and Cortex-R5 processors apply to Zynq® UltraScale™+ MPSoC systems.
- MAC: LwIP supports axi_ethernetlite, axi_ethernet, and Gigabit Ethernet controller and MAC (GigE) cores.
- Timer: to maintain TCP timers, lwIP raw API based applications require that certain functions are called at periodic intervals by the application. An application can do this by registering an interrupt handler with a timer.
- DMA: For axi_ethernet based systems, the axi_ethernet cores can be configured with a soft DMA engine or a fifo interface. For GigE-based Zynq and Zynq® UltraScale™+ MPSoC systems, there is a built-in DMA and so no extra configuration is needed. Same applies to axi_ethernetlite based systems, which have their built-in buffer management provisions.

Figure 1 shows a sample system architecture with a Kintex®-6 device utilizing the axi_ethernet core with DMA.

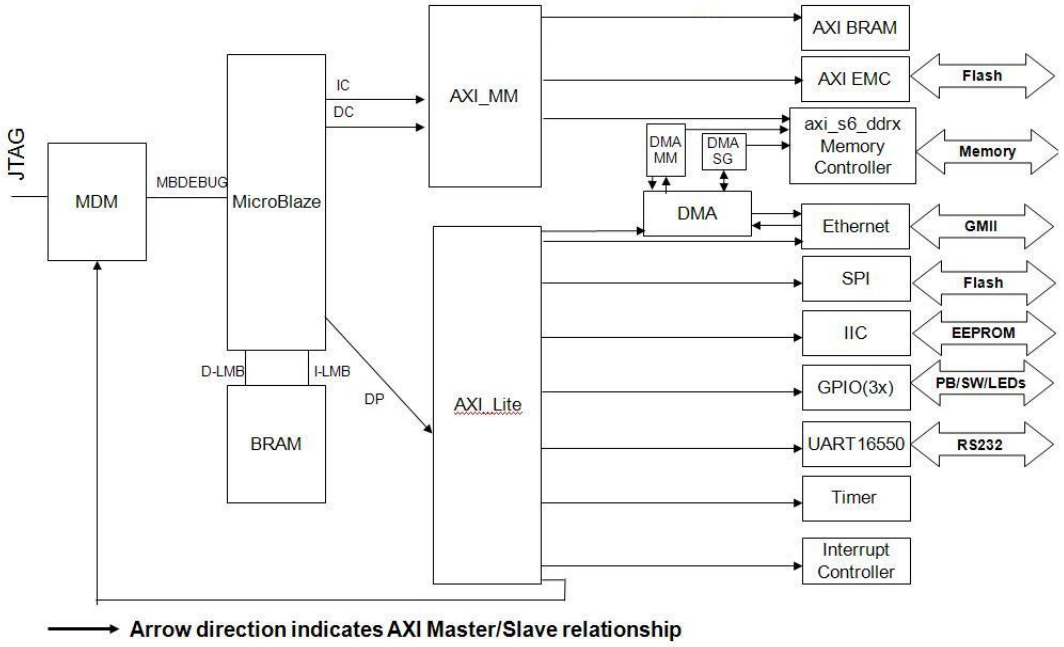

Figure 1: **System Architecture using axi_ethernet core with DMA**

Setting up the Software System

To use lwIP in a software application, you must first compile the lwIP library as part of software application.

To move the hardware design to SDK, you must first export it from the Hardware Tools.

1. Select **Project > Export Hardware Design to SDK**.
2. On the Export to SDK dialog box that opens, click **Export & Launch SDK**.

   Vivado® exports the design to SDK. SDK opens and prompts you to create a workspace.

After SDK opens with hw_platform already present in the Project Explorer, compile the lwIP library:

1. Select **File > New > Xilinx Board Support Package**.

   The New Board Support Package window opens.
2. Give the project a name and select a location for it. Select XilKernel, Standalone, or FreeRTOS, and click **Finish**.

   Note: For Zynq and Zynq® UltraScale™+ MPSoC there is no option for XilKernel. FreeRTOS must be used for Zynq. The FreeRTOS BSP for Zynq is available for download from: http://www.freertos.org/Interactive_Frames/Open_Frames.html?http://interactive.freertos.org/forums

   Follow the steps provided in the pdf document provided with the port to use the FreeRTOS BSP.

   The Board Support Package Settings window opens.
3. Select the lwip141 library with version 1.7.

   On the left side of the SDK window, lwip141_v1_7 appears in the list of libraries to be compiled.
4. Select lwip141 in the Project Explorer tab. The configuration options for lwIP are listed. Configure the lwIP and click **OK**.

   The board support package automatically builds with lwIP included in it.

Configuring lwIP Options

The lwIP provides configurable parameters. The values for these parameters can be changed in SDK. There are two major categories of configurable options:

- Xilinx Adapter to lwIP options: These control the settings used by Xilinx adapters for the ethernet cores.
- Base lwIP options: These options are part of lwIP library itself, and include parameters for TCP, UDP, IP and other protocols supported by lwIP.

The following sections describe the available lwIP configurable options.

Customizing lwIP API Mode

The lwip141_v1_7 supports both raw API and socket API:

- The raw API is customized for high performance and lower memory overhead. The limitation of raw API is that it is callback-based, and consequently does not provide portability to other TCP stacks.
- The socket API provides a BSD socket-style interface and is very portable; however, this mode is not as efficient as raw API mode in performance and memory requirements.

The lwip141_v1_7 also provides the ability to set the priority on TCP/IP and other lwIP application threads. Table 1 provides lwIP library API modes.

Table 1: **API Mode Options and Descriptions**

Attribute/Options	Description	Type	Default
api_mode {RAW_API | SOCKET_API}	The lwIP library mode of operation.	enum	RAW_API

Table 1: **API Mode Options and Descriptions *(Cont'd)***

socket_mode_thread_prio	Priority of lwIP TCP/IP thread and all lwIP application threads. This setting applies only when Xilkernel is used in priority mode. It is recommended that all threads using lwIP run at the same priority level. ***Note:*** For GigE based Zynq-7000 and Zynq® UltraScale™+ MPSoC systems using FreeRTOS, appropriate priority should be set. The default priority of 1 will not give the expected behavior. For FreeRTOS (Zynq-7000 and Zynq® UltraScale™+ MPSoC systems), all internal lwIP tasks (except the main TCP/IP task) are created with the priority level set for this attribute. The TCP/IP task is given a higher priority than other tasks for improved performance. The typical TCP/IP task priority is 1 more than the priority set for this attribute for FreeRTOS.	integer	1
use_axieth_on_zynq	In the event that the AxiEthernet soft IP is used on a Zynq-7000 device or a Zynq® UltraScale™+ MPSoC device. This option ensures that the GigE on the Zynq-7000 PS (EmacPs) is not enabled and the device uses the AxiEthernet soft IP for Ethernet traffic. ***Note:*** The existing Xilinx-provided lwIP adapters are not tested for multiple MACs. Multiple Axi Ethernet's are not supported on Zynq UltraScale+ MPSOC devices.	integer	0 = Use Zynq-7000 PS-based or ZynMP PS-based GigE controller 1= User AxiEthernet.

Configuring Xilinx Adapter Options

The Xilinx adapters for EMAC/GigE cores are configurable.

Ethernetlite Adapter Options

Table 2 provides the configuration parameters for the `axi_ethernetlite` adapter.

Table 2: **xps_ethernetlite Adapter Options**

Attribute	Description	Type	Default
`sw_rx_fifo_size`	Software Buffer Size in bytes of the receive data between EMAC and processor	integer	8192
`sw_tx_fifo_size`	Software Buffer Size in bytes of the transmit data between processor and EMAC	integer	8192

TEMAC Adapter Options

Table 3 provides the configuration parameters for the axi_ethernet and GigE adapters.

Table 3: **axi_Ethernet / GigE Adapter**

Attribute	Default	Type	Description
`n_tx_descriptors`	64	integer	Number of Tx descriptors to be used. For high performance systems there might be a need to use a higher value for this.
`n_rx_descriptors`	64	integer	Number of Rx descriptors to be used. For high performance systems there might be a need to use a higher value for this. Typical values are 128 and 256.
`n_tx_coalesce`	1	integer	Setting for Tx interrupt coalescing[1]
`n_rx_coalesce`	1	integer	Setting for Rx interrupt coalescing[1]
`tcp_rx_checksum_offload`	false	boolean	Offload TCP Receive checksum calculation (hardware support required). For GigE in Zynq and Zynq® UltraScale™+ MPSoC, the TCP receive checksum offloading is always present, so this attribute does not apply.
`tcp_tx_checksum_offload`	false	boolean	Offload TCP Transmit checksum calculation (hardware support required). For GigE cores (for Zynq and Zynq® UltraScale™+ MPSoC) the TCP transmit checksum offloading is always present, so this attribute does not apply.
`tcp_ip_rx_checksum_ofload`	false	boolean	Offload TCP and IP Receive checksum calculation (hardware support required). Applicable only for AXI systems. For GigE in Zynq and Zynq® UltraScale™+ MPSoC the TCP and IP receive checksum offloading is always present, so this attribute does not apply.
`tcp_ip_tx_checksum_ofload`	false	boolean	Offload TCP and IP Transmit checksum calculation (hardware support required). Applicable only for AXI systems. For GigE in Zynq and Zynq® UltraScale™+ MPSoC the TCP and IP transmit checksum offloading is always present, so this attribute does not apply.

Table 3: **axi_Ethernet / GigE Adapter *(Cont'd)***

phy_link_speed	enum	CONFIG_LINKSPEED_AUTODETECT	Link speed as auto-negotiated by the PHY. lwIP configures the TEMAC/GigE for this speed setting. This setting must be correct for the TEMAC/GigE to transmit or receive packets. ***Note:*** The CONFIG_LINKSPEED_AUTODETECT setting attempts to detect the correct linkspeed by reading the PHY registers; however, this is PHY dependent, and has been tested with the Marvell PHYs present on Xilinx development boards. For other PHYs, select the correct speed.
temac_use_jumbo_frames_experimental	false	boolean	Use TEMAC jumbo frames (with a size up to 9k bytes). If this option is selected, jumbo frames are allowed to be transmitted and received by the TEMAC. For GigE in Zynq and Zynq® UltraScale™+ MPSoC there is no support for jumbo frames, so this attribute does not apply.

1. This setting is not applicable for GigE in Zynq and Zynq® UltraScale™+ MPSoC.

Configuring Memory Options

The lwIP stack provides different kinds of memories. Similarly, when the application uses socket mode, different memory options are used. All the configurable memory options are provided as a separate category. Default values work well unless application tuning is required.

The memory parameter options are provided in Table 4:

Table 4: **Memory Parameter Options**

Attribute	Default	Type	Description
mem_size	131072	Integer	Total size of the heap memory available, measured in bytes. For applications which use a lot of memory from heap (using C library malloc or lwIP routine mem_malloc or pbuf_alloc with PBUF_RAM option), this number should be made higher as per the requirements.
memp_n_pbuf	16	Integer	The number of memp struct pbufs. If the application sends a lot of data out of ROM (or other static memory), this should be set high.
memp_n_udp_pcb	4	Integer	The number of UDP protocol control blocks. One per active UDP connection.
memp_n_tcp_pcb	32	Integer	The number of simultaneously active TCP connections.
memp_n_tcp_pcb_listen	8	Integer	The number of listening TC connections.
memp_n_tcp_seg	256	Integer	The number of simultaneously queued TCP segments.
memp_n_sys_timeout	8	Integer	Number of simultaneously active timeouts.
memp_num_netbuf	8	Integer	Number of allowed structure instances of type netbufs. Applicable only in socket mode.
memp_num_netconn	16	Integer	Number of allowed structure instances of type netconns. Applicable only in socket mode.
memp_num_api_msg	16	Integer	Number of allowed structure instances of type api_msg. Applicable only in socket mode.
memp_num_tcpip_msg	64	Integer	Number of TCPIP msg structures (socket mode only).

Note: Because Sockets Mode support uses Xilkernel services, the number of semaphores chosen in the Xilkernel configuration must take the value set for the memp_num_netbuf parameter into account. For FreeRTOS BSP there is no setting for the maximum number of semaphores. For FreeRTOS, you can create semaphores as long as memory is available.

Configuring Packet Buffer (Pbuf) Memory Options

Packet buffers (Pbufs) carry packets across various layers of the TCP/IP stack. The following are the pbuf memory options provided by the lwIP stack. Default values work well unless application tuning is required.

Table 5 provides the parameters for the Pbuf memory options:

Table 5: **Pbuf Memory Options Configuration Parameters**

Attribute	Default	Type	Description
pbuf_pool_size	256	Integer	Number of buffers in pbuf pool. For high performance systems, you might consider increasing the pbuf pool size to a higher value, such as 512.
pbuf_pool_bufsize	1700	Integer	Size of each pbuf in pbuf pool. For systems that support jumbo frames, you might consider using a pbuf pool buffer size that is more than the maximum jumbo frame size.
pbuf_link_hlen	16	Integer	Number of bytes that should be allocated for a link level header.

Configuring ARP Options

Table 6 provides the parameters for the ARP options. Default values work well unless application tuning is required.

Table 6: **ARP Options Configuration Parameters**

Attribute	Default	Type	Description
arp_table_size	10	Integer	Number of active hardware address IP address pairs cached.
arp_queueing	1	Integer	If enabled outgoing packets are queued during hardware address resolution. This attribute can have two values: 0 or 1.

Configuring IP Options

Table 7 provides the IP parameter options. Default values work well unless application tuning is required.

Table 7: **IP Configuration Parameter Options**

Attribute	Default	Type	Description
ip_forward	0	Integer	Set to 1 for enabling ability to forward IP packets across network interfaces. If running lwIP on a single network interface, set to 0. This attribute can have two values: 0 or 1.
ip_options	0	Integer	When set to 1, IP options are allowed (but not parsed). When set to 0, all packets with IP options are dropped. This attribute can have two values: 0 or 1.
ip_reassembly	1	Integer	Reassemble incoming fragmented IP packets.
ip_frag	1	Integer	Fragment outgoing IP packets if their size exceeds MTU.
ip_reass_max_pbufs	128	Integer	Reassembly pbuf queue length.

Table 7: **IP Configuration Parameter Options *(Cont'd)***

Attribute	Default	Type	Description
ip_frag_max_mtu	1500	Integer	Assumed max MTU on any interface for IP fragmented buffer.
ip_default_ttl	255	Integer	Global default TTL used by transport layers.

Configuring ICMP Options

Table 8 provides the parameter for ICMP protocol option. Default values work well unless application tuning is required.

Table 8: **ICMP Configuration Parameter Option**

Attribute	Default	Type	Description
icmp_ttl	255	Integer	ICMP TTL value. For GigE cores (for Zynq and Zynq MPSoC) there is no support for ICMP in the hardware.

Configuring IGMP Options

The IGMP protocol is supported by lwIP stack. When set true, the following option enables the IGMP protocol.

Table 9: **IGMP Configuration Parameter Option**

Attribute	Default	Type	Description
imgp_options	false	Boolean	Specify whether IGMP is required.

Configuring UDP Options

Table 10 provides UDP protocol options. Default values work well unless application tuning is required.

Table 10: **UDP Configuration Parameter Options**

Attribute	Default	Type	Description
lwip_udp	true	Boolean	Specify whether UDP is required.
udp_ttl	255	Integer	UDP TTL value.

Configuring TCP Options

Table 11 provides the TCP protocol options. Default values work well unless application tuning is required.

Table 11: **TCP Options Configuration Parameters**

Attribute	Default	Type	Description
lwip_tcp	true	Boolean	Require TCP.
tcp_ttl	255	Integer	TCP TTL value.
tcp_wnd	2048	Integer	TCP Window size in bytes.
tcp_maxrtx	12	Integer	TCP Maximum retransmission value.
tcp_synmaxrtx	4	Integer	TCP Maximum SYN retransmission value.

Table 11: **TCP Options Configuration Parameters *(Cont'd)***

Attribute	Default	Type	Description
tcp_queue_ooseq	1	Integer	Accept TCP queue segments out of order. Set to 0 if your device is low on memory.
tcp_mss	1460	Integer	TCP Maximum segment size.
tcp_snd_buf	8192	Integer	TCP sender buffer space in bytes.

Configuring DHCP Options

The DHCP protocol is supported by lwIP stack. Table 12 provides DHCP protocol options. Default values work well unless application tuning is required.

Table 12: **DHCP Options Configuration Parameters**

Attribute	Default	Type	Description
lwip_dhcp	false	Boolean	Specify whether DHCP is required.
dhcp_does_arp_check	false	Boolean	Specify whether ARP checks on offered addresses.

Configuring the Stats Option

lwIP stack has been written to collect statistics, such as the number of connections used; amount of memory used; and number of semaphores used, for the application. The library provides the `stats_display()` API to dump out the statistics relevant to the context in which the call is used. The stats option can be turned on to enable the statistics information to be collected and displayed when the `stats_display` API is called from user code. Use the following option to enable collecting the stats information for the application.

Table 13: **Statistics Option Configuration Parameters**

Attribute	Description	Type	Default
lwip_stats	Turn on lwIP Statistics	int	0

Configuring the Debug Option

lwIP provides debug information. Table 14 lists all available options.

Table 14: **Debug Option Configuration Parameters**

Attribute	Default	Type	Description
lwip_debug	false	Boolean	Turn on/off lwIP debugging.
ip_debug	false	Boolean	Turn on/off IP layer debugging.
tcp_debug	false	Boolean	Turn on/off TCP layer debugging.
udp_debug	false	Boolean	Turn on/off UDP layer debugging.
icmp_debug	false	Boolean	Turn on/off ICMP protocol debugging.
igmp_debug	false	Boolean	Turn on/off IGMP protocol debugging.
netif_debug	false	Boolean	Turn on/off network interface layer debugging.
sys_debug	false	Boolean	Turn on/off sys arch layer debugging.
pbuf_debug	false	Boolean	Turn on/off pbuf layer debugging

Software APIs

The lwIP library provides two different APIs: RAW mode and Socket mode.

Raw API

The Raw API is callback based. Applications obtain access directly into the TCP stack and vice-versa. As a result, there is no extra socket layer, and using the Raw API provides excellent performance at the price of compatibility with other TCP stacks.

Xilinx Adapter Requirements when using RAW API

In addition to the lwIP RAW API, the Xilinx adapters provide the `xemacif_input` utility function for receiving packets. This function must be called at frequent intervals to move the received packets from the interrupt handlers to the lwIP stack. Depending on the type of packet received, lwIP then calls registered application callbacks.

Raw API File

The `$XILINX_SDK/sw/ThirdParty/sw_services/lwip141_v1_7/src/lwip-1.4.1/doc/rawapi.txt` file describes the lwIP Raw API.

Socket API

The lwIP socket API provides a BSD socket-style API to programs. This API provides an execution model that is a blocking, open-read-write-close paradigm.

Xilinx Adapter Requirements when using Socket API

Applications using the Socket API with Xilinx adapters need to spawn a separate thread called `xemacif_input_thread`. This thread takes care of moving received packets from the interrupt handlers to the `tcpip_thread` of the lwIP. Application threads that use lwIP must be created using the lwIP `sys_thread_new` API. Internally, this function makes use of the appropriate thread or task creation routines provided by XilKernel or FreeRTOS.

Xilkernel/FreeRTOS scheduling policy when using Socket API

lwIP in socket mode requires the use of the Xilkernel or FreeRTOS, which provides two policies for thread scheduling: round-robin and priority based:

There are no special requirements when round-robin scheduling policy is used because all threads or tasks with same priority receive the same time quanta. This quanta is fixed by the RTOS (Xilkernel or FreeRTOS) being used.

With priority scheduling, care must be taken to ensure that lwIP threads or tasks are not starved. For Xilkernel, lwIP internally launches all threads at the priority level specified in `socket_mode_thread_prio`. For FreeRTOS, lwIP internally launches all tasks except the main TCP/IP task at the priority specified in `socket_mode_thread_prio`. The TCP/IP task in FreeRTOS is launched with a higher priority (one more than priority set in socket_mode_thread_prio). In addition, application threads must launch `xemacif_input_thread`. The priorities of both `xemacif_input_thread`, and the lwIP internal threads (`socket_mode_thread_prio`) must be high enough in relation to the other application threads so that they are not starved.

Using Xilinx Adapter Helper Functions

The Xilinx adapters provide the following helper functions to simplify the use of the lwIP APIs.

`void` **`lwip_init`**`()`

This function provides a single initialization function for the lwIP data structures. This replaces specific calls to initialize stats, system, memory, pbufs, ARP, IP, UDP, and TCP layers.

`struct netif` ***`xemac_add`*** `(struct` *`netif *netif`*`, struct` *`ip_addr *ipaddr`*`, struct` *`ip_addr *netmask`*`, struct` *`ip_addr *gw`*`, unsigned char` *`*mac_ethernet_address unsigned mac_baseaddr`*`)`

The `xemac_add` function provides a unified interface to add any Xilinx EMAC IP as well as GigE core. This function is a wrapper around the lwIP `netif_add` function that initializes the network interface 'netif' given its IP address `ipaddr, netmask`, the IP address of the gateway, *`gw`*, the 6 byte ethernet address `mac_ethernet_address`, and the base address, `mac_baseaddr`, of the `axi_ethernetlite` or `axi_ethernet` MAC core.

`void` **`xemacif_input`**`(struct netif *`*`netif`*`)`

(***RAW mode only***)

The Xilinx lwIP adapters work in interrupt mode. The receive interrupt handlers move the packet data from the EMAC/GigE and store them in a queue. The `xemacif_input` function takes those packets from the queue, and passes them to lwIP; consequently, this function is required for lwIP operation in RAW mode. The following is a sample lwIP application in RAW mode.

```
while (1) {
            /* receive packets */
            xemacif_input(netif);

            /* do application specific processing */
      }
```

The program is notified of the received data through callbacks.

`void` **`xemacif_input_thread`**`(struct netif *`*`netif`*`)`

(***Socket mode only***)

In the socket mode, the application thread must launch a separate thread to receive the input packets. This performs the same work as the RAW mode function, `xemacif_input`, except that it resides in its own separate thread; consequently, any lwIP socket mode application is required to have code similar to the following in its main thread:

```
sys_thread_new("xemacif_input_thread",
xemacif_input_thread, netif, THREAD_STACK_SIZE, DEFAULT_THREAD_PRIO);
```

The application can then continue launching separate threads for doing application specific tasks. The `xemacif_input_thread` receives data processed by the interrupt handlers, and passes them to the lwIP `tcpip_thread`.

`void` **`xemacpsif_resetrx_on_no_rxdata`**`(struct netif *netif)`

(Used in both Raw and Socket mode and applicable only for the Zynq-7000 and Zynq MPSoC processors and the GigE controller)

There is an errata on the GigE controller that is related to the Rx path. The errata describes conditions whereby the Rx path of GigE becomes completely unresponsive with heavy Rx traffic of small sized packets. The condition occurrence is rare; however a software reset of the Rx logic in the controller is required when such a condition occurs.

This API must be called periodically (approximately every 100 milliseconds using a timer or thread) from user applications to ensure that the Rx path never becomes unresponsive for more than 100 milliseconds.

lwIP Performance

Table 15 provides the maximum TCP throughput achievable by FPGA, CPU, EMAC, and system frequency in RAW modes. Applications requiring high performance should use the RAW API.

Table 15: **Library Performance**

FPGA	CPU	EMAC	System Frequency	Max TCP Throughput in RAW Mode	
				Rx Side	Tx Side
Virtex®	MicroBlaze	axi-ethernet	100 MHz	182 Mbps	100 Mbps
Virtex	MicroBlaze	xps-ll-temac	100 MHz	178 Mbps	100 Mbps
Virtex	MicroBlaze	xps-ethernetlite	100 MHz	50 Mbps	38 Mbps

API Examples

Sample applications using the RAW API and Socket API are available on the Xilinx website. This section provides pseudo code that illustrates the typical code structure.

RAW API

Applications using the RAW API are single threaded, and have the following broad structure:

```
int main()
{
        struct netif *netif, server_netif;
        struct ip_addr ipaddr, netmask, gw;

        /* the MAC address of the board.
        * This should be unique per board/PHY */
        unsigned char mac_ethernet_address[] =
            {0x00, 0x0a, 0x35, 0x00, 0x01, 0x02};

        lwip_init();

        /* Add network interface to the netif_list,
         * and set it as default */
        if (!xemac_add(netif, &ipaddr, &netmask,
            &gw, mac_ethernet_address,
            EMAC_BASEADDR)) {
            printf("Error adding N/W interface\n\r");
            return -1;
       }
        netif_set_default(netif);

        /* now enable interrupts */
```

```
        platform_enable_interrupts();

        /* specify that the network if is up */
        netif_set_up(netif);

        /* start the application, setup callbacks */
        start_application();

        /* receive and process packets */
        while (1) {
            xemacif_input(netif);
            /* application specific functionality */
            transfer_data();
        }
}
```

RAW API works primarily using asynchronously called Send and Receive callbacks.

Socket API

XilKernel-based applications in socket mode can specify a static list of threads that Xilkernel spawns on startup in the Xilkernel Software Platform Settings dialog box. Assuming that `main_thread()` is a thread specified to be launched by XIlkernel, control reaches this first thread from application "main" after the Xilkernel schedule is started. In `main_thread`, one more thread (network_thread) is created to initialize the MAC layer.

For FreeRTOS (Zynq-7000 processor systems) based applications, once the control reaches application "main" routine, a task (can be termed as main_thread) with an entry point function as `main_thread()` is created before starting the scheduler. After the FreeRTOS scheduler starts, the control reaches `main_thread()`, where the lwIP internal initialization happens. The application then creates one more thread (network_thread) to initialize the MAC layer.

The following pseudo-code illustrates a typical socket mode program structure.

```
void network_thread(void *p)
{
        struct netif *netif;
        struct ip_addr ipaddr, netmask, gw;

        /* the MAC address of the board.
         * This should be unique per board/PHY */
        unsigned char mac_ethernet_address[] =
            {0x00, 0x0a, 0x35, 0x00, 0x01, 0x02};

        netif = &server_netif;

        /* initialize IP addresses to be used */
        IP4_ADDR(&ipaddr,192,168,1,10);
        IP4_ADDR(&netmask,255,255,255,0);
        IP4_ADDR(&gw,192,168,1,1);

        /* Add network interface to the netif_list,
         * and set it as default */
        if (!xemac_add(netif, &ipaddr, &netmask,
              &gw, mac_ethernet_address,
              EMAC_BASEADDR)) {
            printf("Error adding N/W interface\n\r");
            return;
        }
        netif_set_default(netif);

        /* specify that the network if is up */
```

```
            netif_set_up(netif);

            /* start packet receive thread
             - required for lwIP operation */
            sys_thread_new("xemacif_input_thread", xemacif_input_thread,
                netif,
                THREAD_STACKSIZE, DEFAULT_THREAD_PRIO);

            /* now we can start application threads */
            /* start webserver thread (e.g.) */
            sys_thread_new("httpd" web_application_thread, 0,
                  THREAD_STACKSIZE DEFAULT_THREAD_PRIO);
}

int main_thread()
{
            /* initialize lwIP before calling sys_thread_new */
            lwip_init();

            /* any thread using lwIP should be created using
             * sys_thread_new() */
            sys_thread_new("network_thread" network_thread, NULL,
                  THREAD_STACKSIZE DEFAULT_THREAD_PRIO);

          return 0;
}
```

UG1189 October 5, 2016

Library XilSecure for Zynq UltraScale MPSoC (v1.2)

Summary

The LibXilSecure library provides APIs to access secure hardware on the Zynq® UltraScale+™ MPSoC devices and also provides an algorithm for SHA2 hash generation.

This library includes:

- SHA-3 engine hash functions
- AES for symmetric key encryption
- RSA for authentication

Note: The above libraries are grouped into the Configuration and Security Unit (CSU) on the Zynq UltraScale+ MPSoC device.

- SHA2 hash generation

Note: The SHA2 hash generation is a software algorithm which generates SHA2 hash on provided data.

XilSecure APIs

The following list is a list of functions for Zynq® UltraScale+™ MPSoC devices which are grouped by their respective function You can click on a link to go directly to the function section.

Source Files

- `xsecure_hw.h`: This file contains the hardware interface for all the three modules.
- `xsecure_sha.h`: This file contains the driver interface for SHA-3 module.
- `xsecure_sha.c`: This file contains the implementation of the driver interface for SHA-3 module.
- `xsecure_rsa.h`: This file contains the driver interface for RSA module.
- `xsecure_rsa.c`: This file contains the implementation of the driver interface for RSA module.
- `xsecure_aes.h`: This file contains the driver interface for AES module.
- `xsecure_aes.c` : This file contains the implementation of the driver interface for AES module
- `xsecure_sha2.h`: This file contains the interface for SHA2 hash algorithm.
- `xsecure_sha2_a53_32b.a`: Pre-compiled file which has SHA2 implementation for A53 32bit.
- `xsecure_sha2_a53_64b.a`: Pre-compiled file which has SHA2 implementation for A53 64 bit.
- `xsecure_sha2_a53_r5.a`: Pre-compiled file which has SHA2 implementation for r5.

SHA-3 Functions

This block uses the NIST-approved SHA-3 algorithm to generate 384 bit hash on the input data. Because the SHA-3 hardware only accepts 104 byte blocks as minimum input size, the input data is padded with a 10*1 sequence to complete the final byte block. The padding is handled internally by the driver API.

API Summary

The following is a summary list of APIs provided for using SHA-3 module. Descriptions of the APIs follow the list.

s32 XSecure_Sha3Initialize(XSecure_Sha3 *InstancePtr, XCsuDma* CsuDmaPtr)

void XSecure_Sha3Update(XSecure_Sha3 *InstancePtr, const u8 *Data, const u32 Size)

void XSecure_Sha3Start(XSecure_Sha3 *InstancePtr)

void XSecure_Sha3Finish(XSecure_Sha3 *InstancePtr, u8 *Hash)

void XSecure_Sha3Digest(XSecure_Sha3 *InstancePtr, const u8 *In, const u32 Size u8 *Out)

`s32` **`XSecure_Sha3Initialize`**`(XSecure_Sha3 *InstancePtr, XCsuDma* CsuDmaPtr)`

Description	This API initializes a specific Xsecure_Sha3 instance so that it is ready to be used.
Parameters	`InstancePtr` is a pointer to the XSecure_Sha3 instance.
	`CsuDmaPtr` is the pointer to the XCsuDma instance.
Returns	XST_SUCCESS if initialization was successful.

`void` **`XSecure_Sha3Start`**`(XSecure_Sha3 *InstancePtr)`

Description	This API configures the secure stream switch (SSS) and starts the SHA-3 engine.
Parameters	`InstancePtr` is a pointer to the `XSecure_Sha3` instance.
Returns	None

`void` **`XSecure_Sha3Update`**`(XSecure_Sha3 *InstancePtr, const u8 *Data, const u32 Size)`

Description	This API updates hash for new input data block. This is used after `XSecure_Sha3Start` to update more input data.
	`InstancePtr` is a pointer to the XSecure_Sha3 instance.
Parameters	`Data` is the pointer to the input data for hashing
	Size of the input data in bytes
Returns	None

`void` **`XSecure_Sha3Finish`**`(XSecure_Sha3 *InstancePtr, u8 *Hash)`

Description	This API sends the last block; for example, the padding when block size is not multiple of 104 bytes. The final hash is ready at this stage.
Parameters	`InstancePtr` is a pointer to the XSecure_Sha3 instance.
	`Hash` is the pointer to location where resulting hash will be written
Returns	None

`void` **`XSecure_Sha3Digest`**`(XSecure_Sha3 *InstancePtr, const u8 *In, const u32 Size u8 *Out)`

Description	This API calculates SHA-3 Digest on the given input data. In effect, this does the complete operation that can be achieved by calling `XSecure_Sha3Start`, `XSecure_Sha3Update`, and `XSecure_Sha3Finish` in succession.
Parameters	`InstancePtr` is a pointer to the `XSecure_Sha3` instance. `In` is the pointer to the input data for hashing size of the input data in bytes. `Out` is the pointer to location where resulting hash is written.
Returns	None

Example Usage

`XSecure_Sha3Example.c` : This example is a simple application using SHA-3 device to calculate 384 bit hash on Hello World string.

A more typical use case of SHA-3 has been illustrated in RSA example XSecure_RsaExample.c where it is used to calculate hash of boot image as a step in authentication process.

RSA

This block decrypts data based on RSA-4096 algorithm. A utility function to compare the signature with expected signature (Verification) is also provided.

API Summary

The following is a summary list of APIs provided for using RSA module.. Descriptions of the APIs follow the list.

s32 XSecure_RsaInitialize(XSecure_Rsa *InstancePtr, u8 *Mod, u8 *ModExt, u8 *ModExpo)

s32 XSecure_RsaDecrypt(XSecure_Rsa *InstancePtr, u8 *EncText, u8 *Result)

u32 XSecure_RsaSignVerification(u8 *Signature, u8 *Hash, u32 HashLen)

`s32` **`XSecure_RsaInitialize`**`(XSecure_Rsa *InstancePtr, u8 *Mod, u8 *ModExt, u8 *ModExpo)`

Description	This API initializes a specific `Xsecure_Rsa` instance so that it is ready to be used.
Parameters	`InstancePtr` is a pointer to the `XSecure_Rsa` instance. `Mod` is the pointer to Modulus used for authentication. `ModExt` is the pointer to precalculated R^2 Mod N value used for authentication. `ModExpo` is the pointer to the exponent (public key) used for authentication.
Returns	`XST_SUCCESS` if decryption was successful.

s32 **XSecure_RsaDecrypt**(XSecure_Rsa *InstancePtr, u8 *EncText, u8 *Result)

Description	This API handles the RSA decryption from end-to-end.
Parameters	`InstancePtr` is a pointer to the `XSecure_Rsa` instance. `Result` is the pointer to decrypted data generated by RSA. `EncText` is the pointer to the data (hash) to be decrypted.
Returns	`XST_SUCCESS` if decryption was successful.

---

u32 **XSecure_RsaSignVerification**(u8 *Signature, u8 *Hash, u32 HashLen)

Description	This API matches the decrypted data with expected data.
Parameters	`InstancePtr` is a pointer to the XSecure_Rsa instance. `Signature` is the pointer to RSA signature for data to be authenticated. `Hash` is the pointer to expected hash data. `HashLen` is the length of Hash used.
Returns	`XST_SUCCESS` if decryption was successful.

Example Usage

`XSecure_RsaExample.c` : This example deals with RSA based authentication of FSBL in a Zynq MPSoC boot image. The boot image signature is decrypted using RSA- 4096 algorithm. Resulting digest is matched with SHA digest calculated on the FSBL using SHA-3 driver.

The authenticated boot image should be loaded in memory through JTAG and address of the boot image should be passed to the function. By default, the example assumes that the authenticated image is present at location `0x04000000` (DDR), which can be changed as required.

AES

This block can encrypt/decrypt data using AES-GCM algorithm. Decryption using keyrolling is also supported. The key, IV and the format of the encrypted data should be the same as the one used by Bootgen for encrypting Zynq UltraScale + MPSoC device boot images. The bootgen encrypted images have a secure header at the beginning followed by any number of blocks.

Decryption in chunks for bitstreams is supported in cases where the entire bitstream is not present in single contiguous location. For example, the DDR less systems.

API Summary

The following is a summary list of APIs provided for using AES module. Descriptions of the APIs follow the list.

s32 XSecure_AesInitialize(XSecure_Aes *InstancePtr, XCsuDma *CsuDmaPtr,u32 KeySel, u32* Iv, u32* Key)

void XSecure_AesSetChunking(XSecure_Aes *InstancePtr, u8 Chunking)

void XSecure_AesSetChunkConfig(XSecure_Aes *InstancePtr, u8 *ReadBuffer, u32 ChunkSize, u32(*DeviceCopy)(u32, u64, u32))

s32 XSecure_AesDecrypt(XSecure_Aes *InstancePtr, u8 *Dst, const u8 *Src, *32 Length)

void XSecure_AesEncrypt(XSecure_Aes *InstancePtr, u8 *Dst, const u8 *Src 32 Len)

void XSecure_AesReset(XSecure_Aes *InstancePtr)

s32 XSecure_AesInitialize(XSecure_Aes *InstancePtr, XCsuDma *CsuDmaPtr,u32 KeySel, u32* Iv, u32* Key)

Description This API initializes the instance pointer.

Parameters

`InstancePtr` is a pointer to the `XSecure_Aes` instance.

`CsuDmaPtr` is the pointer to the `XCsuDma instance`.

`KeySel` is the key source for decryption, can be KUP (user- provided) or device key.

`Iv` is pointer to the Initialization Vector for decryption.

`Key` is the pointer to Aes decryption key in case KUP key is used. Passes `Null` if device key is to be used.

Returns `XST_SUCCESS` upon success.

---

void XSecure_AesSetChunking(XSecure_Aes *InstancePtr, u8 Chunking)

Description This function handles the configuration for bitstream chunking.

Parameters

`InstancePtr` is a pointer to the `XSecure_Aes` instance.

`Chunking` is used to enable or disable data chunking

Returns None

---

void XSecure_AesSetChunkConfig(XSecure_Aes *InstancePtr, u8 *ReadBuffer, u32 ChunkSize, u32(*DeviceCopy)(u32, u64, u32))

Description This function handles the AES-GCM decryption.

Parameters

`InstancePtr` is a pointer to the `XSecure_Aes` instance.

`ReadBuffer` is the buffer where the data will be written after copy.

`ChunkSize` is the length of the buffer in bytes.

`DeviceCopy` is the function pointer to copy data from device to buffer. Return value of `DeviceCopy` should be 0 in case of success and 1 in case of failure. Arguments of `DeviceCopy` are:

- `SrcAddress`: Address of data in device.
- `DestAddress`: Address where data will be copied in chunks
- `Length`: Length of data in bytes.

Returns `None.`

`s32 XSecure_AesDecrypt(XSecure_Aes *InstancePtr, u8 *Dst, const u8 *Src, *32 Length)`

Description This function handles the AES-GCM decryption.

Parameters
- `InstancePtr` is a pointer to the `XSecure_Aes` instance.
- `Src` is the pointer to encrypted data source location
- `Dst` is the pointer to location where decrypted data will be written.
- `Length` is the expected total length of decrypted image/data.

Returns
- `XST_SUCCESS` if encryption passed and GCM tag matched.
- `XSECURE_CSU_AES_IMAGE_LEN_MISMATCH` if Image length did not match.
- `XSECURE_CSU_AES_GCM_TAG_MISMATCH` if GCM tag mismatch occurs.
- `XSECURE_CSU_AES_DEVICE_COPY_ERROR` if copy of chunk from device failed.
- `XST_FAILURE` in case of failure.

`void XSecure_AesEncrypt(XSecure_Aes *InstancePtr, u8 *Dst, const u8 *Src 32 Len)`

Description This API encrypts input data using encryption engine.

Parameters
- `InstancePtr` is a pointer to the XSecure_Aes instance.
- `Dst` is pointer to location where encrypted output will be written.
- `Src` is pointer to input data for encryption.
- `Len` is the size of input data in bytes

Returns None

`void XSecure_AesReset(XSecure_Aes *InstancePtr)`

Description This API resets the AES engine.

Parameters `InstancePtr` is a pointer to the `XSecure_Aes` instance.

Returns None

Example Usage

`XSecure_AesExample.c`: This example illustrates AES usage with decryption of a Zynq UltraScale + MPSoC boot image placed at a predefined location in memory. User can select the key type (device key or user-selected KUP key). The example assumes that the boot image is present at `0x0400000` (DDR); consequently, the image must be loaded at that address through JTAG. The example decrypts the boot image and returns `XST_SUCCESS` or `XST_FAILURE` based on whether the GCM tag was successfully matched.

SHA-2 Functions

when all the data is available on which sha2 must be calculated, the sha_256() can be used with appropriate parameters, as described.

When all the data is not available on which sha2 must be calculated, use the sha2 functions in the following order:

1. sha2_update() can be called multiple times till input data is completed.

2. sha2_context is updated by the library only; do not change the values of the context.

SHA2 Example

```
sha2_context ctx;
sha2_starts(&ctx);
sha2_update(&ctx, (unsigned char *)in, size);
sha2_finish(&ctx, out);
Class
struct sha2_context
```

Note: You can also refer to the xilsecure_sha2_example.c file. This is a sample application for illustrating SHA2 calculation of 256bit hash for provided data.

API Summary

The following is a summary list of APIs provided for using SHA-3 module. Descriptions of the APIs follow the list.

void sha2_finish (sha2_context * ctx, unsigned char * output)

void sha2_starts (sha2_context * ctx)

void sha2_update (sha2_context * ctx, unsigned char * input, unsigned int ilen)

void sha_256 (const unsigned char * in, const unsigned int size, unsigned char * out)

`void` **`sha2_finish`** `(sha2_context * ctx, unsigned char * output)`

Description This API finishes the SHA calculation.

Parameters `ctx`: Pointer to sha2_context structure.

`output`: char pointer to calculated hash data.

Returns None

`void` **`sha2_starts`** `(sha2_context * ctx)`

Description This API initializes the SHA2 context.

Parameters `ctx`: Pointer to sha2_context structure that stores status and buffer.

Returns None

`void` **`sha2_update`** `(sha2_context * ctx, unsigned char * input, unsigned int ilen )`

Description This API adds the input data to SHA256 calculation.

Parameters `ctx`: Pointer to sha2_context, structure.

`input`: Char pointer to data to add.

`ilen`: Length of the data.

Returns None

```
void sha_256 (const unsigned char * in, const unsigned int
   size, unsigned char * out)
```

Description This API calculates the hash for the input data using SHA-256 algorithm. This function internally calls the sha2_init, updates and finishes functions and updates the result.

Parameters `in`: Char pointer which contains the input data.

`size`: Unsigned int which contains the length of the input data.

`out`: Output buffer that contains the hash of the input.

Returns None

LibXil RSA for Zynq-7000 AP SoC Devices (v1.2)

LibXil RSA Library Overview

The LibXil RSA library provides APIs to use RSA encryption and decryption algorithms and SHA algorithms.

For an example on usage of this library, refer to the RSA Authentication application and its documentation.

SDK Project Files and Folders

Table 1 shows the SDK project files.

Table 1: **SDK Project Files and Folder Descriptions**

File/Folder	Description
`librsa.a`	Contains the implementation
`xilrsa.h`	Header containing APIs.

Description

The `xilrsa` library contains the description of the RSA and SHA functions that you use to create and verify the signature. The RSA-2048 bit is used for RSA and the SHA-256 bit is used for hash.

Use of SHA-256 Functions

When all the data is available on which `sha2` must be calculated, the `sha_256()` can be used with appropriate parameters, as described.

When all the data is not available on which `sha2` must be calculated, use the `sha2` functions in the following order:

1. `sha2_update()` can be called multiple times till input data is completed.
2. `sha2_context` is updated by the library only; do not change the values of the context.

SHA2 Example

```
sha2_context ctx;
sha2_starts(&ctx);
sha2_update(&ctx, (unsigned char *)in, size);
sha2_finish(&ctx, out);
```

Class

```
struct sha2_context
```

Macros

RSA Definitions

```
#define RSA_DIGIT unsigned long
#define RSA_NUMBER[1] RSA_DIGIT
```

1. RSA_NUMBER is a pointer to RSA_DIGIT

LibXil RSA APIs and Descriptions

This section provides detailed descriptions of the LibXil RSA library APIs.

```
void rsa2048_exp (const unsigned char *base, const
   unsigned char *modular, const unsigned char
   * modular_ext, const unsigned char *exponent, unsigned
   char *result)
```

Parameters	modular: a char pointer which contains the key modulus modular_ext: a char pointer which contains the key modulus extension exponent: a char pointer which contains the private key exponent result: a char pointer which contains the encrypted data
Returns	None
Description	This function is used to encrypt the data using 2048 bit private key.
Includes	xilrsa.h

```
void rsa2048_pubexp (RSA_NUMBER a, RSA_NUMBER x, unsigned
   long e, RSA_NUMBER m, RSA_NUMBER rrm )
```

Parameters	a: RSA_NUMBER containing the decrypted data. x: RSA_NUMBER containing the input data e: unsigned number containing the public key exponent m: RSA_NUMBER containing the public key modulus rrm: RSA_NUMBER containing the public key modulus extension.
Returns	None
Description	This function is used to decrypt the data using 2048 bit public key
Includes	xilrsa.h

```
void sha2_finish (sha2_context * ctx, unsigned char
   * output )
```

Parameters	ctx: Pointer to sha2_context structure. output: char pointer to calculated hash data.
Returns	None
Description	This function finishes the SHA calculation.
Includes	xilsha.h

`void` **`sha2_starts`** `(sha2_context *  ctx)`

Parameters	ctx: Pointer to sha2_context structure that stores status and buffer.
Returns	None
Description	This function initializes the sha2 context.
Includes	xilsha.h

`void` **`sha2_update`** `(sha2_context * ctx, unsigned char * input, unsigned int ilen )`

Parameters	ctx: Pointer to `sha2_context`, structure. input: Char pointer to data to add. ilen: Length of the data.
Returns	None
Description	This function adds the input data to SHA-256 calculation.
Includes	xilsha.h

`void` **`sha_256`** `(const unsigned char * in, const unsigned int size, unsigned char * out)`

Parameters	in: Char pointer which contains the input data. size: Unsigned int which contains the length of the input data. out: Output buffer that contains the hash of the input.
Returns	None
Description	This function calculates the hash for the input data using SHA-256 algorithm. This function internally calls the `sha2_init`, updates and finishes functions and updates the result.
Includes	xilrsa.h

UG1191 November 30, 2016

LibXil SKey for Zynq-7000 UltraScale and Zynq UltraScale+ MPSoC AP SoC Devices (v6.1)

Overview

The LibXil SKey library provides a programming mechanism for user-defined eFUSE bits and for programming the KEY into battery-backed RAM (BBRAM) of Zynq® SoC, provides programming mechanisms for eFUSE bits and BBRAM key of UltraScale™ and the Zynq® UltraScale+™ MPSoC devices.

In Zynq:

- PS eFUSE holds the RSA primary key hash bits and user feature bits, which can enable or disable some Zynq®-7000 processor features.
- PL eFUSE holds the AES key, the user key, and some of the feature bits.
- BBRAM holds the AES key.

In UltraScale™:

- PL eFuse holds the AES key, the user key, RSA key hash and some of the feature bits.
- PL BBRAM holds AES key.

In Zynq® UltraScale+™ MPSoC:

PS eFUSE holds the AES key, the user key, PPK0 and PPK1 hash, SPK ID, JTAG user code and some user feature bits, which can be used to enable or disable some Zynq UltraScale+ MPSoC features. BBRAM holds the AES key.

The following user application (example) files are provided:

- `xilskey_bbram_example.c` file lets you write the key to BBRAM of Zynq.
- `xilskey_efuse_example.c` file lets you write into the PS/PL eFUSE of Zynq and Ultrascale.
- `xilskey_efuseps_zynqmp_example.c` file lets you write into eFUSE PS of Zynq UltraScale+ MPSoC.
- `xilskey_bbramps_zynqmp_example.c` file lets you write BBRAM key of Zynq UltraScale+ MPSoC.
- `xilskey_bbram_ultrascale_example.c` file lets you write BBRAM key of UltraScale.
- `xilskey_puf_registration.c` file lets you to do PUF (Physically Uncloneable Function) registration, generate Black key (encrypted AES key with PUF helper data) and program eFUSe with Black key and PUF data.

Caution! Make sure to enter the correct information before writing or “burning” eFUSE bits. Once burned, they cannot be changed. The BBRAM key can be programmed any number of times.

Note: POR reset is required for the eFUSE values to be recognized.

SDK Project File and Folders

Table 1 lists the eFUSE application SDK project files, folders, and macros.

Table 1: **eFUSE SDK Application Project Files**

File or Folder	Description
`xilskey_efuse_example.c`	Contains the main application code. Does the PS/PL structure initialization and writes/reads the PS/PL eFUSE based on the user settings provided in the `xilskey_input.h`.
`xilskey_input.h`	Contains all the actions that are supported by the eFUSE library. Using the preprocessor directives given in the file, you can read/write the bits in the PS/PL eFUSE. More explanation of each directive is provided in the following sections. Burning or reading the PS/PL eFUSE bits is based on the values set in the `xilskey_input.h` file. Also contains GPIO pins and channels connected to MASTER JTAG primitive and hardware module to access Ultrascale eFUSE In this file, specify the 256 bit key to be programmed into BBRAM. In this file, specify the AES(256 bit) key, User (32 bit and 128 bit) keys and RSA key hash(384 bit) key to be programmed into eFuse of UltraScale.
`XSK_EFUSEPS_DRIVER`	Define to enable the writing and reading of PS eFUSE.
`XSK_EFUSEPL_DRIVER`	Define to enable the writing of PL eFUSE.
`xilskey_bbram_example.c`	Contains the example to program a key into BBRAM and verify the key. ***Note:*** This algorithm only works when programming and verifying key are both done, in that order.
`xilskey_efuseps_zynqmp_example.c`	Contains the example code to program the PS eFUSE and read back of eFUSE bits from the cache.
`xilskey_efuseps_zynqmp_input.h`	Contains all the inputs supported for eFUSE PS of Zynq UltraScale+ MPSoC. eFUSE bits are programmed based on the inputs from the `xilskey_efuseps_zynqmp_input.h` file.
`xilskey_bbramps_zynqmp_example.c`	Contains the example code to program and verify BBRAM key. Default is zero. You can modify this key on top of the file.
`xilskey_bbram_ultrascale_example.c`	Contains example code to program and verify BBRAM key of UltraScale. ***Note:*** Programming and verification of BBRAM key cannot be done separately.
`xilskey_bbram_ultrascale_input.h`	Contains all the preprocessor directives you need to provide. In this file, specify BBRAM AES key or Obfuscated AES key to be programmed, DPA protection enable and, GPIO pins and channels connected to MASTER JTAG primitive.
`xilskey_puf_registration.c`	Contains all the PUF related code. This example illustrates PUF registration and generating black key and programming eFUSE with PUF helper data, CHash and Auxilary data along with the Black key.
`xilskey_puf_registration.h`	Contains all the preprocessor directives based on which read/write the eFUSE bits and Syndrome data generation. More explanation of each directive is provided in the following sections.

User-Configurable Zynq PS eFUSE Parameters

Define the XSK_EFUSEPS_DRIVER macro to use the PS eFUSE. After defining the macro, provide the inputs defined with XSK_EFUSEPS to burn the bits in PS eFUSE.

If the bit is to be burned, define the macro as TRUE; otherwise define the macro as FALSE. See Table 2.

Table 2: **User Configurable Zynq PS eFUSE Parameters**

Macro Name	Description
XSK_EFUSEPS_ENABLE_WRITE_PROTECT	Default = FALSE. TRUE to burn the write-protect bits in eFUSE array. Write protect has two bits. When either of the bits is burned, it is considered write-protected. So, while burning the write-protected bits, even if one bit is blown, write API returns success. As previously mentioned, POR reset is required after burning for write protection of the eFUSE bits to go into effect. It is recommended to do the POR reset after write protection. Also note that, after write-protect bits are burned, no more eFUSE writes are possible. If the write-protect macro is TRUE with other macros, write protect is burned in the last iteration, after burning all the defined values, so that for any error while burning other macros will not effect the total eFUSE array. FALSE does not modify the write-protect bits.
XSK_EFUSEPS_ENABLE_RSA_AUTH	Default = FALSE. Use TRUE to burn the RSA enable bit in the PS eFUSE array. After enabling the bit, every successive boot must be RSA-enabled apart from JTAG. Before burning (blowing) this bit, make sure that eFUSE array has the valid PPK hash. If the PPK hash burning is enabled, only after writing the hash successfully, RSA enable bit will be blown. For the RSA enable bit to take effect, POR reset is required. FALSE does not modify the RSA enable bit.
XSK_EFUSEPS_ENABLE_ROM_128K_CRC	Default = FALSE. TRUE burns the ROM 128K CRC bit. In every successive boot, BootROM calculates 128k CRC. FALSE does not modify the ROM CRC 128K bit.
XSK_EFUSEPS_ENABLE_RSA_KEY_HASH	Default = FALSE. TRUE burns (blows) the eFUSE hash, that is given in XSK_EFUSEPS_RSA_KEY_HASH_VALUE when write API is used. TRUE reads the eFUSE hash when the read API is used and is read into structure. FALSE ignores the provided value.
XSK_EFUSEPS_RSA_KEY_HASH_VALUE	0000000000000000000000000000000000000000000000000000000000000000 The specified value is converted to a hexadecimal buffer and written into the PS eFUSE array when the write API is used. This value should be the Primary Public Key (PPK) hash provided in string format. The buffer must be 64 characters long: valid characters are 0-9, a-f, and A-F. Any other character is considered an invalid string and will not burn RSA hash. When the Xilskey_EfusePs_Write() API is used, the RSA hash is written, and the XSK_EFUSEPS_ENABLE_RSA_KEY_HASH must have a value of TRUE.

Table 2: **User Configurable Zynq PS eFUSE Parameters *(Cont'd)***

Macro Name	Description
XSK_EFUSEPS_DISABLE_DFT_JTAG	Default = FALSE TRUE disables DFT JTAG permanently. FALSE will not modify the eFuse PS DFT JTAG disable bit
XSK_EFUSEPS_DISABLE_DFT_MODE	Default = FALSE TRUE disables DFT mode permanently. FALSE will not modify the eFuse PS DFT mode disable bit

User-Configurable Zynq PL eFUSE Parameters

Table 3 shows the user-configurable PL eFUSE parameters.

Table 3: **User-Configurable Zynq PL eFUSE Parameters**

Macro Name	Definition
XSK_EFUSEPL_FORCE_PCYCLE_RECONFIG	Default = FALSE. If the value is set to TRUE, then the part has to be power-cycled to be reconfigured. FALSE does not set the eFUSE control bit.
XSK_EFUSEPL_DISABLE_KEY_WRITE	Default = FALSE. TRUE disables the eFUSE write to FUSE_AES and FUSE_USER blocks. FALSE does not affect the EFUSE bit.
XSK_EFUSEPL_DISABLE_AES_KEY_READ	Default = FALSE. TRUE disables the write to FUSE_AES and FUSE_USER key and disables the read of FUSE_AES. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_DISABLE_USER_KEY_READ	Default = FALSE. TRUE disables the write to FUSE_AES and FUSE_USER key and disables the read of FUSE_USER. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_DISABLE_FUSE_CNTRL_WRITE	Default = FALSE. TRUE disables the eFUSE write to FUSE_CTRL block. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_FORCE_USE_AES_ONLY	Default = FALSE. TRUE forces the use of secure boot with eFUSE AES key only. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_DISABLE_JTAG_CHAIN	Default = FALSE. TRUE permanently disables the Zynq ARM DAP and PL TAP. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_BBRAM_KEY_DISABLE	Default = FALSE. TRUE forces the eFUSE key to be used if booting Secure Image. FALSE does not affect the eFUSE bit.

MIO Pins for Zynq PL JTAG Operations

You can change the listed pins at your discretion. See Table 4.

Table 4: **MIO Pins for PL JTAG**

Pin Name	Pin Number[1]
XSK_EFUSEPL_MIO_JTAG_TDI	(17)
XSK_EFUSEPL_MIO_JTAG_TDO	(18)
XSK_EFUSEPL_MIO_JTAG_TCK	(19)
XSK_EFUSEPL_MIO_JTAG_TMS	(20)

Notes:

1. The pin numbers listed are examples. You must assign appropriate pin numbers per your hardware design.

MUX

The following subsections describe MUX usage, the MUX selection pin, and the MUX parameter.

MUX Usage Requirements

To write the PL eFUSE using a driver you must:

- Use four MIO lines (TCK,TMS,TDO,TDI)
- Connect the MIO lines to a JTAG port

If you want to switch between the external JTAG and JTAG operation driven by the MIOs, you must:

- Include a MUX between the external JTAG and the JTAG operation driven by the MIOs
- Assign a MUX selection PIN

To rephrase, to select JTAG for PL EFUSE writing, you must define the following:

- The MIOs used for JTAG operations (TCK,TMS,TDI,TDO), shown in Table 4.
- The MIO used for the MUX Select Line, shown in Table 5.
- The Value on the MUX Select line, shown in Table 6, to select JTAG for PL eFUSE writing.

Figure 1 illustrates correct MUX usage.

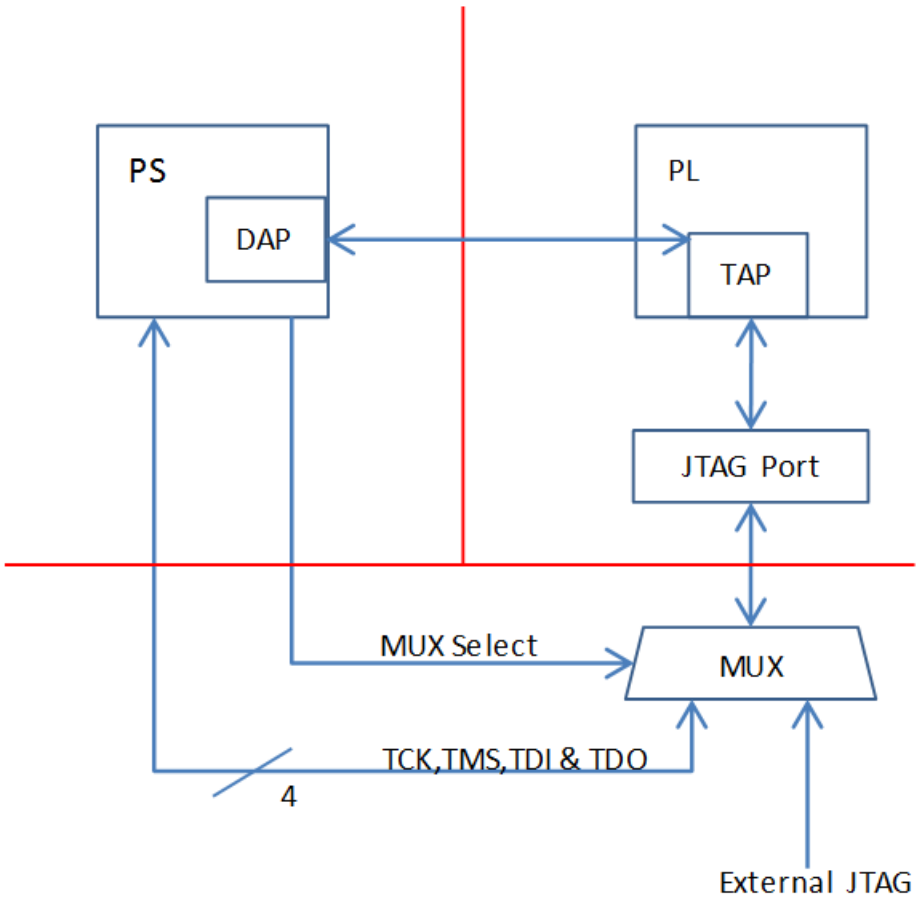

Figure 1: **MUX Usage**

Note: If you use the Vivado Device Programmer tool to burn PL eFUSEs, there is no need for MUX circuitry or MIO pins.

Selection Pin

Table 5 shows the MUX selection pin.

Table 5: **MUX Selection Pin**

Pin Name	Pin Number	Description
XSK_EFUSEPL_MIO_JTAG_MUX_SELECT	(21)	This pin toggles between the external JTAG or MIO driving JTAG operations.

MUX Parameter

Table 6 shows the MUX parameter.

Table 6: **MUX Parameter**

Parameter Name	Description
XSK_EFUSEPL_MIO_MUX_SEL_DEFAULT_VAL	Default = LOW. LOW writes zero on the MUX select line before PL_eFUSE writing. HIGH writes one on the MUX select line before PL_eFUSE writing.

AES and User Key Parameters

Table 7 shows the AES and user key parameters.

Table 7: **AES and User Key Parameters**

Parameter Name	Description
XSK_EFUSEPL_PROGRAM_AES_AND_USER_LOW_KEY	Default = FALSE. TRUE burns the AES and User Low hash key, which are given in the XSK_EFUSEPL_AES_KEY and the XSK_EFUSEPL_USER_LOW_KEY respectively. FALSE ignores the provided values. You cannot write the AES Key and the User Low Key separately.
XSK_EFUSEPL_PROGRAM_USER_HIGH_KEY	Default =FALSE. TRUE burns the User High hash key, given in XSK_EFUSEPL_PROGRAM_USER_HIGH_KEY. FALSE ignores the provided values.
XSK_EFUSEPL_AES_KEY	Default = 0000000000000000000000000000000000000000000000000000000000000000 This value converted to hex buffer and written into the PL eFUSE array when write API is used. This value should be the AES Key, given in string format. It must be 64 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered an invalid string and will not burn AES Key. To write AES Key, XSK_EFUSEPL_PROGRAM_AES_AND_USER_LOW_KEY must have a value of TRUE.
XSK_EFUSEPL_USER_LOW_KEY	Default = 00 This value is converted to a hexadecimal buffer and written into the PL eFUSE array when the write API is used. This value is the User Low Key given in string format. It must be two characters long; valid characters are 0-9,a-f, and A-F. Any other character is considered as an invalid string and will not burn the User Low Key. To write the User Low Key, XSK_EFUSEPL_PROGRAM_AES_AND_USER_LOW_KEY must have a value of TRUE.
XSK_EFUSEPL_USER_HIGH_KEY	Default = "000000" The default value is converted to a hexadecimal buffer and written into the PL eFUSE array when the write API is used. This value is the User High Key given in string format. The buffer must be six characters long: valid characters are 0-9,a-f, A-F. Any other character is considered to be an invalid string and does not burn User High Key. To write the User High Key, the XSK_EFUSEPL_PROGRAM_USER_HIGH_KEY must have a value of TRUE.

Zynq User-Configurable BBRAM Parameters

MIO Pins Used for PL JTAG Signals

The MIO pins shown in Table 8 are used for PL JTAG signals. These can be changed depending on your hardware

Table 8: **MIO Pins Used for PL JTAG Signals**

JTAG Signal	PIN Number
XSK_BBRAM_MIO_JTAG_TDI	17
XSK_BBRAM_MIO_JTAG_TDO	21
XSK_BBRAM_MIO_JTAG_TCK	19
XSK_BBRAM_MIO_JTAG_TMS	20

MUX Parameter

Table 9 shows the MUX parameter.

Table 9: **MUX Parameter**

Parameter	Default Value	Description
XSK_BBRAM_MIO_MUX_SEL_DEFAULT_VAL	LOW	Default value to enable the PL JTAG.

AES Key and Related Parameters

Table 10 shows the AES key and related parameters.

Table 10: **AES Key and Related Parameters**

Parameter Name	Default Value	Description
XSK_BBRAM_AES_KEY	XX	AES key (in HEX) that must be programmed into BBRAM.
XSK_BBRAM_AES_KEY_SIZE_IN_BITS	256	Size of AES key. Must be 256 bits.
XSK_BBRAM_PGM_OBFUSCATED_KEY	FALSE	Default value is FALSE. Setting the value to TRUE programs BBRAM with the Obfuscated key provided in XSK_BBRAM_OBFUSCATED_KEY, DPA protection feature cannot be enabled and the value provided in the XSK_BBRAM_DPA_PROTECT_ENABLE macro be ignored. Setting the value to FALSE programs BBRAM with key provided in XSK_BBRAM_AES_KEY and DPA protection can be enabled or disabled.
XSK_BBRAM_OBFUSCATED_KEY	XX	The Obfuscated key that must be programmed into BBRAM when XSK_BBRAM_PGM_OBFUSCATED_KEY is TRUE.
XSK_BBRAM_DPA_PROTECT_ENABLE	FALSE	Default value is False. Setting the value to TRUE will enable DPA protection for BBRAM key, values provided at XSK_BBRAM_DPA_COUNT and XSK_BBRAM_DPA_MODE will be considered otherwise they are ignored. DPA protection cannot be enable for Obfuscated key.

Table 10: **AES Key and Related Parameters *(Cont'd)***

Parameter Name	Default Value	Description
XSK_BBRAM_DPA_COUNT	0	Default value is 0. This value is considered only when macro XSK_BBRAM_DPA_PROTECT_ENABLE is TRUE. Valid range is 1 to 255.
XSK_BBRAM_DPA_MODE	XSK_BBRAM_INVALID_CONFIGURATIONS	Default value is XSK_BBRAM_INVALID_CONFIGURATIONS This value will be considered only when XSK_BBRAM_DPA_PROTECT_ENABLE is TRUE. Valid inputs are XSK_BBRAM_INVALID_CONFIGURATIONS or XSK_BBRAM_ALL_CONFIGURATIONS

User-Configurable eFuse Parameters of UltraScale

Table 11 shows the user-configurable eFuse parameters.

Table 11: **User-Configurable eFuse Parameters**

Parameter	Default Value	Description
XSK_EFUSEPL_DISABLE_AES_KEY_READ	FALSE	TRUE permanently disables AES CRC check and programming of the AES key. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_DISABLE_USER_KEY_READ	FALSE	TRUE permanently disables reading and programming of 32 bit User key. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_DISABLE_SECURE_READ	FALSE	TRUE permanently disables reading and programming of Secure bits. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_DISABLE_FUSE_CNTRL_WRITE	FALSE	Default = FALSE. TRUE permanently disables programming of Control bits FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_DISABLE_RSA_KEY_READ	FALSE	Default = FALSE. TRUE permanently disables reading and programming of RSA hash key. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_DISABLE_KEY_WRITE	FALSE	Default = FALSE. TRUE permanently disables programming of AES key FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_DISABLE_USER_KEY_WRITE	FALSE	Default = FALSE. TRUE permanently disables programming of 32 bit User key. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_DISABLE_SECURE_WRITE	FALSE	Default = FALSE. TRUE permanently disables programming of Secure bits FALSE does not affect the eFUSE bit.

Table 11: **User-Configurable eFuse Parameters *(Cont'd)***

Parameter	Default Value	Description
XSK_EFUSEPL_DISABLE_RSA_HASH_WRITE	FALSE	Default = FALSE. TRUE permanently disables programming of RSA key Hash. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_DISABLE_128BIT_USER_KEY_WRITE	FALSE	Default = FALSE. TRUE permanently disables programming 128 bit User key. FALSE does not affect the eFUSE bit
Secure bits		
XSK_EFUSEPL_ALLOW_ENCRYPTED_ONLY	FALSE	Default = FALSE. TRUE permanently forces to use only encrypted bitstreams. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_FORCE_USE_FUSE_AES_ONLY	FALSE	Default = FALSE. TRUE permanently forces to use secure boot with eFUSE key only. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_ENABLE_RSA_AUTH	FALSE	Default = **FALSE**. TRUE will permanently enable RSA authentication of bitstream. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_DISABLE_JTAG_CHAIN	FALSE	Default = FALSE. TRUE permanently sets the Ultrscale device in bypass mode. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_DISABLE_TEST_ACCESS	FALSE	Default = FALSE. TRUE permanently disables test access for UltraScale. FALSE does not affect the eFUSE bit.
XSK_EFUSEPL_DISABLE_AES_DECRYPTOR	FALSE	Default = FALSE. TRUE permanently disables AES decryptor. FALSE does not affect the eFUSE bit.

GPIO Pins Used for PL Master JTAG Signal

The following GPIO pins are used for PL master JTAG signals. These can be changed depending on your hardware. Table 12 shows the GPIO pins used for PL JTAG signals.

Table 12: **GPIO Pins Used for PL JTAG Signals**

Master JTAG Signal	PIN Number (Default)
XSK_EFUSEPL_AXI_GPIO_JTAG_TDO	0
XSK_EFUSEPL_AXI_GPIO_JTAG_TDI	0
XSK_EFUSEPL_AXI_GPIO_HWM_READY	1
XSK_EFUSEPL_AXI_GPIO_HWM_END	2
XSK_EFUSEPL_AXI_GPIO_JTAG_TMS	1
XSK_EFUSEPL_AXI_GPIO_JTAG_TCK	2
XSK_EFUSEPL_AXI_GPIO_HWM_START	3

GPIO Channels

Table 13 shows GPIO channel number.

Table 13: **GPIO Channel Numbers**

Parameter	Channel Number (Default)
XSK_EFUSEPL_GPIO_INPUT_CH	2
XSK_EFUSEPL_GPIO_OUTPUT_CH	1

Note: GPIO input (Master JTAG's TDO, Hardware module's READY and END) and output (Hardware module's START, Master JTAG's TDI, TMS and TCK) signals can belongs to same channel *or* inputs in one channel and outputs in the other channel. But some inputs in one channel and others in different channels are not accepted in this library.

Keys and Related Parameters

Table 14 shows AES key and related parameters.

Table 14: **AES Key and Related Parameters**

Parameter Name	Default Value	Description
XSK_EFUSEPL_PROGRAM_AES_KEY	FALSE	Default = FALSE If TRUE will program the AES key provided in the macro XSK_EFUSEPL_AES_KEY into eFUSE. FALSE ignores the provided values in XSK_EFUSEPL_AES_KEY
XSK_EFUSEPL_AES_KEY	0000000000000000000000000000000000000000000000000000000000000000	Default = 0000000000000000000000000000000000000000000000000000000000000000 This value converted to hex buffer and written into the PL eFUSE array when write API is used. This value should be the AES Key, given in string format. It must be 64 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered an invalid string and will not burn the AES key. To write AES key, XSK_EFUSEPL_PROGRAM _AES_ must have a value of TRUE.
XSK_EFUSEPL_CHECK_AES_KEY_CRC	FALSE	Default = FALSE If TRUE will perform CRC check of AES key with provided CRC of estimated AES key in macro XSK_EFUSEPL_CRC_OF_EXPECTED_AES_KEY FALSE ignores the provided values
XSK_EFUSEPL_CRC_OF_EXPECTED_AES_KEY	0x621C42AA	Default is 0x621C42AA. This is the 32 bit hexadecimal CRC value of AES key. 0x621C42AA is CRC of AES key all zeros. In this place have to provide CRC of AES key. The result will be saved in PL instance parameter AESKeyMatched

Table 15 shows 32 bit user key and related parameters.

Table 15: **32 bit User Key and Related Parameters**

Parameter Name	Default Value	Description
XSK_EFUSEPL_PROGRAM_USER_KEY	FALSE	Default = FALSE If TRUE will program the User key provided in the macro XSK_EFUSEPL_USER_KEY into eFUSE. FALSE ignores the provided values in XSK_EFUSEPL_USER_KEY
XSK_EFUSEPL_USER_KEY	00000000	This value converted to hex buffer and written into the PL eFUSE array when write API is used. This value should be the User Key, given in string format. It must be 8 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered an invalid string and will not burn User Key. To write **USER** Key, XSK_EFUSEPL_PROGRAM_USER_KEY_ must have a value of TRUE.
XSK_EFUSEPL_READ_USER_KEY	FALSE	Default = False. TRUE will read the 32 bit user key of eFUSE and store it in PL instance. **FALSE** will not read the 32 bit user key.

Table 16 shows 128 bit user key and related parameters.

Table 16: **128 bit User Key and Related Parameters**

Parameter Name	Default Value	Description
XSK_EFUSEPL_PROGRAM_USER_KEY_128BIT	FALSE	Default = FALSE If TRUE will program the 128 bit User key provided in the macros XSK_EFUSEPL_USER_KEY_128BIT_* into eFUSE FALSE ignores the provided values in XSK_EFUSEPL_USER_KEY_128BIT_*
XSK_EFUSEPL_USER_KEY_128BIT_0	00000000	This value converted to hex buffer and written into the PL eFUSE array when write API is called. This Value should be the User key, given in string format. It must be 8 character long. Valid characters are 0-9, a-f, A-F. Any other character is considered as invalid string and will not burn eFUSE. This macro holds 31:0 bits of 128 bit User key. To write 128 bit user key XSK_EFUSEPL_PROGRAM_USER_KEY_128BIT must have a value of TRUE.
XSK_EFUSEPL_USER_KEY_128BIT_1	00000000	This value converted to hex buffer and written into the PL eFUSE array when write API is called. This Value should be the User key, given in string format. It must be 8 character long. Valid characters are 0-9, a-f, A-F. Any other character is considered as invalid string and will not burn eFUSE. This macro holds 63:32 bits of 128 bit User key. To write 128 bit user key XSK_EFUSEPL_PROGRAM_USER_KEY_128BIT must have a value of TRUE.

Table 16: **128 bit User Key and Related Parameters *(Cont'd)***

Parameter Name	Default Value	Description
XSK_EFUSEPL_USER_KEY_128BIT_2	00000000	This value converted to hex buffer and written into the PL eFUSE array when write API is called. This Value should be the User key, given in string format. It must be 8 character long. Valid characters are 0-9, a-f, A-F. Any other character is considered as invalid string and will not burn eFUSE. This macro holds 95:64 bits of 128 bit User key. To write 128 bit user key XSK_EFUSEPL_PROGRAM_USER_KEY_128BIT must have a value of TRUE.
XSK_EFUSEPL_USER_KEY_128BIT_3	00000000	This value converted to hex buffer and written into the PL eFUSE array when write API is called. This Value should be the User key, given in string format. It must be 8 character long. Valid characters are 0-9, a-f, A-F. Any other character is considered as invalid string and will not burn eFUSE. This macro holds 127:96 bits of 128 bit User key. To write 128 bit user key XSK_EFUSEPL_PROGRAM_USER_KEY_128BIT must have a value of TRUE.
XSK_EFUSEPL_READ_USER_KEY128_BIT	FALSE	Default value is FALSE TRUE will read 128 bit user key of eFUSE and store it in PL instance. FALSE will not read the 12 bit user key.

Note: Single bit programming facility is provided for both 32 and 128 bit USER keys, library throws an error if user requested to program a non-zero bit to zero. For ease of use whole 128 bit of User key has broken into 4 macros.

Table 17 shows the RSA hash key and related parameters.

Table 17: **RSA Hash Key and Related Parameters**

Parameter Name	Default Value	Description
XSK_EFUSEPL_PROGRAM_RSA_KEY_HASH	FALSE	Default = FALSE If TRUE will program the RSA key hash provided in the macro XSK_EFUSEPL_RSA_KEY_HASH_VALUE into eFUSE. FALSE ignores the provided values in XSK_EFUSEPL_RSA_KEY_HASH_VALUE
XSK_EFUSEPL_RSA_KEY_HASH_VALUE	00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000000 00000000	Default = 0000000000000000000000000000000000000000000 0000000000000000000000000000000000000000000 000000000 This value converted to hex buffer and written into the PL eFUSE array when write API is used. This value should be the RSA Key hash, given in string format. It must be 96 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered an invalid string and will not burn RSA Key hash.To write RSA key hash, XSK_EFUSEPL_PROGRAM_RSA_KEY_HASH must have a value of TRUE.
XSK_EFUSEPL_READ_RSA_KEY_HASH	FALSE	Default = Read. TRUE will reads RSA key hash of eFUSE and stores in PL instance. FALSE will not read the user key.

User-Configurable BBRAM Parameters of UltraScale

Following parameters need to be configured. Based on your inputs, BBRAM is programmed with the provided AES key.

GPIO Pins Used for PL Master JTAG Signal

The following GPIO pins are used for PL master JTAG signals. These can be changed depending on your hardware. Table 18 shows the GPIO pins used for PL MASTER JTAG signals.

Table 18: **GPIO Pins Used for PL JTAG Signals**

Master JTAG Signal	PIN Number (Default)
XSK_BBRAM_AXI_GPIO_JTAG_TDO	0
XSK_BBRAM_AXI_GPIO_JTAG_TDI	0
XSK_BBRAM_AXI_GPIO_JTAG_TMS	1
XSK_EFUSEPL_AXI_GPIO_JTAG_TCK	2

GPIO Channels

Table 19 shows GPIO channel number.

Table 19: **GPIO Channel Numbers**

Parameter	Channel Number (Default)
XSK_BBRAM_GPIO_INPUT_CH	2
XSK_BBRAM_GPIO_OUTPUT_CH	1

Note: GPIO input (TDO) and output (TDI, TMS and TCK) signals can belongs to same channel *or* inputs in one channel and outputs in the other channel. But some inputs in one channel and others in different channels are not accepted in this library.

Keys and Related Parameters

Table 20 shows AES key and related parameters.

Table 20: **AES Key and Related Parameters**

Parameter Name	Default Value	Description
XSK_BBRAM_AES_KEY	XX	AES key (in HEX) that must be programmed into BBRAM.
XSK_BBRAM_AES_KEY_SIZE_IN_BITS	256	Size of AES key. Must be 256 bits.
XSK_BBRAM_PGM_OBFUSCATED_KEY	FALSE	Default = FALSE. when XSK_BBRAM_PGM_OBFUSCATED_KEY is FALSE, BBRAM is programmed with a non-obfuscated key provided in XSK_BBRAM_AES_KEY and DPA protection can be either in enabled/disabled state. If TRUE programs the BBRAM with key provided in XSK_BBRAM_OBFUSCATED_KEY and DPA protection cannot be enabled.
XSK_BBRAM_OBFUSCATED_KEY	XX	This is an Obfuscated key(in HEX) of length 256 bits that has to be programmed into BBRAM when XSK_BBRAM_PGM_OBFUSCATED_KEY is TRUE.

Table 21 shows DPA protection for BBRAM Key related parameters.

Note: Below inputs are valid only when BBRAM is programmed with a non-obfuscated key.

Table 21: **DPA Protection for BBRAM key**

Parameter Name	Default Value	Description
XSK_BBRAM_DPA_PROTECT_ENABLE	FALSE	Default = FALSE FALSE will not enable DPA protection. TRUE will enable DPA protection with provided DPA count and configuration in XSK_BBRAM_DPA_COUNT and XSK_BBRAM_DPA_MODE respectively. DPA protection cannot be enabled if BBRAM is programming with an Obfuscated key.
XSK_BBRAM_DPA_COUNT	0	This input is valid only when DPA protection is enabled. Valid range of values are 1 -255 when DPA protection is enabled else 0.
XSK_BBRAM_DPA_MODE	XSK_BBRAM_INVALID_CONFIGURATIONS	Default value is XSK_BBRAM_INVALID_CONFIGURATIONS when DPA protection is enabled DPA mode can be XSK_BBRAM_INVALID_CONFIGURATIONS or XSK_BBRAM_ALL_CONFIGURATIONS. If DPA protection is disabled this input value is ignored.

User-Configurable eFuse PS Parameters of Zynq UltraScale+ MPSoC

Table 22 shows the user-configurable eFuse parameters of Zynq UltraScale+ MPSoC.

Table 22: **User-Configurable eFuse PS Parameters of Zynq UltraScale+ MPSoC**

Parameter	Default Value	Description
XSK_EFUSEPS_AES_RD_LOCK	FALSE	TRUE permanently disables the CRC check of FUSE_AES. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_AES_WR_LOCK	FALSE	TRUE permanently disables the writing to FUSE_AES block. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPs_FORCE_USE_AES_ONLY	FALSE	TRUE permanently disables encrypted booting only using the Fuse key. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_BBRAM_DISABLE	FALSE	TRUE permanently disables the BBRAM key. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_ERR_OUTOF_PMU_DISABLE	FALSE	TRUE permanently disables the error output from the PMU. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_JTAG_DISABLE	FALSE	TRUE permanently disables JTAG controller. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_DFT_DISABLE	FALSE	TRUE permanently disables DFT boot mode. FALSE does not modify this control bit of eFuse.

Table 22: **User-Configurable eFuse PS Parameters of Zynq UltraScale+ MPSoC *(Cont'd)***

Parameter	Default Value	Description
XSK_EFUSEPS_PROG_GATE_0_DISABLE	FALSE	TRUE permanently disables PROG_GATE 0 feature in PPD. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_PROG_GATE_1_DISABLE	FALSE	TRUE permanently disables PROG_GATE 1 feature in PPD. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_PROG_GATE_2_DISABLE	FALSE	TRUE permanently disables PROG_GATE 2 feature in PPD. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_SECURE_LOCK	FALSE	TRUE permanently disables reboot into JTAG mode when doing a secure lockdown. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_RSA_ENABLE	FALSE	TRUE permanently disables RSA authentication during boot. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_PPK0_WR_LOCK	FALSE	TRUE permanently disables writing to PPK0 efuses. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_PPK0_REVOKE	FALSE	TRUE permanently revokes PPK0. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_PPK1_WR_LOCK	FALSE	TRUE permanently disables writing PPK1 efuses. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_PPK1_REVOKE	FALSE	TRUE permanently revokes PPK1. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_USER_WRLK_0	FALSE	TRUE permanently disables writing to USER_0 efuses. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_USER_WRLK_1	FALSE	TRUE permanently disables writing to USER_1 efuses. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_USER_WRLK_2	FALSE	TRUE permanently disables writing to USER_2 efuses. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_USER_WRLK_3	FALSE	TRUE permanently disables writing to USER_3 efuses. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_USER_WRLK_4	FALSE	TRUE permanently disables writing to USER_4 efuses. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_USER_WRLK_5	FALSE	TRUE permanently disables writing to USER_5 efuses. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_USER_WRLK_6	FALSE	TRUE permanently disables writing to USER_6 efuses. FALSE does not modify this control bit of eFuse.
XSK_EFUSEPS_USER_WRLK_7	FALSE	TRUE permanently disables writing to USER_7 efuses. FALSE does not modify this control bit of eFuse.

Keys and Related Parameters

Table 23 shows AES key and related parameters.

Table 23: **AES Key and Related Parameters**

Parameter Name	Default Value	Description
XSK_EFUSEPS_WRITE_AES_KEY	FALSE	Default = FALSE If TRUE, programs the AES key provided in the macro XSK_EFUSEPS_AES_KEY into eFUSE. FALSE ignores the provided values in XSK_EFUSEPL_AES_KEY
XSK_EFUSEPS_AES_KEY	0000000000000000000000000000000000000000000000000000000000000000	Default = 0000000000000000000000000000000000000000000000000000000000000000 This value converted to hex buffer and written into the PS eFUSE array when write API is used. This value should be the AES Key, given in string format. It must be 64 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered an invalid string and will not burn the AES key. To write AES key, XSK_EFUSEPS_WRITE_AES_KEY must have a value of TRUE

Single bit programming is allowed for all the USER fuses. If user requests to revert already programmed bit. Library throws an error. If user fuses is non-zero also library will not throw an error for valid requests

Table 24 shows user key and related parameters.

Table 24: **User Key and Related Parameters**

Parameter Name	Default Value	Description
XSK_EFUSEPS_WRITE_USER0_FUSE	FALSE	Default = FALSE If TRUE, programs the USER_0 key provided in the macro XSK_EFUSEPS_USER0_FUSES into eFUSE. FALSE ignores the provided value in XSK_EFUSEPS_USER0_FUSES.
XSK_EFUSEPS_USER0_FUSES	00000000	Default = 00000000 This value is converted to hex buffer and written into the PS eFUSE array when write API is used. This value should be the USER 0 key, given in string format. It must be 8 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered as invalid string and will not burn the USER 0 key. To program the key provided XSK_EFUSEPS_WRITE_USER0_FUSE must be TRUE.
XSK_EFUSEPS_WRITE_USER1_FUSE	FALSE	Default = FALSE If TRUE, programs the USER_1 key provided in the macro XSK_EFUSEPS_USER1_FUSES into eFUSE FALSE ignores the provided value in XSK_EFUSEPS_USER1_FUSES
XSK_EFUSEPS_USER1_FUSES	00000000	Default = 00000000 This value is converted to hex buffer and written into the PS eFUSE array when write API is used. This value should be the USER 1 key, given in string format. It must be 8 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered as invalid string and will not burn the USER 1 key. To program the key provided XSK_EFUSEPS_WRITE_USER1_FUSE must be TRUE.

Table 24: **User Key and Related Parameters *(Cont'd)***

Parameter Name	Default Value	Description
XSK_EFUSEPS_WRITE_USER2_FUSE	FALSE	Default = FALSE If TRUE, programs the USER_2 key provided in the macro XSK_EFUSEPS_USER2_FUSES into eFUSE. FALSE ignores the provided value in XSK_EFUSEPS_USER2_FUSES.
XSK_EFUSEPS_USER2_FUSES	00000000	Default = 00000000 This value is converted to hex buffer and written into the PS eFUSE array when write API is used. This value should be the USER 2 key, given in string format. It must be 8 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered as invalid string and will not burn the USER 2 key. To program the key provided XSK_EFUSEPS_WRITE_USER2_FUSE must be TRUE.
XSK_EFUSEPS_WRITE_USER3_FUSE	FALSE	Default = FALSE If TRUE, programs the USER_3 key provided in the macro XSK_EFUSEPS_USER3_FUSES into eFUSE. FALSE ignores the provided value in XSK_EFUSEPS_USER3_FUSES.
XSK_EFUSEPS_USER3_FUSES	00000000	Default = 00000000 This value is converted to hex buffer and written into the PS eFUSE array when write API is used. This value should be the USER 3 key, given in string format. It must be 8 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered as invalid string and will not burn the USER 3 key. To program the key provided XSK_EFUSEPS_WRITE_USER3_FUSE must be TRUE.
XSK_EFUSEPS_WRITE_USER4_FUSE	FALSE	Default = FALSE If TRUE, programs the USER_4 key provided in the macro XSK_EFUSEPS_USER4_FUSES into eFUSE. FALSE ignores the provided value in XSK_EFUSEPS_USER4_FUSES.
XSK_EFUSEPS_USER4_FUSES	00000000	Default = 00000000 This value is converted to hex buffer and written into the PS eFUSE array when write API is used. This value should be the USER 4 key, given in string format. It must be 8 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered as invalid string and will not burn the USER 4 key. To program the key provided XSK_EFUSEPS_WRITE_USER4_FUSE must be TRUE.
XSK_EFUSEPS_WRITE_USER5_FUSE	FALSE	Default = FALSE If TRUE, programs the USER_5 key provided in the macro XSK_EFUSEPS_USER5_FUSES into eFUSE. FALSE ignores the provided value in XSK_EFUSEPS_USER5_FUSES.

Table 24: **User Key and Related Parameters *(Cont'd)***

Parameter Name	Default Value	Description
XSK_EFUSEPS_USER5_FUSES	00000000	Default = 00000000 This value is converted to hex buffer and written into the PS eFUSE array when write API is used. This value should be the USER 5 key, given in string format. It must be 8 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered as invalid string and will not burn the USER 5 key. To program the key provided XSK_EFUSEPS_WRITE_USER5_FUSE must be TRUE.
XSK_EFUSEPS_WRITE_USER6_FUSE	FALSE	Default = FALSE If TRUE, programs the USER_6 key provided in the macro XSK_EFUSEPS_USER6_FUSES into eFUSE. FALSE ignores the provided value in XSK_EFUSEPS_USER6_FUSES.
XSK_EFUSEPS_USER6_FUSES	00000000	Default = 00000000 This value is converted to hex buffer and written into the PS eFUSE array when write API is used. This value should be the USER 6 key, given in string format. It must be 8 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered as invalid string and will not burn the USER 6 key. To program the key provided XSK_EFUSEPS_WRITE_USER6_FUSE must be TRUE.
XSK_EFUSEPS_WRITE_USER7_FUSE	FALSE	Default = FALSE If TRUE, programs the USER_7 key provided in the macro XSK_EFUSEPS_USER7_FUSES into eFUSE FALSE ignores the provided value.
XSK_EFUSEPS_USER7_FUSES	00000000	Default = 00000000 This value is converted to hex buffer and written into the PS eFUSE array when write API is used. This value should be the USER 7 key, given in string format. It must be 8 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered as invalid string and will not burn the USER 7 key. To program the key provided XSK_EFUSEPS_WRITE_USER7_FUSE must be TRUE.

Table 25 shows the PPK0 hash key and related parameters.

Table 25: **PPK0 Hash Key and Related Parameters**

Parameter Name	Default Value	Description
XSK_EFUSEPS_WRITE_PPK0_HASH	FALSE	Default = FALSE If TRUE, programs the PPK0 hash provided into the macro XSK_EFUSEPS_PPK0_HASH into eFUSE. FALSE ignores the provided values in XSK_EFUSEPS_PPK0_HASH
XSK_EFUSEPS_PPK0_IS_SHA3	TRUE	Default = TRUE If TRUE, XSK_EFUSEPS_PPK0_HASH is considered as SHA3 hash and hexa-decimal string should be of length 96 characters If FALSE, XSK_EFUSEPS_PPK0_HASH is considered as SHA2 hash and hexa-decimal string should be of length 64 characters
XSK_EFUSEPS_PPK0_HASH	000000000000000000000000000000000000000000000000	Default = 000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000 This value is converted to hex buffer and is written into the PS eFUSE array when write API is used. This value should be the USER Key, given in string format. It must be 96/64 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered an invalid string and will not burn the PPK0 hash. To write PPK0 hash, XSK_EFUSEPS_WRITE_PPK0_HASH must have a value of TRUE. By default PPK0 hash is of length 96 characters length, as XSK_EFUSEPS_PPK0_IS_SHA3 is TRUE One can also program PPK0 hash with SHA2 hash, for programming PPK0 hash with SHA2 hash, XSK_EFUSEPS_PPK0_IS_SHA3 should be FALSE and hash in XSK_EFUSEPS_PPK0_HASH should be length of 64 characters long.

Table 26 shows the PPK1 hash key and related parameters.

Table 26: **PPK1 Hash Key and Related Parameters**

Parameter Name	Default Value	Description
XSK_EFUSEPS_WRITE_PPK1_HASH	FALSE	Default = FALSE If TRUE, programs the PPK1 hash provided into the macro XSK_EFUSEPS_PPK1_HASH into eFUSE. FALSE ignores the provided values in XSK_EFUSEPS_PPK1_HASH

Table 26: **PPK1 Hash Key and Related Parameters *(Cont'd)***

Parameter Name	Default Value	Description
XSK_EFUSEPS_PPK1_IS_SHA3	FALSE	Default = FALSE If FALSE, XSK_EFUSEPS_PPK1_HASH is considered as SHA2 hash and hexa-decimal string should be of length 64 characters If TRUE, XSK_EFUSEPS_PPK1_HASH is considered as SHA3 hash and hexa-decimal string should be of length 96 characters
XSK_EFUSEPS_PPK1_HASH	000000000000000000000000000000000000000000000000000000000000	Default = 000000000000000000000000000000000000000000000000000000000000 This value converted to hex buffer and written into the PS eFUSE array when write API is used. This value should be the USER Key, given in string format. It must be 96/64 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered an invalid string and will not burn the PPK1 hash. To write PPK1 hash, XSK_EFUSEPS_WRITE_PPK1_HASH must have a value of TRUE. By default PPK1 hash is of length 64 characters length, as XSK_EFUSEPS_PPK1_IS_SHA3 is FALSE One can also program PPK1 hash with SHA3 hash, for programming PPK1 hash with SHA3 hash, XSK_EFUSEPS_PPK1_IS_SHA3 should be TRUE and hash in XSK_EFUSEPS_PPK1_HASH macro should be length of 96 characters long.

Table 27 shows the SPK ID and related parameters.

Table 27: **SPK ID and Related Parameters**

Parameter Name	Default Value	Description
XSK_EFUSEPS_WRITE_SPKID	FALSE	Default = FALSE If TRUE, programs the SPK ID provided in the macro XSK_EFUSEPS_SPK_ID into eFUSE. FALSE ignores the provided values in XSK_EFUSEPS_SPK_ID
XSK_EFUSEPS_SPK_ID	00000000	Default = 00000000 This value converted to hex buffer and written into the PS eFUSE array when write API is used. This value should be the SPK ID, given in string format. It must be 8 characters long. Valid characters are 0-9, a-f, A-F. Any other character is considered an invalid string and will not burn the SPK ID. To write SPK ID, XSK_EFUSEPS_WRITE_SPKID must have a value of TRUE

User-Configurable PUF Parameters of Zynq UltraScale+ MPSoC

Table 28 shows the user-configurable PUF parameters of Zynq UltraScale+ MPSoC.

Table 28: **PUF Registration and Programming Related Parameters**

Parameter	Default Value	Description
XSK_PUF_INFO_ON_UART	FALSE	TRUE displays PUF syndrome data on UART com port FALSE will not display any data on UART but data will be stored in InstancePtr.
XSK_PUF_PROGRAM_EFUSE	FALSE	TRUE will program the generated sydrome data, Black key, Chash and Auxilary values into eFUSE FALSE will not program any PUF related data into eFUSE
XSK_PUF_IF_CONTRACT_MANUFATURER	FALSE	This should be enabled when application is hand over to contract manufacturer. TRUE will allow only authenticated application. FALSE authentication is not mandatory.
XSK_PUF_REG_MODE	XSK_PUF_MODE4K	PUF registration is performed in 4K mode. Do not modify the value. Modifying the value will result in errors and unsuccessful PUF registration.
XSK_PUF_AES_KEY	"00000000000000000000000000000000000000000000000000000000000000000000000000000000"	The value mentioned in this will be converted to hex buffer and encrypts this with PUF helper data and generates a black key and written into the ZynqMP PS eFUSE array when XSK_PUF_PROGRAM_EFUSE macro is TRUE. This value should be given in string format. It should be 64 characters long, valid characters are 0-9,a-f,A-F. Any other character is considered as invalid string and will not burn AES Key. Note: Provided here should be red key and application calculates the black key and programs into eFUSE if XSK_PUF_PROGRAM_EFUSE macro is TRUE. To avoid programming eFUSE results can be displayed on UART com port by making XSK_PUF_INFO_ON_UART to TRUE.
XSK_PUF_IV	"000000000000000000000000"	The value mentioned here will be converted to hex buffer. This is Initialization vector(IV) which is used to generated black key with provided AES key and generated PUF key. This value should be given in string format. It should be 24 characters long, valid characters are 0-9,a-f,A-F. Any other character is considered as invalid string.

Table 29 shows the PUF secure bits related parameters.

Table 29: **PUF Secure Bits Related Parameters**

Parameter	Default Value	Description
XSK_PUF_READ_SECUREBITS	FALSE	TRUE will read status of the puf secure bits from eFUSE and will be displayed on UART. FALSE will not read secure bits.
XSK_PUF_PROGRAM_SECUREBITS	FALSE	TRUE will program PUF secure bits based on the user input provided at XSK_PUF_SYN_INVALID, XSK_PUF_SYN_WRLK and XSK_PUF_REGISTER_DISABLE FALSE will not program any PUF secure bits.
XSK_PUF_SYN_INVALID	FALSE	TRUE will permanently invalidates the already programmed syndrome data. FALSE will not modify anything

Table 29: **PUF Secure Bits Related Parameters *(Cont'd)***

Parameter	Default Value	Description
XSK_PUF_SYN_WRLK	FALSE	TRUE will permanently disables programming syndrome data into eFUSE. FALSE will not modify anything.
XSK_PUF_REGISTER_DISABLE	FALSE	TRUE permanently does not allows PUF syndrome data registration. FALSE will not modify anything.

Error Codes

The application error code is 32 bits long.

For example, if the error code for PS is `0x8A05`:

- `0x8A` indicates that a write error has occurred while writing RSA Authentication bit.
- `0x05` indicates that write error is due to the write temperature out of range.

Applications have the following options on how to show error status. Both of these methods of conveying the status are implemented by default. However, UART is required to be present and initialized for status to be displayed through UART.

- Send the error code through UART pins
- Write the error code in the reboot status register

PL eFUSE Error Codes

Table 30 shows the PL eFUSE error codes.PS eFUSE Error Codes

Table 30: **PL eFUSE Error Codes**

Error Code	Value	Description
XSK_EFUSEPL_ERROR_NONE	0	No error
EFUSE Read Error Codes		
XSK_EFUSEPL_ERROR_ROW_NOT_ZERO	0x10	Row is not zero
XSK_EFUSEPL_ERROR_READ_ROW_OUT_OF_RANGE	0x11	Row is out of range
XSK_EFUSEPL_ERROR_READ_MARGIN_OUT_OF_RANGE	0x12	Margin is out of range
XSK_EFUSEPL_ERROR_READ_BUFFER_NULL	0x13	No buffer
XSK_EFUSEPL_ERROR_READ_BIT_VALUE_NOT_SET	0x14	Bit not set
XSK_EFUSEPL_ERROR_READ_BIT_OUT_OF_RANGE	0x15	Bit is out of range
XSK_EFUSEPL_ERROR_READ_TEMPERATURE_OUT_OF_RANGE	0x16	Temperature obtained from XADC is out of range
XSK_EFUSEPL_ERROR_READ_VCCAUX_VOLTAGE_OUT_OF_RANGE	0x17	VCCAUX obtained from XADC is out of range
XSK_EFUSEPL_ERROR_READ_VCCINT_VOLTAGE_OUT_OF_RANGE	PL	VCCINT obtained from XADC is out of range
EFUSE Write Error Codes		
XSK_EFUSEPL_ERROR_WRITE_ROW_OUT_OF_RANGE	0x19	Row is out of range
XSK_EFUSEPL_ERROR_WRITE_BIT_OUT_OF_RANGE	0x1A	Bit is out of range

Table 30: **PL eFUSE Error Codes *(Cont'd)***

Error Code	Value	Description
XSK_EFUSEPL_ERROR_WRITE_TEMPERATURE_OUT_OF_RANGE	0x1B	Temperature obtained from XADC is out of range
XSK_EFUSEPL_ERROR_WRITE_VCCAUX_VOLTAGE_OUT_OF_RANGE	0x1C	VCCAUX obtained from XADC is out of range
XSK_EFUSEPL_ERROR_WRITE_VCCINT_VOLTAGE_OUT_OF_RANGE	0x1D	VCCINT obtained from XADC is out of range
XSK_EFUSEPL_ERROR_IN_PROGRAMMING_ROW	0x29	Error occured when programming row of eFUSE
XSK_EFUSEPL_ERROR_PRGRMG_ROWS_NOT_EMPTY	0x2A	Error when tried to program non Zero rows of eFUSE.
EFUSE Hardware module Error Codes		
XSK_EFUSEPL_ERROR_HWM_TIMEOUT	0x80	Error when hardware module is exceeded the time for programming eFUSE.
XSK_EFUSEPL_ERROR_USER_FUSE_REVERT	0x90	Error occurs when user requests to revert already programmed user eFUSE bit.
EFUSE CNTRL Error Codes		
XSK_EFUSEPL_ERROR_FUSE_CNTRL_WRITE_DISABLED	0x1E	Fuse control write is disabled
XSK_EFUSEPL_ERROR_CNTRL_WRITE_BUFFER_NULL	0x1F	Buffer pointer that is supposed to contain control data is null
EFUSE KEY Error Codes		
XSK_EFUSEPL_ERROR_NOT_VALID_KEY_LENGTH	0x20	Key length invalid
XSK_EFUSEPL_ERROR_ZERO_KEY_LENGTH	0x21	Key length zero
XSK_EFUSEPL_ERROR_NOT_VALID_KEY_CHAR	0x22	Invalid key characters
XSK_EFUSEPL_ERROR_NULL_KEY	0x23	Null key
XSK_EFUSEPL_ERROR_FUSE_SEC_WRITE_DISABLED	0x24	Secure bits write is disabled
XSK_EFUSEPL_ERROR_FUSE_SEC_READ_DISABLED	0x25	Secure bits reading is disabled
XSK_EFUSEPL_ERROR_SEC_WRITE_BUFFER_NULL	0x26	Buffer to write into secure block is NULL
XSK_EFUSEPL_ERROR_READ_PAGE_OUT_OF_RANGE	0x27	Page is out of range
XSK_EFUSEPL_ERROR_FUSE_ROW_RANGE	0x28	Row is out of range
XSKEfusepl_Program_Efuse() Error Codes		
XSK_EFUSEPL_ERROR_KEY_VALIDATION	0xF000	Invalid key
XSK_EFUSEPL_ERROR_PL_STRUCT_NULL	0x1000	Null PL structure
XSK_EFUSEPL_ERROR_JTAG_SERVER_INIT	0x1100	JTAG server initialization error
XSK_EFUSEPL_ERROR_READING_FUSE_CNTRL	0x1200	Error reading fuse control
XSK_EFUSEPL_ERROR_DATA_PROGRAMMING_NOT_ALLOWED	0x1300	Data programming not allowed
XSK_EFUSEPL_ERROR_FUSE_CTRL_WRITE_NOT_ALLOWED	0x1400	Fuse control write is disabled
XSK_EFUSEPL_ERROR_READING_FUSE_AES_ROW	0x1500	Error reading fuse AES row
XSK_EFUSEPL_ERROR_AES_ROW_NOT_EMPTY	0x1600	AES row is not empty
XSK_EFUSEPL_ERROR_PROGRAMMING_FUSE_AES_ROW	0x1700	Error programming fuse AES row

Table 30: **PL eFUSE Error Codes *(Cont'd)***

Error Code	Value	Description
XSK_EFUSEPL_ERROR_READING_FUSE_USER_DATA_ROW	0x1800	Error reading fuse user row
XSK_EFUSEPL_ERROR_USER_DATA_ROW_NOT_EMPTY	0x1900	User row is not empty
XSK_EFUSEPL_ERROR_PROGRAMMING_FUSE_DATA_ROW	0x1A00	Error programming fuse user row
XSK_EFUSEPL_ERROR_PROGRAMMING_FUSE_CNTRL_ROW	0x1B00	Error programming fuse control row
XSK_EFUSEPL_ERROR_XADC	0x1C00	XADC error
XSK_EFUSEPL_ERROR_INVALID_REF_CLK	0x3000	Invalid reference clock
XSK_EFUSEPL_ERROR_FUSE_SEC_WRITE_NOT_ALLOWED	0x1D00	Error in programming secure block
XSK_EFUSEPL_ERROR_READING_FUSE_STATUS	0x1E00	Error in reading FUSE status
XSK_EFUSEPL_ERROR_FUSE_BUSY	0x1F00	Fuse busy
XSK_EFUSEPL_ERROR_READING_FUSE_RSA_ROW	0x2000	Error in reading FUSE RSA block
XSK_EFUSEPL_ERROR_TIMER_INTIALISE_ULTRA	0x2200	Error in initiating Timer
XSK_EFUSEPL_ERROR_READING_FUSE_SEC	0x2300	Error in reading FUSE secure bits
XSK_EFUSEPL_ERROR_PRGRMG_FUSE_SEC_ROW	0x2500	Error in programming Secure bits of efuse
XSK_EFUSEPL_ERROR_PRGRMG_RSA_HASH	0x8000	Error in programming RSA hash
XSK_EFUSEPL_ERROR_PRGRMG_128BIT_USER_KEY	0x5000	Error in programming 128 bit User key
XSK_EFUSEPL_ERROR_PRGRMG_USER_KEY	0x4000	Error in programming 32 bit user key

Table 31 shows the PS eFUSE error codes. These error codes are applicable for both Zynq and Zynq UltraScale+ MPSoC eFUSE PS.

Table 31: **PS eFUSE Error Codes**

Error Code	Value	Description
XSK_EFUSEPL_ERROR_NONE	0	No error
EFUSE Read Error Codes		
XSK_EFUSEPS_ERROR_ADDRESS_XIL_RESTRICTED	0x01	Address is restricted
XSK_EFUSEPS_ERROR_READ_TMEPERATURE_OUT_OF_RANGE	0x02	Temperature obtained from XADC is out of range
XSK_EFUSEPS_ERROR_READ_VCCAUX_VOLTAGE_OUT_OF_RANGE	0x03	VCCAUX obtained from XADC is out of range
XSK_EFUSEPS_ERROR_READ_VCCINT_VOLTAGE_OUT_OF_RANGE	0x04	VCCINT obtained from XADC is out of range
XSK_EFUSEPS_ERROR_READ	0x00B0	Error in reading rows
EFUSE Write Error Codes		
XSK_EFUSEPS_ERROR_WRITE_TEMPERATURE_OUT_OF_RANGE	0x05	Temperature obtained from XADC is out of range
XSK_EFUSEPS_ERROR_WRITE_VCCAUX_VOLTAGE_OUT_OF_RANGE	0x06	VCCAUX obtained from XADC is out of range
XSK_EFUSEPS_ERROR_WRITE_VCCINT_VOLTAGE_OUT_OF_RANGE	0x07	VCCINT obtained from XADC is out of range

Table 31: **PS eFUSE Error Codes *(Cont'd)***

Error Code	Value	Description
XSK_EFUSEPS_ERROR_VERIFICATION	0x08	Verification error
XSK_EFUSEPS_ERROR_RSA_HASH_ALREADY_PROGRAMMED	0x09	RSA hash was already programmed
XSK_EFUSEPS_ERROR_AES_ALREADY_PROGRAMMED	0x12	AES key is already programmed
XSK_EFUSEPS_ERROR_SPKID_ALREADY_PROGRAMMED	0x13	SPK ID is already programmed
XSK_EFUSEPS_ERROR_PPK0_HASH_ALREADY_PROGRAMMED	0x14	PPK0 hash is already programmed
XSK_EFUSEPS_ERROR_PPK1_HASH_ALREADY_PROGRAMMED	0x15	PPK1 hash is already programmed
EFUSE CNTRL Error Codes		
XSK_EFUSEPS_ERROR_CONTROLLER_MODE	0x0A	Controller mode error
XSK_EFUSEPS_ERROR_REF_CLOCK	0x0B	Reference clock not between 20 to 60 MHz
XSK_EFUSEPS_ERROR_READ_MODE	0x0C	Not supported read mode
XADC Error Codes		
XSK_EFUSEPS_ERROR_XADC_CONFIG	0x0D	XADC configuration error
XSK_EFUSEPS_ERROR_XADC_INITIALIZE	0x0E	XADC initialization error
XSK_EFUSEPS_ERROR_XADC_SELF_TEST	0x0F	XADC self-test failed
Utils Error Codes		
XSK_EFUSEPS_ERROR_PARAMETER_NULL	0x10	Passed parameter null
XSK_EFUSEPS_ERROR_STRING_INVALID	0x20	Passed string is invalid
XSKEfuse_Write/Read()common Error Codes		
XSK_EFUSEPS_ERROR_PS_STRUCT_NULL	0x8100	PS structure pointer is null
XSK_EFUSEPS_ERROR_XADC_INIT	0x8200	XADC initialization error
XSK_EFUSEPS_ERROR_CONTROLLER_LOCK	0x8300	PS eFUSE controller is locked
XSK_EFUSEPS_ERROR_EFUSE_WRITE_PROTECTED	0x8400	PS eFUSE is write protected
XSK_EFUSEPS_ERROR_CONTROLLER_CONFIG	0x8500	Controller configuration error
XSK_EFUSEPS_ERROR_PS_PARAMETER_WRONG	0x8600	PS eFUSE parameter is not TRUE/FALSE
XSKEfusePs_Write() Error Codes		
XSK_EFUSEPS_ERROR_WRITE_128K_CRC_BIT	0x9100	Error in enabling 128K CRC
XSK_EFUSEPS_ERROR_WRITE_RSA_HASH	0x9400	Error in writing RSA key
XSK_EFUSEPS_ERROR_WRITE_RSA_AUTH_BIT	0x9500	Error in enabling RSA authentication bit
XSK_EFUSEPS_ERROR_WRITE_WRITE_PROTECT_BIT	0x9600	Error in writing write-protect bit
XSK_EFUSEPS_ERROR_READ_HASH_BEFORE_PROGRAMMING	0x9700	Check RSA key before trying to program
XSK_EFUSEPS_ERROR_WRTIE_DFT_JTAG_DIS_BIT	0x9800	Error in programming DFT JTAG disable bit
XSK_EFUSEPS_ERROR_WRTIE_DFT_MODE_DIS_BIT	0x9900	Error in programming DFT MODE disable bit
XSK_EFUSEPS_ERROR_WRONG_TBIT_PATTERN	0xA200	Error in programming TBIT pattern
XSK_EFUSEPS_ERROR_WRITE_AES_KEY	0xA300	Error in programming AES key

Table 31: **PS eFUSE Error Codes *(Cont'd)***

Error Code	Value	Description
XSK_EFUSEPS_ERROR_WRTIE_AES_CRC_LK_BIT	0x9A00	Error in enabling AES's CRC check lock
XSK_EFUSEPS_ERROR_WRTIE_AES_WR_LK_BIT	0x9B00	Error in programming AES write lock bit
XSK_EFUSEPS_ERROR_WRTIE_USE_AESONLY_EN_BIT	0x9C00	Error in programming use AES only bit
XSK_EFUSEPS_ERROR_WRTIE_BBRAM_DIS_BIT	0x9D00	Error in programming BBRAM disable bit
XSK_EFUSEPS_ERROR_WRTIE_PMU_ERR_DIS_BIT	0x9E00	Error in programming PMU error disable bit
XSK_EFUSEPS_ERROR_WRTIE_JTAG_DIS_BIT	0x9F00	Error in programming JTAG disable bit
XSK_EFUSEPS_ERROR_WRITE_SPK_ID	0xA400	Error in programming SPK ID
XSK_EFUSEPS_ERROR_WRITE_USER_KEY	0xA500	Error in programming User Key
XSK_EFUSEPS_ERROR_WRITE_PPK0_HASH	0xA600	Error in programming PPK 0 hash
XSK_EFUSEPS_ERROR_WRITE_PPK1_HASH	0xA700	Error in programming PPK 1 hash
XSK_EFUSEPS_ERROR_BEFORE_PROGRAMMING	0x80	Error occurred before programming
XSK_EFUSEPS_ERROR_PROGRAMMING_TBIT_PATTERN	0x16	Error in programming TBITS
XSK_EFUSEPS_ERROR_CACHE_LOAD	0xB000	Error in re-loading CACHE
XSK_EFUSEPS_ERROR_WRITE_USER0_FUSE	0xC000	Error in programming USER 0 Fuses
XSK_EFUSEPS_ERROR_WRITE_USER1_FUSE	0xC100	Error in programming USER 1 Fuses
XSK_EFUSEPS_ERROR_WRITE_USER2_FUSE	0xC200	Error in programming USER 2 Fuses
XSK_EFUSEPS_ERROR_WRITE_USER3_FUSE	0xC300	Error in programming USER 3 Fuses
XSK_EFUSEPS_ERROR_WRITE_USER4_FUSE	0xC400	Error in programming USER 4 Fuses
XSK_EFUSEPS_ERROR_WRITE_USER5_FUSE	0xC500	Error in programming USER 5 Fuses
XSK_EFUSEPS_ERROR_WRITE_USER6_FUSE	0xC600	Error in programming USER 6 Fuses
XSK_EFUSEPS_ERROR_WRITE_USER7_FUSE	0xC700	Error in programming USER 7 Fuses
XSK_EFUSEPS_ERROR_WRTIE_USER0_LK_BIT	0xC800	Error in programming USER 0 fuses lock bit
XSK_EFUSEPS_ERROR_WRTIE_USER1_LK_BIT	0xC900	Error in programming USER 1 fuses lock bit
XSK_EFUSEPS_ERROR_WRTIE_USER2_LK_BIT	0xCA00	Error in programming USER 2 fuses lock bit
XSK_EFUSEPS_ERROR_WRTIE_USER3_LK_BIT	0xCB00	Error in programming USER 3 fuses lock bit
XSK_EFUSEPS_ERROR_WRTIE_USER4_LK_BIT	0xCC00	Error in programming USER 4 fuses lock bit
XSK_EFUSEPS_ERROR_WRTIE_USER5_LK_BIT	0xCD00	Error in programming USER 5 fuses lock bit
XSK_EFUSEPS_ERROR_WRTIE_USER6_LK_BIT	0xCE00	Error in programming USER 6 fuses lock bit
XSK_EFUSEPS_ERROR_WRTIE_USER7_LK_BIT	0xCF00	Error in programming USER 7 fuses lock bit
XSK_EFUSEPS_ERROR_WRTIE_PROG_GATE0_DIS_BIT	0xD000	Error in programming PROG_GATE0 disabling bit

Table 31: **PS eFUSE Error Codes *(Cont'd)***

Error Code	Value	Description
XSK_EFUSEPS_ERROR_WRTIE_PROG_GATE1_DIS_BIT	0xD100	Error in programming PROG_GATE1 disabling bit
XSK_EFUSEPS_ERROR_WRTIE_PROG_GATE2_DIS_BIT	0xD200	Error in programming PROG_GATE2 disabling bit
XSK_EFUSEPS_ERROR_WRTIE_SEC_LOCK_BIT	0xD300	Error in programming SEC_LOCK bit
XSK_EFUSEPS_ERROR_WRTIE_PPK0_WR_LK_BIT	0xD400	Error in programming PPK0 write lock bit
XSK_EFUSEPS_ERROR_WRTIE_PPK0_RVK_BIT	0xD500	Error in programming PPK0 revoke bit
XSK_EFUSEPS_ERROR_WRTIE_PPK1_WR_LK_BIT	0xD600	Error in programming PPK1 write lock bit
XSK_EFUSEPS_ERROR_WRTIE_PPK1_RVK_BIT	0xD700	Error in programming PPK0 revoke bit
XSK_EFUSEPS_ERROR_FUSE_PROTECTED	0x00080000	Error when attempted to program a write locked fuse
XSK_EFUSEPS_ERROR_USER_BIT_CANT_REVERT	0x00800000	Error when already programmed bit(1) is requested to revert (0). This error only occurs for User_Fuses, as single bit programming is allowed only for User fuses
XSKEfusePs_Read() Error Codes		
XSK_EFUSEPS_ERROR_READ_RSA_HASH	0xA100	Error in reading RSA key

Table 32 shows the PUF error codes for Zynq UltraScale+ MPSoC.

Table 32: **PUF Error Codes**

Error Code	Value	Description
XSK_EFUSEPS_ERROR_WRITE_PUF_SYN_INVLD	0xD800	Error while programming invalidate the PUF syndrome data bit
XSK_EFUSEPS_ERROR_WRITE_PUF_SYN_WRLK	0xD900	Error while programming Syndrome write lock bit
XSK_EFUSEPS_ERROR_WRITE_PUF_SYN_REG_DIS	0xDA00	Error while programming PUF syndrome register disable bit
XSK_EFUSEPS_ERROR_PUF_INVALID_REG_MODE	0xE000	Error when PUF registration is requested with invalid registration mode
XSK_EFUSEPS_ERROR_PUF_REG_WO_AUTH	0xE100	Error when authentication is not enabled
XSK_EFUSEPS_ERROR_PUF_REG_DISABLED	0xE200	Error when trying to do PUF registration and when PUF registration is disabled
XSK_EFUSEPS_ERROR_PUF_INVALID_REQUEST	0xE300	Error when an invalid mode is requested
XSK_EFUSEPS_ERROR_PUF_DATA_ALREADY_PROGRAMMED	0xE400	Error when PUF is already programmed in eFUSE
XSK_EFUSEPS_ERROR_PUF_DATA_OVERFLOW	0xE500	Error when an over flow occurs

Table 33 shows the BBRAM error codes for Zynq UltraScale+ MPSoC.

Table 33: **BBRAM Error Codes for Zynq UltraScale+ MPSoC**

Error Code	Value	Description
XSK_ZYNQMP_BBRAMPS_ERROR_IN_PRGRMG_ENABLE	0x01	Error in programming enable
XSK_ZYNQMP_BBRAMPS_ERROR_IN_CRC_CHECK	0xB000	Error in CRC check after programming AES key
XSK_ZYNQMP_BBRAMPS_ERROR_IN_PRGRMG	0xC000	Error in programming AES key

Status Code

For Zynq and UltraScale in `xilskey_efuse_example.c` the status is conveyed through a UART or reboot status register in the following format:

`0xYYYYZZZZ`, where:

- `YYYY` Represents the PS eFUSE Status.
- `ZZZZ` Represents the PL eFUSE Status.

Error codes are as described in Table 30, and Table 31. Table 34 shows the status codes.

Table 34: **Status Codes**

Status Code Value	Description
0x0000ZZZZ	Represents PS eFUSE is successful and PL eFUSE process returned with error.
0xYYYY0000	Represents PL eFUSE is successful and PS eFUSE process returned with error.
0xFFFF0000	Represents PS eFUSE is not initiated and PL eFUSE is successful.
0x0000FFFF	Represents PL eFUSE is not initiated and PS eFUSE is successful.
0xFFFFZZZZ	Represents PS eFUSE is not initiated and PL eFUSE is process returned with error.
0xYYYYFFFF	Represents PL eFUSE is not initiated and PS eFUSE is process returned with error.

For Zynq UltraScale+ MPSoC in `xilskey_bbramps_zynqmp_example.c`, `xilskey_puf_registration.c` and `xilskey_efuseps_zynqmp_example.c` files, the status is conveyed as 32 bit error code.

Where Zero represents that no error has occurred and if the value is other than Zero, a 32 bit error code is returned.

Procedures

eFUSE Writing Procedure Running from DDR as an Application

This sequence is same as the existing flow described below.

1. Provide the required inputs in `xilskey_input.h`, then compile the SDK project.
2. Take the latest FSBL (ELF), stitch the `<output>.elf` generated to it (using the bootgen utility), and generate a bootable image.
3. Write the generated binary image into the flash device (for example: QSPI, NAND).
4. To burn the eFUSE key bits, execute the image.

eFUSE Driver Compilation Procedure for OCM

1. Open the linker script (`lscript.ld`) in the SDK project.
2. Map all the sections to point to `ps7_ram_0_S_AXI_BASEADDR` instead of `ps7_ddr_0_S_AXI_BASEADDR`.

   Example: Click the **Memory Region** tab for the `.text` section and select **ps7_ram_0_S_AXI_BASEADDR** from the drop-down list.
3. Copy the `ps7_init.c` and `ps7_init.h` files from the `hw_platform` folder into the `example` folder.
4. In `"xilskey_efuse_example.c`, un-comment the code that calls the `"ps7_init()"` routine".
5. Compile the project.

   The `<Project name>.elf` file is generated and is executed out of OCM.

When executed, this example displays the success/failure of the eFUSE application in a display message via UART (if UART is present and initialized) or the reboot status register.

Status/Error codes are as described in Error Codes.

UltraScale eFUSE Access Procedure

Accessing UltraScale MicroBlaze eFuse is done by using block RAM initialization. Ultrascale eFUSE programming is done through MASTER JTAG. Crucial Programming sequence will be taken care by Hardware module. So Hardware module should be added compulsory in the design. Using hardware module's vhd code and instructions provided to add Hardware module in the design is recommended.

- You need to add the Master JTAG primitive to design, that is, the MASTER_JTAG_inst instantiation has to be performed and AXI GPIO pins have to be connected to TDO, TDI, TMS and TCK signals of the MASTER_JTAG primitive.
- Along with master JTAG, hardware module(HWM) has to be added in design and it's signals XSK_EFUSEPL_AXI_GPIO_HWM_READY , XSK_EFUSEPL_AXI_GPIO_HWM_END and XSK_EFUSEPL_AXI_GPIO_HWM_START, needs to be connected to AXI GPIO pins to communicate with HWM.
- All inputs (Master JTAG's TDO and HWM's HWM_READY, HWM_END) and all outputs (Master Jtag's TDI, TMS, TCK and HWM's HWM_START) can be connected in one channel (or) inputs in one channel and outputs in other channel.
- Some of the outputs of GPIO in one channel and some others in different channels are not supported.
- The design should contain AXI BRAM Ctrl memory mapped (1MB).

Note: MASTER_JTAG will disable all other JTAGs

The procedure is as follows:

1. After providing the required inputs in `xilskey_input.h`, compile the project.

2. Generate a memory mapped interface file using TCL command `write_mem_info $Outfilename`
3. Update memory has to be done using the tcl command `updatemem`.

```
updatemem -meminfo $file.mmi -data $Outfilename.elf -bit $design.bit
-proc design_1_i/microblaze_0 -out $Final.bit
```

4. Program the board using `$Final.bit` bitstream
5. Output can be seen in UART terminal.
6. For calculating CRC of AES key reverse polynomial is `0x82F63B78` or you can use the API u32 Xilskey_CrcCalculation(u8 *Key)

UltraScale BBRAM Access Procedure

Accessing UltraScale MicroBlaze BBRAM is done by using block RAM initialization.

- You need to add the Master JTAG primitive to your design, that is, the MASTER_JTAG_inst instantiation has to be performed and AXI GPIO pins have to be connected to TDO, TDI, TMS and TCK signals of the MASTER_JTAG primitive.
- All inputs (TDO) and all outputs (TDI, TMS, TCK) of MASTER_JTAG can be connected in one channel (or) inputs in one channel and outputs in other channel.
- Some of the outputs of GPIO in one channel and some others in different channels are not supported.
- The design should contain AXI BRAM Ctrl memory mapped (1MB).

Note: MASTER_JTAG will disable all other JTAGs

The procedure is as follows:

1. After providing the required inputs in xilskey_bbram_ultrascale_input.h, compile the project.
2. Generate a memory mapped interface file using TCL command write_mem_info $Outfilename
3. Update memory has to be done using the tcl command updatemem:

```
updatemem -meminfo $file.mmi -data $Outfilename.elf -bit $design.bit
-proc design_1_i/microblaze_0 -out $Final.bit
```

4. Program the board using $Final.bit bitstream
5. Output can be seen in UART terminal.

LibXil SKey Library APIs

This section provides linked summary and detailed descriptions of the LibXil SKey library APIs.

API Summary

The following is a summary list of APIs provided by the LibXil SKey library. Descriptions of the APIs follow the list.

u32 XilSKey_EfusePs_Write (XilSKey_EPs *InstancePtr)

u32 XilSKey_EfusePs_Read(XilSKey_EPs *InstancePtr)

u32 XilSKey_EfusePl_Program (XilSKey_EPl *InstancePtr)

u32 XilSKey_EfusePs_ReadStatus(XilSKey_EPs *InstancePtr, u32 *StatusBits);

u32 XilSKey_EfusePl_ReadStatus(XilSKey_EPl *InstancePtr, u32 *StatusBits);

u32 XilSKey_EfusePl_ReadKey(XilSKey_EPl *InstancePtr);

u32 XilSKey_EfusePs_Write (XilSKey_EPs *InstancePtr)

Parameters	InstancePtr: The pointer to the PS eFUSE handler that describes which PS eFUSE bit should be burned.
Returns	XST_SUCCESS on success. In case of error, value is as defined in xilskey_utils.h. The error value is a combination of an upper 8-bit value and a lower 8-bit value. For example, 0x8A03 should be checked in xilskey_utils.h as 0x8A00 and 0x03. The upper 8-bit value signifies the major error, and the lower 8-bit value provides more detail about the error.
Description	When called, this API • Initializes the timer, XADC subsystems. • Unlocks the PS eFUSE controller. • Configures the PS eFUSE controller. • Writes the hash and control bits if requested. • Programs the PS eFUSE to enable the RSA authentication if requested. • Locks the PS eFUSE controller. Returns an error if: • The reference clock frequency is not in between 20 and 60 MHz. • The system not in a position to write the requested PS eFUSE bits (because the bits are already written or not allowed to write) • The temperature and voltage are not within range
Includes	xilskey_eps.h, xilskey_epshw.h, xilskey_utils.h

u32 XilSKey_EfusePs_Read(XilSKey_EPs *InstancePtr)

Parameters	InstancePtr: The pointer to the PS eFUSE handler.
Returns	XST_SUCCESS on success. In case of error, the value is as defined in xilskey_utils.h. The error value is a combination of an upper 8-bit value and a lower 8-bit value. For example, 0x8A03 should be checked in xilskey_utils.h as 0x8A00 and 0x03. The upper 8-bit value signifies the major error and the lower 8-bit values provides more detail about the error.
Description	When called: • This API initializes the timer, XADC subsystems. • Unlocks the PS eFUSE Controller. • Configures the PS eFUSE Controller and enables read-only mode. • Reads the PS eFUSE (Hash Value), and enables read-only mode. • Locks the PS eFUSE Controller. Returns error if: • The reference clock frequency is not in between 20 and 60MHz. • Unable to unlock PS eFUSE controller or requested address corresponds to restricted bits. • Temperature and voltage are not within range
Includes	xilskey_eps.h, xilskey_epshw.h, xilskey_utils.h

u32 XilSKey_EfusePl_Program (XilSKey_EPl *InstancePtr)

Parameters	InstancePtr is input data to be written to PL eFUSE

Returns XST_SUCCESS on success.
In case of error, the value is defined in xilskey_utils.h. The error value is a combination of the upper 8-bit value and lower 8-bit value. For example, 0x8A03 should be checked in xilskey_utils.h as 0x8A00 and 0x03. The upper 8-bit value signifies the major error, and the lower 8-bit value provides more detail.

Description When called, this API:
- Initializes the timer, XADC and JTAG server subsystems.
- Writes the AES & User Keys if requested.
- Writes the Control Bits if requested.
- In UltraScale, it also programs the RSA key Hash

Returns an error if:
- The reference clock frequency is not in between 20 and 60 MHz.
- The PL DAP ID is not identified.
- The system is not in a position to write the requested PL eFUSE bits (because the bits are already written or not allowed to write)
- Temperature and voltage are not within range.

Includes xilskey_utils.h, xilskey_epl.h

---

u32 XilSKey_EfusePs_ReadStatus(XilSKey_EPs *InstancePtr, u32 *StatusBits);

Parameters
- InstancePtr - Pointer to PS eFUSE instance
- StatusBits - Buffer to store status register value

Returns XST_SUCCESS on success.
On failure, returns error codes as described in "Error Codes," page 23.

Description This API unlocks the controller and reads the PS eFUSE status register.

Includes xilskey_eps.h, xilskey_utils.h

---

u32 XilSKey_EfusePl_ReadStatus(XilSKey_EPl *InstancePtr, u32 *StatusBits);

Parameters
- InstancePtr - Pointer to PL eFUSE instance
- StatusBits - Buffer to store status bits

Returns XST_SUCCESS on success.
On failure, returns error codes as described in "Error Codes," page 23.

Description This API reads the status bits from row 0. It initializes the timer, XADC and JTAG server subsystems, if not already done so. In UltraScale it reads the Status register and gets all the secure and control bits.

Includes xilskey_epl.h, xilskey_utils.h

---

u32 XilSKey_EfusePl_ReadKey(XilSKey_EPl *InstancePtr);

Parameters InstancePtr - Pointer to PL eFUSE instance

Returns XST_SUCCESS on success.
On failure, returns error codes as described in "Error Codes," page 23.

Description	This API reads the AES and user key and stores them in the corresponding arrays in instance structure. It initializes the timer, XADC and JTAG server subsystems, if not already done so. In UltraScale eFuse, this API performs same as the above but reads extra key RSA key hash.
Includes	`xilskey_epl.h, xilskey_utils.h`

BBRAM API Description

This section provides a linked summary and detailed descriptions of the battery-backed RAM (BBRAM) APIs.

API Summary

`int XilSKey_Bbram_Program(XilSKey_Bbram *InstancePtr)`

Parameters	BBRAM instance pointer
Returns	`XST_SUCCESS` on success, or `XST_FAILURE` on failure.
Description	API to program and verify the key. This API can be used to program BBRAM of either Zynq Zynq® or UltraScale™.
Includes	`xilskey_utils.h`, `xilskey_bbram.h`

Important! This API performs BBRAM program and verify together. This is how the BBRAM algorithm works and it is not possible to do program/verify operations independently.

Zynq UltraScale+ MPSoC API Description

This section provides linked summary and detailed descriptions of the Zynq UltraScale+ MPSoC eFUSE and battery-backed RAM (BBRAM) APIs.

BBRAM PS API Summary

The following is a summary list of BBRAM PS APIs for Zynq UltraScale+ MPSoC. Descriptions of the APIs follow the list.

- u32 XilSKey_ZynqMp_Bbram_Program(u32 *AesKey)
- void XilSKey_ZynqMp_Bbram_Zeroise()

`u32 XilSKey_ZynqMp_Bbram_Program(u32 *AesKey)`

Parameters	Aes Key is a pointer to an array which holds AES key to be programmed.
Returns	XST_SUCCESS if programming and verification is done successfully. ErrorCode if it fails to program.
Description	This API programs the Zynq UltraScale+ MPSoc's BBRAM key with the provided key and also performs CRC check of programmed key.
Includes	`xilskey_utils.h, xilskey_bbram.h`

`void XilSKey_ZynqMp_Bbram_Zeroise()`

Parameters	None.
Returns	XST_SUCCESS if programming and verification is done successfully. ErrorCode if it fails to program.

Description	This API zeroises the key programmed in BBRAM.
Includes	`xilskey_utils.h, xilskey_bbram.h`

eFUSE PS API Summary

The following is a summary list of eFUSE APIs for Zynq UltraScale+ MPSoC. Descriptions of the APIs follow the list.

- u32 XilSKey_ZynqMp_EfusePs_CheckAesKeyCrc(u32 CrcValue)
- u32 XilSKey_ZynqMp_EfusePs_ReadUserFuse(u32 *UseFusePtr, u8 UserFuse_Num, u8 ReadOption)
- u32 XilSKey_ZynqMp_EfusePs_ReadPpk0Hash(u32 *Ppk0Hash, u8 ReadOption)
- u32 XilSKey_ZynqMp_EfusePs_ReadPpk1Hash(u32 *Ppk1Hash, u8 ReadOption)
- u32 XilSKey_ZynqMp_EfusePs_ReadSpkId(u32 *SpkId, u8 ReadOption)
- void XilSKey_ZynqMp_EfusePs_ReadDna(u32 *DnaRead)
- u32 XilSKey_ZynqMp_EfusePs_ReadSecCtrlBits(XilSKey_SecCtrlBits *ReadBackSecCtrlBits, u8 ReadOption)
- u32 XilSKey_ZynqMp_EfusePs_CacheLoad()
- u32 XilSKey_ZynqMp_EfusePs_Write(XilSKey_ZynqMpEPs *InstancePtr)
- u32 XilSKey_CrcCalculation(u8 *Key)
- u32 XilSkey_CrcCalculation_AesKey(u8 *Key)

`u32 XilSKey_ZynqMp_EfusePs_CheckAesKeyCrc(u32 CrcValue)`

Parameters	CrcValue is the CRC of expected AES key.
Returns	XST_SUCCESS if CRC check is passed. XST_FAILURE if CRC check is failed.
Description	This API performs the CRC check of eFUSE's AES key.
Includes	`xilskey_utils.h, xilskey_eps_zynqmp.h`

`u32 XilSKey_ZynqMp_EfusePs_ReadUserFuse(u32 *UseFusePtr, u8 UserFuse_Num, u8 ReadOption)`

Parameters	UseFusePtr is a pointer to an array which holds the readback userkey in. UserFuse_Num is a u8 variable which holds the USER FUSE number which needs to be read. ReadOption is a u8 variable which has to be provided by user based on which the input reading happens from cache or from efuse array. • 0 - Reads from cache • 1 - Reads from efuse array
Returns	XST_SUCCESS if key is read successfully. ErrorCode if it fails to read eFUSE user key.
Description	This API reads User key from eFUSE memory or Cache based on user input and stores in UseKeyPtr.
Includes	`xilskey_utils.h, xilskey_eps_zynqmp.h`

u32 XilSKey_ZynqMp_EfusePs_ReadPpk0Hash(u32 *Ppk0Hash, u8 ReadOption)

Parameters	Ppk0Hash is a pointer to an array which holds the readback PPK0 hash in. ReadOption is a u8 variable which has to be provided by user based on which the input reading happens from cache or from efuse array. • 0 - Reads from cache • 1 - Reads from efuse array
Returns	XST_SUCCESS if key is read successfully. ErrorCode if it fails to read PPK0 hash of eFUSE.
Description	This API reads PPK0 hash from eFUSE memory or Cache based on user input and stores in Ppk0Hash.
Includes	`xilskey_utils.h, xilskey_eps_zynqmp.h`

u32 XilSKey_ZynqMp_EfusePs_ReadPpk1Hash(u32 *Ppk1Hash, u8 ReadOption)

Parameters	Ppk1Hash is a pointer to an array which holds the readback PPK1 hash in. ReadOption is a u8 variable which has to be provided by user based on which the input reading happens from cache or from efuse array. • 0 - Reads from cache • 1 - Reads from efuse array
Returns	XST_SUCCESS if key is read successfully. ErrorCode if it fails to read PPK1 hash of eFUSE.
Description	This API reads PPK1 hash from eFUSE memory or Cache based on user input and stores in Ppk1Hash.
Includes	`xilskey_utils.h, xilskey_eps_zynqmp.h`

u32 XilSKey_ZynqMp_EfusePs_ReadSpkId(u32 *SpkId, u8 ReadOption)

Parameters	SpkId is a pointer which holds the readback SPK ID in. ReadOption is a u8 variable which has to be provided by user based on which the input reading happens from cache or from efuse array. • 0 - Reads from cache • 1 - Reads from efuse array
Returns	XST_SUCCESS if key is read successfully. ErrorCode if it fails to read SPK ID of eFUSE.
Description	This API reads SPK ID from eFUSE memory or Cache based on user input and stores in SpkId.
Includes	`xilskey_utils.h, xilskey_eps_zynqmp.h`

void XilSKey_ZynqMp_EfusePs_ReadDna(u32 *DnaRead)

Parameters	DnaRead is a pointer which holds the readback DNA in.

Returns	XST_SUCCESS if key is read successfully. ErrorCode if it fails to read DNA.
Description	This API reads DNA from Cache stores in DnaRead.
Includes	`xilskey_utils.h, xilskey_eps_zynqmp.h`

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u32 XilSKey_ZynqMp_EfusePs_ReadSecCtrlBits(XilSKey_SecCtrlBits *ReadBackSecCtrlBits, u8 ReadOption)

Parameters	ReadBackSecCtrlBits is a pointer to the XilSKey_SecCtrlBits structure which holds the secure control bits read back. ReadOption is a u8 variable which has to be provided by user based on which the input reading happens from cache or from efuse array. • 0 - Reads from cache • 1 - Reads from efuse array
Returns	XST_SUCCESS if key is read successfully. ErrorCode if it fails to read secure and control bits of eFUSE.
Description	This API reads secure control bits from eFUSE memory or Cache based on user input and stores in ReadBackSecCtrlBits.
Includes	`xilskey_utils.h, xilskey_eps_zynqmp.h`

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u32 XilSKey_ZynqMp_EfusePs_CacheLoad()

Parameters	None.
Returns	XST_SUCCESS if cache reload is successfully. ErrorCode if it fails to reload cache of efuse.
Description	This API reloads caches of efuse, it updates cache with efuse memory.
Includes	`xilskey_utils.h, xilskey_eps_zynqmp.h`

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u32 XilSKey_ZynqMp_EfusePs_Write(XilSKey_ZynqMpEPs *InstancePtr)

Parameters	InstancePtr is a pointer to efuse PS instance.
Returns	XST_SUCCESS if efuse programming is successfully. ErrorCode if it fails to program eFUSE.
Description	This API programs the efuse based on the user inputs.
Includes	`xilskey_utils.h, xilskey_eps_zynqmp.h`

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u32 XilSKey_CrcCalculation(u8 *Key)

Parameters	Key is a hexa decimal character string for which CRC has to be calculated.
Returns	CRC of provided key.

Description	This API calculates the CRC of provided AES key of eFUSE. (This API calculates CRC for both Ultrascale and also Zynq MP platform eFUSE).
Includes	`xilskey_utils.h`

`u32 XilSkey_CrcCalculation_AesKey(u8 *Key)`

Parameters	Key is a pointer to buffer of size 32 which contains AES key in hexa decimal.
Returns	CRC of provided AES key.
Description	This API is calculates CRC on AES key provided. This API calculates CRC of AES key for UltraScale™ PL eFuse and Zynq® UltraScale+™ MPSoC PS eFuse. To calculate CRC on the AES string please use XilSKey_CrcCalculation. To call this API one can directly pass array of AES key which exists in an instance. Example for storing key into Buffer: If Key is "123456" buffer should be {0x12 0x34 0x56}
Includes	`xilskey_utils.h`

PUF API Summary

The following is a summary list of PUF APIs for Zynq UltraScale+ MPSoC. Descriptions of the APIs follow the list.

- u32 XilSKey_ZynqMp_EfusePs_WritePufHelprData(XilSKey_Puf *InstancePtr)
- u32 XilSKey_ZynqMp_EfusePs_ReadPufHelprData(u32 *Address)
- u32 XilSKey_ZynqMp_EfusePs_WritePufChash(XilSKey_Puf *InstancePtr)
- u32 XilSKey_ZynqMp_EfusePs_ReadPufChash(u32 *Address, u8 ReadOption)
- u32 XilSKey_ZynqMp_EfusePs_WritePufAux(XilSKey_Puf *InstancePtr)
- u32 XilSKey_ZynqMp_EfusePs_ReadPufAux(u32 *Address, u8 ReadOption)
- u32 XilSKey_Write_Puf_EfusePs_SecureBits (XilSKey_Puf_Secure *WriteSecureBits)
- u32 XilSKey_Read_Puf_EfusePs_SecureBits (XilSKey_Puf_Secure *SecureBitsRead, u8 ReadOption)
- u32 XilSKey_Puf_Debug2(XilSKey_Puf *InstancePtr)
- u32 XilSKey_Puf_Registration(XilSKey_Puf *InstancePtr)

`u32 XilSKey_ZynqMp_EfusePs_WritePufHelprData(XilSKey_Puf *InstancePtr)`

Parameters	InstancePtr is a pointer to the XilSKey_Puf instance.
Returns	XST_SUCCESS if programs successfully Errorcode on failure
Description	This API programs the Zynq UltraScale+ MPSoC PS eFUSE with PUF helper data
Includes	`xilskey_eps_zynqmp_puf.h`

u32 XilSKey_ZynqMp_EfusePs_ReadPufHelprData(u32 *Address)

Parameters	Address is a pointer to data array which holds the Puf helper data read from ZynqMp efuse.
Returns	XST_SUCCESS on success. Errorcode on failure
Description	This API reads the PUF helper data from eFUSE.
Includes	`xilskey_eps_zynqmp_puf.h`

u32 XilSKey_ZynqMp_EfusePs_WritePufChash(XilSKey_Puf *InstancePtr)

Parameters	InstancePtr is a pointer to the XilSKey_Puf instance.
Returns	XST_SUCCESS if chash is programmed successfully. Errorcode on failure
Description	This API programs Zynq UltraScale+ MPSoC eFUSE with CHash value.
Includes	`xilskey_eps_zynqmp_puf.h`

u32 XilSKey_ZynqMp_EfusePs_ReadPufChash(u32 *Address, u8 ReadOption)

Parameters	Address is a pointer which holds the read back value of chash ReadOption is a u8 variable which has to be provided by user based on this input reading is happend from cache or from efuse array. ″ 0(XSK_EFUSEPS_READ_FROM_CACHE)Reads from cache ″ 1(XSK_EFUSEPS_READ_FROM_EFUSE)Reads from efuse array
Returns	XST_SUCCESS on success. Errorcode on failure
Description	This API reads eFUSE PUF CHash data from eFUSE array or cache based on the user read option.
Includes	`xilskey_eps_zynqmp_puf.h`

u32 XilSKey_ZynqMp_EfusePs_WritePufAux(XilSKey_Puf *InstancePtr)

Parameters	InstancePtr is a pointer to the XilSKey_Puf instance.
Returns	XST_SUCCESS if Auxilary data is programmed successfully. Errorcode on failure
Description	This API program Zynq UltraScale+ MPSoC eFUSE with Auxilary data
Includes	`xilskey_eps_zynqmp_puf.h`

u32 XilSKey_ZynqMp_EfusePs_ReadPufAux(u32 *Address, u8 ReadOption)

Parameters	Address is a pointer which holds the read back value of Auxilary ReadOption is a u8 variable which has to be provided by user based on this input reading is happened from cache or from efuse array. ″ 0(XSK_EFUSEPS_READ_FROM_CACHE)Reads from cache ″ 1(XSK_EFUSEPS_READ_FROM_EFUSE)Reads from efuse array
Returns	XST_SUCCESS on success. Errorcode on failure
Description	This API reads efuse puf Auxilary Data from efuse array or cache based on user read option.
Includes	`xilskey_eps_zynqmp_puf.h`

u32 XilSKey_Write_Puf_EfusePs_SecureBits (XilSKey_Puf_Secure *WriteSecureBits)

Parameters	WriteSecureBits is the pointer to the XilSKey_Puf_Secure.
Returns	XST_SUCCESS on success. Errorcode on failure
Description	This function programs the PUF secure/control bits of eFUSE. The PUF configuration which is inteded to program should be made 1 all other members of structure should be 0.
Includes	`xilskey_eps_zynqmp_puf.h`

u32 XilSKey_Read_Puf_EfusePs_SecureBits (XilSKey_Puf_Secure *SecureBitsRead, u8 ReadOption)

Parameters	SecureBitsRead is the pointer to the XilSKey_Puf_Secure which holds the read data of PUF eFUSE secure bits. ReadOption is a u8 variable which has to be provided by user based on this input reading is happend from cache or from efuse array. ″ 0(XSK_EFUSEPS_READ_FROM_CACHE)Reads from cache ″ 1(XSK_EFUSEPS_READ_FROM_EFUSE)Reads from efuse array
Returns	XST_SUCCESS on success. Errorcode on failure
Description	This function reads PUF secure bits from eFUSE ZynqMP+ SoC and updates the members of the structure. ″ 1 - indicates the corresponding eFUSE bit is programmed ″ 0 - indicates the corresponding eFUSE bit is not programmed
Includes	`xilskey_eps_zynqmp_puf.h`

u32 XilSKey_Puf_Debug2(XilSKey_Puf *InstancePtr)

Parameters	InstancePtr is a pointer to the XilSKey_Puf instance
Returns	XST_SUCCESS if debug 2 mode was successful. ERROR if unsuccessful.

Description	This API generates debug 2 result and the result is updated at InstancePtr -> Debug2Data
Includes	`xilskey_eps_zynqmp_puf.h`

`u32 XilSKey_Puf_Registration(XilSKey_Puf *InstancePtr)`

Parameters	InstancePtr is a pointer to the XilSKey_Puf instance
Returns	XST_SUCCESS if registration/re-registration was successful. ERROR if registration was unsuccessful
Description	This API performs PUF registration and stores the PUF syndrome data at InstancePtr ->SyndromeData
Includes	`xilskey_eps_zynqmp_puf.h`