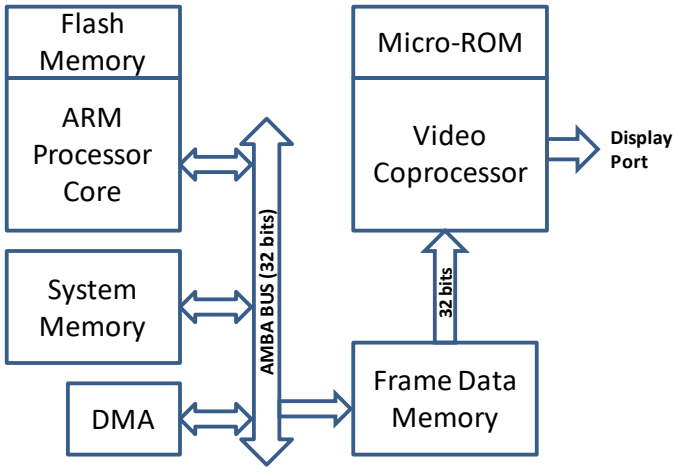
Problem 1. Power Analysis (50 Points)

This problem will look at the software power calculation in Lecture 17 where you are given a system topology and various current/transaction values and you will determine battery life.



Basic operation

The ARM processor pre-processes frame data for the Video Co-Processor. The frame data is located in the System memory. When the ARM processor completes the processing of the data, the DMA engine transfers the data from the System Memory to the Frame Data Memory. In addition to processing frame data the ARM processor executes an additional 60 million instructions every second doing other system level work. When the ARM processor is not executing instructions, it is in a quiescent state. When the DMA is not executing it is also in a quiescent state. NOTE: the quiescent state is accomplished by power supply gating techniques which considerably reduces leakage.

The Video Coprocessor (VCP) reads the data from Frame Data Memory; processes the data and then sends the results out the Display Port to an LCD. The resolution of the LCD is 400 x 300 pixels and has a refresh rate of 30 frames per second. Each pixel requires 1 word (4 bytes) of data. The VCP consumes 2 words of Frame Data for every word that is sent to the Display Port.

The DMA engine transfers one frame of data for each DMA transaction. There are 30 DMA cycles per second. The DMA runs at 300MHz which is same frequency for the AMBA Bus

Transaction Details

The ARM processor executes 1 IPC. The processor executes all instructions from Flash Memory. The processor is running at 600 MHz. All accesses to the AMBA bus stall the ARM processor. During the AMBA bus cycle the processor clocks continue to run even though it is stalled.

NOTE: There are 2 ARM processor clocks for every AMBA bus clock. Reads or Writes from System Memory require 2 AMBA Bus clocks.

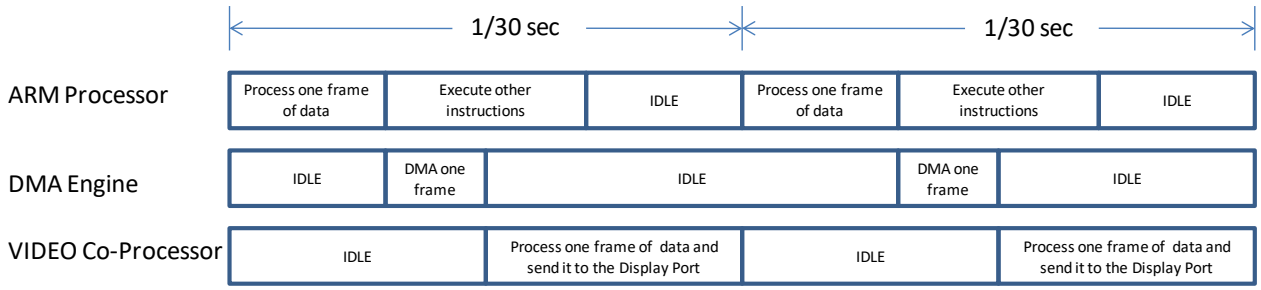
NOTE: All AMBA bus transactions are 4 bytes wide.

For each word of frame data that is written in System Memory, the ARM processor executes 32 instruction cycles and reads 7 words of data and writes the 1 word of data.

The DMA is used to transfer data from the System Memory to the Frame Data Memory. All DMA transactions take 3 AMBA Bus clocks for every operation (2 to read System Memory and 1 to write the Frame Data Memory). The DMA transaction is started once the ARM Processor completes processing the frame data.

The VCP runs at 600 MHz and executes 1 IPC. The instruction memory for the VCP is located in a micro-ROM in the VCP. For each word of data that is sent to the Display Port, the VCP executes 32 micro-instructions and reads 2 words of data from the Frame Data Memory. NOTE: Accesses to the Frame Data memory take 4 VCP clocks. Writes to the Display Port take 1 VCP clock.

The schedule of execution would look something like the following picture which shows 2/30th second of operation:



NOTE: Not to scale ☺

Current during normal operation

During normal operation the processor is consuming both dynamic (C * dv/dt) current and leakage current.

Transaction	Dynamic Current	Leakage Current
ARM Processor	4.7 mA	1.1 mA
AMBA BUS transaction (wire power only -> no leakage)	.7 mA	n/a
DMA Engine	1.8 mA	.4 mA
Video Coprocessor	1.2mA	0.3mA

Idle/Quiescent Current

When the units are not operating they will be in a power supply gated mode, i.e., major portions of the block are not functioning. The only current will be leakage current.

Unit	Leakage Current
ARM Processor	0.3mA
DMA Engine	0.1mA
Video Coprocessor	0.1mA

NOTE: Assume memory current is accounted for in the ARM, AMBA and VCP transactions.

Questions:

1. How many words of data are sent to the Display Port per second?

   400 x 300 x 30 = 3,600,000 words

2. How many words are read by the Video Co-Processor to produce 1 frame of data?

   400 x 300 x 2 = 240,000 words

3. How many processor clocks are required for each AMBA bus transaction to system memory?

   2 processor clocks/ AMBA Clock x 2 AMBA clocks/transaction = 4 processor clocks

4. How many processor clocks are required to process 1 frame of data?

For every word of data that gets sent to the System Memory the processor executes 32 Instruction clocks + 7 x 4 (read) processor clocks + 4 (write) processor clocks = 64 processor clocks.

Each frame of data requires 240,000 words. So, for every frame of data, the processor executes 240,000 X 64 = 15,360,000 processor clocks.

5. How many AMBA bus clocks does the DMA transfer from the System Memory to the Frame Data Memory on every DMA transaction?

There are 3 AMBA bus clocks per word of data transferred.
240,000 words are transferred per DMA transaction.

3 X 240,000 = 720,000 AMBA bus clocks per DMA Transactions

DMA is active 30 * 720,000 = 21,600,000 DMA CLK's/sec

6. How many AMBA bus clocks are required by the ARM core when it processes one frame of video data (that is sent to the Display Memory by the DMA engine)?

There are 8 AMBA bus transactions per word. There are 240,000 words processed

8 x 240,000 x 2 AMBA CLKs/transaction = 3,840,000 AMBA bus clocks

7. How many AMBA bus clocks is the AMBA bus idle in 1 sec?

There are 720,000 x 30 = 21,600,000 AMBA CLKs for the DMA transfers

There are 3,840,000 x 30 = 115,200,000 AMBA CLKs for processor functions

300,000,000 – 21,600,000 – 115,200,000 = 163,200,000 AMBA CLKs (54% of the time)

8. How many ARM Processor clocks are idle per second? NOTE: the ARM processor is in the quiescent state at this time.

The processor uses 15,360,000 x 30 = 460,800,000 clocks/sec to process frame data.

The processor uses 60,000,000 clocks to process additional work.

600,000,000 – 460,800,000 – 60,000,000 = 79,200,000 processor clocks/sec are idle (13.2%)

Processor executes 520,800,000 clocks/sec = 86.8% active

9. How many VCP clocks are idle per second?

There are 3,600,000 words sent to the Display Port per second. This requires 3,600,000 VCP clocks.
There 32 micro-instructions per pixel. There are 300 x 400 pixels per frame
There are 8 VCP clocks to read the data from Frame Memory for each pixel

The total number of active VCP clock cycles is:
3,600,000 + (32 x 300 x 400 x 30) + (8 x 300 x 400 x 30) = 147,600,000 clocks (24.6 %)

The total number of idle clocks:
600,000,000 – 147,600,000 = 452,400,000 clocks (75.4%)

10. You are given an AA battery (1.5V) with 2890 mA-hour capacity which translates to 144.5 ma for 20 hours. NOTE: 3600 Joule = 1 WATT-HOUR and an AA Battery can theoretically provide approximately 15600 Joules of energy

Fill out the following table

Subsystem	% Active	Active Current (mA)	% Idle	Idle Current (mA)	Total Current (mA)
ARM	.868	5.8	.132	.3	5.074
AMBA bus	.46	.7	.54	0	.332
DMA	.072	2.2	.928	.1	.2512
VCP	.246	1.5	.754	.1	.4444

How long will the battery provide power for this system?

Total current = 6.1016 mA

20 * 144.5 / 6.1016 = 473

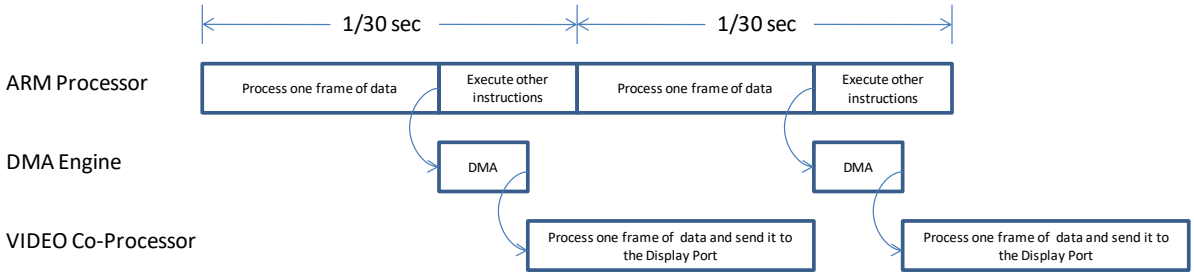
The battery will last for 473 hours = 19.73 days.

Problem 2. Scheduling (25 Points)

a) What is the slowest frequency that we can run the ARM processor and still complete all tasks? Show an updated schedule that comprehends the new frequency.

460,800,000 + 60,000,000 = 520.8 MHz Cycle time is 1.92ns

The new schedule is:



b) What is the slowest frequency that we can run the Video Co-Processor when we are running the ARM core at its lowest frequency (and complete all tasks)?

There are 3,840,000 x 30 = 115,200,000 AMBA CLKs for processor functions

The sum is 4,560,000 AMBA clocks, which is 9,120,000 processor clocks or 17.5ms

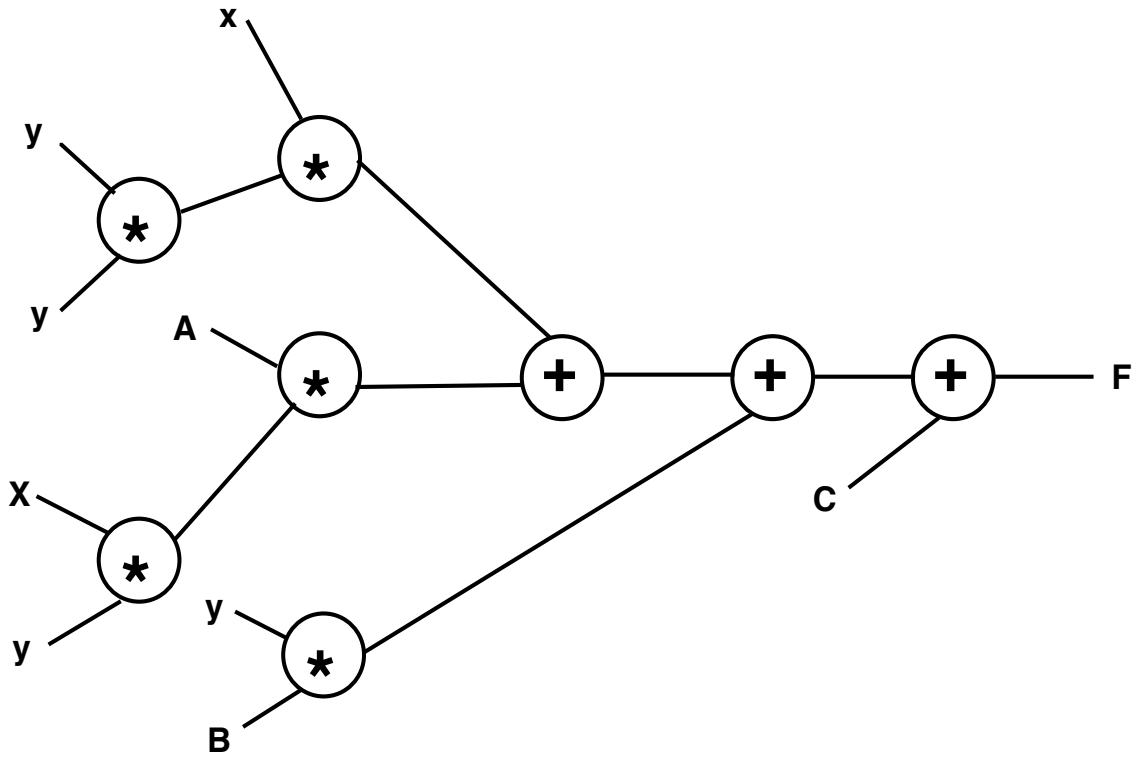
We have 520,800,000 – 9,120,000 = 511,680,000 processor clocks (982.5ms) in which to do the VCP function.

Recall that the VCP takes 147,600,000 clocks @600MHz to complete its tasks (24%)

To find the final VCP frequency, we divide the 147,600,000 clocks by 982.5 ms
=> 150.24 MHz for the VCP slowest frequency.

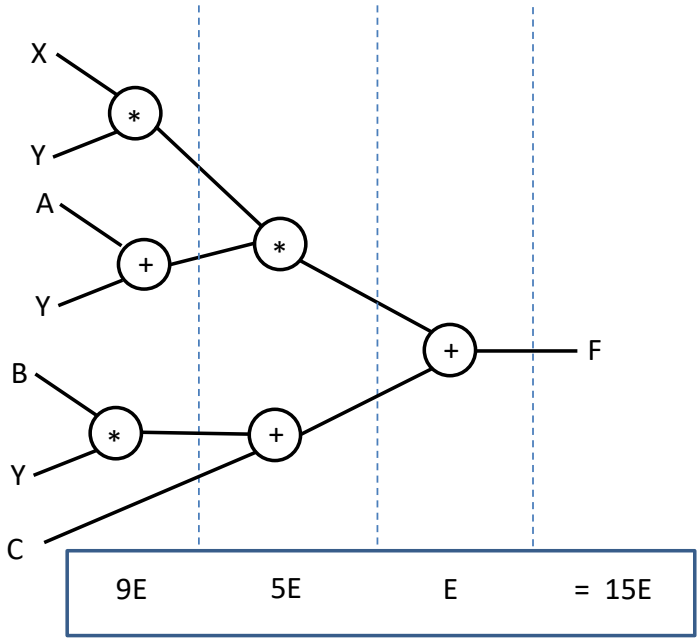
Problem 3. Tree Height Reduction (25 points)

One implementation for an arithmetic expression is shown below, using 2-input adder and multiplier modules.



(a) Write an equation for this expression which takes the least number of cycles.

XYA + YYX + YB + C
XY(Y+A) + (YB + C)
3 cycle implementation



(b) If the energy required to perform an addition is E, and that required for a multiplication is 4E, what is the energy required for:

(i) the original implementation

23E

(ii) your implementation in (a)?

15E

(c) Write an equation that requires the minimum energy for the computation of the original expression, and which takes no more time than the original implementation.

Y(X(Y+A) + B) + C
5 cycles
11E