EE 382M-8 VLSI-II SPRING 2017 -- HMK #1

Assigned: Jan. 17, 2017 Due: Feb. 14, 2017

High performance Hi-K, metal gate planar 22nm and FinFET 14nm transistors will be characterized in this homework assignment. Models are from the Arizona State University's Predictive Technology Models website: http://ptm.asu.edu/.

1. Measure IDSAT (mA/um) for both NFET and PFETs in 22nm and 14nm CMOS technologies at T=30C, TYPICAL process corner and Vgs=Vds=0.9V. Be aware that each Fin in the 14nm transistors has an effective width of 56nm.

2. Measure Ioff (Amps/um) for both NFET and PFETs in 22nm and 14nm CMOS at 30C, TYPICAL process corner and Vgs=0.0V for both Vds=0.05V and 0.9V. Monitor the SOURCE current and not the DRAIN current; why? Plot LOG(ABS(Ids)) .vs. Vgs (0.0V to 0.9V) of the 4 transistors at Vds=0.05V and 0.90V. Why are the FinFETs so much better in Ioff?

3. Measure Cgate (fF/um) for the 4 FETs by integrating the current going into ONE FET in the provided 9-stage FO4 ring oscillator over ONE VDD transition. Using Q=CV, Cgate = (1/VDD)*Integral (Ig(t)dt). Note that the AREA under the Ig(t) curve is the integral over ONE transition.

4. Calculate the Vt's of the 4 FETs using the extrapolated method using the Ids and Gm .vs. Vgs transistor characteristics as follows:
   - Apply 50 milli-volts to Vds; sweep Vgs from 0.0 to 0.9 volts. Gather 91 points.
   - Plot Ids .vs. Vgs; Differentiate Ids with respect to Vgs (this is the Gm of the transistor); plot Gm along the Ids .vs. Vgs curve; Gm will 'peak' at some Vgs value. Draw a tangent on the Ids .vs. Vgs curve at this Vgs value. The Vt of the transistor will be the Vgs value where Ids=0.0 mA 'minus' Vdd/2 (or 25 milli-volts).
   - Use negative values for the PFET characterization; ie. apply -50 milli-volts to Vds, and sweep Vgs from 0.0 to -0.9V. Ids will be negative (Gm will still be positive); add + 25 milli-volts to the final result.
   - How does your 'extrapolated' Vt value compare with the model's Vth0 value?
   - Include all relevant plots.

5. Determine the gate delay of an INVERTER with FO4 (9-stage ring oscillator provided) for both 22nm and 14nm technologies at 30C and TYPICAL process models. Plot stage DELAY (ps) .vs. VDD (volts) for VDD=0.5V to 0.9V in 0.1V increments. Gate delay should be the average of both transitions.

6. What is the performance increase at a constant VDD between the 22nm and 14nm CMOS technologies? What is the power reduction at the same performance level (or iso-GATE DELAY)? Is this performance increase and power reduction constant as a function of VDD?

7. Are these 14nm transistors scaling based on a constant electric field scaling principle?

8. Plot Ids .vs. Vds (0.0V to 0.9V in steps of 0.05V) and Vgs=0.1, 0.3, 0.5, 0.7, and 0.9V for all 4 FETs; use a width=1.008um for the 22nm transistors and 18 Fins for the 14nm transistors (why?). Other than the increase in drive current (Ids), what else is different between the planar 22nm transistors and the 14nm FinFET transistors?

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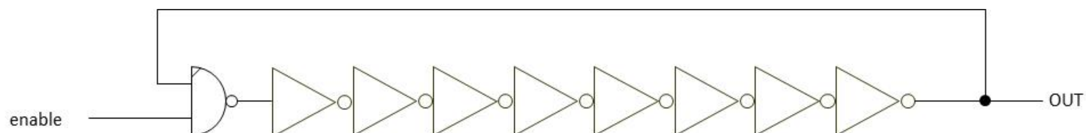
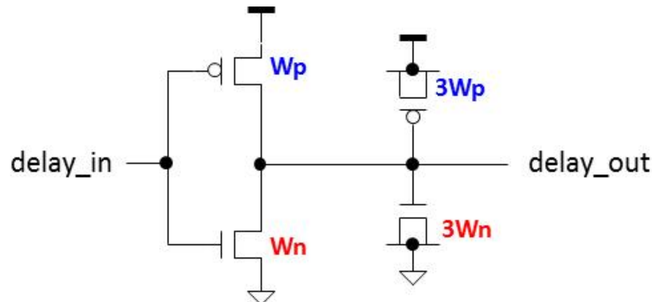
Collaterals you will need to complete Problem 1:

/home/projects/courses/spring_17/ee382m-16810/hw/hw1

hw1_22nm.sp: top-level HSPICE netlist & simulation deck for a 9-stage FO4 ring oscillator in 22nm
hw1_14nm.sp: top-level HSPICE netlist & simulation deck for a 9-stage FO4 ring oscillator in 14nm
block_22nm.txt: netlist for a 22nm inverter delay element with a built-in FO3
block_14nm.txt: netlist for a 14nm inverter delay element with a built-in FO3
14nm_NMOS_HI_K_HP.txt – NFET MOSFET models for a 14nm semiconductor technology
14nm_PMOS_HI_K_HP.txt – PFET MOSFET models for a 14nm semiconductor technology
22nm_NMOS_HI_K_HP.txt – NFET MOSFET models for a 22nm semiconductor technology
22nm_PMOS_HI_K_HP.txt – PFET MOSFET models for a 22nm semiconductor technology
library-14nm.txt - library of 14nm circuit elements (logic gates, transmission gates, tristate inverters, MSFF, and interconnect elements)
library-22nm.txt - library of 22nm circuit elements (logic gates, transmission gates, tristate inverters, MSFF, and interconnect elements)

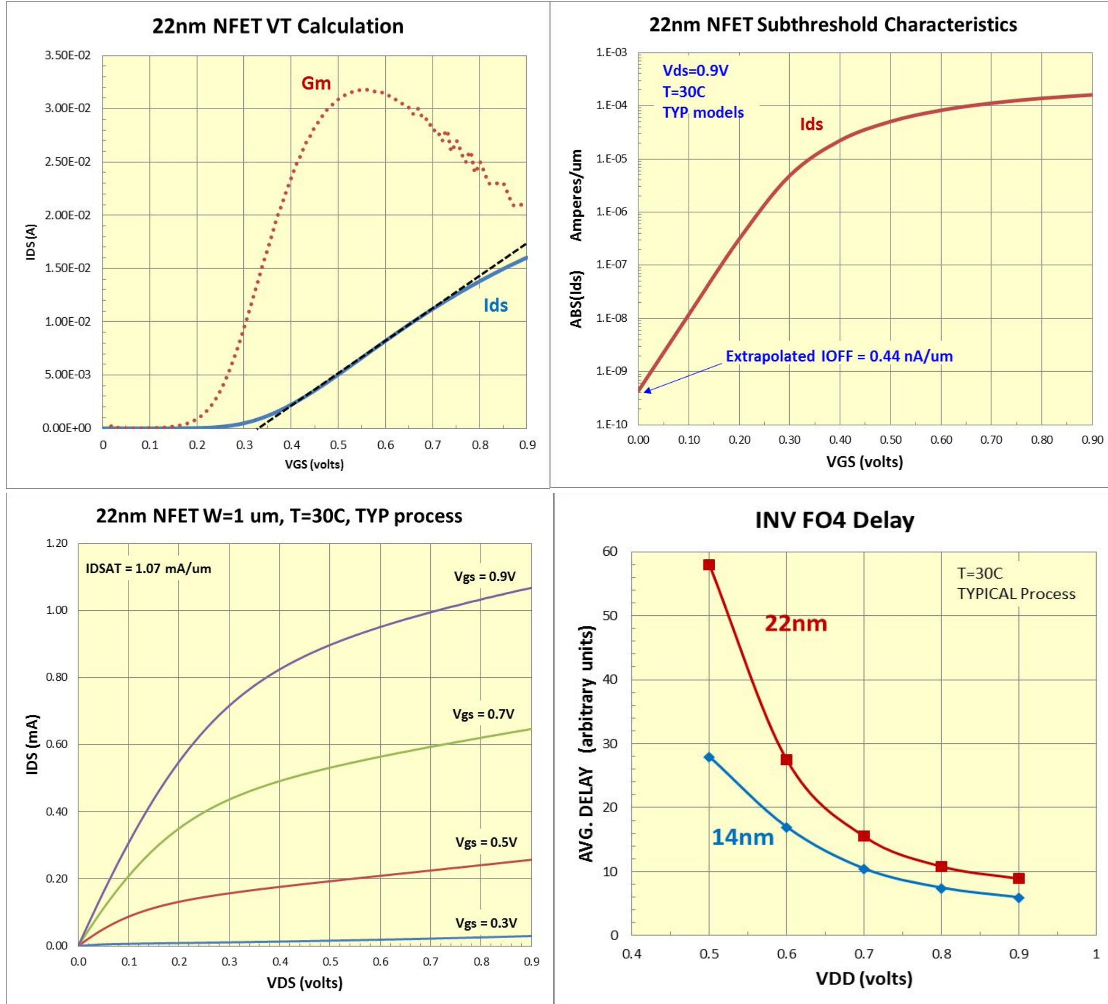


9-stage Ring Oscillator



FO4 DELAY ELEMENT

Sample plots (only for illustration purposes):



CONSTANT ELECTRIC FIELD SCALING:

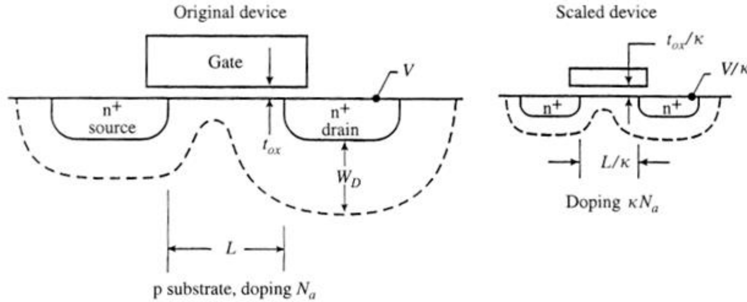


TABLE 2.1 Scaling of MOSFET Device and Circuit Parameters

	MOSFET device and circuit parameters	Multiplicative factor ($\kappa > 1$)
Scaling assumptions	Device dimensions (t_{ox}, L, W, x_j)	$1/\kappa$
	Doping concentration (N_a, N_d)	κ
	Voltage (V)	$1/\kappa$
Derived scaling behavior of device parameters	Electric field (ε)	1
	Carrier velocity (v)	1
	Depletion layer width (W_d)	$1/\kappa$
	Capacitance ($C = \varepsilon A/t$)	$1/\kappa$
	Inversion layer charge density (Q_i)	1
	Current, drift (I)	$1/\kappa$
	Channel resistance (R)	1
Derived scaling behavior of circuit parameters	Circuit delay time ($\tau \sim CV/I$)	$1/\kappa$
	Power dissipation per circuit ($P \sim VI$)	$1/\kappa^2$
	Power-delay product per circuit ($P \times \tau$)	$1/\kappa^3$
	Circuit density ($\propto 1/A$)	κ^2
	Power density (P/A)	1

constant

Design of High-Performance Microprocessor Circuits, IEEE Press, New York, 2001