

## EE 382M.8 VLSI-II Spring 2017 -- HW #2 Assignment

Assigned: Feb. 14<sup>th</sup>, 2017

Due: Mar. 21<sup>st</sup>, 2017

### Part 2.1: (20 points) Area Estimation for EDP

- a. **Register File area estimation (10) in 22nm CMOS:** Assume word-lines are routed in M3 with a pitch of 80nm. Local bit-lines are routed in M2 with a pitch of 80nm and global bit-lines and data-lines are routed in M4 with a pitch of 120nm. Assume word-lines and global bit-lines are half-shielded.

Estimate the area of a 128 entries, 32bits/entry, 5R/3W array. Assume 16 cells per local bit-line and each local bit-line receiver and write data driver is the same area as one cell. Assume decoders make up 20% of the total array area.

| Register File area                           |       |                             |
|--|-------|-----------------------------|
| M2_pitch                                     | 80nm  | local BL pitch              |
| M3_pitch                                     | 80nm  | local word-line pitch       |
| M4_pitch                                     | 120nm | global BL/ data lines pitch |
| # of cells                                   |       |                             |
| entries                                      | 128   |                             |
| bits/entry                                   | 32    |                             |
| read   | 5     |                             |
| write  | 3     |                             |
| cells/local BL                               | 16    |                             |
| WL shield                                    |       |                             |
| GBL shield                                   |       |                             |
| # of sub_arrays                              |       |                             |
|  |       |                             |
| Cell height                                  |       | um                          |
| Cell width                                   |       | um                          |
| cell area                                    |       | um^2                        |
| local bl receiver and write data driver area |       | um^2                        |
| sub_array_area_with_driver/receiver          |       | um^2                        |
| decoder proportion                           | 0.2   |                             |
|  |       |                             |
| RF_array_wo_decoders                         |       | um^2                        |
| RF_area                                      |       | um^2                        |

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b. **Small signal array area estimation (10) in 22nm CMOS:** Assumptions to estimate a 4KB data cache:

- The area of a high performance 6T bitcell in a 22nm CMOS technology is  $0.12 \mu\text{m}^2$ .
- The bitcell sub-array is comprised of 256 columns and 128 rows (32,768 bits).
- Each word is 32b wide (Din and Dout is 32b wide).
- Assume an array efficiency of 50%.

| 4KB SRAM                            |        |                 |
|-------------------------------------|--------|-----------------|
| cell                                | 0.12   | $\mu\text{m}^2$ |
| number of bits                      | 32,768 | 4KB data cache  |
| columns                             | 256    |                 |
| rows                                | 128    |                 |
| word_width                          | 32     |                 |
| array_efficiency                    | 0.5    |                 |
| sub_array_ea                        | 1      |                 |
|                                     |        |                 |
| number of sense_amps                |        |                 |
| width_column_dec                    |        |                 |
| required row address bits           |        |                 |
| required column address bits        |        |                 |
| total address bits required         |        |                 |
|                                     |        |                 |
| area_cells_only                     |        | $\mu\text{m}^2$ |
| decoder area is 15% of bitcell area | 0.15   |                 |
| area_with_decoders                  |        | $\mu\text{m}^2$ |
| area_total                          |        | $\mu\text{m}^2$ |

**Answer the following questions:**

1. How many sense-amps are required?
2. How wide are the column decoders?
3. How many address lines are required?
4. What is the area of this 4KB data cache?  $\mu\text{m}^2$

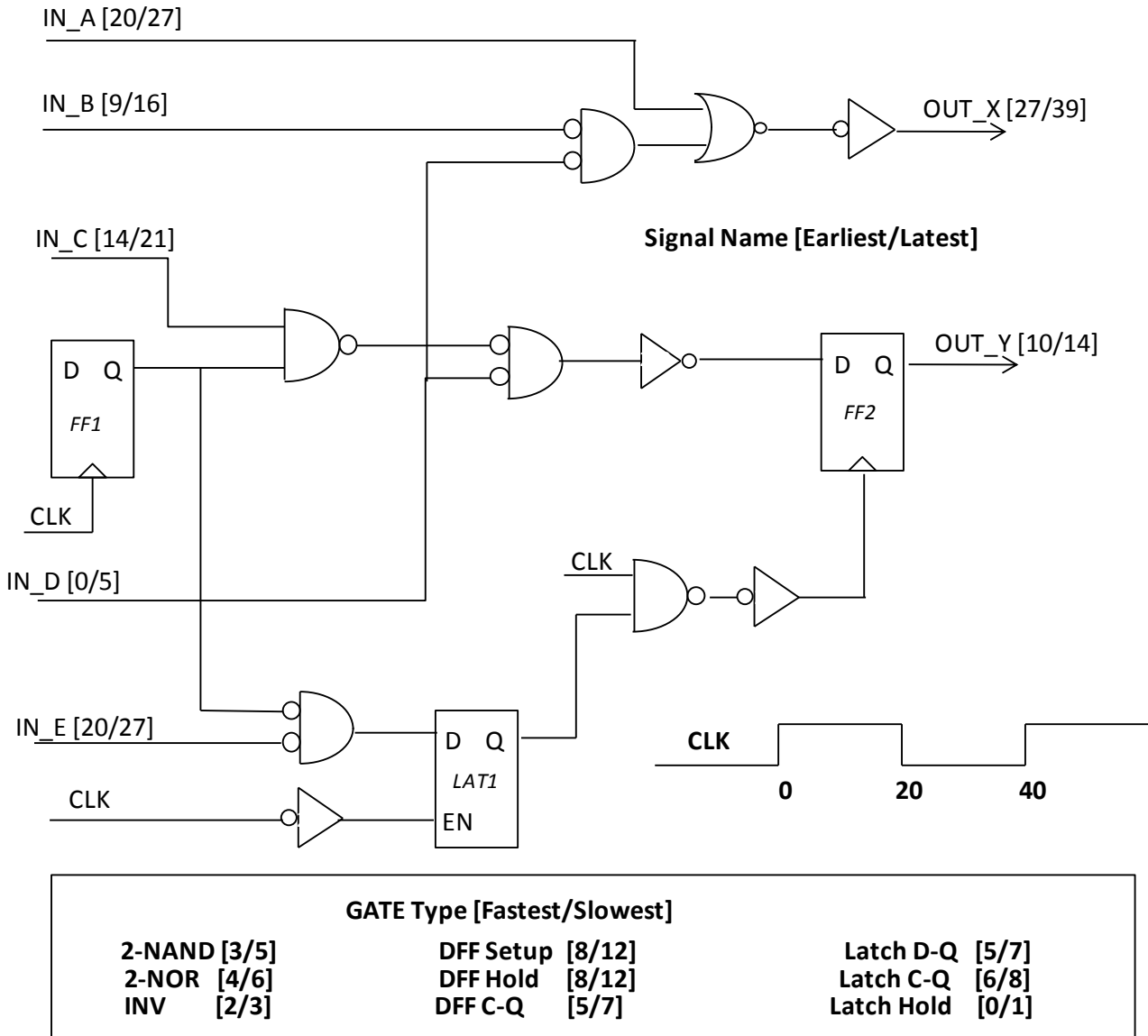
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## Problem 2.2 (30 points): Timing

The I/O timing constraints for this circuit are annotated on the schematic below. The first number is for "MIN Mode" timing and the second number is for "MAX Mode" timing. Your task is to a) identify the critical min and max paths to the primary outputs OUT\_X and OUT\_Y and b) to find the MIN and MAX slack for this circuit.

Note that the timing delays for each combinational logic gate type are given below. The clock period is 40 units. For robustness the integration team has determined that there is a restriction that the setup time to a clock-gater will be [1/1] i.e., 1 unit for "MIN-Mode and 1 unit for "MAX-Mode".



**HINT:** Don't forget about cycle-adjust requirements for some paths.

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- a) What are the critical "Max" paths in this circuit?
- b) What are the critical "MIN" paths in this circuit?
- c) What are the Max-Mode slacks for LAT1 & FF2?
- d) What are the Min-Mode slacks for LAT1 & FF2?

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### **Problem 2.3 (20 points): Power Estimation & Reduction in CMOS circuits**

In a 22nm technology, a processor design has an area of  $2.0\text{mm}^2$  and runs at 2.2 GHz at a typical voltage of 1.0V. Assume that at any given time, approximately half the transistors in the processor are on and half are off; also assume that the Stack Effect = 0.5 and the switching activity factor (AF) = 0.5.

a. Estimate total processor power at  $T=30\text{C}$  assuming:

$$\begin{aligned}C_{\text{switch-effective}} &= 0.5\text{nF/mm}^2 \\ \text{Transistor Density} &= 3.0\text{M/mm}^2 \quad (3.0 \text{ million transistors/mm}^2) \\ W_{\text{avg}} &= 0.2\mu\text{m} \\ I_{\text{OFF}} &= 0.25\mu\text{A}/\mu\text{m} \\ I_{\text{gate}} &= 1\text{nA}/\mu\text{m}\end{aligned}$$

- b. In a 14nm technology with a typical voltage of 0.9V, the same processor design runs at 3.0GHz. Assume an  $I_{\text{OFF}}$  of  $0.5\mu\text{A}/\mu\text{m}$  and  $I_{\text{gate}}$  of  $2\text{nA}/\mu\text{m}$  and all linear dimensions scale by 0.7. Switching density ( $C_{\text{switch-effective}}$ ) increases to  $0.7\text{nF/mm}^2$ . Calculate total power.
- c. List (in priority) all sources of power (both dynamic and leakage) that any CMOS circuit (with a **Ceff** capacitance) dissipates when powered by a **VDD** power rail and operated at **F** frequency.
- d. Describe 3 methods to reduce **leakage** power **without** adversely affecting gate performance or overall block performance (something to keep in mind: typically, a small number of paths in a block or CPU set the maximum frequency of operation).
- e. What is the difference between **active** leakage power and **stand-by** leakage power?

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### Part 2.4: (30 points) 22nm FLOP characterization

For both Din transitions (0->1 and 1->0), determine the input setup (Tsu), input hold (Th), and clock to out (Tcq) for the following 3 FLIP FLOPS (a, b, c). Use 50ps slew rate (full rail) for Din and clock; use the high-performance 22nm CMOS transistor models. For the Tcq measurement, use a Din Tsu.

Show ALL your work; also answer the following questions pertaining to each design:

| Parameter | FLOP a |      | FLOP b |      | FLOP c |      | FLOP c (14nm) |      |
|-----------|--------|------|--------|------|--------|------|---------------|------|
|           | 0->1   | 1->0 | 0->1   | 1->0 | 0->1   | 1->0 | 0->1          | 1->0 |
| Tsu (ps)  |        |      |        |      |        |      |               |      |
| Tcq (ps)  |        |      |        |      |        |      |               |      |
| Th (ps)   |        |      |        |      |        |      |               |      |
| Tdq (ps)  |        |      |        |      |        |      |               |      |

- a) **FLOPa:** List 3 deficiencies with this design. Hint: look at b, c designs.
  
- b) **FLOPb:** Is the Din input capacitance lower than design a? What about the clock capacitance? Plot Tdq (Tsu\_Tcq), Th, and the clock pulse width as a function of VDD; use 0.5V to 0.9V in steps of 0.1V and compare to FLOP C's Tdq and Th. Which FLOP would you use to minimize the use of MINDELAY buffers?
  
- c) **FLOPc:** What are the benefits of placing the slave latch off to the side? Is this a time-borrowing FLOP? Is the clock capacitance lower than design b? Does this mean that clock power is lower in this FLOP design? Any benefit in clocking the master LATCH feedback?
  
- d) Scale **FLOPc** to 14nm CMOS (note that 1 FIN = 56nm, the design will be 'quantized' to the nearest 56nm) and re-characterize for Tsu, Th, and Tcq at 70C, VDD=0.9V and TYPICAL models. Did any of these fundamental timing parameters scale? If not, why not?

#### Simulation Tips:

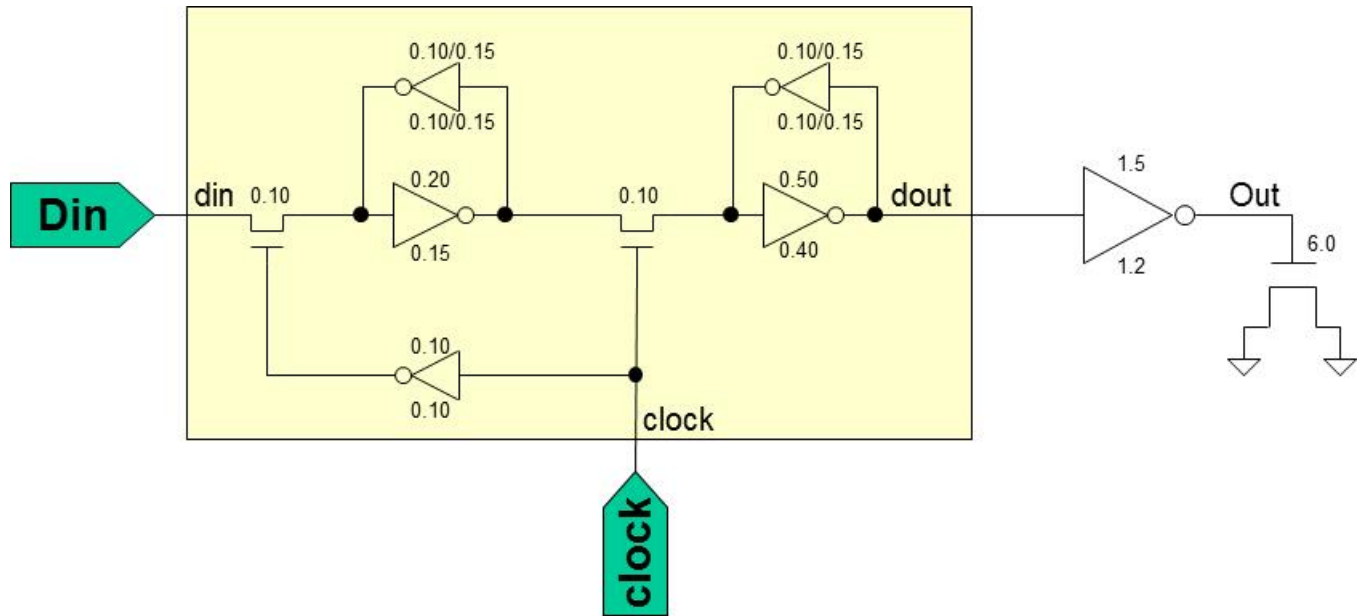
- Use a TEMP=70C, VDD=0.9V, TYPICAL transistor models.
- Use HSPICE ic statements to properly initialize these sequential circuits.
- Use a Din-to-clock step-size of 1ps to search for Tsu, Th and Tcq.
- If a channel length is not specified, then use nominal 22nm transistor length.

Spice netlists are located in the LRC: /home/projects/courses/spring\_17/ee382m-16810/hw/hw2  
or at

[http://projects.ece.utexas.edu/courses/spring\\_17/ee382m-16810/hw/hw2/](http://projects.ece.utexas.edu/courses/spring_17/ee382m-16810/hw/hw2/)

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a) FLOP for part a):



b) FLOP for part b):

