EE 382M VLSI-II Spring 2017 --- HW #3 Assignment

Assigned: March 10th, 2017 Due: April 11th, 2017

Problem 3.1 (20 points): Cross Talk in 14nm

Assume: HSPICE parameters: Nominal 14nm technology, VDD=0.9 Volts, and T=30C

- 100 ps input fall times on inverters I1 and I5.
- Use 10 fins for all PFETs and NFETs on I1, I2, I3, I4, I5, and I6.
- C = 100 fF and R = 0 ohm

For the circuit in the figure below:

a) What do you expect at the input of inverter I4?

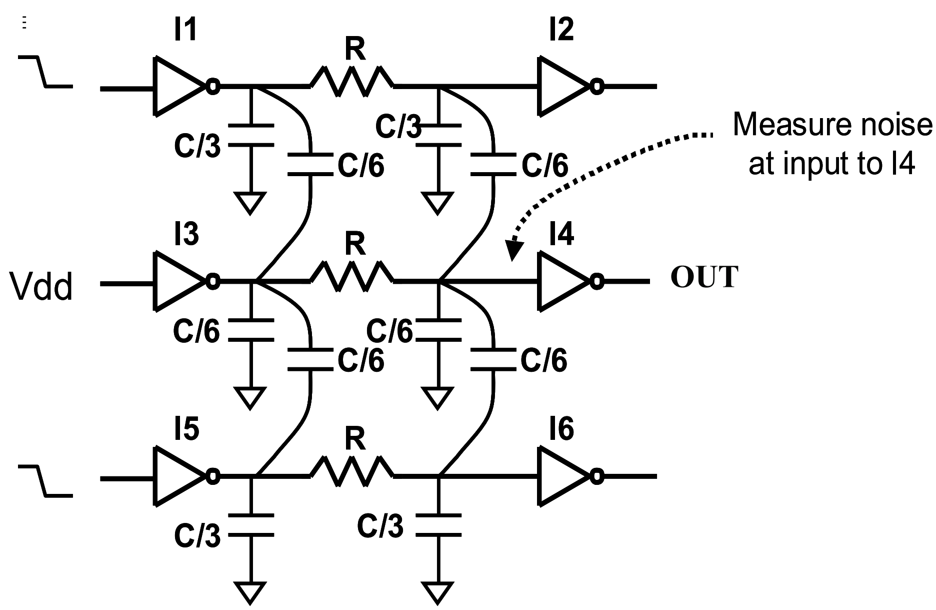
b) Plot the cross-talk at the input of inverter I4.

c) Repeat using 2 fins on both NFET and PFET on inverters I3 & I4 only. Explain the change in behavior.

d) Repeat with 20 fins on each NFET and PFET for all inverters but with R = 2000 ohms on all lines. Explain the change in behavior.

e) Repeat with the weaker devices (2 fins on each NFET and PFET) on I3 & I4 and R = 0 ohms and 2000 ohms on all lines. Is the increased interconnect resistance helping or hurting with cross-talk?

f) Even there is cross talk noise, does output node ***OUT*** get affected?



EE 382M VLSI-II Spring 2017 --- HW #3 Assignment

Assigned: March 10th, 2017 Due: April 11th, 2017

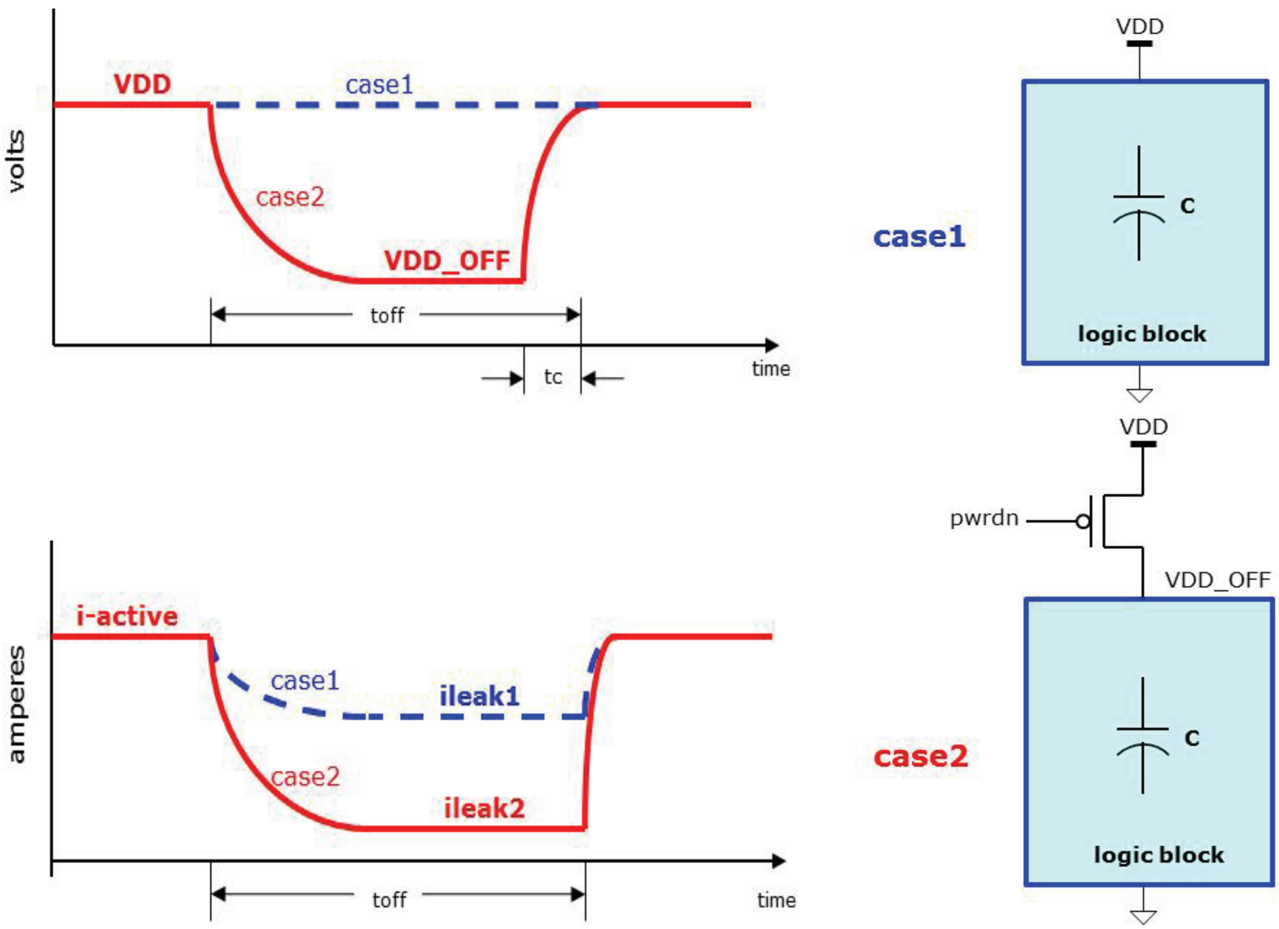
What To Submit:

1) Submit plots for (a, b, c, d and e) for the voltage at the input of inverter I4.
2) Explain briefly the differences in the results obtained for sections a, b, c, d and e.

Problem 3.2: (25 points) To power gate or not?

a) A Floating Point Unit in a CPU can be power gated since it can spend many CPU cycles in idle mode. This problem determines how long it needs to be off for the lowest energy consumption. In case 1, the FPU is not power gated; in case 2 it is power gated for a Toff duration (see following figures). You need to determine the break-even point for Toff (where the total energy is equal for both case1 and case2).

Assumptions: Ileak2 = Ileak1 / 1000
VDD_OFF = VDD / 10
Total FPU capacitance = C
The PFET power gate IR droop is negligible

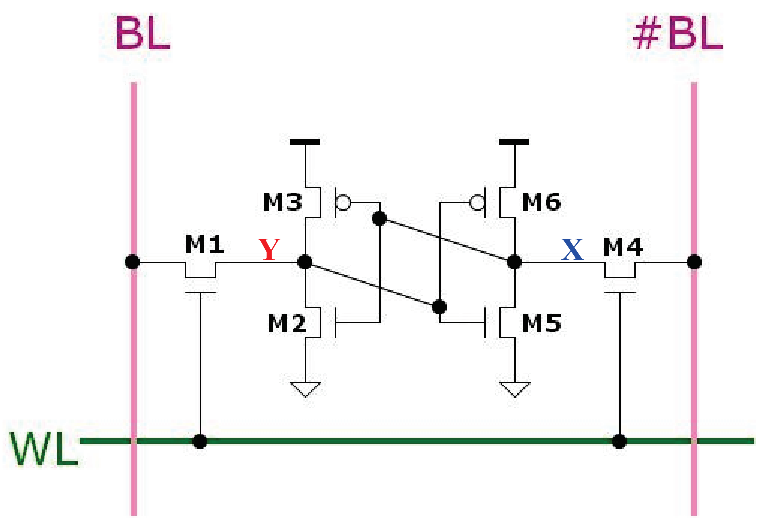


b) Assume that you have 2 CMOS technology options at your disposal to use on a 1GHz CPU; the 1st one gives you a total FPU leakage of 1mA @ 0.75 Volts and T=30C in standby (with NO power gating). The 2nd one gives you leakage reductions of 10X at the same voltage and temperature with no transistor performance loss. In addition, this FPU cannot be shut down for more than 1000 CPU cycles (1000ns) due to the workloads of interest. Is power gating still required using the lower leakage CMOS technology assuming a total FPU capacitance of 0.5nF (connected to its power supply) to be charged/discharged.

EE 382M VLSI-II Spring 2017 --- HW #3 Assignment

Assigned: March 10th, 2017   Due: April 11th, 2017

Problem 3.3: (15 points) Static RAM Design



a) In the 6T cell shown above, will increasing the strengths of transistors M3 and M6 make the cell more or less stable during a read?

b) In the 6T cell shown above, will increasing the strengths of transistors M1 and M4 make the cell more or less stable during a read?

c) What is the definition of Static Noise Margin? Sketch a 'butterfly' curve in 'data retention' state and in 'read' mode. Describe any differences if any.

d) How would you reduce power consumed by the 6T memory cell shown above and not compromise the performance of the cell?

e) If you had the circuitry to implement both READ and WRITE assist, how would you change the 6T bitcell design to make it as small as possible?

f) <u>Problem 3.4 (20 points):</u> Single core .vs. dual-core Power-Performance trade-off

a) You need to decide whether a *single* core processor or a *dual* core processor (using the same core) can provide the maximum performance under a maximum power budget set by your customer. Using Ptotal = Pdyn + Pleak and the following assumptions:

Assumptions:

- ***Vmin*** and ***Vmax*** are the minimum voltage and maximum voltages, respectively, that the cpu core can operate at. ***Vmax*** cannot exceed 1.5 * ***Vmin*** due to reliability limits.
- Frequency scales linearly with supply voltage (VDD) from ***Vmin*** to ***Vmax***.
- Leakage current is proportional to VDD^2.
- Performance is directly proportional to core frequency for a single core design.
- Dual core performance is 2X of a single core at the same frequency.

Given that the power budget for ***Pmax*** (@ ***Vmax***) cannot exceed ***3X*** of a single core ***Pmin*** (@ ***Vmin***), which design would you choose: a single core or a dual core solution for the best performance at the lowest total power? Show all your work for full credit.

b) Assuming that you chose a dual core implementation, in order to maintain a 2X performance over a single core implementation, each core's frequency must be 'bumped' up by 1.15X in order to compensate for operating inefficiencies. Is this still the best solution from a performance/power point of view? Did you exceed the Pmax <= 3X of Pmin budget?

EE 382M VLSI-II Spring 2017 --- HW #3 Assignment

Assigned: March 10th, 2017 Due: April 11th, 2017

<u>Problem 3.5 (10 points):</u> Power Reduction in CMOS circuits

a) List (in priority) all sources of power (both dynamic and leakage) that any CMOS circuit (with a ***Ceff*** capacitance) dissipates when powered by a ***VDD*** power rail and operated at ***F*** frequency.

b) Describe 3 methods to reduce ***leakage*** power ***without*** adversely affecting gate performance or overall block performance (something to keep in mind: typically, a small number of paths in a block or CPU set the maximum frequency of operation).

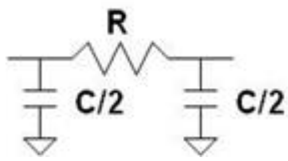
c) What is the difference between ***active*** leakage power and ***stand-by*** leakage power?

d) If power gates (PFET headers or NFET footers) are used to create power 'islands' to reduce stand-by leakage power, what care must be exercised for the interface signals between different power domains?

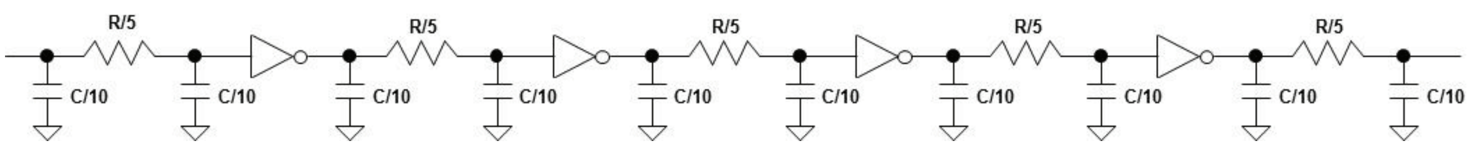
e) List one pro and one con of using a PFET header power-gate switch vs. an NFET footer device. What are the fundamental design trade-offs (or design criteria's) required in power-gate switch design?

Problem 3.6 (10 points): Interconnect

Using a pi-model for a METAL 6 interconnect, solve for the distance at which a total interconnect distance L has the same delay with 4 equally-spaced repeaters (use inverters) or with none; assume a delay of 20ps for each repeater, 25 ohm/micron and 0.20 fF/micron for the **METAL 4** in a **22nm** CMOS technology; show all your work. You can use this Pi-model for each interconnect segment:



No repeaters.



4 equally spaced repeaters.