Final Project Review

May 2, 2017

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Team Member Roles

Brandon
- Team management
- ECO
- Design Compiler
- Primetime / PTPX

Ari
- Primetime / PTPX
- Formality
- Data Extraction

Mike
- ECO
- Research
- Data Extraction

Nalin
- Team management
- IC Compiler
- Front-end advisor
- ECO

Priyam
- IC Compiler
- ECO
- Front-end advisor

Roger
- IC Compiler
- Research
- Data Extraction

Overview

- Review of Mid-Semester Status
- Final Results
- Project Strategy
- Concluding Remarks

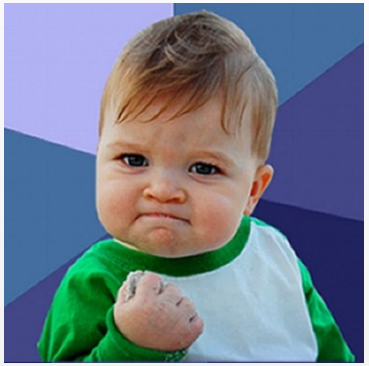
Review of Mid-Semester Status

Parameter	Target	Achieved
Cycle Time (ns)	8	8.02
Total Power (mW)	15	10.3
Die Area (mm^2)	0.7	0.663
Utilization (%)	85	69.24
Setup Worst Negative Slack (ns)	0	0.02
Hold Worst Negative Slack (ns)	0	3.84

LVS Errors	Comments
Floating Port	20 (some flops with unconnected QN pins)
Open	2 (VSS & VDD due to no actual power pads)
Min Area	40 (DDR pins)

Targets vs. Achievements

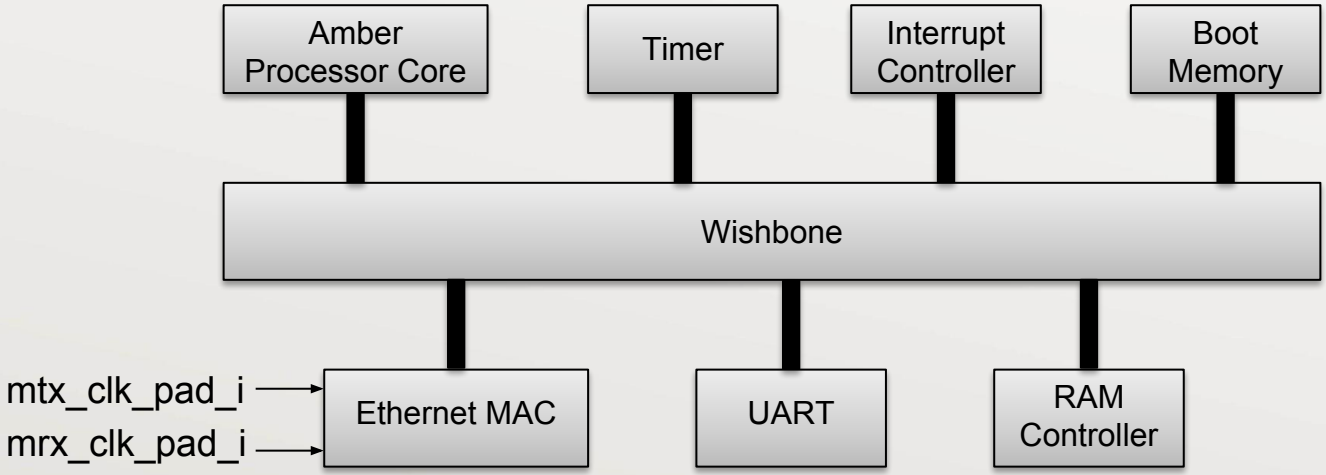
Category	Target	Achieved
Cycle Time (ns)	8	8
Total Power (mW)	15	10.3
Die Area (mm^2)	0.7	0.684
Utilization (%)	85	85.9
Setup Time Violations	0	0
Hold Time Violations	0	0
LVS Errors	0	0*



Project Strategy

System Block Diagram of RTL

- Amber25 processor core (ARM-compatible 32-bit RISC)
- 5-stage pipeline (fetch, decode, execute, memory, and write back)
- 32-bit Wishbone system bus
- Separate instruction and data caches (dcache and icache)
- sys_clk is clock of Amber processor core, the rest of the modules use sys_clk_slow
- **RTL bug found in memory where the clock and chip select are interchanged**



Synthesis Techniques

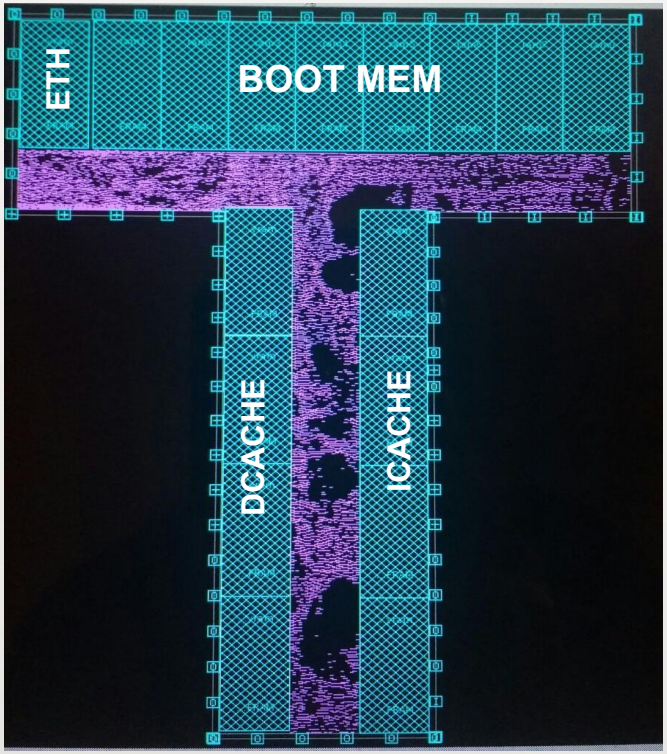
- Hierarchical versus Flat
- RVT versus HVT
- Over-constraining through uncertainty
- Do not use X0 standard cells

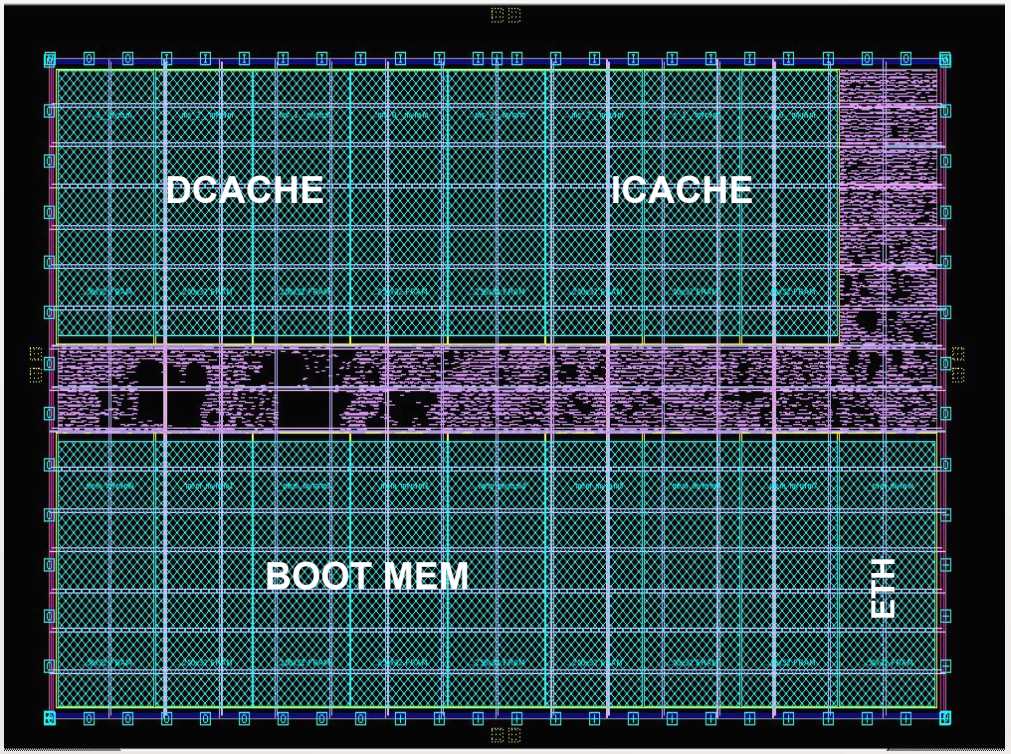
Library	floorplan.def	dc.tcl	Constraints file	Output	Cell Area	Changes
ss0p95vn40c	N/A	results/dc/dc_4.tcl	results/common/constraints_6.sdc	11	545900.7186	From output (10->11): changed ethernet clocks period to 40 from 16 in constraints_6.sdc per TA's request
ss0p95vn40c	N/A	results/dc/dc_4.tcl	results/common/constraints_7.sdc	12	547249.4601	From output (11->12): changed clock uncertainty in constraints_7.sdc to 0.8 from 1 to fix setuptime violation
ss0p95vn40c	N/A	results/dc/dc_4.tcl	results/common/constraints_8.sdc	13	547257.5927	From output (12->13): changed clock uncertainty in constraints_8.sdc to 0.15 for setup and hold in attempt to reduce area in floorplan
ss0p95vn40c	results/icc/floorplan_2.def	results/dc/dc_8.tcl	results/common/constraints_8.sdc	14	552582.1648	From output (13->14): dc_8.sdc is the same as dc_4.sdc, except is setup to run in Topological mode.
ss0p95vn40c	N/A	results/dc/dc_4.tcl	results/common/constraints_9.sdc	15	547257.5927	From output (14->15): No longer running in topo again (i.e, using dc_4.sdc again), until we can finalize an ICC ouput. Also using new constraints file that fixed incorrect input/output delays
ss0p95vn40c	N/A	results/dc/dc_9.tcl	results/common/constraints_9.sdc	16	547970.9754	From output (15->16): created dc_9.tcl so that it specifies clock network delays to match primetime's
ss0p95vn40c	N/A	results/dc/dc_10.tcl	results/common/constraints_9.sdc	17	547614.1577	From output (15->17): Added the line, "set_dont_use [get_lib_cells */*X0*] to match icc.tcl
ss0p95vn40c	N/A	results/dc/dc_10.tcl	results/common/constraints_10.sdc	18		From output 17->18: made new constraints_10.sdc. removed input delay on mrx_clk_pad_i
ss0p95vn40c	N/A	results/dc/dc_10.tcl	results/common/constraints_11.sdc	19		Overconstrained
ss0p95vn40c	N/A	results/dc/dc_10.tcl	results/common/constraints_12.sdc	20		Uncertainty removed
ss0p95vn40c	N/A	results/dc/dc_10.tcl	results/common/constraints_13.sdc	21		Reduce unceratainty from 10% in iter_19 to latency values from icc_10 results
ss0p95vn40c	N/A	results/dc/dc_11.tcl	results/common/constraints_11.sdc	22	549590.6349	From output 19->22: dc_11.tcl now adds RVT cells into the target libraray

Floorplans Revisions

- Design decisions:
  - Floorplan shapes- rectangular, rectilinear (T, L, U)
  - Symmetrical or unsymmetrical
  - Placement of SRAMs and Ethernet
  - Orientation of Macros
  - Spacing
  - Core Height and Width
  - Placement Blockages

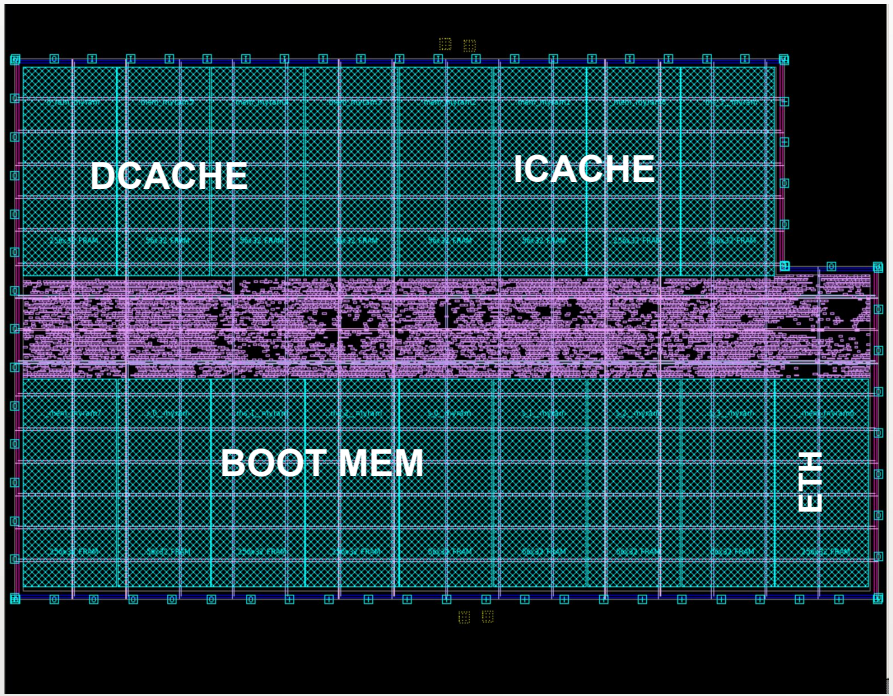
Floorplans (1)



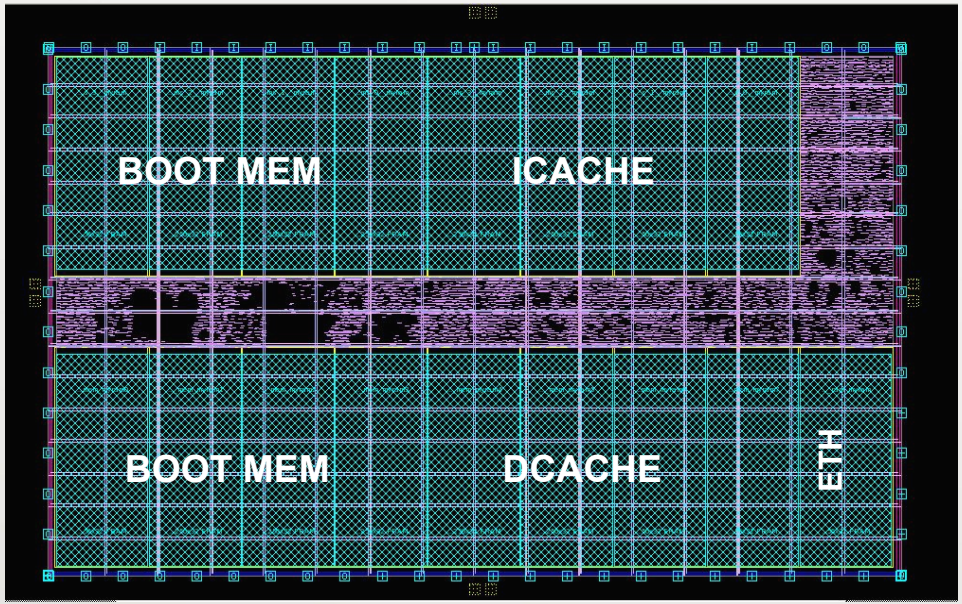


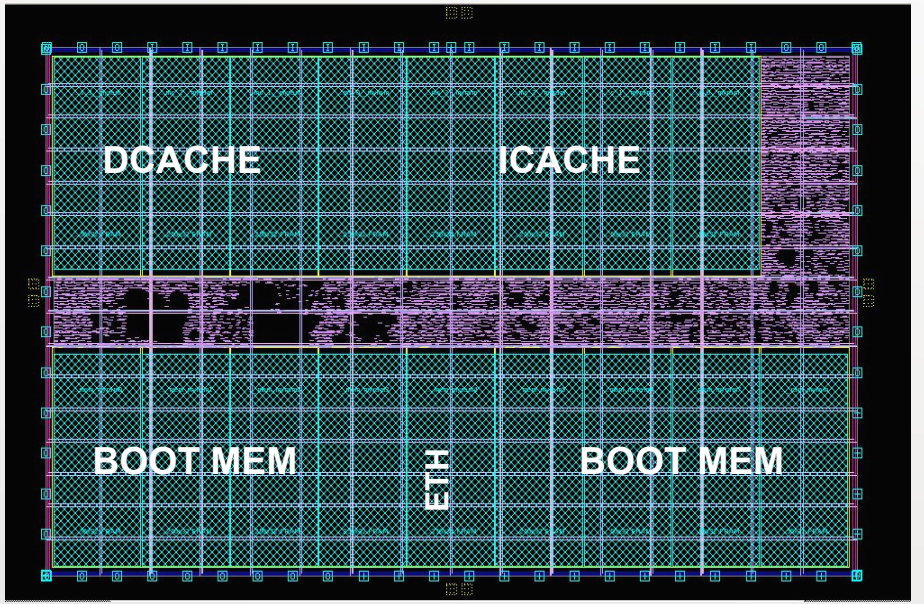
Floorplans (2)

- Rectilinear function to remove the top right rectangle
- Compact Floorplan
- Issues
  - Utilization rate
  - IO and clock pins
  - Routing congestion



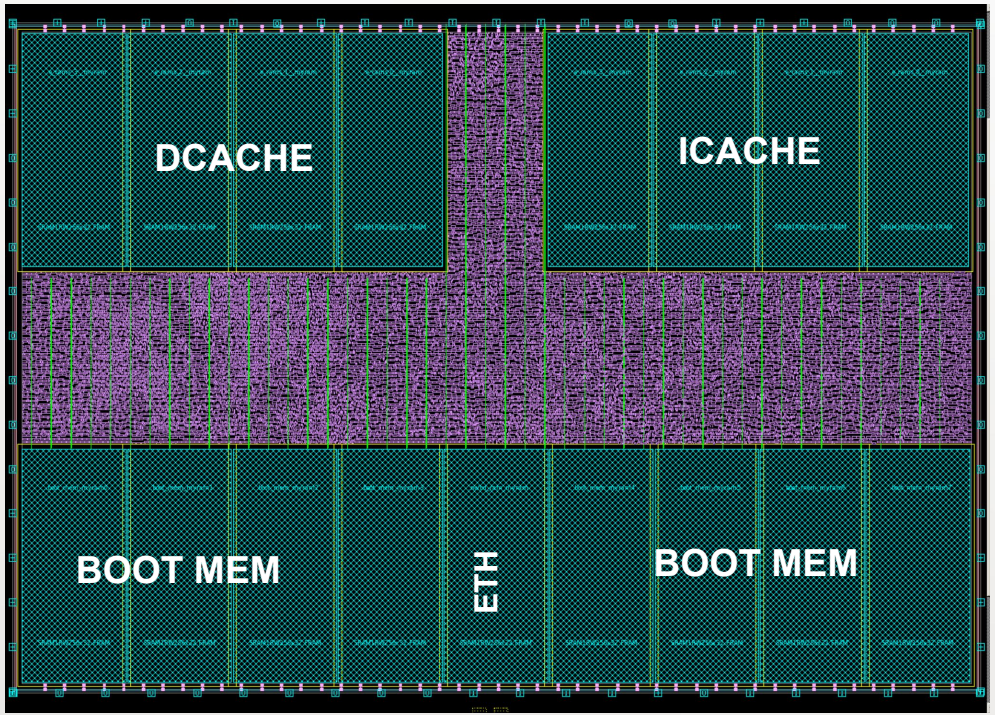
Floorplans (3)





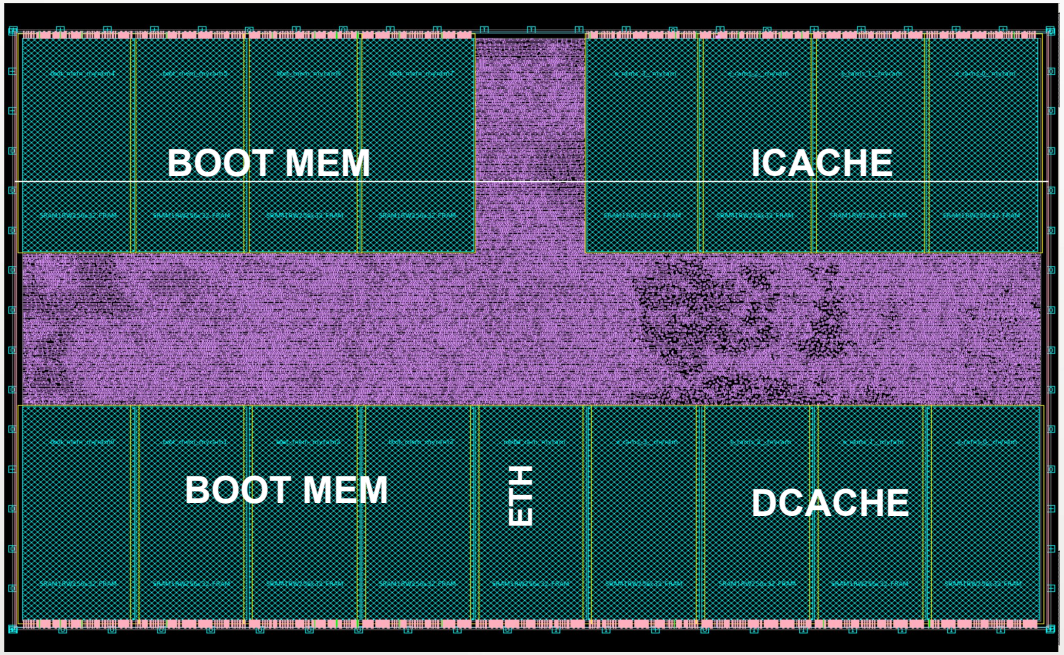
Floorplans (4)

- Another thought on symmetric floorplan
- Boot memory 0-3 followed by ethernet and boot memory 4-7 - Bottom
- Dcache and Icache on the top



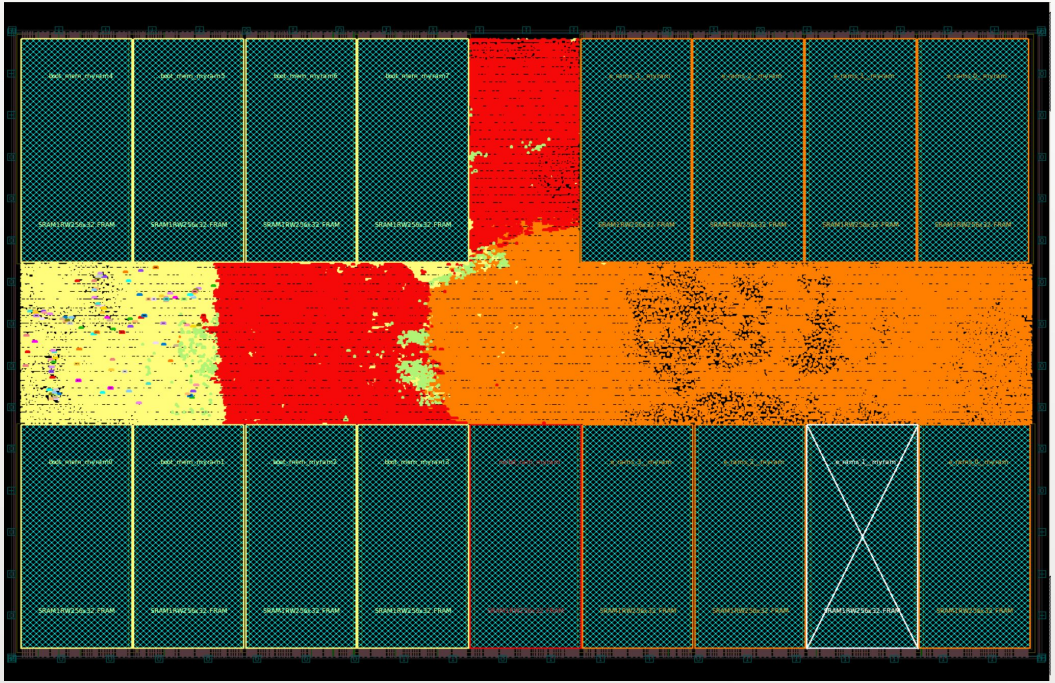
Final Floorplan

- Reposition for Boot memory and cache
- Boot memory 0-3 on the bottom
- Boot memory 4-7 on the top
- Ethernet in the center



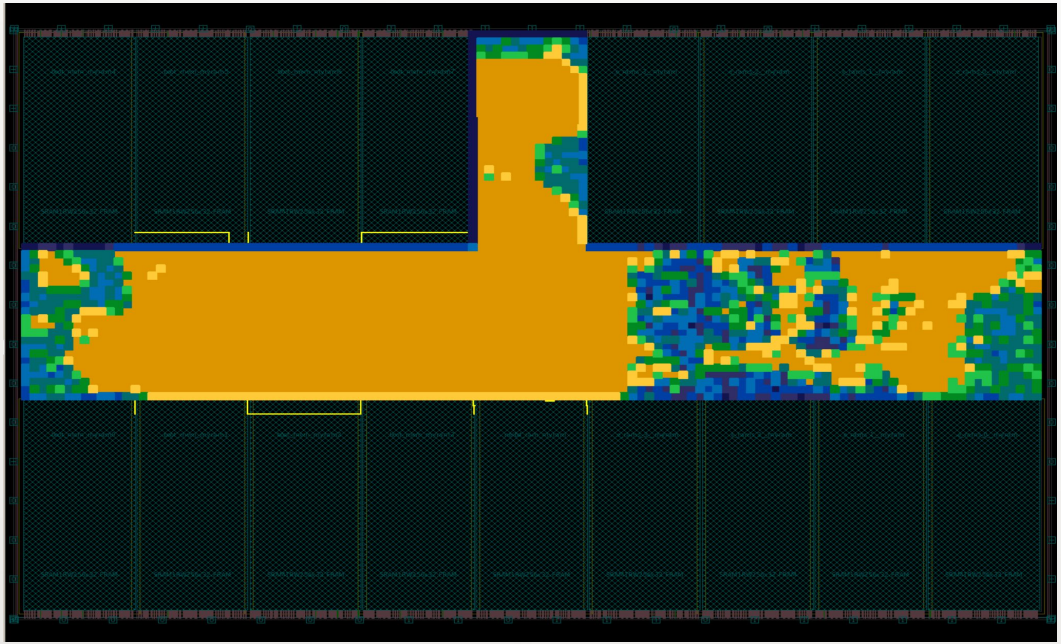
Placement Hierarchy

- ORANGE- Amber
- RED- Ethernet
- YELLOW- Others



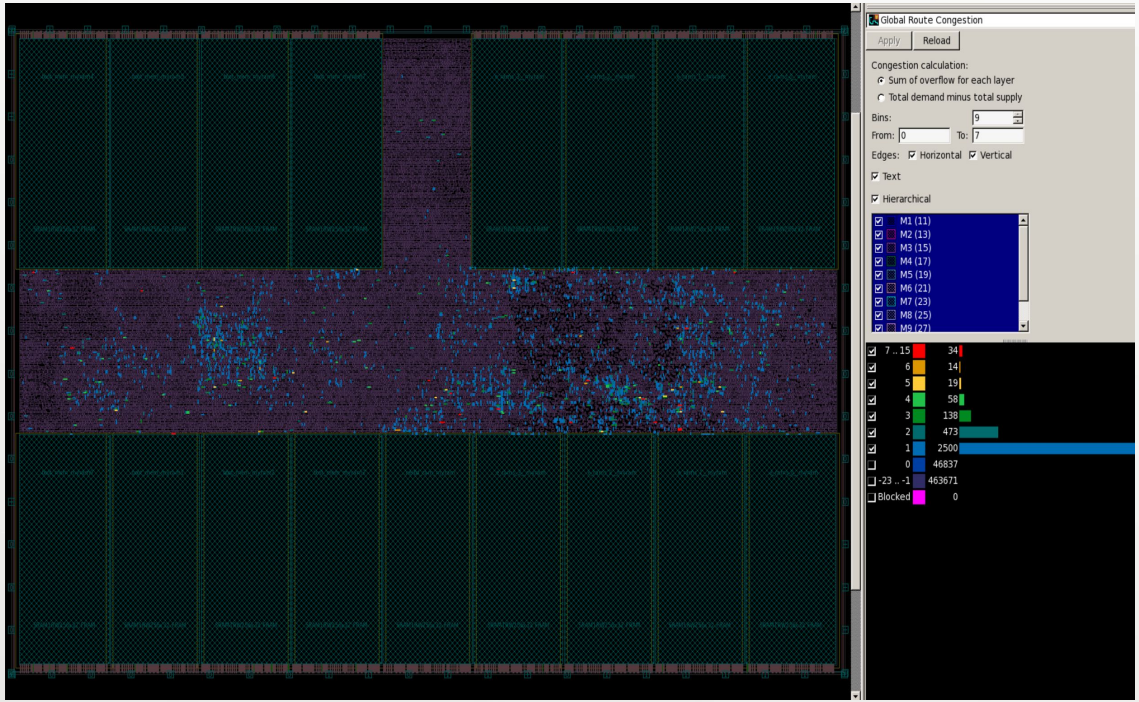
Cell Density Map

- Utilization is = 85.9%
- Blue-Very low cell density
- Green- Low cell density
- Yellow- High cell density
- Overall No cell congestion



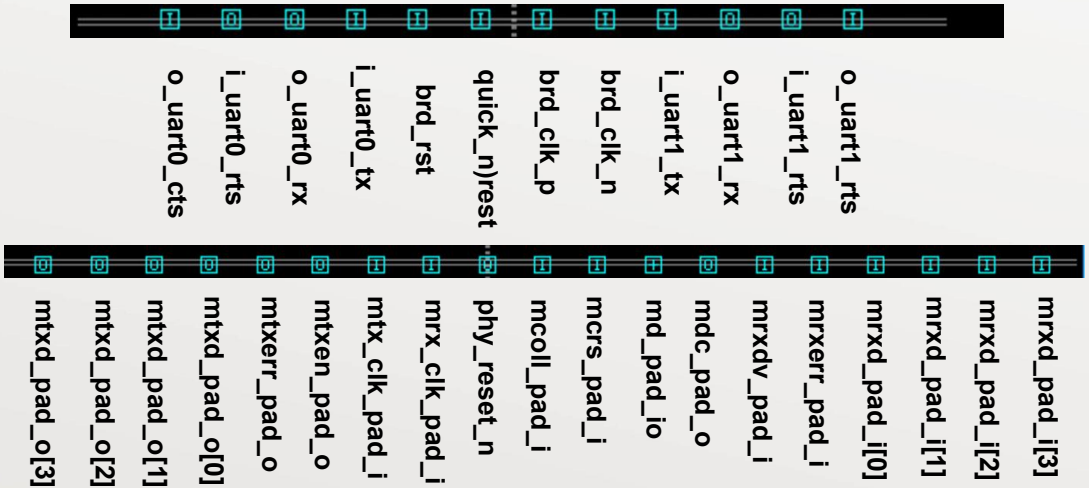
Congestion Map

- Very low routing congestion
- Blue- High congestion
- Overall No routing congestion

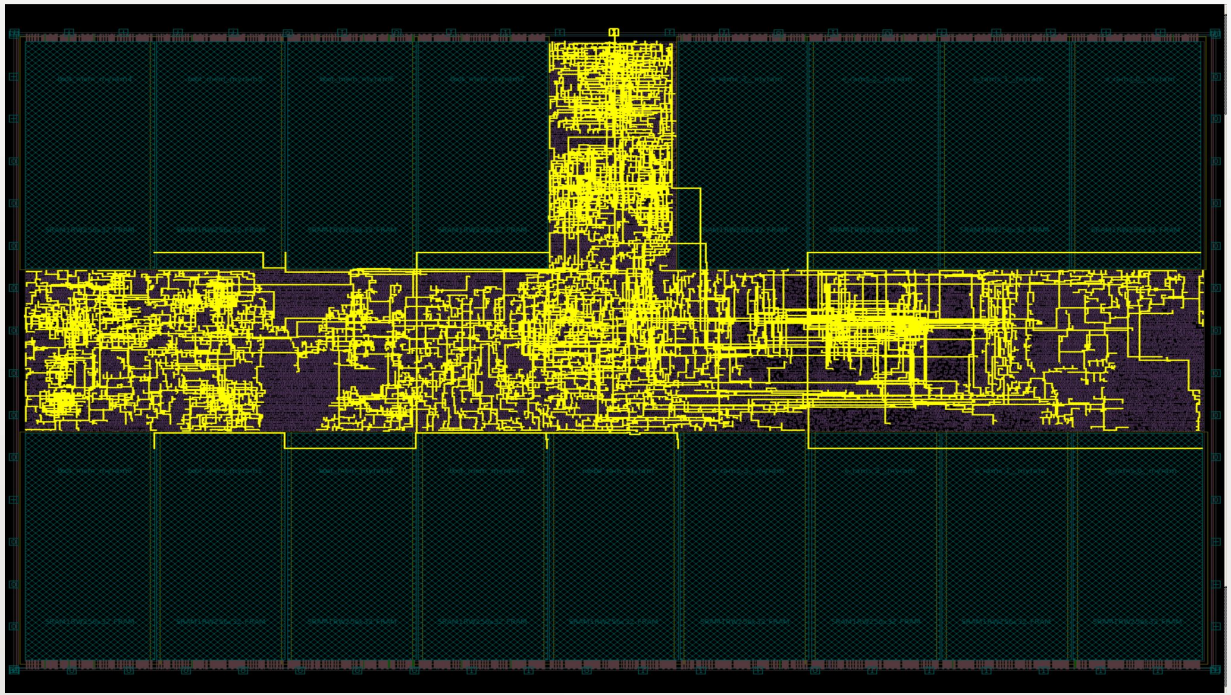


IO Placement

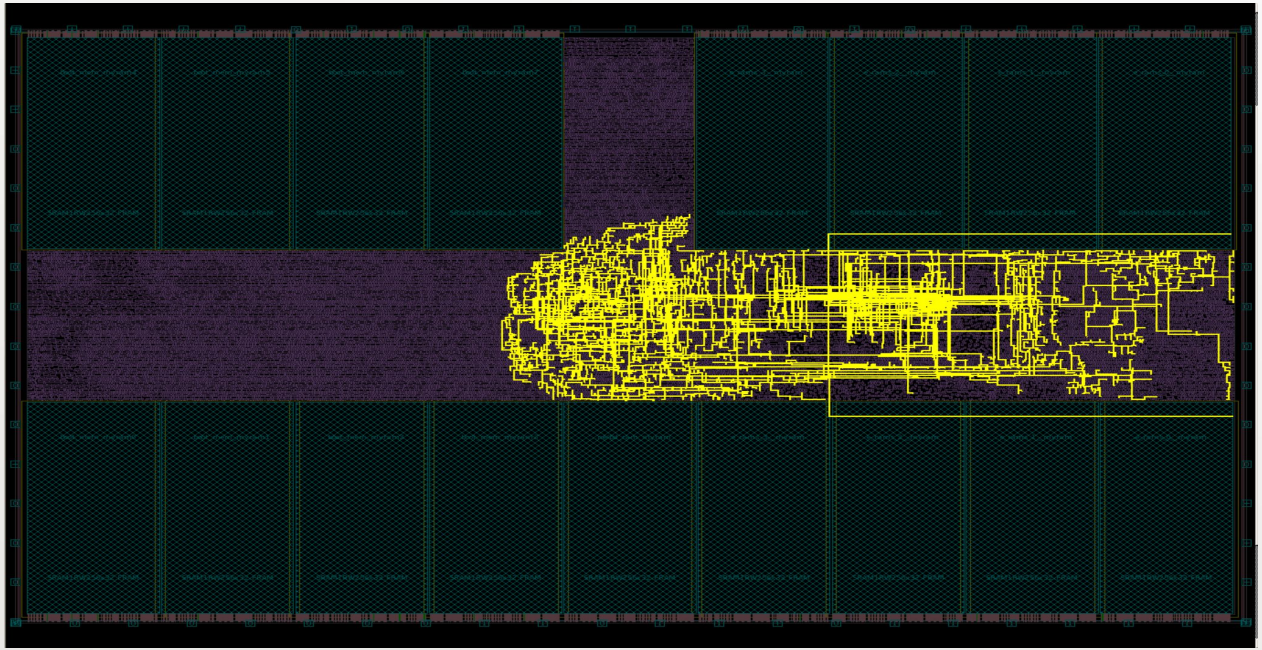
- Bottom: signals of eth_top; Top: signals of uart0 and uart1
- Center: common (important) signals i.e. clk, reset
- Symmetric



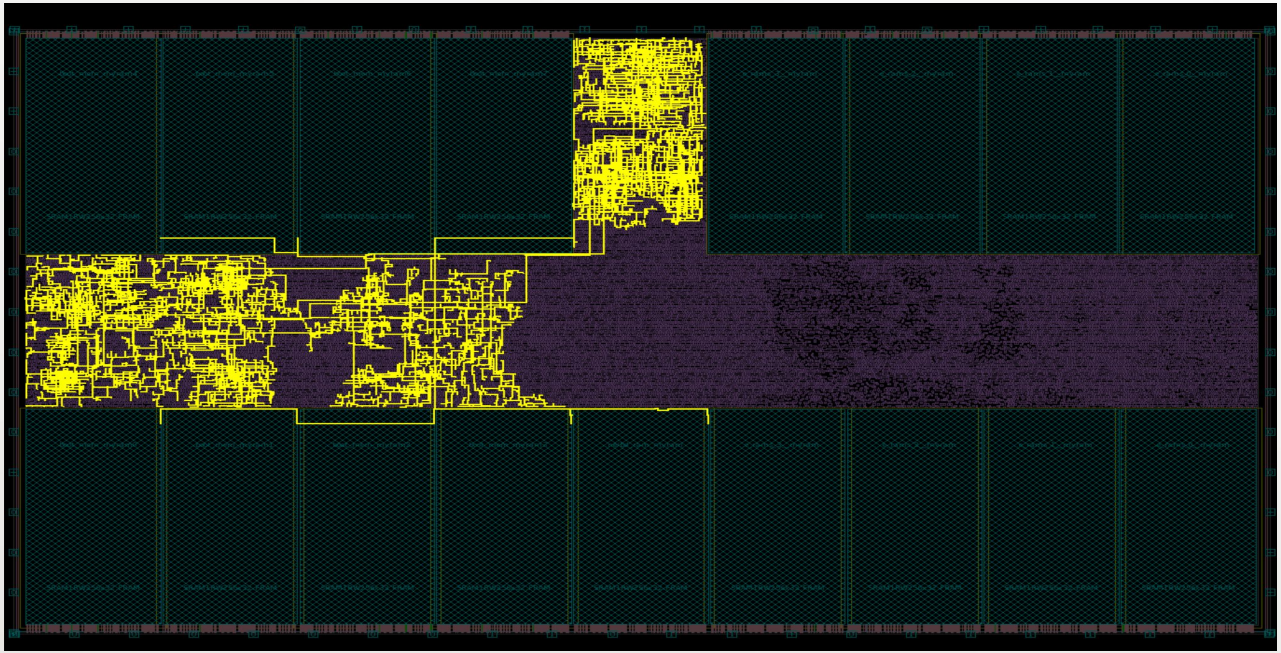
Final CTS Result - brd_clk



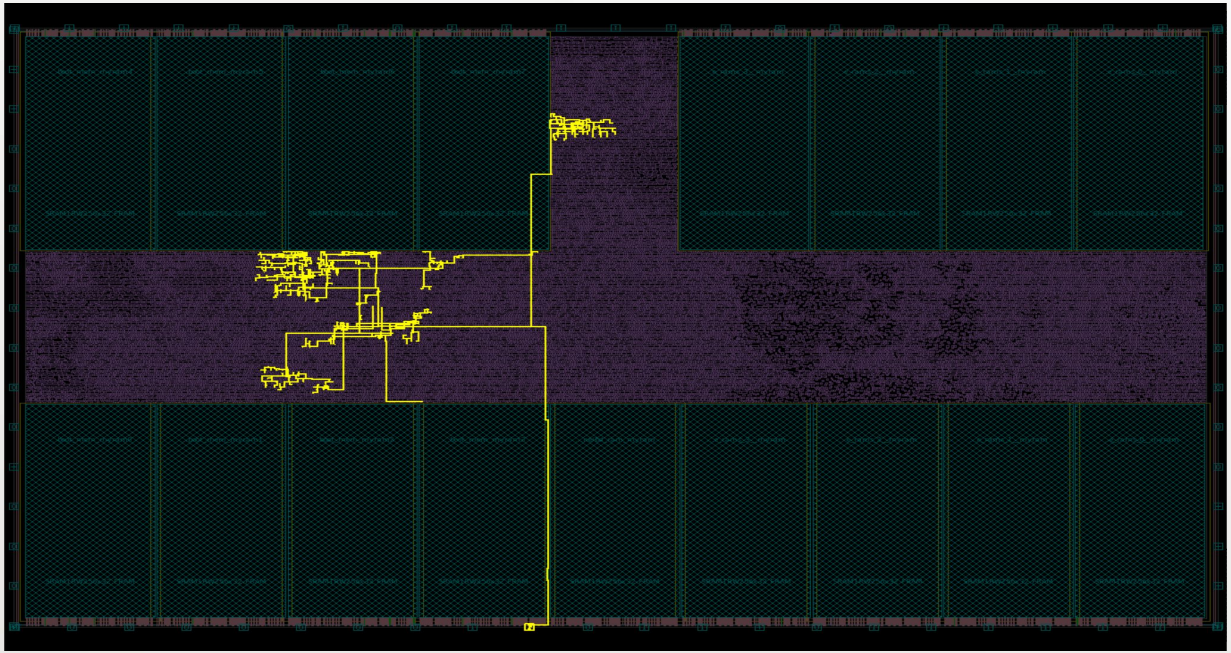
Final CTS Result - sys_clk



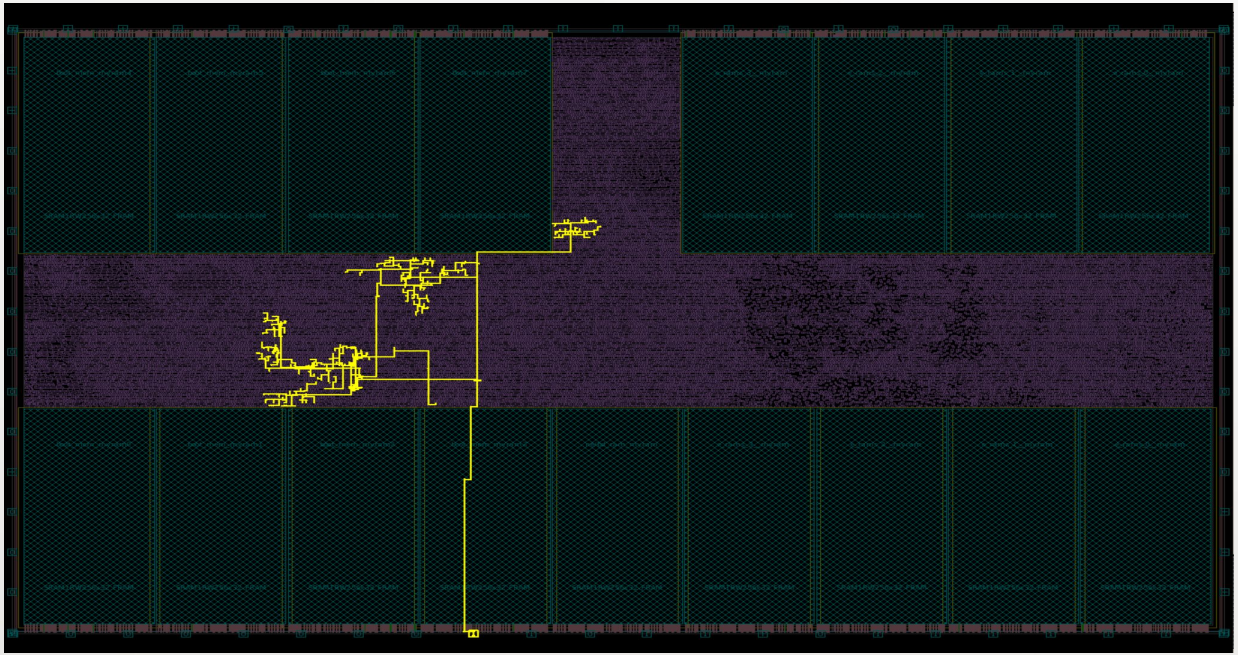
Final CTS Result - sys_clk_slow



Final CTS Result - mrx_clk

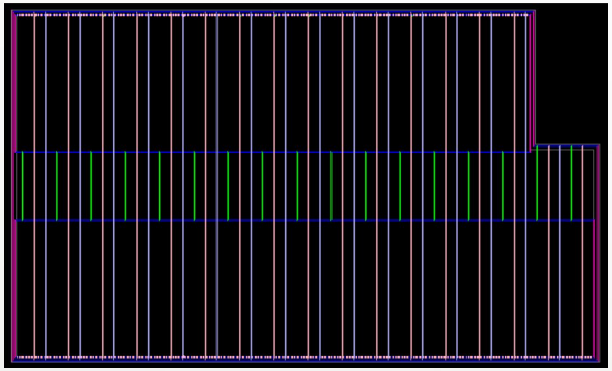


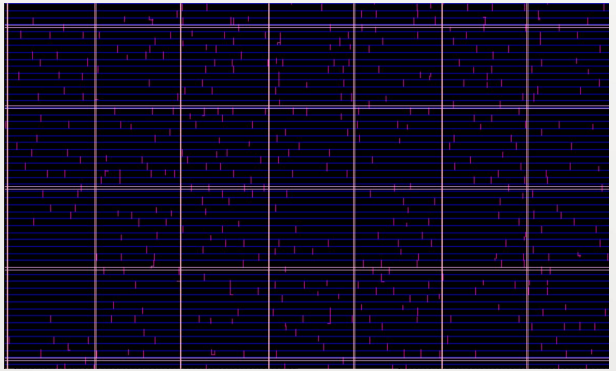
Final CTS Result - mtx_clk

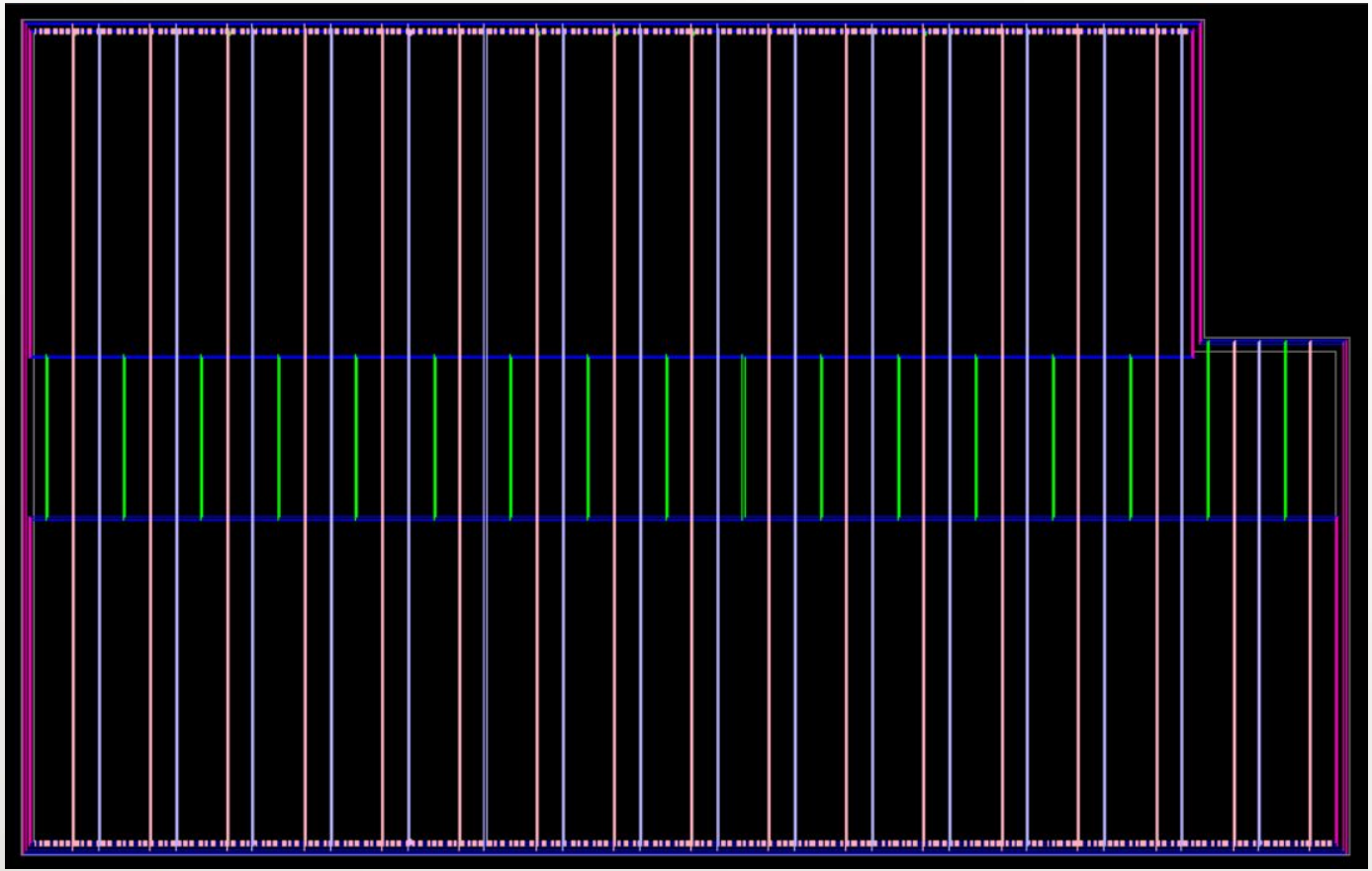


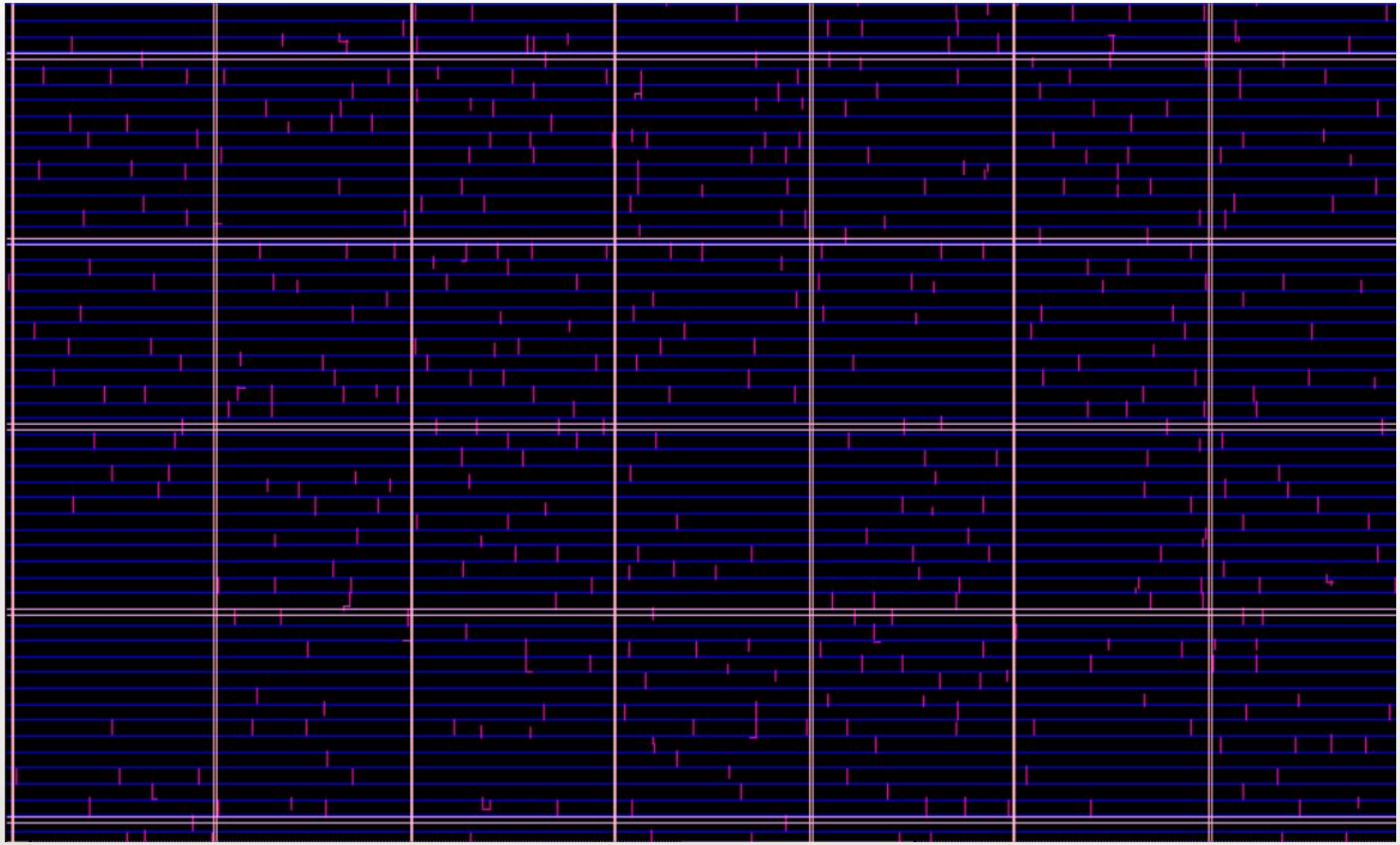
Power Grid

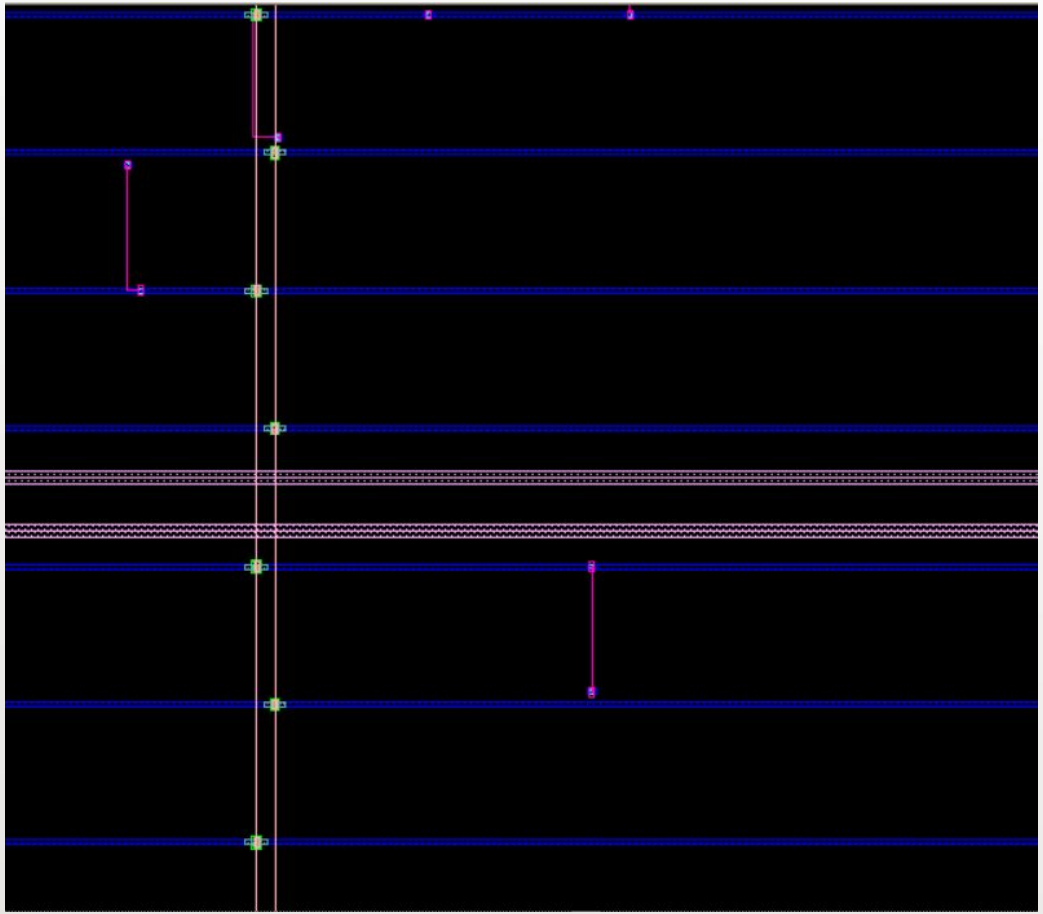
- Design decisions
  - Metal layer for straps
  - Number of horizontal straps
  - Number of vertical straps
  - Width of straps
  - Location of straps
  - Ring around macros
  - Ring around core
  - Metal layers for ring
  - Placement of virtual pads
  - Type of PG routing
  - Metal layers for PG routing





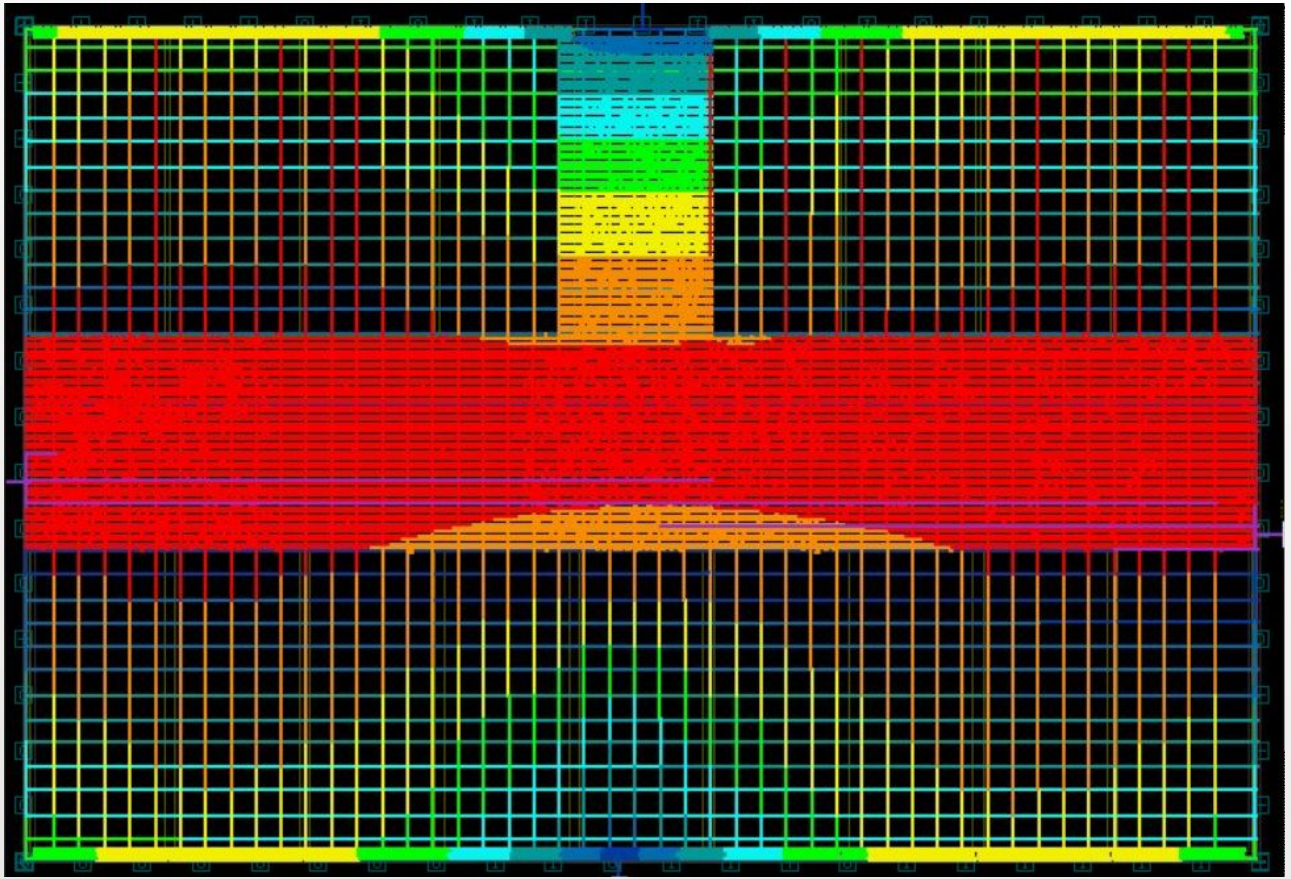






IR Drop

- Max of 76.3mV
- Preroute vias
- More straps over macros



LVS Errors

```
** Total Floating ports are 20.
** Total Floating Nets are 0.
** Total SHORT Nets are 0.
** Total OPEN Nets are 0.
** Total Electrical Equivalent Error are 0.
** Total Must Joint Error are 0.

-- LVS END : --
```

Floating ports are 5000+ (20 is just the default max error number)

The only LVS errors are:

- Floating port due to unconnected memory outputs and QN of Flops.
- MIN Area LVS errors due to DDR ports.

ICC Versus PT Inconsistency

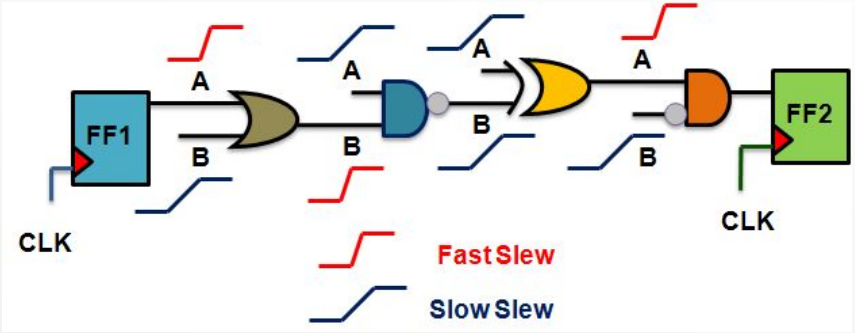
- check_primetime_icc_consistency_settings

- Input clock delay inconsistency
  - An input clock delay on the clock port is considered for timing analysis by Primetime but not by ICC.
  - This was causing setup violations of more than 6ns in PT while no such violations in ICC.
  - FIXED by setting ignore_clock_input_delay_for_skew to TRUE in ICC

- Operating condition inconsistency
  - Default analysis mode in ICC is bc_wc while in PT it is On Chip Variation (OCV)
  - FIXED by changing to OCV in ICC

OCV vs BC_WC

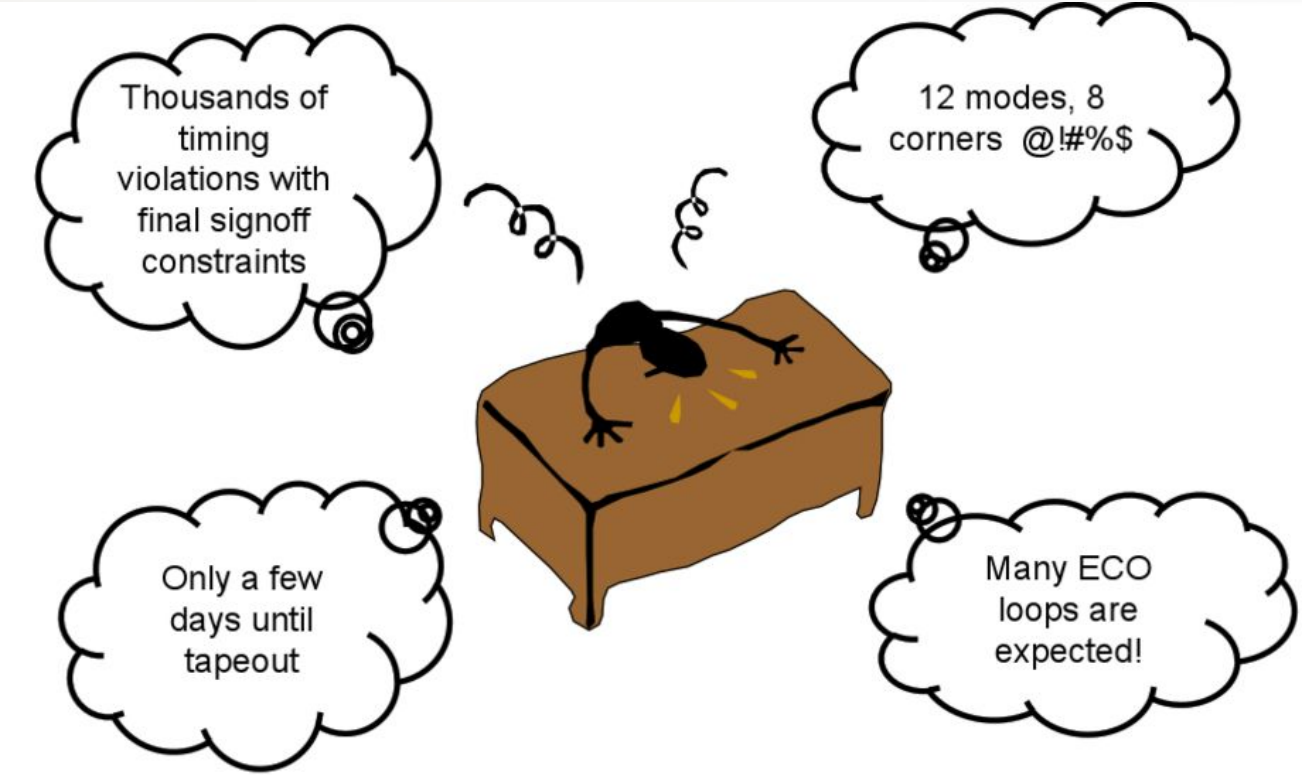
- Slew Propagation



vlsi-soc.blogspot.com

- Bc_wc
  - Setup paths: Max delay arcs for both launch and capture
  - Hold paths: Min delay arcs for both launch and capture
- OCV
  - Setup paths: Max delay for launch and min delay for capture
  - Hold paths: Min delay for launch and max delay for capture

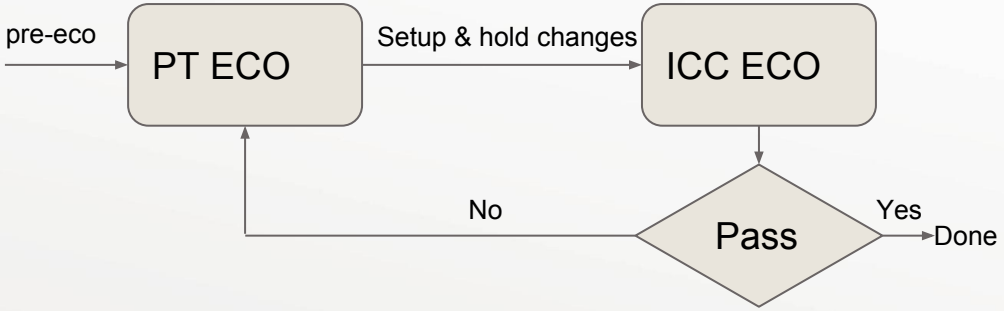
ECO

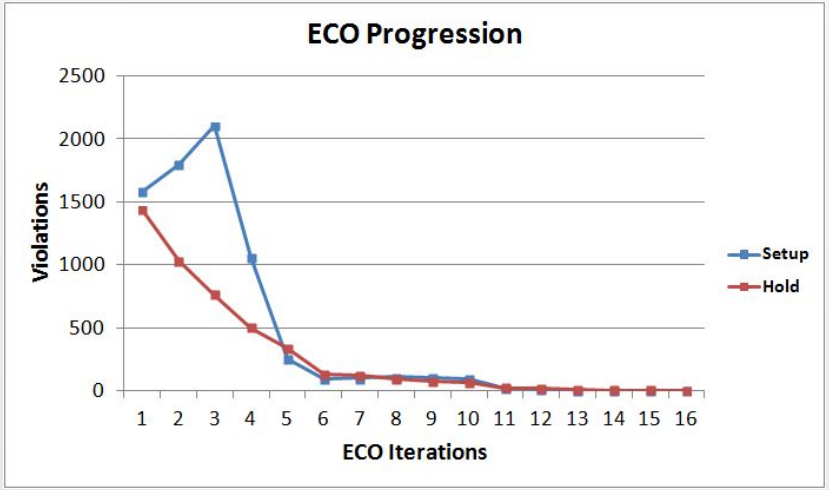


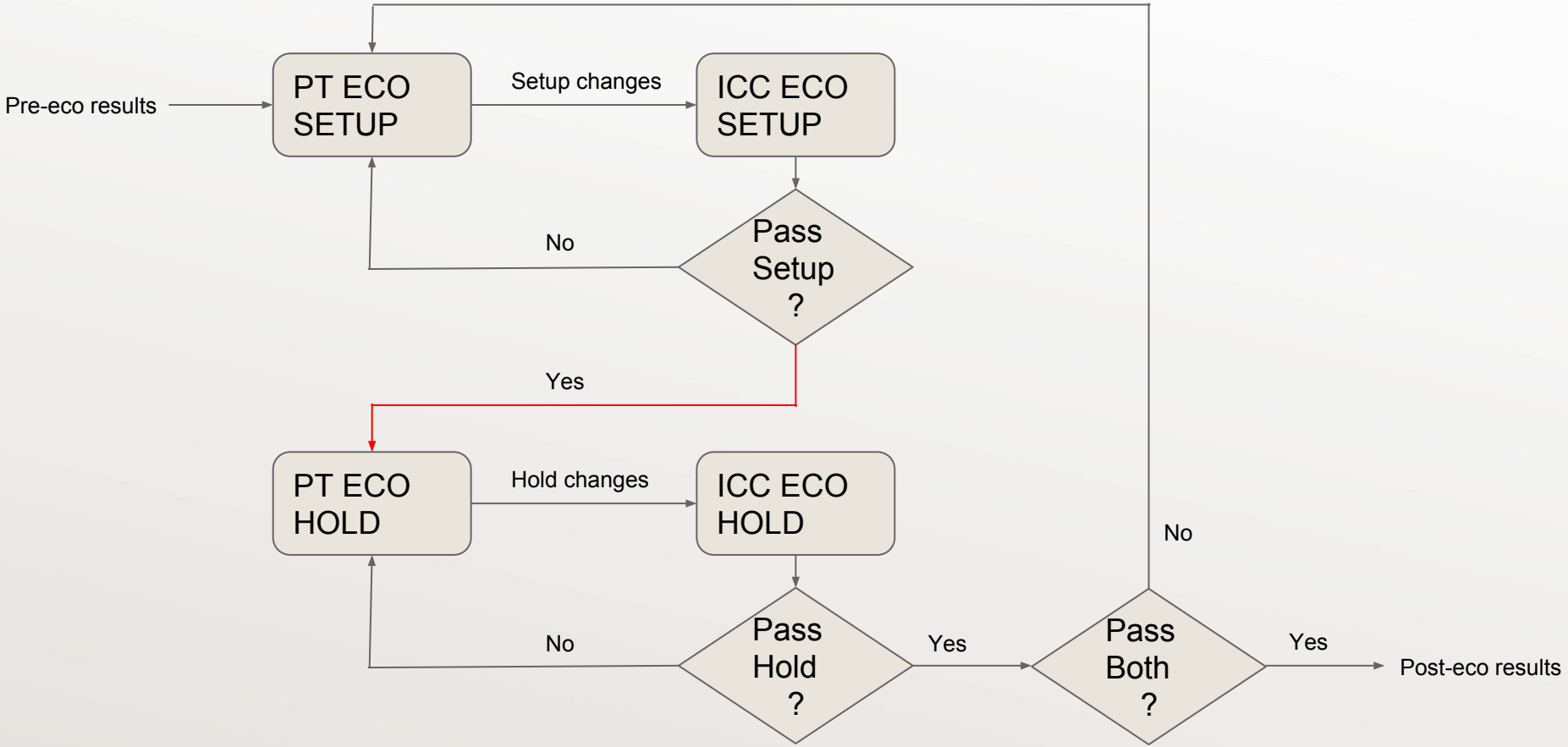
https://wenku.baidu.com/view/ec9a6e2e3169a4517723a3ce.html###

ECO

- We tried fixing setup and hold times in a single ECO flow. Able to converge in both, but we went over our power budget.
- With this method, it is hard to properly load in libraries and specify operating conditions when running both corners at the same time.
- Due to this, we tried fixing setup & hold violations in separate ECO flows. We can now successfully remove all of the timing violations.

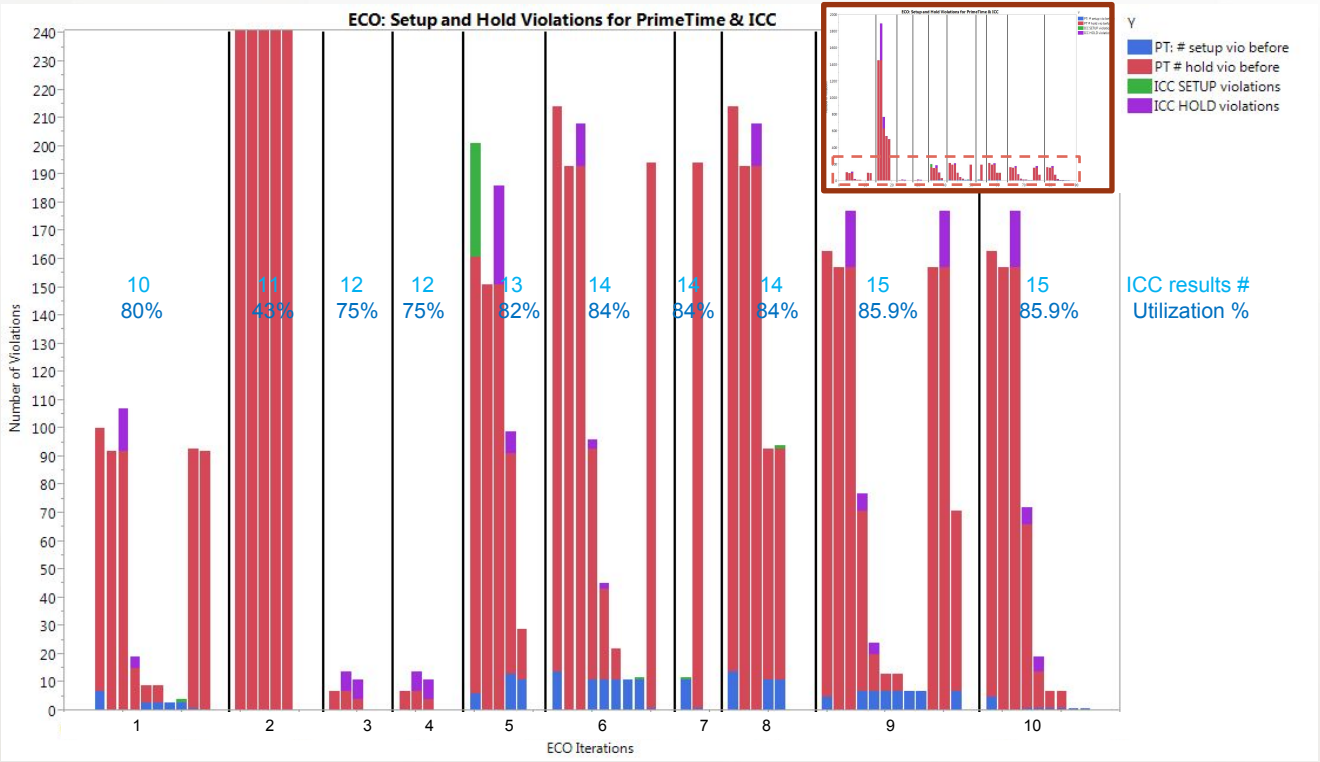





Pre-eco results
PT ECO SETUP
Setup changes
ICC ECO SETUP
Pass Setup ?
No
Yes
PT ECO HOLD
Hold changes
ICC ECO HOLD
Pass Hold ?
No
Yes
Pass Both ?
No
Yes
Post-eco results

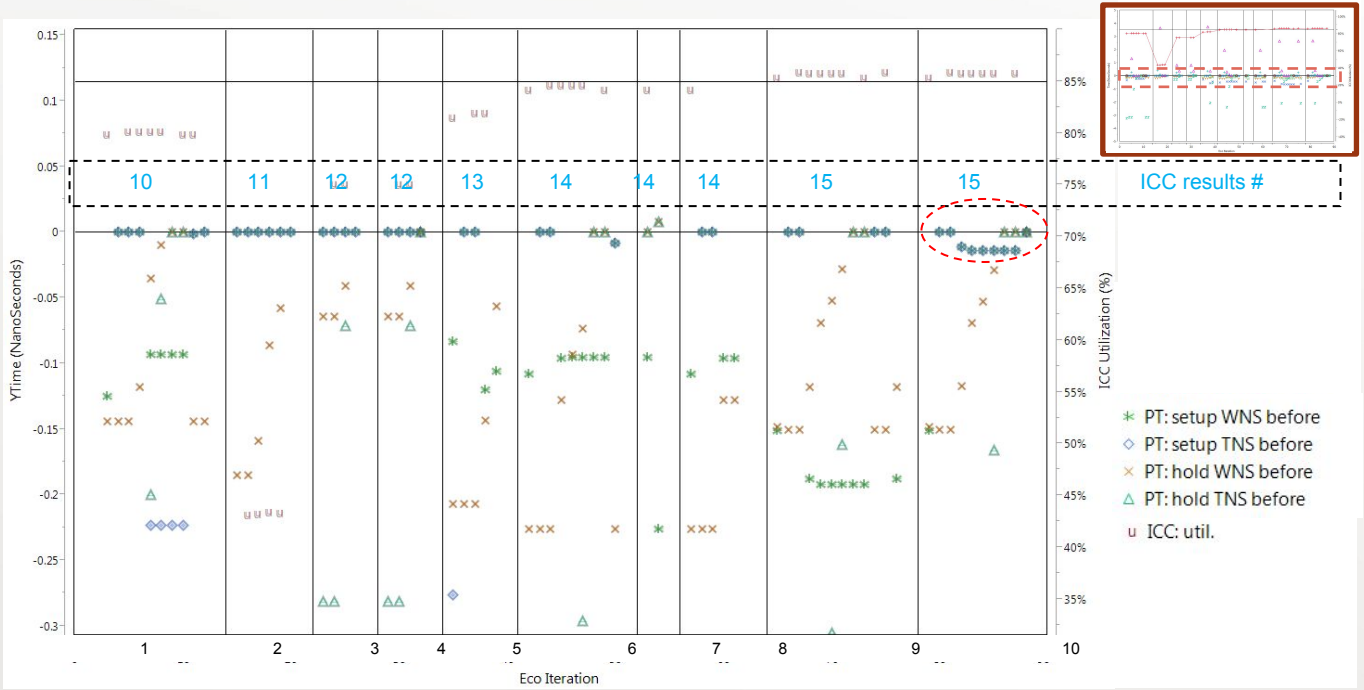
ECO – Setup and Hold Time Violations

- Initial problem with convergence when fixing setup violations followed by hold violations, where setup violations occur after hold fixes
- Setup ECO re-run after hold ECO to address resulting setup violations from hold fixing
- Floorplan modifications to reduce “pre-eco” utilization % to lower congestion and help routing

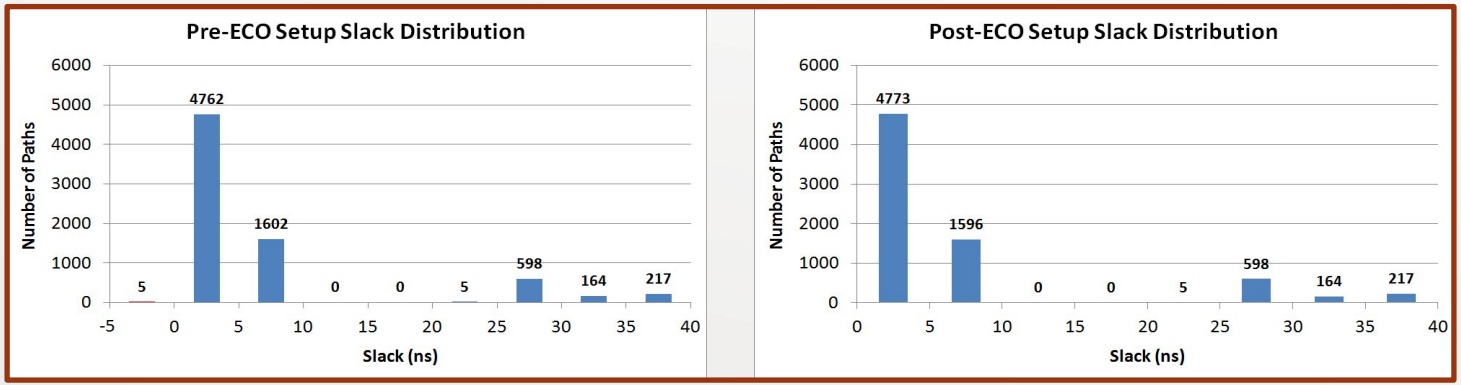


ECO – Positive/Negative Slack

- As expected, showed same response as setup and hold violations.
- Final converging ECO iteration displayed more setup negative slack during Primetime hold fixing than previous iterations, but still converged.



Setup and Hold – Slack Distributions

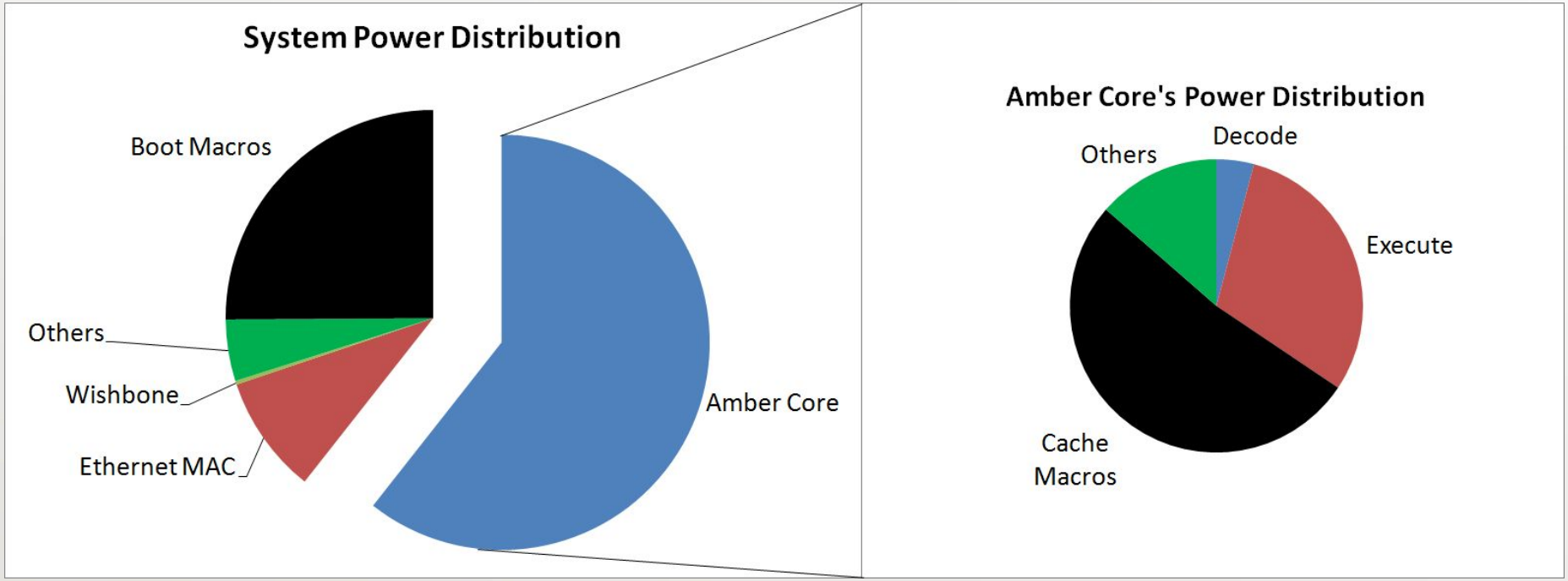


Power Approach and Issues

- Activity factors set for flat netlist
  - Inputs set at 0.25
  - All modules at 0.25
  - Clocks set at 0.5
- Periods
  - Everything set to 32ns, except for amber core which uses 8ns
- Issues encountered with PTPX
  - Mapping activity factor to non-hierarchical topology with cells not being split per module
  - Hard to extract power of some specific cells with non-hierarchical topology
  - No actual issues with meeting power specification, expect when we tried fixing setup and hold times in a single ECO flow

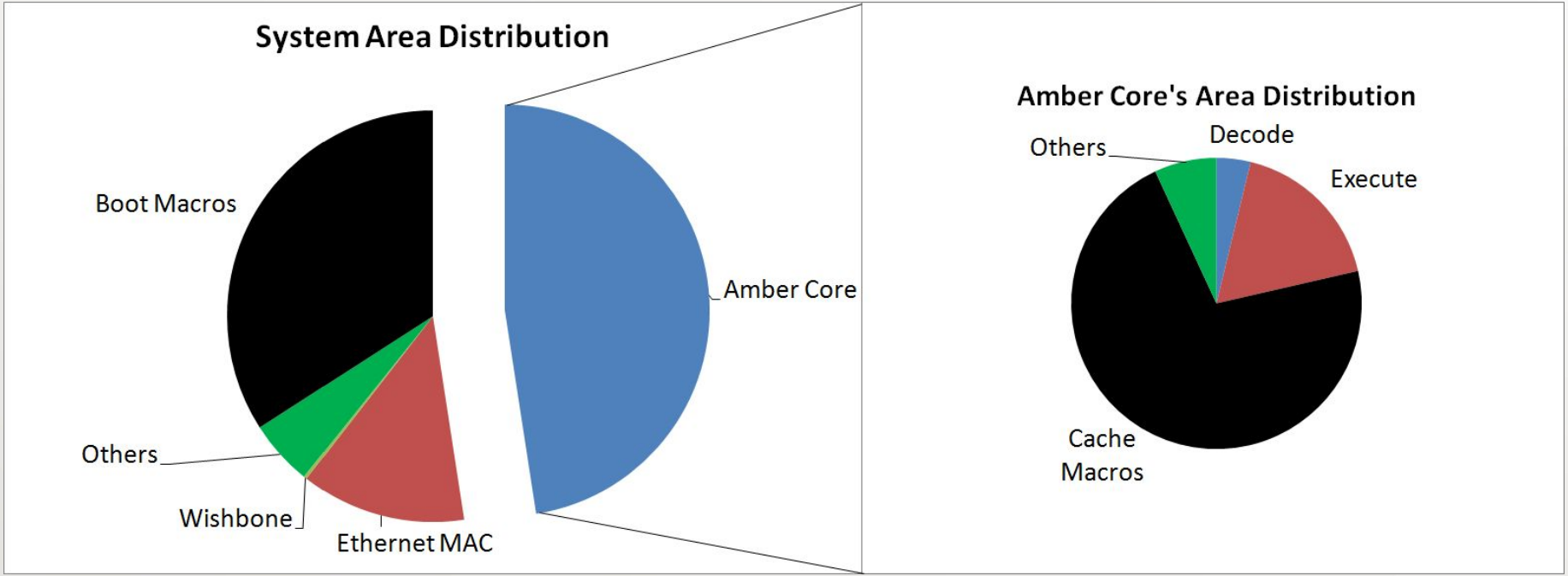
Power Analysis

Total power = 10.3 mW



Area Analysis

Total area = 0.684 mm^2



Formality

- Modified provided scripts to match our design
- Running concurrently throughout the design process
- DC Formality Result
  - In comparison to the RTL
  - Ran formality of final DC result
  - All succeeded
- ICC Formality Result
  - In comparison to DC result
  - Ran formality of final ICC result
  - All succeeded

Matched Compare Points	BBPin	Loop	BBNet	Cut	Port	DFF	LAT	TOTAL
Passing (equivalent)	748	0	0	0	13	5823	0	6584
Failing (not equivalent)	0	0	0	0	0	0	0	0

Formality - Not Compared Points

- 305 Clock-gate LAT
  - Inserted by DC
  - Used to reduce dynamic power dissipation
  - Idle devices on clock network that do not affect the functionality of the design
- 4 Constant reg
  - Initial assignments are not synthesizable
  - Values of registers remaining constant
- 46 don’t verify
  - Do not verify undriven primary outputs
- 1 unread (on DC formality only)
  - Does not drive anything and provides no effect on compare points

Not Compared

Clock-gate LAT							305	305	
Constant reg						4	0	4	
Don't verify	0	0	0	0	46	0	0	46	
Unread	0	0	0	0	0	1	0	1	**(Only in DC formality)**

****

Concluding Remarks

Potential Risks

- In an actual SOC design, IO Placement would also depend on connecting blocks
- IR drop information not propagated to timing and power analysis
- Inaccurate power estimate due to lack of test vectors
- Won’t meet specs if memory bug is fixed. Also won’t work because of the bug
- Can use low power SRAM for better power results
- Unavailability of a memory compiler limits the possible floorplans
- Actual implementation would require strict sign off checks at more corners
- Should be DRC clean for implementation
- Must design to compensate for real world devices (leave margin of error)
- Even though we were diligent, there is still potential for misjudging the importance of warnings provided by tools.

Reflection on Project

What Would We Have Done Differently?

- Use preferred ECO flow
- Do not try to optimize every step right from the start
- Trial and error is not always the best solution
- Automate with care
- Do not dismiss any tool warnings without verification
- Dedicate more people on ICC
- Better team management
- Better record of every step of the project

Summary

- Review of Mid-Semester Status
- Final Results
- Project Strategy
- Concluding Remarks

Category	Target	Achieved
Cycle Time (ns)	8	8
Total Power (mW)	15	10.3
Die Area (mm^2)	0.7	0.684
Utilization (%)	85	85.9
Setup Time Violations	0	0
Hold Time Violations	0	0
LVS Errors	0	0*

Questions?

Appendix A: Total Power Results

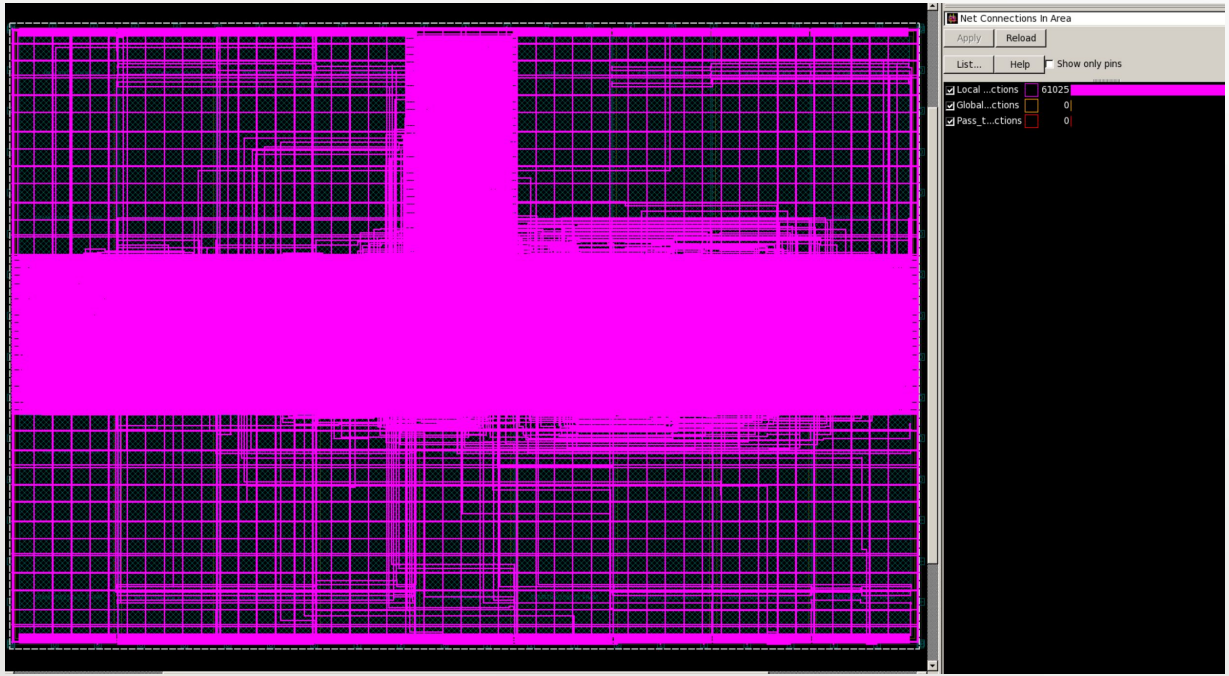
Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
u_amber	4.494e-03	1.010e-03	7.402e-04	6.244e-03	(60.66%)	u
u_decode	1.064e-04	6.345e-05	8.816e-05	2.580e-04	(2.51%)	u
u_execute	8.186e-04	6.889e-04	3.835e-04	1.891e-03	(18.37%)	u
u_iobuf	5.960e-08	2.280e-07	1.358e-07	4.234e-07	(0.00%)	u
u_wishbone_arbiter	1.049e-05	8.889e-06	1.078e-05	3.016e-05	(0.29%)	u
u_eth_top	2.754e-04	7.552e-05	5.973e-04	9.482e-04	(9.21%)	u
u_icache_srams	1.420e-03	3.377e-06	0.0000	1.423e-03	(13.82%)	u
u_dcache_srams	1.818e-03	6.017e-06	0.0000	1.824e-03	(17.72%)	u
u_eth_srams	1.235e-04	2.249e-06	0.0000	1.258e-04	(1.22%)	u
u_boot_mem_srams	2.584e-03	1.572e-06	0.0000	2.585e-03	(25.11%)	u
all_srams	5.945e-03	1.321e-05	0.0000	5.958e-03	(57.88%)	u
clock_network	2.545e-04	9.293e-05	1.164e-04	4.638e-04	(4.51%)	i
register	1.083e-04	2.334e-05	2.218e-04	3.535e-04	(3.43%)	
combinational	1.189e-03	1.085e-03	1.245e-03	3.519e-03	(34.18%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	5.945e-03	1.321e-05	0.0000	5.958e-03	(57.88%)	
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	

Net Switching Power	= 1.214e-03	(11.80%)
Cell Internal Power	= 7.497e-03	(72.83%)
Cell Leakage Power	= 1.583e-03	(15.38%)

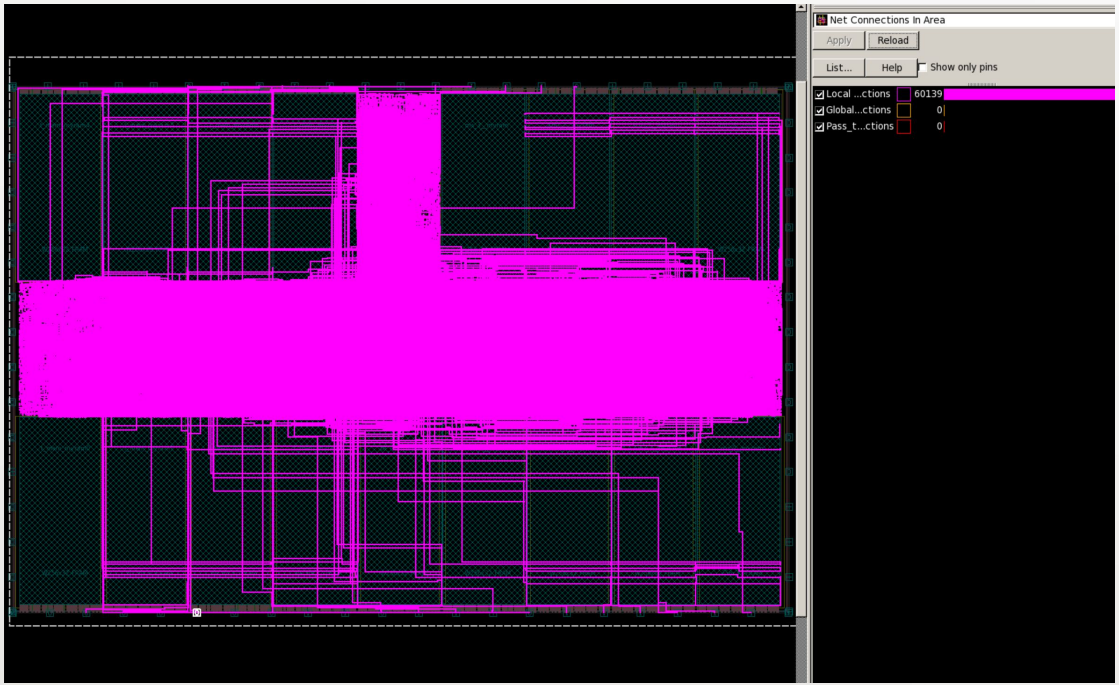
Total Power	= 0.0103	(100.00%)

Appendix B: Net Connections

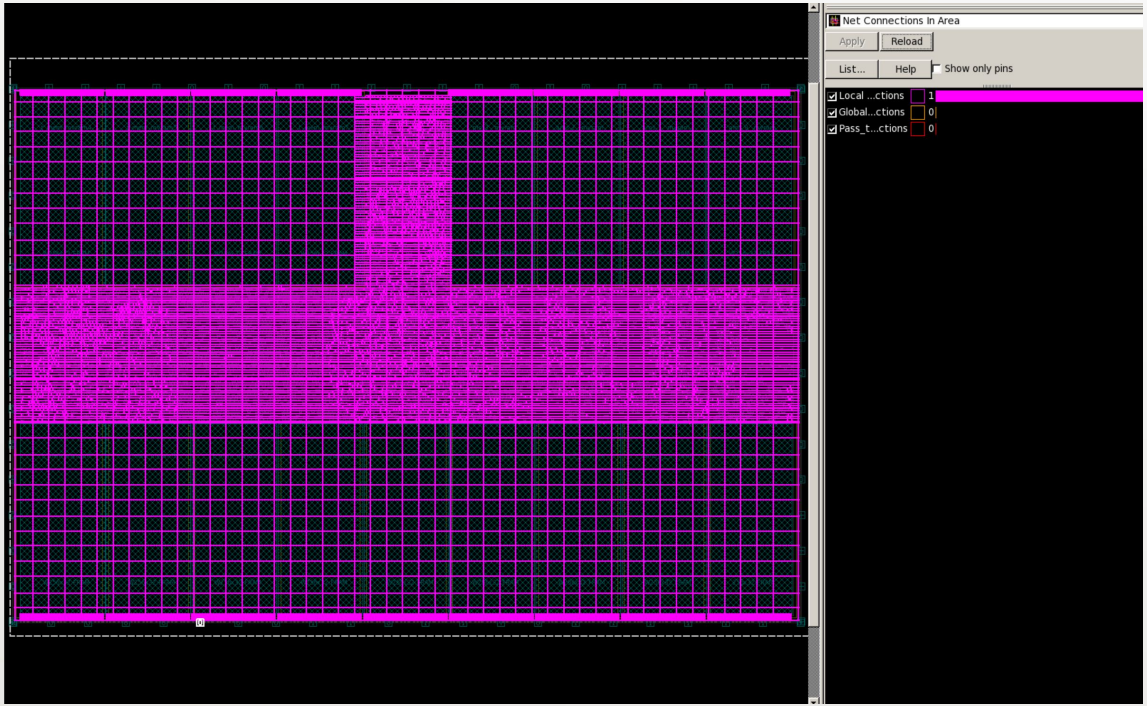
Final Cell Placement (Net Connection)



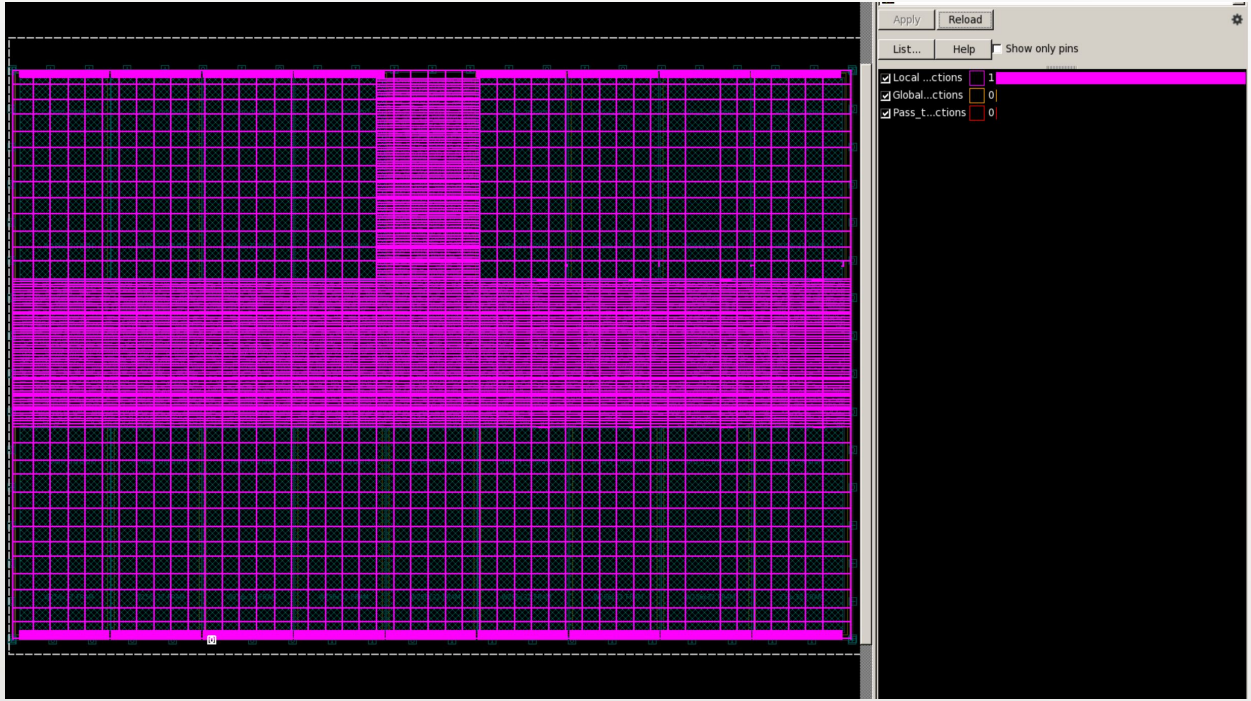
Final Cell Placement (Net Conn-Signal)



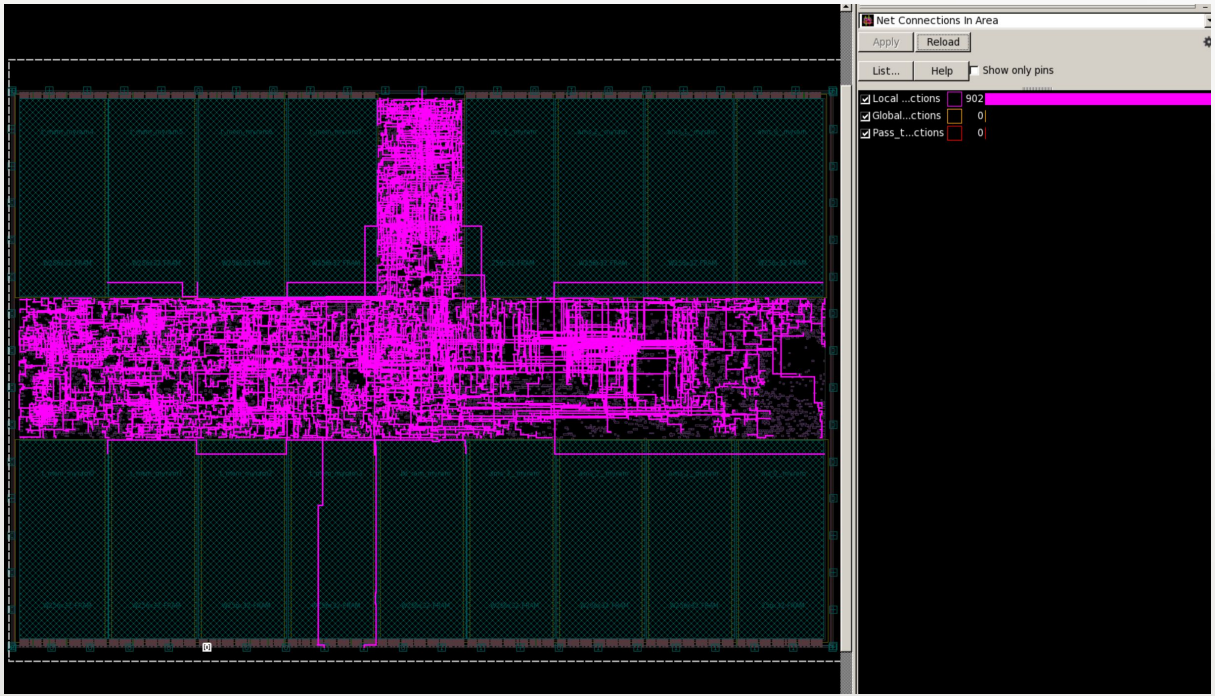
Final Cell Placement (Net Conn-Power)



Final Cell Placement (Net Conn-GND)



Final Cell Placement (Net Conn-CLK)



Appendix C: Issues and optimizations

Issues & Optimizations Summary

- Floorplan Optimization techniques
  - Multiple Iterations
- Power planning
- Clock Tree Synthesis
- IO Placement
  - Driven by CTS and routing
- Cell Placement
- DRC and LVS
- Static Timing Analysis
  - Hold time fixing
- Power Estimation