Mid-Semester Project Review

March 7, 2017

Team 2:
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Brandon Boesch
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Ari Levy
Priyam Sachdeva
Michael Schippers

Team Member Roles

Brandon
- Team management
- Design Compiler
- Primetime/PTPX

Ari
- Design Compiler
- Formality
- Scripts to extract and analyse data

Mike
- Design Compiler
- Formality
- Research

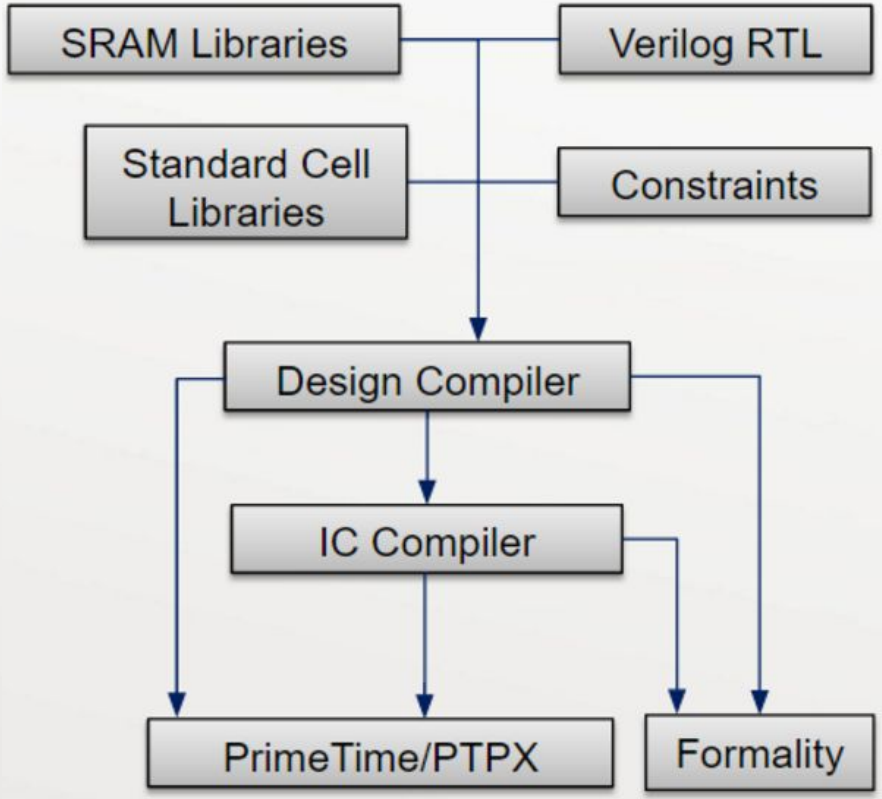
Nalin
- Team management
- IC Compiler
- Front-end advisor

Priyam
- IC Compiler
- Front-end advisor

Roger
- IC Compiler
- Research
- Primetime/PTPX

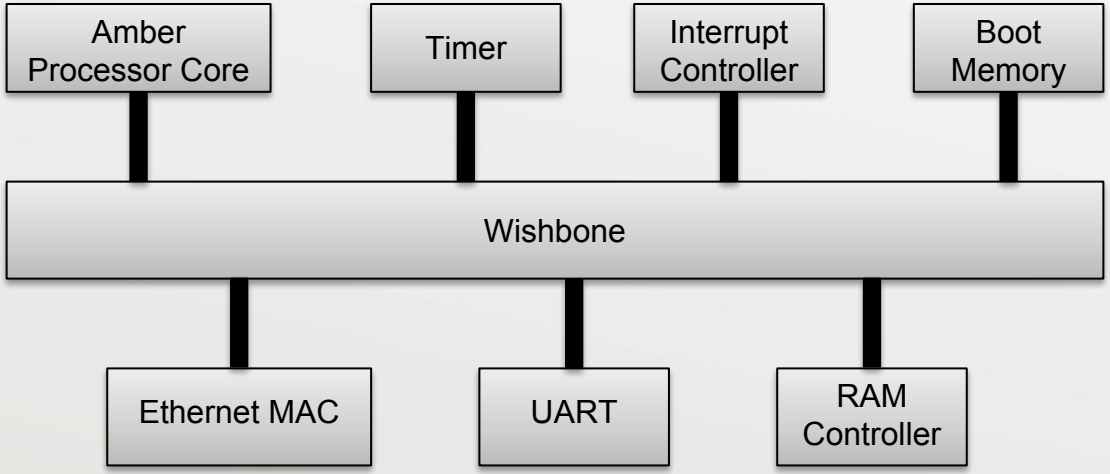
Overview

- Early Design Planning (EDP)
  - Low Power Design Specifications
- Front End Design
  - Synthesis Optimization
  - STA Effort
  - Power Analysis Effort
- Back End Design
  - Physical Design Flow
- Potential Risks
- Future Steps



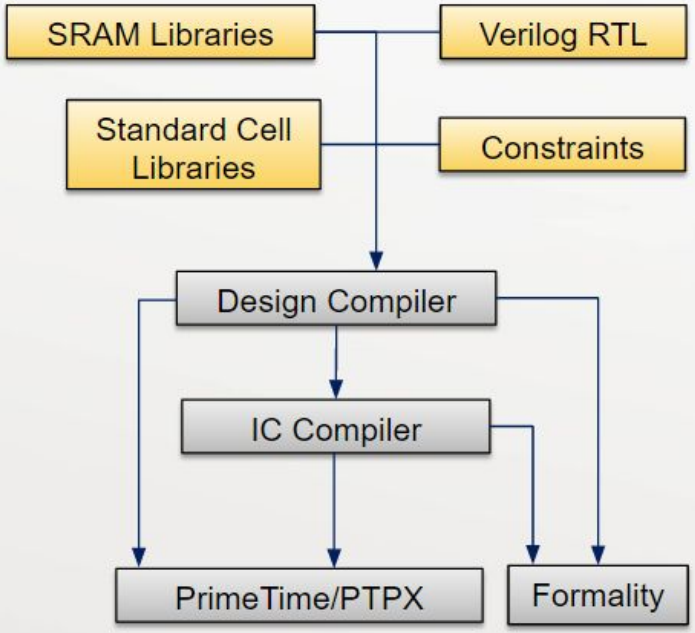
System Block Diagram

- Amber25 processor core
  - ARM-compatible 32-bit RISC
- 5-stage pipeline
- 32-bit Wishbone system bus
- Separate instruction and data caches



Early Design Planning (EDP)

- Review of design environment
- Literature survey of design and optimization methodologies
  - https://opencores.org/amber-core.pdf
  - “A 90nm Power Optimization Methodology and its’ Application to the ARM 1136JF-S Microprocessor”
- Established project management strategy
- Initial responsibilities assigned
- Setup design environment
  - Github project directory setup
  - Script creation/modification
- Mapped out interfaces and connectivity



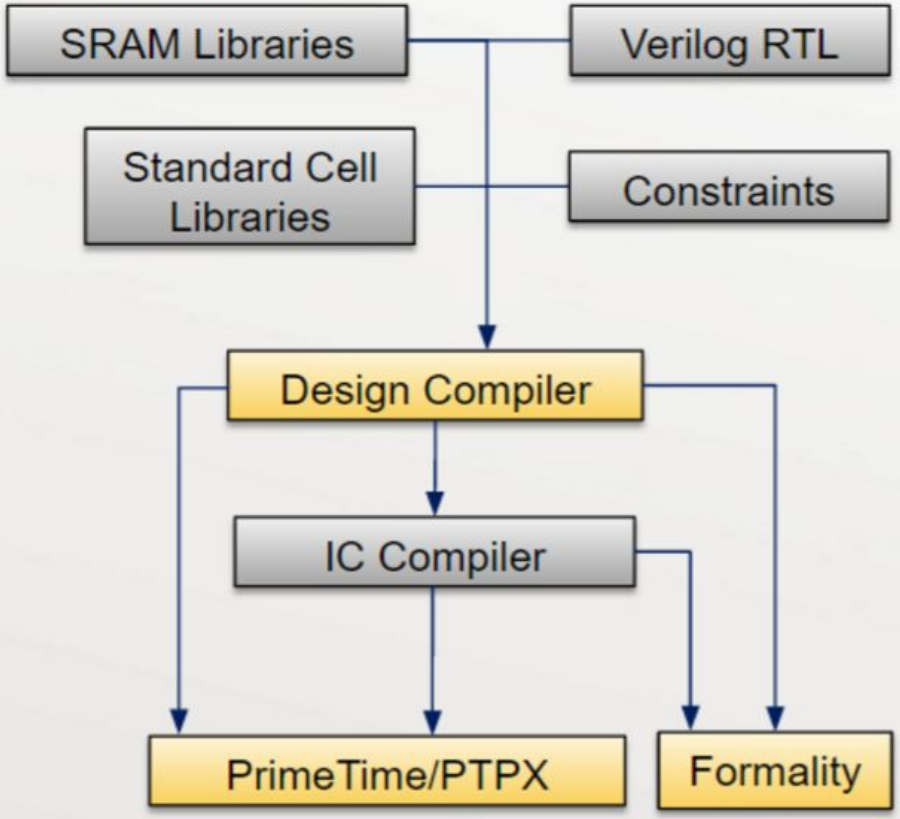
Low Power Design Specifications

- Determined proper design constraints
- *VT* and corner selection
  - ***ss0p95vn40c*** vs *ss0p95v125c*
  - ***HVT*** vs. *RVT/LVT*
- Constraints
  - *brd_clk_p* 8ns
  - sys_clk 8ns
  - sys_clk_slow 32ns
  - mtx_clk & mrx_clk 40ns
  - *clock_uncertainty* 0.15ns
  - *input_delay* 20% of module's clock
  - *output_delay* 20% of module's clock

Categories	HVT	RVT	LVT
Leakage Power	1	7.2	33.7
Delay	1	0.78	0.64

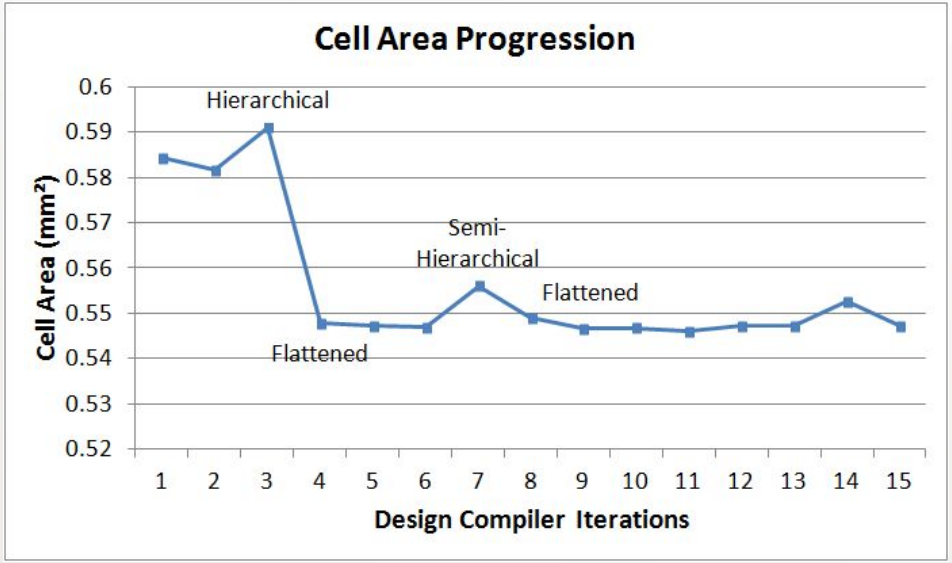
Targets	Low Power
Cycle Time (ns)	8
Total Power (mW)	15
Die Area (mm^2)	0.7
Utilization (%)	85

Front End Design Flow

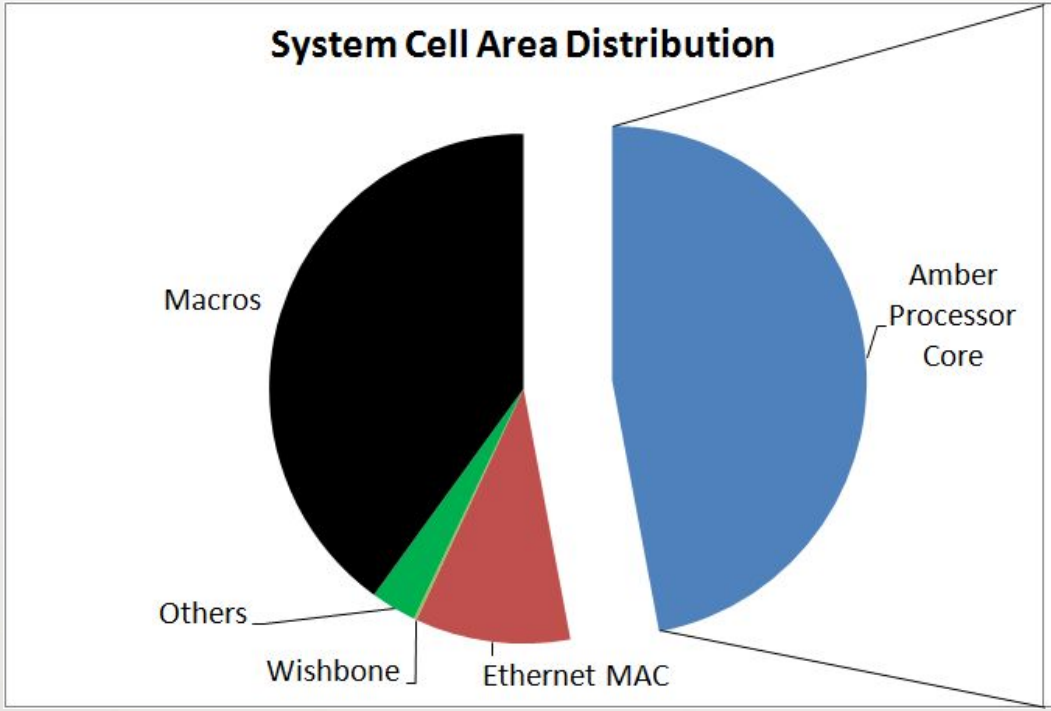


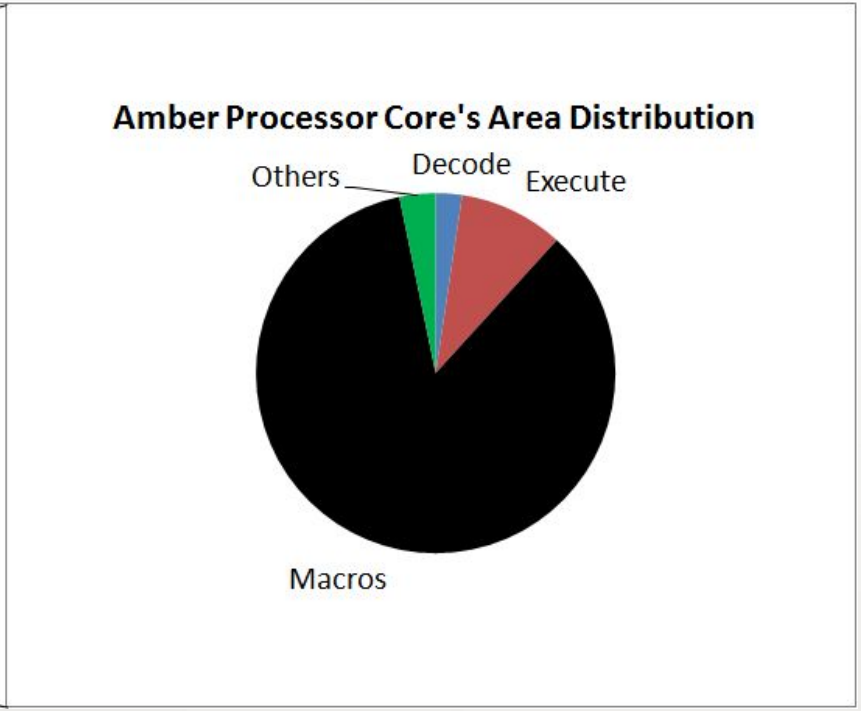
Synthesis Optimization

- Design Compiler
  - Started with 1ns clocks uncertainty (pessimistic). Now at 0.15ns
  - Slow corner (*ss0p95vn40c*) for synthesis
  - Flat netlist (improves timing & area)
  - Current Cell Area = 0.547 mm^2
- Formality
  - Modified provided scripts to match our design
  - Running concurrently throughout the design process



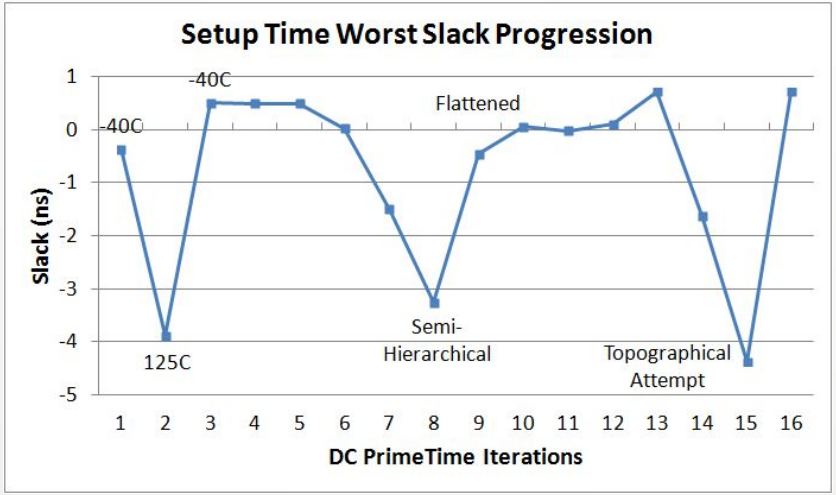
Area Distribution

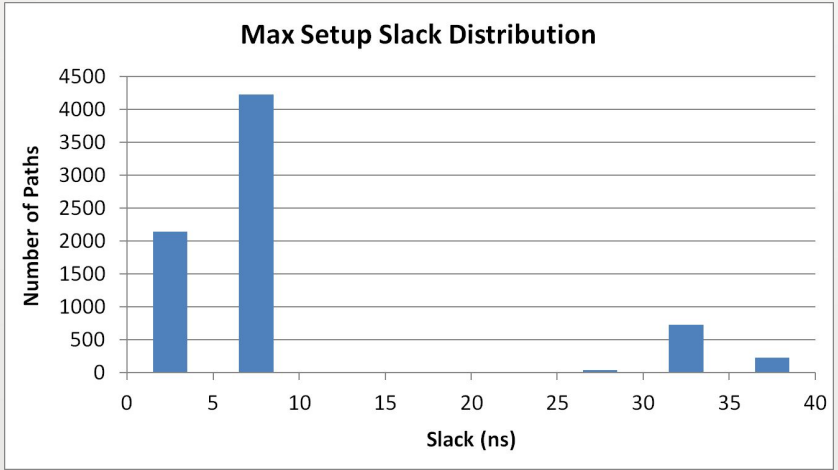




STA Effort

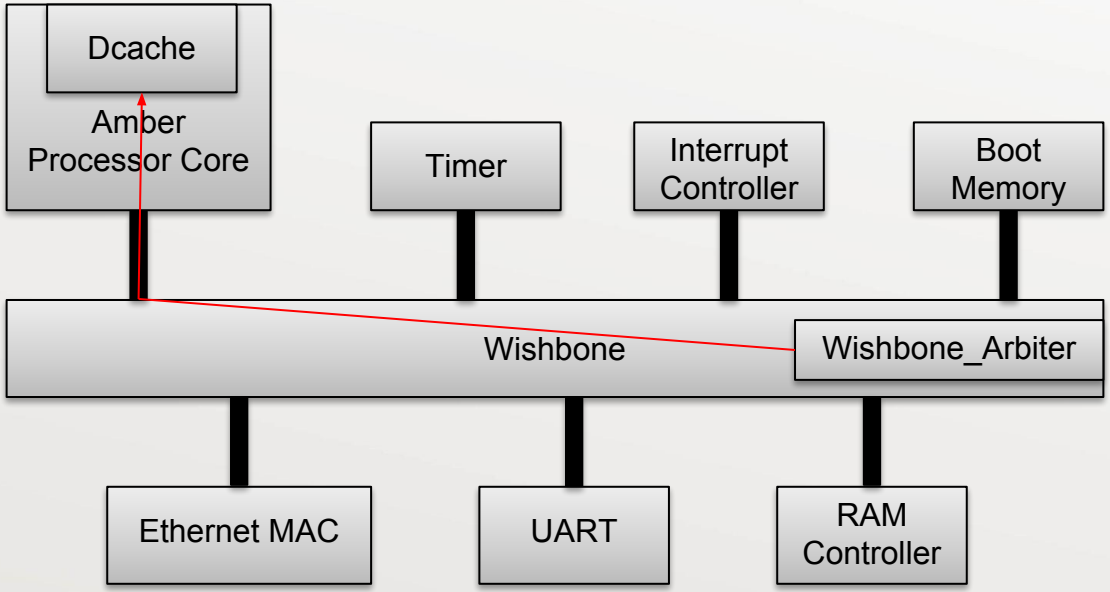
- Fixing setup time slack violations
  - Determine bottlenecks
  - Modify design accordingly
- Critical Paths for Setup-time
  - Wishbone arbiter to data cache
  - Min positive slack on sys_clk = 0.718 ns
- Critical Paths for Hold time
  - Analyzed post layout
- False Paths
  - Not necessary to address since timing is met





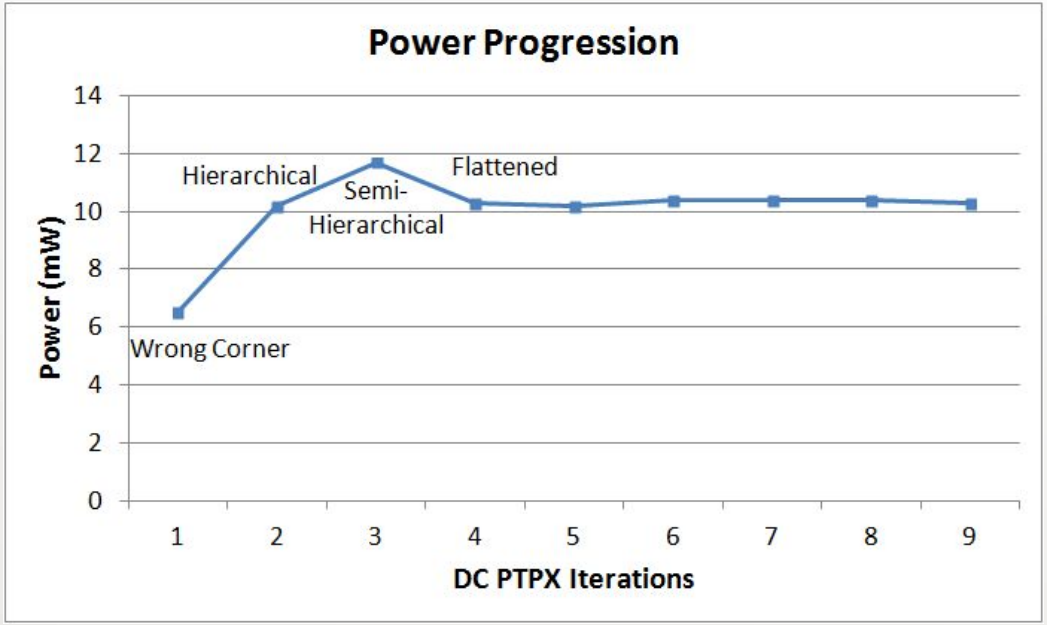
Critical Path Diagram

Critical Path: Wishbone arbiter to dcache

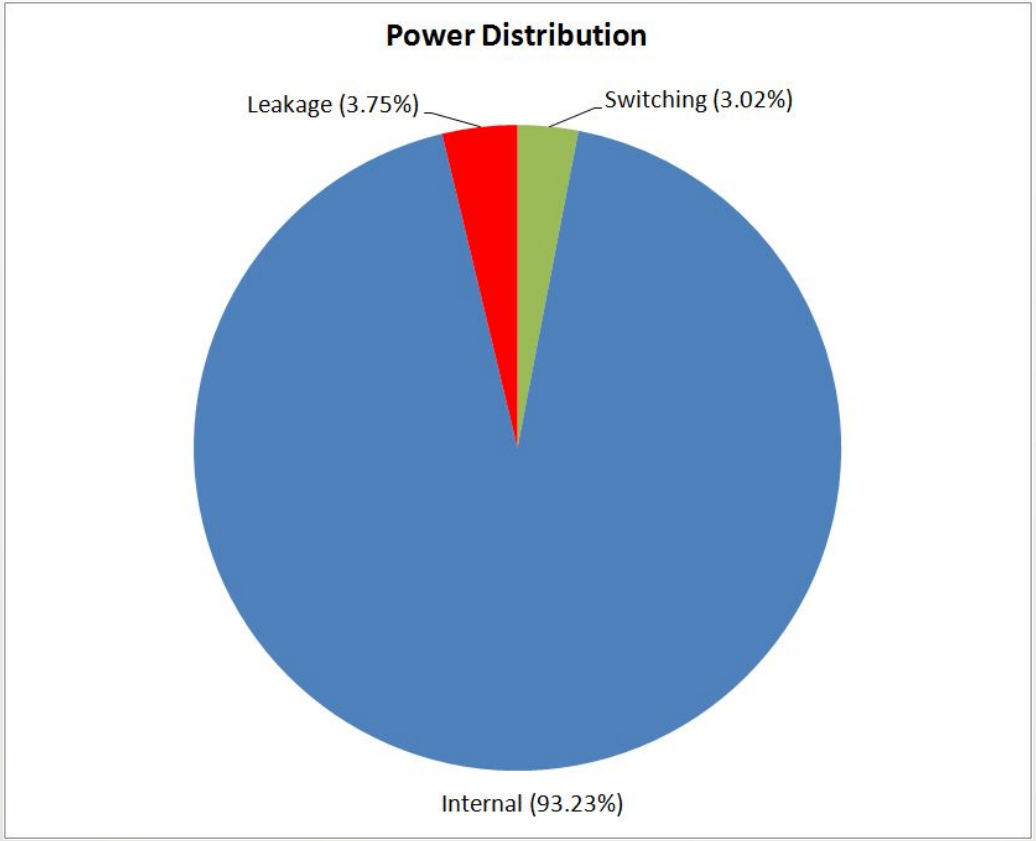


Power Analysis Effort

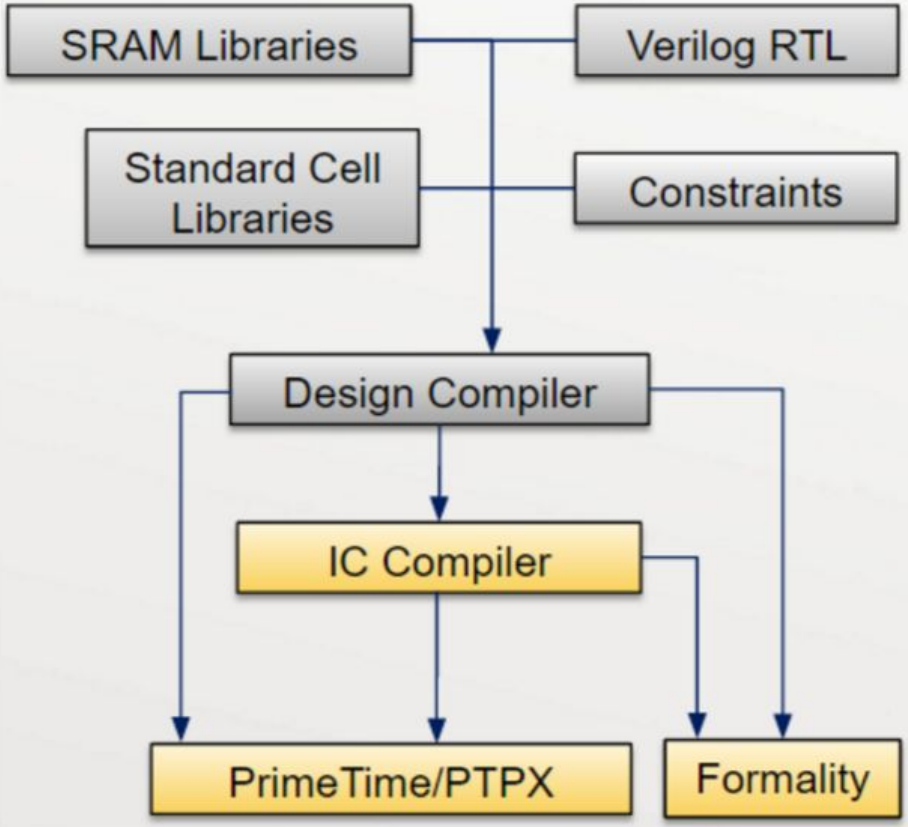
- Activity Factors set for flat netlist
  - Inputs set at 0.25
  - All modules at 0.25
  - Clocks set at 0.5
- Periods
  - Everything set to 32ns, except for amber core which uses 8ns
- Current power = 10.3 mW



Power Distribution

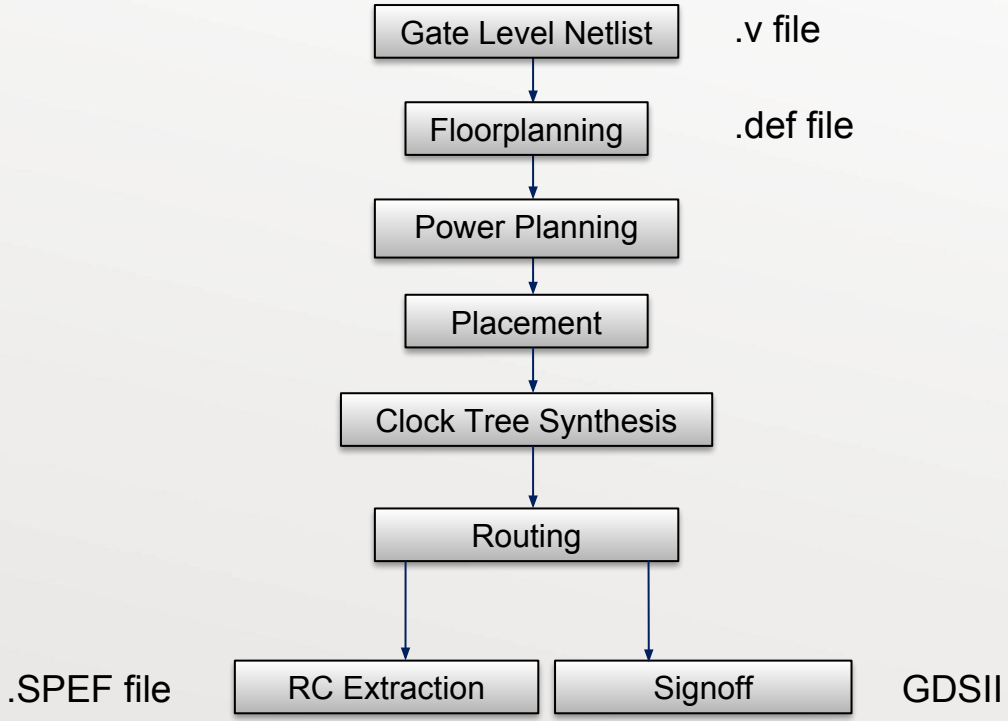


Back End Design Flow



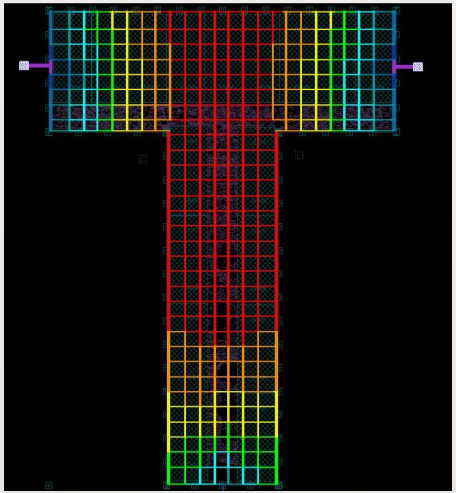
Physical Design Flow

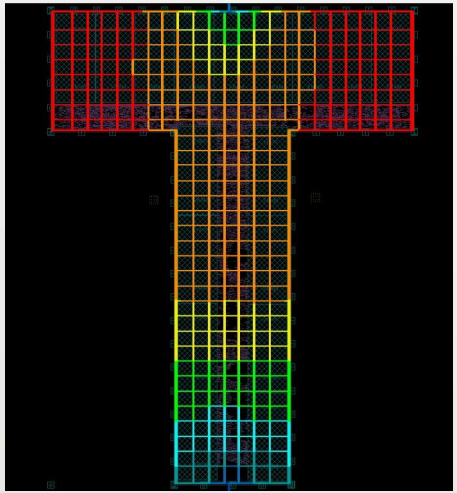
Tool Used: Synopsys ICC

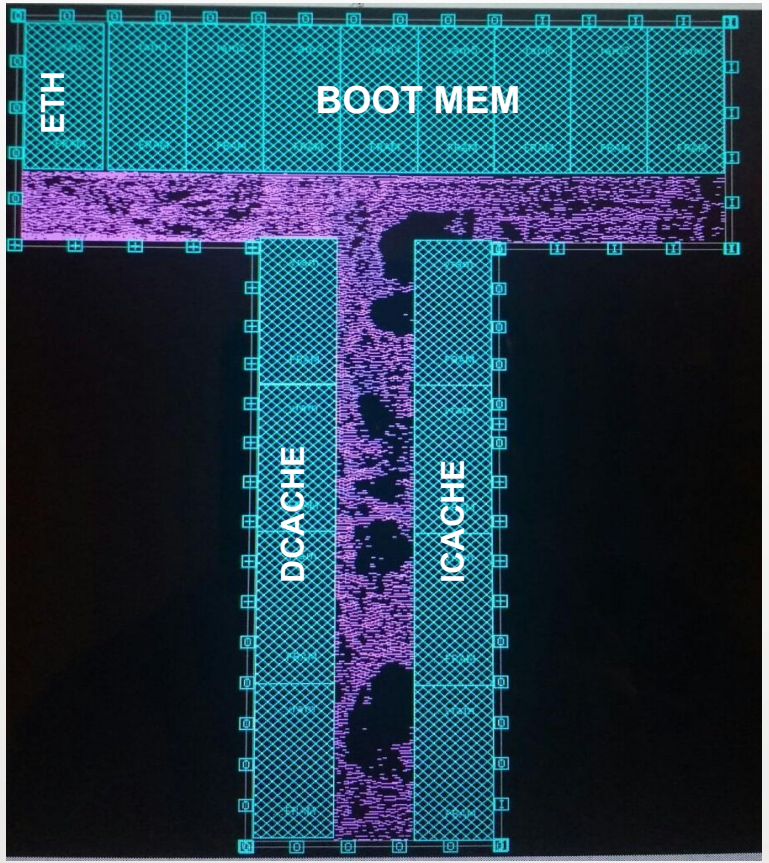


Initial Floorplan

- Allowable orientation: *N*
- Macro pin positions
- Rectilinear placement errors

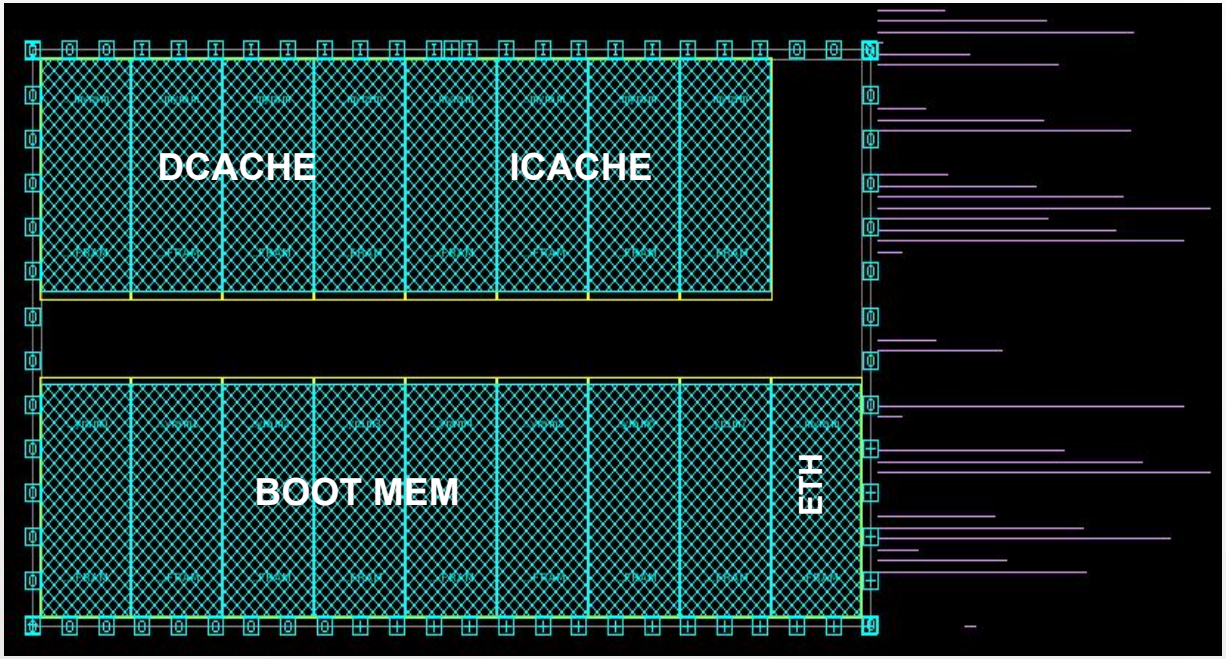






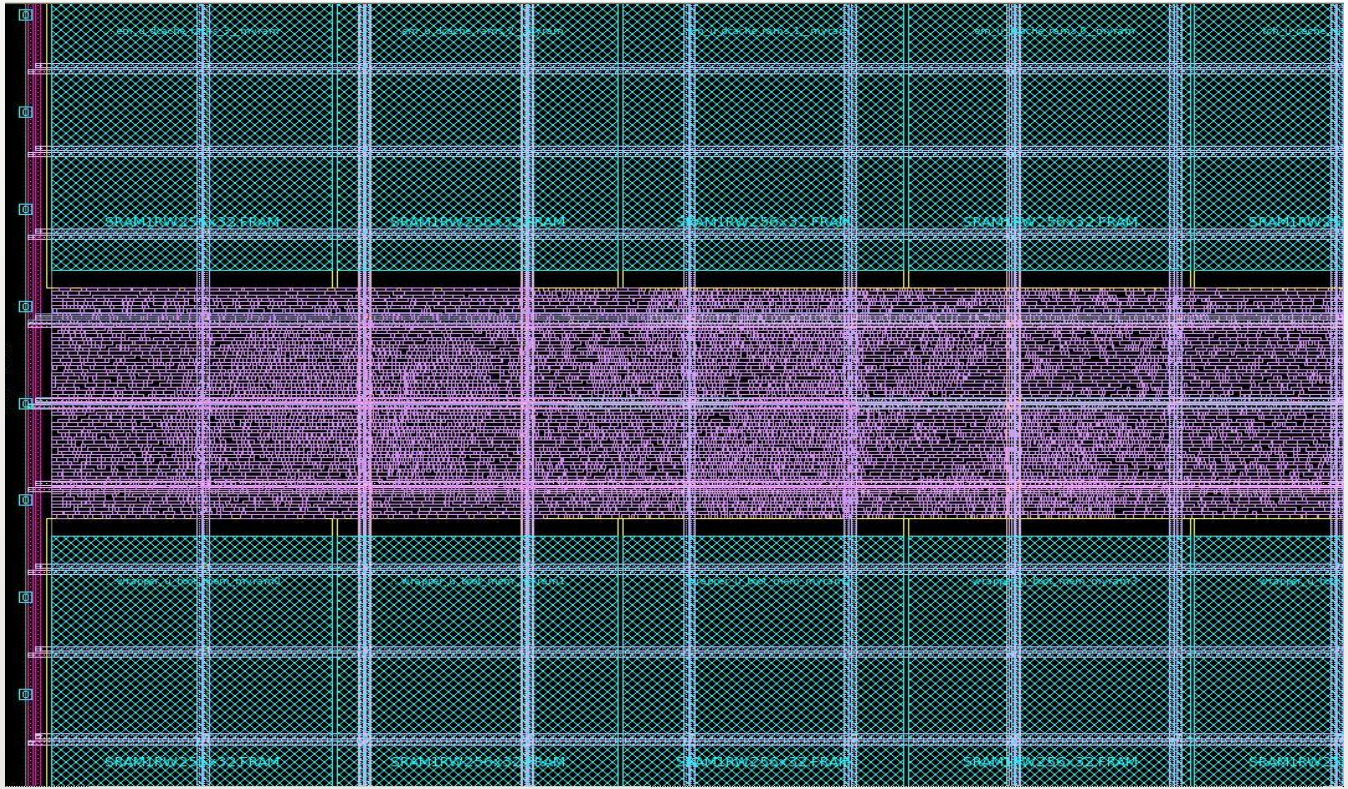
Current Floorplan

- Rectangular
- Memories on top/bottom
- Core width= 1009.629um
- Core height= 574.2936um
- Memory Orientation
- LVS Errors



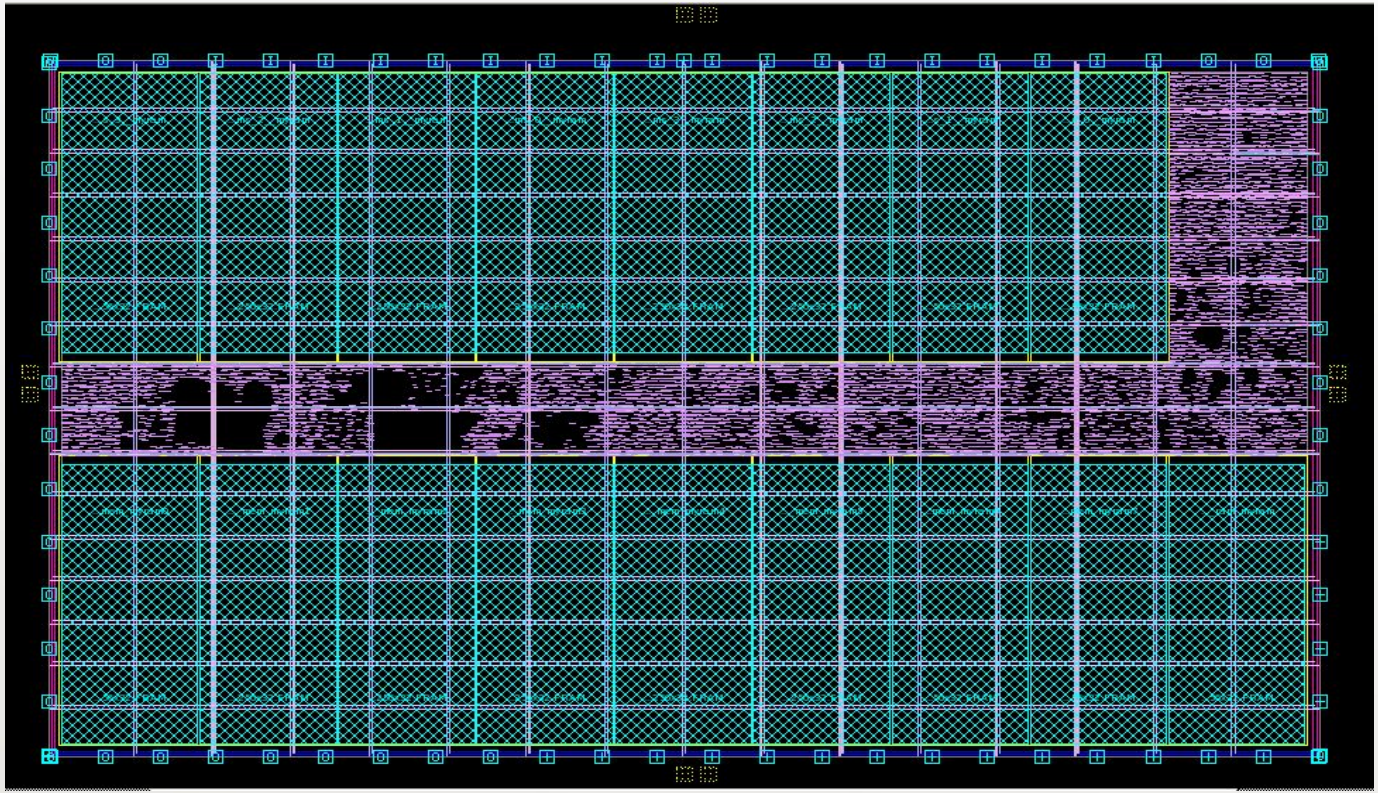
Halo

- Size proportional to number of pins
- Fixed LVS errors



Power Planning

- Ring & Straps
  - Width
  - Spacing
  - Offset
  - Metal Layers

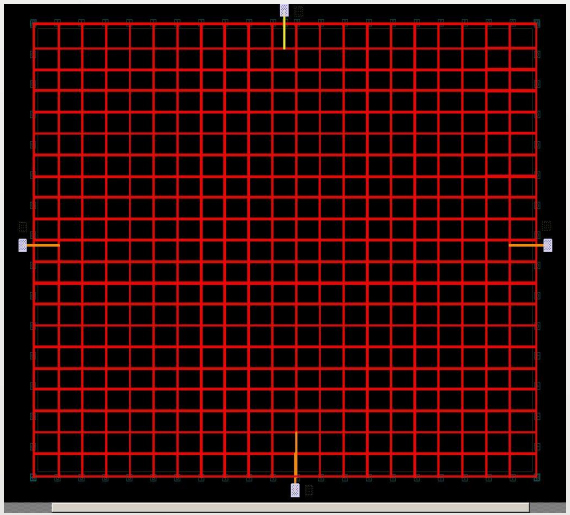


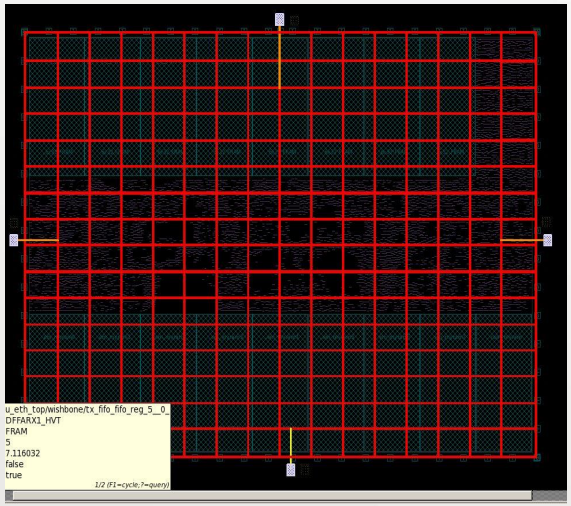
Power Grid: Flow and Tradeoffs

Tradeoffs

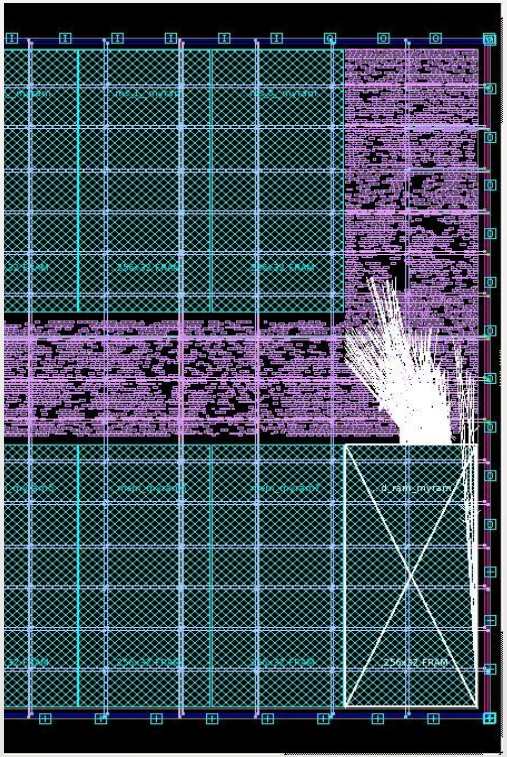
- IR Drop
- Routing blockage
- VIA Wall

Power Grids	Grid Size	Width	IR Drop	Avg Routing Blockage
PowerGrid 1	20x20	2um	38.6mV	3.45%
PowerGrid 2	15x15	2um	47.0mV	2.63%

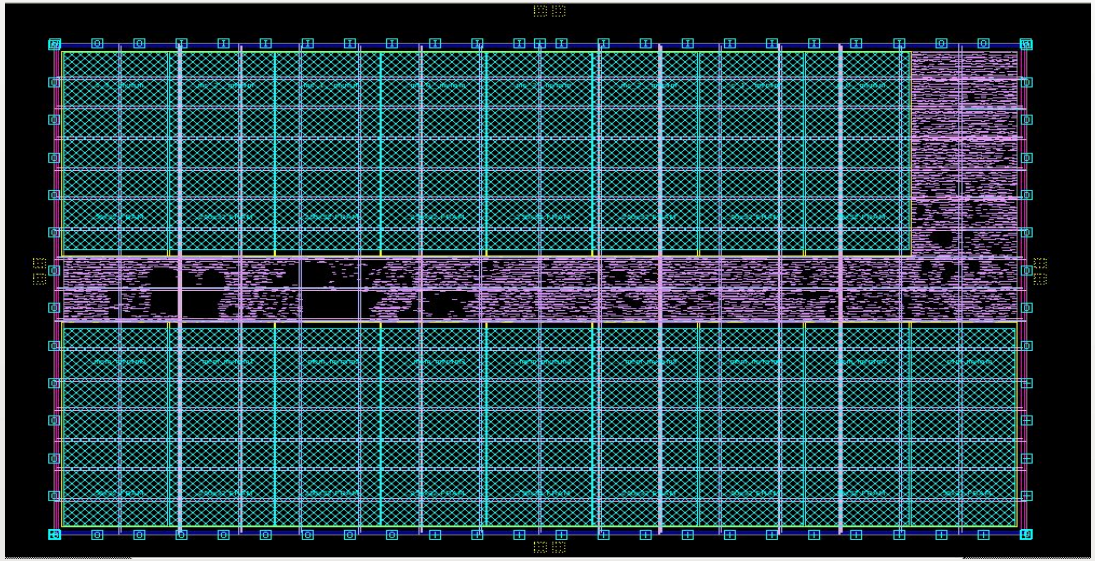




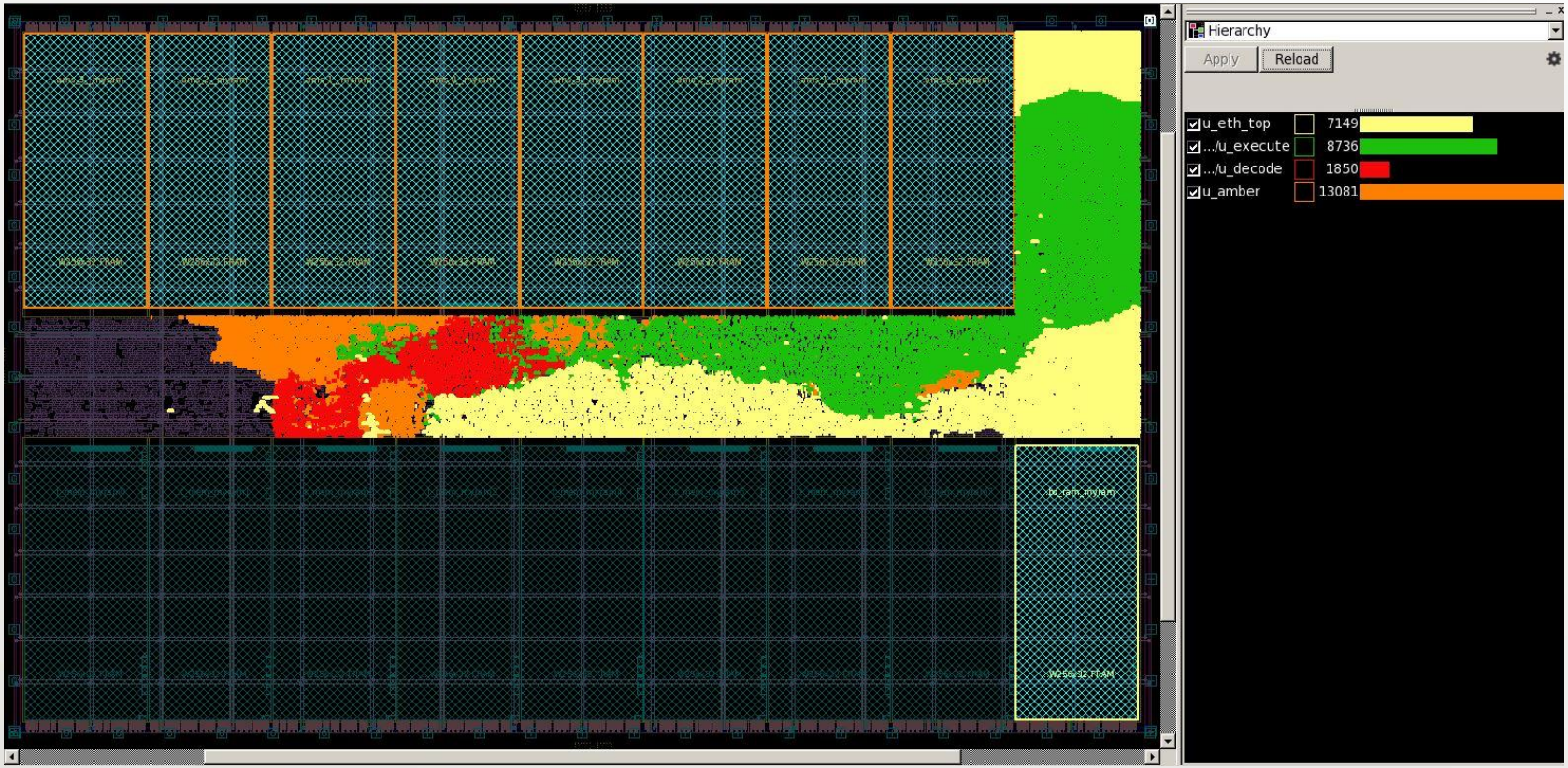
Placement



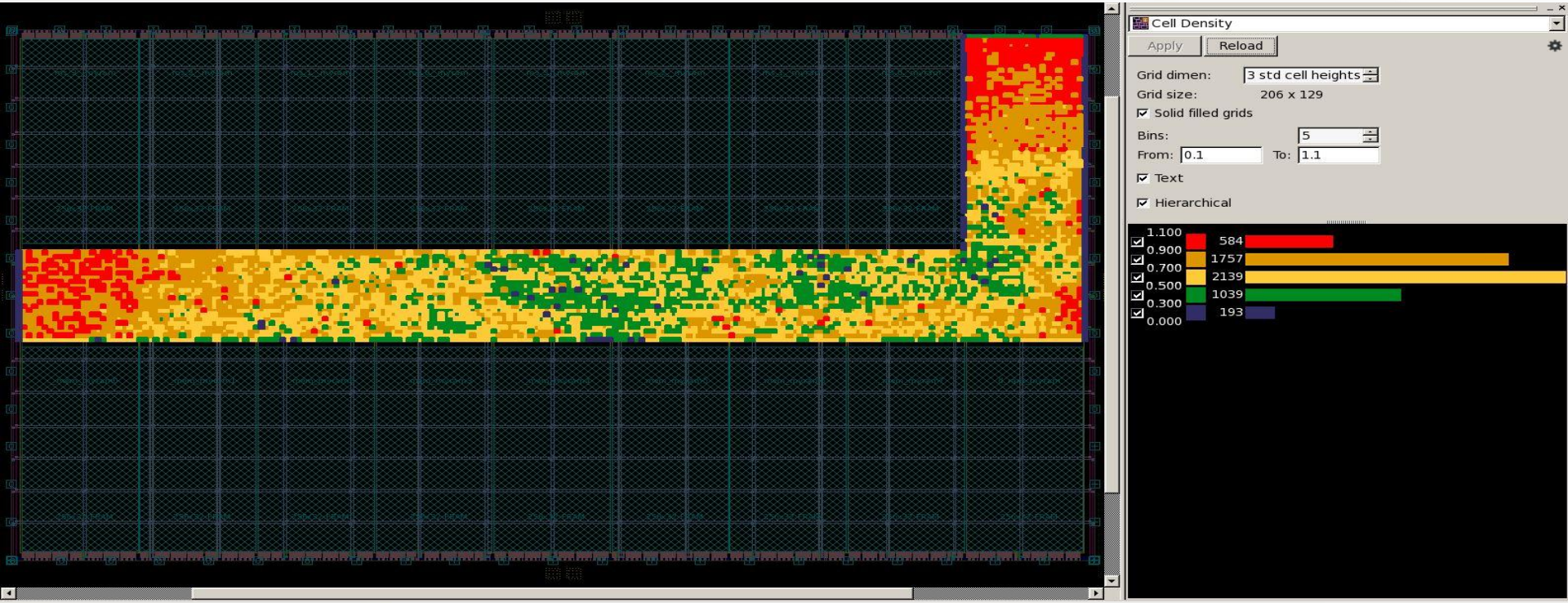
- Flylines used to determine location of macros and IO



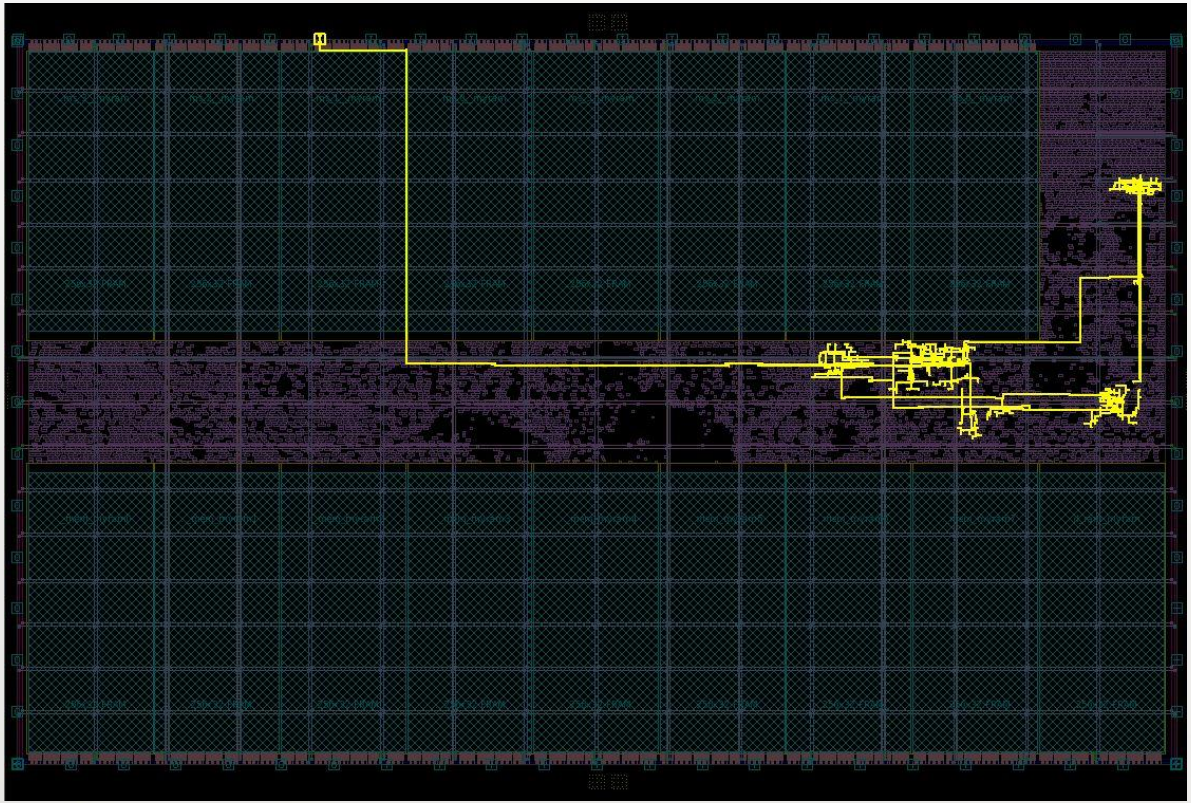
Placement - Hierarchy



Cell Density

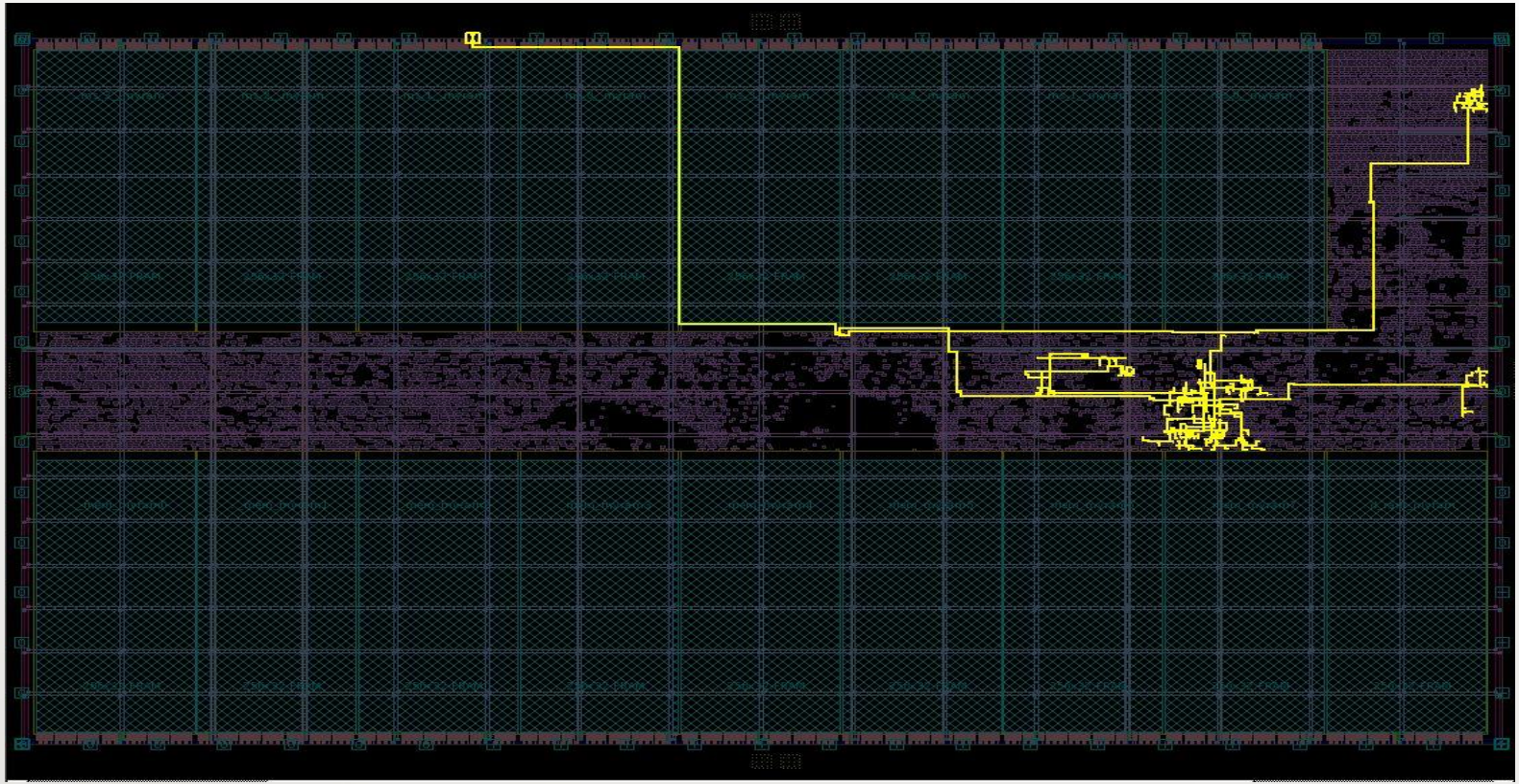


CTS - mrx_clk

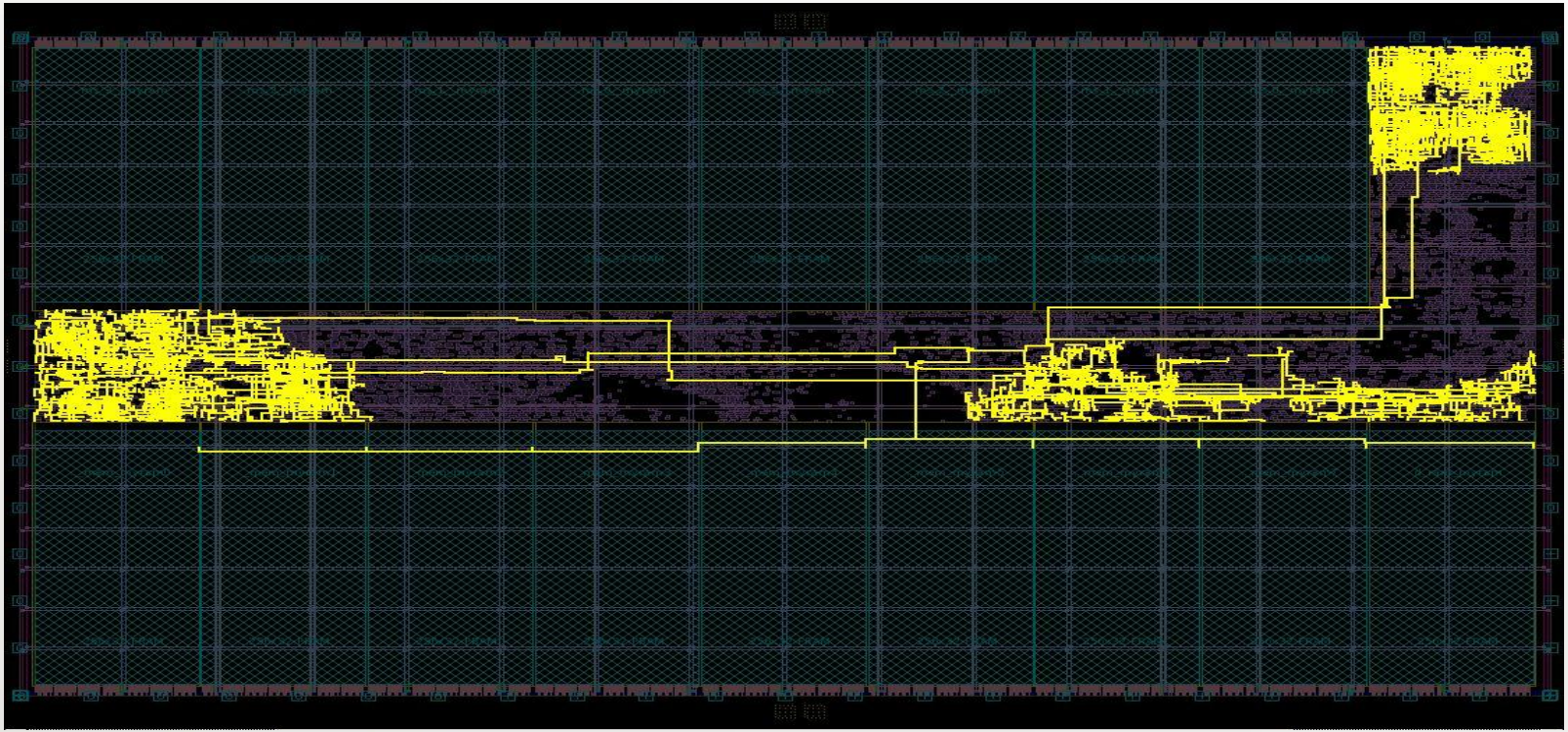


CTS - brd_clk_p

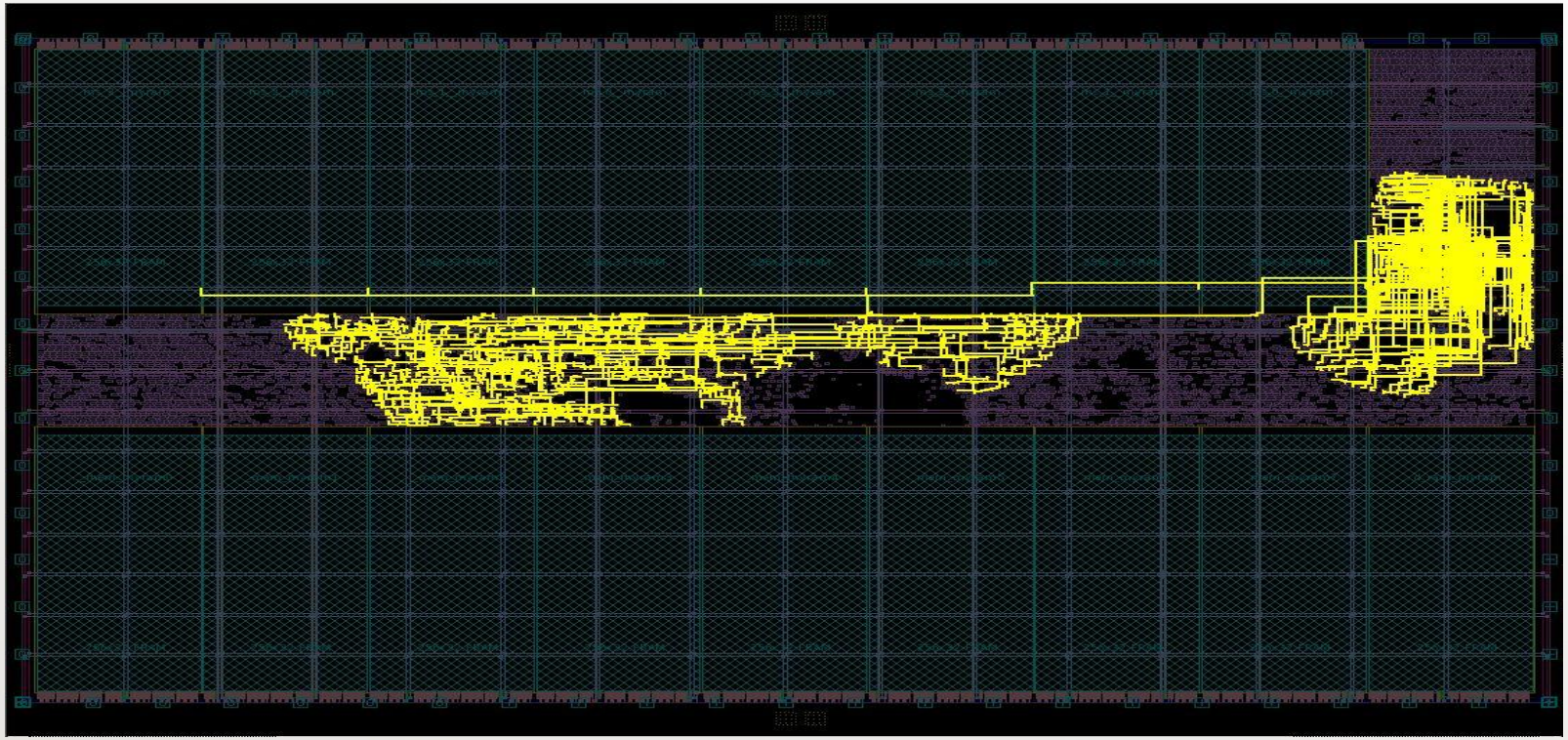
CTS - mtx_clk



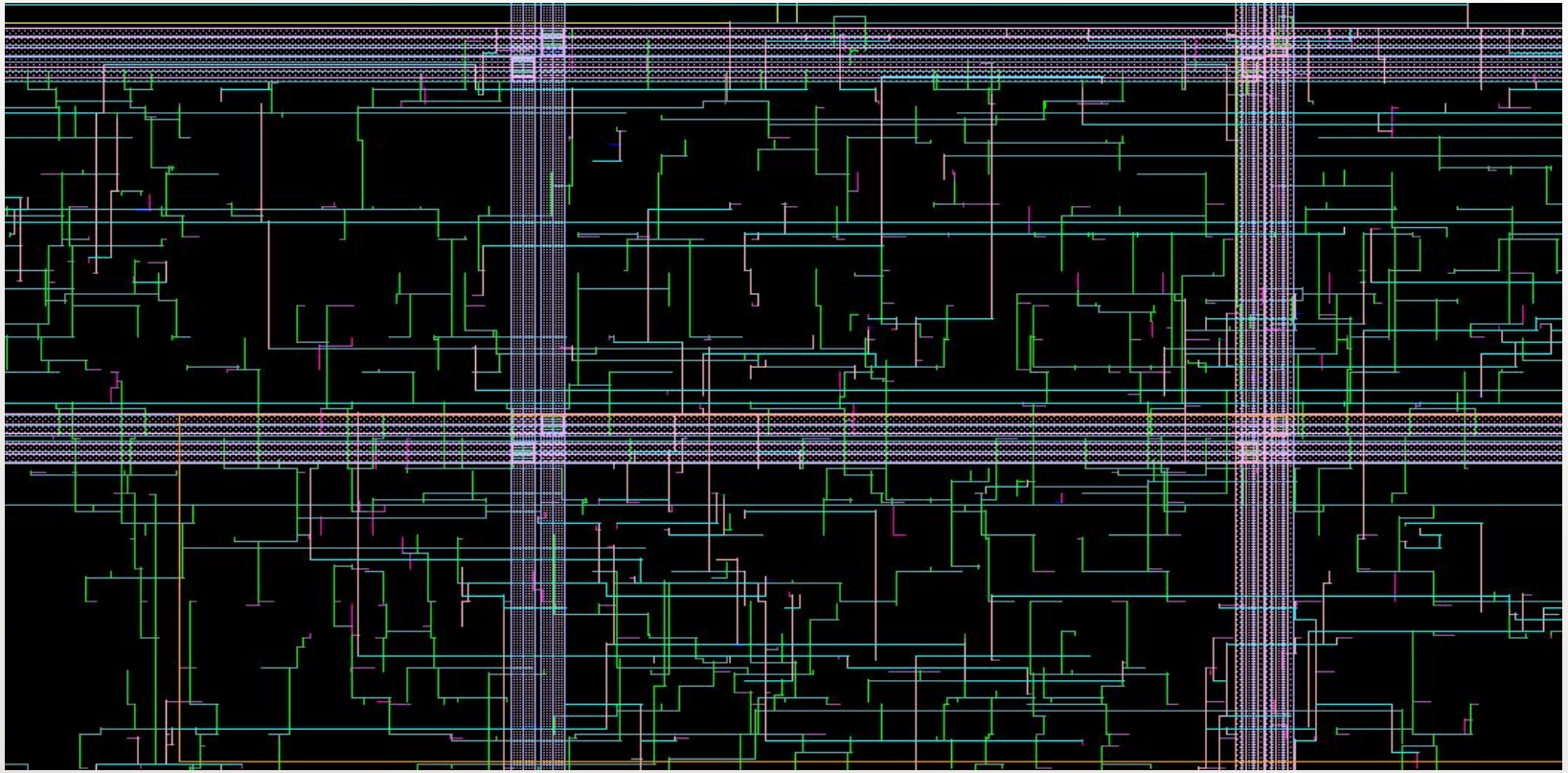
CTS - sys_clk_slow



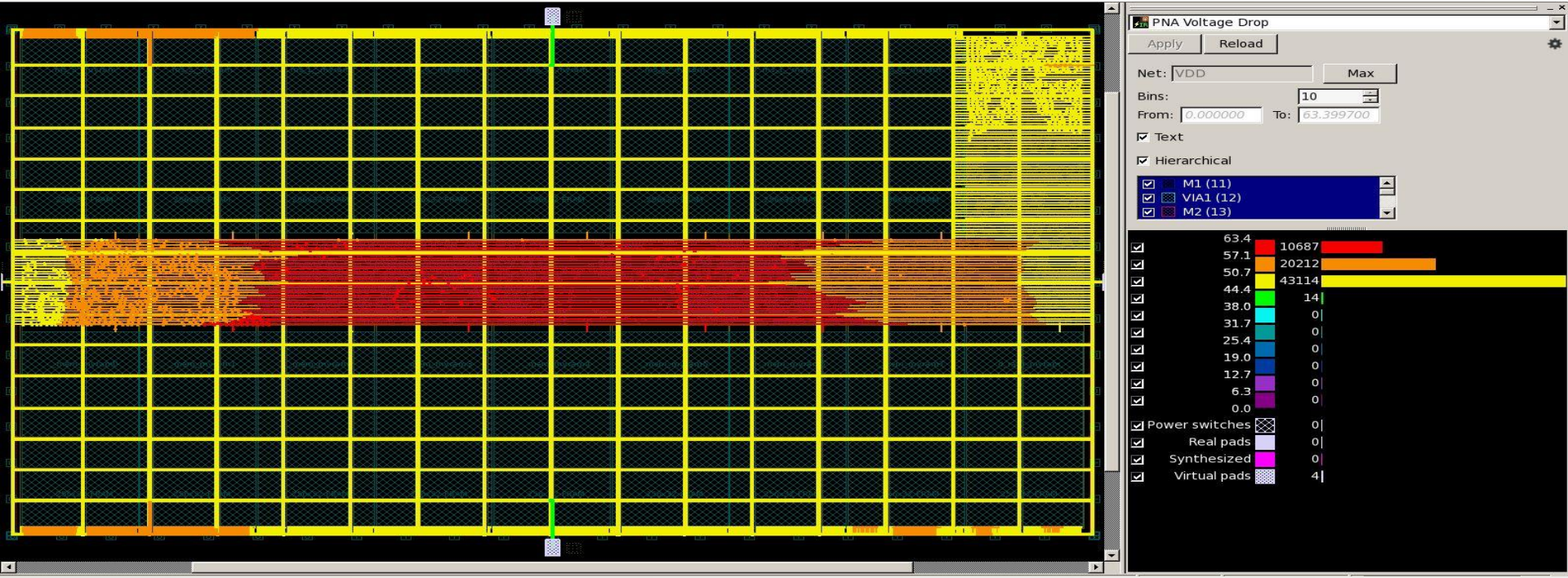
CTS - sys_clk



Routing



Power Analysis Post Routing



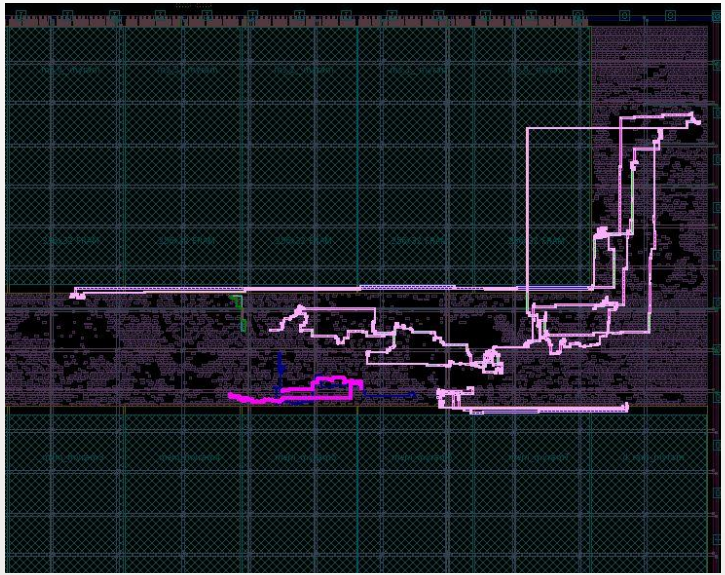
Physical Verification

- DRC Errors
- LVS Errors

LVS Errors	Our Results
Floating Port	20 (some flops with unconnected QN pins)
Open	2 (VSS n VDD due to no actual power pads)
Min Area	40 (DDR pins)

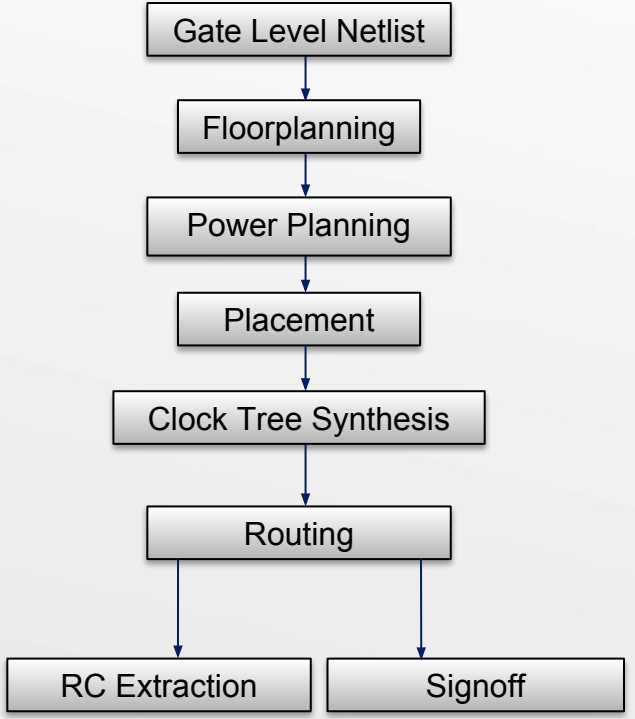
Place & Route Results

Parameter	Our Results
Setup (Worst Negative Slack)	0.02
Hold (Worst Negative Slack)	3.84
Die Area (mm^2)	0.663
Utilization (%)	69.24



Physical Design: Issues & Optimizations

- Floorplan Optimization techniques
  - Multiple Iterations
- Power planning
- Clock Tree Synthesis
- IO Placement
  - Driven by CTS and routing
- Cell Placement
- DRC and LVS
- Static Timing Analysis
  - Hold time fixing
- Power Estimation



Potential Risks

- Risks Associated with Design Completion in a Semester
  - Not enough time to meet all design specifications
  - Possibly misjudging the importance of warnings provided by tools
- Risks Mitigation Plan
  - Follow deadlines
  - Communication amongst team members
  - Check over work
  - Work in a organized fashion

Future Steps

- Front End
  - Continue topographical synthesis with design compiler
  - Further adjust constraints if necessary
- Back End
  - Try different floorplans
    - Increase utilization percentage
  - Improve IR drop
  - Improve I/O pin placement
  - Fix Hold time issues
  - Fix DRC/LVS

Summary

- Early Design Planning (EDP)
  - Low Power Design Specifications
- Front End Design
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  - Power Analysis Effort
- Back End Design
  - Physical Design Flow
- Potential Risks
- Future Steps

Parameter	Low Power Targets	Our Results
Cycle Time (ns)	8	8.02
Total Power (mW)	15	10.3
Die Area (mm^2)	0.7	0.663
Utilization (%)	85	69.24

Questions?