Digital Standard Cell Library

SAED_EDK32/28_CORE

DATABOOK

Document #: SAED_EDK32/28_CORE
Revision : 1.0.0
Technology : SAED32/28nm
Process : SAED32/28nm 1P9M 1.05v/1.8v/2.5v

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. Digital Standard Cell Library SAED_EDK32/28_CORE

1.1. Introduction

The SAED_EDK32/28_CORE Digital Standard Cell Library was built using SAED32/28nm 1P9M 1.05V/1.8V/2.5V design rules. The library was created aimed at optimizing the main characteristics of designed integrated circuits by its help.

The library includes typical miscellaneous combinational and sequential logic cells for different drive strengths.

Besides, the library contains all the cells which are required for different styles of low power (multi-voltage, multi-threshold, etc.) designs. Those are the following: Isolation Cells, Level Shifters, Retention Flip-Flops, Always-on Buffers and Power Gating Cells. In order to implement multi-threshold low power techniques High-Vt(HVT), Low-Vt(LVT) and Standart-Vt(SVT) versions of the Library was created.

The presence of all these cells provide the support of integrated circuits design with different core voltages to minimize dynamic and leakage power. Compiling the cell list has been based on the analysis of different educational designs.

1.2. General Information

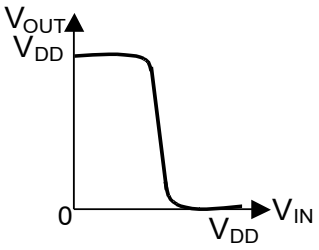
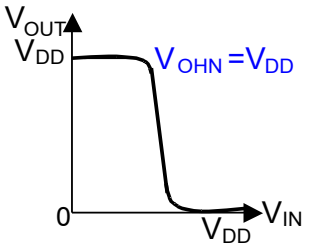
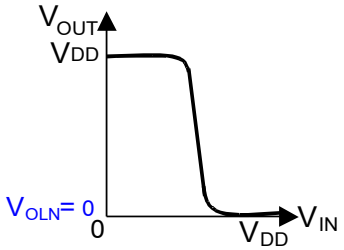
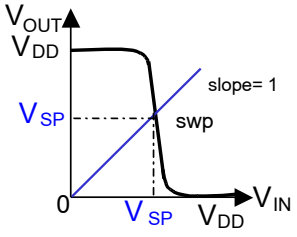
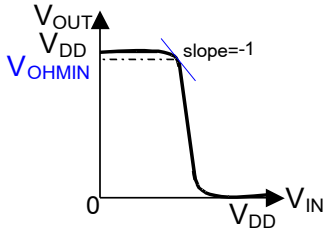
The used symbols of logic elements' states are shown in Table 1.1.

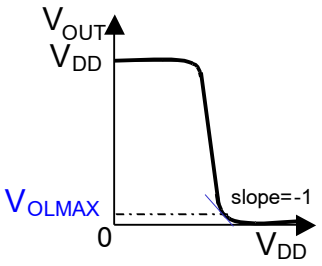
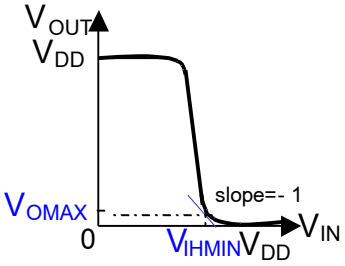
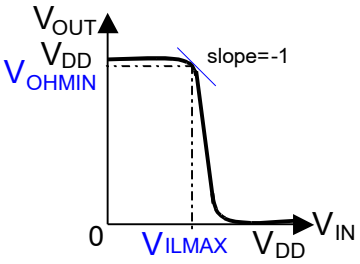
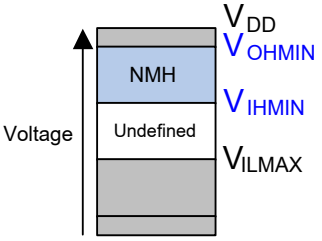
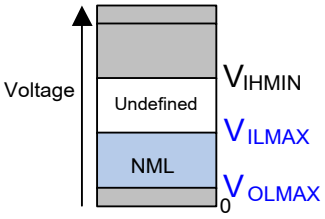
Table 1.1. Symbols of logic elements' states

Symbol	State
L ("0")	LOW Logic Level
H ("1")	HIGH Logic Level
Z	High-impedance State
LH ("0"→"1")	LOW to HIGH Transition
HL ("1"→"0")	HIGH to LOW Transition
X	Either HIGH or LOW Logic Level

DC parameters and measurement conditions of the elements included in SAED_EDK32/28_CORE Digital Standard Cell Library are shown in Table 1.2.

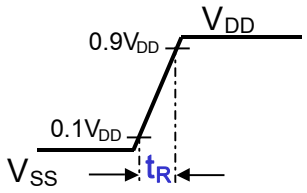
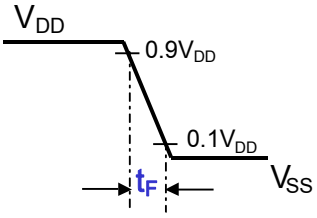
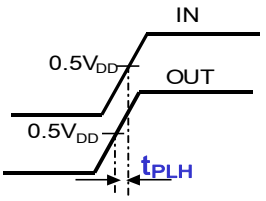
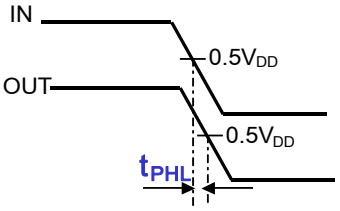
Table 1.2. DC Parameters and measurement conditions of digital cells

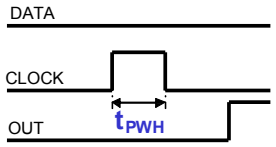
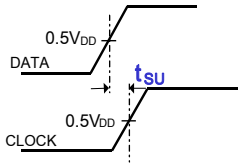
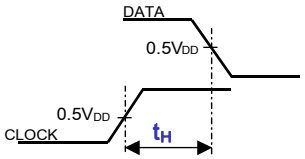
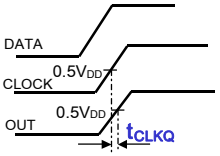
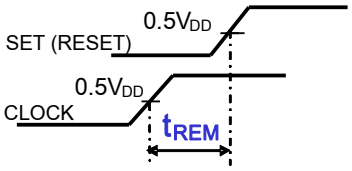
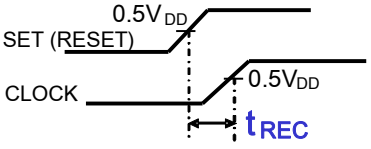
No	Parameter	Unit	Symbol	Figure	Definition
1	Voltage Transfer Characteristic	-	VTC		DC functional dependence between input and output voltages.
2	Output high level voltage (nominal)	V	$V_{OHN}=V_{DD}$		Output high voltage at nominal condition, usually equals to V_{DD}
3	Output low level voltage (nominal)	V	$V_{OLN}=0$ ($V_{OLN}=V_{SS}$)		Output low voltage at nominal condition, usually $V_{OLN}=0$
4	Switching point voltage	V	V_{SP}		Point on VTC where $V_{OUT}=V_{IN}$
5	Output high level minimum voltage	V	V_{OHMIN}		Highest output voltage at slope= -1.

No	Parameter	Unit	Symbol	Figure	Definition
6	Output low level maximum voltage	V	V_{OLMAX}		Lowest output voltage at slope= -1
7	Input minimum high voltage	V	V_{IHMIN}		Highest input voltage at slope = -1
8	Input maximum low voltage	V	V_{ILMAX}		Lowest input voltage at slope = -1
9	High state noise margin	V	NMH= =V_{OHMIN}- V_{IHMIN}		The maximum input noise voltage which does not change the output state when its value is subtracted from the input high level voltage
10	Low state noise margin	V	NML= =V_{ILMAX}- V_{OLMAX}		The maximum input noise voltage which does not change the output state when added to the input low level voltage
11	Static leakage current consumption at output on high state	uA	I_{LEAKH}	None	The current consumed when the output is high
		uA	I_{LEAKL}	None	The current consumed when the output is low
12	Leakage power consumption (dissipation) at output	pW	P_{LEAKH}= =V_{DD} x I_{LEAKH}	None	The power consumed when the output is high
		pW	P_{LEAKL}= =V_{DD} x I_{LEAKL}	None	The power consumed when the output is low

AC parameters and measurement conditions of the elements included in SAED_EDK32/28_CORE Digital Standard Cell Library are shown in Table 1.3.

Table 1.3. AC Parameters and measurement conditions of digital cells

No	Parameter	Unit	Symbol	Figure	Definition
1	Rise transition time	ns	t_R		The time it takes a driving pin to make a transition from kV_{DD} to $(1-k)V_{DD}$ value. Usually k=0.1 (also possible k=0.2, 0.3, etc)
2	Fall transition time	ns	t_F		The time it takes a driving pin to make a transition from $(1-k)V_{DD}$ to kV_{DD} value. Usually k=0.1 (also possible k=0.2, 0.3, etc)
3	Propagation delay low-to-high (Rise propagation)	ns	t_{PLH} (t_{PR})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DD}$ when the output signal is changing from low to high
4	Propagation delay high-to-low (Fall propagation)	ns	t_{PHL} (t_{PF})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DD}$ when the output signal is changing from high to low
5	Average supply current	uA	$I_{V_{DD}AVG} = \int_0^T I_{V_{DD}}(t)dt$	None	The power supply current average value for a period (T)
6	Supply peak current	uA	$I_{VDDPEAK}$= =max(I_{VDD}(t)) t∈[0;T]	None	The peak value of power supply current within one period (T)
7	Dynamic power dissipation	pW	P_{DISDYN}= =I_{VDDAVG} x V_{DD}	None	The average power consumed from the power supply
8	Power-delay product	nJ	PD=P_{DISDYN} x x max (t_{PHL},t_{PLH})	None	The product of consumed power and the largest propagation delay
9	Energy-delay product	nJs	ED=PD x x max(t_{PHL},t_{PLH})	None	The product of PD and the largest propagation delay
10	Switching fall power	nJ	P_{SWF} = =(C_{LOAD}+C_{OUTF}) x x V_{DD}^2/2	None	The energy dissipated on a fall transition. (C_{OUTF} is the output fall capacitance)

No	Parameter	Unit	Symbol	Figure	Definition
11	Switching rise power	nJ	P_{SWR}= =(C_{LOAD}+C_{OUTR}) x x V_{DD}^2/2	None	The energy dissipated on a rise transition. (C_{OUTR} is the output rise capacitance)
12	Minimum clock pulse (only for flip-flops or latches)	ns	t_{PWH} (t_{PWL})		The time interval during which the clock signal is high or low, so that it ensures proper operation of a flip-flop or a latch
13	Setup time (only for flip-flops or latches)	ns	t_{SU}		The minimum period in which the input data to a flip-flop or a latch must be stable before the active edge of the clock occurs
14	Hold time (only for flip-flops or latches)	ns	t_H		The minimum period in which the input data to a flip-flop or a latch must remain stable after the active edge of the clock has occurred
15	Clock-to-output time (only for flip-flops or latches)	ns	t_{CLKQ}		The amount of time that takes the output signal to change after clock's active edge is applied
16	Removal time (only for flip-flops or latches with asynchronous Set or Reset).	ns	t_{REM}		The minimum time in which the asynchronous Set or Reset pin to a flip-flop or latch must remain enabled after the active edge of the clock has occurred
17	Recovery time (only for flip-flops and latches with asynchronous Set or Reset)	ns	t_{REC}		The minimum time in which Set or Reset must be held stable after being deasserted before next active edge of the clock occurs
18	From high to Z-state entry time, (only for tri-state output cells)	ns	t_{HZ}	None	The amount of time that takes the output to change from high to Z-state after control signal is applied
19	From low to Z-state entry time, (only for tri-state output cells)	ns	t_{LZ}	None	The amount of time that takes the output to change from low to Z-state after control signal is applied

No	Parameter	Unit	Symbol	Figure	Definition
20	From Z to high-state exit time (only for tri-state output cells)	ns	t_{ZH}	None	The amount of time that takes the output to change from Z to high-state after control signal is applied
21	From Z to low-state exit time (only for tri-state output cells)	ns	t_{ZL}	None	The amount of time that takes the output to change from Z to low-state after control signal is applied
22	Input pin capacitance	pF	C_{IN}	None	Defines the load of an output pin
23	Maximum capacitance	pF	C_{MAX}	None	Defines the maximum total capacitive load that an output pin can drive

1.3. Operating conditions

SAED_EDK32/28_CORE Digital Standard Cell Library specification is given for 1.05V operation. The used process technology was SAED32/28nm 1P9M 1.05V/1.8V/2.5V, but only the 1P1M option was used.
The operating conditions of SAED_EDK32/28_CORE Digital Standard Cell Library are shown in Table 1.4.

Table 1.4. Operating conditions

Parameter	Min	Typ	Max	Units
Power Supply (VDD) range	0.945	1.05	1.061	V
Operating Temperature range	-40	+25	+125	°C
Operating Frequency (F)	-	300	-	MHz

1.4. Definition of input signal slope, standard load and drive strengths

Preliminary value for the slope of input signal edges were determined from the given operating frequency (F=300 MHz) using the following formula:

$$T_{isl} = \frac{1}{(10 \div 20) \cdot F}$$

The result thus obtained is preliminary and may be revised after specifying the inverter's sizes. Standard load (C_{sl}) was selected as the input pin capacitance of INVX1 cell. The INVX1 cell itself was tuned to drive 4 standard loads.

Table 1.5. Definition of drive strength

Drive Strength	Cell Load
X0	0.5x C_{sl}
X1	1x C_{sl}
X2	2x C_{sl}
X3	3x C_{sl}
X4	4x C_{sl}
X8	8x C_{sl}
X12	12x C_{sl}
X16	16x C_{sl}
X24	24x C_{sl}
X32	32x C_{sl}

1.5. AC Characteristics

1.5.1. Characterization corners

Composite Current Source (CCS) modeling technology was applied for characterization to meet the contemporary methods of low power design. The application of that technology supports timing, noise, and power analyses simultaneously with consideration of the relevant nanometer dependencies. It allows meeting the requirements of variation-aware analysis.
For characterization all 350 cells were split in four groups: high-low level shifters (ulvl), low-high level shifters (dlvl), power gating cells(pg), and all others.
All cells except level shfters were characterized in 27 process/voltage/temperature (PVT) conditions shown in Table 1.6 and 1.7, and Level Shifters were characterized for 45 corners shown in Table 1.6 and 1.7. The cells are grouped in different libraries.

Table 1.6. Base Characterization Corners

#	Corner Name/ Library Name Suffix	Process (NMOS proc. – PMOS proc.)	Power Supply (V)	Temperature (^{0}C)
	Typical Characterization Corners			
1.	tt1p05v25c	Typical - Typical	1.05	25
2.	tt1p05v125c	Typical - Typical	1.05	125
3.	tt1p05vn40c	Typical - Typical	1.05	-40
4.	ss0p95v25c	Slow - Slow	0.95	25
5.	ss0p95v125c	Slow - Slow	0.95	125
6.	ss0p95vn40c	Slow - Slow	0.95	-40
7.	ff1p16v25c	Fast - Fast	1.16	25
8.	ff1p16v125c	Fast - Fast	1.16	125
9.	ff1p16vn40c	Fast - Fast	1.16	-40
	Middle Voltage Operating Conditions			
10.	tt0p85v25c	Typical - Typical	0.85	25
11.	tt0p85v125c	Typical - Typical	0.85	125
12.	tt0p85vn40c	Typical - Typical	0.85	-40
13.	ss0p75v25c	Slow - Slow	0.75	25
14.	ss0p75v125c	Slow - Slow	0.75	125
15.	ss0p75vn40c	Slow - Slow	0.75	-40
16.	ff0p95v25c	Fast - Fast	0.95	25
17.	ff0p95v125c	Fast - Fast	0.95	125
18.	ff0p95vn40c	Fast - Fast	0.95	-40
	Low Voltage Operating Conditions			
19.	tt0p78v25c	Typical - Typical	0.78	25
20.	tt0p78v125c	Typical - Typical	0.78	125
21.	tt0p78vn40c	Typical - Typical	0.78	-40
22.	ss0p7v25c	Slow - Slow	0.7	25
23.	ss0p7v125c	Slow - Slow	0.7	125
24.	ss0p7vn40c	Slow - Slow	0.7	-40
25.	ff0p85v25c	Fast - Fast	0.85	25
26.	ff0p85v125c	Fast - Fast	0.85	125
27.	ff0p85vn40c	Fast - Fast	0.85	-40

Table 1.7. Power gating cell characterization corners

#	Corner Name/ Library Name Suffix	Process (NMOS proc. – PMOS proc.)	Power Supply (V)	Temperature (^{0}C)
	Typical Characterization Corners			
1.	pg_tt1p05v25c	Typical - Typical	1.05	25
2.	pg_tt1p05v125c	Typical - Typical	1.05	125
3.	pg_tt1p05vn40c	Typical - Typical	1.05	-40
4.	pg_ss0p95v25c	Slow - Slow	0.95	25
5.	pg_ss0p95v125c	Slow - Slow	0.95	125
6.	pg_ss0p95vn40c	Slow - Slow	0.95	-40
7.	pg_ff1p16v25c	Fast - Fast	1.16	25
8.	pg_ff1p16v125c	Fast - Fast	1.16	125
9.	pg_ff1p16vn40c	Fast - Fast	1.16	-40
	Middle Voltage Operating Conditions			
10.	pg_tt0p85v25c	Typical - Typical	0.85	25
11.	pg_tt0p85v125c	Typical - Typical	0.85	125
12.	pg_tt0p85vn40c	Typical - Typical	0.85	-40
13.	pg_ss0p75v25c	Slow - Slow	0.75	25
14.	pg_ss0p75v125c	Slow - Slow	0.75	125
15.	pg_ss0p75vn40c	Slow - Slow	0.75	-40
16.	pg_ff0p95v25c	Fast - Fast	0.95	25
17.	pg_ff0p95v125c	Fast - Fast	0.95	125
18.	pg_ff0p95vn40c	Fast - Fast	0.95	-40
	Low Voltage Operating Conditions			
19.	pg_tt0p78v25c	Typical - Typical	0.78	25
20.	pg_tt0p78v125c	Typical - Typical	0.78	125
21.	pg_tt0p78vn40c	Typical - Typical	0.78	-40
22.	pg_ss0p7v25c	Slow - Slow	0.7	25
23.	pg_ss0p7v125c	Slow - Slow	0.7	125
24.	pg_ss0p7vn40c	Slow - Slow	0.7	-40
25.	pg_ff0p85v25c	Fast - Fast	0.85	25
26.	pg_ff0p85v125c	Fast - Fast	0.85	125
27.	pg_ff0p85vn40c	Fast - Fast	0.85	-40

Table 1.8. Multi-VDD characterization corners for high-low level shifters

#	Corner Name/ Library Name Suffix	Process (NMOS proc. – PMOS proc.)	Power Supply1 (V)	Power Supply2 (V)	Temp. (^{0}C)
1.	dlvl_ff1p16v125c_i1p16v	Fast - Fast	1.16	1.16	125
2.	dlvl_ff0p85v125c_i1p16v	Fast - Fast	1.16	0.85	125
3.	dlvl_ff0p85v125c_i0p85v	Fast - Fast	0.85	0.85	125
4.	dlvl_ff1p16v25c_i1p16v	Fast - Fast	1.16	1.16	25
5.	dlvl_ff0p85v25c_i1p16v	Fast - Fast	1.16	0.85	25
6.	dlvl_ff0p85v25c_i0p85v	Fast - Fast	0.85	0.85	25
7.	dlvl_ff1p16vn40c_i1p16v	Fast - Fast	1.16	1.16	-40
8.	dlvl_ff0p85vn40c_i1p16v	Fast - Fast	1.16	0.85	-40
9.	dlvl_ff0p85vn40c_i0p85v	Fast - Fast	0.85	0.85	-40
10.	dlvl_tt1p05v125c_i1p05v	Typical - Typical	1.05	1.05	125
11.	dlvl_tt0p78v125c_i1p05v	Typical - Typical	1.05	0.78	125
12.	dlvl_tt0p78v125c_i0p78v	Typical - Typical	0.78	0.78	125
13.	dlvl_tt1p05v25c_i1p05v	Typical - Typical	1.05	1.05	25
14.	dlvl_tt0p78v25c_i1p05v	Typical - Typical	1.05	0.78	25
15.	dlvl_tt0p78v25c_i0p78v	Typical - Typical	0.78	0.78	25
16.	dlvl_tt1p05vn40c_i1p05v	Typical - Typical	1.05	1.05	-40
17.	dlvl_tt0p78vn40c_i1p05v	Typical - Typical	1.05	0.78	-40
18.	dlvl_tt0p78vn40c_i0p78v	Typical - Typical	0.78	0.78	-40
19.	dlvl_ss0p95v125c_i0p95v	Slow - Slow	0.95	0.95	125
20.	dlvl_ss0p95v125c_i0p7v	Slow - Slow	0.95	0.7	125
21.	dlvl_ss0p7v125c_i0p7v	Slow - Slow	0.7	0.7	125
22.	dlvl_ss0p95v25c_i0p95v	Slow - Slow	0.95	0.95	25
23.	dlvl_ss0p7v25c_i0p95v	Slow - Slow	0.95	0.7	25
24.	dlvl_ss0p7v25c_i0p7v	Slow - Slow	0.7	0.7	25
25.	dlvl_ss0p95vn40c_i0p95v	Slow - Slow	0.95	0.95	-40
26.	dlvl_ss0p75vn40c_i0p95v	Slow - Slow	0.95	0.75	-40
27.	dlvl_ss0p75vn40c_i0p95v	Slow - Slow	0.75	0.75	-40
28.	dlvl_ff0p95v125c_i1p16v	Fast - Fast	1.16	0.95	125
29.	dlvl_ff0p95v125c_i0p95v	Fast - Fast	0.95	0.95	125
30.	dlvl_ff0p95v25c_i1p16v	Fast - Fast	1.16	0.95	25
31.	dlvl_ff0p95v25c_i0p95v	Fast - Fast	0.95	0.95	25
32.	dlvl_ff0p95vn40c_i1p16v	Fast - Fast	1.16	0.95	-40
33.	dlvl_ff0p95vn40c_i0p95v	Fast - Fast	0.95	0.95	-40
34.	dlvl_ff0p85v125c_i1p05v	Typical - Typical	1.05	0.85	125
35.	dlvl_ff0p85v125c_i0p85v	Typical - Typical	0.85	0.85	125
36.	dlvl_ff0p85v25c_i1p05v	Typical - Typical	1.05	0.85	25
37.	dlvl_ff0p85v25c_i0p85v	Typical - Typical	0.85	0.85	25
38.	dlvl_ff0p85vn40c_i1p05v	Typical - Typical	1.05	0.85	-40
39.	dlvl_ff0p85vn40c_i1p85v	Typical - Typical	0.85	0.85	-40
40.	dlvl_ff0p75v125c_i0p95v	Slow - Slow	0.95	0.75	125
41.	dlvl_ff0p75v125c_i0p75v	Slow - Slow	0.75	0.75	125
42.	dlvl_ff0p75v25c_i0p95v	Slow - Slow	0.95	0.75	25
43.	dlvl_ff0p75v25c_i0p75v	Slow - Slow	0.75	0.75	25
44.	dlvl_ff0p75vn40c_i0p95v	Slow - Slow	0.95	0.75	-40
45.	dlvl_ff0p75vn40c_i0p75v	Slow - Slow	0.75	0.75	-40

Table 1.9. Multi-VDD characterization corners for low-high level shifters

#	Corner Name/ Library Name Suffix	Process (NMOS proc. – PMOS proc.)	Power Supply1 (V)	Power Supply2 (V)	Temp. (^{0}C)
1.	ulvl_ff0p85v125c_i0p85v	Fast-Fast	0.85	0.85	125
2.	ulvl_ff0p85v25c_i0p85v	Fast-Fast	0.85	0.85	25
3.	ulvl_ff0p85vn40c_i0p85v	Fast-Fast	0.85	0.85	-40
4.	ulvl_ff0p85v125c_i0p95v	Fast-Fast	0.85	0.95	125
5.	ulvl_ff0p85v25c_i0p95v	Fast-Fast	0.85	0.95	25
6.	ulvl_ff0p85vn40c_i0p95v	Fast-Fast	0.85	0.95	-40
7.	ulvl_ff1p16v125c_i0p85v	Fast-Fast	1.16	0.85	125
8.	ulvl_ff1p16v125c_i0p95v	Fast-Fast	1.16	0.95	125
9.	ulvl_ff1p16v125c_i1p16v	Fast-Fast	1.16	1.16	125
10.	ulvl_ff1p16v25c_i0p85v	Fast-Fast	1.16	0.85	25
11.	ulvl_ff1p16v25c_i0p95v	Fast-Fast	1.16	0.95	25
12.	ulvl_ff1p16v25c_i1p16v	Fast-Fast	1.16	1.16	25
13.	ulvl_ff1p16vn40c_i0p85v	Fast-Fast	1.16	0.85	-40
14.	ulvl_ff1p16vn40c_i0p95v	Fast-Fast	1.16	0.95	-40
15.	ulvl_ff1p16vn40c_i1p16v	Fast-Fast	1.16	1.16	-40
16.	ulvl_ss0p75v125c_i0p75v	Slow-Slow	0.75	0.75	125
17.	ulvl_ss0p75v25c_i0p75v	Slow-Slow	0.75	0.75	25
18.	ulvl_ss0p75vn40c_i0p75v	Slow-Slow	0.75	0.75	-40
19.	ulvl_ss0p7v125c_i0p7v	Slow-Slow	0.7	0.7	125
20.	ulvl_ss0p7v25c_i0p7v	Slow-Slow	0.7	0.7	25
21.	ulvl_ss0p7vn40c_i0p7v	Slow-Slow	0.7	0.7	-40
22.	ulvl_ss0p95v125c_i0p75v	Slow-Slow	0.95	0.75	125
23.	ulvl_ss0p95v125c_i0p7v	Slow-Slow	0.95	0.7	125
24.	ulvl_ss0p95v125c_i0p95v	Slow-Slow	0.95	0.95	125
25.	ulvl_ss0p95v25c_i0p75v	Slow-Slow	0.95	0.75	25
26.	ulvl_ss0p95v25c_i0p7v	Slow-Slow	0.95	0.7	25
27.	ulvl_ss0p95v25c_i0p95v	Slow-Slow	0.95	0.95	25
28.	ulvl_ss0p95vn40c_i0p75v	Slow-Slow	0.95	0.75	-40
29.	ulvl_ss0p95vn40c_i0p7v	Slow-Slow	0.95	0.7	-40
30.	ulvl_ss0p95vn40c_i0p95v	Slow-Slow	0.95	0.95	-40
31.	ulvl_tt0p78v125c_i0p78v	Typical-Typical	0.78	0.78	125
32.	ulvl_tt0p78v25c_i0p78v	Typical-Typical	0.78	0.78	25
33.	ulvl_tt0p78vn40c_i0p78v	Typical-Typical	0.78	0.78	-40
34.	ulvl_tt0p85v125c_i0p85v	Typical-Typical	0.85	0.85	125
35.	ulvl_tt0p85v25c_i0p85v	Typical-Typical	0.85	0.85	25
36.	ulvl_tt0p85vn40c_i0p85v	Typical-Typical	0.85	0.85	-40
37.	ulvl_tt1p05v125c_i0p78v	Typical-Typical	1.05	0.78	125
38.	ulvl_tt1p05v125c_i0p85v	Typical-Typical	1.05	0.85	125
39.	ulvl_tt1p05v125c_i1p05v	Typical-Typical	1.05	1.05	125
40.	ulvl_tt1p05v25c_i0p78v	Typical-Typical	1.05	0.78	25
41.	ulvl_tt1p05v25c_i0p85v	Typical-Typical	1.05	0.85	25
42.	ulvl_tt1p05v25c_i1p05v	Typical-Typical	1.05	1.05	25
43.	ulvl_tt1p05vn40c_i0p78v	Typical-Typical	1.05	0.78	-40
44.	ulvl_tt1p05vn40c_i0p85v	Typical-Typical	1.05	0.85	-40
45.	ulvl_tt1p05vn40c_i1p05v	Typical-Typical	1.05	1.05	-40

1.5.2. The values of Output Load and Input Slope

Characterization should be realized for 7 different values of Output Load and 7 different values of Input Slope shown in Table 1.10.

Table 1.10. The values to be used for characterization

Parameter	Value						
Output Load	0	$0.5*C_{sl}$	$1*C_{sl}$	$2*C_{sl}$	$4*C_{sl}$	$8*C_{sl}$	$16*C_{sl}$
Input Slope (ns)	$0.2*T_{isl}$	$0.4*T_{isl}$	$0.8*T_{isl}$	$1.6*T_{isl}$	$3.2*T_{isl}$	$6.4*T_{isl}$	$12.8*T_{isl}$

The calculation of Setup/Hold times should be realized for 3 different values of Data and Input Slopes shown in Table 1.11.

Table 1.11. The used values for calculating Setup/Hold Times

Parameter	Slope Values (ns)		
Data Input Slope	$0.5*T_{isl}$	$1*T_{isl}$	$5*T_{isl}$
Clock Input Slope	$0.5*T_{isl}$	$1*T_{isl}$	$5*T_{isl}$

2. Digital Standard Library Cells List

SAED_EDK32/28_CORE Digital Standard Cell Library contains 350 cells in total, the list of which is shown in Table 1.12.

Table 2.1. Digital Standard Library Cells List

No	Cell Description	Cell Name
	Inverters, Buffers	
1	Inverter	INVX0
2	Inverter	INVX1
3	Inverter	INVX2
4	Inverter	INVX4
5	Inverter	INVX8
6	Inverter	INVX16
7	Inverter	INVX32
8	Inverting Buffer	IBUFFX2
9	Inverting Buffer	IBUFFX4
10	Inverting Buffer	IBUFFX8
11	Inverting Buffer	IBUFFX16
12	Inverting Buffer	IBUFFX32
13	Non-inverting Buffer	NBUFFX2
14	Non-inverting Buffer	NBUFFX4
15	Non-inverting Buffer	NBUFFX8
16	Non-inverting Buffer	NBUFFX16
17	Non-inverting Buffer	NBUFFX32
18	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX1
19	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX2
20	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX4
21	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX8
22	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX16
23	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX32
	Logic Gates	
24	AND 2-input	AND2X1
25	AND 2-input	AND2X2
26	AND 2-input	AND2X4
27	AND 3-input	AND3X1
28	AND 3-input	AND3X2
29	AND 3-input	AND3X4
30	AND 4-input	AND4X1
31	AND 4-input	AND4X2
32	AND 4-input	AND4X4
33	NAND 2-input	NAND2X0
34	NAND 2-input	NAND2X1
35	NAND 2-input	NAND2X2
36	NAND 2-input	NAND2X4

No	Cell Description	Cell Name
37	NAND 3-input	NAND3X0
38	NAND 3-input	NAND3X1
39	NAND 3-input	NAND3X2
40	NAND 3-input	NAND3X4
41	NAND 4-input	NAND4X0
42	NAND 4-input	NAND4X1
43	OR 2-input	OR2X1
44	OR 2-input	OR2X2
45	OR 2-input	OR2X4
46	OR 3-input	OR3X1
47	OR 3-input	OR3X2
48	OR 3-input	OR3X4
49	OR 4-input	OR4X1
50	OR 4-input	OR4X2
51	OR 4-input	OR4X4
52	NOR 2-input	NOR2X0
53	NOR 2-input	NOR2X1
54	NOR 2-input	NOR2X2
55	NOR 2-input	NOR2X4
56	NOR 3-input	NOR3X0
57	NOR 3-input	NOR3X1
58	NOR 3-input	NOR3X2
59	NOR 3-input	NOR3X4
60	NOR 4-input	NOR4X0
61	NOR 4-input	NOR4X1
62	XOR 2-input	XOR2X1
63	XOR 2-input	XOR2X2
64	XOR 3-input	XOR3X1
65	XOR 3-input	XOR3X2
66	XNOR 2-input	XNOR2X1
67	XNOR 2-input	XNOR2X2
68	XNOR 3-input	XNOR3X1
69	XNOR 3-input	XNOR3X2
	Complex Logic Gates	
70	AND-OR 2/1	AO21X1
71	AND-OR 2/1	AO21X2
72	AND-OR 2/2	AO22X1
73	AND-OR 2/2	AO22X2
74	AND-OR 2/2/1	AO221X1
75	AND-OR 2/2/1	AO221X2

No	Cell Description	Cell Name
76	AND-OR 2/2/2	AO222X1
77	AND-OR 2/2/2	AO222X2
78	AND-OR-Invert 2/1	AOI21X1
79	AND-OR Invert 2/1	AOI21X2
80	AND-OR-Invert 2/2	AOI22X1
81	AND-OR-Invert 2/2	AOI22X2
82	AND-OR-Invert 2/2/1	AOI221X1
83	AND-OR-Invert 2/2/1	AOI221X2
84	AND-OR-Invert 2/2/2	AOI222X1
85	AND-OR-Invert 2/2/2	AOI222X2
86	OR-AND 2/1	OA21X1
87	OR-AND 2/1	OA21X2
88	OR-AND 2/2	OA22X1
89	OR-AND 2/2	OA22X2
90	OR-AND 2/2/1	OA221X1
91	OR-AND 2/2/1	OA221X2
92	OR-AND 2/2/2	OA222X1
93	OR-AND 2/2/2	OA222X2
94	OR-AND-Invert 2/1	OAI21X1
95	OR-AND-Invert 2/1	OAI21X2
96	OR-AND-Invert 2/2	OAI22X1
97	OR-AND-Invert 2/2	OAI22X2
98	OR-AND-Invert 2/2/1	OAI221X1
99	OR-AND-Invert 2/2/1	OAI221X2
100	OR-AND-Invert 2/2/2	OAI222X1
101	OR-AND-Invert 2/2/2	OAI222X2
	Multiplexers	
102	Multiplexer 2 to 1	MUX21X1
103	Multiplexer 2 to 1	MUX21X2
104	Multiplexer 4 to 1	MUX41X1
105	Multiplexer 4 to 1	MUX41X2
	Decoders	
106	Decoder 2 to 4	DEC24X1
107	Decoder 2 to 4	DEC24X2
	Adders and Subtractors	
108	Half Adder 1 bit	HADDX1
109	Half Adder 1 bit	HADDX2
110	Full Adder 1 bit	FADDX1
111	Full Adder 1 bit	FADDX2
	D Flip-Flops	
112	Pos Edge DFF	DFFX1

No	Cell Description	Cell Name
113	Pos Edge DFF	DFFX2
114	Pos Edge DFF, w/ Async Low-Active Set	DFFASX1
115	Pos Edge DFF, w/ Async Low-Active Set	DFFASX2
116	Pos Edge DFF, w/ Async Low-Active Reset	DFFARX1
117	Pos Edge DFF, w/ Async Low-Active Reset	DFFARX2
118	Pos Edge DFF, w/ Async Low-Active Set & Reset	DFFASRX1
119	Pos Edge DFF, w/ Async Low-Active Set & Reset	DFFASRX2
120	Pos Edge DFF, w/ Sync Low-Active Set & Reset	DFFSSRX1
121	Pos Edge DFF, w/ Sync Low-Active Set & Reset	DFFSSRX2
122	Neg Edge DFF	DFFNX1
123	Neg Edge DFF	DFFNX2
124	Neg Edge DFF, w/ Async Low-Active Set	DFFNASX1
125	Neg Edge DFF, w/ Async Low-Active Set	DFFNASX2
126	Neg Edge DFF, w/ Async Low-Active Reset	DFFNARX1
127	Neg Edge DFF, w/ Async Low-Active Reset	DFFNARX2
128	Neg Edge DFF, w/ Async Low-Active Set & Reset	DFFNASRX1
129	Neg Edge DFF, w/ Async Low-Active Set & Reset	DFFNASRX2
130	Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out	DFFNASRQX1
131	Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out	DFFNASRQX2
132	Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out	DFFNASRNX1
133	Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out	DFFNASRNX2
	Scan D Flip-Flops	
134	Scan Pos Edge DFF	SDFFX1
135	Scan Pos Edge DFF	SDFFX2
136	Scan Pos Edge DFF, w/ Async Low-Active Set	SDFFASX1
137	Scan Pos Edge DFF, w/ Async Low-Active Set	SDFFASX2
138	Scan Pos Edge DFF, w/ Async Low-Active Reset	SDFFARX1
139	Scan Pos Edge DFF, w/ Async Low-Active Reset	SDFFARX2
140	Scan Pos Edge DFF, w/ Async Low-Active Set & Reset	SDFFASRX1
141	Scan Pos Edge DFF, w/ Async Low-Active Set & Reset	SDFFASRX2
142	Scan Pos Edge DFF, w/ Async Low-Active Set & Reset, Q, QN, & S0 outs	SDFFASRSX1
143	Scan Pos Edge DFF, w/ Async Low-Active Set & Reset, Q, QN, & S0 outs	SDFFASRSX2
144	Scan Pos Edge DFF, w/ Sync Low-Active Set & Reset	SDFFSSRX1
145	Scan Pos Edge DFF, w/ Sync Low-Active Set & Reset	SDFFSSRX2
146	Scan Neg Edge DFF	SDFFNX1
147	Scan Neg Edge DFF	SDFFNX2
148	Scan Neg Edge DFF, w/ Async Low-Active Set	SDFFNASX1
149	Scan Neg Edge DFF, w/ Async Low-Active Set	SDFFNASX2
150	Scan Neg Edge DFF, w/ Async Low-Active Reset	SDFFNARX1
151	Scan Neg Edge DFF, w/ Async Low-Active Reset	SDFFNARX2
152	Scan Neg Edge DFF, w/ Async Low-Active Set & Reset	SDFFNASRX1
153	Scan Neg Edge DFF, w/ Async Low-Active Set & Reset	SDFFNASRX2
	Latches	

No	Cell Description	Cell Name
154	RS NAND Latch	LNANDX1
155	RS NAND Latch	LNANDX2
156	High-Active Latch	LATCHX1
157	High-Active Latch	LATCHX2
158	High-Active Latch, w/ Async Low-Active Set	LASX1
159	High-Active Latch, w/ Async Low-Active Set	LASX2
160	High-Active Latch, w/ Async Low-Active Reset	LARX1
161	High-Active Latch, w/ Async Low-Active Reset	LARX2
162	High-Active Latch, w/ Async Low-Active Set & Reset	LASRX1
163	High-Active Latch, w/ Async Low-Active Set & Reset	LASRX2
164	High-Active Latch ,w/ Async Low-Active Set & Reset only Q out	LASRQX1
165	High-Active Latch, w/ Async Low-Active Set & Reset only Q out	LASRQX2
166	High-Active Latch, w/ Async Low-Active Set & Reset only QN out	LASRNX1
167	High-Active Latch, w/ Async Low-Active Set & Reset only QN out	LASRNX2
	Clocked Gates	
168	Clock Gating cell, w/ Latched Pos Edge Control Post	CGLPPSX2
169	Clock Gating cell, w/ Latched Pos Edge Control Post	CGLPPSX4
170	Clock Gating cell, w/ Latched Pos Edge Control Post	CGLPPSX8
171	Clock Gating cell, w/ Latched Pos Edge Control Post	CGLPPSX16
172	Clock Gating cell, w/ Latched Neg Edge Control Post	CGLNPSX2
173	Clock Gating cell, w/ Latched Neg Edge Control Post	CGLNPSX4
174	Clock Gating cell, w/ Latched Neg Edge Control Post	CGLNPSX8
175	Clock Gating cell, w/ Latched Neg Edge Control Post	CGLNPSX16
176	Clock Gating cell ,w/ Latched Pos Edge Control Pre	CGLPPRX2
177	Clock Gating cell ,w/ Latched Pos Edge Control Pre	CGLPPRX8
178	Clock Gating cell ,w/ Latched Neg Edge Control Pre	CGLNPRX2
179	Clock Gating cell, w/ Latched Neg Edge Control Pre	CGLNPRX8
	Delay Lines	
180	Non-inverting Delay Line, 250 ps	DELLN1X2
181	Non-inverting Delay Line, 500 ps	DELLN2X2
182	Non-inverting Delay Line, 750 ps	DELLN3X2
	Pass Gates	
183	Pass Gate	PGX1
184	Pass Gate	PGX2
185	Pass Gate	PGX4
	Bi-directional Switches	
186	Bi-directional Switch w/ Low-Active Enable	BSLEX1
187	Bi-directional Switch w/ Low-Active Enable	BSLEX2
188	Bi-directional Switch w/ Low-Active Enable	BSLEX4
	Isolation Cells	
189	Hold 0 Isolation Cell (Logic AND)	ISOLANDX1
190	Hold 0 Isolation Cell (Logic AND)	ISOLANDX2
191	Hold 0 Isolation Cell (Logic AND)	ISOLANDX4

No	Cell Description	Cell Name
192	Hold 0 Isolation Cell (Logic AND)	ISOLANDX8
193	Hold 0 Isolation Cell (Logic AND),Always On	ISOLANDAOX1
194	Hold 0 Isolation Cell (Logic AND),Always On	ISOLANDAOX2
195	Hold 0 Isolation Cell (Logic AND),Always On	ISOLANDAOX4
196	Hold 0 Isolation Cell (Logic AND),Always On	ISOLANDAOX8
197	Hold 1 Isolation Cell (Logic OR)	ISOLORX1
198	Hold 1 Isolation Cell (Logic OR)	ISOLORX2
199	Hold 1 Isolation Cell (Logic OR)	ISOLORX4
200	Hold 1 Isolation Cell (Logic OR),	ISOLORX8
201	Hold 1 Isolation Cell (Logic OR),Always On	ISOLORAOX1
202	Hold 1 Isolation Cell (Logic OR),Always On	ISOLORAOX2
203	Hold 1 Isolation Cell (Logic OR),Always On	ISOLORAOX4
204	Hold 1 Isolation Cell (Logic OR),Always On	ISOLORAOX8
	Level Shifters	
205	Low to High Level Shifter	LSUPX1
206	Low to High Level Shifter	LSUPX2
207	Low to High Level Shifter	LSUPX4
208	Low to High Level Shifter	LSUPX8
209	High to Low Level Shifter	LSDNX1
210	High to Low Level Shifter	LSDNX2
211	High to Low Level Shifter	LSDNX4
212	High to Low Level Shifter	LSDNX8
213	Low to High Level Shifter/ High-Active Enable, Clamp High	LSUPENX1
214	Low to High Level Shifter/ High-Active Enable, Clamp High	LSUPENX2
215	Low to High Level Shifter/ High-Active Enable, Clamp High	LSUPENX4
216	Low to High Level Shifter/ High-Active Enable, Clamp High	LSUPENX8
217	High to Low Level Shifter/ High-Active Enable, Clamp High	LSDNENX1
218	High to Low Level Shifter/ High-Active Enable, Clamp High	LSDNENX2
219	High to Low Level Shifter/ High-Active Enable, Clamp High	LSDNENX4
220	High to Low Level Shifter/ High-Active Enable, Clamp High	LSDNENX8
221	Low to High Level Shifter/ High-Active Enable, Clamp Low	LSUPENCLX1
222	Low to High Level Shifter/ High-Active Enable, Clamp Low	LSUPENCLX2
223	Low to High Level Shifter/ High-Active Enable, Clamp Low	LSUPENCLX4
224	Low to High Level Shifter/ High-Active Enable, Clamp Low	LSUPENCLX8
225	High to Low Level Shifter/ High-Active Enable, Clamp Low	LSDNENCLX1
226	High to Low Level Shifter/ High-Active Enable, Clamp Low	LSDNENCLX2
227	High to Low Level Shifter/ High-Active Enable, Clamp Low	LSDNENCLX4
228	High to Low Level Shifter/ High-Active Enable, Clamp Low	LSDNENCLX8
229	High to Low Level Shifter/Single Supply	LSDNSSX1
230	High to Low Level Shifter/Single Supply	LSDNSSX2
231	High to Low Level Shifter/Single Supply	LSDNSSX3
232	High to Low Level Shifter/Single Supply	LSDNSSX4
233	High to Low Level Shifter/High-Active Enable,Single Supply	LSDNENSSX1

No	Cell Description	Cell Name
234	High to Low Level Shifter/High-Active Enable,Single Supply	LSDNENSSX2
235	High to Low Level Shifter/High-Active Enable,Single Supply	LSDNENSSX4
236	High to Low Level Shifter/High-Active Enable,Single Supply	LSDNENSSX8
237	High to Low Level Shifter/High-Active Enable, Clamp Low, Single Supply	LSDNENCLSSX1
238	High to Low Level Shifter/High-Active Enable, Clamp Low, Single Supply	LSDNENCLSSX2
239	High to Low Level Shifter/High-Active Enable, Clamp Low, Single Supply	LSDNENCLSSX4
240	High to Low Level Shifter/High-Active Enable, Clamp Low, Single Supply	LSDNENCLSSX8
	Retention Flip-Flops and scan Flip-Flops	
241	Pos Edge Retention DFF	RDFFX1
242	Pos Edge Retention DFF	RDFFX2
243	Scan Pos Edge Retention DFF	RSDFFX1
244	Scan Pos Edge Retention DFF	RSDFFX2
245	Neg Edge Retention DFF	RDFFNX1
246	Neg Edge Retention DFF	RDFFNX2
247	Scan Neg Edge Retention DFF	RSDFFNX1
248	Scan Neg Edge Retention DFF	RSDFFNX2
249	Scan Pos Edge Retention DFF ,w/ Async Low-Active Reset	RSDFFARX1
250	Scan Pos Edge Retention DFF ,w/ Async Low-Active Reset	RSDFFARX2
251	Scan Neg Edge Retention DFF,w/ Async Low-Active Reset	RSDFFNARX1
252	Scan Neg Edge Retention DFF,w/ Async Low-Active Reset	RSDFFNARX2
253	Pos Edge Retention DFF, w/ Async Low-Active Reset	RDFFARX1
254	Pos Edge Retention DFF, w/ Async Low-Active Reset	RDFFARX2
255	Neg Edge Retention DFF, w/ Async Low-Active Reset	RDFFNARX1
256	Neg Edge Retention DFF, w/ Async Low-Active Reset	RDFFNARX2
	Retention D Flip-Flops with Save and Restore (SR) pins	
257	Pos Edge DFF SR	RDFFSRX1
258	Pos Edge DFF SR	RDFFSRX2
259	Pos Edge DFF SR, w/ Async Low-Active Set	RDFFSRASX1
260	Pos Edge DFF SR, w/ Async Low-Active Set	RDFFSRASX2
261	Pos Edge DFF SR, w/ Async Low-Active Reset	RDFFSRARX1
262	Pos Edge DFF SR, w/ Async Low-Active Reset	RDFFSRARX2
263	Pos Edge DFF SR, w/ Async Low-Active Set & Reset	RDFFSRASRX1
264	Pos Edge DFF SR, w/ Async Low-Active Set & Reset	RDFFSRASRX2
265	Pos Edge DFF SR, w/ Sync Low-Active Set & Reset	RDFFSRSSRX1
266	Pos Edge DFF SR, w/ Sync Low-Active Set & Reset	RDFFSRSSRX2
267	Neg Edge DFF SR	RDFFNSRX1
268	Neg Edge DFF SR	RDFFNSRX2
269	Neg Edge DFF SR, w/ Async Low-Active Set	RDFFNSRASX1
270	Neg Edge DFF SR, w/ Async Low-Active Set	RDFFNSRASX2
271	Pos Edge DFF SR, w/ Async Low-Active Reset	RDFFNSRARX1
272	Pos Edge DFF SR, w/ Async Low-Active Reset	RDFFNSRARX2
273	Neg Edge DFF SR, w/ Async Low-Active Set & Reset	RDFFNSRASRX1
274	Neg Edge DFF SR, w/ Async Low-Active Set & Reset	RDFFNSRASRX2

No	Cell Description	Cell Name
275	Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out	RDFFNSRASRQX1
276	Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out	RDFFNSRASRQX2
277	Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out	RDFFNSRASRNX1
278	Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out	RDFFNSRASRNX2
	Scan Retention D Flip-Flops with Save and Restore (SR) pins	
279	Scan Pos Edge DFF SR	RSDFFSRX1
280	Scan Pos Edge DFF SR	RSDFFSRX2
281	Scan Pos Edge DFF SR, w/ Async Low-Active Set	RSDFFSRASX1
282	Scan Pos Edge DFF SR, w/ Async Low-Active Set	RSDFFSRASX2
283	Scan Pos Edge DFF SR, w/ Async Low-Active Reset	RSDFFSRARX1
284	Scan Pos Edge DFF SR, w/ Async Low-Active Reset	RSDFFSRARX2
285	Scan Pos Edge DFF SR, w/ Async Low-Active Set & Reset	RSDFFSRASRX1
286	Scan Pos Edge DFF SR, w/ Async Low-Active Set & Reset	RSDFFSRASRX2
287	Scan Pos Edge DFF SR, w/ Sync Low-Active Set & Reset	RSDFFSRSSRX1
288	Scan Pos Edge DFF SR, w/ Sync Low-Active Set & Reset	RSDFFSRSSRX2
289	Scan Neg Edge DFF SR	RSDFFNSRX1
290	Scan Neg Edge DFF SR	RSDFFNSRX2
291	Scan Neg Edge DFF SR, w/ Async Low-Active Set	RSDFFNSRASX1
292	Scan Neg Edge DFF SR, w/ Async Low-Active Set	RSDFFNSRASX2
293	Scan Pos Edge DFF SR , w/ Async Low-Active Reset	RSDFFNSRARX1
294	Scan Pos Edge DFF SR, w/ Async Low-Active Reset	RSDFFNSRARX2
295	Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset	RSDFFNSRASRX1
296	Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset	RSDFFNSRASRX2
297	Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out	RSDFFNSRASRQX1
298	Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out	RSDFFNSRASRQX2
299	Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out	RSDFFNSRASRNX1
300	Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out	RSDFFNSRASRNX2
	Power Gating Cells	
301	Header Cell	HEADX2
302	Header Cell	HEADX4
303	Header Cell	HEADX8
304	Header Cell	HEADX16
305	Header Cell	HEADX32
306	Header Cell (with SLEEPOUT output)	HEAD2X2
307	Header Cell (with SLEEPOUT output)	HEAD2X4
308	Header Cell (with SLEEPOUT output)	HEAD2X8
309	Header Cell (with SLEEPOUT output)	HEAD2X16
310	Header Cell (with SLEEPOUT output)	HEAD2X32
311	Footer Cell	FOOTX2
312	Footer Cell	FOOTX4
313	Footer Cell	FOOTX8
314	Footer Cell	FOOTX16
315	Footer Cell	FOOTX32

No	Cell Description	Cell Name
316	Footer Cell (with SLEEPOUT output)	FOOT2X2
317	Footer Cell (with SLEEPOUT output)	FOOT2X4
318	Footer Cell (with SLEEPOUT output)	FOOT2X8
319	Footer Cell (with SLEEPOUT output)	FOOT2X16
320	Footer Cell (with SLEEPOUT output)	FOOT2X32
	Always on Cells	
321	Always on Inverter	AOINVX1
322	Always on Inverter	AOINVX2
323	Always on Inverter	AOINVX4
324	Always on Non-inverting Buffer	AOBUFX1
325	Always on Non-inverting Buffer	AOBUFX2
326	Always on Non-inverting Buffer	AOBUFX4
327	Always on Pos Edge DFF, w/ Async Low-Active Reset	AODFFARX1
328	Always on Pos Edge DFF, w/ Async Low-Active Reset	AODFFARX2
329	Always on Neg Edge DFF, w/ Async Low-Active Reset	AODFFNARX1
330	Always on Neg Edge DFF, w/ Async Low-Active Reset	AODFFNARX2
	Additional Cells	
331	Bus Keeper	BUSKP
332	P-MOSFET (w=0.4 um, l=0.03um)	PMT1
333	P-MOSFET (w=0.8 um, l=0.03um)	PMT2
334	P-MOSFET (w=1.6 um, l=0.03um)	PMT3
335	N-MOSFET (w=0.2 um, l=0.03um)	NMT1
336	N-MOSFET (w=0.34 um, l=0.03um)	NMT2
337	N-MOSFET (w=0.7 um, l=0.03um)	NMT3
338	Tie High	TIEH
339	Tie Low	TIEL
340	Antenna Diode	ANTENNA
341	Decoupling Capacitance	DCAP
342	Capacitive Load	CLOAD1
	Fillers	
343	Single Height Filler Cell 1 grid width	SHFILL1
344	Single Height Filler Cell 2 grid width	SHFILL2
345	Single Height Filler Cell 3 grid width	SHFILL3
346	Single Height Filler Cell 64 grid width	SHFILL64
347	Single Height Filler Cell 128 grid width	SHFILL128
348	Double Height (high-low-high) Filler Cell 1 grid width	DHFILLUP1
349	Double Height (low-high-low) Filler Cell 1 grid width	DHFILLDN1
350	Double Height (for AO and Retention cells) Filler Cell 1 grid width	DHFILLAO1

3. Digital Standard Cell Library Deliverables

Table 3.1. Digital Standard Cell Library deliverables

N	Type	Description
1	.pdf	Databook / User guide, Layer usage file
2	.db, .lib	Synthesis
3	.v	Verilog simulation models
4	.tv	TetraMAX Verilog models
5	.vhd	VHDL / Vital simulation models
6	.cdl, .sp	LVS, HSPICE netlists
7	.spf	Extracted C and RC netlists for different corners
8	.gds	GDSII layout views
9	.clf	Cell antenna information
10	.lef	LEF files
11	.FRAM, .CEL	FRAM views, layout views
12	.drc, .erc, .lvs	Report files

4. Physical structure of digital cell

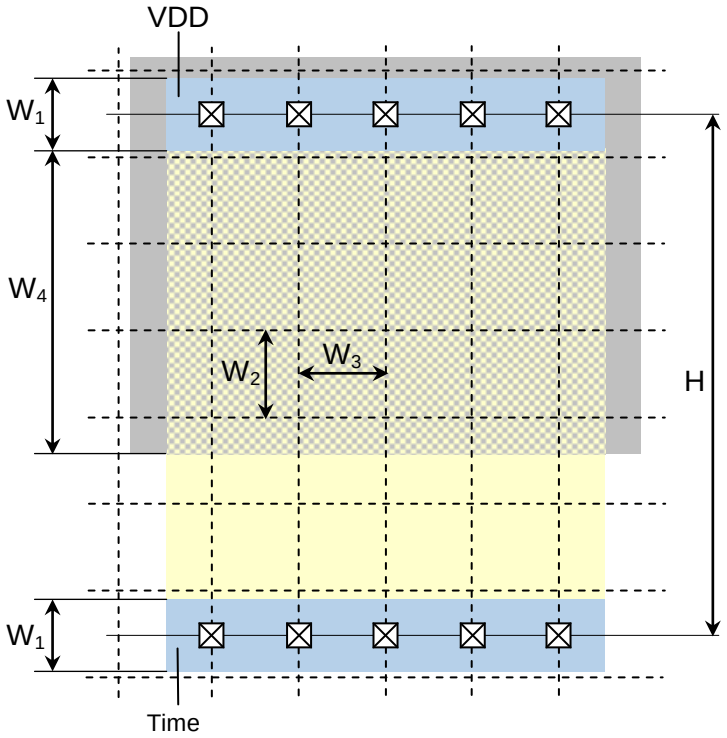


Figure 4.1. Physical structure of digital standard cells

The selection of physical structure of digital cell should be aimed at providing maximum cell density in digital designs. It is more important to provide minimal area for the most frequently used cells. In general, these are usually NAND cells with two inputs, and D flip-flops. The width of the power rails were selected on the basis of acceptable current density given by the design rules, and electromigration.

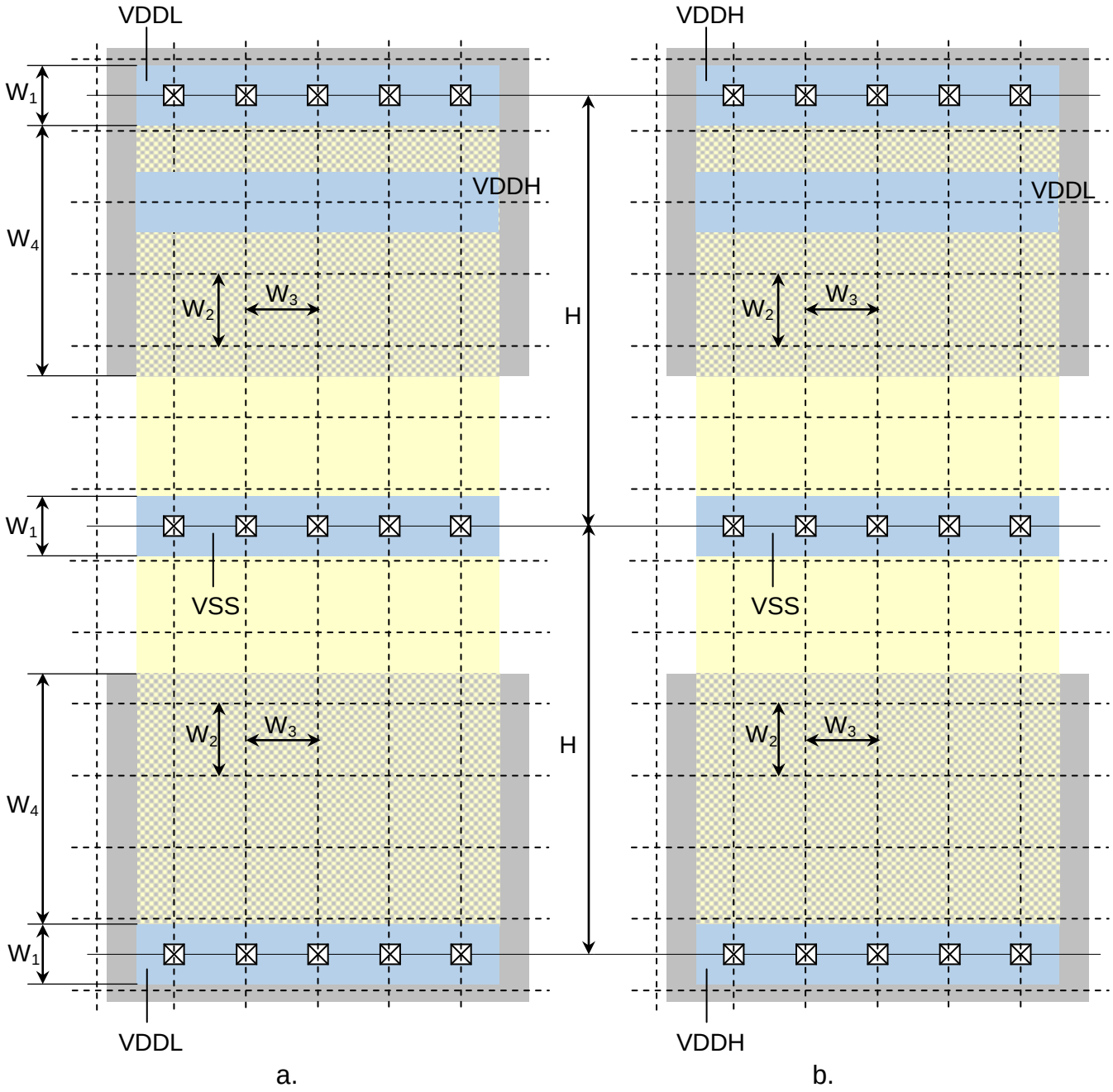


Figure 4.2. Physical structure of Level-shifter cells:
a. High-to-Low, b.Low-to-High

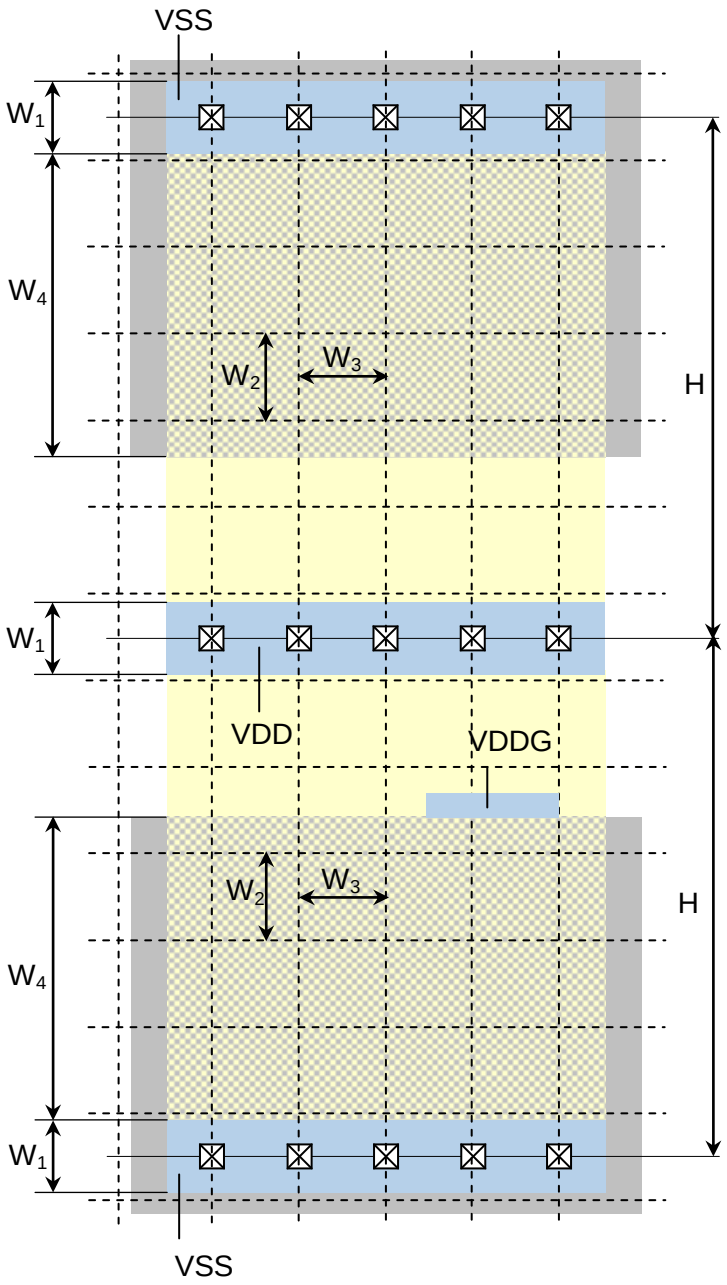


Figure 4.3. Physical structure of Always on and Power Gating Cells

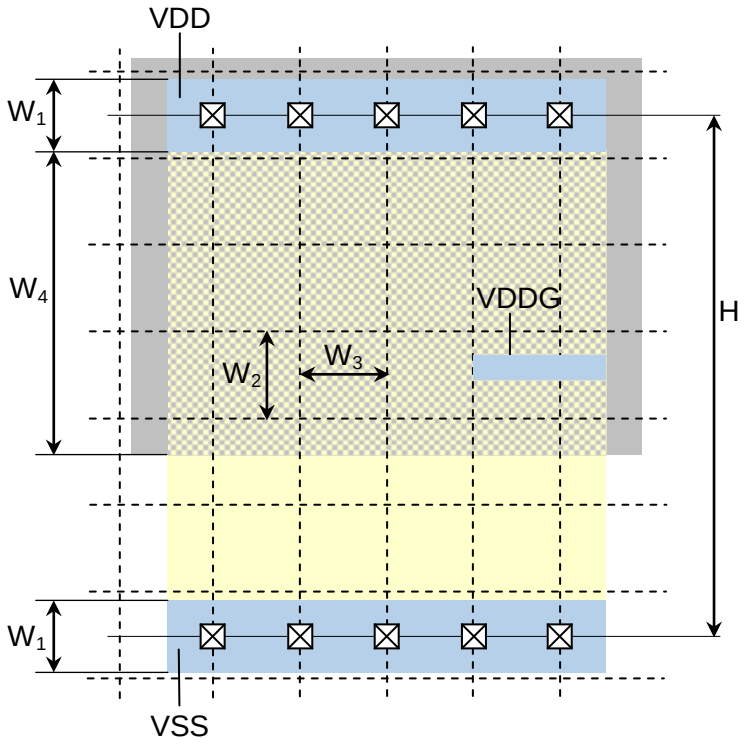
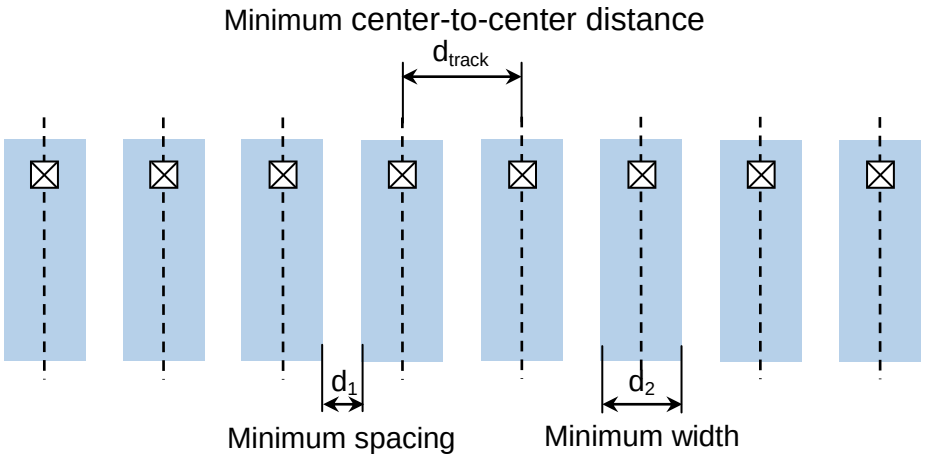


Figure 4.4. Physical structure of digital standard cells: Retention Flip-Flops

Table 4.1. Physical structure specification

Parameter	Symbol	Value
Cell height	H	1.672
Power rail width	W_1	0.056
Vertical grid	W_2	0.152
Horizontal grid	W_3	0.152
NWell height	W_4	0.942

d_{track} is the minimum center-to-center distance for metal2 layers (with VIA12). It was used as agrid for cell architecrure.



$d_{track}=d_1+d_2$.

Figure 4.5. Definition of d_{track}

5. Digital Standard Cells' descriptions

Inverters: INVX0, INVX1, INVX2, INVX4, INVX8, INVX16, INVX32

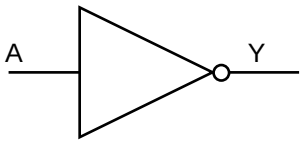


Figure 5.1. Logic Symbol of Inverter

Table 5.1. INV Truth Table

A	Y
0	1
1	0

Table 5.2. Inverter Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um2)
INVX0	0.5 x Csl	*38*	24	0.80	1.27072
INVX1	1 x Csl	30	49	1.30	1.27072
INVX2	2 x Csl	29	100	2.32	1.524864
INVX4	4 x Csl	30	240	4.19	2.033152
INVX8	8 x Csl	28	549	15.80	3.049728
INVX16	16 x Csl	29	1220	15.40	5.08288
INVX32	32 x Csl	29	2580	30.20	9.149184

Inverting Buffers: IBUFFX2, IBUFFX4, IBUFFX8, IBUFFX16, IBUFFX32

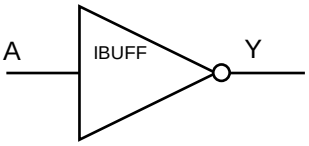


Figure 5.2. Logic Symbol of Inverting Buffer

Table 5.3. IBUFF Truth Table

A	Y
0	1
1	0

Table 5.4. Inverting Buffer Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
IBUFFX2	2 x Csl	54	257	6	2.54144
IBUFFX4	4 x Csl	50	541	10	3.049728
IBUFFX8	8 x Csl	49	1134	18	4.320448
IBUFFX16	16 x Csl	48	2102	36	6.607744
IBUFFX32	32 x Csl	31	4291	71	11.690624

Non-Inverting Buffers: NBUFFX2, NBUFFX4, NBUFFX8, NBUFFX16, NBUFFX32

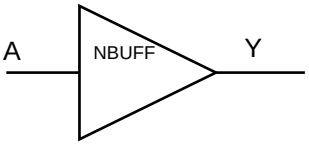


Figure 5.3. Logic Symbol of Non-Inverting Buffer

Table 5.5. NBUFF Truth Table

A	Y
0	0
1	1

Table 5.6. Non-inverting Buffer Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		Ps	nW	nW/MHz	(um^2)
NBUFFX2	2 x Csl	44	514	2	2.033152
NBUFFX4	4 x Csl	30	1041	4	2.54144
NBUFFX8	8 x Csl	33	2106	7	3.81216
NBUFFX16	16 x Csl	33	4168	14	6.099456
NBUFFX32	32 x Csl	34	8301	31	10.674048

Tri-state Non-inverting Buffer w/ High-Active Enable: TNBUFFX1, TNBUFFX2, TNBUFFX4, TNBUFFX8, TNBUFFX16, TNBUFFX32

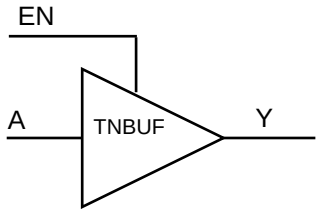


Figure 5.4. Logic Symbol of Tri-state Non-inverting Buffer w/ High-Active Enable

Table 5.7. TNBUFF Truth Table

EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1

Table 5.8. Tri-state Non-inverting Buffer w/ High-Active Enable Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
TNBUFFX1	1 x Csl	60	260	3	3.303872
TNBUFFX2	2 x Csl	63	491	5	3.558016
TNBUFFX4	4 x Csl	65	965	9	4.066304
TNBUFFX8	8 x Csl	61	1929	17	5.845312
TNBUFFX16	16 x Csl	72	3759	36	8.640896
TNBUFFX32	32 x Csl	95	8626	61	17.535936

AND: AND2X1, AND2X2, AND2X4, AND3X1, AND3X2, AND3X4, AND4X1, AND4X2, AND4X4

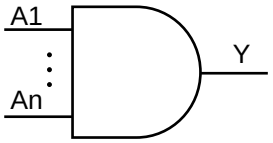


Figure 5.5. Logic Symbol of AND

Table 5.9. AND Truth Table (n=2,3,4)

A1	A2	. . .	An	Y
0	X	. . .	X	0
X	0	. . .	X	0
. . .	. . .	. . .	. . .	0
X	X	. . .	0	0
1	1	1	1	1

Table 5.10. AND Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AND2X1	1 x Csl	100	297	3	2.033152
AND2X2	2 x Csl	110	517	5	2.287296
AND2X4	4 x Csl	70	1008	8	2.795584
AND3X1	1 x Csl	60	296	3	2.287296
AND3X2	2 x Csl	70	501	5	2.54144
AND3X4	4 x Csl	80	998	9	3.049728
AND4X1	1 x Csl	73	294	3.4	2.54144
AND4X2	2 x Csl	93	609	7	3.81216
AND4X4	4 x Csl	130	1151	22	4.320448

NAND: NAND2X0, NAND2X1, NAND2X2, NAND2X4, NAND3X0, NAND3X1, NAND3X2, NAND3X4, NAND4X0, NAND4X1

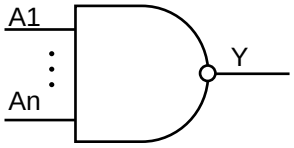


Figure 5.6. Logic Symbol of NAND

Table 5.11. NAND Truth Table (n=2,3,4)

A1	A2	. . .	An	Y
0	X	. . .	X	1
X	0	. . .	X	1
. . .	. . .	. . .	. . .	1
X	X	. . .	0	1
1	1	1	1	0

Table 5.12. NAND Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
NAND2X0	0.5 x Csl	60	150	1	1.524864
NAND2X1	1 x Csl	61	498	4	2.54144
NAND2X2	2 x Csl	60	757	5	2.795584
NAND2X4	4 x Csl	70	1295	12	3.303872
NAND3X0	0.5 x Csl	60	215	1	1.779008
NAND3X1	1 x Csl	100	497	4	2.795584
NAND3X2	2 x Csl	115	743	5	3.049728
NAND3X4	4 x Csl	90	1238	5	3.558016
NAND4X0	0.5 x Csl	68	317	2	2.033152
NAND4X1	1 x Csl	365	495	5	3.049728

OR: OR2X1, OR2X2, OR2X4, OR3X1, OR3X2, OR3X4, OR4X1, OR4X2, OR4X4

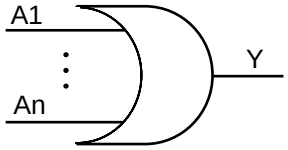


Figure 5.7. Logic Symbol of OR

Table 5.13. OR Truth Table (n=2,3,4)

A1	A2	. . .	An	Y
0	0	. . .	0	0
1	X	. . .	X	1
. . .	. . .	. . .	. . .	1
X	1	. . .	X	1
X	X	X	1	1

Table 5.14. OR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OR2X1	1 x Csl	60	393	4	2.033152
OR2X2	2 x Csl	55	551	4	2.287296
OR2X4	4 x Csl	65	1050	7	2.795584
OR3X1	1 x Csl	73	313	3	2.54144
OR3X2	2 x Csl	70	557	5	2.54144
OR3X4	4 x Csl	77	1205	10	4.066304
OR4X1	1 x Csl	97	460	6	3.558016
OR4X2	2 x Csl	340	710	4	3.81216
OR4X4	4 x Csl	330	1230	10	4.320448

NOR: NOR2X0, NOR2X1, NOR2X2, NOR2X4, NOR3X0, NOR3X1, NOR3X2, NOR3X4, NOR4X0, NOR4X1

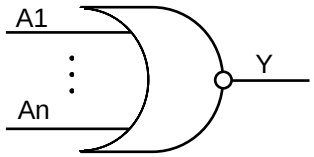


Figure 5.8. Logic Symbol of NOR

Table 5.15. NOR Truth Table (n=2,3,4)

A1	A2	. . .	An	Y
0	0	. . .	0	1
1	X	. . .	X	0
. . .	. . .	. . .	. . .	0
X	1	. . .	X	0
X	X	X	1	0

Table 5.16. NOR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
NOR2X0	0.5 x Csl	73	393	4	2.54144
NOR2X1	1 x Csl	72	393	4	2.54144
NOR2X2	2 x Csl	64	626	5	2.795584
NOR2X4	4 x Csl	68	1064	10	3.303872
NOR3X0	0.5 x Csl	100	356	3	2.795584
NOR3X1	1 x Csl	200	355	4	2.795584
NOR3X2	2 x Csl	73	584	6	3.049728
NOR3X4	4 x Csl	77	1062	5	3.558016
NOR4X0	0.5 x Csl	100	317	5	3.049728
NOR4X1	1 x Csl	90	317	5	3.049728

XOR: XOR2X1, XOR2X2, XOR3X1, XOR3X2

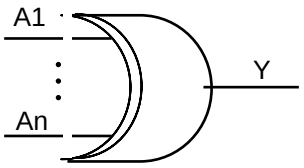


Figure 5.9. Logic Symbol of XOR

Table 5.17. XOR Truth Table (n=2,3)

A1	A2	. . .	An	Y
0	0	. . .	0	0
Odd number of 1's				1
Even number of 1's				0

Table 5.18. XOR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
XOR2X1	1 x Csl	85	344	2	4.320448
XOR2X2	2 x Csl	70	820	0.4	4.574592
XOR3X1	1 x Csl	320	1067	0.4	7.116032
XOR3X2	2 x Csl	140	1116	2	7.370176

XNOR: XNOR2X1, XNOR2X2, XNOR3X1, XNOR3X2

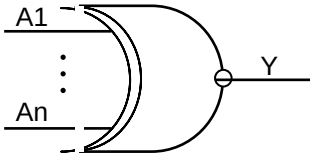


Figure 5.10. Logic Symbol of XNOR

Table 5.19. XNOR Truth Table (n=2,3)

A1	A2	. . .	An	Y
0	0	. . .	0	1
Odd number of 1's				0
Even number of 1's				1

Table 5.20. XNOR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
XNOR2X1	1 x Csl	95	393	1	4.320448
XNOR2X2	2 x Csl	75	906	2	4.574592
XNOR3X1	1 x Csl	135	1078	3	6.099456
XNOR3X2	2 x Csl	247	1415	5	6.3536

AND-OR: AO21X1, AO21X2
Y=(1&2)|3

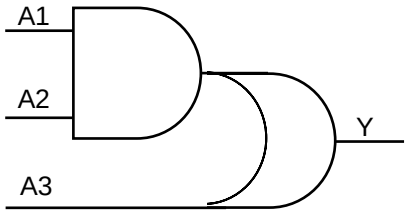


Figure 5.11. Logic Symbol of AND-OR

Table 5.21. AO21 Truth Table

A1	A2	A3	Y
1	1	X	1
X	X	1	1
0	X	0	0
X	0	0	0

Table 5.22. AND-OR 2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AO21X1	1 x Csl	63	277	3	2.54144
AO21X2	2 x Csl	64	524	5	2.795584

AND-OR: AO22X1, AO22X2
Y=(1&2)|(3&4)

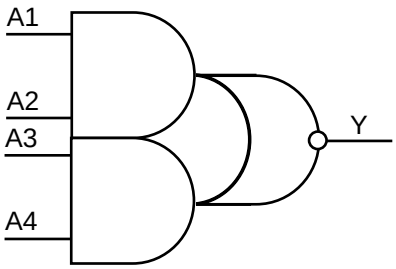


Figure 5.12. Logic Symbol of AND-OR

Table 5.23. AO22 Truth Table

A1	A2	A3	A4	Y
X	X	1	1	1
1	1	X	X	1
0	X	0	X	0
X	0	0	X	0
0	X	X	0	0
X	0	X	0	0

Table 5.24. AND-OR 2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AO22X1	1 x Csl	72	304	3	2.54144
AO22X2	2 x Csl	66	561	5	2.795584

AND-OR: AO221X1, AO221X2
Y=(1&2)|(3&4)|5

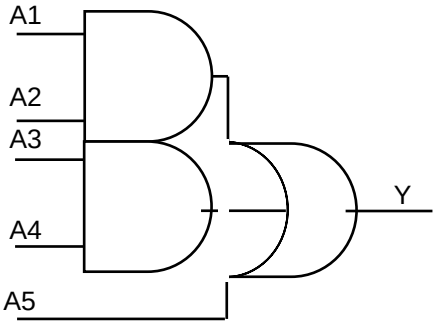


Figure 5.13. Logic Symbol of AND-OR

Table 5.25. AO221 Truth Table

A1	A2	A3	A4	A5	Y
1	1	X	X	X	1
X	X	1	1	X	1
X	X	X	X	1	1
0	X	0	X	0	0
X	0	0	X	0	0
0	X	X	0	0	0
X	0	X	0	0	0

Table 5.26. AND-OR 2/2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AO221X1	1 x Csl	82	284	4	3.049728
AO221X2	2 x Csl	78	545	6	3.303872

AND-OR: AO222X1, AO222X2
Y=(1&2)|(3&4)|(5&6)

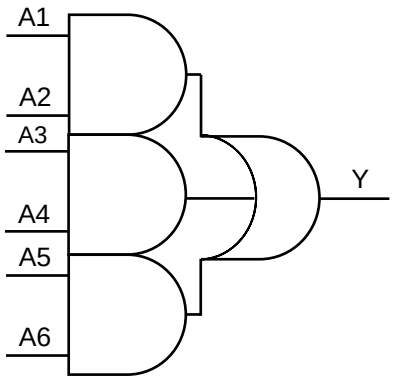


Figure 5.14. Logic Symbol of AND-OR

Table 5.27. AND-OR 2/2/2 Truth Table

A1	A2	A3	A4	A5	A6	Y
1	1	X	X	X	X	1
X	X	1	1	X	X	1
X	X	X	X	1	1	1
0	X	0	X	0	X	0
0	X	0	X	X	0	0
0	X	X	0	0	X	0
0	X	X	0	X	0	0
X	0	0	X	0	X	0
X	0	0	X	X	0	0
X	0	X	0	0	X	0
X	0	X	0	X	0	0

Table 5.28. AND-OR 2/2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AO222X1	1 x Csl	106	339	5	3.303872
AO222X2	2 x Csl	78	630	6	3.558016

AND-OR-Invert: AOI21X1, AOI21X2
!Y=!((1&2)|3)

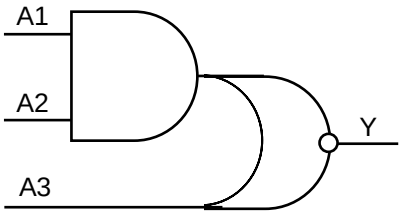


Figure 5.15. Logic Symbol of AND-OR-INVERT

Table 5.29. AOI21 Truth Table

A1	A2	A3	Y
1	1	X	0
X	X	1	0
0	X	0	1
X	0	0	1

Table 5.30. AND-OR-Invert 2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AOI21X1	1 x Csl	79	417	4	3.049728
AOI21X2	2 x Csl	212	665	6	3.303872

AND-OR-Invert: AOI22X1, AOI22X2
Y=!((1&2)|(3&4))

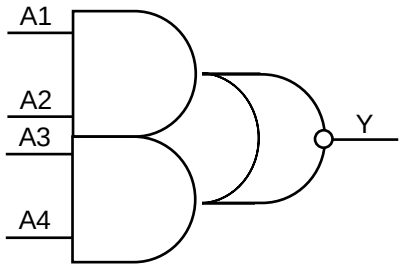


Figure 5.16. Logic Symbol of AND-OR-INVERT

Table 5.31. AOI22 Truth Table

A1	A2	A3	A4	Y
X	X	1	1	0
1	1	X	X	0
0	X	0	X	1
X	0	0	X	1
0	X	X	0	1
X	0	X	0	1

Table 5.32. AND-OR-Invert 2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AOI22X1	1 x Csl	80	462	4	3.049728
AOI22X2	2 x Csl	75	722	7	3.303872

AND-OR-Invert: AOI221X1, AOI221X2
Y=!((1&2)|(3&4)|5)

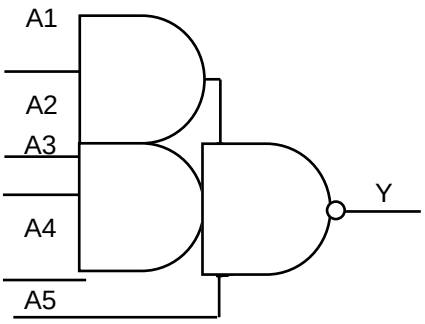


Figure 5.17. Logic Symbol of AND-OR-INVERT

Table 5.33. AOI221 Truth Table

A1	A2	A3	A4	A5	Y
1	1	X	X	X	0
X	X	1	1	X	0
X	X	X	X	1	0
0	X	0	X	0	1
X	0	0	X	0	1
0	X	X	0	0	1
X	0	X	0	0	1

Table 5.34. AND-OR-Invert 2/2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AOI221X1	1 x Csl	91	398	5	3.558016
AOI221X2	2 x Csl	82	724	7	3.81216

AND-OR-Invert: AOI222X1, AOI222X2
Y=!((1&2)|(3&4)|(5&6))

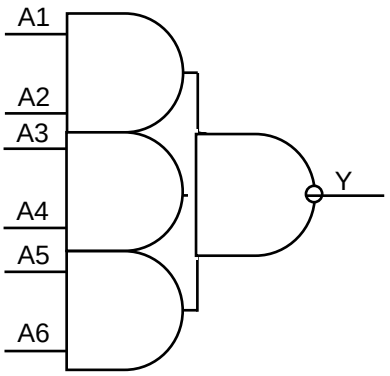


Figure 5.18. Logic Symbol of AND-OR-INVERT

Table 5.35. AOI222 Truth Table

A1	A2	A3	A4	A5	A6	Y
1	1	X	X	X	X	1
X	X	1	1	X	X	1
X	X	X	X	1	1	1
0	X	0	X	0	X	0
0	X	0	X	X	0	0
0	X	X	0	0	X	0
0	X	X	0	X	0	0
X	0	0	X	0	X	0
X	0	0	X	X	0	0
X	0	X	0	0	X	0
X	0	X	0	X	0	0

Table 5.36. AND-OR-Invert 2/2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AOI222X1	1 x Csl	93	446	5	3.81216
AOI222X2	2 x Csl	88	716	7	4.066304

OR-AND: OA21X1, OA21X2
Y=(1|2)&3

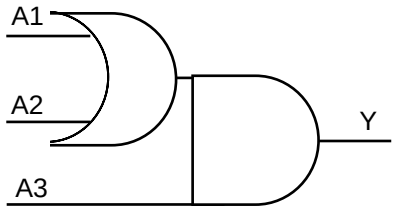


Figure 5.19. Logic Symbol of OR-AND

Table 5.37. OA21 Truth Table

A1	A2	A3	Y
0	0	X	0
X	X	0	0
1	X	1	1
X	1	1	1

Table 5.38. OR-AND 2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.02 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OA21X1	1 x Csl	69	284	3	2.54144
OA21X2	2 x Csl	65	531	5	2.795584

OR-AND: OA22X1, OA22X2
Y=(1|2)&(3|4)

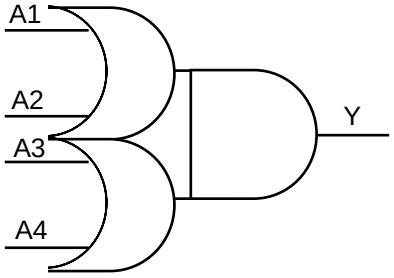


Figure 5.20. Logic Symbol of OR-AND

Table 5.39. OA22 Truth Table

A1	A2	A3	A4	Y
0	0	X	X	0
X	X	0	0	0
1	X	1	X	1
X	1	1	X	1
1	X	X	1	1
X	1	X	1	1

Table 5.40. OR-AND 2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OA22X1	1 x Csl	70	294	3	2.54144
OA22X2	2 x Csl	68	542	5	2.795584

OR-AND: OA221X1, OA221X2
Y=(1|2)&(3|4)&5

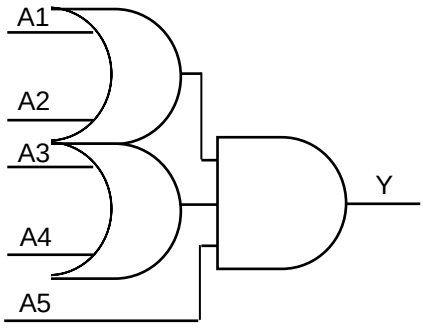


Figure 5.21. Logic Symbol of OR-AND

Table 5.41. OA221 Truth Table

A1	A2	A3	A4	A5	Y
0	0	X	X	X	0
X	X	0	0	X	0
X	X	X	X	0	0
1	X	1	X	1	1
X	1	1	X	1	1
1	X	X	1	1	1
X	1	X	1	1	1

Table 5.42. OR-AND 2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OA221X1	1 x Csl	82	288	3	3.049728
OA221X2	2 x Csl	77	543	6	3.303872

OR-AND: OA222X1, OA222X2
Y=(1|2)&(3|4)&(5|6)

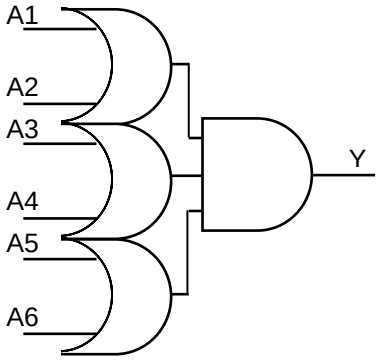


Figure 5.22. Logic Symbol of OR-AND

Table 5.43. OA222 Truth Table

A1	A2	A3	A4	A5	A6	Y
0	0	X	X	X	X	0
X	X	0	0	X	X	0
X	X	X	X	0	0	0
1	X	1	X	1	X	1
1	X	1	X	X	1	1
1	X	X	1	1	X	1
1	X	X	1	X	1	1
X	1	1	X	1	X	1
X	1	1	X	X	1	1
X	1	X	1	1	X	1
X	1	X	1	X	1	1

Table 5.44. OR-AND 2/2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OA222X1	1 x Csl	87	415	4	3.303872
OA222X2	2 x Csl	72	558	6	3.558016

OR-AND-Invert: OAI21X1, OAI21X2
QN=!((1|2)&3)

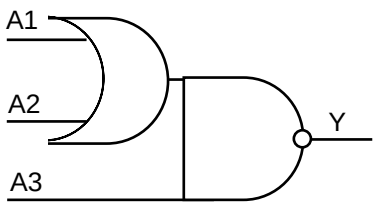


Figure 5.23. Logic Symbol of OR-AND-INVERT

Table 5.45. OAI21 Truth Table

A1	A2	A3	Y
0	0	X	1
X	X	0	1
1	X	1	0
X	1	1	0

Table 5.46. OR-AND-INVERT 2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OAI21X1	1 x Csl	91	333	4	3.049728
OAI21X2	2 x Csl	77	600	6	3.303872

OR-AND-Invert: OAI22X1, OAI22X2
QN=!((1|2)&(3|4))

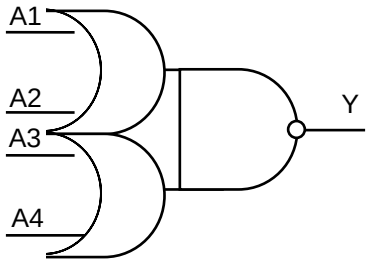


Figure 5.24. Logic Symbol of OR-AND-INVERT

Table 5.47. OAI22 Truth Table

A1	A2	A3	A4	Y
0	0	X	X	1
X	X	0	0	1
1	X	1	X	0
X	1	1	X	0
1	X	X	1	0
X	1	X	1	0

Table 5.48. OR-AND-INVERT 2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
OAI22X1	1 x Csl	78	624	5	3.049728
OAI22X2	2 x Csl	68	887	7	3.303872

OR-AND-Invert: OAI221X1, OAI221X2
QN=!((1|2)&(3|4)&5)

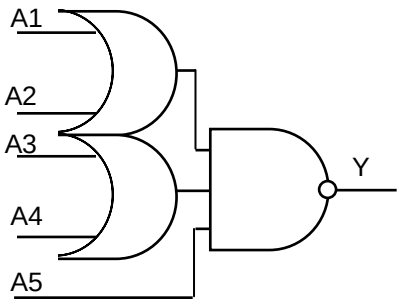


Figure 5.25. Logic Symbol of OR-AND-INVERT

Table 5.49. OAI221 Truth Table

A1	A2	A3	A4	A5	Y
0	0	X	X	X	1
X	X	0	0	X	1
X	X	X	X	0	1
1	X	1	X	1	0
X	1	1	X	1	0
1	X	X	1	1	0
X	1	X	1	1	0

Table 5.50. OR-AND-INVERT 2/2/1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area Cload
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	ps
OAI221X1	1 x Csl	90	458	5	3.558016
OAI221X2	2 x Csl	78	729	7	3.81216

OR-AND-Invert: OAI222X1, OAI222X2
QN=!((1|2)&(3|4)&(5|6))

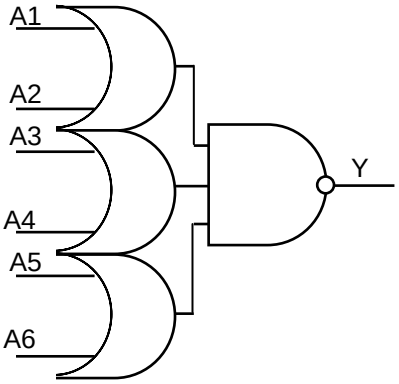


Figure 5.26. Logic Symbol of OR-AND-INVERT

Table 5.51. OAI222 Truth Table

A1	A2	A3	A4	A5	A6	Y
0	0	X	X	X	X	1
X	X	0	0	X	X	1
X	X	X	X	0	0	1
1	X	1	X	1	X	0
1	X	1	X	X	1	0
1	X	X	1	1	X	0
1	X	X	1	X	1	0
X	1	1	X	1	X	0
X	1	1	X	X	1	0
X	1	X	1	1	X	0
X	1	X	1	X	1	0

Table 5.52. OR-AND-INVERT 2/2/2 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area Cload
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	ps
OAI222X1	1 x Csl	93	632	5	3.81216
OAI222X2	2 x Csl	82	911	7	4.066304

Multiplexer 2 to 1: MUX21X1, MUX21X2

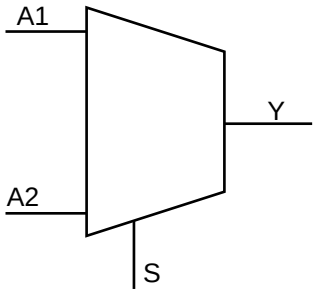


Figure 5.27. Logic Symbol of Multiplexer 2 to 1

Table 5.53. MUX21 Truth Table

S	Y
0	A1
1	A2

Table 5.54. Multiplexer 2 to 1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area Cload
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	ps
MUX21X1	1 x Csl	80	174	4	3.303872
MUX21X2	2 x Csl	67	282	5	3.558016

Multiplexer 4 to 1: MUX41X1, MUX41X2

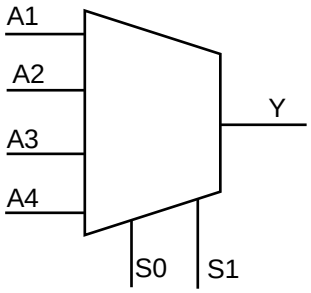


Figure 5.28. Logic Symbol of Multiplexer 4 to 1

Table 5.55. MUX41 Truth Table

S1	S0	Y
0	0	A1
0	1	A2
1	0	A3
1	1	A4

Table 5.56. Multiplexer 4 to 1 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
MUX41X1	1 x Csl	113	320	5	5.591168
MUX41X2	2 x Csl	85	509	7	6.099456

Decoder 2 to 4: DEC24X1, DEC24X2

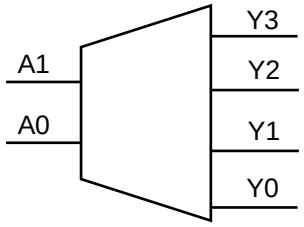


Figure 5.29. Logic Symbol of Decoder 2 to 4

Table 5.57. DEC24 Truth Table

A1	A0	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table 5.58. Decoder 2 to 4 Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DEC24X1	1 x Csl	Y0	75	1030	3	6.099456
		Y1	65			
		Y2	60			
		Y3	55			
DEC24X2	2 x Csl	Y0	100	1503	4	7.116032
		Y1	55			
		Y2	55			
		Y3	50			

Half Adder 1-Bit: HADDX1, HADDX2

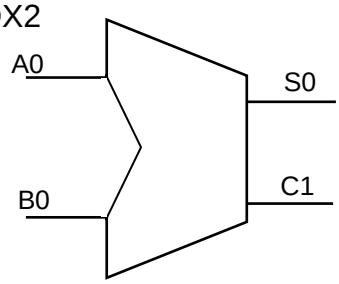


Figure 5.30. Logic Symbol of Half Adder 1-Bit

Table 5.59. HADD Truth Table

A0	B0	S0 (sum)	C1 (carry)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 5.60. Half Adder 1-Bit Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (S0, C1)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
HADDX1	1 x Csl	S0	70	596	5	3.303872
		C1	73		5	
HADDX2	2 x Csl	S0	59	912	5	3.81216
		C1	57		5	

Full Adder 1-Bit: FADDX1, FADDX2

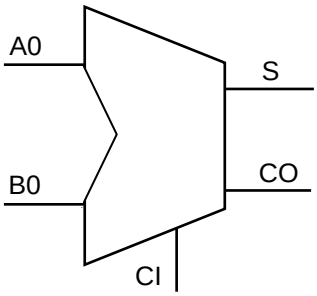


Figure 5.31. Logic Symbol of Full Adder 1-Bit

Table 5.61. FADD Truth Table

A 0	B 0	CI	S (sum)	CO (carry)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 5.62. Full Adder 1-Bit Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (S, CO)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
FADDX1	1 x Csl	S	85	613	5	4.828736
		CO	83		5	
FADDX2	2 x Csl	S	77	1028	5	5.337024
		CO	81		5	

Pos Edge DFF: DFFX1, DFFX2

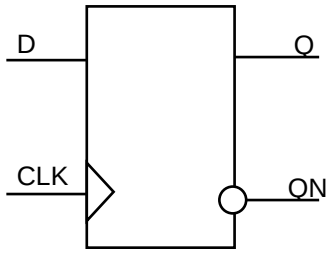


Figure 5.32. Logic Symbol of Pos Edge DFF

Table 5.63. DFF Transition Table

D	CLK	Q	QN
X	Inactive	No change	No change
1	Rise	1	0
0	Rise	0	1

Table 5.64. Pos Edge DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFX1	1 x Csl	Q	112	1178	7	6.607744
		QN	110			
DFFX2	2 x Csl	Q	130	1506	8	7.116032
		QN	120			

Pos Edge DFF w/Async Low-Active Set: DFFASX1, DFFASX2

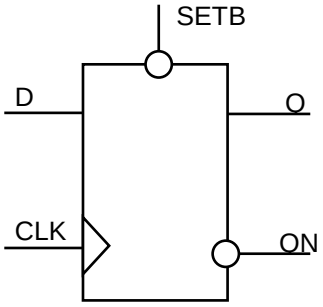


Figure 5.33. Logic Symbol of Pos Edge DFF w/Async Low-Active Set

Table 5.65. DFFAS Transition Table

D	SETB	CLK	Q	QN
X	0	X	1	0
X	1	Inactive	No change	No change
1	1	Rise	1	0
0	1	Rise	0	1

Table 5.66. Pos Edge DFF w/Async Low-Active Set Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFASX1	1 x Csl	Q	120	1152	8	7.116032
		QN	130			
DFFASX2	2 x Csl	Q	125	1474	8	7.62432
		QN	131			

Pos Edge DFF w/Async Low-Active Reset: DFFARX1, DFFARX2

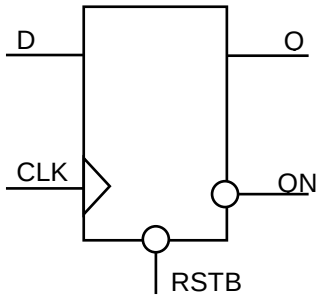


Figure 5.34. Logic Symbol of Pos Edge DFF w/Async Low-Active Reset

Table 5.67. DFFAR Transition Table

D	RSTB	CLK	Q	QN
X	0	X	0	1
X	1	Inactive	No change	No change
1	1	Rise	1	0
0	1	Rise	0	1

Table 5.68. Pos Edge DFF w/Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFARX1	1 x Csl	Q	139	1148	7	7.116032
		QN	143			
DFFARX2	2 x Csl	Q	135	1330	6	7.62432
		QN	130			

Pos Edge DFF w/Async Low-Active Set & Reset: DFFASRX1, DFFASRX2

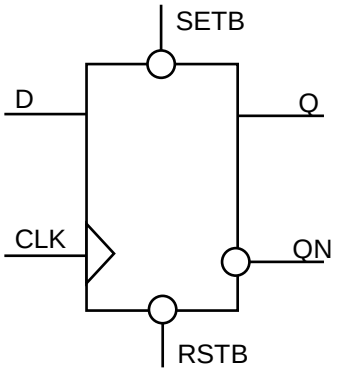


Figure 5.35. Logic Symbol of Pos Edge DFF w/Async Low-Active Set & Reset

Table 5.69. DFFASR Transition Table

D	SETB	RSTB	CLK	Q	QN	Notes
X	0	0	X	X	X	Not Allowed
X	0	1	X	1	0	
X	1	0	X	0	1	
X	1	1	Inactive	No change	No change	
1	1	1	Rise	1	0	
0	1	1	Rise	0	1	

Table 5.70. Pos Edge DFF w/Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFASRX1	1 x Csl	Q	151	1015	9	7.62432
		QN	146			
DFFASRX2	2 x Csl	Q	135	1219	8	8.132608
		QN	141			

Pos Edge DFF w/ Sync Low-Active Set & Reset: DFFSSRX1, DFFSSRX2

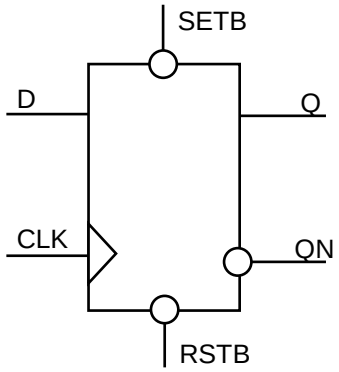


Figure 5.36. Logic Symbol of Pos Edge DFF w/ Sync Low-Active Set & Reset

Table 5.71. DFFASR Transition Table

D	SETB	RSTB	CLK	Q	QN	Notes
X	X	X	Inactive	No change	No change	
0	1	1	Rise	0	1	
1	1	1	Rise	1	0	
X	0	1	Rise	1	0	
X	1	0	Rise	0	1	
X	0	0	Rise	X	X	Not Allowed

Table 5.72. Pos Edge DFF w/ Sync Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFSSRX1	1 x Csl	Q	127	951	7	7.116032
		QN	119			
DFFSSRX2	2 x Csl	Q	142	1278	7	7.62432
		QN	126			

Neg Edge DFF: DFFNX1, DFFNX2

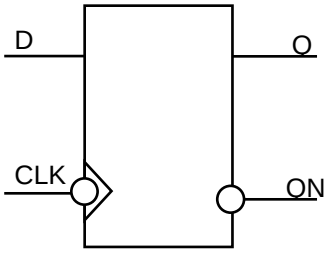


Figure 5.37. Logic Symbol of Neg Edge DFF

Table 5.73. DFFN Transition Table

D	CLK	Q	QN
X	Inactive	No change	No change
1	Fall	1	0
0	Fall	0	1

Table 5.74. Neg Edge DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFNX1	1 x Csl	Q	122	1166	9	6.607744
		QN	116			
DFFNX2	2 x Csl	Q	131	1494	10	7.116032
		QN	134			

Neg Edge DFF w/Async Low-Active Set: DFFNASX1, DFFNASX2

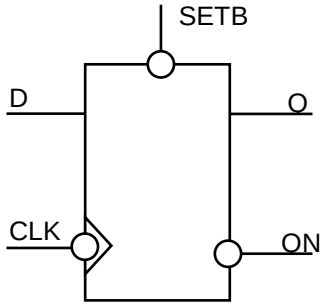


Figure 5.38. Logic Symbol of Neg Edge DFF w/Async Low-Active Set

Table 5.75. DFFNAS Transition Table

D	SETB	CLK	Q	QN
X	0	X	1	0
X	1	Inactive	No change	No change
1	1	Fall	1	0
0	1	Fall	0	1

Table 5.76. Neg Edge DFF w/Async Low-Active Set Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFNASX1	1 x Csl	Q	121	1142	8	7.116032
		QN	120			
DFFNASX2	2 x Csl	Q	129	1352	7	7.62432
		QN	124			

Neg Edge DFF w/Async Low-Active Reset: DFFNARX1, DFFNARX2

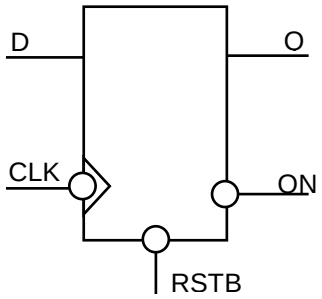


Figure 5.39. Logic Symbol of Neg Edge DFF w/Async Low-Active Reset

Table 5.77. DFFNAR Transition Table

D	RSTB	CLK	Q	QN
X	0	X	0	1
X	1	Inactive	No change	No change
1	1	Fall	1	0
0	1	Fall	0	1

Table 5.78. Neg Edge DFF w/Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFNARX1	1 x Csl	Q	142	1104	8	7.116032
		QN	139			
DFFNARX2	2 x Csl	Q	165	1425	9	7.62432
		QN	161			

Neg Edge DFF w/Async Low-Active Set & Reset: DFFNASRX1, DFFNASRX2

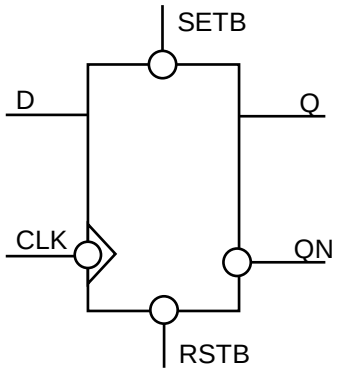


Figure 5.40. Logic Symbol of Neg Edge DFF w/Async Low-Active Set & Reset

Table 5.79. DFFNASR Transition Table

D	SETB	RSTB	CLK	Q	QN	Notes
X	0	0	X	X	X	Not Allowed
X	0	1	X	1	0	
X	1	0	X	0	1	
X	1	1	Inactive	No change	No change	
1	1	1	Fall	1	0	
0	1	1	Fall	0	1	

Table 5.80. Neg Edge DFF w/Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFNASRX1	1 x Csl	Q	151	1092	10	7.62432
		QN	146			
DFFNASRX2	2 x Csl	Q	172	1228	12	8.132608
		QN	168			

Neg Edge DFF w/Async Low-Active Set & Reset, Only Q out: DFFNASRQX1, DFFNASRQX2

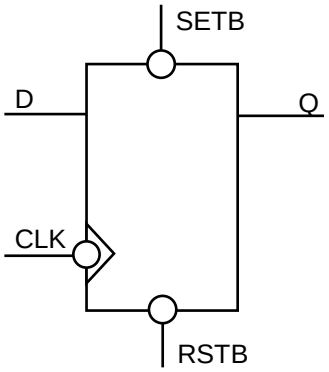


Figure 5.41. Logic Symbol of Neg Edge DFF w/Async Low-Active Set & Reset, Only Q out

Table 5.81. DFQNASBRB Transition Table

D	SETB	RSTB	CLK	Q	Notes
X	0	0	X	X	Not Allowed
X	0	1	X	1	
X	1	0	X	0	
X	1	1	Inactive	No change	
0	1	1	Fall	0	
1	1	1	Fall	1	

Table 5.82. Neg Edge DFF w/Async Low-Active Set & Reset, Only Q out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFNASRQX1	1 x Csl	Q	167	1022	11	7.370176
DFFNASRQX2	2 x Csl	Q	163	1181	13	7.62432

Neg Edge DFF w/Async Low-Active Set & Reset, Only QN out: DFFNASRNX1, DFFNASRNX2

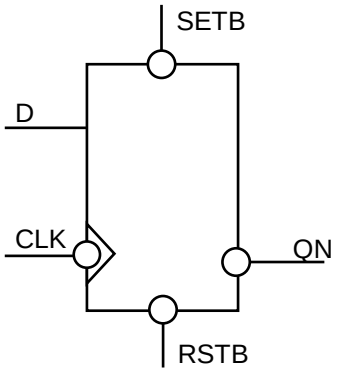


Figure 5.42. Logic Symbol of Neg Edge DFF w/Async Low-Active Set & Reset, Only QN out

Table 5.83. DFFNASRN Transition Table

D	SETB	RSTB	CLK	QN	Notes
X	0	0	X	X	Not Allowed
X	0	1	X	0	
X	1	0	X	1	
X	1	1	Inactive	No change	
0	1	1	Fall	1	
1	1	1	Fall	0	

Table 5.84. Neg Edge DFF w/Async Low-Active Set & Reset, Only QN out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
DFFNASRNX1	1 x Csl	QN	151	1022	6	7.370176
DFFNASRNX2	2 x Csl	QN	162	1130	7	7.62432

Scan Pos Edge DFF: SDFFX1, SDFFX2

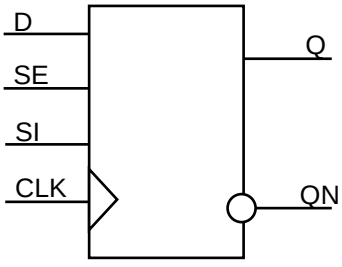


Figure 5.43. Logic Symbol of Scan Pos Edge DFF

Table 5.85. SDFF Transition Table

D	SI	SE	CLK	Q	QN
X	X	X	Inactive	No change	No change
1	X	0	Rise	1	0
0	X	0	Rise	0	1
X	1	1	Rise	1	0
X	0	1	Rise	0	1

Table 5.86. Scan Pos Edge DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFX1	1 x Csl	Q	127	1296	9	8.640896
		QN	112			
SDFFX2	2 x Csl	Q	143	1623	12	9.149184
		QN	120			

Scan Pos Edge DFF w/Async Low-Active Set SDFFASX1, SDFFASX2

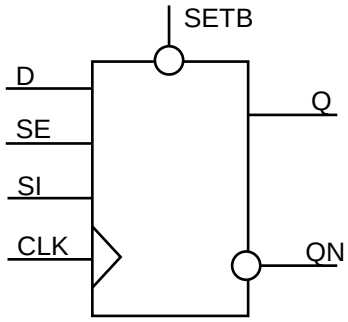


Figure 5.44. Logic Symbol of Scan Pos Edge DFF w/Async Low-Active Set

Table 5.87. SDFFAS Transition Table

D	SI	SE	SETB	CLK	Q	QN
X	X	X	0	X	1	0
X	X	X	1	Inactive	No change	No change
1	X	0	1	Rise	1	0
0	X	0	1	Rise	0	1
X	1	1	1	Rise	1	0
X	0	1	1	Rise	0	1

Table 5.88. Scan Pos Edge DFF w/Async Low-Active Set Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFASX1	1 x Csl	Q	120	1238	7	9.149184
		QN	131			
SDFFASX2	2 x Csl	Q	142	1502	7	9.657472
		QN	149			

Scan Pos Edge DFF w/Async Low-Active Reset: SDFFARX1, SDFFARX2

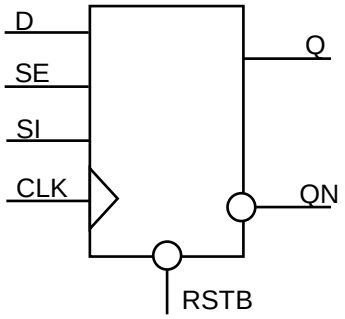


Figure 5.45. Logic Symbol of Scan Pos Edge DFF w/Async Low-Active Reset

Table 5.89. SDFFAR Transition Table

D	SI	SE	RSTB	CLK	Q	QN
X	X	X	0	X	0	1
X	X	X	1	Inactive	No change	No change
1	X	0	1	Rise	1	0
0	X	0	1	Rise	0	1
X	1	1	1	Rise	1	0
X	0	1	1	Rise	0	1

Table 5.90. Scan Pos Edge DFF w/Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFARX1	1 x Csl	Q	147	1252	8	9.149184
		QN	153			
SDFFARX2	2 x Csl	Q	165	1573	9	9.657472
		QN	172			

Scan Pos Edge DFF w/Async Low-Active Set & Reset: SDFFASRX1, SDFFASRX2

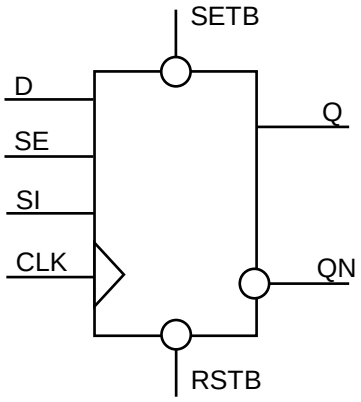


Figure 5.46. Logic Symbol of Scan Pos Edge DFF w/Async Low-Active Set & Reset

Table 5.91. SDFFASR Transition Table

D	SI	SE	SETB	RSTB	CLK	Q	QN	Notes
X	X	X	0	0	X	X	X	Not Allowed
X	X	X	0	1	X	1	0	
X	X	X	1	0	X	0	1	
X	X	X	1	1	Inactive	No change	No change	
1	X	0	1	1	Rise	1	0	
0	X	0	1	1	Rise	0	1	
X	1	1	1	1	Rise	X	1	
X	0	1	1	1	Rise	X	0	

Table 5.92. Scan Pos Edge DFF w/Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFASRX1	1 x Csl	Q	140	1177	8	10.16576
		QN	120			
SDFFASRX2	2 x Csl	Q	145	1559	9	10.16576
		QN	109			

Scan Pos Edge DFF w/Async Low-Active Set & Reset, Q, QN & S0 outs: SDFFASRSX1, SDFFASRSX2

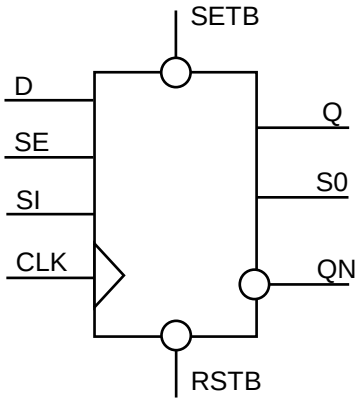


Figure 5.47. Logic Symbol of Scan Pos Edge DFF w/Async Low-Active Set & Reset, Q, QN & S0 outs

Table 5.93. SDFFASRS Transition Table

D	SI	SE	SETB	RSTB	CLK	Q	QN	S0	Notes
X	X	X	0	0	X	X	X	X	Not Allowed
X	X	X	0	1	X	1	0	1	
X	X	X	1	0	X	0	1	0	
X	X	X	1	1	Inactive	No change	No change	No change	
1	X	0	1	1	Rise	1	0	1	
0	X	0	1	1	Rise	0	1	0	
X	1	1	1	1	Rise	1	0	1	
X	0	1	1	1	Rise	0	1	0	

Table 5.94. Scan Pos Edge DFF w/Async Low-Active Set & Reset, Q, QN & S0 outs Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN, S0)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFASRSX1	1 x Csl	Q	173	1454	11	10.16576
		QN	153			
		S0	147			
SDFFASRSX2	2 x Csl	Q	182	1844	13	10.419904

Scan Pos Edge DFF w/ Sync Low-Active Set & Reset: SDFFSSRX1, SDFFSSRX2

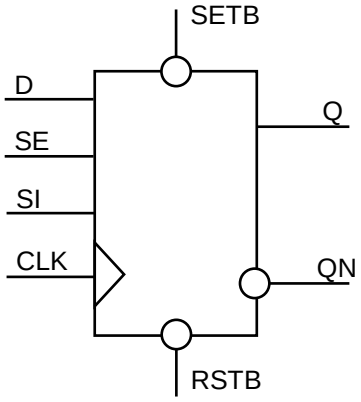


Figure 5.48. Logic Symbol of Scan Pos Edge DFF w/Async Low-Active Set & Reset

Table 5.95. SDFFSSR Transition Table

D	SI	SE	SETB	RSTB	CLK	Q	QN	Notes
X	X	0	0	0	Rise	X	X	Not Allowed
X	X	0	0	1	Rise	1	0	
X	X	0	1	0	Rise	0	1	
X	X	X	X	X	Inactive	No change	No change	
1	X	0	1	1	Rise	1	0	
0	X	0	1	1	Rise	0	1	
X	1	1	1	1	Rise	1	0	
X	0	1	1	1	Rise	0	1	

Table 5.96. Scan Pos Edge DFF w/ Sync Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFSSRX1	1 x Csl	Q	121	1320	9	8.89504
		QN	106			
SDFFSSRX2	2 x Csl	Q	136	1649	11	9.403328
		QN	120			

Scan Neg Edge DFF: SDFFNX1, SDFFNX2

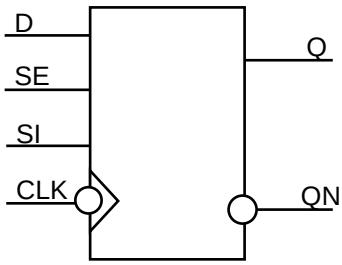


Figure 5.49. Logic Symbol of Scan Neg Edge DFF

Table 5.97. SDFFN Transition Table

D	SI	SE	CLK	Q	QN
X	X	X	Inactive	No change	No change
1	X	0	Fall	1	0
0	X	0	Fall	0	1
X	1	1	Fall	1	0
X	0	1	Fall	0	1

Table 5.98. Scan Neg Edge DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFNX1	1 x Csl	Q	114	1282	10	8.640896
		QN	105			
SDFFNX2	2 x Csl	Q	126	1531	11	9.149184
		QN	112			

Scan Neg Edge DFF w/Async Low-Active Set SDFFNASX1, SDFFNASX2

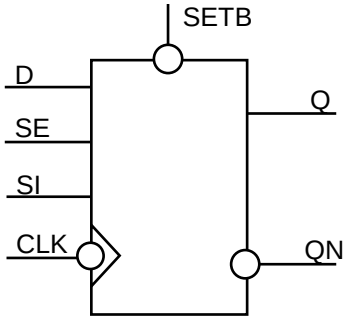


Figure 5.50. Logic Symbol of Scan Neg Edge DFF w/Async Low-Active Set

Table 5.99. SDFFNAS Transition Table

D	SI	SE	SETB	CLK	Q	QN
X	X	X	0	X	1	0
X	X	X	1	Inactive	No change	No change
1	X	0	1	Fall	1	0
0	X	0	1	Fall	0	1
X	1	1	1	Fall	1	0
X	0	1	1	Fall	0	1

Table 5.100. Scan Neg Edge DFF w/Async Low-Active Set Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFNASX1	1 x Csl	Q	105	1258	9	9.149184
		QN	120			
SDFFNASX2	2 x Csl	Q	125	1586	10	9.657472
		QN	131			

Scan Neg Edge DFF w/Async Low-Active Reset: SDFFNARX1, SDFFNARX2

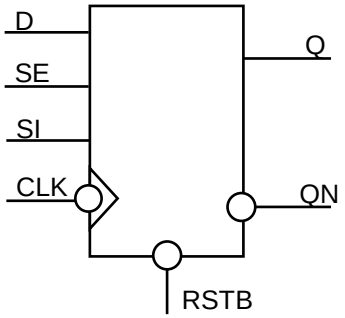


Figure 5.51. Logic Symbol of Scan Neg Edge DFF w/Async Low-Active Reset

Table 5.101. SDFFNAR Transition Table

D	SI	SE	RSTB	CLK	Q	QN
X	X	X	0	X	0	1
X	X	X	1	Inactive	No change	No change
1	X	0	1	Fall	1	0
0	X	0	1	Fall	0	1
X	1	1	1	Fall	1	0
X	0	1	1	Fall	0	1

Table 5.102. Scan Neg Edge DFF w/Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFNARX1	1 x Csl	Q	95	1206	8	9.149184
		QN	93			
SDFFNARX2	2 x Csl	Q	112	1437	10	9.657472
		QN	106			

Scan Neg Edge DFF w/Async Low-Active Set & Reset: SDFFNASRX1, SDFFNASRX2

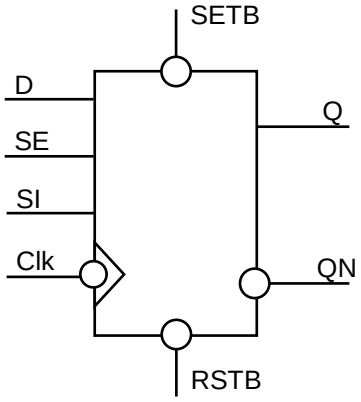


Figure 5.52. Logic Symbol of Scan Neg Edge DFF w/Async Low-Active Set & Reset

Table 5.103. SDFFNASR Transition Table

D	SI	SE	SETB	RSTB	CLK	Q	QN	Notes
X	X	X	0	0	X	X	X	Not Allowed
X	X	X	0	1	X	1	0	
X	X	X	1	0	X	0	1	
X	X	X	1	1	Inactive	No change	No change	
1	X	0	1	1	Fall	1	0	
0	X	0	1	1	Fall	0	1	
X	1	1	1	1	Fall	X	1	
X	0	1	1	1	Fall	X	0	

Table 5.104. Scan Neg Edge DFF w/Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
SDFFNASRX1	1 x Csl	Q	102	1210	8	9.657472
		QN	100			
SDFFNASRX2	2 x Csl	Q	124	1352	9	10.16576
		QN	119			

RS-NAND Latch: LNANDX1, LNANDX2

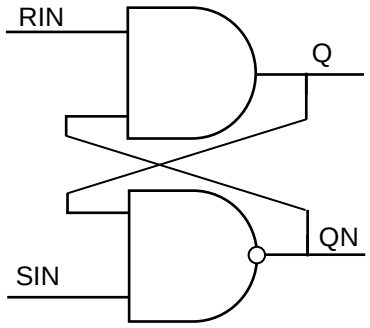


Figure 5.53. Logic Symbol of RS-NAND Latch

Table 5.105. LNAND Transition Table

RIN	SIN	Q	QN
0	0	X	X
0	1	1	0
1	0	0	1
1	1	No change	No change

Table 5.106. RS-NAND Latch Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
LNANDX1	1 x Csl	Q	111	142	3	2.287296
		QN	109			
LNANDX2	2 x Csl	Q	132	286	4	3.303872
		QN	128			

High-Active Latch: LATCHX1, LATCHX2

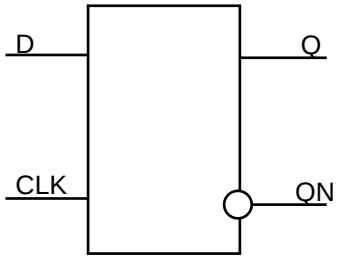


Figure 5.54. Logic Symbol of High-Active Latch

Table 5.107. LATCH Transition Table

D	CLK	Q	QN
X	0	No change	No change
0	1	0	1
1	1	1	0

Table 5.108. High-Active Latch Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
LATCHX1	1 x Csl	Q	85	948	10	5.08288
		QN	95			
LATCHX2	2 x Csl	Q	117	1268	12	5.591168
		QN	125			

High-Active Latch w/ Async Low-Active Set: LASX1, LASX2

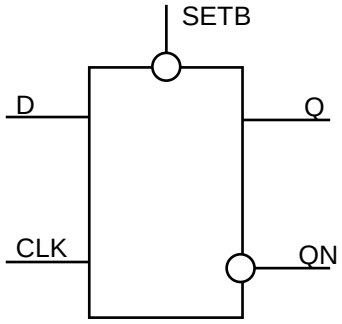


Figure 5.55. Logic Symbol of High-Active Latch w/ Async Low-Active Set

Table 5.109. LAS Transition Table

D	SETB	CLK	Q	QN
X	1	0	No change	No change
X	0	X	1	0
1	1	1	1	0
0	1	1	0	1s

Table 5.110. High-Active Latch w/ Async Low-Active Set Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
LASX1	1 x Csl	Q	103	1181	9	5.337024
		QN	112			
LASX2	2 x Csl	Q	129	1516	9	5.845312
		QN	125			

High-Active Latch w/ Async Low-Active Reset: LARX1, LARX2

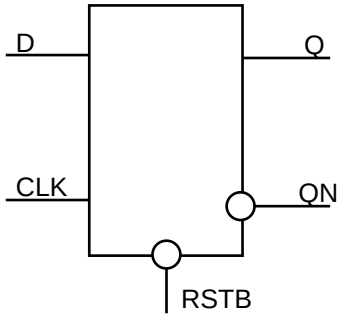


Figure 5.56. Logic Symbol of High-Active Latch w/ Async Low-Active Reset

Table 5.111. LAR Transition Table

D	RSTB	CLK	Q	QN
X	1	0	No change	No change
X	0	X	0	1
1	1	1	1	0
0	1	1	0	1s

Table 5.112. High-Active Latch w/ Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
LARX1	1 x Csl	Q	112	864	5	5.591168
		QN	90			
LARX2	2 x Csl	Q	151	1187	7	6.099456
		QN	123			

High-Active Latch w/ Async Low-Active Set & Reset: LASRX1, LASRX2

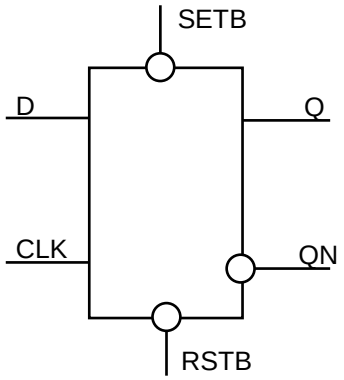


Figure 5.57. Logic Symbol of High-Active Latch w/ Async Low-Active Set & Reset

Table 5.113. LASR Transition Table

D	SETB	RSTB	CLK	Q	QN	Notes
X	1	1	X	X	X	Not Allowed
X	0	1	X	1	0	
X	1	0	X	0	1	
X	1	1	0	No change	No change	
1	1	1	1	1	0	
0	1	1	1	0	1	

Table 5.114. High-Active Latch w/ Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.2 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um^2)
LASRX1	1 x Csl	Q	115	1017	9	5.845312
		QN	110			
LASRX2	2 x Csl	Q	132	1353	10	6.3536
		QN	128			

High-Active Latch w/ Async Low-Active Set & Reset only Q out: LASRQX1, LASRQX2

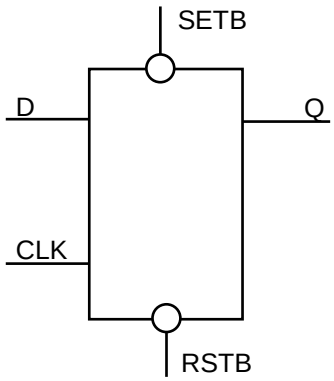


Figure 5.58. Logic Symbol of High-Active Latch w/ Async Low-Active Set & Reset only Q out

Table 5.115. LASRQ Transition Table

D	SETB	RSTB	CLK	Q	Notes
X	0	0	X	X	Not Allowed
X	0	1	X	1	
X	1	0	X	0	
X	1	1	0	No change	
1	1	1	1	1	
0	1	1	1	0	

Table 5.116. High-Active Latch w/ Async Low-Active Set & Reset only Q out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LASRQX1	1 x Csl	122	935	7	5.591168
LASRQX2	2 x Csl	141	1188	4	5.845312

High-Active Latch w/ Async Low-Active Set & Reset only QN out: LASRNX1, LASRNX2

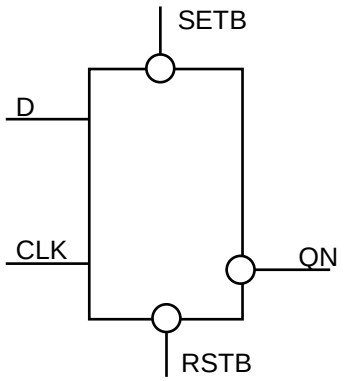


Figure 5.59. Logic Symbol of High-Active Latch w/ Async Low-Active Set & Reset only QN out

Table 5.117. LASRN Transition Table

D	SETB	RSTB	CLK	QN	Notes
X	0	0	X	X	Not Allowed
X	0	1	X	0	
X	1	0	X	1	
X	1	1	0	No change	
1	1	1	1	0	
0	1	1	1	1	

Table 5.118. High-Active Latch w/ Async Low-Active Set & Reset only QN out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LASRNX1	1 x Csl	146	982	8	5.591168
LASRNX2	2 x Csl	152	1232	9	5.845312

Clock Gating cell w/ Latched Pos Edge Control Post: CGLPPSX2, CGLPPSX4, CGLPPSX8, CGLPPSX16

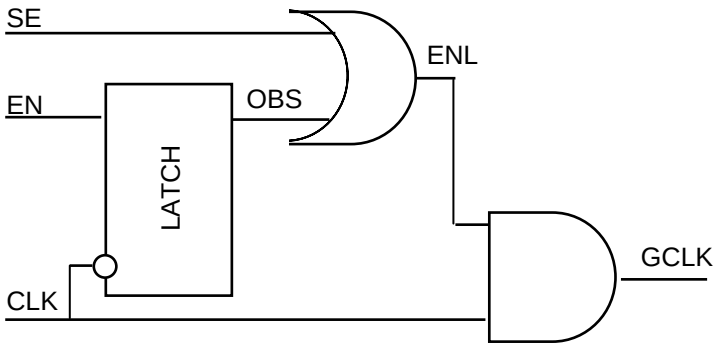


Figure 5.60. Logic Symbol of Clock Gating cell w/ Latched Pos Edge Control Post

Table 5.119. CGLPPS Truth Table

SE	EN	CLK	GCLK
1	X	0	0
1	X	1	1
0	0	0	0
0	0	1	OBS
0	1	0	0
0	1	1	1

Table 5.120. Clock Gating cell w/ Latched Pos Edge Control Post Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
CGLPPSX2	2 x Csl	85	1652	6	6.861888
CGLPPSX4	4 x Csl	84	2200	11	7.370176
CGLPPSX8	8 x Csl	105	3193	31	8.386752
CGLPPSX16	16 x Csl	148	5180	109	10.419904

Clock Gating cell w/ Latched Neg Edge Control Post: CGLNPSX2, CGLNPSX4, CGLNPSX8, CGLNPSX16

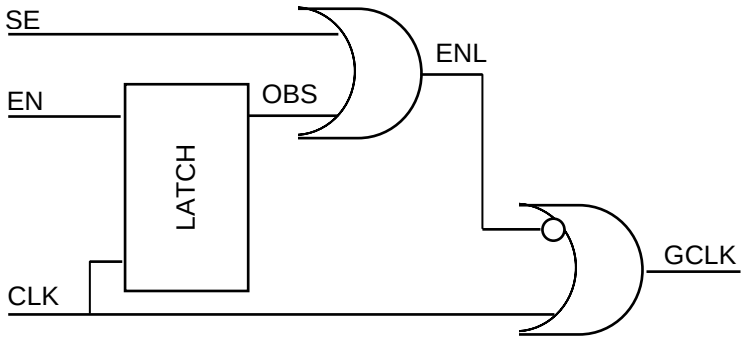


Figure 5.61. Logic Symbol of Clock Gating cell w/ Latched Neg Edge Control Post

Table 5.121. CGLNPS Truth Table

SE	EN	CLK	GCLK
1	X	0	0
1	X	1	1
0	0	0	!OBS
0	0	1	1
0	1	0	0
0	1	1	1

Table 5.122. Clock Gating cell w/ Latched Neg Edge Control Post Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
CGLNPSX2	2 x Csl	79	1214	6	6.3536
CGLNPSX4	4 x Csl	85	1712	11	6.861888
CGLNPSX8	8 x Csl	92	2757	27	7.878464
CGLNPSX16	16 x Csl	88	5581	45	11.944768

Clock Gating cell w/ Latched Pos Edge Control Pre: CGLPPRX2, CGLPPRX8

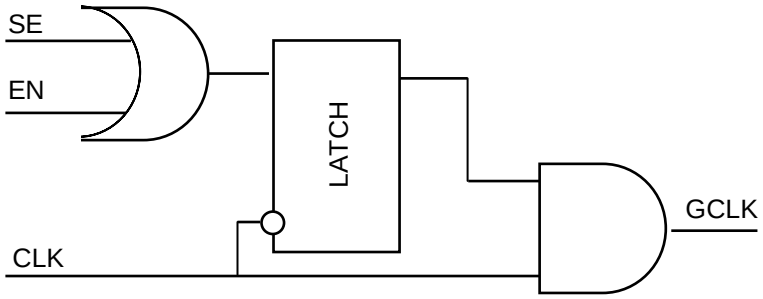


Figure 5.62. Logic Symbol of Clock Gating cell w/ Latched Pos Edge Control Pre

Table 5.123. CGLPPR Truth Table

SE	EN	CLK	ENL
1	X	0	1
X	1	0	1
0	0	0	1
X	X	1	No change

ENL	CLK	GCLK
0	0	0
0	1	0
1	0	0
1	1	1

Table 5.124. Clock Gating cell w/ Latched Pos Edge Control Pre Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
CGLPPRX2	2 x Csl	82	1467	7	5.845312
CGLPPRX8	8 x Csl	209	2968	26	7.370176

Clock Gating cell w/ Latched Neg Edge Control Pre: CGLNPRX2, CGLNPRX8

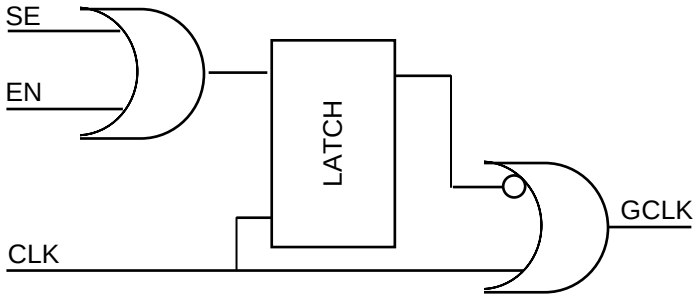


Figure 5.63. Logic Symbol of Clock Gating cell w/ Latched Neg Edge Control Pre

Table 5.125. CGLNPR Truth Table

SE	EN	CLK	ENL
1	X	1	1
X	1	1	1
0	0	1	1
X	X	0	No change

ENL	CLK	GCLK
0	0	1
0	1	1
1	0	0
1	1	1

Table 5.126. Clock Gating cell w/ Latched Neg Edge Control Pre Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
CGLNPRX2	2 x Csl	82	1385	7	6.3536
CGLNPRX8	8 x Csl	260	2939	88348	7.878464

Non-Inverting Delay Line: DELLN1X2, DELLN2X2, DELLN3X2

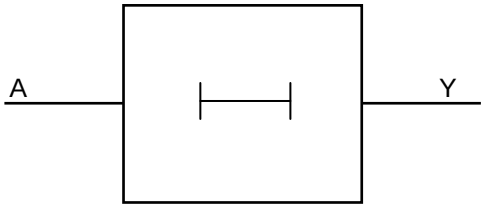


Figure 5.64. Logic Symbol of Non-Inverting Delay Line

Table 5.127. DELLN Truth Table

A	Y
X	A

Table 5.128. Non-Inverting Delay Line Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
DELLN1X2	2 x Csl	137	657	9	5.08288
DELLN2X2	2 x Csl	180	727	11	6.607744
DELLN3X2	2 x Csl	280	867	14	9.657472

Pass Gate: PGX1, PGX2, PGX4

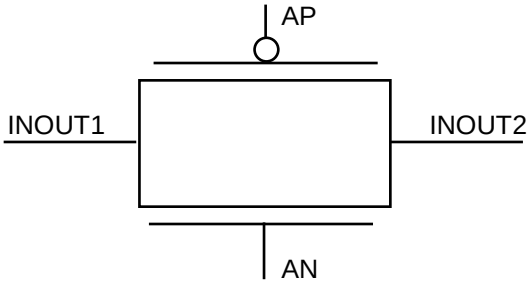


Figure 5.65. Logic Symbol of Pass Gate

Table 5.129. PG Truth Table

INOUT1	AN	AP	INOUT2	Notes
X	0	1	Z	
X	X	0	X	Not Allowed
X	1	X	X	Not Allowed
X	1	0	INQ1	

Table 5.130. Pass Gate Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
PGX1	1 x Csl	25	1.5	9	1.27072
PGX2	2 x Csl	17	3.6	12	1.524864
PGX4	4 x Csl	12	7.2	15	2.033152

Bi-directional Switch w/ Active Low Enable: BSLEX1, BSLEX2, BSLEX4

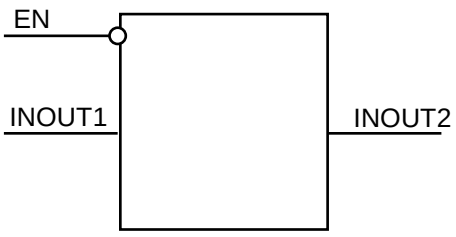


Figure 5.66. Logic Symbol of Bi-directional Switch w/ Active Low Enable

Table 5.131. BSLE Truth Table

INOUT1	EN	INOUT2
X	0	INOUT1
X	1	Z

Table 5.132. Bi-directional Switch w/ Active Low Enable Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
BSLEX1	1 x Csl	28	44	9	1.779008
BSLEX2	2 x Csl	32	132	10	2.033152
BSLEX4	4 x Csl	45	514	13	2.54144

Hold 0 Isolation Cell (Logic AND): ISOLANDX1, ISOLANDX2, ISOLANDX4, ISOLANDX8

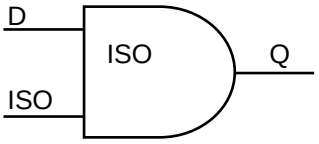


Figure 5.67. Logic Symbol of Hold 1 Isolation Cell (Logic AND)

Table 5.133. ISOLAND Truth Table

D	ISO	Q
0	X	0
X	0	0
1	1	1

Table 5.134. Hold 0 Isolation Cell (Logic AND) Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
ISOLANDX1	1 x Csl	75	376	3	2.54144
ISOLANDX2	2 x Csl	63	591	5	2.795584
ISOLANDX4	4 x Csl	65	1082	10	3.303872
ISOLANDX8	8 x Csl	73	2079	28	4.320448

Hold 0 Isolation Cell (Logic AND), Always On **:** ISOLANDAOX1, ISOLANDAOX2, ISOLANDAOX4, ISOLANDAOX8

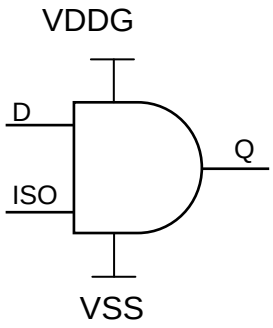


Figure 5.68.Logic Symbol of Hold 0 Isolation Cell (Logic AND),Always On

Table 5.135. ISOLANDAO Truth Table

D	ISO	Q
0	X	0
X	0	0
1	1	1

Table 5.136. Hold 0 Isolation Cell (Logic AND), Always On Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
ISOLANDAOX1	1 x Csl	70	1333	5	5.591168
ISOLANDAOX2	2 x Csl	63	1436	7	5.845312
ISOLANDAOX4	4 x Csl	66	1717	11	6.861888
ISOLANDAOX8	8 x Csl	75	2201	25	8.89504

Hold 1 Isolation Cell (Logic OR): ISOLORX1, ISOLORX2, ISOLORX4, ISOLORX8

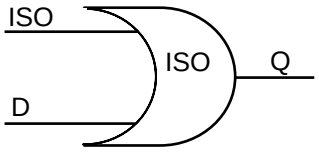


Figure 5.69. Logic Symbol of Hold 0 Isolation Cell (Logic OR)

Table 5.137. ISOLOR Truth Table

D	ISO	Q
0	0	0
X	1	1
1	X	1

Table 5.138. Hold 1 Isolation Cell (Logic OR) Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
ISOLORX1	1 x Csl	64	302	3	2.033152
ISOLORX2	2 x Csl	50	551	5	2.287296
ISOLORX4	4 x Csl	56	1050	9	2.795584
ISOLORX8	8 x Csl	46	2116	21	4.320448

Hold 1 Isolation Cell (Logic OR), Always On : ISOLORAOX1, ISOLORAOX2, ISOLORAOX4, ISOLORAOX8

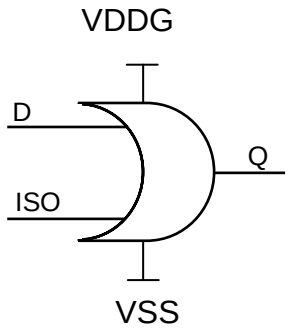


Figure 5.70. Logic Symbol of Hold 0 Isolation Cell (Logic OR), Always On

Table 5.139. ISOLORAO Truth Table

D	ISO	Q
0	0	0
X	1	1
1	X	1

Table 5.140. Hold 1 Isolation Cell (Logic OR), Always On Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
ISOLORAOX1	1 x Csl	72	247	4	5.845312
ISOLORAOX2	2 x Csl	70	374	6	6.3536
ISOLORAOX4	4 x Csl	68	627	10	7.370176
ISOLORAOX8	8 x Csl	72	1158	19	9.911616

Low to High Level Shifter: LSUPX1, LSUPX2, LSUPX4, LSUPX8

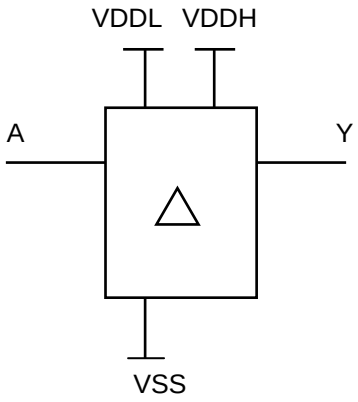


Figure 5.71. Logic Symbol of Low to High Level Shifter

Table 5.141. LSUP Truth Table

A	Y
0	0
1	1

Table 5.142. Low to High Level Shifter Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSUPX1	1 x Csl	140	339	11	7.116032
LSUPX2	2 x Csl	124	1030	14	7.62432
LSUPX4	4 x Csl	115	1700	17	8.640896
LSUPX8	8 x Csl	116	2786	25	11.182336

High to Low Level Shifter: LSDNX1, LSDNX2, LSDNX4, LSDNX8

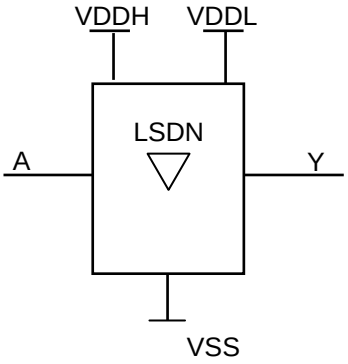


Figure 5.72. Logic Symbol of High to Low Level Shifter

Table 5.143. LSDN Truth Table

A	Y
0	0
X	1
1	1

Table 5.144. High to Low Level Shifter Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSDNX1	1 x Csl	140	858	4	7.116032
LSDNX2	2 x Csl	127	1044	5	7.116032
LSDNX4	4 x Csl	131	1481	7	7.116032
LSDNX8	8 x Csl	120	2941	10	8.640896

High to Low Level Shifter, single supply: LSDNSSX1, LSDNSSX2, LSDNSSX4, LSDNSSX8

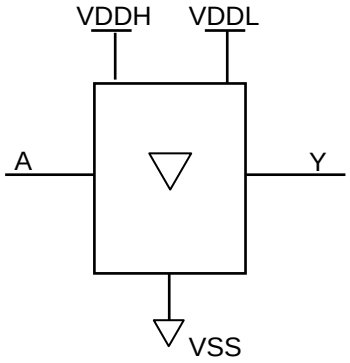


Figure 5.73. Logic Symbol of High to Low Level Shifter

Table 5.145. LSDNSS Truth Table

A	Y
0	0
X	1
1	1

Table 5.146. High to Low Level Shifter,Single supply Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSDNSSX1	1 x Csl	100	1134	1	1.779008
LSDNSSX2	2 x Csl	91	1167	3	2.033152
LSDNSSX4	4 x Csl	96	1232	5	2.54144
LSDNSSX8	8 x Csl	115	1407	9	4.320448

High to Low Level Shifter/ High Activ Enable, single supply: LSDNENSSX1, LSDNENSSX2, LSDNENSSX4, LSDNENSSX8

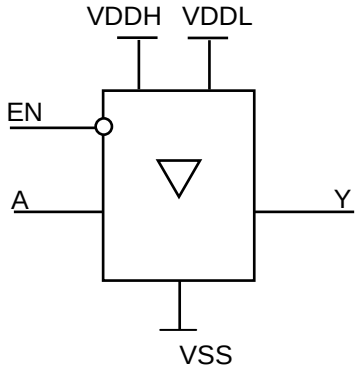


Figure 5.74. Logic Symbol of High to Low Level Shifter/High Activ Enable, single supply

Table 5.147. LSDNENSS Truth Table

A	Y
0	0
X	1
1	1

Table 5.148. High to Low Level Shifter/High Activ Enable,Single supply Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSDNENSSX1	1 x Csl	143	1207	4	4.066304
LSDNENSSX2	2 x Csl	120	1236	5	4.828736
LSDNENSSX4	4 x Csl	115	1297	7	5.337024
LSDNENSSX8	8 x Csl	117	1444	9	7.116032

High to Low Level Shifter/ High Activ Enable, Clamp Low , Single supply: LSDNENCLSSX1, LSDNENCLSSX2, LSDNENCLSSX4, LSDNENCLSSX8

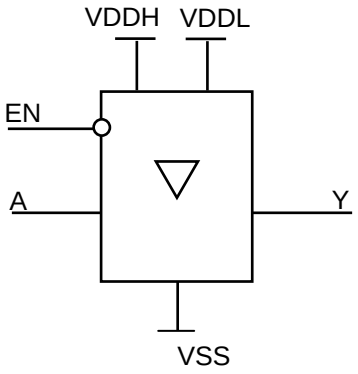


Figure 5.75. Logic Symbol of High to Low Level Shifter/High Activ Enable,Clamp Low, Single Supply

Table 5.149. LSDENNCLSS Truth Table

A	Y
0	0
X	1
1	1

Table 5.150. High to Low Level Shifter/High Activ Enable,Single supply Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSDNENCLSSX1	1 x Csl	186	1112	2	2.287296
LSDNENCLSSX2	2 x Csl	125	1180	5	2.54144
LSDNENCLSSX4	4 x Csl	145	1246	7	3.049728
LSDNENCLSSX8	8 x Csl	173	1378	11	4.066304

Low to High Level Shifter/ Active Low Enable: LSUPENX1, LSUPENX2, LSUPENX4, LSUPENX8

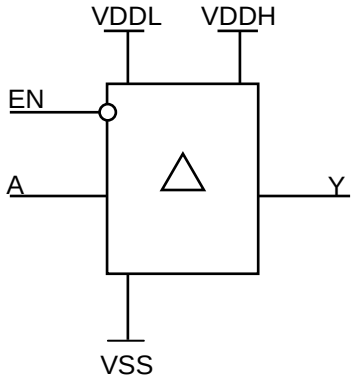


Figure 5.76. Logic Symbol of Low to High Level Shifter/Active Low Enable

Table 5.151. LSUPEN Truth Table

A	EN	Y
X	1	1
0	0	0
1	0	1

Table 5.152. Low to High Level Shifter/Active Low Enable Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSUPENX1	1 x Csl	117	520	6	7.62432
LSUPENX2	2 x Csl	167	1248	11	10.16576
LSUPENX4	4 x Csl	145	1676	14	12.198912
LSUPENX8	8 x Csl	159	2798	22	16.773504

High to Low Level Shifter/ Active Low Enable: LSDNENX1, LSDNENX2, LSDNENX4, LSDNENX8

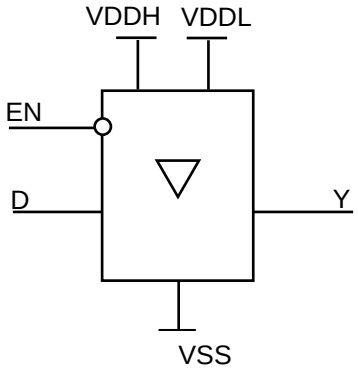


Figure 5.77. Logic Symbol of High to Low Level Shifter/Active Low Enable

Table 5.153. LSDNEN Truth Table

A	EN	Y
X	1	1
0	0	0
1	0	1

Table 5.154. High to Low Level Shifter/ Active Low Enable Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSDNENX1	1 x Csl	128	57	1	7.116032
LSDNENX2	2 x Csl	143	128	4	7.62432
LSDNENX4	4 x Csl	136	206	6	8.640896
LSDNENX8	8 x Csl	133	364	10	11.182336

Low to High Level Shifter/ Active Low Enable, Clamp Low: LSUPENCLX1, LSUPENCLX2, LSUPENCLX4, LSUPENCLX8

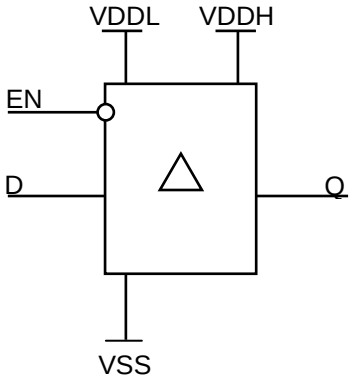


Figure 5.78. Logic Symbol of Low to High Level Shifter/Active Low Enable, Clamp Low

Table 5.155. LSUPENCL Truth Table

A	EN	Y
X	1	0
0	0	0
1	0	1

Table 5.156. Low to High Level Shifter/Active Low Enable Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSUPENCLX1	1 x Csl	122	633	5	7.116032
LSUPENCLX2	2 x Csl	105	953	6	7.116032
LSUPENCLX4	4 x Csl	120	1550	11	10.16576
LSUPENCLX8	8 x Csl	78	4477	22	15.756928

High to Low Level Shifter/ Active Low Enable, Clamp Low: LSDNENCLX1, LSDNENCLX2, LSDNENCLX4, LSDNENCLX8

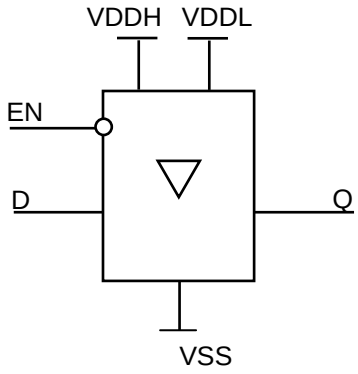


Figure 5.79. Logic Symbol of High to Low Level Shifter/Active Low Enable, Clapm Low

Table 5.157. LSDNENCL Truth Table

A	EN	Y
X	1	0
0	0	0
1	0	1

Table 5.158. High to Low Level Shifter/ Active Low Enable Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
LSDNENCLX1	1 x Csl	163	35	1	7.116032
LSDNENCLX2	2 x Csl	132	127	5	7.62432
LSDNENCLX4	4 x Csl	123	201	7	8.640896
LSDNENCLX8	8 x Csl	119	369	9	11.182336

Pos Edge Retention DFF: RDFFX1, RDFFX2

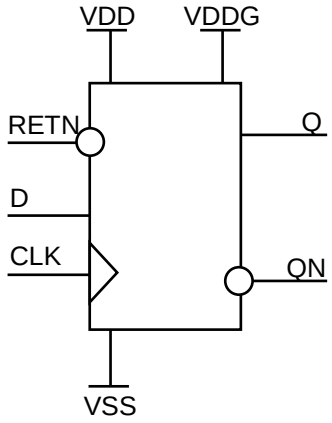


Figure 5.80. Logic Symbol of Pos Edge Retention DFF

Table 5.159. RDFF Transition Table

D	CLK	RETN	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	Rise	1	Q2[n]	0	1	Normal mode write 0
1	Rise	1	Q2[n]	1	0	Normal mode write 1
X	Rise	0	Q[n]	Q[n]	QN[n]	Retention mode
X	Fall	X	Q2[n]	Q[n]	QN[n]	
X	0	X	Q2[n]	Q[n]	QN[n]	
X	1	X	Q2[n]	Q[n]	QN[n]	

Table 5.160. Pos Edge Retention DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um^2)
RDFFX1	1 x Csl	Q	130	1324	13	13.97792
		QN	150			
RDFFX2	2 x Csl	Q	121	1641	15	14.486208
		QN	158			

Scan Pos Edge Retention DFF: RSDFFX1, RSDFFX2

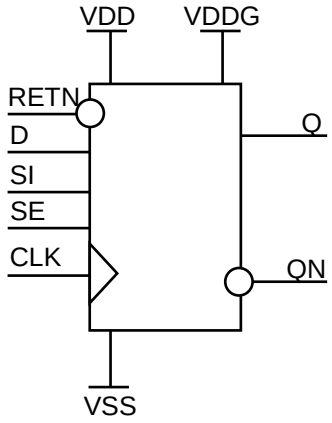


Figure 5.81. Logic Symbol of Scan Pos Edge Retention DFF

Table 5.161. RSDFF Transition Table

D	CLK	SI	SE	RETN	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	Rise	0	1	1	Q2[n]	0	1	Normal mode write 0
X	Rise	1	1	1	Q2[n]	1	0	Normal mode write 1
0	Rise	X	0	1	Q2[n]	0	1	Scan mode write 0
1	Rise	X	0	1	Q2[n]	1	0	Scan mode write 1
X	Rise	X	X	0	Q[n]	Q[n]	QN[n]	Retention mode
X	Fall	X	X	X	Q2[n]	Q[n]	QN[n]	
X	0	X	X	X	Q2[n]	Q[n]	QN[n]	
X	1	X	X	X	Q2[n]	Q[n]	QN[n]	

Table 5.162. Scan Pos Edge Retention DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um^2)
RSDFFX1	1 x Csl	Q	120	1565	16	17.027648
		QN	150			
RSDFFX2	2 x Csl	Q	110	1881	18	17.535936
		QN	140			

Scan Pos Edge Retention DFF,w/Async Low Activ Reset: RSDFFARX1, RSDFFARX2

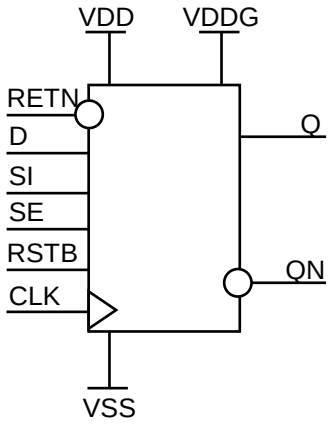


Figure 5.82. Logic Symbol of Scan Pos Edge Retention DFF,w/Async Low Activ Reset

Table 5.163. RSDFFAR Transition Table

RETN	RSTB	CLK	D	SI	SE	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
1	1	Rise	X	0	1	Q2[n]	0	1	Scan mode write 0
1	1	Rise	X	1	1	Q2[n]	1	0	Scan mode write 1
1	1	Rise	0	X	0	Q2[n]	0	1	Normal mode write 0
1	1	Rise	1	X	0	Q2[n]	1	0	Normal mode write 1
0	1	Rise	X	X	X	Q[n]	Q[n]	QN[n]	Retention mode
X	1	Fall	X	X	X	Q2[n]	Q[n]	QN[n]	
X	1	0	X	X	X	Q2[n]	Q[n]	QN[n]	
X	1	1	X	X	X	Q2[n]	Q[n]	QN[n]	
X	0	X	X	X	X	0	0	1	Reset

Table 5.164. Scan Pos Edge Retention DFF,w/Async Low Activ Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um^2)
RSDFFARX1	1 x Csl	Q	134	2392	14	18.044224
		QN	153			
RSDFFARX2	2 x Csl	Q	115	3007	15	18.552512

Neg Edge Retention DFF: RDFFNX1, RDFFNX2

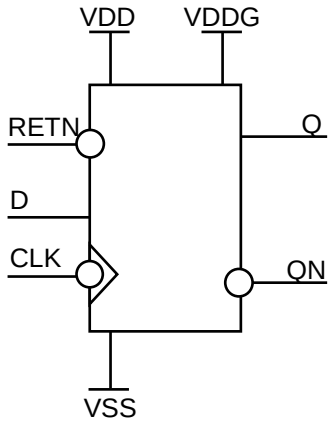


Figure 5.83. Logic Symbol of Pos Edge Retention DFF

Table 5.165. RDFFN Transition Table

D	CLK	RETN	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	Fall	1	Q2[n]	0	1	Normal mode write 0
1	Fall	1	Q2[n]	1	0	Normal mode write 1
X	Fall	0	Q[n]	Q[n]	QN[n]	Retention mode
X	Rise	X	Q2[n]	Q[n]	QN[n]	
X	0	X	Q2[n]	Q[n]	QN[n]	
X	1	X	Q2[n]	Q[n]	QN[n]	

Table 5.166. Neg Edge Retention DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um^2)
RDFFNX1	1 x Csl	Q	127	1328	14	13.97792
		QN	154			
RDFFNX2	2 x Csl	Q	116	1645	15	14.486208
		QN	153			

Scan Neg Edge Retention DFF: RSDFFNX1, RSDFFNX2

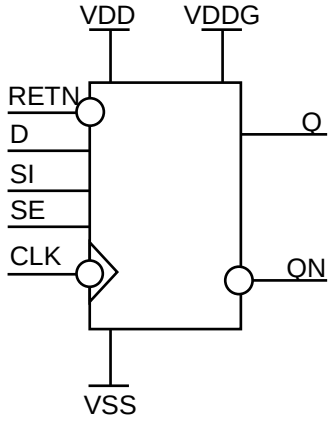


Figure 5.84. Logic Symbol of Scan Neg Edge Retention DFF

Table 5.167. RSDFFN Transition Table

RETN	D	CLK	SI	SE	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
1	X	Fall	0	1	Q2[n]	0	1	Scan mode write 0
1	X	Fall	1	1	Q2[n]	1	0	Scan mode write 1
1	0	Fall	X	0	Q2[n]	0	1	Normal mode write 0
1	1	Fall	X	0	Q2[n]	1	0	Normal mode write 1
0	X	Fall	X	X	Q[n]	Q[n]	QN[n]	Retention mode
X	X	Rise	X	X	Q2[n]	Q[n]	QN[n]	
X	X	0	X	X	Q2[n]	Q[n]	QN[n]	
X	X	1	X	X	Q2[n]	Q[n]	QN[n]	

Table 5.168. Scan Neg Edge Retention DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um^2)
RSDFFNX1	1 x Csl	Q	91	1536	15	17.027648
		QN	110			
RSDFFNX2	2 x Csl	Q	116	1881	18	17.535936
		QN	123			

Scan Neg Edge Retention DFF,w/Async Low Activ Reset: RSDFFNARX1, RSDFFNARX2

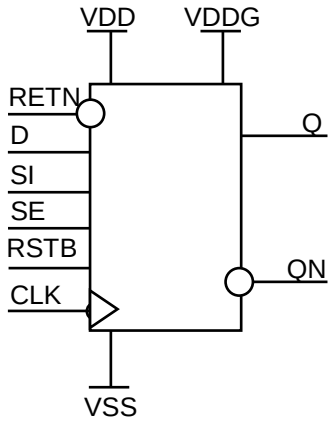


Figure 5.85. Logic Symbol of Scan Neg Edge Retention DFF,w/Async low Activ Reset

Table 5.169. RSDFFNAR Transition Table

RETN	RSTB	D	CLK	SI	SE	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
1	1	X	Fall	0	1	Q2[n]	0	1	Scan mode write 0
1	1	X	Fall	1	1	Q2[n]	1	0	Scan mode write 1
1	1	0	Fall	X	0	Q2[n]	0	1	Normal mode write 0
1	1	1	Fall	X	0	Q2[n]	1	0	Normal mode write 1
0	1	X	Fall	X	X	Q[n]	Q[n]	QN[n]	Retention mode
X	1	X	Rise	X	X	Q2[n]	Q[n]	QN[n]	
X	1	X	0	X	X	Q2[n]	Q[n]	QN[n]	
X	1	X	1	X	X	Q2[n]	Q[n]	QN[n]	
X	0	X	X	X	X	0	0	1	Reset

Table 5.170. Scan Neg Edge Retention DFF Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um^2)
RSDFFNARX1	1 x Csl	Q	128	2392	15	18.044224
		QN	119			
RSDFFNARX2	2 x Csl	Q	121	2714	17	18.552512
		QN	158			

Pos Edge DFF SR: RDFFSRX1, RDFFSRX2

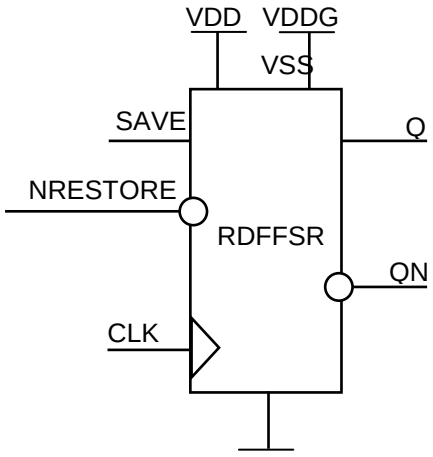


Figure 5.86. Logic Symbol of Pos Edge DFF SR

Table 5.171. RDFFSR Transition Table

SAVE	NRESTORE	D	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	1	0	Rise	Q2[n]	0	1	Normal mode write 0
0	1	1	Rise	Q2[n]	1	0	Normal mode write 1
0	X	X	Fall	Q2[n]	Q[n]	QN[n]	
0	X	X	0	Q2[n]	Q[n]	QN[n]	
0	1	X	1	Q2[n]	Q[n]	QN[n]	
1	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
0	0	X	1	Q2[n]	Q2[n]	!Q2[n]	Restore mode
0	0	X	0	Q2[n]	Q[n]	QN[n]	

Table 5.172. Pos Edge DFF SR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFSRX1	1 x Csl	QN	124	1425	9	13.215488
RDFFSRX2	2 x Csl	QN	110	1746	13	13.723776

Pos Edge Retention DFF, w/ Async Low-Active Reset: RDFFARX1, RDFFARX2

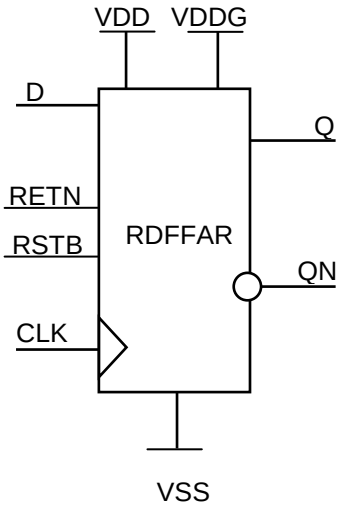


Figure 5.87. Logic Symbol of Pos Edge Retention DFF, w/ Async Low-Active Reset

Table 5.173. RDFFAR Transition Table

CLK	D	RETN	RSTB	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
Rise	0	1	1	Q2[n]	0	1	Normal mode write 0
Rise	1	1	1	Q2[n]	1	0	Normal mode write 1
Rise	X	0	1	Q[n]	Q[n]	QN[n]	Retention mode
Fall	X	X	1	Q2[n]	Q[n]	QN[n]	
0	X	X	1	Q2[n]	Q[n]	QN[n]	
1	X	X	1	Q2[n]	Q[n]	QN[n]	
X	X	X	0	0	0	1	Reset

Table 5.174. Pos Edge DFF SR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF	Area

	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFARX1	1 x Csl	QN	153	2140	10	14.994496
RDFFARX2	2 x Csl	QN	159	2462	14	15.502784

Neg Edge Retention DFF,w/Async Low Activ Reset: RDFFNARX1, RDFFNARX2

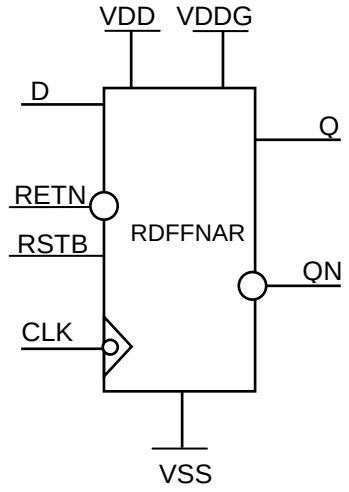


Figure 5.88. Logic Symbol of Pos Edge DFF SR

Table 5.175.RDFFNAR Transition Table

CLK	D	RETN	RSTB	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
Fall	0	1	1	Q2[n]	0	1	Normal mode write 0
Fall	1	1	1	Q2[n]	1	0	Normal mode write 1
Fall	X	0	1	Q[n]	Q[n]	QN[n]	Retention mode
Rise	X	X	1	Q2[n]	Q[n]	QN[n]	
0	X	X	1	Q2[n]	Q[n]	QN[n]	
1	X	X	1	Q2[n]	Q[n]	QN[n]	
X	X	X	0	0	0	1	Reset

Table 5.176. Pos Edge DFF SR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFNARX1	1 x Csl	QN	158	2145	11	14.994496
RDFFNARX2	2 x Csl	QN	162	2467	12	15.502784

Pos Edge DFF SR, w/ Async Low-Active Set: RDFFSRASX1, RDFFSRASX2

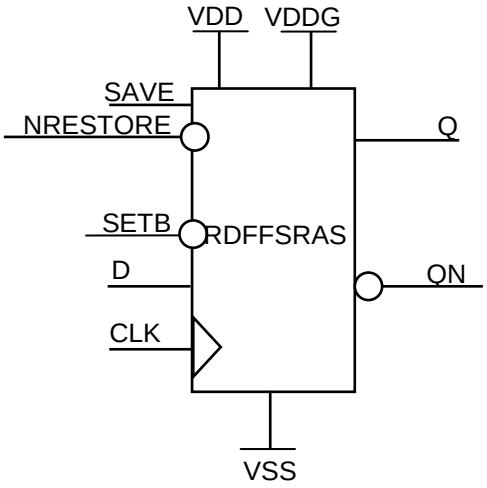


Figure 5.89. Logic Symbol of Pos Edge DFF SR, w/ Async Low-Active Set

Table 5.177. RDFFSRAS Transition Table

SAVE	NRESTORE	SETB	CLK	D	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	X	0	X	X	Q2[n]	1	0	SETB mode
0	1	1	Rise	0	Q2[n]	0	1	Normal made write 0
0	1	1	Rise	1	Q2[n]	1	0	Normal mode write 1
0	X	1	Fall	X	Q2[n]	Q[n]	QN[n]	
0	X	1	0	X	Q2[n]	Q[n]	QN[n]	
0	1	1	1	X	Q2[n]	Q[n]	QN[n]	
1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
0	0	1	1	X	Q2[n]	Q2[n]	!Q2[n]	Restore mode
0	0	1	0	X	Q2[n]	Q[n]	QN[n]	

Table 5.178. Pos Edge DFF SR, w/ Async Low-Active Set

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFSRASX1	1 x Csl	QN	126	1450	11	14.232064
RDFFSRASX2	2 x Csl	QN	141	1769	14	14.740352

Pos Edge DFF SR, w/ Async Low-Active Reset: RDFFSRARX1, RDFFSRARX2

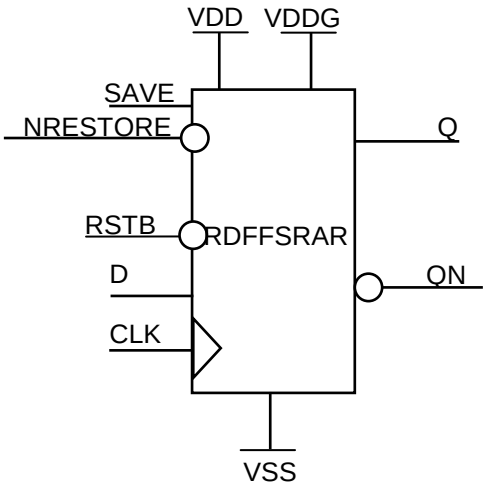


Figure 5.90. Logic Symbol of Pos Edge DFF SR, w/ Async Low-Active Reset

Table 5.179. RDFFSRAR Transition Table

SAVE	NRESTORE	RSTB	CLK	D	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	X	0	X	X	Q2[n]	0	1	RSTB mode
0	1	1	Rise	0	Q2[n]	0	1	Normal made write 0
0	1	1	Rise	1	Q2[n]	1	0	Normal mode write 1
0	X	1	Fall	X	Q2[n]	Q[n]	QN[n]	
0	X	1	0	X	Q2[n]	Q[n]	QN[n]	
0	1	1	1	X	Q2[n]	Q[n]	QN[n]	
1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
0	0	1	1	X	Q2[n]	Q2[n]	!Q2[n]	Restore mode
0	0	1	0	X	Q2[n]	Q[n]	QN[n]	

Table 5.180. Pos Edge DFF SR, w/ Async Low-Active Reset

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFSRARX1	1 x Csl	QN	143	1481	13	13.723776
RDFFSRARX2	2 x Csl	QN	131	1731	17	14.232064

Pos Edge DFF SR, w/ Async Low-Active Set & Reset: RDFFSRASRX1, RDFFSRASRX2

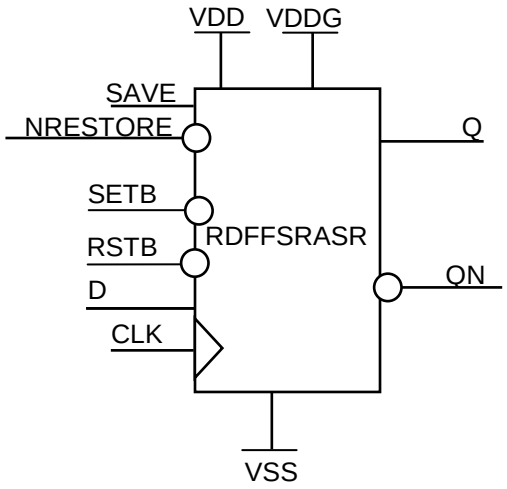


Figure 5.91. Logic Symbol of Pos Edge DFF SR, w/ Async Low-Active Set & Reset

Table 5.181. RDFFSRASR Transition Table

SAVE	NRESTORE	SETB	RSTB	D	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	X	X	0	X	X	Q2[n]	0	1	RSTB mode
0	X	0	1	X	X	Q2[n]	1	0	SETB mode
0	1	1	1	0	Rise	Q2[n]	0	1	Normal mode write 0
0	1	1	1	1	Rise	Q2[n]	1	0	Normal mode write 1
0	X	1	1	X	Fall	Q2[n]	Q[n]	QN[n]	
0	X	1	1	X	0	Q2[n]	Q[n]	QN[n]	
0	1	1	1	X	1	Q2[n]	Q[n]	QN[n]	
1	X	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
0	0	1	1	X	1	Q2[n]	Q2[n]	!Q2[n]	Restore mode
0	0	1	1	X	0	Q2[n]	Q[n]	QN[n]	

Table 5.182. Pos Edge DFF SR, w/ Async Low-Active Set & Reset

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFSRASRX1	1 x Csl	QN	124	1508	11	14.232064
RDFFSRASRX2	2 x Csl	QN	136	1789	16	14.740352

Pos Edge DFF SR, w/ Sync Low-Active Set & Reset: RDFFSRSSRX1, RDFFSRSSRX2

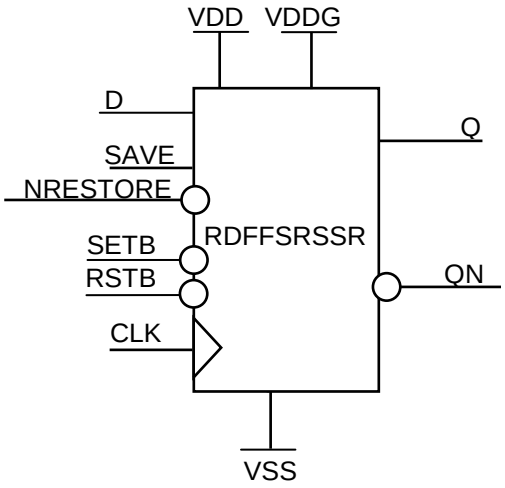


Figure 5.92. Logic Symbol of Pos Edge DFF SR, w/ Sync Low-Active Set & Reset

Table 5.183. RDFFSRSSR Transition Table

D	SAVE	NRESTORE	SETB	RSTB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	0	X	X	0	Rise	Q2[n]	0	1	RSTB mode
X	0	X	0	1	Rise	Q2[n]	1	0	SETB mode
0	0	1	1	1	Rise	Q2[n]	0	1	Normal mode write 0
1	0	1	1	1	Rise	Q2[n]	1	0	Normal mode write 1
X	0	X	X	X	Fall	Q2[n]	Q[n]	QN[n]	
X	0	X	X	X	0	Q2[n]	Q[n]	QN[n]	
X	0	1	X	X	1	Q2[n]	Q[n]	QN[n]	
X	1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	0	0	1	1	1	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	0	0	1	1	0	Q2[n]	Q[n]	QN[n]	

Table 5.184. Pos Edge DFF SR, w/ Sync Low-Active Set & Reset

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFSRSSRX1	1 x Csl	QN	160	24868	75	15.24864
RDFFSRSSRX2	2 x Csl	QN	163	25186	72	15.756928

Neg Edge DFF SR: RDFFNSRX1, RDFFNSRX2

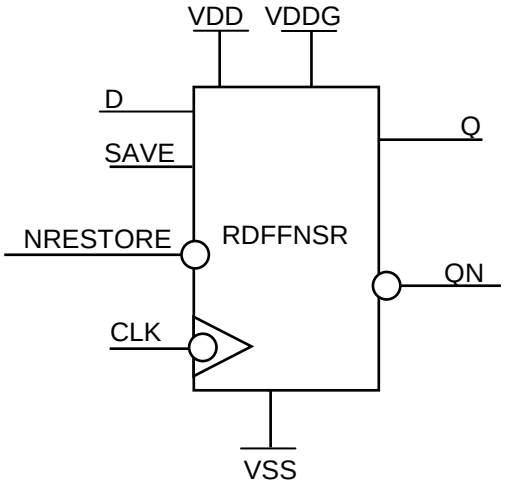


Figure 5.93. Logic Symbol of Neg Edge DFF SR

Table 5.185. RDFFNSR Transition Table

D	SAVE	NRESTORE	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	0	1	Fall	Q2[n]	0	1	Normal mode write 0
1	0	1	Fall	Q2[n]	1	0	Normal mode write 1
X	0	X	Rise	Q2[n]	Q[n]	QN[n]	
X	0	X	1	Q2[n]	Q[n]	QN[n]	
X	0	1	0	Q2[n]	Q[n]	QN[n]	
X	1	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	0	0	0	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	0	0	1	Q2[n]	Q[n]	QN[n]	

Table 5.186. Neg Edge DFF SR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFNSRX1	1 x Csl	QN	121	1394	16	13.215488
RDFFNSRX2	2 x Csl	QN	129	1748	19	13.723776

Neg Edge DFF SR, w/ Async Low-Active Set: RDFFNSRASX1, RDFFNSRASX2

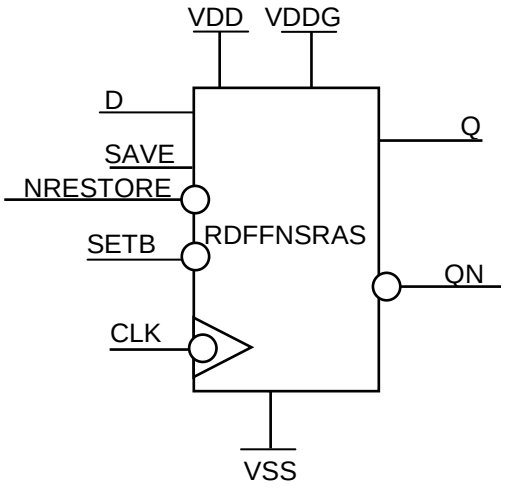


Figure 5.94. Logic Symbol of Edge DFF SR, w/ Async Low-Active Set

Table 5.187. RDFFNSRAS Transition Table

D	SAVE	NRESTORE	SETB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Notes
X	0	X	0	X	Q2[n]	1	0	SETB mode
0	0	1	1	Fall	Q2[n]	0	1	Normal mode 0
1	0	1	1	Fall	Q2[n]	1	0	Normal mode 1
X	0	X	1	Rise	Q2[n]	Q[n]	QN[n]	
X	0	X	1	1	Q2[n]	Q[n]	QN[n]	
X	0	1	1	0	Q2[n]	Q[n]	QN[n]	
X	1	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	0	0	1	0	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	0	0	1	1	Q2[n]	Q[n]	QN[n]	

Table 5.188. Neg Edge DFF SR, w/ Async Low-Active Set Electrical Parameters and Area

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFNSRASX1	1 x Csl	QN	140	1454	15	14.232064
RDFFNSRASX2	2 x Csl	QN	125	1774	16	14.740352

Neg Edge DFF SR, w/ Async Low-Active Reset: RDFFNSRARX1, RDFFNSRARX2

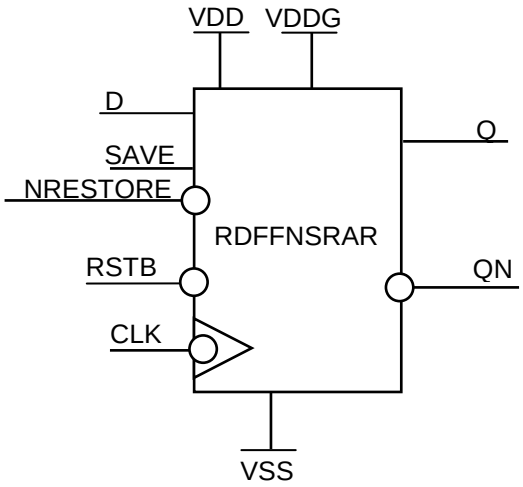


Figure 5.95. Logic Symbol of Neg Edge DFF SR, w/ Async Low-Active Reset

Table 5.189. RDFFNSRAR Transition Table

D	SAVE	NRESTORE	RSTB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Notes
X	0	X	0	X	Q2[n]	0	1	RSTB mode
0	0	1	1	Fall	Q2[n]	0	1	Normal mode write 0
1	0	1	1	Fall	Q2[n]	1	0	Normal mode write 1
X	0	X	1	Rise	Q2[n]	Q[n]	QN[n]	
X	0	X	1	1	Q2[n]	Q[n]	QN[n]	
X	0	1	1	0	Q2[n]	Q[n]	QN[n]	Save mode
X	1	X	X	X	Q[n]	Q[n]	QN[n]	Restore mode
X	0	0	1	0	Q2[n]	Q2[n]	!Q2[n]	
X	0	0	1	1	Q2[n]	Q[n]	QN[n]	

Table 5.190. Pos Edge DFF SR, w/ Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFNSRARX1	1 x Csl	QN	142	1427	13	13.723776
RDFFNSRARX2	2 x Csl	QN	129	1735	15	14.232064

Neg Edge DFF SR, w/ Async Low-Active Set & Reset: RDFFNSRASRX1, RDFFNSRASRX2

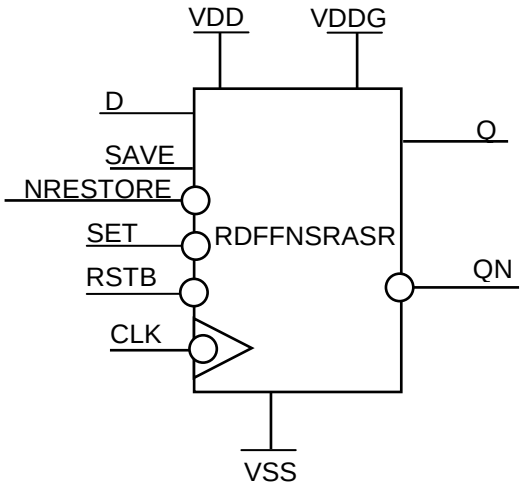


Figure 5.96. Logic Symbol of Neg Edge DFF SR, w/ Async Low-Active Set & Reset

Table 5.191. RDFFNSRASR Transition Table

D	SAVE	NRESTORE	SETB	RSTB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	0	X	X	0	X	Q2[n]	0	1	RSTB mode
X	0	X	0	1	X	Q2[n]	1	0	SETB mode
0	0	1	1	1	Fall	Q2[n]	0	1	Normal mode write 0
1	0	1	1	1	Fall	Q2[n]	1	0	Normal mode write 1
X	0	X	1	1	Rise	Q2[n]	Q[n]	QN[n]	
X	0	X	1	1	1	Q2[n]	Q[n]	QN[n]	
X	0	1	1	1	0	Q2[n]	Q[n]	QN[n]	
X	1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	0	0	1	1	0	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	0	0	1	1	1	Q2[n]	Q[n]	QN[n]	

Table 5.192. Neg Edge DFF SR, w/ Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFNSRASRX1	1 x Csl	QN	131	1504	15	14.232064
RDFFNSRASRX2	2 x Csl	QN	116	1785	16	14.740352

Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out: RDFFNSRASRQX1, RDFFNSRASRQX2

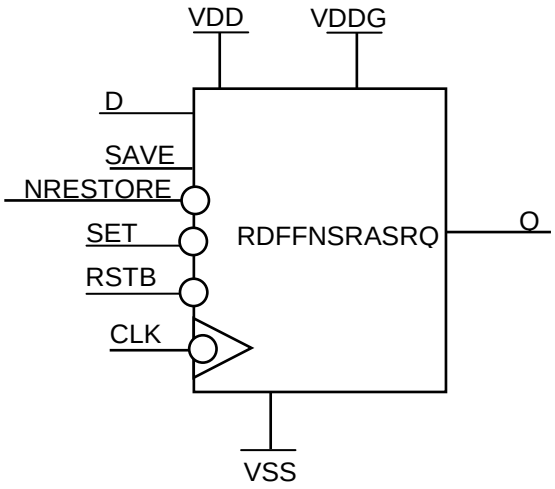


Figure 5.97. Logic Symbol of Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out

Table 5.193.RDFFNSRASRQ Transition Table

D	SAVE	NRESTORE	SETB	RSTB	CLK	Q2[n+1]	Q[n+1]	Mode
X	0	X	X	0	X	Q2[n]	0	RSTB mode
X	0	X	0	1	X	Q2[n]	1	SETB mode
0	0	1	1	1	Fall	Q2[n]	0	Normal mode write 0
1	0	1	1	1	Fall	Q2[n]	1	Normal mode write 1
X	0	X	1	1	Rise	Q2[n]	Q[n]	
X	0	X	1	1	1	Q2[n]	Q[n]	
X	0	1	1	1	0	Q2[n]	Q[n]	
X	1	X	X	X	X	Q[n]	Q[n]	Save mode
X	0	0	1	1	0	Q2[n]	Q2[n]	Restore mode
X	0	0	1	1	1	Q2[n]	Q[n]	

Table 5.194. Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFNSRASRQX1	1 x Csl	Q	150	1437	10	13.97792
RDFFNSRASRXQ2	2 x Csl	Q	178	1628	12	14.232064

Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out: RDFFNSRASRNX1, RDFFNSRASRNX2

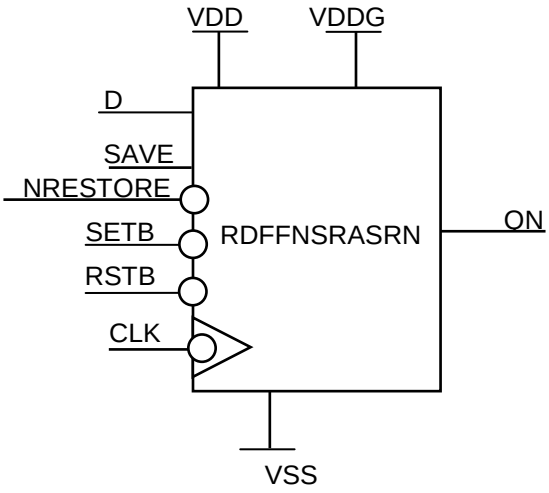


Figure 5.98. Logic Symbol of Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out

Table 5.195. RDFFNSRASRN Transition Table

D	SAVE	NRESTORE	SETB	RSTB	CLK	Q2[n+1]	QN[n+1]	Mode
X	0	X	X	0	X	Q2[n]	0	RSTB mode
X	0	X	0	1	X	Q2[n]	1	SETB mode
0	0	1	1	1	Fall	Q2[n]	1	Normal mode write 0
1	0	1	1	1	Fall	Q2[n]	0	Normal mode write 1
X	0	X	1	1	Rise	Q2[n]	Q[n]	
X	0	X	1	1	1	Q2[n]	Q[n]	
x	0	1	1	1	0	Q2[n]	Q[n]	
X	1	X	X	X	X	Q[n]	Q[n]	Save mode
X	0	0	1	1	0	Q2[n]	Q2[n]	Restore mode
X	0	0	1	1	1	Q2[n]	Q[n]	

Table 5.196. Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RDFFNSRASRNX1	1 x Csl	QN	129	1438	7	13.97792
RDFFNSRASRNX2	2 x Csl	QN	137	1638	9	14.232064

Scan Pos Edge DFF SR: RSDFFSRX1, RSDFFSRX2

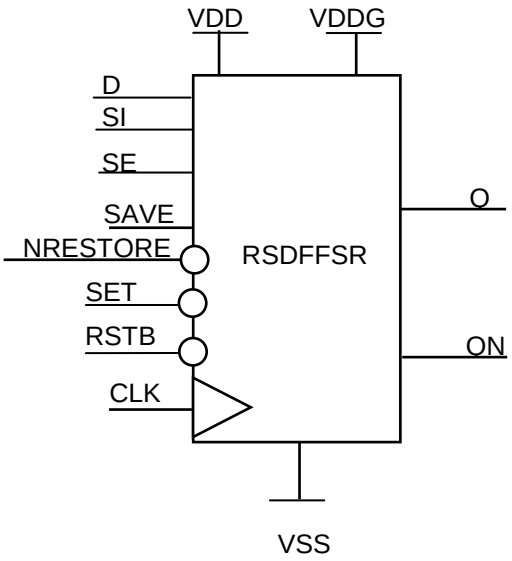


Figure 5.99. Logic Symbol of Scan Pos Edge DFF SR

Table 5.197. RSDFFSR Transition Table

D	SAVE	NRESTORE	CLK	SE	SI	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	0	1	Rise	0	X	Q2[n]	0	1	Normal mode write 0
1	0	1	Rise	0	X	Q2[n]	1	0	Normal mode write 1
X	0	X	Fall	X	X	Q2[n]	Q[n]	QN[n]	
X	0	X	0	X	X	Q2[n]	Q[n]	QN[n]	
X	0	1	1	X	X	Q2[n]	Q[n]	QN[n]	
X	0	1	Rise	1	0	Q2[n]	0	1	Scan mode write 0
X	0	1	Rise	1	1	Q2[n]	1	0	Scan mode write 1
X	1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	0	0	1	X	X	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	0	0	0	X	X	Q2[n]	Q[n]	QN[n]	

Table 5.198. Scan Pos Edge DFF SR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFSRX1	1 x Csl	QN	124	1874	7	16.265216
RSDFFSRX2	2 x Csl	QN	109	2196	11	16.773504

Scan Pos Edge DFF SR, w/ Async Low-Active Set: RSDFFSRASX1, RSDFFSRASX2

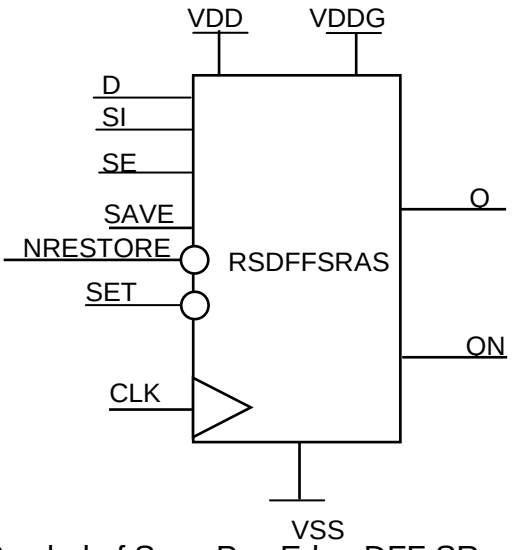


Figure 5.100. Logic Symbol of Scan Pos Edge DFF SR, w/ Async Low-Active Set

Table 5.199. RSDFFSRAS Transition Table

D	SI	SE	SAVE	NRESTORE	SETB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	Q2[n]	1	0	SETB mode
0	X	0	0	1	1	Rise	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	1	Rise	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	1	Fall	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	1	0	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1		1	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	1	Rise	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	1	Rise	Q2[n]	1	0	Scan mmode write 1
X	X	X	1	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	1	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	0	Q2[n]	Q[n]	QN[n]	

Table 5.200. Scan Pos Edge DFF SR, w/ Async Low-Active Set Transition Table

D	SI	SE	SAVE	NRESTORE	SETB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	Q2[n]	1	0	SETB mode
0	X	0	0	1	1	Rise	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	1	Rise	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	1	Fall	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	1	0	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1		1	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	1	Rise	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	1	Rise	Q2[n]	1	0	Scan mmode write 1
X	X	X	1	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	1	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	0	Q2[n]	Q[n]	QN[n]	

Scan Pos Edge DFF SR, w/ Async Low-Active Reset: RSDFFSRARX1, RSDFFSRARX2

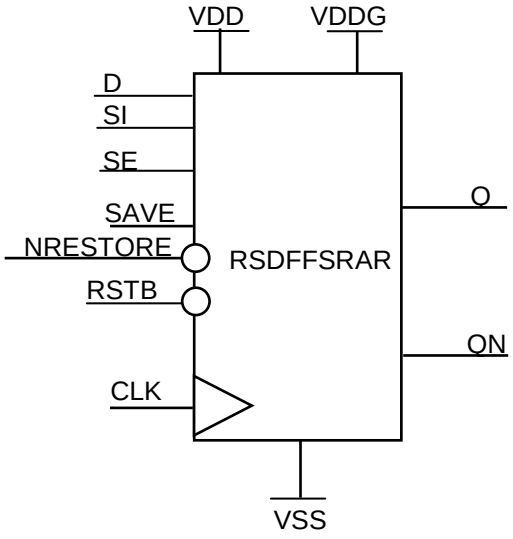


Figure 5.101. Logic Symbol of Scan Pos Edge DFF SR, w/ Async Low-Active Reset

Table 5.201. RSDFFSRAR Transition Table

D	SI	SE	SAVE	NRESTORE	RSTB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	Q2[n]	0	1	RSTB mode
0	X	0	0	1	1	Rise	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	1	Rise	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	1	Fall	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	1	0	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1		1	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	1	Rise	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	1	Rise	Q2[n]	1	0	Scan mmode write 1
X	X	X	1	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	1	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	0	Q2[n]	Q[n]	QN[n]	

Table 5.202. Scan Pos Edge DFF SR, w/ Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFSRARX1	1 x Csl	QN	124	1675	11	16.773504
RSDFFSRARX2	2 x Csl	QN	109	1995	18	17.281792

Scan Pos Edge DFF SR, w/ Async Low-Active Set & Reset: RSDFFSRASRX1, RSDFFSRASRX2

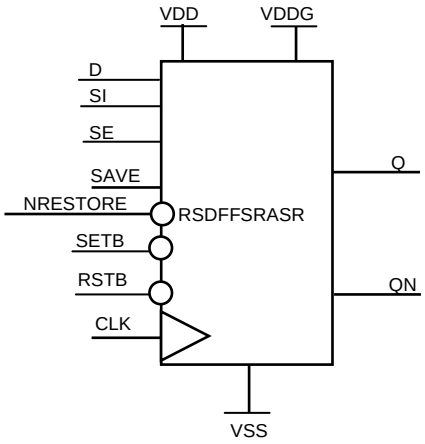


Figure 5.102. Logic Symbol of Scan Pos Edge DFF SR, w/ Async Low-Active Set & Reset

Table 5.203. RSDFFSRASR Transition Table

D	SI	SE	SAVE	NRESTORE	RSTB	SETB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	X	Q2[n]	0	1	RSTB mode
X	X	X	0	X	1	0	X	Q2[n]	1	0	SETB mode
0	X	0	0	1	1	1	Rise	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	1	1	Rise	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	1	1	Fall	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	1	1	0	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1	1	1	1	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	1	1	Rise	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	1	1	Rise	Q2[n]	1	0	Scan mmode write 1
X	X	X	1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	1	1	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	1	0	Q2[n]	Q[n]	QN[n]	

Table 5.204. Scan Pos Edge DFF SR, w/ Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
				Power		
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFSRASRX1	1 x Csl	QN	135	1770	15	17.281792
RSDFFSRASRX2	2 x Csl	QN	123	2074	21	17.79008

Scan Pos Edge DFF SR, w/ Sync Low-Active Set & Reset: RSDFFSRSSRX1, RSDFFSRSSRX2

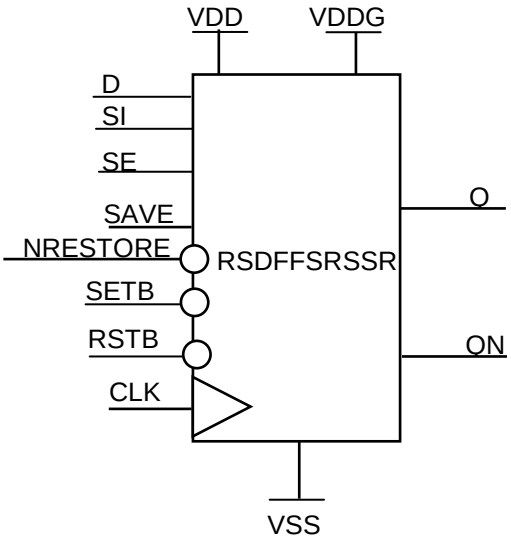


Figure 5.103. Logic Symbol of Scan Pos Edge DFF SR, w/ Sync Low-Active Set & Reset

Table 5.205. RSDFFSRSSR Transition Table

D	SI	SE	SAVE	NRESTORE	RSTB	SETB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	Rise	Q2[n]	0	1	RSTB mode
X	X	X	0	X	1	0	Rise	Q2[n]	1	0	SETB mode
0	X	0	0	1	1	1	Rise	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	1	1	Rise	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	X	X	Fall	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	X	X	0	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1	X	X	1	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	1	1	Rise	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	1	1	Rise	Q2[n]	1	0	Scan mmode write 1
X	X	X	1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	1	1	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	1	0	Q2[n]	Q[n]	QN[n]	

Table 5.206. Scan Pos Edge DFF SR, w/ Sync Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFSRSSRX1	1 x Csl	QN	123	14484	12	16.51936
RSDFFSRSSRX2	2 x Csl	QN	109	14802	8	17.027648

Scan Neg Edge DFF S: RSDFFNSRX1, RSDFFNSRX2

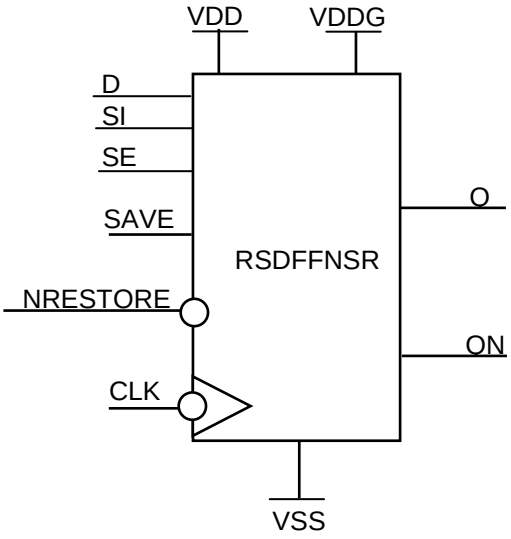


Figure 5.104. Logic Symbol of Scan Neg Edge DFF SR

Table 5.207. RSDFFNSR Transition Table

D	SI	SE	SAVE	NRESTORE	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	X	0	0	1	Fall	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	Fall	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	Rise	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	1	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1	0	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	Fall	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	Fall	Q2[n]	1	0	Scan mmode write 1
X	X	X	1	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	0	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	Q2[n]	Q[n]	QN[n]	

Table 5.208. Scan Neg Edge DFF SR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFNSRX1	1 x Csl	QN	121	21593	20	16.265216
RSDFFNSRX2	2 x Csl	QN	107	21924	21	16.773504

Scan Neg Edge DFF SR, w/ Async Low-Active Set: RSDFFNSRASX1, RSDFFNSRASX2

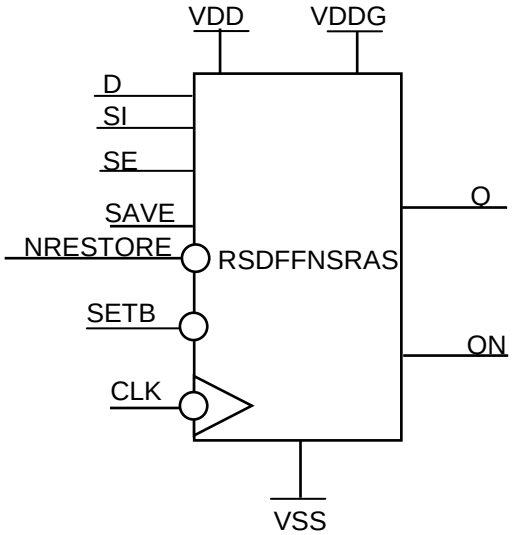


Figure 5.105. Logic Symbol of Scan Neg Edge DFF SR, w/ Async Low-Active Set

Table 5.209. RSDFFNSRAS Transition Table

D	SI	SE	SAVE	NRESTORE	SETB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	Q2[n]	1	0	SETB mode
0	X	0	0	1	1	Fall	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	1	Fall	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	1	Rise	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	1	1	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1	1	0	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	1	Fall	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	1	Fall	Q2[n]	1	0	Scan mode write 1
X	X	X	1	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	0	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	1	Q2[n]	Q[n]	QN[n]	

Table 5.210. Scan Neg Edge DFF SR, w/ Async Low-Active Set Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFNSRASX1	1 x Csl	QN	130	1716	13	17.281792
RSDFFNSRASX2	2 x Csl	QN	116	2036	17	17.79008

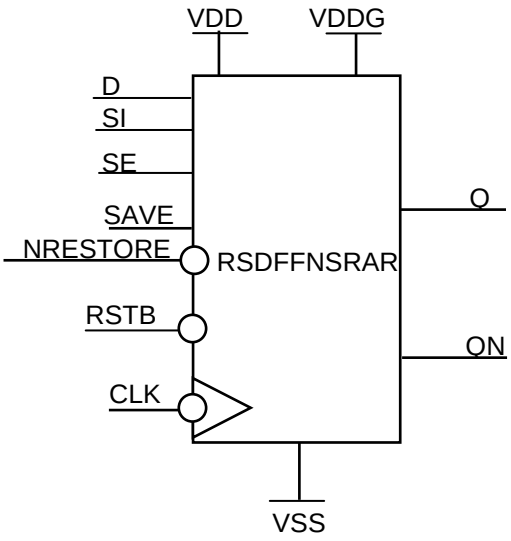


Figure 5.106. Logic Symbol of Scan Neg Edge DFF SR, w/ Async Low-Active Reset

Table 5.211. RSDFFNSRAR Transition Table

D	SI	SE	SAVE	NRESTORE	RSTB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	Q2[n]	0	1	RSTB mode
0	X	0	0	1	1	Fall	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	1	Fall	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	1	Rise	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	1	1	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1	1	0	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	1	Fall	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	1	Fall	Q2[n]	1	0	Scan mode write 1
X	X	X	1	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	0	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	1	Q2[n]	Q[n]	QN[n]	

Table 5.212. Scan Pos Edge DFF SR, w/ Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFNSRARX1	1 x Csl	QN	120	1775	9	16.773504
RSDFFNSRARX2	2 x Csl	QN	106	33445	53	17.281792

Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset: RSDFFNSRASRX1, RSDFFNSRASRX2

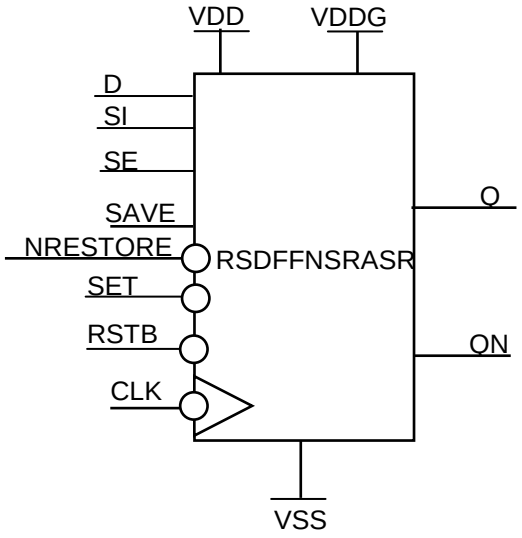


Figure 5.107. Logic Symbol of Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset

Table 5.213. RSDFFNSRASR Transition Table

D	SI	SE	SAVE	NRESTORE	RSTB	SETB	CLK	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	X	Q2[n]	0	1	RSTB mode
X	X	X	0	X	1	0	X	Q2[n]	1	0	SETB mode
0	X	0	0	1	1	1	Fall	Q2[n]	0	1	Normal mode write 0
1	X	0	0	1	1	1	Fall	Q2[n]	1	0	Normal mode write 1
X	X	X	0	X	1	1	Rise	Q2[n]	Q[n]	QN[n]	
X	X	X	0	X	1	1	1	Q2[n]	Q[n]	QN[n]	
X	X	X	0	1	1	1	0	Q2[n]	Q[n]	QN[n]	
X	0	1	0	1	1	1	Fall	Q2[n]	0	1	Scan mode write 0
X	1	1	0	1	1	1	Fall	Q2[n]	1	0	Scan mmode write 1
X	X	X	1	X	X	X	X	Q[n]	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	1	0	Q2[n]	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	1	1	Q2[n]	Q[n]	QN[n]	

Table 5.214. Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFNSRASRX1	1 x Csl	QN	130	1770	13	17.281792
RSDFFNSRASRX2	2 x Csl	QN	116	2051	17	17.79008

Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out: RSDFFNSRASRQX1, RSDFFNSRASRQX2

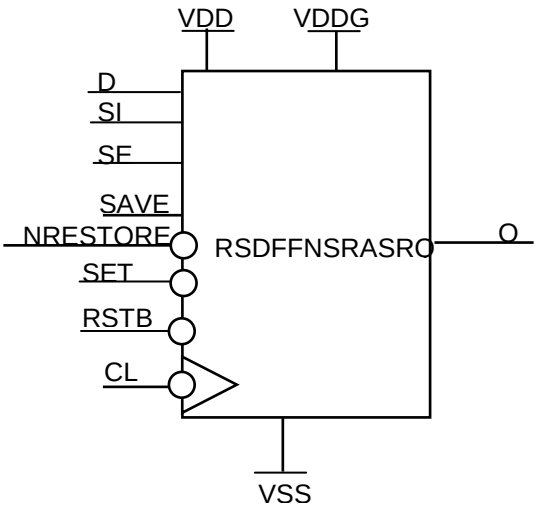


Figure 5.108. Logic Symbol of Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out

Table 5.215. RSDFFNSRASR Transition Table

D	SI	SE	SAVE	NRESTORE	RSTB	SETB	CLK	Q2[n+1]	Q[n+1]	Mode
X	X	X	0	X	0	X	X	Q2[n]	0	RSTB mode
X	X	X	0	X	1	0	X	Q2[n]	1	SETB mode
0	X	0	0	1	1	1	Fall	Q2[n]	0	Normal mode write 0
1	X	0	0	1	1	1	Fall	Q2[n]	1	Normal mode write 1
X	X	X	0	X	1	1	Rise	Q2[n]	Q[n]	
X	X	X	0	X	1	1	1	Q2[n]	Q[n]	
X	X	X	0	1	1	1	0	Q2[n]	Q[n]	
X	0	1	0	1	1	1	Fall	Q2[n]	0	Scan mode write 0
X	1	1	0	1	1	1	Fall	Q2[n]	1	Scan mmode write 1
X	X	X	1	X	X	X	X	Q[n]	Q[n]	Save mode
X	X	X	0	0	1	1	0	Q2[n]	Q2[n]	Restore mode
X	X	X	0	0	1	1	1	Q2[n]	Q[n]	

Table 5.216. Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only Q out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFNSRASRQX1	1 x Csl	Q	149	1703	9	17.027648
RSDFFNSRASRQX2	2 x Csl	Q	138	1990	10	17.281792

Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out: RSDFFNSRASRNX1, RSDFFNSRASRNX2

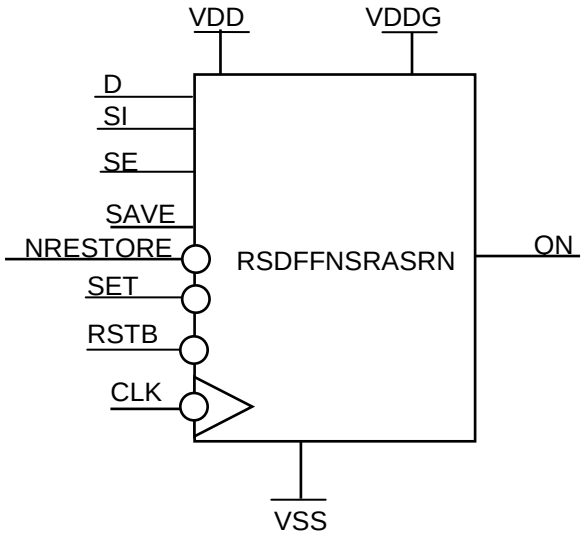


Figure 5.109. Logic Symbol of Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out

Table 5.217. RSDFFNSRASRN Transition Table

D	SI	SE	SAVE	NRESTORE	RSTB	SETB	CLK	Q2[n+1]	QN[n+1]	Mode
X	X	X	0	X	0	X	X	Q2[n]	1	RSTB mode
X	X	X	0	X	1	0	X	Q2[n]	0	SETB mode
0	X	0	0	1	1	1	Fall	Q2[n]	1	Normal mode write 0
1	X	0	0	1	1	1	Fall	Q2[n]	0	Normal mode write 1
X	X	X	0	X	1	1	Rise	Q2[n]	QN[n]	
X	X	X	0	X	1	1	1	Q2[n]	QN[n]	
X	X	X	0	1	1	1	0	Q2[n]	QN[n]	
X	0	1	0	1	1	1	Fall	Q2[n]	1	Scan mode write 0
X	1	1	0	1	1	1	Fall	Q2[n]	0	Scan mmode write 1
X	X	X	1	X	X	X	X	Q[n]	QN[n]	Save mode
X	X	X	0	0	1	1	1	Q2[n]	!Q2[n]	Restore mode
X	X	X	0	0	1	1	0	Q2[n]	QN[n]	

Table 5.218. Scan Neg Edge DFF SR, w/ Async Low-Active Set & Reset, Only QN out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
RSDFFNSRASRNX1	1 x Csl	QN	129	1700	9	17.535936
RSDFFNSRASRNX2	2 x Csl	QN	117	1904	13	17.535936

Header Cell: HEADX2, HEADX4, HEADX8, HEADX16, HEADX32

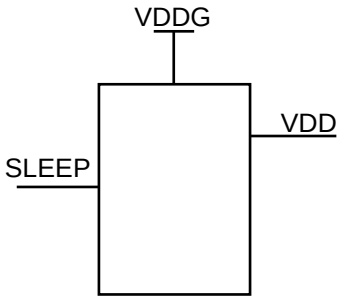


Figure 5.110. Logic Symbol of Header Cell

Table 5.219. HEAD Truth Table

SLEEP	VDDG	VDD	
0	1	1	
1	1	hi-z	

Table 5.220. Header Cell Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
HEADX2	2 x Csl	-	105	1	7.116032
HEADX4	4 x Csl	-	236	2	8.132608
HEADX8	8 x Csl	-	549	4	10.16576
HEADX16	16 x Csl	-	1222	8	14.232064
HEADX32	32 x Csl	-	2580	17	22.364672

Header Cell (with SLEEPOUT output): HEAD2X2, HEAD2X4, HEAD2X8, HEAD2X16, HEAD2X32

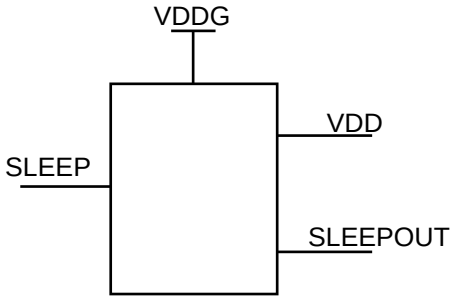


Figure 5.111. Logic Symbol of Header Cell (with SLEEPOUT output)

Table 5.221. Header Cell (with SLEEPOUT output) Truth Table

SLEEP	VDDG	VDD	SLEEPOUT
0	1	1	0
1	1	hi-z	1

Table 5.222. Header Cell Electrical Parameters and Areas(with SLEEPOUT output)

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
HEAD2X2	2 x Csl	36	560	5	7.62432
HEAD2X4	4 x Csl	44	1065	9	8.640896
HEAD2X8	8 x Csl	37	2146	18	10.674048
HEAD2X16	16x Csl	38	4227	38	15.24864
HEAD2X32	32 x Csl	40	8400	83	24.397824

Footer Cell: FOOTX2, FOOTX4, FOOTX8, FOOTX16, FOOTX32

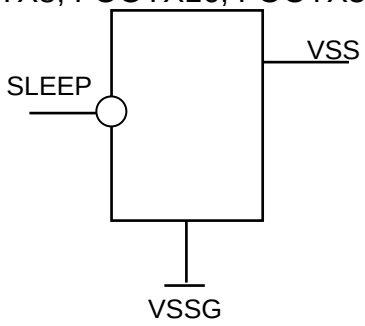


Figure 5.112. Logic Symbol of Footer Cell

Table 5.223. FOOT Truth Table

SLEEP	VSSG	VSS
1	0	0
0	0	hi-z

Table 5.224. Footer Cell Electrical Parameters and Areas(without SLEEPOUT output)

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
FOOTX2	2 x Csl	-	1103	2	7.116032
FOOTX4	4 x Csl	-	1102	9	7.62432
FOOTX8	8 x Csl	-	1102	19	10.16576
FOOTX16	16x Csl	-	4227	38	14.232064
FOOTX32	32 x Csl	-	1152	3	22.364672

Footer Cell (with SLEEPOUT output): FOOT2X2, FOOT2X4, FOOT2X8, FOOT2X16, FOOT2X32

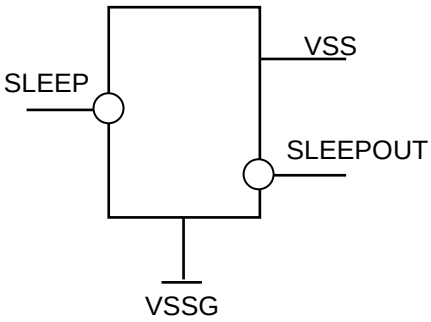


Figure 5.113. Logic Symbol of Footer Cell (with SLEEPOUT output)

Table 5.225. Footer Cell (with SLEEPOUT output) Truth Table

SLEEP	VSSG	VSS	SLEEPOUT
0	1	1	0
1	1	hi-z	1

Table 5.226. Footer Cell Electrical Parameters and Areas(with SLEEPOUT output)

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
FOOT2X2	2 x Csl	67	22	4	7.116032
FOOT2X4	4 x Csl	58	48	8	10.674048
FOOT2X8	8 x Csl	60	98	14	15.24864
FOOT2X16	16x Csl	73	198	29	25.4144
FOOT2X32	32 x Csl	103	398	61	45.74592

Always on Inverter: AOINVX1, AOINVX2, AOINVX4

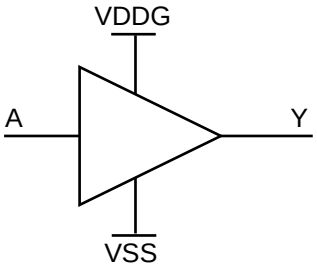


Figure 5.114. Logic Symbol of Always on Inverter

Table 5.227. AOINV Truth Table

A	VDDG	VSS	Y
0	1	0	1
1	1	0	0

Table 5.228. Always on Inverter Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AOINVX1	1 x Csl	48	1251	1	6.607744
AOINVX2	2 x Csl	31	1401	2	7.62432
AOINVX4	4 x Csl	21	1688	4	8.132608

Always on Non-inverting Buffer: AOBUFX1, AOBUFX2, AOBUFX4

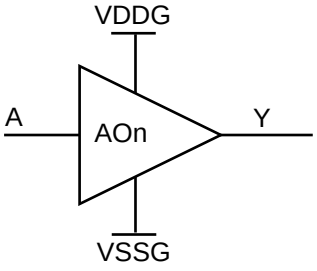


Figure 5.115. Logic Symbol of Always on Non-inverting Buffer

Table 5.229. AOBUF Truth Table

A	VDDG	VSSG	Y
0	1	0	0
1	1	0	1

Table 5.230. Always on Non-inverting Buffer Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AOBUFX1	1 x Csl	52	1413	3	6.607744
AOBUFX2	2 x Csl	43	1639	5	7.116032
AOBUFX4	4 x Csl	40	2143	8	8.132608

Always on Pos Edge DFF, w/ Async Low-Active Reset: AODFFARX1, AODFFARX2

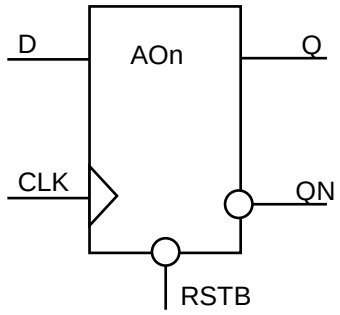


Figure 5.116. Logic Symbol of Always on Pos Edge DFF, w/ Async Low-Active Reset

Table 5.231. AODFFAR Transition Table

RSTB	CLK	D	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	X	X	Q2[n]	0	1	RSTB mode
1	Rise	0	Q2[n]	0	1	Normal mode write 0
1	Rise	1	Q2[n]	1	0	Normal mode write 1
1	Fall	X	Q2[n]	Q[n]	QN[n]	
1	1	X	Q2[n]	Q[n]	QN[n]	
1	0	X	Q2[n]	Q[n]	QN[n]	

Table 5.232. Always on Pos Edge DFF, w/ Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
AODFFARX1	1 x Csl	Q	125	2135	10	8.640896
		QN	103			
AODFFARX2	2 x Csl	Q	126	2494	12	9.657472
		QN	95			

Always on Neg Edge DFF, w/ Async Low-Active Reset: AODFFNARX1, AODFFNARX2

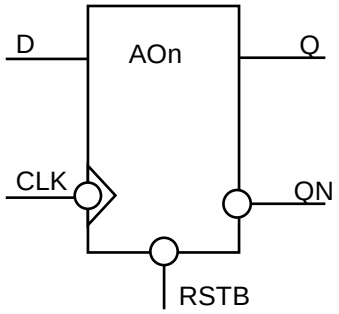


Figure 5.117. Logic Symbol of Always on Neg Edge DFF, w/ Async Low-Active Reset

Table 5.233. AODFFNAR Transition Table

RSTB	CLK	D	Q2[n+1]	Q[n+1]	QN[n+1]	Mode
0	X	X	Q2[n]	0	1	RSTB mode
1	Fall	0	Q2[n]	0	1	Normal mode write 0
1	Fall	1	Q2[n]	1	0	Normal mode write 1
1	Rise	X	Q2[n]	Q[n]	QN[n]	
1	1	X	Q2[n]	Q[n]	QN[n]	
1	0	X	Q2[n]	Q[n]	QN[n]	

Table 5.234. Always on Neg Edge DFF, w/ Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.05 V DC, Temp=25 Deg.C, Operating Frequency: Freq=500 MHz, Capacitive Standard Load: Csl=4 fF					Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		
				Leakage (VDD=1.05 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um^2)
AODFFNARX1	1 x Csl	Q	123	2131	11	8.640896
		QN	101			
AODFFNARX2	2 x Csl	Q	125	2492	13	9.657472
		QN	95			

Bus Keeper: BUSKP

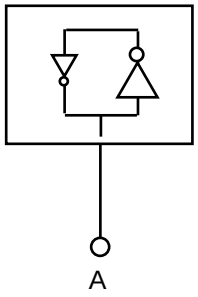


Figure 5.118. Logic Symbol of Bus Keeper

Table 5.235. BUSKP Truth Table

Z
1

P-MOSFET: PMT1, PMT2, PMT3

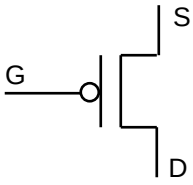


Figure 5.119. Logic Symbol of P-MOSFET

Table 5.236. PMT Truth Table

Z
1

N-MOSFET: NMT1, NMT2, NMT3

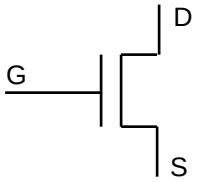


Figure 5.120. Logic Symbol of N-MOSFET

Table 5.237. NMT Truth Table

Z
1

Tie High: TIEH

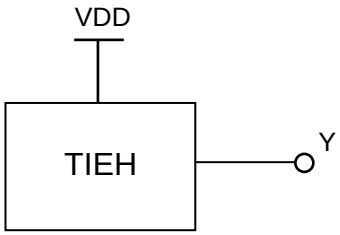


Figure 5.121. Logic Symbol of Tie High

Table 5.238. TIEH Truth Table

Y
1

Tie Low: TIEL

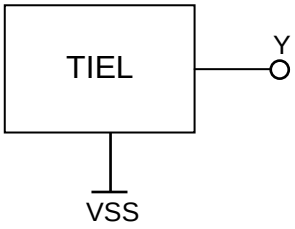


Figure 5.122. Logic Symbol of Tie Low

Table 5.239. TIEL Truth Table

Y
0

Antenna Diode: ANTENNA

Figure 5.123. Logic Symbol of Antenna Diode

Table 5.240. ANTENNA Truth Table

INP
*

Decoupling Capacitance: DCAP

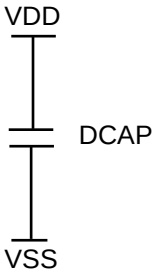


Figure 5.124. Logic Symbol of DCAP Decoupling Capacitance

Capacitive Load: CLOAD1

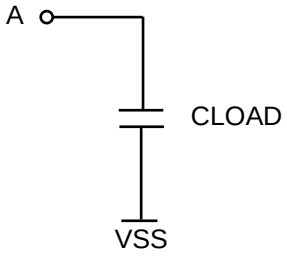
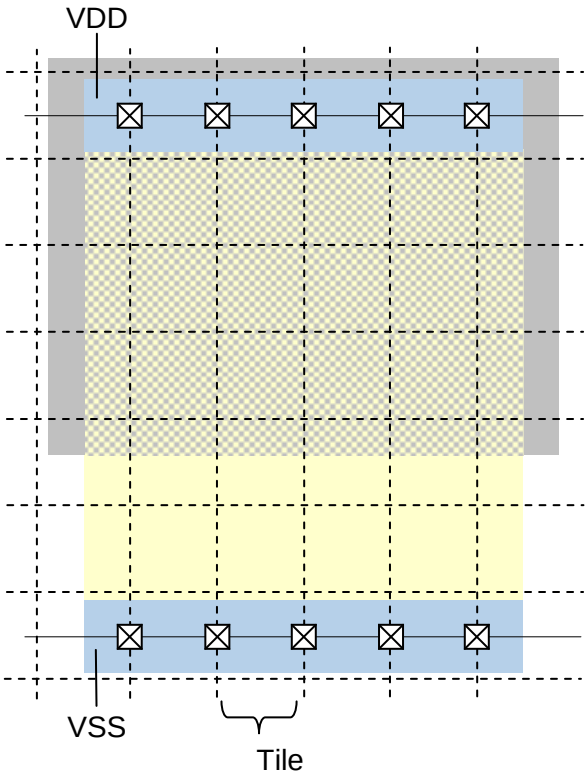


Figure 5.125. Logic Symbol of Capasitive Load

Single Height Filler Cells: SHFILL1, SHFILL2, SHFILL3, SHFILL64, SHFILL128



FILLER	Number of Tiles
SHFILL1	1
SHFILL2	2
SHFILL3	3
SHFILL64	64
SHFILL128	128

Figure 5.126.Physical structure of Single Hight Filler Cell

Double Height Filler cells: DHFILLUP1, DHFILLDN1, DHFILLAO1

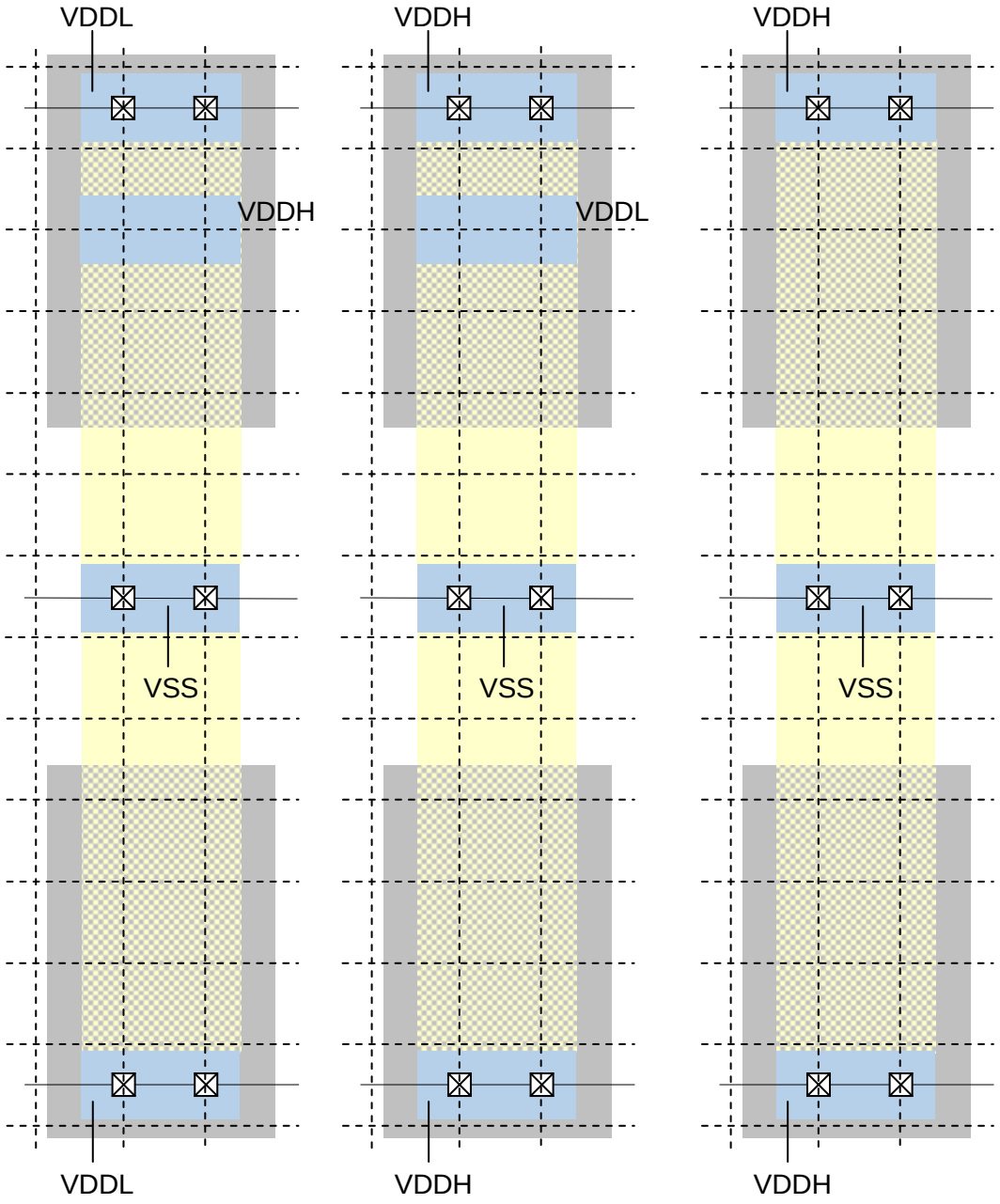


Figure 5.127. Physical structure of double height filler cells

6. Revison history

Table 6.1. Revision history

Revision	Date	EDK Version	Change
1.0.0	31/01/2012	b1.0.0	Initial release