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IC Compiler 2010.03 Incremental Training

Design Planning: Flip Chip, Floorplanning, Power Network Analysis / Power Network Synthesis, and In Place Optimization

Agenda

- Flip-Chip Enhancements
  - Personality type support on flip-chip driver pins
- Floorplanning
  - Physical Tcl constraints command consolidation
  - Pin placement for designs with mixed pins and pads
- Power Network Analysis (PNA) and Power Network Synthesis (PNS)
  - Multithreshold-CMOS (MTCMOS) ring placement using a user-specified pattern
- In-Place Optimization Enhancements
  - High-fanout synthesis support and no new cells at the top level
  - New trace mode

Personality Type Setting Support on Flip-Chip Driver Pins

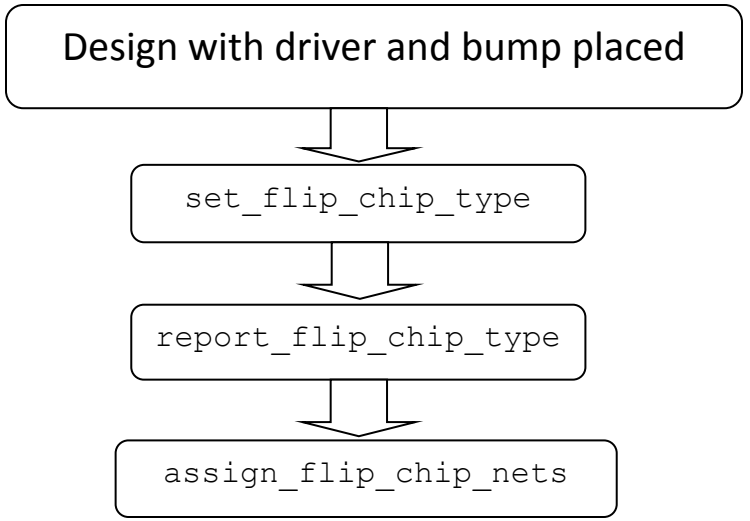
- Overview
  - Enables the setting, resetting, and reporting of a flip-chip personality type on pins

- UI
  - **report_flip_chip_type**
    [*cell_or_pin_list*]
  - **set_flip_chip_type**
    [-personality_type *string*]
    [-pin]
    [*cell_or_pin_or_net_list*]

Personality Type Setting Support on Flip-Chip Driver Pins

- User Benefit
  - Supports setting of a personality type on pins
  - Reports personality type on pins
  - Allows you to clear previously set personality types

- Flow Recommendation



Personality Type Setting Support on Flip-Chip Driver Pins

- Limitations
  - Before setting a personality type on cells, the personality type on pins should be cleared

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Consolidation of Physical Tcl Constraints for Pins and Pads

- Overview
  - Consolidates some Tcl physical constraint commands and makes these commands easier to use in the design flow

- UI

NEW	OLD
`read_pin_pad_physical_constraints`	`read_io_constraints`
`write_pin_pad_physical_constraints`	`write_io_constraints`
`report_pin_pad_physical_constraints`	`report_io_constraints`
`remove_pin_pad_physical_constraints`	`remove_io_constraints`

Consolidation of Physical Tcl Constraints for Pins and Pads

- UI
  - New command options:
    - **set_pad_physical_constraint**
      [-chip_level_distance
      {{dist_left_edge_to_pad *float*}
      {dist_bottom_edge_to_pad *float*}
      {dist_right_edge_to_pad *float*}
      {dist_top_edge_to_pad *float*}}]
    - **set_fp_pin_constraints**
      [-use_physical_constraints on | off]
    - **set_pin_physical_constraints**
      [-pin_spacing *pin_spacing_number*]
      [-exclude_sides *side_numbers*]
      [-nets *net_list*]

Consolidation of Physical Tcl Constraints for Pins and Pads

- User Benefit
  - Ease of use
  - Fewer commands
  - Naming consistency
  - `set_pin_physical_constraints` can be used to set all kinds of individual pin constraints, either per pin or for a collection of pins
  - `set_fp_pin_constraints` can be used to set global pin constraints, either per block or for the whole design

- Flow Recommendation
  - Use the regular design planning flow with these new commands and options.

Consolidation of Physical Tcl Constraints for Pins and Pads

- Limitations
  - No known limitations

- Further Information
  - `set_chiplevel_pad_physical_constraints` has been removed from version 2010.03

Terminal Placement for Designs With Mixed Pins and Pads

- Overview
  - Enhanced the `initialize_floorplan` command to handle designs with mixed pads and ports

- UI

```
initialize_floorplan
place_fp_pins -block_level
analyze_fp_routing
    -include_flip_chip_connections
```

Terminal Placement for Designs With Mixed Pins and Pads

- User Benefit
  - Supports the proper placement of I/O cells and terminals
  - Improves timing

- Flow Recommendation
  - Block-level pin placement (bottom-up):

```
initialize_floorplan
place_fp_pins -block_level
```

  - Soft-macro pin placement (top-down):

```
analyze_fp_routing
   -include_flip_chip_connections
commit_fp_plan_groups
place_fp_pins
```

Terminal Placement for Designs With Mixed Pins and Pads

- Limitations
  - Any terminal connected to and placed on top of an I/O cell is not moved in sync with the I/O cell if it is moved.

- Further Information
  - These changes have no impact on ILM, multivoltage, and multicorner-multimode flows

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MTCMOS Ring Placement Using a User-Specified Pattern

- Overview
  - The `create_power_switch_ring` command now allows you to define your own pattern for power switch cell placement
  - You specify your pattern by using the new **`-place_pattern`** option
  - IC Compiler considers the pattern as a group and places this group in the specified density
- UI

```
create_power_switch_ring -place_pattern
  {id1 id2 {id3 5}}
```

  - The command treats the {*id1 id2* {*id3* 5}} group of cells as one cell

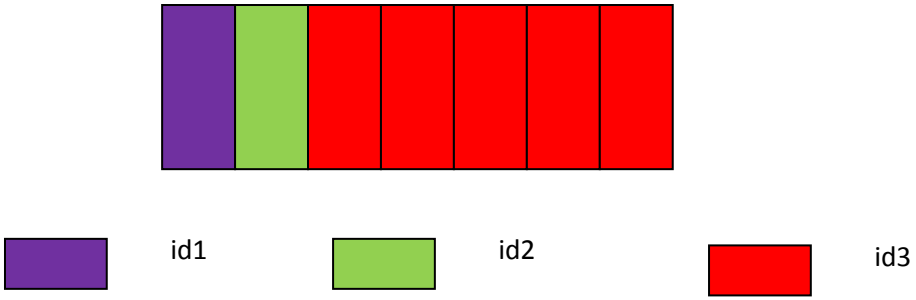
MTCMOS Ring Placement Using a User-Specified Pattern

- User Benefit
  - Insertion of power switches in a more complicated pattern
  - Insertion of a group of cells together

- Flow Recommendation
  - You need to define the pattern before inserting the power switches

MTCMOS Ring Placement Using a User-Specified Pattern

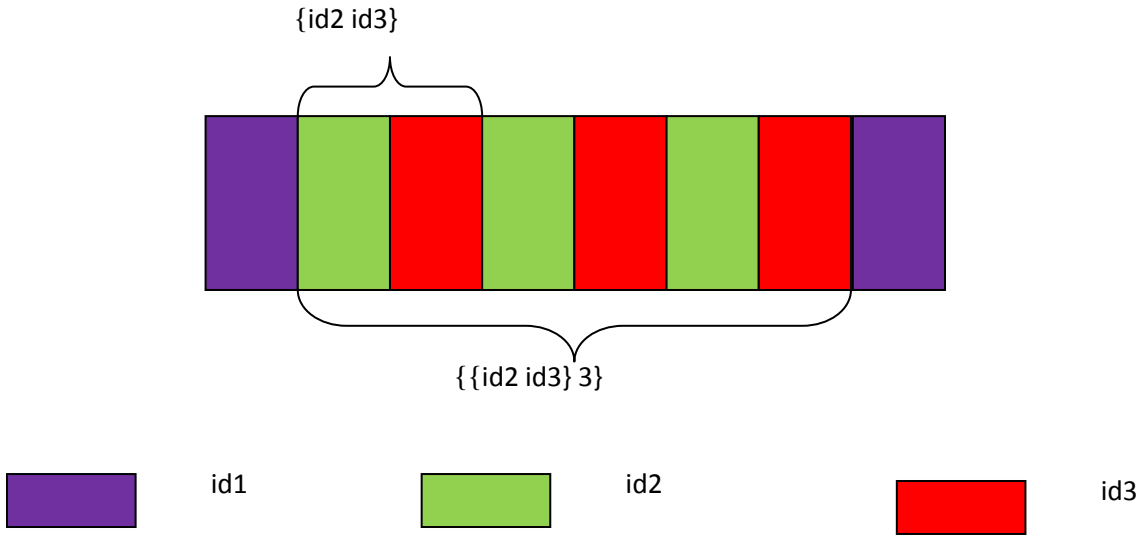
- **`-place_pattern {`*`id1 id2 {id3`*` 5}}`**
  (*id1*, *id2*, *id3* are reference cell names)



- {*id3* 5} means to iterate one cell 5 times

MTCMOS Ring Placement Using a User-Specified Pattern

- To support complex patterns, you can nest patterns
- For example: *{id1 {{id2 id3} 3} id1}*



MTCMOS Ring Placement Using a User-Specified Pattern

- Limitations
  - The pattern can include only one type of power switch cell
- Further Information
  - This capability works in multicorner-multimode designs and in UPF mode
  - Man page provides detailed information

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High-Fanout Synthesis Support and No New Cells at the Top Level

- Overview
  - Adds the following capabilities to in-place optimization:
    - Optimize only high-fanout nets
    - Do not place new cells at the top level
- UI

```
optimize_fp_timing
    [-effort medium | high]
    [-fix_design_rule]
    [-area_recovery]
    [-report_qor]
    [-feedthrough_buffering_only]
    [-keep_global_routes]
    [-no_new_cells_at_top_level]
    [-hfs_only]
```

High-Fanout Synthesis Support and No New Cells at the Top Level

- User Benefit
  - Supports abutted and narrow channel designs where there is no need to add buffers at the top level

- Flow Recommendation
  - Combine the following two options when working on fully abutted designs

    `-hfs_only`

    `-no_new_cells_at_top_level`
  - `-hfs_only` and `-no_new_cells_at_top_level` can also be used independently

New Trace Mode

- Overview
  - Enables in-place optimization to work only on the interface logic or on both the top-level logic and the interface logic
    - Old trace mode always worked on both the top-level logic and the interface logic
  - The new algorithm improves robustness

- UI
  - **set_fp_trace_mode**
    [-include_top_logic]
    [-verbose]
  - **end_fp_trace_mode**
  - **get_fp_trace_mode**
  - **report_fp_trace_mode_options**

New Trace Mode

- User Benefit
  - Fast optimization run time
  - Good QoR for requested subset of logic (interface or top+interface), which results in better budgets

- Flow Recommendation
  - To generate good budgets, the default trace mode (interface logic only) is sufficient
  - Trace mode can be used in any flow: low power, multicorner-multimode, and UPF

New Trace Mode

- Limitations
  - No known limitations
- Further Information
  - GUI command is available
  - Memory usage is the same as non-trace mode
  - Man pages provide detailed information
  - New trace mode works on any design size
  - No runtime benefits with `-hfs_only`

Summary of Design Planning Updates

Module 1

- You can set/report/remove the personality type of a flip-chip cell(s)/pin(s)
- The Tcl physical constraint commands have been simplified/consolidated to make their usage easier and more intuitive
- Power switch ring creation now has the flexibility to let you define your own pattern for power switch cell placement
- High-fanout synthesis and no new cells at the top level supported in in-place optimization

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