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Predictable Success

IC Compiler 2010.03 Incremental Training

Design Planning: Clock Planning, Pin Assignment, and Routing

Agenda

- Clock Planning
  - Enhanced hierarchical clock tree planning and budgeting flow
- Pin Assignment
  - Pin-cutting flow supports user-specified feedthrough topology
- Routing
  - Zroute-based top-down and block-level pin assignment
  - Fast plan-group-aware Zroute

Hierarchical Clock Tree Planning Flow

- Overview
  - Enhanced clock tree planning and budgeting flow allows clock tree adjustment and uses actual clock latency for timing analysis and budgeting

- UI
  - Default behavior is changed to keep clock trees inside plan groups

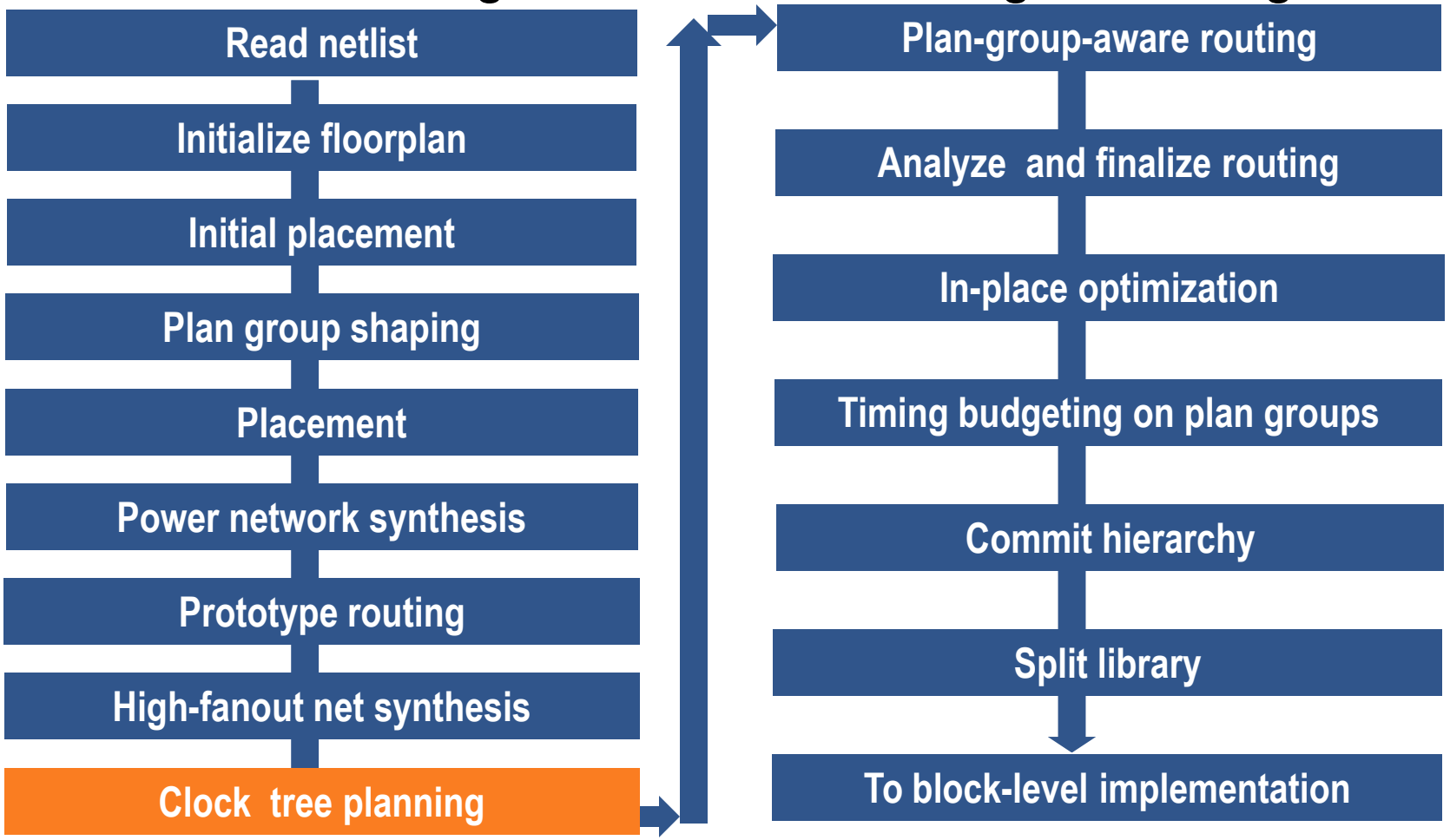
```
set_fp_clock_plan_options -keep_block_tree true
```

Hierarchical Clock Tree Planning Flow

- User Benefit
  - Default clock tree planning keeps block-level and top-level clock trees for accurate clock tree analysis and reporting
  - Timing analysis uses propagated clocks to identify timing violations resulting from clock skew
  - You can perform interclock delay balancing after clock tree planning to improve timing
  - Timing budgeting generates clock latency budgets based on actual clock trees

Hierarchical Clock Tree Planning Flow

- Clock Tree Planning in Hierarchical Design Planning Flow



Hierarchical Clock Tree Planning Flow

Flow Details

High-fanout net synthesis

Clock tree planning
- Insert anchor cells
- Generate plan-group clock tree
- Generate top-level clock tree
- Set propagated clocks

Plan-group-aware routing

Analyze and finalize routing

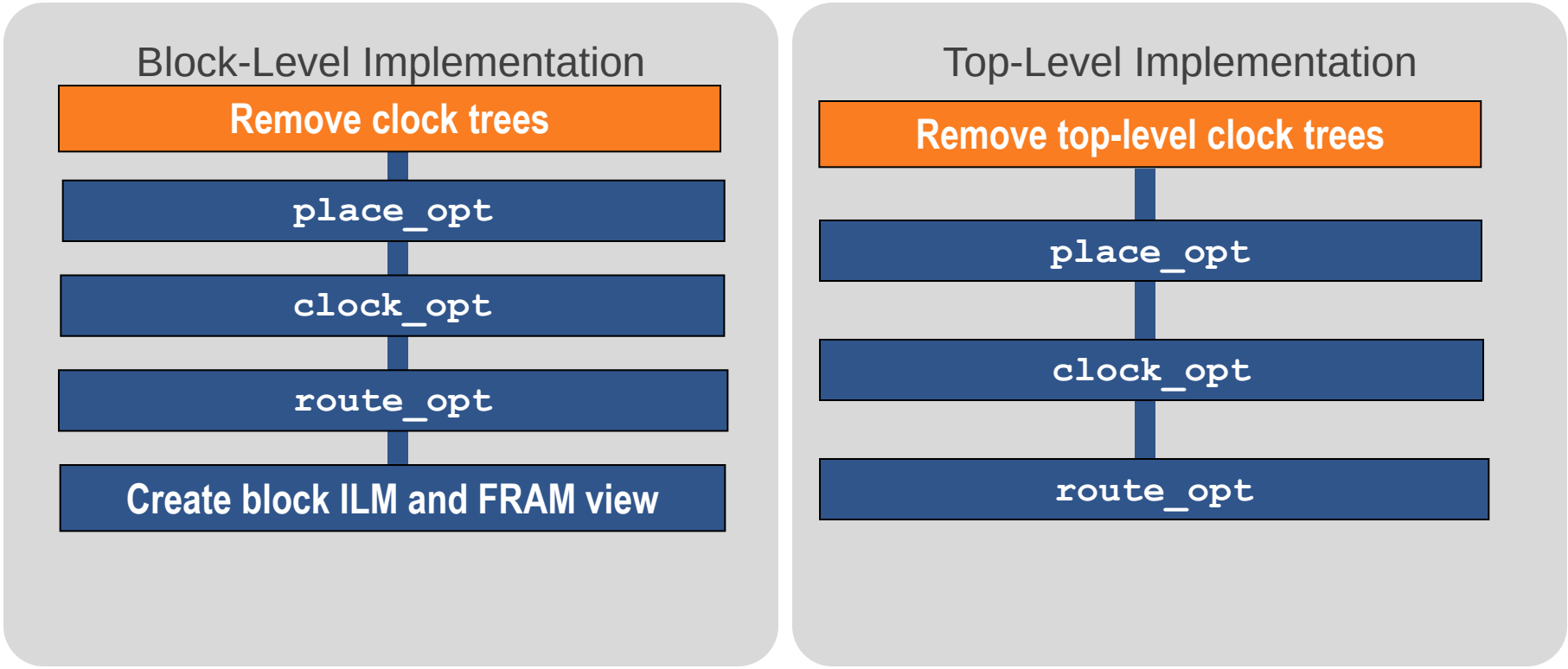
In-place optimization

Timing budgeting on plan groups
- Generate timing budgets
- Generate clock budgets (latency)
- Set ideal clocks in block SDC

Commit hierarchy

```
…
optimize_fp_timing -hfn_only

set_fp_clock_plan_options -anchor_cell
compile_fp_clock_plan

(clock tree adjustment if needed)

set_route_zrt_common_options
  -plan_group_aware
route_zrt_global
analyze_fp_routing -finalize
…
optimize_fp_timing

allocate_fp_budgets

commit_fp_plan_groups
…
```

Hierarchical Clock Tree Planning Flow
Block- and Top-Level Implementation



Hierarchical Clock Tree Planning Flow

- Limitations
  - Clock tree planning might create new clock ports on a plan group. To avoid,

```
foreach_in_collection pgroup [get_plan_groups *] {
  set_clock_tree_exceptions -preserve_hierarchy \
    [get_attribute $pgroup name] }
```

- Further Information
  - More details on the 2010.03 flow script and the handling of different design styles are in the 2010.03 Clock Tree Planning Flow application note (see https://solvnet.synopsys.com/retrieve/029907.html)

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Pin Cutting Supports User-Specified Feedthrough Topology

- Overview
  - You can provide a mapping file to control
    - How the tool should route a net or feedthrough
    - Which blocks the tool should route through
    - The order in which the blocks should be connected

- UI

```
set_fp_pin_constraints
    -allow_feedthroughs on
    -read_feedthrough_map on
    -write_feedthrough_map on
```

  - The feedthrough mapping files must be named **feedthroughMapIn** *(for read)* and **feedthroughMapOut** *(for write)* in the current directory

Pin Cutting Supports User-Specified Feedthrough Topology

- UI (Mapping File Template)
  - The mapping file's content is in following format:

```
Net1_Name:
    {object_type1 object_name1} {object_type2 object_name2}
    …
Net2_Name:
    {object_type1 object_name1} {object_type2 object_name2}
    …
```

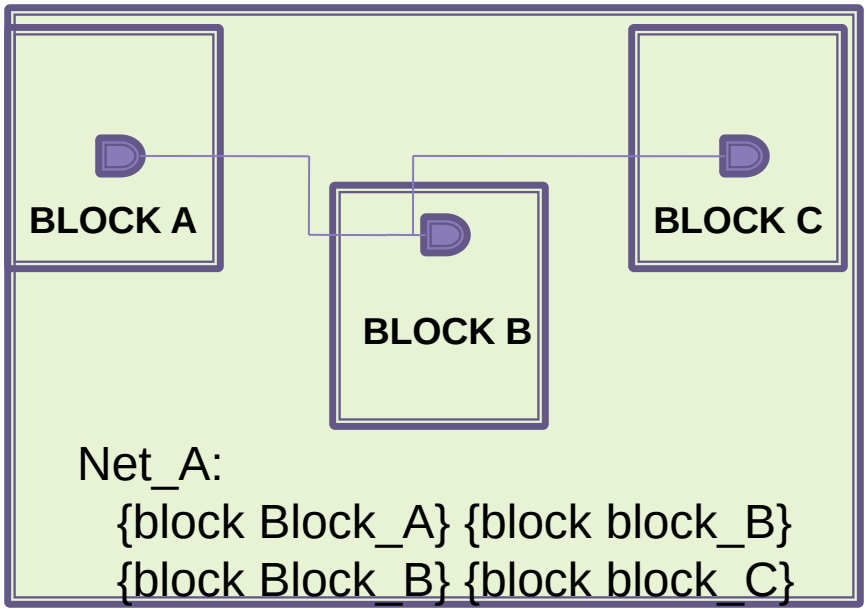
  - Legends
    - The object type can be
      - A block (plangroup),
      - An I/O port or a pin (pins on soft macros, hard macros, or I/O pad cells)
      - A cell (soft macros, hard macros, or I/O pad cells)
    - The object name is either a
      - Plan group name
      - Top-level port name
      - Macro or I/O pad's pin name

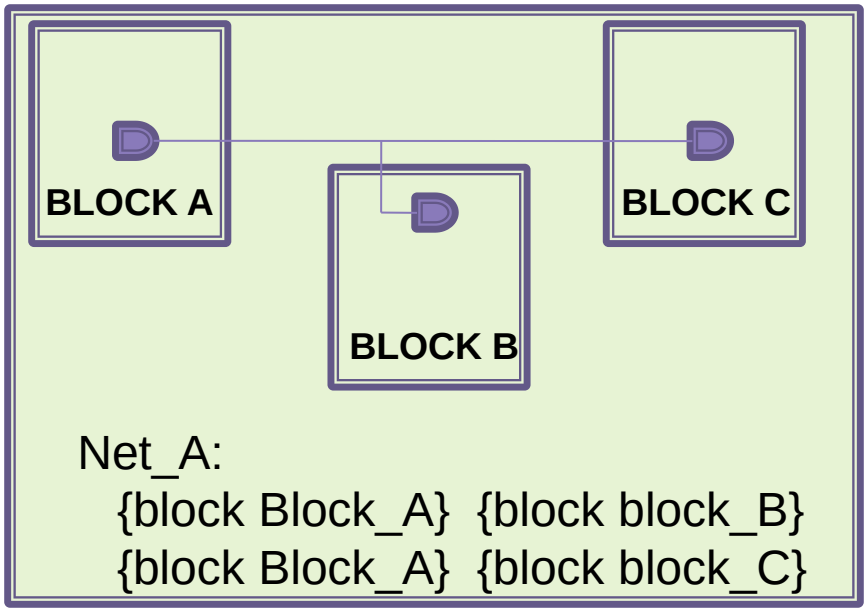
Pin Cutting Supports User-Specified Feedthrough Topology

- User Benefit
  - You can control the routing of specified nets
  - Feedthrough insertion is deterministic

Pin Cutting Supports User-Specified Feedthrough Topology

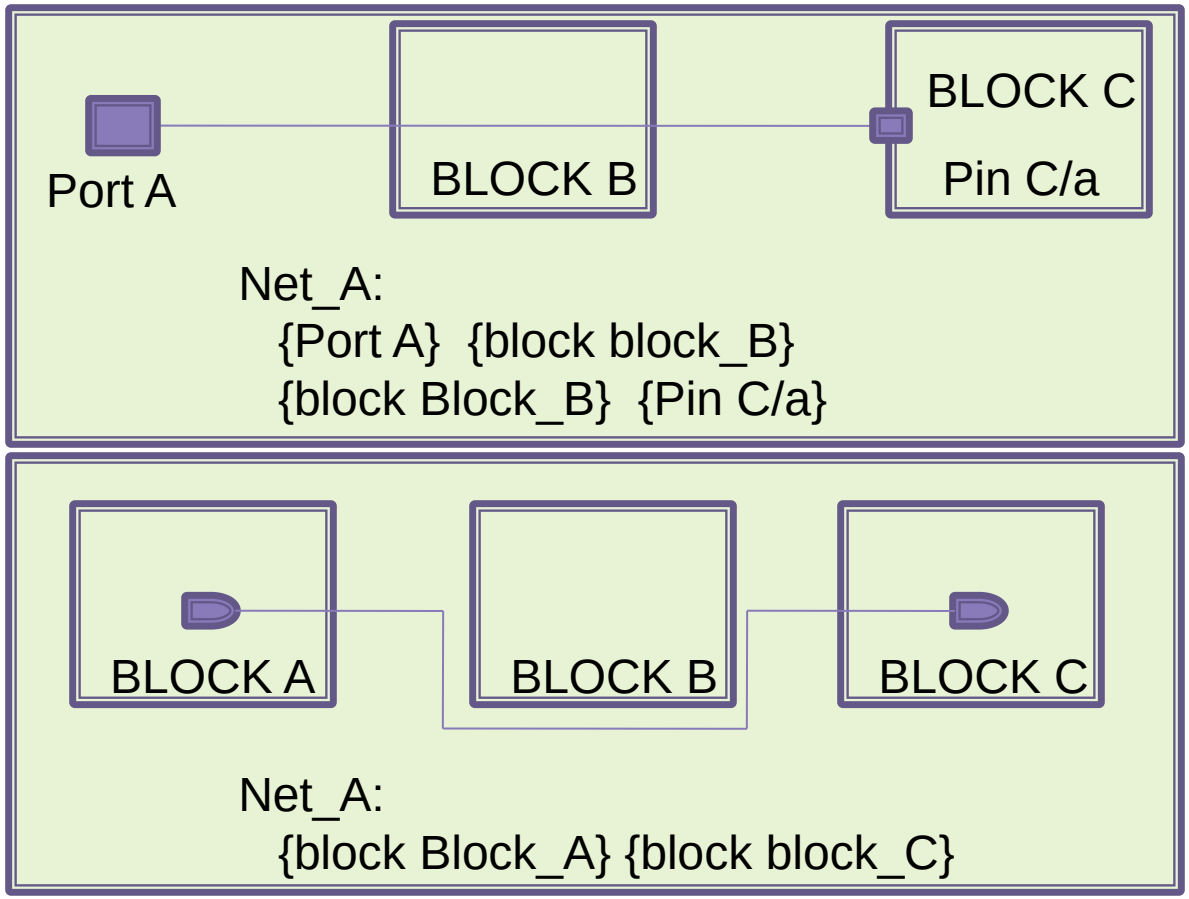
- User Benefit (Continued)
  - The following figures show the effect of this new feature





Pin Cutting Supports User-Specified Feedthrough Topology

- User Benefit (Continued)



Pin Cutting Supports User-Specified Feedthrough Topology

- Flow Recommendation
  - `set_fp_pin_constraints -allow_feedthroughs on -read_feedthrough_map on`
    - The feedthrough mapping file must be named **feedthroughMapIn** in the current directory
  - `set_route_zrt_common_options -plan_group_aware all_routing | top_level_only | off`
  - `route_zrt_global`

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Zroute-Based Top-Down and Block-Level Pin Assignment

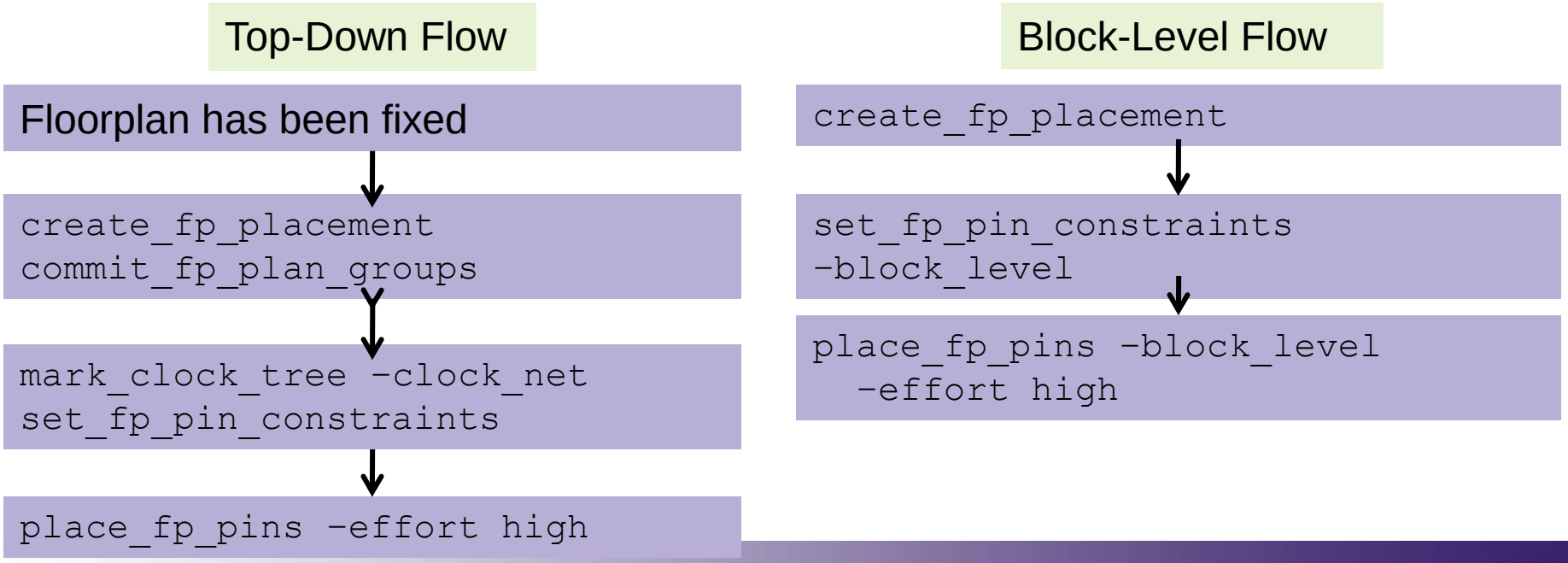
- Overview
  - Pin-cutting flow's plan-group-aware routing (PGAR) was been from the classic router to Zroute in C-2009.06
  - The `-effort high` option of the `place_fp_pins` now uses Zroute instead of the classic router
- UI
  - **`place_fp_pins`**

```
[-effort low | high]
[-block_level]
[-output_feedthroughs output_feed]
[-verbose]
```

  - `-effort low` (flyline-based pin assignment)
  - `-effort high` (Zroute-based pin assignment)

Zroute-Based Top-Down and Block-Level Pin Assignment

- User Benefit
  - Making use of the high performance Zroute router
- Flow Recommendation



Fast Plan-Group-Aware Zroute

- Overview
  - You can run plan-group-aware Zroute quickly on designs with
    - High congestion
    - Blocked pins
    - Non-legalized floorplan

- UI
  - `set_route_zrt_common_options -plan_group_aware_quality exploration`

Fast Plan-Group-Aware Zroute

- User Benefit
  - Should use this mode during the early design stage where there might be
    - Highly congested areas
    - Many blocked pins
    - Non-legalized (overlapping) cells
- Flow Recommendation

```
set_route_zrt_common_options
  -plan_group_aware_quality exploration
  -plan_group_aware all_routing| top_level_only
route_zrt_global
```

Summary of Design Planning Updates

Module 2

- Clock tree planning in 2010.03 enables accurate clock tree analysis
- Pin-cutting flow gives you the control to specify the exact feedthrough topology (deterministic)
- `place_fp_pins -effort high` option uses the high performance Zroute engine for pin assignment
- Use fast plan-group-aware Zroute in exploration mode in the early design stage

Predictable Success