

IC Compiler 2010.03 Incremental Training

**Design Planning:
Time Budgeting,
Hierarchy Management,
and GUI Enhancements**

Agenda



- **Timing Budgeting**
 - Support for multiply instantiated module (MIM) Designs
 - Fast time to budget
- **Hierarchy Management**
 - Cross-hierarchy push-down and push-up enhancements
- **GUI**
 - Pin analysis enhancements
 - Budgeting report

Timing Budgeting Support for Multiply Instantiated Modules

- Overview

- Enhances `allocate_fp_budgets` to consider all instances of a MIM module
- Generates one SDC file that captures the strictest constraints for all soft macros in the MIM set

- UI

- `select_mim_master_instance`
- `allocate_fp_budgets`
 - `-file_format_spec sdc/m.sdc`

Timing Budgeting Support for Multiply Instantiated Modules

- User Benefit
 - If budgeting according to master names, the tool generates only one file for each set of MIMs
 - Having one SDC file for each set of MIM soft macros allows you to run optimization only once
 - No need to run optimization several times with the different constraints generated for each MIM

MIM Virtual Flat Flow

Flow Recommendation

```
read_verilog $netlist_file
uniquify_fp_mw_cel -store_mim_property {inst_names}
report_mim
initialize_floorplan
create_fp_placement
create_plan_group
shape_fp_blocks
create_fp_placement
copy_mim -type {placement blockage}

synthesize_fp_rail
set_fp_flow_strategy -plan_group_aware_routing true
#(no feedthroughs on MIM plan groups)
set_fp_pin_constraints
route_global

optimize_fp_timing
analyze_fp_routing -finalize_pins_feedthroughs {}

select_mim_master_instance
check_fp_timing_environment
allocate_fp_budgets -file_format_spec sdc/m.sdc
check_budget_result

commit_fp_plan_groups
report_mim
```

Timing Budgeting Support for MIM

- Limitations
 - The results of the `check_fp_budget_results` command do not change when MIM budgeting is used
- Further Information
 - You can generate one file for each MIM soft macro by budgeting according to the instance names


Fast Time To Budget

- Overview
 - Achieve reasonably accurate budgets with high-fanout synthesis, feedthrough in-place optimization, and virtual in-place optimization only
 - No need to run in-place optimization in design planning
 - Multicorner-multimode and ILM flows are supported
- UI
 - `allocate_fp_budgets`
 `[-exploration]`

Fast Time To Budget

- User Benefit
 - Eliminates the need to have an optimized netlist as a budgeting prerequisite
- Flow Recommendation
 - Initial placement
 - Create plan groups
 - Hierarchical placement
 - High-fanout synthesis
 - Plan-group-aware routing
 - Finalize routing
 - Feedthrough in-place optimization
 - Virtual in-place optimization
 - `allocate_fp_budgets -exploration`
 - Commit hierarchy

Agenda

- Timing Budgeting
 - Support for multiply instantiated module (MIM) Designs
 - Fast time to budget
-  • Hierarchy Management
 - Cross-hierarchy push-down and push-up enhancements
- GUI
 - Pin analysis enhancements
 - Budgeting report


Cross-Hierarchy Push-Down and Push-Up Enhancements

- Overview
 - Many new features were added in 2010.03 to support various cross-hierarchy push-down and push-up scenarios in the hierarchical design flow
- UI
 - `push_down_fp_objects`
 - `push_up_fp_objects`

Cross-Hierarchy Push-Down and Push-Up Enhancements

- User Benefit
 - Ability to push objects up and down per layer base
 - Ability to specify a margin around the boundary of a soft macro for push down to avoid potential DRC issues when performing place and route on the soft macro
 - Ability to specify the type of the resulting object after push down – Original type or corresponding blockage type
 - Ability to push up objects that were not previously pushed down
 - Ability to push up selected child-level objects
- Flow Recommendation
 - Apply these commands after plan groups have been committed into soft macros

Agenda

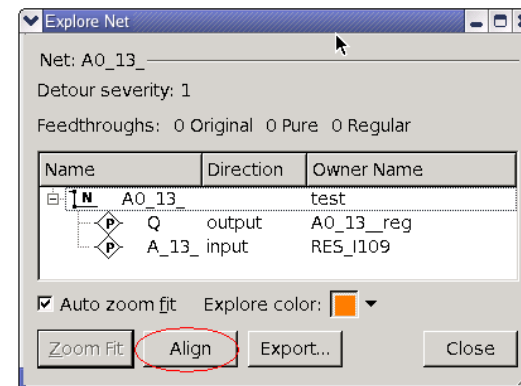
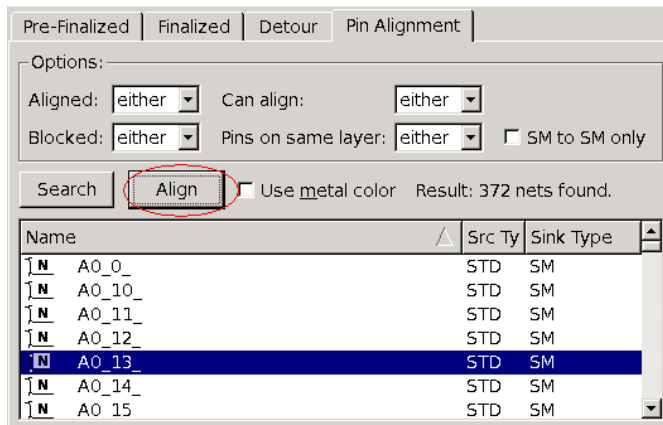
- Timing Budgeting
 - Support for multiply instantiated module (MIM) Designs
 - Fast time to budget
- Hierarchy Management
 - Cross-hierarchy push-down and push-up enhancements
-  • GUI
 - Pin analysis enhancements
 - Budgeting report

GUI: Pin Analysis Enhancements

- Overview
 - Integrated pin position update during pin alignment
 - Export and report from the pin analysis tool
 - Pin analysis tool enhancements:
 - Disjoint voltage area support
 - Annotation of voltage area names with module names
 - Annotation of signal direction on soft macro pins
 - Support check pin assignment GUI
- UI
 - Pin Assignment > Pin and Feedthrough Analysis

GUI: Pin Analysis Enhancements

- User Benefit
 - Click Align button to physically align the pin
 - Pin alignment can be performed more easily



GUI: Pin Analysis Enhancements

- User Benefit (Continued)
 - Integrated pre-finalized, finalized, detour, pin alignment, and pin assignment in one pin analysis tool

The screenshot displays the 'Pin and Feedthrough Analysis' tool interface, which is integrated with several other dialog boxes. The main window has tabs for 'Pre-Finalized', 'Finalized', 'Detour', 'Pin Alignment', and 'Pin Assignment'. The 'Finalized' tab is active, showing a list of feedthroughs with columns for Name and Results. The results for the selected item 'hvf_init1_add_34' are 676 feedthroughs found. Other tabs are also visible, showing options for 'Pre-Finalized Options', 'Finalized Options', 'Pin Alignment Options', and 'Pin Assignment Options'. The 'Pin Assignment Options' dialog is open, showing settings for 'Block level check', 'Macro objects to check pins', 'Macro types', 'Nets to check pins', 'Pin types', and 'Check for'.

Pre-Finalized Options

- All nets Specified: []
- Specified blocks: []
- Buttons: OK, Cancel, Apply, Default

Finalized Options

- Specified nets: []
- Specified pins: []
- All nets All feedthroughs All non-feedthroughs
- Specified blocks: []
- Bus nets only
- Buttons: OK, Cancel, Apply, Default

Pin and Feedthrough Analysis

Analysis mode: Blocks Voltage areas Buffered feedthrough

Pre-Finalized | **Finalized** | Detour | Pin Alignment | Pin Assignment

Results: 676 feedthroughs nets found.

Name	Results
avail_space10	
avail_space7	
avail_space_sn11	
avail_space_sn8	
hvf_init1_add_34	676
hvf_init1_add_3_sn5	
hvf_init1_opc4[0]	
hvf_init1_opc4[4]	
hvf_init1_opc4[5]	

Show status columns Show detour bbox

Remove Feedthroughs Remove original also

Zoom and coloring

Color Auto color [] Clear All

Zoom Fit Auto zoom fit Exclude child net

Explore Net window

Select Export... Report...

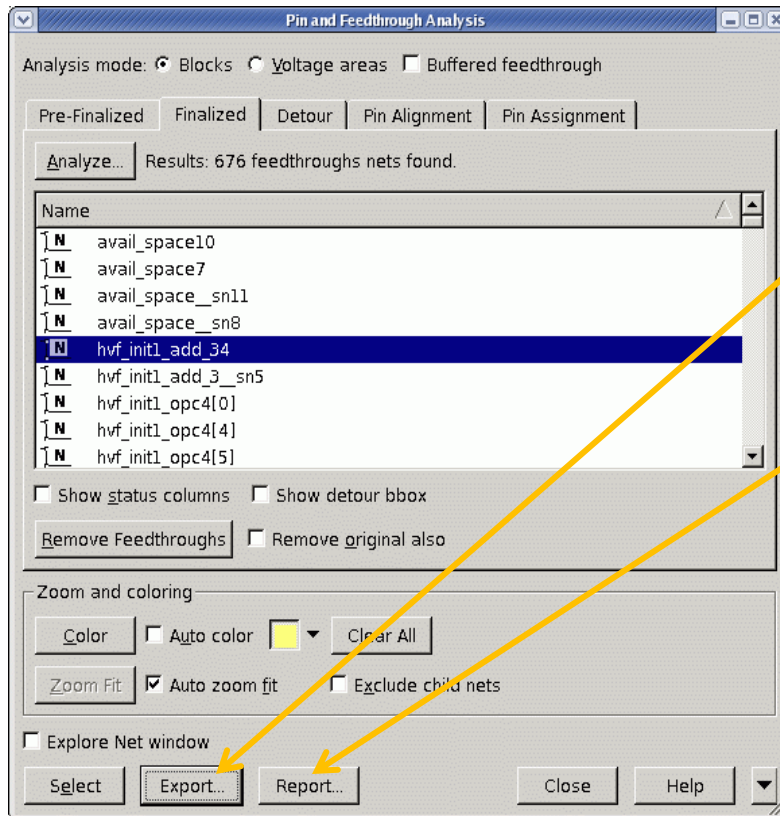
Pin Assignment Options

- Block level check
- Macro objects to check pins: All Specified
- Macro types: All Soft macro only Hard macro only
- Nets to check pins: All Specified
- Pin types: All Signal P/G
- Check for:
 - Spacing between signal pins
 - Spacing between preroute and pins
 - Pins overlapped on same layers
 - Pins on legal layers
 - Pins overlapped on across layers
 - Pins not centered on wire track
 - Missing signal pins
 - Off edge pins
 - Pins outside pin guide
 - Imperfect pin abutment/overlap
 - Pins with user-specified routing constraints
 - Non-routable pins on abutted edges

Buttons: OK, Cancel, Apply, Default

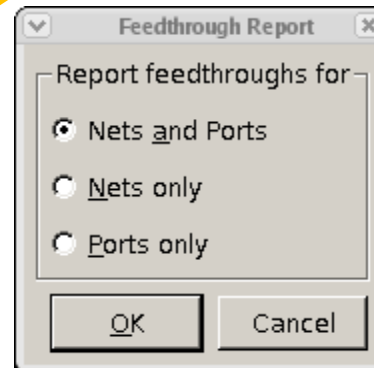
GUI: Pin Analysis Enhancements

- User Benefit (Continued)
 - Export and report from pin analysis tool



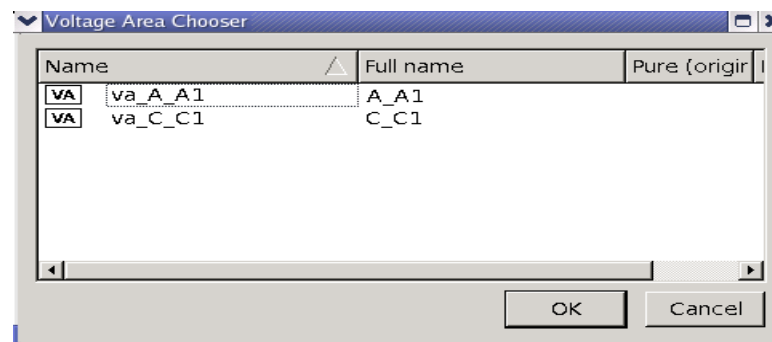
Click Export: IC Compiler displays a window for entering a file name that will store the listed feedthrough nets

Click Report: IC Compiler displays the following window and triggers different report-generating Tcl commands



GUI: Pin Analysis Enhancements

- User Benefit (Continued)
 - Pin analysis tool enhancements:
 - Disjoint voltage area support
 - Correctly process and display connections to / feedthroughs across disjoint voltage areas
 - Voltage area names are annotated with the module names



GUI: Pin Analysis Enhancements

- User Benefit (Continued)
 - Pin analysis tool enhancements:
 - Annotation of signal direction on soft macro pins
 - In the layout view, a soft macro pin is annotated so that the signal direction of the pin is clearly visible
 - » Example:
 - On the top of the pin there is one of the following marks:
 - 'O' if the pin is an output pin
 - 'I' if the pin is an input pin
 - 'IO' if the pin is an input-output pin

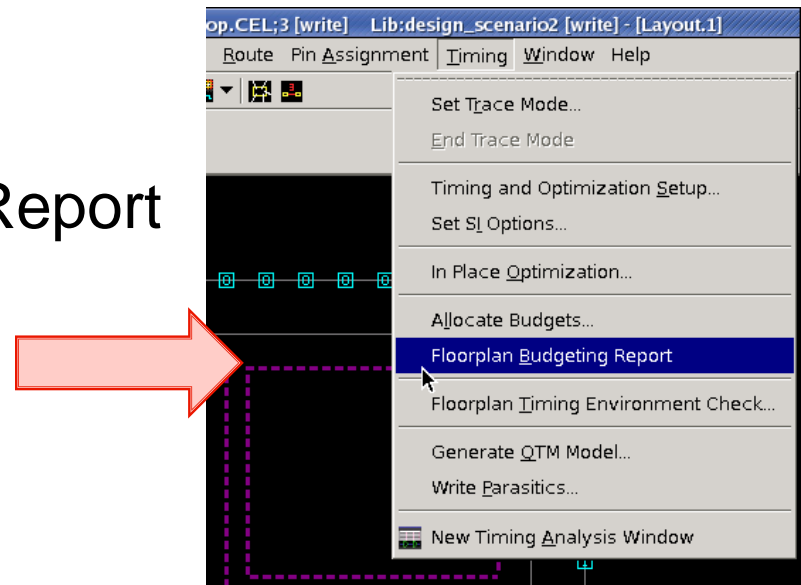
GUI: Pin Analysis Enhancements

- Flow Recommendation
 - The pin analysis tool can be used
 - After plan-group-aware routing (PGAR)
(`route_zrt_global`)
 - After finalizing the routing
(`analyze_fp_routing -finalize {plan_groups}`)
 - After committing the hierarchy
(`commit_fp_plan_groups`)

GUI: Budgeting Report

- Overview
 - Checks the budgeting result using the GUI
 - The GUI tool is implemented based on the `check_fp_budget_result` command

- UI
 - Timing > Floorplan Budgeting Report



GUI: Budgeting Report

- User Benefit
 - The analysis report breaks down the paths into segments corresponding to each hierarchy block
 - Helps to analyze the budgeting results
- Flow Recommendation
 - Run the budgeting report following the timing budgeting command

GUI: Budgeting Report

- Example
 - Report one block budgeting
 - Cross-path highlighting

The screenshot displays the Synopsys GUI with a 'BudgetingReportWindow.1 - budget - [TimingBudgetingCheckReport.1]' window open. The window has a menu bar (File, Edit, View, Highlight, Select, Report, Window, Help) and a toolbar. Below the toolbar, there are two radio buttons for budgeting options: 'Check budget from command: check_fp_budget_result' (selected) and 'Check budget by selecting pin delay ranges of the blocks:'. The first option has a 'Set options' button and a text field containing '-blocks {T/L1} -delay max'. The second option has a 'Load table' button. Below these are several filter buttons: 'Block Name', 'Pins (Delay<20%)', 'Pins (20%<Delay<40%)', 'Pins (40%<Delay<60%)', 'Pins (60%<Delay<80%)', and 'Pins (80%<Delay<100%)'. A 'Report' button is located below the filters. The main area of the window is divided into two tables. The left table, titled 'Paths of budgeted target pin on its delay:', has columns: 'Path Name', 'Target Pin', 'Direction', and 'In/Out'. It contains the following data:

Path Name	Target Pin	Direction	In/Out
3 path4	T/L1/2ct_en	IN	0.67
4 path5	T/L1/sync_reset_n	IN	0.70
5 path6	T/L1/sync_reset_n	IN	0.70
6 path7	T/L1/SFEIbreap	OUT	0.96

The right table, titled 'Hier-pins list of paths:', has columns: 'HierPin Name', 'Is Target Pin', 'Type', 'Real Delay', and 'Budget'. It contains the following data:

HierPin Name	Is Target Pin	Type	Real Delay	Budget
paths				

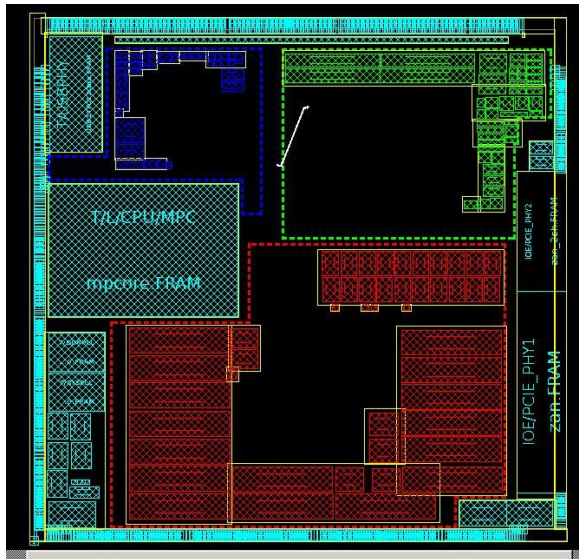
Below the tables is a 'Path Inspector' section with a 'Close' button. At the bottom of the window, there is a 'ready' status bar and a 'Path' dropdown menu showing 'SEL/count_reg_5_D'. The background of the GUI shows a circuit schematic with various blocks and connections. A specific path is highlighted in red, and a block labeled 'mpcore_FRAM' is visible. A legend on the left side of the GUI lists various components with checkboxes and color-coded boxes.

GUI: Budgeting Report

- Example

- All blocks can be reported together
- Pin delay range

The screenshot shows the 'BudgetingReportWindow.1' interface. At the top, there are menu options: File, Edit, View, Highlight, Select, Report, Window, Help. Below the menu is a toolbar with various icons. The main area contains a table with columns for 'Block Name', 'Pins (Delay<20%)', 'Pins (20%<Delay<40%)', 'Pins (40%<Delay<60%)', 'Pins (60%<Delay<80%)', and 'Pins (80%<Delay)'. The table lists three blocks: T/LI, T/LP, and T/LS. The 'Pins (20%<Delay<40%)' column for T/LP has a checked checkbox. Below the table is a 'Report' button. To the right of the table, there are two sections: 'Paths of budgeted target pin on its delay:' and 'Hier-pins list of paths:'. The 'Paths of budgeted target pin on its delay:' section contains a table with columns: 'Path Name', 'Target Pin', 'Direction', and 'In/Out Delay'. The table lists paths from 0 to 10, with 'path8090' highlighted in blue. The 'Hier-pins list of paths:' section shows a tree view with 'path8090' selected. At the bottom, there is a 'Path Inspector' button and a 'Close' button. The status bar at the bottom shows 'Ready' and the current path: 'Path ... turedPixel_reg_1_D'.



GUI: Budgeting Report

- Limitations
 - Timing budgeting and the budgeting report must be run in the same session

Summary of Design Planning Updates

Module 3

- MIM support added for generating timing budgets (`allocate_fp_budgets`)
- Budgeting support in exploration mode
- Enhancements that enable you to push objects up/down objects after plan groups are committed into soft macros
- Integrated Pin & Feedthrough Analysis GUI tool
- The GUI budgeting reporting tool and how it helps you to analyze budgeting results

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