Synthesis
Error Messages

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SYNOPSYS®

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ACS-100 (error) The program cannot find all Automated Chip Synthesis (ACS) initialization files.

DESCRIPTION

You receive this message because the program did not find all files that are necessary for proper initialization. The Synopsys software installation is incomplete or corrupted.

WHAT NEXT

Reinstall the software to fix the problem. You can continue working with the current installation, although some ACS functionality is not available.

ACS-101 (error) %s

DESCRIPTION

You receive this message because an error occurs when the **acs_read_hdl** command is scanning through the source files to detect interfile dependencies. It has found either a syntax error or an unsupported construct.

WHAT NEXT

Fix the syntax error or work around the unsupported construct. Another way to avoid this error message is to run the **acs_read_hdl** command with the **-no_dependency_check** option. This omits dependency checking so you should specify all source files in the proper order. For Verilog source, this means that files included by any other file should not appear in the **hdl_source** list. VHDL files defining any library objects should be specified before any files using those objects.

SEE ALSO

acs_read_hdl (2).

ACS-102 (error) Internal error: The '%s' command is not

available.

DESCRIPTION

You receive this message because an internal error occurred during the initialization phase. The described Automated Chip Synthesis (ACS) command could not be registered with the shell. It is not available. This error should not occur under normal circumstances.

WHAT NEXT

Reinstall the software to fix the problem. You can continue working with the current installation, although the described ACS functionality is not available.

ACS-103 (error) Internal error: Some Automated Chip Synthesis (ACS) functions are not available.

DESCRIPTION

You receive this message because an internal error occurred during the initialization phase. An ACS command could not be registered with the shell. Some ACS functionality will not be available. This error should not occur under normal circumstances.

WHAT NEXT

Reinstall the software to fix the problem. You can continue working with the current installation, although you should not use any ACS commands.

ACS-104 (error) The above libraries are not readable.

DESCRIPTION

You receive this message because the specified design libraries are used in the design, but are not currently mapped to a valid directory name.

WHAT NEXT

Use the **define_design_lib** command to create a new design library. The directory to which the library is mapped must exist and should have read permissions set. To analyze HDL source files into a specific library, the directory to which the library is mapped should also have write permissions set.

SEE ALSO

acs_read_hdl (2), **analyze** (2), **define_design_lib** (2), **get_design_lib_path** (2).

ACS-105 (error) Cannot access file '%s'.

DESCRIPTION

You receive this message because an attempt failed to retrieve information about the specified file from the operating system.

WHAT NEXT

In most cases this error should not cause any problems. However, if the specified file is an include file, it may be analyzed and cause analyzer errors. If you run the command again, the error should not reoccur.

ACS-106 (information) The file '%s' appears more than once in the source file list. Ignoring all further occurrences.

DESCRIPTION

You receive this message because you specified an HDL source file more than once in the source file list of the **acs_read_hdl** command. It is analyzed only once.

SEE ALSO

acs_read_hdl (2).

ACS-107 (information) All use statements of the form 'use <LIB>.all' are ignored during dependency checking.

DESCRIPTION

The **acs_read_hdl** command attempts to detect interfile dependencies to analyze files in the correct order. You receive this message because the above statement creates a dependency that is too general to be of any use. Thus it is ignored.

WHAT NEXT

If the **acs_read_hdl** command cannot resolve all dependencies and analysis of the source code fails, it may help if you replace 'use <lib>.all' statements with more-specific 'use <lib>.<package>' statements in the HDL source code.

SEE ALSO

acs_read_hdl (2).

ACS-108 (error) Cyclic dependencies are detected in the above source files.

DESCRIPTION

The **acs_read_hdl** command attempts to detect interfile dependencies to analyze source files in the correct order. Definitions of library objects must be analyzed before the object is used.

You receive this message because this is not possible for all library objects with the current source files. The above list shows the cyclic dependency in the files.

WHAT NEXT

Change your source files and move object definitions so that the files can be analyzed correctly. The above list gives hints about the files and library objects that are involved in the cyclic dependency. There are some implicit dependencies, such as a package body that depends on its package definition or an architecture that depends on its entity. Use of a package implies a dependency on the package body.

SEE ALSO

acs_read_hdl (2).

ACS-109 (error) Library object(s) are multidefined.

DESCRIPTION

The list above this error message shows all library objects that are defined in more than one file and the corresponding filenames. You receive this message because it is not clear which definition to use.

WHAT NEXT

Modify the source files, deleting all definitions except one for each multidefined object, or remove the source files containing the additional definitions from the source file list.

ACS-110 (error) Multiple architectures are defined for one entity.

DESCRIPTION

The list above this error message shows all files defining architectures for each entity with multiple architectures. You receive this message because it is not clear which architecture to use.

WHAT NEXT

Modify the source files, deleting all architecture definitions except one for each entity, or remove the source files containing the extra architecture definitions from the source file list.

ACS-111 (error) You cannot specify -recursive when using the search_path as a Verilog source file list.

DESCRIPTION

You receive this message because using the **-recursive** option in conjunction with the **search_path** variable can cause unexpected behavior. For the command to recursively look for source code files in directories, you cannot use the **search_path** variable to specify the same directories.

WHAT NEXT

Use the **acs_hdl_source** variable or the **-hdl_source** option to specify the source directories (using the **-recursive** option, if needed), and include the names of all include directories in the **search_path** variable.

SEE ALSO

acs_hdl_source (3).

ACS-112 (error) Cannot detect source language of file '%s'.

DESCRIPTION

You receive this message because the specified file occurs in the HDL source list, but has none of the language-specific extensions. The **acs_read_hdl** command cannot determine the source language of the file, because the **-format** option is not set.

WHAT NEXT

Do either of the following:

• Specify the **acs_read_hdl** command with the **-format** option. A side effect of this is that it analyzes only Verilog or VHDL files (with an extension from the corresponding **acs_verilog_extensions** or **acs_vhdl_extensions** variable).

• Add the extension of the identified file to one (or both) of the **acs_verilog_extensions** and **acs_vhdl_extensions** variables to indicate the source language. This causes all files with this extension to be analyzed, not only the one specified above.

SEE ALSO

acs_read_hdl (2), **acs_verilog_extensions** (3), **acs_vhdl_extensions** (3).

ACS-113 (error) File '%s' is specified twice in the HDL source files list.

DESCRIPTION

You receive this message because you explicitly specified the mentioned file twice in the HDL source files list for the **acs_read_hdl** command. If you have symbolic links in your source directories, different paths may specify the same file.

WHAT NEXT

Remove the specified filename from the HDL source files list.

SEE ALSO

acs_read_hdl (2).

ACS-114 (warning) No source files are found for '%s'.

DESCRIPTION

You receive this message because you specified an item in the HDL source files list that could not be expanded to any filename. If the specified item is a file, that file was not found; if it is a directory, that directory does not contain any source files.

WHAT NEXT

You can ignore the warning if all of your source files have been analyzed. Remove the specified HDL source list item from the HDL source files list to eliminate this warning. If the **acs_read_hdl** command has found source files matching the expression, check the syntax of that item, and check the **acs_exclude_extensions**, **acs_exclude_list**, **acs_verilog_extensions**, and **acs_vhdl_extensions** Tcl variables.

SEE ALSO

acs_read_hdl (2), **acs_exclude_extensions** (3), **acs_exclude_list** (3), **acs_verilog_extensions** (3), **acs_vhdl_extensions** (3).

ACS-115 (error) No input files specified.

DESCRIPTION

You receive this message because you specified an empty HDL source file list.

WHAT NEXT

Set the **acs_hdl_source** Tcl variable to a non-empty list of file and directory names or specify that list by using the **-hdl_source** option at the command line.

SEE ALSO

acs_read_hdl (3).

ACS-116 (error) No top-level module name specified.

DESCRIPTION

You receive this message because the command requires the name of the top-level module to elaborate the design.

WHAT NEXT

Specify the top-level module name at the command line. You can also set the **-no_elaborate** option, which prevents the **acs_read_hdl** command from performing elaboration.

SEE ALSO

acs_read_hdl (2).

ACS-117 (error) An error or unsupported construct is detected during the Verilog include file detection phase.

DESCRIPTION

You receive this message because an error or unsupported construct was detected during the Verilog include file detection phase. It is also possible that all specified source files are include files so no files are left to be analyzed.

WHAT NEXT

Correct all syntax errors or work around unsupported constructs, and rerun the command. Another workaround for this error message is to use the **acs_read_hdl** command with the **-no_dependency_check** option. This prevents the command from detecting Verilog include files; however, you have to manually remove all include files from the HDL source files list.

SEE ALSO

acs_read_hdl (2).

ACS-118 (warning) Mixed language designs are not automatically elaborated.

DESCRIPTION

You receive this message because the tool has implicitly set the **-no_elaborate** flag, since it cannot elaborate a design that has Verilog and VHDL source code parts.

WHAT NEXT

After the command finishes you must manually do the elaboration. Execute the **elaborate** command separately for each top-level module of each language, doing the

design top-level module last.

SEE ALSO

acs_read_hdl (2), **elaborate** (2).

ACS-119 (information) Automated Chip Synthesis (ACS) is analyzing Verilog file '%s'.

DESCRIPTION

You receive this message because The **acs_read_hdl** command is describing its activity.

WHAT NEXT

No action is necessary. The result is informative. Remove the**-verbose** option from the command line if you prefer not to view these messages,

SEE ALSO

acs_read_hdl (2), **analyze** (2).

ACS-120 (information) Automated Chip Synthesis (ACS) is analyzing VHDL file '%s' into lib '%s'.

DESCRIPTION

You receive this message because the **acs_read_hdl** command is describing its activity.

WHAT NEXT

No action is necessary. The result is informative. Remove the**-verbose** option from the command line if you prefer not to view these messages,

SEE ALSO

acs_read_hdl (2), **analyze** (2).

ACS-121 (error) No files have been analyzed.

DESCRIPTION

You receive this message because either you have not specified an HDL source files list or the **acs_read_hdl** command has not found any source files in the specified locations.

WHAT NEXT

Include all directories containing source files in the HDL source files list, and properly set the exclude and extensions variables.

SEE ALSO

acs_read_hdl (2).

ACS-122 (warning) Analyzer ended with errors.

DESCRIPTION

You receive this message because analyzer ended for one or more files with errors. You used the **-ignore_analyze_errors** option at the command line, so this message informs you only that one or more errors occurred and does not describe the errors.

WHAT NEXT

Ignore this message or fix the problems that generated the errors and rerun the command.

SEE ALSO

acs_read_hdl (2).

ACS-123 (information) Automated Chip Synthesis (ACS) is elaborating module '%s'.

DESCRIPTION

You receive this message because the **acs_read_hdl** command is describing its activity.

WHAT NEXT

No action is necessary. The result is informative. Remove the**-verbose** option from the command line if you prefer not to view these messages,

SEE ALSO

acs_read_hdl (2), **elaborate** (2).

ACS-124 (error) More than one module with name '%s' found.

DESCRIPTION

You receive this message because you specified a top-level module name that is not unique. Another design has the same name in memory. The current design cannot be set. The GTECH result of the **acs_error_user** command is still in memory.

WHAT NEXT

Ensure that the **current_design** variable is set to the top-level module of your design.

SEE ALSO

acs_read_hdl (2), **current_design** (3).

ACS-125 (warning) The command line argument '%s' overrides the Tcl variable '%s'.

DESCRIPTION

You receive this message because you have assigned a value to the specified Tcl variable and you are providing an option at the command line that specifies the same thing. This warning just informs you that the **acs_read_hdl** command ignores the value of the Tcl variable.

WHAT NEXT

Nothing to do, if this doesn't surprise you.

SEE ALSO

acs_read_hdl(2).

ACS-126 (error) Invalid file or directory name: ’%s’ is ignored.

DESCRIPTION

You receive this message because you specified an invalid item in a file list. The invalid expression is specified in the message. The invalid item is ignored.

WHAT NEXT

This error message may be caused by an unknown user (in a "~<user>" expression) or an inaccessable current working directory (if you specified "."). You do not have to take any action unless you require the ignored expression as part of your specification of the source code location.

SEE ALSO

acs_read_hdl (2).

ACS-127 (error) Invalid extension: ’%s’ is Ignored.

DESCRIPTION

You receive this message because you used an invalid extension in one of the extensions lists. The invalid extension is specified in the message and is ignored. The slash character (/) and backslash character (\) are not allowed in extensions.

WHAT NEXT

Remove the invalid extension from the list. If you actually have a source code file with a slash or backslash character in the extension you must rename it.

SEE ALSO

acs_read_hdl (2).

ACS-128 (information) ACS is starting Verilog include file detection.

DESCRIPTION

You receive this message because the Automated Chip Synthesis (ACS) **acs_read_hdl** command is reporting its current activity: starting Verilog include file detection.

SEE ALSO

acs_read_hdl (2).

ACS-129 (information) ACS is starting VHDL dependency extraction.

DESCRIPTION

You receive this message because the Automated Chip Synthesis (ACS) **acs_read_hdl** command is reporting its current activity: starting VHDL dependency extraction.

SEE ALSO

acs_read_hdl (2).

ACS-130 (information) ACS is starting Verilog analysis.

DESCRIPTION

You receive this message because the Automated Chip Synthesis (ACS) **acs_read_hdl** command is reporting its current activity: starting Verilog analysis.

SEE ALSO

acs_read_hdl (2).

ACS-131 (information) ACS is starting VHDL analysis.

DESCRIPTION

You receive this message because the Automated Chip Synthesis (ACS) **acs_read_hdl** command is reporting its current activity: starting VHDL analysis.

SEE ALSO

acs_read_hdl (2).

ACS-132 (error) DC-Expert license for ACS is not enabled.

DESCRIPTION

You receive this message because the license feature DC-Expert is not available. Every Automated Chip Synthesis (ACS) command checks it.

ACS-133 (error) No additional DC-Expert licenses are available.

DESCRIPTION

You receive this message because all your licenses are already checked out. The command you executed failed to retrieve one.

Each dc_shell using an Automated Chip Synthesis (ACS) command checks out one license of the DC-Expert feature. Other commands might also be using this license feature.

WHAT NEXT

Do one of the following, and then try again to execute the command:

- Quit any other dc_shell that uses DC-Expert licenses.
- Wait until any other dc_shell that uses DC-Expert licenses is done.
- Obtain more licenses.

ACS-134 (information) Starting Design Compiler Design Budgeting.

DESCRIPTION

You receive this message to inform you that Design Compiler (DC) is reporting its current activity: starting Design Budgeting.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

acs_compile_design (2), **acs_refine_design** (2).

ACS-135 (information) Starting PrimeTime Design Budgeting.

DESCRIPTION

You receive this message because PrimeTime is reporting its current activity: starting Design Budgeting.

SEE ALSO

acs_compile_design (2), **acs_refine_design** (2).

ACS-136 (error) Variable '%s' must be a value between 0 and 100.

DESCRIPTION

You receive this message because the variable value is not between 0 and 100.

SEE ALSO

set_compile_partitions (2).

ACS-137 (warning) The current design contains less than %d levels of hierarchy.

DESCRIPTION

You receive this message because you used the **-level** option to specify where to set the compile partitions on the design, but the number of hierarchy levels in the design is less than the specified value.

WHAT NEXT

Take either of the following actions:

• Specify a different hierarchy level (a lower number) that contains instances with the **-level** option.

• Use a different option to specify where to set compile partitions. For detailed information, see the **set_compile_partitions** man page.

SEE ALSO

acs_compile_design (2), **set_compile_partitions** (2).

ACS-138 (error) Unresolved Multiple Instances.

DESCRIPTION

You receive this message because there are multiply-instantiated modules in the design and the settings of the **MasterInstance** attribute are not correct.

WHAT NEXT

See the **MasterInstance** man page or the *Automated Chip Synthesis, User Guide* for more detailed information. If the directions you find there for resolving this problem are not acceptable, take one of the following actions:

• Uniquify the design.

• Set the **MasterInstance** attribute on exactly one instance of each multiply-instantiated design.

• Set the **dont_touch** attribute on the multiply-instantiated design.

• Set the **dont_touch** attribute on all but one instance of the multiply-instantiated design.

SEE ALSO

remove_attribute (2), **set_attribute** (2), **sub_designs_of** (2), **sub_instances_of** (2), **uniquify** (2), **MasterInstance** (3).

ACS-139 (error) Design '%s' is not part of the current design.

DESCRIPTION

You receive this message because the command works only with modules that are linked to the *current design*. The **current_design** command is set to a design that, within its hierarchy, does not instantiate the specified design.

WHAT NEXT

Perform one of the following tasks:

- Call the command with a design that is part of the *current design*.
- Set the **current_design** command to a parent module of the specified design.
- Set the **current_design** command to the design itself.

SEE ALSO

current_design (2), **link** (2), **sub_designs_of** (2), **sub_instances_of** (2).

ACS-140 (warning) MasterInstance of module '%s' is not found in design '%s' children. Randomly choosing '%s' instance instead.

DESCRIPTION

You receive this message because you specified the **-master_only** command line option, but one of the following conditions applies to the instance that has the **MasterInstance** attribute set:

- It is not a child of the specified design.
- It is not in the design subtree (if the **-hierarchy** option was set).
- The master instance does not qualify with respect to the other options (for example like **-dt_only** or **-ndt_only**).

The command returns an instance representing the module, but it is not the master instance.

WHAT NEXT

Do one of the following:

- Specify a design that has the master instance of the specified module in its subtree
- Change the other command line options so that the master instance is not filtered out.
- Change the **MasterInstance** attribute settings.

SEE ALSO

find (2), **remove_attribute** (2), **report_attribute** (2), **set_attribute** (2), **sub_designs_of** (2), **sub_instances_of** (2), **MasterInstance** (3).

ACS-141 (warning) Multiple master instances found for design '%s': '%s' and '%s'. Randomly choosing '%s' instance.

DESCRIPTION

You receive this message because you specified the **-master_only** command line option, and the command found two instances of the same design that have the **MasterInstance** attribute set. This compromises the concept of the master instance, which is that you can have only one.

WHAT NEXT

Remove the **MasterInstance** attribute from one of the specified instances.

SEE ALSO

find (2), **remove_attribute** (2), **report_attribute** (2), **set_attribute** (2), **sub_designs_of** (2), **sub_instances_of** (2), **MasterInstance(3).**

ACS-142 (error) Multiple designs are found matching the '%s' name.

DESCRIPTION

You receive this message because you specified a name that is not unique.

WHAT NEXT

When designs with identical names are loaded into memory, the filename is added to the design name to make it unique. You can use the **find** and **get_designs** commands to determine the unique name of the design that you want to specify.

SEE ALSO

find (2), **get_designs** (2).

ACS-143 (error) No parent partition found in the current design

for design '%s'.

DESCRIPTION

You receive this message because you need to set your compile partitions in order for this command to work properly, and the current_design has to be set to a design that has partitions in its subhierarchy (or is a partition itself).

WHAT NEXT

Set the compile partitions on the current design, or set the *current design* to a design (preferably the top level module) that has partitions in its design subtree.

SEE ALSO

current_design (2), **report_partitions** (2), **set_compile_partitions** (2), **sub_designs_of** (2).

ACS-144 (error) Multiply-instantiated design '%s' is not a compile partition.

DESCRIPTION

You receive this message because the specified design is a parent module in the logical hierarchy of the module for which you want to find the parent partition. It is impossible to find the parent partition as it might be different for the different instances. The design is multiply-instantiated, but is not marked as partition. This should not happen if the compile partitions are correctly set.

WHAT NEXT

Correctly set the compile partitions on the current design. This entails either of the following:

- The design must be made unique by using the **uniquify** command.
- All multiply-instantiated designs and the top level module must be partitions, and an instance must be picked as master instance.

SEE ALSO

acs_get_parent_partition (2), **current_design** (2), **report_partitions** (2), **set_compile_partitions** (2), **uniquify** (2), **MasterInstance** (3).

ACS-145 (error) Directory %s, which should contain the mapped design, does not exist.

DESCRIPTION

You receive this message because the directory which should contain the mapped designs does not exist. This is either the default directory (pass0) or a directory you specified by using the **-mapped** and **-type** options of the **acs_merge_design** command. The program cannot merge the designs in the process of being updated into the mapped designs.

WHAT NEXT

Use the **acs_merge_design** command with the **-mapped** option at the command line to specify a directory for the mapped designs.

SEE ALSO

acs_merge_design (2).

ACS-146 (error) No unique top design '%s' after merge from unmapped directory '%s'.

DESCRIPTION

You receive this message because after the merge from the directory specified by the -**unmapped** option (default: elab/db) to the design specified by the -**mapped** option (default: pass0) there does not exist a unique top design. Either there is no top design at all because the unmapped directory does not contain this design, or there are several top designs with the same name because there are several db files in the unmapped directory containing the top design.

WHAT NEXT

Ensure that in the unmapped directory there exists a complete unique design database containing exactly one version of the top design.

SEE ALSO

acs_merge_design (2).

ACS-147 (warning) Previous partition '%s' does not have

a corresponding design after the merge.

DESCRIPTION

You receive this message because the design specified by the **-mapped** option of **acs_merge_design** command contained a partition whose associated design does no longer exists in the design hierarchy after merging the updated designs. Thus, the previous partition will no longer be present in the updated design. This can happen if your design updates contains changes to the design hierarchy, e.g. if you have ungrouped or flattened some design within the updated design part.

WHAT NEXT

No action is necessary if this is what you expected. However, after major changes to the design hierarchy it is recommended to re-partition the design and map it from scratch using **acs_compile_design**.

SEE ALSO

acs_merge_design (2).

ACS-148 (error) The top design '%s' does not link after merging updates from directory '%s' specified by the -unmapped option (elab/db by default).

DESCRIPTION

You receive this message because the design does not link completely after the **acs_merge_design** command has merged in the updated designs from the directory specified by the **-unmapped** option (elab/db by default).

WHAT NEXT

Ensure that the specified unmapped design directory contains a complete design database for the top design which is consistent with the mapped design specified by option '-mapped' for acs_merge_design.

SEE ALSO

acs_merge_design (2).

ACS-149 (warning) Designs are merged into mapped designs

in default mapped path %s.

DESCRIPTION

You receive this message because you did not use the **-mapped** option of the **acs_merge_design** command in the command line to provide a directory for the mapped designs. This warning message informs you that the program is using the default directory for the mapped designs.

WHAT NEXT

No action is necessary, if this is what you expected.

SEE ALSO

acs_merge_design (2).

ACS-150 (warning) Using unmapped designs in default directory elab/db.

DESCRIPTION

You receive this message because you did not use the **-unmapped** option of the **acs_merge_design** command in the command line to provide a directory for the unmapped designs and designs being merged. This warning message informs you that the program is using the default directory for the unmapped designs.

WHAT NEXT

No action is necessary, if this is what you expected.

SEE ALSO

acs_merge_design (2).

ACS-151 (warning) MasterInstance of the ’%s’ module is not found.

Randomly choosing the '%s' instance instead.

DESCRIPTION

You receive this message because you specified the **-master_only** command line option, but the instance that has the **MasterInstance** attribute set is not found for the specified module.

WHAT NEXT

Perform one of the following tasks:

- Specify a module that has a master instance.
- Change the **MasterInstance** attribute settings on one of the instances of the specified module.

SEE ALSO

find (2), **remove_attribute** (2), **report_attribute** (2), **set_attribute** (2), **sub_instances_of** (2).

ACS-152 (warning) Report for design %s might not be valid.

DESCRIPTION

You receive this message because the ACS compile flow is a bottom-up compile. At the end of the compile on the top level design, the **compile** command is run with the **-top** option, which might cause changes in subpartitions. Thus, reports generated immediately after the compile of the subpartitions might be invalid after running after **compile -top**.

WHAT NEXT

You can either choose not to use custom report scripts on subpartitions, or choose to ignore the warning message, but consider that the subpartition reports you have might be invalid.

ACS-153 (warning) No area estimation numbers are available

yet.

DESCRIPTION

You receive this message because the **report_partitions** command has been executed before any area estimation has been done. Area estimation is performed only by the "auto partitioning" command, which is the **-auto** option of the **set_compile_partitions** command. At this time the report of the design partitions shows only zeros in the percentage column.

WHAT NEXT

No action is necessary, if this is what you expected. However, if it is necessary to get useful percentage numbers, run the **set_compile_partitions** command with the **-auto** option.

SEE ALSO

report_partitions (2), **set_compile_partitions** (2).

ACS-154 (error) Cannot open file '%s' for reading.

DESCRIPTION

You receive this message from the **acs_read_hdl** command because the tool is unable to open (or read data or text from) the named file in the message.

WHAT NEXT

Verify the existence and correct spelling of the file you specified and that you have read privileges to this file and all directories leading to it. Also check to confirm that you spelled correctly the path to the file. Make any necessary corrections. Then run the **acs_read_hdl** command again.

SEE ALSO

acs_read_hdl (2).

ACS-155 (information) Expanding the search_path with '%s'.

DESCRIPTION

You receive this message from the **acs_read_hdl** command to let you know that, because

Automated Chip Synthesis (ACS) detects that HDL Analyzer might not be able to locate some of the HDL files you listed in the **search_path** variable, ACS is appending one or more paths to the variable.

If you specified the **-recurse** option of the **acs_read_hdl** command, the tool might see more Verilog include files than the **analyze** command sees, because the **analyze** command does not search recursively the directories of the files listed in the **search_path** variable.

This automatic expansion of the search path eliminates your having to enter manually into the **search_path** variable all paths to Verilog include files.

WHAT NEXT

This message is informational only and requires no action on your part.

SEE ALSO

acs_read_hdl (2), **analyze** (2); **search_path** (3).

ACS-156 (information) Found %d include files in the search_path matching '%s'.

DESCRIPTION

You receive this message from the **acs_read_hdl** command to inform you that Automated Chip Synthesis (ACS) has encountered an include Verilog preprocessor directive that gives the file name of the include file but does not specify the path to the include file.

After searching all directories in the order in which they are listed in the **search_path** variable, the tool has found more than one file with the same name as that given in the preprocessor directive. ACS is assuming that the first matching file is the one you want to include.

WHAT NEXT

This message is informational only and requires no action on your part. However, because the Design Compiler **analyze** and **read_verilog** commands will show the same behavior, and because the behavior of these commands is always implementation- and release-dependent, it is no doubt wise to identify the correct path information and add it to the preprocessor directive. Then run the **acs_read_hdl** command again.

SEE ALSO

acs_read_hdl (2), **analyze** (2); **search_path** (3).

ACS-157 (warning) Could not locate include file %s, included by file %s.

DESCRIPTION

You receive this message from the **acs_read_hdl** command because Automated Chip Synthesis (ACS) encountered an include Verilog preprocessor statement that does not specify a path to the include file.

ACS first tries to locate the file by searching all the directories listed in the **search_path** variable. If this search is not successful, ACS then searches all of the directories of all files listed in the **-hdl_source** option (if defined) of **acs_read_hdl**.

If you also specified the **-recurse** option of **acs_read_hdl**, ACS searches further all of the subdirectories of all the files listed in the **-hdl_source** option of **acs_read_hdl**.

The **-recurse** option of **acs_read_hdl** does not search all subdirectories listed in the **search_path** variable, however. (In this respect, the command mimics the behavior of the **analyze** and **read_verilog** commands.)

After searching all of these directories, ACS did not find the missing include file.

WHAT NEXT

This warning message alerts you to a possible conflict, which, if not resolved, might prevent a later **analyze** command being able to find the include file, resulting in an error.

To ensure a smooth process here, it is no doubt preferable to locate and identify the correct include file and add its path to the statement or to the **search_path** variable. Then run the **acs_read_hdl** command again.

SEE ALSO

acs_read_hdl (2), **analyze** (2); **search_path** (3).

ACS-158 (warning) Found more than one matching include file %s, wanted by file %s.

DESCRIPTION

You receive this message from the **acs_read_hdl** command because Automated Chip Synthesis (ACS) encountered an include Verilog preprocessor statement that does not specify a path to the include file.

ACS first tries to locate the file by searching all the directories listed in the **search_path** variable. If this search is not successful, ACS then searches all of the directories of all files listed in the **-hdl_source** option (if defined) of **acs_read_hdl**.

If you also specified the **-recurse** option of **acs_read_hdl**, ACS searches further all of the subdirectories of all the files listed in the **-hdl_source** option of **acs_read_hdl**.

The **-recurse** option of **acs_read_hdl** does not search all subdirectories listed in the **search_path** variable, however. (In this respect, the command mimics the behavior of the **analyze** and **read_verilog** commands.)

Although ACS could not find the include file in the directories listed in the **search_path** variable, it did locate, by searching all directories (and possibly subdirectories) listed in the **-hdl_source** option of **acs_read_hdl**, more than one include file with the same name. (The implicit assumption is that the **search_path** variable presents an ordered list of directories, but this assumption does not apply to the list of directories in the **-hdl_source** option.)

WHAT NEXT

This warning message alerts you to a possible conflict, which, if not resolved, might prevent a later **analyze** command being able to find the include file, resulting in an error.

To ensure a smooth process here, it is no doubt preferable to identify the correct include file and add its path to the **search_path** variable. Then run the **acs_read_hdl** command again.

SEE ALSO

acs_read_hdl (2), **analyze** (2); **search_path** (3).

ACS-159 (warning) Multiple Master Instances found for design '%s'. Using instance '%s'.

DESCRIPTION

You receive this message because you've specified multiple Master Instances for a multiply instantiated design. You've also specified the '-force' option with the 'set_compile_partitions' command, causing the command to pick the alphabetically smallest instance as Master Instance now.

WHAT NEXT

There is nothing to do, if the instance mentioned in the warning is the instance you want to use as Master Instance for this design. If you want to specify a different

instance as Master Instance you would need to remove the **MasterInstance** attribute on all but the desired instance of this design.

See the **MasterInstance** man page or the *Automated Chip Synthesis, User Guide* for more detailed information.

SEE ALSO

remove_attribute (2), **set_attribute** (2), **set_compile_partitions** (2), **sub_designs_of** (2), **sub_instances_of** (2), **uniquify** (2), **MasterInstance** (3).

ACS-160 (warning) No qualifying designs are found in level '%d'.

DESCRIPTION

You receive this message because you used the **-level** option to specify where to set the compile partitions on the design, but no design at this hierarchical level qualified to become a partition. Only standard hierarchical cells can be treated as partitions. A cell will not be treated as partition if it is not hierarchical, dont touched, or a DesignWare part.

WHAT NEXT

Take either of the following actions:

• Specify a different hierarchy level (a lower number) that contains instances with the **-level** option.

• Use a different option to specify where to set compile partitions. For detailed information, see the **set_compile_partitions** man page.

SEE ALSO

acs_compile_design (2), **set_compile_partitions** (2).

ACS-161 (warning) Executable '%s' does not exist.

DESCRIPTION

You receive this message because the specified executable could not be found. This is often due to a wrong setting of the ACS variable **acs_dc_exec**. If one of these variables is set, ACS will use the specified executable instead of the default ones.

WHAT NEXT

Take either of the following actions:

• Check the ACS variables listed above for typographical errors.

• Use absolute path descriptions instead of relative ones.

SEE ALSO

acs_compile_design (2), **ACS-162.**

ACS-162 (warning) You do not have execute permissions for file '%s'.

DESCRIPTION

You receive this message because you do not have the right permissions to execute the specified file.

WHAT NEXT

Take either of the following actions:

• Try to set the execute-permission (e.g., with 'chmod' on UNIX platforms).

• Ask your system administrator for help.

SEE ALSO

chmod (1), **chown** (1), **ACS-161.**

ACS-163 (information) Starting Design Compiler Design Budgeting.

DESCRIPTION

This message indicates that ACS is using Design Compiler for slack allocation (budgeting).

ACS distinguishes between RTL budgeting and gate-level budgeting. RTL budgeting is performed, e.g., by the **acs_compile_design** command and utilizes Design Compiler's built-in design budgeting facilities.

Gate-level budgeting is performed, e.g., by the **acs_recompile_design** and **acs_refine_design** command. ACS offers three different methods for gate-level slack allocation: Design Compiler budgeting, PrimeTime budgeting, and budgeting via a user budgeting script. Design Compiler budgeting is the recommended way for design budgeting and selected by default. PrimeTime budgeting is deprecated and currently kept for backwards compatibility.

WHAT NEXT

If you wish to use a custom budgeting script for gate-level budgeting, please place a script named **budget.scr** into the directory defined by the **user_budget_script** file type.

SEE ALSO

acs_compile_design (2), **acs_recompile_design** (2), **acs_refine_design** (2), **acs_report_directories** (2), **dc_allocate_budgets** (2).

ACS-164 (information) Starting PrimeTime Design Budgeting.

DESCRIPTION

This message indicates that ACS is using PrimeTime for slack allocation (budgeting).

ACS distinguishes between RTL budgeting and gate-level budgeting. RTL budgeting is performed, e.g., by the **acs_compile_design** command and utilizes Design Compiler's built-in design budgeting facilities.

Gate-level budgeting is performed, e.g., by the **acs_recompile_design** and **acs_refine_design** command. ACS offers three different methods for gate-level slack allocation: Design Compiler budgeting, PrimeTime budgeting, and budgeting via a user budgeting script. Design Compiler budgeting is the recommended way for design budgeting and selected by default. PrimeTime budgeting is deprecated and currently kept for backwards compatibility.

WHAT NEXT

If you wish to use a custom budgeting script for gate-level budgeting, please place a script named **budget.scr** into the directory defined by the **user_budget_script** file type.

SEE ALSO

acs_compile_design (2), **acs_recompile_design** (2), **acs_refine_design** (2),

acs_report_directories (2), **dc_allocate_budgets** (2).

ACS-165 (information) Using custom budgeting script '%s'.

DESCRIPTION

This message indicates that ACS is using a custom busgeting script for slack allocation (budgeting).

ACS distinguishes between RTL budgeting and gate-level budgeting. RTL budgeting is performed, e.g., by the **acs_compile_design** command and utilizes Design Compiler's built-in design budgeting facilities.

Gate-level budgeting is performed, e.g., by the **acs_recompile_design** and **acs_refine_design** command. ACS offers three different methods for gate-level slack allocation: Design Compiler budgeting, PrimeTime budgeting, and budgeting via a user budgeting script. Design Compiler budgeting is the recommended way for design budgeting and selected by default. PrimeTime budgeting is deprecated and currently kept for backwards compatibility.

WHAT NEXT

If you do not wish to use a custom busgeting script, please remove file **budget.scr** from the directory defined by the **user_budget_script** file type.

SEE ALSO

acs_compile_design (2), **acs_recompile_design** (2), **acs_refine_design** (2), **acs_report_directories** (2), **dc_allocate_budgets** (2).

ACS-166 (information) Compile design '%s' in '%s'.

DESCRIPTION

This message is issued by **acs_compile_design** and indicates the source where the specified design is loaded from.

SEE ALSO

acs_compile_design (2), **acs_recompile_design** (2), **acs_refine_design** (2).

ACS-167 (information) Compile design in memory.

DESCRIPTION

This message is issued by **acs_compile_design** and indicates that ACS is going to compile the in-memory design.

SEE ALSO

acs_compile_design (2), **acs_recompile_design** (2), **acs_refine_design** (2).

ACS-168 (information) Re-compile design '%s' in '%s'.

DESCRIPTION

This message is issued by **acs_recompile_design** and indicates the source where the specified design is loaded from.

SEE ALSO

acs_compile_design (2), **acs_recompile_design** (2), **acs_refine_design** (2).

ACS-169 (information) Re-compile design in memory.

DESCRIPTION

This message is issued by **acs_recompile_design** and indicates that ACS is going to re-compile the in-memory design.

SEE ALSO

acs_compile_design (2), **acs_recompile_design** (2), **acs_refine_design** (2).

ACS-170 (information) Refine design '%s' in '%s'.

DESCRIPTION

This message is issued by **acs_refine_design** and indicates the source where the specified design is loaded from.

SEE ALSO

acs_compile_design (2), **acs_recompile_design** (2), **acs_refine_design** (2).

ACS-171 (information) Refine design in memory.

DESCRIPTION

This message is issued by **acs_refine_design** and indicates that ACS is going to refine the in-memory design.

SEE ALSO

acs_compile_design (2), **acs_recompile_design** (2), **acs_refine_design** (2).

ACS-172 (information) Reading partition '%s' from '%s'.

DESCRIPTION

This message is issued whenever a partition is read into memory.

SEE ALSO

acs_compile_design (2), **acs_recompile_design** (2), **acs_refine_design** (2), **read_partition** (2).

ACS-173 (information) Writing partition '%s' to '%s'.

DESCRIPTION

This message is issued whenever a partition is written to disc.

SEE ALSO

acs_compile_design (2), **acs_recompile_design** (2), **acs_refine_design** (2), **write_partition** (2).

ACS-174 (information) Deriving budgets from gate-level design

in ’%s’.

DESCRIPTION

This message is issued by **acs_recompile_design** and indicates the source of the gate-level design that is utilized for slack allocation (budgeting). Note that in **acs_recompile_design**, the design used for budgeting is different than the design to be compiled.

SEE ALSO

acs_recompile_design (2), **dc_allocate_budgets** (2).

ACS-175 (information) Removing designs from memory.

DESCRIPTION

This message indicates that all in-memory designs are discarded. Design deletion takes place at the end of each invocation of **acs_compile_design**, **acs_recompile_design**, and **acs_refine_design** in order to avoid confusion between the pre-compiled and the post-compiled designs. If designs were not deleted, a possible confusion could occur, e.g., if **acs_refine_design** is called right after **acs_compile_design**. The refine command would compile the design in memory which is unchanged and not the result of **acs_compile_design**. The automatic design deletion ensures than **acs_refine_design** does not find any design in memory and therefore reads the design, by default, from the destination directory of **acs_compile_design**.

SEE ALSO

acs_recompile_design (2), **dc_allocate_budgets** (2).

ACS-176 (information) Using user override procedure for command ’%s’.

DESCRIPTION

This message indicates that ACS has found a user override procedure for the specified command. This procedure will be executed instead of the default one. User override procedures can be defined for the commands **acs_compile_design** (procedure **acs_compile_design_user**), **acs_recompile_design** (procedure **acs_recompile_design_user**), and **acs_refine_design** (procedure **acs_refine_design_user**). The easiest way to set up a user override procedure is to customize one of the predefined **.template** files **acs_compile_design.template**, **acs_recompile_design.template**, and **acs_refine_design.template**.

WHAT NEXT

If you do not wish to override the default behaviour, delete the procedures **acs_compile_design_user**, **acs_recompile_design_user**, and **acs_refine_design_user**.

SEE ALSO

acs_compile_design (2), **acs_recompile_design** (2), **acs_refine_design** (2).

ACS-177 (Error) ILM design '%s' is a subdesign of ILM design '%s'.

DESCRIPTION

You receive this message because you have nested ILMs in your design. This is not supported yet. ILMs are detected by testing the **is_interface_model** or the **useILM** attribute. The first indicates that a design is an ILM, the latter tells ACS to create an ILM for the design. In your current design the mentioned designs are ILMs (or are tagged to become ILMs), but the first is instantiated in the logical hierarchy of the other. This is currently not allowed.

WHAT NEXT

Make sure you don't have nested ILMs in your design and you don't set the **useILM** attribute on any design that is instantiated in the logical hierarchy of another ILM (or a design with the "useILM" attribute set). You can either remove the "useILM" attribute from the specified designs, or make sure that the full design representation of the designs is linked in, instead of the ILM representation.

SEE ALSO

acs_refine_design (2), **acs_set_attribute** (2), **set_attribute** (2), **remove_attribute** (2).

ACS-178 (Error) Partition '%s' is inside the ILM design '%s'.

DESCRIPTION

You receive this message because you have marked the specified design as ACS partition, but it is instantiated in the logical hierarchy of the ILM design. Part of the ILM design is or will be cut out which may lead to unexpected constraints for the partition. This is why partitions inside ILMs are not allowed.

WHAT NEXT

Make sure you only created ILMs for designs marked as partitions or designs below partitions. Also, don't set the **useILM** attribute on a design above an ACS partition.

SEE ALSO

acs_refine_design (2), **acs_set_attribute** (2), **remove_attribute** (2), **set_attribute** (2), **set_compile_partitions** (2).

ACS-179 (Error) ILM design '%s' contains an unresolved reference '%s'.

DESCRIPTION

You receive this message because you have marked the specified design with the **useILM** attribute to become an ILM, but it instantiates a design that couldn't be resolved by the linker.

WHAT NEXT

Make sure your **search_path** and **link_library** are set correctly (see the man page of the **link** command).

SEE ALSO

acs_refine_design (2), **acs_set_attribute** (2), **link** (2), **remove_attribute** (2), **set_attribute** (2).

ACS-180 (Error) ILM design '%s' detected in full design.

DESCRIPTION

You receive this message because you are trying to compile a design in memory with **acs_refine_design** and this design contains an ILM. The ACS flow needs the full design representation (in memory or in the source pass) in order to run a useful ILM based flow. The ILM in your design will be considered as full design representation for this partition (i.e. the "is_interface_logic" attribute will be removed). The post_compile db file created by acs_refine_design will contain only the functionality contained in the mentioned ILM design.

SEE ALSO

acs_refine_design (2).

ACS-182 (warning) Multiple instances found for design '%s'. Using instance '%s'.

DESCRIPTION

You receive this message because the design you specified is multiply instantiated and cannot be uniquely identified with a single instance in the design. Therefore, the command you invoked has selected an arbitrary cell instance to proceed.

WHAT NEXT

There is nothing to do, if the instance mentioned in the warning is the one you want to use as instance for this design. If the wrong instance has been chosen, you might want to uniquify the design in order to eliminate multiple instances in your design.

SEE ALSO

sub_designs_of (2), **sub_instances_of** (2), **uniquify** (2).

ACS-183 (error) Option '%s' can be used only inside of another tool.

DESCRIPTION

This error occurs because because you have used an option that is not supported in this tool. For example, physical ACS rtl2pg and gates2pg flow can be applied only inside a different tool than the one you are currently using.

SEE ALSO

acs_compile_design(2)
acs_recompile_design(2)
acs_refine_design(2)

ACS-184 (error) Option '%s' is not comatible with the update option.

DESCRIPTION

You receive this message because you have specified an option that cannot be combined with the 'update' feature. E.g., the physical ACS flows cannot be used inside an update flow.

SEE ALSO

acs_compile_design (2), **acs_recompile_design** (2), **acs_refine_design** (2).

ACS-185 (error) Option '%s' is not comatible with physical ACS flows.

DESCRIPTION

You receive this message because you have specified an option that cannot be combined with the physical ACS flows.

SEE ALSO

acs_compile_design (2), **acs_recompile_design** (2), **acs_refine_design** (2).

ACS-186 (warning) Option '-ignore_analyze_errors' of command 'acs_read_hdl' is no longer supported.

DESCRIPTION

You receive this message because you have specified an option that is no longer supported.

Even with this option set, the analyze command used by acs_read_hdl internally, halts upon encountering an error and forgets all data obtained during that call to analyze. As acs_read_hdl always tries to implicitly call analyze with as many files as possible, the result of this option is not exactly what you would expect.

Preceeding internal calls to analyze and following calls to analyze are still executed. Therefore you can still use this option for a trial analysis.

WHAT NEXT

There is nothing to do.

SEE ALSO

acs_read_hdl (2).

ACS-187 (warning) false dont_touch attribute is detected on

object '%s'. It may be lost or ACS may not be able to complete successfully.

DESCRIPTION

This message indicates that there is dont_touch being set to false in your design. Right now, ACS cannot guarantee that ACS could complete successfully if your design has false dont_touch attribute and the object who has false dont_touch is a multiply instantiated design or is an instance of a multiply instantiated design. Or, the false dont_touch attribute is not be hornored if the object who has false dont_touch is a singly instantiated non-partition design or its instance, and this false dont_touch attribute may cause long runtime on the upper level partitions' compile (object who has false dont_touch attribute may be re-compiled during upper level partitions' compile). Or, the false dont_touch attribute may be lost after compile by using ACS if the object who has false dont_touch is a singly instantiated partition design or its instance.

WHAT NEXT

You need to optimize/compile the design (who or whose instance has false dont_touch) independently, and remove the false dont_touch attribute on your design before ACS to make sure that ACS could run through successfully. It is not recommended to apply false dont_touch attribute on your design when you use ACS.

SEE ALSO

acs_compile_design (2), **acs_recompile_design** (2), **acs_refine_design** (2).

ACS-188 (Error) '%s' is not an ACS supported attribute.

DESCRIPTION

This message indicates that you specified an attribute which is not currently supported by ACS.

WHAT NEXT

To see the whole list of ACS supported attributes, their valid values and their default value, please check the man page for acs_set_attribute.

SEE ALSO

acs_report_attribute (2), **set_compile_partitions** (2), **report_partitions** (2).

ACS-190 (error) Top module does not link.

DESCRIPTION

This error message occurs when the the **link** command issued within the Automated Chip Synthesis auto update flow fails. The failure occurs when the GTECH library or the target Technology library is omitted or incorrectly specified.

WHAT NEXT

Ensure that the **search_path** is set correctly and that all of the source directories are specified in the **-hdl_source** option of the **acs_read_hdl** command.

SEE ALSO

acs_read_hdl(2)
current_design(2)
link(2)

ACS-191 (error) Corrupt elab_times table.

DESCRIPTION

This error message occurs when the design’s elab_times table is corrupted.

The elab_times table is an ASCII table created during the Automated Chip Synthesis auto update flow to keep track of the update times of the designs in the design hierarchy. The default location for the table is elab/db.

WHAT NEXT

To continue, delete the design’s elab_time table. Then regenerate the table using the **acs_read_hdl** command with the **-auto_update** or **-update** option.

SEE ALSO

acs_read_hdl(2)

ACS-192 (warning) Cell ’%s’ does not have reference design.

DESCRIPTION

This message is printed because ACS could not locate referencing design for the

cell.

WHAT NEXT

Take either of the following actions:

- Make sure design is properly linked.

- Make sure all design units are read properly and there are no syntax errors.

SEE ALSO

acs_read_hdl (2), **read_file** (2), **link** (2)

ACS-193 (error) Valid target library for cell '%s' could not be found.

DESCRIPTION

ACS issues this error when valid target library for cell could not be found. This can happen when libraries which are characterized for specified operating condition are not found. ACS also issues this message when target library subset and library set characterized for operating conditions have no common elements.

WHAT NEXT

- Make sure operating conditions and target library subset is properly specified.

SEE ALSO

set_target_library_subset (2), **set_operating_conditions** (2),

ACS-194 (error) Attribute '%s' is no longer supported by ACS.

DESCRIPTION

ACS issues this message when attempting to set an obsolete ACS attribute. ACS attributes become obsolete when their corresponding DC commands become obsolete.

The list of obsolete attributes and the corresponding DC commands is given below.

Attribute Name	Design Compiler Command
HasArithmetic	transform_csa
PartitionDP	partition_dp

WHAT NEXT

Remove the obsolete attribute from the compilation scripts and re-run ACS.

SEE ALSO

acs_set_attribute (2), **transform_csa** (2), **partition_dp** (2)

ACS-195 (warning) Attribute '%s' set on partition '%s' is obsolete and will be ignored.

DESCRIPTION

ACS prints this message when it finds an obsolete attribute on a partition. Please refer to the ACS Users Guide or the acs_set_attribute man page for a list of supported attributes.

WHAT NEXT

Remove the obsolete attribute from the partition and run ACS again.

SEE ALSO

acs_set_attribute (2)

APL-001 (error) Internal error.

DESCRIPTION

This error message occurs when the tool encounters an internal error and cannot continue.

WHAT NEXT

Submit a testcase that reproduces the problem to the Synopsys Customer Support Center by using Enter A Call at http://solvnet.synopsys.com/EnterACall.

APL-002 (error) Out of memory.

DESCRIPTION

This error message occurs when the tool encounters a memory allocation error and cannot continue.

WHAT NEXT

Either run the command on a machine with more internal memory, or submit a testcase that reproduces the problem to the Synopsys Customer Support Center by using Enter A Call at http://solvnet.synopsys.com/EnterACall.

APL-003 (error) Cannot read the attached file.

DESCRIPTION

This error message occurs when the tool cannot read the external file attached to the Milkyway design and/or library. The file is unreadable if any of the following are true:

- The file does not exist.
- There is an error in the file syntax.
- You do not have read permission for the file.

WHAT NEXT

Verify that the file exists, that there are no errors in the file syntax, and that you have read permission for the design and/or library. After making your changes, rerun the command.

APL-004 (error) Cannot write the attached file.

DESCRIPTION

This error message occurs when the tool cannot write the external file attached to the Milkyway design and/or library. The cause may be that you do not have permission to write the file.

WHAT NEXT

Verify that you have write permission for the design and/or the library. After making your changes, run the command again.

APL-005 (warning) Failed to load intercell spacing constraints.

DESCRIPTION

This warning message occurs when either spacing labels are defined without defining rules, or when rules are defined without defining labels.

You must define both labels and rules, to successfully load intercell spacing constraints. If neither spacing labels nor rules are defined, no constraints are used.

WHAT NEXT

This is only a warning message. No action is required.

However, if you want the legalizer to use intercell spacing constraints, define both spacing labels and spacing label rules, and run the command again.

SEE ALSO

set_lib_cell_spacing_label(2)
set_spacing_label_rule(2)

APL-006 (warning) Lib cell %s could not be found in the design.

DESCRIPTION

You received this warning message because the lib cells passed in a collection as input to set_lib_cell_spacing_label command could not be found in the Milkyway database. The most likely reason for this is that the lib cell is not used in the current design. In that case this warning message can be safely ignored.

WHAT NEXT

Verify that the named lib cell exists in the Milkyway library.

SEE ALSO

set_lib_cell_spacing_label (2) **report_reference** (2)

APL-007 (warning) Failed to find label %s. Rule skipped.

DESCRIPTION

This warning message occurs when an intercell spacing constraint set with the **set_spacing_label_rule** command references a label that has not been set with the **set_lib_cell_spacing_label** command.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, check that the named label has been set with the **set_lib_cell_spacing_label** command and then run the initial command again.

SEE ALSO

set_lib_cell_spacing_label(2)
set_spacing_label_rule(2)

APL-008 (warning) Placement of cells %s and %s violates

intercell spacing constraints.

DESCRIPTION

This warning message occurs when intercell spacing constraints set with the **set_spacing_label_rule** and **set_lib_cell_spacing_label** commands are violated.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, run the **legalize_placement** command to fix placement violations, and then rerun the initial command.

SEE ALSO

legalize_placement(2)
set_lib_cell_spacing_label(2)
set_spacing_label_rule(2)

APL-009 (error) Must provide both tie-high and tie-low lib cell names.

DESCRIPTION

You received this error message because command connect_tie_cells requires that both tie-high and tie-low lib cell names be specified if -tie_high_low_lib_cell option is not used.

WHAT NEXT

See command man page. Provide correct input to command.

SEE ALSO

connect_tie_cells (2)

APL-010 (error) Must provide both tie-high and tie-low port

names.

DESCRIPTION

You received this error message because command connect_tie_cells requires that both tie-high and tie-low port names be specified if -tie_high_low_lib_cell option is used.

WHAT NEXT

See command man page. Provide correct input to command.

SEE ALSO

connect_tie_cells (2)

APL-011 (error) Lib cell %s not found.

DESCRIPTION

You received this error message because the tie-cell lib cell you provided cannot be found in the linked reference libraries.

WHAT NEXT

Verify lib cell name. Verify that the desired reference library is being linked to the design.

APL-012 (error) Lib cell %s has more than one output.

DESCRIPTION

You received this error message because the tie-cell lib cell you provided has multiple output pins. A tie-high or tie-low cell must have a single output pin.

WHAT NEXT

Specify different tie-high and/or tie-low lib cell.

APL-013 (error) Port %s is not an output port.

DESCRIPTION

You received this error message because the tie-high or tie-low port name you specified is not an output port on the tie-highlow lib cell.

WHAT NEXT

Specify different tie-high and/or tie-low port name.

APL-014 (error) Output ports for tie-highlow lib cell %s not found.

DESCRIPTION

You received this error message because the tie-high and tie-low ports for the tie-highlow lib cell you specified can not be found.

WHAT NEXT

Specify different tie-high and/or tie-low port name(s).

APL-015 (warning) New cell %s is not connected to Power/Ground nets.

DESCRIPTION

You received this warning message because the newly created could not be connected to Power/Ground nets.

WHAT NEXT

Run derive_pg_connection.

SEE ALSO

derive_pg_connection (2)

APL-016 (warning) Object %s is not a tie-high/tie-low port. Skipping.

DESCRIPTION

You received this warning message because the object is not appropriate for connect_tie_cells.

WHAT NEXT

Verify this object is a tie-off port that needs to be tied-off by connect_tie_cells. This message can be safely ignored otherwise.

APL-017 (warning) Object %s is not a cell with tie-high/tie-low ports. Skipping.

DESCRIPTION

You received this warning message because the object is not appropriate for connect_tie_cells.

WHAT NEXT

Verify this object is a cell with tie-off port that need to be tied-off by connect_tie_cells. This message can be safely ignored otherwise.

APL-018 (warning) Object %s is not a lib cell with tie-high/tie-low ports. Skipping.

DESCRIPTION

You received this warning message because the object is not appropriate for connect_tie_cells.

WHAT NEXT

Verify this object is a lib cell of cells in the design with tie-off ports that need to be tied-off by connect_tie_cells. This message can be safely ignored otherwise.

APL-019 (warning) Port %s on cell instance %s is outside core. Skipping.

DESCRIPTION

You received this warning message because connect_tie_cells detected a cell with tie-off ports that lies outside the core placement area. Connect_tie_cells only works on cells inside the core. Others are ignored.

WHAT NEXT

Verify the core placement area of the design is correct.

APL-020 (warning) Port %s on cell instance %s is disconnected . Skipping.

DESCRIPTION

You received this warning message because connect_tie_cells detected a cell with tie-off port that is not connected to any net. These ports are ignored. Connect_tie_cells is intended to run after connect_pg_nets.

WHAT NEXT

Verify the connectivity of the cell. Run connect_pg_nets.

SEE ALSO

connect_pg_nets (2)

APL-021 (warning) Port %s on cell instance %s is connected to wrong polarity. Skipping.

DESCRIPTION

You received this warning message because connect_tie_cells detected a cell with tie-off port that is connected to Power but should be tied-low, or is connected to Ground but should be tied-high. These ports are ignored.

WHAT NEXT

Verify the connectivity of the cell.

APL-022 (warning) Port %s on cell instance %s is driven by wrong cell master. Skipping.

DESCRIPTION

You received this warning message because connect_tie_cells detected a cell with tie-off port that is driven by an incorrect lib cell or bound port. These ports are ignored.

WHAT NEXT

Verify the connectivity of the cell.

APL-023 (warning) %d violations of maximum wirelength (%d microns) found.

DESCRIPTION

You received this warning message because connect_tie_cells was unable to complete without violating the maximum wirelength constraint. This is most likely caused by high cell utilization. It may also be caused by a blockage preventing insertion of a tie cell within the maximum distance.

WHAT NEXT

Verify layout.

APL-024 (error) Reference cell %s has no cell boundary.

DESCRIPTION

You received this message because no boundary has been defined for the reference cell in the database.

WHAT NEXT

Verify reference library preparation.

APL-025 (error) Overlapping rows detected in the design.

DESCRIPTION

You received this message because there are overlapping rows in this design. This is not supported.

WHAT NEXT

Verify chip layout preparation.

APL-026 (warning) Reference cell %s bounding box not multiple of tile.

DESCRIPTION

You received this warning message because the reference cell size is not a multiple of the tile. This may be caused by an error in reference cell setup, possibly because this is a multi-height cell.

WHAT NEXT

Verify reference cell preparation.

APL-027 (warning) Metal %d tracks may not cover core area at the %s side.

DESCRIPTION

You received this warning message because the metal tracks on given layer do not extend to the edge of the chip core area.

WHAT NEXT

Verify chip metal layout.

APL-028 (warning) Pin %s of reference cell %s has no physical location.

DESCRIPTION

You received this warning message because information about pin layout within the reference cell was not found in the database.

WHAT NEXT

Verify reference cell and pin liyout.

APL-029 (warning) Number of metal layers defined in design %d is greater than the number defined in the tech file %d.

DESCRIPTION

You received this warning message because the number of metal layers in the design does not match the number in the tech file. The definition from the tech file will be used.

WHAT NEXT

Verify design and tech file preparation.

APL-030 (warning) Can not determing Power/Ground nets for new cells.

DESCRIPTION

You received this warning message because the tool could not determine which Power/Ground nets to use to automatically connect the newly inserted filler cells. This may happen if there are multiple Power/Ground nets in the design.

WHAT NEXT

Run connect_pg_nets.

SEE ALSO

connect_pg_nets (2)

APL-031 (warning) Failed to add newly created end cap instance to plan group.

DESCRIPTION

You received this warning message because the tool created a new end cap instance cell that is added to logic hierarchy but failed to update the corresponding plan group. When committing the plan group, the end caps will not be automatically pushed down.

WHAT NEXT

You may need to consult your technical support contact to further investigate why automatic plan group updating failed. Alternatively you can use push_down_fp_objects to push the end caps into the soft macro.

SEE ALSO

commit_fp_plan_groups (2) **,** push_down_fp_objects **(2)** , **push_up_fp_objects** (2)

APL-032 (error) IC Compiler cannot find the top-level hierarchical cell instance for MW CEL.

DESCRIPTION

You received this error message because IC Compiler cannot find the top-level hierarchical cell instance while trying to insert a filler cell.

WHAT NEXT

This is an internal error and should be reported to Synopsys.

APL-033 (warning) Ignoring spacing constraints for hard macro

%s.

DESCRIPTION

You received this warning message because the lib cell passed as input to set_lib_cell_spacing_label command is a hard macro. Inter-cell spacing constraints are only supported for standard cells.

WHAT NEXT

Remove the hard macro lib cell from input to set_lib_cell_spacing_label command.

SEE ALSO

set_lib_cell_spacing_label (2) **report_reference** (2)

APL-034 (warning) Incompatible multiple core areas %s and %s found in the design.

DESCRIPTION

You received this warning message because the tool detected the presence of multiple incompatible core areas in the design. A typical design only has a single core area. Multiple core areas are incomaptible if the rectangles formed by their coordinates do not overlap completely.

WHAT NEXT

Verify the coordinates of the core areas.

SEE ALSO

get_core_area (2)

APL-035 (warning) No cells with ports for tie-off found.

DESCRIPTION

You received this warning message because there are no cells with ports that need to be tied-off to tie_high or tie_low in the design.

WHAT NEXT

Verify this design has cell(s) with tie-off port(s) that need to be tied-off by connect_tie_cells. This message can be safely ignored otherwise.

APL-036 (warning) Skip the %dth tap cell insertion at (%f, %f).

DESCRIPTION

You received this warning message because add_tap_cell_array skipped off-distance tap insertion. It may cause DRC errors in the future.

WHAT NEXT

Turn off the following option of add_tap_cell_array to insert extra off-distance tap cells for DRC-free purpose.

-at_distance_only false

APL-037 (error) Input polygon out of core area.

DESCRIPTION

You received this error message because coordinates of the polygon passed to spread_spare_cells lies entirely outside the core area.

WHAT NEXT

Correct the input and try again.

APL-038 (warning) Input rectangle out of core area.

DESCRIPTION

You received this warning message because coordinates of one of the rectangles passed to spread_spare_cells lies entirely outside the core area.

WHAT NEXT

Correct the input and try again.

APL-039 (error) offset should come with a value less than distance/2

DESCRIPTION

You received this error message because add_tap_cell_array only allows offset to be set as a value less than distance/2.

WHAT NEXT

Correct the input and try again.

APL-040 (warning) UPF: ICC can not find the power domain of top level design.

DESCRIPTION

You received this warning message because there is no power domain information for top level design.

WHAT NEXT

Apply create_power_domain to set database for UPF support.

APL-041 (warning) UPF: ICC can not find the specified voltage area(%s).

DESCRIPTION

You received this warning message because the voltage area can not be found in this design.

WHAT NEXT

Apply create_voltage_area to set database for UPF support.

APL-042 (warning) Please specify the power domain of the

voltage area(%s).

DESCRIPTION

You received this warning message because there is no power domain information set for the voltage area.

WHAT NEXT

Apply create_voltage_area or update_voltage_area to set database for UPF support.

APL-043 (warning) UPF: ICC can not find the specified power domain for the voltage area(%s).

DESCRIPTION

You received this warning message because the specified power domain of the voltage area doesn’t exist in database.

WHAT NEXT

Apply create_power_domain to set database for UPF support.

APL-044 (warning) UPF: ICC can not find power net of power domain(%s).

DESCRIPTION

You received this warning message because the power net doesn’t exist in database for power domain.

WHAT NEXT

Apply create_supply_net or set_domain_supply_net to set database for UPF support.

APL-045 (warning) UPF: User’s power net(%s) doesn’t match

the information(%s) from power domain(%s).

DESCRIPTION

You received this warning message because the inconsistency happens between the user input and the data from power domain.

WHAT NEXT

Either update power domain or re-enter power net of user inputs to resolve this conflict.

APL-046 (warning) UPF: ICC can not find ground net of power domain(%s).

DESCRIPTION

You received this warning message because the ground net doesn’t exist in database for power domain.

WHAT NEXT

Apply create_supply_net or set_domain_supply_net to set database for UPF support.

APL-047 (warning) UPF: User’s ground net(%s) doesn’t match the information(%s) from power domain(%s).

DESCRIPTION

You received this warning message because the inconsistency happens between the user input and the data from power domain.

WHAT NEXT

Either update power domain or re-enter ground net of user inputs to resolve this conflict.

APL-048 (warning) UPF: No input power net. Apply (%s) for

voltage area (%s) by default.

DESCRIPTION

You received this warning message because there is no input power net for the specific voltage area. ICC UPF will retrieve power net from the associated power domain automatically.

WHAT NEXT

If the assigned power net is not correct, please check whether the voltage area is linked to the proper power domain or not.

APL-049 (warning) UPF: No input ground net. Apply (%s) for voltage area (%s) by default.

DESCRIPTION

You received this warning message because there is no input ground net for the specific voltage area. ICC UPF will retrieve ground net from the associated power domain automatically.

WHAT NEXT

If the assigned ground net is not correct, please check whether the voltage area is linked to the proper power domain or not.

APL-050 (warning) "-ignore_existing_cells" is an obsolete option. Please use "-skip_fixed_cells" instead.

DESCRIPTION

You received this warning message because option "-ignore_existing_cells" is obsolete.

WHAT NEXT

Please use "-skip_fixed_cells" instead.

APL-051 (warning) Skip the %dth tap cell insertion at (%f, %f).

DESCRIPTION

You received this warning message because add_tap_cell_array skipped off-distance tap insertion. It may cause DRC errors in the future.

WHAT NEXT

Turn off the following option of add_tap_cell_array to insert extra off-distance tap cells for DRC-free purpose.

-at_distance_only false

APL-052 (warning) Legalizer did not find a solution. Removing group %s constraint.

DESCRIPTION

You received this warning message because legalize_fp_placement failed to find a legal solution for the named group. This may be caused by very high group utilization, or other factors. The legalizer proceeds from this point with the group contraint removed.

WHAT NEXT

Review the floorplan to determine whether group constraint is valid. You may choose to run legalize_placement instead. Alternately you can try setting the following set_fp_placement_strategy -legalizer_effort low

APL-053 (Warning) %s filler abuts with %s and they are located at (%f, %f) and (%f, %f).

DESCRIPTION

You received this warning message because there are two consecutive standard-cell fillers in this design. ICC reports their corresponding coordinates for your reference.

WHAT NEXT

APL-054 (Information) %s standard-cell filler is located at (%f, %f).

DESCRIPTION

You received this message because a standard-cell filler exists in this design. ICC reports its corresponding coordinates for your reference.

WHAT NEXT

APL-055 (warning) Using classical router on a Zroute-routed design.

DESCRIPTION

You received this warning message because the command insert_stdcell_filler -cell_with_metal is using the classical router engine on a design that has been routed with Zroute. This may result in inconsistent behavior.

WHAT NEXT

To assure that insert_stdcell_filler uses the Zroute engine do the following
set_route_mode_options -zroute true

SEE ALSO

insert_stdcell_filler(2)
set_route_mode_options(2)

APL-056 (Information) %s
Number of filler cells with metal: %d
Number of irremovable filler cells with metal: %d
Total leakage power of filler cells with metal: %f mW

Total area of filler cells with metal: %f um^2

DESCRIPTION

You received this message because the constrained decoupling capacitor feature of insert_stdcell_filler was turned on and it is the status report of filler cells with metal for this design.

WHAT NEXT

APL-057 (error) Region #%d has more cell area (%.0lf %s^2) than placeable area (%.0lf %s^2).

DESCRIPTION

You received this error message because cells belonging to a region in the design (e.g. plangroup or voltage area) demand more placeable area than is available.

WHAT NEXT

Submit a testcase that reproduces the problem to the Synopsys Customer Support Center by using Enter A Call at http://solvnet.synopsys.com/EnterACall.

APL-058 (warning) the %s constraint(s) can’t be fulfilled because there is no more removable filler cells with metal in the insertion area(s).

DESCRIPTION

You received this message because the constrained decoupling capacitor feature of insert_stdcell_filler was turned on and it is the final status report for this design. Please check if the metal fillers in the insertion area(s) are fixed, L/R fillers, or all deleted. If so, it is the best the tool can do for this design.

WHAT NEXT

APL-059 (error) Corrupt database. Number of objects of type

DESCRIPTION

This error message occurs when a mismatch of number of objects in DB and that seen by the tool is encountered.

WHAT NEXT

Submit a testcase that reproduces the problem to the Synopsys Customer Support Center by using Enter A Call at http://solvnet.synopsys.com/EnterACall.

APL-060 (warning) The specified lib_cell, %s is not a filler cell. report_filler_placement will not report the location of its cell instance, %s.

DESCRIPTION

You received this message because this cell was not marked as a subtype of std filler.

WHAT NEXT

Please check the data preparation of cell masters in libraries to make sure they are all with correct subtypes before applying report_filler_placement.

APL-061 (Information) decoupling capacitor insertion has fullfilled the power and area constraints.

DESCRIPTION

You received this message because the constrained decoupling capacitor feature of insert_stdcell_filler was turned on and it is the final report for this design.

WHAT NEXT

APL-062 (warning) cannot legally place %s corner cell at (%d, %d)

DESCRIPTION

You received this warning message because corner cell cannot be legally placed at this location.

WHAT NEXT

Check design

APL-063 (warning) short vertical segment skipped : (%d,%d)-(%d,%d).

DESCRIPTION

You received this warning message because the vertical segment is too short to place corner cell.

WHAT NEXT

Check design

APL-064 (warning) no room for %s horizontal cell at (%d,%d)

DESCRIPTION

You received this warning message because horizontal cell cannot be legally placed at this location.

WHAT NEXT

Check design

APL-065 (warning) no feasible vertical end cap for location

(%f,%f)

DESCRIPTION

You received this warning message because no vertical cell can be legally placed at this location.

WHAT NEXT

Check design

APL-066 (warning) row end (%f,%f) doesn’t allow mirrored pattern.

DESCRIPTION

You received this warning message because mirrored cell pattern horizontal cell cannot be legally placed at this location.

WHAT NEXT

Check design

APL-067 (warning) The capability of decoupling capacitance was not activated.

DESCRIPTION

You received this message because both -leakage_power and -metal_filler_coverage_area are negtive values. The behavior of ICC is as same as none of these two options is applied. The default of them is -1.

WHAT NEXT

To turn on the feature of decoupling capacitance, ICC needs to have at least one of these two options specified as a positive value.

APL-068 (error) Error in mapping coordinate to placement site.

DESCRIPTION

You received this warning message because the specific cell is out of the bound of its row.

WHAT NEXT

Verify to see if the location of that cell is legal.

SEE ALSO

insert_stdcell_filler -check **(2)**

APL-069 (error) incorrect insert_stdcell_filler command option usage

DESCRIPTION

You received this warning message because of incorrect usage of insert_stdcell_filler option.

WHAT NEXT

see command man page for details

SEE ALSO

APL-070 (warning) no 1x violation

DESCRIPTION

You received this warning message because there is a 1x gap or tool cannot place L/R filler because it would create 1x gap.

WHAT NEXT

Check design or provide right size L/R filler

APLUI-001 (error) No library is open.

DESCRIPTION

This error message occurs when attempting to run a command that requires an open library.

WHAT NEXT

Open the library with the **open_mw_lib** command and run the initial command again.

SEE ALSO

open_mw_lib(2)

APLUI-002 (error) Incorrect command syntax.

DESCRIPTION

This error message occurs when the incorrect syntax is used for the command.

WHAT NEXT

Check the man page for the command you are attempting to run, and rerun the command with the proper syntax.

APLUI-003 (error) No object found in the collection.

DESCRIPTION

This error message occurs because the tool requires at least one object to be specified. The object(s) with the given name may not exist in the Milkyway library.

WHAT NEXT

Check that the specified object is spelled correctly, and that it exists in the library or design. Check the command man page to verify the correct syntax.

After making any changes, run the command again.

APLUI-004 (error) The %s command failed.

DESCRIPTION

This error message occurs when the tool cannot successfully complete the command.

WHAT NEXT

Check the log file to to determine the cause of the failure. If necessary, check the man page for the command. After making any needed corrections, run the command again.

APLUI-005 (error) Lower value of illegal spacing range %d is beyond the maximum %d.

DESCRIPTION

You received this error message because spacing constraints apply only to spacing smaller than the maximum.

WHAT NEXT

Modify your constraint.

APLUI-006 (warning) Upper value of illegal spacing range %d is beyond the maximum %d. Reset to maximum

DESCRIPTION

You received this error message because spacing constraints apply only to spacing smaller than the maximum.

WHAT NEXT

Modify your constraint.

APLUI-007 (error) Illegal range {%d %d}.

DESCRIPTION

You received this error message because the spacing constraints are illegal. This may be because one or both of the values is negative.

WHAT NEXT

Modify your constraint.

APLUI-008 (warning) Range in bad format {%d %d}.

DESCRIPTION

You received this error message because the spacing constraints are incorrectly formatted. This may be because the constraints are given as {max min}. The tool interprets this as {min max}.

WHAT NEXT

Modify your constraint.

APLUI-009 (warning) Option %s is obsolete; use %s instead.

DESCRIPTION

You received this warning message because you used an obsolete option for the command.

WHAT NEXT

See command man page. Use correct option.

APLUI-010 (Error) can not find power switch %s from current

scope

DESCRIPTION

This error message occurs because command fail to get UPF power switch from current scope.

WHAT NEXT

See command man page. Use correct UPF power switch name.

APLUI-011 (Error) can not find power domain %s from current scope

DESCRIPTION

This error message occurs because command fail to get UPF power domain from current scope.

WHAT NEXT

See command man page. Use correct UPF power domain name.

APLUI-012 (warning) Cannot apply built-in label %s to library cells.

DESCRIPTION

You received this warning message because you tried to apply a built-in label to a library cell.

WHAT NEXT

Please choose a different label name.

APLUI-013 (warning) Could not find power/ground net name

%s, use default.

DESCRIPTION

You received this warning message because the given power or ground net name was not found in the database. Default name is used instead.

WHAT NEXT

Verify net name.

APLUI-014 (error) create_floorplan multi-ring I/O feature could not support %s floorplan.

DESCRIPTION

You received this error message because the your option is not supported by multi-ring I/O placement of create_floorplan.

WHAT NEXT

Try single-ring I/O placement.

APLUI-015 (error) I/O ring %dth is empty.

DESCRIPTION

You received this error message because create_floorplan multi-ring I/O feature doesn’t allow a ring without any pad.

WHAT NEXT

Reset ring_depth by set_chiplevel_pad_physical_constraints or modify constraints of pads by set_pad_physical_constraints

APLUI-016 (warning) Metal filler %s is not available in target

libraries.

DESCRIPTION

You received this error message because the specific metal filler is not ready to use in target libraries.

WHAT NEXT

Please check .lib files to verify if this filler is marked as "do not use".

APLUI-017 (error) connect_tie_cells cannot be used in Freeze Silicon mode.

DESCRIPTION

You received this error message because command connect_tie_cells is not compatible with freeze_silicon mode.

WHAT NEXT

You need to manually insert and connect tie cells.

APR

APR-001 (error) Database error.

DESCRIPTION

This error message occurs when the tool encounters a database error.

WHAT NEXT

Submit a testcase that reproduces the problem to the Synopsys Customer Support Center by using Enter A Call at http://solvnet.synopsys.com/EnterACall.

APR-002 (error) Net %d is not Power/Ground net.

DESCRIPTION

This error message occurs when connect_net or disconnect_net expects a Power/Ground net, but the input net is not Power/Ground.

WHAT NEXT

Verify the intended functionality. Submit a testcase that reproduces the problem to the Synopsys Customer Support Center by using Enter A Call at http://solvnet.synopsys.com/EnterACall.

SEE ALSO

connect_net(2)
disconnect_net(2)

APR-003 (error) Pin %d is already connected to a net.

DESCRIPTION

This error message occurs when connect_net encounters a pin that is already connected. Connect_net only operates on fully unconnected pins. It is skipped.

WHAT NEXT

Verify the intended functionality. Submit a testcase that reproduces the problem to

the Synopsys Customer Support Center by using Enter A Call at http://
solvnet.synopsys.com/EnterACall.

SEE ALSO

connect_net(2)
disconnect_net(2)

APR-004 (error) Pin %d is in the wrong hierarchy.

DESCRIPTION

This error message occurs when connect_net encounters a pin that is in a different hierarchy than the net to which the user wants to connect it to. It is skipped.

WHAT NEXT

Verify the intended functionality. Submit a testcase that reproduces the problem to the Synopsys Customer Support Center by using Enter A Call at http://
solvnet.synopsys.com/EnterACall.

SEE ALSO

connect_net(2)
disconnect_net(2)

APR-005 (warning) connect_pg_nets is no longer supported. Please use derive_pg_connection instead.

DESCRIPTION

connect_pg_nets does not support hierarchical PG database. So starting in 2008.09 release, connect_pg_nets are replaced by derive_pg_connection.

WHAT NEXT

Please use command derive_pg_connection instead.

SEE ALSO

derive_pg_connection(2)

ATTR-1 (warning) Attribute '%s' has not been defined for %s

DESCRIPTION

The attribute you are referencing is not defined for the class of object(s) you are using. It is possible that the attribute is not defined at all.

Application attributes are all defined at runtime by the application. You can create user-defined attributes at any time.

WHAT NEXT

Verify that the attribute name is spelled correctly. If this is a documented application attribute, contact support. If this is a user-defined attribute, ensure that you have defined the attribute for all appropriate classes.

ATTR-2 (warning) Attribute '%s' is not user-defined for %ss; can't %s it

DESCRIPTION

The attribute you are referencing is an application attribute. These cannot be set or removed by the user using set_user_attribute or remove_user_attribute, respectively. There might be other commands which allows you to set or remove the attribute.

WHAT NEXT

Consult the documentation to determine if it is possible to set or remove this attribute.

ATTR-3 (warning) Attribute '%s' does not exist on %s '%s'

DESCRIPTION

The attribute you are trying to get is not found on the object. This is definitely a sparse attribute, and most likely user-defined. There is a way to suppress this message if you desire. For example, if this is in a loop or in a procedure (-quiet?)

WHAT NEXT

ATTR-4 (warning) Value '%s' is not valid for '%s' on %ss

DESCRIPTION

The value you are trying to set on the attribute cannot be converted to the data type defined for the attribute. For example, if the attribute is defined as "float", setting the attribute to "true" is not valid.

WHAT NEXT

Enter an appropriate value for the attribute.

ATTR-5 (warning) Value '%s' for '%s' is not in range (%s)

DESCRIPTION

The numeric value you are trying to set on the attribute is not in the range specified for the attribute. Ranges are either within a minimum and maximum value, greater than or equal to a minimum value, or less or equal to a maximum value. The message text indicates the violated constraint.

WHAT NEXT

Enter an appropriate value for the attribute.

ATTR-6 (warning) Value '%s' for '%s' is not valid. Specify one of: %s

DESCRIPTION

The string value you are trying to set on the attribute is not one of the valid strings defined for the attribute. The message text indicates the allowable values.

WHAT NEXT

Enter an appropriate value for the attribute.

ATTR-7 (information) Inferred definition of attribute '%s' for class '%s'
because it is imported for class '%s'

DESCRIPTION

You used the **define_user_attribute** command to define a design or port attribute, and asked for it to be imported from DB files. Since design attributes are inherited onto cells (an instance of a design) and port attributes are inherited onto pins (an instance of a port), the attribute you defined for a design/port must also be defined for a cell/pin, respectively. PrimeTime defines the attribute for you if you have not already done so, and issues this message.

WHAT NEXT

If you want to remove this message, add the appropriate class to the list of classes in your **define_user_attribute** command, or add a dedicated **define_user_attribute** command earlier in the script to define the attribute for the cell or pin class.

SEE ALSO

define_user_attribute (2).

ATTRDEF

ATTRDEF-001.n

ATTRDEF-001 (error) This visual (%s) does not exist.

DESCRIPTION

This visual does not exist. Please check the visual name.

ATTRDEF-002.n

ATTRDEF-002 (error) Internal error. Not valid type set %s.

DESCRIPTION

Type set is not valid.

ATTRDEF-003.n

ATTRDEF-003 (error) Not valid class name.

DESCRIPTION

Design object class is not valid. Please, specify one of the following:

ATTRDEF-004.n

ATTRDEF-004 (error) (error) Incompatible type and subtype values.

DESCRIPTION

Subtype can be specified only if type is string.

ATTRDEF-005.n

ATTRDEF-005 (error) (error) Type must be specified.

DESCRIPTION

Type must be specified if subtype is presented.

ATTRDEF-006.n

ATTRDEF-006 (error) Incompatible type and format values.

DESCRIPTION

Format can be specified only if type is int or double.

ATTRDEF-007.n

ATTRDEF-007 (error) Type must be specified.

DESCRIPTION

Type must be specified if format is presented.

ATTRDEF-008.n

ATTRDEF-008 (error) Attribute %s not found.

DESCRIPTION

Specified attribute not found.

ATTRDEF-009.n

ATTRDEF-009 (error) Internal error. Can’t create attribute %s.

DESCRIPTION

Specified attribute can not be created.

ATTRDEF-010.n

ATTRDEF-010 (error) Attribute %s already exists.

DESCRIPTION

Specified attribute already exists and can not be created.

ATTRDEF-011.n

ATTRDEF-011 (error) Attribute %s is not user-defined.

DESCRIPTION

Specified attribute is not user-defined and not allowed for this command.

ATTRDEF-012.n

ATTRDEF-012 (error) Internal error. Removing of attribute %s failed.

DESCRIPTION

Removing of attribute failed.

ATTRDEF-013.n

ATTRDEF-013 (error) Internal error. Error getting list of attdefs for %s.

DESCRIPTION

Getting list of attdefs failed.

ATTRDEF-014.n

ATTRDEF-014 (error) Internal error. Error getting list of object

types.

DESCRIPTION

Getting list of object types failed.

ATTRDEF-015.n

ATTRDEF-015 (error) Error. Option -name valid with -class only

DESCRIPTION

Option -name valid with -class only.

ATTRDEF-016.n

ATTRDEF-016 (error) Attribute group %s already exist.

DESCRIPTION

Specified attribute group already exist and can not be created.

ATTRDEF-017.n

ATTRDEF-017 (error) Attribute group %s not found.

DESCRIPTION

Specified attribute group not found.

ATTRDEF-018.n

ATTRDEF-018 (error) Internal error. Removing of attribute group %s failed.

DESCRIPTION

Removing of attribute group failed.

ATTRDEF-019.n

ATTRDEF-019 (error) Internal error. Removing all attribute groups of class %s failed.

DESCRIPTION

Removing of attribute groups failed.

ATTRDEF-020.n

ATTRDEF-020 (error) Error. Options -add, -delete or -move are exclusive with -attr_list.

DESCRIPTION

Options -add, -delete or -move are exclusive with -attr_list.

ATTRDEF-021.n

ATTRDEF-021 (error) Error. Attribute name -attr is required.

DESCRIPTION

Attribute name -attr is required.

ATTRDEF-022.n

ATTRDEF-022 (error) Error. Attribute list or single attribute is required.

DESCRIPTION

Attribute list or single attribute with add/delete/move option is required.

ATTRDEF-023.n

ATTRDEF-023 (error) Error. Option -anchor should be specified with -move.

DESCRIPTION

```
Option -anchor should be specified with -move after/before options.

### ATTRDEF-024.n ###
```

ATTRDEF-024 (error) Error. Either -add, -delete or -move should be specified.

DESCRIPTION

```
Either -add, -delete or -move should be specified.

### ATTRDEF-025.n ###
```

ATTRDEF-025 (error) Internal error. Error getting list of attribute groups for class %s failed.

DESCRIPTION

```
Getting list of attribute groups failed.

### ATTRDEF-026.n ###
```

ATTRDEF-026 (error) Attribute %s is user-defined.

DESCRIPTION

```
Specified attribute is user-defined and can not be deleted.

### ATTRDEF-027.n ###
```

ATTRDEF-027 (error) Attribute %s is user-defined.

DESCRIPTION

Specified attribute is user-defined. Options -width, -show|-hide, and -show_infotip|-hide_infotip are valid for this type of attribute.

ATTRDEF-028.n

ATTRDEF-028 (error) Attribute group %s is system defined.

DESCRIPTION

Specified attribute group is system defined and cannot be deleted or modified.

BS

BS-1 (error) Every block in a design built for scheduling must be triggered by a clock%s

DESCRIPTION

If a design is being built for scheduling, all processes must be sensitive to a clock edge. This is required to ensure that the behavior before and after synthesis matches.

WHAT NEXT

Make all blocks sensitive to a clock.

BS-2 (error) Blocks with an asynchronous reset are not supported in designs being built for scheduling%s

DESCRIPTION

Currently, scheduling does not support designs with an asynchronous reset.

WHAT NEXT

Modify the asynchronous reset into a synchronous reset.

BS-3 (error) Blocks with three state devices are not supported in designs being built for scheduling%s

DESCRIPTION

Currently, tri-state inference is not supported in designs being built for scheduling.

WHAT NEXT

Remove Z's from your hdl source.

BUDG-001 (error) Cannot use the file format specification '%s'.

DESCRIPTION

You receive this message because the specified file format specification cannot be used for one of the following reasons:

- No permission to write in the directory extracted from the file format specification.
- More than one conversion specification is found in the file format specification.
- No conversion specification is in the file format specification.
- Bad conversion specification is in the file format specification. The '%D' and '%C' conversion specifications are the only ones allowed.

WHAT NEXT

See the man page for the **allocate_budgets** command for more information on the **-file_format_spec** option.

SEE ALSO

allocate_budgets (2).

BUDG-002 (error) Separator string must be a single character.

DESCRIPTION

You receive this message because the separator string cannot be more than one character long.

WHAT NEXT

Reduce the separator string to one character.

BUDG-003 (error) Cannot specify '%c' as a separator character.

DESCRIPTION

You receive this message because the specified character cannot be used as a separator. Single or multiple slash characters (/), backslash characters (\), and space ( ) characters cannot be used as separator characters.

WHAT NEXT

Use characters such as the at sign (@), the underscore (_), and so on, as separator characters.

SEE ALSO

dc_allocate_budgets(2).

BUDG-004 (error) Must specify only one of these options: '%s'.

DESCRIPTION

You receive this message because this command requires that only one of the options in the list be specified.

WHAT NEXT

See the man page for this command for detailed information on valid options.

BUDG-005 (warning) The user budget setting on pin %s is not valid and is ignored.

DESCRIPTION

You receive this message because a pin does not meet one of the conditions described below and is ignored. Any pin specified in the **set_user_budget** command **-from** or **-to** option must be one of the following:

- A hierarchical pin.
- A pin on a sequential element.
- A clock.

WHAT NEXT

Ensure that every pin set by the the **set_user_budget** command **-from** or **-to** option meets one of the conditions listed above.

SEE ALSO

set_user_budget (2).

BUDG-006 (error) The command is not successful due to %s.

DESCRIPTION

You receive this message because the command did not succeed.

WHAT NEXT

See the command man page for more information.

BUDG-007 (error) '%s' cannot be opened.

DESCRIPTION

You receive this message because the specified file cannot be opened.

WHAT NEXT

See the command man page for more information.

SEE ALSO

dc_allocate_budgets (2).

BUDG-008 (warning) Cannot find design for object '%s', so ignoring it.

DESCRIPTION

You specified a cell that has no design.

WHAT NEXT

Either remove the cell name from the list of cells; or, if this warning is due to a unresolved reference, you can add the design to the search_path or link_library if you want, so that the linker can resolve the reference.

SEE ALSO

allocate_budgets (2), **characterize** (2), **write_environment** (2).

CDNO

CDNO-1 (error) Design ’%s’ has no schematic.

DESCRIPTION

WHAT NEXT

CDNO-2 (error) Can’t find the sheet template symbol for schematic ’%s’.

DESCRIPTION

WHAT NEXT

CDNO-3 (warning) Unnamed off-sheet connector encountered--pinInstance command not written.

DESCRIPTION

WHAT NEXT

CDNO-4 (warning) Unnamed port encountered--pinInstance command not written.

DESCRIPTION

WHAT NEXT

CDNO-5 (warning) Unnamed cell encountered--instance

command not written.

DESCRIPTION

WHAT NEXT

CDNO-6 (warning) Duplicate cell name ’%s’ renamed to ’%s’.

DESCRIPTION

WHAT NEXT

CHR-001 (error) Cannot specify '-no_timing' unless '-constraints' or '-connections' is also specified.

DESCRIPTION

The **characterize** command processes timing information only by default. The **-no_timing** option turns off characterization of timing information. This option is useful only in combination with **-constraints** or **-connections**.

WHAT NEXT

Determine what type of information you want to characterize and use the appropriate options.

CHR-002 (error) Characterize failed.

DESCRIPTION

The **characterize** command did not succeed on the given list of cells. For example, you may have used **characterize** on leaf cells.

WHAT NEXT

Check the list of cells to verify that the cells are hierarchical.

CHR-003 (error) Cannot characterize leaf cell '%s'.

DESCRIPTION

The **characterize** works only on hierarchical cells. This message indicates that a leaf cell was given to the **characterize** command.

WHAT NEXT

CHR-004 (warning) There are multiple clocks in the fanin of pin ’%s’ on cell ’%s’. Ignoring clock ’%s’.

DESCRIPTION

characterize will create clocks on ports of the subdesign. If a port is in the fanout of multiple clocks, **characterize** will arbitrarily choose one clock. This warning will be shown for other clocks that also fan in to the port.

WHAT NEXT

Use **check_timing** to find cases of multiple clock fanin on leaf cell clock pins. Often this will be due to multiplexed clock signals. Correct these problems with **set_disable_timing** so that only one clock is propagated.

CLE-01 (information) Command line editor mode is set to %s successfully.

DESCRIPTION

This information message confirms that the command line editor mode is set to the mode you specified. Use command **set_cle_options** to set the line editing mode to either vi or emacs.

WHAT NEXT

This is an information message only. No action is required.

SEE ALSO

set_cle_options(2)

CLE-02 (error) Command line editor mode cannot be set to %s. Proceeding with %s mode.

DESCRIPTION

This error message occurs when you attempt to set the line editor mode to an invalid value. The value can be either set to **vi** or **emacs**. If you attempt to set the edit mode to an invalid value, then the tool uses either the existing edit mode, if the mode is set, or the default emacs mode.

WHAT NEXT

Use the **set_cle_options** command to specify a valid mode.

SEE ALSO

set_cle_options(2)

CLE-03 (warning) Command line editor is already in %s mode.

DESCRIPTION

This warning message occurs when you specify the same value for the command line editor mode that is currently in use by the editor.

WHAT NEXT

This is a warning message only. No action is required.

However, if the result is not what you intended, use the **set_cle_options** command to set the line editing mode to either vi or emacs.

SEE ALSO

set_cle_options(2)

CLE-04 (warning) Variable sh_enable_line_editing can be set only in .synopsys_dc.setup file.

DESCRIPTION

This warning message occurs when you attempt to enable command line editing by setting the **sh_enable_line_editing** variable in the shell rather than in the .synopsys_dc.setup file.

WHAT NEXT

This is a warning message only. No action is required.

However, you can enable command line editing by setting the **sh_enable_line_editing** variable to true in the .synopsys_dc.setup file.

Refer to the *Design Compiler Command-Line Interface Guide* for more information.

SEE ALSO

sh_enable_line_editing(3)

CLE-05 (error) Command line editor is not enabled.

DESCRIPTION

This error message occurs when command line editing is not active.

WHAT NEXT

Set the **sh_enable_line_editing** variable to true in the .synopsys_dc.setup file to enable command line editing.

Refer to the *Design Compiler Command-Line Interface Guide* for more information.

SEE ALSO

sh_enable_line_editing(3)

CLE-06 (information) %s is currently in %s editing mode.

DESCRIPTION

This information message displays the current editing mode.

WHAT NEXT

This is only an informational message. No action is required.

However, you can use the **set_cle_options** command to set the line editing mode to either vi or emacs.

SEE ALSO

set_cle_options(2)

CLE-07 (information) Terminal beep is %s.

DESCRIPTION

This information message displays the current terminal beep mode.

WHAT NEXT

This is only an informational message. No action is required.

However, you can use the **set_cle_options** command to set the terminal beep to either on or off.

SEE ALSO

set_cle_options(2)

CLE-08 (error) Terminal beep mode value can be either on or off.

DESCRIPTION

This message occurs when you attempt to set the line editor beep mode to an invalid value. The value can be either **on** or **off**. If you attempt to set the beep mode to an invalid value, then the tool uses the existing beep mode.

WHAT NEXT

Use the **set_cle_options** command to specify a valid beep mode.

SEE ALSO

set_cle_options(2)

CLE-09 (warning) -defaults option will override other options.

DESCRIPTION

-defaults option will override the other options of **set_cle_options** command.

WHAT NEXT

This is only a warning message. No action is required.

SEE ALSO

set_cle_options(2)

CLUS-2 (error) Cell %s could not be assigned to a cluster.

DESCRIPTION

This message indicates that the specified new or modified cell could not be assigned to a cluster during optimization.

WHAT NEXT

CLUS-3 (info) Loading route layer data from technology library: %s.

DESCRIPTION

Indicates the library from which library routing layer data is being loaded from. This data is used to calculate delay values during optimizations which take cell locations into account.

WHAT NEXT

CLUS-4 (warning) Could not generate 'preferred' region for new cell %s in cluster %s.

DESCRIPTION

A new cell was added during location based optimization and was assumed to be at a specific location. The specific locations are supposed to be converted into 'preferred' regions because the environment variable lbo_use_cell_regions was set to 'true'. For this particular cell, it was not possible to determine a region. As a result, the PDEF for the design will indicate that the cell exists at a specific location.

WHAT NEXT

Determination of a region typically fails because it was not possible to determine the coordinates of the cell rows within the cluster. Make sure that the row orientation attribute ROW_ORIENT is set correctly for the cluster in question (default is horizontal).

CLUS-5 (error) Could not find a top cluster in the design.

DESCRIPTION

You receive this message because there is no top cluster in the design. This happens when every cluster becomes a placement obstruction. The result is that no cells can be written out in the PDEF.

WHAT NEXT

Simply add one cluster in the pdef. If you have pins, you should move them to the new cluster.

CLUS-6 (warning) Could not find rp cluster %s for cell %s.

DESCRIPTION

You receive this message because the expected cluster is not found in the design.

WHAT NEXT

Add the cluster information in the Physical Design Exchange Format (pdef) file or check the Synopsys database format (.db) design.

CMCR-003 (warning) replacing host options '%s'.

DESCRIPTION

The command is defining host/pool options with the name specified. However, options of the same name already exist. The original options will be removed, and the new host/pool options will replace the original ones.

CMCR-008 (error) the host options named '%s' does not exist.

DESCRIPTION

The named host/pool options referred to do not exist.

WHAT NEXT

Use the **set_host_options** command to create the named host/pool options.

CMCR-011 (error) Incomplete host/pool specification.

DESCRIPTION

Not enough parameters have been given to fully specify a host collection or compute pool. Either a named host list, the **-pool** option, or the **-submit_command** option must be given.

If you want to specify only the **-max_cores** parameter for the main (parent) job, give that option by itself, without any of the host/pool options mentioned above.

WHAT NEXT

Rerun the command with a complete set of options.

CMD

CMD-001 (error) Cannot specify ’%s’ with ’%s’.

DESCRIPTION

The listed command options are exclusive. Only one of them can be specified.

WHAT NEXT

Look at the manpage for this command for more information on command options.

CMD-002 (error) Value for ’%s’ cannot be negative

DESCRIPTION

The value for this option must be greater than or equal to zero.

WHAT NEXT

Enter the command again with a valid option value.

CMD-003 (error) Cannot specify %s without %s.

DESCRIPTION

One command option requires another.

WHAT NEXT

Refer to the manual page for this command for detailed information on valid options.

CMD-004 (error) Must specify one of these options: %s.

DESCRIPTION

This command requires that one of the options in the list is specified.

WHAT NEXT

Refer to the manual page for this command for detailed information on valid options.

CMD-005 (error) unknown command '%s'

DESCRIPTION

The command is not recognized.

WHAT NEXT

Look for a typographical error in the command. If it is correct, make sure that the program you are running supports the command, or you have the license to use the command.

CMD-006 (error) ambiguous command '%s' matched %d commands:
(%s)

DESCRIPTION

The command does not have sufficient characters to distinguish it from other commands. The first three commands which match the abbreviation are listed. To see them all, use the help as follows: if the abbreviation is cmd, type 'help cmd*'. This lists all commands that begin with 'cmd'.

WHAT NEXT

Type enough characters so the command is unambiguous.

CMD-007 (error) Required argument '%s' was not found

DESCRIPTION

The listed argument to the command might not be omitted.

WHAT NEXT

Supply the required argument.

CMD-008 (error) value not specified for option '%s'

DESCRIPTION

The listed argument requires a value (that is, it is not a boolean option), and none were supplied.

WHAT NEXT

Supply a value for the argument.

CMD-009 (error) value '%s' for option '%s' not of type '%s'

DESCRIPTION

The value given for the listed argument is not the correct type. For example, if 'abc' is given for an integer option, this error occurs.

WHAT NEXT

Supply a compatible value for the argument.

CMD-010 (error) unknown option '%s'

DESCRIPTION

The option is not recognized.

WHAT NEXT

If this is not a simple mistake, retype the command with by the -help option. This lists all of the possible options.

CMD-011 (error) ambiguous option '%s'

DESCRIPTION

The option does not have sufficient characters to distinguish it from other options.

WHAT NEXT

Type enough characters so that the option is unambiguous.

CMD-012 (error) extra positional option '%s'

DESCRIPTION

The command expects some positional arguments and has already received enough. It might also be the case that this was intended as a dash option and is misspelled.

WHAT NEXT

Verify that the option given is not a misspelled dash option. If it is not, use -help with the command to verify which arguments are already given.

CMD-013 (error) %s
Use error_info for more info.

DESCRIPTION

A script or complex command failed and there is a stack trace for the failure. The trace points out the source files and loops where the error occurred. The error_info command is used to display this stack.

WHAT NEXT

Fix the error indicated by error_info.

CMD-014 (error) Invalid %s value '%s' in list.

DESCRIPTION

A list argument is expected to be a common type (like integer or float) and one or more elements cannot be converted to that format.

WHAT NEXT

Fix the offending list element.

CMD-015 (error) could not open %s file "%s

DESCRIPTION

A script or an output redirect file cannot be opened.

WHAT NEXT

Verify that the file exists or that you have write access to the directory. Write access depends on the file type.

CMD-016 (error) could not close %s file "%s

DESCRIPTION

A script or an output redirect file cannot be closed.

WHAT NEXT

CMD-017 (warning) duplicate option ’%s’ ignored.

DESCRIPTION

The given option is already issued. This command uses the first value of the option, and subsequent values are ignored.

WHAT NEXT

Make sure this is the option you want to use. If so, decide which value you want and verify that you get the correct one.

CMD-018 (warning) duplicate option ’%s’ overrides previous value.

DESCRIPTION

The given option has already been issued. This command uses the last value of the option, and previous values are ignored.

WHAT NEXT

Make sure that this is the option you want to use. If so, decide which value you want and make sure that you get the correct one.

CMD-019 (error) value '%s' for option '%s' not in range (%s).

DESCRIPTION

The value given for the listed argument is not in the allowable range. For example, if 4 is given for an integer option, which has a range of 1 to 3, this error occurs.

WHAT NEXT

Supply a compatible value for the argument.

CMD-020 (error) unknown OR extra positional option '%s'

DESCRIPTION

The dash option is not recognized. Further, all positional arguments have already been received. This is most likely a misspelled dash option.

WHAT NEXT

Check to see if the option is misspelled. Look at the entire command, as other options may have misled the interpreter.

CMD-021 (warning) invoked %s outside of a loop

DESCRIPTION

The listed control command (break or continue) was used outside of the context of control structure (such as foreach, while, and so on).

WHAT NEXT

Look for a loop that ends prematurely or for a misspelled control word.

CMD-022 (warning) Can’t create alias named ’%s’ - %s%s.

DESCRIPTION

An attempt was create an alias with an invalid name. Invalid names include those which match an existing command or procedure, and those which can be converted to a decimal, hexadecimal, or octal number.

WHAT NEXT

Choose another name. Use ’help’ and ’alias’ (with no arguments) to see what names are in use.

CMD-023 (error) Alias loop: %s

DESCRIPTION

You have aliases that refer to one another.

WHAT NEXT

Use the alias command to look at the aliases listed in the diagnostic. Remove the loop and re-execute the command.

CMD-024 (error) can’t %s "%s": %s

DESCRIPTION

You attempted an operation on a variable which failed. You may have tried to read a non-existent variable (set var). Or, you may have tried to unset a non-existent or application-owned variable. The text of the message will indicate which operation failed.

WHAT NEXT

Verify that the variable exists with the printvar command. If it’s not a user variable, you cannot remove (unset) it.

CMD-025 (error) No manual entry for '%s'

DESCRIPTION

The topic for which you requested man pages does not exist.

WHAT NEXT

Verify that the topic is spelled correctly.

CMD-026 (error) %s required for the '%s' argument.

DESCRIPTION

The command is incomplete as entered. The specified argument requires a valid object or list of objects.

WHAT NEXT

Enter the command with valid values for all arguments.

CMD-027 (error) couldn't change working directory to '%s'

DESCRIPTION

The directory which you specified to the cd command is not valid.

WHAT NEXT

Verify that the directory is spelled correctly.

CMD-028 (error) couldn't get working directory name

DESCRIPTION

The pwd command was unable to access the current directory. It is most likely the case that the directory which you are in no longer exists,

WHAT NEXT

Use the cd command to get into an existing directory.

CMD-029 (warning) no aliases matched '%s'

DESCRIPTION

You specified a pattern to the unalias command, and there are no aliases which match that pattern.

WHAT NEXT

There is no adverse effect of this action. However, check the spelling of the arguments to unalias to ensure that you removed all of the aliases which you wanted to remove.

CMD-030 (warning) File '%s' was not found in search path.

DESCRIPTION

The 'which' command evaluated an filename argument and the file was not found.

WHAT NEXT

No adverse effect on the result of the command, but check spelling, etc.

CMD-031 (error) value '%s' for option '%s' is not valid. Specify one of:
%s

DESCRIPTION

The value given for the listed argument is not one of the limited allowable strings. This messages lists all of the appropriate values.

WHAT NEXT

Supply a compatible value for the argument.

CMD-032 (warning) command '%s' requires some options.

DESCRIPTION

No options were given for the command, yet some are required.

WHAT NEXT

Supply appropriate arguments.

CMD-033 (error) cannot source the current log file.

DESCRIPTION

An attempt to source the log file of the currently running interpreter is not allowed. It would cause the tool to infinitely loop.

WHAT NEXT

Copy the part of the log to be a source for another file, then source that file instead.

CMD-035 (error) Value for %s cannot be larger than the %s value.

DESCRIPTION

Some commands work in pairs, specifying a maximum and minimum value. The minimum value should be less than the maximum value. For example, never specify a **min_capacitance** which is larger than the **max_capacitance** for the same design or port.

WHAT NEXT

Remove the old value or use a different value.

CMD-036 (error) Value for list '%s' must have %s elements.

DESCRIPTION

The value given for the list argument does not have the correct number of elements. Some commands have list arguments which require either a specific number or an even number of elements. The message will indicate which it is.

WHAT NEXT

Supply a correct number of elements in the list.

CMD-037 (error) value '%s' for option '%s' is invalid: must be %s.

DESCRIPTION

The value given for the listed argument is greater than or less than the allowable limit. For example, if 4 is given for an integer option, which is required to be less than or equal to 3, this error occurs.

WHAT NEXT

Supply a compatible value for the argument.

CMD-038 (information) The '%s' option for %s is unsupported.%s

DESCRIPTION

The option which you specified is not currently supported.

WHAT NEXT

CMD-039 (information) The '%s' variable is unsupported.%s

DESCRIPTION

The variable which you specified is not supported.

WHAT NEXT

If a replacement variable is specified, use it instead of this one.

CMD-040 (information) No %s matched '%s'.

DESCRIPTION

In command or variable search functions (help and printvar), you specified a pattern that did not match any variables or commands.

Note that printvar cannot find a specific array element; it can only find the entire array by name.

WHAT NEXT

Try using more wildcards (* or ?) in your search pattern.

CMD-041 (information) Defining new variable '%s'.

DESCRIPTION

This message is issued when a variable is set for the first time.

When combined with the **printvar** command, this message can be used to isolate spelling errors in system (application) variables. However, like many debugging features, this has significant CPU cost. Therefore, the feature should only be used interactively or when developing scripts.

This feature is enabled by setting the **sh_new_variable_message** variable to true. When combined with a true value for variables **sh_new_variable_message_in_script** or **sh_new_variable_message_in_proc**, this setting causes a warning message (CMD-042) to be issued, which indicates that the performance of scripts (or Tcl procedures) will be adversely affected. To enable the feature in Tcl procedures, set the **sh_new_variable_message_in_proc** variable to true. To enable the feature in Tcl scripts, set the **sh_new_variable_message_in_script** variable to true.

In the following example, the user has misspelled the variable **sh_continue_on_error** by making it plural. With this feature, debugging is simplified.

```
prompt> set sh_continue_on_errors true
Information: Defining new variable 'sh_continue_on_errors' (CMD-041)
true
prompt> printvar sh*
sh_arch              = "sparcOS5"
sh_continue_on_error = "false"
sh_continue_on_errors = "true"
```

```
sh_enable_page_mode  = "false"
sh_new_variable_message = "true"
sh_new_variable_message_in_proc = "false"
sh_product_version   = ""
sh_source_uses_search_path = "false"
prompt> unset sh_continue_on_errors
prompt> set sh_continue_on_error true
true
```

Application variables are always defined, so if this message appears, a new user-defined variable has been created.

WHAT NEXT

If attempting to set an application variable, use **printvar** with wildcards to get the correct spelling for the variable.

SEE ALSO

printvar(2), sh_new_variable_message(3), sh_new_variable_message_in_proc(3), sh_new_variable_message_in_script(3), CMD-042(n).

CMD-042 (warning) Enabled new variable message tracing - Tcl scripting optimization disabled.

DESCRIPTION

This message is issued when you enable new variable tracing for Tcl scripts or procedures. That occurs when you set the variable **sh_new_variable_message** to TRUE, and when you set the variables **sh_new_variable_message_in_proc** or **sh_new_variable_message_in_script** to TRUE. It warns you that the performance of the application will be negatively mpacted because this feature is costly in CPU time when enabled.

This feature is intended for debugging, and should only be used interactively or when developing scripts. It should not be used in a main flow.

WHAT NEXT

Set one or more of the variables to FALSE unless you are debugging a script.

SEE ALSO

sh_new_variable_message(3), sh_new_variable_message_in_proc(3), sh_new_variable_message_in_script(3).

CMD-050 (error) Unknown procedure '%s'.

DESCRIPTION

The procedure name argument to **define_proc_attributes** is not a procedure.

WHAT NEXT

Verify that the argument is correct.

CMD-051 (error) Procedure '%s' cannot be modified.

DESCRIPTION

The procedure that you passed to **define_proc_attributes** is a permanent procedure that cannot be modified.

WHAT NEXT

The procedure might be part of the application, in which case it was correctly defined with *-permanent*. If it is not part of the application, it is possible that it was erroneously defined with *-permanent*.

CMD-052 (error) Unknown command group '%s'

DESCRIPTION

The command group referenced does not exist. For example, using the *-command_group* option with the **define_proc_attributes** command, and passing in a non-existent command group will raise this error.

WHAT NEXT

Verify that the correct command group name is being used.

CMD-053 (warning) The body of procedure '%s' is protected

DESCRIPTION

You attempted to examine the body of a procedure using **info body**. That procedure was

protected by the writer so that it’s body cannot be displayed.

WHAT NEXT

No action required.

CMD-060 (error) Syntax error in argument definition %d for proc ’%s’.

DESCRIPTION

Using the *-define_args* option for **define_proc_attributes**, there is some kind of syntax error, for example, an improperly formatted list.

WHAT NEXT

Use **error_info** to narrow the problem, then reenter the command.

CMD-061 (error) Need at least 2 fields in argument definition %d for proc ’%s’.

DESCRIPTION

Using the *-define_args* option for **define_proc_attributes**, an argument definition had insufficient arguments. At least 2 are required: the argument name and the option help text.

WHAT NEXT

Reenter the argument definition with the correct number of fields.

CMD-062 (error) Unknown %s ’%s’ in argument definition %d (%s) for proc ’%s’.

DESCRIPTION

Using the *-define_args* option for **define_proc_attributes**, either a data type or attribute is invalid.

The allowable data types are string, boolean, int, float, and list. The allowable attributes are required and optional.

WHAT NEXT

Correct the invalid data and reenter the command.

CMD-063 (error) Illegal name '%s' for Boolean argument definition %d for proc '%s': must begin with '-'.

DESCRIPTION

Using the *-define_args* option for **define_proc_attributes**, you attempted to create a Boolean argument with a name not preceded by a '-'. Boolean arguments require a leading '-'.

WHAT NEXT

Correct the argument name and reenter the command.

CMD-064 (warning) Value help ignored for Boolean option %s in argument definition %d for proc '%s'.

DESCRIPTION

Using the *-define_args* option for **define_proc_attributes**, you tried to add value help for a Boolean argument. Boolean arguments cannot have the value help.

WHAT NEXT

Remove the value help field for boolean arguments and reenter the command.

CMD-065 (error) Can't specify both 'optional' and 'required' in argument

definition %d (%s) for procedure '%s'

DESCRIPTION

This message indicates an attempt to specify conflicting flag values as part of the definition of a procedure argument within the **define_proc_attributes** command.

WHAT NEXT

Decide whether the argument is optional or required, and remove the opposite flag.

CMD-066 (error) Must specify a value for attribute 'values' when using '%s'
option type as in option %d (%s) for procedure '%s'

DESCRIPTION

This message is issued by the **define_proc_attributes** command when you attempt to define an argument whose value must be one of a set of pre-defined strings (the one_of_string data type), without specifying the set of valid strings.

WHAT NEXT

If the value type really needs to be one_of_string, pass the values in as a list within the attributes list (i.e. {values {a b c}}).

CMD-067 (error) Invalid attribute specification for attribute '%s' (%s)
in option %d (%s) for procedure '%s'

DESCRIPTION

This message is issued by the **define_proc_attributes** command. It indicates an incorrect attempt at specifying an attribute for a procedure argument. The reason for the error is included in the message.

WHAT NEXT

Fix the syntax of the command and try again.

CMD-068 (error) Could not find procedure '%s'. Arguments can't be parsed.

DESCRIPTION

This message indicates an attempt to use the parse_proc_arguments command from within a procedure which has not been defined using define_proc_attributes.

WHAT NEXT

Define the procedure's arguments using define_proc_attributes and try again.

CMD-069 (error) Could not set '%s(%s)' while parsing arguments in '%s'.

DESCRIPTION

This message indicates that the **parse_proc_arguments** command was not able to set the specified Tcl array variable to hold the value of a command option.

WHAT NEXT

This typically indicates that the variable was read-only. Use a different variable and try again.

CMD-070 (error) %s can only be called from within a procedure

DESCRIPTION

This message indicates an attempt to use the given command from the interpreter command line. Calls to this command are only supported from within a Tcl procedure.

WHAT NEXT

Create a procedure and call the command from within the scope of the procedure body.

CMD-080 (error) Command '%s' is disabled.

DESCRIPTION

Although part of the application, the listed command is not currently enabled.

WHAT NEXT

Look at the user documentation to determine how various commands are enabled and disabled.

CMD-081 (information) script '%s' stopped at line %d due to %s.

DESCRIPTION

The execution of a script was terminated. This message tells you which script stopped, the line number where it stopped, and why it stopped.

If the **sh_continue_on_error** variable is false (the default), any Tcl error, either syntax or semantic, stops the script. If **sh_continue_on_error** is false and the **sh_script_stop_severity** variable is W or E, messages of that severity or higher stop the script.

If the **sh_continue_on_error** variable is true, the **sh_script_stop_severity** variable is ignored and the script continues even if there are errors or warnings.

WHAT NEXT

Use the information in this message to identify and correct the source of errors and warnings. Then reexecute the script.

SEE ALSO

sh_continue_on_error (3), **sh_script_stop_severity** (3).

CMD-082 (information) %s occurred at or before line %d in script '%s'.

DESCRIPTION

You receive this message if an error or warning occurs while a script is executing,

and the variable **sh_source_emits_line_numbers** is set to E or W. A setting of E causes this message to be issued only if an error occurs, while for a setting of W, this message is issued for both warnings and errors. This message tells you the error or warning and the line and script in which it occurred.

The setting of the **sh_script_stop_severity** variable affects the output of the CMD-082 message. If **sh_script_stop_severity** is set to E, the script stops executing if an error occurs; for a setting of W, the script stops executing if a warning or error occurs. In both cases, message CMD-081 is issued, and takes precedence over CMD-082.

WHAT NEXT

Use the information in this message to identify and correct the source of errors and warnings. Then reexecute the script.

SEE ALSO

sh_script_stop_severity (3), **sh_source_emits_line_numbers** (3); **CMD-081** (n).

CMD-085 (warning) Renaming %s %s cause %s commands which use it to fail.

DESCRIPTION

You receive this message if you rename a command which is not a user-defined Tcl procedure. Renaming commands can be dangerous. Parts of the application are written in Tcl, and if you rename a command that the application is using, it is possible that those parts of the application will not function.

The only true use for **rename** is to wrap a command. For example:

```
shell> rename command1 command1_orig
shell>  \
  proc command1 {args} {
    # ...
    eval command1_orig $args
    # ...
  }
```

If you use **rename** in this way, it is more likely that application will continue to function correctly. Still, use **rename** with extreme care and at your own risk.

WHAT NEXT

Consider using **alias**, Tcl procedures, or a private namespace before using **rename**.

SEE ALSO

rename (2).

CMD-086 (error) Could not find command '%s'.

DESCRIPTION

This message indicates that the command name entered does not exist and therefore operation on associated command mode could not be performed.

WHAT NEXT

Check to make sure command name is typed correctly.

CMD-087 (error) The command requires either a command name or a command mode name.

DESCRIPTION

This command requires either a command name or a command mode name to be specified.

WHAT NEXT

Enter **set_current_command_mode** with the **-command** option flag followed by a command name or the **-mode** option flag followed by a command mode name. These options are mutually exclusive.

CMD-088 (error) Could not find command mode '%s'.

DESCRIPTION

This message indicates that the command mode name entered does not exist and therefore could not be set as the current mode.

WHAT NEXT

Check to make sure command mode name is typed correctly. **get_command_modes -all** lists all defined command mode names.

CMD-089 (error) Initialization of command '%s' failed.

DESCRIPTION

This message indicates that a failure occurred during initialization and the specified command could not be evaluated.

CMD-090 (error) Initialization of command mode '%s' failed.

DESCRIPTION

This message indicates that a failure occurred during initialization of the command mode and the specified command mode could not be made current.

CMD-100 (warning) Detected use of obsolete/unsupported feature. The following will not be available in a future release of the application: %s. Use %s instead

DESCRIPTION

You have used a feature which is no longer supported by the application, and the feature is planned to be removed at some future date. The supported method is given in the message.

WHAT NEXT

Update your command usage as indicated.

CMD-101 (error) Failed to set value of option %s for command %s.

DESCRIPTION

A run of a command such as set_command_option_value failed to set the default or current value of an option. The command option may not have been enabled for value-tracking or a conversion error may have occurred when attempting to set the option value.

WHAT NEXT

It may be necessary to enable the option for value-tracking.

CMD-102 (error) No such positional option %d for command %s.

DESCRIPTION

An attempt was made to find the positional option of the command at the given position. No such positional option was found. Either the given command has no positional options, or the given position is "out of range". Note that positional options are numbered 0, 1, 2, ... (N-1) where N is the number of postional options of the command.

WHAT NEXT

Retry the operation using a positional option position that is "in range" for the command.

CMD-103 (error) A Severe error has occurred. To ensure that the script does not continue, the value of shell_continue_on_error has been overridden to be false. Your script is being interrupted. To see the Tcl call stack for the part of your script which generated the Severe error use the error_info command.

DESCRIPTION

A Severe error has occurred during a command execution. To ensure that the script does not continue, the value of shell_continue_on_error has been overridden to be false. Your script is being interrupted. To see the Tcl call stack for the part of your script which generated the Severe error use the error_info command.

WHAT NEXT

For details on the Severe error please look in your log file. You can also run man on the Severe error id to learn more about the error. Study the Severe error and try to fix the error in your script.

CMD-104 (error) Variable ’%s’ is not an application variable.

Value will still be set in Tcl.

DESCRIPTION

The specified variable is not declared as an application variable (not returned by get_app_var -list). This message is only generated when the application variable sh_allow_tcl_with_set_app_var is true.

Please see the manpages for get_app_var and set_app_var for additional details.

WHAT NEXT

Make sure you are using the correct variable name.

CMD-105 (warn) Option '%s' is obsolete, use '%s' instead.

DESCRIPTION

This option is obsolete, you should use a different option for this command feature. The code has automatically used a compatible option setting, but in the future the old option may be removed, so you should update your scripts.

WHAT NEXT

Update your script to use the new option.

CMD-106 (warn) Option '%s' is obsolete, ignoring it.

DESCRIPTION

This option is no longer supported, specifying it has no effect.

WHAT NEXT

Update your script

CMD-999 (severe) A Severe error has occurred during testing.

DESCRIPTION

A Severe error has occurred during testing. This should never happen in production.

WHAT NEXT

CNTXT-001 (error) Cannot characterize context in min and max mode.

DESCRIPTION

The design has a minimum and a maximum operating condition defined on it. Context characterization requires only one operating condition be set on the design.

WHAT NEXT

Set the operating condition for which you want to characterize the context on the design.

CNTXT-002 (information) Characterizing the context for cell '%s'

DESCRIPTION

You receive this message to inform you that the **characterize_context** command is characterizing the context for the specified cell.

WHAT NEXT

This is an informational message only. No action is required on your part.

CNTXT-003 (information) Deleting the context for cell '%s'

DESCRIPTION

The internal data structures associated with the context of the cell were deleted. Therefore the context cannot be written out (*write_context*) or reported (*report_context*). This occurs when the context is deleted by *remove_context*.

WHAT NEXT

This is an information message. No action is required unless you want to use *write_context* or *report_context* on the cell for which **CNTXT-003** was issued. Otherwise context must be created by *characterize_context*.

CNTXT-004 (error) This command applies to hierarchical cells only

Cell '%s' is a leaf cell.

DESCRIPTION

You receive this message because the specified cell is a leaf cell, and the command you executed applies only to hierarchical cells.

WHAT NEXT

Re-execute the command and ensure that you do not specify a leaf cell.

CNTXT-005 (information) The design has rise/fall qualified exceptions which will not be written out.

DESCRIPTION

You receive this message to inform you that **write_context** will not write out the rise/fall qualified exceptions in your design. Rise/Fall qualified exceptions are supported only by Primetime; neither **write_context** nor **write_sdc** will write them out for either dcsh or dctcl mode.

WHAT NEXT

This is an informational message only. No action is required on your part.

CO-001 (error) No design library opened.

DESCRIPTION

This error message occurs when the design library is not loaded.

WHAT NEXT

Open a design library using *open_mw_lib*.

SEE ALSO

open_mw_lib(2)

CO-002 (error) Cannot read input file %s : %s.

DESCRIPTION

This error message occurs because the stated input file could not be read. Possible reasons for this are that the file does not exist, or there is no read permission on the file.

WHAT NEXT

Check that the stated input file is available for read access.

SEE ALSO

import_design(2)

CO-003 (error) Cannot create partitioner, %s.

DESCRIPTION

This error message occurs because the partitioner could not be created. This most likely would happen because there is no free memory on the machine.

WHAT NEXT

Check that the machine has enough free memory.

SEE ALSO

read_partition(2)

CO-004 (error) Cannot find partitioner, %s.

DESCRIPTION

This error message occurs because the partitioner specified does not exist.

WHAT NEXT

Use read_partition -input_files <file.v> to create a partitioner.

SEE ALSO

create_partition(2)
read_partition(2)

CO-005 (error) Option %s cannot be used with other options.

DESCRIPTION

This error message occurs because the option specified is mutually exclusive with all other options.

WHAT NEXT

Use specifed option alone.

SEE ALSO

create_partition(2)
list_partition_data(2)
read_partition(2)
set_partition_data(2)

CO-006 (error) Cannot create output directory %s.

DESCRIPTION

This error message occurs because the tool could not create the specified directory.

WHAT NEXT

Check that you have write permission in the specified directory.

SEE ALSO

list_partition_data(2)
create_partition(2)

CO-007 (error) Option -initialize_floorplan cannot be used with %s.

DESCRIPTION

This error message occurs because of certain limitations on the -initialize_floorplan option. This option will only work if there is exactly 1 top module in the design. Also this option does not handle situation when there are multiple instantiated modules (MIMs) which are marked as physical (ie sub-block). It is ok to have MIMs as logical nodes. Finally this option requires that all sub-block have an area estimate, so that the sizes of each sub-block can be determined.

WHAT NEXT

If you have any of above situations, you can output Verilog files only. Then proceed to load the verilog and create a floorplan.

SEE ALSO

list_partition_data(2)
set_partition_data(2)
create_partition(2)

CO-008 (error) Option %s requires a value between %s and %s.

DESCRIPTION

This error message occurs because the specified option will only take values in a

certain range. For example, a utilization value should be between 0 and 1.

WHAT NEXT

Input values within allowable range.

SEE ALSO

create_partition(2)
set_partition_data(2)
read_partition(2)

CO-009 (error) The options %s are mutually exclusive.

DESCRIPTION

This error message occurs because the specified options are mutually exclusive and so only one of the specified options can be used at a time.

WHAT NEXT

Run the command with only one of the specified option. You can run the command multiple times each time with a different option.

SEE ALSO

list_partition_data(2)
create_partition(2)
run_parallel_jobs(2)

CO-010 (error) The option %s cannot be used with a list of module names.

DESCRIPTION

This error message occurs because the specified option cannot be used at the same time as specifing a list of module names. This option was meant for use at the top level.

WHAT NEXT

Do not specify the module name list.

SEE ALSO

list_partition_data(2)
create_partition(2)

CO-011 (error) No verilog files have been loaded.

DESCRIPTION

This error message occurs because you have not yet loaded any verilog files to the partitioner.

WHAT NEXT

Use read_partition -input_files <files> to load your verilog files.

SEE ALSO

create_partition(2)
list_partition_data(2)
read_partition(2)

CO-012 (error) Found multiple definitions of module %s.

DESCRIPTION

This error message occurs because the input verilog files contain a module that is defined more than once. When this happens, one of the modules will remain in existence while the others are ignored.

WHAT NEXT

It is best to remove the redundant modules as there is no way to tell which module survived. However, if you are certain that all the modules with the same name are actually identical, then it is safe to proceed.

SEE ALSO

list_partition_data(2)
create_partition(2)

CO-013 (error) Cannot set an %s keepout on module %s.

DESCRIPTION

This error message occurs because the specified module does not allow you to set an internal or external keepout. Internal keepouts are only allowed on logical modules, black boxes, and the top level. External keepouts are not allowed at the top level of design.

WHAT NEXT

Check the specified module. If it is a missing module, then convert it to a black box by giving it an area estimate.

SEE ALSO

list_partition_data(2)
create_partition(2)
set_partition_data(2)

CO-014 (error) Use -force option to set area on module %s.

DESCRIPTION

This error message occurs because the specified module does not allow you to set an area on it normally. Normal usage is to set area only on missing modules. For other modules, the area is calculated from the utilization and the cells inside the module.

WHAT NEXT

If you want to override the estimated area, then use the -force option.

SEE ALSO

list_partition_data(2)
create_partition(2)
set_partition_data(2)

CO-015 (error) Use -force option to set utilization on module %s.

DESCRIPTION

This error message occurs because the specified module does not allow you to set an

utilization on it normally. This is to highlight that this module has a special consideration. One example is that this module may be multiply instantiated, so by changing this utilization you are actually changing mulitple instantiations.

WHAT NEXT

If you are sure you want to do this, then use the -force option.

SEE ALSO

list_partition_data(2)
create_partition(2)
set_partition_data(2)

CO-016 (error) Use -force option to set physical/logical on module %s.

DESCRIPTION

This error message occurs because the specified module did not allow you to change it between physical and logical states. This is to highlight that this module has a special consideration. The most common is that this module may be multiply instantiated. So for example, if you are marking it physical, you are actually changing mulitple instantiations to be physical.

WHAT NEXT

If you are sure you want to do this, then use the -force option.

SEE ALSO

list_partition_data(2)
create_partition(2)
set_partition_data(2)

CO-017 (error) Cannot set utilization on leaf or IO module %s.

DESCRIPTION

This error message occurs because the specified module is a leaf or IO module. These modules have a fixed size and thus it does not make sense to set a utilization on them.

WHAT NEXT

Do not set utilization on leaf or IO modules.

SEE ALSO

list_partition_data(2)
create_partition(2)
set_partition_data(2)

CO-018 (error) Cannot set module %s as physical because has physical %s.

DESCRIPTION

This error message occurs because the specified module is either the child or parent of an already physical module. This is not allowed because nested physical modules is not supported.

WHAT NEXT

Determine which of the nested modules really should be physical and mark only that one as physical.

SEE ALSO

list_partition_data(2)
create_partition(2)
set_partition_data(2)

CO-019 (error) Cannot open file %s for %s.

DESCRIPTION

This error message occurs because the stated input file could not be opend for read or write. Possible reasons for this are that the file does not exist, or there is no read/write permission on the file or there is no disk space.

WHAT NEXT

Check that the stated input file is available for read (or write) access.

SEE ALSO

list_partition_data(2)
create_partition(2)
read_partition(2)

CO-020 (error) Internal error: %s %s.

DESCRIPTION

This error message occurs because there has been an unexpected internal error.

WHAT NEXT

Contact Synopsys support for further assistance.

SEE ALSO

list_partition_data(2)
create_partition(2)
run_parallel_jobs(2)
send_flow_Status(2)

CO-021 (error) Cannot access output directory %s.

DESCRIPTION

This error message occurs because the specified output directory either does not exist or is protected.

WHAT NEXT

Check that the output directory is available for read and write.

SEE ALSO

list_partition_data(2)
create_partition(2)

CO-022 (error) Library length unit %s not %s.

DESCRIPTION

This error message occurs because the tech file length units are in a not supported length. Typically they should be in microns.

WHAT NEXT

Change the tech file length units to microns or contact Synopsys support for further assistance.

SEE ALSO

list_partition_data(2)
create_partition(2)
read_partition(2)

CO-023 (error) Need to close all CEL views before using %s

DESCRIPTION

This error message occurs because the command or option you are using requires that all CEL views are closed. This is because this command or option modifies certain CEL views and if they are opened while this command is executed, that may cause database consistency issues.

WHAT NEXT

Use close_mw_cel * to close all CEL views before rerunning the command.

SEE ALSO

list_partition_data(2)
create_partition(2)

CO-024 (error) Incorrect usage of option -parallel.

DESCRIPTION

This error message occurs because you have given an incorrect input to **run_parallel_jobs -parallel** option. The option -parallel takes as input either the string "all" or a positive integer.

WHAT NEXT

Look at the man page of run_parallel_jobs for more details.

SEE ALSO

run_parallel_jobs(2)

CO-025 (error) Option -job_name is required.

DESCRIPTION

This error message occurs because given the options you have specified, the option -job_name is required. There are certain option settings in which -job_name is not required, but with other option settings -job_name is required.

WHAT NEXT

Look at the man page of run_parallel_jobs for more details.

SEE ALSO

run_parallel_jobs(2)

CO-026 (error) Option %s requires a %s.

DESCRIPTION

This error message occurs because you have given an incorrect input to an option. Look at the error message for details on which option is incorrectly specified and what input is required to correct it.

WHAT NEXT

Look at the man page of the command for more details.

SEE ALSO

run_parallel_jobs(2)
send_flow_status(2)

CO-027 (error) Nested calls to run_parallel_jobs not supported.

DESCRIPTION

This error message occurs because you tried to run more than one *run_parallel_jobs* command. This is not supported. Only 1 *run_parallel_jobs* can be executed at a time.

WHAT NEXT

Look at the man page of *run_parallel_jobs* for more details.

SEE ALSO

run_parallel_jobs(2)

CO-028 (error) Option %s or %s environment variable is required.

DESCRIPTION

This error message occurs because the specified option must be used or the specified environment variable must be set.

WHAT NEXT

Look at the man page of *send_flow_status* for more details.

SEE ALSO

run_parallel_jobs(2)
send_flow_status(2)

CO-029 (error) Command %s has failed.

DESCRIPTION

This error message occurred because the specified command has failed. This is a generic failure message. There should be more detailed messaging on the cause of failure before this message was output.

WHAT NEXT

Look for previous error or warnning messages before this message. Look at the man page of the command.

SEE ALSO

run_parallel_jobs(2)
send_flow_status(2)

CO-030 (error) Cannot find %s job(s) to %s.

DESCRIPTION

This error message occurred because the specified job(s) could not be found. They may have died unexpectedly, or the wrong jobs were specified. If the specified job(s) is "any" that means that no jobs were found.

WHAT NEXT

Check that you specified the correct jobs.

SEE ALSO

run_parallel_jobs(2)
send_flow_status(2)

CO-031 (error) Please specify name of partition to remove.

DESCRIPTION

This error message occurs because you tried to remove a partitioner without using the -name option and there is more than one partitioner available. For safety, in this situation, it is required that you specify the partitioner to be removed.

WHAT NEXT

The log file contains a list of available partitioners. Rerun command with the -name option with the name of partitioner you want to remove.

SEE ALSO

create_partition(2)

CO-032 (error) Option %s can only be used with option %s.

DESCRIPTION

This error message occurs because you tried to use an option which only works in conjunction with another option.

WHAT NEXT

Look at man page of command to see why these options must be used together.

SEE ALSO

create_partition(2)

CO-501 (warning) Cannot find module, %s.

DESCRIPTION

This warning message occurs because you have specified a module that does not exist in the partitioner. This module will be skipped.

WHAT NEXT

It is likely a typo, check the module name is spelled correctly.

SEE ALSO

create_partition(2)
list_partition_data(2)
set_partition_data(2)

CO-502 (warning) Module %s has a terminal %s which has %s.

DESCRIPTION

This warning message occurs because an issue with the specified terminal was found while loading the specified module. This issue will not stop the loading of the verilog files to the partitioner, but it implies that there may be an issue (in verilog) with this module that should be further investigated.

WHAT NEXT

Take a look at the specified verilog module and terminal to further investigate this issue.

SEE ALSO

list_partition_data(2)
create_partition(2)
read_partition(2)

CO-503 (warning) Cannot find leaf module %s in MW lib %s.

DESCRIPTION

This warning message occurs because a leaf module was found in verilog, but was not found in the MW reference libraries. This is means that this cell will not have any area associated with it, ie it will be a missing module.

WHAT NEXT

If this leaf module is supposed to be missing (ie it is intended to be a black box), then there is no problem. However if this leaf module is intended to be a standard cell, a hard macro, or an IO, then it should not be missing. Check your setup to ensure all the MW reference libraries are available and this cell is included in the libraries.

SEE ALSO

list_partition_data(2)
create_partition(2)
read_partition(2)

CO-504 (warning) Need to start_gui to see partitioner window.

DESCRIPTION

This warning message occurs because you have not started the gui yet. The partitioner window will not pop up unless you have started the gui.

WHAT NEXT

Start the gui with start_gui command.

SEE ALSO

create_partition(2)
partition_design(2)
read_partition(2)
start_gui(2)

CONV-1 (error) Undefined variable on or near line %d at or near '%s'.

DESCRIPTION

WHAT NEXT

CONV-2 (error) Undefined operator on or near line %d at or near '%s'.

DESCRIPTION

WHAT NEXT

CONV-3 (error) Incorrect number of operands on or near line %d at or near '%s'.

DESCRIPTION

WHAT NEXT

CONV-4 (error) Invalid operand type on or near line %d at or near '%s'.

DESCRIPTION

WHAT NEXT

CONV-5 (error) Evaluation error on or near line %d at or near

’%s’.

DESCRIPTION

WHAT NEXT

CONV-6 (error) Internal error.

DESCRIPTION

WHAT NEXT

CONV-7 (error) Evaluation error on or near line %d at or near ’%s’.

DESCRIPTION

WHAT NEXT

CONV-8 (error) Error on or near line %d at or near ’%s’

DESCRIPTION

WHAT NEXT

CONV-9 (error) Operator used in bad context on or near line %d

at or near ’%s’.

DESCRIPTION

WHAT NEXT

CONV-10 (error) Defining new variable ’%s’.

DESCRIPTION

WHAT NEXT

COPT-001 (error) -only_psyn is used, can not use CTS related options.

DESCRIPTION

You specify one or more CTS related options when -only_psyn is being used.

WHAT NEXT

This is only an error message.

SEE ALSO

clock_opt(2)

COPT-002 (error) -only_cts is used, you can not use optimization options.

DESCRIPTION

You specify one or more optimization related options when -only_cts is being used.

WHAT NEXT

This is only an error message.

SEE ALSO

clock_opt(2)

COPT-003 (error) You must specify either "low", "medium" or "high" in -effort_psyn option.

DESCRIPTION

You must specify either "low", "medium" or "high" in -effort_psyn option.

WHAT NEXT

This is only an error message.

SEE ALSO

clock_opt(2)

COPT-004 (error) -only_optimize_pre_cts_power is used, any options other than -operating_condition cannot be used.

DESCRIPTION

WHAT NEXT

This is only an error message.

SEE ALSO

clock_opt(2)

CORRLIB-1 (error) Required option %s is not defined.

DESCRIPTION

This error message occurs when the specified option is not defined in the command shell.

WHAT NEXT

Define the required option using the Library Compiler command shell **set_correlate_library_options** command.

SEE ALSO

set_correlate_library_options(2)

CORRLIB-2 (error) Failed loading library %s.

DESCRIPTION

This error message occurs when the tool cannot read the library defined with the **db_file** option.

WHAT NEXT

Make sure that the library file exists.

CORRLIB-3 (error) Library correlation failed.

DESCRIPTION

This error message because an error occurred during the library correlation flow.

WHAT NEXT

Refer to all error and warning messages issued during the correlation flow.

CORRLIB-4 (error) File %s not found.

DESCRIPTION

This error message occurs when the specified file is not found in the current path or the searching path.

WHAT NEXT

Make sure the file exists and run the command again.

CORRLIB-5 (error) Failed reading %s.

DESCRIPTION

This error message occurs when the tool fails to read the required library.

WHAT NEXT

Check the library .db file and run the command again.

CORRLIB-6 (warning) Failed analysis on %s %s.

DESCRIPTION

This warning message occurs when reading information from a .db file for a specific cell, port, or arc.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, check the library and other error messages for the cause.

EXAMPLE MESSAGE

```
Warning: Failed analysis on cell CELL1.  (CORRLIB-6)
```

CORRLIB-7 (error) Required information %s not found or incorrectly defined.

DESCRIPTION

This error message occurs when the specified information in the library .db file is not found or is incorrectly defined.

WHAT NEXT

Modify the library so it contains the correct required information and run the command again.

CORRLIB-8 (warning) Cell %s does not have the required CCS Noise information for correlation.

DESCRIPTION

This warning message occurs when CCS Noise information does not exist for the specified cell in the .db file.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, run the command again using the correct .db file for the specified cell.

EXAMPLE MESSAGE

Warning: Cell cell_under_test does not have the required CCS Noise information for correlation. (CORRLIB-8)

CORRLIB-100 (error) .

DESCRIPTION

This message occurs when .

WHAT NEXT

Please refer to .

EXAMPLES

EXAMPLE MESSAGE

Error: . (CORRLIB-100)

CORRLIB-101 (error) Required option %s NOT defined.

DESCRIPTION

This message occurs when required options NOT defined in command shell.

WHAT NEXT

Please define the required option using Library Compiler command shell command set_correlate_library_options.

EXAMPLES

EXAMPLE MESSAGE

Error: Required option db_file NOT defined. (CORRLIB-101)

CORRLIB-102 (error) Failed loading library %s.

DESCRIPTION

This message occurs when there was failure reading library defined with option db_file.

WHAT NEXT

Please make sure the library file exist.

EXAMPLES

EXAMPLE MESSAGE

Error: Failed loading library corr.db. (CORRLIB-102)

CORRLIB-103 (error) Library correlation failed.

DESCRIPTION

This message occurs whenever there’s error during the library correlation flow.

WHAT NEXT

Please refer to all error/warning message issued during correlation flow.

EXAMPLES

EXAMPLE MESSAGE

Error: Library correlation failed. (CORRLIB-103)

CORRLIB-104 (error) File %s NOT found.

DESCRIPTION

This message occurs when file NOT found in current path or searching path.

WHAT NEXT

Please make sure the file exist.

EXAMPLES

EXAMPLE MESSAGE

Error: File corr.lib NOT found. (CORRLIB-104)

CORRLIB-105 (error) Failed reading %s.

DESCRIPTION

This message occurs when tool failed reading required library.

WHAT NEXT

Please check the library db file.

EXAMPLES

EXAMPLE MESSAGE

```
Error: Failed reading corr.db. (CORRLIB-105)
```

CORRLIB-106 (error) Failed analysys on %s %s.

DESCRIPTION

This message occurs when reading information from db file for specific cell, port or arc.

WHAT NEXT

Please check the library and other error messages.

EXAMPLES

EXAMPLE MESSAGE

```
Error: Failed analysys on cell CELL1.  (CORRLIB-106)
```

CORRLIB-107 (error) Required information %s NOT found or incorrectly defined.

DESCRIPTION

This message occurs when required information in DB NOT found or incorrectly defined.

WHAT NEXT

Please modify the library to have correct required information.

EXAMPLES

EXAMPLE MESSAGE

```
Error: Required information sensitization master NOT found or incorrectly defined.
(CORRLIB-107)
```

CORRLIB-200 (warning) Warning message.

DESCRIPTION

This message occurs when .

WHAT NEXT

Please refer to .

EXAMPLES

EXAMPLE MESSAGE

Warning: Warning message. (CORRLIB-200)

CORRLIB-300 (information) Message.

DESCRIPTION

This message occurs when .

WHAT NEXT

Please refer to .

EXAMPLES

EXAMPLE MESSAGE

Information: Message. (CORRLIB-300)

CPFP-001 (information) Copied %d of total %d wire tracks from the source cell.

DESCRIPTION

This message occurs in the copy_floorplan command after wire trackes have been copied. It shows the statistics of the number of wire tracks copied and the total number of wire tracks in the source cell.

CPFP-002 (information) Copied %d of total %d wire tracks from the source cell.

DESCRIPTION

This message occurs in the copy_floorplan command after wire trackes have been copied. It shows the statistics of the number of wire tracks copied and the total number of wire tracks in the source cell.

CPFP-003 (information) Copied gcell grid attachment file %s to the destination cell.

DESCRIPTION

This message occurs in the copy_floorplan command after gcell grid attachment file been copied, showing the name of the file.

CPFP-004 (information) Created macro cell '%s' in the destination cell.

DESCRIPTION

This message occurs in the copy_floorplan command when the tool created a macro cell with the given name in the destination cell.

CPFP-005 (information) Created IO pad cell '%s' in the destination cell.

DESCRIPTION

This message occurs in the copy_floorplan command when the tool created a IO pad cell with the given name in the destination cell.

CPFP-006 (information) Created corner pad cell '%s' in the destination cell.

DESCRIPTION

This message occurs in the copy_floorplan command when the tool creates a corner pad cell with the given name in the destination cell.

CPFP-007 (information) Created filler cell '%s' in the destination cell.

DESCRIPTION

This message occurs in the copy_floorplan command when the tool creates a filler cell with the given name in the destination cell.

CPFP-008 (information) Created net %s in the destination cell.

DESCRIPTION

This message occurs in the copy_floorplan command when the tool creates a net with the given name in the destination cell. The net is created because it connects to one or more newly created physical cells.

CPFP-009 (information) Connected net %s to port %s of cell %s.

DESCRIPTION

This message occurs in the copy_floorplan command when the tool creates a net and

builds its connection in the destination cell.

CPFP-010 (information) Created %d macro, %d io pad, %d corner pad, %d flip chip pad, %d filler cells in the destination cell.

DESCRIPTION

This message occurs in the copy_floorplan command giving a statistics on the number of different types of physical cells created by the command in the destination cell.

CPFP-011 (information) Created %d new physical cells in the destination cell.

DESCRIPTION

This message occurs in the copy_floorplan command giving a statistics on the number of physical cells created by the command in the destination cell.

CPFP-012 (information) Copied the placement of %d of total %d cells from the source cell.

DESCRIPTION

This message occurs in the copy_floorplan command giving a statistics on the number of cells whose placement information are copied to the destination cell.

CPFP-013 (information) Copied the routing of %d of total %d nets from the source cell.

DESCRIPTION

This message occurs in the copy_floorplan command giving a statistics on the number of nets whose routing are copied to the destination cell.

CPFP-014 (information) Created port %s in the destination cell.

DESCRIPTION

This message occurs in the copy_floorplan command when the tool creates a top-level port with the given name in the destination cell.

CPFP-015 (information) Created pin %s in the destination cell.

DESCRIPTION

This message occurs in the copy_floorplan command when the tool creates a pin with the given name in the destination cell.

CPFP-016 (information) Copied %d of total %d pins from the source cell.

DESCRIPTION

This message occurs in the copy_floorplan command giving a statistics on the number of pins created or whose coordinates are copied in the destination cell.

CPFP-017 (information) Copied %d of total %d variable route rules from the source cell.

DESCRIPTION

This message occurs in the copy_floorplan command giving a statistics on the number of variable route rules copied to the destination cell.

CPFP-018 (information) Plan group %s exists in the destination cell, skipped.

DESCRIPTION

This message occurs in the copy_floorplan command when the plan group with a given name already exists in the destination cell before copying from the source cell.

Then the data of this plan group will not be updated.

CPFP-019 (information) Copied %d of total %d plan groups from the source cell.

DESCRIPTION

This message occurs in the copy_floorplan command giving a statistics on the number of plan groups copied to the destination cell.

CPFP-020 (warning) Cell instance %s not found in the source cell, skipped copying its power connection.

DESCRIPTION

This warning message occurs in the copy_floorplan command. The tool finds that a cell instance is missing in the destination cell when it is trying to copy power connections.

CPFP-021 (information) The source cell does not have gcell grid info attachment file.

DESCRIPTION

This message occurs in the copy_floorplan command. It indicates that there is no attachment file of gcell grid information in the source cell, so that no gcell grid information is copied.

CPFP-022 (error) Failed to create destination cell gcell grid info attachment file, skipped copying gcell grid definition.

DESCRIPTION

This message occurs in the copy_floorplan command when the tool failed to create the attachment file of the gcell grid information for the destination cell. Thus the gcell grid information is not correctly copied for the destination cell.

CPFP-023 (error) Cannot open destination cell gcell grid attach file.

DESCRIPTION

This message occurs in the copy_floorplan command when the tool failed to open the gcell grid attach file of the destination cell. The gcell grid information is not copied correctly.

CPFP-024 (error) Unable to create physical cell '%s' in the destination cell.

DESCRIPTION

This message occurs in the copy_floorplan command, when the tool failed to create a physical cell in the destination cell.

CPFP-025 (error) Cell %s not found in the destination cell, skipped.

DESCRIPTION

This message occurs in the copy_floorplan command, when the tool is trying to copy the coordinates of the given cell, but fails to find it in the destination cell.

CPFP-026 (error) Net %s not found in the destination cell, skipped.

DESCRIPTION

This message occurs in the copy_floorplan command, when the tool is trying to copy the wiring of the given net, but fails to find it in the destination cell.

CPFP-027 (warning) Port %s not found in the destination cell,

skipped copying its pins.

DESCRIPTION

This warning message occurs in the copy_floorplan command, when the tool is trying to copy the pins but cannot find their corresponding port in the destination cell.

CPFP-028 (warning) Cell instance %s connects to a non P/G net %s in the source cell, not creating it in the destination cell.

DESCRIPTION

This warning message occurs in the copy_floorplan command, when the tool skipped creating a missing physical cell instance in the destination cell because in the source cell, the cell instance connects to non-P/G nets.

CPFP-029 (warning) Cell inst %s not found in destination cell, not attached to power domain %s.

DESCRIPTION

This warning message occurs in the copy_floorplan command, when the tool cannot find a cell instance belonging to a power domain being copied in the destination cell and skipped attaching it to the power domain.

CPFP-031 (information) Copied %d of total %d move bounds from the source cell.

DESCRIPTION

This message occurs in the copy_floorplan command giving a statistics on the number of move bounds copied to the destination cell.

CPFP-032 (information) Group bound %s exists in the

destination cell, skipped.

DESCRIPTION

This message occurs in the copy_floorplan command when the group bound with the given name already exists in the destination cell before copying from the source cell. Then the data of this group bound will not be updated.

CPFP-033 (information) Copied %d of total %d group bounds from the source cell.

DESCRIPTION

This message occurs in the copy_floorplan command giving a statistics on the number of group bounds copied to the destination cell.

CPFP-034 (information) Copied %d of total %d voltage areas from the source cell.

DESCRIPTION

This message occurs in the copy_floorplan command giving a statistics on the number of voltage areas copied to the destination cell.

CPFP-035 (information) Copied %d via rules from the source cell.

DESCRIPTION

This message occurs in the copy_floorplan command giving a statistics on the number of via rules copied to the destination cell.

CPFP-036 (information) Copied %d of total %d power domains

from the source cell.

DESCRIPTION

This message occurs in the copy_floorplan command giving a statistics on the number of power domains copied to the destination cell.

CPFP-037 (information) Copied %d of total %d power ground net info from the source cell.

DESCRIPTION

This message occurs in the copy_floorplan command giving a statistics on the number of power ground net info copied to the destination cell.

CPFP-038 (information) Power ground net info %s exists in the destination cell, skipped.

DESCRIPTION

This message occurs in the copy_floorplan command when the power ground info with the given name already exists in the destination cell before copying from the source cell. Then the data of this power ground info will not be updated.

CPFP-039 (information) Created power net %s in the destination cell.

DESCRIPTION

This message occurs in the copy_floorplan command, when the tool copies a missing power net in the destination cell.

CPFP-040 (information) Created flip chip pad cell '%s' in the

destination cell.

DESCRIPTION

This message occurs in the copy_floorplan command when the tool created a flip chip pad cell with the given name in the destination cell.

CPFP-041 (information) Copied %d rectangles from the source cell.

DESCRIPTION

This message occurs in the copy_floorplan command giving a statistics on the number of rectangles copied to the destination cell.

CPFP-042 (information) Copied %d polygons from the source cell.

DESCRIPTION

This message occurs in the copy_floorplan command giving a statistics on the number of polygons copied to the destination cell.

CPSR-001 (warning) Total %d switches/filler cells/corner cells overlaps with existing cells or blockage.

DESCRIPTION

This warning message occurs when option "-check_overlap" is specified, the inserted switches/filler cells/corner cells overlaps with existing cells or blockage.

WHAT NEXT

The command doesn’t guarantee the inserted cells will not overlap with existing cells or blockage. If you don’t want that happen, please adjust cell’s position.

SEE ALSO

CPSR-002 (warning) Multiple %d voltage areas or macros found.

DESCRIPTION

This warning message occurs when multiple voltage areas or macros found based on the option "-area_obj" The command will pick up the first object that matches

WHAT NEXT

Check the option "-area_ob".

SEE ALSO

CPSR-003 (error)Can not find %s lib cell %s.

DESCRIPTION

This error message occurs when the lib cell can not be found. Please check the lib cell name.

WHAT NEXT

Please check the lib cell name.

SEE ALSO

CPSR-004 (error) Can not find cell %s's dimension.

DESCRIPTION

This error message occurs when we can not get cell's dimension. Either cell name is not correct or we cell's FRAM view can not be found.

WHAT NEXT

SEE ALSO

CPSR-005 (error) Switch cell, filler cell, corner cell's height don't match.

DESCRIPTION

This error message occurs when switch cell, filler cell and corner cell can not be found or their height don't match. We have the assumption that switch cell, filler cell and corner cell should have the same height and corner cell should be square. If cell's orientation is not like the same with standard, user should specifies such option: -switch_orientation, -filler_orientation, -outer_corner_orientation, -inner_corner_orientation.

WHAT NEXT

Please check whether cell name is correct and whether set the cell to a correct orientation.

SEE ALSO

CPSR-006 Offset number %d should match the area edge

number %d!

DESCRIPTION

This error message occurs when offset number doesn’t match the area edge number. If only one value is specified, the value is applied to all edges. To specify a different offset value for a different edge, a set of values can be specified. If more than one values are specified, they must match the number of edges of the voltage area or macro.

WHAT NEXT

Please check the offset number to match the area edge number.

SEE ALSO

CPSR-007 (error) Start_point or end_point in bad format.

DESCRIPTION

This error message occurs when start_point or end_point is in bad format. User should specifies the point like {x y}.

WHAT NEXT

Please check the start_point or end_point format.

SEE ALSO

CPSR-008 (error) Point %s is not on the object boundary.

DESCRIPTION

This error message occurs when the give start_point or end_point is not on the object boundary. If the option -offset is specified, the boundary is not the given voltage area or macro, it should also consider the offset.

WHAT NEXT

Please check the start_point or end_point

SEE ALSO

CPSR-009 (error) Density %f should be between the range (0.0 1.0].

DESCRIPTION

This error message occurs when user specifies a wrong density value. The density value should be between the range (0.0 1.0].

WHAT NEXT

Please check the -density option.

SEE ALSO

CPSR-010 (warning) Can not fill the gap with fillers from %s to %s.

DESCRIPTION

This warning message occurs when filler cells can not totally fill the gap between switch cells and corner cells.

WHAT NEXT

User should either connect the pin manually or choose different filler cells, start_point, end_point.

SEE ALSO

CPSR-011 (error) driver_point in bad format.

DESCRIPTION

This error message occurs when driver_point is in bad format. User should specifies the point like {x y}.

WHAT NEXT

Please check the driver_point format.

SEE ALSO

CPSR-012 (error) Start point and end point are not on the same polygon.

DESCRIPTION

This error message occurs when area_obj is a disjoint voltage area, but start point and end point are not on the same polygon.

WHAT NEXT

Start point and end point should be on the same polygon. When start point or end point is specified, power switches will only be inserted around that specified polygon even it is a disjoint voltage area.

SEE ALSO

CPSR-013 (error) Polygon format error.

DESCRIPTION

This error message occurs when a error polygon format is detected when parsing polygon coordinates.

WHAT NEXT

If -polygon option is used, please examine the input format. If it is a rectangle, you can input it as {llx lly urx ury }. Or you can input the coordinates of all the corners in the format of {{x1 y1} {x2 y2} {x3 y3}...}.

SEE ALSO

CPSR-014 (Warning) No filler lib cell specified, the ring will not

be adjusted.

DESCRIPTION

This error message occurs when both -filler_lib_cell and -seal_ring are specified. Since there are no filler cells to fill the gap, the ring will not be adjusted.

WHAT NEXT

SEE ALSO

CPSR-015 (ERROR) %s is a beta feature. If you want to test this beta feature, please request the beta license from SYNOPSYS.

DESCRIPTION

This error message occurs when this feature is a beta feature.

WHAT NEXT

SEE ALSO

CPSR-016 (Error) Pattern syntax error for -place_pattern option.

DESCRIPTION

This error message occurs when there is error for -place_pattern option. Please refer to above information.

WHAT NEXT

SEE ALSO

CPSR-017 (ERROR) Unexpected number %s after number %s.

DESCRIPTION

This error message occurs when there is error for -place_pattern option. There should not be two numbers adjacent with each other.

WHAT NEXT

Please check the pattern syntax.

SEE ALSO

create_power_switch_ring(2)

CPSR-018 (ERROR) Number is not allowed on the start of pattern.

DESCRIPTION

This error message occurs when there is error for -place_pattern option. Number is not allowed on the start of pattern, including nested pattern.

WHAT NEXT

Please check the pattern syntax.

SEE ALSO

create_power_switch_ring(2)

CPSR-019 (ERROR) Unexpected double number after %s. Is it

supposed to be an integer?

DESCRIPTION

This error message occurs when there is error for -place_pattern option. Double value is only allowed after "EMPTY" keyword.

WHAT NEXT

Please check the pattern syntax.

SEE ALSO

create_power_switch_ring(2)

CPSR-020 (ERROR) Expect double number after "EMPTY" keyword.

DESCRIPTION

This error message occurs when there is error for -place_pattern option. EMPTY keyword is different with other cell or nested pattern. Double value is expected after "EMPTY" keyword. The unit is micron.

WHAT NEXT

Please check the pattern syntax.

SEE ALSO

create_power_switch_ring(2)

CPSR-021 (ERROR) * symbol can not be in the nested pattern .

DESCRIPTION

This error message occurs when there is error for -place_pattern option. * symbol means to add this cell or pattern as many times as possible. It can not be put in the nested pattern. For example: Correct: {a b *} Wrong: {a {b *} 2}

WHAT NEXT

Please check the pattern syntax.

SEE ALSO

create_power_switch_ring(2)

CPSR-022 (ERROR) There should be no * symbol in the pattern if -density is specified..

DESCRIPTION

This error message occurs when there is error for -place_pattern option. * symbol means to add this cell or pattern as many times as possible. When -density is given, the pattern should have a fixed length, so * symbol is not allowed.

WHAT NEXT

Please check the pattern syntax.

SEE ALSO

create_power_switch_ring(2)

CPSR-023 (Warning) -continue_pattern is useless when both -place_pattern and -density is given.

DESCRIPTION

WHAT NEXT

SEE ALSO

create_power_switch_ring(2)

CPSR-024 (Warning) -continue_pattern should be used

together with -place_pattern option.

DESCRIPTION

This warning occurs when -continue_pattern is specified while no -place_pattern is specified. In this case, -continue_pattern is useless.

WHAT NEXT

SEE ALSO

create_power_switch_ring(2)

CPSR-025 (error) Illegal option value for %s. %s.

DESCRIPTION

This error message occurs when user specifies a wrong option value.

WHAT NEXT

Please check the option.

SEE ALSO

CTL-301 (warning) NameMaps inheritance not supported.

DESCRIPTION

This warning is generated when the user specifies an InheritNameMap statement in the NameMaps block. Currently the Namemaps inheritance is not supported in the NameMaps block.

WHAT NEXT

Find alternative way to reach the goal.

CTL-302 (warning) Specifying more than one TestMode in %s CTL block.

DESCRIPTION

This warning is generated when user specifies more than one TestMode in the TestMode statement in the CTL block mentioned. Currently we only recognize the first TestMode in the TestMode statement, while others will be discarded.

WHAT NEXT

Keep the TestMode desired and discard others.

CTL-303 (error) Core instance %s does not exist.

DESCRIPTION

This error is generated when an undefined CoreInstance was referenced somewhere. The CoreInstance must be defined before being used according STIL syntax.

WHAT NEXT

Define the CoreInstance before using it.

CTL-304 (error) PatternBurst %s does not exist.

DESCRIPTION

This error is generated when an undefined PatternBurst was used. It is required by the STIL syntax to define the PatternBurst before it is referenced.

WHAT NEXT

Define the PatternBurst before using it.

CTL-306 (error) %s Connection mismatch.

DESCRIPTION

This error is generated when there is a size mismatch related to the mentioned signal, core signal or scancell in the IsConnected block of CTL block.

WHAT NEXT

Find out the mismatched connection and fix it.

CTL-307 (error) Signal connection not allowed outside Internal block.

DESCRIPTION

This error is generated when user tried to define a Signal connection outside Internal block, e.g CoreInternal or ScanInternal block. CoreInternal block needs a CoreSignal connection; ScanInternal blocks needs a ScanCell connection.

WHAT NEXT

Define other types of connections in other blocks.

CTL-308 (error) Cannot find pattern matching name ’%s’ in

existing CTL model.

DESCRIPTION

This error is generated when user specifies a Pattern Name which is not defined previously in the PatternBurst or Pattern block. Usually, it happens in the PatternInformation block in CTL block.

WHAT NEXT

See if the Pattern name is correct or not.

CTL-309 (error) The patinfo for Pattern '%s' already existed.

DESCRIPTION

This error is generated when user tries to read in PatternInformation for the same Pattern more than once without specifying the overwrite value of the read option to truth.

WHAT NEXT

Specify the overwrite option to truth or change the Pattern name.

CTL-310 (error) CTL block %s redefined.

DESCRIPTION

This error is generated when the mentioned CTL block is defined more than once in the same Environment block. CTL block must be uniquely defined within an Environment block.

WHAT NEXT

Remove the duplicated definition of CTL block.

CTL-311 (warning) Both CTL block and TRC block are defined

in the %s Environment block.

DESCRIPTION

This warning is generated when both CTL block and TRC block are defined in the same Environment block. The latter one will be discarded. Currently we require that CTL block and TRC block to be defined in seperate Environment block.

WHAT NEXT

Define the CTL block and TRC block in seperate Environment block.

CTL-313 (error) Environment block %s redefined.

DESCRIPTION

This error is generated when the mentioned Environment block is defined more than once . Environment block must be uniquely defined according to STIL syntax.

WHAT NEXT

Remove the duplicated definition of Environment block.

CTL-314 (warning) Ignoring invalid characters from Mask field "%s

DESCRIPTION

This warning is generated when the Mask field contains invalid characters. The only valid characters for this field are ’0’ and ’1’. Any other characters will ignored and their value replaced with ’0’.

WHAT NEXT

Correct the value of the Mask field.

SEE ALSO

define_mbist_program (2)

CTL-315 (warning) Ignoring Test %s as Algorithm %s not found

DESCRIPTION

This warning is generated when the Algorithm specified in the Test statement is not found in the current CTL.

WHAT NEXT

Correct the value of the Algorithm field or declare the Algorithm used in the Test statement before its usage.

SEE ALSO

define_mbist_program (2)

CTL-316 (warning) Ignoring Background %s in Test %s as not found

DESCRIPTION

This warning is generated when the Background specified in the Test statement is not found in the current CTL.

WHAT NEXT

Correct the value of the Background field or declare the Background used in the Test statement before its usage.

SEE ALSO

define_mbist_program (2)

CTS

CTS-000 (Error) Pin forced as Sink can not be a root

DESCRIPTION

An attempt to set the root of the clock tree on the pin on which exception has already been preset.

WHAT NEXT

Make sure which purpose given pin should serve. Depending on that you should either remove exception from that pin or specify another pin as a root of the clock tree.

CTS-001 (Error) Could not find a clock tree by that name: %s

DESCRIPTION

The clock tree name passed through option -clock_tree_name is not defined. This command needs a defined clock tree name as argument.

WHAT NEXT

Check the name for mistype or use ’set_clock_tree_options’ to create the clock tree definition.

CTS-002 (Error) Unable to setup data base driver

DESCRIPTION

WHAT NEXT

CTS-003 (Error) Unable to setup timing engine driver

DESCRIPTION

WHAT NEXT

CTS-004 (Error) Unable to setup routing engine driver

DESCRIPTION

WHAT NEXT

CTS-005 (Error) Unable to link node to external DB

DESCRIPTION

WHAT NEXT

CTS-006 (Warning) Pin %s is driven by pin %s in the netlist - overriding using driving cell constraint on root pin.

DESCRIPTION

The hierarchical port specified as the root of the clock tree has a driver inside the netlist. Since a driving cell timing assertion is available on the root pin, the 'set_clock_tree_options' command will use it instead of the real netlist driver.

WHAT NEXT

If you do not want to retain this override, reset the driving cell timing assertion on the root port.

CTS-007 (Information) Driving cell %s (%s to %s) will be applied to the root pin.

DESCRIPTION

The root pin of the clock tree is a hierarchical pin. Its driver was specified using the **set_driving_cell** command.

WHAT NEXT

Use **set_driving_cell** if you want to specify another driver.

CTS-008 (Error) Could not find layer information for pin %s - clock tree definition aborted.

DESCRIPTION

The 'set_clock_tree_options' command is trying to determine the technology layer assigned to this pin, but no information on the physical terminal was found.

WHAT NEXT

Run 'assign_pins' in each of the clock tree hierarchies and make sure a layer is assigned to all the clock tree ports and pins.

CTS-009 (Error) hierarchy of pin '/%s' at {%ld %ld} does not match the hierarchy at that location ('/%s').

DESCRIPTION

This indicates serious inconsistencies between the clock tree description and the design hierarchy. It could also be caused by a failure to find a valid legal location for one of the clock tree cell while doing synthesis, or by incorrect floorplan data. The update phase of 'compile_clock_tree' command will create ports as needed to establish the connection, but the physical location of those ports may

be outside or not near the boundary of some of the crossed hierarchy boundaries.

WHAT NEXT

Check the floorplan and redo CTS. Check that some valid locations can be found for clock tree buffers. You can also try to manually fix the problem by moving the incorrect ports and clock tree cells by hand, then update the clock tree using 'report_clock_tree'.

CTS-010 (Error) Could not find a valid placement for clock tree buffer at { %ld %ld }: this buffer will not have a legal placement.

DESCRIPTION

This error probably indicates a serious floorplan or library issue that prevents the CTS tool from finding legal placement sites for the synthesized clock tree buffers.

WHAT NEXT

Check the floorplan around the specified location.

CTS-011 (Error) Inconsistent connectivity for cell %s - buffer removal on clock domain %s aborted

DESCRIPTION

This error is raised in two cases: 1) the current clock description contains multiply instantiated buffers (i.e. the clock domain touches some non-uniquified parts of the netlist); or 2) the database is corrupted and there are serious inconsistencies between the clock domain internal description and the netlist (for instance the logical description of the cell matched with a buffer, but the cell has more that 2 connections).

WHAT NEXT

Check that all the hierarchies covered by the clock network are uniquified.

CTS-012 (Information) removing buffer or inverter: %s in cell %s

in clock tree %s

DESCRIPTION

The cell is a buffer or inverter of the specified clock tree. This cell is being removed because you perform 'remove_clock_tree_buffering' on this clock tree. Buffer and inverter are removed only if 'remove_clock_tree_buffering' can do so without changing the logic of the clock signal.

WHAT NEXT

CTS-013 (Error) could not update the definition of clock domain %s

DESCRIPTION

The connectivity of the clock network has not been preserved during buffer removal. A serious error or database corruption has occurred.

WHAT NEXT

Please contact your support.

CTS-014 (Warning) Could not find a valid timing arc matching %s to drive the specified root.

DESCRIPTION

You have passed a hierarchical port as the root of the clock tree to the **set_clock_tree_options** command, and you specified a driver timing arc using the *-timing_arc* option, but **set_clock_tree_options** cannot find a library timing arc that matches your search criteria. The command will attempt to find a driver timing arc for you using the netlist information or driving cell port constraints defined using the **set_driving_cell** command.

WHAT NEXT

Check the pin argument passed to the *-timing_arc* option is really connected to the specified root port. Check your *link_path* and *search_path* variables. Check for disabled timing arcs using **report_disable_timing**. Use **remove_disable_timing** to fix the problem.

CTS-015 (Error) Logic loop in clock network at output pin %s

DESCRIPTION

The netlist starting at the specified root traces through looping logic.

WHAT NEXT

Use the ’set_clock_tree_stop_pin’ or ’set_clock_tree_exclude_pin’ command to prevent reconvergence in the clock network.

CTS-016 (Error) Multiple driver on the clock network detected while tracing pin %s of cell %s

DESCRIPTION

WHAT NEXT

CTS-017 (Error) Multiple driver on the clock network detected while tracing pin %s of top level cell %s

DESCRIPTION

WHAT NEXT

CTS-018 (Error) Can not determine unique outputPin use -timing_arc

DESCRIPTION

WHAT NEXT

CTS-019 (Warning) Instance %s in design %s can be traced to

more than one output. Selecting pin %s to trace through the cell.

DESCRIPTION

Your netlist contains a gating cell along the current clock tree which contains several output pins to which the cell can be traced through. The clock tree tracing algorithm has selected the random pin reported in the message to trace through this gate.

WHAT NEXT

If the instance reported is not really part of the clock tree you want to buffer, use **set_clock_tree_exceptions** to prevent this cell to be traced through. If you want to select another pin to trace through the cell, disable all the timing arcs but the one you want to use to cross this cell using **set_disable_timing**.

CTS-020 (Warning) Non Unate cell: %s (%s) in design %s - assuming %s-unate timing arc.

DESCRIPTION

The root cell or one of the gating cells of the current clock domain is traced through using a non-unate timing arc. This is a problem as the timing analysis will not be able to assert the polarity of the clock signal behind that cell, nor balance delays and optimize skew accordingly. The polarity of the timing arc will be considered non-inverting, to allow clock tree synthesis to carry on, but the insertion delay and skew optimization will be performed considering a clock edge that may not correspond to a real functional mode of the circuit.

WHAT NEXT

Please use **set_disable_timing** to resolve the polarity of this timing arc.

CTS-021 (Error) Illegal clock tree node

DESCRIPTION

This means that clock tree data has likely been corrupted.

WHAT NEXT

Try to reccreate clock tree data by issuing set_clock_tree_options command

CTS-022 (Error) Invalid clock tree node type

DESCRIPTION

WHAT NEXT

CTS-023 (Error) Timer not initialized

DESCRIPTION

WHAT NEXT

CTS-024 (Error) Invalid clock tree node status

DESCRIPTION

WHAT NEXT

CTS-025 (Error) Can not trace through multiple (%d) occurences of pin %s

DESCRIPTION

```
Can not trace through multiple (%d) occurences of a pin %s . Design must be
uniquified or pin s property set to FLOAT.
```

WHAT NEXT

CTS-026 (Information) Emptying nets for Preserved

connections...

DESCRIPTION

WHAT NEXT

CTS-027 (Information) Cleaned %d preserved connections

DESCRIPTION

WHAT NEXT

CTS-028 (Information) Purging clock nets from deleted connections...

DESCRIPTION

Informs the user that clock tree synthesis is in the phase of removing obsolete nets.

WHAT NEXT

Just wait a little bit

CTS-029 (Information) Cleaned %d broken connections...

DESCRIPTION

WHAT NEXT

CTS-030 (Error) pin %s does not have a layer

DESCRIPTION

WHAT NEXT

CTS-031 (Error) Could not initialize layer information for clock %s

DESCRIPTION

WHAT NEXT

CTS-032 (Error) there is no clock tree object named %s in the database

DESCRIPTION

You receive this message because the specified clock tree name is not in the database. When the specified clock tree name is not present in the database, you must define a clock tree object by using the **set_clock_tree_options** command with the **-root** option. CTS-032 might be raised when you are attempting to define a clock tree and define an illegal clock tree root. In this case, CTC first issues a message saying the clock tree root pin was not found or is illegal, and then you might receive this error message because CTC could not find or create the clock tree and, therefore, it is not in the database.

WHAT NEXT

Provide the **-root** option the first time you define a clock tree object by using the **set_clock_tree_options** command.

SEE ALSO

set_clock_tree_options(2).

CTS-033 (Error) Can not remove port %s of instance %s from

net %s in cell %s

DESCRIPTION

WHAT NEXT

CTS-034 (Error) can not remove port %s from net %s in cell %s

DESCRIPTION

WHAT NEXT

CTS-035 (Error) Can not remove net %s in cell %s

DESCRIPTION

WHAT NEXT

CTS-036 (Information) Deleted net %s in cell %s

DESCRIPTION

WHAT NEXT

CTS-037 (Information) Inserting new buffer cells...

DESCRIPTION

WHAT NEXT

CTS-038 (Information) Added %d buffers

DESCRIPTION

WHAT NEXT

CTS-039 (Information) Updating connections...

DESCRIPTION

WHAT NEXT

CTS-040 (Warning) No %s for library pin %s/%s - resetting to default (%s)

DESCRIPTION

Some gating cells or buffer cells in the logical library files (.db files) you provided do not have valid values for the following parameters needed by clock tree synthesis: input pin capacitance, output pin max_capacitance, output pin max_transition, output pin max_fanout.

WHAT NEXT

Make sure the '.db' library files for your libraries provide accurate values for input pin capacitance and other library cells parameters. If the library contains invalid (<=0) values, they will be reset to a default value as specified in the error message.

CTS-041 (Information) Updated %d new connection

DESCRIPTION

WHAT NEXT

CTS-042 (Information) Updating global routing of preserved

connections...

DESCRIPTION

WHAT NEXT

CTS-043 (Information) Updated %d preserved connection

DESCRIPTION

WHAT NEXT

CTS-044 (Error) layer %s is not a routing layer

DESCRIPTION

You have passed a layer name to the '-layer_list' option of 'set_clock_tree_options' that is not a routing layer name

WHAT NEXT

If it is a typo error, please correct. Otherwise refer to the documentation to define this layer as a routing layer.

CTS-045 (Warning) could not find pin %s on cell %s

DESCRIPTION

You have specified a pin name using the *-timing_arc* option of **set_clock_tree_options** or the *-input* or *-output* option **set_clock_tree_references** which does not exist on the specified reference.

WHAT NEXT

Those commands will attempt to find a valid pin name for you for which timing information is available in the library, but you need to provide the correct pin name if the choice is not the one you expected.

CTS-046 (Warning) Selected timing arc of cell %s (%s to %s) is not unate! Clock tree synthesis will consider it unate with a %s polarity.

DESCRIPTION

The timing arc specified to the **set_clock_tree_options**, **set_clock_tree_references** command is not unate. Those commands will choose a default unateness for you based on the timing arcs available in the library. If both inverting and non-inverting timing arcs are available, the non-inverting timing arc will be chosen.

WHAT NEXT

If you do not want the chosen timing arc polarity, use **set_case_analysis** to invalidate the unwanted timing arc on the instance. You cannot use this method if the message was raised with the **set_clock_tree_references** commands, because there is no cell which the **set_case_analysis** command could be applied to.

CTS-047 (Warning) No valid timing arc found for specified pin %s in cell %s - selected timing arc is %s to %s

DESCRIPTION

A timing arc pin was specified using option *-timing_arc* of the **set_clock_tree_options** command, or option *-input* or *-output* of the **set_clock_tree_references** commands, but no valid timing arc was found using the specified port in the timing library. The command selected another valid timing arc for you.

WHAT NEXT

Check the port name that you specified. Check the data in the timing library.

CTS-048 (Warning) Could not find a%s timing arc for cell %s - will use cell as %s.

DESCRIPTION

Tool cannot find a timing arc of a proper polarity in the library for the specified reference.

WHAT NEXT

Use another cell or check library data.

CTS-049 (Error) Could not find a valid library timing arc to drive clock domain root pin: %s. Clock domain definition aborted.

DESCRIPTION

Either timing information cannot be accessed or the timing arc to or from the specified root pin are disabled.

WHAT NEXT

Check your 'link_path' and 'search_path' variables. Check for disabled timing arcs using 'report_disable_timing'. Use 'remove_disable_timing' to fix the problem. If the root of the clock tree is a top-level port, it is possible that no driving timing arc can be derived if no buffer is defined for the current clock tree (or if only inverters are defined), and no valid library cells with a buffer function can be found in the library (for instance because all the buffer library cells are set as dont_touch or dont_use cells). In this case, the easiest way out is to define a driving cell for the clock port using the **set_driving_cell** command. Another way is to remove dont_touch and dont_use attributes on some buffer library cells, and rerun **set_clock_tree_options**.

CTS-050 (error) Clock tree update failed for clock %s

DESCRIPTION

This error occurs because the update phase of the **compile_clock_tree** command is not able to modify the database according to the result of a clock tree synthesis run. Possible causes are the following: the specified clock tree has not been compiled, some library information is missing, or serious inconsistencies between the compiled clock tree database and the tool's database prevent the update from running successfully.

WHAT NEXT

Ensure that a **compile_clock_tree** command has run successfully. Ensure that logical libraries are available. Remove and redefine the clock tree, and recompile it.

CTS-051 (Error) no compiled database available for clock tree

%s - please run ’compile_clock_tree’ before updating

DESCRIPTION

You want to run ’compile_clock_tree’ but there is currently no compiled in-memory database for the clock tree that you specified.

WHAT NEXT

Make sure that ’compile_clock_tree’ has run successfully. Use ’report_clock_tree’ after running ’compile_clock_tree’ to retreive information about the compiled clock tree structure and performances.

CTS-052 (Error) cell %s is not legally placed

DESCRIPTION

You want to run ’compile_clock_tree’ or ’report_clock_tree’ but some hierarchies covered by the current clock tree are not legally placed. Timing cannot be estimated and clock cannot be synthesized if some hierarchies are not legally placed.

WHAT NEXT

Make sure that placement has been legalized at least in all the hierarchies covered by this clock tree.

CTS-053 (Information) Removing buffers and inverter pairs in clock tree %s: %s ...

DESCRIPTION

The ’remove_clock_tree_buffering’ performs buffer removal in two passes.

WHAT NEXT

CTS-054 (Error) An error occured while setting up the routing

engine driver

DESCRIPTION

WHAT NEXT

CTS-055 (Error) An error occured while setting up the placement legalization engine driver

DESCRIPTION

WHAT NEXT

CTS-056 (error) Could not refresh placement information for clock %s

DESCRIPTION

This error occurs because the **compile_clock_tree** or **report_clock_tree** command attempted to update the clock tree synthesis internal data structure according to the current placement of the clock tree cells, but failed to do so. Possible causes are: some of the clock tree's instances or hierarchical blocks are not legally placed. The placement information must be available prior to running the clock tree synthesis tool.

WHAT NEXT

Run legalize_placement in all hierarchies touched by the clock tree.

CTS-057 (Error) Could not build blockage map for clock %s

DESCRIPTION

The 'compile_clock_tree' command failed to initialize the blockage information needed by the CTS routing engine.

WHAT NEXT

Contact your support.

CTS-058 (Error) Could not initialize buffer property tables for clock tree %s

DESCRIPTION

This indicates one of three error conditions: - absent or incorrect buffer cell defined for the clock tree - pin name mismatch between logical and physical library - logic libraries unavailable

WHAT NEXT

Check the library search path. Make sure at least one buffer cell was defined using 'set_clock_tree_references' for the current clock tree. Check the consistency of physical and logical libraries.

CTS-059 (Error) Clock tree synthesis failed for clock %s

DESCRIPTION

The 'compile_clock_tree' command was not able to produce a valid buffer tree for one of the subtrees of the current clock tree. This usually happens when some clock pins is so isolated that no clustering can be made without violating the buffer design rules even using low fanouts.

WHAT NEXT

Use a different buffer with higher drive strength. Override the max_capacitance constraint of the chosen buffer cell by using 'set_clock_tree_references' with the '-max_load' option. Manually insert buffers in front of those pathological clock pins and try to find a location for that buffer as close as possible to other sinks of the same subtree.

CTS-060 (Error) Could not build placement blockage map for

clock tree %s

DESCRIPTION

The ’compile_clock_tree’ command failed to initialize the blockage information needed by the CTS routing engine.

WHAT NEXT

Contact your support.

CTS-061 (Warning) Clock tree constraint modified for trees %s - Please update clock tree definition using ’set_clock_tree_options -initialize’.

DESCRIPTION

You have used one of the commands that modify the clock tree tracing constraints, but the corresponding clock tree has already been defined. This command has modified the clock tree tracing properties on the specified object, but the clock tree definition has not been updated to reflect this change.

WHAT NEXT

You need to perform ’set_clock_tree_options’ using the ’-intialize’ option in order to reflect these changes in the CTS database of this clock tree.

CTS-062 (Error) Could not find a valid buffering solution for the current set of %s sinks

DESCRIPTION

The current set of sinks cannot be buffered without violating the driving cell and/or buffer design rules. This usually happens when the sinks are too scattered to produce clusters that the chosen buffers or gating cell can drive.

WHAT NEXT

CTS-063 (Information) Initializing placement blockage maps...

DESCRIPTION

WHAT NEXT

CTS-064 (Warning) No gating cell or sink pin can be traced to from pin %s: pin %s will be considered a sink of the clock domain.

DESCRIPTION

The reported gating cell pin does not have any fanout in the current netlist. The input pin that correspond to this gating cell or this hierarchical pin will be forced as a sink of the current clock domain.

WHAT NEXT

CTS-065 (Warning) Could not trace to any sink pin from specified root: %s.

DESCRIPTION

In the current netlist, the specified clock root instance output is not connected to any sink or gating cell pin. Please check your netlist.

WHAT NEXT

CTS-066 (Information) Legalizing buffer positions

DESCRIPTION

WHAT NEXT

CTS-067 (Information) Searching optimized buffering scheme for subtree rooted at %s (%d sinks)...

DESCRIPTION

WHAT NEXT

CTS-068 (Information) searching buffering scheme for excluded pins of subtree rooted at %s (%d excluded pins)...

DESCRIPTION

WHAT NEXT

CTS-069 (Error) Initializing routing blockage maps...

DESCRIPTION

```
Information message. The CTS needs information about routing blockages because it
needs to know how to route the synthesized clock nets.
```

WHAT NEXT

CTS-070 (Information) compiling buffer trees for clock domain

%s...

DESCRIPTION

Information message.

WHAT NEXT

CTS-071 (Information) final routing and timing clock tree graph...

DESCRIPTION

Information message. The routing and timing information in the CTS database is being updated according yo the results of placement legalization.

WHAT NEXT

CTS-072 (Information) buffering subtree rooted at %s (%d sinks) using user-defined buffer structure...

DESCRIPTION

Information message.

WHAT NEXT

CTS-073 (Information) Cleaning blockage maps...

DESCRIPTION

Information message. This is the last step of the 'compile_clock_tree' command.

WHAT NEXT

CTS-074 (Error) No buffer defined for clock tree %s

DESCRIPTION

CTS cannot be performed until a set of references are marked as available for the compilation of a given clock tree using the 'set_clock_tree_references' command.

WHAT NEXT

Use the 'set_clock_tree_references' command to define some buffers or inverters for this clock tree.

CTS-075 (Error) Could not find %s pin %s on cell %s

DESCRIPTION

This error is caused by an inconsistency between the physical and logical libraries. For instance when the timing model of the cell is missing or the pin names in the physical library do not match the pin names in the logical library.

WHAT NEXT

Check the cell and pin names for mistype. Make sure that the correct logical and physical libraries are used. Check the library search paths.

CTS-076 (Error) Loop clock logic detected at pin %s - no clock tree will be created.

DESCRIPTION

Looping logic path inside clock networks are not supported. A looping logic path was detected in the fanout of the clock network for which you attempt to define a clock tree. The 'set_clock_tree_options' command will continue the tracing of the current clock tree netlist in order to detect all loops in the clock network, but will not create a clock tree object.

WHAT NEXT

Please define stop pins, excluded pins or floatpins as needed to define cut points

in the clock network in order to exclude looping logic.

CTS-077 (Warning) Instance %s does not have any output pin that can be timed from pin %s and drives a non-empty fanout. Cannot trace through cell.

DESCRIPTION

Your clock network contains a combinatorial cell that does not have any output, lacks timing information or does not drive any pins. The 'set_clock_tree_options' command tries to make a gating cell out of the instance, but finds no timing arc to trace to valid output.

WHAT NEXT

The pin reported in the message is going to be forced as a sink of the current clock tree. If you want to change this, you have to make sure this cell has one output pin that drives some fanout and has suitable timing information. If you do not want to balance clock delays to this pin, use the **set_clock_tree_exceptions** command to exclude it from the delay balancing, and skew report.

CTS-078 (Error) capacitive load of %s%s pin is %.3f, while the best buffer can drive only %.3f

DESCRIPTION

Clock tree cannot be compiled because the fanout associated with one of the pins is too large to be driven by any of the buffers available from design library specified.

WHAT NEXT

Use a different buffer with higher drive strength. If this is a capacitance associated with a floatpin, then appearance of this error could mean that the capacitance value of the floatpin, specified in 'set_clock_tree_exceptions' command, is unrealistic.

CTS-079 (Warning) Delay calculation failed. Estimating delays

for the instance %s of cell %s.

DESCRIPTION

The delay calculation using Primetime timing engine did not succeed The delays are being estimated.

WHAT NEXT

The delay values may not be as accurate.

CTS-080 (Error) Could not find a logic library pin %s on cell %s.

DESCRIPTION

Inconsistent or missing logic library data.

WHAT NEXT

Check your logic library search path and the accessibility of the logic library files.

CTS-081 (Error) Timing engine failed to time timing arc between pins %s and %s for cell %s.

DESCRIPTION

Timing environment was not properly initialized prior to CTS.

WHAT NEXT

Check your timing library search path. Check the accessibility of the timing library data.

CTS-082 (Error) Unable to find a buffering solution satisfying

design rules

DESCRIPTION

Unable to find a buffering solution which will conform to all the design rules using the buffer/inverter specifed.

WHAT NEXT

Choose a buffer with a higher capacity

CTS-083 (Warning) The cell %s specified as reference does not exist in any library

DESCRIPTION

The cell specified as reference does not exist in the given libraries

WHAT NEXT

Either choose a cell which exists in the libraries or add the library which contains this cell.

CTS-084 (Error) The reference name has not been specified

DESCRIPTION

The reference name has not been specified

WHAT NEXT

Please specify a valid cell name as argument to -reference

CTS-085 (Error) Root pin of the clock tree (%s) actually drives nothing

DESCRIPTION

The external net is missing for the output pin of the clock tree (%s). This error

might be caused by either error in design file, or when PrimeTime removed several timing arcs, which also indicates potential problems with design.

WHAT NEXT

Check specified clock root and make sure it drives the clock net. Analyse the PrimeTime warning messages.

CTS-086 (Error) Pin %s is not connected - clock tree definition aborted.

DESCRIPTION

The pin specified as the clock root does not have any nets within the block. The clock pin must be connected inside for Clock tree synthesis to proceed correctly.

WHAT NEXT

Specify a clock pin which does have a internal net

CTS-087 (Warning) max_transition constraint for library pin %s/%s (%f) is not compatible with the selected max_capacitance for that cell (%f) - resetting to %f.

DESCRIPTION

Loading this pin with the selected max_capacitance leads to situations where the current max_transition constraint for that pin is violated. A new value for the max_transition constraint of that library pin will be computed to be used within CTS, so that the whole range of allowable load capacitances can be used without violating its max_transition constraint.

WHAT NEXT

Make sure that your library defines compatible values for the max_transition and max_capacitance of library cell pins.

CTS-088 (Warning) CTS and HFCTS cannot be performed

simultaneously.

DESCRIPTION

The option -high_fanout_net in compile_clock_tree tells the tool to perform HFCTS which is a high fanout net synthesis for signal nets using clock tree synthesis (CTS) techniques. When the both options -clock_trees and -high_fanout_net are given in compile_clock_tree, you are asking the tool to perform CTS on clock nets and HFCTS on signal nets simultaneously. Current version of compile_clock_tree doesn't support such kind of synthesis.

WHAT NEXT

Please specify either -clock_trees or -high_fanout_net option in compile_clock_tree command.

CTS-089 (Error) could not create db object for clock-tree domain %s - aborting.

DESCRIPTION

WHAT NEXT

Contact your application support.

CTS-090 (Error) could not match a db pin for %s - aborting.

DESCRIPTION

WHAT NEXT

Check the pin name passed to '-root '-timing_arc' option of 'set_clock_tree_options

CTS-091 (Error) Could not backannotate pin-to-pin delay

between %s and %s

DESCRIPTION

WHAT NEXT

CTS-092 (Error) Could not run dplacer after finishing clock tree synthesis

DESCRIPTION

The run of dplacer has finished abnormally after compilation of buffered clock tree

WHAT NEXT

CTS-093 (Warning) Port %s has back-annotated fanout number and/or wire-load model. CTS will assume an external load of %f capacitance units for that port.

DESCRIPTION

CTS currently does not support the computing of external port load based on wire-load models and the fanout number. Only capacitance values annotated on the port using the **set_load** command will be taken into account.

WHAT NEXT

Use the **set_load** command to annotate the desired external load on the specified clock port. Remove the annotated fanout number on the port using **remove_attribute**. Make sure that annotated capacitance not only does not violate max_cap DRC constraint but also leaves enough margin for CTC to meet this constraint for the net driven by the clock tree root port.

CTS-094 (Information) Running legalizer ...

DESCRIPTION

Legalizer is running after compilation of buffered clock tree.

WHAT NEXT

CTS-095 (Error) Could not provide a report for the clock %s

DESCRIPTION

'report_clock_tree' command failed to provide a report of the clock tree

WHAT NEXT

CTS-096 (Information) Checking the legality of placement...

DESCRIPTION

Checking the legality of placement after lagalizing the placement.

WHAT NEXT

CTS-097 (Error) Design is not flattened.

DESCRIPTION

Commands related to clock tree synthesis can only be run on flat designs in this release.

WHAT NEXT

Flatten the design by using the command "ungroup -flatten -all".

SEE ALSO

ungroup(2)

CTS-098 (Information) Removing clock latency on %s %s ...

DESCRIPTION

You receive this information message because the synthesized clock is set to be propagated, and clock latency, which is the attribute of an ideal clock, is removed.

WHAT NEXT

This is an informational message only. No action is required on your part.

CTS-099 (Warning) CTS will use a library cell %s, which has dont_touch or dont_use attribute.

DESCRIPTION

Library cell with a dont_use or dont_touch attribute is being specified as a clock tree reference.

WHAT NEXT

If you are positive this library cell is a right choice for CTS, you can ignore this message. Otherwise, please remove this library cell from clock tree reference list.

CTS-100 (Error) No exception type has been specified for %s.

DESCRIPTION

set_clock_tree_exceptions and remove_clock_tree_exceptions commands need at least one exception to be specified.

WHAT NEXT

Specify list of stop pins and/or list of exclude pins and/or list of float pins.

CTS-101 (warning) Incomplete float pin definition. Using default

values to fill in missing parameters.

DESCRIPTION

This warning message occurs because the **set_clock_tree_exceptions** command requires a list of input pins, the appropriate values of **-float_pin_min_delay_rise**, **-float_pin_max_delay_rise** (and/or **-float_pin_min_delay_fall**, **-float_pin_max_delay_fall**), This warning indicates that maximum/minimum delay is not specified and its value is copied from the specified minimum/maximum delay with the same edge type.

WHAT NEXT

This is only a warning message. If the results are not what you intended, check that the float pin definitions meet your expectations.

SEE ALSO

set_clock_tree_exceptions(2)

CTS-102 (Information) Removing clock uncertainty on %s %s ...

DESCRIPTION

You receive this information message because the synthesized clock is set to be propagated, and clock uncertainty, which is the attribute of an ideal clock, is removed.

WHAT NEXT

This is an informational message only. No action is required on your part.

CTS-103 (Information) Removing clock transition on %s %s ...

DESCRIPTION

You receive this information message because the synthesized clock is set to be propagated, and clock transition, which is the attribute of an ideal clock, is removed.

WHAT NEXT

This is an informational message only. No action is required on your part.

CTS-104 (Error) Incorrect float pin definition

DESCRIPTION

Float pin definition has been provided for set_clock_tree_exceptions command without specifying a list of float pins to which this definition should be applied, or without specifying any delay value for float pin, or with specifying min_delay(rise/fall) value larger than max_delay(rise/fall) value.

WHAT NEXT

Make sure to specify a list of input pins to be treated as float pins. Make sure that at least one of max_delay_rise, min_delay_rise, max_delay_fall and min_delay_fall values should be specified. Make sure that max_delay >= min_delay if delay values for rise/fall are specified.

SEE ALSO

set_clock_tree_exceptions(2)

CTS-105 (warning) Cannot route high fanout net

DESCRIPTION

This warning occurs because noback-annotation is accepted from the core clock tree synthesis algorithm When this occurs the tool applies its internal global router to route new nets that have appeared in the netlist as a result of clock tree synthesis. This message indicates that the net driven by the clock tree root (in the case when it is a port of the top level design), is a high-fanout net. Thus, the internal router cannot route it, and no back-annotation is applied. High-fanout nets receive special treatment during timing analysis. This might cause unreasonable delay estimations.

WHAT NEXT

You can apply the **set_port_fanout_number** command to set reasonable value (for example: 1) of fanout on the clock port used as the root of a clock tree. Then, recompile your clock tree.

CTS-106 (Warning) Clock root drives unreasonably high load

DESCRIPTION

Total load of a root pin of a clock tree does not meet design constraints. This is

likely caused by the fact that the clock net has received special treatment on ealier stages of design flow. report_clock_tree command will straightforwardly apply this unreasonable load while estimating path delays.

WHAT NEXT

If there is no intention to use this load on synthisized clock tree, make sure to remove 'load' and 'wire_capacitance' attributes on the clock root pin. Rerun report_clock_tree. Otherwise, accept the result of report_clock_tree command as is.

CTS-107 (Error) Cannot use library cell %s for CTS buffering as cell is not in the physical library.

DESCRIPTION

Library cells without physical description cannot be used by synthesis and CTS.

WHAT NEXT

Update the physical library or specify another library cell.

CTS-108 (Warning) No timing arc available to cross cell %s (%s) from pin % to pin %s in design %s - forcing cell as sink.

DESCRIPTION

One of the combinatorial cells in the transitive fanout of the current clock root does not have a valid timing arc that can be traced through. The input of that cell will be considered a sink of the clock-tree for the purpose of CTS and the potential clock-sinks that it drives will not be considered.

WHAT NEXT

Check disabled timing arcs on this cell using **report_disable_timing**. Check if the cell has timing information using **report_cell**.

CTS-109 (Warning) Cannot resolve timing arc %s -> %s in cell

%s (%s) to a unate timing arc - forcing cell as sink.

DESCRIPTION

One of the combinatorial cells in the transitive fanout of the current clock root does not have a timing arc that can be forced to a unate arc type. The input of that cell will be considered a sink of the clock-tree for the purpose of CTS and the potential clock-sinks that it drives will not be considered.

WHAT NEXT

Check disabled timing arcs on this cell using **report_disable_timing**. Check if the cell has timing information using **report_cell**. Check the function implemented by that cell: if all the possible transitions through that cell are not a superset of the two possible unate transition sets, then this cell cannot be considered as a gating element for the clock signal because it actually changes the waveform of the resulting signal.

CTS-110 (Warning) Specified -clock_trees did not match any clock tree, or no clock tree defined under current design. Ignoring reference list specification.

DESCRIPTION

You receive this message because there is no clock tree matching the specified criteria to which the command that generated the warning message can be applied. If no **-clock_trees** option is specified, the command defines the default buffer/inverter reference list for every clock tree in the design, regardless of whether some clock tree objects already exist at the time the command is issued. If no the **-clock_trees** option is present on the command line with a valid argument, then the error is raised in the case where the argument does not match a currently-existing clock tree object.

WHAT NEXT

No action is required on your part. However, you can ensure that you are in the right design by using the **current_design** command. Use the **set_clock_tree_options** to create an initial clock tree object in your database. If you want to apply current reference list to all the clock trees in the design, do not use *-clock_trees* option at all. Using the **set_clock_tree_references** command may produce this message.

SEE ALSO

current_design (2), **set_clock_tree_options** (2), **set_clock_tree_references** (2). options (2), **set_clock_tree_references** (2).

CTS-111 (Warning) Incorrect range specification %s - ignored.

DESCRIPTION

Refer to the **get_clock_tree_object** man page for a description of the *-levels* option syntax.

WHAT NEXT

Check the option syntax.

CTS-112 (Information) Moved %d preexisting cells in the clock tree.

DESCRIPTION

Clock Tree Synthesis has moved some clock tree cells to get the better delay and skew.

WHAT NEXT

CTS-113 (Information) Estimating the loads and delays on the nets...

DESCRIPTION

Legalizer might move some cells to avoid the overlaps between the clock buffers and existing cells. The estimated delays and loads might not remain accurate. It is estimating the delays and loads on the nets.

WHAT NEXT

CTS-114 (Information) Estimating the loads and delays on the nets terminated abnormally.

DESCRIPTION

Estimating the loads and delays on the nets was not successful.

WHAT NEXT

CTS-115 (Error) Hierarchical pin %s found in clock domain %s.

DESCRIPTION

When a clock is defined on a hierarchical pin, the hierarchical pin will show up on the timing graph. Since hierarchical pins do not have physical location, timing information cannot be calculated correctly for CTS and CTS will skip the clock domains that contain such hierarchical pins.

If a timing constraint or exception is defined on a hierarchical pin, the hierarchical pin will also show up on the timing graph and cause CTS to skip the clock domain that contains the pin. This is often due to improper use of wild-card in SDC statements that put timing constraints/exceptions on clock networks.

WHAT NEXT

Dump out SDC, then search and remove clock definitions and timing constraints/ exceptions on the hierarchical pin.

CTS-116 (Error) Cannot use library cell %s for CTS buffering as this library cell does not have exactly one input and one output pin.

DESCRIPTION

Library cells which have more than one input or output pins, or any bidirectional pins, cannot be used for CTS buffering.

WHAT NEXT

Please specify the library cell which has only one input pin and one output pin.

SEE ALSO

set_clock_tree_references(2)

CTS-117 (Warning) Set %s exception on a pin with %s

exception already

DESCRIPTION

Specified exception is set on a pin that already has an explicit exception on it. Explicit exceptions of pin has rule of precedence: Explicit-Nonstop > Explicit-Ignore > Explicit-Float > Explicit-Stop. Exception with higher priority can override that with lower priority. If the specified exception is lower than the former one in priority, the former will be retained and the latter is ignored.

WHAT NEXT

Make sure you are using the right exception on a specified pin. If you really want to set the latter exception but it is ignored for lower priority, please use **remove_clock_tree_exceptions** command to remove the pre-existing exception on that pin first.

SEE ALSO

set_clock_tree_exceptions(2)
remove_clock_tree_exceptions(2)

CTS-118 (Information) Pin %s is connected to a pad net. CTS will attempt buffering behind pad cell %s.

DESCRIPTION

You receive this message because the root of the clock-tree was specified on a top-level port or an input pin of a pad cell that connects to a pad net. (A pad net is a net that connects a top-level design port to a pad cell pin.) Clock Tree Synthesis (CTS) cannot buffer such nets because they are implemented outside of the chip. CTS is attempting to use the pad cell as the real root cell for the current clock tree.

WHAT NEXT

Ensure that the reported pad cell is the correct driver for the current clock tree. If not, change the definition of the current clock tree and use an input pad output pin or a core cell pin to define the clock root.

CTS-119 (Warning)Input transition of %f and/or output capacitance %f lead to negative delay while timing %s (%s) cell

between %s and %s pins. Using zero delay value instead.

DESCRIPTION

You receive this message because the delay calculation engine returned a negative cell delay.

WHAT NEXT

No action is required on your part. However, you can ensure that you are using your library cells within their characterization range.

CTS-120 (Warning) Input transition of %f and/or output capacitance %f lead to negative output slew while timing %s (%s) cell between %s and %s pins. Using zero slew value instead.

DESCRIPTION

You receive this message because the output slew calculation engine returned a negative output transition value.

WHAT NEXT

No action is required on your part. However, you can ensure that you are using your library cells within their characterization range.

CTS-121 (Warning) Clock %s has ideal clock attributes. No timing will be reported.

DESCRIPTION

You receive this message because the **report_clock_tree** command detected that the reported clock tree is part of a clock network that carries one or more ideal clock attributes, as set by using the **set_clock_latency**, **set_clock_uncertainty**, or **set_clock_transition** command. Meaningful clock delays cannot be reported for such a clock. In this case, the **report_clock_tree** command reports only the clock tree netlist structure. For this command to report meaningful clock delays, the clock tree must be part of a clock network that is set in propagated delay mode and does not have ideal clock attributes.

WHAT NEXT

No action is required on your part. However, this message usually appears when you attempt to run **report_clock_tree** on a nonsynthesized clock. To be able to time the clock network, you must first synthesize it by using the **compile_clock_tree** command, or you must run it on a netlist that already has buffered clock networks from a third-party tool. The **compile_clock_tree** command manages any ideal attributes present on the clock, but if your goal is to report a clock tree generated from a third-party tool, you must manually remove the ideal clock attributes by using the **remove_clock_latency**, **remove_clock_uncertainty**, and **remove_clock_transition** commands.

SEE ALSO

compile_clock_tree (2), **remove_clock_latency** (2), **remove_clock_transition** (2), **remove_clock_uncertainty** (2), **report_clock_tree** (2), **set_clock_latency** (2), **set_clock_transition** (2), **set_clock_uncertainty** (2).

CTS-122 (Error) Cannot modify dont_touch hierarchy %s for %s/%s pin.

DESCRIPTION

You receive this message because a clock tree in your design traces to the reported pin, which is found within a subdesign protected by the dont_touch attribute. Clock Tree Synthesis cannot compile this clock tree because a dont_touch subdesign cannot be modified.

WHAT NEXT

Remove the **dont_touch** attribute from the subdesign represented by the specified hierarchical cell as follows.

1. Execute the **report_cell** command for the hierarchical cell specified by this message. This provides you with the name of the corresponding subdesign.

2. Use the **current_design** command to set this subdesign to be the *current_design*.

3. Remove the **dont_touch** attribute from the *current_design*.

4. Set the *current_design* back to the one you work on.

5. Uniquify the design.

SEE ALSO

current_design (2), **report_cell** (2).

CTS-123 (Information) Convergent clock paths in clock network at output pin %s

DESCRIPTION

You receive this message because two different clock paths in the netlist start at the specified root and trace to the same pin.

The **compile_clock_tree** command automatically infers subtrees starting from each convergence cell in the clock network and automatically compiles the inferred subtrees in a bottom-up order. When compiling the main clock tree, a dont_touch_subtree constraint is automatically applied on the pins of each convergence cell.

WHAT NEXT

You may choose to define a stop pin or an exclude pin exception on the pins of certain convergence cells. This might be desirable, for example, if the subtree rooted behind a reconvergence does not drive any sequential cell clock pins. In this situation, you could choose to define a stop pin or an exclude pin exception on the pins of certain convergence cells. The **compile_clock_tree** command does not automatically detect such design-specific situations, and it is the user's responsibility to set the appropriate clock tree exceptions in these cases.

SEE ALSO

compile_clock_tree (2).

CTS-124 (Warning) Convergent clock paths detected at pin %s - Please define a clock tree rooted at that pin and compile it prior to compiling the current clock tree.

DESCRIPTION

Two different clock paths tracing to the same pin were detected in the fanout of the clock network for which you attempt to define a clock tree. The *set_clock_tree_options* command will force the subtree rooted at the reconvergence to be a dont_touch_subtree.

WHAT NEXT

Apply one of the following methods, depending on the desired design functionality: 1)if the clock tree does not contain any sinks behind the reconvergence, define all the input pins of the reconvergent cell that are on the clock network as stop or excluded pins. Declare them as stop pins if you want the delay at the reconvergent

cell input to be the same as other clock pins, or declare them as excluded pins if you do not care about the clock delays behind the reconvergence. 2)if the clock tree does not contain any sinks before the reconvergence, redefine the root of the clock tree at the output of the reconvergent cell. 3)if the clock tree contains sinks both before and after the reconvergence, declare a new clock tree rooted at the output of the reconvergent cell and compile it before the main clock tree. While compiling the main clock tree, the **compile_clock_tree** command will automatically force this sub-clock tree as a dont_touch_subtree, and will preserve existing buffering on that subtree. Make sure that you compile the any reconvergence subtree BEFORE you compile the main clock tree, otherwise this part of the clock-tree will not be properly buffered. If a reconvergent clock tree contains reconvergences, make sure that the deepest subtrees are compiled first and compile the convergence subtrees in a bottom up order.

In case 3), it is the user responsibility to ensure that a convergence subtree is compiled before compiling the clock tree that contains it.

CTS-125 (Warning) Skew values reported possibly are between exclusive clock paths behind a reconvergence in the clock network.

DESCRIPTION

You receive this message because the tool detected two different clock paths that trace to the same pin in the fanout of the clock network that you are attempting to report. The *report_clock_tree* command might have computed a skew that can be obtained only from exclusive clock paths.

WHAT NEXT

Use the **set_case_analysis** command to resolve conflicting clock paths at each reconvergence. Use the list of the reconvergences signaled by the **CTS-126** message to set appropriate case analysis conditions for verifying the clock tree timings. Run the **report_clock_tree** command for each exclusive clock propagation scenario.

SEE ALSO

CTS-126 (n); **report_clock_tree** (2).

CTS-126 (Information) reconvergence detected between pins

%s/%s and %s/%s.

DESCRIPTION

You receive this message because the two reported pins are driven from two distinct branches of the clock network and drive a shared portion of the clock network, called a reconvergence. The *report_clock_tree* may have computed a skew that can be obtained only from exclusive clock paths. It is important to set timing constraints appropriately to study the propagation of the clock signal in each of the exclusive scenarios resulting from the reconvergence.

WHAT NEXT

Use **set_case_analysis** to resolve conflicting clock paths at each reconvergence. Use the list of the reconvergences signaled by this message to set appropriate case analysis conditions in order to verify the clock tree timings. Run **report_clock_tree** for each exclusive clock propagation scenario.

SEE ALSO

report_clock_tree (2), **set_case_analysis** (2).

CTS-127 (warning) Possible clock tree overlap detected for %s .

DESCRIPTION

This warning occurs because the specified clock, which has not yet been compiled, includes one or more cells that either belong to one of the already-compiled clock trees or represent existing buffering.

WHAT NEXT

No action is required on your part if you want to keep preexisting buffering. Otherwise, use the **remove_buffer_tree** command to remove it.

The tool automatically handles overlapping clock paths by setting an implicit dont_touch subtree exception on the overlapping clock subtree after you synthesize the first clock in the overlapping clock path. For the best results, compile the most critical clock first.

SEE ALSO

remove_buffer_tree(2)
set_clock_tree_exceptions(2)

CTS-128 (Error) Non-default routing rule %s for clock tree %s does not exist in current technology database - clock routes will be implemented using default routing rule.

DESCRIPTION

The *-routing_rule* option of **set_clock_tree_options** was passed a routing rule name which cannot be matched in the technology database of the current design.

WHAT NEXT

Please check for typos and make sure that you are passing the correct routing rule name to the command **set_clock_tree_options**.

CTS-129 (Information) Specified hard constraint of %d buffer levels for %s clock.

DESCRIPTION

You receive this information message because there is a nonzero number of buffer levels either in the design database file or being passed through the **-number_of_levels** option of the **set_clock_tree_options** command for the use by the Clock Tree Compiler.

This constraint is considered for nongated clock trees only.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

set_clock_tree_options (2).

CTS-130 (Information) Specified soft constraint the structure of minimum number of buffers per level for %s clock.

DESCRIPTION

You receive this information message because the tool found the specified structure

of the minimum number of buffers and/or inverters per level in the design database file or passed through the **-number_of_instances_per_level** option of the **set_clock_tree_options** command for use by the Clock Tree Compiler (CTC).

WHAT NEXT

The CTC does not precisely follow this structure, but handles it as a soft constraint instead.

This is an informational message only. No action is required on your part.

SEE ALSO

set_clock_tree_options (2).

CTS-131 (Warning) Max_delay of %f is less than Min_delay of %f for %s clock. Min_delay value will be ignored.

DESCRIPTION

You receive this warning message because inconsistent max_delay and min_delay constraints occur in the design database file, or are passed through the **-max_delay** and **-min_delay** options of **set_clock_tree_options** command for use by the Clock Tree Compiler (CTC).

CTC cannot satisfy contradicting constraints, so min_delay is ignored.

WHAT NEXT

This is a warning message only. No action is required on your part.

However, you can eliminate the warning message by making the referred constraints consistent.

SEE ALSO

set_clock_tree_options (2).

CTS-132 (Warning) The difference between Max_delay of %f and Min_delay of %f is less than Max_skew of %f for %s clock.

Max_skew value will be ignored.

DESCRIPTION

You receive this warning message because inconsistent max_delay, min_delay, and max_skew constraints occur in the design database file, or are passed through the **-max_delay**, **-min_delay**, and **-max_skew** options of the **set_clock_tree_options** command for the use by the Clock Tree Compiler (CTC).

CTC cannot satisfy contradicting constraints, so max_skew is ignored.

WHAT NEXT

This is a warning message only. No action is required on your part.

However, you can eliminate the warning message by making the referred constraints consistent.

SEE ALSO

set_clock_tree_options (2).

CTS-133 (Error) Port %s of design %s cannot be a root port because it is not a port of the top-level design.

DESCRIPTION

You receive this error message because the **set_clock_tree_options** command or another Clock Tree Compiler command was passed a root port that is not a port of the top-level hierarchy. Only top-level ports or leaf-cell pins can be specified as the root of a clock tree.

WHAT NEXT

Check the root pin and root port arguments in the script. You might have passed the result of a **get_ports** command instead of the result of a **get_pins** command as a root pin or root port argument.

Make the necessary corrections and run the command again.

SEE ALSO

get_pins (2), **get_ports** (2), **set_clock_tree_options** (2).

CTS-134 (Error) Design database does not have routing grid.

DESCRIPTION

The information about the routing tracks on the metal layers is missing from the design database. Global router cannot be run for the net synthesized during clock tree synthesis. The delays and capacitances on the nets will not be backannotated. The post route results might not correlate well with the report_clock_tree.

WHAT NEXT

Update the design database with the information regarding the routing grid.

CTS-135 (Information) Setting %s clock to be propagated...

DESCRIPTION

You receive this information message because the synthesized clock is set to be propagated.

WHAT NEXT

This is an informational message only. No action is required on your part.

CTS-136 (Information) Driving cell %s (%s to %s) has been found in the netlist for the root pin of the clock tree.

DESCRIPTION

You receive this information message when the tool applies the cell found in the netlist as the driver of the root of your clock tree.

WHAT NEXT

This is an informational message only. No action is required on your part.

However, if the root is a hierarchical pin, you can use the **set_driving_cell** command to specify another driver.

SEE ALSO

set_driving_cell (2).

CTS-137 (Information) Detected an ILM block clock port %s - forcing a dont_touch_subtree

DESCRIPTION

You receive this information message because an input clock pin of an SILM hierarchy is detected on the clock tree. The clock subtree driven inside the SILM hierarchy is forced as a dont_touch_subtree.

WHAT NEXT

This is an informational message only. No action is required on your part.

CTS-138 (Information) There are exceptions for %s clock tree. Use -exceptions option to get more information.

DESCRIPTION

You receive this information message because there are exceptions on the specified clock tree.

WHAT NEXT

This is an informational message only. No action is required on your part.

However, you can use the **-exceptions** option for the **report_clock_tree** command to get detailed information on the pin name and type of each exception.

SEE ALSO

report_clock_tree (2).

CTS-139 (Warning) Library cell %s will not be used for CTS buffering since it carries a dont_touch or dont_use attribute.

DESCRIPTION

You receive this warning message because library cells with a **dont_use** or **dont_touch** attribute cannot be used by synthesis and CTS.

WHAT NEXT

This is a warning message only. No action is required on your part.

However, if you are positive this library cell is a correct choice for CTS, you can remove the **dont_touch** or **dont_use** attribute on the library cell with the following commands:

```
set_dont_touch [get_lib_cell lib_name/reference_name] false
set_attribute [get_lib_cell lib_name/reference_name] dont_use false
```

SEE ALSO

set_attribute (2), **set_dont_touch** (2).

CTS-140 (Error) Cannot find any valid reference for buffering.

DESCRIPTION

This error message indicates that none of the library cells specified in the list of available references can be used by synthesis and CTS. If your flow does not use the **set_clock_tree_references** command, this is valid for the entire list of buffers/inverters available in the target library. This error message occurs when all of the library cells have the **dont_touch** or **dont_use** attribute.

WHAT NEXT

Confirm that the library cell you specified with the **set_clock_tree_references** command is the correct choice for CTS. Use the following commands to remove the **dont_touch** or **dont_use** attribute on the library cell and then run the command again.

```
set_dont_touch [get_lib_cell lib_name/reference_name] false
set_attribute [get_lib_cell lib_name/reference_name] dont_use false
```

Alternatively, you can reset the entire list of references using the **reset_clock_tree_references** command. All of the appropriate references from the library are then available for the synthesis engine.

SEE ALSO

reset_clock_tree_references (2), **set_attribute** (2), **set_clock_tree_references** (2), **set_dont_touch** (2).

CTS-141 (Information) Sink pin %s has timing arcs to internal

pins and will be forced as a floatpin exception

DESCRIPTION

You receive this information message when the Clock Tree Compiler (CTC) detects timing arcs between the specified pin and internal pin of the same cell. The timing arcs are used to estimate internal clock delays in the cell.

WHAT NEXT

This is an informational message only. No action is required on your part.

CTS-142 (Warning) Sink pin %s is a floatpin and has timing arcs to internal pins - overriding internal delay model with the floatpin definition

DESCRIPTION

You receive this warning message because the Clock Tree Compiler (CTC) detects timing arcs between the specified sink pin and the internal pin of the same cell. The timing arcs are ignored because there is also a floatpin attribute on that pin.

The CTC uses the floatpin attributes to evaluate the internal delays associated with this sink pin.

WHAT NEXT

This is a warning message only. No action is required on your part.

However, if you want the CTC to use the internal delay models instead of the floatpin attributes, use the **remove_clock_tree_exceptions** command on the pin to delete the floatpin attributes.

SEE ALSO

remove_clock_tree_exceptions (2).

CTS-143 (Error) Could not find the logical or physical libraries.

DESCRIPTION

Inconsistent or missing library data.

WHAT NEXT

Check your search path and the accessibility of the library files.

CTS-144 (Warning) Some routing tracks on layer %s are outside the core area.

DESCRIPTION

Some of the routing track on the specified layer in the floorplan are outside the core area.

WHAT NEXT

Check your floorplan. Write out the PDEF file to see the core area and routing track definition, correct it and read back the modified PDEF file.

CTS-145 (Error) Port %s has back-annotated external load of %f capacitance units, which exceeds max_cap DRC constraint of %f.

DESCRIPTION

CTS currently does not support the computing of external port load based on wire-load models and the fanout number. Only capacitance values annotated on the port using the **set_load** command will be taken into account. If this capacitance exceeds max_cap DRC constraint, there is no way compiled clock tree will meet this constraint.

WHAT NEXT

Use the **set_load** command to annotate the desired external load on the specified clock port. Remove the annotated fanout number on the port using **remove_attribute**. Make sure that annotated capacitance not only does not violate max_cap DRC constraint but also leaves enough margin for CTC to meet this constraint for the net driven by the clock tree root port. One can resolve the problem in the opposite way, namely by relaxing max_cap constraint.

CTS-146 (Information) Removed %d buffers and/or inverters

DESCRIPTION

WHAT NEXT

CTS-147 (Warning) Invalid argument value for -edge: %s - resetting to default.

DESCRIPTION

Possible values for this options are {rise fall both default}.

WHAT NEXT

Check your script. Consult the **set_clock_tree_exceptions** man pages for more details on the **-active_edge** option.

CTS-148 (Error) Cannot specify *-active_edge* without *-stop_pins*.

DESCRIPTION

The *-active_edge* option was specified on the command line but there was no *-stop_pins* list.

WHAT NEXT

Check your script. Consult the **set_clock_tree_exceptions** man pages for more details on the **-active_edge** option.

CTS-149 (Error) Invalid *-priority* value specified.

DESCRIPTION

The value for *-priority* option can only include one or more items from the following list {'skew' 'delay' 'instances' 'area'}.

WHAT NEXT

Check your script. Make sure to use correct values.

CTS-150 (Warning) Tracing through sequential preexisting cell: %s.

DESCRIPTION

A latch or some other type of sequential cell is found on the clock network and considered as preexisting logic because it contains combinatorial arcs that can be traced through.

WHAT NEXT

Define a stop_pin or exclude_pin on the input pin of this preexisting cell using the **set_clock_tree_exceptions** command if you do not want to balance clock delays on clock pins beyond the reported cell. Define a stop_pin if you want to balance the delay to the input of the preexisting cell with the delays to the other clock pins. Define an exclude pin in case you do not want to balance this delay.

CTS-151 (Information) Sizing the preexisting cells in the clock tree %s.

DESCRIPTION

The tool is beginning the gate sizing stage for the specified clock tree.

WHAT NEXT

This is an informational message only. No action is required on your part.

However, If you do not want to size gates, reissue the **compile_clock_tree** command without specifying the **-size_gates** option.

SEE ALSO

compile_clock_tree (2).

CTS-152 (Information) Replaced the library cell of %s from %s

to %s.

DESCRIPTION

The tool is pointing to the instance cell being sized. The message includes both source and destination reference cells.

WHAT NEXT

This is an informational message only. No action is required on your part.

CTS-153 (Information) Sized %d preexisting cells.

DESCRIPTION

The tool is showing the number of sized cells in the clock network.

WHAT NEXT

This is an informational message only. No action is required on your part.

CTS-154 (Warning) Reference %s will be ignored for compilation of %s clock tree.

DESCRIPTION

You specified a reference using -reference_per_level option of 'set_clock_tree_options' command but this reference is not in the list available for compilation of a given clock tree.

WHAT NEXT

Make sure to pass the reference through 'set_clock_tree_references' command prior to issuing 'compile_clock_tree'. Alternatively, you can rerun 'set_clock_tree_options' command where specified reference is removed from the list passed through -reference_per_level option.

CTS-155 (Warning) Specified -reference_per_level option will

be ignored to avoid bad logic in %s clock tree.

DESCRIPTION

You specified an odd number of inverters in -reference_per_level option of 'set_clock_tree_options' command, which could result in bad logic if followed strictly.

WHAT NEXT

Make sure to pass an even number of inverters through 'set_clock_tree_references' command.

CTS-156 (Warning) drive of root pin %s is incompatible with max_transition constraint %f: input transitions (%f, %f), load %f lead to (%f, %f) output transition on the root pin

DESCRIPTION

Clock Tree Compiler detects an incompatibility between the library model of the reported clock tree root cell and the specified max_transition constraint currently in use for this clock tree. Even using "reasonable" input transitions (the minimum between a typical input transition and the actual transition times on the input of the root), and a typical root net load, the transition times computed at the root pin are bigger than the reported constraint. The values of the input transitions and output load, as well as the resulting root pin transition values are reported in the message.

WHAT NEXT

Consider swapping the root cell to a logical equivalent with a higher drive. Check the timing library model of the root cell. Check that the max_transition constraint is feasible. Do not use 0 max_transition constraint as way to give a higher cost to max_transition DRC while compiling clock trees. Use instead the dedicated options of compile_clock_tree in order to control the cost trade-offs of the CTS buffering algorithm.

CTS-157 (Error) library model for root pin %s is incompatible with max_insertion_delay constraint %f: input transitions (%f,

%f), load %f lead to (%f, %f) insertion delay spent in the root cell

DESCRIPTION

Clock Tree Compiler detects an incompatibility between the library model of the reported clock tree root cell and the specified max_insertion_delay constraint used for this clock tree. Even using "reasonable" input transitions (the minimum between a typical input transition and the actual transition times on the input of the root), and a typical root net load, the delay spent in the root cell is bigger than the insertion delay allocated for the whole clock tree. The values of the input transitions and output load, as well as the resulting root cell delay values are reported in the message.

WHAT NEXT

Consider swapping the root cell to a logical equivalent with a higher drive. Check the timing library model of the root cell. Check that the insertion delay constraint is feasible. Do not use 0 as the insertion delay constraint in the hope of getting the minimum insertion delay possible. Use instead the dedicated options of compile_clock_tree in order to control the cost trade-offs of the CTS buffering algorithm.

CTS-158 (Error) transitions (%f, %f) on root cell input pin %s limit output load to %f using max_transition rule %f on the output

DESCRIPTION

The input side of the clock tree root cell is driven by a signal with the transition times reported in the message. This prevents Clock Tree Compiler from loading the root net with more than the advertised value, which seems too small with regard to the value of the gate capacitance of available clock tree buffers. Clock tree compilation is aborted because no solution to buffer the root net is feasible without violating the Design Rule Checks currently in use.

WHAT NEXT

If the input transitions are fairly close to the max_transition rule currently in use, it may result in a tight load constraint on the output. This may also be caused by the weak drive of the root cell. Consider swapping the root cell to a logical equivalent with a higher drive. If applicable, investigate the reason for the high input transition times and fix them. Available alternatives include, but are not limited to: buffering the fanin of the root cell, increasing the drive strength of the fanin net driver, removing or relaxing ideal or back-annotated clock transitions propagated to the root cell input.

CTS-159 (Warning) transitions (%f, %f) on root cell input pin %s limit output load to %f: using input transition of (%f, %f), max_capacitance of %f

DESCRIPTION

The input side of the clock tree root cell is driven by a signal with the reported transition time. Using this input transition on the root cell, a typical load on the output pin leads to a violation of the max_transition rule. The root cell was identified as the root of a convergence subtree. Therefore Clock Tree Compiler is assuming that these input transitions are likely to be reduced after the input net gets buffered. Clock Tree Compiler is using the reported transition values (rise and fall) on the input of the root cell while compiling this subtree. The max_capacitance value reported corresponds to the maximum value of the load on the root pin that can be accomodated using those input transitions.

WHAT NEXT

The violation of output transition with a typical load is an indication that the drive of the root cell of this subtree might be too weak. If you cannot meet your skew and insertion delay constraints using this cell, you need to consider using a logical equivalent of the root cell with a higher drive strength.

CTS-160 (Warning) violating transitions (%f, %f) on root cell input pin %s limit output load to %f using max_transition rule %f on the output

DESCRIPTION

The input side of the clock tree root cell is driven by a signal with a violating transition time. This prevents Clock Tree Compiler from loading the root net with more than the advertised value, which seems too small with regard to the value of the gate capacitance of available clock tree buffers. Clock tree compilation is aborted because no solution to buffer the root net is feasible without violating the Design Rule Checks currently in use.

WHAT NEXT

This condition may be only caused by the violating input transition on the input of the root cell, or may be a combination of this and a weak drive of the root cell. Consider swapping the root cell to a logical equivalent with a higher drive. Investigate the reason for the violating input transition and fix this condition. Available alternatives include, but are not limited to: buffering the fanin of the root cell, increasing the drive strength of the fanin net driver, removing or relaxing any violating ideal or back-annotated clock transitions propagated to the

root cell input.

CTS-161 (Warning) violating transitions (%f, %f) on subtree root cell input pin %s: using input transition of (%f, %f), max_capacitance of %f

DESCRIPTION

The input side of the clock tree root cell is driven by a signal with violating transition times. Using this input transition on the root cell, a typical load on the output pin leads to a violation of the max_transition rule. The root cell was identified as the root of a convergence subtree. Therefore Clock Tree Compiler is assuming that these violating input transitions are likely to disappear after the input net gets buffered. Clock Tree Compiler is using the reported transition values (rise and fall) on the input of the root cell while compiling this subtree. The max_capacitance value reported corresponds to the maximum value of the load on the root pin that can be accomodated using those input transitions.

WHAT NEXT

The violation of output transition with a typical load is an indication that the drive of the root cell of this subtree might be too weak. If you cannot meet your skew and insertion delay constraints using this cell, you need to consider using a logical equivalent of the root cell with a higher drive strength.

CTS-162 (Warning) violating transitions (%f, %f) on root cell input pin %s limit output load to %f using max_transition rule %f on the output

DESCRIPTION

The input side of the clock tree root cell is driven by a signal with a violating transition time. This does not prevent Clock Tree Compiler from buffering the clock tree, but forces it to limit the load of the root to the advertised value.

WHAT NEXT

If the value of the load limit cannot be achieved during compilation, you need to consider fixing this high transition value on the root cell input first. This may be caused by unrealistic ideal clock transition, too high back annotated transitions or capacitance on the root input net, possibly because the input net has not been buffered yet.

CTS-163 (Warning) violating transitions (%f, %f) on subtree root cell input pin %s: using input transition of (%f, %f), max_capacitance of %f

DESCRIPTION

The input side of the clock tree root cell is driven by a signal with a violating transition time. The root cell was identified as the root of a convergence subtree. Therefore Clock Tree Compiler is assuming that this violating input transition is likely to disappear after the input net gets buffered. Clock Tree Compiler is using the reported transition values (rise and fall) on the input of the root cell while compiling this subtree. The max_capacitance value reported corresponds to the maximum value of the load on the root pin that can be accomodated using those input transitions.

WHAT NEXT

CTS-164 (Error) drive and external load of root port of clock tree %s causes max_transition violation, even assuming 0 internal load: (%f, %f)

DESCRIPTION

The root of the clock tree is a top-level design port, and this port has back-annotated external loads and drive constraints that causes a max_transition violation with respect to the library, design or CTS DRC constraints you have specified. This condition effectively prevents Clock Tree Compiler from producing a clock tree buffering compliant with the DRC constraints in use.

WHAT NEXT

Either increase the drive of the driving cell associated with the root port and, if applicable, relax the design and CTS max_capacitance constraints to accomodate the back-annotated load on the root port; or remove or lower the value of the *load* and *wire_capacitance* attributes on the port using the **remove_attribute** or **set_load** commands.

CTS-165 (Error) root port of clock tree %s has violating external

load: %f

DESCRIPTION

The root of the clock tree is a top-level design port, and this port has a back-annotated external load that causes a max_capacitance violation with respect to the library, design or CTS DRC constraints you have specified. This condition effectively prevents Clock Tree Compiler from producing a clock tree buffering compliant with the DRC constraints in use.

WHAT NEXT

Either increase the drive of the driving cell associated with the root port and, if applicable, relax the design and CTS max_capacitance constraints to accomodate the back-annotated load on the root port; or remove or lower the value of the *load* and *wire_capacitance* attributes on the port using the **remove_attribute** or **set_load** commands.

CTS-166 (Error) Design database does not have correct routing grid.

DESCRIPTION

The information about the routing tracks on the metal layers is not correct in the design database. Global router cannot be run for the net synthesized during clock tree synthesis. The delays and capacitances on the nets will not be backannotated. The post route results might not correlate well with the report_clock_tree.

One of the following might be true, if you are seeing this warning message: - Global tracks are only defined in one (X or Y) direction. Global tracks should be defined in both the direction for a valid routing grid. - The area covered by the placement grid (site rows) is greater than the area covered by the routing grid. The distance unit for specifying the routing tracks might be different than the distance unit specifying for location of the cells and other objects in the design.

WHAT NEXT

Write out the PDEF (version 3.0 or later) file by using the command write_pdef and check for the abovementioned symptoms in the PDEF file. Correct the routing grid information in the design database accordingly.

CTS-167 (Warning) net driven by pin %s in clock tree %s has back-annotated load from CTS but no dont_touch_subtree

constraint: forcing a dont_touch_subtree beyond this pin

DESCRIPTION

The reported net has the *has_cts_ba* attribute - which is the sign that it has been buffered by Clock Tree Compiler - but is not in a dont_touch_subtree part of the clock tree. This usually happens when there are overlapping clock trees (clock trees which share part of their respective networks), and the overlapping parts of the clock trees have not been properly constrained using a *dont_touch_subtree* clock tree exception.

WHAT NEXT

Clock Tree Compiler will infer a *dont_touch_subtree* exception for you beyond this pin. Not doing so in case this part of the clock tree is also seen from the root of an already compiled clock tree will result in disrupting the balancing of delays obtained while compiling the first clock tree. If it is your intention to buffer that part of the clock tree a second time, please contact your support.

CTS-168 (Warning) net driven by pin %s in clock tree %s has back-annotated load from CTS but no dont_touch_subtree constraint: a dont_touch_subtree constraint has been propagated to this pin from an ancestor pin in the clock tree

DESCRIPTION

The reported net has the *has_cts_ba* attribute - which is the sign that it has been buffered by Clock Tree Compiler - but is not in a dont_touch_subtree part of the clock tree. This usually happens when there are overlapping clock trees (clock trees which share part of their respective networks), and the overlapping parts of the clock trees have not been properly constrained using a *dont_touch_subtree* clock tree exception.

WHAT NEXT

Clock Tree Compiler will infer a *dont_touch_subtree* exception for you beyond this pin. Not doing so in case this part of the clock tree is also seen from the root of an already compiled clock tree will result in disrupting the balancing of delays obtained while compiling the first clock tree. If it is your intention to buffer that part of the clock tree a second time, please contact your support.

CTS-169 (Error) net driven by pin %s in clock tree %s has back-

annotated load from CTS but no dont_touch_subtree constraint

DESCRIPTION

The reported net has the *has_cts_ba* attribute - which is the sign that it has been buffered by Clock Tree Compiler - but is not in a dont_touch_subtree part of the clock tree. This usually happens when there are overlapping clock trees (clock trees which share part of their respective networks), and the overlapping parts of the clock trees have not been properly constrained using a *dont_touch_subtree* clock tree exception.

WHAT NEXT

By default, Clock Tree Compiler will infer a *dont_touch_subtree* exception for you beyond this pin. Not doing so in case this part of the clock tree is also seen from the root of an already compiled clock tree will result in disrupting the balancing of delays obtained while compiling the first clock tree. But you have set a control variable that causes the **compile_clock_tree** command to abort when such inconsistencies are detected instead of attempting to repair them. If this is not your intention, revert the control variable to its default value.

CTS-170 (Warning) net driven by pin %s in clock tree %s has back-annotated load from CTS but no dont_touch_subtree constraint

DESCRIPTION

The reported net has the *has_cts_ba* attribute - which is the sign that it has been buffered by Clock Tree Compiler - but is not in a dont_touch_subtree part of the clock tree. This usually happens when there are overlapping clock trees (clock trees which share part of their respective networks), and the overlapping parts of the clock trees have not been properly constrained using a *dont_touch_subtree* clock tree exception.

WHAT NEXT

By default, Clock Tree Compiler will infer a *dont_touch_subtree* exception for you beyond this pin. Not doing so in case this part of the clock tree is also seen from the root of an already compiled clock tree will result in disrupting the balancing of delays obtained while compiling the first clock tree. But you have set some control variables that causes the **compile_clock_tree** command to just report such inconsistencies instead of attempting to repair them. If this is not your intention, revert the control variables to their default values.

CTS-171 (Error) net driven by pin %s in clock tree %s is beyond a dont_touch_subtree pin but does not have the has_cts_ba attribute

DESCRIPTION

The reported pin is in a *dont_touch_subtree* part of the clock tree, but it drives a net which does not hold an accurate load estimation. In this situation, Clock Tree Compiler cannot guarantee a good correlation of the skew results after detailed routing.

WHAT NEXT

By default, Clock Tree Compiler will abort the compilation when this situation is detected. Fix the condition by buffering or forcing the load estimation on the incriminated net separately. In the pre-CTS phase, clock nets are usually set in ideal mode which prevents them from being estimated by the **run_router** command. If this is the case, set the clock network rooted at that pin in propagated mode using the **set_propagated_clock** command. Then use **run_router** to provide a realistic load estimation of the nets in the fanout of this pin.

CTS-172 (Warning) net driven by pin %s in clock tree %s is beyond a dont_touch_subtree pin but does not have the has_cts_ba attribute

DESCRIPTION

The reported pin is in a *dont_touch_subtree* part of the clock tree, but it drives a net which does not hold an accurate load estimation. In this situation, Clock Tree Compiler cannot guarantee a good correlation of the skew results after detailed routing.

WHAT NEXT

By default, Clock Tree Compiler will abort the compilation when this situation is detected. You have used some control variable to ignore this inconsistency and continue compiling the clock tree. You are likely to observe a poor correlation of the skew results post-detailed route.

CTS-173 (Error) net driven by root pin %s in clock tree %s already has back-annotated load from CTS: incremental clock

tree compilation detected

DESCRIPTION

The root of the clock tree drives a net which already has the *has_cts_ba* attribute. This is a sign that compile_clock_tree has already been run on this clock tree. Clock tree compilation is aborted as Clock Tree Compiler does not currently support incremental compilation.

WHAT NEXT

By default, Clock Tree Compiler will abort the compilation when this situation is detected. You need to cleanup any existing clock tree using the **remove_clock_tree** command before recompiling a new clock tree with new options. If it is your intention to run of **compile_clock_tree** incrementally, please contact your support.

CTS-174 (Warning) net driven by root pin %s in clock tree %s already has back-annotated load from CTS: attempting incremental clock tree compilation

DESCRIPTION

The root of the clock tree drives a net which already has the *has_cts_ba* attribute. This is a sign that compile_clock_tree has already been run on this clock tree. Clock Tree Compiler does not currently support incremental compilation.

WHAT NEXT

By default, Clock Tree Compiler will abort the compilation when this situation is detected. You are supposed to cleanup any existing clock tree using the **remove_clock_tree** command before recompiling a new clock tree with new options. You have used a control variable that forces the compilation of this clock tree to continue. Do not expect improved skew and insertion delay out of such incremental run.

CTS-175 (Error) Cell %s does not have a logical or physical library cell associated with it.

DESCRIPTION

Inconsistent or missing library data.

WHAT NEXT

Check the values of the variables search_path, target_library, link_library, physical_library and the accessibility of the library files.

CTS-176 (Error) Clock tree synthesis has abnormally terminated.

DESCRIPTION

This message indicates that the compile_clock_tree has terminated and has not written the intermediate design back to the database. Because the design has not been written back to the database, the current design is unchanged.

WHAT NEXT

Please contact your Synopsys support representative.

CTS-177 (Warning) No placement site available near the root %s/%s and hence cannot fix DRC violation.

DESCRIPTION

No placement site available near the root and hence cannot fix DRC violation.

WHAT NEXT

Check placement or floorplan. Loose DRC constraints.

CTS-178 (Warning) There are %d Steiner routed nets.

DESCRIPTION

Unsufficient routing resources for the layers specified for clock tree. Reverting to using steiner routing. The steiner router does not know about routing blockages. This will cause problems in timing correlation post detail route.

WHAT NEXT

Specify more routing layers for clock tree. Check correctness of routing rules.

CTS-179 (Information) Updating connections for hierarchical design.

DESCRIPTION

Informs the user that CTC is reconnecting the netlist objects through logical hierarchy.

WHAT NEXT

Just wait.

CTS-180 (Information) clock tree %s uses Useful Skew mode.

DESCRIPTION

Informs the user that CTC has detected the presence of set_clock_useful_skew constraints in the database applying to the reported clock tree.

WHAT NEXT

Make sure you want to run CTS in Useful Skew mode on this clock tree.

CTS-181 (Information) Clock tree %s uses Zero Skew mode.

DESCRIPTION

Informs the user that CTC is set to use Zero Skew mode on this clock tree.

WHAT NEXT

If you intend to run Useful Skew synthesis on that clock, check that 'set_clock_useful_skew' constraints are properly set.

CTS-182 (Error) Must specify at least one pin, port or clock

argument

DESCRIPTION

The **set_useful_skew** command must apply to a valid collection of clock, pin or port objects. An empty or invalid collection was passed in argument to the command.

WHAT NEXT

Check the syntax of the command. Check that your arguments match valid netlist objects.

CTS-183 (Error) incorrect effort argument: %s, must be in {disable low medium high ultra}

DESCRIPTION

The **set_useful_skew** command was passed a *-tns_effort* or *-wns_effort* argument which is not in the supported set.

WHAT NEXT

Check the syntax of the command.

CTS-184 (Warning) could not derive valid floatpin constraints for Useful skew

DESCRIPTION

The Useful Skew mode is on for the current clock but no valid adjusted clock timings could be computed. No floatpin constraints will be generated and the compilation results will be identical to the Zero Skew mode.

WHAT NEXT

Contact your support.

CTS-185 (Warning) clock %s has no defined clock attributes - a

null latency will be assumed

DESCRIPTION

The Useful Skew mode is on for the current clock but no ideal clock attributes (latency, uncertainty) are available to model the ideal clock timings. The clock adjustment calculations will be done with respect to an ideal clock latency of 0 for all clock pins of the current clock tree.

WHAT NEXT

Check whether your ideal clock definitions are consistent with a CTS flow. CTS will insert buffering which will cause the clock latency to flip-flops and latches to become non-null. Timing paths versus IO ports are likely to change and new violations are likely to occur if you do not capture the CTS insertion delay budget using a clock latency statement, and the CTS skew budget using an uncertainty statement.

CTS-186 (Information) generated %d float pin constraints for Useful Skew mode (%d positive, %d negative)

DESCRIPTION

The Useful Skew mode performs clock latency adjustment based on the pre-CTS ideal clock timings and translate this automatically into float pin constraints that are passed to the CTS engine. This message provides you with information about how many such constraints were generated for the current clock tree.

WHAT NEXT

The number of float pin constraints generated in Useful Skew mode should not be too big because the QoR will typically degrade as the number of exceptions gets larger. Even though the target latency values aimed by CTS theoretically improves the timing QoR, CTS then has a harder time getting close to the targets. If you see large numbers of exceptions, try to reduce the Useful Skew efforts to generate less float pin constraints. CTS does not share buffers chains used to accomodate negative float pin constraints. If you see predominentely negative float pin values in large numbers, try to tweak the plus and minus adjust bound parameters of the **set_clock_useful_skew** command so as to reduce the number of negative float pins.

CTS-187 (Warning) CTC is performing high fanout net

synthesis. No backannotation is expected.

DESCRIPTION

-high_fanout option has been specified for **set_clock_tree_options** command for current clock tree. CTC does not backannotate pin-to-pin delays and net capacitances as well as global preroutes.

WHAT NEXT

If high fanout net synthesis is not what is expected here, reissue **set_clock_tree_options** command for current clock tree without -high_fanout option.

CTS-188 (Information) Removing buffer trees for clock domain %s...

DESCRIPTION

Information message.

WHAT NEXT

Wait a little.

CTS-189 (Information) Tracing through sequential cell of type %s to generated clock source output %s/%s

DESCRIPTION

This information message is issued during Clock Tree Tracing to notify you that the clock tree contains generated clock subtrees. This means that the clock tree synthesis will balance clock tree delays up to clock pins in the clock domain of the generated clock.

WHAT NEXT

If you do not want Clock Tree Compiler to balance generated clock with the primary clock domain, use the **-dont_trace_generated_clocks** switch on the **set_clock_tree_option** command line.

CTS-190 (Warning) Cell %s has several generated clock source output pins - pin %s was selected for clock tree tracing

DESCRIPTION

A sequential cell was traced-through during Clock Tree Tracing, but Clock Tree Compiler detected that this cell has several output pin bearing generated clock definitions. Clock Tree Compiler does not support tracing through a cell to multiple outputs, and therefore selects only one output to trace through the cell.

WHAT NEXT

If your design requires Clock Tree Compiler to balance all generated clocks at the output of this cell together with the main clock, please contact your support.

CTS-191 (Warning) Cell %s has some generated clock source output pins but combinatorial output pin %s was preferred for clock tree tracing

DESCRIPTION

The advertised cell was traced-through during Clock Tree Tracing, but Clock Tree Compiler detected that this cell has at least one output pin supporting a generated clock definition. Clock Tree Compiler does not support tracing through a cell to multiple outputs, and therefore selects only one output to trace through the cell. While doing so, it priviledges outputs with combinatorial timing arcs.

WHAT NEXT

If your design requires Clock Tree Compiler to balance the generated clock(s) at the output of this cell together with the main clock, please contact your support.

CTS-192 (Warning) Clock tree %s contains generated clock source pins but was set in Useful Skew mode - resetting to Zero Skew mode

DESCRIPTION

Clock Tree Compiler detected some generated clock source pins in your clock tree, but you are also using the Useful Skew mode on this clock tree. The current Useful

Skew capability in Clock Tree Compiler does not support adjusting clock delays through multiple clock domains. Therefore your clock tree is run in Zero Skew mode.

WHAT NEXT

If your design requires Clock Tree Compiler to balance a clock tree with generated clock(s) in Useful Skew mode, please contact your support.

CTS-193 (Information) Noncritical sinks are ignored during compilation and reporting of %s clock tree.

DESCRIPTION

Compilation and reporting specified clock tree are performed according to ignore noncritical sinks mode. Skew and delay up to noncritical sinks will not be taken into account.

WHAT NEXT

If you do not want to use this mode, reissue set_clock_tree_options command.

CTS-194 (Warning) No driving cell found for root port %s on cell %s (%s) - using 0 delays and slews on the root port

DESCRIPTION

The root of your clock tree is a top-level port or an SILM block port. No driving cell was detected by CTC on the top-level port, or no driver was found in the SILM netlist for the SILM block port. In such a case, CTC assumes a fixed transition time of 0 on the root during compilation.

WHAT NEXT

Define a more realistic drive model of your root port using the **set_annotated_transition** command on an SILM block port root, or the **set_driving_cell** constraint on a top-level port root.

CTS-195 (Warning) No timing arc found for root pin %s of cell

%s (%s) - using 0 delays and slews on the root pin

DESCRIPTION

The specified root cell does not have a timing arc for establishing the drive model of the specified root pin. The clock tree compilation assumes a fixed transition time of 0 on the root cell output in this case, and a null delay throughthe root cell independent of the capacitive load on the root net.

WHAT NEXT

There is no timing information available to derive the drive model of this net. After clock tree synthesis, you need to back annotate a realistic transition time on the root cell ouput pin using the **set_annotated_transition** command. Not doing so may result in an unrealistic estimation of the transition time on the root net.

CTS-196 (Error) Insufficient free sites to place buffer.

DESCRIPTION

No empty space was found for buffer inserted during clock tree compilation, so **compile_clock_tree** failed and clock tree synthesis was not completed for this reason.

WHAT NEXT

Please check placement obstructions.

CTS-197 (Warning) Undefined transition at the input of the root of the clock tree occurred. Assuming zero value.

DESCRIPTION

CTC faced undefined transition at the starting pin of the root timing arc. To resolve the issue CTC assumes zero slew at that point.

WHAT NEXT

Beware of possible inconsistencies of report_clock_tree and report_timing as the latter command assumes zero transition at the output of the root cell regardless of the load.

CTS-198 (Warning) Subtree driven by %s/%s will be buffered to meet %s constraint.

DESCRIPTION

The specified subtree has satisfied delay and fanout requirements for avoiding buffering. However, it will be buffered anyway, since not buffering it would cause design rule checking (DRC) violations as described in the message you have received.

WHAT NEXT

No action is required on your part.

However, if you want to avoid buffering the net, you can relax the DRC constraints. You can also see the man page for the command that caused the warning for detailed information on specifying optional and required parameters.

CTS-199 (Warning) Net '%s' is not %sconnected and will be ignored.

DESCRIPTION

The **retime_clock_tree** command has detected a net that is not fully connected by global routing segments. Hence, it is not possible to recalculate the delay and capacitance of this net. The **retime_clock_tree** command ignores the net and currently-annotated delay and capacitance values are preserved.

WHAT NEXT

No action is required on your part.

However, if you want, you can examine the **CTS-178** error message warning regarding Steiner routed nets. You can also see the man page for the command that caused the warning for detailed information on specifying optional and required parameters.

SEE ALSO

compile_clock_tree (2), **retime_clock_tree** (2); **CTS-178** (n).

CTS-200 (Error) Nonexisting routing layer '%s' has been

specified for %s clock tree.

DESCRIPTION

You receive this error message because no layer ID can be found in design database for the layer specified.

WHAT NEXT

Check layer names existing in the design database. Then issue set_clock_tree_options command for the specified clock tree with the names of valid layers only.

CTS-201 (Warning) There are no suitable routing layers. The Steiner tree algorithm will be used for net delay estimation.

DESCRIPTION

The **compile_clock_tree** command has determined that there are no unoccupied routing layers specified by the **set_clock_tree_options** command. All specified routing layers appear to be completely utilized by routing obstructions. Hence, it is not possible to use global routing for net delay and capacitance estimation. The **compile_clock_tree** command uses the Steiner tree algorithm for routing estimation and does not annotate any global routing to the design database.

WHAT NEXT

Check the layers specified by the **set_clock_tree_options** command. Examine the routing obstructions in the design database. After making the necessary changes, run the command again.

SEE ALSO

compile_clock_tree (2), **set_clock_tree_options** (2); **CTS-178** (n).

CTS-202 (Warning) Incorrect routing rule specified for clock nets.

DESCRIPTION

The **compile_clock_tree** command has detected that the number of routing tracks required to place one global segment exceeds the capacity of the global cell. Hence, it is not possible to use global routing for net delay and capacitance estimation.

The **compile_clock_tree** command uses the Steiner tree for routing estimation.

WHAT NEXT

This is a warning message only, and no action is required on your part. However, you can check the routing rule specified by the **set_clock_tree_options** command. After making any changes, rerun the command.

SEE ALSO

compile_clock_tree (2), **set_clock_tree_options** (2), **CTS-178** (n).

CTS-203 (Error) Design database does not have routing layers.

DESCRIPTION

The information about the routing layers is missing from the design database.

WHAT NEXT

Update the design database with information regarding the routing layers.

SEE ALSO

read_db (2), **write** (2), **write_pdef** (2).

CTS-204 (warning) Incompatible direction of hierarchical pins. Ignoring %s.

DESCRIPTION

This warning message occurs when the tool traces through the hierarchical design and finds two hierarchical pins driving the same local net.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by checking the clock network and removing the duplicate pins that are driving the same local net.

CTS-205 (Warning) Option -use_default_routing_for_sinks will be applied to all clocks.

DESCRIPTION

Option *-use_default_routing_for_sinks* of **set_clock_tree_options** will be applied globally.

WHAT NEXT

Synthesize one clock at a time if different values needs to be used for different clocks.

CTS-206 (Error) User max_cap constraint (%f fF) is too small.

DESCRIPTION

Set_clock_tree_options assumes that the given constraint values are in main library units. The error is usually arised when the main library unit is smaller than that is assumed.

WHAT NEXT

Convert the constraint values into main library units and re-apply constraints again.

CTS-207 (Error) User max_tran constraint (%f ps) is too small.

DESCRIPTION

Set_clock_tree_options assumes that the given constraint values are in main library units. The error is usually arised when the main library unit is smaller than that is assumed.

WHAT NEXT

Convert the constraint values into main library units and re-apply constraints again.

CTS-208 (Error) User target_early_delay constraint (%f ps) is

too small.

DESCRIPTION

Set_clock_tree_options assumes that the given constraint values are in main library units. The error is usually arised when the main library unit is smaller than that is assumed.

WHAT NEXT

Convert the constraint values into main library units and re-apply constraints again.

CTS-209 (Warning) Either the driven net has been synthesized previously or clock path overlaps/reconverges at pin %s.

DESCRIPTION

Either the net driven by the pin has been synthesized or the pin is reachable from multiple clock paths that belong to either different clocks or the same clock.

WHAT NEXT

CTS-210 (Information) %s is a don"t size cell instance, skip sizing.

DESCRIPTION

The cell instance is specified in set_clock_tree_exception -dont_size_cell. Such cells will not be sized during CTS and CTO.

WHAT NEXT

If sizing is needed to improve QoR, please remove the exception setting.

CTS-211 (information) Pin %s is ignored. Cannot set

cts_synthesized on net %s.

DESCRIPTION

This information message advises you that when a driving pin is an ignore pin, the net may not be DRC clean and the **cts_synthesized** attribute is not set.

WHAT NEXT

This is only an information message. No action is required. However, the net can be handled by optimization for DRC.

CTS-212 (Information) Adding delay cell %s after driving pin %s.

DESCRIPTION

A delay cell, buffer or inverter, is added to reduce the global skew.

WHAT NEXT

If no delay insertion is desired, it can be turned off through command options.

CTS-213 (Warning) Adding buffer will cause capacitance constraint violation on the net %s.

DESCRIPTION

This message tries to give the reason on why delay cells can not be added, the tool sees adding any cell would cause capacitance violation. It is possible the net is violating capacitance constraint before adding cell and adding a cell can not remove the violation.

WHAT NEXT

Please check the root net or the first bufferable net capacitance.

CTS-214 (Warning) Adding buffer will cause transition constraint

violation on the net %s.

DESCRIPTION

This message tries to give the reason on why delay cells can not be added, the tool sees adding any cell would cause transition violation. It is possible the net is violating transition constraint before adding cell and adding a cell can not remove the violation.

WHAT NEXT

Please check the root net or the first bufferable net transition and capacitance.

CTS-215 (Warning) Adding buffer will cause skew degradation on the net %s.

DESCRIPTION

This message tries to give the reason on why delay cells can not be added, the tool sees adding any cell would cause skew degradation.

WHAT NEXT

Select balanced buffer list for delay insertion using set_clock_tree_reference -ref {list of lib cells} -delay_insertion may help.

CTS-216 (Warning) No buffer can fit the delay gap on net %s.

DESCRIPTION

This message tries to give the reason on why delay cells can not be added, the tool sees adding any cell would be over the target insertion delay.

WHAT NEXT

Provide small delay buffer list for delay insertion using set_clock_tree_reference -ref {list of lib cells} -delay_insertion may help.

CTS-217 (Warning) option -sync_phase will be ignored in CTS.

DESCRIPTION

The option -sync_phase in compile_clock_tree is for HFCTS only. That is, the option must be specified with option -high_fanout_net.

WHAT NEXT

If you intend to perform HFCTS, please specify -high_fanout_net option in compile_clock_tree command. If you intend to perform CTS, you don’t need to care about the message.

CTS-218 (Warning) unknow sync_phase %s. Set to default.

DESCRIPTION

The command compile_clock_tree -sync_phase takes only 3 options, rise (default), fall or both. If none of those is given, you will see the message. The tool will assume rise phase. The -sync_phase tells the tool how to calculate skew for the inserted buffer tree. If rise is given, the rising edge arrival time at buffer tree’s end points are used for skew calculation.

WHAT NEXT

If the default (rise) is not what you want, please specify fall or both option for command.

CTS-219 (Warning) %s is neithter a net nor a pin

DESCRIPTION

The tool cannot find neither a net nor a pin from the name specified in command line.

WHAT NEXT

Please make sure the name specified in command line is correct. For example, use get_nets or get_pins commands to check.

CTS-220 (Error) HFCTS failed

DESCRIPTION

HFCTS failed due to timing analsys failed, buffer tree construction failed or buffer tree optimization failed. Please check the log file before this message for details on which part failed.

WHAT NEXT

Check the log file before the message and fix those errors.

CTS-221 (Information) DRC violations at pin %s cannot be fixed since there is a huge pin cap at its load pin %s. (load pin cap [rise,fall] = [%f %f]; constraint [rise,fall] = [%f,%f])

DESCRIPTION

This message explains why the DRC violation at the pin cannot be fixed. When the input cap of a load pin exceeds max cap constraint, even the tool places a driving cell near by the load pin, the DRC violation still cannot be fixed.

WHAT NEXT

Ignore this message if you are sure the constraint specified in your liberaries, SDC files, set_clock_tree_options are less than the pin cap specified in your liberaries.

CTS-222 (Warning) No boundary cell insertion on dont_buffer net %s.

DESCRIPTION

When a boundary net has dont_buffer_net attribute, boundary cell insertion will not be performed on the net.

WHAT NEXT

Remove dont_buffer_net attribute on the boundary net if boundary cell needs to be inserted on the net.

CTS-223 (Warning) No boundary cell insertion on boundary net %s.

DESCRIPTION

There is no boundary cell insertion on the net because it is either a PAD net or a boundary cell has been inserted.

WHAT NEXT

CTS-224 (Warning) Distance between boundary cell %s and clock port %s is larger than three row height.

DESCRIPTION

A boundary cell may be placed away from the input port. This might be due to placement blockages near the port. In multi-voltage designs, boundary cell may be placed away from the port if default voltage area is far away from the port.

WHAT NEXT

Check for placement blockages and voltage areas near the clock port.

CTS-225 (Information) DRC violations at pin %s cannot be fixed since there is no buffer zone in region (x0=%d,y0=%d) (x1=%d,y1=%d)

DESCRIPTION

This message explains why the DRC violation at the pin cannot be fixed. When the region (given in the message) is a no buffer zone, the tool cannot place a buffer close to the load pin(s). As a result, the DRC vilations cannot be fixed.

WHAT NEXT

Remove the blockage on the region. Place the load pin on other side of the region. Relax the constraint specified in your liberaries, SDC files, set_clock_tree_options. Ignore the DRC violation.

CTS-226 (Information) DRC violations at pin %s cannot be fixed since it is connected to the dont_buffer_net %s

DESCRIPTION

This message explains why the DRC violation at the pin cannot be fixed. The tool doesn’t touch the net with dont_buffer_net

WHAT NEXT

Remove dont_buffer_net on the net. Ignore the DRC violation

CTS-227 (Information) no DRC fixing for ILM net %s

DESCRIPTION

The net shown in the message is a net inside an ILM block. The ILM block cannot be modified since it is a timing view for top level design.

WHAT NEXT

Open the cell view of ILM block and fix DRC violations using the same commands.

CTS-228 (Information) no DRC fixing for dont_buffer_net %s

DESCRIPTION

The net shown in the message is a dont_buffer_net defined by users. It cannot be modified by the tool.

WHAT NEXT

Remove dont_buffer_net on the net. Ignore the DRC violation

CTS-229 (Information) DRC violations at pin %s cannot be fixed

since it is connected to net %s inside ILM

DESCRIPTION

This message explains why the DRC violation at the pin cannot be fixed. The ILM block cannot be modified since it is a timing view for top level design.

WHAT NEXT

Open the cell view of ILM block and fix DRC violations using the same commands.

CTS-230 (Warning) Ignore cell %s since it has %d timing arcs.

DESCRIPTION

Clock tree synthesis generates this warning message for each cell in the clock tree reference list (as set by set_clock_tree_references) that have more than one timing arc from input pin to output pin.

These types of cells are typically used for multithreshold or MTCMOS designs. IC Compiler does not currently support MTCMOS scenarios.

WHAT NEXT

To disable this message, set the cts_use_multi_input_buffer variable to true before running clock tree synthesis.

CTS-231 (Warning) Ignore net %s since it has no synchronous pins.

DESCRIPTION

CTS cannot find any synchronous pin (e.g. float pin, stop pin or regular clock pin) on the net and will not synthesize this net.

WHAT NEXT

If a pin on the net should be treated as a synchronous pin, make sure it is not an implicit or explicit ignore pin.

CTS-232 (Warning) Net %s has been marked as synthesized.

DESCRIPTION

CTS found a net that has been synthesized. This message is usually found when CTS reaches an overlapping clock domain the second time. CTS also issues this warning when the net is synthesized in previous CTS session.

WHAT NEXT

Use remove_clock_tree to remove synthesized clock tree before re-synthesizing the net.

CTS-233 (Warning) Stop to insert buffers to fix DRC on net %s (current buffer levels = %d, constraint = %d).

DESCRIPTION

CTS cannot insert more buffers to fix DRC violations on the net due to buffer level constraint. The default maximum buffer level is 20, which is sufficient for most of the designs.

For blockage-dominant designs, block-mode CTS may not be able to avoid blockage with given maximum buffer level constraint. In this case, consider using top-mode CTS to build the clock tree.

Note that the constraint is automatically increased until the receiving pin with the largest phase delay has been selected for clustering.

WHAT NEXT

Find out why CTS cannot fix DRC with the given maximum buffer level constraint. Either relax the constraint or switch to top-mode CTS.

CTS-234 (Error) Root clock net %s has been marked as synthesized.

DESCRIPTION

CTS found a root clock net that has been synthesized and no clock tree for this root net will be re-built.

WHAT NEXT

Use remove_clock_tree to remove synthesized clock tree.

CTS-235 (Information) DRC violations at pin %s cannot be fixed since it is defined as dont_touch_subtree

DESCRIPTION

This message explains why the DRC violation at the pin and beyond cannot be fixed. The tool doesn’t touch any net beyond the pin with dont_touch_subtree defined.

WHAT NEXT

Remove dont_touch_subtree at the pin. Ignore the DRC violation

CTS-236 (Error) Cannot move cell %s to location (%d, %d).

DESCRIPTION

Clock tree synthesis generates this error message when it can not place a clock buffer or gate around the location (x, y).

The usual cause of this error message includes: over-utilization of chip area, floorplan which has narrow channels, voltage area caused placement blockages, and other floorplan constraints, e.g. placement bound.

WHAT NEXT

Check the cell utilization ratio, adjust floorplan if needed.

CTS-237 (error) Cannot find a legal clock reference for the boundary cell at port %s.

DESCRIPTION

This error message occurs when CTS cannot find a clock reference that is characterized for the voltage area of the specified port, and so it does not insert a boundary cell for the port.

WHAT NEXT

Add a buffer or an inverter that is characterized for the default voltage area into the boundary cell clock reference list, and run the command again.

CTS-238 (warning) The %s exception is not defined on %s.

DESCRIPTION

This warning message occurs when attempting to remove the specified exception from an object (such as a pin, cell, or net), but the exception does not exist on that object.

WHAT NEXT

Make sure that an exception is defined on the object and run the command again.

SEE ALSO

remove_clock_tree_exceptions(2)
set_clock_tree_exceptions(2)

CTS-239 (information) A new version of set_clock_tree_exceptions is enabled by default.

DESCRIPTION

This warning message occurs because the **set_clock_tree_exceptions** command is rewritten in the z2007.03-SP2 release. The new version supports float pins and stop pins with active_edge, and supports the pin exceptions precedence.

WHAT NEXT

This is an information message only. You can suppress this message to avoid seeing it in the future.

SEE ALSO

set_clock_tree_exceptions(2)

CTS-240 (warning) The %s exception is overridden by the %s

exception on %s.

DESCRIPTION

This warning message occurs when the former exception on the object is deleted and the latter exception is set. The two exceptions conflict and the latter exception has higher priority.

WHAT NEXT

This is only a warning message. No action is required.

SEE ALSO

set_clock_tree_exceptions(2)

CTS-241 (warning) Former exception %s is retained on %s, and %s exception is ignored.

DESCRIPTION

This message warns you that the specified exception is not set on the object because a former exception already exists on the object, and the former exception has a higher priority.

WHAT NEXT

This is only a warning message. No action is required.

However, if you want to set the specified exception on the object, first remove the preexisting exception using the **remove_clock_tree_exceptions** command.

SEE ALSO

remove_clock_tree_exceptions(2)
set_clock_tree_exceptions(2)

CTS-242 (warning) Some cells in the design are not legal.

DESCRIPTION

This error message occurs when the current design has floorplan or placement problems. CTS continues, but these problems may cause CTS failure, unacceptable QoR,

or QoR correlation issues.

WHAT NEXT

Run the **check_legality -verbose** command for details about the error. Correct the problems with a command such as **legalize_placement**, and then rerun the initial command.

SEE ALSO

check_legality(2)
legalize_placement(2)

CTS-243 (warning) Internal pin %s found in clock domain %s.

DESCRIPTION

This warning message occurs when CTS encounters a macro with an internal pin. CTS may not synthesize clock nets beyond the macros with internal pins.

WHAT NEXT

This is only a warning message. No action is required.

However, to ensure that the clock nets beyond a macro with internal pins are synthesized, either move the clock definition to its output pin, or create a generated clock at its output pin.

CTS-244 (Warning) dont_touch_subtree is defined at clock source %s.

DESCRIPTION

This message reminds you that the source pin/port of certain clock domain is defined as dont_touch_subtree by set_clock_tree_exceptions. Thus this clock domain will not be synthesized by CTS.

WHAT NEXT

If you want to do CTS on the clock domain rooted from this source pin/port, please remove dont_touch_subtree exception by using remove_clock_tree_exceptions first.

SEE ALSO

set_clock_tree_exceptions(2)
remove_clock_tree_exceptions(2)

CTS-245 (warning) Please specify at least one attribute or constraint to move from specified clock network.

DESCRIPTION

This warning message occurs when no option related to attribute or constraint is specified with mark_clock_tree command. So mark_clock_tree will not have any operation.

WHAT NEXT

Make sure to specify at least one attribute or constraint, such as -clock_synthesized, -clock_net, and run the command again.

SEE ALSO

mark_clock_tree(2)

CTS-246 (warning) root net %s is global routed.

DESCRIPTION

This warning message occurs before mark_clock_tree will change the routing rule or layer list on a global routed clock tree.

WHAT NEXT

This is only a warning message. No action is required.

SEE ALSO

mark_clock_tree(2)

CTS-247 (warning) root net %s is detail routed.

DESCRIPTION

This warning message occurs before mark_clock_tree will change the routing rule or layer list on a detail routed clock tree.

WHAT NEXT

This is only a warning message. No action is required.

SEE ALSO

mark_clock_tree(2)

CTS-248 (warning) Cell %s cannot be removed since it is in dont_touch hierarchy.

DESCRIPTION

If remove_clock_tree -honor_dont_touch, cells within dont_touch hierarchy will be retained.

WHAT NEXT

This is only a warning message. If you want this cell to be removed, either remove the dont_touch attribute from the logical hierarchy of this cell first or do not specify -honor_dont_touch.

SEE ALSO

remove_clock_tree(2)

CTS-250 (Information) Adding delay cell %s after driving pin %s.

DESCRIPTION

A buffer as a delay cell is added to reduce the global skew.

WHAT NEXT

If no delay insertion is desired, it can be turned off through command options.

CTS-251 (Information) Adding inverter delay cell %s after driving pin %s.

DESCRIPTION

An inverter as a delay cell is added to reduce the global skew.

WHAT NEXT

If no delay insertion is desired, it can be turned off through command options. If no inverter is disired for delay insertion, put buffers only in set_clock_tree_reference for delay insertion.

CTS-252 (Warning) Clock %s defined in multiple options with conflict.

DESCRIPTION

Optimization options or inter-clock delay balance options defined on the clock have conflicts. For example, a clock is defined in different balance group in set_inter_clock_delay_options.

WHAT NEXT

Check and correct conflicting options.

CTS-253 ICC only supports pre-route inter clock delay balance in this release.

DESCRIPTION

Command balance_inter_clock_delay finds the db is routed or partial routed, however, this command only supports pre-route stage balancing.

WHAT NEXT

Move the balancing command before nets get routed.

CTS-254 (Warning) Inter-clock delay balance failed to find a

bufferable net from source %s Clock

DESCRIPTION

Inter-clock delay balance adds buffers on root clock net or the next bufferable net from the root. This meesage means the clock tree has no bufferable net before it fanouts to multiple clock gates with clock sinks. This meesage also shows up when a clock has no clock sink.

WHAT NEXT

Check and remove dont_buffer_net on clock root net or the next few levels, or clock tree excpetions.

CTS-255 Clock %s defined in balance group not found in the design or the clock has no bufferable net or sinks.

DESCRIPTION

Clock defined in the balance group either cannot be found in the design or the clock has no bufferable net. In some cases, the clock has no sinks which leads to no bufferable net. No bufferable net here means there is no net from clock root net and down until it fanouts from multiple clock gates.

WHAT NEXT

Check and correct constraints or exceptions on the clock.

CTS-256 (Information) Offset from clock %s will not be balanced.

DESCRIPTION

During inter clock delay balance, when offset is defined, clock from is a reference clock and clock to will be balanced to clock from clock with an offset. Reference clock (from clock) will not be changed.

WHAT NEXT

If this clock needs to be balanced, use other clock as reference clock in offset definition.

SEE ALSO

set_inter_clock_delay_options(2)
balance_inter_clock_delay(2)

CTS-257 Cannot insert buffer for multiple ilm output port net %s.

DESCRIPTION

Found multiple ILM output ports on a clock net, no clock buffer insertion on such net.

WHAT NEXT

If this clock needs to be balanced, use other clock as reference clock in offset definition.

SEE ALSO

balance_inter_clock_delay(2)

CTS-258 Clock %s defined in multiple balance groups.

DESCRIPTION

A clock is found defined in multiple balance group for inter-clock delay balance.

WHAT NEXT

Correct the balance group specification.

SEE ALSO

set_inter_clock_delay_options(2)
balance_inter_clock_delay(2)

CTS-259 Clock %s in the script for inter-clock delay balance

option is not found in the design.

DESCRIPTION

Clock for inter-clock delay balance options cannot be found in the design.

WHAT NEXT

Correct the clock from specification.

SEE ALSO

set_inter_clock_delay_options(2)
balance_inter_clock_delay(2)

CTS-260 (Warning) Net %s is an Ideal Net, Removing the attribute.

DESCRIPTION

You receive this message because incoming netlist to CTS has some nets marked as Ideal.

WHAT NEXT

No action is required on your part. CTS will remove the Ideal Net attribute to ensure correct load and transition delay calculation for the given net.

CTS-261 (Warning) Cell %s is a fixed cell instance.

DESCRIPTION

You receive this message because the cell in question is marked as fixed.

WHAT NEXT

If a cell is marked as fixed, CTS optimization mainly sizing and relocation will not work on it. If you think Optimization should work on this cell please remove the is_fixed attribute from the cell.

CTS-262 (Warning) No LEQ library cell found for cell %s library cell %s.

DESCRIPTION

You receive this message because the tool cannot find a Logically Equivalent(LEQ) library cell for a given cell

WHAT NEXT

This happens sometimes when the LEQs cells in the library are marked as dont_use. CTS optimization does not find these cells available for sizing. You might want to remove the dont_use attribute on the cells in the library.

CTS-263 (Warning) invalid phase delay at pin %s.

DESCRIPTION

This debugging message tells you that the timer had difficulty calculating the phase delay at a certain pin in the clock network. This can cause clock tree synthesis to not balance the clock tree properly. This message is displayed in the log only when debug mode is on.

WHAT NEXT

Determine whether the pin has the proper timing characteristics or should be set as ignore pin, stop pin, or float pin.

CTS-264 (Error) Clock tree synthesis error, aborted.

DESCRIPTION

This message indicates that clock tree synthesis could not build a clock tree. A possible cause of this problem is an error in the clock definitions. For example, if you define the clock on an internal check pin of an ETM model, clock tree synthesis cannot build a tree and you get this message.

WHAT NEXT

Check your clock definitions and rerun clock tree synthesis.

CTS-265 (Error) Timer initialization failed.

DESCRIPTION

This message, Error: Timer initialization failed, indicates that clock tree synthesis cannot find the capacitance model TLU, TLU+, or Synopsys design constraints (SDC) in your design. If any of this information is missing in your design, clock tree synthesis will fail.

WHAT NEXT

Load the capacitance model and load SDC in your design

CTS-266 (Warning) Net % has been marked for synthesis

DESCRIPTION

This warning message indicates that the specified clock net has already been processed by clock tree synthesis. Clock tree synthesis will not process the specified clock net, but will continue to process other clock nets that have not been previously been processed. This happens in two scenarios. First, there are overlapping clock domains. Second, given net has already been synthesized by some previous run of CTS.

WHAT NEXT

If you do not want clock tree synthesis to resynthesize this clock net, use the set_clock_tree_exceptions -dont_touch_subtrees command to define this clock net as a don’t touch subtree. If you want to resynthesize this clock net, use the remove_clock_tree command to remove the clock tree on this net before running clock tree synthesis.

CTS-267 (Error) get capacitance on net %s failed.

DESCRIPTION

This message indicated that CTS was unable to calculate capacitance for a given net. The common reasons being the following: a. Net has been marked as Ideal. b. Net has high fanouts (usually > 1000) c. Net has some illegal connection (mainly open). d. Net is a logic constant. e. Net has multiple driver.

WHAT NEXT

You should check the given net for ideal net attribute or illegal connection.

CTS-268 (Warning) No delay insertion for hard configuration tree on net %s

DESCRIPTION

The mentioned clock net has a hard configuration defined in the configuration file specified with set_clock_tree_options -config_file_read. Inserting delay cells to this clock tree would conflict with the specified configuration. Clock tree optimization will not perform delay cell insertion on this net.

WHAT NEXT

If you do not want to preserve the manually specified clock tree configuration for the net remove the entry for this net from the configuration file. If you want to preserve the net configuration no action is required.

CTS-269 (warning) Buffer count (%d) specified for current buffer level on net %s is too small.

DESCRIPTION

This warning message occurs when the specified clock net has a hard configuration defined in the configuration file, and the number of buffers specified is too small. Therefore, some buffers in the current buffer level are driving more fanouts than they should, which causes DRC violations.

WHAT NEXT

Increase the buffer count for the current buffer level, or use a soft configuration for the current buffer level, and run the command again.

CTS-270 (information) Stopped growing cluster due to %s.

DESCRIPTION

This information message occurs when RC constraints are enabled using the **cts_enable_rc_constraints** switch. Clock tree synthesis stops adding a pin to a cluster if it creates maxRC or maxRCSkew constraints.

WHAT NEXT

This is only an information message. No action is required.

CTS-271 (Warning) RC delay (%f) and skew (%f) exceed target on net %s.

DESCRIPTION

When RC constraints are enabled (through cts_enable_rc_constraints switch) and a net has hard configuration, there could have maxRC violation at driving cell output.

WHAT NEXT

Consider adding extra buffer levels for the net in config file.

CTS-272 (Warning) Ignoring Clock Tree Configuration for net %s as it is marked as dont_touch, dont_buffer or ignore net.

DESCRIPTION

This message means a net has a clock tree configuration defined in configuration file. It is also marked as dont_buffer or dont_touch net. In this case CTS will ignore the configuration file for this net. This message can also appear for net which is a PAD net and hence being ignored by CTS.

WHAT NEXT

Consider removing the dont_touch or dont_buffer attribute. PAD nets will be ignored by CTS, irrespective of configuration file.

CTS-275 Clock %s defined in multiple offset option.

DESCRIPTION

A clock is found defined in multiple offset options for inter-clock delay balance.

WHAT NEXT

Correct the offset specification.

SEE ALSO

set_inter_clock_delay_options(2)
balance_inter_clock_delay(2)

CTS-276 Clock %s and its subtree can not be balanced together, exclude them for balancing.

DESCRIPTION

Inter-clock delay balance can only balance independent clocks.

WHAT NEXT

Correct the balance clock specification.

SEE ALSO

set_inter_clock_delay_options(2)
balance_inter_clock_delay(2)

CTS-277 Update Phase Delay Failed.

DESCRIPTION

Update phase delay failed, check your setup/script.

WHAT NEXT

Check design setup.

SEE ALSO

compile_clock_tree(2)
optimize_clock_tree(2)
balance_inter_clock_delay(2)

CTS-278 Cannot find any clock definition for clock tree optimization or balance.

DESCRIPTION

During clock tree optimization or inter-clock delay balance initialization, no clock is found.

WHAT NEXT

Check design setup.

SEE ALSO

optimize_clock_tree(2)
balance_inter_clock_delay(2)

CTS-279 Inter-clock delay balance cannot handle multiple fanout when it traverses to lower level net %s for balancing.

DESCRIPTION

Inter-clock delay balance cannot handle multiple fanout when it traverses to lower level net %s for balancing.

WHAT NEXT

Check root net attribute.

SEE ALSO

balance_inter_clock_delay(2)

CTS-280 (error) Wrong input for routed_clock_stage option: %s, use none, global, track or detail.

DESCRIPTION

This error message occurs when an invalid value is used for the **-routed_clock_stage** option. Accepted values for this option are **none** for preroute, and **global**, **track**, or **detail** for different stages of postroute.

WHAT NEXT

Rerun the command, specifying the value for the **-routed_clock_stage** option as either **none**, **global**, **track**, or **detail**.

See the command man page for further information.

SEE ALSO

optimize_clock_tree(2)

CTS-281 (warning) CTO delay insertion is not supported in postroute mode.

DESCRIPTION

This warning message indicates that clock tree optimization delay insertion is not performed in postroute mode. When the **-routed_clock_stage** option is specified for a postroute **optimize_clock_tree** command, only buffer sizing and gate sizing are supported.

WHAT NEXT

This is only a warning message. However, if delay insertion is the only optimization specified in the postroute stage, the tool skips the optimization. Remove delay insertion from the script for best results and to avoid this warning message.

SEE ALSO

optimize_clock_tree(2)

CTS-282 (warning) CTO buffer relocation is not supported in postroute mode.

DESCRIPTION

This warning message indicates that clock tree optimization buffer relocation is not performed in postroute mode. When the **-routed_clock_stage** option is specified for a postroute **optimize_clock_tree** command, only buffer sizing and gate sizing are supported.

WHAT NEXT

This is only a warning message. However, if buffer relocation is the only optimization specified in the postroute stage, the tool skips the optimization. Remove buffer relocation from the script for best results and to avoid this warning message.

SEE ALSO

optimize_clock_tree(2)

CTS-283 (warning) CTO gate relocation is not supported in postroute mode.

DESCRIPTION

This warning message indicates that clock tree optimization gate relocation is not performed in postroute mode. When the **-routed_clock_stage** option is specified for a postroute **optimize_clock_tree** command, only buffer sizing and gate sizing are supported.

WHAT NEXT

This is only a warning message. However, if gate relocation is the only optimization specified in the postroute stage, the tool skips the optimization. Remove gate relocation from the script for best results and to avoid this warning message.

SEE ALSO

optimize_clock_tree(2)

CTS-284 (warning) The -no_clock_eco_route and -search_repair_loop options are only valid with postroute CTO.

DESCRIPTION

This warning message advises you that the **-no_clock_eco_route** and **-search_repair_loop** options are ignored because they are only valid with postroute clock tree optimization. When the **-routed_clock_stage** option is set to **none** (the default), clock tree optimization performs only preroute optimization and ignores **-no_clock_eco_route** and **-search_repair_loop**.

WHAT NEXT

If you intended to perform preroute clock tree optimization, the ignored options have no impact on the result.

If you intended to perform postroute clock tree optimization, rerun the command, specifying the correct value for **-routed_clock_stage**.

SEE ALSO

optimize_clock_tree(2)

CTS-285 (warning) CTO is in postroute mode, but net %s is not routed.

DESCRIPTION

This warning message occurs when clock tree optimization is in postroute mode, but the specified net is not routed. No routing is performed.

WHAT NEXT

If you intended to run clock tree optimization in postroute mode with the net routed, then route the clock nets and run the command again.

If you do not want to route the clock nets, run the **optimize_clock_tree** command in preroute mode.

SEE ALSO

optimize_clock_tree(2)

CTS-286 (warning) CTO is in preroute mode, but the .ddc file is global routed.

DESCRIPTION

This warning message occurs when the **optimize_clock_tree** command is run in preroute optimization mode, but the .ddc file is (partially) global routed. No routing is performed.

WHAT NEXT

Rerun the command with the correct routing mode. See the command man page for routing mode information.

SEE ALSO

optimize_clock_tree(2)

CTS-287 (warning) CTO is in preroute mode, but the .ddc file is

(partially) detail routed.

DESCRIPTION

This warning message occurs when the **optimize_clock_tree** command is run in preroute optimization mode, but the .ddc file is (partially) detail routed. No routing is performed.

WHAT NEXT

Rerun the command with the correct routing mode. See the command man page for routing mode information.

SEE ALSO

optimize_clock_tree(2)

CTS-288 CTO is in postroute mode, but no routing is performed.

DESCRIPTION

This warning message occurs when the **optimize_clock_tree** command is in postroute optimization mode, but the .ddc file is not routed. No routing is performed.

WHAT NEXT

Rerun the command with the correct routing mode. See the command man page for routing mode information.

SEE ALSO

optimize_clock_tree(2)

CTS-289 (Information) Removing clock source latency on %s %s …

DESCRIPTION

You receive this information message because the synthesized clock is set to be propagated, and clock source latency, which is the attribute of an ideal clock, is removed.

WHAT NEXT

This is an informational message only. No action is required on your part.

CTS-290 (Warning) Clock %s is partially synthesized

DESCRIPTION

You receive this warning message because the multi-source clock is partially synthesized. The clock latency value applied to its related virtual clock may be incorrect.

WHAT NEXT

Make sure all clock nets from every source pin of the clock are synthesized correctly and rerun update_clock_latency command again.

SEE ALSO

update_clock_latency(2)
set_latency_adjustment_options(2)

CTS-291 (Warning) Cell %s has clock definition on it. It will not be sized.

DESCRIPTION

You receive this message because CTO is trying to size a cell with clock definition defined on one of its pins.

WHAT NEXT

If a cell has clock definition defined on one of its pins, Sizing cannot size this cell in Standalone CTO. If you want to size this cell you might want to remove the clock definiton.

CTS-292 (error) Wrong input for routed_clock_stage option: %s,

use none, track or detail.

DESCRIPTION

This error message occurs when an invalid value is used for the **-routed_clock_stage** option. Accepted values for this option are **none** for preroute, and **track**, or **detail** for different stages of postroute.

WHAT NEXT

Rerun the command, specifying the value for the **-routed_clock_stage** option as either **none**, **track**, or **detail**.

See the command man page for further information.

SEE ALSO

optimize_clock_tree(2)

CTS-295 Inter-clock delay balance cannot handle clock %s defined at input pin and it goes to multiple output pins.

DESCRIPTION

Inter-clock delay balance cannot handle clock %s defined at input pin and it goes to multiple output pins.

WHAT NEXT

Check clock definition.

SEE ALSO

set_inter_clock_delay_options(2)
balance_inter_clock_delay(2)

CTS-296 Cannot find a clock called %s, skipping.

DESCRIPTION

A clock is given for optimization or inter-clock delay balance, but the initialization process cannot find the clock.

WHAT NEXT

Check design setup and script.

SEE ALSO

optimize_clock_tree(2)
balance_inter_clock_delay(2)

CTS-297 Memory allocation failed in clock tree optimization or inter-clock balancing.

DESCRIPTION

Memory allocation failed in clock tree optimization or inter-clock balancing.

WHAT NEXT

Check machine environment.

SEE ALSO

optimize_clock_tree(2)
balance_inter_clock_delay(2)

CTS-298 String buffer for library cell name overflow.

DESCRIPTION

String buffer for library cell name overflow. This is not expected.

WHAT NEXT

Check error message before this.

SEE ALSO

optimize_clock_tree(2)
balance_inter_clock_delay(2)

CTS-299 No buffer/inverter’s LEQ classes in the library.

DESCRIPTION

No buffer/inverter’s LEQ classes in the library used for clock tree optimization or inter-clock delay balance.

WHAT NEXT

Check library setup.

SEE ALSO

optimize_clock_tree(2)
balance_inter_clock_delay(2)

CTS-300 (Error) Invalid CTS operating condition %s.

DESCRIPTION

This error occurs when the operating condition specified by -operating_condition option.

WHAT NEXT

Please specify one of the following options for -operating_conditions 1.min 2.max (default) 3. min_max

CTS-301 Need only one offset from clock.

DESCRIPTION

Clock from is the reference clock and only one clock can be the refernce clock.

WHAT NEXT

Correct clock from specification in the script.

SEE ALSO

set_inter_clock_delay_options(2)
balance_inter_clock_delay(2)

CTS-302 No clock from found when clock to is given for inter-clock delay balance options.

DESCRIPTION

A clock should be given as reference clock (clock from) when offset clock to is given in inter-clock delay balance options.

WHAT NEXT

Correct clock from specification in the script.

SEE ALSO

set_inter_clock_delay_options(2)
balance_inter_clock_delay(2)

CTS-310 (Error) %d coincident fanout pins at (%d,%d), including %s

DESCRIPTION

When doing clustering, all the pins (sink and hookup) are collected and sorted geometrically. The sorted list should not include multiple pins coincide on a same location. When such a condition is found, although CTS will continue, this is usually a sign of some problem in design.

WHAT NEXT

Check for connection errors in the clock net list.

CTS-311 (Warning) cell %s has inverting timing arc but is modeled as a buffer.

DESCRIPTION

Timing arc found on a cell has different logic polarity from the functional model of it.

WHAT NEXT

Check if the functional model of the cell is correct.

SEE ALSO

CTS-312(n)

CTS-312 (Warning) cell %s has non-inverting timing arc but is modeled as an inverter.

DESCRIPTION

Timing arc found on a cell has different logic polarity from the functional model of it.

WHAT NEXT

Check if the functional model of the cell is correct.

SEE ALSO

CTS-311(n)

CTS-313 (Error) Class not found <%d> for cell <%s>.

DESCRIPTION

The function of the cell is not registered as any class.

WHAT NEXT

Check the LEF library.

CTS-314 (Warning) The VA id got from plan group is invalid.

DESCRIPTION

The voltage area ID got from plan group is either smaller than 0 or larger than allowed.

WHAT NEXT

Check the voltage area setting and plan group creation/setting in the design.

CTS-315 (Error) Error found in clock net %s during clustering!

DESCRIPTION

Clustering process meets error when working on the clock net.

SEE ALSO

CTS-316(n)

CTS-316 (Error) %d clusters { bufferlevel %s} > %d pins

DESCRIPTION

During clustering, the number of cluster generated (for the given buffer level) is larger than the number of pins being generated.

SEE ALSO

CTS-315(n)

CTS-317 (Error) Found pin connection problem at buffer(%d) of level(%d)

DESCRIPTION

The given buffer at the given buffer level has problem in its output pin or output net.

CTS-318 (Warning) %s is not a buffer

DESCRIPTION

A cell used as clock buffer is found to be not a buffer cell.

CTS-319 (Warning) A clock tree defined on the don’t-touch net %s.

DESCRIPTION

A clock tree is marked as don’t touch net and CTS will skip working on the don’t touch net.

WHAT NEXT

Check the clock tree definition and definition of don’t touch net in your design.

CTS-320 (Warning) No buffer level specified for net %s.

DESCRIPTION

When loading clock tree configuration file, a clock net does not have a buffer level defined for it.

WHAT NEXT

Check the clock tree configuration file.

CTS-321 (Warning) No clock tree synthesis on the %s net (net name: %s)

DESCRIPTION

A clock net is found to be one of several net-types that cause CTS to skip synthesizing it. The possible types include: -HTV net -bi-direction net -ILM net -cts_dont_buffer_internal net -routed net

WHAT NEXT

Verify that the clock tree definition and net type are what the design intended.

CTS-350 (Error) No enabled buffers were found in the library.

Aborting.

DESCRIPTION

Clock tree optimization requires buffers or inverters for optimization. All candidate cells have been disallowed, and optimization cannot continue.

WHAT NEXT

Supply more target libraries, remove dont_use attributes from library cells, or explicitly supply a valid buffer list with set_clock_tree_references.

SEE ALSO

set_clock_tree_references (2),

CTS-351 (Warning) The cts integrated global router has not been activated. Using virtual route estimation.

DESCRIPTION

Clock tree optimization is designed to predict routing by creating actual global routes. By disabling the global router, the accuracy of skew estimation of the optimizer will be lessened.

WHAT NEXT

Turn on the integrated router by using "optimize_clock_tree -effort high".

SEE ALSO

CTS-352 (Warning) set_delay_calculation is currently set to ’elmore’. ’clock_arnoldi’ is suggested.

DESCRIPTION

Clock tree optimization will use the timing analysis engine specified by set_delay_calculation. In modern technologies, elmore delay calculation may lead to inferior accuracy in skew estimation.

WHAT NEXT

Turn on arnoldi delay calculation for the clocks by using "set_delay_calculation clock_arnoldi".

SEE ALSO

set_delay_calculation (2),

CTS-353 (Warning) Skew target %.3f ns is too high. Using %.3f ns.

DESCRIPTION

The specified skew target is ridiculously high and is probably specified with the wrong units. A more reasonable target is being assumed.

WHAT NEXT

Specify a lower target, and make sure that you use the units of the first target library.

SEE ALSO

set_clock_tree_options (2),

CTS-354 (Error) Skew target %.3f is not legal. Using %.3f ns.

DESCRIPTION

The target skew must be a positive number.

WHAT NEXT

Specify a correct target.

SEE ALSO

set_clock_tree_options (2),

CTS-355 (Warning) Skew target %.3f ns is very low for global

optimization. Using %.3f ns.

DESCRIPTION

Global clock optimization works on every cell in the tree. Very aggressive skew targets cause it to over-optimize. Your skew target will only be used in operations which work specifically on problem clock paths.

WHAT NEXT

Consider setting a higher skew target by using the -target_skew or -corner_target_skew options of set_clock_tree_options.

SEE ALSO

set_clock_tree_options (2),

CTS-356 (Warning) Max transition will cause the default target of %.3f ns to be lowered.

DESCRIPTION

By default, clock tree optimization chooses a very aggressive transition target for most nets. You have set your transition so that the target needs to be set even lower. There may be cases where optimization will be blocked by transitions that cannot be met. Degradation of skew and insertion delay may result.

WHAT NEXT

Consider setting a higher max_transition.

SEE ALSO

set_clock_tree_optimization_options (2),

CTS-357 (Warning) Max transition will override the default target of %.3f ns.

DESCRIPTION

You have chosen to loosen max_transition. This also has the effect of loosening the internal transition target of clock tree optimization. In some cases this will help

clock tree optimization achieve smaller gate areas. However, loosening max_transition too much may degrade insertion delays, skews, and immunity to noise.

WHAT NEXT

Make sure that the benefit of loosening max_transition outweighs the costs. In particular, very high max_transition is almost never worthwhile.

SEE ALSO

set_clock_tree_optimization_options (2),

CTS-358 (Warning) Cell '%s' is not legally placed and will not be optimized.

DESCRIPTION

The specified cell was not placed legally prior to clock tree optimization. Clock tree optimization will correctly optimization around the cell. But the cell itself will not be considered for sizing, relocation, splitting, or deleting.

WHAT NEXT

Try using legalize_placement prior to clock tree optimization.

SEE ALSO

legalize_placement
check_placement

CTS-359 (Warning) Cell '%s' cannot be legally moved and will not be optimized.

DESCRIPTION

The specified cell is currently placed legally, but cannot now be replaced legally near its original location. Clock tree optimization will correctly optimization around the cell. But the cell itself will not be considered for sizing, relocation, splitting, or deleting.

WHAT NEXT

Remove the restriction that keeps the cell from being moved.

SEE ALSO

legalize_placement
check_placement

CTS-360 (Warning) Library cell '%s' cannot be legally placed in this block.

DESCRIPTION

The specified library cell has no legal site in the block. The cell will not be used for optimization.

WHAT NEXT

Remove the restriction that keeps the cell from being used.

SEE ALSO

legalize_placement
check_placement

CTS-361 (Warning) Net '%s' has more than %d fanouts. Treating as ideal.

DESCRIPTION

The given net has a very large fanout. The timing of the net will be ideal, and all cells connected to the nets will be don't touched.

WHAT NEXT

The net should be buffered using compile_clock_tree or some other high-fanout synthesis.

SEE ALSO

compiler_clock_tree

CTS-362 (Warning) Library cell '%s' is not optimizable used in

voltage region ’%s’ (target_library_subset=’%s’).

DESCRIPTION

One or more cells in the given region have the given library cell. These cells are not currently optimizable in this region -- possibly because of set_target_library_subset. These cells may be relocated, but will not be sized.

WHAT NEXT

Use the check_mv_design command to get a better understanding of the library constraints within the given region.

SEE ALSO

set_target_library_subset
check_mv_design

CTS-363 (Error) Cell ’%s’ cannot be sized to ’%s’ and placed legally. Optimization will be adversely effected.

DESCRIPTION

An attempt was made to size the given cell to the given lib_cell. After sizing, the cell could not be legally placed in the block. The cell has left in its original location, without legal placement. Also the lib_cell is being marking as "dont_use" for the remainder of the optimization run.

WHAT NEXT

Resolve the issue that keeps this lib_cell from being placed. If that is not possible, you should exclude this lib_cell from the optimization run by either updating your set_clock_tree_references command or by manually setting dont_use on the lib_cell before optimization begins.

SEE ALSO

set_clock_tree_references

CTS-364 (Error) Source pin ’%s/%s’ is in the fanout of another source pin which which is being simultaneously optimized.

Optimization aborted.

DESCRIPTION

If you are trying to balance the subtrees of several clock sources against each other, one clock source may not be in the subtree of another source.

WHAT NEXT

Define clock sources which are not in each other’s fanout.

SEE ALSO

CTS-365 (Error) Library cells %s and %s have mismatched pins. Swapping will be disabled in the clock tree.

DESCRIPTION

The two clock-tree cells are not compatible and cannot be resized to one another.

WHAT NEXT

Cells must have the same number of pins to be swapped in the clock tree.

SEE ALSO

CTS-366 (Warning) Clock tree cells %s and %s have mismatched pin names.

DESCRIPTION

The two clock-tree cells have different pin names. Resizing between the two cells is handled correctly.

WHAT NEXT

Mismatched pin names are not a serious problem. But you should check the library just to make sure that the cells are actually compatible.

SEE ALSO

CTS-367 (Warning) Clock tree cells %s and %s have pins in differing order. Cells will be swapped based on pin names.

DESCRIPTION

The two clock-tree cells have different pin orders. Resizing between the two cells is allowed, based on the names of the pins. This should preserve functionality.

WHAT NEXT

Check the library to make sure that the cells are actually compatible. If the only difference between the cells is pin order, then you are OK.

SEE ALSO

CTS-368 (Error) Scenario '%s' is not defined.

DESCRIPTION

You must specify corners as "scenario:max" or "scenario:min". The scenario must be defined. You may use "default:max" or "default:min" if there are no scenarios defined.

WHAT NEXT

Define the desired scenarios or use "default".

SEE ALSO

CTS-369 (Error) Misformatted corner spec '%s'. Must be 'scenario:max' or 'scenario:min'

DESCRIPTION

You must specify corners as "scenario:max" or "scenario:min". The scenario must be defined. You may use "default:max" or "default:min" if there are no scenarios defined.

WHAT NEXT

Define the desired scenario or use "default".

SEE ALSO

CTS-370 (Information) Not optimizing corner '%s' because it has identical characteristics as '%s'.

DESCRIPTION

The two corners listed have identical process, voltage, temparature and wire chacteristics. Only one of the corners is needed. The other corner is being skipped to save redundant CPU usage.

WHAT NEXT

No action is required.

SEE ALSO

CTS-371 (Warning) 'clock_arnoldi' delay calculation will be activated during optimize_clock_tree.

DESCRIPTION

You have selected multicorner optimization for your clock tree optimization. Yet your current timing mode, by default or as selected by set_delay_calculation, is 'elmore'. Elmore delay calculation is too inaccurate for multicorner clock optimization. (And in fact, elmore delay is generally too inaccurate for *any* clock optimization in modern techologies.)

When clock optimization is performed by optimize_clock_tree, your timing mode will automatically be changed to "clock_arnoldi".

WHAT NEXT

No action is required. Resetting of the timing mode is automatic. To avoid this warning message in the future, you can manually call "set_delay_calculation clock_arnoldi" yourself.

SEE ALSO

set_delay_calculation (2),
optimize_clock_tree (2),

CTS-372 (Error) You must use set_lib_scaling_group along with your scenario definitions.

DESCRIPTION

As of the 2007.12 release, the set_lib_scaling_group command is recommended for associating libraries with the "max" and "min" corners of a scenario. Your defined scenarios require you to use set_lib_scaling_group. Failure to do so will cause incorrect timing calculation in future processing.

WHAT NEXT

Check the documentation, and then add set_lib_scaling_group to each of your scenario definitions.

SEE ALSO

set_delay_calculation (2),
optimize_clock_tree (2),

CTS-373 (Error) The corner specification '%s' is not valid. Ignoring constraint setting.

DESCRIPTION

The given corner is either improperly formatted or is not currently selected for optimization. Corner specifications must be in one of the following forms:

default:max
default:min
secanrio_name:max
scenario_name:min
RC

WHAT NEXT

Make sure you are using one of the accepted corner formats. Make sure your scenario name is spelled correctly. Make sure the corner is currently selected for optimization in the set_clock_tree_optimzation_options command.

SEE ALSO

set_clock_tree_optimization_options (2),
optimize_clock_tree (2),

CTS-374 (Error) Constraint specification '%s' is illegal.

DESCRIPTION

The given constraint specification is improperly formatted. A proper specification is of the following form:

```
    corner_specification=value
```

A corner specification has one of the following forms:

```
    default:max
    default:min
    secanrio_name:max
    scenario_name:min
RC
```

WHAT NEXT

You probably either forgot the equal sign (=) in the specification or you inserted extra spaces. You should only use spaces between contraint specifications, not with a specification. A correct example would be:

```
    "default:max=0.050 default:min=0.030"
```

An incorrect example would be:

```
    "default:max = 0.050  default:min = 0.030"
```

SEE ALSO

set_clock_tree_options (2),
optimize_clock_tree (2),

CTS-375 (Information) Float pin scale factor for the '%s' operating condition of scenario '%s' is set to %.3f

DESCRIPTION

In the given corner, float pin delay values will be scaled by the given amount. Refer to the set_clock_tree_exception man page for more details.

WHAT NEXT

This setting may have been derived automatically. If you wish to use a different value, use the set_clock_tree_exceptions command before calling optimization.

SEE ALSO

set_clock_tree_exceptions (2),
optimize_clock_tree (2),

CTS-376 (Warning) Float pin scale factor is not set for the '%s' operating condition of scenario '%s'. Skews may be inaccurate.

DESCRIPTION

When timing clocks in multiple process corners, you need to scale float pin values appropriately. Failure to do so may cause unrealistic skews to be reported.

WHAT NEXT

If you have no float pin settings, then no action is required. If you are reporting in your primary CTS corner, then the skews may be OK. Otherwise, you need scale factors. Scale values may be set manually or automatically. Refer to the set_clock_tree_exceptions man page for more deatils.

SEE ALSO

set_clock_tree_exceptions (2),
optimize_clock_tree (2),

CTS-377 (Warning) Clock tree cells %s and %s have pins in differing order. Order will be honored.

DESCRIPTION

The two clock-tree cells have different pin orders. For example, one AND gate might have pins A and B. Another might have B and A. Resizing between the two cells is allowed, and the first pin of one cell will be swapped for the first pin of the other cell. This means that the pin names will change when cell sizing occurs. The tool only allows this situation when two pins have identical function. So the functionality of your circuit will be preserved.

WHAT NEXT

Check the library to make sure that the cells are actually compatible. If the only difference between the cells is pin order, then you are OK.

SEE ALSO

CTS-378 (Error) Clock net '%s' is not legally routed or extracted. Using ideal parasitics.

DESCRIPTION

The given net is either not routed, cannot be cleanly extracted, or has user-annotated parasitics. Post-route optimization will continue, but the parasitics of this net will be estimated based on lumped or annotated values. This may cause timing inaccuracies.

WHAT NEXT

Make sure you've routed all of your clock nets. The usual command for clock routing is "route_group -all_clocks". Also, run "extract_rc" and check for warning messages such as RCEX-060 which indicate routes that are not fully connected. Also check for user annotated parasitics.

SEE ALSO

CTS-379 (Information) Primary corner '%s:max' is from the %s scenario.

DESCRIPTION

The given "primary" corner is used for querying all CTS constraints, such as clock definitions, exclude pins, stop pins, and float pins. Float pin values will be scaled for use in other corners.

The given "primary" corner is used for some operations that are not multicorner-aware. So the corner should be the worst case of all corners that you specify. This will generally be a corner with slow gates and high-resistance wires.

The primary corner is taken from the "cts scenario", if specified. Otherwise, the "current scenario" is used. If the primary corner is currently taken from the "current scenario", you may want to consider defininig a cts scenario to make sure that the selection of the primary corner is always the same.

WHAT NEXT

Make sure a worst-case corner is defined. Use set_cts_scenario to single out that case to the algorithms.

SEE ALSO

set_cts_scenario

CTS-380 (Error) Cannot process hierarchical clock source '%s' of clock '%s'.

DESCRIPTION

When a clock source is declared on a logical hierarchy port, it is required that that port be driven by a physical cell -- such as a buffer or clock gate. If the hierarchical port is undriven, it is not possible to properly process the fanout clock tree. Optimization of the tree will be skipped.

WHAT NEXT

Modify your netlist to ensure that the hierarchy port has a cell driving it.

SEE ALSO

CTS-381 (Warning) Multicorner clock tree optimization will use high effort.

DESCRIPTION

When you use set_clock_tree_optimization_options to set -enable_multicorner_optimization to any value other than "none", the value of -effort will implicitly be set to "high". Manually setting the -effort switch to another value will have no effect.

WHAT NEXT

If you want low effort clock tree optimization, you cannot use multicorner optimization.

SEE ALSO

CTS-382 (Warning) Max capacitance %f on lib_cell %s is very constraining. Your max_transition suggests that %f would be more appropriate.

DESCRIPTION

One of the outputs of the given lib_cell has a very low max_capacitance constraint. This restricts the cell from being used in situations where it could easily meet your max_transition constraint.

WHAT NEXT

Reconsider whether your max_capacitance constraint is appropriate. If not, you should patch your synthesis library.

SEE ALSO

set_cts_scenario

CTS-383 (Warning) Delta delays have not been activated for clock optization.

DESCRIPTION

When performing post-route clock tree optimization, it is desirable to take crosstalk into account. Crosstalk may cause undesired skew by inducing both "push out" and "pull in" of clock net delays. Post-route clock optimization can be used to offset this effect. Post-route optimization for crosstalk has not been activated.

WHAT NEXT

You need to activate SI delta delays. This is done with the following command:

set_si_option -delta_delay true -min_delta_delay true

SEE ALSO

set_delay_calculation
set_si_options

CTS-384 (Warning) Arnoldi delay has not been activated for clock optization.

DESCRIPTION

When performing post-route clock tree optimization, it is desirable to be as accurate as possible. Your current setting for elmore delays may lead to timing problems during signoff.

WHAT NEXT

You need to activate arnoldi delta delays. This is done with the following command:

```
set_delay_calculation -arnoldi
```

SEE ALSO

set_delay_calculation
set_si_options

CTS-385 (Warning) Min delta delay has not been activated for clock optization.

DESCRIPTION

When performing post-route clock tree optimization, it is desirable to take crosstalk into account. Crosstalk may cause undesired skew by inducing both "push out" and "pull in" of clock net delays. Post-route clock optimization can be used to offset this effect.

You are currently only optimizing for clock push out, but it is often the case that clock pull in is an even more severe effect.

WHAT NEXT

You need to activate SI delta delays for both push out and pull in. This is done with the following command:

```
set_si_option -delta_delay true -min_delta_delay true
```

SEE ALSO

set_delay_calculation
set_si_options

CTS-386 (Warning) Can only check max_length constraint when the CTS router is activated.

DESCRIPTION

The max_length constraint requires routing to be performed during CTO. If rouing is disabled, the no check is performed.

WHAT NEXT

Use high effort for optimize_clock_tree to turn on router and activate the max_length check.

SEE ALSO

optimize_clock_tree

CTS-387 (Error) Clock tree routing initialization failed.

DESCRIPTION

This error occurs when clock tree routing initialization failed in the hidden command optimize_clock_global_routing.

WHAT NEXT

CG and DB may not be in sync, or timer initialization failed. Look for CTS-265 error.

CTS-388 (Error) Clock tree routing%s failed.

DESCRIPTION

This error occurs when clock tree routing failed in the hidden command optimize_clock_global_routing. It is likely that no clock nets are specified.

WHAT NEXT

Please specify the list of clock names.

CTS-389 (Error) report net routing error: no nets specified.

DESCRIPTION

This error occurs when no clock nets or valid clock nets are specified for the hidden command lr_report_net_routing.

WHAT NEXT

Please specify the net names for reporting.

CTS-390 (Error) Report net routing error: no valid clocks specified.

DESCRIPTION

This error occurs when no valid clock nets are specified for the hidden command lr_report_clock_routing.

WHAT NEXT

Please specify the clock names for reporting.

CTS-391 (Error) Library cells %s and %s do not have a matching arc between pins '%s' and '%s'. Swapping will be disabled in the clock tree.

DESCRIPTION

The two clock-tree cells are not compatible and cannot be resized to one another.

WHAT NEXT

Cells must have matching timing arcs to be swapped in the clock tree.

SEE ALSO

CTS-400 (Warning) Top mode will be applied to all clocks.

DESCRIPTION

Top mode currently is a global setting.

WHAT NEXT

Synthesize the clocks that require top mode separately from the rest. Turn on top mode for the clocks that require top mode, and turn off top mode for the rest.

CTS-401 (Error) Could not process %s.

DESCRIPTION

This error message occurs when the arguments specified are incorrect. Either the arguments to the option do not exist or there were incorrect number of arguments given.

WHAT NEXT

Please refer to the command man page for information about the valid arguments to the option.

CTS-402 (Warning) Could not transfer wires from net %s to net %s.

DESCRIPTION

This warning message occurs when the transfer of mesh wires from sending net to receiving net fails.

WHAT NEXT

Please check whether valid sending and receiving nets have been specified.

CTS-403 (Error) Bad layer.

DESCRIPTION

This error message occurs when the layer which is specified is incorrect.

WHAT NEXT

Try get_layers to get proper layer name.

CTS-404 (Error) More than one %s specified.

DESCRIPTION

This error message occurs when the option which requires only one object(pin or net etc) is supplied with more than one object in the command.

WHAT NEXT

Please refer to the command man page for information about the valid arguments to the various options and also try object specific get* commands to get the proper objects.

CTS-405 (Error) Could not create proper premesh tree sturcture.

DESCRIPTION

This error message occurs because either the level configuration is wrong with respect to buffer grid or no appropriate buffer was found.

WHAT NEXT

Please check the configuration specified.

CTS-406 (Warning) Preferred direction for layer %s is not %s.

DESCRIPTION

Each metal, on which the routes are created, has a direction which is preferred for the routing tracks on it. The direction is either horizontal or vertical. In case the direction of the route doesn't match with the preferred direction of the metal, the routes might not be optimal or might result into some other side issues. It is advisable that the routes follow the preferred direction on a metal when created.

WHAT NEXT

Please check the preferred direction of the metal to be used for the routes.

CTS-407 (Info) Cell %s predicted move exceeds max displacement limit (%s > %s). Suppressing cell.

DESCRIPTION

When a cell needs to be added in the pre-mesh tree for the mesh , there should enough placeable area near the derived location for that cell. The location of the cell is derived mainly based on the loads' locations. However, the actual placement location depends on existence of placement blockages, cell overlapping, allowable maximum displacement etc. If there is no suitable place for the cell to be placed honoring the given maximum displacement constraint, the tool will not instantiate and place that cell.

WHAT NEXT

Please check the value of the maximum allowable displacement.

CTS-408 (Warning) %d cells were added, %d cells could not be added. Unable to connect %d buffers.

DESCRIPTION

When a cell needs to be added in the pre-mesh tree for the mesh , there should enough placeable area near the derived location for that cell and also its driver cell and load cell(s) must also be instantiated from proper libraries and placed. The location of the cell is derived mainly based on the loads' locations. However, the actual placement location depends on existence of placement blockages, cell overlapping, allowable maximum displacement etc. If there is no suitable place for the cell to be placed * or in case its driver and/or load cells are not properly

instantiated in the tree, this cell will not be connected to its driver or loads and will result into a distorted/unconnected pre-mesh tree.

WHAT NEXT

Please check the placement blockages in the floorplan, the mesh load distribution, the value of maximum allowable displacement, properly characterized library from which the cells will be instantiated.

CTS-409 (Error) No library cell defined for buffer %s.

DESCRIPTION

This error occurs when no appropriate cell is found in the given library for the particular buffer.

WHAT NEXT

Please check the target library or target library subset specified for the hierarchy in which the driver is expected. Also check and the driver name if specified or operating condition for the cell.

CTS-410 (Error) Could not annotate : No clocks found at pin '%s'.

DESCRIPTION

This error occurs when a pin on a non-clock net is encountered during timing annotation where it is expected to be on clock net.

WHAT NEXT

Please check the clock network.

CTS-411 (Warning) Please use -clock_trees instead of -root.

DESCRIPTION

This warning occurs because the option -root is no longer support in the command set_clock_tree.

WHAT NEXT

Please use -clock_trees instead of -root.

CTS-412 (Error) No cell can be added at level %d.

DESCRIPTION

This error occurs when no cells in a certain level in the tree can be added due to placement bloackage or due to the violation of maximum displacement constraint.

WHAT NEXT

Please check the floorplan to know the location of placement blockages and may try to re-plan the load distribution and/or change the constraint values that affects the placement of the buffers in the tree.

CTS-413 (Warning) Detect an invalid timing data: %s

.

DESCRIPTION

The corrupt or syntactically incorrect input file containing timing data to be used in analyze_subcircuit results in this warning condition.

WHAT NEXT

Please rectify the file contents.

CTS-414 (Error) Cannot instantiate %s object on pre-mesh tree inside the voltage area '%s'

DESCRIPTION

In multi-voltage design this error happens when the optimal hierarchy selected for the newly created object on pre-mesh tree doesn't fall inside the voltage area of the mesh loads.

WHAT NEXT

Please check the mesh loads’ hierarchies and the voltage area information.

CTS-415 (Error) Mesh loads are in different voltage areas.

DESCRIPTION

In multi-voltage design this error happens when the loads of a single mesh is spread over multiple voltage areas. For a single mesh, loads must be in the same voltage area. Even if the operating condition for the different voltage areas is same this error is reported because such a VA may be for the purpose of asynchronous switching.

WHAT NEXT

Please check the mesh loads’ positions.

CTS-416 (Error) Mesh loads are belonging to hierarchies of different operating conditions.

DESCRIPTION

In multi-voltage design this error happens when the loads of a single mesh is spread over multiple hierarchies of different operating conditions. For a single mesh, loads must be of same operating conditions.

WHAT NEXT

Please check the mesh loads’ operating conditions.

CTS-418 (Error) Bounding box narrower than vertical wire pitch, %s < %s.

DESCRIPTION

This error message occurs when the width of the bounding box specified in the command is less than the horizontal pitch. Horizontal pitch is the horizontal distance between vertical straps of the mesh.

WHAT NEXT

Please check the bounding box and the pitch value specified in the command.

CTS-419 (Error) Bounding box shorter than horizontal wire pitch, %s < %s.

DESCRIPTION

This error message occurs when the bounding box height specified in the command is less than the vertical pitch. Vertical pitch is the vertical distance between horizontal straps of the mesh.

WHAT NEXT

Please check the bounding box and the pitch value specified in the command.

CTS-420 (Error) To use -ring, must have >= 2 straps in horizontal and vertical dimensions.

DESCRIPTION

This error message occurs when you specify the "-ring" option in "create_clock_mesh" when there are less than 2 straps specified for the mesh. The -ring option puts a rectangular ring around the entire mesh. This will connect the ends of the horizontal and vertical straps. So a minimum of 2 horizontal and vertical straps is required.

WHAT NEXT

Please check the number of straps you have specified and refer to the command man page.

CTS-421 (Error) Cannot support multiple nets on load pins. The actual load net is %s,but pin %s has net %s.

DESCRIPTION

This error message occurs when the load pins are on 2 different net groups which is not supported. The mentioned pin belongs to a different net group than the specified

load net.

WHAT NEXT

Please check the load pins specified and check the command man-page.

CTS-422 (Error) Cannot use prefix %s, conflicts with %s: %s.

DESCRIPTION

This error message occurs when the name given in "-prefix" option in add_clock_drivers conflicts with the name of an existing object. The prefix should be unique.

WHAT NEXT

Please provide a valid prefix in the command.

CTS-423 (Error) Bad MW cellID on mesh net.

DESCRIPTION

This error message occurs when the milkyway cellID for the mesh-net is not does not match with the top cellID.

WHAT NEXT

Please check the mesh-net specified in the command.

CTS-424 (Error) No placeable area found for cells to be placed. Mesh creation has been aborted.

DESCRIPTION

The error occurs when placeable area is not found in the command create_clock_mesh.

WHAT NEXT

Please check the bounding box specified in the command and the placeable area available.

CTS-425 (Error) Could not write shell file '%s'.

DESCRIPTION

Command **analyze_subcircuit** could not write the above mentioned shell file. This is needed to invoke Star-RCXT.

WHAT NEXT

Check if the file already exists and if so check if you have UNIX write permissions on this file.

SEE ALSO

analyze_subcircuit

CTS-426 (Error) Failed to mark the shell-control-file '%s' executable. extraction.

DESCRIPTION

Command **analyze_subcircuit** could not "chmod +x" the above specified file.

WHAT NEXT

Check if the file already exists and if so check if you have appropriate UNIX permissions on this file.

SEE ALSO

analyze_subcircuit

CTS-427 (Error) Extractor path test failed, check '%s' and '%s', and look at your 'path' and other UNIX variables.

DESCRIPTION

Command **analyze_subcircuit** could not find Star-RCXT in the path.

WHAT NEXT

Check if Star-RCXT is in the path and can be executed.

SEE ALSO

analyze_subcircuit

CTS-428 (Error) Could not re-open the log file '%s' for reading.

DESCRIPTION

Command **analyze_subcircuit** could not re-open the log file used for testing Star-RCXT executable.

WHAT NEXT

Check if the extractor is in the path and can be executed and also check the permissions for the mentioned file.

SEE ALSO

analyze_subcircuit

CTS-429 (Error) Could not find Star-RCXT path in logfile %s.

DESCRIPTION

Command **analyze_subcircuit** could not find the Star-RCXT executable.

WHAT NEXT

Check if the extractor is in the path and can be executed.

SEE ALSO

analyze_subcircuit

CTS-430 (Error) Could not run Star-RCXT for extraction.

DESCRIPTION

Star-RCXT could not be invoked for extraction in "analyze_subcircuit". This may be due to several reasons such as permissions or else wrong executable path.

WHAT NEXT

SEE ALSO

analyze_subcircuit

CTS-431 (Error) Could not open the SPEF file %s in analyze_subcircuit.

DESCRIPTION

The above mentioned file could not be opened for read. This may be due to lack of necessary permissions.

WHAT NEXT

Please check the file path and the permissions.

SEE ALSO

analyze_subcircuit

CTS-432 (Error) Could not verify the SPEF file %s in analyze_subcircuit.

DESCRIPTION

The SPEF file could not be verified. This could be because the SPEF file is in an improper format, is unreadable or is not written properly .

WHAT NEXT

Please check whether the SPEF file is generated properly by the extractor.

SEE ALSO

analyze_subcircuit

CTS-435 (Error) Could not write Star-RCXT command file %s. Extraction will be done by "extract_rc" command instead of Star-RCXT.

DESCRIPTION

Command **analyze_subcircuit** could not write the command file needed for Star-RCXT to run. Hence analyze_subcircuit will continue with "extract_rc" command for extraction.

WHAT NEXT

Check permissions for the filename mentioned.

SEE ALSO

analyze_subcircuit

CTS-436 (Error) Could not find library path for Star-RCXT command file. Extraction will be done by "extract_rc" command instead of Star-RCXT .

DESCRIPTION

Command **analyze_subcircuit** could not find the library path to be specified for Star-RCXT command file. Hence Star-RCXT cannot be invoked and extract_rc will be used for extraction.

WHAT NEXT

Check the library path given.

SEE ALSO

analyze_subcircuit

CTS-437 (Error) Could not create Star-RCXT working directory. Extraction will be done by "extract_rc" command instead of Star-RCXT.

DESCRIPTION

Command **analyze_subcircuit** could not create the working directory for Star-RCXT. Extract_rc will be used for extraction.

WHAT NEXT

Check the permissions to create the working directory.

SEE ALSO

analyze_subcircuit

CTS-438 (Error) Could not save the milkyway cell to be used by Star-RCXT. Extraction will be done by "extract_rc" command instead of Star-RCXT.

DESCRIPTION

Command **analyze_subcircuit** could not save milkyway cell to be used by Star-RCXT. So Star-RCXT cannot be invoked and hence "extract_rc" command will be used for extraction.

WHAT NEXT

SEE ALSO

analyze_subcircuit

CTS-439 (Warning) Bounding_box is not a subset of placeable area.

DESCRIPTION

This warning message occurs when the bounding box specified in "create_clock_mesh"

command is not contained within a placeable area.

WHAT NEXT

Please check the bounding box specified for the command and refer to command man-page.

CTS-440 (Error) The location assigned to cell %s is not in VA.

DESCRIPTION

This Error message occurs when the mentioned cell is not found to be within the legal voltage area.

WHAT NEXT

CTS-441 (Error) Bad simulator name '%s' specified.

DESCRIPTION

The simulator name mentioned is invalid in command **analyze_subcircuit**.

WHAT NEXT

Check the simulator name specified.

SEE ALSO

analyze_subcircuit

CTS-442 (Error) Could not rename SPEF file generated based on the name of the scenario for scenario : %s.

DESCRIPTION

The command **analyze_subcircuit** cannot rename the SPEF file generated based on the name of the scenario in case of multiple active scenarios. This maybe because you dont have the write permissions for the directory or the SPEF file was not generated.

WHAT NEXT

Check the extractor log files to check if extraction was successful and check the permissions.

SEE ALSO

analyze_subcircuit

CTS-443 (Error) Could not set %s as current scenario in command **analyze_subcircuit**.

DESCRIPTION

The command **analyze_subcircuit** cannot set the above mentioned scenario as current scenario.

WHAT NEXT

Check if the scenario exists and is active..

SEE ALSO

current_scenario

CTS-444 (Error) Could not duplicate cell instance to drive the float pins.

DESCRIPTION

This error occurs in split_clock_net when -isolate_float_pins option is specified and the command fails to duplicate the cell instance to drive the separated float pins.

WHAT NEXT

CTS-445 (Error) The spice subcircuit model not found in case of

scenario %s.

DESCRIPTION

This Error message occurs when the command analyze_subcircuit does not find the spice subcircuit models for the above mentioned scenario. This maybe because proper subcircuit files were not specified in the -config option.

WHAT NEXT

CTS-446 (Error) No wires found for net %s on pin %s.

DESCRIPTION

This error occurs when analyze_subcircuit command finds a net which is not routed. The command expects a routed clock circuit which is to be simulated.

WHAT NEXT

Check if the routing was run properly on this net.

CTS-447 (Error) Could not find spice model for lib %s.

DESCRIPTION

This error occurs when analyze_subcircuit command is unable to find the SPICE model for the given library cell.

WHAT NEXT

Check if the proper SPICE settings are specified for the command.

CTS-448 (Error) Command should be run with the -premesh option only after analyze_subcircuit annotates the delay on the isolation buffer.

DESCRIPTION

This error occurs when adjust_premesh_connection command is run with the -premesh

option before running the analyze_subcircuit. A correct phase delay needs to be annotated on the isolation buffer for the command to optimize the clock path for skew.

WHAT NEXT

Check if the command analyze_subcircuit was run successfully before invoking this command, or if the analyze_subcircuit was run from the output pin of the isolation buffer.

CTS-449 (Error) More than one untied input for cell %s.

DESCRIPTION

This error occurs when analyze_subcircuit command when the tool finds that more than one input pin of a multi input cell is untied. For the multi input cells the pins other than the clock pin need to be tied either high or low for the clock to propagate. If this is not done then the simulation will fail.

WHAT NEXT

Check if the non clock pins of the multi input gates are sensitized properly.

CTS-450 (Warning) Incorrect circuit structure found for pin %s.

DESCRIPTION

This error occurs when analyze_subcircuit command finds a incorrect circuit structuure in design. It may occur if multi input gates have untied input pins.

WHAT NEXT

Check if the connectivity of the pins is proper.

CTS-451 (Warning) Negative cell delay %f found for pin %s. It will be ignored.

DESCRIPTION

This warning occurs when analyze_subcircuit command finds a negative cell delay for the cell mentioned. Typically the related cell resides in the last level of the

premesh tree. It might happen for the cases when the premesh skew is large. In that case, at the output pin of the cell on a faster path, clock reaches earlier compared the output pins of some other mesh drivers on the slower paths. Since those output pins are shorted by the clock-mesh net, the output pins of the slower drivers might see the clock signal earlier than the input pins of the corresponding drivers see the clock. This causes analysize_subcircuit to see the negative delay on those slower cells. This is called short-circuit effect of clock-mesh. The command ignores this negative delay and continues.

WHAT NEXT

Check if the premesh skew is too large. Try to minimize the premesh skew. Delay cells can be added on the paths which results in faster arrival of the clock.

CTS-452 (Warning) Net %s is not of clock type.

DESCRIPTION

This warning occurs when the specified net is not of type clock. The command requires a clock net to be specified.

WHAT NEXT

Check if the net specified is a valid clock net and the clock type attribute is set on it.

CTS-453 (Error) Bad timing values in simulation output file. %d lines had proper measurement values and %d had zero timing value.

DESCRIPTION

This error occurs when the simulation output file has too many lines with zero timing values. This may have occured because of improper circuit. Hence some part of the circuit was not triggered during simulation. The various reasons for this may be : a. SPICE models may be incorrect (such as missing VDD or VSS). b. There may be disconnects in the circuit. c. It may have happened that starting from the root and moving towards the loads the clock pulse got progressively narrower at each stage and by the time clock reached the mesh it was not transitioning. Insufficient number of buffer levels in the premesh tree may be the reason. d. The mesh may not be capable of driving the loads.

WHAT NEXT

1. Check if the circuit is fully connected and the SPICE models specified have all the pins included. 2. Check if enough levels of buffers were put so that the transition time can be within constraints. Try increasing the clock period. 3. If premesh is unable to drive the mesh then try constructing a logic level balanced tree or a tree with proper drive capability. 4. Add appropriate number of cells below the mesh so that the clock propagates properly. 5. Appropriate mesh loads and mesh drivers can be added.

CTS-455 (Error) Could not find the given clock %s for clock-mesh analysis.

DESCRIPTION

This error occurs when the clock mesh analyzer doesn’t find the given clock for the circuit to be analyzed.

WHAT NEXT

Please ensure that the given clock is correct.

CTS-456 (Error) Exactly one clock should be specified for the mesh analysis.

DESCRIPTION

This error occurs when multiple clocks are given for one clock-mesh analysis.

WHAT NEXT

Specify only one valid clock.

CTS-460 (Error) The -max_rc_delay_constraint option cannot be used together with -max_rc_scale_factor.

DESCRIPTION

Both options can turn on the maximum RC delay constraint. The -max_rc_delay_constraint option directly sets a maximum RC delay in the main library

unit, while the -max_rc_scale_factor option specifies a scale factor, which multiplied by an internal derived RC delay gives the maximum RC delay constraint.

WHAT NEXT

Choose the one which fits the design and re-apply the constraint again.

CTS-461 (Error) User max_rc_scale_factor (%f) is too small.

DESCRIPTION

The -max_rc_scale_factor option turns on the maximum RC delay constraint by setting a scale factor, which multiplied by an internal derived RC delay gives the maximum RC delay constraint. A small scale factor (< 0.1) can bring the constraint out of the appropriate range.

WHAT NEXT

Adjust the scale factor and re-apply the constraint again.

CTS-462 (Error) User max_rc_delay_constraint (%f ps) is too small.

DESCRIPTION

Set_clock_tree_options assumes that the given constraint values are in main library units. The error is usually arised when the main library unit is smaller than that is assumed.

WHAT NEXT

Convert the constraint values into main library units and re-apply constraints again.

CTS-463 (Error) Could not get source for clock %s.

DESCRIPTION

This error occurs when the source for the given clock could not be found.

WHAT NEXT

Check if the clock definition is proper.

CTS-464 (Error) Could not delete route for net %s.

DESCRIPTION

This error occurs when the command remove_clock_mesh could not remove all the routes of the premesh tree.

WHAT NEXT

Check if the command inputs are correct and also that the nets are properly routed.

CTS-465 (Error) First level premesh tree buffers are in different hierarchies.

DESCRIPTION

This error occurs when the command remove_clock_mesh finds that the first level cells of the premesh tree are in different hierarchies. Such a structure may give incorrect connectivity after remove_clock_mesh. Hence command returns.

WHAT NEXT

Check if the circuit structure has been properly build.

CTS-466 (Error) Premesh tree or the clock mesh has not been removed, aborting postmesh removal.

DESCRIPTION

This error occurs when the command remove_clock_mesh is run with -postmesh option before the premesh tree and the clockmesh both have been removed. For the -postmesh to work both premesh tree and clock mesh need to be removed.

WHAT NEXT

Run remove_clock_mesh to remove the premesh tree and clock mesh and then try

postmesh removal.

CTS-467 (Warning) Multiple use of -trans_wires_from. Will be ignored.

DESCRIPTION

This warning occurs when -transfer_wires_from is specified multiple times. It should be specified for the last level. The option specified in other levels will be ignored.

WHAT NEXT

Check the -transfer_wires_from usage.

CTS-468 (Warning) Tech problem. Could not find steps for hor layer %d.

DESCRIPTION

This warning occurs in create_clock_mesh command when the tool cannot find steps for the mentioned layer when the -no_snap option is specified.

WHAT NEXT

Check if proper layer has been specified and also check the command man page.

CTS-469 (Error) Could not perform %s. Aborting command.

DESCRIPTION

This warning occurs in the command because the mentioned operation dcould not be performed. Check the log files for more details about why the failure occured.

WHAT NEXT

Check if proper arguments are given to the command.

CTS-470 (Warning) The output pin of cell instance %s is an open pin.

DESCRIPTION

This warning occurs in when the tool finds a cell which has an open output pin.

WHAT NEXT

Check the connectivity in the design.

CTS-471 (Warning) Cell %s has multiple output pins.

DESCRIPTION

This warning occurs in when the command finds a cell which has more than one output pins.

WHAT NEXT

CTS-472 (Error) Net %s is an ideal net. Cannot proceed with extraction.

DESCRIPTION

This error occurs when the command finds that one of the nets is an ideal net. Extraction canot be done on an ideal net.

WHAT NEXT

Please check why the ideal net attribute is there and whether it can be removed.

CTS-473 (Warning) no clock tree synthesis on the HTV net %s.

DESCRIPTION

Tool would not do clock tree synthesis on the HTV net, for it can not insert buffers or inverts on HTV net. This is only a warning message.

WHAT NEXT

Check this HTV net.

CTS-474 (Error) Clock tree initialization failed.

DESCRIPTION

This error indicates that the clock tree synthesis could not initialize. This may be because the tool did not find the appropriate clock root.

WHAT NEXT

CTS-475 (Error) The given input pins and load pins do not belong to the same clock.

DESCRIPTION

This error indicates that the inputs and loads provided to the command do not belong to the same clock and hence the command could not proceed.

WHAT NEXT

Check if the input pins and load pins specified are proper. Also refer to the command man page.

CTS-476 (Error) The clock %s has multiple sources or logical ports associated wit it.

DESCRIPTION

This error indicates that the clock the command is operating on has multiple clock root or sources. This situation is not supported in the clock mesh flow.

WHAT NEXT

Check if the clock given is proper.

CTS-501 (Error) Invalid usage of command set_latency_adjustment_options.

DESCRIPTION

This error occurs when none of the options are specified : -from_clock, -latency, -exclude_clock

WHAT NEXT

Please specify one of the options : -from_clock, -latency, -exclude_clock

CTS-502 (Error) Invalid usage of command set_latency_adjustment_options. The -latency option must be accompanied by the -to_clock option.

DESCRIPTION

Please note that the -latency option must be accompanied by the -to_clock option.

WHAT NEXT

Please use the -to_clock option together with the -latency option.

CTS-503 (Error) Invalid usage of command set_latency_adjustment_options. -from_clock %s must be a real clock, cannot be a virtual clock.

DESCRIPTION

The clock specified in the -from_clock option of the command must be a real clock

WHAT NEXT

Please make sure that the clock specified in the -from_clock option is a real clock.

CTS-504 (Error) Invalid usage of command

set_latency_adjustment_options. -from_clock cannot be accompanied by -latency option.

DESCRIPTION

Please note that the -from_clock option cannot be accompanied by the -latency option.

WHAT NEXT

Please remove the -latency option if you want to use the -from_clock option.

CTS-505 (Error) Invalid usage of command set_latency_adjustment_options. -from_clock must be accompanied by -to_clock option.

DESCRIPTION

Please note that the -from_clock option must be accompanied by the -to_clock option.

WHAT NEXT

Please add the -to_clock option if you want to use the -from_clock option.

CTS-506 (Error) Invalid usage of command set_latency_adjustment_options. Clock %s cannot be in the -from_clock option and also in the -exclude_clock list at the same time.

DESCRIPTION

There is a conflicting specification on a clock.

WHAT NEXT

Please remove the affected clock from either -from_clock or the -exclude_clock list.

CTS-507 (Warning) Clock %s is set to be propagated. The timing analysis will ignore the latency values set on the clock object and affect I/O paths.

DESCRIPTION

If a clock is propagated, the **report_timing** command will ignore the latency value set on this clock object, and then cause problems for I/O paths because the I/O timing is modeled as regard to an associated clock object.

WHAT NEXT

Please use remove_propagated_clock to delete propagated attribute on the clock.

SEE ALSO

set_clock_latency(2)
update_clock_latency(2)
set_propagated_clock(2)
remove_propagated_clock(2)

CTS-510 (Warning) -latency was set for clock %s. Using -from_clock will override the previous setting.

DESCRIPTION

WHAT NEXT

CTS-511 (Warning) -from_clock was set for clock %s. Using -latency will override the previous setting.

DESCRIPTION

WHAT NEXT

CTS-512 (Warning) -from_clock was set for clock %s. Using -

from_clock again will override the previous setting.

DESCRIPTION

WHAT NEXT

CTS-513 (Warning) -latency was set for clock %s. Using -latency again will override the previous setting.

DESCRIPTION

WHAT NEXT

CTS-520 (Error) -from_clock %s is not synthesized.

DESCRIPTION

WHAT NEXT

CTS-521 (Warning) clock %s is not synthesized.

DESCRIPTION

WHAT NEXT

CTS-530 (Information) Latency computed from clock %s will be

applied on clock %s.

DESCRIPTION

WHAT NEXT

CTS-531 (Information) Updating the latency of clock %s to %f (max) %f (min).

DESCRIPTION

WHAT NEXT

CTS-532 (Information) Latency of clock %s has not been changed.

DESCRIPTION

The latency of the clock is not updated by update_clock_latency. Possible scenarios include: 1) the clock is excluded from update 2) cannot find its from clock 3) its from clock is not synthesized

WHAT NEXT

CTS-533 (Information) Updating the latency of clock %s to %.6f based on user-specified latency.

DESCRIPTION

The user-specified latency (by previous set_latency_adjustment_options -latency) was applied to the clock.

WHAT NEXT

CTS-534 (Warning) Clock %s does not have any boundary register related to %s. Using full boundary register set to update %s's network latency.

DESCRIPTION

update_clock_latency cannot find any boundary register driven by from-clock related to virtual clock to-clock, so it will use the full boundary register set of from-clock to update to-clock's network latency&.

WHAT NEXT

This is only a warning message&. Check the correct relation beteen from-clock and to-clock&. Then use set_latency_adjustment_options to update the relation if necessary&.

SEE ALSO

update_clock_latency(2), set_latency_adjustment_options(2)

CTS-535 (Warning) Clock %s does not drive any boundary register. Using full fanout set to update %s's network latency.

DESCRIPTION

update_clock_latency cannot find any boundary register driven by from-clock, so it will use the full fanout register set of from-clock to update to-clock's network latency&.

WHAT NEXT

This is only a warning message&. Check the correct relation beteen from-clock and to-clock&. Then use set_latency_adjustment_options to update the relation if necessary&.

SEE ALSO

update_clock_latency(2), set_latency_adjustment_options(2)

CTS-536 (Warning) user speficified a positive float pin delays but negative logic level on the pin %s. The logic level assignment will be ignored.

DESCRIPTION

An inconsistent assignment of set_clock_tree_exceptions -float_pins command has been found. The delays of the float pin are positive but the logic level is a negative value, so the logic level assignment will be ignored.

WHAT NEXT

This is only a warning message&. Please check the set_clock_tree_exceptions -float_pins command on this pin and fix the conflict between delays and logic level.

SEE ALSO

set_clock_tree_exceptions(2)

CTS-538 (Information) Update clock latency for scenario %s.

DESCRIPTION

WHAT NEXT

CTS-540 (Warning) Turning off -logic_level_balance since is not compatible with -top_mode.

DESCRIPTION

Top mode algorithm does not honor level balancing constraint.

WHAT NEXT

Use either -top_mode or -logic_level_balance for clock tree synthesis.

CTS-541 (Warning) Turning off -delay_insertion since it is not

compatible with -logic_level_balance true.

DESCRIPTION

Delay insertion will create unbalanced clock tree and needs to be turned off.

WHAT NEXT

Some unbalanced clock structures require delay insertion to achieve good QoR. If the final QoR is not within the target, consider re-synthesize the clock tree with delay insertion turned on and logic level balance turned off.

CTS-542 (Warning) Logic level difference among clock paths is large (%d).

DESCRIPTION

The clock paths from current net have very different logic levels. For example, there may be many gate levels on one clock path but no gates on another clock path. It is also possible that one subtree is significantly larger than others. Logic level balance is not suitable for these designs.

WHAT NEXT

Use regular CTS to synthesize this clock net, or refine the initial clock tree structure and re-synthesize this clock net.

CTS-543 (Warning) Level balance violation, (maxLevel, minLevel) = (%d, %d), on don’t touch subtree of pin (%s).

DESCRIPTION

The don’t touch subtree defined at the given pin is not level balanced.

WHAT NEXT

CTS cannot fix level balance violations in don’t touch subtrees. It will use the maximum logic level of the don’t touch subtree to build the rest of the clock tree.

CTS-544 (Warning) Clock tree (%s) does not have complete

logic level information.

DESCRIPTION

Some of the float pins / subtrees contain logic level information while others don’t.

WHAT NEXT

Define logic level on all float pins and re-run CTS.

CTS-545 (Warning) Top buffer level converged to clock tree driver prematurely.

DESCRIPTION

CTS stops building buffer levels when all buffers have been placed near clock tree driver. CTS might not be able to improve skew or fix DRC at the driver output.

WHAT NEXT

Check the design and CTS constraints if QoR is not within target.

CTS-546 (Warning) Skew among same logic level pins is large.

DESCRIPTION

When pins with same logic level have large skew, CTS might not be able to compensate the skew.

WHAT NEXT

This is likely caused by unbalanced initial clock tree structure or because difference on number of gate levels for two clock paths is large. Try to create a more balanced initial clock tree for CTS.

CTS-547 (Warning) On net (%s), ratio of sink pins among

subtrees is too large (> %d).

DESCRIPTION

When subtrees are disproportional in size, CTS might not be able to achieve good skew under level balance constraint.

WHAT NEXT

Try to create a more balanced initial clock tree for CTS, or turn off logic level balance.

CTS-548 (Warning) Logic level balance mode will be applied to all clocks.

DESCRIPTION

Logic level balance mode currently is a global setting.

WHAT NEXT

Synthesize the clocks that require logic level balance separately from the rest. Turn on logic level balance for the clocks that require logic level balance, and turn off logic level balance for the rest.

CTS-549 (Warning) Turning off -logic_level_balance since is not compatible with -config_file_read.

DESCRIPTION

Logic level balance CTS does not support -config_file_read.

WHAT NEXT

Use either -config_file_read or -logic_level_balance for clock tree synthesis.

CTS-550 (Warning) Turning off -insert_boundary_cell since is

not compatible with -config_file_read.

DESCRIPTION

Boundary cell insertion is not compatible with -config_file_read.

WHAT NEXT

Use either -config_file_read or -insert_boundary_cell for clock tree synthesis.

CTS-551 (Warning) There is a clock called %s and a net called %s that is not a root net of clock %s. CTS will synthesize clock %s.

DESCRIPTION

The specified clock object name corresponds to a clock name and a net name. In addition, the net is not the root net for the clock. In this case, CTS will synthesize the clock instead of the net.

WHAT NEXT

To force CTS to synthesize the net instead of the clock, specify the driving pin of the net with -clock_trees option.

CTS-552 (Error) Skipping net %s because it does not have a driver.

DESCRIPTION

CTS cannot synthesize a clock tree for a net that does not have a driver.

WHAT NEXT

Check the connectivity of the net.

CTS-553 (Error) Cannot find clock object called %s, skipping...

DESCRIPTION

There is no clock domain, clock net, or clock pin with the given name in current design.

WHAT NEXT

Find the correct clock object name and re-run CTS. You can report all the clocks in your design using the command report_clocks.

CTS-554 (Error) Skipping pin %s because it is a hierarchical port.

DESCRIPTION

CTS does not support clocks defined on hierarchical ports. This is because hierarchical ports do not have physical location that is required for calculating clock timing values.

WHAT NEXT

Move the clock definition to a physical pin or port and re-run CTS.

CTS-555 (Error) Skipping pin %s because it is not on clock network.

DESCRIPTION

The pin or the driving pin of the given net is outside clock network, or it does not drive any clock sinks. The latter can happen when there are set_case_analysis or set_disable_timing at the fanout cone of the pin. This is because set_case_analysis or set_disable_timing may cause the clock sinks in the fanout cone to be disconnected in the timing graph, causing the pin to become an implicit ignore pin.

WHAT NEXT

Check to see if there are set_case_analysis or set_disable_timing settings in the fanout cone of the output pin. If there are, make sure they are intended for CTS. Otherwise, specify a pin or a net within clock network and re-run CTS.

CTS-556 (Error) Skipping open pin %s.

DESCRIPTION

The pin or the driving pin of the given net is an open pin.

WHAT NEXT

Fix the pin connectivity problem and re-run CTS.

CTS-557 (Error) Skipping pin %s because its output net %s is inside ILM.

DESCRIPTION

CTS does not support clock defined inside ILM.

WHAT NEXT

Move the clock definition to the outside of ILM and re-run CTS.

CTS-558 (Warning) Skipping output pin %s (from pin %s) because it is not on clock network.

DESCRIPTION

When a clock is defined on the input pin of a clock gate, CTS will iterate through all the output pins of the clock gate to find root clock nets. This message indicates that the output pin does not drive any clock sinks, which is normal for multiple-output gates with some output pins driving data network. It is best to check whether there are set_case_analysis at the fanout cone of the output pin. This is because set_case_analysis may cause the clock sinks in the fanout cone to be disconnected in the timing graph, causing the output pin to become an implicit ignore pin.

WHAT NEXT

Check to see if there are set_case_analysis settings in the fanout cone of the output pin. If there are, make sure they are intended for CTS.

CTS-559 (Warning) Skipping output net %s of pin %s because it is inside ILM.

DESCRIPTION

When a clock is defined on the input pin of a clock gate, CTS will iterate through all the output pins of the clock gate to find root clock nets. CTS will skip the output nets that are inside ILM.

WHAT NEXT

CTS-560 (Warning) Skipping output pin %s (from pin %s) because it is open.

DESCRIPTION

When a clock is defined on the input pin of a clock gate, CTS will iterate through all the output pins of the clock gate to find root clock nets. This message indicates that the output pin is open, which is normal for multiple-output gates with some dangling output pins.

WHAT NEXT

Check to see if the connectivity of the output pin is broken unintentionally.

CTS-561 (Error) Skipping pin %s because there is no valid clock net for CTS to work on at its fanout cone.

DESCRIPTION

When a clock is defined on the input pin of a clock gate, CTS will iterate through all the output pins of the clock gate to find root clock nets. This message indicates that all the output nets of the clock gate are not valid root clock net.

A clock defined on an internal pin of a macro will also trigger this message because CTS currently does not go through macros with internal pins. In this case, consider moving the clock definition to the output pin of the macro, or create a generated clock at the output pin of the macro.

WHAT NEXT

Exclude this clock from CTS if there is no clock net for CTS to work on.

CTS-562 (Warning) Cell %s is not an ICG cell, Skipping...

DESCRIPTION

Since the cell is not an ICG, it will not be duplicated in split_clock_net. In order not to skip ICG cloning, user can set cts_split_any_gate as true.

WHAT NEXT

The cell wont be cloned.

CTS-563 (Warning) Cell %s is not an ICG cell, split anyway.

DESCRIPTION

When cts_split_any_gate is set to trun, a non-ICG cell can be cloned in split_clock_net.

WHAT NEXT

The cell will be cloned.

CTS-564 (Warning) No clock gates to duplicate.

DESCRIPTION

This warning occurs when there no clock gates that can be duplicated are found from the object list specified for the split_clock_net command.

WHAT NEXT

This is only a warning message.

Please double-check if there are any clock tree exceptions defined on the specified nets or cells in the object list.

SEE ALSO

split_clock_net(2)

CTS-565 (Warning) Skip cell instance %s since it is a macro.

DESCRIPTION

Skip to clone the instance in split_clock_net since it is a macro.

WHAT NEXT

The cell wont be cloned.

CTS-566 (Warning) Skip cell instance %s since it is a pad.

DESCRIPTION

Skip to clone the instance in split_clock_net since it is a pad.

WHAT NEXT

The cell wont be cloned.

CTS-567 (Warning) Boundary cell insertion will be applied on all clocks.

DESCRIPTION

Boundary cell insertion currently is a global setting.

WHAT NEXT

Synthesize the clocks that require boundary cell insertion separately from the rest. Turn on -insert_boundary_cell for the clocks that require boundary cell, and turn off -insert_boundary_cell for the rest.

CTS-568 (Warning) Input pin(s) of cell instance %s has ignore/

float/stop exception specified.

DESCRIPTION

Input pin(s) of cell instance %s has ignore/float/stop exception specified.

WHAT NEXT

N/A.

CTS-569 (Warning) Skip cell instance %s since its input pin has don_touch_subtree attribute.

DESCRIPTION

Skip to clone the instance in split_clock_net since its input pin has don_touch_subtree attribute.

WHAT NEXT

The cell wont be cloned.

CTS-570 (Warning) Skip cell instance %s since its output pin has don_touch_subtree attribute.

DESCRIPTION

Skip to clone the instance in split_clock_net since its output pin has don_touch_subtree attribute.

WHAT NEXT

The cell wont be cloned.

CTS-571 (Warning) Skip cell instance %s since its pin has clock

source definition.

DESCRIPTION

Skip cell instance %s since its pin has clock source definition.

WHAT NEXT

The cell wont be cloned.

CTS-572 (Warning) Net %s is a MVDD dont touch net.

DESCRIPTION

Net %s is a MVDD dont touch net.

WHAT NEXT

N/A.

CTS-573 (Warning) Input pin(s) of cell instance %s has non-stop exception specified.

DESCRIPTION

Input pin(s) of cell instance %s has non-stop exception specified.

WHAT NEXT

N/A.

CTS-574 (Warning) Input net of cell instance %s has dont_buffer_net specified.

DESCRIPTION

Input net of cell instance %s has dont_buffer_net specified.

WHAT NEXT

The cell wont be cloned.

CTS-575 (Warning) Output net of cell instance %s has dont_buffer_net specified.

DESCRIPTION

Input pin(s) of cell instance %s has dont_buffer_net specified.

WHAT NEXT

The cell wont be cloned.

CTS-576 (Warning) Cell %s has dont_size_cell specified.

DESCRIPTION

Cell %s has dont_size_cell specified.

WHAT NEXT

N/A

CTS-577 (Warning) Pin %s has multicycle paths constraint specified.

DESCRIPTION

Pin %s has multicycle paths constraint specified.

WHAT NEXT

N/A

CTS-578 (Warning) Pin %s has min_delay or max_delay

constraint specified.

DESCRIPTION

Pin %s has min_delay or max_delay constraint specified.

WHAT NEXT

N/A

CTS-579 (Warning) Pin %s has false_path constraint specified.

DESCRIPTION

Pin %s has false_path constraint specified.

WHAT NEXT

N/A

CTS-580 (Warning) Pin %s has clock latency constraint specified.

DESCRIPTION

Pin %s has clock latency constraint specified.

WHAT NEXT

N/A

CTS-581 (Warning) Cell %s has size_only_cell specified.

DESCRIPTION

Cell %s has size_only_cell specified.

WHAT NEXT

The cell wont be cloned.

CTS-582 (Warning) cell %s cannot be removed since it has size_only_cell specified.

DESCRIPTION

Cell %s cannot be removed since it has size_only_cell specified.

WHAT NEXT

N/A

CTS-587 (Warning) ILM %s of port %s was created by ICC with version earlier than 2007.03-SP1.

DESCRIPTION

The ILM was created using an ICC with version earlier than 2007.03-SP1. The options that were used to create the ILM were not stored in the database. CTS may see incorrect clock timing at the port if the ILM was not created with -keep_full_clock_tree option.

WHAT NEXT

Make sure the ILM is created with -keep_full_clock_tree option or re-create ILM with -keep_full_clock_tree option.

SEE ALSO

CTS-588 (n).

CTS-589 (Warning) Boundary cell insertion will be applied on all

clocks.

DESCRIPTION

Boundary cell insertion currently is a global setting.

WHAT NEXT

Synthesize the clocks that require boundary cell insertion separately from the rest. Turn on -insert_boundary_cell for the clocks that require boundary cell, and turn off -insert_boundary_cell for the rest.

CTS-590 (Information) Inserted a guide buffer %s for ILM input port %s.

DESCRIPTION

CTS inserts a guide buffer to isolate the ILM input port from top-level clock tree. CTS will not insert any buffer between the guide buffer and the ILM port, but may size or relocate the guide buffer to improve QoR.

WHAT NEXT

This is an informational message only. No action is required.

CTS-591 (Information) Inserted a guide buffer %s for ILM output port %s.

DESCRIPTION

CTS inserts a guide buffer to isolate the ILM output port from top-level clock tree. CTS will not insert any buffer between the guide buffer and the ILM port, but may size or relocate the guide buffer to improve QoR.

WHAT NEXT

This is an informational message only. No action is required.

CTS-592 (Error) Config file entry for ILM boundary net %s found.

DESCRIPTION

CTS inserts guide buffers on ILM boundary nets to isolate ILMs from top-level clock tree. If the boundary net goes into an ILM, its config file entry should not contain ILM port or pins inside ILM. If the boundary net goes out of an ILM, the config file entry will become invalid because the net name will change after guide buffer insertion.

WHAT NEXT

If the boundary net goes into an ILM, make sure the config file entry does not contain ILM port or pins inside ILM. If the boundary net goes out of an ILM, remove the config file entry before CTS.

CTS-593 (Error) Cannot insert a guide buffer for ILM input port %s.

DESCRIPTION

CTS fails to insert a guide buffer to isolate the ILM input port from top-level clock tree. Possible scenarios include:

1) The ILM port is driven by a level shifter and the output net of a level shifter is not bufferable. 2) There is cts_dont_buffer attribute on the ILM boundary net. 3) The ILM port is directly driven by another macro or abutted ILM port. 4) The ILM is inside another ILM.

Note that CTS might still be able to synthesize top-level clock tree correctly.

WHAT NEXT

Check to see if the ILM boundary net is synthesized by CTS correctly.

CTS-594 (Error) Cannot insert a guide buffer for ILM output port %s.

DESCRIPTION

CTS fails to insert a guide buffer to isolate the ILM output port from top-level clock tree. Possible scenarios include:

1) There is cts_dont_buffer attribute on the ILM boundary net. 2) The ILM port is directly driving another macro or abutted ILM port. 3) The ILM is inside another ILM.

Note that CTS might still be able to synthesize top-level clock tree correctly.

WHAT NEXT

Check to see if the ILM boundary net is synthesized by CTS correctly.

CTS-595 (Warning) Cannot place guide buffer %s near ILM port %s.

DESCRIPTION

CTS cannot place the guide buffer near the ILM port. This may cause DRC violation on the ILM boundary net.

A guide buffer may be placed far away from the ILM port due to placement blockages near the port. In multi-voltage designs, a guide buffer may be placed away from the port if its voltage area is far away from the port.

WHAT NEXT

Check the placement, voltage area and total cap of the net inside ILM near the port if there is DRC violation on the ILM boundary net.

CTS-596 (Warning) The shortest path under %s operating condition for clock %s of root pin %s ends on pin %s inside ILM.

DESCRIPTION

When a shortest path ends inside an ILM, CTS may not be able to produce good skew. This is because CTS cannot insert clock buffers inside ILM to increase shortest path delay and improve skew.

WHAT NEXT

If the skew is not within target, run optimize_clock_tree or re-synthesize the clock network inside ILM with proper constraints.

CTS-597 (warning) Cell %s is a hierarchical ICG cell that cannot be split because there are other cells in the hierarchy.

DESCRIPTION

This warning message occurs when the split_clock_net command encounters a hierarchical integrated clock gating cell (ICG) with other cells in the hierarchy. A hierarchical ICG cell consists of an ICG captured inside a level of hierarchy. The ICG cell should be the only cell in the hierarchy. The hierarchy is marked with the clock gating logic attribute.

WHAT_NEXT

This is only a warning message.

However, if you want the clock gate to be duplicated, then please check your flow to determine how the additional cell(s) were added inside the hierarchy.

SEE ALSO

split_clock_net(2)

CTS-598 (warning) Cell %s is inside of ILM and cannot be split.

DESCRIPTION

This warning message occurs when the split_clock_net command encounters a cell inside of ILM.

WHAT_NEXT

Please specify clock nets or gates outside of ILM for split_clock_net.

SEE ALSO

split_clock_net(2)

CTS-599 (Warning) Cell %s has clock tree exceptions specified

on all of its input pins, so it will not be split.

DESCRIPTION

This warning message occurs when the split_clock_net command encounters a clock gate with clock tree exceptions (ignore, float, stop) defined on all of its input pins.

WHAT NEXT

This is only a warning message.

However, if you want the clock gate to be duplicated, then please check your clock tree exception settings.

SEE ALSO

split_clock_net(2)

CTS-600 (Warning) Turning off -ocv_clustering since is not compatible with -config_file_read.

DESCRIPTION

OCV-aware clustering is not compatible with -config_file_read.

WHAT NEXT

Use either -config_file_read or -ocv_clustering for clock tree synthesis.

CTS-601 (Warning) Turning off -ocv_clustering since is not compatible with -logic_level_balance.

DESCRIPTION

OCV-aware clustering is not compatible with -logic_level_balance.

WHAT NEXT

Use either -logic_level_balance or -ocv_clustering for clock tree synthesis.

CTS-602 (Warning) OCV-aware clustering will be applied on all clocks.

DESCRIPTION

OCV-aware clustering currently is a global setting.

WHAT NEXT

Synthesize the clocks that require OCV-aware clustering separately from the rest. Turn on -ocv_clustering for the clocks that require OCV-aware clustering, and turn off -ocv_clustering for the rest.

CTS-603 (warning) Cell %s is an intermediate level clock gate with an unsynthesized subtree, so it will not be split.

DESCRIPTION

This warning message occurs when the split_clock_net command encounters an intermediate level clock gate with an unsynthesized subtree. By default, this command will not split such cells because splitting cells which have unsynthesized subtrees in their fanout will result in bad skew and insertion delay. It is recommended that users process the nets in the clock tree starting from the lowest level nets. If, however, you would like to override this check, you can run the split_clock_net command with the -split_intermediate_level_clock_gates option. Now you will have a clock structure which has some nets that are marked as synthesized at the intermediate level. When you subsequently run compile_clock_tree on the related clock, it will stop traversal at these nets that have been marked as synthesized. As a result you will have an incorrect clock tree, with some still unsynthesized subtrees. To workaround this, that is, to ensure that compile_clock_tree traverses through all the subtrees in the clock structure, you can run the remove_clock_tree command prior to compile_clock_tree. The remove_clock_tree command will remove the attribute that indicates that a net has been synthesized.

WHAT_NEXT

You can force the split_clock_net command to split this instance by running it with the -split_intermediate_level_clock_gates option. However, it is not recommended to split intermediate level clock gates without first processing the lower level nets as this may result in bad skew and insertion delay

SEE ALSO

split_clock_net(2)

CTS-604 (warning) Splitting cell %s, even though it is an intermediate level clock gate with an unsynthesized subtree.

DESCRIPTION

This warning message occurs when the split_clock_net command encounters an intermediate level clock gate with an unsynthesized subtree, and cts_split_intermediate_level_clock_gates is set to true, thereby forcing the gate to be split.

WHAT_NEXT

This is only a warning message.

SEE ALSO

split_clock_net(2)

CTS-605 (warning) Cell %s has implicit ignore pin.

DESCRIPTION

This warning message occurs when the split_clock_net command encounters a clock gate to be duplicated that has a pin considered as implicit ignore by the timer.

WHAT_NEXT

This is only a warning message.

SEE ALSO

split_clock_net(2)

CTS-606 (warning) All pins driven by cell %s are inside of ILM, so it will not be split.

DESCRIPTION

This warning message occurs when the split_clock_net command encounters a cell inside of ILM.

WHAT_NEXT

Please specify clock nets or gates whose fanout is outside of ILM for split_clock_net.

SEE ALSO

split_clock_net(2)

CTS-607 (Warning) Pin %s has ideal network defined. Removing the attribute.

DESCRIPTION

This warning message occurs when the split_clock_net command encounters a gate with ideal network defined on one of its pins.

WHAT NEXT

This is only a warning message. The ideal network designation is removed, in order to ensure correct load and transition delay calculation for the related net.

SEE ALSO

split_clock_net(2)

CTS-608 (Warning) Turning off -top_mode since is not compatible with -config_file_read/write.

DESCRIPTION

Top mode is not compatible with -config_file_read/write.

WHAT NEXT

Use either -config_file_read/write or -top_mode for clock tree synthesis.

CTS-610 (Warning) no DRC fixing on the net %s inside ILM.

DESCRIPTION

In general, ILM is a read only cell. CTS doesn’t insert any buffer to fix DRC violations for the nets inside ILM.

WHAT NEXT

Open the ILM cell and run compile_clock_tree with DRC fixing beyond exception pins or ignore this warning.

CTS-611 (Information) no clock tree synthesis on the net %s inside ILM.

DESCRIPTION

This message shows that the tool see the ILM net while it traverses clock paths. CTS doesen’t synthesize the nets inside ILM because they are supposed synthesized nets.

WHAT NEXT

If the net inside ILM is not a synthesized net, open the ILM cell and run compile_clock_tree.

CTS-612 (Warning) no delay insertion on the net %s inside ILM.

DESCRIPTION

In general, ILM is a read only cell. CTS doesn’t insert any buffer for the nets inside ILM.

WHAT NEXT

Open the ILM cell and run compile_clock_tree with delay balance. You may have to set correct sync pin phase delay for all clock output ports on ILM in order to balance delays.

CTS-613 (Information) no clock tree optimization on the net %s

inside ILM.

DESCRIPTION

This message shows that the tool see the ILM net while it traverses clock paths. CTO doesen’t optimize the nets inside ILM.

WHAT NEXT

Open the ILM cell and run optimize_clock_tree.

CTS-614 (Information) no clock tree synthesis on don’t touch net %s.

DESCRIPTION

The net is either a PAD net, a dont_buffer net, a net inside ILM or a net beyond dont_touch_subtree exception. Therefore, CTS will not synthesize the net.

WHAT NEXT

CTS-615 (Information) no clock tree synthesis on hier don’t touch net %s.

DESCRIPTION

The net is an input/output net of a level shifter. Therefore, CTS will not synthesize the net.

WHAT NEXT

CTS-616 (Warning) cannot fix transition violation at pin/port %s.

DESCRIPTION

WHAT NEXT

CTS-617 (Warning) cannot fix capacitance violation at pin/port %s.

DESCRIPTION

WHAT NEXT

CTS-618 (Warning) No LEQ library cell found for cell %s (%s).

DESCRIPTION

The cell does not have any LEQ cell and CTS will not size the cell to improve QoR.

WHAT NEXT

Check to see if the LEQ cells are included in the target library and they do not have dont_use or dont_touch attributes.

CTS-619 (Warning) too small maximum %s (=%f) defined at library cell %s.

DESCRIPTION

The value of the listed constraint for the library cell is too small. The constraint comes from SDC or library. It can cause CTS to use excessive number of buffers to build clock trees.

WHAT NEXT

Relax the listed constraint from SDC and/or library.

CTS-620 (Warning) too small maximum %s (=%f) defined at pin %s.

DESCRIPTION

The value of the listed constraint for the clock tree at the pin is too small. The value comes from either per-clock or global clock tree options. It can cause CTS to use excessive number of buffers to build the clock tree. Also, the constraints may not be feasible at all and can lead to many DRC violations.

WHAT NEXT

Relax the listed per-clock or global constraint.

CTS-621 (Warning) no global maximum %s constraint defined, set it to 9999.

DESCRIPTION

The listed global maximum constraint is an invalid value and CTS automatically sets it to a large number.

WHAT NEXT

Set a proper global maximum constraint if necessary.

CTS-622 (Warning) The Tcl variable cts_push_down_buffer is obsolete.

DESCRIPTION

The variable is obsolete.

WHAT NEXT

Use split_clock_net -drive_ungated_registers to enable the feature.

CTS-623 (warning) Marking clock pin %s on enable of discrete clock gating cell as exclude pin.

DESCRIPTION

This warning message will be triggered for designs with discrete clock gating cells during initialization of the clock tree synthesis and optimization commands. For latch-based discrete clock gating cells, in order to prevent the clock pin on the latch delaying the clock gating enable signal from being balanced with the other registers in the design, it is automatically marked with an exclude pin clock tree exception. These latch clock pins will then also be reported as explicit ignore pins by report_clock_tree -exceptions, along with any other exclude pins specified by the user.

WHAT_NEXT

This is only a warning message.

SEE ALSO

compile_clock_tree (2)
optimize_clock_tree (2)
report_clock_tree (2)

CTS-624 (Information) no delay cells inserting on hier don’t touch net %s.

DESCRIPTION

The net is an input/output net of a level shifter. Therefore, CTS will not insert delay cells in the net.

WHAT NEXT

CTS-630 (Error) The CTS engine failed to connect the pin %s to

the net %s.

DESCRIPTION

The CTS engine failed to connect a pin to a net when inserting a buffer or inverter. Please check whether this net has multiple drivers or any unusual property which the CTS cannot support.

WHAT NEXT

This is an internal failure of CTS engine.

CTS-650 (Error) Proper power options have not been enabled for optimize_pre_cts_power.

DESCRIPTION

The **optimize_pre_cts_power** command has not found any valid power options. At least one of low_power_placement and clock_gating options should be turned on.

WHAT NEXT

User should use **set_power_options** command to specify low_power_placement and/or clock_gating for power optimization, before running **optimize_pre_cts_power**.

SEE ALSO

set_power_options (2),
set_optimize_pre_cts_power_options (2),

CTS-651 (Warning) Found no clock gates to optimize.

DESCRIPTION

Clock gate optimization has been enabled, but the **optimize_pre_cts_power** command was unable to find any optimizable clock gates. Clock gate optimization will be skipped.

WHAT NEXT

If needed, please check clock gates with **identify_clock_gating** command.

SEE ALSO

set_power_options (2),
identify_clock_gating (2),

CTS-652 (Error) Cannot read the constraint file %s.

DESCRIPTION

The **optimize_pre_cts_power** cannot correctly read the constraint file given by **set_optimize_pre_cts_power_options**.

WHAT NEXT

Check the name and location of the constraint file, and make sure you can 'source' the file.

SEE ALSO

set_optimize_pre_cts_power_options (2),

CTS-653 (Warning) Found a clock that already has been synthesized, so all existing clock trees will be removed.

DESCRIPTION

optimize_pre_cts_power encountered a clock on which CTS already has been applied. All the clock trees will be removed to ensure pre-CTS stage. If -honor_dont_touch flag was set in **set_optimize_pre_cts_power_options** , dont_touch attributes will be honored during the clock tree removal.

WHAT_NEXT

Please run **optimize_pre_cts_power** on a pre-CTS stage. Or, use remove_clock_tree command to remove current clock trees before running it.

SEE ALSO

set_optimize_pre_cts_power_options (2),
remove_clock_tree (2),

CTS-654 (Warning) Transition to Capacitance Conversion

Failed.

DESCRIPTION

This message is a debug message. This message indicates that the transition to capacitance conversion for a given library arc did not succeed. CTS in this case will use the default values.

WHAT_NEXT

If the conversion does not succeed, tool will use the default target values.

SEE ALSO

CTS-655 (Warning) The cts_enable_rc_constraints Tcl variable is obsolete. Please use the set_clock_tree_options command to enable the maximum RC constraint.

DESCRIPTION

This message indicates that the cts_enable_rc_constraints Tcl variable is not supported. To enable the maximum RC constaint, please use the **set_clock_tree_options** command with **-max_rc_delay_constraint** or **-max_rc_scale_factor** option.

WHAT_NEXT

Please do not use the cts_enable_rc_constraints variable. Instead, run the **set_clock_tree_options** command with **-max_rc_delay_constraint** or **-max_rc_scale_factor** option.

SEE ALSO

set_clock_tree_options(2)

CTS-656 (Warning) cts_size_clock_gate is no longer supported. Clock gates will be sized automatically.

DESCRIPTION

Tcl variable cts_size_clock_gate is outdated. Clock gates are now being sized

automatically. To turn off this behavior please use Tcl variable cts_prects_upsize_gates.

WHAT_NEXT

This variable is not needed. CTS will size up the clock gates automatically.

SEE ALSO

CTS-657 (Error) Cannot open file %s to write.

DESCRIPTION

CTS cannot open the give file for writing.

WHAT_NEXT

Please check the ownership and permissions for the given file.

SEE ALSO

CTS-658 (Warning) Ignoring net <%s> since its driving pin is ignored.

DESCRIPTION

CTS is ignoring the given net for synthesis, since its driver is ignored. This happens when the driver does not have a valid connection or invalid phase delay.

WHAT_NEXT

Please check the connections. If driver has an open pin or invalid phase delay, this might lead to the driving pin being ignored.

SEE ALSO

CTS-659 (Warning) Check configuration file at line %d: no such

routing rule: %s .

DESCRIPTION

This message indicates an error in user input in config file. Tool is unable to find the non-default routing rule defined at the given line.

WHAT_NEXT

Please check the non-default routing rule specified at the given line.

SEE ALSO

CTS-660 (Warning) Check configuration file at line %d: invalid min_layer constraint: %s.

DESCRIPTION

This message indicates an error in user input in config file. Tool is unable to find the minimum layer constraint defined at the given line.

WHAT_NEXT

Please check the minimum layer constraints specified at the given line.

SEE ALSO

CTS-661 (Warning) Check configuration file at line %d: invalid max_layer constraint: %s.

DESCRIPTION

This message indicates an error in user input in config file. Tool is unable to find the maximum layer constraint defined at the given line.

WHAT_NEXT

Please check the maximum layer constraints specified at the given line.

SEE ALSO

CTS-662 (Warning) No %s found for opcond %s.

DESCRIPTION

This message indicates that tool is unable to find an inverter or buffer for a given operating condition. This happens when the library specified for the given operating condition does not contain the inverters or buffers specified. The library might have the inverters or buffers but they can be marked as dont_use or dont_touch.

WHAT_NEXT

Please check the library to see if it contains buffers or inverters. If library has the specified cells, please check if these cells have dont_touch or dont_use attribute defined on them.

SEE ALSO

CTS-670 (Warning) No delay insertion for target early delay on dont_buffer_net %s.

DESCRIPTION

Target_early_delay is set on this clock and the net has dont_buffer_net attribute and the tool will skip the net for adding delay cells to meet the target.

WHAT_NEXT

Check target_early_delay constraint or the dont_buffer_net attribute on the net.

SEE ALSO

CTS-671 Inter-clock delay balance cannot handle a cell drives multiple clock nets %s and %s.

DESCRIPTION

To balance inter-clock delay, delay cells are added on clock root net or downstream

net if root net is not bufferable. If it traces to a cell with multiple output cell with valid clock sink from each output, the tool fails to do the balancing and skip this clock.

WHAT_NEXT

Re-define the clock with multiple sources at each output of the cell to use the inter-clock balance comamnd. Or use other clock tree target delay constraints to build the clock tree.

SEE ALSO

CTS-680 (error) Clock has already been synthesized! Please remove the clock tree before using this command.

DESCRIPTION

This message occurs when user tries to call split_clock_gates command after clock tree synthesis. Split_clock_gates will remove all synthesized clock trees in the end.

WHAT_NEXT

Please call split_clock_gates on a pre-CTS stage. Or use remove_clock_tree to remove current clock trees before it.

SEE ALSO

split_clock_gates(2)

CTS-681 (warning) No clock gating cells found. Splitting is not performed.

DESCRIPTION

This message indicates that tool is unable to find any clock gating cells, when running the **split_clock_gates** command. Clock gates splitting will be skipped.

WHAT_NEXT

If needed, please check clock gates with **identify_clock_gating** command.

SEE ALSO

split_clock_gates (2),
identify_clock_gating (2),

CTS-682 (Error) clock %s of pin %s also specified as clock tree to optimize

DESCRIPTION

This error message occurs during initialization for optimize_clock_tree if both a pin that was specified as a clock tree optimize and one of its clocks are specified for the -clock_trees argument.

WHAT NEXT

Please adjust the -clock_trees argument to include either the pin or the clock, not both.

SEE ALSO

optimize_clock_tree (2)

CTS-700 (Error) net %s is marked as a dont_buffer_net.

DESCRIPTION

This error message is triggered when an interactive CTS netlist editing command tries to insert a buffer on a net with the dont_buffer_net clock tree_exception specified. This applies to buffer insertion and reparenting.

WHAT NEXT

remove_clock_tree_exceptions -dont_buffer_nets can be used to remove the attribute from the net. The user should pay close attention to the reason why clock tree synthesis was restricted from buffering the net. report_clock_tree -exceptions can be used to report clock nets marked with the dont_buffer_net attribute.

SEE ALSO

remove_clock_tree_exceptions (2)
report_clock_tree (2)

CTS-701 (Error) %s is in dont_touch_subtree.

DESCRIPTION

This error message is triggered when an interactive CTS netlist editing command tries to make a netlist change to a part of the clock network designated as dont_touch_subtree using the set_clock_tree_exceptions.

WHAT NEXT

remove_clock_tree_exceptions -dont_touch_subtrees can be used to remove the attribute from the net. The user should pay close attention to the reason why clock tree synthesis was restricted from buffering the subtree. report_clock_tree -exceptions can be used to report pins to which the dont_touch_subtree exception applies.

SEE ALSO

remove_clock_tree_exceptions (2)
report_clock_tree (2)

CTS-702 (Warning) no interactive CTS changes to undo!

DESCRIPTION

This warning message is triggered when the user invokes interactive CTS (iCTS) undo when no uncommitted iCTS changes have been made.

WHAT NEXT

This is only a warning message.

CTS-750 (Error) Can not open file (%s) for Writing Nets.

DESCRIPTION

Open file error.

WHAT NEXT

Check the accessiblity of this file.

CTS-751 (Error) Can not open file (%s) for Writing Buffers.

DESCRIPTION

Open file error.

WHAT NEXT

Check the accessiblity of this file.

CTS-752 (Error) Can not open acoInsertionDelay.trees file.

DESCRIPTION

Open file error.

WHAT NEXT

Check the accessiblity of this file.

CTS-753 (Error) Can not open file for Writing Targets Violations.

DESCRIPTION

Open file error.

WHAT NEXT

Check the accessiblity of this file.

CTS-754 (Error) Can not open file for Dumping Ignore Pins.

DESCRIPTION

Open file error.

WHAT NEXT

Check the accessiblity of this file.

CTS-755 (Warning) no clock tree synthesis on the bi-direction net %s.

DESCRIPTION

Tool would not do clock tree synthesis on the bi-direction net, for it can not insert buffers or inverts on bi-direction net. This is only a warning message.

WHAT NEXT

Check this bi-direction net.

CTS-757 (Warning) no clock tree synthesis on the routed net %s.

DESCRIPTION

Tool would not do clock tree synthesis on routed net. This is only a warning message.

WHAT NEXT

Remove the routing information of this net.

CTS-759 (Error) Unable to hookup pin.

DESCRIPTION

This error occurred because buffer level exceed the limitation (1000) when bulid the clock tree based on target load capacitance.

WHAT NEXT

CTS-760 (Warning) net %s: the estimated number of buffer levels (=%d) exceed the maximum buffer levels constraint

(=%d) due to the big delay in its sub-trees.

DESCRIPTION

This warning caused by the big delay in sub-trees when bulid clock tree with budged delay.

WHAT NEXT

CTS-761 (Warning) stop to insert buffers to fix DRC on net %s (current buffer levels = %d, constraint = %d).

DESCRIPTION

This warning caused by the big delay in sub-trees when bulid clock tree with budged delay.

WHAT NEXT

CTS-762 (Warning) Exceeded maximum buffer levels on net %s in order to fix DRC violations current buffer levels = %d; constraint = %d.

DESCRIPTION

WHAT NEXT

CTS-810 (Warning) There is a clock-tree exception on the hierarchical pin '%s'.

DESCRIPTION

The **check_clock_tree** command has encountered a hierarchical pin with one or more clock-tree exceptions on it. Clock-tree synthesis will ignore exceptions on hierarchical pins.

WHAT NEXT

Clock-tree exceptions can be removed with the **remove_clock_tree_exceptions** command or if required, exception should be moved to the leaf pin driving the hierarchical pin.

SEE ALSO

check_clock_tree (2),
remove_clock_tree_exceptions (2).

CTS-811 (Warning) The clock '%s' is defined on the hierarchical pin '%s'.

DESCRIPTION

The **check_clock_tree** command has encountered a clock or generated-clock with its source defined on a hierarchical pin. Clock-tree synthesis will ignore such clocks.

WHAT NEXT

The clock should be removed with the remove_clock **or** remove_generated_clock **command as appropriate and then redefined with the respective** create_clock **or** create_generated_clock **command using a non-hierarchical pin or port as the clock source.**

SEE ALSO

check_clock_tree (2),
remove_clock (2),
remove_generated_clock (2),
create_clock (2),
create_generated_clock (2).

CTS-812 (Error) The clock source of net %s is defined at a hierarchical port and drives sink/load pins in multiple voltage areas.

DESCRIPTION

The **compile_clock_tree** command cannot insert guide buffer when the clock source at a hierarchical port drives sink/load pins in multiple voltage areas.

WHAT NEXT

Please create the clock at the output of a valid drive cell when driving sink/load pins in multiple voltage areas.

SEE ALSO

CTS-813 (Error) No always on buffer available for net '%s'.

DESCRIPTION

The **compile_clock_tree** command need to insert always on buffer for a clock net, buf no always on buffer available in the library.

WHAT NEXT

Please create always on buffer in the library or create power guides in the corresponding power down domain.

SEE ALSO

CTS-814 (Error) Net '%s' needs always on buffer and there is no always on buffer available.

DESCRIPTION

The **compile_clock_tree** command need to insert always on buffer for a clock net, buf no always on buffer available in the library.

WHAT NEXT

Please create always on buffer in the library or create power guides in the corresponding power down domain.

SEE ALSO

CTS-821 (Warning) The master-clock '%s' does not propagate

to the generated-clock ’%s’ defined at the %s ’%s’.

DESCRIPTION

The **check_clock_tree** command has encountered a generated-clock whose master-clock does not propagate to it. Although the master-clock is only used as a waveform reference, and propagation to the generated-clock source pin is not strictly required, in most designs a path between master and generated clock is intended. Often the user has specified either the wrong master-clock or the wrong generated-clock source pin.

WHAT NEXT

The clock should be removed with the remove_generated_clock **command and redefined with the** create_generated_clock **command using the correct master-clock and/or generated-clock source pin.**

If there is no problem with the generated-clock specification, then use the report_case_analysis **and/or** report_disable_timing **commands to see if pins within the clock-tree are affected. Use the** report_timing **command to verify there is a path from the master-clock source pin to the generated-clock source pin.**

SEE ALSO

check_clock_tree (2),
remove_generated_clock (2),
create_generated_clock (2),
report_case_analysis (2),
report_disable_timing (2),
report_timing (2).

CTS-822 (Warning) The generated-clock ’%s’ defined at the %s ’%s’ has an improperly specified master-clock.

DESCRIPTION

The **check_clock_tree** command has encountered a generated-clock with an improperly specified master-clock. The most common cause of this is incorrectly specifying the master-clock and/or the master-clock source pin for the create_generated_clock **command.**

WHAT NEXT

The report_clock **command can be used to verify that the generated-clock has an improper specification, and to see what master-clock and master-clock source pin were used in the specification. The** report_clock_tree **command can be used to verify that the master-clock source pin is within the master-clock domain.**

SEE ALSO

check_clock_tree (2),
create_generated_clock (2),
report_clock (2),
report_clock_tree (2).

CTS-823 (Warning) The clock '%s' terminates at the multi-clock %s '%s' without a corresponding generated-clock.

DESCRIPTION

The **check_clock_tree** command has encountered a generated-clock source pin that has one or more unrelated master-clocks terminating at it. Hence this pin will be treated as a non-stop pin for the generated-clock and as a stop-pin for the unrelated master-clock(s). This inconsistency will cause large skew for clocks having the second kind of treatment to be synthesized.

Please note that the shell variable **timing_enable_multiple_clocks_per_reg** must be set true in order for the timing-engine to propagate multiple clocks per register. If this variable is set false, **check_clock_tree** will perform an additional check to see if the design has overlapping clock domains (CTS-834).

WHAT NEXT

For each master-clock at the pin with no related generated-clock, the create_generated_clock **command can be used to create enough additional generated-clocks so that the pin is treated consistently for all clocks. Alternatively, generated-clocks can be removed with the** remove_generated_clock **command. The user should double-check the desireability of the incoming and outgoing clocks to support the design intention.**

SEE ALSO

check_clock_tree (2),
timing_enable_multiple_clocks_per_reg (3),
CTS-834 (n),
create_generated_clock (2),
remove_generated_clock (2).

CTS-831 (Information) The clock '%s' defined at %s '%s' has no

synchronous pins.

DESCRIPTION

The **check_clock_tree** command has encountered a clock tree with no synchronous pins. Clock-tree synthesis will skip such clocks unless they connect to a dependent and valid generated-clock which does have synchronous pins. There are some subtleties to this:

- A generated-clock may be invalid if it has an improperly specified master clock (CTS-822).
- Synchronous pins with explicit exclude clock-tree exceptions are ignored.
- Stop, float, and exclude clock-tree exceptions block downstream synchronous pins.

The number of synchronous pins is not necessarily the number of "sink" pins reported by the **report_clock_tree** command, because that includes exclude-pins and any subordinate generated-clock sink pins.

The number of synchronous pins is not necessarily the number reported by the **report_clock_timing** command, because that ignores clock-tree exceptions.

WHAT NEXT

This message is informational only. If synchronous pins for the clock were intended for the design, the user should double-check that there are synchronous pins in the netlist fanout of the clock source, and that clock-tree exceptions, case-analysis, and/or disable-timing have not been set in a way that block or ignore them. The **report_clock_timing** latency report can be used to see the synchronous pins for each clock. The **report_clock_tree** command can be used to see the clock-tree exceptions on synchronous pins.

SEE ALSO

check_clock_tree (2),
CTS-822 (n),
report_clock_tree (2),
report_clock_timing (2),
report_clock (2),
set_clock_tree_exceptions (2),
report_case_analysis (2),
report_disable_timing (2).

CTS-832 (Warning) The clock '%s' defined at %s '%s' loops to itself.

DESCRIPTION

The **check_clock_tree** command has encountered a clock tree with a path that loops from the clock source to itself.

Please note that a loop can exist for clock-tree synthesis where it does not for timing-analysis. In particular, timing-analysis will consider loops to be broken at clock and generated-clock source or sink pins, whereas clock-tree synthesis will jump across implicit and explicit non-stop pins and see a problematic loop.

It is possible that **check_clock_tree** will not see a loop through a non-unate (e.g. exclusive-or) cell in a clock-tree, but the timing-engine will issue warning message TIM-052.

WHAT NEXT

If there are no sequential elements within the looping path, it is very likely the looping path can be seen by using **report_timing** from the clock source to itself. If the user does not manually set a clock-tree exclude exception to break the loop, such simple loops will be automatically detected and broken during clock-tree synthesis (but without user choice).

However, if there are sequential elements within the looping path, it is very likely the looping path cannot be seen by using **report_timing**, and such complex loops will not be automatically handled by clock-tree synthesis. The user will have to manually set a clock-tree exclude exception to break the loop.

At this time we know of complex loops which require clock-specific clock-tree exceptions to support correctly; a future version of IC Compiler will include support for that. In the interim, **check_clock_tree** can be used to catch these loops.

SEE ALSO

check_clock_tree (2),
TIM-052 (n),
report_timing (2),
set_clock_tree_exceptions (2).

CTS-833 (Information) The clock '%s' defined at %s '%s' should be synthesized before the clock '%s' defined at %s '%s'.

DESCRIPTION

The **check_clock_tree** command has encountered cascaded clocks which require a

particular sequence of clock-tree syntheses to achieve the best results.

This informational message is triggered during the traversal of the upper-level clock tree when a lower-level clock is encountered that satisfies these criteria:

-- not a generated-clock -- defined on a driver pin -- not synthesized yet

If the upper-level clock is synthesized before the lower-level clock, the driver of the lower-level clock will see an unrealistic load. This can cause improper cell sizes to be used to fix the bogus design-rule problem in the upper-level clock tree at the expense of global-skew and/or insertion-delay.

WHAT NEXT

Synthesize the clock trees in the specified order using the **compile_clock_tree** command.

SEE ALSO

check_clock_tree (2),
compile_clock_tree (2).

CTS-834 (Warning) The shell variable timing_enable_multiple_clocks_per_reg is false but multiple clocks fan-into %s '%s'.

DESCRIPTION

The **check_clock_tree** command has encountered overlapping clock trees, but the shell variable **timing_enable_multiple_clocks_per_reg** is false, thus preventing the timing-engine from propagating multiple clocks per register. This will prevent **check_clock_tree** from seeing potential problems specific to overlapping clocks (e.g. CTS-823).

This check works by detecting when two clocks on different from-pins are incident upon the same to-pin. Only one warning is issued per to-pin, so if there are more than two clocks overlapping at the pin, only the first pair encountered will be warned about. This check is not performed if the shell variable **timing_enable_multiple_clocks_per_reg** is set true.

WHAT NEXT

The user can set the shell variable **timing_enable_multiple_clocks_per_reg** true, or they can use the **set_clock_tree_exceptions**, **set_case_analysis**, and/or **set_disable_timing** commands to prevent overlapping clocks.

SEE ALSO

check_clock_tree (2),
timing_enable_multiple_clocks_per_reg (3),
CTS-823 (n),
set_clock_tree_exceptions (2),
set_case_analysis (2),
set_disable_timing (2).

CTS-835 (Warning) There is a %s clock-tree exception on the output pin '%s'.

DESCRIPTION

The **check_clock_tree** command has encountered a stop or float clock-tree exception on an output pin. If the total capacitance seen at that pin is larger than the max-capacitance design rule for clock-tree synthesis, design-rule fixing may degrade the clock-tree quality after the clock-tree is synthesized.

WHAT NEXT

Unless you are certain the total load seen at the output pin is less than the max-capacitance design rule specified with the **set_clock_tree_options** command, the exception should be moved to an input pin within the same clock domain. You can remove exceptions with the **remove_clock_tree_exceptions** command and set them with the **set_clock_tree_exceptions** command. You can list clock-tree settings and exceptions with the **report_clock_tree** command.

SEE ALSO

check_clock_tree (2),
set_clock_tree_options (2),
remove_clock_tree_exceptions (2),
set_clock_tree_exceptions (2),
report_clock_tree (2).

CTS-836 (Warning) The following unclocked sink pins were found while tracing clock '%s' from %s '%s':

DESCRIPTION

The **check_clock_tree** command has encountered one or more unclocked sink pins in the specified clock domain while tracing from the specified clock source pin.

An unclocked sink pin is one that is associated with a clock tree for the purposes

of clock tree synthesis, but it is not associated with any clock object for the purposes of constraining timing.

Unclocked sink pins are unconstrained and not in any path-group. They are not present in the output of the **report_clock_timing** command. **set_clock_latency** commands on clock objects do not affect unclocked sink pins.

Unclocked sink pins are caused by having a sequential arc within the clock tree that is not detected as part of a clock-gating cell or a generated-clock source. The sequential arc blocks the association of the clock object with the sink pins, but it does not affect the association of the clock tree with the sink pins for the purpose of clock tree synthesis.

WHAT NEXT

Review the intention of the unclocked sink pins and any blocking sequential arc(s).

If the unclocked sink pins are to be clocked, then often an additional generated-clock definition is required to convert a blocking sequential arc into a non-blocking one.

If the intention is to have the sink pins in question be unclocked, then the pins should be marked with explicit exclude clock tree exceptions via the **set_clock_tree_exceptions** command. If the **skew_opt** command is used to create useful-skew, unclocked sink pins will be automatically given exclude clock tree exceptions.

SEE ALSO

check_clock_tree (2),
report_clock_timing (2),
set_clock_latency (2),
set_clock_tree_exceptions (2),
skew_opt (2).

CTS-840 (Warning) There are multiple clock-tree exceptions on %s '%s' for clock '%s' defined at %s '%s'.

DESCRIPTION

The **check_clock_tree** command has encountered a pin or port with multiple clock-tree exceptions on it. This can potentially lead to inconsistent treatment throughout the flow and/or across releases of IC Compiler.

WHAT NEXT

For a given pin or port, the user should use the **remove_clock_tree_exceptions** command to remove an existing exception before using the **set_clock_tree_exceptions** command to set a new one. The exceptions on clock-tree pins can be reported with the **report_clock_tree** command.

SEE ALSO

check_clock_tree (2),
remove_clock_tree_exceptions (2),
set_clock_tree_exceptions (2),
report_clock_tree (2).

CTS-841 (Warning) The clock '%s' defined at %s '%s' has ignored exceptions along a path through %s '%s'.

DESCRIPTION

The **check_clock_tree** command has encountered a path within a clock-tree where one clock-tree exception blocks another.

Only one warning is given for each blocking exception. If an exception blocks more than one exception in its fanout, only the first blocked exception will be warned about. This prevents a flood of messages in case there are many clock-tree exceptions in the design (e.g. when useful-skew is applied).

WHAT NEXT

The user should use the **remove_clock_tree_exceptions** command to remove either the blocking or blocked exception. Clock-tree exceptions can be set with the **set_clock_tree_exceptions** command. The exceptions on clock-tree pins can be reported with the **report_clock_tree** command.

SEE ALSO

check_clock_tree (2),
remove_clock_tree_exceptions (2),
set_clock_tree_exceptions (2),
report_clock_tree (2).

CTS-842 (Warning) library cell '%s' is marked with dont_use attribute.

DESCRIPTION

This warning message occurs when an interactive CTS command (**insert_buffer** or **size_cell** with -interactive_cts option) is being invoked using a library cell with the dont_use attribute.

WHAT NEXT

Interactive CTS allows for buffer insertion and cell sizing to use library cells even if they are marked with dont_use, so no further action is required.

SEE ALSO

insert_buffer(2)
size_cell(2)

CTS-843 (Error) cell '%s' is inside ILM.

DESCRIPTION

This warning message occurs when an interactive CTS command (**insert_buffer**, **remove_buffer**, or **size_cell** with -interactive_cts option, or **icts_move_cell**) is being called for a cell inside of an ILM.

WHAT NEXT

Changes cannot be made to cells inside ILM.

SEE ALSO

insert_buffer(2)
remove_buffer(2)
size_cell(2)
icts_move_cell(2)

CTS-844 (Warning) no clock nets found.

DESCRIPTION

This warning message occurs when an interactive CTS command (**insert_buffer**, **remove_buffer**, or **size_cell** with -interactive_cts option, or **icts_move_cell**) is being called before CTS.

WHAT NEXT

The interactive CTS commands do not support pre-CTS designs. Please run compile_clock_tree first.

SEE ALSO

insert_buffer(2)

remove_buffer(2)
size_cell(2)
icts_move_cell(2)
compile_clock_tree(2)

CTS-845 (Error) failed to find cell %s to move.

DESCRIPTION

This error message occurs when the interactive CTS **icts_move_cell** command is called with a cell that cannot be found in the current design.

WHAT NEXT

Please double-check whether or not the specified cell exists using get_cells.

SEE ALSO

icts_move_cell(2)

CTS-846 (Error) number of sets of coordinates (%d) does not match with number of cells (%d)

DESCRIPTION

This error message occurs when the number of locations and number of cells specified for the interactive CTS icts_move_cell command are not the same.

WHAT NEXT

Please double-check that each cell to be moved has a corresponding location specified.

SEE ALSO

icts_move_cell(2)

CTS-847 (Error) Clock tree initialization failed

DESCRIPTION

This error message occurs when the **optimize_clock_tree** command fails during initialization.

WHAT NEXT

Please check for previous error messages in the log file for related details.

SEE ALSO

optimize_clock_tree(2)

CTS-848 (Information) no optimization on the bi-direction net %s.

DESCRIPTION

The **optimize_clock_tree** will skip bi-directional nets.

WHAT NEXT

This is only a informational message.

SEE ALSO

optimize_clock_tree(2)

CTS-849 (Information) no optimization on the routed net %s.

DESCRIPTION

The **optimize_clock_tree** command will skip routed nets when post-route clock tree optimization is not enabled.

WHAT NEXT

This is only a informational message.

SEE ALSO

optimize_clock_tree(2)

CTS-850 (Warning) No buffer available: library cell %s has dont_use/dont_touch attribute set on it.

DESCRIPTION

When user does not set clock tree reference list by using set_clock_tree_references command, CTS can not use the buffer with dont_use/dont_touch attribute for clock tree synthesis.

WHAT NEXT

If user want to use those buffers, she/he needs to remove the dont_use attribute set on the buffer

SEE ALSO

set_clock_tree_references (2),

CTS-851 (Warning) There are multiple arcs between input and output pins for buffer %s.

DESCRIPTION

The **check_clock_tree** command has detected duplicate timing arc on a buffer. Duplicate arc may cause inherient skew and increase the CTS runtime.

WHAT NEXT

User should remove this buffer from the reference list specified with **set_clock_tree_references** command.

SEE ALSO

check_clock_tree (2),
set_clock_tree_references (2),
report_clock_tree (2).

CTS-852 (Warning) There is case analysis set on pin '%s' .

DESCRIPTION

The **check_clock_tree** command has detected a case analysis set on a pin of a clock cell on the clock path. Case analysis setting may affect the clock structure seen by the tool. It is recommended for user to double check if those settings are intended for clock networks.

WHAT NEXT

Remove the unnecessary case analysis settings with the **remove_case_analysisP command.**

SEE ALSO

check_clock_tree (2),
set_case_analysis (2),
remove_case_analysis (2),
report_clock_tree (2).

CTS-853 (Warning) There is disable timing set on pin '%s' .

DESCRIPTION

The **check_clock_tree** command has detected a disable timing set on a pin on the clock path. Disable timing setting may affect the clock structure seen by the tool. It is recommended for user to double check if those settings are intended for clock networks.

WHAT NEXT

Remove the unnecessary disable timing settings with the **remove_disable_timingP command.**

SEE ALSO

check_clock_tree (2),
set_disable_timing (2),
remove_disable_timing (2),
report_clock_tree (2).

CTS-854 (Error) Clock tree optimization failed

DESCRIPTION

This error message occurs when the **optimize_clock_tree** command fails.

WHAT NEXT

Please check for previous error messages in the log file for related details.

SEE ALSO

optimize_clock_tree(2)

CTS-855 (Warning) CTS reference list defined but no reference can be used.

DESCRIPTION

The **check_clock_tree** found user-specified reference list, but none of these user-specified references can be used. Please check if the references are set to dont_use or dont_touch.

WHAT NEXT

User should check and make sure that the buffers in the reference list are not marked as dont_use or dont_touch after the CTS reference list defination.

SEE ALSO

check_clock_tree (2),
set_clock_tree_references (2),
report_clock_tree (2).
set_dont_use (2).
set_dont_touch (2).

CTS-856 (Warning) Cell %s has no orientation

DESCRIPTION

This warning message occurs during initialization of the CTS commands when there are cells without a valid orientation set.

WHAT NEXT

This is only a warning message. Please double-check whether or not the reported cells have been legally placed using **check_legality -verbose**. If the cell is not of interest for CTS, then the warning message can be safely ignored.

SEE ALSO

check_legality (2)
legalize_placement (2)
compile_clock_tree (2)
optimize_clock_tree (2)
balance_inter_clock_delay (2)

CTS-857 (Warning) %d cells have no orientation

DESCRIPTION

This warning message occurs during initialization of the CTS commands when there are cells without a valid orientation set. It will always be issued after the **CTS-856** message to report the number of cells with no orientation.

WHAT NEXT

This is only a warning message. Please double-check whether or not the reported cells have been legally placed using **check_legality -verbose**. If the cell is not of interest for CTS, then the warning message can be safely ignored.

SEE ALSO

check_legality (2)
legalize_placement (2)
compile_clock_tree (2)
optimize_clock_tree (2)
balance_inter_clock_delay (2)

CTS-880 (Error) User pulse_max_transition constraint (%f ps) is too small.

DESCRIPTION

Set_clock_tree_options assumes that the given constraint values are in main library units. The error is usually arised when the main library unit is smaller than that is assumed.

WHAT NEXT

Convert the constraint values into main library units and re-apply constraints again.

CTS-881 (Error) User pulse_min_width constraint (%f ps) is too small.

DESCRIPTION

Set_clock_tree_options assumes that the given constraint values are in main library units. The error is usually arised when the main library unit is smaller than that is assumed.

WHAT NEXT

Convert the constraint values into main library units and re-apply constraints again.

CTS-882 (Error) Pulse latch %s ’s clock sense (%s) does not match with driving pulse generator output: %s.

DESCRIPTION

Pulse clock synthesis encountered mismatching clock sense between driving pulse and input pulse of latch. This should be an error since clock sense inverting is not allowed in pulse clock synthesis. The reporting on this PL is skipped.

WHAT NEXT

Please check if clock sense is inverted through the clock path.

CTS-883 (Error) Cascaded pulse generators found! PG %s driving another PG %s.

DESCRIPTION

Pulse clock synthesis or reporting encountered cascaded pulse generator connection. There should be only one pulse generator between regular clock source to pulse latches. The reporting of this PL is skipped.

WHAT NEXT

Please check if CTS used pulse generator cells (pulse_clock_cell) as clock buffers.

CTS-884 (Error) Cannot get pulse width at pin %s.

DESCRIPTION

Pulse clock synthesis or reporting encountered an error while tryting to obtain a pulse width at the pin within pulse clock trees.

WHAT NEXT

Please check the library and/or PG to PL connection.

CTS-885 (Error) Cannot find a valid clock sense at pin %s.

DESCRIPTION

Pulse clock synthesis or reporting encountered an error while tryting to obtain a pulse clock sense at the pin, or an unexpected (unsupported) clock sense was retrieved.

WHAT NEXT

Please check which pulse clock sense type was used by set_pulse_clock_cell to specify the pulse generator.

CTS-886 (Error) PCS cannot find a corresponding pulse latch for the flop %s (%s).

DESCRIPTION

Pulse clock synthesis cannot swap the flop since the corresponding pulse latch is not found.

WHAT NEXT

Please check if flop to pulse latch pair is correctly specified.

SEE ALSO

set_pulse_clock_configuration(2)
report_pulse_clock_configuration(2)

CTS-887 (Error) The pulse type of the library cell %s is not supported in PCS.

DESCRIPTION

Pulse clock synthesis found a invalid pulse clock sense at output pin of the library cell.

WHAT NEXT

Please check the pulse clock sense type specified in the library.

CTS-888 (Error) %s is not a pulse generator cell, hence cannot be used in PCS.

DESCRIPTION

Pulse clock synthesis found a invalid pulse clock cell, which is not identified as a pulse generator.

WHAT NEXT

Please check if the library cell is correctly specified as a pulse generator using set_pulse_clock_cell

SEE ALSO

set_pulse_clock_configuration(2)
set_pulse_clock_cell(2)

CTS-909 (Warning) legalize_placement did not succeed.

DESCRIPTION

legalize_placement command called from inside add_clock_drivers command did not succeed.

WHAT NEXT

Run legalize_placement explicitly.

SEE ALSO

legalize_placement
add_clock_drivers

CTS-910 (Error) Could not invoke '%s'.

DESCRIPTION

The above mentioned simulator cannot be invoked in command "analyze_subcircuit".

WHAT NEXT

Check if you have given appropriate simulator name and also check for the path of the simulator executable.

SEE ALSO

analyze_subcircuit

CTS-911 (Error) Could not write simulator test shell file '%s'.

DESCRIPTION

Command **analyze_subcircuit** could not write the simulator test shell file. This is needed to invoke the simulator.

WHAT NEXT

Check if the file already exists and if so check if you have UNIX write permissions on this file.

SEE ALSO

analyze_subcircuit

CTS-912 (Error) Failed to mark the simulator path-test shell-

control-file ’%s’ executable.

DESCRIPTION

Command **analyze_subcircuit** could not "chmod +x" the above specified file.

WHAT NEXT

Check if the file already exists and if so check if you have appropriate UNIX permissions on this file.

SEE ALSO

analyze_subcircuit

CTS-913 (Error) Simulation path test failed, check ’%s’ and ’%s’, and look at your ’path’ and EPIC_HOME UNIX variables.

DESCRIPTION

Command **analyze_subcircuit** could not find the simulator in the path.

WHAT NEXT

Check if the simulator is in the path and can be executed.

SEE ALSO

analyze_subcircuit

CTS-914 (Error) Could not re-open the simulation log file ’%s’ for reading.

DESCRIPTION

Command **analyze_subcircuit** could not re-open the simulation log file used for testing simulator executable.

WHAT NEXT

Check if the simulator is in the path and can be executed.

SEE ALSO

analyze_subcircuit

CTS-915 (Error) Could not find 'Version' in text from '%s' - simulator was not runable.

DESCRIPTION

Command **analyze_subcircuit** checks if the simulator is available and executable by executing it once and checking if the string "Version" is found in the log file. The string Version has not been found in the current run of analyze_subcircuit.

WHAT NEXT

Check if the simulator is in the path and can be executed.

SEE ALSO

analyze_subcircuit

CTS-916 (Warning) Output pin(s) of cell instance %s has ignored exception specified. It's downstream buffer levels will not be balanced.

DESCRIPTION

Output pin(s) of cell instance %s has ignored exception specified. It's downstream buffer levels will not be balanced.

WHAT NEXT

This is only a warning message.

SEE ALSO

balance_clock_tree_level(2)

CTS-917 (Warning) Output pin(s) of cell instance %s of level %d has dont_touch_subtree exception specified. It's downstream

buffer level will not be balanced.

DESCRIPTION

Output pin(s) of cell instance has dont_touch_subtree exception specified. It’s downstream buffer level will not be balanced.

WHAT NEXT

This is only a warning message.

SEE ALSO

balance_clock_tree_level(2)

CTS-918 (Warning) Net of output pin(s) of cell instance %s of level %d has dont_buffer_net exception specified. It’s downstream buffer level will not be balanced.

DESCRIPTION

Net of output pin(s) of cell instance has dont_buffer_net exception specified. It’s downstream buffer level will not be balanced.

WHAT NEXT

This is only a warning message.

SEE ALSO

balance_clock_tree_level(2)

CTS-919 (Warning) Cell %s has clock tree exceptions specified on all of its input pins, so it’s downstream buffer levels will not be balanced.

DESCRIPTION

This warning message occurs when the balance_clock_tree_level command encounters a clock gate with clock tree exceptions (ignore, float, stop) defined on all of its

input pins.

WHAT NEXT

This is only a warning message.

SEE ALSO

balance_clock_tree_level(2)

CTS-920 (error) You must specify either "low", or "high" in -cts_effort option.

DESCRIPTION

You must specify either "low", or "high" in -cts_effort option.

WHAT NEXT

This is only an error message.

SEE ALSO

clock_opt(2)

CTS-921 (error) No cells could be created as there are some legality violations.

DESCRIPTION

This error happens when there are some legality violation. The legality violation includes the violation of multi-voltage design constraints, max_displacement constraints, connectivity legality constraints and/or other generic legalization constraints.

WHAT NEXT

Please check the correctness of the design in terms of various legality constraints.

SEE ALSO

check_mv_design(2)

check_legality(2)
report_net(2)

CTS-922 (error) Skipping pin addition %s in user skew group

DESCRIPTION

This error indicates a pin cannot be added to a skew group definition. Only clock sink pin can be added to a skew group definition.

WHAT NEXT

Please check if pin is a clock sink pin.

SEE ALSO

set_clock_tree_exception

CTS-923 (error) Pin %s , already part of %s skew group. Skipping pin addition in %s skew group

DESCRIPTION

This error happens when a given pin is already part of a user skew group. One pin can be part of a single skew group.

CTS-924 (Error) The skew group '%s' contains pins from different clock domain(s).

DESCRIPTION

The **commit_skew_group** command has encountered a skew group with pins from different clock domains. All pins in a single skew group should belong to same master clock domain(s).

WHAT NEXT

Incorrect skew group definition can be removed with the **remove_skew_group** command and new definition can be created using **set_skew_group** command.

SEE ALSO

set_skew_group (2),
remove_skew_group (2).

CTS-925 (Error) The skew group '%s' contains pins having upstream/downstream relationship.

DESCRIPTION

The **commit_skew_group** command has encountered a skew group with pins having either upstream or downstream relation with each other.

WHAT NEXT

Incorrect skew group definition can be removed with the **remove_skew_group** command and new definition can be created using **set_skew_group** command.

SEE ALSO

set_skew_group (2),
remove_skew_group (2).

CTS-926 (Error) Looping dependency found between skew group '%s' and skew group '%s'.

DESCRIPTION

The **commit_skew_group** command has encountered looping dependency between two skew groups. Pins from first skew group have upstream/downstream relation with pins from second skew group and vice-versa.

WHAT NEXT

Incorrect skew group definition can be removed with the **remove_skew_group** command and new definition can be created using **set_skew_group** command.

SEE ALSO

set_skew_group (2),
remove_skew_group (2).

CTS-927 (Error) The skew group '%s' has more than one level of dependency.

DESCRIPTION

The **commit_skew_group** command has encountered more than one level of dependency between skew groups.

WHAT NEXT

Incorrect skew group definition can be removed with the **remove_skew_group** command and new definition can be created using **set_skew_group** command.

SEE ALSO

set_skew_group (2),
remove_skew_group (2).

CTS-928 (Error) The pin '%s' in skew group '%s' does not belong to any clock domain(s).

DESCRIPTION

The **commit_skew_group** command has encountered a skew group with non clock pins.

WHAT NEXT

Incorrect skew group definition can be removed with the **remove_skew_group** command and new definition can be created using **set_skew_group** command.

SEE ALSO

set_skew_group (2),
remove_skew_group (2).

CTS-929 (Error) Found independent skew group(s) with sink pins in more than one sub-trees.

DESCRIPTION

The **commit_skew_group** command has encountered independent skew group(s) with sink

pins in more than one sub-trees. All sink pins of an independent skew group should be part of single tree.

WHAT NEXT

Incorrect skew group definition can be removed with the **remove_skew_group** command and new definition can be created using **set_skew_group** command.

SEE ALSO

set_skew_group (2),
remove_skew_group (2).

CTS-930 (Error) skew group feature is not supported with '%s'.

DESCRIPTION

The **commit_skew_group** command has found that one or more clock tree options that are not supported with skew group feature is turned on.

WHAT NEXT

Incorrect skew group definition can be removed with the **remove_skew_group** command and new definition can be created using **set_skew_group** command.

SEE ALSO

set_skew_group (2),
remove_skew_group (2).

CTS-931 (warning) Net %s can not be buffered to separate skew groups.

DESCRIPTION

This warning message occurs when the commit_skew_group command encounters a Net that can not be buffered to separate skew groups.

WHAT_NEXT

Please redefine skew groups such that clock sinks under this net belong to same skew group.

SEE ALSO

set_skew_group(2)

CTS-932 (Error) Pin not on clock path

DESCRIPTION

The **compile_clock_tree** command has encountered netlink pin %s with hierarchy presevation exception set on it but its not on clock path

WHAT NEXT

Hierarchy preservation exception can be set only for netlink pin on clock path

SEE ALSO

CTS-933 (warning) skew group %s contains some pins beyone exception.

DESCRIPTION

This warning message occurs when the commit_skew_group command encounters pins in a skew group that are beyond exception pins.

WHAT_NEXT

Please redefine skew groups such that it does not have any pins beyond exception.

SEE ALSO

set_skew_group(2)

CTS-934 (error) skew group definitions cannot be updated after commit_skew_group

DESCRIPTION

This error message comes when user is trying to add or remove skew group definition after commit_skew_group command is executed. Skew group definitions cannot change

once commited

WHAT_NEXT

Please use preCTS design or design in which skew group definition are not committed

SEE ALSO

commit_skew_group

CTS-935 (error) Skew group name %s is not unique

DESCRIPTION

This error comes when user is trying to use same skew group name more than once. Incremental updated for a skew group is not supported.

WHAT_NEXT

Please use unique name for skew group definitions. To update already defined skew group, please remove and create new skew group with updated definition

SEE ALSO

set_skew_group
remove_skew_group
report_skew_group

CTS-936 (Warning) Cell %s is not an ICG cell, clone anyway.

DESCRIPTION

a non-ICG cell can be cloned in commit_skew_group to separate skew group pins.

WHAT NEXT

The cell will be cloned.

CTS-937 (Warning) Can not split cell %s.

DESCRIPTION

a cell could not be cloned in commit_skew_group to separate skew group pins in commit_skew_group.

WHAT NEXT

The cell will not be cloned.

CTS-938 (Warning) Ignoring preserve hierarchy exception at inout pin: %s.

DESCRIPTION

inout ports of a logical hierarchy can not be preserved.

WHAT_NEXT

This exception is ignored.

CTS-939 (error) Specify either remove_clock_trees -clock_trees net_list or remove_clock_trees net_list but not both

DESCRIPTION

This error message occurs when both remove_clock_trees -clock_trees net_list or remove_clock_trees net_list are specified

WHAT NEXT

Please specify only either of remove_clock_trees -clock_trees net_list or remove_clock_trees net_list of options

CTS-940 (error) Unable to find pin object in db

DESCRIPTION

This error message occurs when pin object is not found in data base

WHAT NEXT

Please check specified pin

CTS-941 (error) CTS could not get CCI interpreter

DESCRIPTION

This error message occurs when CTS engine is not able to get CCI interpreter

WHAT NEXT

cts ui setup failed

CTS-942 (error) Failed to get library distance coversion factor

DESCRIPTION

This error message occurs when CTS engine is not able to get lib distance unit conversion

WHAT NEXT

Please check library settings

CTS-943 (error) Failed to get wire capacitance and resistance unit

DESCRIPTION

This error message occurs when CTS engine is not able to get unit for wire capacitance and resistance

WHAT NEXT

Please check library settings

CTS-944 (error) Syntax error in routing_layer_constraints at line %d of config file %s

DESCRIPTION

Unable to read min or max layer constraints from config file

WHAT NEXT

Please check config file syntax. Please correct min/max layer constraint definitions

CTS-945 (warning) Invalid routing layer constraint for %s : %s at line number %d

DESCRIPTION

routing layer constraint specified are not correct

WHAT NEXT

Please check config file syntax. Please correct min/max layer constraint definitions

CTS-946 (error) Cannot open input config file for %s from %s

DESCRIPTION

Unable to read/write config file

WHAT NEXT

Please check config file path and permissions

CTS-947 (warning) pin %s at line number %d was previously

specified for %s

DESCRIPTION

Cannot specify pin again if specified as root level pin or upper buffer level pin

WHAT NEXT

Please check config file. Please correct pin definitions.

CTS-948 (warning) Failed to assign routing layer constraint on net %s

DESCRIPTION

Unable to assign routing layer constraint on net.

WHAT NEXT

Please check routing layer constraint settings.

CTS-949 (warning) Failed to clear routing rule on net %s

DESCRIPTION

CTS is unable to clear routing on mentioned net.

WHAT NEXT

Please check routing rule settings.

CTS-950 (warning) No clock net matched entry for %s from config file

DESCRIPTION

Net specified in config file is not a clock net

WHAT NEXT

Please check config file statements.

CTS-951 (warning) Ignoring net %s since it doesn’t have any driving pin

DESCRIPTION

Mentioned net doesn’t have any driving pin. Ignoring net from clock tree.

WHAT NEXT

Please check drivers for the net

CTS-952 (error) Failed to build buffer level. Please check configuration file line number %d

DESCRIPTION

Unable to build buffer level

WHAT NEXT

Please check config file.

CTS-953 (warning) Please check configuration file at %d .Unable to read routing rule %s.

DESCRIPTION

Unable to read definition for mentioned routing rule.

WHAT NEXT

Please check config file.

CTS-954 (warning) Invalid tree. Error at %d

DESCRIPTION

Invalid tree

WHAT NEXT

Please check config file.

CTS-955 (warning) Check configuration file at line number %d . Attempt to reassign buffer level %s

DESCRIPTION

Attempt to reassign buffer level routing constraints

WHAT NEXT

Please check config file.

CTS-956 (error) Unrecognized statement at line %d in config file %s

DESCRIPTION

Unrecognized statement in config file.

WHAT NEXT

Please check config file syntax.

CTS-957 (error) Pin name %s does not exist

DESCRIPTION

Unable to find mentioned pin

WHAT NEXT

Please check config file settings.

CTS-958 (error) invalid buffer level, more buffers than sinks on net %s

DESCRIPTION

More buffer than sink pin on mentioned net.

WHAT NEXT

Please check config file.

CTS-959 (warning) Ignoring net %s

DESCRIPTION

Ignored net as its driving pin is ignored

WHAT NEXT

Please check config file.

CTS-960 (error) Ignoring statement %s at line number %d from config file

DESCRIPTION

Statement is ignored as it is not a valid buffer master

WHAT NEXT

Please check config file settings.

CTS-961 (error) Ignoring statement %s at line number %d from

config file %s

DESCRIPTION

Statement ignored because there is no current tree

WHAT NEXT

Please check config file settings.

CTS-962 (error) Incorrect placement of begin_clock_subtree at line number %d for config file %s

DESCRIPTION

begin_clock_subtree makes no sense if more than one clock tree is being constructed

WHAT NEXT

Please check config file settings.

CTS-963 (error) Incorrect usage of begin_clock_subtree statement at line number %d in config file at %s

DESCRIPTION

begin_clock_subtree statement ignored because there is no current tree

WHAT NEXT

Please check config file settings.

CTS-964 (warning) Can not separate skew groups inside an ILM.

DESCRIPTION

This warning message occurs when the commit_skew_group command encounters sinks that

belong to more than one skew groups within an ILM.

WHAT_NEXT

Please redefine skew groups such that clock sinks under ILM belong to same skew group.

SEE ALSO

set_skew_group(2)

CTS-965 (error) Cannot set %s on skew group commited design

DESCRIPTION

Skew group definitions are not supported with logic level balancing and ocv clustering. If design has skew group definition and design is skew group commited these settings will not be honoured by other cts modules.

WHAT NEXT

Please check clock tree options. If logic level balance or ocv clustering is required, design should not be skew group commited

CTS-966 (Warning) Cell %s is driving hierarchical clock source pin.

DESCRIPTION

Cell %s is driving a hierarchical pin with clock source definition on it.

WHAT NEXT

The cell wont be cloned.

CTS-967 (error) Unable to find master clock for generated clock

%s

DESCRIPTION

CTS is not able to find master clock corresponding to generated clock. This could happen because of incorrect clock definition of generated clock. Please check if generated clock source is on clock path or not.

WHAT NEXT

Please check clock definition of generated clock.

CTS-968 (Error) target_early_delay or target_skew constraint found for skew group %s.

DESCRIPTION

target_early_delay and target_skew constraints not supported for skew groups with dependencies on them or depending on other skew groups.

WHAT NEXT

remove these constraints.

CTS-969 (Error) Found independent sub-tree(s) for more than one skew groups below skew group %s.

DESCRIPTION

If a skew group depends on more than one skew groups, only one of them is allowed to contain pins in independent sub-tree.

WHAT NEXT

change the skew group definition to remove such pins.

CTS-970 (Warning) Specified reference %s can not be reset

DESCRIPTION

This warning message indicated that reset_clock_tree_reference command is not able to remove the specified reference cell. This could happen if specified reference cell is not part of reference list OR reference cell is part of reference list but the way it is being reset is not proper. If setting of reference was done using set_clock_reference -clock it can be reset using "reset_clock_tree_reference -clock" only, it can not be reset without -clock switch in reset_clock_tree_reference command. If setting of reference was done using set_clock_tree_reference without -clock it can be reset using reset_clock_tree_refernce without -clock only. For gates -size_only switch has to be given to reset_clock_tree_reference commands.

WHAT NEXT

Please check if specified reference cell is a part of reference list If specified reference is part of reference list, please check using what switches set_clock_tree_reference was done. Please use same set of switches to reset a reference cell

CTS-971 (Error) Clock gates can be specified using -sizing_only switch. Please check %s

DESCRIPTION

Clock gates will be used by optimization engine to size any preexsisting gate to user reference list. Clock gates can be given through -sizing_only switch only.

WHAT NEXT

Please add -sizing_only switch while specifying clock gate

CTS-972 (Information) Instance %s has exceptions %s on it and will not be sized

DESCRIPTION

This message indicated that the specified clock gate instance has an exception on it and will not be sized to any other equivalent clock gate from reference list

WHAT NEXT

This is an informational message only. No action is required on your part.

CTS-549 (Warning) Turning off -multi_mode_cts since is not compatible with -config_file_read.

DESCRIPTION

Multi mode CTS does not support -config_file_read.

WHAT NEXT

Use either -config_file_read or -multi_mode_cts for clock tree synthesis.

CTS-974 (warning) Clocks %s %s are overlapping clock which has different %s referneces

DESCRIPTION

Clock are overlapping clock and different references are specified. Under this union of references will be used in overlapping region

WHAT NEXT

Please reference settings done through set_clock_tree_refernce command.

CTS-975 (error) cell %s is not a reference cell for clock %s

DESCRIPTION

Cell is not a reference for clock %s

WHAT NEXT

Please check reference cell specified through set_clock_tree_reference command

CTS-976 (error) Incorrect spacing settings

DESCRIPTION

Spacing settings specified for EM aware CTS placement are incorrect. Spacing values should be greater then 0. Default value of spacing is 0 which means no spacings.

WHAT NEXT

Please specify a valid spacing value.

CTS-977 (error) Spacing value for clock %s and lib cell %s are already present

DESCRIPTION

Spacing values for specified clock and lib cell is already present. Please use remove_clock_cell_spacing and set_clock_cell_spacing command to reset the values. "default" value indicates global settings.

WHAT NEXT

Please use remove_clock_cell_spacing command to reset spacing setting and then reset using set_clock_cell_spacing command

CTS-977 (error) Spacing rules are not specified for %s %s

DESCRIPTION

This error comes when spacing rules are not specified for given clock and lib cell name Please check spacing settings using report_clock_cell_spacing. Setting specified with -clocks switch in set_clock_cell_spacing can be removed by -clocks switch in remove_clock_cell_spacing command and vice-versa. Same is true for lib cell settings

WHAT NEXT

Please check spacing settings using report_clock_cell_spacing command Please use remove_clock_cell_spacing with same switches as set_clock_cell_spacing command

CTS-977 (error) -all switch in remove_clock_cell_spacing command cannot be used with other switches

DESCRIPTION

"-all" switch in remove_clock_cell_spacing command should not be used with -clocks OR -lib_cells switch

WHAT NEXT

Please correct usage of remove_clock_cell_spacing command

CTS-1050 (Error) Net has %d load pins, it can’t make a route of shape %s.

DESCRIPTION

This error message occurs when the number of load pins on a net does not correlate to the route shape to be obtained on that net. For a net with 2 load pins, the possible route shape is either I or rotated-I (I_90). For such a net, H or rotated-H shaped route is not possible. Similarly for a net with 4 load pins, the possible route shape is either H or rotated H (H_90).

WHAT NEXT

Check the net connection details.

CTS-1051 (Error) Couldn’t find any suitable %s track for the route to connect the points (%g %g) and (%g %g).

DESCRIPTION

While connecting two points through wire, the tracks should be available to do the connection within the proximity. This error comes when no suitable tracks are found in the proximity for making such a connection.

WHAT NEXT

Check the physical design to verify of the tracks are available around that part of the design. In case, if only tried to route using the tracks aligned with the grids, may now be tried with off-grid tracks.

CTS-1052 (Error) Couldn’t create the H (or H_90) or I (or I_90) shaped route topology for the given net.

DESCRIPTION

This error message comes when for the given net, H or H_90 or I or I_90 route topology generation is not possible due to some reasons.

The topology generation may not be possible when the load pins can’t be connected using a route or the driver pin can’t be connected to the route. The unavailibility of suitable tracks, existence of blockages on the path might be the possible reasons.

WHAT NEXT

Check the physical design.

CTS-1053 (Error) Couldn’t create the H (or H_90) or I (or I_90) shaped route for the given net.

DESCRIPTION

This error message comes when for the given net, H or H_90 or I or I_90 the actual route generation is not possible due to some reasons.

The actual route generation may not be possible when the wires or vias can’t be instantiated in the required places due to blockages, routing rules etc.

WHAT NEXT

Check the physical design.

CTS-1054 (Warning) %s-shaped route is not possible for %d nets.

DESCRIPTION

This error message comes when for the given net is not suitable to have H or H_90 or I or I_90 shaped routes.

WHAT NEXT

Check the net connectivity and/or physical design constraints.

CTS-1055 (Warning) cell instance %s has invalid voltage area (%d).

DESCRIPTION

This error message comes when the given cell instance has invalid voltage area.

WHAT NEXT

Check and make sure the given cell instance is in valid voltage area, and check the voltage area setting.

CTS-1056 Unable to get total cap of %s.

DESCRIPTION

This error message comes when CTS cannot get valid capacitance value on the given net.

WHAT NEXT

Check the connectivity of the net, make sure the net is fully connected and legal.

CTS-1057 can not get location of pin %s.

DESCRIPTION

This error message comes when the given pin does not have a valid phsical location.

WHAT NEXT

Check and make sure the cell of the given pin is placed, and the pin is not netlink.

CTS-1058 Fail to find driver on net %s to %s.

DESCRIPTION

This error message comes when the given net does not have a valid driver pin.

WHAT NEXT

Check and make sure the net is not floating and has a valid driver pin.

CTS-1059 Per-clock exception can only be set for master clock.

DESCRIPTION

This error message comes when the given clock for the command set_clock_tree_exceptions -clock is a generated clock.

WHAT NEXT

Use the master clock of the generated clock to specify the clock. In the case that a pin is on a generated clock of another generated clock, use the highest ancestor clock (which is a master clock).

CTS-1060 (Warning) Option -multi_scenarios will be applied to all clocks.

DESCRIPTION

Option *-multi_scenarios* of **set_clock_tree_options** will be applied globally, not just for the specified clock.

WHAT NEXT

Use set_clock_tree_options -multi_scenarios only once before compile_clock_tree and optimize_clock_tree to turn on multi-mode CTS. It is not supposed to be combined with -clock_trees or -root.

CTS-1061 (Error) didn’t read in constraints for cell (%s).

DESCRIPTION

The lib cell (%s) is not in CTS reference cell, buffer cell, or delay cell list.

WHAT NEXT

Check and make sure the lib cell (%s) is in CTS reference cell list.

CTS-1062 (Error) no maximum transition delay defined.

DESCRIPTION

This error message comes when user didn’t define maximum transition.

WHAT NEXT

Define the maximum transition.

CTS-1063 (Warning) don’t touch sub-tree defined at pin %s.

DESCRIPTION

This error message comes during CTS initialization when the user define dont touch on the pin. CTS will still try to initialize the subtree of this pin.

WHAT NEXT

CTS-1064 (Warning) Cannot insert ignore pin guide buffer for net %s.

DESCRIPTION

This error message comes when ICC cannot find a legal location for the guide buffer inserted to isolate ignore pins.

WHAT NEXT

check core utilization, placement blockage, etc, and make sure there is room for the guide buffer to be inserted.

CTS-1065 (Warning) No guide buffer insertion for large cap pin %s. It has a pin cap larger than max_cap of any clock buffer.

DESCRIPTION

This error message comes when ICC cannot find a buffer from buffer list which can drive the large pin cap. A guide buffer will not be inserted in this case.

WHAT NEXT

Add in a larger buffer in CTS buffer/reference list may be necessary.

CTS-1066 (Warning) Failed to get the location of ILM port %s.

DESCRIPTION

This error message comes when ICC cannot find the location of an ILM port. Guide buffer will not be inserted.

WHAT NEXT

CTS-1067 (Warning) Cannot insert guide buffer for ILM port %s since net %s is a dont_buffer_net.

DESCRIPTION

This error message comes when ICC try to insert guide buffer for ILM port which is on dont buffer net.

WHAT NEXT

CTS-1068 (Warning) No bufferable net found to insert guide

buffer for ILM port %s.

DESCRIPTION

This warning message occurs when the ILM port is on a net which is not bufferable. Guide buffer will not be inserted.

WHAT NEXT

CTS-1069 (Warning) ignore routing on net %s.

DESCRIPTION

This warning occurs during CTS initialization when the net is already routed. CTS will not do initialization on this net.

WHAT NEXT

CTS-1070 (Warning) No bufferable net found to insert guide buffer for ILM port %s.

DESCRIPTION

This warning message occurs when the ILM port is on a net which is not bufferable. Guide buffer will not be inserted.

WHAT NEXT

CTS-1071 (Warning) %s pin is a hierachical pin without location. Setting float or stop pin exception is not supported.

DESCRIPTION

This warning message occurs when user tries to set float or stop exception on a hierachical pin without location. Since hierachical pins have no physical location, it is impossible for CTS to try to balance them.

WHAT NEXT

CTS-1072 (Information) No register met the timing/switching activity criteria for XOR clock-gating.

DESCRIPTION

This information message occurs when the XOR clock-gating engine cannot find any register (flip-flop) that is eligible for clock-gating as per the criteria required on the register in terms of timing slack or switching activity at its pins.

WHAT NEXT

Check to see if RTL-SAIF file was annotated on the design, as that might cause the switching activity information on the register pins to be inaccurate.

CTS-1073 XOR-CG: Required library cells (ICG/logic) not found.

DESCRIPTION

This error message occurs when the library cells required for XOR clock-gating cannot be found. The engine requires ICG cells, XOR cells, NAND cells, OR cells, Inverter cells and AND cells for clock-gating.

WHAT NEXT

Check to see if the required ICG and logic gate cells exist in the library.

CTS-1074 (Information) Register Clusters Created = %d in XOR clock gating.

DESCRIPTION

This information message gives the total number of XOR clock-gated register clusters that have been created in the design.

WHAT NEXT

CTS-1075 (Information) Totals Registers XOR Clock-Gated = %d

DESCRIPTION

This information message gives the total number of registers (flip-flops) that have been XOR clock-gated.

WHAT NEXT

CTS-1076 (Information) Total flip-flops for XOR clock-gating in the design = %d

DESCRIPTION

This information message gives the total number of flip-flops that exist in the design.

WHAT NEXT

CTS-1077 (Information) Total flip-flops %d of unsupported type for XOR clock-gating.

DESCRIPTION

This information message gives the total number of flip-flops that belong to a type that is not supported presently by the XOR clock-gating engine.

WHAT NEXT

CTS-1078 XOR-CG: ICG library cell marked as dont_use/

dont_touch. Check attribute on library cell

DESCRIPTION

This error message occurs when the ICG library cells have been marked as dont_use/ dont_touch which prevents ICG cells from getting appropriately sized. The XOR clock-gating engine requires the user to ensure that ICG library cells are usable.

WHAT NEXT

Please check the library cell attributes

CTS-1079 XOR-CG: Largest ICG does not have adequete drive strength for self-gating

DESCRIPTION

This error message occurs when the largest available ICG in the library does not have adequete drive strength to drive a cluster of registers being XOR clock-gated. This poses a significant DRC hazard and hence we avoid XOR clock-gating in this case.

WHAT NEXT

Check to see if the drive strength of the largest ICG cells is appropriate or that the ICG cells in the library are large enough to drive a cluster of gates.

CTS-1080 XOR-CG: ICG library cell could not be identified in the library

DESCRIPTION

This information message occurs when no ICG library cells could be found by the XOR clock-gating engine.

WHAT NEXT

Please check to ensure that appropriate ICG cells are present in the library.

CTS-1081 (Warning) Reset user switching activity annotation on

pin %s of XOR clock-gated register %s

DESCRIPTION

This information message occurs when the clock-pin of a register that is XOR clock-gated has a user switching activity annotation (from SAIF/VCD file). If this reset is not done, the power computation of the register would be erroneous. Also, the user must be careful about re-annotating the design with the same SAIF file as that would again over-ride the XOR clock-gating based switching activity and lead to erroneous computation.

WHAT NEXT

CTS-1082 (Information) Flip-Flop %s of library cell type %s is not supported for XOR clock-gating.

DESCRIPTION

This information message occurs when the design has a flip-flop of library cell type that is not supported by the XOR-CG engine.

WHAT NEXT

CTS-1083 (Warning) don’t touch sub-tree defined at pin %s.

DESCRIPTION

This warning message occurs when there is a don’t touch sub-tree exception defined at this pin. As a result of this exception, CTS will not touch or modify the clock network downstream of this pin.

WHAT NEXT

Make sure this don’t touch sub-tree is user expected.

CTS-1084 (Warning) Some clocks are not listed in the -clock_trees list, and Multi_mode CTS may not be able to get the

best result.

DESCRIPTION

This warning message occurs when user did not list all the real clocks of all the cts-mode scenarios. Because only a subset of clocks are being synthesized, it may result in bad QoR for the clocks not listed, and also large DRC violations. Doing so with Multi-mode CTS is not taking advantage of the benefits of multi-mode CTS.

WHAT NEXT

Make sure that the ’-clock’ list all the master clocks of all the cts-mode scenarios.

DB

DB-1 (error) File is not a DB file.

DESCRIPTION

The identified file was not in the DB file format.

WHAT NEXT

Check to see what format the file is in, and read it with the appropriate command. For example, edif files can be read into **dc_shell** with the **read -format edif <filename>** command.

DB-3 (warning) Can’t locate file ’%s’.

DESCRIPTION

This warning message will be printed out the first time if we can not resolve a link to a given file. In the absense of the given file, there will be some unresolved references.

WHAT NEXT

Check the link_library and the search_path variables and set their value accordingly.

DB-4 (error) Open gen_state (0x%x) -- %s object ’%s’ (0x%x) attach ’%s’ id = %d

DESCRIPTION

WHAT NEXT

DB-5 (error) Limit exceeded: Cannot create attribute %s for

class %s, so program cannot continue.

DESCRIPTION

This message appears when the internal limit of 32k attributes per database object is exceeded. Once this limit is exceeded, work in progress cannot be saved and the program cannot continue.

WHAT NEXT

Check the scripts to see if an excessive number of **create_attribute** commands are run with unique attribute names. Try to reuse names where possible. If many scripts are run in one large session, attempt to break up the single long run into a number smaller runs, saving your work each time.

DB-6 (error) Limit exceeded: Cannot create attach %s for class %s, so program cannot continue.

DESCRIPTION

This message appears when the internal limit of 32k types of attaches per database object is exceeded. Once this limit is exceeded, work in progress cannot be saved and the program cannot continue.

WHAT NEXT

If many scripts are run in one large session, attempt to break up the single long run into a number smaller runs, saving your work each time.

DBCK

DBCK-1 (error) Line is not connected to anything - Sheet: %s.

DESCRIPTION

WHAT NEXT

DBCK-2 (error) Endpoint of a line touches a line of another net - Sheet: %s.

DESCRIPTION

WHAT NEXT

DBCK-3 (error) Schematic has coexistent lines of different nets - Sheet: %s.

DESCRIPTION

WHAT NEXT

DBCK-4 (information) Input cell/pin (%s) is not driven, assumed to be shorted to logic 0.

DESCRIPTION

All unconnected input pins that are not driven are assumed to be shorted to logic 0. This assumption applies only to cells explicitly named by the designer. Unconnected inputs to cells that are allocated during the synthesis process are shorted to logic 0, but this message is suppressed. This situation can cause the results of synthesis to differ from those of simulation.

WHAT NEXT

DBR-001 (error) Cannot read file '%s'.

DESCRIPTION

The file you specified either does not exist or you do not have read access to the file.

WHAT NEXT

Check the search_path or use the **file** command to verify the existence and other attributes of the file.

DBR-002 (information) Errors reading file '%s'.

DESCRIPTION

Errors occurred while reading the specified file.

WHAT NEXT

Check previous messages, which indicate what went wrong and what action you can take to correct the problem. If there are no messages preceeding DBR-002, then the file is most likely corrupt.

DBR-003 (warning) Design '%s' (file '%s') is already registered. Remove the design before rereading.

DESCRIPTION

While reading a design from a file, that design/file combination was found in memory. This means that the file was read previously.

WHAT NEXT

If the file has changed and you want to reread it, remove the design using the **remove_design** command, then reread the file.

DBR-004 (warning) Library '%s' (file '%s') is already registered.

DESCRIPTION

While reading a DB file, a library/file combination that is already in memory was found. This means that the file was read previously.

WHAT NEXT

If the file has changed and you want to reread it, you can remove the library using the **remove_lib** command, then reread the file. However, in the process, if a linked design references this library, that design will need to be unlinked and will need to be completely rebuilt.

DBR-005 (information) Design '%s' not loaded.

DESCRIPTION

While reading in a design, some inconsistencies were found, so the design was not loaded. It's likely that the db file has errors, such as multiple nets with the same name on a single design.

WHAT NEXT

Check previous messages which will indicate what went wrong, and what action you can take to correct the problem. Usually, the application which created the db is the cause.

DBR-006 (error) Unknown pin '%s' makes instance '%s' of '%s' in design '%s' inconsistent with previous instances.

DESCRIPTION

While reading in a design, an instance of a design is inconsistent with previous instances because a pin is not found.

WHAT NEXT

Make sure that the DB is valid.

DBR-007 (warning) Found unsupported LSI reference '%s' to '%s' in design '%s'.
The linker will not be able to resolve this reference.

DESCRIPTION

While reading in a design, an instance of a design was found to be derived from an LSI netlist. This tool only supports fully name-based references from LSI netlists. Order-based or mixed order and name based references are not supported.

WHAT NEXT

Use another Synopsys tool to read the DB, link it, and write it out to a new DB file. This will resolve the naming issue.

DBR-008 (error) Cannot remove library '%s':

DESCRIPTION

The library contains objects which are being referenced. For example, some cells may used in the current design, or a wire load model may be in use. If a QTM model is being created, and it is referencing the library, then it must be saved before the library can be removed.

Each reason why the library cannot be removed is listed.

WHAT NEXT

Remove the designs with the **remove_design** command before using **remove_lib**, since a design is the source of most library references. Other causes, like QTM model creation, may require other actions.

DBR-009 (warning) Found name-based LSI reference '%s' to '%s' in design '%s'.
The linker might not be able to resolve this reference.

DESCRIPTION

While reading in a design, an instance of a design was found to be derived from an

LSI netlist. The reference is fully name-based. However, even in the case of name-based references, the linker might not be able to resolve references. The LSI netlist allows unconnected pins to be omitted from the reference, so, for example, an FD1 with D, CP, and Q pins connected, would be represented with the QN pin missing. The linker will indicate that the reference has too few ports.

WHAT NEXT

Use another Synopsys tool (like Design Compiler) to read the DB, link it, and write it out to a new DB file. This will resolve the missing pins issue.

DBR-010 (error) Cannot access temp directory '%s'%s.

DESCRIPTION

The read process utilizes a temporary directory to create transient files. These files are deleted when the read process completes. The name of the directory is found in the variable 'pt_tmp_dir'. In this case, the program was unable to create files in that directory.

WHAT NEXT

Verify that the specified directory exists, is writeable, and that the disk has some space available. If no space is available, try setting pt_tmp_dir to an alternate directory.

DBR-011 (error) Problem in read_%s: %s.

DESCRIPTION

The read process detected an error, which is detailed in the message. Some are intermediate file problems (see DBR-010); others are process related. For example, if the message indicates "invalid access", it means that the command is not being used correctly.

WHAT NEXT

Action based on the message text.

DBR-012 (error) Cannot read design db files. A db file must be

a library.

DESCRIPTION

Reading designs in the db format is not supported. Reading of db files is supported for libraries only.

WHAT NEXT

Do not read files containing designs in db format. Use other supported formats for reading design files.

DBR-013 (error) read_min_max_lib can only merge libraries.

DESCRIPTION

The **read_min_max_lib** can only be used to read and merge two library DBs - one min library, and one max library.

WHAT NEXT

Check the arguments provided to command read_min_max_lib.

DBR-014 (error) multiple libraries in a single DB not supported.

DESCRIPTION

Command read_min_max_lib can only be used on a DB file which contains multiples libraries.

WHAT NEXT

Check the arguments provided to command read_min_max_lib.

DBR-015 (warning) Ignoring degenerated cell '%s' from library

’%s’.

DESCRIPTION

This message warns you that PrimeTime has found a degenerated cell in the library and is ignoring it.

WHAT NEXT

This is a warning message only. No action is required on your part.

DBR-016 (error) Cannot find port ’%s’ for cell ’%s’ in all libraries.

DESCRIPTION

You receive this message because PrimeTime has found the specified port in either the min or max condition library db file but not the other. The ports of the library cells in the min and max condition libraries must be identical.

WHAT NEXT

Examine the min and max condition libraries and ensure that they contain the same set of library cells with the same ports.

DBR-017 (error) Cannot find %s ’%s’ in all libraries.

DESCRIPTION

You receive this message because PrimeTime has found the specified cell in either the min or max condition library db file but not the other. The library cells in the min and max condition libraries must be identical.

WHAT NEXT

Examine the min and max condition libraries and ensure that they contain the same set of library cells.

DBR-018 (error) %s value ’%g’ of operating condition ’%s’ is

different from the nominal %s value '%g'.

DESCRIPTION

You receive this message if PrimeTime finds the specified operating condition value in either the min or max condition library db file and that value is different from the nominal value.

WHAT NEXT

Ensure that all operating conditions in the min and max library db files are nominal.

DBR-019 (error) Cannot find operating condition '%s' in library '%s'.

DESCRIPTION

You receive this message because the operating condition you specified cannot be found in the specified library.

WHAT NEXT

Use the **report_lib** command to list the operating conditions in the specified library. Then re-execute the command, using only the available operating conditions.

DBR-020 (information) Renamed scalar %s '%s' to '%s' in design '%s'.

DESCRIPTION

While reading a Verilog file with PrimeTime's native Verilog reader, two net or port names were found to be in conflict, requiring one of the objects to be renamed. This can occur for one of two reasons: an ambiguous bus naming style or escaped names.

Given a bus_naming_style of "%s%d" and the following verilog port declarations:

```
output z1;
output [1:0] z;
```

the bus reference z[1] infers a port named z1. This conflicts with the scalar port

z1, declared with the first output statement.

The second case can be shown with the following verilog wire declarations:

```
wire \z[1];
wire [1:0] z;
```

Assuming the default bus_naming_style of "%s[%d]", the problem here is that bus reference z[1] infers a net named z[1], and so does the scalar declaration.

WHAT NEXT

No action is required. This is an informational message.

DBR-021 (warning) Library file '%s' is already registered.

DESCRIPTION

You tried to read a library DB file which has already been loaded into memory.

WHAT NEXT

If the file has changed and you want to reread it, you can remove the library using the **remove_lib** command, then reread the file. However, in the process, if a linked design references this library, that design will need to be unlinked and will need to be completely rebuilt. If you were using **read_min_max_lib**, then using the -force option will do all of this for you.

DBR-022 (error) Template %s is not the same in min and max libraries.

DESCRIPTION

The two libraries given to command read_min_max_lib contain a template of the same name but different content. Two templates must be the same to allow use of the cell lookup tables from two libraries as one min-max table. This is both an implementation limitation and a feature to improve performance of delay calculation. Two templates are considered same if the variables and indices have same name and same order, same size of the array for each index, and each index value is the same.

WHAT NEXT

Check the libraries provided to command read_min_max_lib. They should contain same templates. The easiest way to achieve this is to do textual difference on the two .lib files and make sure that the sections describing templates are absolutely the same (excluding blanks and formating). In case when the templates differ you will have to choose one of the sets of templates, put it into the other .lib file, and manually or using a script recalculate all cell delay tables in that library to conform to the new templates. Another way is to set options in the characterization tool that generates .lib files to use a fixed template for both libraries if such option is available.

DBR-023 (error) Duplicate reference port '%s/%s' in module %s ending at line %d in %s

DESCRIPTION

While reading a Verilog file with PrimeTime's native Verilog reader, an instance was found where a scalar port and a bus port in the terminal list are in conflict because of the bus_naming_style. For example:
BOX i0 (.DATA1(a), .D({c ,d}), .\D[1] (b), .Z(z));
Here, the scalar port D[1] and the bus port D[1] are in conflict if the bus_naming_style is %s[%d]. If the bus_naming_style is %d(%d), there is no conflict. This is an error because renaming reference ports is unpredictable, and therefore, not supported.

WHAT NEXT

Either change the bus_naming_style or investigate how such a conflict was introduced into your netlist.

DBR-024 (warning) Can't connect pin '%s' to net '%s' in design '%s': already connected to net '%s'

DESCRIPTION

An attempt was made to connect a pin to a net and the pin is already connected to a net. This is typically an error in the netlist, such as a duplicated connection. For example, this message would be generated when reading an EDIF file which has a construct similar to this:

```
(net d
  (joined
```

```
       (portRef d)
       (portRef D (instanceRef n1))
       (portRef D (instanceRef n1))
      )
     )
```

WHAT NEXT

This is a warning indicating that the connection was ignored, so no specific action is necessary.

DBR-026 (error) Unable to create %s '%s' in design '%s'

DESCRIPTION

While reading in a design, an object (such as a port, cell, or net) could not be created. It's likely that the db file has errors, such as multiple nets with the same name on a single design. The object name and design name are given in the message. Such an error will cause the loading of the design to fail, although other designs in the file which do not exhibit problems will be loaded.

WHAT NEXT

Usually, the application which created the db is the cause.

DBR-030 (error) Invalid global reference '%s' - %s in module ending at line %d in %s

DESCRIPTION

You receive this message if PrimeTime finds an invalid global reference while reading a Verilog file with PrimeTime's native Verilog reader. A global reference is a connection to a wire in another module. PrimeTime's native Verilog reader puts several restrictions on the use of global references. For a reference of the form **module.wire**, all of the following must be true:

- The module must exist in the file being read.
- The module must precede the module that is making the reference.
- The wire must exist in the module.

• The wire must be a logic constant.

Any deviation from these rules generates this error message.

WHAT NEXT

There is no other support for global signals. You must remove them from your netlist.

DBR-031 (error) Attribute '%s' cannot be imported: You defined it as %s; db defines it as '%s'.

DESCRIPTION

You receive this error message because while reading an attribute from db, there was a mismatch between the type (integer, string, etc.) that db defines for the attribute and the type that PrimeTime defines for the attribute. Usually, this is a user-defined attribute, defined with the **-import** option on **define_user_attribute**, and the types do not match.

WHAT NEXT

Rerun PrimeTime and define the attribute correctly. You might need to use other Synopsys applications to determine the actual type of the attribute.

DBR-032 (information) Ignoring library cell '%s' which does not have any pins defined on it.

DESCRIPTION

This message indicates that while reading the library, PrimeTime detects that the named library cell does not have any pins defined on it. Library cells without pins are ignored and not loaded because they do not have any effect in the timing analysis.

WHAT NEXT

There is no user actions required unless you think the indicated cell should have pins. If so, you need to go back to the original source of the library in order to fix it.

DBR-033 (warning) Found bad bus definition for '%s' - %s.

DESCRIPTION

This message indicates that while reading the DB file, PrimeTime detected that the named bus definition is wrong or not consistent. PrimeTime may not be able to properly link the design due to this problem.

WHAT NEXT

Normally, this indicates errors in the DB file. Please fix the bus definition in the DB file by going back to the source of the DB file and regenerate it from the tools originally created this DB file.

DBR-040 (error) Design '%s' was not found in '%s'

DESCRIPTION

You receive this message because **swap_cell** loaded the file you specified using the **-file** option, but did not find the specified design in the file. This error could be caused by a misspelling or typo in the design name or filename, or both; or by inadvertently specifying a file that does not contain the intended design.

WHAT NEXT

Examine the file, verify that the intended design name is contained in the file, and note the spelling of the design name. Then re-execute **swap_cell** using the correct design and file names.

DBR-050 (warning) Number of state table inputs for %s/%s/%s (%d) exceeds %d.

DESCRIPTION

During the reading of a sequential cell from a DB library, an output pin was found with a state table for more than 16 inputs. This message warns you that the presence of this cell with its large state table will degrade read performance, because processing is exponential.

WHAT NEXT

This is a warning message only. No action is required on your part.

DBR-051 (error) Too many table inputs for %s/%s/%s (%d). State table information ignored in this case.

DESCRIPTION

During the reading of a sequential cell from a DB library, an output pin was found with a state table for more than 30 inputs. PrimeTime cannot load state table information for more than 30 inputs, and is ignoring this information.

WHAT NEXT

Consult the Library Compiler documentation for alternatives to storing state tables.

DBR-060 (error) Can’t set min library to %s.

DESCRIPTION

You receive this message if the min library you passed to **set_min_library** is invalid. For example, the min library you specified might have been the same as the max library, or it might have already been used as the max library in a **set_min_library** command. The max and min libraries must be different. The message text will indicate the condition.

WHAT NEXT

Re-execute **set_min_library** and specify a valid min library.

DBR-061 (information) ’%s’ already has ’%s’ as its min library.

DESCRIPTION

The min library you passed to **set_min_library** has already been related to the max library using **set_min_library**.

WHAT NEXT

This is an informational message only; no action is required on your part. However,

if you intended to change the relationship of the max library to a different min library, check the spelling of the min library argument and re-execute the command if necessary.

DBR-062 (warning) Cannot create max/min library cell relationship for '%s': %s.

DESCRIPTION

The **set_min_library** command found a library cell in the min library that matches the library cell in the max library. However, some aspect of the two library cells is different. For example, one might have more pins than the other; the pins might be in a different order; or the timing arcs might be different. The text of the message states the most serious difference. To create a max/min library cell relationship, both cells must have the same timing arcs and the same pins, with the same order and direction.

For cells where the max/min relationship fails, as in the current situation, the command uses a minimum condition delay calculation based on the max library. If even one of the library cell pairs matches and compares correctly, the **set_min_library** command continues executing and succeeds.

WHAT NEXT

This is a warning message; no action is required on your part. However, you should read the message text to determine why the cells are different, and ensure that the max and min libraries are compatible.

DBR-063 (warning) No match for %s/%s in library '%s'.

DESCRIPTION

The **set_min_library** command could not find a library cell in the min library that matches the specified library cell in the max library. Therefore, a max/min library cell relationship cannot be created for that cell.

For cells where the max/min relationship fails, as in the current situation, the command uses a minimum condition delay calculation based on the max library. If even one of the library cell pairs matches and compares correctly, the **set_min_library** command continues executing and succeeds.

WHAT NEXT

This is a warning message; no action is required on your part. However, you should

determine why there is not a match for the specified cell, and ensure that the max and min libraries are compatible.

DBR-100 (information) Ignoring external links found in design '%s' (file '%s') because dbr_ignore_external_links is set to true.

DESCRIPTION

You receive this message if your design contains external links but the **dbr_ignore_external_links** variable is set to *true*. In this case, the application ignores the external links and instead searches for an object by name only in the libraries in the **link_path**.

External links are created by Design Compiler in certain situations when writing a DB file; for example, when there is a link from a design to a wire load model in a library. The external link records information about the library to which the wire load was linked. Operating conditions can also have external links created for them.

You would set the **dbr_ignore_external_links** variable to *true* if you wanted to use a different library in PrimeTime than was used in Design Compiler.

WHAT NEXT

If you intended for the external links to be ignored, no action is required on your part. Otherwise, set the **dbr_ignore_external_links** variable to *false* and reexecute the application.

DBR-101 (warning) Pin '%s' is not found on library cell '%s'. Generated clock defined on this pin will not be created.

DESCRIPTION

While reading in a design, a generated clock definition has been found for a library cell, but the source pin of the generated clock does not exist on that library cell. Thus, the generated clock will not be created if this was the only source pin of the generated clock.

WHAT NEXT

The Synopsys database format (.db) appears to be incorrect. Please recreate the database with the correct source pin name for the generated clock.

DBR-200 (warning) Cannot read DDC attribute %s for design %s.

DESCRIPTION

The specified attribute could not be read for the given design. The attribute is ignored.

WHAT NEXT

Modify the design in the tool that generated the DDC file so that it does not generate this attribute.

DBR-201 (warning) Unknown pin direction in DDC for pin %s

DESCRIPTION

The DDC file has a pin direction that PrimeTime does not recognize. It uses the internal direction for such pins.

WHAT NEXT

Change the design so that the tool that generates the DDC file does not generate the bad pin direction.

DBR-202 (error) Scenario name %s supplied when no scenarios stored

DESCRIPTION

A **read_ddc** command was issued with a scenario name argument, but there were no scenarios stored in the DDC file.

WHAT NEXT

Either re-generate the DDC rile with the scenario, re-issue the **read_ddc** command as *-netlist_only* to ignore all constraints, or re-issue the **read_ddc** command without the scenario to pick up the non-scenario constraints.

DBR-203 (error) Scenario name %s did not match an available

scenario %s.

DESCRIPTION

A **read_ddc** command was issued with a scenario name that did not match any of the scenarios in the DDC file. A list of available scenarios is listed.

WHAT NEXT

Choose one of the available scenarios and re-issue the **read_ddc** command with the chosen scenario.

DBR-204 (error) File %s is not in DDC format.

DESCRIPTION

The **read_ddc** command was issued for the given file, but the file is not in DDC format.

WHAT NEXT

Either remove the file from the **read_ddc** command, or generate the file as a DDC file.

DBR-205 (error) File %s has too old a version for PrimeTime to read.

DESCRIPTION

PrimeTime cannot read the given file because the DDC version number is too old.

WHAT NEXT

Convert the DDC file to a new version. Simply read the file into a tool that can write DDC (such as DC), then write the file out again. The tool will write it out as a new version.

DBR-206 (Warning) The library has non-continuous base curves and can have a negative impact on PrimeTime’s

performance and memory.

DESCRIPTION

The base-curve ids for the CCS library that is used is not numbered continuously. For eg, the curve_y ids for the base curves in the library are (1, 2, 5, 6, 7 ..) instead of the recommended sequential ordering (1, 2, 3, 4, 5, ...). Such libraries can cause a negative impact on performance and memory of PrimeTime.

WHAT NEXT

Use the latest version of Library Compiler to get a compatible version of the library.

DBRBO-1 (error) Attribute ’%s’ does not have valid values.

DESCRIPTION

This might have occurred because you incorrectly set this attribute or is internal to the program. Regardless, the attribute is considered as "not set", and its effect is nil.

WHAT NEXT

DBSEC-1 (error) Can’t read %s; it contains protected data generated by %s.

DESCRIPTION

The information in the database file is protected and cannot be read by the tool that issued this error message.

WHAT NEXT

Check the manual of the tool that generated the protected data to determine which Synopsys tools may access it.

DBVH-1 (warning) Time units are not specified in the '%s' library.

DESCRIPTION

This message is given if the technology library does not have the **time_unit** attribute specified.

The optional **time_unit** attribute is used by the VHDL library generator to identify the physical time unit used in the generated library.

The physical time unit defaults to 1 nanosecond.

WHAT NEXT

Add the **time_unit** attribute to the technology library to explicitly specify the physical time units of the library.

```
library(dbvh1) {
  time_unit : "10ns";
  ...
}
```

EXAMPLE MESSAGE

```
Warning: Time units are not specified in the 'dbvh1' library. (DBVH-1)
```

DBVH-2 (error) The '%s' library contains no valid library cells.

DESCRIPTION

A correct VHDL model could not be created for any one of the library cells. There is at least one VHDL generation error for each library cell. Because the resulting VHDL files are of no use, all generated VHDL files are deleted.

This error is issued when all VHDL models generated for the specified architectures are incorrect.

WHAT NEXT

Correct the invalid library cells.

EXAMPLE MESSAGE

```
Results summary:
  Total cells in library           = 1
Error: The 'dbvh2' library contains no valid library cells. (DBVH-2)
```

DBVH-3 (warning) The '%s' pin on the '%s' cell has duplicate timing constraints.
Only one of them is used.

DESCRIPTION

The pin on the library cell has more than one timing constraint of the same **timing_type** with the same related pins.

The VHDL generator warns that an error might have been made. Only the first unique constraint is accepted, while all following constraints are ignored.

This warning pertains only to the full-timing structural, optimized gate-level, and VITAL models. The unit-delay structural models ignore timing.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning.

Otherwise, include only the timing arc that belongs in the simulation model in the technology library. If possible, remove all duplicates.

DBVH-4 (warning) The '%s' pin on the '%s' cell has duplicate timing arcs.
Only one of the timing arc is used.

DESCRIPTION

The pin on the library cell has, with the same related pins, more than one timing arc of the same **timing_type**.

Although the synthesis tools support multiple timing arcs, the VHDL generator does not.

The VHDL generator warns the user that an error might have been made. Only the first unique timing arc is accepted, while all following ones are ignored.

This warning pertains only to full-timing structural, optimized gate-level, and

VITAL models. Unit-delay structural models ignore timing.

During the **read_lib** command, a similar warning (LBDB-242) gives you the line numbers of the duplicate timing arcs.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning. Otherwise, include in the technology library only the timing arc that belongs in the simulation model. If possible, remove all duplicates.

EXAMPLES

```
    cell(dbvh4) {
  area : 7
  pin(D P CP) {
    direction : input;
    capacitance : 1;
  }
  ff ("IQ","IQN") {
      next_state : "D";
      clocked_on : "CP P";
  }
  pin(QN) {
    direction : output;
    function : "IQN";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 4.0000;
      intrinsic_fall : 2.0000;
      rise_resistance : 0.1000;
      fall_resistance : 0.1000;
      related_pin : "CP";
    }
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 3.0000;
      intrinsic_fall : 3.0000;
      rise_resistance : 0.1000;
      fall_resistance : 0.1000;
      related_pin : "CP P";
    }
  }
    }
```

In this case, the ’rising_edge’ timing_type is defined twice. During the VHDL generation, only the first occurrence is used.

EXAMPLE MESSAGE

```
Warning: The ’QN’ pin on the ’dbvh4’ cell has duplicate timing arcs.
        Only one of them is used. (DBVH-4)
```

DBVH-5 (warning) The ’%s’ pin has an invalid timing type related to ’%s’.
The invalid timing arc is ignored.

DESCRIPTION

This warning is given for any one of the following conditions:

- The pin is an input and has a timing arc.
- The pin is an output and has a timing constraint.
- The pin is a non-tristatable pin and has a disable timing group.
- The pin has a timing arc with an unrecognized timing type.

This warning is issued if any of the above conditions occur. As a result, the VHDL generator ignores the illegal timing arc or constraint.

This warning pertains only to full-timing structural, optimized gate-level, and VITAL models. Unit-delay structural models ignore timing.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning. Otherwise, correct the illegal timing arc or timing constraint.

EXAMPLES

```
cell(dbvh5) {
  area : 9;
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : preset;
      intrinsic_rise : 0.9;
      intrinsic_fall : 0.9;
      related_pin : "CP";
    }
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
    min_period : 3.0
  }
```

```
}
```

In this case, ’D’ is an input pin and has a ’preset’ timing_arc.

EXAMPLE MESSAGE

```
Warning: The ’D’ pin has an invalid timing type related to ’CP’.
        The invalid timing arc is ignored. (DBVH-5)
```

DBVH-6 (error) The ’%s’ pin is unused in the ’%s’ sequential cell.

DESCRIPTION

An input pin in the sequential library cell is not part of the function of any output.

If an input pin to a sequential library cell is unused, Library Compiler forces the library cell to become a black box. As a result, the VHDL generator cannot determine the function for this cell and can only generate a black box template.

Therefore, the VHDL generator creates a black box template for the optimized gate-level and VITAL simulation models, and an empty cell for both the unit-delay and full-timing structural models.

WHAT NEXT

Either remove the unused pin or use it in an output function.

EXAMPLES

```
cell(dbvh6) {
  area : 9;
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : preset;
      intrinsic_rise : 0.9;
      intrinsic_fall : 0.9;
      related_pin : "CP";
    }
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
    min_period : 3.0
  }
}
```

EXAMPLE MESSAGE

```
Error: The 'D' pin is unused in the 'dbvh6' sequential cell. (DBVH-6)
```

DBVH-7 (error) Missing timing arc between '%s' and '%s' pins in the '%s' cell.

DESCRIPTION

An output pin lacks a timing arc related to an input pin, which is in the output pin's function.

Synthesis allows output pins in sequential library cells to lack timing arcs to asynchronous inputs. For example, you can omit clear-to-output arcs for a flip-flop, and data-to-output arcs for a latch. Simulation requires a timing arc between each output pin and all its functionally dependent input pins.

A full-timing structural model always makes a best guess for the missing timing arc and continues.

This warning pertains only to full-timing structural models. Unit-delay structural models ignore timing.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning. Otherwise, add the missing timing arc to the technology library.

EXAMPLES

```
    cell(dbvh7) {
area : 16;
bundle( D ) {
members( D_1 D_2 );
capacitance : 1.0;
direction : input;
    }
pin( CLK ) {
capacitance : 1.0;
direction : input;
}
bundle( Q ) {
members( Q_1 Q_2  );
direction : output;
function : "IQ";
}
ff_bank( IQ, IQN, 2) {
next_state : "D";
clocked_on : "CLK";
}
```

```
   }
```

EXAMPLE MESSAGE

```
Error: Missing timing arc between 'D_1' and 'Q_1'  pins in the 'dbvh7' cell. (DBVH-
7)
```

DBVH-8 (warning) The '%s' pin on the '%s' cell has no 'function' attribute.

DESCRIPTION

The pin on the library cell is missing a **function** attribute. It is not a pull-up or pull-down pin, it does not have a three_state attribute, and it does not have any related timing arcs.

As a result, the output pin is at a constant logic state of unknown X. The pin is initialized to the constant logic state during the entity declaration.

This message pertains to all architectures.

WHAT NEXT

If the output pin is not at a constant logic state, define a **function** attribute for the pin in the technology library.

EXAMPLES

```
    cell(dbvh8) {
area : 3;
pin(A) {
    direction : input;
    capacitance : 2;
}
pin(Z) {
    direction : output;
    timing() {
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "A";
    }
}
    }
```

EXAMPLE MESSAGE

```
Warning: The 'Z' pin on the 'dbvh8' cell has no 'function' attribute. (DBVH-8)
```

DBVH-9 (warning) The '%s' pin on the '%s' cell has an unknown direction.
The direction defaults to inout.

DESCRIPTION

The VHDL generator must be able to recognize the direction of each pin. The pin on this library cell has an unknown direction, and the VHDL generator assumes the direction to be **inout** (the most flexible choice).

This message pertains to all architectures.

WHAT NEXT

Clearly define the direction of every pin in the technology library.

DBVH-10 (warning) The '%s' function on the '%s' pin in the '%s' cell is not recognized.

DESCRIPTION

The pin's function in the library cell is not internally recognized. Either the **function** attribute is an empty string or a sequential output does not follow one of the internal variables.

The format of the **function** attribute is not clear to the VHDL generator, which assumes that the library cell passed Library Compiler.

The **function** attribute is ignored; the pin is unknown.

This message pertains to all architectures: full-timing structural, unit-delay structural, optimized gate-level, and VITAL models.

WHAT NEXT

Modify the **function** attribute to follow the syntax the VHDL generator accepts. It must be a non-empty string and, if sequential, must follow one of the internal variables.

DBVH-11 (warning) The '%s' pin has an unsupported constraint related to '%s'.
The invalid timing arc is ignored.

DESCRIPTION

The library cell is a flip-flop with one of the following invalid conditions:

* A pin has a timing constraint related to a clock input.
* A pin has a non-recovery timing constraint related to an
  asynchronous input.
* A pin has a recovery timing constraint related to a
  non-asynchronous input.

The timing constraint is thus invalid, and the VHDL generator checks for invalid timing constraints. Either you were trying to use a timing constraint for an unsupported purpose, or the timing constraint was incorrectly identified. In either case, the invalid timing constraint is ignored.

This warning pertains only to full-timing structural, optimized gate-level, and VITAL models. Unit-delay structural models ignore timing.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning. Otherwise, either remove the invalid timing constraint from the technology library or correctly identify it.

EXAMPLES

```
    cell(dbvh11) {
      area : 9;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(CP) {
direction : input;
capacitance : 1;
timing() {
  timing_type : recovery_rising;
  intrinsic_rise : 1.17;
  intrinsic_fall : 0;
  related_pin : "D";
}
      }
      ff("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
      }
```

```
      pin(Q) {
direction : output;
function : "IQ";
      }
    }
```

In this case, The clock input pin ’CP’ has a timing constraint.

EXAMPLE MESSAGE

```
Warning: The ’CP’ pin has an unsupported constraint related to ’D’.
        The invalid timing arc is ignored. (DBVH-11)
```

DBVH-12 (warning) The ’%s’ cell has constraints with both rise and fall edges.

DESCRIPTION

The library cell has a timing constraint related to both the rising edge and the falling edge of the same related input.

The VHDL generator recognizes a pin to be related to only one edge of another pin. The activation edge of the related input can be either the rising edge or the falling edge, but not both.

The trigger edge is assumed to be the last one encountered. The previous rising or falling edge constraints are ignored. The generated VHDL code is commented to indicate the choice.

This warning pertains only to the full-timing structural, optimized gate-level, and VITAL models. The unit-delay structural models ignore timing.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning. Otherwise, correct the technology library to reflect a consistent activation timing edge. Make alltiming arcs for each related input consistently rising or consistently falling.

EXAMPLES

```
    cell(dbvh12) {
      area : 5;
      pin(D) {
direction : input;
capacitance : 1;
timing() {
  timing_type : setup_rising;
  intrinsic_rise : 0.5;
  intrinsic_fall : 0.5;
```

```
  related_pin : "G";
}
timing() {
  timing_type : hold_falling;
  intrinsic_rise : 0.4;
  intrinsic_fall : 0.4;
  related_pin : "G";
}
      }
      pin(G) {
direction : input;
capacitance : 1;
      }
      pin(CD) {
direction : input;
capacitance : 1;
      }
      latch ("IQ","IQN") {
data_in : "D" ;
enable : "G" ;
clear : "CD'" ;
      }
      pin(Q) {
direction : output;
function : "IQ";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.07;
  intrinsic_fall : 0.94;
  rise_resistance : 0.1523;
  fall_resistance : 0.0718;
  related_pin : "G";
}
timing() {
  intrinsic_rise : 1.07;
  intrinsic_fall : 0.94;
  rise_resistance : 0.1523;
  fall_resistance : 0.0718;
  related_pin : "D";
}
timing() {
  timing_type : clear;
  timing_sense : positive_unate;
  intrinsic_rise : 1.07;
  intrinsic_fall : 0.94;
  rise_resistance : 0.1523;
  fall_resistance : 0.0718;
  related_pin : "CD";
}
      }
    }
```

In this example, the 'G' pin is related to the 'D' pin in two timing constraint groups: setup_rising and hold_falling.

EXAMPLE MESSAGE

```
Warning: The 'dbvh12' cell has constraints with both rise and fall edges. (DBVH-12)
```

DBVH-13 (error) Could not open '%s' file for writing.

DESCRIPTION

An error is encountered when the VHDL generator tried to open a file for writing. This problem might be caused by

1. Writing to a directory for which you do not have write permission
2. Writing to an existing file for which you do not have write permission
3. An output file name that specifies a non-existing path
4. The file system being full

As a result, the VHDL generator fails and exits.

WHAT NEXT

First, check the correctness of the file name and path name. If the file system is full, provide more disk space. If permission is denied, either change the access permission or target the output files elsewhere.

EXAMPLES

```
write_lib -format vhdl -output /etc/dbvh13.vhd dbvh13
```

In this example, you do not have permission to write to /etc directory.

EXAMPLE MESSAGE

```
Error: Could not open '/etc/dbvh13_components.vhd' file for writing. (DBVH-13)
```

DBVH-14 (warning) The '%s' pin in the '%s' cell is related to more than one output.

DESCRIPTION

The inout/output pin in the sequential library cell is related, timing-wise, to more than one output.

The condition is unusual and probably a mistake. Therefore, the VHDL generator flags it as a warning.

The VHDL generator tries to create the correct full-timing structural model with the

pin related to more than one output. The generator, however, creates a full-timing gatesim model, with the pin related to only one output, while ignoring all other outputs that are also related timing-wise to the pin.

This warning pertains only to full-timing structural, and full-timing gatesim models. Unit-delay structural models ignore timing, and the VITAL model does not support output-to-output delays.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning. Otherwise, verify the questionable timing arcs.

EXAMPLES

```
    cell(dbvh14) {
      area : 9;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(CP) {
direction : input;
capacitance : 1;
      }

      ff("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
      }
      pin(Q) {
direction : output;
function : "IQ";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.00;
  intrinsic_fall : 1.00;
  rise_resistance : 0.1000;
  fall_resistance : 0.1000;
  related_pin : "CP";
}
      }
      pin(Q2) {
direction : output;
function : "IQ";
timing() {
intrinsic_rise : 2.0;
intrinsic_fall : 3.0;
rise_resistance : 0.1458;
fall_resistance : 0.0523;
related_pin : "Q";
}
      }
      pin(Q3) {
```

```
direction : output;
function : "IQ";
timing() {
  intrinsic_rise : 2.0;
  intrinsic_fall : 3.0;
  rise_resistance : 0.1000;
  fall_resistance : 0.1000;
  related_pin : "Q Q2";
}
      }
    }
```

EXAMPLE MESSAGE

```
Warning: The 'Q3' pin in the 'dbvh14' cell is related to more than one output. (DBV
H-14)
```

DBVH-15 (warning) The '%s' cell contains circular timing arcs. The '%s' pin
is in one of the cycles.

DESCRIPTION

The pin in the library cell has circular timing arcs. A circular timing arc occurs when an inout/output pin is related to itself through other inout/output pins. A change in one pin belonging to a circular timing arc loops around and around.

Circular timing arcs do not make sense and are probably mistakes. Therefore, the VHDL generator flags them with warnings and tries to create the correct model.

This warning pertains only to full-timing structural, optimized gate-level, and VITAL models. Unit-delay structural models ignore timing.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning. Otherwise, verify the questionable circular timing arcs.

EXAMPLES

```
    cell(dbvh15) {
      area : 9;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(CP) {
direction : input;
```

```
capacitance : 1;
      }

      ff("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
      }
      pin(Q) {
direction : output;
function : "IQ";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "CP";
}
      }
      pin(Q2) {
direction : output;
function : "IQ";
timing() {
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "Q3";
}
      }
      pin(Q3) {
direction : output;
function : "IQ";
timing() {
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "Q2";
}
      }
    }
```

EXAMPLE MESSAGE

```
Warning: The 'dbvh15' cell contains circular timing arcs. The 'Q2' pin
        is in one of the cycles. (DBVH-15)
```

DBVH-16 (warning) The '%s' pin in the '%s' cell is related to an output and

the ’%s’ input pin.

DESCRIPTION

An inout/output pin is related both to another output pin and a non-enabled input pin.

Having an output pin related to both another output pin and a non-enabled input pin can lead to problems in the generated simulation models.

For the optimized gate-level model, if a sequential output pin is related to another output pin, it must be either unrelated to all asynchronous clear/preset inputs or related to them all.

For the full-timing structural model, if a sequential output pin is related to another output, it cannot be related to any asynchronous clear/preset inputs.

The VITAL model does not support output-to-output timing arcs.

This warning pertains only to full-timing structural, optimized gate-level, and VITAL models. Unit-delay structural models ignore timing.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning. Otherwise, verify that the generated simulation model is correct.

EXAMPLES

```
    cell(dbvh16) {
      area : 9;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(CP) {
direction : input;
capacitance : 1;
      }
      pin(CD) {
direction : input;
capacitance : 2;
      }

      ff("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
clear   : "CD’";
      }

      pin(Q) {
direction : output;
```

```
function : "IQ";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.00;
  intrinsic_fall : 1.00;
  rise_resistance : 0.1000;
  fall_resistance : 0.1000;
  related_pin : "CP";
}
timing() {
  timing_type : clear;
  timing_sense : positive_unate;
  intrinsic_fall : 0.1;
  fall_resistance : 0.1;
  related_pin : "CD";
}
      }
      pin(Q2) {
direction : output;
function : "IQ";
timing() {
  intrinsic_rise : 2.0;
  intrinsic_fall : 3.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "Q";
}
timing() {
  timing_type : clear;
  timing_sense : positive_unate;
  intrinsic_fall : 0.1;
  fall_resistance : 0.1;
  related_pin : "CD";
}
      }
    }
```

EXAMPLE MESSAGE

```
Warning: The 'Q2' pin in the 'dbvh16' cell is related to an output and
        the 'CD' input pin. (DBVH-16)
```

DBVH-17 (warning) The '%s' cell has two opposite output pins, '%s' and '%s',
with the same '%s' value. The '%s' pin should not be related

to the opposite ’%s’ output.

DESCRIPTION

This is a sequential library cell with two or more outputs and both clear and preset functions defined. The current output is related to a functionally opposite output pin. In addition, the values of the **clear_preset_var1** and **clear_preset_var2** attributes are the same.

It is not possible for one output to be the opposite of another output and yet be forced to the same value.

The generated full-timing models override the **clear_preset_var1** and **clear_preset_var2** declarations and always maintain the output pins opposite of each other.

This warning pertains to unit-delay structural models, full-timing structural, optimized gate-level, and VITAL models.

WHAT NEXT

Change the value of clear_preset_var1 or clear_preset_var2, or remove the output-to-output timing arc.

EXAMPLES

```
    cell(dbvh17) {
      area : 9;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(CP) {
direction : input;
capacitance : 1;
      }
      pin(CD) {
direction : input;
capacitance : 2;
      }
      pin(SD) {
direction : input;
capacitance : 2;
      }
      ff("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
clear   : "CD’";
preset  : "SD’";
clear_preset_var1 : L;
clear_preset_var2 : L;
      }
```

```
      pin(Q) {
direction : output;
function : "IQ";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.00;
  intrinsic_fall : 1.00;
  rise_resistance : 0.1000;
  fall_resistance : 0.1000;
  related_pin : "CP";
}
timing() {
  timing_type : preset;
  timing_sense : negative_unate;
  intrinsic_rise : 0.1;
  rise_resistance : 0.1;
  related_pin : "SD";
}
timing() {
  timing_type : clear;
  timing_sense : positive_unate;
  intrinsic_fall : 0.1;
  fall_resistance : 0.1;
  related_pin : "CD";
}
      }
      pin(QN) {
direction : output;
function : "IQN";
timing() {
  intrinsic_rise : 2.0;
  intrinsic_fall : 3.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "Q";
}
      }
    }
```

EXAMPLE MESSAGE

```
Warning: The 'dbvh17' cell has two opposite output pins, 'Q' and 'QN',
        with the same 'L' value. The 'QN' pin should not be related
        to the opposite 'Q' output. (DBVH-17)
```

DBVH-18 (error) The '%s' pin is missing.

DESCRIPTION

The pin is part of a **function** string, but it is not defined in the library cell.

The VHDL generator cannot continue without a definition of the pin. All VHDL models fail.

This error is never displayed since the missing pin is caught during the **read_lib** command.

WHAT NEXT

Either define the missing pin, or remove it from the **function** string.

DBVH-19 (error) The '%s' cell has more than %d pins.

DESCRIPTION

The library cell has more than 127 pins.

The VHDL generator supports up to 127 pins.

All models fail.

WHAT NEXT

There is no simple workaround. Create the model by hand.

DBVH-20 (warning) The '%s' pin is unused in the '%s' cell.

DESCRIPTION

An input pin in the combinational library cell is not part of the function of any output.

If an input pin to a combinational library cell is unused, the VHDL generator leaves the input pin unconnected.

A correct VHDL model is created but, since there is no reason for an unused input, a warning is given.

WHAT NEXT

Verify that the unused pin is not a mistake.

EXAMPLES

```
cell(dbvh20) {
  area : 9;
```

```
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
    min_period : 3.0
  }
}
```

EXAMPLE MESSAGE

```
Warning: The 'D' pin is unused in the 'dbvh20' cell. (DBVH-20)
```

DBVH-21 (warning) The '%s' time is a nonpositive setup or hold constraint.

DESCRIPTION

A setup or hold timing constraint is a negative or zero value.

The VHDL simulator does not support nonpositive setup or hold timing constraints.

The full-timing structural model gets zero timing constraints instead. The Optimized gate-level simulation model keeps the nonpositive constraint values, which are also ignored during simulation. The current VITAL simulation model does not support negative setup or hold constraints.

This warning pertains only to full-timing structural, optimized gate-level, and VITAL simulation models. Unit-delay structural models ignore timing.

WHAT NEXT

If you are generating unit-delay structural models, you can ignore this warning. Otherwise, edit the generated models to support setup and hold checkers.

EXAMPLES

```
cell(dbvh21) {
  area : 14;
  pin(CP) {
    direction : input;
    capacitance : 1;
  }
  pin(J) {
    direction : input;
    capacitance : 1;
    timing() {
```

```
      timing_type : hold_rising;
      intrinsic_rise : 0.0;
      intrinsic_fall : 0.0;
      related_pin : "CP";
    }
  }
}
```

EXAMPLE MESSAGE

```
Warning: The 'thold_J_CP' time is a nonpositive setup or hold constraint. (DBVH-21)
```

DBVH-22 (error) The '%s' cell is overwriting the '%s' cell in the '%s' library.

DESCRIPTION

A library cell has the same VHDL name as another library cell.

Library cell names are case-sensitive in Library Compiler and case-insensitive in VHDL. Therefore, two unique names in Library Compiler can be identical in VHDL. For example, VDD and vdd are two different names in Library Compiler, but the same name in VHDL.

The VHDL generator overwrites previous library cells with the same VHDL library name. Only one unique VHDL named library cell is created per library.

WHAT NEXT

Give identical VHDL named library cells unique VHDL names.

DBVH-23 (warning) The minimum period attribute is allowed only on clock pins.
The '%s' port has a minimum period constraint and is not a clock.
The constraint is ignored.

DESCRIPTION

A minimum-period attribute is placed on a nonclock pin.

The VHDL generator recognizes minimum-period constraints only on clock pins. Thus, the illegal minimum-period constraint is ignored.

This warning pertains only to full-timing structural, full-timing gate-level, and VITAL simulation models. Unit-delay structural models ignore timing.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning. Otherwise, either remove the minimum period constraint or make the pin a clock pin.

EXAMPLES

```
    cell(dbvh23) {
    area : 9;
    pin(D) {
    direction : input;
    capacitance : 1;
    min_period : 3.0;
    }
    pin(CP) {
    direction : input;
    capacitance : 1;
    }
    ff(IQ, IQN) {
    next_state : "D";
    clocked_on : "CP";
    }
    pin(Q) {
    direction : output;
    function : "IQ";
    timing() {
    timing_type : falling_edge;
    intrinsic_rise : 4;
    intrinsic_fall : 2.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "CP";
}
}
    }
```

EXAMPLE MESSAGE

```
Warning: The minimum period attribute is allowed only on clock pins.
        The 'D' port has a minimum period constraint and is not a clock.
        The constraint is ignored. (DBVH-23)
```

DBVH-24 (warning) The driver_type attribute on the '%s' pin is

ignored.

DESCRIPTION

This warning is given for any one of the following reasons:

* A pull_up pin has a function of ’0’, or a pull_down pin has a function of ’1’.
* The output pin has no three_state attribute, the output is driven by input pins, and the output has a pull_up or pull_down **driver_type** attribute.

The invalid **driver_type** attribute is ignored.

WHAT NEXT

Correct the conflicting invalid **driver_type** either by removing it or by changing the output pin.

EXAMPLES

```
    cell(dbvh24) {
      area : 2;
      pin(A) {
direction : input;
capacitance : 1.0;
      }
      pin(Z) {
direction : output;
function : "A";
driver_type : pull_up;
timing() {
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  related_pin : "A";
}
      }
    }
```

The output pin ’Z’ has no three_state attribute. It is driven by the input pin ’A’ and has a pull_up **driver_type** attribute.

EXAMPLE MESSAGE

Warning: The driver_type attribute on the ’Z’ pin is ignored. (DBVH-24)

DBVH-25 (error) Cannot read the '%s' file.

DESCRIPTION

The **vhdlmacro** library technology database **vhdlmacro.db** could not be found in the search path or could not be read. Both the unit-delay and the full-timing structural models require reading in the **vhdlmacro.db** file. The file defines the simulation primitives of the targeted simulator. This error message is specific to structural models, because no structural models can be created without **vhdlmacro.db** first being read in.

The optimized gate-level, and VITAL models do not require this file and ignore the error.

WHAT NEXT

If you are creating a structural library, place the **vhdlmacro.db** file in the search path and make it readable.

EXAMPLES

```
lc_shell> read_lib dbvh25.lib
lc_shell> search_path = {}
lc_shell> write_lib -format vhdl dbvh25
```

EXAMPLE MESSAGE

```
Error: Cannot read the 'vhdlmacro.db' file. (DBVH-25)
```

DBVH-26 (warning) Unknown '%s' architecture in vhdllib_architecture.
The unknown architecture is ignored.

DESCRIPTION

The architecture name identified in the **dc_shell** or **lc_shell** environment variable **vhdllib_architecture** is not recognized.

The following architecture names are recognized:

* FTGS (optimized gate-level model)
* VITAL (VITAL model)

Unrecognized architecture names are ignored. Recognized architecture names are processed.

WHAT NEXT

Use only the architecture names listed previously. For example,

vhdllib_architecture = {FTGS,VITAL}

EXAMPLES

```
lc_shell> vhdllib_architecture = "dbvhd26_arch"
lc_shell> write_lib -format vhdl dbvh26
```

EXAMPLE MESSAGE

```
Warning: Unknown 'dbvh26_arch' architecture in vhdllib_architecture.
The unknown architecture is ignored. (DBVH-26)
```

DBVH-27 (error) The '%s' cell component is not in vhdlmacro library.

DESCRIPTION

The cell component could not be removed from the structural netlist of the library cell, and the translation failed.

A library cell that the VHDL generator expected it could create a structural model for could not be compiled. Therefore, even though **report_lib** lists the library cell as removable, it is not.

This error message is specific to the structural model. A black box is created for the structural models.

WHAT NEXT

Verify that the library cell is correctly specified in the technology library. If it is correct, then you cannot automatically generate the structural models.

EXAMPLE MESSAGE

```
Error: The 'dbvh27' cell component is not in vhdlmacro library. (DBVH-27)
```

DBVH-28 (warning) The 'U%d' component instance has open

pins.

DESCRIPTION

The component instance in the generated unit-delay or full-timing structural model has open (unconnected) output pins.

The structural netlist is not fully optimized. Open output pins means that the structural netlist has unused simulation primitives.

This warning message is specific to structural models.

WHAT NEXT

You can further hand-optimize the generated structural models to use fewer simulation primitives.

EXAMPLES

```
    cell(dbvh28) {
area : 6.0;
pin(CLK) {
direction : input;
capacitance : 1.0;
}
pin(SET) {
direction : input;
capacitance : 3.0;
}
ff("IQ","IQN") {
next_state : "IQ’";
clocked_on : "CLK";
preset     : "SET’";
}
pin(Q) {
direction : output;
function : "IQ";
timing() {
timing_type : rising_edge;
intrinsic_rise : 0.1;
intrinsic_fall : 1.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "CLK";
}
timing() {
timing_type : preset;
timing_sense : negative_unate;
intrinsic_rise : 0.1;
rise_resistance : 0.1;
related_pin : "SET";
}
```

```
}
pin(QN) {
direction : output;
function : "IQN";
timing() {
timing_type : rising_edge;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "CLK";
}
timing() {
timing_type : clear;
timing_sense : positive_unate;
intrinsic_fall : 0.1;
fall_resistance : 0.1;
related_pin : "SET";
}
}
}
```

In this case, the generated full-timing structural model has ’open’ associated with the ’Q’ port in the U7 instance.

```
-- Netlist U7 : DFFSRL_00MAC port map( D => QN_net3_1, CLK => prop_QN(1), CLR => n1,
PRE => prop_QN( 0), Q => open, QN => QN_net3_1);
```

EXAMPLE MESSAGE

```
Warning: The ’U7’ component instance has open pins. (DBVH-28)
```

DBVH-29 (error) Cell cannot have both force_00 and force_11. Try another force combination.

DESCRIPTION

The sequential library cell has both a **force_00** and a **force_11** declared.

The translation algorithm cannot handle library cells with both of these declarations.

This warning message is specific to structural models.

WHAT NEXT

Declare instead either a pair of **force_10** and **force_01**, **force_10** and **force_11**, **force_00** and **force_01**, **force_00** and **force_10**, or **force_01** and **force_11**.

DBVH-30 (warning) Missing timing arc between '%s' and '%s' pins in the '%s' cell.
A timing arc is estimated.

DESCRIPTION

An output pin lacks a timing arc that is related to an input pin that is in the output pin's function.

Synthesis allows output pins in sequential library cells to lack timing arcs to asynchronous inputs. For example, clear-to-output for a flip-flop and data-to-output for a latch can be omitted. But for simulation, a timing arc is required for every output pin to every functionally-dependent input pin.

A full-timing structural model always makes a best guess for the missing timing arc and then continues.

This warning pertains only to full-timing structural, optimized gate-level, and VITAL structural models. Unit-delay structural models ignore timing.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning. Otherwise, add the missing timing arc to the technology library.

DBVH-31 (warning) A pull-up or pull-down on the '%s' input pin is not visible
outside the cell. Make the pin an inout pin.

DESCRIPTION

An input pin has a **driver_type** attribute of pull-up or pull-down.

If an output pin driving the input pin has a three_state attribute, the pull-up or pull-down pulls the input pin to a resistive high or low. The driving output pin should also be affected by the pull-up or pull-down and go to a resistive high or low. However, because the pull-up or pull-down is on an input pin, the driving output pin cannot see the effect of the pull-up or pull-down.

This warning is given, but the pull-up or pull-down is still placed on the input pin. It is not visible outside the library cell.

WHAT NEXT

If the pull-up or pull-down should be visible outside of the library cell, change

the pulled input pin to an inout pin.

DBVH-32 (warning) '%s' to '%s' %s input delay ranges %0.3f to %0.3f.
The maximum input delay %0.3f is chosen.

DESCRIPTION

For the full-timing structural model, the worst-case timing arc has to be selected for an input buffer. This warning message specifies the matching timing arc, the range of timing delays possible, and the input delay chosen.

The VHDL generator must fit the library cell's pin-to-pin timing onto the library cell's structural netlist by lumping delays onto input buffers and output pins. Whenever the fit does not match perfectly and an estimate is required, this warning is given to notify the user of the degree of error of the estimate.

WHAT NEXT

If the delay range is wide, you need to hand-modify the full-timing structural model.

EXAMPLES

```
    cell(dbvh32) {
      area : 9;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(CP) {
direction : input;
capacitance : 1;
      }
      pin(CD) {
direction : input;
capacitance : 2;
      }
      ff("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
clear   : "CD'";
      }
      pin(Q) {
direction : output;
function : "IQ";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.00;
```

```
  intrinsic_fall : 2.00;
  rise_resistance : 0.1000;
  fall_resistance : 0.1000;
  related_pin : "CP";
}
timing() {
  timing_type : clear;
  timing_sense : positive_unate;
  intrinsic_rise : 3.0;
  intrinsic_fall : 4.0;
  fall_resistance : 0.1;
  related_pin : "CD";
}
      }
    }
```

EXAMPLE MESSAGE

```
Warning: 'CP' to 'Q' rise/fall input delay ranges 1.000 to 2.000.
        The maximum input delay 2.000 is chosen. (DBVH-32)
```

DBVH-33 (warning) Could not lump all the timing related to the '%s' pin.

DESCRIPTION

For the full-timing structural model, the library cell's pin-to-pin delays could not be lumped onto the library cell's structural netlist.

There are many causes of this problem but it should rarely occur. Delays can be lumped only on the inputs or outputs, and not on internal nodes. In some cases, it is not possible to lump all the timing on the inputs or the outputs.

The full-timing structural model is generated, but the unlumped timing delays are ignored.

WHAT NEXT

For better accuracy, hand-modify the generated full-timing VHDL structural model. You can add missing lumped timing to the internal netlist.

EXAMPLES

```
    cell(dbvh33) {
      area : 9;
      pin(D) {
direction : input;
capacitance : 1;
      }
```

```
      pin(CP) {
direction : input;
capacitance : 1;
      }
      pin(CD) {
direction : input;
capacitance : 2;
      }
      ff("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
clear   : "CD'";
      }
      pin(Q) {
direction : output;
function : "IQ";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "CP";
}
timing() {
  timing_type : clear;
  timing_sense : positive_unate;
  intrinsic_fall : 0.1;
  fall_resistance : 0.1;
  related_pin : "CD";
}
      }
      pin(Q2) {
direction : output;
function : "IQ";
timing() {
  intrinsic_rise : 2.0;
  intrinsic_fall : 3.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "Q";
}
timing() {
  timing_type : clear;
  timing_sense : positive_unate;
  intrinsic_fall : 0.1;
  fall_resistance : 0.1;
  related_pin : "CD";
}
      }
    }
```

In this case, since the output pin Q2 is related to the output pin Q, and the input pin CD and the output pin Q is related to CD, the Q2 and CD pin-to-pin delay could not be lumped.

EXAMPLE MESSAGE

```
Warning: Could not lump all the timing related to the 'CD' pin. (DBVH-33)
```

DBVH-34 (warning) Timing arcs related to the '%s' pin have inconsistent timing sense. The pin is chosen to be active %s in the recovery checker.

DESCRIPTION

The asynchronous input pin is specified to be both active-high and active-low. There are two recovery timing constraints related to the same input pin. In one, the input pin is active-high, and in another the input pin is active-low.

For full-timing structural models, the recovery asynchronous input must be consistently active-high or active-low.

The input pin is assumed to be active-high.

WHAT NEXT

Correct the recovery timing constraints in the technology library.

DBVH-35 (warning) The '%s' pin is related to an output and only some asynchronous inputs. All asynchronous inputs are ignored.

DESCRIPTION

An inout or output pin is related to another output pin and to some, but not all, of the asynchronous inputs.

Having an output pin related to another output pin and to only some of the asynchronous inputs can lead to problems in the generated simulation models.

For the full-timing structural model, if a sequential output pin is related to another output, it cannot be related to any asynchronous clear/preset inputs.

The VITAL model does not support output-to-output timing arcs. As a result, all of the related asynchronous inputs are ignored.

This warning pertains only to full-timing structural, and optimized gate-level

models. Unit-delay structural models ignore timing.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning. Otherwise, verify that the generated simulation model is correct.

EXAMPLES

```
    cell(dbvh35) {
      area : 9;
      pin(D) {
direction : input;
capacitance : 1;
timing() {
  timing_type : setup_rising;
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  related_pin : "CP";
}
timing() {
  timing_type : hold_rising;
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  related_pin : "CP";
}
      }
      pin(CP) {
direction : input;
capacitance : 1;
      }
      pin(CD) {
direction : input;
capacitance : 2;
      }
      pin(SD) {
direction : input;
capacitance : 2;
      }
      ff("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
clear   : "CD'";
preset  : "SD'";
clear_preset_var1 : L;
clear_preset_var2 : L;
      }
      pin(Q) {
direction : output;
function : "IQ";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
```

```
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "CP";
}
timing() {
  timing_type : preset;
  timing_sense : negative_unate;
  intrinsic_rise : 0.1;
  rise_resistance : 0.1;
  related_pin : "SD";
}
timing() {
  timing_type : clear;
  timing_sense : positive_unate;
  intrinsic_fall : 0.1;
  fall_resistance : 0.1;
  related_pin : "CD";
}
      }
      pin(Q2) {
direction : output;
function : "IQ";
timing() {
  intrinsic_rise : 2.0;
  intrinsic_fall : 3.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "Q";
}
timing() {
  timing_type : clear;
  timing_sense : positive_unate;
  intrinsic_fall : 0.1;
  fall_resistance : 0.1;
  related_pin : "CD";
}
      }
    }
```

EXAMPLE MESSAGE

```
Warning: The 'Q2' pin is related to an output and only some
        asynchronous inputs. All asynchronous inputs are ignored. (DBVH-35)
```

DBVH-36 (warning) The '%s' pin is a clock, and bundled clocks

are not supported.

DESCRIPTION

The sequential library cell has a bundled clock declared in the **ff, latch, ff_bank**, or **latch_bank** groups.

For the optimized gate-level, and VITAL models, bundled clocks are unsupported. Instead, all the banked outputs share a single set of clocks. As a result, only the first member of the bundled clock is valid. The other members are ignored.

This warning pertains only to the optimized gate-level, and VITAL models. Structural models fully support bundled clocks.

WHAT NEXT

If you are generating structural models, ignore this warning. Otherwise, edit the VHDL model.

EXAMPLES

```
cell(dbvh36) {
    area : 16;
    bundle( D ) {
members( D_1 D_2 );
capacitance : 1.0;
direction : input;
    }
    pin( CLK ) {
capacitance : 1.0;
direction : input;
    }
    bundle( Q ) {
members( Q_1 Q_2  );
direction : output;
function : "IQ";
    }
    ff_bank( IQ, IQN, 2) {
next_state : "CLK";
clocked_on : "D";
    }
}
```

In this case, there is a mistake where D and CLK are switched in the ff_bank group.

EXAMPLE MESSAGE

Warning: The ’D’ pin is a clock, and bundled clocks are not supported. (DBVH-36)

DBVH-37 (error) Unknown logic system '%s' in vhdllib_logic_system.
Use the logic system 'IEEE-1164'. Aborting the execution.

DESCRIPTION

This message indicates that the **dc_shell/lc_shell** environment variable **vhdllib_logic_system** is currently set to the name of an invalid logic system. The default logic system, IEEE-1164 (IEEE standard none-logic-state) is the only logic system currently supported. An invalid logic system causes Library Compiler to quit.

This error message pertains to all architectures.

WHAT NEXT

Set the **dc_shell** or **lc_shell** environment variable **vhdllib_logic_system** to **IEEE-1164**

DBVH-38 (error) The '%s' pin on the '%s' cell has a timing arc whose
related_pin '%s' is not functionally related.

DESCRIPTION

This error pertains to full-timing structural, optimized gate-level, and VITAL models. Unit-delay structural models ignore timing.

The pin on the library cell has one timing arc whose **related_pin** is not functionally related to the pin.

Simulation models require both timing and functional information to be defined between inputs and outputs.

The VHDL generator reports to the user that an error might have been made. Remove functionally unrelated timing arcs from the library description file.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning. Otherwise, include only the timing arcs that are also functionally related to the output port in the technology library. Remove all functionally unrelated timing arcs.

EXAMPLES

```
    cell(dbvh38) {
```

```
      area : 3;
      pin(A) {
direction : input;
capacitance : 2;
      }
      pin(Z) {
direction : output;
timing() {
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "A";
}
      }
    }
```

EXAMPLE MESSAGE

```
Error: The 'Z' pin on the 'dbvh38' cell has a timing arc whose
        related_pin 'A' is not functionally related. (DBVH-38)
```

DBVH-39 (error) The '%s' pin on the '%s' cell has duplicate delay paths
from the '%s' related pin.

DESCRIPTION

This error message pertains to full-timing structural, optimized gate-level, and VITAL models. Unit-delay structural models ignore timing.

The pin on the library cell has more than one delay path of the same **timing_type** with the same related pins.

Simulation models are not generated if either of these situations occur: (1) If multiple delay paths of the same **timing_type** with the same related pins are specified. (2) If timing-arc redundancy occurs. For example,consider a cell with the timing arcs - A->X, X->Y, and A->Y. An error message is issued on pin Y even though pin Y does not have any duplicate timing arcs directly defined.

The VHDL generator warns that an error might have been made. Remove the unwanted delay path from the technology library.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning. Otherwise, remove all duplicates from the technology library.

DBVH-40 (error) The ’%s’ pin on the ’%s’ cell has 5 or more parameters
in the ’three_state’ function.

DESCRIPTION

VHDL generator supports **three_state**functions with with no more than four inputs parameters.

This error message pertains to only full-timing gatesim models, since this restriction is due to a limitation on the current sequential generic component(SEQGEN) for sequential cells.

WHAT NEXT

Change your library to meet the restriction of the input parameter number.

EXAMPLES

```
    cell(dbvh40) {
      area : 3;
      pin(A) {
direction : input;
capacitance : 1;
      }
      pin(EN EN1 EN2) {
direction : input;
capacitance : 2;
      }
      pin(TN TN1 TN2) {
direction : input;
capacitance : 2;
      }
      pin(IO) {
direction : inout;
function : "A";
three_state : "!(TN EN’ TN1 EN1’ TN2 EN2’)";
timing() {
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "A";
}
timing() {
  intrinsic_fall : 1.0;
  intrinsic_rise : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "EN EN1 EN2 TN TN1 TN2";
```

```
}
timing() {
  timing_type : three_state_disable;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "EN EN1 EN2 TN TN1 TN2";
}
      }
    }
```

EXAMPLE MESSAGE

```
Error: The 'IO' pin on the 'dbvh40' cell has 5 or more parameters
        in the 'three_state' function. (DBVH-40)
```

DBVH-41 (error) The '%s' function on the '%s' sequential cell has more than 5 parameters.

DESCRIPTION

Due to limitations on the current sequential generic component (SEQGEN) for sequential cells, the FTGS generator does not support sequential cells with more than five synchronous/asynchronous inputs.

This error message pertains only to full-timing gatesim models.

WHAT NEXT

Change your library to meet the restriction of the input parameter number.

EXAMPLES

```
  latch (IQ, IQN) {
clear : "CLR' + (GN' * CLR * D' * D1 * D2 * D3)" ;
preset : "GN' * CLR * D * D1 * D2 * D3" ;
clear_preset_var1 : L;
clear_preset_var2 : H;
  }
```

In this case, 'clear' has 6 input parameters in the string.

EXAMPLE MESSAGE

```
Error: The 'clear' function on the 'dbvh41' sequential cell has
```

more than 5 parameters. (DBVH-41)

DBVH-42 (error) The functionally unrelated output timing arc is defined in the '%s' pin group with the '%s' related pin on the '%s' cell.

DESCRIPTION

If a OUTPUT1-to-OUTPUT2 timing arc is defined, OUTPUT2 must be a function of OUTPUT1 and perhaps other input parameters. For example,

if OUTPUT1 = A + B

OUTPUT2 = A' * B' * C'

then OUTPUT2 = (OUTPUT1)' * C'

An error message is issued if OUTPUT2 is not a function of OUTPUT1. For example,

OUTPUT1 = A + B

OUTPUT2 = A * B

WHAT NEXT

Correct the error in OUTPUT2 function or OUTPUT1 function.

EXAMPLES

```
    cell(dbvh42) {
      area : 2;
pin(A B ) {
direction : input;
capacitance : 1;
      }

      pin(Z) {
direction : output;
function : "A + B";
timing() {
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "A B";
}
      }
      pin(W) {
```

```
direction : output;
function : "A B";
timing() {
  timing_sense : positive_unate;
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "Z ";
}
      }
    }
```

EXAMPLE MESSAGE

```
Error: The functionally unrelated output timing arc is defined in the
'W' pin group with the 'Z' related pin on the 'dbvh42' cell. (DBVH-42)
```

DBVH-43 (error) An obsolete 'state' group is found in the '%s' sequential cell.
Use the 'ff' group or 'latch' group instead.

DESCRIPTION

The **state** group is not supported after v3.0. Instead, the sequential function is now described in the **ff** or **latch** group.

VITAL architecture supports only **ff** and **latch** groups. It does not support the **state** group.

This message is issued when the **liban** Library Analyzer reads in .db files generated by Library Compiler 3.3a or an earlier version.

WHAT NEXT

If you have access to the technology library source file change the **state** group to the **ff** or **latch** group. Otherwise, contact the vendor and inform them about the problem.

EXAMPLE MESSAGE

```
Error: An obsolete 'state' group is found in the 'dbvh43' sequential cell.
      Use the 'ff' group or 'latch' group instead. (DBVH-43)
```

DBVH-44 (error) The '%s' master-slave cell is currently not

supported.

DESCRIPTION

This message is issued when the **liban** Library Analyzer reads a db file that was generated by Library Compiler v3.3a or an earlier version.

VITAL architecture supports only **ff** and **latch** groups. It does not support the **state** group.

WHAT NEXT

Generate a db file using a version later than 3.3a of Library Compiler.

EXAMPLE MESSAGE

Error: The 'dbvh44' master-slave cell is currently not supported. (DBVH-44)

DBVH-45 (error) Neither the 'next_state' nor 'data_in' function is defined in the '%s' cell.

DESCRIPTION

A sequential cell has to define either the **next_state** function or the **data_in** function when the **clocked_on** function or the **enable** have been specified. Only in cases where the **next_state** function is missing when **clocked_on** has been specified, or when **data_in** is missing when **enable** has been specified can this error message occur.

WHAT NEXT

If this error occurs, correct the technology library by adding the appropriate **next_state** function or **data_in** function. Also, when this construct is missing, Library Compiler does not compile a library. Contact Synopsys Support Center to indicate a problem with Library Compiler.

DBVH-46 (error) Neither the 'clocked_on' nor 'enable' function is defined in the '%s' cell.

DESCRIPTION

A sequential cell has to define either the **clocked_on** function or the **enable**

function when the **next_state** function or the **data_in** have been specified. Only in cases where the **clocked_on** function is missing when **next_state** has been specified, or when **enable** is missing when **data_in** has been specified can this error message occur.

WHAT NEXT

If this error occurs, correct the technology library by adding the appropriate **clocked_on** function or **enable** function. Also, when this construct is missing, Library Compiler does not compile a library. Contact Synopsys Support Center to indicate a problem with Library Compiler.

DBVH-47 (warning) The '%s' input pin active edge is unknown in the '%s' sequential cell.

DESCRIPTION

A clock or enable pin needs to be **unate** in **clock** or **enable** function to have a consistently active edge level. Library Compiler requires **clock** or **enable** functions to be unate to perform pulse width and minimum period constraint checking. An example of non-unate **enable** function is

```
enable : "EN1 ^ EN2";
```

A warning message is given if a non-unate **enable** function is detected, and FTGS model assumes positive active edge in pulse width and minimum period constraint checking.

Sometimes the **enable** function of a latch cell is implicitly expressed in **clear** and **preset** functions. In such a case, **timing_type** of all timing arcs related to the input pin is used to determined the active edge of the enable pin. If the active edges implied in **timing_type** are inconsistent Library Compiler issues a warning when reading in the library - LIBG-40. The FTGS generator assumes a positive active edge.

This error can also occur when minimum period or minimum pulse width constraints have been specified for nonclock pins.

WHAT NEXT

Change the technology library by either specifying consistent edges or removing the constraints specified for non_clock pins.

EXAMPLES

```
cell(dbvh47) {
  area : 2.1 ;
  pin(CLK) {
    direction : input;
    capacitance : 0.1;
    clock : true ;
  }
  pin(D) {
    direction : input;
    capacitance : 0.1;
  }
  pin(SET) {
    direction : input;
    capacitance : 0.1;
  }
  pin(CLEAR) {
    direction : input;
    capacitance : 0.1 ;
    min_pulse_width_low : 1.0;
  }
  ff(IQ,IQN) {
    clocked_on : "CLK" ;
    next_state : "D" ;
    clear : "SET" ;
    preset : "!CLEAR" ;
    clear_preset_var1 : "L" ;
    clear_preset_var2 : "H" ;
  }
  pin(Q1) {
    direction : output;
    function : "IQ" ;
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 1.0;
      fall_resistance : 1.0;
      related_pin : "Q2";
    }
  }
  pin(Q2) {
    direction : output;
    function : "IQN" ;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 1.0;
      fall_resistance : 1.0;
      related_pin : "CLK";
    }
    timing() {
      timing_type : preset;
      timing_sense : positive_unate;
```

```
          intrinsic_rise : 1.0;
          rise_resistance : 1.0;
          related_pin : "SET";
        }
        timing() {
          timing_type : clear;
          timing_sense : positive_unate;
          intrinsic_fall : 1.0;
          fall_resistance : 1.0;
          related_pin : "CLEAR";
        }
      }
    }
```

In this case, the 'CLEAR' pin has a pulse width constraint attribute.

EXAMPLE MESSAGE

```
Warning: The 'CLEAR' input pin active edge is unknown in
        the 'dbvh47' sequential cell. (DBVH-47)
```

DBVH-48 (warning) Unknown pulse handling algorithm '%s' in the vhdllib_pulse_handle. Use the default value "use_vhdllib_glitch_handle".

DESCRIPTION

The pulse-handling algorithm defined in the **dc_shell** environment variable **vhdllib_pulse_handle** is not recognized.

The following pulse-handling algorithms are recognized:

use_vhdllib_glitch_handle (use **vhdllib_glitch_handle** variable value)

inertial (use inertial algorithm)

glitch (use glitch algorithm)

spike (use spike algorithm)

Unrecognized pulse-handling name is ignored, and the default value is used instead.

WHAT NEXT

Check the value of the **vhdllib_pulse_handle** variable, and make the necessary change.

EXAMPLES

```
dc_shell> vhdllib_pulse_handle = "use_wrong_handle"
```

EXAMPLE MESSAGE

```
Warning: Unknown pulse handling algorithm 'use_wrong_handle' in the
vhdllib_pulse_handle. Use the default value "use_vhdllib_glitch_handle". (DBVH-48)
```

DBVH-49 (warning) Unable to properly associate timing with the '%s' function.
All related timing arcs defined in the '%s' output pin group of the '%s' cell are ignored.

DESCRIPTION

This is a sequential library cell with two or more outputs. The current output has a timing arc related to another output and one or more timing arcs related to asynchronous inputs (clear or preset).

If the current output has a timing arc related to an asynchronous clear pin, it must define timing arcs related to all clear pins. If at least one of the timing arcs required is not defined, all other timing arcs related to asynchronous clear pins are ignored and a warning message is issued.

If the current output has a timing arc related to an asynchronous preset pin, it must define timing arcs related to all preset pins. If at least one of the timing arcs required is not defined, all other timing arcs related to asynchronous preset pins are ignored and a warning message is issued.

This warning pertains only to the FTGS model.

WHAT NEXT

If you are not generating an FTGS model, ignore the warning. Otherwise, either remove the asynchronous timing arcs from the output pin group or insert missing asynchronous timing arcs to the output pin group.

DBVH-50 (warning) The 'clear_preset_var1'/'clear_preset_var2' value is incompatible
with the asynchronous timing arcs in the '%s' output pin group of the '%s' cell.

One or more asynchronous timing arcs are ignored.

DESCRIPTION

This is a sequential library cell with two or more outputs and both **clear** and **preset** functions defined. The current output has a timing arc related to another output and one or more timing arcs related to asynchronous inputs (clear or preset).

If the current output has timing arcs related to asynchronous clear pins only, its corresponding **clear_preset_var** (**clear_preset_var1** for non-inverting output and **clear_preset_var2** for inverting output) must be "L". Otherwise, this warning message is issued and all asynchronous timings are ignored.

If the current output has timing arcs related to asynchronous preset pins only, its corresponding **clear_preset_var** (**clear_preset_var1** for non-inverting output, and **clear_preset_var2** for inverting output) must be "H". Otherwise, this warning message is issued and all asynchronous timings are ignored.

If the current output has timing arcs related to both asynchronous clear and preset pins, both **clear_preset_var1** and **clear_preset_var2** must be "H" or "L". Otherwise, this warning message is issued and all asynchronous timings are ignored.

This warning pertains only to FTGS models.

WHAT NEXT

Ignore this warning if you are not generating an FTGS model. Otherwise, correct the asynchronous timings defined in the current output pin group, or change **clear_preset_var1** or **clear_preset_var2** attribute values.

DBVH-51 (error) The '%s' output pin on the '%s' sequential cell with an output timing arc has 5 or more asynchronous timing arcs. Currently, this is not supported.

DESCRIPTION

The output pin of this sequential cell has an output timing arc and asynchronous timing arcs. The full-timing **gatesim** model supports, with output timing arc, only one to four asynchronous timing arcs on an output pin.

This error message pertains only to optimized gate-level simulation models.

WHAT NEXT

This model cannot be generated automatically. It has to be generated manually.

EXAMPLES

```
cell(dbvh51) {
  area : 2.1 ;
  pin(CLK) {
    direction : input;
    capacitance : 0.1;
    clock : true ;
  }
  pin(D) {
    direction : input;
    capacitance : 0.1;
  }
  pin(SD SD1 SD2 SD3 SD4) {
    direction : input;
    capacitance : 0.1;
  }
  pin(CD) {
    direction : input;
    capacitance : 0.1 ;
  }
  ff(IQ,IQN) {
    clocked_on : "CLK" ;
    next_state : "D" ;
    clear : "SD SD1 SD2 SD3 SD4" ;
    preset : "!CD" ;
    clear_preset_var1 : "L" ;
    clear_preset_var2 : "H" ;
  }
  pin(Q1) {
    direction : output;
    function : "IQ" ;
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 1.0;
      fall_resistance : 1.0;
      related_pin : "Q2";
    }
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 1.0;
      fall_resistance : 1.0;
      related_pin : "CLK";
    }
    timing() {
      timing_type : preset;
      timing_sense : positive_unate;
      intrinsic_rise : 1.0;
```

```
          rise_resistance : 1.0;
          related_pin : "SD SD1 SD2 SD3 SD4";
        }
        timing() {
          timing_type : clear;
          timing_sense : positive_unate;
          intrinsic_fall : 1.0;
          fall_resistance : 1.0;
          related_pin : "CD";
        }

      }
      pin(Q2) {
        direction : output;
        function : "IQN" ;
        timing() {
          timing_type : rising_edge;
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
          rise_resistance : 1.0;
          fall_resistance : 1.0;
          related_pin : "CLK";
        }
        timing() {
          timing_type : preset;
          timing_sense : positive_unate;
          intrinsic_rise : 1.0;
          rise_resistance : 1.0;
          related_pin : "SD SD1 SD2 SD3 SD4";
        }
        timing() {
          timing_type : clear;
          timing_sense : positive_unate;
          intrinsic_fall : 1.0;
          fall_resistance : 1.0;
          related_pin : "CD";
        }
      }

    }
```

EXAMPLE MESSAGE

```
Error: The 'Q1' output pin on the 'dbvh51' sequential cell with an
        output timing arc has 5 or more asynchronous timing arcs.
Currently, this is not supported. (DBVH-51)
```

DBVH-52 (error) Incomplete functional and/or timing information is

specified for the ’%s’ cell. The cell is a black box.

DESCRIPTION

The cell becomes a black box in either of these situations: (1) The pin on the library cell is missing a **function** attribute. (2) The pin is not a pull-up or pull-down pin and has no related timing arcs. or (3) The pin has no three_state attribute and has no related timing arcs.

As a result, thee FTGS model generation fails.

This message pertains only to optimized gate-level models.

WHAT NEXT

If the output pin is not at a constant logic state, define a **function** attribute for the pin in the technology library.

EXAMPLES

```
    cell(dbvh52) {
      area : 0;
      pin (D) {
direction : input;
      }
      pin (Q) {
direction : output;
      }
    }
```

EXAMPLE MESSAGE

```
Error: Incomplete functional and/or timing information is specified
for the ’dbvh52’ cell. The cell is a black box. (DBVH-52)
```

DBVH-53 (warning) The ’%s’ pin on the ’%s’ cell has duplicate ’%s’ timing arcs
from the same related_pin. Only one of them is used.

DESCRIPTION

The pin on the library cell has more than one timing arc of the same **timing_type** and **timing_sense** with the same related pins. One of the timing arcs is of the state dependent type.

Simulation models are not generated if either of these situations occur: (1) If

multiple delay paths of the same **timing_type** with the same related pins are specified. (2) If timing-arc redundancy occurs. For example,consider a cell with the timing arcs - A->X, X->Y, and A-> Y. An error message is issued on pin Y even though pin Y has no duplicate timing arcs directly defined.

The VHDL generator warns the user that an error might have been made. Only the first unique timing arc is accepted; all the following timing arcs are ignored.

This warning pertains only to full-timing gatesim models.

WHAT NEXT

Include in the technology library only the timing arc that belongs in the simulation model. Remove all duplicates if possible.

EXAMPLES

```
    cell(dbvh53) {
      area : 2;
      pin(A) {
direction : input;
capacitance : 1;
      }
      pin(B) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "A^B";
timing() {
  when : "B'";
  sdf_cond : "!B";
  timing_sense : positive_unate;
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "A";
}
timing() {
  timing_sense : non_unate;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "A";
}
timing() {
  timing_sense : non_unate;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
```

```
  related_pin : "A";
}
      }
    }
```

EXAMPLE MESSAGE

```
Warning: The 'Z' pin on the 'dbvh53' cell has duplicate 'non_unate' timing arcs
        from the same related_pin. Only one of them is used. (DBVH-53)
```

DBVH-55 (warning) The inertial algorithm is chosen as the pulse handling algorithm for FTGS models.

DESCRIPTION

The inertial algorithm is chosen as the pulse-handling algorithm because both **Timing_mesg** and **Timing_xgen** are set to false.

This warning pertains only to optimized gate-level simulation models.

WHAT NEXT

If you want to use either the glitch or spike algorithm for hazard detection, set **Timing_mesg** or **Timing_xgen** to true.

EXAMPLES

```
dc_shell> vhdllib_timing_mesg = "false"
dc_shell> vhdllib_timing_xgen = "false"
```

EXAMPLE MESSAGE

```
Warning: The inertial algorithm is chosen as the pulse handling algorithm for FTGS
models. (DBVH-55)
```

DBVH-57 (error) The '%s' cell component is not in the testsimmacro library.

DESCRIPTION

The cell component could not be removed from the structural netlist of the library cell, and the translation failed.

A library cell that the VHDL generator expected, it could create a structural model for could not be compiled. Therefore, even though **report_lib** lists the library cell as removable, it is not.

This error message is specific to the fault simulation structural model. A black box is created for the fault simulation structural models.

WHAT NEXT

Verify that the library cell is correctly specified in the technology library. If it is correct, you cannot automatically generate the fault simulation structural models.

EXAMPLE MESSAGE

Error: The 'dbvh57' cell component is not in the testsimmacro library. (DBVH-57)

DBVH-58 (error) Unable to find a nonscan equivalent cell in the current library.

DESCRIPTION

The library cell is a black box. Its normal nontest behavior is not matched by any cell in the current library.

This error message is specific to the fault-simulation structural model. A blackbox is created for the fault-simulation structural models.

WHAT NEXT

Verify that the library cell is correctly specified in the technology library. Check if a nonscan equivalent cell should be defined in the same library. If it is correct, you cannot automatically generate the fault simulation structural models.

EXAMPLES

```
    cell(dbvh58) {
      area : 10;
      pin(D C SI SE) {
direction : input;
capacitance : 1;
      }
      pin(Q SO) {
direction : output;
      }
      test_cell() {
pin(D C) {
  direction : input;
```

```
}
pin(SI) {
  direction : input;
  signal_type : "test_scan_in";
}
pin(SE) {
  direction : input;
  capacitance : 1;
  signal_type : "test_scan_enable";
}
state ("IQ","IQN") {
  force_01 : "C D'";
  force_10 : "C D";
}
pin(Q) {
  direction : output;
  function : "IQ";
}
pin(SO) {
  direction : output;
  signal_type : "test_scan_out";
}
      }
    }
```

EXAMPLE MESSAGE

```
Error: Unable to find a nonscan equivalent cell in the current library. (DBVH-58)
```

DBVH-59 (warning) A minimum pulse-width constraint on '%s' is only allowed on clock and asynchronous clear/preset pins. The constraint is ignored.

DESCRIPTION

A minimum pulse-width attribute is placed on a data pin.

The VHDL generator allows only minimum pulse-width constraints on clock pins and asynchronous clear/preset pins.

As a result, the illegal minimum pulse-width constraint is ignored.

This warning pertains to full-timing structural, optimized gate-level, and VITAL simulation models. Unit-delay structural models ignore timing.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning. Otherwise, either remove the minimum pulse-width constraint or make the pin a clock pin.

EXAMPLES

```
    cell(dbvh59) {
      area : 9;
      pin(D) {
direction : input;
capacitance : 1;
min_pulse_width_high : 1.5;
min_pulse_width_low : 1.6;
      }
      pin(CP) {
direction : input;
capacitance : 1;
      }
      pin(CD) {
direction : input;
capacitance : 2;
      }
      ff("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
clear   : "CD'";
      }
    }
```

EXAMPLE MESSAGE

```
Warning: A minimum pulse-width constraint on 'D' is only allowed on
        clock and asynchronous clear/preset pins. The constraint is ignored. (DBVH-
59)
```

DBVH-60 (warning) Using the nonscan equivalent cell, the fault simulation structural model will model the nonscan behavior only.

DESCRIPTION

The library cell is a black box. Only its normal nontest behavior is being used to build the fault-simulation structural model.

This error message is specific to the fault-simulation structural model when executing the **write_testsim_lib** command with the **-depends** flag.

WHAT NEXT

Fault simulation of circuits using these library cells should be performed on functional vectors and parallel load scan vectors only. Fault simulation cannot correctly simulate vectors that exercise the scan path.

EXAMPLES

```
    cell(dbvh60) {
      area : 12;
      pin_opposite("Q","XQ");
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(A,B, CK, IH) {
direction : input;
capacitance : 2;
clock : true;
      }
      pin(SI) {
direction : input;
capacitance : 1;
timing() {
  timing_type : setup_falling;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "A";
}
timing() {
  timing_type : hold_falling;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "A";
}
      }
      pin(Q) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "A CK IH";
}
timing() {
  timing_type : falling_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "B";
}
      }
```

```
      pin(XQ) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "A CK IH";
}
timing() {
  timing_type : falling_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.10;
  fall_resistance : 0.10;
  related_pin : "B";
}
      }
      test_cell(){
pin(D,CK){
  direction : input;
}
pin(IH){
  direction : input;
  signal_type : "test_clock";
}
pin(SI){
  direction : input;
  signal_type : "test_scan_in";
}
pin(A){
  direction : input;
  signal_type : "test_scan_clock_a";
}
pin(B){
  direction : input;
  signal_type : "test_scan_clock_b";
}
ff("IQ","IQN"){
  clocked_on : "CK";
  next_state : "D";
}
pin(Q){
  direction : output;
  function : "IQ";
  signal_type : "test_scan_out";
}
pin(XQ){
  direction : output;
  function : "IQN";
  signal_type : "test_scan_out_inverted";
}
      }
    }
```

EXAMPLE MESSAGE

```
Warning: Using non-scan equivalent cell. The fault simulation structural
         model will model the non-scan behavior only. (DBVH-60)
```

DBVH-61 (error) MVL7 is not an acceptable logic system in the VITAL architecture, so VITAL architecture is not generated.

DESCRIPTION

The VITAL architecture allows only the IEEE-1164 logic system. If the **vhdllib_architecture** variable has "VITAL" and **vhdllib_logic_system** is set to "mvl7", Library Compiler ignores the VITAL architecture and generates FTGS as defined in the **vhdllib_architecture** variable.

This error message is specific to the VITAL simulation model.

WHAT NEXT

To generate VITAL architecture, set **vhdllib_logic_system = "IEEE-1164"**.

DBVH-62 (warning) The '%s' output pin has an output-related timing arc from the '%s' output. All timing arcs of the '%s' pin are ignored.

DESCRIPTION

The VITAL architecture does not support output-to-output delay. If a 'Q1' output pin has a timing arc related to another output, Library Compiler ignores this arc, and 'Q1' is left unconnected.

The model results in incorrect simulation.

This error message is specific to VITAL simulation models.

WHAT NEXT

Remove the output-to-output timing arcs in the technology library, and regenerate VHDL libraries.

EXAMPLES

```
cell(dbvh62) {
  area : 2.1 ;
  pin(CLK) {
    direction : input;
    capacitance : 0.1;
    clock : true ;
  }
  pin(D) {
    direction : input;
    capacitance : 0.1;
  }
  pin(SET) {
    direction : input;
    capacitance : 0.1;
  }
  pin(CLEAR) {
    direction : input;
    capacitance : 0.1 ;
  }
  ff(IQ,IQN) {
    clocked_on : "CLK" ;
    next_state : "D" ;
    clear : "SET" ;
    preset : "!CLEAR" ;
    clear_preset_var1 : "L" ;
    clear_preset_var2 : "H" ;
  }
  pin(Q1) {
    direction : output;
    function : "IQ" ;
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 1.0;
      fall_resistance : 1.0;
      related_pin : "Q2";
    }
  }
  pin(Q2) {
    direction : output;
    function : "IQN" ;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 1.0;
      fall_resistance : 1.0;
      related_pin : "CLK";
    }
```

```
        timing() {
          timing_type : preset;
          timing_sense : positive_unate;
          intrinsic_rise : 1.0;
          rise_resistance : 1.0;
          related_pin : "SET";
        }
        timing() {
          timing_type : clear;
          timing_sense : positive_unate;
          intrinsic_fall : 1.0;
          fall_resistance : 1.0;
          related_pin : "CLEAR";
        }
      }

    }
```

EXAMPLE MESSAGE

```
Warning: The 'Q1' output pin has an output-related timing arc from
         the 'Q2' output . All timing arcs of the 'Q1' pin are ignored. (DBVH-
62)
```

DBVH-63 (warning) The '%s' output pin has undefined value if both clear and preset are active. Force the output value to X.

DESCRIPTION

There is an error in the library cell function description. The **clear_preset_var1** or **clear_preset_var2** attribute is missing from the **ff** or **latch** group description. As a result, if both clear and preset pins are active, VITAL model generator cannot determine the output behavior. VITAL generator assigns X value to the output.

The model results in incorrect simulation.

This error message is specific to VITAL simulation models.

WHAT NEXT

Check the cell description in the technology library, and fix the error.

DBVH-64 (error) Cannot write the library to the '%s' file.

DESCRIPTION

An attempt to write out a testsim library (**db**) file with **write_testsim_lib** failed. The common causes of this failure are no write permission with the target directory; or not enough disk space for the file.

As a result, the TESTSIM model generator exits abnormally.

WHAT NEXT

Check disk space and permissions of the target directory. Make sure you have enough disk space, and write permission before using **write_testsim_lib**.

DBVH-65 (error) Design compiler does not recognize the cell's function.

DESCRIPTION

Design Compiler does not recognize the following cell's functions: (1) Xilinx CLBs; (2) Xilinx IOBs; (3) complex UNIGEN function with internal pins and functions.

Therefore, the VHDL generator creates an empty cell for both the unit-delay and full-timing structural models.

WHAT NEXT

Verify that the library cell is correctly defined in the technology library. If it is correct, you cannot automatically generate the structural models.

EXAMPLE MESSAGE

Error: Design compiler does not recognize the cell's function. (DBVH-65)

DBVH-66 (error) The vhdllib_logic_system is set to the obsolete 'MVL7' logic system.
Use the 'IEEE-1164' logic system. Quitting execution.

DESCRIPTION

This message indicates that the **dc_shell/lc_shell** environment variable

vhdllib_logic_system is currently set to **mvl7**, which is obsolete. The default logic system, IEEE-1164 (IEEE standard none-logic-state), is the only one currently supported. A value of **mv17** causes Library Compiler to quit.

This error message pertains to all architectures.

WHAT NEXT

Set the **dc_shell** environment variable **vhdllib_logic_system** to **IEEE-1164**. ~

EXAMPLES

```
lc_shell> vhdllib_logic_system = MVL7
```

EXAMPLE MESSAGE

```
Error: The vhdllib_logic_system is set to the obsolete 'MVL7' logic system.
       Use the 'IEEE-1164' logic system. Quitting execution.(DBVH-66)
```

DBVH-67 (warning) The internal timing arc between the '%s' and '%s' pins is ignored.

DESCRIPTION

The VHDL generator in Library Compiler only supports the pin-to-pin delay model. All timing arcs related to internal pins are ignored. The generated models have incorrect timing behavior and possibly incorrect logic behavior during simulation.

This warning pertains to full-timing structural, optimized gate-level (FTGS), and VITAL models.

WHAT NEXT

If you are generating unit-delay structural models, ignore this warning. Otherwise, modify the technology library to define only pin-to-pin timing arcs.

EXAMPLES

```
    cell(dbvh67) {
      area : 10;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(CP) {
direction : input;
capacitance : 1;
      }
```

```
      statetable ( "D CP", "Q QB") {
table : "L/H R  : - - : L/H H/L,
                -   ~R : - - : N   N";
      }

      pin(Q1) {
direction : internal;
internal_node : "Q";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "CP";
}
      }

      pin(Q) {
direction : output;
state_function  :"Q1";
      }
    }
```

EXAMPLE MESSAGE

```
Warning: The internal timing arc between the 'CP' and 'Q1' pins is ignored. (DBVH-
67)
```

DBVH-68 (error) The '%s' output pin has more than 16 pins in the function.

DESCRIPTION

The VITAL generator in Library Compiler only supports sequential output port with up to 16 input pins in its function. Output functions with large numbers of input ports yield huge truth tables in the generated VITAL models and simulation performance suffers as a result.

This error message pertains only to VITAL models.

WHAT NEXT

If you are not generating VITAL models, ignore this warning. Otherwise, modify the technology library to define output functions using no more than 16 pins. Internal pins can be used to break a large table into several smaller tables.

EXAMPLES

```
    cell(dbvh68) {
      area : 10;
      pin(D D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16) {
direction : input;
capacitance : 1;
      }
      pin(CP) {
direction : input;
capacitance : 1;
      }

   statetable ("D D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 CP", "Q QB
") {
     table : "L/H - H - L - H - L - H - L - H - L R  : - - : L/H H/L,\

              L/H L - L - H - L - H - L - H - L - R  : - - : L/H H/L,\

               - - - - - - - - - - - - - - - - -  ~R : - - : N   N";
      }

      pin(Q) {
direction : output;
internal_node : "Q";
inverted_output : TRUE;
      }
    }
```

EXAMPLE MESSAGE

```
Error: The 'Q' output pin has more than 16 pins in the function. (DBVH-68)
```

DBVH-69 (error) The state table function fails to transform into an FTGS netlist.

DESCRIPTION

The FTGS generator cannot successfully map the state table description into an FTGS netlist. This cell becomes a black box.

This error message pertains only to FTGS models.

WHAT NEXT

If you are not generating FTGS models, ignore this warning. Otherwise, verify the technology library to define output functions.

EXAMPLES

```
    cell(dbvh69) {
      area : 13;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(C) {
direction : input;
capacitance : 2;
      }
      pin(SDI) {
direction : input;
capacitance : 1;
      }
      pin(SE) {
direction : input;
capacitance : 2;
      }
      pin(Q) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "C";
}
      }
      pin(SDO) {
direction : output;
timing() {
  timing_type : falling_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "C";
}
      }

      test_cell() {
pin(D) {
  direction : input;
}
pin(C) {
  direction : input;
}
pin(SDI) {
  direction : input;
  signal_type : "test_scan_in";
}
pin(SE) {
```

```
  direction : input;
  capacitance : 2;
  signal_type : "test_scan_enable";
}
state ("IQ","IQN") {
  force_01 : "C D'";
  force_10 : "C D";
}
pin(Q) {
  direction : output;
  function : "IQ";
}
pin(SDO) {
  direction : output;
  signal_type : "test_scan_out";
}
      }
    }
```

EXAMPLE MESSAGE

```
Error: The state table function fails to transform into an FTGS netlist. (DBVH-69)
```

DBVH-70 (error) Test cell related pin '%s' has unknown unateness.

DESCRIPTION

A test_scan_in or test_scan_enable pin must have known unateness, or the cell becomes a black box.

This error message pertains only to FTGS models.

WHAT NEXT

Verify the technology library.

DBVH-71 (error) Cannot handle multiple clocks in a single state.

DESCRIPTION

Sequential cells with more than one clock in a single state, such as a cell with a system clock and a test scan clock, cannot be transformed into FTGS models succesfully. A black box cell is generated.

This error message pertains only to FTGS models.

WHAT NEXT

Verify the technology library.

EXAMPLES

```
    cell(FFCS) {
      area : 13;
      pin(D D2) {
direction : input;
capacitance : 1;
      }
      pin(C C2) {
direction : input;
capacitance : 2;
      }
      pin(Q) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "C C2";
}
      }
      test_cell() {
pin(D) {
  direction : input;
}
pin(C) {
  direction : input;
}
pin(D2) {
  direction : input;
  signal_type : "test_scan_in";
}
pin(C2) {
  direction : input;
  signal_type : "test_scan_clock";
}
state ("IQ","IQN") {
  next_state : "D";
  clocked_on : "C";
}
pin(Q) {
  direction : output;
  function : "IQ";
  signal_type : "test_scan_out";
}
      }
    }
```

In this case, there are two clocks, ’C’ and ’C2’ defined by the test_scan_clock

type.

EXAMPLE MESSAGE

Error: Cannot handle multiple clocks in a single state. (DBVH-71)

DBVH-72 (error) Error in the library db file.

DESCRIPTION

An error in the library db file is detected. A black box cell is generated.

This error pertains only to FTGS models.

WHAT NEXT

Verify the technology library. It might be a Library Compiler problem.

EXAMPLES

```
    cell(dbvh72) {
      area : 10;
      pin(force11) {
direction : input;
capacitance : 1;
      }
      pin(force10) {
direction : input;
capacitance : 1;
      }
      pin(force01) {
direction : input;
capacitance : 1;
      }
      pin(force00) {
direction : input;
capacitance : 2;
      }
      pin(ck) {
direction : input;
capacitance : 2;
      }
      pin(next) {
direction : input;
capacitance : 2;
      }
      statetable ("next ck ck* force00 force01 force10 force11", "out") {
table : "- - - L H L L : - : L,\

     - - - L H L L : L/H : L,\
```

```
      - - - L L H L : - : H,\

      - - - L L L H : - : H,\

      L/H H L L L L L : - : L/H,\

      - L L L L L L : - : N,\

      - L H L L L L : - : N,\

      - L L L L L L : - : N,\

      - - - - - - - : - : X";
       }

       pin(Q) {
internal_node : "out";
direction : output;
inverted_output : FALSE;
       }
     }
```

EXAMPLE MESSAGE

```
Error: Error in the library db file. (DBVH-72)
```

DBVH-73 (error) Cannot derive the output state when clear and preset are
both active.

DESCRIPTION

```
Library Generator fails to derive clear_preset_var1 from a state table function.
clear_preset_var1 can be L, H, T, N, or X.

A black box cell is generated.

This error message pertains only to FTGS models.
```

WHAT NEXT

```
Verify the technology library.
```

EXAMPLES

```
cell(dbvh73) {
  area : 2.1 ;
  pin(CLK) {
    direction : input;
    capacitance : 0.1;
    clock : true ;
  }
  pin(D) {
    direction : input;
    capacitance : 0.1;
  }
  pin(SET) {
    direction : input;
    capacitance : 0.1;
  }
  pin(CLEAR) {
    direction : input;
    capacitance : 0.1 ;
  }
  ff(IQ,IQN) {
    clocked_on : "CLK" ;
    next_state : "D" ;
    clear : "SET" ;
    preset : "!CLEAR" ;
    clear_preset_var1 : "X" ;
    clear_preset_var2 : "H" ;
  }
  pin(Q1) {
    direction : output;
    function : "IQ" ;
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 1.0;
      fall_resistance : 1.0;
      related_pin : "Q2";
    }
  }
  pin(Q2) {
    direction : output;
    function : "IQN" ;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 1.0;
      fall_resistance : 1.0;
      related_pin : "CLK";
    }
    timing() {
      timing_type : preset;
      timing_sense : positive_unate;
      intrinsic_rise : 1.0;
```

```
          rise_resistance : 1.0;
          related_pin : "SET";
        }
        timing() {
          timing_type : clear;
          timing_sense : positive_unate;
          intrinsic_fall : 1.0;
          fall_resistance : 1.0;
          related_pin : "CLEAR";
        }
      }

    }
```

In this case, the ’CLEAR’ pin has a pulse-width constraint attribute.

EXAMPLE MESSAGE

```
Error: Cannot derive the output state when clear and preset are
        both active. (DBVH-73)
```

DBVH-74 (warning) The cell is in the state table format. Only FTGS and VITAL models might be generated.

DESCRIPTION

The Library Generator only supports FTGS and VITAL generation for the state table format.

WHAT NEXT

If you are generating optimized gate-level models (FTGS) or VITAL models, ignore this warning. Otherwise, change the technology library to modify the description of the cell functionality.

EXAMPLE MESSAGE

```
Warning: The cell is in the state table format. Only FTGS and VITAL
models might be generated. (DBVH-74)
```

DBVH-75 (warning) The timing check between the ’%s’ and ’%s’

pins is ignored.

DESCRIPTION

The timing check cannot be modeled in the FTGS model due to the following reasons:

* One or both pins are not in any sequential function.
* The timing check is a recovery or removal check, and there are more than 5 asynchronous clear pins and more than 5 asynchronous preset pins in a sequential function.

As a result, the timing check is ignored in FTGS models.

This warning message pertains only to optimized gate-level models.

WHAT NEXT

Change the technology library to remove any unecessary timing checks.

EXAMPLES

```
    cell(dbvh75) {
      area : 7;
      pin(D) {
direction : input;
capacitance : 1;
timing() {
  timing_type : setup_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "CP2";
}
timing() {
  timing_type : hold_falling;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "CP2";
}
timing() {
  timing_type : setup_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "CP";
}
timing() {
  timing_type : hold_falling;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "CP";
}
      }
      pin(CP CP2) {
```

```
direction : input;
capacitance : 1;
      }
      ff ("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
clocked_on_also : "CP2";
      }
      pin(Q) {
direction : output;
function : "IQ";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.10;
  fall_resistance : 0.1;
  related_pin : "CP";
}
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "CP2";
}
      }
      pin(QN) {
direction : output;
function : "IQN";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "CP";
}
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "CP2";
}
      }
    }
```

EXAMPLE MESSAGE

```
Warning: The timing check between the 'D' and 'CP2' pins is ignored. (DBVH-75)
```

DBVH-76 (information) A black box TESTSIM model is created for the '%s' cell.

DESCRIPTION

This error message is specific to the fault-simulation structural model when executing the **write_testsim_lib** command with the **-depends** flag.

A black box TESTSIM model is created for this library cell because a model representing the full functionality could not be generated.

WHAT NEXT

All instances of this cell will be black boxes during fault simulation. If this is not what you want, modify your library so that Library Compiler understands the functionality of this cell and can create a good TestSim model.

EXAMPLE MESSAGE

Information: A black box TESTSIM model is created for the 'dbvh76' cell. (DBVH-76)

DBVH-77 (information) Black box TESTSIM models are created for all cells that failed.

DESCRIPTION

This error message is specific to the fault-simulation structural model when executing the **write_testsim_lib** command with the **-depends** flag.

Black box models are created for all failed library cells because models representing the full functionality could not be generated.

WHAT NEXT

All instances of these cells are black boxes during fault simulation.

If this is not what you want, modify your library so that Library Compiler understands the functionality of these cells and can create a good TestSim model for them.

EXAMPLE MESSAGE

Information: Black box TESTSIM models are created for all cells that failed. (DBVH-77)

DBVH-78 (error) A different bus/bundle size is found between bus/bundle ports '%s' and '%s'.

DESCRIPTION

The Library Generator cannot handle bank cells with an inconsistent bus/bundle width. The bank cell must have only one bus/bundle width.

This error message pertains to all simulation models.

WHAT NEXT

Verify the technology library and make sure all bus ports on a bank cell have the same bus/bundle width.

EXAMPLES

```
    cell (dbvh78) {
      area : 1.0;
      pin (WEN) {
direction : input ;
capacitance : 1.0;
      }
      bundle (RA) {
members (RA0, RA1, RA2);
direction : input ;
capacitance : 1.0;
      }
      bundle (WA) {
members (WA0, WA1, WA2, WA3);
direction : input ;
capacitance : 1.0;
      }
      bundle (D) {
members (D0,D1,D2,D3);
direction : input ;
capacitance : 1.0;
      }
      latch_bank (m1, m2, 4) {
enable: "!WEN";
data_in : "D ^ (WA0 ^ WA1 ^ WA2 ^ WA3)";
      }
      bundle (Q) {
members (Q0,Q1,Q2,Q3);
direction : output ;
function : "m1";
timing () {
  related_pin : " D WEN RA0 RA1 RA2 WA0 WA1 WA2 WA3";
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
```

```
  fall_resistance : 0.1;
}
      }
    }
```

EXAMPLE MESSAGE

```
Error: Different bus/bundle size is found between
        bus/bundle ports 'RA' and 'WA'. (DBVH-78)
```

DBVH-79 (error) A RAM cell with more than %d write ports is unsupported.

DESCRIPTION

This error message is specific to the fault-simulation structural model when executing the **write_testsim_lib** command.

The TestSim does not support RAMs with more than two write ports. The RAM cell is modeled as a black box cell.

WHAT NEXT

No action is required.

EXAMPLES

```
cell (dbvh79) {
      area : 1000.0;
      interface_timing : TRUE;

      memory() {
        type : ram;
address_width : 10;
word_width : 8;
      }

      bus (RA) {
bus_type  : "bus10_1";
direction : input;
capacitance : 1.0;
 }
      bus (WA1) {
bus_type  : "bus10_1";
direction : input;
capacitance : 1.0;
      }
      bus (WA2) {
bus_type  : "bus10_1";
```

```
direction : input;
capacitance : 1.0;
      }
      bus (WA3) {
bus_type  : "bus10_1";
direction : input;
capacitance : 1.0;
      }
     bus (DI1) {
       bus_type   : "bus8_1"
       direction : input;
       capacitance : 1.0;
       memory_write() {
          address : WA1;
          enable : WE;
       }
     }
     bus (DI2) {
       bus_type   : "bus8_1"
       direction : input;
       capacitance : 1.0;
       memory_write() {
          address : WA2;
          enable : WE;
       }
     }
     bus (DI3) {
       bus_type   : "bus8_1"
       direction : input;
       capacitance : 1.0;
       memory_write() {
          address : WA3;
          enable : WE;
       }
     }
     pin (WE) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }
     bus(QO){
       bus_type  : "bus8_1";
       direction : output;
       memory_read() {
         address : RA;
       }
       timing () {
           timing_sense : non_unate;
           intrinsic_rise : 1.0;
           rise_resistance : 0.1;
           intrinsic_fall : 1.0;
           fall_resistance : 0.1;
           related_bus_pins : "RA";
       }
    }
```

```
 }
```

EXAMPLE MESSAGE

```
Error: A RAM cell with more than 2 write ports is unsupported. (DBVH-79)
```

DBVH-80 (error) The '%s' RAM is edge-triggered and level sensitive.
TestSim does not support it.

DESCRIPTION

```
TestSim cannot support RAMs specified as having both edge-triggered and level-
sensitive enable types. This cell is modeled as a black box cell.
```

WHAT NEXT

```
Use either edge-triggered or level-sensitive RAMs.
```

EXAMPLES

```
    cell (dbvh80) {
      area : 8000.0;
      interface_timing : TRUE;

      memory() {
        type : ram;
address_width : 4;
word_width : 8;
      }

      bus (RA1) {
           bus_type  : "bus4";
           direction : input;
           capacitance : 1.0;
     }

      bus (RA2) {
           bus_type  : "bus4";
           direction : input;
           capacitance : 1.0;
     }

      bus (WA1) {
           bus_type  : "bus4";
           direction : input;
           capacitance : 1.0;
     }
```

```
      bus (WA2) {
            bus_type  : "bus4";
            direction : input;
            capacitance : 1.0;
      }

      bus (DI1) {
            bus_type   : "bus8_1"
            direction : input;
            capacitance : 1.0;
            memory_write() {
              address : WA1;
              enable : WCLK1;
            }
      }

      bus (DI2) {
            bus_type   : "bus8_1"
            direction : input;
            capacitance : 1.0;
            memory_write() {
              address : WA2;
              clocked_on : WCLK2;
            }
            timing () {
                 timing_type : setup_rising;
                 intrinsic_rise : 1.0;
                 intrinsic_fall : 1.0;
                 related_pin : "WE2";
           }

           timing () {
               timing_type : hold_rising;
               intrinsic_rise : 1.0;
               intrinsic_fall : 1.0;
               related_pin : "WE2";
          }
      }

       pin (WE1 WE2 CLK ) {
direction : input;
capacitance : 1.0;
clock : true;
       }
       pin (WCLK1) {
direction : internal;
capacitance : 1.0;
clock : true;
state_function : "WE1 * CLK";
       }

      pin (WCLK2) {
        direction : internal;
        capacitance : 1.0;
```

```
      clock : true;
      state_function : "WE2 * CLK";
    }

    bus(QO1){
      bus_type  : "bus8_1";
      direction : output;
      memory_read() {
        address : RA1;
      }
   }

    bus(QO2){
      bus_type  : "bus8_1";
      direction : output;
      memory_read() {
        address : RA2;
      }

   }
}
```

EXAMPLE MESSAGE

```
Error: The 'dbvh80' RAM is edge-triggered and level sensitive.
TestSim does not support it. (DBVH-80)
```

DBVH-81 (error) Cannot find the '%s' cell in the testsimmacro.db TestSim library.

DESCRIPTION

The appropriate RAM primitive cannot be found in the testsimmacro.db library in your search_path.

This message is also issued if your RAM cell has more than 24 address lines. RAM cells with more than 24 address lines are not supported. Support can be added on request. Contact the Synopsys Support Center to login this request.

WHAT NEXT

Check that your search_path has v3.4a or later version of testsimmacro.db.

EXAMPLES

```
    type(bus25) {
      base_type : array;
      data_type : bit;
      bit_width : 25;
```

```
      bit_from : 0;
      bit_to : 24;
      downto : false;
    }
    type(bus2) {
      base_type : array;
      data_type : bit;
      bit_width : 2;
      bit_from : 0;
      bit_to : 1;
      downto : false;
    }

    cell (dbvh81) {
      area : 5000.0;
      interface_timing : TRUE;

      memory() {
        type : ram;
address_width : 25;
word_width : 2;
      }

      bus (RA) {
bus_type  : "bus25";
direction : input;
capacitance : 1.0;
timing () {
  timing_type : setup_falling;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "WR";
}
timing () {
  timing_type : hold_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "WR";
}
      }

      bus (DI) {
bus_type   : "bus2";
direction : input;
capacitance : 1.0;
fanout_load : 1.0;

memory_write() {
  address : RA;
  enable : WR;
}
timing () {
  timing_type : setup_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
```

```
  related_pin : "WR";
}

timing () {
  timing_type : hold_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "WR";
}
      }

      pin (WR) {
direction : input;
capacitance : 1.0;
clock : true;
      }

      bus(DO){
bus_type  : "bus2";
direction : output;
memory_read() {
  address : RA;
}

timing () {
  timing_sense : non_unate;
  intrinsic_rise : 1.0;
  rise_resistance : 0.1;
  intrinsic_fall : 1.0;
  fall_resistance : 0.1;
  related_bus_pins : "RA";
}
      }
    }
```

EXAMPLE MESSAGE

```
Error: Cannot find the 'RAM25_LEVEL_SENSITIVE_MACRO' cell in the
testsimmacro.db library TestSim. (DBVH-81)
```

DBVH-82 (error) The '%s' RAM contains complex sequential devices in the wrapper network.

DESCRIPTION

TestSim does not support RAMs with wrapper logic containing complex sequential devices. You must be able to map the sequential devices in the RAM wrapper logic to D flip-flops or D latches. Anything more complex, such as a multiport device, is not supported.

The RAM cell is modeled as a black box cell.

WHAT NEXT

Use simple sequential devices in the input and output wrapper logic network of the RAM.

EXAMPLES

```
    cell (dbvh82) {
      area : 5000.000;
      interface_timing : TRUE;

      memory() {
        type : ram;
address_width : 2;
word_width : 2;
      }

      statetable ( " RA1 RA2 RE1 RE2", "RQ") {
table : "   L/H  -    R   ~R : - : L/H ,\

             -   L/H  ~R   R : - : L/H ,\

             -   -    ~R  ~R : - : N ";
      }

      bus (RA1) {
bus_type  : "bus2";
direction : input;
capacitance : 1.0;
timing () {
  timing_type : setup_falling;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "RE1";
}

timing () {
  timing_type : hold_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "RE1";
}
      }

      bus (RA2) {
bus_type  : "bus2";
direction : input;
capacitance : 1.0;
timing () {
  timing_type : setup_falling;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
```

```
  related_pin : "RE2";
}
timing () {
  timing_type : hold_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "RE2";
}
      }

      bus (RQ) {
bus_type  : "bus2";
direction : internal;
capacitance : 1.0;
pin (RQ[0]) {
  internal_node : "RQ";
  input_map : " RA1[0], RA2[0], RE1, RE2 ";
  timing () {
    timing_type : setup_falling;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "WE";
          }
          timing () {
    timing_type : hold_rising;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "WE";
  }
}
pin (RQ[1]) {
  internal_node : "RQ";
  input_map : " RA1[1], RA2[1], RE1, RE2 ";
  timing () {
    timing_type : setup_falling;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "WE";
          }
          timing () {
    timing_type : hold_rising;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "WE";
  }
}
      }

      bus (DI) {
bus_type   : "bus2";
direction : input;
capacitance : 1.0;
memory_write() {
  address : RQ ;
  clocked_on : WE;
```

```
}
timing () {
  timing_type : setup_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "WE";
}
timing () {
  timing_type : hold_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "WE";
}
      }

      pin (WE RE1 RE2) {
direction : input;
capacitance : 1.0;
clock : true;
      }

      bus(DO){
bus_type  : "bus2";
direction : output;
memory_read() {
  address : RQ;
}
timing () {
  timing_sense : non_unate;
  intrinsic_rise : 1.0;
  rise_resistance : 0.1;
  intrinsic_fall : 1.0;
  fall_resistance : 0.1;
  related_pin : "RA1";
}
      }
    }
```

EXAMPLE MESSAGE

```
Error: The 'dbvh82' RAM contains complex sequential devices in the wrapper network.
 (DBVH-82)
```

DBVH-83 (error) Testsim does not support bundles. The '%s' RAM contains bundle ports.

DESCRIPTION

TestSim does not support RAMs with bundles (bundled ports). The RAM cell will be modeled as a black box cell.

WHAT NEXT

Do not use bundled ports in the RAM cell’s description. Buses are supported so use buses.

EXAMPLES

```
    cell(dbvh83) {
      area : 800.0;
      interface_timing : TRUE;

      memory() {
        type : ram;
address_width : 4;
word_width : 2;
      }

      bundle(RA) {/* not supported */
members(RA1 RA2);
direction : input;
capacitance : 1.0;
timing () {
  timing_type : setup_falling;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "WR";
}
timing () {
  timing_type : hold_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "WR";
}
      }

      bus (DI) {
bus_type   : "bus2";
direction : input;
capacitance : 1.0;
memory_write() {
  address : RA;
  enable : WR;
}
timing () {
  timing_type : setup_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "WR";
}
timing () {
  timing_type : hold_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "WR";
}
```

```
      }

      pin (WR) {
direction : input;
capacitance : 1.0;
clock : true;
      }

      bus(DO) {
bus_type  : "bus2";
direction : output;
capacitance : 1.0;
memory_read() {
  address : RA;
}
timing () {
  timing_sense : non_unate;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_bus_pins : "RA";
}
      }
    }
```

EXAMPLE MESSAGE

```
Error: Testsim does not support bundles. The 'dbvh83' RAM contains bundle ports.(DB
VH-83)
```

DBVH-84 (error) An undriven '%s' net is found in the '%s' cell. RAM modeling failed.

DESCRIPTION

```
There is at least one undriven (internal) net in the TestSim generated RAM model.
The RAM cell is modeled as a black box cell.
```

WHAT NEXT

```
Fix all pertinent warnings and errors generated when reading the RAM library
description file.
```

DBVH-85 (error) A no fanout '%s' net is found in the '%s' cell.

The RAM modeling failed.

DESCRIPTION

There is at least one (internal) net with no fanout in the TestSim generated RAM model. The RAM cell is modeled as a black box cell.

WHAT NEXT

Fix all pertinent warnings and errors generated when reading the RAM library description file.

DBVH-86 (error) An unconnected '%s' port is found in the '%s' cell.
The RAM modeling failed.

DESCRIPTION

There is at least one unconnected port in the Testsim generated RAM model. The RAM cell will be modeled as a black box cell.

WHAT NEXT

Fix all pertinent warnings and errors generated when reading the RAM library description file.

EXAMPLES

```
    cell (dbvh86) {
      area : 8000.0;
      interface_timing : TRUE;
      memory() {
        type : ram;
address_width : 4;
word_width : 8;
      }

      bus (RA1) {
           bus_type  : "bus4";
           direction : input;
           capacitance : 1.0;
     }

      bus (RA2) {
           bus_type  : "bus4";
           direction : input;
```

```
            capacitance : 1.0;
      }

       bus (WA1) {
            bus_type  : "bus4";
            direction : input;
            capacitance : 1.0;
      }

      bus (DI1) {
            bus_type   : "bus8_1"
            direction : input;
            capacitance : 1.0;
            memory_write() {
              address : WA1;
              enable : WCLK1;
            }
      }

       pin (WE1 WE2 CLK ) {
direction : input;
capacitance : 1.0;
clock : true;
       }
       pin (WCLK1) {
direction : internal;
capacitance : 1.0;
clock : true;
state_function : "WE1 * CLK";
       }

      bus(QO1){
        bus_type  : "bus8_1";
        direction : output;
        memory_read() {
          address : RA1;
        }
     }

      bus(QO2){
        bus_type  : "bus8_1";
        direction : output;
        memory_read() {
          address : RA2;
        }
     }
 }
```

EXAMPLE MESSAGE

```
Error: An unconnected 'WE2' port is found in the 'dbvh86' cell.
The RAM modeling failed. (DBVH-86)
```

DBVH-87 (information) The worst-case timing arc is used for non-unate inputs.

DESCRIPTION

The TestSim library generator fits the library cell's pin-to-pin timing onto the TestSim structural netlist for the library cell by lumping delays onto input buffers and output pins.

This can be handled precisely for unate inputs (both positive unate and negative unate). However, for non-unate inputs and for inputs for which the timing sense is unknown, the worst-case timing arc is used.

WHAT NEXT

No action is required.

EXAMPLES

```
    cell(async_single) {
      area : 800.0;
      interface_timing : TRUE;

      memory() {
        type : ram;
address_width : 4;
word_width : 2;
      }

      bus (RA) {
bus_type  : "bus4";
direction : input;
capacitance : 1.0;
timing () {
  timing_type : setup_falling;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "WR";
}

timing () {
  timing_type : hold_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "WR";
}
      }

      bus (DI) {
bus_type   : "bus2";
direction : input;
```

```
capacitance : 1.0;

memory_write() {
  address : RA;
  enable : WR;
}

timing () {
  timing_type : setup_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "WR";
}

timing () {
  timing_type : hold_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "WR";
}
      }

      pin (WR) {
direction : input;
capacitance : 1.0;
clock : true;
      }

      bus(DO){
bus_type  : "bus2";
direction : output;
capacitance : 1.0;

memory_read() {
  address : RA;
}

timing () {
  timing_sense : non_unate;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_bus_pins : "RA";
}
      }
    }
```

EXAMPLE MESSAGE

```
Information: The worst-case timing arc is used for non-unate inputs. (DBVH-87)
```

DBVH-88 (warning) The FTBM architecture is obsolete with 1997.01 release.
The architecture is ignored.

DESCRIPTION

The full-timing behavioral model (FTBM) architecture name identified in the **dc_shell** or **lc_shell** environment variable **vhdllib_architecture** is not supported anymore.

This architecture is supported up to 1996 but not for subsequent releases.

The following architecture names are recognized:

* FTGS (optimized gate-level model)
* VITAL (VITAL model)

The FTBM architecture name is ignored. Recognized architecture names are processed.

WHAT NEXT

Use only the architecture names listed previously. For example,

vhdllib_architecture = {FTGS,VITAL}

EXAMPLES

```
lc_shell> vhdllib_architecture = "dbvhd26_arch"
lc_shell> write_lib -format vhdl dbvh26
```

EXAMPLE MESSAGE

```
Warning: The FTBM architecture is obsolete with 1997.1 release.
The architecture is ignored. (DBVH-88)
```

DBVH-89 (warning) Pin name '%s' on cell '%s' contains underscore characters.
The generated VITAL model will not be VITAL-compliant.

DESCRIPTION

IEEE1076.4 (VITAL) standard disallows underscore characters in pin names. The pin name on the library cell contains one or more underscore characters. The generated VITAL model will not be VITAL level0 compliant.

WHAT NEXT

Remove underscore characters from the pin name.

DBVH-90 (error) DCM delay model is used in library ’%s’.

DESCRIPTION

Library Compiler does not generate any VHDL models for libraries using DCM delay model.

WHAT NEXT

Use only non-DCM delay models.

EXAMPLES

```
lc_shell> write_lib -format vhdl dbvh90
```

EXAMPLE MESSAGE

```
Warning: DCM delay model is used in library ’dbvh90’. (DBVH-90)
```

DBVH-92 (warning) The ’%s’ pin has no invalid timing type for statement "period". The verilog generator will use "posedge" for default.

DESCRIPTION

This warning is given for the following conditions: Liberty file has a simple attribute "minimum_period" in pin group. When verilog generator find this attibute, there is no way to identify edges for period checks from the attribute itself. We may look up in output pin groups, for a timing group with timing_type = rising_edge or falling_edge, where related_pin is same clock pin as in period checks. Rising edge denotes posedge, falling edge denotes negedge.

In case a timing group like this can not be found, verilog generator will issue this warning and assume a posedge for period check.

WHAT NEXT

If you have the proper timing type of this pin, rising_edge or falling_edge. Add the timing type in liberty file for this pin. constraint.

DBVH-93 (error) Could not parse the html file '%s'

DESCRIPTION

An attempt to parse a html file has failed. This problem might be caused by the html file doesn't follow HTML 4.01 standard.

Trying to check whether the html file conforming to HTML 4.01 standard.

WHAT NEXT

check the html file conforming to HTML 4.01 standard.

DBVH-94 (warning) The %s data table in html template does not supported by html datasheet generator.

DESCRIPTION

An attempt to check html table has failed. This problem might be caused by the html table does not follow HTML datasheet generator standard.

Trying to check whether the html table conforming to HTML
datasheet generator standard.

WHAT NEXT

check the html table conforming to HTML datasheet generator standard.

DBVH-95 (error) initialize htmlparser module failed.

DESCRIPTION

System error occurs.

WHAT NEXT

Please contact developper of Library Compiler.

DCDDEFR-1 (error) Netlist Input Mode: Reset & Import; Physical Input Mode: Incremental. This is not supported. Please select again.

DESCRIPTION

```
This error message occurs when Netlist Input Mode is Reset & Import and Physical
Input is Incremental. DEF reader support following 5 type input modes:

Netlist Input ModePhysical Input Mode

Incremental       Incremental IncrementalReset & Import Reset & ImportReset & Import
No Change         Incremental No ChangeReset & Import
```

WHAT NEXT

```
Please select again.
```

DCDDEFR-2 (error) No "LEF File Name" specified (for incremental importing rotated vias and nonDefaultRule).

DESCRIPTION

```
This error message occurs when no 'LEF File Name' is specified.
```

WHAT NEXT

```
Please specify the lef file name.
```

DCDDEFR-3 (error) Cannot advance cell version.

DESCRIPTION

WHAT NEXT

DCDDEFR-4 (error) Detect %s near token '%s' at line %d.

DESCRIPTION

This error message occurs when unexpected syntax has been parsed.

WHAT NEXT

Please change your DEF file according to the DEF manual.

DCDDEFR-5 (warning) NAMECASESENSITIVITY always assumed to be ON.

DESCRIPTION

The read_def parser always assume name case sensitivity to be ON.

WHAT NEXT

Check if the input DEF file is case insensitive.

DCDDEFR-6 (error) Illegal value %d for UNIT specified in input DEF.

DESCRIPTION

The only legal values for UNIT in DEF are 100, 200, 1000, 2000, 10000, 20000. The values of 10000 and 20000 are only supported in DEF 5.6.

WHAT NEXT

Regenerate the DEF file to have correct UNIT.

DCDDEFR-7 (error) The Milkyway database precision (%d) is not a multiple of the input DEF unit (%d), this might cause roundoff error.

DESCRIPTION

This might cause roundoff error.

WHAT NEXT

To continue reading in the input DEF regardless of possible roundoff error, please select the option 'Force Scaling' or use the switch -enforce_scaling.

DCDDEFR-8 (error) Unable to find definition for via %s.

DESCRIPTION

This error message occurs when the definition for this via is neither in the input DEF nor in the reference libraries.

WHAT NEXT

Please make sure that all vias referred in the input DEF are either defined in reference libraries or in the input DEF.

DCDDEFR-9 (warning) The blockage coordinate (%d %d) is out of bound, the coordinates for the die area are (%d %d) (%d %d).

DESCRIPTION

This warning message occurs when the blockage coordinate is out of bound with respect to the die area.

WHAT NEXT

No action is required on your part.

DCDDEFR-10 (warning) Version is a required statement.

Assume version to be 5.5.

DESCRIPTION

This warning message occurs when no VERSION is specified in def file.

WHAT NEXT

No action is required on your part if DEF reader can parse this file, otherwise please specify the correct version.

DCDDEFR-11 (warning) BusBitChars is a required statement. Assume BusBitChars to be ’[]’.

DESCRIPTION

This warning message occurs when no BusBitChars is specified in def file.

WHAT NEXT

Please specify your BusBitChars if ’[]’ is not expected.

DCDDEFR-12 (warning) DividerChar is a required statement. Assume DividerChar to be ’/’.

DESCRIPTION

This warning message occurs when no DividerChar is specified in def file.

WHAT NEXT

Please specify your DividerChar if ’/’ is not expected.

DCDDEFR-13 (warning) Failed to match via layer (%d) for via

(%s) of net %s (%d).

DESCRIPTION

This error message occurs when current layer can not match the via upper or lower layer.

For example, this error will occur when proceed to VIA34. 1) + ROUTED METAL1 (100 200) VIA34 2) + ROUTED METAL1 (100 200) VIA12 (* 300) (200 *) VIA34

WHAT NEXT

Regenerate the DEF file to have correct routing data.

DCDDEFR-14 (error) This scan-in/scan-out pin pair of adjacent components in the ordered list have different owning net.

DESCRIPTION

This error message occurs when scan-in/scan-out pin pair of adjacent components in the ordered list have different owning net.

WHAT NEXT

Regenerate the DEF file to have correct scan-in/scan-out pin pair.

DCDDEFR-15 (error) The scanchain %s is incomplete.

DESCRIPTION

This error message occurs when the scanchain is a broken chain.

WHAT NEXT

Regenerate the DEF file to have complete scanchain.

DCDDEFR-16 (error) Failed to set shape for pin %s.

DESCRIPTION

The error message occurs when the specified layer is not defined in the technology file.

WHAT NEXT

Check the layer name of the pin, make sure it is defined in the technology file.

DCDDEFR-17 (warning) Please execute "auSetLayerPreferDir layerNum #t" to make the preferred wire track direction be vertical for alternating layers. If you don’t use auSetLayerPreferDir, the default preferred wire track direction for all layers is horizontal.

DESCRIPTION

The preferred wire track direction for all layers is horizontal. This may cause problem when you run Astro routing.

WHAT NEXT

There are 3 solutions to solve this problem: 1) Select the option "Set Layer Preferred Direction" in read_def GUI, or the option "-h_layer <list_of_h_layers>" in tcl mode. 2) Execute "auSetLayerPreferDir layerNum #t" to make the preferred wire track direction be vertical for alternating layers. 3) Use axgDefineWireTracks to set the WireDirection objects of "unitTile" cell in design library or reference libraries, which can be used to set preferred wire track direction by read_def.

DCDDEFR-18 (error) The placed pin (%s) does not contain layer information.

DESCRIPTION

If you specify a placement status for a pin, you must also include a LAYER statement.

WHAT NEXT

Regenerate the DEF file to have LAYER statement for the placed pin.

DCDDEFR-19 (error) The spacing between the tracks is less than "min width + min spacing" of the routing layer(Line %d).

DESCRIPTION

This error message occurs when "STEP space" is less than "min width + min spacing" of the specified routing layer(s). Astro router need metal TRACKS to be larger or equal than metal "min width + min spacing".

WHAT NEXT

Manually edit the input DEF file to meet the minimum requirements of our tool flow. Or select option "Adjust Tracks" to recondition the tracks to meet minimum requirements automatically.

DCDDEFR-20 (error) Cannot create rectangle for FILL on layer "%s".

DESCRIPTION

This error message occurs when the specified layer is not defined in the technology file..

WHAT NEXT

Check the layer name of the FILL, make sure it is defined in the technology file.

DCDDEFW-1 (error) No "LEF File Name" specified (for incremental exporting rotated vias and nonDefaultRule).

DESCRIPTION

This error message occurs when no "LEF File Name" is specified.

WHAT NEXT

Please specify a LEF file’s name.

DCDDEFW-2 (warning) Failed to insert layer ’%s’ in hash table.

DESCRIPTION

The write_def command creates a hash table for all the layers present in a design. This message means that write_def failed to insert the layer into the hash table. This could mean that either the name or the id for the layer is invalid.

WHAT NEXT

Please verify if the layer name and id are correct within the DB.

DCDDEFW-3 (warning) Failed to insert via ’%s’ (’%d’) in hash table.

DESCRIPTION

The write_def command creates a hash table for all the vias present in a design. This message means that write_def failed to insert the via into the hash table. This could mean that either the name or the id for the via is invalid.

WHAT NEXT

Please verify if the via name and id are correct within the DB.

DCDDEFW-4 (warning) Undefined layer id '%d'.

DESCRIPTION

Within DB all layers are referenced with their unique id's. This message means that the layer id, which write_def encountered in the DB, does not correspond to any of the layers in DB.

WHAT NEXT

Please verify how this layer id is referenced in the DB. This could be in any of the DEF sections that have layer references.

DCDDEFW-5 (warning) Undefined via id '%d'.

DESCRIPTION

Within DB all vias are referenced with their unique id's. This message means that the via id, which write_def encountered in the DB, does not correspond to any of the vias in DB.

WHAT NEXT

Please verify how this via id is referenced in the DB. This could be in any of the DEF sections that have via references.

DCDDEFW-6 (information) Creating dummy net '%s' for unconnected port '%s'.

DESCRIPTION

There are unconnected ports in the design. For each port of such kind, write_def command will dump a dummy net in the PINS section as well as in the NETS section.

WHAT NEXT

Please verify whether the port(s) are really unconnected.

DCDDEFW-7 (warning) Illegal value for unit (%s) specified.

DESCRIPTION

The value specified does not match the allowed values. The only valid values for DEF UNIT are 100, 200, 1000, 2000, 10000 and 20000. 10000 and 20000 are only supported in DEF 5.6. When an invalid value is specified in the write_def command, the tool uses the conversion factor of main library.

WHAT NEXT

No action is required on your part.

However, if you want, you can specify one of the valid values. You can also see the man page for the write_def command for detailed information on specifying optional or required parameters.

DCDDEFW-8 (warning) Rectangle:(%d %d) (%d %d) edges are on grid, but center point is off-grid. Ignore it in DEF file.

DESCRIPTION

This error is caused by insufficient database unit.

WHAT NEXT

Specify the DEF output unit to be double length resolution of technology file.

Note: when read this DEF file back into the original library, you need to select 'Force Scaling' option (-enforce_scaling switch).

DCFPGA_PART-1 (Error) Invalid step value '%s' for the device '%s'.

DESCRIPTION

You receive this message because the step value specified for the target part is invalid.

DCFPGA_UISN-1 (warning) partition_dp command is disabled for fpga technology.

DESCRIPTION

partition_dp command is not applicable while targeting fpga technology.

WHAT NEXT

DCFPGA_UEGI-1 (error) Clearbox path not defined.

DESCRIPTION

This error message occurs when Design Compiler FPGA cannot find the path to Altera's Clearbox loader (External logic generator).

WHAT NEXT

Set the UNIX **CLEARBOX_EXEC_PATH** environment variable to the absolute path to the Clearbox loader.

DCFPGA_TRI-1 (warning) Three-state bus %s is connected to the black-box inout pin %s(%s). Three-state to mux conversion

cannot happen.

DESCRIPTION

This warning message occurs when the specified three-state bus is connected to a black box cell. Since there can be three-state drivers inside the black box, Design Compiler FPGA cannot convert this bus to MUX logic. This results in unmapped three-state elements in the netlist.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Try setting the Boolean **fpga_blackbox_inout_as_bus_load** variable to **TRUE**. Design Compiler FPGA converts three-state buses to MUX logic by considering the black box pins as input pins. Make this setting only if you are sure that the bus under consideration is not driven by any more three-state elements from inside the black box.

SEE ALSO

fpga_blackbox_inout_as_bus_load(3)

DCFPGA_ROM-1 (information) Unable to implement constant MUX_OP cell '%s' using architecture specific ram blocks.

DESCRIPTION

You receive this message because DCFPGA could not implement the constant MUX_OP cell using architecture specific ram blocks.

DCFPGA_RAM-1 (error) RAM operators in design cannot be expanded.

DESCRIPTION

The RAM operators that are inferred for this design cannot be expanded. This may be because RAM Inference is not supported for this technology or the synthetic libraries provided do not describe how to implement the RAM operator.

WHAT NEXT

Make sure that RAM Inference is supported for this technology, by referring to the RAM Inference Application Notes.

Make sure that you have enabled **Tornado Module Generator** since RAM implementations are only provided for this particular flow.

DCFPGA_BUFG-1 (warning) BUFG resource '%s' being removed from design '%s' to be redeployed"

DESCRIPTION

You receive this message because the DCFPGA has removed a BUFG that does not have a dont_touch attribute on it. The removed BUFGs will be redeployed by the clock buffer insertion algorithm at the higher fanout clock nets.

WHAT NEXT

DCFPGA_COUNTER-1 (information) Inferred Counter '%s' of width '%d' in design '%s'

DESCRIPTION

WHAT NEXT

DCFPGA_CMD-1 (warning) This command is not applicable to Design Compiler FPGA.

DESCRIPTION

This warning message occurs when you use a command that is not supported for Design Compiler FPGA synthesis.

WHAT NEXT

Enable this command using the **fpga_enable_commands** variable.

SEE ALSO

fpga_enable_commands(3)

DCFPGA_DEATOM-1 (warning) Invalid %s '%s' is detected. Skipping deatomization.

DESCRIPTION

You receive this message because the library complex cell under deatomization is detected as an invalid one.

DCFPGA_PMCD-1 (information) Propagating clocks through cell '%s' instantiated from design '%s'.

DESCRIPTION

This information message occurs when the tool is generating output clocks for special cells, such as PMCD.

WHAT NEXT

This is only an information message. No action is required.

DCFPGA_PLL-1 (information) Propagating clocks through cell '%s' instantiated from design '%s'.

DESCRIPTION

This information message occurs when the tool is generating output clocks for special cells, such as ALTPLL.

WHAT NEXT

This is only an information message. No action is required.

DCFPGA_DCM-1 (information) Propagating clocks through cell

'%s' instantiated from design '%s'.

DESCRIPTION

Generate ouput clocks for special cells such as DLL/DCM.

DCFPGA_FM-1 (warning) You need to perform set_svf to enable generation of setup information for formality.

DESCRIPTION

Use set_svf to generate a Formality setup information file to ensure efficient compare point matching in Formality.

WHAT NEXT

To avoid receiving this message, perform a set_svf prior to issuing set_fpga_defaults -formality

SEE ALSO

set_svf(2).

DCFPGA_LPM-1 (error) LPM library (lpm.sldb) required for technology mapping not found in synthetic library set.

DESCRIPTION

You receive this message because Design Compiler FPGA requires lpm.sldb in the synthetic_library set to perform some technology mapping for the target architecture you have chosen.

WHAT NEXT

Add lpm.sldb (provided as part of Design Compiler FPGA installation), to the "synthetic_library" and "link_library" and try again.

DCFPGA_LUT7-1 (warning) Invalid lut_mask '%s' is detected.

Place and Route may fail for this 128 bit lut_mask.

DESCRIPTION

You receive this message because the LUT7 lut_mask for stratixii_lcell_comb is detected as an invalid one. You need to convert this 128 bit INIT value to 64 bit lut_mask.

DCFPGA_MULT18X18S-1 (information) Multiplier %s not considered for MULT18X18S inference.

DESCRIPTION

One of the output nets(%s) of multiplier cell drives multiple loads. DCFPGA neglects such multipliers for MULT18X18S inference.

WHAT NEXT

DCFPGA_PAD-1 (information) 'dont_touch' on cell %s (%s) has been ignored for pad mapping.

DESCRIPTION

This information message occurs when your FPGA vendor no longer supports the named primitive, but supports unified primitives instead. Design Compiler FPGA ignores the don't touch attribute to replace the old primitive with the newer primitive.

WHAT NEXT

This is only an information message. No action is required.

DCFPGA_MUX-1 (information) MUX_OP: '%s' extracted.

DESCRIPTION

You receive this message because a SELECT_OP cell is converted into a MUX_OP cell.

DCFPGA_BUFG-2 (warning) Can not insert global buffer '%s' at pin '%s'. The maximum permissible resource limit '%d' for this PART has reached.

DESCRIPTION

You receive this message because all the resources of the type mentioned in the message for this PART have been completely utilized and there no global clock buffers of the type mentioned above are available for insertion at this pin.

WHAT NEXT

DCFPGA_DCM-2 (information) The clock '%s' with period '%s' generated on pin '%s'.

DESCRIPTION

Generate a clock for ouptut pin of special cells such as DLL/DCM.

DCFPGA_CMD-2 (warning) No command matched the name '%s'.

DESCRIPTION

This warning message occurs when none of the commands match this command specified in the **fpga_enable_commands** list.

WHAT NEXT

To view all of the disabled commands that can be enabled using the **fpga_enable_commands** variable, invoke the **list_commands** Tcl command from the Design Compiler FPGA shell. The **list_commands** command displays a group of commands that are disabled for Design Compiler FPGA.

SEE ALSO

fpga_enable_commands(3)

DCFPGA_MULT18X18S-2 (information) Register driven by net %s, is not pulled in.

DESCRIPTION

Net has multiple loads. DCFPGA does not pull in any register driven by such net and also neglects any other registers present at the same level.

WHAT NEXT

DCFPGA_ADDABC-2 (information) Cell %s is not considered for ADD_ABC inference.

DESCRIPTION

Some of the output pins of the cell are not connected. DCFPGA neglects such cells for ADD_ABC inference.

WHAT NEXT

DCFPGA_ROM-2 (information) The select or output lines of constant MUX_OP cell ’%s’ contains "infer_rom" attribute with value ’%s’.

DESCRIPTION

You receive this message because DCFPGA could not implement the constant MUX_OP cell using architecture specific ram blocks as the output or the select lines of the constant MUX_OP cell contains "infer_rom" attribute with value other than "block".

WHAT NEXT

You can remove the "infer_rom" attribute from the select or output lines or you can set the value as "block".

DCFPGA_MUX-2 (warning) Cell : ’%s’ can not be converted into

MUX_OP.

DESCRIPTION

You receive this message because the SELECT_OP cell can not be converted into a MUX_OP cell.

DCFPGA_PLL-2 (information) The clock '%s' with period '%s' generated on pin '%s'.

DESCRIPTION

Generate a clock for ouptut pin of special cells such as ALTPLL.

DCFPGA_PMCD-2 (information) The clock '%s' with period '%s' generated on pin '%s'.

DESCRIPTION

This information message occurs when the tool generates a clock for an output pin of special cells, such as PMCD.

WHAT NEXT

This is only an information message. No action is required.

DCFPGA_RAM-2 (information) Converting Dual Port RAM %s to Single Port RAM.

DESCRIPTION

The Dual Port RAM is being converted to Single Port RAM. This is done if, the data_out_a port is unused and both the ports share the same address lines.

DCFPGA_RAM-3 (information) RAMs %s and %s are merged.

DESCRIPTION

Two RAM operators are merged to form a single operator to improve area.

DCFPGA_ROM-3 (information) The number of address lines '%d' of constant MUX_OP cell '%s' is less than the minimum width '%d' specified by user.

DESCRIPTION

You receive this message because DCFPGA could not implement the constant MUX_OP cell using architecture specific ram blocks as the number of address lines is less than the minimum number of address lines specified by the user.

WHAT NEXT

Incase you want the architecture specific ram block for this constant MUX_OP, decrease the minimum value by using the variable fpga_block_rom_min_addr_width.

DCFPGA_MULT18X18S-3 (information) Register %s is not similar to register %s.

DESCRIPTION

DCFPGA neglects any register level from pulling into pipelined multiplier, if any of the registers in that level is not similar to the registers in the previous level.

WHAT NEXT

DCFPGA_CMD-3 (warning) Command '%s' is already enabled in Design Compiler FPGA.

DESCRIPTION

This error message occurs when you try to enable a command that is already available in the Design Compiler FPGA shell.

WHAT NEXT

Remove the command name from the **fpga_enable_commands** list.

SEE ALSO

fpga_enable_commands(3)

DCFPGA_MULT18X18S-4 (information) Suitable pipelined multiplier not found. You may need to add Designware Foundation to synthetic_library.

DESCRIPTION

WHAT NEXT

DCFPGA_CMD-4 (information) Ultra optimizations applicable to FPGA are already incorporated into the Design Compiler FPGA flow.

DESCRIPTION

This information message occurs because Ultra compiler optimizations that apply to FPGA synthesis is already a part of the standard FPGA synthesis flow. There is no need to invoke any Ultra commands to perform these tasks.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

fpga_enable_commands(3)

DCFPGA_ADDABC-4 (information) Cell %s is already

considered for ADD_ABC inference.

DESCRIPTION

This cell is already a part of another ADD_ABC module.

WHAT NEXT

DCFPGA_ROM-4 (information) The number of address lines '%d' of constant MUX_OP cell '%s' is greater than the maximum width '%d' specified by user.

DESCRIPTION

You receive this message because DCFPGA could not implement the constant MUX_OP cell using architecture specific ram blocks as the number of address lines is greater than the maximum number of address lines specified by the user.

WHAT NEXT

Incase you want the architecture specific ram block for this constant MUX_OP, increase the maximum value by using the variable fpga_block_rom_max_addr_width.

DCFPGA_RAM-4 (information) Pulled in registers at port %s for RAM %s.

DESCRIPTION

The registers at the given port have been pulled into the RAM operator.

DCFPGA_ADDABC-5 (information) Cell %s is not the first valid

cell for ADD_ABC inference.

DESCRIPTION

WHAT NEXT

DCFPGA_MULT18X18S-5 (information) Pipelined multiplier not inferred. %d registers expected, but only %d are found.

DESCRIPTION

WHAT NEXT

DCFPGA_RAM-5 (information) No read operation at Port A for Dual Port RAM %s.

DESCRIPTION

DCFPGA_ROM-5 (information) The total number of rom bits '%d' of constant MUX_OP cell '%s' is less than the minimum number of rom bits '%d' specified by the user.

DESCRIPTION

```
You receive this message because DCFPGA could not implement the constant MUX_OP cell
using architecture specific ram blocks as the total number of rom bits is less than
the minimum number of rom bits specified by the user.
```

WHAT NEXT

```
Incase you want the architecture specific ram block for this constant MUX_OP,
decrease the minimum value by using the variable fpga_block_rom_min_total_bits.
```

DCFPGA_MULT18X18S-6 (information) Suitable pipelined

multiplier not found. Cell %s(DW02_mult) has variable TC port and drives registers with Sync Clear/Enable.

DESCRIPTION

WHAT NEXT

DCFPGA_ADDABC-6 (information) Cell %s is not considered for ADD_ABC inference.

DESCRIPTION

One of the output nets of the cell drives multiple loads. DCFPGA neglects such cells for ADD_ABC inference.

WHAT NEXT

DCFPGA_ROM-6 (information) There is no valid register bank at the address or output lines of constant MUX_OP cell ’%s’.

DESCRIPTION

You receive this message because DCFPGA could not implement the constant MUX_OP cell using architecture specific ram blocks as there is no valid register bank at the address or output lines of the constant MUX_OP cell. The registers at the address lines can have only clock and clock enable signals and the registers at the output lines can have asynchronous signals.

WHAT NEXT

Incase you want the architecture specific ram block for this constant MUX_OP, place valid register banks at the address or output lines.

DCFPGA_RAM-6 (information) Read operation at Ports A and B are not of the same type. Unable to implement RAM %s of configuration "Address width: %d, Data width: %d, Type: %s"

using Block RAMs.

DESCRIPTION

DCFPGA_RAM-7 (information) Read operation at Port B is not synchronous. Unable to implement RAM %s of configuration "Address width: %d, Data width: %d, Type: %s" using Block RAMs.

DESCRIPTION

DCFPGA_ADDABC-7 (information) Cannot infer ADD_ABC.

DESCRIPTION

The cells doesn’t have compatiable output widths. DCFPGA neglects such cells for ADD_ABC inference.

WHAT NEXT

DCFPGA_MULT18X18S-7 (information) Inferred %d stage multiplier for cell %s.

DESCRIPTION

WHAT NEXT

DCFPGA_ROM-7 (information) The register bank at the address or output lines of constant MUX_OP cell ’%s’ has a

fanout greater than one.

DESCRIPTION

You receive this message because DCFPGA could not implement the constant MUX_OP cell using architecture specific ram blocks as the registers at the address or output lines has a fanout greater than one.

DCFPGA_RAM-8 (information) Read operation at Port B has a data enable. Unable to implement RAM %s of configuration "Address width: %d, Data width: %d, Type: %s" using Block RAMs.

DESCRIPTION

DCFPGA_ADDABC-9 (information) Suitable ADD_ABC module not found in the synthetic_library.

DESCRIPTION

WHAT NEXT

DCFPGA_RAM-9 (information) Read and Write operations are from different clocks%s. Unable to implement RAM %s of configuration "Address width: %d, Data width: %d, Type: %s" using Block RAMs.

DESCRIPTION

DCFPGA_RAM-10 (information) Read operation has an enable%s. Unable to implement RAM %s of configuration "Address width: %d, Data width: %d, Type: %s" using Block

RAMs.

DESCRIPTION

DCFPGA_RAM-11 (information) Only write first mode is supported for VIRTEXE technology. Unable to implement RAM %s of configuration "Address width: %d, Data width: %d, Type: %s" using Block RAMs.

DESCRIPTION

DCFPGA_RAM-12 (information) Data or address width is too small. Unable to implement RAM %s of configuration "Address width: %d, Data width: %d, Type: %s" using Block RAMs. Set the variables fpga_ramb_min_address_width and fpga_ramb_min_total_bits appropriately to infer BLOCK RAM.

DESCRIPTION

DCFPGA_RAM-13 (information) Choosing %s implementation for RAM %s.

DESCRIPTION

```
The HDL specified implementation for this RAM is not valid. So, a new appropriate
implementation is chosen.
```

DCFPGA_RAM-14 (information) RAM %s is implemented using %s RAM primitives.

DESCRIPTION

DCM-100 (warning) Unable to load DCM library for '%s'. Using the default delay model as specified in the .db library.

DESCRIPTION

The program is unable to load the DCM library corresponding to the .db library as specified in the error message. This happens because of one of the following reasons:

* One or more of the following shell environment variables
  are not set or are incorrectly set:
DCMRULEPATH (or CDCRULEPATH)
DCMRULESPATH (or CDCRULESPATH)
DCMTABLEPATH (or CDCTABLEPATH)
* The DCM library does not exist in the location specified or
  it does not have the proper file permissions.
* Your installation is not authorized for the DCM-Delay-Calculation
          feature.

When this error is encountered, the program treats the library as a non-DCM library and derives the delay model as though it were a .db library.

WHAT NEXT

The error messages preceding this one should make the exact cause of the problem clear. Make sure that the aforementioned shell environment variables are set correctly and the DCM library exists as specified with the correct file permissions. Make sure your Synopsys key file includes the DCM-Delay-Calculation license.

DCM-101 (error) Errors found during rule_init() - library '%s' will be unloaded.

DESCRIPTION

The PI function rule_init() of the Delay Calculation System (DCS) standard returned an error code. Typically, the DCS itself issues the diagnostic messages that display before this message. When this message is issued, the program cannot load the remaining DCM subrules and link the EXPOSE and EXTERNAL functions correctly.

WHAT NEXT

Please contact the library provider or Synopsys if you encounter this message.

DCM-102 (warning) No DCM model for cell '%s' of library '%s'.

DESCRIPTION

This error message is issued when the DCM library returns a nonzero error status

WHAT NEXT

Check the error messages issued by the DCM prior to this error message and correct any problems. Verify that you have matching versions of the DCM timing and auxilary cell libraries. Contact your library provider for more information.

DCM-103 (error) Unable to load DCM EXPOSE function '%s' from the DCM library. This library cannot be used by this program without the specified EXPOSE function.

DESCRIPTION

This message is issued when the program tries to load the specified DCM EXPOSE function from the specified DCM library and cannot locate a matching function. Because this EXPOSE function is considered critical for the proper calculation of delay values, this library cannot be used by this program for timing calculations.

WHAT NEXT

Please contact your library provider for more information.

DCM-104 (error) The following feature of the DCL language is not (yet) supported by this program: %s.

DESCRIPTION

The current implementation of the program does not fully support the specified

feature of the Delay Calculation System (DCS) standard specification. This can result in this particular DCM library being unsuitable for use for delay calculations by this program.

WHAT NEXT

You cannot use this DCM library for timing calculations until this restriction is removed. Please contact your library provider to see if a version of the library without the specific feature is available.

DCM-105 (error) Error while processing DCL external function '%s' - passed pin '%s' is not part of the current timing arc.

DESCRIPTION

The DCL-PI standard defines a number of functions that request the netlist information from the timer application using the pin name rather than the pin pointer. The current implementation of the program supports this feature only as long as the referenced pin name is part of the timing arc currently under consideration. That is, you can substitute the external call with the equivalent byPin() call.

by the equivalent byPin() call.

WHAT NEXT

If you have access to the DCM library source, modify it such that the equivalent byPin() function is used instead of the named external function. Otherwise, please contact your library vendor. equivalent byPin() function is used instead of the named external function. Otherwise, please contact your library vendor.

DCM-106 (warning) The DCL-PI function '%s' returned a nonzero error code %d while processing the timing segment '%s'.

DESCRIPTION

This message appears when the program calls one of the CALCULATION functions as defined in the DCS standard specification and that function returns a bad error code. This typically indicates a problem in the DCM library itself.

WHAT NEXT

If you have access to the DCL source code of the library, modify please contact your library provider.

DCM-107 (warning) Unsupported test type or edge propagation pair '%s' specified for the arc '%s'. This arc will be ignored.

DESCRIPTION

This message is displayed when the program loads the timing arc and detects that test type or the edge propagation characteristics specified for this arc types and edge propagation pairs, please consult your documentation.

WHAT NEXT

If you have access to the DCL source code of the library, change program. Otherwise, please contact your DCM library provider.

DCM-108 (warning) Internal timing pin '%s' of cell '%s' in library '%s' is not defined in the corresponding .db library. Any timing arcs connecting to or from this pin will be ignored.

DESCRIPTION

This message is displayed when the program loads the timing arcs and detects that the DCM has requested the creation of a new timing point, but no of the library cell's pins, including the internal timing points, must be defined in the technology library .db file before they can be referenced in the DCM.

WHAT NEXT

If you have access to the source code of the Synopsys technology library (.lib) corresponding with the DCM being loaded, you can add a new internal timing pin for the corresponding cell in the library. Note that current limitations of the Library Compiler product dictate that a "timing()" group must be present for each internal timing pin. However, when using the DCM library, all the each internal timing pin. However, when the DCM library is used, all the timing information comes from the DCM

library and any timing data specified in the .db library is ignored.

DCM-109 (warning) %s '%s' is invalid. The valid values are '%s' and '%s'

DESCRIPTION

This message is displayed when an invalid version is set.

WHAT NEXT

Change the version to one of the valid values and re-run the design.

DCM-110 (warning) DPCM expose dpcmAddWireLoadModel not supported in DPCL library. Therefore DB/custom wireload models are not supported.

DESCRIPTION

This message is displayed when the expose dpcmAddWireloadModel is not supported in the DPCM Procedural Interface.

WHAT NEXT

Use DPCM wireloads. If db wireload has to be used support the expose in DPCM.

DCM-111 (warning) The design %s read in has wireload %s, which is not present in the current DPCM. Changing to default DPCM wireload %s.

DESCRIPTION

You receive this warning message when the current wireload attached to the design is not present in one of the DPCM libraries.

WHAT NEXT

Use a wireload that is in one of the DPCM libraries. To see a list of wireloads in

the DPCM libraries, use the **report_lib** command.

DCM-112 (warning) The design %s read in has a DCPM wireload %s. Deleting the dpcm wireload.

DESCRIPTION

This message is displayed when the current wireload attached to the design is from a DPCM library and not db.

WHAT NEXT

Use DB wireloads. List DB wireloads by doing report lib.

DCM-113 (information) Propagating clocks through cell '%s' instantiated from design '%s'.

DESCRIPTION

Generate ouput clocks for special cells such as DLL/DCM.

DCM-114 (information) The clock '%s' with period '%s' generated on pin '%s'.

DESCRIPTION

Generate a clock for ouptut pin of special cells such as DLL/DCM.

DCM-115 (information) Please check CLKFX_DIVIDE value: '%s'.

DESCRIPTION

CLKFX_DIVIDE value is not valid.

DCM-116 (information) Please check CLKFX_MULTIPLY value: '%s'.

DESCRIPTION

CLKFX_MULTIPLY value is not valid.

DCM-117 (information) Please check CLKDV_DIVIDE value: '%s'.

DESCRIPTION

CLKDV_DIVIDE value is not valid.

DCM-118 (warning) During the polynomial reduction procedure, the '%s' variable is saturated from %f to %f.

DESCRIPTION

This warning message occurs when a boundary value instead of the original variable value is used for polynomial reduction.

WHAT NEXT

A polynomial is reduced before final calculation if its parameters contain one of the following variables defined in the operating conditions: *temperature*, *parameter1*, *parameter2*, *parameter3*, *parameter4*, *parameter5*, *voltage*, *voltage1*, ..., *voltage99*.

If the variable value defined in the operating conditions is out of the boundary defined in the polynomial, then the closest boundary value for the variable will be used for polynomial reduction.

For example, if the *temperature* variable defined in the current operating condition is 20, while the range of the *temperature* in the polynomial is [25, 40], then 25 instead of 20 is used to reduce this polynomial.

DCSH-1 (fatal) %s is not enabled.

DESCRIPTION

You don’t have the given license available.

WHAT NEXT

Check and get the desired license by invoke the **get_license** command.

DCSH-3 (fatal) System ".synopsys

DESCRIPTION

WHAT NEXT

DCSH-7 (fatal) Error in .synopsys file. Cannot continue.

DESCRIPTION

If there is an error is issued during reading the .synopsys file from the synopsys root, the Design Compiler will exits.

Fatal in reading .synopsys file includes syntax errors found.

Sample errors are

Error: Undefined operator on or near line %d at or near ’%s’. (EQN-2) Error: Previous error has stopped reading include file ’%s’. (UI-21)

WHAT NEXT

Run Design Compiler with -no_init option will eleminate this error.

Identify and correct the cause of the fatal in reading .synopsys file and reinvoke the dc_shell or design_analyzer.

DCSH-9 (fatal) %s: could not connect to parent '%s'.

DESCRIPTION

WHAT NEXT

DCSH-10 (fatal) At least one of the following must be enabled : %s.

DESCRIPTION

WHAT NEXT

DCSH-11 (error) Can't read Tcl file %s in your working directory because
you read the default format in home init.

DESCRIPTION

In default dc_shell (dcsh) mode, the program just read default dcsh format in home init. Now it can't read Tcl file in your working directory. In default dcsh mode, the setup files are supported as follow:

Synopsys RootHome Working Directory ---------- - Tcl-subset dcsh dcsh Tcl-subset Tcl-subset Tcl-subset Tcl-subset Tcl-subset dcsh Tcl-subset dcsh Tcl-subset NON SUPPORT

WHAT NEXT

Convert your Tcl file into the default format in your current working directory and rerun the program. Or you may continue the program.

DCSH-12 (error) No additional DC-XG licenses are available.

DESCRIPTION

You receive this message because all your DC-XG licenses are already checked out or your site is not enabled for DC-XG license feature.

This license feature is required while DesignCompiler is in xg-mode.

As soon as DC switches to xg-mode one token of DC-XG license feature is checked out. Upon leaving xg-mode the token is checked in again.

WHAT NEXT

Do one of the following, and then try again to enter xg-mode:

- Use command license_users to check who else is working with XG mode.
- Quit any other dc_shell that uses DC-XG licenses.
- Wait until any other dc_shell that uses DC-XG licenses is done.
- Obtain more license tokens.

SEE ALSO

list_licenses (2), **license_users** (2)

DCSH-13 (information) Checking out DC-XG license token.

DESCRIPTION

You receive this message because you have entered XG mode.

As soon as DC switches to xg-mode one token of DC-XG license feature is checked out. Upon leaving xg-mode the token is checked in again.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

list_licenses (2), **license_users** (2)

DCSH-14 (information) Successfully checked out feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE in dc_shell.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

DCSH-15 (information) Started queuing for feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE in dc_shell.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

DCSH-16 (information) Still waiting for feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE in dc_shell.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

DCSH-17 (information) Timeout while waiting for feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE in dc_shell.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

DCSH-18 (information) License queuing is enabled.

DESCRIPTION

You receive this message because you have enabled licensing queuing.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

DCT-001 (Error) Hierarchical cell %s is an ILM, cannot set as a physical hierarchy.

DESCRIPTION

You receive this error message because a hierarchical cell cannot be a physical hierarchy if it is already an ILM.

WHAT NEXT

To have this cell as a physical hierarchy, please provide the full netlist of the hierarchy at the top level, instead of an ILM.

SEE ALSO

set_physical_hierarchy (2), **create_ilm** (2)

DCT-002 (Error) Cell %s is not a hierarchical cell placed by DCT, thus cannot be set as a physical hierarchy.

DESCRIPTION

You receive this error message because for a cell to be set as a physical hierarchy, it has to be a hierarchical cell placed by DCT.

WHAT NEXT

To have this cell as a physical hierarchy, please make sure the cell is a hierarchical cell and provide DCT placed full netlist of the hierarchy at the top level.

SEE ALSO

set_physical_hierarchy (2), **create_ilm** (2)

DCT-003 (Info) Cell %s is a physical hierarchy already. The

command is ignored.

DESCRIPTION

You receive this information message because for a cell has been set as a physical hierarchy by a previous set_physical_hierarchy command. The currently issued command is ignored.

WHAT NEXT

To avoid getting this message, dont issue set_physical_hierarchy on the same cell more than once.

SEE ALSO

set_physical_hierarchy (2)

DCT-004 (warning) The newly created cell does not have location. Timing will be inaccurate.

DESCRIPTION

This warning message occurs when you create a new cell in DC topographical mode by using the command create_cell. In topographical mode, DC uses cell locations to estimate net delays. Since the new cell does not have a location, the timing information for the nets connected to this cell will not be accurate.

WHAT NEXT

You can assign cell locations by running compile_ultra -incremental, which also updates the timing information for the nets. You can also set cell location using set_cell_location -fixed, and then call update_timing or report_timing to update the net delays.

SEE ALSO

report_timing(2)
set_cell_location(2)

DCT-005 (Error) Cannot run compile_ultra incremental in congestion mode.
Design was not compiled with DC-Topographical congestion

optimizations.

DESCRIPTION

You receive this error message because **compile_ultra** incremental in congestion mode cannot be used with designs that were compiled in DC-Topographical non-congestion mode.

WHAT NEXT

Rerun **compile_ultra** in non-incremental congestion mode to get the benefits of DC-Topographical congestion optimization.

SEE ALSO

DCT-006 (Warning) Some checks cannot be performed because of previous errors.

DESCRIPTION

You receive this error message because **compile_ultra -check_only** meets some errors before some checks are executed.

WHAT NEXT

Make sure your target library is not empty and physical layer data is sufficient.

SEE ALSO

DCT-007 (Information) Total fixed/moveable cell area and utilization are not completely calculated because the design contains unmapped logic.

DESCRIPTION

You receive this message because the design contains unmapped logic.

WHAT NEXT

Compile the design, then apply **report_area -physical**.

SEE ALSO

DCT-008 (Information) Core area and utilization/aspect ratio were not calculated because there are no site rows.

DESCRIPTION

You receive this message because no site rows are applied during **extract_physical_constraints**.

WHAT NEXT

Check the DEF contains legal site rows, then use **extract_physical_constraints** to apply them.

SEE ALSO

DCT-009 (Error) Failed to generate intermediate file used to extract physical constraints.

DESCRIPTION

You receive this error message because **extract_physical_constraints** failed to generate an intermediate file, which is used to save the physical constraints extracted from DEF.

WHAT NEXT

Make sure you have write permissions on the following place: (1) the place of the env variable TMPDIR, if you set it. (2) the current directory ".", if env variable TMPDIR is not set. (3) the default "/tmp";

SEE ALSO

DCT-010 (Error) Failed to apply physical constraints.

DESCRIPTION

You receive this error message because **extract_physical_constraints** failed to apply the physical constraints extracted from the DEF.

WHAT NEXT

Make sure the intermediate file was not modified.

SEE ALSO

extract_physical_constraints (2)

DCT-011 (Error) at line: %d, failed to apply the physical constraints command:
%s

DESCRIPTION

You receive this error message because **extract_physical_constraints** failed to apply the command printed out.

WHAT NEXT

Make sure the intermediate file was not modified.

SEE ALSO

extract_physical_constraints (2)

DCT-012 (Error) Inconsistent number of physical constraints:

%d extracted while %d applied

DESCRIPTION

You receive this error message because the number of extracted commands is not consistent with the applied one in **extract_physical_constraints**.

WHAT NEXT

Make sure the intermediate file was not modified.

SEE ALSO

extract_physical_constraints (2)

DCT-016 (Error) Failed to recognize the type of net shape.

DESCRIPTION

You receive this error message because **create_net_shape** cannot recognize the type of net shape from the specified options.

WHAT NEXT

Please check: (1) "-points", "-bbox" or "-origin" cannot be specified together, and at least one of them should be specified. (2) "-points" should be specified with "-type path", "-bbox" should be specified with "-type rect|bbox", "-origin" should be specified with "-type rect".

SEE ALSO

extract_physical_constraints (2)

DCT-017 (Error) Only horizontal or vertical net shapes allowed.

DESCRIPTION

You receive this error message because invalid value of option '-points' is specified in **create_net_shape**.

WHAT NEXT

Please check the values specified in "-points", ensure that segment in the path should be vertical or horizontal.

SEE ALSO

extract_physical_constraints (2)

DCT-018 (Error) net shape geometry style ’%s’ should be specified in option ’%s’.

DESCRIPTION

You receive this error message because invalid value of option specified in **create_net_shape**.

WHAT NEXT

SEE ALSO

extract_physical_constraints (2)

DCT-019 (Error) mutually exclusive options: ’-points’, ’-origin’ and ’-bbox’.

DESCRIPTION

You receive this error message because ’-points’, ’-origin’ and ’-bbox’ cannot be used together in **create_net_shape**.

WHAT NEXT

SEE ALSO

extract_physical_constraints (2)

DCT-020 (Information) net shape with type %s will be created

during compile.

DESCRIPTION

You receive this message because the physical information of **create_net_shape** is recorded, and the real net shape will be created in compile.

WHAT NEXT

SEE ALSO

extract_physical_constraints (2)

DCT-021 (Information) %d net shapes were created from physical constraints.

DESCRIPTION

You receive this message because real net shapes were created from the physical information recorded from the command **create_net_shape**.

WHAT NEXT

SEE ALSO

extract_physical_constraints (2)

DCT-022 (Error) Failed to transfer current design to MW database.

DESCRIPTION

This error occurs when the tool failed to transfer the DC design into Milkyway CEL database. The command you are using requires that the design will be saved as an intermediate CEL in the current Milkyway library. For this command to work properly, it is required that you use Milkyway library for the physical data of the design.

WHAT NEXT

Use **open_mw_lib** command to open an existing Milkyway library. Use **create_mw_lib**

command to create a Milkyway library if one does not exist. Run the command again.

DCT-023 (Warning) %s in command %s is not supported in topographical mode.
Adding %s to the command.

DESCRIPTION

You receive this message because the command **create_net_shape** does not support snapping on the geometries, it is the same with the situation that "-no_snap" is added to the command.

WHAT NEXT

SEE ALSO

create_net_shape (2)

DCT-024 (Error) should specify ’-net_type’ for invalid physical net %s.

DESCRIPTION

You receive this message because an invalid net name is specified in the command **create_net_shape**, in this case, ’-net_type’ should be specified.

WHAT NEXT

SEE ALSO

create_net_shape (2)

DCT-025 (Error) should avoid option ’-net_type’ for existing physical net %s.

DESCRIPTION

You receive this message because the value of option ’-net_type’ is not consistent

with the type of the existing nets.

WHAT NEXT

Remove the option '-net_type'.

SEE ALSO

create_net_shape (2)

DCT-026 (Information) Turning on congestion optimizations for '%s'.

DESCRIPTION

Design Compiler Topographical has detected that the design was optimized for reduced routing related congestion. The command being executed has the ability to further optimize for reduced routing related congestion and this is being enabled automatically. Congestion optimization and reporting is available with Design Compiler Graphical.

WHAT NEXT

SEE ALSO

DCT-027 (Error) The version of DC-Topographical %s data stored in the design is newer than your executable.

DESCRIPTION

You received this message because the tool version you used to save DC-Topographical data is newer than the tool version you are using to read it. The indicated data will be ignored.

WHAT NEXT

Use the same or newer tool version to read the design.

SEE ALSO

DCT-028 (Information) net shapes on net %s are being ignored and removed.

DESCRIPTION

You receive this message because DC-Topographical has identified that the net shapes associated with the indicated net should not be created during **compile_ultra**. net shape information for a net is maintained if one of the following conditions is met: (1) Net is defines as Power or Ground by **create_net_shape**. (2) The net does not exist in the logical netlist and did not exist when the **create_net_shape** commands was called for it. (3) Net is a "physical only" net.

SEE ALSO

create_net_shape (2) **compile_ultra** (2)

DCT-029 (Warning) Using pdb file(s) for physical library information in DC-Topographical flow is not supported.

DESCRIPTION

You received this message because .pdb format is not supported in DC-Topographical for physical library information. Milkyway format should be used for physical library information.

WHAT NEXT

Setup your flow to use Milkyway library and rerun.

SEE ALSO

create_mw_lib (2) **open_mw_lib** (2)

DCT-030 (Error) Arnoldi-based delay calculation is not

supported in '%s'.

DESCRIPTION

You received this message because your RC delay calculation is set to use post-route Arnoldi model. DC-Topographical does not support Arnoldi-based delay calculation in the given command. Arnoldi-based delay calculation is usually set using the command **set_delay_calculation -arnoldi**.

WHAT NEXT

Modify your script to avoid setting post-route delay calculation mode and rerun.

SEE ALSO

set_delay_calculation (2)

DCT-031 (Error) design %s contains %d net shapes but only %d were restored.

DESCRIPTION

You received this message because DC-Topographical failed to restore some or all of the net shapes associated with the design. This may be due to missing physical information when linking the design. Specifically, this issue is commonly caused by incomplete physical layer information when the design is linked.

WHAT NEXT

Fix your script to correctly setup DC-Topographical physical data and rerun.

SEE ALSO

compile_ultra (2)

DCT-032 (Warning) Preroute extraction is disabled since no Milkyway library is open.

DESCRIPTION

You received this message because **extract_physical_constraints** command requires a

Milkyway library to be open in order to extract pre-route data correctly. Since DC-Topographical could not find any open Milkyway library, extraction of pre-routes is being automatically disabled.

WHAT NEXT

If pre-route extraction is desired, modify your script to setup and open a Milkyway library and rerun.

SEE ALSO

extract_physical_constraints (2) **create_mw_lib** (2) **open_mw_lib** (2)

DCT-033 (warning) Failed to derive preferred routing direction for the design routing layers.

DESCRIPTION

This warning message occurs when Design Compiler topographical fails to automatically derive the preferred routing direction for the design layers. The cause may be that the tool could not find *unitTile* in the Milkyway main and reference libraries, or that *WireDirection* is missing in the *unitTile* library.

WHAT NEXT

Set the preferred routing direction for layers with the **set_preferred_routing_direction** command.

SEE ALSO

set_preferred_routing_direction(2)

DCT-034 (warning) No TLUPlus file identified.

DESCRIPTION

This warning message occurs when Design Compiler topographical is not set up to use TLUPlus files for RC extraction. For better accuracy specify a TLUPlus file using the **set_tlu_plus_files** command.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, set up the flow to use TLUPlus files for RC extraction and run the command again.

SEE ALSO

report_tlu_plus_files(2)
set_tlu_plus_files(2)

DCT-035 (information) No preferred routing direction is found for design layer %s. Automatically deriving direction %s.

DESCRIPTION

This information message occurs when the routing direction is missing for the specified layer. Design Compiler topographical automatically derives a preferred routing direction for the layer.

WHAT NEXT

This is an information only message. No action is required.

SEE ALSO

set_preferred_routing_direction(2)

DCT-036 (warning) Components '%s' associated with the blockage are ignored.

DESCRIPTION

You receive this warning message because components associated with the blockage are ignored in the **extract_physical_constraints** command.

WHAT NEXT

This is only a warning message. No action is required.

SEE ALSO

extract_physical_constraints(2)

DCT-037 (warning) 'POLYGON' blockage is not supported.

DESCRIPTION

You receive this warning message because 'POLYGON' blockage is not supported in the **extract_physical_constraints** command.

WHAT NEXT

This is only a warning message. No action is required.

SEE ALSO

extract_physical_constraints(2)

DCT-041 (information) Core area not specified.

DESCRIPTION

This information message occurs because the core area is not specified for this design. The floorplan information will be automatically generated whe the **compile_ultra** command is run. This may not correlate with the ICC runs.

WHAT NEXT

This is only an information message. No action is required.

However, to set the core area, use the **extract_physical_constraints** command and ensure that the placement area is specified.

SEE ALSO

compile_ultra(2)
extract_physical_constraints(2)
report_physical_constraints(2)

DCT-042 (information) The port %s does not have a user-defined location.

DESCRIPTION

This information message occurs when the port does not have a user-specified location. The port will be assigned a location when the **compile_ultra** command is

run. The information may not correlate with the ICC run.

WHAT NEXT

This is only an information message. No action is required.

However, if you want to set the port location, use either the **set_port_location** or the **extract_physical_constraints** command.

SEE ALSO

compile_ultra(2)
extract_physical_constraints(2)
report_physical_constraints(2)
set_port_location(2)

DCT-043 (information) The %s %s does not have a user-defined location.

DESCRIPTION

This warning message occurs when the macro or pad does not have a user-specified location. The macro will be assigned a location when the **compile_ultra** command is run. The information may not correlate with the ICC run.

WHAT NEXT

This is only a warning message. No action is required.

However, if you want to to set the macro or pad location, use either the **set_cell_location** or the **extract_physical_constraints** command.

SEE ALSO

compile_ultra(2)
extract_physical_constraints(2)
report_physical_constraints(2)
set_cell_location(2)

DCT-044 (information) The cell %s is a black box.

DESCRIPTION

This information message occurs when the tool will generate a physical size for the black box. The information may not correlate with ICC.

WHAT NEXT

This is only an information message. No action is required.

However, you can update the target libraries and physical libraries to include the specified cell.

SEE ALSO

extract_physical_constraints(2)
report_physical_constraints(2)

DCT-046 (information) The ILM %s does not have a user-specified location.

DESCRIPTION

This information message occurs when the ILM does not have a user-specified location. The ILM will be assigned a location when the **compile_ultra** command is run. The information may not correlate with the ICC run.

WHAT NEXT

This is only information message. No action is required.

However, you can avoid this message by placing the ILM.

SEE ALSO

compile_ultra(2)
extract_physical_constraints(2)
report_physical_constraints(2)

DCT-047 (information) The physical block %s does not have a user-specified location.

DESCRIPTION

This information message occurs when because the specified physical block is not placed. The **compile_ultra** command run will place this physical block.

WHAT NEXT

This is only an information message. No action is required.

However, to avoid this message, place the physical block.

SEE ALSO

compile_ultra(2)
extract_physical_constraints(2)
report_physical_constraints(2)

DCT-048 (error) Unable to find location for port %s of ILM or physical block %s.

DESCRIPTION

This error message occurs when the port location cannot be found for the ILM or physical block.

WHAT NEXT

Ensure that all ports for the ILM or physical blocks have legal locations and run the command again.

SEE ALSO

compile_ultra(2)

DCT-049 (error) Unable to find location for cell %s of ILM or physical block %s.

DESCRIPTION

This error message occurs because the locations cannot be found for the specified cells of the ILM or physical block.

WHAT NEXT

Ensure that all cells of the ILM or physical blocks have legal locations and run the command again.

SEE ALSO

compile_ultra(2)

DCT-050 (error) Option %s is no longer supported in the %s command.

DESCRIPTION

This error message occurs because the specified option to the command is obsolete. You can no longer use this option with this command.

WHAT NEXT

Modify your script to use only the current options and rerun the command.

DCT-051 (Information) The port %s has internally generated location.

DESCRIPTION

This information message occurs when the port does not have a user-specified location. The port is assigned a location when the **compile_ultra** command is run. This information may not correlate with the ICC run.

WHAT NEXT

This is only an information message. No action is required.

However, if you want to set the port location use either the **set_port_location** or the **extract_physical_constraints** command.

SEE ALSO

extract_physical_constraints(2)
report_physical_constraints(2)

DCT-052 (warning) Site row ’%s’ exists.

DESCRIPTION

This warning message occurs when a site row with the same name already exists.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, ensure that there are no duplicated names for the site rows and run the command again.

SEE ALSO

create_site_row(2)
extract_physical_constraints(2)

DCT-053 (warning) The bounding box of the site row '%s' to be created is overlapped with the existing site row '%s'.

DESCRIPTION

This warning message occurs when the site row to be created has overlapped with the existing site row.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, make sure that there is no overlap between the bounding box of the site rows and run the command again.

SEE ALSO

create_site_row(2)
extract_physical_constraints(2)

DCT-054 (error) Cannot run compile_ultra incremental in spg mode.
Design was not compiled with DC-Topographical spg optimizations.

DESCRIPTION

This error message occurs because **compile_ultra** incremental in spg mode cannot be used with designs that were compiled in Design Compiler topographical non-spg mode.

WHAT NEXT

Rerun **compile_ultra** in non-incremental spg mode to get the benefits of Design Compiler topographical spg optimization.

SEE ALSO

compile_ultra(2)

DCT-055 (warning) Run compile_ultra incremental in spg mode. Design was compiled with DC-Topographical spg optimizations.

DESCRIPTION

This warning message occurs when the **compile_ultra** command with the **incremental** option will run in spg mode for designs that were compiled in Design Compiler topographical spg mode.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, rerun **compile_ultra** in non-incremental non-spg mode if you do not want **compile_ultra -incremental** to run in spg mode.

SEE ALSO

compile_ultra(2)

DCT-056 (warning) Cannot create wiring keepouts on unroutable layer %s.

DESCRIPTION

This warning message occurs when the tool attempts to create wiring keepouts on unroutable layers.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, make sure that you specify a routable layer and run the command again.

SEE ALSO

create_wiring_keepouts(2)
extract_physical_constraints(2)

DDB

DDB-1 (warning) Cell %s not added to design %s because a cell with that name already exists.

DESCRIPTION

WHAT NEXT

DDB-2 (warning) Net %s not added to design %s because a net with that name already exists.

DESCRIPTION

A net with the specified name already exists.

WHAT NEXT

Reissue the command with a new net name. Use the **report_net** command to find a list of all the nets currently present in the design.

DDB-3 (warning) Consistency problem: port %s is not owned by any design or reference.

DESCRIPTION

The specified port is not owned by any design.

WHAT NEXT

Check the consistency of your design database.

DDB-4 (warning) Consistency problem: a pin is not owned by

any cell.

DESCRIPTION

The specified pin is not owned by any design.

WHAT NEXT

Check the consistency of your design database.

DDB-5 (warning) Consistency problem: cell %s is not owned by any design.

DESCRIPTION

WHAT NEXT

DDB-7 (warning) Consistency problem: net %s is not owned by any design.

DESCRIPTION

WHAT NEXT

DDB-8 (warning) Consistency problem: a pin was found without a corresponding port.

DESCRIPTION

WHAT NEXT

DDB-9 (warning) Consistency problem: cell %s was found

without a corresponding reference.

DESCRIPTION

WHAT NEXT

DDB-10 (warning) Consistency problem detected in design %s %s

DESCRIPTION

WHAT NEXT

DDB-11 (warning) Internal error %s

DESCRIPTION

WHAT NEXT

DDB-12 (warning) Removed duplicate cell '%s'.

DESCRIPTION

WHAT NEXT

DDB-13 (warning) The name of net '%s' in design '%s' can't be changed

to the name of both ports '%s' and '%s' to which it's connected.

DESCRIPTION

WHAT NEXT

DDB-14 (warning) The net '%s' in design '%s' is connected to both
ports '%s' and '%s'.

DESCRIPTION

Two ports can only be connected to a net if they are inout ports or if they drive wired logic. Connecting two input ports to a net can limit the optimization that can be performed by Design Compiler on the net.

WHAT NEXT

Disconnect one of the ports from the net using the **disconnect_net** command.

DDB-21 (error) Conflict between logic 0 and 1. Can't %s.

DESCRIPTION

The two specified ports were set previously as logic 0 and 1. They might not have been directly set, but could have been implicitly set by a sequence of **set_equal** and **set_opposite** commands.

WHAT NEXT

If the ports were directly set as logic 0 and 1, the next steps are as follows:

Use **report_attributes** commands on the two ports. They will have the driven_by_logic_zero and driven_by_logic_one attributes set.

Remove one of these two attributes, one of which is incorrect, using the **remove_attribute** command

Reissue the original command.

If the ports were implicitly set as logic 0 and 1 through a sequesce of **set_equal** and **set_opposite** commands, the next step is as follows:

Use the **reset_design** command to remove the setting of 0 and 1 on the ports. this command removes all other constraints on the design and should be used with caution.

DDB-22 (error) Can't set equal ports opposite in design '%s': '%s' '%s'.

DESCRIPTION

The two ports were set as equal ports previously. They might not have been directly set, but could have been implicitly set by a sequence of **set_equal** and **set_opposite** commands.

WHAT NEXT

The two specified ports were set previously as equal ports. The only way to revert back this setting is to reset the design using the **reset_design** command. This command removes all other constraints on the design and should be used with caution.

DDB-23 (error) Can't set opposite ports equal in design '%s': '%s' '%s'.

DESCRIPTION

The two ports were set as opposite ports previously. They might not have been directly set, but could have been implicitly set by a sequence of **set_equal** and **set_opposite** commands.

WHAT NEXT

The two specified ports were previously set as opposite ports. The only way to revert back this setting is to reset the design using the **reset_design** command. This command removes all other constraints on the design and should be used with caution.

DDB-24 (warning) Overwriting design file '%s/%s'.

DESCRIPTION

Overwriting the specified version of the design with more recent version.

WHAT NEXT

Warning only. No action is required.

DDB-27 (error) ’%s’ value must be positive.

DESCRIPTION

A negative value was entered. Constraint values must be positive (or 0).

WHAT NEXT

Please enter a non-negative value.

DDB-28 (error) ’%s’ cannot be set on %s pin ’%s’.

DESCRIPTION

The specified constraint cannot be set on a pin of the specified direction. The constraint command will be ignored.

WHAT NEXT

Please enter a correct constraint command.

DDB-29 (error) ’%s’ cannot be set on %s port ’%s’.

DESCRIPTION

The specified constraint cannot be set on a port of the specified direction. The constraint command will be ignored.

WHAT NEXT

Please enter a correct constraint command.

DDB-30 (error) Can’t specify output port ’%s’ as a path

startpoint.

DESCRIPTION

Output ports are not valid as path startpoints. There are no timing paths from such ports.

WHAT NEXT

Examine the design to determine the correct startpoint for the path.

DDB-31 (error) Can’t specify input port ’%s’ as a path endpoint.

DESCRIPTION

Input ports are not valid as path endpoints. There are no timing paths to such ports.

WHAT NEXT

Examine the design to determine the correct endpoint for the path.

DDB-32 (error) Can’t specify hierarchical cell ’%s’ as a path ’%s’.

DESCRIPTION

Hierarchical cell names are not valid as path startpoints or endpoints.

WHAT NEXT

Use a clock, port, pin (leaf or hierarchical), or cell (leaf only) as the path startpoint or endpoint.

DDB-33 (error) Pin ’%s’ does not have a library hold time.

DESCRIPTION

None.

WHAT NEXT

Check the target library.

DDB-34 (error) %s '%s' is in design '%s', but %s '%s' is in design '%s'.

DESCRIPTION

None.

WHAT NEXT

None.

DDB-35 (error) '%s' does not exist in library '%s'.

DESCRIPTION

The listed key in the error message does not exist in the library.

WHAT NEXT

Check the key file.

DDB-38 (error) Can't open security file '%s' for protected library '%s'.

DESCRIPTION

Cannot open security file.

WHAT NEXT

Check the security file.

DDB-39 (error) Bad security key in file '%s' for library '%s'.

DESCRIPTION

You are trying to invoked **read_lib** on a protected library.

WHAT NEXT

If a nodelocked library, check and correct these attributes: key_file, key_seed, and key_bit. If a network licensing library, check and correct these attributes: key_feature, key_version, and key_seed. Then reinvode the **read_lib** command.

DDB-40 (error) Can't read protected library '%s'.

DESCRIPTION

You are trying to invoked **read_lib** on a protected library.

WHAT NEXT

If a nodelocked library, check and correct these attributes: key_file, key_seed, and key_bit. If a network licensing library, check and correct these attributes: key_feature, key_version, and key_seed.

DDB-41 (error) Incomplete library protection attributes.

DESCRIPTION

WHAT NEXT

DDB-43 (warning) Could not create attribute ’%s’ for %s objects.

DESCRIPTION

WHAT NEXT

DDB-44 (error) Can’t read unprotected library ’%s’.

DESCRIPTION

WHAT NEXT

DDB-45 (error) A design with name ’%s’ already exists in the same
design file as design ’%s’.

DESCRIPTION

WHAT NEXT

DDB-46 (error) A reference with name ’%s’ already exists in

design ’%s’.

DESCRIPTION

WHAT NEXT

DDB-47 (error) A cell with name ’%s’ already exists in design ’%s’.

DESCRIPTION

WHAT NEXT

DDB-48 (warning) Creating port ’%s’ on design ’%s’ with direction unknown.

DESCRIPTION

WHAT NEXT

DDB-51 (warning) In the value of %s,
the characters separating the "%%s" and "%%d those separating each "%%d

DESCRIPTION

WHAT NEXT

DDB-52 (error) The value of %s

must include one "%%s" and two "%%d

DESCRIPTION

WHAT NEXT

DDB-53 (error) The value of %s must include one "%%s" and one "%%d

DESCRIPTION

The message is printed out when the current command found invalid value in the indicated variable.

WHAT NEXT

Check the value of the given variable and provide the valid value.

DDB-54 (error) The value of %s must include only one "%%s" and only two "%%d

DESCRIPTION

The error message is printed out when the current command found invalid value in the indicated variable.

WHAT NEXT

Provide the valid value for this variable.

DDB-55 (error) The value of %s must include only one "%%s" and only one "%%d

DESCRIPTION

The error message is printed out when the current command found invalid value for the indicated variable name included in the message.

WHAT NEXT

Provide the valid value for this variable.

DDB-56 (error) In the value of %s, there are no characters separating %s.

DESCRIPTION

This error message is printed out when the current command found that there are no character separators.

WHAT NEXT

Provide the valid value for the command.

DDB-57 (error) In the value of %s, the %s of the characters separating %s must not be%s a digit.

DESCRIPTION

This error message is printed out when the current command found digit in the character separators.

WHAT NEXT

Provide the valid value for the command.

DDB-58 (warning) In the value of %s, there are no characters separating the "%%s" and "%%d be ambiguous).

DESCRIPTION

If no characters separate the array name from the member number, the bus names will be ambiguous for arrays whose names end in a digit. For example, with **bus_naming_style** set to "%s%d", the name of the third member of array "A1" and the thirteenth element of array "A" would both have the name "A13".

WHAT NEXT

Most likely you should change the value of the bus naming style to contain some characters between the "%s" and "%d". See the help page for **bus_naming_style** for details.

DDB-60 (error) Could not find library pin for pin '%s'.

DESCRIPTION

The back-annotation failed because the pin does not have a corresponding pin in the link library.

WHAT NEXT

Verify that the design is fully linked with the 'link' command. Verify that all link and target library search paths are valid.

DDB-66 (warning) Removing group '%s'.

DESCRIPTION

The path group is being removed because the operation being performed has removed the last path from the group.

WHAT NEXT

Be aware that any subsequent attempts to use this path group will fail because the group has been deleted. If you think the group should not have been deleted, identify at least one path you think should still be in the group and trace back to find which action deleted that path.

DDB-67 (warning) Removing %s from group '%s'.

DESCRIPTION

WHAT NEXT

DDB-68 (warning) Removing external delay related to clock %s.

DESCRIPTION

When a clock source is deleted from the design using the 'remove_clock' command, all input and output delay values that were specified relative to that clock are also deleted from the design. For example, consider the following script:

```
create_clock -name CLK -period 10 set_input_delay 2 -clock CLK all_inputs()
set_output_delay 2 -clock CLK all_outputs()

remove_clock CLK
```

The 'remove_clock' command will also have the effect of removing the input and output delay values that were specified relative to CLK.

WHAT NEXT

No action is required, this is merely an informational warning.

DDB-70 (error) None of the selected cells were grouped.

DESCRIPTION

When using the 'group' command on an hdl design that has not been compiled yet, it is possible that the cells you specified to be grouped cannot be grouped because they need to stay with thier neighboors until the design has gone through resource sharing in compile.

WHAT NEXT

Use the 'group' command after the design has been compiled.

DDB-71 (error) Design '%s' requires one of the following

licenses: '%s'.

DESCRIPTION

The specified design is licensed and requires one of the listed licenses to be available. An error has occurred because none of the licenses could be obtained.

WHAT NEXT

Verify that your site has at least one of the specified licenses. If it does not, then one must be purchased. If your site does have one of the licenses, try again when the license is available.

DDB-72 (information) Added key list '%s' to design '%s'.

DESCRIPTION

Indicates that the listed set of licenses have been associated with the specified design. Accessing the design will require that one of the listed licenses can be successfully checked out.

WHAT NEXT

No action is required since this is just an information message.

DDB-73 (warning) License '%s' contains the illegal character '%c'.
It was ignored.

DESCRIPTION

One of the licenses associated with a design contains an invalid character. That license will be dropped from the list of licenses which can be used to access the design.

WHAT NEXT

If a design is associated with multiple licenses, it may be possible to access the design via a different, valid license. In any case the license name should be updated so that it does not contain any invalid characters. Invalid characters include: ',', '}', '{', '*', ''.

DDB-74 (warning) Design '%s' inherited license information from design '%s'.

DESCRIPTION

All of the licenses associated with one design have now been associated with another design. This typically happens when a design is ungrouped. In that situation, the parent design will inherit all licensing information from the ungrouped design.

WHAT NEXT

Although this is classified as a warning, it is essentially just an information message. No action is required.

DDB-75 (warning) Design '%s' is being converted to a limited design.

DESCRIPTION

This message indicates that the indicated design has been converted into a limited design. A limited design is a design which can be compiled and analyzed, but whose contents may not be examined or written out.

A design gets converted into a limited design in two situations. In the first case you have only an evaluation license for the design (obtained by manually setting synlib_disable_limited_licenses = "FALSE"), and the design will remain limited because the intent of an evaluation license is for the design data to be restricted. In the second case the design was derived from a DesignWare part and has not yet been run through the **compile** command. In this latter case the design remains limited only until after it has been compiled, at which point the limitation is removed. The intent of this latter limitation is to protect the technology- independent structure of the design.

WHAT NEXT

If you have only an evaluation license for the limited design, then the only way to gain access to the internals of that design is through the use of a full license for that part; if a full license is subsequently obtained then the first **compile** command will remove the 'limited design' restrictions. If the design has already been compiled, it is sufficient to run the **get_license** command to convert the limited design back to a regular, unrestricted format.

If you already have a full license for the limited design, then after the first **compile** command you can expect the design to be converted back to a regular, unrestricted format.

DDB-76 (error) Cannot load design '%s'.

DESCRIPTION

The named design cannot be loaded into Design Compiler's internal data structures. This can happen if certain synthetic parts cannot be found.

WHAT NEXT

Attempt to link the design with the command *link -all*. If this fails, check that the software is correctly installed.

DDB-77 (error) License '%s' is a Synopsys internal key and should not have a seed associated with it.

DESCRIPTION

When license names are set on a design, third party keys must have a seed associated with them. It is an error, however, for Synopsys internal keys to have seeds.

WHAT NEXT

When creating your own license names, make sure that they do not clash with the Synopsys internal license names.

DDB-78 (error) No seed provided for the third-party license '%s'.

DESCRIPTION

When adding a third-party license, you must specify both a license name and a non-zero seed. This prevents third party vendors from creating keys for each other's licenses.

WHAT NEXT

Specify the license name as *name/seed*. For example: "MY_LIC/1234"

DDB-79 (error) The license '%s' has an invalid seed associated

with it.

DESCRIPTION

This error occurs when the *set_design_license command* is used to store a third party license and a seed, and the seed that is specified is not consistent with the seed that was used to create the key.

WHAT NEXT

Either generate a new key with the correct seed, or change the *set_design_license* command line so that the seeds are consistent.

DDB-80 (error) The seed '%s' specified for license '%s' is not a valid 32-bit integer.

DESCRIPTION

Licenses can be specified in the from '<license>/<seed>' where <seed> is supposed to be a valid integer which can be represented in 32 bits. In this case the <seed> specified was either not an integer, or was too large to be represented in 32 bits.

WHAT NEXT

The <seed> associated with the license needs to be corrected such that it is a valid integer which can be stored in at most 32 bits.

DDB-81 (warning) Unable to find specified driving_cell for port '%s'.

DESCRIPTION

The driving_cell attributes indicate that a port should inherit its drive capability from a certain library cell. This error means that the tool was unable to locate a matching library cell or pin on that library cell. This may happen if the link_library does not contain the library for that cell, or if the cell name or pin name was incorrect. The driving cell information can be seen using **report_port -drive**. It may have been set by either **set_driving_cell** or **characterize**.

WHAT NEXT

If the driving cell requires a library that has not been identified in the

link_library, the **link_library** should be changed to include that library. Otherwise, check the information for errors in cell_name, library name, or pin names using **report_port -drive -only *port_name***.

DDB-84 (error) Only ports of the same direction can be grouped.

DESCRIPTION

WHAT NEXT

DDB-85 (error) Objects must be either all ports or all nets.

DESCRIPTION

This error message is issued if a mixture of objects of different types is given as input to a command that requires a homogenous set of ports or nets as input.

WHAT NEXT

Re-issue the command specifying only ports or only nets as input.

DDB-86 (error) Bus name '%s' conflicts with existing names.

DESCRIPTION

This error message is issued when an attempt is made to create a bus with a name that conflicts with the name of an existing bus.

WHAT NEXT

Re-issue the command with a non-conflicting name for the bus.

DDB-87 (error) All objects must be from the same design.

DESCRIPTION

This error message is issued if a command that requires a set of objects belonging to the same design is invoked with objects that belong to different designs.

WHAT NEXT

Re-issue the command with a set of objects that belong to the same design.

DDB-88 (error) At least one of the port objects specified is already a member of a bus.

DESCRIPTION

This error message is displayed if an attempt is made to insert a port that belongs to a bus into a new bus.

WHAT NEXT

Re-issue the command with ports that do not belong to an existing bus.

DDB-89 (error) Type name '%s' conflicts with existing type.

DESCRIPTION

This error message is issued if an attempt to create a type for a new bus object is made with a type name that is already used for another bus object with a different width.

WHAT NEXT

Change the name of the new bus type.

DDB-90 (error) specified range is different from number of objects to be bussed.

DESCRIPTION

WHAT NEXT

DDB-91 (error) only designs or references can have busses

created in them.

DESCRIPTION

WHAT NEXT

DDB-92 (error) Cannot load design '%s' for an HDL embedded command.

DESCRIPTION

The named design cannot be loaded for the current command embedded in an HDL file. The current embedded command is not legal within an embedded script. See the HDL Compiler Manual for details.

WHAT NEXT

Change the embedded script so that it does not use the offending command.

DDB-95 (warning) Unable to find net instance '%s' in design '%s'.

DESCRIPTION

Back-annotation, such as a set_load or set_resistance value, was stored on a net instance within the design, but that instance can no longer be found. This can occur if a lower-level design containing the net instance was modified but the top-level design was unaware of this change. Commands which could modify lower level designs include **ungroup**, **change_names**, and **compile**.

WHAT NEXT

Perform **ungroup** and **change_names** at the top level so that the top level design will have a chance to update its back-annotation records. Use **characterize** to move annotation to a subdesign before running **compile** or **reoptimize_design** on that subdesign.

DDB-100 (warning) Unable to find minimum version of library

cell '%s/%s' in library '%s'.

DESCRIPTION

The **set_min_library** command has been used to indicate that timing data for minimum analysis must use a particular library, but this library cell cannot be found in that minimum library. Design Compiler will use the maximum version of the cell for both maximum and minimum analysis in this case.

WHAT NEXT

Check that the **set_min_library** command specified the correct library for minimum analysis. See if the indicated library cell was accidentally left out of the minimum analysis library.

DDB-101 (warning) Unable to find minimum version of library pin '%s/%s' in library '%s'.

DESCRIPTION

The **set_min_library** command has been used to indicate that timing data for minimum analysis must use a particular library, but the indicated library cell has conflicting pin descriptions between the maximum and minimum libraries. In this case, a pin exists on the library cell in the maximum library, but that pin does not exist in the minimum library. Design Compiler will use the maximum version of the library pin for both maximum and minimum analysis in this case.

WHAT NEXT

Check that the **set_min_library** command specified the correct library for minimum analysis. See if the indicated library pin was accidentally left out of the minimum analysis library.

DDB-102 (warning) Conflicting timing arc descriptions between maximum library '%s' and minimum library '%s' to pin '%s/%s'.

DESCRIPTION

The **set_min_library** command has been used to indicate that timing data for minimum analysis must use a particular library, but the indicated library cell has conflicting timing arc descriptions between the maximum and minimum libraries. In this case, a timing arc exists on the library cell in the maximum library, but a corresponding timing arc does not exist in the minimum library. Design Compiler will

use the maximum version of the timing arc for both maximum and minimum analysis in this case.

In order to consider timing arcs as compatible between minimum and maximum libraries, they must have the same sense (for example, positive unate, or clear), they must have the same SDF condition, and there must be the same number of arcs of each type between a pair of pins.

WHAT NEXT

Check that the **set_min_library** command specified the correct library for minimum analysis. See if timing arcs to the indicated library pin were accidentally left out of the minimum analysis library.

DDB-103 (warning) Pin %s of lib cell %s exists in maximum library %s but not in minimum library %s. Assuming min delay for pin to be same as max delay.

DESCRIPTION

The **set_min_library** command has been used to indicate that timing data for minimum analysis must use a particular library, but the indicated library cell has some pins in the max library which don’t exist in the minimum libraries. Design Compiler will use the maximum version of the timing arc for both maximum and minimum analysis in this case.

In order to be compatible between minimum and maximum libraries, the library cells must have the same pins and same timing arcs (same sense (for example, positive unate, or clear), they must have the same SDF condition), and there must be the same number of arcs of each type between a pair of pins.

WHAT NEXT

Check that the **set_min_library** command specified the correct library for minimum analysis. See if the specified pins of the specified library cell were accidentally left out of the minimum analysis library.

DDB-105 (warning) Design ’%s’ requires one of the following licenses: ’%s’.
Waiting for license to become available, press <ctrl>-C to

terminate.

DESCRIPTION

The specified design is licensed and requires one of the listed licenses to be available. None of the licenses could be obtained. Design Compiler will wait for one of the licenses to become available and then continue.

WHAT NEXT

Verify that your site has at least one of the specified licenses. If it does not, then one must be purchased. If you wish to terminate the command instead of waiting for the license to become available, set synlib_wait_for_design_license = {}

DDB-107 (warning) Deleted or recreated %d internal pin(s) on cell '%s'. All attributes and attaches on it(them) are lost.

DESCRIPTION

The **access_internal_pins** variable controls creation and deletion of internal pins and user access to them. Because of the source of internal pins, they are created or deleted during link time, depending on the setting of this variable. You can use the **find** and **get_pins** commands to show internal pins, if such pins exist. Certain timing commands can also set constraints on internal pins.

WHAT NEXT

If this is what you intended to do, no action is necessary.

SEE ALSO

find (2), **get_pins** (2), **link** (2); **access_internal_pins** (3).

DDC-1 (error) Unable to open DDC file '%s' for writing.

DESCRIPTION

dc_shell encountered an I/O error when it attempted to open the specified DDC file for writing.

WHAT NEXT

Check that the file name is correct, that the directory exists and is writable, and that the filesystem is not full. If the target file already exists it must be writable in order for dc_shell to overwrite it.

DDC-2 (error) Unable to open file '%s' for reading.

DESCRIPTION

The tool encountered an error when it attempted to open the specified DDC file for reading.

WHAT NEXT

Check that the path to the file is correct and that the file is readable by the current user. Also verify that the file was written in DDC format.

SEE ALSO

write_file(2)

DDC-3 (error) DDC internal write error in design '%s'.

DESCRIPTION

dc_shell encountered an internal error while attempting to write the specified design. No DDC file was produced.

WHAT NEXT

Please contact the Synopsys Support Center for assistance.

DDC-4 (error) DDC internal read error in file '%s'.

DESCRIPTION

dc_shell encountered an internal error while attempting to read the specified file. No designs were read.

WHAT NEXT

Please contact the Synopsys Support Center for assistance.

DDC-5 (error) Design data is corrupt in DDC file.

DESCRIPTION

The file being read has been modified or corrupted since it was originally written by **dc_shell**.

WHAT NEXT

The DDC file must be re-created from the original design source. Note that DDC files cannot be edited by the user.

DDC-6 (error) DDC file version is not compatible. The DDC file was written with dc_shell version %s dated %s.

DESCRIPTION

The file being read is an incompatible version of DDC that cannot be read with this release of **dc_shell**.

WHAT NEXT

If the DDC file was written with an older release of **dc_shell**, you can run that version of **dc_shell** to read the file and write it out in DB format. The current version of **dc_shell** should be able to read the DB file and convert it to the current DDC format.

If a newer release of **dc_shell** was used to write the DDC file, you must use that version to read it back in.

DDC-7 (error) File is not in DDC format.

DESCRIPTION

dc_shell has determined that the file being read is not a DDC format file.

WHAT NEXT

Verify that the correct format option has been provided to the read_file command, and that the file path is correct.

DDC-8 (error) Attempt to write duplicate design name '%s' to DDC file.

DESCRIPTION

dc_shell detected an attempt to write multiple designs with the same name to a DDC file, which is not allowed by the DDC format.

WHAT NEXT

Check the list of designs provided to the write command. It is possible, although unusual, for duplicate design names to have been read from different files, such as multiple .db files. If the duplicate design names must be preserved, they must be written to separate DDC files.

DDC-9 (warning) The DDC format cannot be used to store physical data. Any physical information that is present will not be written to the DDC file.

DESCRIPTION

You receive this warning message when you write out a DDC file that contains physical data. The DDC file format is not capable of representing physical data. Only the logical representation will be written to the DDC file.

WHAT NEXT

It is considered best practice to use the Milkyway storage format for designs that contain physical information. You can use the **write_milkyway** command to write the design to a Milkyway database.

SEE ALSO

write_milkyway(2)

DDC-10 (error) Scenario '%s' does not exist.

DESCRIPTION

The specified scenario, which was provided with the -scenarios option to the **write** command, does not exist.

WHAT NEXT

Check that the scenario name is correct, and that any scenarios which are to be written to the DDC file have been created.

SEE ALSO

write(2)
create_scenario(2)

DDC-11 (error) DDC file contains packed command syntax that cannot be processed by this version of dc_shell. Please use a current version of dc_shell to read this file.

DESCRIPTION

The current DDC file contains embedded commands (constraints) which were written by a newer version of **dc_shell** and utilize a syntax which cannot be parsed by the current executable.

WHAT NEXT

Use the same (or newer) version of **dc_shell** to read the file as was used to write it.

SEE ALSO

ddc_allow_unknown_packed_commands(3)
read_file(2)

DDC-12 (warning) DDC file was written with a newer version of dc_shell.
Some embedded commands may be ignored.

DESCRIPTION

You are trying to read a DDC file which was written by a newer version of **dc_shell**, and the DDC file contains some packed commands (constraints) which are not recognized by the older version of **dc_shell**. Normally this would result in a DDC-6 error; however, if the variable ddc_allow_unknown_packed_commands is set to "true" then **dc_shell** will attempt to read the file, but any unrecognized packed commands will be ignored. (A DDC-13 warning message will be printed when each such command is first encountered.)

WHAT NEXT

To avoid losing potentially important information, always read the DDC file with the same (or newer) version of **dc_shell** as was used to write it.

SEE ALSO

DDC-13(n)
ddc_allow_unknown_packed_commands(3)
read_file(2)

DDC-13 (warning) Ignoring unknown packed command #%d: %s

DESCRIPTION

dc_shell attempted to unpack an embedded command which it does not recognize. This can happen when a DDC (or Milkyway) file which was written with a newer version of **dc_shell** is read with an older version of the product, while the variable ddc_allow_unknown_packed_commands is set to "true". The unrecognized command is simply discarded.

WHAT NEXT

To avoid losing potentially important information, always read the DDC file with the same (or newer) version of **dc_shell** as was used to write it.

SEE ALSO

ddc_allow_unknown_packed_commands(3)

DDC-14 (information) This file contains data for the following %d scenarios:
%s

DESCRIPTION

The DDC or Milkyway reader prints this message if the file being read contains any scenario-specific constraint data. The message will report the name of each scenario for which the file contains data. If the scenario was inactive when the file was written, an asterisk (*) appears after the scenario name.

WHAT NEXT

This is an informational message. No action is required.

SEE ALSO

read_file(2)
read_milkyway(2)
create_scenario(2)
current_scenario(2)
all_scenarios(2)
all_active_scenarios(2)

DDC-15 (warning) Ignoring %s attribute %s on %s object(s): Attribute type conflicts with existing attributes.

DESCRIPTION

An attribute contained in the DDC file conflicts in type with with an attribute that is already registered with the tool. The conflicting attribute is ignored by the DDC reader.

An attribute saved in a DDC file must have the same type as an existing attribute of the same name on the same netlist object class (e.g., string attribute on design objects).

This message is most likely seen when reading in DDC files written by the X-2005.09 release or earlier. Attribute conflicts from more-recent files are silently discarded.

WHAT NEXT

This message could appear if there happens to be a user-defined attribute that has the same name (but different type) as a built-in attribute that was added in a later

version of the tool. It is good practice to use a prefix for user-defined attributes, such as your company's name, that is unlikely to be used by Synopsys in the future.

SEE ALSO

set_attribute(2)
report_attribute(2)

DDC-16 (error) ddc file contains no scenario-specific data. Cannot specify -scenarios option for this file.

DESCRIPTION

The *-scenarios* option to the **read_file** command can only be used to read files that contain scenario-specific constraint data.

WHAT NEXT

See **read_file**(2) for more information on controlling which scenarios' constraints are read from the ddc file.

SEE ALSO

read_file(2)
read_ddc(2)

DDC-17 (error) ddc file contains no data for any of the requested scenarios

DESCRIPTION

The specified ddc file does not contain any constraint data for any of the scenarios specified to the *-scenarios* option to the **read_file** command.

WHAT NEXT

Check the list of scenario names supplied to the **read_file** *-scenarios* option. See **read_file**(2) for more information on controlling which scenarios' constraints are read from the ddc file.

SEE ALSO

read_file(2)
read_ddc(2)

DDC-18 (error) DDC file contains no data for any of the requested active scenarios

DESCRIPTION

The specified ddc file does not contain any constraint data for any of the scenarios specified to the *-active_scenarios* option to the **read_file** command.

WHAT NEXT

Check the list of scenario names supplied to the **read_file** *-active_scenarios* option. See **read_file**(2) for more information on controlling which scenarios' constraints are read from the ddc file.

SEE ALSO

read_file(2)
read_ddc(2)

DDC-19 (warning) ddc file contains no data for the following requested scenarios:
%s

DESCRIPTION

The specified ddc file does not contain any constraint data for one or more of the scenarios specified to the *-scenarios* option to the **read_file** command. The file will be read and the list of scenarios to be read in will be restricted according to the remaining scenarios specified to the *-scenarios* option.

WHAT NEXT

Check the list of scenario names supplied to the **read_file** *-scenarios* option. See **read_file**(2) for more information on controlling which scenarios' constraints are read from the ddc file.

SEE ALSO

`read_file(2)`
`read_ddc(2)`

DDP

DDP-1 (error) Bad status %x from ’%s’

DESCRIPTION

WHAT NEXT

DDP-2 (error) Can’t open map file ’%s’

DESCRIPTION

WHAT NEXT

DDP-3 (warning) Duplicated symbol ’%s’ specified

DESCRIPTION

WHAT NEXT

DDP-4 (error) The map file ’%s’ is corrupted at line ’%s’

DESCRIPTION

WHAT NEXT

DDP-5 (warning) No symbol to be created

DESCRIPTION

WHAT NEXT

DDP-6 (error) Unable to Write library ’%s’

DESCRIPTION

WHAT NEXT

DDP-7 (error) Can’t open file ’%s’

DESCRIPTION

WHAT NEXT

DDP-8 (information) Scan symbol ’%s’

DESCRIPTION

WHAT NEXT

DDP-9 (error) Can’t open symbol ’%s’ under component ’%s’ for

symbol ’%s’

DESCRIPTION

WHAT NEXT

DDP-10 (error) Unable to scan symbol ’%s’

DESCRIPTION

WHAT NEXT

DDP-11 (warning) Find netcon ’%s’ different from ’%s’

DESCRIPTION

WHAT NEXT

DDP-12 (error) More than one bus end on ripper ’%s’

DESCRIPTION

WHAT NEXT

DDP-13 (error) Can’t find bus end for ripper ’%s’

DESCRIPTION

WHAT NEXT

DDP-14 (warning) Different user units exist in the symbols

DESCRIPTION

WHAT NEXT

DDP-15 (error) Error in writing symbol ’%s’

DESCRIPTION

WHAT NEXT

DDP-16 (warning) ’%s’ does not exist for %s

DESCRIPTION

WHAT NEXT

DDP-17 (error) Unable to traverse design ’%s’

DESCRIPTION

WHAT NEXT

DDP-18 (error) Unable to translate symbol ’%s’

DESCRIPTION

WHAT NEXT

DDP-19 (error) Error in adding instance symbols for design ’%s’

DESCRIPTION

WHAT NEXT

DDP-20 (error) Error in translating schematic of ’%s’

DESCRIPTION

WHAT NEXT

DDP-21 (error) Can’t load design ’%s’

DESCRIPTION

WHAT NEXT

DDP-22 (error) Unrecognized unit ’%s’

DESCRIPTION

WHAT NEXT

DDP-23 (information) Create schematic of ’%s’

DESCRIPTION

WHAT NEXT

DDP-24 (warning) Sheet ’%s’ of design ’%s’ does not pass

check

DESCRIPTION

WHAT NEXT

DDP-25 (warning) Close sheet ’%s’ of design ’%s’ failed

DESCRIPTION

WHAT NEXT

DDP-26 (error) Can’t open ’%s’ of schematic ’%s’ under

component ’%s’

DESCRIPTION

WHAT NEXT

DDP-27 (error) Can’t instantiate symbol ’%s’ of component ’%s’

DESCRIPTION

WHAT NEXT

DDP-28 (error) Can’t find symbol ’%s’

DESCRIPTION

WHAT NEXT

DDP-29 (error) Global net ’%s’ is not recognized

DESCRIPTION

WHAT NEXT

DDP-30 (information) Symbol ’%s’ of type ’%s’ is ignored

DESCRIPTION

WHAT NEXT

DDP-31 (information) Create symbol of ’%s’

DESCRIPTION

WHAT NEXT

DDP-32 (error) Can’t create symbol ’%s’ under component ’%s’

DESCRIPTION

WHAT NEXT

DDP-33 (error) Ripper symbol ’%s’ does not have a ’bundle’ pin

DESCRIPTION

WHAT NEXT

DDP-34 (error) Can’t find pin name

DESCRIPTION

WHAT NEXT

DDP-35 (warning) Symbol’%s’ does not pass check

DESCRIPTION

WHAT NEXT

DDP-36 (warning) Close symbol of ’%s’ failed

DESCRIPTION

WHAT NEXT

DDP-37 (warning) Can’t find instance ’%s’

DESCRIPTION

WHAT NEXT

DDP-38 (warning) Can’t find pin ’%s’ of instance ’%s’

DESCRIPTION

WHAT NEXT

DDP-39 (warning) Can’t find symbol for library cell ’%s’

DESCRIPTION

WHAT NEXT

DDP-40 (warning) Symbol library ’%s’ has symbols with off-grid pins. Recreate
library with a v2.2b or later version of dc_shell or design

analyzer.

DESCRIPTION

WHAT NEXT

DDP-41 (error) %s have different route grids

DESCRIPTION

WHAT NEXT

DDP-42 (warning) Designs without schematics: %s

%s

DESCRIPTION

WHAT NEXT

DDP-43 (error) Can’t read the file ’%s’

DESCRIPTION

WHAT NEXT

DDP-44 (error) ’%s’ is not a %s library file

DESCRIPTION

WHAT NEXT

DDP-45 (error) Error in translating symbols from library ’%s’

DESCRIPTION

WHAT NEXT

DDP-46 (warning) Can’t add property ’%s’

DESCRIPTION

WHAT NEXT

DDP-47 (error) Can’t find design ’%s’ in file ’%s’

DESCRIPTION

WHAT NEXT

DDP-48 (error) Can’t find symbol for instance ’%s’ of design ’%s’

DESCRIPTION

WHAT NEXT

DDP-49 (information) The content of the additional sheet ’%s’ in design ’%s’ is removed

DESCRIPTION

WHAT NEXT

DDX

DDX-1 (error) In design ’%s’, connection to %s is too wide.

DESCRIPTION

WHAT NEXT

DDX-2 (error) In design ’%s’, connection to %s is too narrow.

DESCRIPTION

WHAT NEXT

DDX-3 (warning) In design ’%s’, port ’%s’ is not an array. "multiple_port" attribute ignored.

DESCRIPTION

WHAT NEXT

DEFIN-1 (error) Failed to read file '%s'.

DESCRIPTION

The file might not exist in your path.

WHAT NEXT

Check if the file exist or rerun the program.

DEFIN-2 (warning) Ignore '%s' at line %d.

DESCRIPTION

The DEF syntax has been ignored. The reader will not store any information for this line, but continue to read the rest of the file.

WHAT NEXT

Check if this line can be ignored. If not, edit the PDEF output file according to the IEEE PDEF syntax.

DEFIN-3 (warning) Extract the pin location from this section, assuming pin name is matching netlist port name.

DESCRIPTION

The reader does not read logical netlist information therefore, it assumes all the pins in this section will match with the ports in the logical netlist.

WHAT NEXT

Examine the output PDEF and check with the logical netlist to make sure the pin is not in logical netlist.

DEFIN-4 (warning) Probably the DIEAREA statement has

unexpected syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax is the following: DIEAREA <pt pt> ; <pt pt> is the corner points of the bounding rectangle for the design. For example: The following design uses a rectangle with lower left corner (100 100) and upper right corrner (900 900). DIEAREA 100 100 900 900

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFIN-5 (warning) Probably inside the COMPONENTS section, the plus statement is incorrect.

DESCRIPTION

This happens when unexpect syntax has been parsed. The important plus statments inside the COMPONENTS section are the following : [+ {FIXED | COVER | PLACED | UNPLACED } <pt> <orient>] where <pt> is the location for the component <orient> is the orientation for the component

For example: + FIXED (199 199) N

[+ REGION { <pt> <pt> | <regionName> }] where the first <pt> is the lower left corner of the region. the second <pt> is the upper right corner of the region. <regionName> is the name defined in the REGIONS section.

For example: + REGION (10 10) (500 500) or + REGION region1

If other plus statments than above has syntax error then you can ignore. But if they are one of above statments, you need to follow the 5.1 DEF manual, corect them.

Please refer to the 5.1 DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFIN-6 (error) Failed to read file '%s' because of missing PINS

section.

DESCRIPTION

The program only takes the DEF with the pins section.

WHAT NEXT

add the pins section in your DEF.

DEFIN-7 (error) Require to read pdb which contains macro class definition to tell which components are PAD, so the program can take that as port location.

DESCRIPTION

The version of this DEF file is 4.x, it requires PINS section and library in pdbformat which contains io/dummy macro definition.

WHAT NEXT

Generate pdb using library compiler.

DEFIN-8 (warning) Can not find macro type for this component '%s'.

DESCRIPTION

This information is needed to tell which component is an IO.

WHAT NEXT

make sure pdb include every component used in DEF.

DEFIN-9 (error) Only support 5.1 version. Ignore the Site

statement at line %d.

DESCRIPTION

The Site statments indicate there this DEF may not use 5.1 version syntax. Please regenerate your DEF in 5.1 version using your floorplan tool. The correct syntax to define the site array information to the tool is the following DEF 5.1 syntax :

The correct syntax to define the site array information to the tool is the following DEF syntax :

ROW <row_name> <site_name> <X> <Y> <orientation> { DO <N> BY 1 STEP <spaceX> 0 | DO 1 by <N> STEP 0 <spaceY> };

where <row_name> is a unique string identifying this particular row. <site_name> is a site used for the row. The site is defined in the LEF. <X> <Y> is the coordinates of the row's starting point <orientation> Orientation of all sites in the row. { DO <N> BY 1 STEP <spaceX>0 | DO 1 by <N> STEP 0 <spaceY> } Horizontal or vertical step pattern to create the row.

For Example : The row_1 is using site CORE starting -10000 -10000. There are 222 sites in this row and the space between lower left corner of a site to the next lower left corner is 84. ROW row_1 CORE -10000 -10000 N DO 222 BY 1 STEP 84 0 ;

WHAT NEXT

Use the floorplan tool to regenerate the DEF file.

DEFIN-10 (error) The program requires reading pdb.

DESCRIPTION

This pdb is a library pdb which contains library technology information. The reader needs to read library pdb to find out which site in DEF belongs to the CORE, and layer and via definitions.

WHAT NEXT

The library pdb can be generate using library compiler.

DEFIN-11 (warning) Pin '%s' does not have location.

DESCRIPTION

The pin locations are part of floorplan information. Lossing pin locations will have

incomplete floorplan information.

WHAT NEXT

Add pin location for it to make floorplan contraints complete.

DEFIN-12 (warning) Only extract the first rectangle as boundary at line '%d'.

DESCRIPTION

Currently multiple rectangles are not supported for move bounds. This message issued when reader tries to extract region contraints. Only the first rectangle will be use.

WHAT NEXT

If there are multiple rectangles then merge the multiple rectangles into one rectangle.

DEFIN-13 (warning) Only support regions in GROUPS at line '%d'.

DESCRIPTION

Currently we do not extract perimeter attributes from GROUPS. Only REGIONS information will be extracted. Ignore all other soft fence attribute.

WHAT NEXT

If soft fence attribute is needed then translate them into REGIONS.

DEFIN-14 (warning) Only support regular expressions '*','%','-' in GROUPS

DESCRIPTION

The '*' means any sequence of characters. The '%' means any single character. The '-' means any sequence of characters up to the next period '.'. Currently the reader

only can understand the regular expression described using the characters from above.

WHAT NEXT

Expand the unsupprted regular expression.

DEFIN-15 (error) This layer %s is not defined in the library. The PDEF file will be incorrect.

DESCRIPTION

This layer is missing in the physcial library.

WHAT NEXT

Add the layer to your physcial library (a plib file) and use read_lib and write_lib to write out the library.

DEFIN-16 (warning) Detect %s near token '%s' at line %d. Continue to parse until the next correct rule can be applied.

DESCRIPTION

This happens when unexpect syntax has been parsed. It contines to read the file until the next syntax can be applied in the grammar rules.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFIN-17 (warning) Probably the UNITS statement has incorrect syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax is the following: UNITS DISTANCE MICRONS <DEFconvertFactor> For example: UNITS DISTANCE MICRONS 1000 ;

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFIN-18 (warning) Probably the ROW statement has incorrect syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax to define the site array information to the tool is the following DEF syntax :

ROW <row_name> <site_name> <X> <Y> <orientation> { DO <N> BY 1 STEP <spaceX> 0 | DO 1 by <N> STEP 0 <spaceY> };

where <row_name> is a unique string identifying this particular row. <site_name> is a site used for the row. The site is defined in the LEF. <X> <Y> is the coordinates of the row's starting point <orientation> Orientation of all sites in the row. { DO <N> BY 1 STEP <spaceX>0 | DO 1 by <N> STEP 0 <spaceY> } Horizontal or vertical step pattern to create the row.

For Example : The row_1 is using site CORE starting -10000 -10000. There are 222 sites in this row and the space between lower left corner of a site to the next lower left corner is 84. ROW row_1 CORE -10000 -10000 N DO 222 BY 1 STEP 84 0 ;

WHAT NEXT

Edit the DEF file to change the ROW statement or use the floorplan tool to regenerate the DEF file.

DEFIN-19 (warning) Probably inside the SPECIALNETS section, the plus statement is incorrect.

DESCRIPTION

This happens when unexpect syntax has been parsed. The important plus statments inside the SPECIALNETS section are the following : [+ WIDTH <layername> <width>] where <layername> is the layer defined in LEF. <width> is the width used in for this specail route. For example: + WIDTH layer1 0.9

[+ SPACING <layername> <spacing> [RANGE <minwidth> <maxwidth>]] where <layername> is the lyser defined in LEF <spacing> is the spacing used for this special route. <minwidth> <maxwidth> defines the range of the wire width

For example: + SPACING layer1 .05 RANGE 0.01 0.08

If other plus statments than above has syntax error then you can ignore. But if they are one of above statments, you need to follow the 5.1 DEF manual, corect them. Please refer to the 5.1 DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFIN-20 (warning) Probably the special wiring continue point has incorrect syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. They are have to be one of the following forms: 1. (X *) means the Y is from the previous point. 2. (* Y) means the X is from the previous point. 3. <viaName> means the use this via to connect the wire. The via location is decirbed previously. For example : use the previus Y and 1000 connect to via 1 with location = 1000 1000 (1000 *) (* 1000) via1 You need to follow the 5.1 DEF manual, corect them. Please refer to the 5.1 DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFIN-21 (warning) Probably the special wiring section has incorrect syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax is the following:

{ROUTED| FIXED | COVER} <layername> <width> [+ SHAPE {RING|STRIPE}] (x y) [(x *) | (* y) | <viaName>] ... where: <layername> is a layer name defined in LEF. <width> is the wire width.

For example : a wire on layer1 with width .01 from (200 200) to connect to (1000 200)connect to via 1 with location = 1000 1000

ROUTED layer1 .01 +SHAPE STRIPE (200 200) (1000 *) (* 1000) via1

You need to follow the 5.1 DEF manual, corect them. Please refer to the 5.1 DEF manual for the detailed explanation.

Please refer to the 5.1 DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFIN-22 (warning) Probably the new special wiring statment has incorrect syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax is the following:

[NEW <layername> <width> [+ SHAPE {RING|STRING}] (x y) [(x *) | (* y) | <viaName>] ...

where: <layername> is a layer name defined in LEF. <width> is the wire width.

For example : a wire on layer1 with width .01 from (200 200) to connect to (1 000 200)connect to via 1 with location = 1000 1000

NEW layer1 .01 +SHAPE STRIPE (200 200) (1000 *) (* 1000) via1

Please refer to the 5.1 DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFIN-23 (warning) Probably the regular wiring section has incorrect syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax is the following:

{ROUTED| FIXED | COVER} <layername> [TAPER] (x y) [(x *) | (* y) | <viaName>] ... where <layername> is a layer defined in the LEF.

For example : a wire on layer1 from (200 200) to connect to (1 000 200)connect to via 1 with location = 1000 1000

ROUTED layer1 (200 200) (1000 *) (* 1000) via1

Please refer to the 5.1 DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFIN-24 (warning) Probably the new regular wiring statment has incorrect syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax is the following:

[NEW <layername> [TAPER] [+ SHAPE {RING|STRING}] (x y) [(x *) | (* y) | <viaName>] ...

where: <layername> is a layer name defined in LEF.

For example : a wire on layer1 with width .01 from (200 200) to connect to (1 000 200)connect to via 1 with location = 1000 1000

NEW layer1 (200 200) (1000 *) (* 1000) via1

Please refer to the 5.1 DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFIN-25 (warning) Probably inside the PINS section, the plus statement is incorrect.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax is the following: [- <pinName> + NET <netName>] where <netName> is a net this pin connected to and is defined in the NETS section.

[+ SPECIAL] [+ DIRECTION { INPUT | OUTPUT | INOUT | FEEDTHRU }] [+ USE [SIGNAL | POWER | GROUND | CLOCK | TIEOFF | ANALOG]] [+ {FIXED | PLACED | COVER} <pt> <orient>] where <pt> is the location for the pin. <orient> is the orientation for this pin. For example: + FIXED (199 199) N

[+ LAYER <layername> <pt> <pt>] where <layername> is a layer which this pin is on

and defined in LEF. <pt> <pt> defines the pin geometry on that layer. For example: + LAYER layer1 (100 100) (200 200)

Please refer to the 5.1 DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFIN-26 (warning) Probably inside the REGIONS section, the plus statement is incorrect.

DESCRIPTION

This happens when unexpect syntax has been parsed. The important plus statments inside the REGIONS section are the following: [- <regionName> <pt> <pt> [pt pt]...] where one pair of <pt> defines one rectangle. Currently it only take the first rectangle and ignore the rest of rectangles. If other plus statments than above has syntax error then you can ignore. But if they are one of above statments, you need to follow the 5.1 DEF manual, corect them.

Please refer to the 5.1 DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFIN-27 (warning) Probably inside the GROUPS section, the plus statement is incorrect.

DESCRIPTION

This happens when unexpect syntax has been parsed. The important plus statments inside the GROUPS section are the following: [- groupName compNameRegExpr... where compNameRegExpr contains the regular expression like '*','%' or '-' For example: create a group called group1 containing all the cells with INST as the prefix. - group1 INST*

[+ REGION { <pt> <pt> | regionName }] where <pt> <pt> define the a rectangle. <regionName> is defined in the REGIONS section

For example: group1 is with (100 100) and (200 200) + group1 INST* - REGION (100 100)(200 200)

If other plus statments than above has syntax error then you can ignore. But if they

are one of above statments, you need to follow the 5.1 DEF manual, corect them.

Please refer to the 5.1 DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFIN-28 (error) Duplicate EEQ macro %s defined at line %d.

DESCRIPTION

You receive this error message because there is more than one EEQ macro defined in the DEF file. Only one EEQ macro can be defined for a cell.

WHAT NEXT

Edit the DEF file so there is only one EEQ macro defined for the cell.

DEFIN-29 (error) EEQ macro %s defined at line %d is not present in the physical library.

DESCRIPTION

The EEQ macro defined in the Design Exchange Format (DEF) file is not defined in the Synopsys physical library database (.pdb) files.

WHAT NEXT

Include the physical library that has the definition for the cell.

DEFR-1 (error) Failed to read file '%s'.

DESCRIPTION

The file might not exist in your path.

WHAT NEXT

Check if the file exist or rerun the program.

DEFR-2 (warning) Ignore '%s' at line %d.

DESCRIPTION

The DEF syntax has been ignored. The reader will not store any information for this line, but continue to read the rest of the file.

WHAT NEXT

Check if this line can be ignored. If not, edit the PDEF output file according to the IEEE PDEF syntax.

DEFR-3 (warning) Extract the pin location from this section, assuming pin name is matching netlist port name.

DESCRIPTION

The reader does not read logical netlist information therefore, it assumes all the pins in this section will match with the ports in the logical netlist.

WHAT NEXT

Examine the output PDEF and check with the logical netlist to make sure the pin is not in logical netlist.

DEFR-4 (warning) Probably the DIEAREA statement has

unexpected syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax is the following: DIEAREA <pt pt> ; <pt pt> is the corner points of the bounding rectangle for the design. For example: The following design uses a rectangle with lower left corner (100 100) and upper right corrner (900 900). DIEAREA 100 100 900 900

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFR-5 (warning) Probably inside the COMPONENTS section, the plus statement is incorrect.

DESCRIPTION

This happens when unexpect syntax has been parsed. The important plus statments inside the COMPONENTS section are the following : [+ {FIXED | COVER | PLACED | UNPLACED } <pt> <orient>] where <pt> is the location for the component <orient> is the orientation for the component

For example: + FIXED (199 199) N

[+ REGION { <pt> <pt> | <regionName> }] where the first <pt> is the lower left corner of the region. the second <pt> is the upper right corner of the region. <regionName> is the name defined in the REGIONS section.

For example: + REGION (10 10) (500 500) or + REGION region1

If other plus statments than above has syntax error then you can ignore. But if they are one of above statments, you need to follow the 5.x DEF manual, corect them.

Please refer to the 5.x DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFR-6 (error) Failed to read file '%s' because of missing PINS

section.

DESCRIPTION

The program only takes the DEF with the pins section.

WHAT NEXT

add the pins section in your DEF.

DEFR-7 (error) Require to read pdb which contains macro class definition to tell which components are PAD, so the program can take that as port location.

DESCRIPTION

The version of this DEF file is 4.x, it requires PINS section and library in pdbformat which contains io/dummy macro definition.

WHAT NEXT

Generate pdb using library compiler.

DEFR-8 (warning) Can not find macro type for this component '%s'.

DESCRIPTION

This information is needed to tell which component is an IO.

WHAT NEXT

make sure pdb include every component used in DEF.

DEFR-9 (error) Only support 5.x version. Ignore the Site

statement at line %d.

DESCRIPTION

The Site statments indicate there this DEF may not use 5.x version syntax. Please regenerate your DEF in 5.x version using your floorplan tool. The correct syntax to define the site array information to the tool is the following DEF 5.x syntax :

The correct syntax to define the site array information to the tool is the following DEF syntax :

ROW <row_name> <site_name> <X> <Y> <orientation> { DO <N> BY 1 STEP <spaceX> 0 | DO 1 by <N> STEP 0 <spaceY> };

where <row_name> is a unique string identifying this particular row. <site_name> is a site used for the row. The site is defined in the LEF. <X> <Y> is the coordinates of the row's starting point <orientation> Orientation of all sites in the row. { DO <N> BY 1 STEP <spaceX>0 | DO 1 by <N> STEP 0 <spaceY> } Horizontal or vertical step pattern to create the row.

For Example : The row_1 is using site CORE starting -10000 -10000. There are 222 sites in this row and the space between lower left corner of a site to the next lower left corner is 84. ROW row_1 CORE -10000 -10000 N DO 222 BY 1 STEP 84 0 ;

WHAT NEXT

Use the floorplan tool to regenerate the DEF file.

DEFR-10 (error) The program requires reading pdb.

DESCRIPTION

This pdb is a library pdb which contains library technology information. The reader needs to read library pdb to find out which site in DEF belongs to the CORE, and layer and via definitions.

WHAT NEXT

The library pdb can be generate using library compiler.

DEFR-11 (warning) Pin '%s' does not have location.

DESCRIPTION

The pin locations are part of floorplan information. Lossing pin locations will have

incomplete floorplan information.

WHAT NEXT

Add pin location for it to make floorplan contraints complete.

DEFR-12 (warning) Only extract the first rectangle as boundary at line '%d'.

DESCRIPTION

Currently multiple rectangles are not supported for move bounds. This message issued when reader tries to extract region contraints. Only the first rectangle will be use.

WHAT NEXT

If there are multiple rectangles then merge the multiple rectangles into one rectangle.

DEFR-13 (warning) Only support regions in GROUPS at line '%d'.

DESCRIPTION

Currently we do not extract perimeter attributes from GROUPS. Only REGIONS information will be extracted. Ignore all other soft fence attribute.

WHAT NEXT

If soft fence attribute is needed then translate them into REGIONS.

DEFR-14 (warning) Only support regular expressions '*','%','-' in GROUPS

DESCRIPTION

The '*' means any sequence of characters. The '%' means any single character. The '-' means any sequence of characters up to the next period '.'. Currently the reader

only can understand the regular expression described using the characters from above.

WHAT NEXT

Expand the unsupprted regular expression.

DEFR-15 (error) This layer %s is not defined in the library. The DEF file will be incorrect.

DESCRIPTION

This layer is missing in the physcial library.

WHAT NEXT

Add the layer to your physcial library (a plib file) and use read_lib and write_lib to write out the library.

DEFR-16 (warning) Detect %s near token '%s' at line %d. Continue to parse until the next correct rule can be applied.

DESCRIPTION

This happens when unexpect syntax has been parsed. It contines to read the file until the next syntax can be applied in the grammar rules.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFR-17 (warning) Probably the UNITS statement has incorrect syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax is the following: UNITS DISTANCE MICRONS <DEFconvertFactor> For example: UNITS DISTANCE MICRONS 1000 ;

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFR-18 (warning) Probably the ROW statement has incorrect syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax to define the site array information to the tool is the following DEF syntax :

ROW <row_name> <site_name> <X> <Y> <orientation> { DO <N> BY 1 STEP <spaceX> 0 | DO 1 by <N> STEP 0 <spaceY> };

where <row_name> is a unique string identifying this particular row. <site_name> is a site used for the row. The site is defined in the LEF. <X> <Y> is the coordinates of the row's starting point <orientation> Orientation of all sites in the row. { DO <N> BY 1 STEP <spaceX>0 | DO 1 by <N> STEP 0 <spaceY> } Horizontal or vertical step pattern to create the row.

For Example : The row_1 is using site CORE starting -10000 -10000. There are 222 sites in this row and the space between lower left corner of a site to the next lower left corner is 84. ROW row_1 CORE -10000 -10000 N DO 222 BY 1 STEP 84 0 ;

WHAT NEXT

Edit the DEF file to change the ROW statement or use the floorplan tool to regenerate the DEF file.

DEFR-19 (warning) Probably inside the SPECIALNETS section, the plus statement is incorrect.

DESCRIPTION

This happens when unexpect syntax has been parsed. The important plus statments inside the SPECIALNETS section are the following : [+ WIDTH <layername> <width>] where <layername> is the layer defined in LEF. <width> is the width used in for this specail route. For example: + WIDTH layer1 0.9

[+ SPACING <layername> <spacing> [RANGE <minwidth> <maxwidth>]] where <layername> is the lyser defined in LEF <spacing> is the spacing used for this special route. <minwidth> <maxwidth> defines the range of the wire width

For example: + SPACING layer1 .05 RANGE 0.01 0.08

If other plus statments than above has syntax error then you can ignore. But if they are one of above statments, you need to follow the 5.x DEF manual, corect them. Please refer to the 5.x DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFR-20 (warning) Probably the special wiring continue point has incorrect syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. They are have to be one of the following forms: 1. (X *) means the Y is from the previous point. 2. (* Y) means the X is from the previous point. 3. <viaName> means the use this via to connect the wire. The via location is decirbed previously. For example : use the previus Y and 1000 connect to via 1 with location = 1000 1000 (1000 *) (* 1000) via1 You need to follow the 5.x DEF manual, corect them. Please refer to the 5.x DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFR-21 (warning) Probably the special wiring section has incorrect syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax is the following:

{ROUTED| FIXED | COVER} <layername> <width> [+ SHAPE {RING|STRIPE}] (x y) [(x *) | (* y) | <viaName>] ... where: <layername> is a layer name defined in LEF. <width> is the wire width.

For example : a wire on layer1 with width .01 from (200 200) to connect to (1000 200)connect to via 1 with location = 1000 1000

ROUTED layer1 .01 +SHAPE STRIPE (200 200) (1000 *) (* 1000) via1

You need to follow the 5.x DEF manual, corect them. Please refer to the 5.x DEF manual for the detailed explanation.

Please refer to the 5.x DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFR-22 (warning) Probably the new special wiring statment has incorrect syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax is the following:

[NEW <layername> <width> [+ SHAPE {RING|STRING}] (x y) [(x *) | (* y) | <viaName>] ...

where: <layername> is a layer name defined in LEF. <width> is the wire width.

For example : a wire on layer1 with width .01 from (200 200) to connect to (1 000 200)connect to via 1 with location = 1000 1000

NEW layer1 .01 +SHAPE STRIPE (200 200) (1000 *) (* 1000) via1

Please refer to the 5.x DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFR-23 (warning) Probably the regular wiring section has incorrect syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax is the following:

{ROUTED| FIXED | COVER} <layername> [TAPER] (x y) [(x *) | (* y) | <viaName>] ... where <layername> is a layer defined in the LEF.

For example : a wire on layer1 from (200 200) to connect to (1 000 200)connect to via 1 with location = 1000 1000

ROUTED layer1 (200 200) (1000 *) (* 1000) via1

Please refer to the 5.x DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFR-24 (warning) Probably the new regular wiring statment has incorrect syntax.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax is the following:

[NEW <layername> [TAPER] [+ SHAPE {RING|STRING}] (x y) [(x *) | (* y) | <viaName>] ...

where: <layername> is a layer name defined in LEF.

For example : a wire on layer1 with width .01 from (200 200) to connect to (1 000 200)connect to via 1 with location = 1000 1000

NEW layer1 (200 200) (1000 *) (* 1000) via1

Please refer to the 5.x DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFR-25 (warning) Probably inside the PINS section, the plus statement is incorrect.

DESCRIPTION

This happens when unexpect syntax has been parsed. The correct syntax is the following: [- <pinName> + NET <netName>] where <netName> is a net this pin connected to and is defined in the NETS section.

[+ SPECIAL] [+ DIRECTION { INPUT | OUTPUT | INOUT | FEEDTHRU }] [+ USE [SIGNAL | POWER | GROUND | CLOCK | TIEOFF | ANALOG]] [+ {FIXED | PLACED | COVER} <pt> <orient>] where <pt> is the location for the pin. <orient> is the orientation for this pin. For example: + FIXED (199 199) N

[+ LAYER <layername> <pt> <pt>] where <layername> is a layer which this pin is on

and defined in LEF. <pt> <pt> defines the pin geometry on that layer. For example: + LAYER layer1 (100 100) (200 200)

Please refer to the 5.x DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFR-26 (warning) Probably inside the REGIONS section, the plus statement is incorrect.

DESCRIPTION

This happens when unexpect syntax has been parsed. The important plus statments inside the REGIONS section are the following: [- <regionName> <pt> <pt> [pt pt]...] where one pair of <pt> defines one rectangle. Currently it only take the first rectangle and ignore the rest of rectangles. If other plus statments than above has syntax error then you can ignore. But if they are one of above statments, you need to follow the 5.x DEF manual, corect them.

Please refer to the 5.x DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFR-27 (warning) Probably inside the GROUPS section, the plus statement is incorrect.

DESCRIPTION

This happens when unexpect syntax has been parsed. The important plus statments inside the GROUPS section are the following: [- groupName compNameRegExpr... where compNameRegExpr contains the regular expression like '*','%' or '-' For example: create a group called group1 containing all the cells with INST as the prefix. - group1 INST*

[+ REGION { <pt> <pt> | regionName }] where <pt> <pt> define the a rectangle. <regionName> is defined in the REGIONS section

For example: group1 is with (100 100) and (200 200) + group1 INST* - REGION (100 100)(200 200)

If other plus statments than above has syntax error then you can ignore. But if they

are one of above statments, you need to follow the 5.x DEF manual, corect them.

Please refer to the 5.x DEF manual for the detailed explanation.

WHAT NEXT

To remove this warning simple change your DEF file according to the DEF manual.

DEFR-28 (error) Duplicate EEQ macro %s defined at line %d.

DESCRIPTION

You receive this error message because there is more than one EEQ macro defined in the DEF file. Only one EEQ macro can be defined for a cell.

WHAT NEXT

Edit the DEF file so there is only one EEQ macro defined for the cell.

DEFR-29 (error) EEQ macro %s defined at line %d not present in physical library.

DESCRIPTION

You receive this error message because the EEQ macro defined in the DEF file is not defined in pdb files.

WHAT NEXT

Include the physical library which has the definition for the cell.

DEFR-30 (warning) Site ’%s’ has no type defined in physical library, ignored.

DESCRIPTION

The site definition

WHAT NEXT

Check if the physical_library variable is set correctly.

DEFR-31 (warning) Clusters exist in netlist, will be deleted.

DESCRIPTION

Clusters are present in the netlist. All the existing clusters will be deleted before annotating any data from the input DEF file.

WHAT NEXT

Please make sure that the input netlist is a pure logical netlist.

DEFR-32 (warning) Reference to undefined region '%s' in GROUPS section.

DESCRIPTION

The region referenced in the GROUPS section has not been defined in the REGION section.

WHAT NEXT

Please provide a definition of the undefined region referenced.

DEFR-33 (info) Adding spare cell '%s'.

DESCRIPTION

The spare cell present in DEF is being added into the netlist.

WHAT NEXT

DEFR-34 (info) Adding physical only cell '%s'.

DESCRIPTION

The physical only cell present in input DEF is being added into the netlist, because read_def command was called with -allow_physical_cells switch.

WHAT NEXT

If this is not desired, please call the read_def command without the -allow_physical_cells switch.

DEFR-35 (warning) Cell instance '%s' does not correspond to a real cell.

DESCRIPTION

The identified cell instance cannot be found in the logical hierarchy beneath **current_design**. The instance will be ignored unless the -allow_physical_cells switch of read_def is used.

WHAT NEXT

Check to see why the instance identified in the message was included in the DEF file. If the instance is meant to be in the DEF file as a physical-only cell, such as a filler cell or endcap cell, re-run read_def with the -allow_physical_cells option.

DEFR-36 (warning) The cell intance '%s' is not linked. It's presence within the cluster will be ignored.

DESCRIPTION

This message indicates that the specified cell instance is not linked. Each cell instance defined within a cluster must refer to a fully linked leaf cell. You cannot define a cell in a cluster that is not fully linked.

WHAT NEXT

Find the design or library cell to which this cell instance should be linked, and include it in the **search_path** or **link_library**.

DEFR-37 (warning) Attribute found on hierarchical cell '%s', will be ignored.

DESCRIPTION

The input DEF file has had an attribute defined for a hierarchical cell. Attributes are not currently supported on hierarchical cells.

WHAT NEXT

Remove the attributes from the hierarchical cell or else put leaf cells in the DEF file instead, and set the attributes on the leaf cells.

DEFR-38 (warning) The cell instance '%s' has already been listed under cluster '%s'. The previous classification will be overwritten.

DESCRIPTION

This message indicates that the identified cell instance was previously listed as part of another cluster. The previous association is ignored. Only the most recent cluster association (that is, the cluster association furthest down in the file) will be preserved.

WHAT NEXT

Investigate the reason why the cell instance was listed in more than one cluster, and correct any errors.

DEFR-39 (warning) The pin '%s' does not exist.

DESCRIPTION

The identified pin/port cannot be found in the **current_design**. The pin/port will be ignored.

WHAT NEXT

Check to see why the pin identified in the message was listed in the DEF file.

DEFR-40 (info) Input DEF version is '%1.1f.'

DESCRIPTION

This message prints out the version of the input DEF file.

WHAT NEXT

DEFR-41 (warning) DEF design '%s' is different from current design '%s'.

DESCRIPTION

The design name in the input DEF file is different from the design specified using -design switch in the read_def command. The design in the netlist with the same name as DEF desing will be annotated.

WHAT NEXT

Provied the same design name in -switch option as in the input DEF file.

DEFR-42 (warning) DEF design '%s' is different from current_design '%s'.

DESCRIPTION

The design name in the input DEF file is different from the current_design. The design in the netlist with the same name as DEF desing will be annotated.

WHAT NEXT

Please set the current_design to the same as design in input DEF file.

DEFR-43 (info) Annotating design '%s'.

DESCRIPTION

This message prints the name of the design which is being annotated.

WHAT NEXT

DEFR-44 (warning) NAMECASESENSITIVITY always assumed to be ON.

DESCRIPTION

The read_def parser always assume name case sensitivity to be ON.

WHAT NEXT

Check if the input DEF file is cases insensitive.

DEFR-45 (warning) DIVIDERCHAR always assumed to be '/'.

DESCRIPTION

The read_def parser always assumes the hierarchy divider to be '/'.

WHAT NEXT

Check if the input DEF uses a different character for hierarchy divider. If so, it needs to be replaced by '/'.

DEFR-46 (warning) BUSBITCHAR will be converted to '[]'.

DESCRIPTION

The input DEF file contains BUSBITCHAR other than '[]'. The read_def parser is capable of parsing DEF files with different busbit characters. But the parser internally converts it to '[]' before storing in db.

WHAT NEXT

Please note that even though the input DEF is allowed to have a different bus bit character, the output DEF file will always use '[]'.

DEFR-47 (warning) Unsupported DEF construct '%s' parsed. Will be ignored.

DESCRIPTION

The read_def command does not support the identified DEF construct, and will ignore it. The related information will not be stored within db.

WHAT NEXT

Please note that all the information pertaining to unsupported DEF constructs will be lost.

DEFR-48 (warning) Conversion factor < 1, will result in loss of accuracy.

DESCRIPTION

The read_def command computes the conversion factor based on the distance unit in the input DEF file and variables 'physopt_scaling_factor' & 'pdef_scale_location_by'. Since all the distances in an input DEF file are multiplied by this conversion factor before storing within db, there will be a loss of accuracy if this value is less than one.

WHAT NEXT

Please set the variables 'physopt_scaling_factor' & 'pdef_scale_location_by' appropriately such that the conversion factor is greater than or equal to one.

DEFR-49 (info) DEF DISTANCE UNIT %.0f.

DESCRIPTION

This message indicates the value of distance unit read from the input DEF file.

WHAT NEXT

DEFR-50 (info) DIE AREA: '(%d, %d) (%d, %d)'

DESCRIPTION

This message indicates the value of DIE AREA read from the input DEF file.

WHAT NEXT

DEFR-51 (info) Annotating '%s' information in netlist.

DESCRIPTION

This message indicates that the identified section from input DEF file is currently being annotated into the netlist.

WHAT NEXT

DEFR-52 (info) Annotating via information from pdb in netlist.

DESCRIPTION

This message indicates that the via information from physical library is being annotated into the netlist.

WHAT NEXT

DEFR-53 (warning) Top level cluster was not created, skipping nets.

DESCRIPTION

This message indicates that the read_def command was not able to find out the top level cluster while annotating nets. The nets section will be skipped.

WHAT NEXT

The probable cause of the top level cluster not being created would be a syntax error in the input DEF. Please remove syntax errors if any from the input DEF file.

DEFR-54 (info) Skipping signal nets.

DESCRIPTION

This message indicates that the read_def command is skipping the signal nets section. This is because the read_def command was called with the -skip_signal_nets switch.

WHAT NEXT

If signal nets are desired to be annotated, please call the read_def command without the -skip_signal_nets switch.

DEFR-55 (warning) Missing UNITS DISTANCE in DEF, assuming 1000.

DESCRIPTION

This message indicates that the input DEF file does not have the UNITS DISTANCE section. A default value of 1000 is assumed by the read_def command.

WHAT NEXT

Please add the distance unit in the input DEF file.

DEFR-56 (info) Reading input def file '%s'.

DESCRIPTION

This message indicates that the identified DEF file is being read.

WHAT NEXT

DEFR-57 (error) This version of read_def cannot read version

1.2 of pdb. Please use version 2.0 of pdb.

DESCRIPTION

This message indicates that the version of pdb is not supported by the read_def command.

WHAT NEXT

Please regenerate version 2.0 or above of the pdb.

DEFR-58 (error) Unable to find definition for via %s.

DESCRIPTION

The via named in the message was referenced without being defined. The read_def command looks for via definitions in the input DEF and in the pdb. The definition for this via was not found in either places.

WHAT NEXT

Please make sure that all vias referred in the input DEF are either defined in pdb's or in the input DEF.

DEFR-59 (warning) Illegal value %d for UNIT specified in input DEF, using 1000.

DESCRIPTION

The only legal values for UNIT in DEF are 100, 200, 1000, 2000. If a value other than these is specified, read_def will use a value of 1000, and scale all the numerical values accordingly. Please be aware that there could be a loss of accuracy if UNIT value in input DEF is greater than 1000. So it is always advisable to use legal value for UNIT in the input DEF.

WHAT NEXT

Please modify the input DEF to use correct UNIT value.

DEFR-60 (error) The current system DEF unit (%d) is not a

multiple of the input DEF unit (%d), possibly causing a roundoff error.

DESCRIPTION

The DEF writer generates this error message when a roundoff error might occur due to an incorrect UNIT value.

The DEF writer checks for the input DEF unit and compares it with the current system DEF unit. If the input DEF unit is not a whole number multiple of the current DEF unit in the system, the tool generates this message.

WHAT NEXT

To continue reading in the input DEF regardless of a possible roundoff error, use the **-enforce_scaling** switch.

To avoid a possible roundoff error, regenerate the DEF file with the correct unit value.

DEFR-61 (warning) The blockage coordinate (%d %d) is out of bound; the coordinates for the die area are (%d %d) (%d %d).

DESCRIPTION

The DEF writer generates this error message when the blockage coordinate is out of bound with respect to the die area.

WHAT NEXT

Regenerate the DEF file with correct values for blockages.

DEFR-62 (information) The design is reloaded for syncing from Milkyway.

DESCRIPTION

This message informs you that the tool is reloading the design data from the Milkyway database. This is done internally so that the physical data from the input DEF file is consistent in the memory.

WHAT NEXT

This is an informational message only. No action is required.

DEFR-63 (error) The read_def command failed because the Milkyway executable version is outdated. The read_def command failed.

DESCRIPTION

You receive the error message when the Milkyway executable is not compatible for read_def and write_def actions.

WHAT NEXT

Install the latest Milkyway executable prior to running **read_def** or **write_def** commands.

SEE ALSO

read_def(2)
write_def(3)

DEFR-64 (error) The Milkyway executable cannot be found. The read_def command failed.

DESCRIPTION

You receive this error message when the Milkyway executable cannot be found at the installed location.

WHAT NEXT

Install the latest Milkyway executable prior to running the **read_def** command.

SEE ALSO

read_def(2)

DEFR-65 (warning) Using .pdb for the physical library is not

recommended. Use FRAM for the physical library.

DESCRIPTION

This warning message occurs when attempting to use the physical library datatbase (.pdb) for the physical library.

WHAT NEXT

Use the following commands and variable settings for the FRAM physical libraries:

```
set use_pdb_lib_format FALSE
set mw_reference_library "..."
set mw_design_library string
create_mw_design ...
max_tluplus_file_name ...
```

For example:

```
prompt> set use_pdb_lib_format FALSE

prompt> set mw_reference_library "./ref/mw_lib/sc ./ref/mw_lib/io \
         /ref/mw_lib/ram16x128"

prompt> set mw_design_library design_lib_orca

prompt> create_mw_design -tech_file tech_file_name
        -max_tluplus Bmax_tluplus_file_name \
        -min_tluplus min_tluplus_file_name \
        tf2itf_map tf2itf_map_file_name
```

SEE ALSO

create_mw_design(2)

DEFR-100 (Warning) Site '%s' is not defined in physical library, ignored.

DESCRIPTION

The site used in ROW in DEF needs to be defined in physical libary so that the site size can be used to compute core area. Without definition in physical library, the ROW will be ignored and the computed core area may be wrong.

WHAT NEXT

Check whethe the design is using FRAM library but the site in DEF is not unit. If

this is the case, for example, the site in DEF is CORE, use set mw_site_name_mapping "CORE unit"

DEFR-101 (Error) No site in DEF can be found in physical library. No core area is generated.

DESCRIPTION

The site used in ROW in DEF needs to be defined in physical libary so that the site size can be used to compute core area. Without matcing site definition in physical library, all ROWs are ignored and no core area can be generated.

WHAT NEXT

Check whethe the design is using FRAM library but the site in DEF is not unit. If this is the case, for example, the site in DEF is CORE, use set mw_site_name_mapping "CORE unit"

DEFR-102 (Warning) Use the default site ’unit’ to compute placement area, since the site ’%s’ and its mapped one ’%s’ are not defined in physical library.

DESCRIPTION

The site used in ROW in DEF needs to be defined in physical libary so that the site size can be used to compute core area. If the site in ROW is not defined in physical library, then the mapped site will be used. If neither the site in the ROW nor its mapped one is defined in the physical library, then the default site "unit" is used.

WHAT NEXT

Check whether the design is using FRAM library but the site in DEF is not unit. If this is the case, for example, the site in DEF is CORE, use set mw_site_name_mapping "CORE unit"

DEFR-103 (warning) Unmapped cell ’%s’ in DEF is ignored to

extract physical constraints.

DESCRIPTION

This warning message advises you that an unmapped cell is being ignored. Locations cannot be set for unmapped cells. The **extract_physical_constraints** command ignores unmapped cells in the DEF.

WHAT NEXT

This is only a warning message. No action is required.

SEE ALSO

extract_physical_constraints(2)
set_cell_location(2)

DEFR-104 (Warning) Use the default site ’unit’ to compute placement area, since the site ’%s’ is not defined in physical library.

DESCRIPTION

The site used in ROW in DEF needs to be defined in physical libary so that the site size can be used to compute core area. If the site in ROW is not defined in physical library, then the mapped site will be used. If neither the site in the ROW nor its mapped one is defined in the physical library, then the default site "unit" is used.

WHAT NEXT

Check whether the design is using FRAM library but the site in DEF is not unit. If this is the case, for example, the site in DEF is CORE, use set mw_site_name_mapping "CORE unit".

DEFR-105 (Warning) Section %s count doesn’t match. Expected count is %d, Actual count is %d.

DESCRIPTION

In DEF, each section has a count at its begining to indicate the number of the items to appear in this section, this warning shows that it doesn’t match the actual number of the items in this section.

WHAT NEXT

Nothing to be done.

DEFR-106 (warning) The '%s' hierarchical cell in DEF is omitted from the extract physical constraints process.

DESCRIPTION

This warning message occurs when attempting to set the location on a hierarchical cell that is not an IC Compiler or Design Compiler topographical ILM, or a Design Compiler topographical placed hierarchy.

The location is ignored in the extract physical constraints process.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, you can modify the DEF to provide a location to a valid hierarchy, and run the command again.

SEE ALSO

extract_physical_constraints(2)
set_cell_location(2)

DEL-001 (error) You cannot mix an LCD operating conditon with a non LCD operating condition.

DESCRIPTION

A operating condition is detected to be an LCD operating condition, while another specified operating condition is not an LCD operating condition. The ability to specify two different types of operating conditions is not supported.

WHAT NEXT

Supply a consistent min and max operating conditions. Either two non-LCD operating conditions or two LCD operating conditions.

DEL-002 (error) You cannot specify a single LCD operating conditon.

DESCRIPTION

LCD operating conditions can be specified in min-max mode only.

WHAT NEXT

You need to use the min-max mode with LCD operating conditions.

DEL-003 (warning) Library '%s' has time unit of %gns but the main library unit is %gns

DESCRIPTION

If multiple libraries are used in analysis, they must have the same units. This restriction will be removed in a future version of PrimeTime.

WHAT NEXT

Convert the units in the .lib and regenerate a library .db file using Library Compiler if possible.

DEL-004 (warning) Library '%s' has capacitive_load unit of %gpF
but the main library unit is %gpF

DESCRIPTION

If multiple libraries are used in analysis, they must have the same units. This restriction will be removed in a future version of PrimeTime.

WHAT NEXT

Convert the units in the .lib and regenerate a library .db file using Library Compiler if possible.

DEL-005 (error) Cannot remove operating_condition from cell '%s': Power rails inherited from '%s' would not match rails of cell '%s'.

DESCRIPTION

Removing rail voltages or an operating condition from a hierarchical cell, may cause a lower level leaf cell to inherit a new set of power rails from a higher level hierarchical cell. Such a removal is disallowed unless the power rails in the library of the leaf cell are a subset of the newly inherited rails.

WHAT NEXT

Ensure that appropriate rail voltages/ operating conditions have been previously set on such leaf cells.

DEL-006 (warning) The operating condition does not define all rails
of cell '%s'.

DESCRIPTION

The operating condition or rail voltage does not contain all power rails therefore default voltages will be used on the remaining power rails. The default voltages are defined in power_supply section of the .lib.

WHAT NEXT

Ensure that the power rails specified in the library of the cell are same as (or a subset of) the rails in the operating condition.

DEL-007 (warning) Setting of multi-rail operating condition or rail voltage on hierarchical cell '%s' may result in incomplete assignment of power rails.

DESCRIPTION

Assignment of voltages to power rails on multi-rail cells is based on matching rail names in the operating conditions and power_supply definition in library description of the cell.

When setting operating condition or rail voltages on hierarchical cell this information is inherited by all cells in the hierarchy unless they have their explicit operating condition or rail voltage. Since rails in two different libraries can have same name then the effect of setting operating condition or rail voltage with multiple rails on hierarchical cell may result in unintended or incomplete voltage assignment.

WHAT NEXT

Set an operating condition or rail voltages on any lower level cells that require different power rail voltages.

DEL-008 (warning) Default %s operating conditions per library resulted in cells having different temperature, e.g., %s has %g but %s has %g.

DESCRIPTION

This warning message tells you that default operating conditions assigned to cells may not represent actual operating environment because temperature is not same for all cells in the design.

This message is displayed during update_timing.

WHAT NEXT

If the temperature difference is intentional and you are trying to model temperature variation on the chip then no action is required. If not intentional then use set_operating_conditions to explicitly set operating conditions on the design or individual blocks.

SEE ALSO

set_operating_conditions (2). **report_cell** (2). **default_oc_per_lib** (3).

DEL-009 (error) Cannot set single rail voltage on multirail cell '%s'.

DESCRIPTION

You may not set a single rail voltage on a cell using set_rail_voltage -rail_rvalue if that cell has multiple power rails defined in the library.

WHAT NEXT

Use set_rail_voltage -rail_list.

DEL-010 (Error) Unable to parse input/output_voltage in lib '%s': ('%s' = '%s').

DESCRIPTION

When parsing the input_voltage or output_voltage attribute of a library, PrimeTime has encountered a string that it cannot parse. Note that PrimeTime can only parst binary expressions for input/output_voltage.

WHAT NEXT

Ensure that the input/output_voltage attributes of you library contain only binary expressions.

DEL-011 (information) The most constraining rise and fall values of the '%s'

constraint arc occur for different input conditions.

DESCRIPTION

Due to non-monotonicity in arc data, the most constraining rise and fall delay values arise from different computation input parameters. In most libraries, constraint arcs are characterized with respect to the transition time at the clock or reference pin as well as the transition time at the data or related pin. In min-max analysis modes, the arc delay can be computed in two libraries, with min and max values on the input transitions. Specifically, in on-chip-variation (OCV) mode, up to eight calculations may be necessary to identify the most constraining value of the arc delay.

Given that the delay is a potential permutation of various input parameters, it is possible that the most constraining, or maximum, rise and fall delays arise from different permutations of the input parameters. This scenario has occurred for the specific constraint arc delay being reported.

WHAT NEXT

This is an advisory message as no further action is necessary.

DEL-012 (error) The desired operating-condition or rail-voltage or temperature for cell '%s' is outside the domain covered by the applicable scaling library group.

DESCRIPTION

You may not set an operating-condition or rail-voltage or temperature that goes outside the domain covered by an applicable scaling library group. If the **define_scaling_lib_group** command was used to setup a group of libraries that includes the specified cell, any operating-condition or rail-voltage set on the cell must be within the process, voltage, and temperature domain covered by the group.

WHAT NEXT

Correct either the operating condition or the scaling library group.

SEE ALSO

define_scaling_lib_group (2), **create_operating_conditions** (2), **set_operating_conditions** (2), **set_rail_voltage** (2). **set_temperature** (2).

DEL-013 (information) Assuming the default level shifter strategy '%s'

DESCRIPTION

The commands without any arguments resets the level shifter strategy to the default 'all'. Default strategy is to reports all driver and load signal signal level mismatches.

WHAT NEXT

To set a specific startegy use **set_level_shifter_strategy -rule <strategy>**.

SEE ALSO

set_level_shifter_strategy (2), **check_timing** (2), **set_level_shifter_threshold** (2).

DEL-014 (information) The operating conditions set are outside the conditions defined by the libraries in the scaling group for atleast one instance in the design, so extrapolation is being done.

DESCRIPTION

If you set an operating-condition that goes outside the domain covered by an applicable scaling library group, extrapolation will be done for the given operating condition it the scaling libraries are defined for atleast two different operating conditions. If the define_scaling_lib_group command was used to setup a group of libraries that includes the specified cell, any operating-condition or rail-voltage set on the cell must be within the process, voltage, and temperature domain covered by the group to avoid any extrapolation.

WHAT NEXT

Correct either the operating condition or the scaling library group if extrapolation is not desirable.

SEE ALSO

define_scaling_lib_group (2), **create_operating_conditions** (2), **set_operating_conditions** (2),

DEL-015 (warning) The operating conditions set are far outside the conditions defined by the libraries in the scaling group for atleast one instance in the design, so extrapolation far beyond the safe range is being done.

DESCRIPTION

If you set an operating-condition that is outside the domain covered by an applicable scaling library group, extrapolation will be done for the given operating condition if the scaling libraries are defined for atleast two different operating conditions. If the define_scaling_lib_group command was used to setup a group of libraries that includes the specified cell, any operating-condition set on the cell must be within the process, voltage, and temperature domain covered by the group to avoid any extrapolation. The accuracy of results may not be good if the operating conditions are set far outside the domain of the scaling group.

WHAT NEXT

Correct either the operating condition or the scaling library group if extrapolation is not desirable.

SEE ALSO

define_scaling_lib_group (2), **create_operating_conditions** (2), **set_operating_conditions** (2),

DEL-016 (information) PrimeTime did not compute a valid '%s' transition at input; report_delay_calculation will use zero instead.

DESCRIPTION

Transition times at the output of disabled arcs or non-driven transitions of half unate arcs are considered invalid and are propagated as such in PrimeTime so as not to merge with valid signal transitions downstream. For the purposes of delay calculation, a zero slew is used to perform the cell arc calculation. Even though using a zero input slew could result in a corresponding non-zero output slew, this output slew is in turn marked invalid.

WHAT NEXT

This is an advisory message as no further action is necessary.

DEL-017 (information) The minimum values of the '%s' constraint arc
are not used by timing analysis.

DESCRIPTION

For the evaluating the worst possible conditions for a timing violation and given that timing constraint senses implicitly encode minimum versus maximum conditions such as hold and setup, PrimeTime strictly uses the maximum computed constraint arc delay values for computing endpoint slack.

PrimeTime computes and preserves the minimum delay values for constraint arcs for two reasons. First, these minimum values are exported through attributes off the timing_arc object for general use. Second, other applications dependent on PrimeTime delay calculation through SDF generation do require minimum values to be present.

WHAT NEXT

This is an advisory message as no further action is necessary.

DES-001 (error) Current design is not defined.

DESCRIPTION

The current design is not defined. Many commands require that the current design is set.

WHAT NEXT

You must read a design database file and link a design.

DES-002 (error) Cannot find %s '%s' in design '%s'

DESCRIPTION

The specified object cannot be found in the given design. This is sometimes seen while reading SDF and parasitics files. In those cases, it could indicate a file which is out of sync with the design.

WHAT NEXT

If reading SDF or parasitics, verify that the file matches the design.

DES-003 (error) '%s' cannot be used on %s %s '%s'.

DESCRIPTION

Certain commands are valid only for input or output objects.

WHAT NEXT

Enter the command with a valid list of objects.

DES-004 (error) Cannot find design '%s'.

DESCRIPTION

There is no design with that name is in memory.

WHAT NEXT

Read in the design or reenter the command with a different name.

DES-005 (error) Cannot set current instance to leaf cell '%s'.

DESCRIPTION

The current instance must be a hierarchical cell.

WHAT NEXT

DES-006 (error) Cannot find pin '%s' on cell '%s'.

DESCRIPTION

The pin does not exist on the specified cell.

WHAT NEXT

Use **query_objects [select_pin -of_object [select_cell *cell_name*]]** to list pin names on the cell.

DES-007 (warning) '%s' is not a valid object type.

DESCRIPTION

When -from or -to option is used with set_disable_timing or remove_disable_timing , the object list can only be a cell or a lib cell. This warning is generated for objects of type port and pin.

WHAT NEXT

Don’t use -from or -to option to disable pins or ports.

DES-008 (error) Cannot find %s ’%s’ in library ’%s’.

DESCRIPTION

The specified object cannot be found in the given library.

WHAT NEXT

Enter the command again with a valid object name.

DES-009 (error) Cannot find pin ’%s’ on library cell ’%s’.

DESCRIPTION

The pin does not exist on the specified library cell.

WHAT NEXT

Enter the command again with a valid object name.

DES-010 (error) Cannot find %s ’%s’.

DESCRIPTION

The specified object cannot be found.

WHAT NEXT

Enter the command again with a valid object name.

DES-011 (error) Cell '%s' is not hierarchical.

DESCRIPTION

The command only works on hierarchical cells.

WHAT NEXT

Enter the command again with a hierarchical cell.

DES-012 (error) Cannot use '%s' command on %s '%s'.

DESCRIPTION

The command works only on ports of a specific direction.

WHAT NEXT

DES-013 (error) Current design is not in min-max mode.

DESCRIPTION

Most of the -min and -max options of commands work only when the design is in min-max mode. The design is considered in min-max mode when 2 operating conditions are specified, such as "set_operating_condition -min OCbest -max OCworst". The design can also be in min-max mode after reading an SDF file with the -min_max option (for example, read_sdf -min_max mydesign.sdf).

WHAT NEXT

DES-014 (error) Object '%s' is not in the current design.

DESCRIPTION

You attempted an operation on an object that is outside of the scope of current design. For example, if you select a cell from one design, and attempt to set the current instance to that cell in a different (current) design, this error is generated.

WHAT NEXT

DES-015 (error) Cannot use '%s' command on %s '%s' because it is a limited design.

DESCRIPTION

Access to a design is limited because it requires a license and the only license available was a limited license. As a result, the internals of the design are hidden. Some reports are able to work around limited designs (and instances of them), but some cannot.

WHAT NEXT

If the design is licensed for full access, ensure that you can check out that license before reading the design. Some designs will always be limited.

DES-016 (error) Cannot use '%s' command on %s '%s' because it contains instances of limited designs%s.

DESCRIPTION

Access to a design is limited because it requires a license and the only license available was a limited license. As a result, the internals of the design are hidden. Some reports are able to work around limited designs (and instances of them), but others cannot.

WHAT NEXT

If the design is licensed for full access, ensure that you can check out that license before reading the design. Some designs will always be limited.

DES-017 (information) Could not auto-link design '%s'.

DESCRIPTION

You executed a command that tried to link the current design. The design could not be linked or it already failed to link. The design now has unresolved references.

WHAT NEXT

Determine the reason for the unresolved references. This might require changing the value of the search_path or link_path variables. If these references are not yet defined, you can make the linker create black-boxes for them by setting the variable link_create_black_boxes to true. Finally, relink the design using the **link_design** command.

DES-018 (error) There is already an operating condition named '%s' in library '%s'.

DESCRIPTION

The **create_operating_condition** command cannot overwrite an existing operating condition.

WHAT NEXT

Choose a new name for the operating condition. To list the existing operating conditions in the specified library, use **report_lib**.

DES-019 (warning) Library '%s' has been generated with an old version of the Library Compiler. It needs to be rebuilt to support case analysis on sequential cells.

DESCRIPTION

You receive this message if the current library DB is out of date. The library DBs have detailed functional information generated by Library Compiler from the library .lib file. Information generated by Library Compiler prior to version 2000.11 is not supported.

WHAT NEXT

Use Library Compiler to regenerate your library DB. Follow these steps:

1. Read in the .lib file.

```
dc_shell> read_lib mylibrary.lib
```

2. Write out the .db file.

```
dc_shell> write mylibrary.db
```

DES-020 (warning) No operating condition is specified, assuming a voltage value of %s volts for RC delay calculation.

DESCRIPTION

No operating condition is specified for the current library, so PrimeTime does not know what is the voltage value when performing RC delay calculation

WHAT NEXT

Specify the operating condition of the current library with **set_operating_condition**. To get a list of the operating conditions of your library, use **report_library**.

```
pt_shell> report_library my_lib.db

   Name                 Process     Temp        Voltage     Tree Type
   --------------------------------------------------------------------------
   WCCOM                3.00      115.00        3.00     balanced_case

pt_shell> set_operating_condition WCCOM
```

DES-021 (warning) These environment variables need to be set for accurate RC delay calculation:

Variable name Default

---

rc_slew_lower_threshold_pct_rise 20
rc_slew_lower_threshold_pct_fall 20
rc_slew_upper_threshold_pct_rise 80
rc_slew_upper_threshold_pct_fall 80
rc_input_threshold_pct_rise 50
rc_input_threshold_pct_fall 50
rc_output_threshold_pct_rise 50
rc_output_threshold_pct_fall 50
rc_slew_derate_from_library 1

DESCRIPTION

When parasitics are annotated on a design, timing calculations use these variables to compute delays and transition times. The values can be set by either a cell library or equivalent shell variables. If one of these approaches does not set all of the values, this warning message is issued to alert the user. If both approaches set the values, the shell variables take precidence.

WHAT NEXT

Either set all of the above values in a cell library or set them all with shell variables. See the man page for each variable for more info.

DES-022 (warning) Some of the following settings have an incorrect value less than or equal to 1, or they are equal to 100. The proper range for these values is exclusively between 1 and 100. Here are the fallback values that will be used:

Setting Fallback

---

rc_slew_lower_threshold_pct_rise %d
rc_slew_lower_threshold_pct_fall %d
rc_slew_upper_threshold_pct_rise %d
rc_slew_upper_threshold_pct_fall %d
rc_input_threshold_pct_rise %d
rc_input_threshold_pct_fall %d
rc_output_threshold_pct_rise %d
rc_output_threshold_pct_fall %d

DESCRIPTION

These values are used by delay-calculation with annotated parasitics. They should be set by libraries, but if not, shell variables with the same names can be set to provide the values. In either case, the values represent percentages, not decimal fractions. If a value less than or equal to 1 is encountered, it will be interpreted

as a decimal fraction and this warning will be issued.

If a zero value is encountered, it will be changed to 5%; if 1 or 100 value is encountered, it will be changed to 95%. We suggest the user to set the delay and slew trip point thresholds in the library directly, and suggest the user to keep them in the range of 10 to 90.

Please note that this warning message is only shown for either the main library (i.e. first in link_path) or the shell variables.

WHAT NEXT

Set a percentage value between 1 and 100 (exclusive) to specify the characterization thresholds of the Synopsys library.

SEE ALSO

lib_thresholds_per_lib (3), **rc_input_threshold_pct_fall** (3), **rc_input_threshold_pct_rise** (3), **rc_output_threshold_pct_fall** (3), **rc_output_threshold_pct_rise** (3), **rc_slew_lower_threshold_pct_fall** (3), **rc_slew_lower_threshold_pct_rise** (3), **rc_slew_upper_threshold_pct_fall** (3), **rc_slew_upper_threshold_pct_rise** (3).

DES-023 (warning) Net '%s' is multi-driven.

DESCRIPTION

The specified net is multi-driven by non-three-state cells. PrimeTime will try to peform multi-driven delay calculation for all switching scenarios defined by the networks attached to the drivers' from-pins. In order for such scenarios to be valid, a given from-net must uniquely cover all of the strong drivers attached to the multi-driven to-net.

If a from-net does not cover all of the strong drivers, or if a from-net is attached to more than one pin on a specific driver, detailed RC delay calculation cannot be performed. Instead, fractional lumped analysis will be used; the load will be assumed to be the total capacitance of the multi-driven net divided by the number of drivers.

WHAT NEXT

Verify that you indeed want the indicated net to be multi-driven. This capability is commonly used to wire cells in parallel to achieve greater drive strength.

SEE ALSO

RC-002 (n), **RC-003** (n).

DES-024 (warning) Net '%s' has an incomplete RC network.

DESCRIPTION

The specified net has an imcomplete RC network. This means that some RC elements are dangling, or that all drivers and loads of the nets are not connected by all the RC elements.

WHAT NEXT

The RC network annotation is ignored for the specified net.

DES-025 (error) Pin '%s' is not connected to net '%s'. Ignoring annotation on net '%s'.

DESCRIPTION

You receive this message if the **read_parasitics** command has found the specified pin in the parasitics file but not in the design file; therefore, **read_parasitics** cannot annotate the associated net. Possible causes for this error could include spelling errors or typos, or writing the parasitics file and the design file from different versions of the design.

WHAT NEXT

Verify that the specified pin is connected to the specified net in both the parasitics file and the design file, and that both are spelled correctly. Regenerate the files if necessary, then reexecute **read_parasitics**.

SEE ALSO

read_parasitics (2).

DES-026 (error) %s pin '%s' is not connected to the RC network of

net '%s'. Ignoring the incomplete RC network of the net.

DESCRIPTION

You receive this message if **report_annotated_parasitics** detects an incompletely back-annotated RC network in the current design. The message informs you that the RC network on the specified net is being ignored, because it is incomplete; the specified pin is not physically connected to the RC network.

An incomplete RC network might be caused by errors in the parasitics file, or by missing information from the tool that generated the parasitics file. For example, a parasitics file generated by a place and route tool that has parasitics only for the top level (between the blocks) would generate this error, because PrimeTime requires the RC network to connect all leaf drivers to all leaf nodes.

WHAT NEXT

Examine the SPF or SPEF file to determine why the specified RC network is incomplete. If the error is caused by a valid incomplete network, you can complete it using the parasitics completion feature **read_parasitics -complete_with** or **complete_net_parasitics**. For other errors, you must correct the parasitics file manually. You might need to estimate the missing segments and manually add them. After you have corrected the SPF or SPEF file, reexecute **read_parasitics**.

To determine whether the parasitics file contains a valid incomplete RC network, start from a driver and try to reach all loads through resistances. If all missing segments of a net are between two pins, you can complete them using the parasitics completion feature; otherwise, you must correct the SPF or SPEF file manually.

SEE ALSO

complete_net_parasitics (2), **read_parasitics** (2), **report_annotated_parasitics** (2).

DES-027 (warning) net '%s' has too many (%d) RC elements. Lumped capacitance is used.

DESCRIPTION

The specified net has too many RC elements (more than 10,000). RC delay calculation using AWE technique cannot handle such large RC networks.

WHAT NEXT

The very large RC network of the net needs to be reduced to a smaller number of RC elements to be handled by PrimeTime.

DES-028 (info) Derived library resistance unit is %f Kohm (Time unit is %.f ns, and Capacitance unit is %f pF).

DESCRIPTION

The library resistance unit is implicit in the synopsys library, it is derived from the library time and capacitance units which are explicit.

WHAT NEXT

DES-029 (error) Library '%s' has no voltage rails defined.

DESCRIPTION

An attempt was made to define rail voltages to a library which does not have defined rail voltages. It is usually because the library is not a DPCM library, or that the DPCM library does not have pre-defined rail voltages.

WHAT NEXT

DES-030 (error) cannot find rail voltage '%s' in library '%s'.

DESCRIPTION

The specified rail voltage is not declared in the DPCM library. It may be because of a typo.

WHAT NEXT

Report the specified rail voltage names specified in the DPCM library by executing command report_lib for the specified library. report_lib reports all specified rail voltage names declared in DPCM.

DES-031 (error) Upper threshold must be greater than lower threshold for variables rc_slew_lower_threshold_pct_* and

rc_slew_upper_threshold_pct_*.

DESCRIPTION

The variable rc_slew_upper_threshold_pct_rise must be strictly greater than rc_slew_lower_threshold_pct_rise. Similarly, variables rc_slew_upper_threshold_pct_fall must be strictly greater than rc_slew_lower_threshold_pct_fall.

WHAT NEXT

Set variables rc_slew_lower_threshold_pct_rise, rc_slew_upper_threshold_pct_rise, rc_slew_lower_threshold_pct_fall, rc_slew_upper_threshold_pct_fall.

DES-032 (warning) Failed to compute %s RC net delay from '%s' to '%s'.

DESCRIPTION

The delay calculation failed to compute the delay for the given detailed RC network, hence the lump model will be used for delay calculation.

WHAT NEXT

Simplify the RC network and check if the RC enviorment vairables are set correctly.

DES-033 (warning) Failed to compute C-effective for the following timing arc:
(%s) %s/%s-->%s (%s %s)

DESCRIPTION

The cell delay calculation failed to compute the effective capacitance of the detailed RC network driven by a specific timing arc, so the total capacitance will be used.

The two most common reasons for this failure are (1) an unrealistically large input transition time or output capacitance has occurred, and/or (2) the RC threshold environment variables are set incorrectly.

Another frequent reason is that library data for the specific sense of timing arc in question is missing or invalid. The timing arc is displayed by the warning message

in the following manner:

(<reference-name>) <instance-name>/<from-pin>--><to-pin> (<sense-name>)

The sense name has two parts: a rising/falling direction on the to-pin and a sense description.

WHAT NEXT

You may have to annotate transition times with **set_annotated_transition** to circumvent unrealistic loading conditions (e.g. like those which you might later solve with buffer trees). Also, be sure the RC threshold environment variables are set correctly, and that valid library data exists for the desired sense of timing arc through the cell of interest.

SEE ALSO

set_annotated_transition (2), **rc_slew_lower_threshold_pct_rise** (3), **rc_slew_lower_threshold_pct_fall** (3), **rc_slew_upper_threshold_pct_rise** (3), **rc_slew_upper_threshold_pct_fall** (3), **rc_input_threshold_pct_rise** (3), **rc_input_threshold_pct_fall** (3), **rc_output_threshold_pct_rise** (3), **rc_output_threshold_pct_fall** (3), **rc_slew_derate_from_library** (3).

DES-034 (warning) subckt '%s' defined multiple times.

DESCRIPTION

The SPICE deck and all its include files that define the pin order for the SPICE output of the critical has define a sub-circuit multiple times.

DES-035 (error) out of memory at file %s line %d.

DESCRIPTION

Run out of memory during SPICE pin order deck parsing.

DES-036 (warning) pin '%s defined multiple times in subckt '%s'.

DESCRIPTION

A pin is defined multiple time on the SPICE subckt header. Only the first one is used.

DES-037 (warning) No SPICE pin order info for cell '%s' (%s).

DESCRIPTION

You receive this message if **write_spice_deck** cannot find the specified cell type in the file you specified using the **-sub_circuit_file** option.

WHAT NEXT

Examine the subcircuit file and verify that it contains the subcircuit description of the specified library cell. Make any corrections necessary, then re-execute **write_spice_deck**.

DES-038 (error) Library pin '%s' for cell '%s' is not in the SPICE sub-circuit definition.

DESCRIPTION

You receive this message if **write_spice_deck** finds the specified cell in the file you specified using the **-sub_circuit_file** option, but does not find the specified pin.

WHAT NEXT

Examine the subcircuit file and verify that it contains the specified pin and is consistent with the PrimeTime library. Make any corrections necessary, then re-execute **write_spice_deck**.

DES-039 (warning) SPICE pin '%s' for cell '%s' is not in the library.

DESCRIPTION

You receive this message if **write_spice_deck** finds the specified pin in the subcircuit file but cannot find it in the library. If the pin is a power or ground pin, PrimeTime might still be able to do the analysis.

WHAT NEXT

If the pin is not a power or ground pin, examine the subcircuit file and verify that it is consistent with the PrimeTime library. Make any corrections necessary, then re-execute **write_spice_deck**.

DES-040 (warning) The driver waveform %s is bad and will be ignored.

DESCRIPTION

While reading the driver waveform, the application found that waveform is bad. For example, the number of voltage points in the waveform are less than two.

WHAT NEXT

Examine your waveform is according to the liberty syntax for driver waveforms. Correct the waveform and re-execute it.

DES-050 (error) Too many %ss matched '%s' in design '%s'

DESCRIPTION

While searching for an object by name, the application found multiple objects that match the name. This usually occurs after some flattening of the design, when the hierarchy character becomes embedded in the names. For backannotation, this is an ambiguous situation, because the application cannot determine which object to annotate.

This situation occurs rarely, during the reading of parasitics files, and could be caused by a design error. Multiple objects in the flat space should not have the same name.

WHAT NEXT

Examine your design to determine why multiple objects in the flattened file have the same name. Correct the design, then re-execute the application.

DES-051 (Error) Command requires a linked design but linking is blocked because auto_link_disable is TRUE.

DESCRIPTION

You receive this message if you execute a command that requires a linked design, your design is not linked, and the **auto_link_disable** variable is set to true. By default, many PrimeTime commands automatically attempt to link the current design for you (for example, **set_load** invokes the linker if the current design is not

linked). Setting **auto_link_disable** to true disables the default auto-link process.

WHAT NEXT

If you intend for auto linking to be disabled, you must link the design manually before executing any commands that require a linked design. Setting **auto_link_disable** to true is intended to be used in conjunction with a manual link step. For more information, see the manual page for the **auto_link_disable** variable.

Alternatively, if you want to enable auto linking, set the **auto_link_disable** variable to false.

DES-060 (warning) Ignoring retain library timing arc from '%s' to '%s'.

DESCRIPTION

You receive this message if the current library DB is out of date. Retain arcs generated by Library Compiler prior to version 2000.11 are not supported.

WHAT NEXT

Use Library Compiler to regenerate your library DB. Follow these steps:

1. Read in the .lib file.

```
dc_shell> read_lib mylibrary.lib
```

2. Write out the .db file.

```
dc_shell> write mylibrary.db
```

DES-061 (warning) Found duplicate instantiation of cell '%s' when flattening the hierarchical netlist.

DESCRIPTION

You receive this message while outputting a hierarchical netlist in a flattened manner. When flattening the netlist, two instances are being mapped to same name. For example, you may have a cell by name "a/b" at top level and a cell named "b" inside a hierachy named "a". The name of the cell under conflict is given in this message.

WHAT NEXT

You should uniquify the names of the cells under conflict before doing the current operation.

DES-062 (warning) '%s' unit specified as '%s' does not match with the main library unit '%s%s'.

DESCRIPTION

set_units command can only check the consistency of the specified units with the main library units. Actual setting of units are not allowed.

WHAT NEXT

If the units of sdc scripts are different, change the sdc scripts so that the units are same as the main library units. It is also possible to select a different library as the main library, which has consistent units as that of sdc scripts.

DES-063 (warning) '%s' unit should be specified in '%s'.

DESCRIPTION

.

WHAT NEXT

.

DES-064 (warning) Power unit cannot be checked.

DESCRIPTION

Power unit cannot be checked since no power unit available.

WHAT NEXT

Enable power analysis mode by setting power_enable_analysis to true, and running power related commands, such as update_power, read_vcd, read_saif, set_switching_activity, etc.

DES-065 (warning) ’%c’ is an unsupported scale.

DESCRIPTION

Valid scales are f|p|n|u|m|k|M.

WHAT NEXT

Scale the value to the supported scale.

DES-066 (error) Command requires a linked design but linking is blocked
because of existing collections.

DESCRIPTION

You receive this message if you execute a command that requires a linked design, your design is not linked, and there are some collections with this design.

WHAT NEXT

Perform a link first and re-issue the command.

DES-067 (error) Design is already linked.

DESCRIPTION

You are attempting to link a design that is already fully linked. If you want PT to relink, please use -force option.

WHAT NEXT

No need of any action.

DES-068 (error) Could not find library cell ’%s’.

DESCRIPTION

You are attempting to use a library cell in a command and the library cell could not

be located in any of the loaded libraries.

WHAT NEXT

Re-issue the command with the correct library cell.

DFI

DFI-1 (error) Could not open viewpoint ’%s’

DESCRIPTION

WHAT NEXT

DFI-2 (error) Error in traversing design viewpoint ’%s’

DESCRIPTION

WHAT NEXT

DFI-3 (error) Could not find referenced design for instance ’%s’

DESCRIPTION

WHAT NEXT

DFI-4 (error) Could not add design ’%s’

DESCRIPTION

WHAT NEXT

DFI-5 (error) Could not add port ’%s’ for design ’%s’

DESCRIPTION

WHAT NEXT

DFI-6 (error) Could not add instance ’%s’ for design ’%s’

DESCRIPTION

WHAT NEXT

DFI-7 (warning) Design ’%s’ contains no instance

DESCRIPTION

WHAT NEXT

DFI-8 (warning) Both ’%s’ and ’%s’ has the same design name ’%s’

DESCRIPTION

WHAT NEXT

DFI-9 (warning) Design in path ’%s’ is renamed to ’%s’

DESCRIPTION

WHAT NEXT

DFI-10 (warning) Property ’%s’ is not visible, port will have

unknown direction

DESCRIPTION

WHAT NEXT

DFI-11 (warning) Property ’%s’ for ’%s’ is not visible

DESCRIPTION

WHAT NEXT

DFI-12 (error) Can’t connect pin ’%s’ of instance ’%s’

DESCRIPTION

WHAT NEXT

DFI-13 (error) Could not find referenced design ’%s’

DESCRIPTION

WHAT NEXT

DFI-14 (error) Bus ’%s’ contains ports of different types

DESCRIPTION

WHAT NEXT

DFI-15 (error) Can’t add bus ’%s’

DESCRIPTION

WHAT NEXT

DFI-16 (error) Can’t write ’%s’ db file

DESCRIPTION

WHAT NEXT

DFI-17 (error) Port ’%s’ is missing in the interface of design ’%s’

DESCRIPTION

WHAT NEXT

DFI-18 (error) Can’t connect ’%s’ to ’%s’ net

DESCRIPTION

WHAT NEXT

DFI-19 (warning) Could not add bus port ’%s’ for design ’%s’ because %s

DESCRIPTION

WHAT NEXT

DFTSCHD

```
### DFTSCHD-001.n ###
```

DFTSCHD-001 (warning) No schematic support for DFT violation (%s).

DESCRIPTION

```
Check the man page for %s DRC violation.
```

DMWDB-1 (warning) Milkyway database does not contain hierarchy information.

DESCRIPTION

There is no hierarchy information in the Milkyway database. DEF/PDEF uses this info to decide if the hierarchy delimiter (usually ’/’) contained in the instance name needs to be escaped or not, as different inputs source might use different approaches. Consequently, DEF/PDEF will use the full name in the database, which might not be escaped correctly.

WHAT NEXT

If you do not use the special hierarchy character ’/’ in the instance name, you can ignore this message. Otherwise, you need to consider to preserve the hierarchy in the flow.

See Also

write_pdef (2) write_def (2)

DP

DP-1 (information) Datapath optimization is enabled.

DESCRIPTION

This message informs you that datapath optimization is enabled (the default).

WHAT NEXT

This an informational message only. No action is required.

SEE ALSO

DP-2 (error) You have requested datapath optimization but the DesignWare license is not accessible.

DESCRIPTION

This error message occurs when the the DesignWare or DesignWare-Foundation-Ultra license is not accessible. A license is required in order to enable built-in datapath optimization in the **compile** command.

WHAT NEXT

You can either obtain a DesignWare license, or disable datapath optimization by setting the **hlo_disable_datapath_optimization** DC variable to *true*.

SEE ALSO

hlo_disable_datapath_optimization(3)

DP-3 (information) Datapath optimization is limited for '%s'.

DESCRIPTION

This message notifies you that limited datapath optimization is enabled in the **compile** flow when the **set_datapath_optimization_effort** command has set the datapath_optimization_effort attribute to **medium** or **low** for the specified design or instance.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

compile(2)
compile_ultra(2)
set_datapath_optimization_effort(2)
set_ultra_optimization(2)
hlo_disable_datapath_optimization(3)

DP-4 (warning) '%s' is an invalid argument for variable/attribute '%s'.

DESCRIPTION

This warning message occurs when an invalid argument is set for the specified variable or attribute. The valid arguments are as follows:

- all - to duplicate all common subexpression (cse) in datapath block
- critical - to duplicate only common subexpressions on critical paths
- none - no cse duplication.

WHAT NEXT

The current common subexpression duplication is reset to **none**. If this is not what you intended, reset to another valid argument.

SEE ALSO

compile_ultra(2)
set_ultra_optimization(2)
hlo_datapath_duplicate_cse(3)
hlo_datapath_optimization(3)

DP-5 (warning) The duplicate_csa and dont_duplicate_csa

attributes are not supported in the built-in datapath optimization.

DESCRIPTION

This warning message occurs when the **duplicate_csa** or **dont_duplicate_csa** attributes are set. These attributes are not supported in the built-in datapath optimization function of the **compile** command. The attributes are ignored in the current datapath flow.

WHAT NEXT

This is only a warning message and no action is required. However, if you want to selectively set common subexpression (cse) duplication on particular design blocks, set the following attribute on the designs:

```
set_attribute design_list "datapath_duplicate_cse" <plain
[none | critical | all]
```

SEE ALSO

compile_ultra(2)
set_ultra_optimization(2)
hlo_datapath_duplicate_cse(3)
hlo_disable_datapath_optimization(3)

DP-6 (warning): Missing datapath expression on datapath cell '%s'.

DESCRIPTION

This warning message occurs when the tool encounters a datapath cell with missing expressions. Implementation selection is disabled on this cell to avoid expected behavior. This may result in less optimal QoR for the datapath block.

The datapath expression is removed if the datapath design is modified by other command, e.g. remove_unconnected_ports.

WHAT NEXT

Do not modify the datapath design if you want the datapath to be regenerated.

SEE ALSO

compile_ultra(2)
set_ultra_optimization(2)
hlo_disable_datapath_optimization(3)

DP-7 (warning) Internal error: Missing datapath common subexpression on datapath cell '%s'.

DESCRIPTION

This warning message occurs when you encounter an internal error that results in missing the datapath common subexpressions for the current DP cell.

WHAT NEXT

Submit a testcase that reproduces the problem to the Synopsys Customer Support Center by using Enter A Call at http://solvnet.synopsys.com/EnterACall.

SEE ALSO

compile_ultra(2)
set_ultra_optimization(2)
hlo_disable_datapath_optimization(3)

DP-8 (warning) Datapath cell '%s' will be skipped during implementation selection due to missing expressions.

DESCRIPTION

This warning message occurs when the tool encounters a datapath cell with missing expressions. Implementation selection is disabled on this cell to avoid expected behavior. This may result in less optimal QoR for the datapath block.

WHAT NEXT

Do not modify the datapath design if you want the datapath to be regenerated.

SEE ALSO

compile_ultra(2)
set_ultra_optimization(2)
hlo_disable_datapath_optimization(3)

DPB-001 (error) No design %s.

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command before loading the design. Please load the design before running the budgeting command.

WHAT NEXT

Please load the design by reading verilog or loading Milkyway database. command.

SEE ALSO

allocate_fp_budgets(2), **check_fp_timing_environment**(2),

DPB-002 (error) No DC Design.

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command without linking the design.

WHAT NEXT

Please run the *link* command to link the design. If you have already run *link* command, please check if there were any errors during linking.

SEE ALSO

allocate_fp_budgets(2), **check_fp_timing_environment**(2),

DPB-003 (error) No master or instance name defined in the file format spec. The file format spec should be <directory>/<m/

i>.<extension>.

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command with incorrect -*file_format_spec* option. Please note format of the option and provide -*file_format_spec* option again.

WHAT NEXT

Please change the file format spec given in -*file_format_spec* option by calling *allocate_fp_budgets* command again. It accepts <directory>/<m/i>.<extension>, where <directory>: Name of the output directory, where SDC files are created <m/i>: Whether to use instance name or master of the block <extension>: Suffix of the SDC files

SEE ALSO

allocate_fp_budgets(2)

DPB-004 (warning) There are no hierarchical pin locations. Please run analyze routing by running "analyze_fp_routing

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command without running the Pin Cutting Flow. If the design has plan groups, and the plan groups have no pins assigned, then you will receive this message.

WHAT NEXT

Please run the Pin Cutting Flow to have the pins assgined on the plan groups. Running Pin Cutting Flow will improve the QoR of the Budgeter.

SEE ALSO

allocate_fp_budgets(2)

DPB-005 (error) Can not attach a file to the CEL.

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command and the Budgeter is unable to create budgeting information.

WHAT NEXT

Please check the disk space on the design directory.

SEE ALSO

allocate_fp_budgets(2)

DPB-006 (error) Budgeting has not been run.

DESCRIPTION

You received this message when you run *check_fp_budget_result* command without running *allocate_fp_budgets* command before. The *check_fp_budget_result* will only work if *allocate_fp_budgets* command has been run before in the same ICC session.

WHAT NEXT

Please run the Budgeter by calling *allocate_fp_budgets* command, before calling *check_fp_budget_result* command.

SEE ALSO

allocate_fp_budgets(2), **check_fp_budget_result**(2)

DPB-007 (warning) -blocks and -pins options are mutually exclusive.
-blocks option will be ignored.

DESCRIPTION

You received this message when you run *check_fp_budget_result* command with both *-blocks* and *-pins* options. These two options are mutually exclusive.

WHAT NEXT

Please use either *-blocks* or *-pins* option to *check_fp_budget_result* command.

SEE ALSO

check_fp_budget_result(2)

DPB-008 (error) No file name is provided.

DESCRIPTION

You received this message when you run *check_fp_budget_result* command without *-file_name* option. The file option is the location of the output of *check_fp_budget_result* command.

WHAT NEXT

Please provide the file name by providing *-file_name* option to *check_fp_budget_result* command.

SEE ALSO

check_fp_budget_result(2)

DPB-009 (error) Cannot open file %s.

DESCRIPTION

You received this message when you run *check_fp_budget_result* command and the command is unable to open the file provided in *-file_name* option.

WHAT NEXT

Please check the disk space and permssions of file provided in *-file_name* option.

SEE ALSO

check_fp_budget_result(2)

DPB-010 (warning) No option to check_timing_environment has

been specified. No report file will be generated.

DESCRIPTION

You received this message when you run *check_fp_timing_environment* command with no vaild options. No Check Timing report file will generated.

WHAT NEXT

Please check the syntax of the *check_fp_timing_environment* command. Please correct the errors on the command-line options.

SEE ALSO

check_fp_timing_environment(2)

DPB-011 (warning) Cannot find budgeted %s cell for cell '%s'.

DESCRIPTION

You received this message when you run *check_fp_timing_environment* command and the tool is unable to locate a plan group in the design.

WHAT NEXT

Please check if the link has been called before calling the *check_fp_timing_environment* command. Please check if there are any errors in the log file, before calling *check_fp_timing_environment* command.

SEE ALSO

check_fp_timing_environment(2)

DPB-012 (warning) The command fp_allocate_budgets is obsolete. Please use allocate_fp_budgets instead.

DESCRIPTION

You received this message when you run *fp_allocate_budgets* command. This command is obsolete and has been replaced by *allocate_fp_budgets* command. The *allocate_fp_budgets* command has exactly the same options as *fp_allocate_budgets* command. The *fp_allocate_budgets* may be removed in the future release of IC

Compiler.

WHAT NEXT

Please use the *allocate_fp_budgets* command, instead of *fp_allocate_budgets* command.

SEE ALSO

allocate_fp_budgets(2)

DPB-013 (error) Must specify one of '%s', '%s' or '%s' Check Timing Environment GUI options.

DESCRIPTION

You received this message when you run the Check Timing Environment GUI, with more than one of the three mutually exclusive options. The Check Timing Environment GUI has exited.

WHAT NEXT

Please call Check Timing Environment GUI with one out of the three options, at one time.

SEE ALSO

check_fp_timing_environment(2)

DPB-014 (warning) No source latency info stored by CP on pin %s.

DESCRIPTION

You receive this message when you run budgeting after clock planning and the clock source latency information for the blocks cannot be retrieved by budgeting.

WHAT NEXT

Please re-run clock planning to synthesize all the clocks. If you run clock planning with the option to keep the clock trees in the blocks, please use **set synthesized_clocks true** before budgeting.

SEE ALSO

allocate_fp_budgets(2)

DPB-015 (warning) No network latency info stored by CP on pin %s.

DESCRIPTION

You receive this message when you run budgeting after clock planning and the clock network latency information for the blocks cannot be retrieved by budgeting.

WHAT NEXT

Please re-run clock planning to synthesize all the clocks. If you run clock planning with the option to keep the clock trees in the blocks, please use **set synthesized_clocks true** before budgeting.

SEE ALSO

allocate_fp_budgets(2)

DPB-016 (warning) No anchor cell found for clock source %s.

DESCRIPTION

You receive this message when you run budgeting after clock planning and there is a clock source in a block that does not have an anchor cell inserted after it.

WHAT NEXT

Please re-run clock planning to synthesize all the clocks. Please check that the clock nets do not have dont_touch attribute defined on them. If you run clock planning with the option to keep the clock trees in the blocks, please use **set synthesized_clocks true** before budgeting.

SEE ALSO

allocate_fp_budgets(2)

DPB-017 (error) Cannot open CEL %s for write.

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command on a design with ILMs, and the CEL views corresponding to the ILMs cannot be opened for write. In this cases the budgeted timing constraints cannot be stored with the CEL view.

WHAT NEXT

Please check your milkyway library to make sure that your CEL views are not marked read-only.

SEE ALSO

allocate_fp_budgets(2)

DPB-018 (error) Cannot find CEL %s.

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command on a design with ILMs, and the CEL views corresponding to the ILMs cannot be found. In this cases the budgeted timing constraints cannot be stored with the CEL view.

WHAT NEXT

Please check your milkyway library to make sure that it contains the CEL views corresponding to the ILMs.

SEE ALSO

allocate_fp_budgets(2)

DPB-019 (warning) There are propagated and non-propagated clocks co-existing in the design.

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command on a design with both propagated and non-propagated clocks. In this case, the budgeted input/output delays might not be accurate enough for block implementation.

WHAT NEXT

Please check top level SDC constraints. If you are calling the *allocate_fp_budgets* command before clock tree synthesis, it is recommended not to have propagated clocks in the top level SDC as it would give unrealistic clock latency numbers. If you are calling *allocate_fp_budgets* command after clock tree synthesis, please set *synthesized_clock* variable to true.

SEE ALSO

allocate_fp_budgets(2) **set_propagated_clock**(2) **remove_propagated_clock**(2)

DPB-020 (warning) Pin %s is not a block pin.

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command with the option -fixed_delay_objects, and the specified pin you passed through the option is not a block pin. In this case, this pin is not considered by the command as fixed delay pin.

WHAT NEXT

Check if the pin name is correctly given in the command line.

SEE ALSO

allocate_fp_budgets(2)

DPB-021 (warning) Pin %s has too much fixed delay on path from %s to %s.

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command. The tool issues this warning message when it detects too much fixed delay in a path and there is no room to budget the adjustable delays.

WHAT NEXT

Check if there are too many pins/blocks/cells specified as fixed delay objects. If so, try to see if some of them can be removed. If not, and if you are running incremental budgeting, it means the block implementations are having a hard time to meet timing. It might be hard to meet top level timing closure.

SEE ALSO

allocate_fp_budgets(2)

DPB-022 (error) Incremental budgeting stopped because there is no ILM pin with block level timing violation.

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command with -incremental option. The tool issues this error message when it detects no pin of any ILM blocks in the design has timing violation at the block level when ILM model for the block was created. Then incremental budgeting stops.

WHAT NEXT

Check if all the block pins meet timing when ILM for the block is created. If there is no interface path violation, there is no need to run incremental mode budgeting. If there is interface path violation when the ILM is created, check if the ILM is created using IC Compiler release 2009.06 or later.

SEE ALSO

allocate_fp_budgets(2)

DPB-023 (info) Incremental budgeting found critical pin %s.

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command with -incremental option. The tool issues this informational message when it finds a pin on an ILM block that was hard to meet timing at the block level.

WHAT NEXT

Too many critical pins can cause budgeting to over-constrain the related blocks.

SEE ALSO

allocate_fp_budgets(2)

DPB-024 (info) Time given to startpoint %s is %.6f(r) and %.6f(f) for block pin %s.

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command with the variable jtb_print_time_borrowing_info set to true. The tool issues this informational message when it finds that a path used to calculate the input delay of the specified block pin starts from a transparent latch and that time borrowing is not zero at this latch.

WHAT NEXT

SEE ALSO

allocate_fp_budgets(2)

DPB-025 (info) Time borrowed from endpoint %s is %.6f(r) and %.6f(f) for block pin %s.

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command with the variable jtb_print_time_borrowing_info set to true. The tool issues this informational message when it finds that a path used to calculate the output delay of the specified block pin ends in a transparent latch and that time borrowing is not zero at this latch.

WHAT NEXT

SEE ALSO

allocate_fp_budgets(2)

DPB-026 (info) Budgets on pin %s may be tightened.

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command with the option -incremental. The tool issues this informational message when it finds that a budgeting block pin’s budget is affected by the critical pins the tool identified

automatically. If options -fixed_delay_objects and/or -no_interblock_logic is also specified, this message could mean that the pin's budget is affected by the objects given in the options.

WHAT NEXT

This is a informational message. No action needed.

SEE ALSO

allocate_fp_budgets(2)

DPB-027 (info) Fixed delays on path from %s to %s are changed to adjustable to calculate input/output delay for pin %s.

DESCRIPTION

You received this message when you run *allocate_fp_budgets* command with the option -incremental. The tool prints this informational message when it decides to ignore some fixed delays in the design and treat them as adjustable delays to calculate the input/output delay for the specified pin. This happens when the tool finds too much fixed delay in the specified path and there is no room to budget the adjustable delays.

WHAT NEXT

Check if there are too many pins/blocks/cells specified as fixed delay objects. If so, try to see if some of them can be removed. If not, it means the block implementations are having a hard time to meet timing. It might be hard to meet top level timing closure.

SEE ALSO

allocate_fp_budgets(2)

DPB-028 (warning) The variable synthesized_clocks is true. The setting of the variable virtual_clocks_from_cp will be adjusted to false.

DESCRIPTION

You receive this message when you run *allocate_fp_budgets* command, using both

set synthesized_clocks true

and

set virtual_clocks_from_cp false

WHAT NEXT

If your design has fully synthesized clocks and you do not want separate virtual clocks created to capture the latency, use *set synthesized_clocks false*. If you have run clock planning but do not have fully synthesized clocks use *set virtual_clocks_from_cp false* to turn off the virtual clock generation.

SEE ALSO

allocate_fp_budgets(2) **virtual_clocks_from_cp**(3) **synthesized_clocks**(3)

DPB-029 (warning) No master instance is specified for MIM master %s.

DESCRIPTION

You receive this message when you run *allocate_fp_budgets* command on a design with MIM (multiply instantiated module) plan groups or soft macros, and you didn't select a master instance using the *select_mim_master_instance* command for the specified MIM master.

WHAT NEXT

allocate_fp_budgets command will automatically select a master instance for this MIM set. If you want to choose your own master instance, please run *select_mim_master_instance* and re-run *allocate_fp_budgets* after that.

SEE ALSO

allocate_fp_budgets(2) **select_mim_master_instance**(2)

DPB-030 (warning) %s is set as master instance for MIM master %s.

DESCRIPTION

You receive this message when you run *allocate_fp_budgets* command on a design with

MIM (multiply instantiated module) plan groups or soft macros, and you didn't select a master instance using the *select_mim_master_instance* command.

WHAT NEXT

allocate_fp_budgets command will automatically select the specified instance as master instance for the specified MIM set. If you want to choose your own master instance, please run *select_mim_master_instance* and re-run *allocate_fp_budgets* after that.

SEE ALSO

allocate_fp_budgets(2) **select_mim_master_instance**(2)

DPB-031 (warning) MIM cell %s is not specified with -cells option.

DESCRIPTION

You receive this message when you run *allocate_fp_budgets* command on a design with MIM (multiply instantiated module) plan groups or soft macros, and you specified the cells to budget using the option *-cells*, but the cells you specified covers part but not all the instantiations of a MIM set.

WHAT NEXT

If you want *allocate_fp_budgets* command to generate a single merged SDC file for a set of MIM in the design, please include all the instantiated instances with the option *-cell*. You can also not using the *-cell* option, and let *allocate_fp_budgets* command to find and budget all the cells.

SEE ALSO

allocate_fp_budgets(2)

DPI-001 (information) All of the movable filler cells will be removed!

DESCRIPTION

This message indicates that ICC detail placer has detected that there are some movable filler cells inside this design while performing the detail placement. ICC detail placer will remove all of the movable filler cells and perform the detail placement. Later on, Users need to insert filler cells again.

WHAT_NEXT

DPI-002 (warning) Cell %s is violating "Via-Spacing" Rule.

DESCRIPTION

This warning informs you that the named cell is violating the "Via-Spacing" rule in the design. The placement of the cell is not valid.

WHAT NEXT

To make the placement valid, use the **legalize_placement** command.

SEE ALSO

legalize_placement (2).

DPI-003 (error) The input scan chain %s is broken between pin %s and pin %s, which come from different logical hiearchies!

DESCRIPTION

This message indicates that ICC has detected that the input scan chain is brokenbetween two different logical hierarchies. Command connect_dft_eco can not support this.

WHAT_NEXT

Users need to make sure that the scan chain is not broken between two different logical hierarchy boundaries.

DPI-004 (error) NO SCAN_IN/SCAN_OUT pin for scan chain %s!

DESCRIPTION

This message indicates that ICC can not find the SCAN_IN/SCAN_OUT pins for the given scan chain. Command connect_dft_eco requires that both SCAN_IN pin and SCAN_OUT pin should be present for a scan chain.

WHAT_NEXT

User needs to double check the scan chain data, and make sure that both SCAN_IN and SCAN_OUT pins are present.

DPI-005 (error) new scan cell %s does not belong to the logical hierarchy which the input scan chain %s resides. Therefore this new cell will not be added into the scan chain!

DESCRIPTION

This message indicates that command connect_dft_eco has detected that the new cell does not belong to the logical hiearchy where the scan chain resides. Therefore, this new cell can not be added into the given scan chain.

WHAT_NEXT

Command connect_dft_eco can support this situation at this moment. Users need to use other way to add this new cell into the scan chain.

DPI-006 (error) skip scan chain %s since it has some errors.

Command connect_dft_eco failed!

DESCRIPTION

This message indicates that command connect_dft_eco has detected that the input scan chain has some errors, and commnad connect_dft_eco can not proceed.

WHAT_NEXT

Users need to fix the input scan chain problem before they run command connect_dft_eco.

DPI-007 (information) pin %s was disconnected during ECO reconnection operation!

DESCRIPTION

This message indicates that command connect_dft_eco has disconnected this pin because it will be connected to a different scan cell which is inside the SCANDEF. By default, command connect_dft_eco will reconnect the scan chain based on the scan cell order which is from SCANDEF. You are seeing this message may also because of the fact that with some new cells being added into the scan chain, some existing connection will be disconnected and reconnected to some different cells.

WHAT_NEXT

If users want to control the order of the scan chain after this command, users can update their SCANDEF with the desired order before they run command connect_dft_eco.

DPI-008 (information) skip net %s (connecting to port %s) because the net is dont_touch!

DESCRIPTION

This message indicates that command insert_port_protection_diodes can not add port_protection_diode cell to the net because this net is a "dont_touch" net.

WHAT_NEXT

Double-check the net/port settting, remove the dont_touch attribute before you want to use command insert_port_protection_diodes to add port_protection_diodes to this net/port.

DPI-009 (warning) port %s has already connected to one port_protection_diode %s!

DESCRIPTION

This message indicates that command insert_port_protection_diodes has detected that this port has connected to at least one port_protection_diode already.

WHAT_NEXT

There may be a chance that users have added multiple port_protection_diodes for the same port by mistake. Although command insert_port_protection_diodes is issuing this warning message, it will still insert a new port_protection_diode for this port. However, users need to double-check the port_protection_diode creatation for this port.

DPI-010 (information) port %s is not connecting to any port_protection_diode!

DESCRIPTION

This message indicates that command report_port_protection_diodes has detected that this port is not connecting to any port_protection_diode.

WHAT_NEXT

One port_protection_diode may need to be added for this port since it does not have any. Users can use command insert_port_protection_diodes to do so.

DPI-011 (Error) %s

DESCRIPTION

This is a general message indicates that some errors are happenning during the current command execution.

WHAT_NEXT

Correct the error, and try again.

DPI-012 (Error) %s

DESCRIPTION

This is a general internal error message indicates that some internal errors are happenning during the current command execution. Please pay attention to the detail message.

WHAT_NEXT

Correct the error, and try again.

DPI-013 (warning) port %s is connecting to multiple port_protection_diodes %s !

DESCRIPTION

This message indicates that command report_port_protection_diodes has detected that this port has connected to at least two port_protection_diode already.

WHAT_NEXT

There may be a chance that users have added multiple port_protection_diodes for the same port by mistake. Users may need to double-check the port_protection_diode creatation for this port.

DPI-014 (warning) port_protection_diode %s is not connecting to any port!

DESCRIPTION

This message indicates that command report_port_protection_diodes has detected that this port_protection_diode does not connect to any port. It is expected that one port_protection_diode should connect to one port. However this port_protection_diode does not.

WHAT_NEXT

There may be a chance that users have added some new logic in between the port_protection_diode and the port which the diode should protect. Users may need to double-check the connection of the port_protection_diode and take some proper action for this.

DPI-015 (information) %d port_protection_diodes have been added, legalized and marked as FIXED!

DESCRIPTION

This message indicates that command insert_port_protection_diodes has added some port_protection_diodes into the netlist. Moreover, the newly added port_protection_diodes have been legalized and marked as FIXED.

WHAT_NEXT

This message indicates that command insert_port_protection_diodes has added some new port_protection_diodes into the design.

DPI-016 (error) Can not find any proper driver for all the specified ECO cells!

DESCRIPTION

This message indicates that command derive_eco_cell_locations can not find any proper driver cell which are driving the specified "ECO cells" when the "-driver_neighbour" has been specified. This message may indicate that there is an issue with the specified "ECO cells": they may not have any connection, or may not connect to any proper driver.

WHAT_NEXT

Users need to double-check the connectivity of the specified "ECO cells", make sure that there are some proper driver cells which are connecting to the ECO cells when "-driver_neighbour" has been specified.

DPI-017 (error) The specified library cell %s has a problem and can not be added into the current design!

DESCRIPTION

This message indicates that command insert_port_protection_diodes has detected that the specified library cell is not the correct type of library cell which may not match the current operating condition or current voltage area specification. In addition, there is also a chance that this user-specified library cell has been marked as "dont_use" with the library setting.

This message may indicate that there is an issue with the specified library cell.

WHAT_NEXT

There may be multiple types of library cells inside different target libraries, yet they have the same library cell name. Users need to double-check the specified library cell, make sure that the specifed library cell match the current operating condition and voltage area specification (P, V, T). In addition, the user needs to double-check whether this library has a "dont_use" marking with the current library setting.

DPI-018 (information) a port protection diode has been added into net %s which is only connecting to port %s !

DESCRIPTION

This message indicates that command insert_port_protection_diodes has detected that the specified port is the only connection of the net. However, a port protection diode is still being inserted into such a net. This message may indicate that the user need to check the specified ports.

WHAT_NEXT

User may need to check their specified ports, and make sure that a port protection diode needs to be added even though the port is the only connection of the corresponding net.

DPI-019 (information) "Treat %s as physical-only since it has IS_PHYSICAL_ONLY flag!"

DESCRIPTION

This message indicates that the above cell instance will be treated as "physical-only" cells due to the IS_PHYSICAL_ONLY flag.

WHAT_NEXT

DPI-020 (information) "Treat %s as physical-only since it has no

signal connection!"

DESCRIPTION

This message indicates that the above cell instance will be treated as "physical-only" cells because it has no signal connection.

WHAT_NEXT

Check your design and make sure the netlist is correct.

DPI-100 (Error) This design does not have floorplan.

DESCRIPTION

The command insert_spare_cells require designs to have floorplan to continue.

WHAT_NEXT

read_def to create floorplan or initialize_floorplan.

DPS

DPS-001 (Warning) The module %s does not have any hierarchy below.It has %d violating paths and will be set as a seperate partition.

DESCRIPTION

This Warning message is generated if the given module does not have any submodules below it.It also specifies the number of violating paths present in the module.

WHAT NEXT

Check the partition_list

DPS-002 (Warning) The module %s does not have any hierarchy below.It has %d leaf cells and will be set as a seperate partition.

DESCRIPTION

This Warning message is generated if the given module does not have any submodules below it.It also specifies the number of leaf cells present in the module.

WHAT NEXT

Check the partition_list

DPS-003 (Error) There is no hierarchy in the design. The design cannot be partitioned.

DESCRIPTION

This Error message is generated if the given design does not have any modules and submodules below it.

DPS-004 (Error) The value for -max_size is very large for the design. The design does not require partitioning.

DESCRIPTION

This Error message is generated if the -max_size value specified is very large as compared to the number of number of leaf cells present in the given design .Hence the given design does not require partitioning.

WHAT NEXT

Free the autopartition info elements

DPS-005 (Error) Must specify the path to %s executable with variable dps_%s_path.

DESCRIPTION

This Error message is generated if the path of the given executable is not specified.

WHAT NEXT

Exit the process.

DPS-006 (Warning) No architecture specified for %s, default architecture is %s.

DESCRIPTION

This Warning message is generated if the architecture is not specified for the process.

WHAT NEXT

Set the architecture to its default value.

DPS-007 (Error) Unable to %s file %s %s.

DESCRIPTIONi

This Error message is generated if a file cannot be opened for reading or writing. This message is also generated if the file cannot be created or if the file is already opened for reading or writing.

WHAT NEXT

Exit the process.

DPS-008 (Error) No clocks founds in this design. Please apply clock constraints .

DESCRIPTION

This Error message is generated if no clocks are found in the design.

WHAT NEXT

Apply the clock constraints.

DPS-009 (Error) Unable to parse host information, the format is hostname:arch.

DESCRIPTION

This Error message is generated if there is an error in parsing the host information i.e. the hostname and the architecture.

WHAT NEXT

Check the various cases of the host error.

DPS-010 (Error) Please load the AHFS optimized design for -

skip_setup option.

DESCRIPTION

This Error message is generated if AHFS optimized design is not loaded for -skip_setup option.

WHAT NEXT

Load the optimized design for skip setup option.

DPS-011 (Error) Unable to find host by name %s.

DESCRIPTION

This Error message is generated if no host exists which has the specified name.

WHAT NEXT

Check the various cases of the host error.

DPS-012 (Error) No architecture specified with host %s, format is <hostname>:<architecture>.

DESCRIPTION

This Error message is generated if no architecture is specified for the given host.

WHAT NEXT

Check the various cases of the host error.

DPS-013 (Error) Invalid host %s specified, host name is ignored.

DESCRIPTION

This Error message is generated if invalid host is specified.

WHAT NEXT

Ignore the hostname.

DPS-014 (Error) Unable to find out nhost path.

DESCRIPTION

This Error message is generated when nhost path is not found.

WHAT NEXT

Check the nhost path.

DPS-015 (Warning) In DPS both "-effort high" and -"timing_driven_congestion" cannot be used. The option "-effort high" is ignored.

DESCRIPTION

DPS does not support the options "-effort high" and -"timing_driven_congestion" togather. You can use each one of them independently. If both the options are specified, DPS will ignore the option "-effort high".

WHAT NEXT

Check the physopt options specified in the set_dps_options or set_dps_module_options command and avoid using both these options togather.

DTC-1 (warning) The scaling factor given for %s is invalid. Using default value of 1.0.

DESCRIPTION

This message occurs if you have tried to scale derived constraints by a nonpositive number. Constraints cannot be scaled by a negative number, or by zero.

WHAT NEXT

Rerun **derive_timing_constraints** without the bogus scaling factor.

DTC-2 (warning) Unable to create clock on pin '%s' (%s).

DESCRIPTION

This warning can be issued by the **derive_clocks** command or the **derive_timing_constraints** command. It can happen if the command is issued before some synthetic cells are built.

WHAT NEXT

Use **compile** before issuing the **derive_clocks** or **derive_timing_constraints** command to build synthetic parts.

DVI-3 (warning) view_script_submenu_items variable exists but is invalid.

DESCRIPTION

You receive this message if the **view_script_submenu_items** variable, which defines the user-definable menu, exists but has an invalid value. The variable must contain a homogeneous list of strings.

WHAT NEXT

Change the value of the **view_script_submenu_items** variable so that it is a homogeneous list of strings. Then reexecute the command.

SEE ALSO

view_script_submenu_items (3).

DVI-4 (error) Script menu overflow.

DESCRIPTION

You receive this message if the user-definable menu has more than (%d) entries. (%d) is the maximum capacity for the menu.

WHAT NEXT

Adjust the **view_script_submenu_items** variable so that it contains no more than (%d) items. Then re-execute the command.

SEE ALSO

view_script_submenu_items (3).

DVI-5 (error) The current design is not constrained; cannot

create histogram.

DESCRIPTION

You receive this message if you issue a command to create a histogram, but the current design is not constrained. A histogram cannot be created unless the current design is constrained.

WHAT NEXT

Apply constraints to the current design, then create the histogram.

SEE ALSO

current_design (2).

DVI-6 (error) No current design, or current design not constrained; cannot create histogram.

DESCRIPTION

You receive this message if you issue a command to create a histogram, but there is no current design or the current design is not constrained. You cannot create a histogram unless there is a current design defined, and that current design is constrained.

WHAT NEXT

Ensure that a design is currently loaded and constrained.

SEE ALSO

current_design (2).

DVI-7 (warning) Design has been modified or removed. Closing Timing Analysis views.

DESCRIPTION

You receive this message because you have changed or removed the *current design* while one or more Timing Analysis windows are active. This message warns you that

these windows are being closed. When the *current design* is modified or deleted, Timing Analysis Windows (for example, Histogram View and Path Schematics) are invalidated.

WHAT NEXT

Regenerate the histogram with the changed *current design*.

SEE ALSO

current_design (2), **remove_design** (2).

DVI-8 (warning) Timing information in design has changed. Closing Timing Analysis views.

DESCRIPTION

You receive this message because you have changed timing information for the *current design* while one or more Timing Analysis windows are active. This message warns you that these windows are being closed. When the *current design* is modified or deleted, Timing Analysis Windows (for example, Histogram View and Path schematics) are invalidated.

WHAT NEXT

Regenerate the histogram with the changed *current design*.

SEE ALSO

current_design (2), **reset_design** (2).

DVI-9 (warning) The current design has changed. Closing Timing Analysis views.

DESCRIPTION

You receive this message because the *current design* has changed while one or more Timing Analysis windows are active. This message warns you that these windows are being closed. When the *current design* is modified or deleted, Timing Analysis Windows (for example, Histogram View and Path schematics) are invalidated.

WHAT NEXT

Regenerate the histogram with the changed *current design*.

SEE ALSO

current_design (2), **show_path_slack_histogram** (2).

DVI-10 (warning) Cannot perform this operation. Selected objects must be at the same hierarchical level.

DESCRIPTION

You receive this message because you have attempted to perform a group operation on objects at different hierarchical levels. For a group operation, all objects must be at the same hierarchical level.

WHAT NEXT

Execute the group operation again, using only cells from the same hierarchical level.

SEE ALSO

group (2), **ungroup** (2).

DVI-11 (warning) Cannot perform this operation. Selected nets must be at the same hierarchical level.

DESCRIPTION

You receive this message because you have attempted to perform this operation on nets in different hierarchical levels. For this operation, all nets must be at the same hierarchical level.

WHAT NEXT

Execute the command again using only nets from the same hierarchical level.

SEE ALSO

report_port (2), **report_timing** (2).

DWSC-2 (error) Port number %d of implementation '%s' of synthetic module '%s' should be '%s'.

DESCRIPTION

The netlist or hdl description of the named implementation does not match the module declaration in the synthetic library.

WHAT NEXT

Make sure that the ports in your netlist or hdl description match your module declaration exactly, both in name and order.

DWSC-3 (error) Direction of port '%s' in implementation '%s' does not match the declared synthetic module '%s'.

DESCRIPTION

The netlist or hdl description of the named implementation does not match the module declaration in the synthetic library.

WHAT NEXT

Make sure that the netlist or hdl description has the correct direction for the named port.

DWSC-4 (error) Width of port '%s' in implementation '%s' does not match the declared synthetic module '%s'.

DESCRIPTION

The netlist or hdl description of the named implementation does not match the module declaration in the synthetic library.

WHAT NEXT

Make sure that the netlist or hdl description has the correct width for the

named port. The width must match for all possible parameter values.

DWSC-5 (error) Port '%s' in implementation '%s' is not declared in the synthetic module '%s'.

DESCRIPTION

The netlist or hdl description of the named implementation does not match the module declaration in the synthetic library.

WHAT NEXT

Make sure that the netlist or hdl description has the same ports as the synthetic module.

DWSC-6 (warning) The dont_touch on the synthetic library implementation '%s' (module '%s') will be ignored during model generation.

DESCRIPTION

A dont_touch attribute on a top-level design is ignored. When a synthetic library implementation is modelled, it is treated as a top-level design. Later in the compile process, the implementation is a sub-design and the dont_touch will be adhered to.

WHAT NEXT

Remove the dont_touch on the design and apply the dont_touch to the cells in the implementation that the user wants to be dont_touched.

DWSC-7 (error) Design hierarchy is not allowed inside a synthetic library part. The module '%s' implementation '%s' has hierarchy in it.

DESCRIPTION

We support only hierarchy that is a technology library or a synthetic library module or operator.

WHAT NEXT

If the hierarchy is a technology library or a synthetic library, check the *synthetic_library* and *link_library* variables and the *set_local_link_library* directive.

DWSC-8 (error) The synthetic library module '%s' implementation '%s' failed to link.

DESCRIPTION

This error occured when linking a synthetic part. One possible problem is that the part has illegal hierarchy (eg: a level of hierarchy that is not a synlib part). Another possible problem is that there one synlib part contains another part (or technology cell) and both part's .sldb files are not in the synthetic_library variable. Another possible problem is that the subpart is not mentioned as a contained operator/module/implementation of the parent part, so the license for the subpart was not checked out and the subpart was not considered an authorized synthetic library part. Another possible problem is the local_link_library variable was not set correctly.

WHAT NEXT

Make sure the parts linked are synlib parts, technology cells, or GTECH cells. Add the subpart's .sldb file to the synthetic_library variable. Ensure that the subpart is listed as a contained operator/module/implementation of the parent part in the parent part's .sl file.
Make sure the local_link_path is set correctly.

DWSC-9 (information) Modeled %s(%s). (Wire load = %s Operating Conditions = %s)

DESCRIPTION

The named synthetic design was optimized to obtain representative timing and area numbers for the part. These numbers will be used to model the part in subsequent optimizations.

Once a part is modeled, it can be stored in a synthetic cache. Thus, subsequent compiles will not have to recreate the model. Use the variables *cache_read* and *cache_write* to set up your cache. You can also use the **create_cache** command to store parts in your cache.

WHAT NEXT

Store in a synthetic cache the synthetic implementations you use often. For more details, refer to the DesignWare reference manual.

DWSC-10 (information) The synthetic model '%s' was read from a cache.

DESCRIPTION

WHAT NEXT

DWSC-11 (information) Read %s as a cache element.

DESCRIPTION

Indicates that the specified design was read from the current Synopsys cache.

WHAT NEXT

No action is required as this is just an information message.

DWSC-12 (information) The cache entry '%s' is out of date with respect to the information in the design library or the generator '%s' (module '%s', implementation '%s'). The cache entry has been removed.

DESCRIPTION

A cache entry is tagged with a timestamps from the design library entry or the generator's executable that it was created from.
If the design library or the generator's executable is updated, then the cache entry may not be valid, so it is removed.

WHAT NEXT

DWSC-13 (warning) The cache entry '%s' should be removed, but the attempt to remove it has failed. The entry is either out of date or corrupted with respect to its entry in the design library or the generator '%s' (module '%s', implementation '%s').

DESCRIPTION

A cache entry is tagged with a timestamp from the design library entry or the generator's executable that it was created from. When the design library or the generator executable is updated, then the cache entry may not be valid and so it is removed. This warning indicates that the attempt to remove it failed. If the cached item is not removed manually, the cached entry may cause the compile command to require more time generating netlist for that synthetic library part.

WHAT NEXT

DWSC-14 (information) The cache entry '%s' is out of date with respect to its target library '%s'. The cache entry has been removed.

DESCRIPTION

A cache entry is tagged with a timestamp from the target library that it was created from. If the target library is updated, then the cache entry may not be valid, so it is removed.

WHAT NEXT

DWSC-15 (warning) The cache entry '%s' should be removed, but the attempt to remove it has failed. The entry should be removed because either it is corrupted

or it is out of date due to newer target library '%s'.

DESCRIPTION

A cache entry is tagged with a timestamp from the target library that it was created from. If the target library is updated, then the cache entry may not be valid, so it is removed.
The attempt to remove it failed.
If it is not removed manually, it may cause the compile command to take more time generating netlist for that synthetic library part.

WHAT NEXT

DWSC-16 (information) The v3.3b cache element format has changed.
The cache entry, '%s', is being removed.

DESCRIPTION

A new cache element will be built and cached.

WHAT NEXT

Nothing needs to be done.

DWSC-17 (warning) The cache entry '%s'
should be removed, but the attempt to remove it has failed.
The entry should be removed because it is written in the older format, v3.3b.

DESCRIPTION

The cache entry is written in the older format which does not have required information for further optimizations. The attempt to remove it failed.
If it is not removed manually, it may cause the compile command to take more time while it optimizes that synthetic library part.

WHAT NEXT

Manually remove the cache element.

DWSC-18 (information) The cache entry '%s' has been corrupted, so it is being removed.

DESCRIPTION

The cache is a directory structure and the files in it have a predefined format. The entry listed above does not conform to the format.

WHAT NEXT

No action is necessary; the file has been removed.

DWSC-19 (warning) The cache entry '%s' should be removed, but the attempt to remove it has failed. The entry should be removed because it is either corrupted or obsolete.

DESCRIPTION

The cache is a directory structure and the files in it have a predefined format. The entry listed above does not conform to the format.

WHAT NEXT

DWSC-20 (warning) Improper octal value for variable cache_file_chmod_octal or cache_dir_chmod_octal: %s

DESCRIPTION

The value specified for either cache_file_chmod_octal or cache_dir_chmod_octal was invalid. These values are used to set the directory and file permissions on directories and files created inside of a Synopsys cache. The values must be octal numbers and less than 0777 for file permissions and less than 01777 for directory

permissions.

WHAT NEXT

Check the values of these two variables and update them so that they have valid values.

DWSC-21 (warning) Cannot set protections on the cache directory %s.

DESCRIPTION

After creating the specified directory, an attempt was made to chmod it to the permissions specified by the cache_dir_chmod_octal variable. The chmod system call failed.

WHAT NEXT

Fix the problem that prevented the chmod from succeeding if possible. Otherwise try creating the directory and setting the permissions manually.

DWSC-22 (information) Wrote %s as cache element.

DESCRIPTION

Indicates that the specified design was written to the current Synopsys cache.

WHAT NEXT

No action is required as this is just an information message.

DWSC-23 (warning) Cannot set protections on the cache file %s.

DESCRIPTION

After creating the cache file, an attempt was made to chmod it to the permissions specified by the cache_file_chmod_octal variable. The chmod system call failed.

WHAT NEXT

Fix the problem that prevented the chmod from succeeding if possible. Otherwise try creating the directory and setting the permissions manually.

DWSC-24 (warning) Cache element %s could not be written.

DESCRIPTION

An error occurred while trying to write a cache element to the specified file. This is most likely due to file permissions problems or a full disk.

WHAT NEXT

Resolve the problem with the specified file/directory and try the failing command again.

DWSC-25 (error) Unable to resolve environment variable %s for generator %s.

DESCRIPTION

The environment variable which defines the location of the generator is not defined.

WHAT NEXT

Set the generator’s executable environment variable to point to a valid location

DWSC-26 (information) User interrupted execution of generator.

DESCRIPTION

WHAT NEXT

DWSC-27 (error) Synthetic library ’%s’

is from an incompatible version of the software.

DESCRIPTION

You cannot use the given synthetic library with this version of the software. If you are worried about obtaining "standard.sldb", do not worry. An up-to-date version of standard.sldb is automatically used, regardless of the contents of the synthetic_library variable. The correct default setting for synthetic_library is **{}**.

WHAT NEXT

DWSC-28 (warning) Inout port type on port %s is currently not supported.

DESCRIPTION

WHAT NEXT

DWSC-29 (warning) Unknown input oper_pin ’%s’ specified as permutable.

DESCRIPTION

WHAT NEXT

DWSC-30 (warning) Input oper_pin ’%s’ multiply specified as

permutable.

DESCRIPTION

WHAT NEXT

DWSC-31 (error) Unable to find the generator at '%s'.

DESCRIPTION

The pathname to the generator executable which is defined by the environment variable in the synthetic library is invalid.

WHAT NEXT

Reset the generator's environment variable to point to a valid executable.

DWSC-32 (error) %s.

DESCRIPTION

This message may have several different outputs. Below is information on each one:

No formula or specified value for parameter '%s' in library specification for module '%s', implementation '%s'. The synthetic module or implementation requires the given parameter. When instantiating the module, the parameter was not specified.

Remember, synthetic library parameter names are case-sensitive. Keep in mind that the offending part instantiation might be nested inside another synthetic implementation.

WHAT NEXT

No formula or specified value for parameter '%s' in library specification for module '%s', implementation '%s'. Make sure you specify the required parameter. If you are using DesignWare developer, you can modify the module/implementation definition in your *.sl file so that the parameter is derived automatically (via a formula attribute).

DWSC-33 (error) Parameter '%s' does not evaluate to a numeric

value %s.

DESCRIPTION

WHAT NEXT

DWSC-34 (information) The cache entry '%s' is out of date with respect to the information in the synthethic library '%s' (module '%s', implementation '%s'). The cache entry has been removed.

DESCRIPTION

```
A cache entry is tagged with a timestamps from the synthetic library entry
 that it was created from. If the synthetic library is updated, then the
 cache entry may not be valid, so it is removed.
```

WHAT NEXT

DWSC-35 (warning) The cache entry '%s' should be removed, but the attempt to remove it has failed. The entry is either out of date or corrupted with respect to its entry in the synthetic library '%s' (module '%s', implementation '%s').

DESCRIPTION

```
A cache entry is tagged with a timestamps from the synthetic library entry
 that it was created from. If the synthetic library is updated, then the cache
 entry may not be valid, so it is removed.
 The attempt to remove it failed.
 If it is not removed manually, it may cause the compile command
 to take more time generating netlist for that synthetic library part.
```

WHAT NEXT

DWSC-36 (warning) Could not find port ’%s’ in implementation %s
of synthetic module ’%s’.

DESCRIPTION

Each port defined in a synthetic library implementation must exist in the
netlist used to instantiate the implementation.

WHAT NEXT

DWSI-1 (error) Parameter '%s' does not evaluate to a positive value
%s.

DESCRIPTION

WHAT NEXT

DWSI-2 (info) Re-generating implementation '%s' for '%s' with timing context.

DESCRIPTION

During second pass iis, if the mentioned part is the only choice for incremental implementation selection, and this part is from mce generator, it is forced to be re-generated with timing context.

WHAT NEXT

DWSI-3 (warning) Power optimization feature in DesignWare generator is disabled because the required '%s' license is not available.

DESCRIPTION

The DesignWare build in power optimization feature requires DesignWare-LP license. This license can not be checked out. Therefore, this feature is disabled.

WHAT NEXT

DWSI-4 (information) Dynamic power optimization is enabled in

DesignWare generator.

DESCRIPTION

This information message advises you that the DesignWare built-in dynamic power optimization feature is enabled implicitly, even in the absence of dynamic power constraints. The feature is enabled when power optimization features, such as datapath gating, are turned on.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

power_enable_datapath_gating(3)

EA

EA-001 (error) Estimate_fp_area component failure.

DESCRIPTION

This error message occurs when one of the major components of command fails. Major component include die creation, placement, power network synthesis and routing.

WHAT NEXT

Check in the log file before this message and see what errors occurred.

EA-002 (error) File %s not found.

DESCRIPTION

This error message occurs during the loading of user defined scripts. It indicates that the script could not be found.

WHAT NEXT

Check if the script is available, and that the spelling is correct. Try putting script in run directory and loading it from that location.

EA-003 (error) The options %s and %s are mutually exclusive.

DESCRIPTION

This error message occurs when you use two options which are mutually exclusive.

WHAT NEXT

Check the man page of the command to determine why these options are mutually exclusive. Do not use one of the two options.

EA-004 (error) The value given for option %s must be less or

equal to option %s.

DESCRIPTION

This error message occurs when you have two options which have a relationship such that one option value must be less than or equal to the other. For example, setting a minimum and maximum value, the minimum value must be less than or equal to the maximum value.

WHAT NEXT

Change the input option values to satisfy the above constraint.

EA-005 (error) No design is loaded.

DESCRIPTION

This error message occurs if there is no design loaded and a loaded design is needed.

WHAT NEXT

Load a design.

SEE ALSO

open_mw_cel(2)
open_mw_lib(2)

EA-006 (error) Failure in Power Network Synthesis.

DESCRIPTION

This error message occurs when you are using power network synthesis (PNS) and there was an error while running PNS.

WHAT NEXT

Look at log file to see what was error in PNS. Try changing how you are using PNS, or do not use PNS to see if that will work.

EA-007 (error) Failed to get cell/core boundary.

DESCRIPTION

This error message occurs when there is no die and/or core in the design.

WHAT NEXT

Use initialize_floorplan to create the die and core before running this command.

SEE ALSO

initialize_floorplan(2)

EA-008 (error) Unfixed hard macros outside core boundary.

DESCRIPTION

This error message occurs when you have unfixed hard macros that are outside or partially outside the core.

WHAT NEXT

Take a look at the macros which are outside or partially outside the core. If they are intended to be that way, then mark them as fixed. If they are not intended to be outside the core, then move them to be inside the core.

EA-009 (error) Failed to get design utilization.

DESCRIPTION

This error message occurs when the tool is unable to calculate the design utilization. Design utilization consists of two parts, the area of the cells in the design and the area of the core. If either of these two parts cannot be calculated, then this error will result.

WHAT NEXT

If there is no core in design, create one with initialize_floorplan.

SEE ALSO

initialize_floorplan(2)

EA-010 (error) Missing the required license, %s.

DESCRIPTION

This error message occurs because you have accessed a command or feature that requires a license which is not available.

WHAT NEXT

Check if there are any licenses available or if there is any problem with the license server.

EA-011 (error) Fixed HM/SM overlaps detected.

DESCRIPTION

This error message occurs because you have fixed (in location) hard macros or soft macros which are overlapping. This is not supported in estimate_fp_area.

WHAT NEXT

Determine which are the overlapping macros, and remove the overlap. You can use report_fp_placement to determine which are the overlapping macros.

SEE ALSO

report_fp_placement(2)

EA-012 (error) Core BBox is not inside cell BBox.

DESCRIPTION

This error message occurs because the bounding box of the core is not inside the bounding box of the cell. It is allowed for the core boundary to be rectangular while the cell boundary is rectilinear, but the bounding box of the core must be inside the bounding box of the cell.

WHAT NEXT

Change the core or cell boundary to satisfy this constraint.

SEE ALSO

initialize_floorplan(2)

EA-013 (error) Overlapping placement constraints detected

DESCRIPTION

This error message occurs because the design contains overlapping (or nested) placement constraints. These constraints include plan groups, hard movebounds, exclusive movebounds, and voltage areas. None of these constraints can overlap for this command to work properly.

WHAT NEXT

Determine what are the overlapping constraints. Remove or delete the constraints as appropriate.

EA-014 (error) Large pin %s (%lf %lf %lf %lf) detected.

DESCRIPTION

This error message occurs because the design contains very large pins which will limit the shrink that can be done because pins are not shrunk. Typically these pins are power pins.

WHAT NEXT

Find these large pins either by the name or by the dimensions given. Remove all these large pins before using estimate_fp_area.

EA-015 (error) Failed to save design.

DESCRIPTION

This error message occurs when **estimate_fp_area** tries to save the design but fails. **estimate_fp_area** needs to save a copy of the design to keep a backup copy of the design while it is changing the original design.

WHAT NEXT

Make sure you have write permission on disk and that disk is not full.

EA-016 (error) Failed to load TDF constraints.

DESCRIPTION

This error message occurs when there is a problem in loading TDF constraints.

WHAT NEXT

Check the TDF constraints to make sure they are correct. The TDF constraints are in the file "io_temp.tdf".

SEE ALSO

write_io_constraints(2)
read_io_constraints(2)

EA-017 (error) Design contains both pins and IO pads.

DESCRIPTION

This error message occurs because the design contains both pins and IO pads. This situation is not supported by this command. The design should have only pins or only IO pads.

WHAT NEXT

Delete the pins or the IO pads as appropriate.

EA-018 (error) The option %s is required when using option %s.

DESCRIPTION

This error message occurs when you use two options which depend on each other. The first option is required when you are using the second option.

WHAT NEXT

Check the man page of the command to determine why these options are related. Add the required option or remove the second option.

EA-019 (error) The -power_net_names string format is not

correct.

DESCRIPTION

This error message occurs when there is a problem in parsing the -power_net_names string. It is expected that the string will be of the form {VDD net name> <VSS net name>}.

WHAT NEXT

Fix the -power_net_names string as specified by the format above.

ECO

ECO-1 (error) The subdesign '%s' has %d %s cells.

DESCRIPTION

During **eco_implement**, all the cells in the old implementation and new implementation must be mapped, not generic cells or unmapped DesignWare parts.

WHAT NEXT

Compile or map the implementation designs. Try again.

ECO-2 (error) Current design pair is not defined.

DESCRIPTION

This error is generated when current design pair is not defined in the dc_shell.

WHAT NEXT

Use **list_designs** command to see whether there are any designs in the memory or use **read** command to read a design in. Then invoke **eco_current_design_pair** command to set the desired current design pair.

ECO-3 (error) Cannot set a design in current design pair to library design '%s'.

DESCRIPTION

WHAT NEXT

ECO-4 (error) Some black box cells cannot be handled

in design '%s'.

DESCRIPTION

The listed cells are most likely cells within DesignWare cells whose library cell reference cannot be found. ECO Compiler cannot handle cells without library references inside DesignWare cells.

Note: ECO Compiler can handle some cells with unresolved references: user instantiated cells from the link library as well as user-defined subdesigns whose underlying DB reference design has been removed. However, the cells must be in pairs, one in the old netlist and one in the new netlist, with the same cell name and pin names.

Such cell pairs are treated as aligned black boxes during the ECO process. No changes to black box cells or subdesigns are made. The cell pair input pins are treated as endpoints and their output pins are treated as sourcepoints. Cells that are mentioned in the **set_eco_reuse** command are treated in the same way.

WHAT NEXT

Attempt to resolve all unresolved references related to the cells listed and run **eco_implement** again.

ECO-5 (error) The current design pair is inappropriate for the command.

DESCRIPTION

Most likely you tried to do **eco_analyze_design** or **eco_implement** and the options to the last **eco_current_design_pair** were inappropriate.

Suppose that the following four top-level DB designs are involved in an ECO process:

Design Name	Role in ECO process
OH	old HDL
ON	old netlist
NH	new HDL
NN	new netlist

For these top-level designs, there are only four valid combinations of the options:

1) **eco_current_design_pair -old_hdl OH -new_hdl NH**

Use this for **eco_align_design** and **eco_analyze_design**.

2) **eco_current_design_pair -old_hdl OH -old_netlist ON**
Use this for **eco_align_design** of the two old designs.

3) **eco_current_design_pair -new_hdl NH -new_netlist NN**
Use this for **eco_align_design** of the two new designs.

4) **eco_current_design_pair -old_netlist ON -new_netlist NN**.
Use this for **eco_align_design** and **eco_implement** on the netlists.

eco_current_design_pair is irrelevant during **eco_recycle** and has no effect if it is set.

WHAT NEXT

Choose one of the aforementiond options and rerun command.

ECO-6 (error) Design %s is a limited design and can not be processed by ECO Compiler.

DESCRIPTION

WHAT NEXT

ECO-7 (error) Do not use on cell '%s' attributes eco_spare and eco_obsolete
together with set_eco_unique, set_eco_align, and set_eco_reuse.

DESCRIPTION

The **eco_implement** and **eco_recycle** commands identify spare cells using the **eco_spare** and **eco_obsolete** DB attributes. Do not apply any directives, such as **set_eco_unique**, **set_eco_align** or **set_eco_reuse** to such cells.

The **set_eco_align** command is unnecessary because spare cells in the new netlist are not utilized. Instead, spare cells in the old netlist are copied into the new netlist and (possibly) connected to other design cells.

WHAT NEXT

If you have a spare register in the old netlist (named old_reg), and you want it to replace a unique register in the new netlist (new_reg) do the following:

Set **current_design** to the old netlist.
Remove the **eco_spare** attribute from the register, thereby converting it into part of the old netlist design.
Set **eco_current_design_pair** to the old netlist and new netlist.
Use **set_eco_align** so that the name old_reg will be put on the register new_reg during **eco_implement**.

This cannot be done for a combinational cell.

ECO-8 (information) In design '%s' cell '%s' has unique name to avoid collision.

DESCRIPTION

The cell mentioned was copied from the old implementation to the new implementation, but its name collided with a sequential cell name in the new implementation. **eco_implement** gave the copied old cell a unique name so that the sequential cell name did not have to change. One reason for doing this is that compare_design requires sequential cell names to be the same in order to verify two designs. With this naming rule the new specification can be compared with the result of **eco_implement** without name conflicts.

WHAT NEXT

The user will have to resolve the naming conflicts between combinational and sequential cells in the new implementation.

ECO-9 (error) Exactly one target must be specified to set_eco_target.

DESCRIPTION

You either specified no target or more than one target to **set_eco_target.** You can only specify exactly one target.

WHAT NEXT

Specify one target point and rerun.

ECO-10 (error) Missing library cell '%s' for cell '%s' in '%s'. Make sure the dont_use attribute is not on target_library cell.

DESCRIPTION

The **target_library** does not contain the type of cell needed to copy a cell from the old implementation to the new implementation.

WHAT NEXT

Make sure the **target_library** contains all cells that are present in the old implementation and rerun **eco_implement**.

ECO-11 (information) The verification limit was reached for some ECO endpoints:

DESCRIPTION

The listed (aligned) endpoints cannot be verified during **eco_implement** using the same formal verification techniques that are used in **compare_design**.

eco_implement treats these endpoints as changed endpoints in the new implementation, because verification could not establish that the endpoint functions are unchanged from the old implementation.

If the endpoints are in reality functionally unchanged, some new cells can be needlessly introduced by **eco_implement**.

(Endpoints that have identical fanin logic between the old specification and new specification are never listed by this message and are not submitted to formal verification; the old implementation is used in its entirety.)

WHAT NEXT

Currently, there is no directive for you to indicate that an endpoint is functionally unchanged and must be reused from the old implementation.

Try to rewrite the new specification so that only endpoints that need to change functionally are rewritten. Other endpoints are then most likely to be determined to have identical fanin logic and the old implementation logic can be used in its entirety (without any need for formal verification).

ECO-12 (error) The designs of the current design pair have

incongruent hierarchies.

DESCRIPTION

You called **eco_implement** for a design pair, the designs of which have incongruent hierarchies. The **eco_implement** command cannot handle incongruent hierarchies. Run **eco_align_design** for that particular design pair to get more information about those hierarchies.

WHAT NEXT

You might need to use the **ungroup** command to partially flatten one or both of the design hierarchies.

ECO-14 (warning) The library cells of cell %s and %s have the same names but have different functionality.

DESCRIPTION

Two library cells with identical names but different functionality have been found. The reason for this might be that they are from different libraries. The cells linked to these library cells are treated as different in functionality.

WHAT NEXT

If using multiple libraries check for consistency. You shouldn’t have library cells with different functionality but identical names.

ECO-15 (warning) Specifying high effort level for the eco_implement
command may lead to excessive run-times.

DESCRIPTION

This message indicates that you have set the **eco_implement_effort_level** variable to the value of "high". When this variable is set to "high" **eco_implement** tries harder in verifying end-points between the old and new netlists.

WHAT NEXT

Try setting the **eco_implement_effort_level** variable to "low" before running the

eco_implement command.

SEE ALSO

eco_implement_effort_level (3)

ECO-16 (info) If you would like eco_implement to work harder on these endpoints, try setting the eco_implement_effort_level variable to 'high'.

DESCRIPTION

This message follows the **ECO-11** information message. If the **eco_implement** command is run in the low effort mode (default mode) and the verification limit is reached for some endpoints, then this message indicates that you can try running **eco_implement** in high effort mode by setting the **eco_implement_effort_level** variable to "high". In high effort mode, **eco_implement** tries harder in identifying endpoints that are functionally identical between the old and new netlists.

Note on excessive run-time in the **eco_implement** *command:* Setting this variable to "high" can lead to excessive run-times in the **eco_implement** command. You should only set this variable to "high" if the **eco_implement** command issues a **'ECO-11'** information message indicating that verification limit was reached for some endpoints.

Even in this case, you should first examine the list of endpoints following this message as well as **eco_implement** command's quality of reuse before setting this variable to "high". If that list includes endpoints that you believe have not changed as the result of the ECO, and you are not satisfied with the number of old and new cells in the ECO implementation generated by the **eco_implement** command, then you can try setting this variable to "high" in your ECO script. You should then repeat the ECO implementation process.

WHAT NEXT

Set the **eco_implement_effort_level** variable to the value "high".

SEE ALSO

eco_implement (2), **eco_implement_effort_level** (3), **ECO-11.**

ECO-17 (information) Uniquifying design %s in order to change

the reference design of cell %s/%s.

DESCRIPTION

When applied to hierarchical cells, the **set_eco_reuse** command changes the reference design of the new netlist cell to the DB design of the old netlist cell.

If the new and old netlist cells have the same reference design names (although different implementations), and you perform the **link** command on the new design after the **set_eco_reuse** command, the new netlist cell may be linked to its original reference design, effectively undoing the intent of the **set_eco_reuse** command.

In order to avoid this problem, ECO Compiler checks the names of the reference designs of the new and old cells mentioned in the **set_eco_reuse** command. If the names match, then ECO Compiler uniquifies the parent design of the old cell before changing the reference design of the new cell to the uniquified reference design of the old cell. This resolves the name collision since the name of the old cell's reference design (and all of its sub-designs, if any) is made unique in the dc_shell database.

ECO Compiler uses the **uniquify_naming_style** dc_shell variable in creating the new design names.

WHAT NEXT

Make sure that the specified designs are unique. Refer to the **uniquify** man page for more information on how to make designs unique within dc_shell.

SEE ALSO

set_eco_reuse, **uniquify**, **uniquify_naming_style**

ECO-18 (error) Identical DB reference '%s' for the instances '%s' and '%s'.

DESCRIPTION

The designs specified in the command have the same DB reference. The designs in the command are expected to be distinct designs.

WHAT NEXT

Make sure that the specified designs are unique. Refer to the **uniquify** man page for more information on how to make designs unique within dc_shell.

ECO-19 (error) The following DesignWare designs are instantiated in
both hierarchies.

DESCRIPTION

The same DesignWare design is referenced in both the new as well as the old design hierarchies. Instances of DesignWare designs in the new and old hierarchies must refer to distinct designs.

WHAT NEXT

Make sure that the new and old design hierarchies are linked correctly and that the specified designs are unique. Refer to the **uniquify** manual page for more information on how to make designs unique within dc_shell. Also refer to the *ECO Compiler User Guide* for information related to linking designs. If you are certain that two DesignWare instances are identical in the old and new designs, and want them to refer to the same DesignWare design, you can use the **set_eco_reuse** command prior to **set_eco_align** and **set_eco_implement** commands.

SEE ALSO

uniquify, **set_eco_reuse**

ECO-20 (error) The following DesignWare designs are instantiated more
than once in the %s.

DESCRIPTION

The same DesignWare design is referenced more than once in the new (or old) design hierarchy. DesignWare instances in the design hierarchy must refer to distinct designs. This message refers to the new, old, or current design hierarchy depending on the ECO Compiler command that issues the message.

WHAT NEXT

Make sure that the new (or old or current) design hierarchies are linked correctly and that the specified designs are unique. Refer to the **uniquify** man page for more information on how to make designs unique within dc_shell. Also refer to the *ECO Compiler User Guide* for information related to linking designs.

SEE ALSO

uniquify

ECO-21 (error) Do not apply both set_eco_align and %s attribute on cell '%s'.

DESCRIPTION

Never apply **set_eco_align** or **set_eco_reuse** to a cell with either the *eco_spare* or *eco_obsolete* DB attributes. Spare and obsolete cells do not need to be aligned or identified as unique.

WHAT NEXT

If the reported cell is intended to be a spare cell, remove any **set_eco_align** or **set_eco_reuse** that mention it. If the reported cell is not intended to be a spare cell, remove any *eco_spare* or *eco_obsolete* DB attributes from the cell. Do not use **reset_design** because it removes these DB attributes from all cells.

Recommended flow:

1) Instantiate spare cells in the old netlist only. Put the *eco_spare* attribute on each cell. Do not apply any directives to the spare cells.

2) Perform all alignment after instantiating spare cells.

ECO-22 (error) Design '%s' has '%d' black boxes but design '%s' has '%d' black boxes.

DESCRIPTION

Because all the black boxes of a design have to be aligned, different numbers of black boxes in two related designs are not allowed, although **eco_align_design** results in a dc_shell status of 0.

WHAT NEXT

A missing library might cause the black boxes. Check for proper linking of the design, or make sure that all the black boxes can be pairwise aligned. If there are library cells with the black box attribute, remove this attribute and try again.

ECO-23 (error) cell '%s''%s' is a unalignable black box.

DESCRIPTION

All Black Boxes have to be aligned. Unique Black Boxes are not allowed. Though **eco_align_design** will result in a dc_shell status of 0.

WHAT NEXT

Use **set_eco_align** to pairwise align all the black boxes or check for correct linking of the design. The cause for black boxes may be a missing library.

ECO-24 (warning) The following hierarchical cells of the old netlist have the same DB reference as some cells in the new netlist due to the set_eco_reuse command. This can cause inaccuracies in the output.

DESCRIPTION

The designs specified in the warning have the same DB reference as a result of a previously issued **set_eco_reuse** command. This can cause inaccuracies in the output of the **eco_netlist_diff** command.

WHAT NEXT

Make sure that **set_eco_reuse** command is not issued before the **eco_netlist_diff** command.

ECO-25 (error) set_eco_reuse applies only to netlist design pair.

DESCRIPTION

The user has attempted to use **set_eco_reuse** on an **eco_current_design_pair** other than the old_netlist and new_netlist. This not permitted. It is not necessary to use **set_eco_reuse** to indicate that HDL sub-designs should be reused.

WHAT NEXT

Check that the **eco_current_design_pair** is properly set or remove the **set_eco_reuse**

command if it applies to another pair.

ECO-26 (information) Ignoring eco_spare attribute on hierarchical cell %s of %s:%s

DESCRIPTION

This message indicates that ECO Compiler is ignoring the 'eco_spare' attribute on a hierarchical cell. This attribute is intended for leaf-level library cell instances. ECO Compiler will treat this cell just as any other hierarchical cell in the design.

WHAT NEXT

If you want ECO Compiler to use the cells in this block as spare cells, then set you current_design to the design associated with the this block and apply the 'eco_spare' attribute to the library cell instances of that design.

ECO-40 (error) Remapping of registers failed.

DESCRIPTION

eco_implement tries to remap each aligned register in the new implementation so that it has the same library cell type as the aligned register in the old implementation.

If the remapping cannot be performed, possibly due to changes in clocking or asynchronous behavior, **eco_implement** tries to remap the register in the old implementation to the type in the new implementation.

If this remapping fails, this error message is issued and **eco_implement** terminates.

WHAT NEXT

If you set the **dc_shell** environment variable "eco_allow_register_type_difference = TRUE", **eco_implement** continues without pin-compatibility.

ECO-41 (warning) Some registers in old implementation could

not be re-mapped:

DESCRIPTION

eco_implement has failed to remap the registers in the old implementation to have the same type as the aligned registers in the new implementation.

The default behavior of **eco_implement** is to terminate execution in this case, so that the user can review whether these register incompatibilities reflect intended and necessary changes to the new specification. Changes in asynchronous properties of the registers are the most common cause of remapping failure.

WHAT NEXT

If you set the **dc_shell** environment variable "eco_allow_register_pin_difference = TRUE", **eco_implement** continues without pin-compatibility.

ECO-42 (information) Some new register types were used to remap some old registers:

DESCRIPTION

This message indicates that **eco_implement** has achieved pin-compatibility for some aligned register pairs; for example, reg_old and reg_new in the old and new netlists, respectively.

eco_implement has successfully remapped reg_old in the old netlist, so that it has the same library cell type as reg_new in the new netlist.

WHAT NEXT

No further user action required.

ECO-43 (information) Continuing with some non-pin-compatible registers.

DESCRIPTION

By setting the **dc_shell** environment variable "eco_allow_register_pin_difference = TRUE" the user has opted to continue **eco_implement** without pin-compatibility between aligned registers.

Pin-compatibility is a highly desirable property to achieve between pairs of

sequential cells (say reg_old and reg_new) in order to maximize cell reuse.

The user should be aware that cell reuse may be reduced.

Output pins of incompatible registers may not be alignable, thus causing **eco_implement** to introduce new cells in the fanout of new_reg.

WHAT NEXT

If the type of reg_new is not used anywhere in old netlist, then the user may apply **set_dont_use** to that type in the library, thus preventing its use in the new netlist. This may cause the compile process of the new HDL to map reg_new to the type of reg_old.

ECO-44 (information) Some old register types were used to remap some new registers:

DESCRIPTION

This message indicates that **eco_implement** has achieved pin-compatibility for some aligned register pairs, say old_reg and new_reg, in the old and new netlists, respectively.

eco_implement has successfully re-mapped new_reg, in the new netlist, so that it has the same library cell type as old_reg, in the old netlist.

WHAT NEXT

No further user action required.

ECO-45 (warning) Some registers in new implementation could not be re-mapped:

DESCRIPTION

eco_implement failed to achieve pin-compatibility for some aligned register pairs, say reg_old and reg_new.

Re-mapping of reg_new may or may not be possible, depending on the nature of the design change to the new specification.

Changes in the new specification to clocking or asynchronous set and reset conditions are common causes of re-mapping failure.

eco_implement automatically tries to re-map old_reg to be pin-compatible with

new_reg, thus changing the old implementation.

WHAT NEXT

Pin-compatibility is a highly desirable property to achieve between the implementations in order to maximize cell reuse.

If the user sets the **dc_shell** environment variable "eco_allow_register_type_difference = TRUE" then **eco_implement** will continue without pin-compatibility.

The user should be aware that cell reuse may be reduced.

Output pins of incompatible registers may not be alignable, thus causing **eco_implement** to introduce new cells in the fanout of new_reg.

ECO-46 (information) Because, the reference type associated with the corresponding aligned register in the %s implementation is not present in the target library.

DESCRIPTION

This message supports warning messages that are issued during the register re-mapping phase of the **eco_implement** command.

It indicates that some of the register types necessary for register re-mapping are not present in the list of target library registers visible to **eco_implement**.

This can occur when you forget to specify a technology library in the **target_library** list (although the library may be in the **link_library** list). It can also occur if the target library cell has the **dont_use** attribute.

WHAT NEXT

If the problem is due to a missing library in the **target_library**, then add that library to the list.

If the problem is due to a **dont_use** attribute on the library cell, then remove that attribute using the **remove_attribute** command. For example:

dc_shell> remove_attribute <lib_name>/<reg_type_name> dont_use

If you would like **eco_implement** to continue without pin-compatibility between aligned registers in the old and new implementations, then set the **dc_shell** environment variable "eco_allow_register_pin_difference = TRUE"

You should be aware that cell reuse may be reduced.

SEE ALSO

ECO-45, ECO-41, **eco_implement**, **remove_attribute**, **dont_use**

ECO-70 (info) Accepting logic in the transitive fan-in of object '%s' in design '%s'.

DESCRIPTION

WHAT NEXT

ECO-71 (error) Can't set eco_accept_endpoint directive on unique object '%s'.

DESCRIPTION

Setting eco_accept_endpoint directive on an end-point in the old design directs ECO Compiler to freeze the logic in the transitive fan-in of that end-point in the old design, and copy that logic into the ECO design in the transitive fan-in of the corresponding aligned end-point in the new design. This directive is ignored if the specified end-point is unique to the old design (does not exist in the new design, therefore does not exist in the ECO design).

WHAT NEXT

ECO-72 (error) Can't set object '%s' unique because it has the eco_accept_endpoint directive.

DESCRIPTION

Setting eco_accept_endpoint directive on an end-point in the old design directs ECO Compiler to freeze the logic in the transitive fan-in of that end-point in the old design, and copy that logic into the ECO design in the transitive fan-in of the corresponding aligned end-point in the new design. You can not set an end-point unique if that end-point already has the eco_accept_endpoint directive.

WHAT NEXT

ECO-73 (warning) Ignoring eco_accept_endpoint directive on %s %s.

DESCRIPTION

This message indicates that ECO Compiler is ignoring an eco_accept_endpoint directive. This occurs when you apply this directive to an invalid design object. For example this directive cannnot be applied to combinational cell pins or input ports.

WHAT NEXT

ECO-74 (information) Because, parent DesignWare cell has the set_eco_reuse directive.

DESCRIPTION

This message supports the ECO-73 warning message and explains the reason for ECO Compiler ignoring an eco_accept_endpoint directive.

WHAT NEXT

ECO-75 (information) Because, pin '%s' in level hierarchy '%s' can not be found.

DESCRIPTION

This message supports the ECO-73 warning message and explains the reason for ECO Compiler ignoring an eco_accept_endpoint directive. In this case, the specified pin can not be found in the hierarchy. This can occur, for example, when the eco_accept_endpoint is specified on a pin of a DesignWare cell which is instantiated inside another DesignWare cell, and the parent DesignWare cell is not aligned.

WHAT NEXT

ECO-76 (information) Because, endpoint is not aligned.

DESCRIPTION

This message supports the ECO-73 warning message and explains the reason for ECO Compiler ignoring an eco_accept_endpoint directive. In this case, the **eco_accept_endpoint** is specified on an endpoint in the old netlist, which is not aligned with any endpoints in the new netlist.

WHAT NEXT

Align the endpoint with an endpoint in the new netlist.

ECO-77 (information) Because, the eco_accept_endpoint directive is also applied to the corresponding aligned endpoint "%s" in the new netlist.

DESCRIPTION

This message supports the ECO-73 warning message and explains the reason for ECO Compiler ignoring an eco_accept_endpoint directive. In this case, the **eco_accept_endpoint** is specified on an endpoint in the old netlist. However, the **eco_accept_endpoint** is also applied to the corresponding aligned endpoint in the new netlist. This is contradictory.

WHAT NEXT

Remove the eco_accept_endpoint directive from one of the endpoints or check the alignment between endpoints in the old and new netlists.

ECO-78 (information) Because the following startpoints in the support of end-point "%s" in the old netlist are not aligned with any startpoints in the support of endpoint "%s" in the new netlist.

DESCRIPTION

This message supports the ECO-73 warning message and explains the reason for ECO

Compiler ignoring an eco_accept_endpoint directive. In this case, the eco_accept_endpoint is specified on an endpoint in the old netlist. However, some of the startpoints in the transitive fanin of that endpoint are not aligned with the startpoints in the transitive fanin of the corresponding aligned endpoint in the new netlist.

WHAT NEXT

If you apply the eco_accept_endpoint to an endpoint in the old netlist, make sure that all startpoints in the transitive fanin of that endpoint are aligned with startpoints of the new netlist in the transitive fanin of the corresponding aligned endpoint.

ECO-79 (information) The following start-points in the support of end-point "%s" in the new netlist are not aligned with any start-points in the support of frozen end-point "%s" in the old netlist.

DESCRIPTION

ECO Compiler issues this message if the eco_accept_endpoint is specified on an end-point in the old netlist ("old netlist accepted end-point"), and some of the start-points in the transitive fan-in of the corresponding aligned end-point in the new netlist are not aligned with any start-points in the transitive fan-in of the end-point in the old netlist.

WHAT NEXT

ECO Compiler does allow for start-points that are unique to the cone of logic driving the end-point which is aligned with an old netlist accepted end-point. This message is issued so that you are aware of this situation just in case the set_eco_accept_endpoint command was used on an end-point unintentionally.

ECO-82 (error) Error encountered during unique directives processing.

DESCRIPTION

An error has occurred during processing of unique directives.

WHAT NEXT

Please refer to previous error messages for more information.

ECO-83 (error) Complete alignment of all ports and registers not satisfied.

DESCRIPTION

eco_analyze, **eco_implement**, and **eco_recycle** require complete alignment of all input ports, output ports and registers between the two (hierarchical) designs in **eco_current_design_pair**.

WHAT NEXT

Use **eco_align_design** on the same **eco_current_design_pair** to determine a complete alignment.

eco_align_design uses exact name alignment as well as other heuristics to determine a complete alignment of input ports, output ports, and registers.

A report is given of all alignments that are not by exact name.

The user should always review these heuristic alignments; if some are incorrect the user should apply **set_eco_align** to establish the correct alignments and re-run **eco_align_design**.

set_eco_unique must be used to indicate ports or registers that exist in only one design in **eco_current_design_pair** and thus do not align with any other port or register.

ECO-84 (info) %s objects '%s' and '%s' in designs '%s' and '%s'.

DESCRIPTION

This message indicates that ECO Compiler is "Aligning" or "Re-using" a pair of design objects. An example is:

```
Aligning objects 'reg_old' and 'reg_new' in designs   (ECO-84)
  '/system/eco/old_netlist.db' and
  '/system/eco/new_netlist.db'.
```

WHAT NEXT

This informational message can be turned off by setting environment variable **eco_directives_verbose** = false.

ECO-85 (info) Object '%s' will be considered unique in design '%s'.

DESCRIPTION

This message indicates that a port or register will be treated as unique to the given design and hence not present in the other design of the **eco_current_design_pair**.

Uniqueness is a property of a port or register with respect to a given design pair. The port or register might not be unique when the design is paired with another design. For instance, an output port of the new HDL design can be unique when paired with the old HDL design, but not when paired with the new netlist design.

WHAT NEXT

This informational message can be turned off by setting environment variable **eco_directives_verbose** = false.

ECO-86 (info) Performing %s on object '%s'.

DESCRIPTION

This message indicates that an ECO Compiler command is being performed on a design object. The commands issuing this message are **set_eco_target** and **set_eco_unique**.

WHAT NEXT

This informational message can be turned off by setting environment variable **eco_directives_verbose** = false.

ECO-87 (info) No DB reference designs for cells: '%s' and '%s'.

DESCRIPTION

The ECO Compiler command **set_eco_align** issues this message to alert you that the two mentioned cells do not have corresponding DB reference designs.

This can happen when there is an unresolved reference during **link**, or because you intentionally removed some subdesigns from dc_shell, knowing that they did not

change from the old netlist to the new netlist. In either case, ECO Compiler performs the alignment and the two cells are treated during **eco_implement** and **eco_recycle** as aligned black boxes, whose internal functions are unknown.

WHAT NEXT

See the man page for **eco_implement** for a discussion of black boxes.

ECO-88 (error) No DB reference design for %s cell '%s'.

DESCRIPTION

This error is issued by ECO Compiler command **set_eco_align**. The two arguments of **set_eco_align** must be of the same type (port, cell, register, or subdesign instance) and they must either both have DB reference designs or both not have DB reference designs. This error occurs when one argument has a DB reference and the other does not.

WHAT NEXT

Make sure that the cells with unresolved references, if any, in the **eco_current_design_pair** can be put into one-to-one correspondence. Use **set_eco_align** to identify pairs of cells with unresolved references if they do not have the same names already.

ECO-89 (error) set_eco_reuse cannot change link of unresolved reference.

DESCRIPTION

set_eco_reuse cannot handle cells with unresolved references.

WHAT NEXT

set_eco_align may be what the user intended to do if both command arguments are cells with unresolved references.

If only one command argument has an unresolved reference, then the user needs to stop the ECO process and make sure that the cells with unresolved references, if any, in the **eco_current_design_pair** can be put into one-to-one correspondence.

Use **set_eco_align** to identify pairs of cells with unresolved references if they do not have the same names already.

ECO-90 (error) Must align DesignWare cell '%s' before aligning its pins.

DESCRIPTION

ECO Compiler requires that DesignWare cells be aligned before any of their pins are aligned.

WHAT NEXT

Use **set_eco_align** to align the DesignWare cells prior to the command that issued this error message.

ECO-91 (error) The design cells are from different libraries.

DESCRIPTION

set_eco_align or **set_eco_reuse** issues this error when the two command arguments are from different libraries or are incompatible DesignWare cells. ECO Compiler is unable to verify that the cell in the old netlist can replace the cell in the new netlist.

This error prevents the possibility of logical errors occurring in the ECO result due to an erroneous replacement of one cell by another.

WHAT NEXT

set_eco_reuse can be used only on a pair of cells from the same technology library with the same DB reference design, unless both cells are DesignWare cells.

If both cells are DesignWare cells, then the following must be true:

    the input ports match by name;
    the output ports match by name;
    the inout ports match by name;
    the cells have the same DesignWare implementation.

set_eco_align can be used to align DesignWare cells that have different ports and implementations, but in this case the two cells are treated as subdesigns and all cell reuse within the new subdesign is formally verified. Cell reuse may be less than 100 percent within the subdesign. Align the cells first, then align any misnamed pin pairs, and then use **set_eco_unique** to identify any unique pins on each cell.

ECO-92 (error) One cell is Designware and the other is not.

DESCRIPTION

set_eco_align and **set_eco_reuse** cannot be used to align a DesignWare cell with a cell from a technology library.

These commands can be applied to two DesignWare cells from different libraries, as long as the following is true of the DesignWare cells:

    the input ports match by name;
    the output ports match by name;
    the inout ports match by name;
    the cells have the same DesignWare implementation.

WHAT NEXT

If you plan to use **set_eco_reuse** on DesignWare cells, read the serious warning in the Man Page first.

ECO-93 (error) Some pins on cell '%s' are not alignable by name on cell '%s':

DESCRIPTION

If both cell arguments to **set_eco_reuse** are DesignWare cells, then the following must be true:

    the input ports match by name;
    the output ports match by name;
    the inout ports match by name;
    the cells have the same DesignWare implementation.

WHAT NEXT

If the two cells are do not meet the criteria above, the user may consider using **set_eco_align** instead. **set_eco_align** can be used to align DesignWare cells that have different pins and implementations, but in this case the two cells are treated as subdesigns and all cell reuse within the new subdesign is formally verified. Cell reuse may be less than 100 percent within the subdesign.

Align the cells first, then align any misnamed pin pairs, and then use **set_eco_unique** to identify any unique pins on each cell.

ECO-94 (warning) Combinational feedback loops found in

design
'%s'.

DESCRIPTION

The **eco_analyze_design** command cannot handle designs with combinational feedback loops. No identical endpoints will be determined between the two designs in **eco_current_design_pair**. The ECO process can continue without knowledge of identical endpoints, but **eco_implement** might now take longer while functionally comparing endpoint pairs.

Also, during **eco_implement**, endpoints driven by combinational feedback loops are temporarily set to logic zero during the functional analysis process, because the underlying verification procedures cannot handle loops.

IMPORTANT: By default, if a new endpoint is aligned with an old endpoint and both are driven by loops, both are set to logic zero, and thus considered logically equivalent. This implies that the old cone of logic is copied into the new netlist, even though there might be functional design changes. Therefore, by default, ECO compiler does not expect functional design changes to affect endpoints driven by loops.

WHAT NEXT

If you know that there are changes from the old HDL to the new HDL for one of the endpoints, you must unconnect the endpoints in the old HDL and old netlist, using **disconnect_net**, so that the old and new endpoints are not, erroneously, considered equivalent.

After unconnecting the old endpoints, the new endpoints driven by loops will be treated as design changes.

Cell reuse can be reduced, but the result will be logically correct.

ECO-95 (error) Alignment not complete. Must use eco_align_design command.

DESCRIPTION

eco_implement cannot align all sourcepoints and endpoints, or there are some unique points that were not identified using **set_eco_unique**.

WHAT NEXT

The user must rerun **eco_align_design -out bad.align** for **eco_current_design** and examine the generated file, bad.align. There may be some suggested alignments and

some unalignable points that the user must either align or indicate to be unique with **set_eco_unique**. Then **eco_implement** can be run again.

ECO-96 (warning) ECO target '%s' not found in design instance '%s'.

DESCRIPTION

The *target_object* argument to **set_eco_target** could not be found. **eco_implement** will continue without any directives set for the target.

WHAT NEXT

The **current_design** should be the old netlist when applying **set_eco_target**. The target pin or port mentioned by the **set_eco_target** command should be in the old netlist. The taps mentioned may be pins or ports in the old netlist or may be input ports, register output pins, or hierarchical cell output pins in the new netlist.

Make sure the **current_design** is the old netlist before applying **set_eco_target**.

Check that the rules above are followed and re-run the command.

ECO-97 (warning) ECO tap '%s' not found in design '%s'.

DESCRIPTION

One of the objects in the *tap_objects* argument to **set_eco_target** cannot be found. The **eco_implement** command will continue as if that tap were not in the list.

WHAT NEXT

The **current_design** should be the old netlist when applying **set_eco_target**. The target pin or port mentioned by the **set_eco_target** command should be in the old netlist. The taps mentioned may be pins or ports in the old netlist or may be input ports, register output pins, or hierarchical cell output pins in the new netlist.

Make sure the **current_design** is the old netlist before applying **set_eco_target**.

Check that the rules above are followed and re-run the command.

ECO-98 (info) Boundary optimization prevents identical

endpoints computation in
'%s'.

DESCRIPTION

The subdesign mentioned has the boundary optimization attribute. This means that the new netlist and old netlist versions of the subdesign might have been optimized differently with respect to their boundaries. For instance, different constants might have been propagated down the hierarchies during **compile -boundary_optimization**. Unfortunately, no record is kept during optimization of any boundary optimizations.

The possibility of this happening prevents the utilization of Identical Endpoint information derived from the HDL designs by **eco_analyze_design**. In this case, it is not true that identical endpoints in the HDL imply equivalent implementations in the netlists, and so **eco_implement** cannot safely take advantage of such information.

Consequently, **eco_implement** might take longer to perform its various verification tasks; but the result will be logically correct.

WHAT NEXT

If you anticipate many ECOs in the future, consider not using the *boundary_optimization* option on **compile**. This ensures computation of identical endpoints during **eco_analyze_design**.

ECO-99 (info) Changing ECO subdesign instance name from %s to %s.

DESCRIPTION

During **eco_implement** the names of registers and subdesign instances are changed in the new netlist to agree with names in the old netlist. This enables incremental place and route tools that perform a netlist difference in which cells are considered the same if they have the same name.

However, you also might want to perform **compare_design** between the new HDL and the ECO netlist to ensure logical correctness of the ECO process. To handle the name changes gracefully, **eco_implement** annotates DB attributes on some cells and designs in the new netlist: "eco_inst_name," "eco_reg_name," "eco_nn_path." Later, **compare_design** reads these attributes in order to restore the original register and subdesign names, and verification proceeds as usual, with complete name agreement between sourcepoints and endpoints.

The user does not need to consider these DB attributes further.

WHAT NEXT

If verification failures occur, the user will have to interpret the failures as if the names of all registers are from the new HDL.

ECO-100 (error) -struct, -functional, -big_fish and -reusableflags are exclusive.

DESCRIPTION

Only one of -struct, -functional, -big_fish, or -reusable can be used with **eco_correspond**.

WHAT NEXT

Use only one of -struct, -functional, -big_fish, or -reusable with **eco_correspond**.

ECO-101 (error) Four designs expected as arguments.

DESCRIPTION

eco_compile expects four designs as its argument: old and new specifications and old and new implementations. For more information on the arguments to **eco_compile**, please refer to the man page for the command.

WHAT NEXT

Re-execute **eco_compile** with the proper arguments.

ECO-102 (error) Design '%s' is specified twice in the argument list.

DESCRIPTION

Design '%s' is specified more than once for **eco_compile**. Arguments to **eco_compile** must be distinct designs.

WHAT NEXT

You might want to **uniquify** the designs or specify each with a file name prefix so

that they are interpreted as distinct designs.

ECO-103 (error) Two or zero designs expected as an argument.

DESCRIPTION

eco_write_script expects as its argument zero or two designs. If no designs are specified, designs in current design pair (set through **eco_current_design_pair**) are used as arguments.

WHAT NEXT

Specify two distinct designs as arguments.

ECO-104 (error) Can’t specify -all along with designs.

DESCRIPTION

For **eco_write_script**, -all and designs are exclusive options. If -all is specified, designs cannot be specified, and if designs are specified, -all cannot be specified.

WHAT NEXT

Specify either -all or the designs.

ECO-105 (error) No directives has been specified. No script written.

DESCRIPTION

If no directives have been specified during **eco_write_script**, no script is written. At least one directive must be specified before a script is written.

WHAT NEXT

Specify directives before attempting to write out the script.

ECO-106 (error) Hierarchical names are not allowed: '%s'

DESCRIPTION

Hierarchical names are not allowed while specifying the directives.

WHAT NEXT

You must specify the designs (using **eco_current_design_pair**) before specifying the design objects.

ECO-107 (error) Parent design for object '%s' not found. Please report this message to Synopsys immediately.

DESCRIPTION

While processing the directives, parent design for object '%s' was not found. In order to associate the directives with the designs, parent design must be found. This error message identifies the need for stricter object classification.

WHAT NEXT

Please report this message to Synopsys immediately.

ECO-108 (error) Parent designs '%s' and '%s' of the specified objects have the same DB references.

DESCRIPTION

Parent designs of the objects specified (while setting the directives for ECO Compiler) have the same DB references. The parent designs must be unique designs. This problem should have been identified during other commands.

WHAT NEXT

Please report this problem to Synopsys.

ECO-109 (error) Objects '%s' and '%s' have the same DB reference, corresponding designs %s are:

'%s' and '%s'. Please notify Synopsys.

DESCRIPTION

Objects specified in the message have the same DB references. This can occur if the specified objects belong to the same design. This message identifies a need for stricter checks in other commands.

WHAT NEXT

Please notify Synopsys.

ECO-110 (error) Ports/pins '%s' and '%s' have different direction types.

DESCRIPTION

Pins or ports specified in the directives for ECO Compiler have different directions. Both the pins or both the ports must have the same direction type.

WHAT NEXT

Check the objects and their direction types and reenter the command.

ECO-111 (error) Ports/pins are not of the required type.

DESCRIPTION

There is a discrepancy between the specified direction type and the actual direction type of the specified objects.

WHAT NEXT

ECO-112 (error) Number of input/outputs are different for the specified objects.

DESCRIPTION

Objects which have different numbers of inputs or outputs cannot be reused. In order

for the objects to be reused, they must have the same number of inputs and outputs.

WHAT NEXT

Make sure that the objects to be reused have the same number of inputs and outputs.

ECO-113 (error) '%s' is an invalid category. It must be either 'first' or 'second'.

DESCRIPTION

For **set_eco_unique**, the category must be either 'first' or 'second'. For more information, please refer to the manual page for **set_eco_unique**.

WHAT NEXT

ECO-114 (error) Object '%s' not found in the design of eco pair.

DESCRIPTION

The object specified in the **set_eco_unique** command is expected to be found in the design specified by the category field (first or second). This error message indicates that the object was not found in the specified design.

WHAT NEXT

Make sure the object name and the design names are consistent in the command.

ECO-115 (error) Port '%s' is not an input port.

DESCRIPTION

Input port is expected as an argument to this command.

WHAT NEXT

ECO-116 (error) Pin '%s' is not an output pin of a cell.

DESCRIPTION

Output pin of a cell is expected as an argument to this command.

WHAT NEXT

ECO-117 (error) Object '%s' is not a pin or a port.

DESCRIPTION

A port or a pin is expected as an argument to this command.

WHAT NEXT

ECO-118 (warning) Discarding set_eco_target command not pertaining to old netlist, but to design '%s'.

DESCRIPTION

The **current_design** should be the old netlist when applying **set_eco_target**. The target pin or port mentioned by the **set_eco_target** command should be in the old netlist. The taps mentioned may be pins or ports in the old netlist or may be input ports, register output pins, or hierarchical cell output pins in the new netlist.

WHAT NEXT

Make sure the **current_design** is the old netlist before applying **set_eco_target**.

Check that the rules above are followed and re-run the command.

ECO-119 (error) The two designs have the same DB reference.

DESCRIPTION

The designs specified in the command have the same DB reference. The designs in the command are expected to be distinct designs.

WHAT NEXT

Make sure that the specified designs are unique. Refer to the **uniquify** manual page for more information on how to make designs unique within **dc_shell**.

ECO-120 (error) In the %s hierarchy, object '%s' could not be found in design '%s'.

DESCRIPTION

The mentioned object could not be found in the first (or second) design of **eco_current_design_pair**.

WHAT NEXT

The **set_eco_unique** command should only be applied to input ports, output ports, or sequential cells. The recommended methodology is to set the **eco_current_design_pair** to refer to the top-level designs of two design hierarchies and to use instance pathnames to refer to objects within subdesigns.

ECO-121 (error) Attribute not set on any object.

DESCRIPTION

While specifying directives for ECO Compiler, attributes are set on the objects specified in the commands (**set_eco_***). While processing the objects, an error was encountered and as a result the attribute was not put on any of the objects.

WHAT NEXT

ECO-122 (error) No tap points were specified to set_eco_target.

DESCRIPTION

No tap points were specified to **set_eco_target**. See the man page for a complete description of acceptable tap points.

WHAT NEXT

Add tap points to the **set_eco_target** command and rerun.

ECO-200 (warning) The design '%s' is hierarchical; no sharing of cells among different levels of hierarchy possible.

DESCRIPTION

In a hierarchical design, **eco_recycle** treats each level of hierarchy seperately. In order to substitute some new cells in one level of the logical hierarchy, only spare or obsolete cells within the same level of hierarchy are considered.

WHAT NEXT

Use **ungroup -all -flatten** to get a flat design. Then run **eco_recycle** again.

ECO-201 (warning) The design '%s' has no physical information (pdef) available.

DESCRIPTION

In order to optimize the result of **eco_recycle** with respect to cell locations physical design information is necessary. If no physical information is available the choice of cells during the recyceling process is arbitrary.

WHAT NEXT

Annotate the physical information onto the design by using **read_clusters**.

ECO-202 (error) Cannot use respect_physical_hier or respect_distance
without annotated pdef information.

DESCRIPTION

You only can use the options **respect_physical_hier** or **respect_distance** of **eco_recycle** if physical design information (pdef) is available.

WHAT NEXT

Annotate the physical information onto the design by using **read_clusters** and try again, or run **eco_recycle** whithout these options.

ECO-203 (error) Cannot find library cell of cell %s in the target library.

DESCRIPTION

During **eco_recycle** a cell without a library cell has been detected. This cell is excluded from the further recyceling process.

WHAT NEXT

Make sure that the library cell of the mentioned cell is present in the target library. Check for target library load errors.

ECO-204 (warning) No location information for cell %s available.

DESCRIPTION

Although the design has physical information available, the location information for the mentioned cell could not be found.

WHAT NEXT

Make sure the cell name mentioned in the warning message can be found in the pdef file. Watch out for warnings or errors during **read_clusters**.

ECO-205 (error) Current_design has not been set.

DESCRIPTION

eco_recycle works on the current design. The current design has not been set.

WHAT NEXT

Use **current_design** to set the design you want **eco_recycle** to work on.

ECO-206 (error) Cell %s is not a valid resource cell.

DESCRIPTION

By evaluating the resource cells of the design **eco_recycle** found a resource cell that drives a nonresource cell. Because the recycling process might pull this cell out of its current environment in order to replace a new cell, this can cause bad logic. Thus, each resource cell that drives a nonresource cell is invalidated.

WHAT NEXT

Make sure that resource cells are not within the transitive fanin of a nonresource cell.

ECO-207 (error) Missing distance value to option respect_distance.

DESCRIPTION

You specified the respect_distance option to **eco_recycle** without giving a value argument to this option.

WHAT NEXT

Call **eco_recycle** again with the appropriate distance value added right after the respect_distance option.

ECO-208 (error) Resource cell %s is driving a non-resource cell.

DESCRIPTION

By evaluating the resource (spare and obsolete) cells of the design a resource cell has been found that drives a non-resource cell. This case is currently not supported for the **eco_implement** command. Please see the user manual for a more detailed description how to use the eco_spare and eco_obsolete attributes.

WHAT NEXT

Make sure that resource cells are not within the transitive fanin of a non-resource cells. Use the **remove_attribute** command to remove eco_spare and/or eco_obsolete attributes from the mentioned cell. Then run **eco_implement** again.

ECO-220 (error) The given directive will be ignored because it already is specified.

DESCRIPTION

The given **set_eco_recycle** or **set_eco_obsolete** directive already is specified. It doesn't make any difference to specify it a second time. In order to avoid duplicates in the set of directives, it is ignored.

WHAT NEXT

In order to find out which directives are already set, use the print options to the commands **set_eco_recycle** and **set_eco_obsolete**.

ECO-221 (error) The specified directive cannot be removed because it is not in the set of already stored directives.

DESCRIPTION

The specified **set_eco_recycle** or **set_eco_obsolete** directive cannot be found in the list of already set directives. Hence, the given remove command cannot be performed.

WHAT NEXT

To find out which directives are currently set, use the print options to the commands **set_eco_recycle** and **set_eco_obsolete**.

ECO-222 (error) The specified directive cannot be applied because the cell %s is not found in the current design.

DESCRIPTION

The cell specified by the **set_eco_recycle** or **set_eco_obsolete** directive is not found in the current design. The specified directive cannot be set.

WHAT NEXT

Use the **find** command to check whether the specified cell can be found in the design.

ECO-223 (error) The recycle directive for cell %s and cell %s cannot be applied because the cells are in different categories.

DESCRIPTION

The cells specified by the **set_eco_recycle** directive are of different categories. **eco_recycle** distinguishes cells into the three categories: combinational, sequential and special cells. (For a detailed discussion about cell categories, see the user manual.) It is only possible to substitute cells in the same category. For instance, one cell of the pair you specified might be a sequential cell the other a combinational one.

WHAT NEXT

Check the type of the specified cells and make sure they are within the same category.

ECO-224 (error) The specified cell %s is not a resource cell.

DESCRIPTION

set_eco_recycle -set requires two cell names as arguments. The first name needs to point to a new cell, the second two a resource cell. The second name of the specified **set_eco_recycle** command doesn’t point to a resource cell.

WHAT NEXT

Check the db_cell attributes of the resource cell; it needs to have either the *eco_spare* or the *eco_obsolete* attribute attached. (For further requirements for resource cells see the user manual.)

ECO-225 (error) The specified cell %s is not a new cell.

DESCRIPTION

set_eco_recycle -set requires two cell names as arguments. The first name needs to point to a new cell, the second two a resource cell. The first name of the specified **set_eco_recycle** command doesn't point to a new cell.

WHAT NEXT

Check the db_cell attributes of the new cell; it can't have an *eco_spare*, an *eco_obsolete*, or an *eco_old* attribute attached to it.

ECO-226 (error) The specified cell %s is not an old or a recycled cell.

DESCRIPTION

The **set_eco_obsolete -set** command requires as arguments a name of an old or a recycled cell and optionally a new name for this cell. The specified name for the old or recycled cell doesn't actually point to an old or recycled cell.

WHAT NEXT

Check the db_cell attributes of the old or recycled cell, it should have the eco_old or eco_recycle attribute attached.

ECO-227 (warning) The **set_eco_obsolete** doesn't provide a new name. A new name will be automatically generated.

DESCRIPTION

The specified **set_eco_obsolete -set** command doesn't provide a new name as an argument to the command. At runtime of **eco_recycle**, a new name for the new cell is automatically generated.

WHAT NEXT

If you want to refer to the new cell in following directives, use the new name option to specify a name to give to the new cell.

ECO-228 (warning) The specified new name %s is not unique in the design.

DESCRIPTION

The directive couldn’t be accepted because the specified new name of the **set_eco_obsolete -set** command is not unique in the current design. There is already a cell with this name present.

WHAT NEXT

Use the **find** command to check whether a name is unique to the design. Retry the command with a unique name.

ECO-229 (warning) Skipping directive because specified resource cell %s is already used.

DESCRIPTION

The resource cell specified by the recycle directive is already used. The reason for this might be a previous directive for the same resource cell which has been successfully applied already.

WHAT NEXT

ECO-230 (warning) Skipping directive because the specified new cell %s is already mapped.

DESCRIPTION

The new cell specified by the recycle directive is already mapped. The reason for this might be a previous directive for the same new cell which has been successfully applied already.

WHAT NEXT

ECO-231 (error) The directive couldn’t be applied because the new cell %s and the resource cell %s are not in the same level

of the hierarchy

DESCRIPTION

The new and the resource cell specified by the recycle directive are not within the same level of the logical hierarchy. Cells cannot be recycled across different levels of the hierarchy.

WHAT NEXT

If the user wants to recycle cells among different levels of the hierarchy the hierarchy needs to be flattened up to the common root level of both hierarchies.

ECO-232 (Warning) The new cell %s couldn’t be mapped to the resource cell %s because it has more inputs than the resource cell.

DESCRIPTION

To force map a new cell to a resource cell the number of inputs of the resource cell must be at least as high as the number of inputs of the new cell. For a more detailed discussion about force mapping technology see the user manual

WHAT NEXT

ECO-233 (error) The directive couldn’t be applied because the directive specified multiple output gates.

DESCRIPTION

WHAT NEXT

ECO-234 (Warning) The new cell %s couldn’t be mapped to the resource cell %s because there are not enough inverters

available.

DESCRIPTION

Force mapping tries to use inverters at the inputs or the outputs of the resource cell in order to reproduce the functionality of the new cell. In this case, the desired functionality can be reproduced, but the inverters are not available. The substitution cannot be performed.

WHAT NEXT

Give another directive that doesn't require that many inverters to perform the force mapping, or, if possible, instantiate more inverters in the pool of resource cells.

ECO-235 (error) Force mapping of the resource cell %s to the new cell %s is impossible.

DESCRIPTION

The new and the resource cell specified by the recycle directive cannot be force mapped into each other. (To get a more detailed description about the capabilities of the force mapping see the user manual).

WHAT NEXT

ECO-236 (Warning) The specified new cell %s could not be found.

DESCRIPTION

The specified new cell of the **set_eco_recycle** command could not be found in the design. At runtime of **eco_recycle** this directive will cause an error and the command to terminate unless a further **set_eco_obsolete** directive would create a new cell of the given name.

WHAT NEXT

Make sure that the specified name is correct and a cell with that name can be found in the design. If you plan to issue an **set_eco_obsolete** command which will generate a new cell with the specified name you can ignore this error message.

ECO-237 (Warning) The specified new cell %s is not a new cell.

DESCRIPTION

The specified new cell of the **set_eco_recycle** command is either a resource cell or an already reused cell. Only new cells are allowed as the second string argument of **set_eco_recycle**. At runtime of **eco_recycle** this directive will cause an error and the command to terminate.

WHAT NEXT

Check the db_attributes on the specified cell. It is not allowed to have an *eco_old*, an *eco_spare*, or an *eco_obsolete* attribute. You might want to use the **set_eco_obsolete** command in order to turn an already reused cell into a new cell. You might use the remove option to **set_eco_recycle** in order to remove an incorrect directive.

ECO-238 (Warning) The specified resource cell %s could not be found.

DESCRIPTION

The specified resource cell of the **set_eco_recycle** command could not be found in the design. At runtime of **eco_recycle**, this directive will cause an error, and the command will terminate unless a further **set_eco_obsolete** directive creates a resource cell of the given name.

WHAT NEXT

Make sure that the specified name is correct and that a cell with that name can be found in the design. If you plan to apply an **set_eco_obsolete** command that will generate a resource cell with the specified name, then you can ignore this error message.

ECO-239 (Warning) The specified resource cell %s is not a resource cell.

DESCRIPTION

The specified resource cell of the **set_eco_recycle** command is either a new cell or an already reused cell. Only resource cells are allowed as the first string argument of **set_eco_recycle**. At runtime of **eco_recycle**, this directive will cause an error, and the command will terminate unless a further **set_eco_obsolete** directive creates a

resource cell of the given name.

WHAT NEXT

Make sure that the specified name is correct and that a cell with that name can be found in the design. If you plan to apply an **set_eco_obsolete** command that will generate a resource cell with the specified name, then you can ignore this error message. You might also use the remove option of **set_eco_obsolete** to remove incorrect directives.

ECO-240 (Error) The specified cell %s is not a reused cell.

DESCRIPTION

The specified reused cell of the **set_eco_obsolete** command is not a reused cell. Only reused cells are allowed as the first string argument of **set_eco_obsolete**.

WHAT NEXT

Make sure that the specified cell is a reused cell and is marked with the *eco_old* attribute.

ECO-241 (Error) The specified new name %s is already used.

DESCRIPTION

The given new name for the new cell is not unique, it is already used for another cell in the design.

WHAT NEXT

Use the find command to check whether a specific name is already used in the design. By omitting the new name argument, a unique new name is automatically generated.

ECO-242 (Error) The set_eco_obsolete command requires a cell name as an option .

DESCRIPTION

The command **set_eco_recycle** requires the user to give the cell name of a reused or an already recycled cell as an option. This cell name has not been given as an

argument to the command.

WHAT NEXT

Specify the name of a reused or recycled cell as an argument to the **set_eco_obsolete** command.

ECO-243 (Error) The set_eco_recycle command requires as arguments the name of a new cell as well as the name of a resource cell.

DESCRIPTION

The **set_eco_recycle** command has been invoked without giving the cell name arguments. The command requires as arguments first the name of a new cell and second the name of a resource cell. At least one of those arguments is missing.

WHAT NEXT

Specify the name of a new cell as well as the name of a resource cell as arguments to the **set_eco_recycle** command.

ECO-300 (warning) Removing dont_touch attribute from design '%s'.

DESCRIPTION

If eco_recycle sees a dont_touch attribute on a design it automatically removes it. This avoids generation of inconsistent designs after writing the design to db after finishing the eco_recycle command. In general the ECO commands don't respect dont_touches.

WHAT NEXT

If you want to exclude a design or a single cell from the recycling process you can use the eco_dont_recycle attribute on the design or on a single cell instance.

EDFN-1 (warning) Line %d: A port is declared without a name. Using "DUMMY_NAME_xx".

DESCRIPTION

You receive this warning message to inform you that the specified line in the EDIF input file contains a port declaration without a name. In such a case, the system automatically generates a dummy name "DUMMY_NAME_xx".

WHAT NEXT

You can accept the dummy name temporarily, but for correctness and to avoid receiving this warning message in the future, edit your EDIF input file so that the specified line contains a port delcaration with a name.

EDFN-2 (error) Line %d: Too few elements in %s form.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and detects the required elements for the specified EDIF construct are missing.

WHAT NEXT

The EDIF file is probably corrupted. The recommended solution is to regenerate the EDIF file. However, if you know EDIF and the design well, refer to the line number in the error message and fill in the missing information.

EXAMPLES

```
   ...
5   (library DESIGN (edifLevel 0) (technology (numberDefinition))
6     (cell size1 (cellType GENERIC)
7       (view Netlist_representation (viewType NETLIST)
8       (contents
         ...
```

EXAMPLE MESSAGE

```
Error: Line 7: Too few elements in 'view' form. (EDFN-2)
```

In the above example, the required interface form is missing from the view form. Below is an example of a complete view form.

```
   ...
   (library DESIGN (edifLevel 0) (technology (numberDefinition))
6     (cell size1 (cellType GENERIC)
7       (view Netlist_representation (viewType NETLIST)
        (interface
          (port a (direction INPUT))
          ...
18       (contents
         ...
```

EDFN-3 (error) Line %d: Incorrect number of elements in %s form.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and detects that the number of required elements for a certain EDIF construct is incorrect.

WHAT NEXT

The EDIF file is probably corrupted due to manual editing. The recommended solution is to regenerate the EDIF file. However, if you know EDIF and the design well, refer to the line number in the error message and change the number of required elements to the correct number.

EXAMPLES

```
1 (edif Synopsys_edif (edifVersion 2 0 0 0)
2   (edifLevel 0)
   ...
```

EXAMPLE MESSAGE

```
Error: Line 1: Incorrect number of elements in 'edifVersion' form. (EDFN-3)
```

In the above example, the edifVersion construct on line has 5 elements total. Only four elements are required (edifVersion 2 0 0). Below is a correct example.

```
1 (edif Synopsys_edif (edifVersion 2 0 0)
2   (edifLevel 0)
   ...
```

EDFN-4 (error) Line %d: Expected a list.

DESCRIPTION

Obsolete

WHAT NEXT

Obsolete

EDFN-5 (warning) Line %d: Unknown function is being ignored.

DESCRIPTION

The EDIF reader is not able to verify the function on the line specified in the error message.

WHAT NEXT

Fix the EDIF input file and make sure all of the functions are properly defined.

EDFN-6 (error) Line %d: Expected a parenthesis.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters a syntax error.

WHAT NEXT

Refer to the line number in the error message and locate the missing parenthesis. You can fix the problem by regenerating the EDIF file and reimport, or if you know EDIF well, you can correct the problem.

EXAMPLES

```
1 (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
```

```
2  (keywordMap (keywordLevel 0)) status)
    ...
```

EXAMPLE MESSAGE

```
Error: Line 2: Expected a parenthesis (EDFN-6)
```

In the above example, the parenthesis which marks the beginning of the "status" construct is missing.

EDFN-7 (error) Line %d: Expected a non-empty list.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters a set of parenthesis () with nothing inside.

WHAT NEXT

The edif file is probably corrupted. You can regenerate the EDIF input file or take out the empty set of parenthesis in the EDIF file. Reimport the EDIF input file into dc_shell.

EXAMPLES

```
(edif Synopsys_edif (edifVesion 2 0 0) () (edifLevel 0)
 (keywordMap (keywordLevel 0)) (status)
..
```

EXAMPLE MESSAGE

```
Error: Line 1: Expected a non-empty list. (EDFN-7)
```

In the above example, there is an empty set of parenthesis after the edifVersion construct on line one.

EDFN-8 (warning) Line %d: Multiple views not supported. View '%s' of cell '%s' ignored.

DESCRIPTION

The EDIF reader does not support cells with multiple views. The reader processes the first view it finds and ignores the rest of the views.

WHAT NEXT

Fix the EDIF input file so that it does not contain cells with multiple views.

EDFN-9 (error) Line %d: Can not add the design to the root.

DESCRIPTION

Obsolete

WHAT NEXT

Obsolete

EDFN-10 (error) Line %d: Instance specified without cell ref in view ref.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters an EDIF cell-instantiated construct that fails to specify its reference.

WHAT NEXT

The recommended solution is to locate the construct that instantiates the cell. Fix the construct at the source and regenerate the EDIF file. If you know EDIF and the design well, locate the construct that instantiates the cell, and include the correct cell references for the design.

EXAMPLES

```
1 (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
    ...
4    (cell or2 (cellType GENERIC)
5       (view Netlist_representation (viewType NETLIST)
        ... ))
15   (library DESIGNS (edifLevel 0) (technology (numberDefinition))
16     (cell size1 (cellType GENERIC)
         ...
24       (contents
25         (instance pcell2
26           (portInstance YA (property PIN_PR (string "better")))
            ...
           ))))))
```

EXAMPLE MESSAGE

```
Error: Line 25: Instance specified without cell ref in view ref. (EDFN-10)
```

In the above example (line 25), the instance pcell2 is instantiated, but its reference is not specified. Below is a correct example of an instantiated instance. You should instantiate an instance with its source, which includes a view reference (line 26 below), cell reference (line 27 below), and library reference (line 28 below).

```
1 (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
     ...
4    (cell or2 (cellType GENERIC)
5       (view Netlist_representation (viewType NETLIST)
        ... ))
14   )
15   (library DESIGNS (edifLevel 0) (technology (numberDefinition))
16     (cell size1 (cellType GENERIC)
         ...
24       (contents
25         (instance pcell2
26           (viewRef Netlist_representation
27             (cellRef or2
28               (libraryRef size1_lib)
29             )
30           )
            ...
```

EDFN-11 (error) Line %d: Can not find the design %s of the cell.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters a reference to a non-existing design. This usually happens when the user set the edifin_view_identifier_property_name to a non-existing design , and have cell instantiation whose property name is the same as the edifin_view_identifier_property_name.

WHAT NEXT

To get pass this problem, you can either do not use the edifin_view_identifier_property_name flag or regenerate the EDIF file. Or if you know EDIF and the design well, you can include a property id (should have the same id as the edifin_view_identifier_property_name) to the interface of the desired design.

EXAMPLES

```
>dc_shell edifin_view_identifier_property_name = "COMP"
```

```
"COMP"
read -format edif view2.iedif

   ...
55   (cell (rename CASE_TEST "case_test") (cellType GENERIC)
56   (view ONE (viewType SCHEMATIC)
57     (interface
       ...
200       (property (rename COMP2 "COMP2") (string "COMP2_ALREADY_DEFINED"))
       ...
300       (instance test (viewRef ONE (cellRef CASE_TEST))
         ...
350          (property (rename COMP "COMP")
351            (string (stringDisplay "COMP_ALREADY_DEFINED"
         ...
```

EXAMPLE MESSAGE

```
Error: Line 1214: Can’t find the design COMP_ALREADY_DEFINED of the cell. (EDFN-11)
```

In the above example, the flag edifin_view_identifier_property_name is set to "COMP", and view ONE (line 56) of cell CASE_TEST (line 55) has a property id of COMP2 (line 200). Later, when cell "test" is instantiated (line 300), it references the property id "COMP" (line 350). Below is a fix to this problem. Change the propery id on line 200 to "COMP".

```
... 55 (cell (rename CASE_TEST "case_test") (cellType GENERIC) 56 (view ONE
(viewType SCHEMATIC) 57 (interface ... 200 (property (rename COMP "COMP") (string
"COMP_ALREADY_DEFINED")) ... 300 (instance test (viewRef ONE (cellRef CASE_TEST))
... 350 (property (rename COMP "COMP") 351 (string (stringDisplay
"COMP_ALREADY_DEFINED" ...
```

EDFN-12 (error) Line %d: Cannot add the cell reference to the design.

DESCRIPTION

The system is not able to find the reference of the cell.

WHAT NEXT

Make sure the cell reference exists.

EDFN-13 (error) Line %d: Cell ref specified that is not defined in

this file.

DESCRIPTION

WHAT NEXT

Obsolete

WHAT NEXT

Obsolete

EDFN-14 (warning) Line %d: Duplicate instance ’%s’ renamed as ’%s’ in design ’%s’.

DESCRIPTION

The system detected duplication of cell instances, and it renamed the second instance "instanceName_xx".

WHAT NEXT

Fix the EDIF input file so that it does not contain any duplicate identifiers.

EDFN-15 (error) Line %d: Can not add the instance to the design.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters either memory issue or there are duplicate instance names in the design.

WHAT NEXT

Refer to the line number in the error message and locate the problem by looking for the instance name. First, make sure all of the instance names in your design are unique. If the instance names in your design are not unique, fix your design so that all of the instance names are unique within your design. Reimport the EDIF file. If the problem persists, pleace contact Synopsys help line.

EDFN-16 (error) Line %d: Cannot build the array specification.

DESCRIPTION

The system is not able to build an array specification.

WHAT NEXT

Check the syntax of the array on the line specified in the error message.

EDFN-17 (error) Line %d: Cannot build the symbol specification.

DESCRIPTION

Obsolete

WHAT NEXT

Obsolete

EDFN-18 (error) Line %d: Cannot add the nets.

DESCRIPTION

The system is not able to create an object for the bussed net due either to a memory issue, incorrect syntax on the bussed net construct, or incorrect syntax on the construct prior to the specified bussed net.

WHAT NEXT

Re-execute the command, or check the syntax of the EDIF input file.

EDFN-19 (error) Line %d: Cannot add the net.

DESCRIPTION

The system is not able to build an object for the net on the line specified in the error message due to incorrect syntax of the specified net construct, or incorrect syntax of the constructs prior to the net.

WHAT NEXT

Check the syntax of the EDIF input file.

EDFN-20 (error) Line %d: Cannot add the net to the design.

DESCRIPTION

The system is not able to create a db net object due to a memory issue or a conflict in the net name.

WHAT NEXT

Check to make sure there is no conflict in the net name, or re-execute the command to see if the system is able to create a db net object.

EDFN-21 (error) Line %d: Cannot connect the object to the net.

DESCRIPTION

The system is not able to connect design objects in a netlist.

WHAT NEXT

Check the schematic of the design to see if the objects are from two different designs.

EDFN-22 (error) Line %d: Port or instance reference count exceeds net array size.

DESCRIPTION

The EDIF reader issues this error message when it parses the EDIF file and encounters a net array joining a list of ports or instances bigger than its size.

WHAT NEXT

Refer to the line number in the error message and locate the error. Regenerate and re-import the EDIF input file.

EXAMPLES

```
  ...
150   (net (array (rename u3_B_3_0_ "u3/B[3:0]") 4)
151     (joined (portRef B_3_0_ (instanceRef u3))
152      (portList
153        (portRef (member bus_end 0) (instanceRef Ripper_1))
154        (portRef (member bus_end 1) (instanceRef Ripper_1))
155        (portRef (member bus_end 2) (instanceRef Ripper_1))
156        (portRef (member bus_end 3) (instanceRef Ripper_1))
157        (portRef (member bus_end 3) (instanceRef Ripper_1))
   ...
```

EXAMPLE MESSAGE

```
Error: Line 157: Port or instance reference count exceeds net array size. (EDFN-22)
```

In the above example, net u3_B_3_0 is a net array of size 4, but the portList it is joining is a list of 5 ports.

EDFN-23 (error) Line %d: Port is not an array member.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters a port member reference, which is previously defined as a symbol port. Port member referencing is only used with port array. The referenced port is part of a cell whose type is GENERIC.

WHAT NEXT

Refer to the line number in the error message and locate the incorrect port reference. Fix the problem in the source, regenerate and reimport the EDIF input file. However, if you know EDIF and your design well, you can take a look at the port definition and reference and fix the problem.

EXAMPLES

```
    ...
50  (cell Test (cellType GENERIC)
51   (view Netlist_representation (viewType NETLIST)
52    (interface (port CI (direction INPUT)) (port CO (direction OUTPUT))
53     (port (array (rename DIFF_6_0_ "DIFF[6:0]") 7) (direction OUTPUT))
54     (port tmp (direction OUTPUT))
    ...
100     (net n5
101      (joined (portRef (member DIFF_6_0_ 6)) (portRef P20 (instanceRef U3))
102              (portRef (member tmp 0)))
     ...
```

EXAMPLE MESSAGE

```
Error: Line 102: Port is not an array member. (EDFN-23)
```

In the above example, cell "Test" is of type GENERIC (line 50), it contains a port "tmp" of symbol type. Line 102, the symbol type port "tmp" is being reference through a member construct.

```
... 50 (cell Test (cellType GENERIC) 51 (view Netlist_representation (viewType
NETLIST) 52 (interface (port CI (direction INPUT)) (port CO (direction OUTPUT)) 53
(port (array (rename DIFF_6_0_ "DIFF[6:0]") 7) (direction OUTPUT)) 54 (port tmp
(direction OUTPUT)) ... 100 (net n5 101 (joined (portRef (member DIFF_6_0_ 6))
(portRef P20 (instanceRef U3)) 102 (portRef (member tmp 0))) ...
```

EDFN-24 (error) Line %d: Port reference %s count of %d exceeds net size.

DESCRIPTION

The EDIF reader issues this error message when it reads the EDIF input file with the old_ripper_reading flag set to true, and encounters a ripper with difference size pins. Synopsys EDIF reader only support ripper with two of the same size pins.

WHAT NEXT

Locate the problem by referring to the line number in the error message. You might need to change you source so that your design only contains rippers with two pins of the same width. Regenerate and reimport the EDIF input file.

EXAMPLES

```
...
(cell (rename rip_1x1 "rip_1x1") (cellType RIPPER)
(view (rename Schematic_representation "Schematic_representation")
 (viewType SCHEMATIC)
 (interface (port (array (rename bundle "bundle") 512))
  (port (array (rename wire "wire") 513))
  (joined (portRef bundle) (portRef wire))
...
```

EXAMPLE MESSAGE

```
dc_shell > edifin_old_ripper_reading = t dc_shell > read -f edif size1.edif Loading
edif file 'size1.edif' Error: Line 161: Port reference wire count of 513 exceeds net
size. (EDFN-24)
```

In the above example, a ripper with two pins of different widths 512 and 513 is defined.

EDFN-25 (warning) Line %d: The net %s is not an array.

DESCRIPTION

The EDIF reader detected that the design contains a connection between a bussed port and a single net.

WHAT NEXT

Fix the EDIF input file, and make sure that the connections are properly made.

EDFN-26 (error) Line %d: Instance is not an array member.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters an array member referencing of an instance, which is previously defined as a symbol instance. Instance member referencing is only used with instance array.

WHAT NEXT

Refer to the line number in the error message and locate the incorrect instance reference. Fix the problem in the source, regenerate and reimport the EDIF input file. However, if you know EDIF and your design well, you can take a look at the instance definition and reference and fix the problem.

EXAMPLES

```
      ...
50    (instance (rename Ripper_2 "Ripper_2")
51      (viewRef Schematic_representation
52       (cellRef rip_1x1 (libraryRef genlib_rip1x1))
      ...
100     (net (rename out0)
101       (joined (portRef (member wire 0) (instanceRef (member Ripper_2 0))) (port
Ref out0))
      ...
```

EXAMPLE MESSAGE

Error: Line 101: Instance is not an array member. (EDFN-26)

In the above example, instance Ripper_2 is an instantiation of cell rip_1x1, and it is a symbol type instance (line 50). The instance Ripper_2 is referenced in line 101 with the member construct. Below is an correct example of cell instantiation and instance reference.

```
... 50 (instance (rename Ripper_2 "Ripper_2") 51 (viewRef Schematic_representation
52 (cellRef rip_1x1 (libraryRef genlib_rip1x1)) ... 100 (net (rename out0) 101
(joined (portRef (member wire 0) (instanceRef Ripper_2 )) (portRef out0)) ...
```

EDFN-27 (error) Line %d: Instance reference count exceeds net array size.

DESCRIPTION

The EDIF reader issues this error when it reads the EDIF input file and encounters a net array is referencing an instance array of bigger size.

WHAT NEXT

Refer to the line number in the error message and check out the array sizes of the net array and the referenced instance array. Fix the source, regenerate and reimport the EDIF input file. However, if you know EDIF and your design well, you can fix the problem by changing to the correct array size.

EXAMPLES

```
     ...
50   (instance (array (rename Ripper_2 "Ripper_2") 2)
51   (viewRef Schematic_representation
      ...
100   (net
101     (array (rename in_0_1_) 1)
102       (joined (portRef bundle (instanceRef Ripper_2))
103         (portRef bundle (instanceRef Ripper_1)) (portRef in)
          ...
```

EXAMPLE MESSAGE

Error: Line 102: Instance reference count exceeds net array size. (EDFN-27)

In the above example, (line 102) the net array of size 1 "in_0_1_" is referencing an instance an instance array of size 2. The array instance is defined in line 50.

EDFN-28 (error) Line %d: Nets cannot be connected to an array of ports on an array of instances.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters

nets which connect to an array of ports on an array of instances. Nets can only connect to an array of ports on individual member of an instance array. See the below example.

WHAT NEXT

Refer to the line number in the error message and locate the net(s) which have the illegal connections, fix the source and regenerate the EDIF file. Alternatively, if you know EDIF and the design well, you can fix the problem by fixing the EDIF input file. Instead of referencing the whole instance array, you can individually reference each member of the instance array.

EXAMPLES

```
     ...
50    (cell ripper (cellType RIPPER)
51      (view Schematic_representation (viewType SCHEMATIC)
52        (interface (port (array bus_end 4)) (port (array w 4))
53          (joined (portRef bus_end) (portRef w))
     ...
100    (instance (array Ripper_1234 4)
101       (viewRef Schematic_representation
102        (cellRef ripper (libraryRef generic_sdb))
     ...
150    (net (array (rename SUM_0_3_ "SUM") 4)
151       (joined (portRef SUM_0_3_)
152        (portRef bus_end (instanceRef Ripper_1234))
       )
     ...
```

ERROR MESSAGE

Error: Line 152: Nets cannot be connected to an array of ports on an array of instances. (EDFN-28)

In the above example, net array SUM_0_3_ is referencing port array bus_end of instance array Ripper_1234 (lilne 152). Instead of referencing the whole array, you can reference each member of the instance array.

... 50 (cell ripper (cellType RIPPER) 51 (view Schematic_representation (viewType SCHEMATIC) 52 (interface (port (array bus_end 4)) (port (array w 4)) 53 (joined (portRef bus_end) (portRef w)) ... 100 (instance (array Ripper_1234 4) 101 (viewRef Schematic_representation 102 (cellRef ripper (libraryRef generic_sdb)) ... 150 (net (array (rename SUM_0_3_ "SUM") 4) 151 (joined (portRef SUM_0_3_) 152 (portRef bus_end (instanceRef (member Ripper_1234 0))) 153 (portRef bus_end (instanceRef (member Ripper_1234 1))) 154 (portRef bus_end (instanceRef (member Ripper_1234 2))) 155 (portRef bus_end (instanceRef (member Ripper_1234 39)))) ...

EDFN-29 (error) Line %d: Can not find the pin on the cell.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters a pin reference in a design with multiple views. The EDIF reader only processes the first view and ignore other views. The system will not be able to find the pins on the views which are being ignored.

WHAT NEXT

Regenerate the EDIF input file so that each design contains only one view, and re-import.

EXAMPLES

```
  ...
100  (cell case_test
   ...
105   (view ONE (viewType SCHEMATIC
106     (interface
107       (port A (direction INPUT))
108       (port B (direction OUTPUT))
109       (property (rename COMP "COMP")
110         (string "ALREADY DEFINED COMP")))
111   (view TWO (viewType SCHEMATIC
112     (interface
113       (port C (direction INPUT))
114       (port D (direction OUTPUT))
115       (property (rename COMP "COMP")
116         (string "ALREADY DEFINED COMP"))
      ...
150      (instance test (viewRef ONE (cellRef case_test))
      ...
172      (net a (joined
173        (portRef C (instanceRef test
      ...
```

EXAMPLE MESSAGE

```
dc_shell > edifin_view_identifier_property_name = "COMP" "COMP"

read -f edif size1.edif Loading edif file '/remote/dtg245/anguyen/Test/Temp/
size1.edif' Error: Line 173: Can not find the pin on the cell. (EDFN-29)
```

In the above example, pin C of cell case_test view TWO is referenced in line 172, the system ignores the second view, therefore it cannot find pin C.

EDFN-30 (error) Line %d: Port (on instance) reference count

exceeds net array size.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters a net array which has a reference to a port array of bigger size.

WHAT NEXT

Refer to the line number in the error message, and locate the net array which caused the EDIF reader to issue this error message, and see what port array(s) it is referencing. Check out the size of the net array and the referenced port array(s). You can regenerate and reimport the EDIF input file, or if you know EDIF and your design well, you can change the array size to the correct size.

EXAMPLES

```
... 50 (interface (port (array (rename bundle "bundle") 2)) 51 (port (array (rename
wire "wire") 2)) 52 (joined (portRef bundle) (portRef wire) ... 250 (net (array
in_0_1_ 1) 252 (joined (portRef bundle (instanceRef Ripper_1)) 253 (portRef bundle
(instanceRef Ripper_2)) (portRef in) ...
```

EXAMPLE MESSAGE

```
Error: Line 251: Port (on instance) reference count exceeds net array size. (EDFN-
30)
```

In the above example, net array in_0_1_ of size 1 (line 250) is referencing the port array bundle which is defined to be a port array of size 2 (line 50), in this case, it is probably a typo. The correct example would be:

```
... 50 (interface (port (array (rename bundle "bundle") 2)) 51 (port (array (rename
wire "wire") 2)) 52 (joined (portRef bundle) (portRef wire) ... 250 (net (array
in_0_1_ 2) 252 (joined (portRef bundle (instanceRef Ripper_1)) 253 (portRef bundle
(instanceRef Ripper_2)) (portRef in) ...
```

EDFN-31 (error) Line %d: Net array size exceeds port reference count.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters a net array which has a reference to a port array of smaller size.

WHAT NEXT

Refer to the line number in the error message, and locate the net array which caused the EDIF reader to issue this error message, and see what port array(s) it is referencing. Check out the size of the net array and the referenced port array(s). You can regenerate and reimport the EDIF input file, or if you know EDIF and your design well, you can change the array size to the correct size.

EXAMPLES

```
... 50 (interface (port (array (rename bundle "bundle") 2)) 51 (port (array (rename
wire "wire") 2)) 52 (joined (portRef bundle) (portRef wire) ... 250 (net (array
in_0_1_ 3) 252 (joined (portRef bundle (instanceRef Ripper_1)) 253 (portRef bundle
(instanceRef Ripper_2)) (portRef in) ...
```

EXAMPLE MESSAGE

```
Error: Line 250: Net array size exceeds port reference count. (EDFN-31)
```

In the above example, net array in_0_1_ of size 3 (line 250) is referencing the port array bundle w hich is defined to be a port array of size 2 (line 50), in this case, it is probably a typo. The c orrect example would be:

```
... 50 (interface (port (array (rename bundle "bundle") 2)) 51 (port (array (rename
wire "wire") 2)) 52 (joined (portRef bundle) (portRef wire) ... 250 (net (array
in_0_1_ 2) 252 (joined (portRef bundle (instanceRef Ripper_1)) 253 (portRef bundle
(instanceRef Ripper_2)) (portRef in) ...
```

EDFN-32 (error) Line %d: Can not add the port.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters problem with port definition.

WHAT NEXT

Refer to the line in the error message, and pay attention to the errors or warnings regarding the port mentioned in the error message. Regenerate the EDIF input file or fix the port definition, and reimport the EDIF input file.

EXAMPLES

```
... 50 (cell EO (cellType GENERIC) 51 (view Schematic_representation (viewType
SCHEMATIC) 52 (interface (port A (direction INPUTA)) (port B (direction INPUT)) 53
(port Z (direction OUTPUT)) ...
```

EXAMPLE MESSAGE

```
Error: Line 52: unrecognized port direction: INPUTA. (EDFN-33) Error: Line 52: Can
not add the port. (EDFN-32)
```

In the above example, the direction for port A is incorrectly defined "INPUTA" (line 52). The port direction can only be "inout", "input", or "output". The system is not able to create a port object, and issue an error.

EDFN-33 (error) Line %d: unrecognized keyword: %s.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters a non EDIF keyword after a left parenthesis.

WHAT NEXT

Refer to the line number in the error message and locate the incorrect EDIF keyword. You can either regenerate the EDIF input file and reimport, if you know what keyword it is supposed to be, then fix it and reimport the EDIF input file.

EXAMPLES

```
  (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
    (keywordMap (keywordLevela 0)) (status)
      (library (rename generic_sdb "generic.sdb") (edifLevel 0)
       (technology (numberDefinition (scale 1 (e 496094 -11)
   ...
```

EXAMPLE MESSAGE

```
Error: Line 2: unrecognized keyword: keywordLevela. (EDFN-33)
```

In the above example, there is a typo in "keywordLevela" (line 2), the correct keyword should be "keywordLevel".

EDFN-34 (error) Line %d: Can not add the port to the design.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters some internal problem.

WHAT NEXT

Restart the command, if the problem persists please contact Synopsys' help line.

EDFN-35 (error) Line %d: Cannot add the power or ground cell to the design.

DESCRIPTION

The EDIF reader issues this error when the system is not able to create a power or ground db object.

WHAT NEXT

Check to see if the reference for power and for the ground cell exists.

EDFN-36 (error) Line %d: Cannot add the power or ground net to the design.

DESCRIPTION

The EDIF reader issues this error when the system is not able to create a power or ground db net object.

WHAT NEXT

Re-execute the command.

EDFN-37 (error) Line %d: Cannot add the array.

DESCRIPTION

The system is not able to create an array object due to an unknown bus type or illegal range.

WHAT NEXT

Go to the line number in the error message and check the array, its type, and its range.

EDFN-38 (error) Line %d: Index array value exceeds bounding array value.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters a port member reference with the index bigger than the array size. If the array size is 8, its port member indexes should be from 0:7.

WHAT NEXT

Refer to the line number in the error message, and locate the port member index which causes the EDIF reader to issue this error. You can either regenrate the EDIF input file, or if you know EDIF and your design well, fix the port member index, and reimport the EDIF file.

EXAMPLES

```
     ...
50    (cell ripper (cellType RIPPER)
51      (view Schematic_representation (viewType SCHEMATIC)
52        (interface (port (array bus_end 4)) (port (array w 4))
53          (joined (portRef bus_end) (portRef w))
     ...
100    (instance (array Ripper_1234 4)
101       (viewRef Schematic_representation
102        (cellRef ripper (libraryRef generic_sdb))
     ...
150    (net (array (rename SUM_0_3_ "SUM") 4)
151       (joined (portRef SUM_0_3_)
152        (portRef bus_end (instanceRef (member Ripper_1234 4)))
       )
     ...
```

ERROR MESSAGE

```
Error: Line 152: Net array size exceeds port reference count. (EDFN-31)
```

In the above example, instance Ripper_1234 is an array of 4, therefore its indexes should go from 0 to 3. There is a reference to the instance Ripper_1234 on line 125 with the index of 4.

EDFN-39 (error) Line %d: multiple definition of %s '%s' in %s '%s', or there is a missing construct prior to the specified EDIF

construct.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and detects multiple definitions of libraries, cells, ports, pages, or other constructs within the same scope. The system also issues this error message when there is a missing construct. For instance, the edifLevel and technology constructs are the required constructs for the EDIF library construct, and if the technology construct is missing, the system will issue this error.

WHAT NEXT

The recommended solution is to find the line referenced in the error message and see what is defined multiple times. Or check to make sure all of the required constructs prior to the specified construct are present. Correct the error at the source, and regenerate the EDIF file. If you know EDIF and the design well, correct the error at the source, and correct all of the appropriate references in the rest of the EDIF file.

EXAMPLES

```
 ...
 (external size1_lib (edifLevel 0) (technology (numberDefinition))
5 (cell or2 (cellType GENERIC)
6   (view Netlist_representation (viewType NETLIST)
7    (interface
8      (port A (direction INPUT ))
        ...
11    )
12   )
13 )
14 (cell or2 (cellType GENERIC)
15   (view Netlist_representation (viewType NETLIST)
16    (interface
17      (port X (direction INPUT ))
  ...
```

EXAMPLE MESSAGE

```
Error: Line 14: multiple definition of cell 'or2' in library 'size1_lib'. (EDFN-39)
```

In the above example, the cell "or2" is defined twice (one on line 5 and one on line 14) in the library "size1_lib". Below is a correct example:

```
 ...
 (external size1_lib (edifLevel 0) (technology (numberDefinition))
5 (cell or2 (cellType GENERIC)
6   (view Netlist_representation (viewType NETLIST)
7    (interface
8      (port A (direction INPUT ))
```

```
       ...
11    )
12   )
13 )
14 (cell or3 (cellType GENERIC)
15   (view Netlist_representation (viewType NETLIST)
16    (interface
17      (port X (direction INPUT ))
  ...
```

EDFN-40 (warning) Line %d: Ending %s name space with %s name space (mismatch).

DESCRIPTION

The EDIF reader detected a syntax error on or near the line number indicated in the error message.

WHAT NEXT

Check the parentheses around the major constructs.

EDFN-41 (error) Line %d: Cannot find %s '%s' in definition of %s '%s'.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and cannot find the specified reference in the specified scope. For example, during cell instantiation, a cell reference is specified along with the library which contains the cell definition.

WHAT NEXT

Refer to the line number in the error message and locate the error. The recommended solution is to regenerate the EDIF file and rerun the program. However, if you know EDIF and the design well, check that the reference is appropriate for the definition. If not, include the appropriate references.

EXAMPLES

```
  ...
5  (external lib1 (edifLevel 0) (technology (numberDefinition))
6    (cell or2 (cellType GENERIC)
```

```
7       (view Netlist_represenatation (viewType NETLIST)
8         (interface
9           (port A (direction INPUT))
10           (port B (direction OUTPUT))))))
11   (library DESIGNS (edifLevel 0) (technology (numberDefinition))
12     (cell or2 (cellType GENERIC)
13       (view Netlist_represenatation (viewType NETLIST)
14         (interface
15           (port X (direction INPUT))
15           (port Y (direction OUTPUT)))
16         (contents
17           (instance pcell2 (viewRef Netlist_representation
18             (cellRef or2A (libraryRef lib1))))
         ...
```

EXAMPLE MESSAGE

```
Error: Line 18: Cannot find cell 'or2A' in definition of library 'lib1'. (EDFN-41)
```

In the above example (line 18), the cell "or2A" is not defined in the external library "lib1". Below is the correct example:

```
  ...
5   (external lib1 (edifLevel 0) (technology (numberDefinition))
6     (cell or2 (cellType GENERIC)
7       (view Netlist_represenatation (viewType NETLIST)
8         (interface
9           (port A (direction INPUT))
10           (port B (direction OUTPUT))))))
11   (library DESIGNS (edifLevel 0) (technology (numberDefinition))
12     (cell or2 (cellType GENERIC)
13       (view Netlist_represenatation (viewType NETLIST)
14         (interface
15           (port X (direction INPUT))
15           (port Y (direction OUTPUT)))
16         (contents
17           (instance pcell2 (viewRef Netlist_representation
18             (cellRef or2 (libraryRef lib1))))
         ...
```

EDFN-42 (error) Line %d: The %s reference has a missing or invalid name.

DESCRIPTION

Obsolete

WHAT NEXT

Obsolete

EDFN-43 (error) Line %d: The %s reference has a missing or invalid %s reference.

DESCRIPTION

The EDIF reader issues this error message when it parses the EDIF file and encounters an incomplete reference. For example, during cell instantiation, a view reference is always specified along with a cell reference. If you instantiate a cell and only specifiy the view reference, you will receive this error message.

WHAT NEXT

Refer to the line number in the error message and locate the error. The recommended solution is to regenerate the EDIF file and rerun the program. However, if you know EDIF and the design well, you can go to the spot specified in the error message and include the appropriate references.

EXAMPLES

```
  ...
5  (library lib1 (edifLevel 0) (technology (numberDefinition))
6    (cell or2 (cellType GENERIC)
7      (view Netlist_represenatation (viewType NETLIST)
      ...
16        (contents
17          (instance pcell2 (viewRef Netlist_representation))
        ...
```

EXAMPLE MESSAGE

Error: Line 18: The view reference has a missing or invalid cell reference. (EDFN-43)

In the above example, (line 17) the cell "pcell2" is instantiated only with the view reference. Below is an example of cell instantiation with complete references.

```
  ...
5  (library lib1 (edifLevel 0) (technology (numberDefinition))
6    (cell or2 (cellType GENERIC)
7      (view Netlist_represenatation (viewType NETLIST)
        ...
16        (contents
17         (instance pcell2 (viewRef Netlist_representation (cellRef or2 ))
```

```
...
```

EDFN-44 (error) Line %d: Cannot find the current %s symbol specification.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters an incomplete construct which might put subsequent constructs out of scope. This will cause problems later on in the EDIF file during library, cell, or page referencing.

WHAT NEXT

To fix this problem, refer to the line number in the error message, and check to see what is being referenced. The recommended solution is to regenerate the EDIF file and rerun the program. If you know EDIF and the design well, locate the symbol and the symbol definition and see what is missing from the symbol definition.

EXAMPLES

```
1 (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
2 (keywordMap (keywordLevel 0)) (status)
3  external size1_lib (edifLevel 0) (technology (numberDefinition))
4  (cell or2 (cellType GENERIC )
   ...
25 (library DESIGNS (edifLevel 0) (technology (numberDefinition))
26  (cell size1 (cellType GENERIC)
27   (view Netlist_representation (viewType NETLIST)
    ...
35   (contents
36     (instance pcell2
37       (viewRef Netlist_representation
38       (cellRef or2 (libraryRef size1_lib))
    ...
```

EXAMPLE MESSAGE

```
Error: Line 38: Cannot find the current edif symbol specification. (EDFN-44)
```

In the above example, the left parenthesis is missing from line 3, at the beginning of an external library definition. This caused the other constructs to be out of scope. To fix this, add the left parenthesis at the beginning of line 3.

EDFN-45 (error) Line %d: Value of %s:%s not successfully interpreted.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and detects an invalid cell type (cellType) or view type (viewType). EDIF only support cell types of: TIE, GENERIC, and RIPPER, and view types of: BEHAVIOR, DOCUMENT, GRAPHIC, LOGICMODEL, MASKLAYOUT, NETLIST, PCBLAYOUT, SCHEMATIC, STRANGER, and SYMBOLIC.

WHAT NEXT

Refer to the line number in the error message and locate the error. The recommended solution is to regenerate the EDIF input file and reimport the file. However, if you know EDIF and the design well, you can go to the error line and specify the correct viewType or cellType.

EXAMPLES

```
  ...
5  (library lib1 (edifLevel 0) (technology (numberDefinition))
6    (cell or2 (cellType GENERICAA)
7      (view Netlist_represenatation (viewType NETLIST)
      ...
16        (contents
17          (instance pcell2 (viewRef Netlist_representation))
        ...
```

EXAMPLE MESSAGE

Error: Line 6: Value of cellType:GENERICAA not successfully interpreted. (EDFN-45)

To fix the above example, go to line 6 change cellType from GENERICAA to GENERIC.

EDFN-46 (error) Line %d: unmatched right parenthesis.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters an extra right parenthesis after parsing a complete construct.

WHAT NEXT

If you receive this message, proceed as follows:

1. Locate the line referenced in the error message. This line contains the unmatched right parenthesis.

2. Working backwards in the file from the unmatched right parthensis, examine each line until you identify the location where the missing left parenthesis should be added.

3. Correct the EDIF file and re-read it.

EXAMPLES

```
1 (edif Synopsys_edif
   ...
25    library lib1
      ...
87    )
```

EXAMPLE MESSAGE

```
Error: Line 87: unmatched right parenthesis. (EDFN-46)
```

In this example, line 87 contains unmatched right parenthesis. Working backwards from line 87, you find the matching right parenthesis missing from line 25. The corrected example is as follows:

```
1 (edif Synopsys_edif
   ...
25    (library lib1
      ...
87    )
```

EDFN-47 (error) Line %d: missing left parenthesis.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters an EDIF construct without a left parenthesis.

WHAT NEXT

To fix this problem, refer to the line number in the error message, and start from there to look for the missing left parenthesis.

EXAMPLES

```
1 edif Synopsys_edif
   ...
```

```
25    library lib1
      ...
87    )
```

EXAMPLE MESSAGE

```
Error: Line 1: missing left parenthesis. (EDFN-47)
```

In the above example, the left parenthesis at the beginning of the "edif" construct is missing. Below is the correct example:

```
1 (edif Synopsys_edif
   ...
25    (library lib1
      ...
87    )
```

EDFN-48 (error) Line %d: misplaced ’%%’.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters a to incorporate ASCII characters into a string token.

WHAT NEXT

To fix the problem, refer to the line referenced in the error message and see if the % symbol is the right place. If it is supposed to be part of a string token, it needs to be in double quotes.

EXAMPLES

```
1 (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
2 (keywordMap (keywordLevel 0)) (status)
3 (external size1_lib (edifLevel 0) (technology (numberDefinition))
4  (cell or2 (cellType %%GENERIC)
```

EXAMPLE MESSAGE

```
Error: Line 4: misplaced ’%’. (EDFN-48)
```

In the above example, the %% symbols in line 4 are misplaced. Below is a correct example:

```
1 (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
2 (keywordMap (keywordLevel 0)) (status)
```

```
3 (external size1_lib (edifLevel 0) (technology (numberDefinition))
4  (cell or2 (cellType GENERIC)
```

EDFN-49 (error) Line %d: unrecognized token.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters a % sign when it is expecting an identifier.

WHAT NEXT

To fix the problem, refer to the line in the error message and take out the % sign.

EXAMPLES

```
1 (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
2 (keywordMap (keywordLevel 0)) (status)
3 (external size1_lib (edifLevel 0) (technology (numberDefinition))
4  (cell or2 (cellType %%GENERIC)
```

EXAMPLE MESSAGE

```
Error: Line 4: unrecognized token. (EDFN-49)
```

In the above example, the %% signs in line 4 are misplaced. Below is an correct example:

```
1 (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
2 (keywordMap (keywordLevel 0)) (status)
3 (external size1_lib (edifLevel 0) (technology (numberDefinition))
4  (cell or2 (cellType GENERIC)
```

EDFN-50 (error) Line %d: missing right parenthesis.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and finds missing right parenthesis. It normally parses until the end of the file to match left parenthesises to right parenthesises, so the line number shown in the error message is usually not correct.

WHAT NEXT

Go through the EDIF file and look for the missing parenthesis, or you can regenerate the EDIF file.

EXAMPLES

```
1 (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
2   (keywordMap (keywordLevel 0)) (status)
3     (external size1_lib (edifLevel 0) (technology (numberDefinition))
      ...
86    )
87  )
```

EXAMPLE MESSAGE

Error: Line 88: missing right parenthesis. (EDFN-50)

In the above example, there are only 87 lines in this file. The missing right parenthesis occurs in line 85, but the error message refers to line 88. The EDIF reader reads until the EOF mark to find the matching right parenthesis. This is why you get the error message refering to line 88.

EDFN-51 (error) Line %d: No edif design encountered.

DESCRIPTION

The EDIF reader issues this error if the input file is empty.

WHAT NEXT

Make sure you specified the correct input file.

EDFN-52 (error) Line %d: ASCII character is not between 0 and 127.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters a non-readable character. Your ASCII EDIF file is probably corrupted or it is not an ASCII file.

WHAT NEXT

Refer to the line referenced in the error message and see if there is an incorrect character in this line.

EDFN-53 (error) Line %d: invalid string token.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encouters an invalid specification string. A string is surrounded by quotes, and you can use the % symbol as part of a string to specify an embeded ASCII character. The EDIF reader expects an integer after the % symbol in a string.

WHAT NEXT

Refer to the line number in the error message and take out the % symbol in the string if it is not used to specify an embeded ASCII character. If the % symbol is used to specify an embeded ASCII character, it needs to be followed by an integer.

EXAMPLES

```
   ...
10    (port VDD (direction INPUT)
11      (property implicitPortClass (string "%abc") (owner "Schematic_TSC"))
   ...
```

EXAMPLE MESSAGE

```
Error: Line 10: invalid string token. (EDFN-53)
```

In the above example, the string "%abc" causes the EDIF reader to issue the error because the EDIF reader expects an integer after the % symbol. The following example has the correct syntax for a string token:

```
   ...
10    (port VDD (direction INPUT)
11      (property implicitPortClass (string "abc") (owner "Schematic_TSC"))
   ...
```

EDFN-54 (error) Line %d: Expected an arc or point.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters an EDIF construct that is out of scope. The curve construct only supports the arc and

point constructs.

WHAT NEXT

Refer to the line number in the error message, and locate the illegal EDIF construct within the scope of the curve construct. You need to regenerate and reimport the EDIF input file.

EXAMPLES

```
  ...
25  (portImplementation A
26       (connectLocation (figure cell_layer (dot (pt -2653 -1024))))
27      )
28      (figure cell_layer
29       (openShape
30        (curve (rectangle (pt -3071 2047) (pt -2523 -1) (pt -3072 -2048))
  ...
```

EXAMPLE MESSAGE

```
Error: Line 30: Expected an arc or point. (EDFN-54)
```

In the above example, a curve is define (line 30), and it is followed by a rectangle construct. After a curve construct, only an arc or a point construct can be used.

```
... 25 (portImplementation A 26 (connectLocation (figure cell_layer (dot (pt -2653 -
1024)))) 27 ) 28 (figure cell_layer 29 (openShape 30 (curve (pt -3071 2047) (pt -
2523 -1) (pt -3072 -2048)) ...
```

EDFN-55 (error) Line %d: Expected a rectangle.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters an out of scope EDIF construct. A rectangle construct is expected after the boundingBox and Page constructs.

WHAT NEXT

Refer to the line number in the error message and locate the error by looking for the construct immediatly after the boundingBox or Page construct. You need to regenerate and reimport the EDIF input file.

EXAMPLES

```
       ...
55    (symbol (boundingBox (curve (rectangle (pt -3858 -2048) (pt 2597 2048)))
```

```
   ...
```

EXAMPLE MESSAGE

```
Line 21: Expected a rectangle. (EDFN-55)
```

In the above example, after the boundingBox construct is the curve construct, this causes the error. The curve construct needs to be removed.

EDFN-56 (error) Line %d: Expected a curve.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters an EDIF construct which is in the wrong scope. After the openShape and shape constructs, the only supported construct is the curve construct.

WHAT NEXT

Refer to the line number in the error message and locate the error by looking for the shape construct. Regenerate and reimport the EDIF input file.

EXAMPLES

```
   ...
21   (openShape (boundingBox (curve (rectangle (pt -3858 -2048) (pt 2597 2048))
   ...
```

EXAMPLE MESSAGE

```
Error: Line 21: Expected a curve. (EDFN-56)
```

In the above example, after the openShape construct, the boundingBox construct is read. This caused the error, because the EDIF reader is expecting a curve construct.

EDFN-57 (error) Line %d: Expected a point.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters an EDIF construct which is out of scope.

WHAT NEXT

Regenrate the EDIF input file and reimport it into dc_shell.

EXAMPLES

```
    ...
35  (figure cell_layer
36     (openShape (curve (arc (arc (pt -950 2048) (pt 1098 1499) (pt 2597 0))
    ...
```

EXAMPLE MESSAGE

```
Error: Line 36: Expected a point. (EDFN-57)
```

In the above example, after the curve construct, a pt construct is expected, but reader is reading an arc construct.

EDFN-58 (error) Line %d: Expected a number.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters a non-numeric character when it expecting a numeric character. For example, the reader expects a numeric character for array size, EDIF version number, EDIF level, EDIF keyword level, or other constructs.

WHAT NEXT

Refer to the line number in the error message to see if any alpha character is misplaced, or regenerate the EDIF file.

EXAMPLES

```
1 (edif Synopsys_edif (edifVersion a2 0 0) (edifLevel 0)
2  (keywordMap (keywordLevel 0)) (status)
     ...
```

EXAMPLE MESSAGE

```
Error: Line 1: Expected a number. (EDFN-58)
```

In the above example, the edif version number is a2 0 0 (edifVersion a2 0 0). The correct syntax would be (edifVersion 2 0 0).

EDFN-59 (error) Line %d: Expected a name.

DESCRIPTION

The EDIF reader issues this error message when it parses the EDIF input file and encounters a non-string name used to defy a unit definition.

WHAT NEXT

Refer to the line number in the error message, and locate the unit construct. Understand the problem, and you can either regenerate the EDIF input file, or if you know the unit defintion and fix the problem. Reimport the EDIF input file.

EXAMPLES

```
1  (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
2   (keywordMap (keywordLevel 0)) (status)
3   (library (rename generic_sdb "generic.sdb") (edifLevel 0)
4    (technology (numberDefinition (scale 1 (e 496094 -11) (unit 3333)))
5     (figureGroup fat_layer (color 99 0 0))
     ...
```

EXAMPLE MESSAGE

```
Error: Line 4: Expected a name. (EDFN-59)
```

In the above example, the unit is defined to be 3333 (line 4), the reader is expecting a name not an integer. If the unit definition changed from 3333 to DISTANCE, the EDIF reader will accept it.

EDFN-60 (error) Could not open file '%s'.

DESCRIPTION

The EDIF reader issues this error when it cannot open the EDIF input file.

WHAT NEXT

Make sure the EDIF input file exists and is readable.

EDFN-61 (warning) Line %d: Edifin_lib_%s_symbol '%s' not

found in library '%s'.

DESCRIPTION

The EDIF reader is not able to find the specified symbol in any of the libraries.

WHAT NEXT

Specify the library that contains the symbol shown in the error message.

EDFN-62 (error) Line %d: 'DISTANCE' scale not defined for library '%s'.

DESCRIPTION

The EDIF reader issues this error when it is used in conjunction with the **read_lib** command to create a synopsys library and the DISTANCE scale is not specified in the EDIF input file.

WHAT NEXT

To fix this problem, you need to regenerate the EDIF input file and specify the EDIF writer to write out the DISTANCE scale.

EXAMPLES

```
   ...
7   (library LIBRARYNAME
8    (EDIFLevel 0)
9    (technology
10      (numberDefinition)
11         (figureGroup BODY_FGP
12           (color 0 89 89)
13           (textHeight 43)
14           (visible
15           (true)))
         ...
```

EXAMPLE MESSAGE

```
dc_shell> read_lib size1.edif -f EDIF
```

Error: Line 11: 'DISTANCE' scale not defined for library 'LIBRARYNAME'. (EDFN-62) In the above example, the DISTANCE scale is not defined. Below is an example with the DISTANCE scale defined.

```
   ...
7   (library LIBRARYNAME
8    (EDIFLevel 0)
9    (technology
10      (numberDefinition
11          (scale 240
12           (e 254 -4)
13           (unit DISTANCE)))
14      (figureGroup BODY_FGP
15        (color 0 89 89)
16        (textHeight 43)
17        (visible
18        (true)))
         ...
```

EDFN-63 (information) Line %d: Could not find port connect location. Using derived connect location from ’%s’ viewRef, ’%s’ cellRef, or ’%s’ libraryRef.

DESCRIPTION

This message informs you that the system could not find the port connect location, and is using the derived connnect location from the cell, library, or view reference.

WHAT NEXT

Modify the design so that it contains the connect locations for all ports.

EDFN-64 (error) Line %d: Connect location derived for ’%s’ viewRef of ’%s’ cellRef of ’%s’ libraryRef is not equal to previously derived location.

DESCRIPTION

The EDIF reader issues this error message when it parses the EDIF input file and encounters a design with incorrect connect location.

WHAT NEXT

Regenerate and re-import the EDIF input file.

EXMAMPLES

EXAMPLE MESSAGE

```
Error: Line 296: Connect location derived for 'Graphic_representation' viewRef of
'in_port' cellRef of 'generic_sdb' libraryRef is not equal to previously derived
location. (EDFN-64)
```

EDFN-65 (warning) Line %d: No connect location found for '%s' viewRef, '%s' cellRef, or '%s' libraryRef.

DESCRIPTION

The EDIF reader is not able to find the port connect location for the specified references.

WHAT NEXT

Modify the design so that it contains the connect locations for all ports.

EDFN-66 (warning) Line %d: Derived connect location rejected for '%s' viewRef, '%s' cellRef, and '%s' libraryRef.

DESCRIPTION

The EDIF reader could not find the connect location for the specified objects. It uses the connect location from the specified references, but the connect location from the references is not valid.

WHAT NEXT

Modify the EDIF input file, and make sure the connect location is valid.

EDFN-67 (error) Line %d: The %s element within the '%s' construct must be %s.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and finds missing

required EDIF constructs for the specified EDIF construct. For example, the cell construct requires the cell name and the cellType (cell cellName, cellType GENERIC).
...

WHAT NEXT

Refer to the line number in the error message and see what caused the problem. The recommended solution is to regenerate the EDIF input file. However, if you know EDIF and the design well, you can fix the problem by following the error message.

EXAMPLES

```
1 (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
2  (keywordMap (keywordLevel 0)) (status)
3   (external size1_lib (edifLevel 0) (technology (numberDefinition))
4     (cell or2
5      (view Netlist_representation (viewType NETLIST)
        ...
```

EXAMPLE MESSAGE

Error: Line 4: The 3rd element within the ’cell’ construct must be the ’cellType’ construct. (EDFN-67)

In the example above, the declaration of a cell (line 4) fails to specify the cell type. Below is a correct example:

```
1 (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
2  (keywordMap (keywordLevel 0)) (status)
3   (external size1_lib (edifLevel 0) (technology (numberDefinition))
4     (cell or2 (cellType GENERIC)
5      (view Netlist_representation (viewType NETLIST)
        ...
```

EDFN-68 (error) Line %d: The keywordAlias construct is only valid in keywordLevel 1 or higher.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters a keyword alias specification for the keywordLevel 0 construct. The keywordAlias construct can only be used with keywordLevel 1, 2, or 3.

WHAT NEXT

The recommended solution is to regenerate the EDIF file. However, if you know EDIF and the design well, look at the rest of the file and see if and how the keyword

alias is used. Change the keyword level accordingly. If the keyword alias is not used, change the keyword level to 0.

EXAMPLES

```
1 (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
2  (keywordMap (keywordLevel 0) (keywordAlias p pt)) (status)
3   (external size1_lib (edifLevel 0) (technology (numberDefinition))
4    (cell or2 (cellType GENERIC)
      ...
```

EXAMPLE MESSAGE

```
Error: Line 2: The keywordAlias construct is only valid in keywordLevel 1 or higher.
(EDFN-68)
```

In the example above (line 2), the keywordLevel is 0, yet the keywordAlias construct is used. Since there is no keyword alias used in this file, the keywordAlias construct can be taken out. Here is a correct example.

```
1 (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
2  (keywordMap (keywordLevel 0)) (status)
3   (external size1_lib (edifLevel 0) (technology (numberDefinition))
4    (cell or2 (cellType GENERIC)
      ...
```

EDFN-69 (error) Line %d: Expected an identifier.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters an incorrect keywordAlias definition (keywordAlias identifier).

WHAT NEXT

To fix this problem, refer to the line number in the error message, and check the keyword alias definition. If you know the keyword alias, then you can fix it. If you do not know the keyword alias, you can regenerate the EDIF input file.

EXAMPLES

```
1 (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
2  (keywordMap (keywordLevel 1) (keywordAlias  "p" "pt")) (status)
3   (external size1_lib (edifLevel 0) (technology (numberDefinition))
4    (cell or2 (cellType GENERIC)
5     (view Netlist_representation (viewType NETLIST)
    ...
```

EXAMPLE MESSAGE

```
Error: Line 2: Expected an identifier. (EDFN-69)
```

In the above example (line 2), the keywordAlias contruct contains two strings, "p" and "pt", instead of two identifiers. Below is the fix the above example.

```
1 (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
2  (keywordMap (keywordLevel 1) (keywordAlias  p pt)) (status)
3   (external size1_lib (edifLevel 0) (technology (numberDefinition))
4    (cell or2 (cellType GENERIC)
5     (view Netlist_representation (viewType NETLIST)
    ...
```

EDFN-70 (warning) Could not find template symbol '%s' for sheet size '%s' or orientation '%s' in library '%s'.

DESCRIPTION

The EDIF reader is not able to find the template symbol for the specified sheet, size, and orientation in the specified library.

WHAT NEXT

Include the correct library which contains the template symbol for the specification in the error message.

EDFN-71 (error) Line %d: The points defining the arc are not distinct.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters an incorrect definition of an arc.

WHAT NEXT

Regenerate and reimport the EDIF input file.

EXAMPLES

```
  ...
34  (figure cell_layer
```

```
35    (openShape (curve (arc (pt -950 2048) (pt 2597 1499) (pt 2597 1499))))
  ...
```

EXAMPLE MESSAGE

```
Error: Line 35: The points defining the arc are not distinct. (EDFN-71)
```

In the above example, the second and third points defining the arc are identical.

EDFN-72 (error) Line %d: Can not create attribute '%s' on the cell instance.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters some internal problem.

WHAT NEXT

Restart the command, if the problem persists please contact Synopsys' help line.

EDFN-73 (error) Line %d: Can not set attribute '%s' on the cell instance.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters some internal problem.

WHAT NEXT

Restart the command, if the problem persists please contact Synopsys' help line.

EDFN-74 (error) Line %d: There is no pin named '%s' on the cell instance.

DESCRIPTION

Obsolete

WHAT NEXT

Obsolete

EDFN-75 (error) Line %d: Can not create attribute '%s' on pin '%s'.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters some internal problem.

WHAT NEXT

Restart the command, if the problem still occurs please contact Synopsys' help line.

EDFN-76 (error) Line %d: Can not set attribute '%s' on pin '%s'.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters some internal problem.

WHAT NEXT

Restart the command, if the problem still occurs please contact Synopsys' help line.

EDFN-77 (error) Line %d: Can not create attribute '%s' on port '%s'.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters some internal problem.

WHAT NEXT

Restart the command, if the problem still occurs please contact Synopsys' help line.

EDFN-78 (error) Line %d: Can not set attribute '%s' on port '%s'.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters some internal problem.

WHAT NEXT

Restart the command, if the problem still occurs please contact Synopsys' help line.

EDFN-79 (error) Line %d: The attribute 'disabled' may not be set on power or ground port '%s'.

DESCRIPTION

Obsolete

WHAT NEXT

Obsolete

EDFN-80 (error) Line %d: Duplicate view property name in library '%s'.
View '%s' of cell '%s' has the same view identifier '%s' property value of '%s' as view '%s' of cell '%s'.

DESCRIPTION

The EDIF reader issues this error when it detects duplicating view property names in the same design.

WHAT NEXT

Synopsys EDIF reader only support single view design. As for multiple view design, it only reads and process the first view in the design and ignore the rest. Therefore, it highly recommended that you regenerate the EDIF input file with single view design.

EXAMPLES

```
  ...
200  (cell case_test (cellType GENERIC)
201    (view &_ONE (viewType SCHEMATIC)
202     (interface
       ...
350      (property
351        (rename COMP "COMP")
352        (string "COMP_ALREADY_DEFINED"))
       ...
400    (view &_TWO (viewType SCHEMATIC)
401     (interface
       ...
451      (property
452        (rename COMP "COMP")
453        (string "COMP_ALREADY_DEFINED"))
       ...
```

EXAMPLE MESSAGE

```
>dc_shell edifin_view_identifier_property_name = "COMP" "COMP"

Error: Line 401: Duplicate design name in library 'LIBRARYNAME'. View '_TWO_' of
cell 'case_test' has the same view identifier 'COMP' property value of
'COMP_ALREADY_DEFINED' as view '_ONE_' of cell 'case_test'. (EDFN-80)

In the above example, view _ONE and _TWO has the sampe property name "COMP".
```

EDFN-81 (error) Line %d: Duplicate design name in library '%s'. View '%s' of cell '%s' already has a view identifier '%s' property value of '%s'.

DESCRIPTION

The EDIF reader issues this error message when it parses the EDIF input file and encounters a view property whose name is the same as the edifin_view_identifier_property_name and a design whose name is the same as the value of the view property.

WHAT NEXT

Locate the problem by refering to the line number in the error message. Regenerate and reimport the EDIF input file, or do not use the edifin_view_identifier_property_name flag.

EXAMPLES

```
...
(cell test_case
  ...
   (property
     (rename COMP "COMP")
     (string "COMP_ALREADY_DEFINED"))
  ...
 (cell
   COMP_ALREADY_DEFINED
   (cellType GENERIC)
  ...
```

EXAMPLE MESSAGE

```
dc_shell > edifin_view_identifier_property_name = "COMP" "COMP" dc_shell > read -f
edif size1.edif Loading edif file 'size1.edif' Error: Line 363: Duplicate design
name in library 'LIBRARYNAME'. View '_ONE_' of cell 'case_test' already has a view
identifier 'COMP' property value of 'COMP_ALREADY_DEFINED'. (EDFN-81)
```

In the above example, the variable edifin_view_identifier_property_name is set to "COMP". The EDIF input file has a view property whose name is COMP and value is "COMP_ALREADY_DEFINED", the input file also has a design whose name is "COMP_ALREADY_DEFINED".

EDFN-82 (error) The value of variable '%s' isn't valid.

DESCRIPTION

The EDIF reader issues this error message when it parses the EDIF file and use a bus related variable incorrectly set in dc_shell.

WHAT NEXT

Refer to the line number in the error message, and locate the error. Go to the dc_shell command window and re-set the variable to the correct value.

EXAMPLES

```
dc_shell > bus_extraction_style = "%s(%d-%d)"
"%s(%d-%d)"
read -f edif s13884_3.iedif
Loading edif file '/remote/qe1/test/unit/designs/edif/stars/s13884_3.iedif'
```

EXAMPLE MESSAGE

```
Error: In the value of variable 'bus_extraction_style', the last (rightmost) of the
characters separating each "%d" must not be a plus or minus sign or a digit. (DDB-
```

```
57) Error: The value of variable 'bus_extraction_style' isn't valid. (EDFN-82)
```

In the above example, the bus_extraction-style variable was set incorrectly. It should be: bus_extraction_style = "%d[%s:%s]"

EDFN-83 (error) Line %d: The range from %d to %d of array '%s' does not match its width.

DESCRIPTION

The EDIF reader issues this error message when it parses the EDIF file and encounter an array whose width does not match its range. An array is defined with a range and the size, e.g. (port (array (rename DUMMY "IN<_15...0_")16). The array DUMMY has a range from 15 to 0, and the size is 16.

WHAT NEXT

Refer to the line number in the error message, and locate the array with the incorrect definition. If you know EDIF and the design well, you can change the array size and range to the correct number, or regenerate the EDIF input file.

EXAMPLES

```
  ...
21  (port (rename &1_DUMMY "A<_15...0_>"))
22  (port (Array (rename &2_DUMMY "IN<_15...0_>") 16))
23  (port (Array (rename &3_DUMMY "OUT<_15...0_>") 15))
  ...
```

EXAMPLE MESSAGE

```
Error: Line 23: The range from 15 to 0 of array 'OUT<_15...0_>' does not match its
width. (EDFN-83)
```

In the above example, array 3_DUMMY has a range from 15 to 0, so its size should be 16 instead of 15.

EDFN-84 (error) Line %d: Multiple cells of the same name are not supported.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters multiple cells of the same name in the EDIF input file.

WHAT NEXT

Regenerate your EDIF file and make sure the cell names are unique.

EXAMPLES

```
   ...
1000   (library A
     ...
1010     (cell TT
       ...
1300   (library A
     ...
1329     (cell TT
   ...
```

EXAMPLE MESSAGE

Error: Line 1329: Multiple cells of the same name are not supported. (EDFN-84)

In the above example, cell TT is defined twice (line 1010 and 1329) in library A.

EDFN-85 (warning) Line %d: Cannot create attribute '%s' on net '%s'.

DESCRIPTION

The EDIF reader is not able to create the specified attribute of the specified net due to an invalid attribute definition.

WHAT NEXT

Fix the EDIF input file and make sure that all of the attributes in the design are properly defined.

EDFN-86 (warning) Line %d: Cannot set attribute '%s' on net '%s'.

DESCRIPTION

The EDIF reader is not able to set an attribute on the specified net due to an invalid attribute definition.

WHAT NEXT

Modify the EDIF input file and make sure the specified attributes are properly defined.

EDFN-87 (warning) Line %d: Cannot create attribute '%s' on design '%s'.

DESCRIPTION

The EDIF reader is not able to create an attribute on the design due to an invalid attribute definition.

WHAT NEXT

Fix the EDIF input file, and make sure all of the attributes in the design are properly defined.

EDFN-88 (warning) Line %d: Cannot set attribute '%s' on design '%s'.

DESCRIPTION

The EDIF reader is not able to set an attribute on the design due to an invalid attribute definition.

WHAT NEXT

Check the EDIF input file to make sure all of the attributes are properly defined.

EDFN-89 (error) Line %d: Library '%s' is corrupted. Not all view identifier properties of cell '%s' are found.

DESCRIPTION

The EDIF reader issues this error message when the system cannot find the specified view identifier property. The EDFI reader does not support cells with multiple views.

WHAT NEXT

Fix the design so it only contains cells with single view.

EDFN-90 (error) Line %d: The port '%s' on instance '%s' isn't an array.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters a reference to a simple port using the member construct. Member construct can only be used to reference an array port.

WHAT NEXT

Refer to the line number in the error message and locate the incorrect port reference. You can either fix the source, regenerate and reimport the EDIF input file. Or, if you know EDIF and your design well, you can check the port definition and fix the port reference.

EXAMPLES

```
  ...
50  cell FULL_ADDER (cellType GENERIC)
51   (view Schematic_representation (viewType SCHEMATIC)
52    (interface (port A (direction INPUT)) (port B (direction INPUT))
  ...
100  (instance (rename U1_1_ "U1[1]")
101       (viewRef Schematic_representation
102        (cellRef FULL_ADDER (libraryRef ADDER_db))
  ...
150       (joined
151        (portRef (member w 1) (instanceRef (member Ripper_5678 1)))
152        (portRef (member B 0)(instanceRef U1_1_))
   ...
```

EXAMPLE MESSAGE

Error: Line 152: The port 'B' on instance 'U1[1]' isn't an array. (EDFN-90)

In the above example, port B is defined to be a simple port (line 52), but it is referenced (line 152) using the member construct. Below is an example:

... 50 cell FULL_ADDER (cellType GENERIC) 51 (view Schematic_representation (viewType SCHEMATIC) 52 (interface (port A (direction INPUT)) (port B (direction INPUT)) ... 100 (instance (rename U1_1_ "U1[1]") 101 (viewRef Schematic_representation 102 (cellRef FULL_ADDER (libraryRef ADDER_db)) ... 150 (joined 151 (portRef (member w 1) (instanceRef (member Ripper_5678 1))) 152 (portRef

```
B (instanceRef U1_1_)) ...
```

EDFN-91 (warning) Line %d: The value '%s' of the duplicate %s property '%s' is ignored.

DESCRIPTION

The EDIF reader detected duplicate properties with different values. It processed and kept the first set of values.

WHAT NEXT

Modify the EDIF input file, and make sure the property values are properly set.

EDFN-92 (warning) Line %d: Cannot create attribute '%s' on the cell instance.

DESCRIPTION

The EDIF reader is not able to create an attribute on the cell instance due to an invalid attribute definition.

WHAT NEXT

Check the EDIF input file to make sure all of the attributes are properly defined.

EDFN-93 (warning) Line %d: Cannot set attribute '%s' on the cell instance.

DESCRIPTION

The EDIF reader cannot set the specified attribute on the cell instance, because the attribute has an invalid setting or type.

WHAT NEXT

Check the EDIF input file to make sure all of the attributes are properly defined.

EDFN-94 (warning) Line %d: Cannot create attribute '%s' on pin '%s'.

DESCRIPTION

The EDIF reader is not able to create an attribute on the design due to an invalid attribute definition.

WHAT NEXT

Check the EDIF input file to make sure all of the attributes are properly defined.

EDFN-95 (warning) Line %d: Cannot set attribute '%s' on pin '%s'.

DESCRIPTION

The EDIF reader is not able to set the attribute on the design due to an invalid attribute definition.

WHAT NEXT

Check the EDIF input file to make sure all of the attributes are properly defined.

EDFN-96 (warning) Line %d: Cannot create attribute '%s' on port '%s'.

DESCRIPTION

The EDIF reader is not able to create the specified attribute due to an invalid attribute definition.

WHAT NEXT

Check the EDIF input file and make sure all of the attribues are correctly defined.

EDFN-97 (warning) Line %d: Cannot set attribute '%s' on port

’%s’.

DESCRIPTION

The EDIF reader is not able to set an attribute on a design object due to an invalid attribute definition.

WHAT NEXT

Check the EDIF input file to make sure all of the attributes are properly defined.

EDFN-98 (warning) Line %d: Net bus not added to the design because a net’s connections to the previously added net).

DESCRIPTION

The EDIF reader detected that there is a net or a bussed net with the same name that has already been added to the system. The first net will be used to make the connection.

WHAT NEXT

Fix the EDIF input file, or make sure that all of the net connections are correct.

EDFN-99 (warning) Line %d: Port array connected to a net that is not an array.

DESCRIPTION

The EDIF reader detects that there is a bussed port connected to a single net in the design.

WHAT NEXT

Fix the EDIF input file.

EDFN-100 (warning) Line %d: Port (on instance) array

connected to a net that is not an array.

DESCRIPTION

The system has encountered a connection of a single net to an array of ports. An array of ports can only connect to an array nets.

WHAT NEXT

Fix the input file so that the connections are made correctly.

EDFN-101 (error) Line %d: The portBundle is not supported.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters an EDIF portBundle construct, which is currently not supported by the Synopysy EDIF reader.

WHAT NEXT

The recommended solution is to regenerate the EDIF file, specifying that the EDIF writer is not to write out the portBundle constructs. As an alternative, if you know EDIF and the design well, you can remove the portBundle construct and all references to it from the EDIF file.

EXAMPLE:

```
With portBundle:
  ...
40  (portBundle Clocks
41    (listOfPorts
42      (port clk1)
43      (port clk2)
44    )
45  )
  ...
80  (net clock
81    (joined
82      (portRef clk1 (portRef Clocks))
      ...
```

EXAMPLE MESSAGE

```
Error: Line 40: The portBundle is not suppported.
```

In the above example (line 40), the portBundle construct is used and triggers the error message. The example below shows the section of the EDIF file without the portBundle construct.

Without portBundle: ... 40 (port clk1) 41 (port clk2) ... 78 (net clock 80 (joined 81 (portRef clk1) ...

EDFN-102 (information) Line %d: Defining view '%s' of cell '%s' to be the bus ripper.

DESCRIPTION

The variables **edifin_lib_ripper_cell_name** and **edifin_lib_ripper_view_name** specify that the ripper cell attributes be included on that view of that cell.

WHAT NEXT

This is an informational message. No action is required on your part.

EDFN-103 (information) Line %d: Defining view '%s' of cell '%s' to be the bus ripper.

DESCRIPTION

The variable **edifin_lib_ripper_cell_name** indicates that the ripper cell attributes be included on the specified view of the specified cell.

WHAT NEXT

This is an informational message. Not action is required on your part.

EDFN-104 (warning) Line %d: No symbol created for cell '%s' because the view that has been defined to be the correct view of the bus ripper cell (by setting the variable edifin_lib_ripper_view_name) was not found.

DESCRIPTION

The 'RIPPER' cellType of that cell specifies that the ripper cell attributes be included on the view of that cell that has been defined by setting the variable edifin_lib_ripper_view_name to be the correct view of the bus ripper cell, but the specified view wasn't found.

WHAT NEXT

If that cell is the correct one to use as the bus ripper cell, then (1) determine which view of that cell is the correct one to use, (2) set the variable edifin_lib_ripper_view_name to define that view to be the correct one, and (3) execute the edif format read_lib command again.

If that cell isn't the correct one to use as the bus ripper cell, then (1) determine which cell is the correct one to use, (2) set the variable edifin_lib_ripper_cell_name to define that cell to be the correct one, and (3) execute the edif format read_lib command again.

EDFN-105 (error) Line %d: invalid identifier token.

DESCRIPTION

This error occurs when the EDIF reader parses the EDIF file and detects an improperly formed identifier (one containing a character that cannot be part of an identifier). An identifier is composed only of alphanumeric or underscore characters.

WHAT NEXT

To fix this problem, refer to the line number in the error message to locate the improperly-formed identifier and correct it.

EXAMPLES

```
1  (edif Synopsys.edif (edifVersion 2 0 0) (edifLevel 0)
2   (keywordMap (keywordLevel 0)) (status)
3   (external (rename ADDER_db "ADDER.db") (edifLevel 0)
4    (technology (numberDefinition))
5    (cell ADDER (cellType GENERIC)
```

EXAMPLE MESSAGE

```
Error: Line 1: invalid identifier token. (EDFN-105)
```

In the above example, the name of the EDIF-generated program, "Synopsys.edif", is an identifier and cannot contain a dot as part of its name. Below is the correct example.

```
1  (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
2   (keywordMap (keywordLevel 0)) (status)
3   (external (rename ADDER_db "ADDER.db") (edifLevel 0)
4    (technology (numberDefinition))
5    (cell ADDER (cellType GENERIC)
```

EDFN-106 (error) Line %d: invalid integer token.

DESCRIPTION

This error occurs when the EDIF reader parses the EDIF file and detects an improperly formed integerToken (one containing a character that cannot be part of an integerToken). An integerToken can only contain numeric characters, and + and - signs; for example 123, -123, or +123.

WHAT NEXT

To fix the problem, refer to the line number in the error message to locate the improperly formed integerToken and correct it.

EXAMPLES

```
1  (edif Synopsys_edif (edifVersion 2B 0 0) (edifLevel 0)
2   (keywordMap (keywordLevel 0)) (status)
3   (external (rename ADDER_db "ADDER.db") (edifLevel 0)
4    (technology (numberDefinition))
5    (cell ADDER (cellType GENERIC)
```

EXAMPLE MESSAGE

```
Error: Line 1: invalid integer token. (EDFN-106)
```

In the above example, the edifVersion number (edifVersion 2B 0 0) is specified incorrectly. It should be specified as follows:

```
1  (edif Synopsys_edif (edifVersion 2 0 0) (edifLevel 0)
2   (keywordMap (keywordLevel 0)) (status)
3   (external (rename ADDER_db "ADDER.db") (edifLevel 0)
4    (technology (numberDefinition))
5    (cell ADDER (cellType GENERIC)
```

EDFN-107 (warning) Line %d: Expected an identifier.

DESCRIPTION

The EDIF reader detected a syntax error on the line number referenced in the error message.

WHAT NEXT

Fix the EDIF input file to contain the correct syntax.

EDFN-108 (warning) Line %d: Expected a nameDef.

DESCRIPTION

The EDIF reader detected a syntax error in the EDIF input file on the line number specified in the error message.

WHAT NEXT

Fix or regenerate the EDIF input file.

EDFN-109 (warning) Line %d: Expected a nameRef.

DESCRIPTION

The EDIF reader detected a syntax error on the line number in the error message.

WHAT NEXT

Fix or regenerate the EDIF input file.

EDFN-110 (warning) Line %d: No connect location recognized.

DESCRIPTION

The EDIF reader detected that there is no connect location for the port specified on or near the line number in the error message.

WHAT NEXT

Fix the EDIF input file.

EDFN-111 (warning) Line %d: Multiple connect location ignored.

DESCRIPTION

The EDIF reader detected multiple connection locations for the port on or near the specified line number in the error message.

WHAT NEXT

Fix the EDIF input file.

EDFN-112 (warning) Line %d: Ignoring explicit bus declaration because the variable 'bus_inference_style' is set; individual port members will be added instead. Port busses will be inferred after all design objects are read.

DESCRIPTION

The system is ignoring the explicit bus declaration because the variable **bus_inference_style** is set. If this variable is set, the system will treat port members as individuals and infer them at the end when all of the design objects are read.

WHAT NEXT

If this is not a desirable behavior, do not use this variable.

EDFN-113 (warning) Line %d: Duplicate base name '%s' for %s bus. Using '%s' for base name instead.

DESCRIPTION

You receive this message to warn you that the EDIF reader detected in your EDIF file multiple busses with the same base name (for example, AAA[0:7], &AAA[0:7], AAA{7:0}).

WHAT NEXT

For convenience, you can temporarily accept the name specified in this message. However, to avoid receiving this message each time your EDIF file is read, edit the EDIF file so that it contains a unique base name for the specified bus.

EDFN-114 (error) File %s, Line %d and File %s, Line %d: %s '%s' and %s '%s' both are changed to '%s' in '%s'.

DESCRIPTION

Obsolete

WHAT NEXT

Obsolete

EDFN-115 (error) port '%s' and port '%s' both are changed to '%s' in cell '%s' according to your names file.

DESCRIPTION

Obsolete

WHAT NEXT

Obsolete

EDFN-116 (information) Line %d: On cell '%s', defining view '%s' to be the bus ripper.

DESCRIPTION

The 'RIPPER' cellType and the variable **edifin_lib_ripper_view_name** specify that the ripper cell attributes be included on the specified view of the specified cell.

WHAT NEXT

This is an informational message. No action is required on your part.

EDFN-117 (information) Line %d: On cell '%s', defining view '%s' to be the bus ripper.

DESCRIPTION

You receive this message to inform you that the ripper cell attributes are being included on the specified view of the specified cell.

WHAT NEXT

This is an informational message only. No action is required on your part.

EDFN-118 (warning) Line %d: Base name and range extraction are not supported for multidimensional %s array '%s'.

DESCRIPTION

The EDIF reader does not support multidimensional arrays.

WHAT NEXT

Fix the design so it does not use multidemensional arrays.

EDFN-119 (warning) Line %d: Ignoring the ripper cell attributes specified here for cell '%s'; the attributes have already been included on cell '%s'.

DESCRIPTION

You receive this message if your EDIF input file contains multiple definitions of ripper cell attributes for a specific cell. In this case, the first definition encountered is used, and all subsequent definitions are ignored. This message informs you that a subsequent definition is being ignored.

WHAT NEXT

Edit the EDIF input file and ensure that it contains only one definition of the ripper cell attribute for each cell.

EDFN-120 (warning) Line %d: No symbol created for cell '%s' because the view that has been defined to be the correct view of the bus ripper cell (by setting the variable edifin_lib_ripper_view_name) was not found.

DESCRIPTION

The variable edifin_lib_ripper_cell_name specifies that the ripper cell attributes be included on the view of that cell that has been defined by setting the variable edifin_lib_ripper_view_name to be the correct view of the bus ripper cell, but the specified view wasn't found.

WHAT NEXT

If that cell is the correct one to use as the bus ripper cell, then (1) determine which view of that cell is the correct one to use, (2) set the variable edifin_lib_ripper_view_name to define that view to be the correct one, and (3) execute the edif format read_lib command again.

If that cell isn't the correct one to use as the bus ripper cell, then (1) determine which cell is the correct one to use, (2) set the variable edifin_lib_ripper_cell_name to define that cell to be the correct one, and (3) execute the edif format read_lib command again.

EDFN-121 (warning) Line %d: No symbol created for cell '%s' because the view that has been defined to be the correct view of the bus ripper cell (by setting the variable edifin_lib_ripper_view_name) was not found.

DESCRIPTION

The 'RIPPER' cellType of that cell and the variable edifin_lib_ripper_cell_name specify that the ripper cell attributes be included on the view of that cell that has been defined by setting the variable edifin_lib_ripper_view_name to be the correct view of the bus ripper cell, but the specified view wasn't found.

WHAT NEXT

If that cell is the correct one to use as the bus ripper cell, then (1) determine which view of that cell is the correct one to use, (2) set the variable edifin_lib_ripper_view_name to define that view to be the correct one, and (3) execute the edif format read_lib command again.

If that cell isn't the correct one to use as the bus ripper cell, then (1) determine which cell is the correct one to use, (2) set the variable edifin_lib_ripper_cell_name to define that cell to be the correct one, and (3) execute the edif format read_lib command again.

EDFN-122 (information) Line %d: On cell '%s', defining view '%s' to be the bus ripper.

DESCRIPTION

The 'RIPPER' cellType of the specified cell, and the variables **edifin_lib_ripper_cell_name** and **edifin_lib_ripper_view_name** specify that the ripper cell attributes be included on the specified view of the cell referenced in the error message.

WHAT NEXT

This is an informational message. No action is required on your part.

EDFN-123 (information) Line %d: On cell '%s', defining view '%s' to be the bus ripper.

DESCRIPTION

The 'RIPPER' cellType and the variable **edifin_lib_ripper_cell_name** specify that the ripper cell attributes will be included on the specified view of the cell referenced in the error message.

WHAT NEXT

This is an informational message. No action is required on your part.

EDFN-124 (error) Line %d: A connection to a pin on a member of an array of ripper cell instances is not supported.

DESCRIPTION

Obsolete

WHAT NEXT

Obsolete

EDFN-125 (error) Line %d: A portRef member construct referencing a port that is not an array is not valid.

DESCRIPTION

The EDIF reader issues this error message when it parses the EDIF file and encounters a reference to a member of a port array, but the port itself is not declared as an array.

WHAT NEXT

Regenerate the EDIF input file.

EXAMPLES

```
 ...
20  (cell (rename rip_1x1 "rip_1x1") (cellType RIPPER)
    ...
24   (interface (port (rename bundle "bundle"))
25    (port (rename wire "wire") )
26    (joined (portRef bundle) (portRef wire))
   )
 ...
100   (net out0
101     (joined (portRef (member wire 0) (instanceRef Ripper_2)) (portRef out0))
```

...

EXAMPLE MESSAGE

```
Error: Line 326: A portRef member construct referencing a port that is not an array
is not valid. (EDFN-125)
```

In the above example, port wire is defined as a single port (line 25), but it is being referenced through a member construct (line 101). Below is a correct example:

```
... 20 (cell (rename rip_1x1 "rip_1x1") (cellType RIPPER) ... 24 (interface (port
(array (rename bundle "bundle") 2)) 25 (port (array (rename wire "wire") 2 )) 26
(joined (portRef bundle) (portRef wire)) ) ... 100 (net out0 101 (joined (portRef
(member wire 0) (instanceRef Ripper_2)) (portRef out0)) ...
```

EDFN-126 (error) Line %d: The ripper cell instance is corrupt.

DESCRIPTION

The system is not able to build an object for the instance specified by the line number in the error message.

WHAT NEXT

Check your design to make sure that the syntax for the construct of the specified instance, or the constructs before the instance is correct.

EDFN-127 (warning) Line %d: Connections to a ripper with more than two pins are not supported.

DESCRIPTION

To reduce the amount of memory the EDIF format **read** command takes, a new method of reading rippers is being used. In this method, connections to a ripper with more than two pins are not supported.

WHAT NEXT

If the EDIF file contains connections to a ripper with more than two pins, set the

variable *edifin_old_ripper_reading* to TRUE. Then execute again the EDIF format **read** command.

EDFN-128 (error) Line %d: A ripper with pins of different widths is not valid.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF file and encounters a ripper with pins of different widths. The Synopsy EDIF reader can only support a ripper with pins of the same size.

WHAT NEXT

You need to regenerate the EDIF file. You can either instruct the EDIF reader to not generate a ripper design, or you can change the size of the ripper pins so that they are the same.

EXAMPLES

```
  ...
62  (cell ripCell (cellType RIPPER)
63   (view ripView (viewType SCHEMATIC)
64    (interface
65      (port (array (rename BUNDLE "bundle") 512 ))
66      (port (array (rename WIRE "wire") 256))
67      (joined
68        (portRef BUNDLE)
69        (portRef WIRE)
       ...
```

EXAMPLE MESSAGE

```
Error: Line 66: A ripper with pins of different widths is not valid. (EDFN-128)
```

In the above example, the interface of design ripCell contains two port arrays, BUNDLE and WIRE, of two different sizes, 512 and 256. Below is an example of a design with same size ripper pins which would satisfy the Synopsys EDIF reader requirement:

```
  ...
62  (cell ripCell (cellType RIPPER)
63   (view ripView (viewType SCHEMATIC)
64    (interface
65      (port (array (rename BUNDLE "bundle") 512 ))
66      (port (array (rename WIRE "wire") 512))
67      (joined
```

```
68        (portRef BUNDLE)
69        (portRef WIRE)
       ...
```

EDFN-129 (error) Line %d: An array member index less than 0 is not valid.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters a reference to an array member with a negative index. A reference call to a member of an array should have an index greater or equal to 0.

WHAT NEXT

Refer to the line number in the error message and locate the error. The recommended solution is to regenrated the EDIF file. However, if you know EDIF and the design well, you can go the error line and correct the problem by providing the correct member index.

EXAMPLES

```
  ...
50  (cell (rename rip_1x1 "rip_1x1") (cellType RIPPER)
51  (view (rename Schematic_representation "Schematic_representation")
52   (viewType SCHEMATIC)
53   (interface (port (array (rename bundle "bundle") 2))
54    (port (array (rename wire "wire") 2) )
55    (joined (portRef bundle) (portRef wire))
   )
  )
  ...
326  (joined (portRef (member wire -1) (instanceRef Ripper_2)) (portRef out0))
```

EXAMPLE MESSAGE

```
Error: Line 326: An array member index less than 0 is not valid. (EDFN-129)
```

In the above example, "wire" is an array of 2 (line 54), so the valid member indexes for "wire" are 0 and 1. Line 326 has reference to "wire" with the specified member index of -1. Below is a correct example:

```
... 50 (cell (rename rip_1x1 "rip_1x1") (cellType RIPPER) 51 (view (rename
Schematic_representation "Schematic_representation") 52 (viewType SCHEMATIC) 53
(interface (port (array (rename bundle "bundle") 2)) 54 (port (array (rename wire
"wire") 2) ) 55 (joined (portRef bundle) (portRef wire)) ) ) ... 326 (joined
(portRef (member wire 0) (instanceRef Ripper_2)) (portRef out0)
```

EDFN-130 (error) Line %d: The array member index is greater than the size of the referenced array.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters a reference to an array member with an index greater than the array size. You can reference a member of an array, but the index has to be between 0 and array size -1. For example, if the array size is 8, the index member should be from 0 to 7.

WHAT NEXT

Refer to the line number in the error message and locate the error. The recommended solution is to regenrated the EDIF file. However, if you know EDIF and the design well, you can go the error line and correct the problem by providing the correct member index.

EXAMPLES

```
  ...
50  (cell (rename rip_1x1 "rip_1x1") (cellType RIPPER)
51  (view (rename Schematic_representation "Schematic_representation")
52   (viewType SCHEMATIC)
53   (interface (port (array (rename bundle "bundle") 2))
54    (port (array (rename wire "wire") 2) )
55    (joined (portRef bundle) (portRef wire))
   )
  )
  ...
326  (joined (portRef (member wire 2) (instanceRef Ripper_2)) (portRef out0))
```

EXAMPLE MESSAGE

Error: Line 326: The array member index is greater than the size of the referenced array. (EDFN-130)

In the above example, "wire" is an array of 2 (line 54), so the valid member indexes for "wire" are 0 and 1. Line 326 has reference to "wire" with the specified member index of 2. Below is a correct example:

... 50 (cell (rename rip_1x1 "rip_1x1") (cellType RIPPER) 51 (view (rename Schematic_representation "Schematic_representation") 52 (viewType SCHEMATIC) 53 (interface (port (array (rename bundle "bundle") 2)) 54 (port (array (rename wire "wire") 2)) 55 (joined (portRef bundle) (portRef wire)))) ... 326 (joined (portRef (member wire 1) (instanceRef Ripper_2)) (portRef out0))

EDFN-131 (error) Line %d: A ripper with a multi-dimensional

port array is not supported.

DESCRIPTION

The EDIF reader issues this error when it encounters a ripper cell containing a multi-dimensional port array. The Synopsys EDIF reader only supports a ripper cell with two ports or two single-dimensional port arrays of the same width.

WHAT NEXT

Regenerate the EDIF file and specify to the EDIF writer not to write out a multi-dimensional port array for a ripper cell.

EXAMPLES

```
   ...
57   (cell ripCell (cellType RIPPER)
58    (view ripView (viewtype SCHEMATIC)
59     (interface
60      (port (array (rename BUNDLE "bundle") 2 4)
61      (port (array (rename WIRE "wire") 2 4)
    ...
```

EXAMPLE MESSAGE

```
Error: Line 60: A ripper with a multi-dimensional port array is not supported.
(EDFN-131)
```

In the above example, line 60 defines a two-dimensional array BUNDLE of size 2 by 4, and line 61 defines a two-dimensional array WIRE of size 2 by 4.

EDFN-132 (error) Line %d:
The dimension of the %sRef member construct does not match the dimension of the %s array being referenced.

DESCRIPTION

The EDIF reader issues this error message when it parses the EDIF input file and encounters a port member reference with the dimension which does not match the dimension of the referenced port array.

WHAT NEXT

Refer to the line number in the error message, and locate the problem. You can either regenerate the EDIF input file, or if you know EDIF and the design well, you can fix the dimension and re-import the EDIF input file.

EXAMPLES

```
      ...
90  (port (array (rename DIFF_6_0_ "DIFF[6:0]") 7) (direction OUTPUT))
      ...
188  (net n5
189   (joined (portRef (member DIFF_6_0_ 2 6)) (portRef P20 (instanceRef U3)))
      ...
```

EXAMPLE MESSAGE

Error: Line 189: The dimension of the portRef member construct does not match the dimension of the port array being referenced. (EDFN-132)

In the above example, port array DIFF[6:0] is a one dimensional arrray, but the port member reference a two dimensional array.

EDFN-133 (error) Line %d: The ripper cell is corrupt.

DESCRIPTION

The EDIF reader issues this error when it parses the EDIF input file and encounters an internal problem.

WHAT NEXT

To fix this problem, restart the command. If the problem persists, please contact the Synopsys help line.

EDFO-1 (warning) Some designs have no schematic.

DESCRIPTION

The variable edifout_netlist_only is set to false, and you executed the edif format write command. But for some of the designs that you want to write, no schematics have been created.

WHAT NEXT

If you want to write the designs without including schematic descriptions, set the variable edifout_netlist_only to true. Then execute the edif format write command again.

If you want to write the designs including schematic descriptions, execute the create_schematics command. Then execute the edif format write command again. If you're going to execute the edif format write command with the -hierarchy option, then be sure to also execute the create_schematics command with the -hierarchy option.

EDFO-2 (error) The meter scales in libraries '%s' and '%s' aren't equal.

DESCRIPTION

The meter scale is an attribute of a symbol library. It's used to ensure that when each of the symbols in that library is used in schematics creation, the scale of that symbol is compatible with that of every other symbol used in schematics creation. The scales in all libraries used in schematics creation must therefore be equal.

WHAT NEXT

If you want to use symbols from both of those symbol libraries, change the meter scale setting in the source text file of one or both of those libraries so that the attributes in each of the libraries will be equal to each other. Then compile those libraries again with the read_lib command. Then execute the create_schematics command again. Then execute the edif format write command again.

If one of those symbol libraries is not one that you want to use symbols from, make sure that there's a symbol in the source text file for each of the cell components that's instantiated in the designs that you want to write. Then compile again with the read_lib command those libraries that you just added symbols to. Then execute

the create_schematics command again. Then execute the edif format write command again.

EDFO-3 (error) The meter scale in library '%s' and external scale in library '%s' aren't equal.

DESCRIPTION

The meter scale and external scale are attributes of a symbol library. They are exactly equivalent to and interchangeable with each other (if a library has both attributes, the external scale is ignored and the meter scale is used). They're used to ensure that when each of the symbols in that library is used in schematics creation, the scale of that symbol is compatible with that of every other symbol used in schematics creation. The scales in all libraries used in schematics creation must therefore be equal.

WHAT NEXT

If you want to use symbols from both of those symbol libraries, change the meter scale (or external scale) setting in the source text file of one or both of those libraries so that the attributes in each of the libraries will be equal to each other. Then compile those libraries again with the read_lib command. Then execute the create_schematics command again. Then execute the edif format write command again.

If one of those symbol libraries is not one that you want to use symbols from, make sure that there's a symbol in the source text file for each of the cell components that's instantiated in the designs that you want to write. Then compile again with the read_lib command those libraries that you just added symbols to. Then execute the create_schematics command again. Then execute the edif format write command again.

EDFO-4 (error) The external scales in libraries '%s' and '%s' aren't equal.

DESCRIPTION

The external scale is an attribute of a symbol library. It's used to ensure that when each of the symbols in that library is used in schematics creation, the scale of that symbol is compatible with that of every other symbol used in schematics creation. The scales in all libraries used in schematics creation must therefore be equal.

WHAT NEXT

If you want to use symbols from both of those symbol libraries, change the external scale setting in the source text file of one or both of those libraries so that the attributes in each of the libraries will be equal to each other. Then compile those libraries again with the read_lib command. Then execute the create_schematics command again. Then execute the edif format write command again.

If one of those symbol libraries is not one that you want to use symbols from, make sure that there's a symbol in the source text file for each of the cell components that's instantiated in the designs that you want to write. Then compile again with the read_lib command those libraries that you just added symbols to. Then execute the create_schematics command again. Then execute the edif format write command again.

EDFO-5 (error) The external scale in library '%s' and meter scale in library '%s' aren't equal.

DESCRIPTION

The external scale and meter scale are attributes of a symbol library. They are exactly equivalent to and interchangeable with each other (if a library has both attributes, the external scale is ignored and the meter scale is used). They're used to ensure that when each of the symbols in that library is used in schematics creation, the scale of that symbol is compatible with that of every other symbol used in schematics creation. The scales in all libraries used in schematics creation must therefore be equal.

WHAT NEXT

If you want to use symbols from both of those symbol libraries, change the external scale (or meter scale) setting in the source text file of one or both of those libraries so that the attributes in each of the libraries will be equal to each other. Then compile those libraries again with the read_lib command. Then execute the create_schematics command again. Then execute the edif format write command again.

If one of those symbol libraries is not one that you want to use symbols from, make sure that there's a symbol in the source text file for each of the cell components that's instantiated in the designs that you want to write. Then compile again with the read_lib command those libraries that you just added symbols to. Then execute the create_schematics command again. Then execute the edif format write command again.

EDFO-6 (warning) No meter scale found for symbol libraries--

using external scale.

DESCRIPTION

The meter scale and external scale are attributes of a symbol library. They are exactly equivalent to and interchangeable with each other. If a library has both attributes, the external scale is ignored and the meter scale is used.

WHAT NEXT

Specify a symbol library that contains a meter scale.

EDFO-7 (warning) No meter scale or external scale found for symbol libraries.

DESCRIPTION

The meter scale and external scale are attributes of a symbol library. They are equivalent to and interchangeable with each other. If a library has both attributes, the external scale is ignored and the meter scale is used. The scales are used to ensure that when each of the symbols in that library are used in a schematics creation, the scale of that symbol is compatible with that of every other symbol used in the schematics creation. The scales in all libraries used in a schematics creation must, therefore, be equal.

If no meter scale or external scale attribute is found for the symbol libraries, then an arbitrary scale of 1 is used in the schematics creation.

WHAT NEXT

Specify symbol libraries which contain scale information.

EDFO-8 (error) %s ’%s’ has no symbol.

DESCRIPTION

If the schematic being written was created with the current release of the Synopsys Schematics Generator, then that schematic might be corrupt.

WHAT NEXT

If the schematic being written was created with the current release of the Synopsys Schematics Generator, please notify your Synopsys applications engineer. If you can

provide a test case, that will aid in fixing the problem. A test case that includes the original source and a log of the commands executed is the most useful.

If the schematic being written wasn't created with the current release of the Synopsys Schematics Generator, then execute the create_schematics command again. Then execute the edif format write command again.

EDFO-9 (error) A pin on cell '%s' has no port reference.

DESCRIPTION

If the schematic being written was created with the current release of the Synopsys Schematics Generator, then that schematic might be corrupt.

WHAT NEXT

If the schematic being written was created with the current release of the Synopsys Schematics Generator, please notify your Synopsys applications engineer. If you can provide a test case, that will aid in fixing the problem. A test case that includes the original source and a log of the commands executed is the most useful.

If the schematic being written wasn't created with the current release of the Synopsys Schematics Generator, then execute the create_schematics command again. Then execute the edif format write command again.

EDFO-10 (information) Net '%s' is renamed to '%s' in design '%s' because it's connected to the port by that name.

DESCRIPTION

The variable edifout_name_nets_same_as_ports is set to true, and you executed the edif format write command.

WHAT NEXT

If you don't want the name of each net that's connected to a port to be changed to the name of that port, set the variable edifout_name_nets_same_as_ports to false. Then execute the edif format write command again.

EDFO-11 (warning) Net '%s' is renamed to '%s' in design '%s'

because it’s not connected to the port by that name.

DESCRIPTION

The variable edifout_name_nets_same_as_ports is set to true, and you executed the edif format write command. Because the name of each net that’s connected to a port is changed to the name of that port, in order to avoid there being two different nets with the same name, the name of each net that’s not connected to a port but that is the same as the name of that port must be changed.

WHAT NEXT

If you don’t want the name of each net that’s connected to a port to be changed to the name of that port, set the variable edifout_name_nets_same_as_ports to false. Then execute the edif format write command again.

EDFO-12 (error) There’s %s in %s ’%s’ that has no name.

DESCRIPTION

This common error occurs when a pin in a cell instance has no name. It might happen when the original source of the design being written was in a format that can use order-based instantiation as well as name-based instantiation. Order-based instantiation occurs when pins are described by the *order* of the pins in a cell instance instead of by the *names* of the pins. The names of the pins therefore aren’t known.

WHAT NEXT

Change the description of the design in the original source of that design. Make sure that you use only name-based instantiation in the original source. Then read again with the **read** command the original source of the design that you just changed. Then execute the edif format **write** command again.

Alternatively, resolve the reference for this cell reference. If the reference is resolved, the pin name, direction, and width will be known. The reference can be resolved by reading in the design for this reference. To avoid the memory usage of reading in the entire design, make a copy of the design that contains only the port interface descriptions. This "dummy" design can be read in place of the entire design.

EDFO-13 (error) The value of variable '%s' isn't valid.

DESCRIPTION

The edif file can't be written unless the value of this variable is valid.

WHAT NEXT

Set this variable to a valid value. Then execute the edif format write command again.

EDFO-14 (warning) The variable 'edifout_power_and_ground_representation' is not defined using 'cell'.

DESCRIPTION

If you do not indicate how to represent power and ground, power and ground are arbitrarily represented as cells.

WHAT NEXT

cell is the default option for **edifout_power_and_ground_representation** variable, but you can specify **port** or **net** to represent power and ground.

EDFO-15 (error) The symbols '%s' and '%s' are both used as %s symbols.

DESCRIPTION

These are attributes of a symbol library: logic_0_symbol, logic_1_symbol, in_port_symbol, out_port_symbol, inout_port_symbol, in_osc_symbol, out_osc_symbol, inout_osc_symbol. They specify for each of these special components which symbol to use in schematics creation. There must be only one such attribute for each one.

WHAT NEXT

For example, there might be two attributes for the power cell symbol in the source text file of one of the symbol libraries: logic_1_symbol : "PWR"; logic_1_symbol : "VDD"; Delete all but one of those power cell symbol attributes. Then compile that library again with the read_lib command. Then execute the create_schematics command

again. Then execute the edif format write command again.

EDFO-16 (error) The schematic ’%s’ was created %s the "-no_bus" option, but the schematic ’%s’ was created %s the "-no_bus" option.

DESCRIPTION

When you execute the edif format write command with the -hierarchy option, all the schematics you want to write must have been created with or all must have been created without the "-no_bus" option.

WHAT NEXT

Either with or without the "-no_bus" option, execute the create_schematics command again with the -hierarchy option. Then execute the edif format write command again.

EDFO-17 (error) The width of bussed port ’%s’ in design ’%s’ can’t be resolved.

DESCRIPTION

If the design being written was compiled with the current release of the Synopsys Design Compiler, then that design might be corrupt.

WHAT NEXT

If the design being written was compiled with the current release of the Synopsys Design Compiler, please notify your Synopsys applications engineer. If you can provide a test case, that will aid in fixing the problem. A test case that includes the original source and a log of the commands executed is the most useful.

If the design being written wasn’t compiled with the current release of the Synopsys Design Compiler, then execute the compile command again. Then execute the edif format write command again.

EDFO-18 (error) The library of cell ’%s’ is corrupted.

Not all view identifier properties of the cell are found.

DESCRIPTION

These attributes are the view identifier properties of the symbol for a cell: edif_cell_name, edif_view_name, and edif_name_property. If a symbol has any of these attributes, then it must have all three of them.

WHAT NEXT

Change the symbol definition for the cell in the source text file of the symbol library. Either delete the view identifier property attributes that are there, so that the symbol has none of those attributes, or add appropriate view identifier property attributes, so that the symbol has all three of those attributes. Then compile that symbol library again with the read_lib command. Then execute the create_schematics command again. Then execute the edif format write command again.

EDFO-19 (warning) The library of cell '%s' is corrupted. Not all view identifier properties of the cell are found.

DESCRIPTION

These attributes are the view identifier properties of the symbol for a cell: edif_cell_name, edif_view_name, and edif_name_property. If a symbol has any of these attributes, then it must have all three of them.

WHAT NEXT

Change the symbol definition for the cell in the source text file of the symbol library. Either delete the view identifier property attributes that are there, so that the symbol has none of those attributes, or add appropriate view identifier property attributes, so that the symbol has all three of those attributes. Then compile that symbol library again with the read_lib command. Then execute the create_schematics command again. Then execute the edif format write command again.

EDFO-20 (warning) Change '%s' of type %s to '%s' to match vhdl name.

DESCRIPTION

The variable edifout_match_vhdl_names is set to true, and you executed the edif format write command.

WHAT NEXT

If you don’t want the names of objects changed to conform to VHDL naming rules, set the variable edifout_match_vhdl_names to false.

EDFO-21 (error) A bussed off-sheet connector of width %d and an off-sheet connector are both named ’%s’.

DESCRIPTION

If the schematic being written was created with the current release of the Synopsys Schematics Generator, then that schematic might be corrupt.

WHAT NEXT

If the schematic being written was created with the current release of the Synopsys Schematics Generator, please notify your Synopsys applications engineer. If you can provide a test case, that will aid in fixing the problem. A test case that includes the original source and a log of the commands executed is the most useful.

If the schematic being written wasn’t created with the current release of the Synopsys Schematics Generator, then execute the create_schematics command again. Then execute the edif format write command again.

EDFO-22 (error) Two bussed off-sheet connectors of width %d and of width %d are both named ’%s’.

DESCRIPTION

If the schematic being written was created with the current release of the Synopsys Schematics Generator, then that schematic might be corrupt.

WHAT NEXT

If the schematic being written was created with the current release of the Synopsys Schematics Generator, please notify your Synopsys applications engineer. If you can provide a test case, that will aid in fixing the problem. A test case that includes the original source and a log of the commands executed is the most useful.

If the schematic being written wasn’t created with the current release of the Synopsys Schematics Generator, then execute the create_schematics command again.

Then execute the edif format write command again.

EDFO-23 (error) One of the pins or ports in %s '%s' is corrupted.

DESCRIPTION

If the schematic being written was created with the current release of the Synopsys Schematics Generator, then that schematic might be corrupt.

WHAT NEXT

If the schematic being written was created with the current release of the Synopsys Schematics Generator, please notify your Synopsys applications engineer. If you can provide a test case, that will aid in fixing the problem. A test case that includes the original source and a log of the commands executed is the most useful.

If the schematic being written wasn't created with the current release of the Synopsys Schematics Generator, then execute the create_schematics command again. Then execute the edif format write command again.

EDFO-24 (error) Port reference '%s' on cell '%s' has no design reference.

DESCRIPTION

If the schematic being written was created with the current release of the Synopsys Schematics Generator, then that schematic might be corrupt.

WHAT NEXT

If the schematic being written was created with the current release of the Synopsys Schematics Generator, please notify your Synopsys applications engineer. If you can provide a test case, that will aid in fixing the problem. A test case that includes the original source and a log of the commands executed is the most useful.

If the schematic being written wasn't created with the current release of the Synopsys Schematics Generator, then execute the create_schematics command again. Then execute the edif format write command again.

EDFO-25 (error) There's no port for port reference '%s' on

design ’%s’.

DESCRIPTION

If the schematic being written was created with the current release of the Synopsys Schematics Generator, then that schematic might be corrupt.

WHAT NEXT

If the schematic being written was created with the current release of the Synopsys Schematics Generator, please notify your Synopsys applications engineer. If you can provide a test case, that will aid in fixing the problem. A test case that includes the original source and a log of the commands executed is the most useful.

If the schematic being written wasn’t created with the current release of the Synopsys Schematics Generator, then execute the create_schematic command again. Then execute the edif format write command again.

EDFO-26 (error) One of the nets in schematic ’%s’ is corrupted.

DESCRIPTION

If the schematic being written was created with the current release of the Synopsys Schematics Generator, the schematic may be corrupt.

WHAT NEXT

If the schematic being written was created with the current release of the Synopsys Schematics Generator, notify your Synopsys applications engineer. To aid in fixing the problem, provide a test case if possible. Most useful are a test case that includes the original source and a log of the commands executed.

If the schematic being written wasn’t created with the current release of the Synopsys Schematics Generator, execute the **create_schematics** command again. Then execute the edif format **write** command again.

EDFO-27 (error) The schematic ’%s’ is corrupted.

DESCRIPTION

If the schematic being written was created with the current release of the Synopsys Schematics Generator, then that schematic might be corrupt.

WHAT NEXT

If the schematic being written was created with the current release of the Synopsys Schematics Generator, please notify your Synopsys applications engineer. If you can provide a test case, that will aid in fixing the problem. A test case that includes the original source and a log of the commands executed is the most useful.

If the schematic being written wasn’t created with the current release of the Synopsys Schematics Generator, then execute the create_schematics command again. Then execute the edif format write command again.

EDFO-28 (error) The schematic ’%s’ was created with the "-bit_mappers" option.

DESCRIPTION

When you execute the edif format write command, the schematics you want to write must not have been created with the "-bit_mappers" option.

WHAT NEXT

Without the "-bit_mappers" option, execute the create_schematics command again. Then execute the edif format write command again.

EDFO-29 (error) The schematic ’%s’ was created with the "-implicit" option.

DESCRIPTION

When you execute the edif format write command, the schematics you want to write must not have been created with the "-implicit" option.

WHAT NEXT

Without the "-implicit" option, execute the create_schematics command again. Then execute the edif format write command again.

EDFO-30 (error) The symbol for '%s' is corrupted.

DESCRIPTION

If the schematic being written was created with the current release of the Synopsys Schematics Generator, then that schematic might be corrupt.

WHAT NEXT

If the schematic being written was created with the current release of the Synopsys Schematics Generator, please notify your Synopsys applications engineer. If you can provide a test case, that will aid in fixing the problem. A test case that includes the original source and a log of the commands executed is the most useful.

If the schematic being written wasn't created with the current release of the Synopsys Schematics Generator, then execute the create_schematics command again. Then execute the edif format write command again.

EDFO-31 (information) Schematic '%s' might have been modified due to netcon insertion.

DESCRIPTION

Obsolete

WHAT NEXT

Obsolete

EDFO-32 (error) The cell for '%s' is corrupted.

DESCRIPTION

If the design being written was created with the current release, then that design might be corrupt.

WHAT NEXT

If the design being written was created with the current release, please notify your Synopsys applications engineer. If you can provide a test case, that will aid in fixing the problem. A test case that includes the original source and a log of the commands executed is the most useful.

If the design being written wasn’t created with the current release, then create the design again. Then execute the edif format write command again.

EDFO-33 (error) The special symbols in the schematic ’%s’ are not the same as the special symbols in the schematic ’%s’.

DESCRIPTION

When you execute the edif format **write** command with the *-hierarchy* option, all of the schematics you want to write must have been created with the same special symbols.

WHAT NEXT

Execute the **create_schematics** command again with the *-hierarchy* option. Then execute the edif format **write** command again.

EDFO-34 (error) Library ’%s’ has no symbols.

DESCRIPTION

A library created with the current release of the Synopsys Library Compiler has no symbols.

WHAT NEXT

Make sure the library source text file has symbol constructs in it, and execute the **read_lib** command again. Then execute the edif format **write_lib** command again.

EDFO-35 (error) The library ’%s’ is corrupted.

DESCRIPTION

If the library being written was created with the current release of the Synopsys Library Compiler, the library might be corrupt.

WHAT NEXT

If the library being written was created with the current release of the Synopsys

Library Compiler, notify your Synopsys applications engineer. It will help to correct the problem if you can provide a test case that includes the original source and a log of the commands executed.

If the library being written was not created with the current release of the Synopsys Library Compiler, execute the **read_lib** command again. Then execute the edif format **write** command or the edif format **write_lib** command again.

EDFO-36 (error) The schematic '%s' was created with the "-no_rip" option.

DESCRIPTION

When you execute the edif format **write** command, the schematics you want to write must not have been created with the *-no_rip* option.

WHAT NEXT

Without the *-no_rip* option, execute the **create_schematics** command again. Then execute the edif format **write** command again.

EDFO-37 (warning) The variable '%s' is obsolete.

DESCRIPTION

This variable no longer has any effect.

WHAT NEXT

Remove the setting of this variable from your script.

EDFO-38 (error) The values of variables '%s' and '%s' aren't compatible.

DESCRIPTION

The edif file can't be written unless the values of these variables are compatible.

WHAT NEXT

Set these variables to compatible values. Then execute the edif format **write** command again.

EDFO-39 (error) The values of variables '%s' and '%s' aren't compatible.

DESCRIPTION

The edif file can't be written unless the values of these variables are compatible.

WHAT NEXT

Set these variables to compatible values. Then execute the edif format **write** command again.

EDFO-40 (warning) Bussed port '%s' in design '%s' cannot be represented as a multidimension array.

DESCRIPTION

The structure of the bus is such that there can be no multidimension array interpretation.

WHAT NEXT

Do not to use multidimension buses in your design.

EDFO-41 (error) One of the bussed pins or ports in design '%s' can't be represented as a numerical array.

DESCRIPTION

The structure of the bus is one for which there can be no numerical array interpretation.

WHAT NEXT

edifout_numerical_array_members variable can only support buses which have indexes greater than 0, check your design to make sure all of the buses have indexes greater than 0.

EDFO-42 (error) The power or ground reference is corrupted.

DESCRIPTION

If the design being written was created with the current release of the Synopsys Design Compiler, the design might be corrupt.

WHAT NEXT

If the design being written was created with the current release of the Synopsys Design Compiler, notify your Synopsys applications engineer. It will help to correct the problem if you can provide a test case that includes the original source and a log of the commands executed.

If the design being written was not created with the current release of the Synopsys Design Compiler, execute the **read** command again. Then execute the edif format **write** command again.

EDFO-43 (error) Specified to write the power cell in the external library that actually contains the ground cell and to write the ground cell in the external library that actually contains the power cell. This is not supported.

DESCRIPTION

Writing both the power cell in the external library that actually contains the ground cell and the ground cell in the external library that actually contains the power cell is not supported.

WHAT NEXT

Set the variables edifout_power_library_name and edifout_ground_library_name correctly. Then execute the edif format **write** command again.

EDFO-44 (error) %s '%s' in %s '%s' is corrupted.

DESCRIPTION

If the design or schematic being written was created with the current release of the Synopsys Design Compiler or Schematics Generator respectively, then that design or schematic might be corrupt.

WHAT NEXT

If the design or schematic being written was created with the current release of the Synopsys Design Compiler or Schematics Generator respectively, please notify your Synopsys applications engineer. If you can provide a test case, that will aid in fixing the problem. A test case that includes the original source and a log of the commands executed is the most useful.

If the design or schematic being written wasn't created with the current release of the Synopsys Design Compiler or Schematics Generator respectively, then execute the **read** or **create_schematics** command respectively again. Then execute the edif format **write** command again.

EDFO-45 (information) The design '%s' uses the logic %s reference '%s' in the library '%s'.

DESCRIPTION

WHAT NEXT

EDFO-46 (warning) The design '%s' uses the built-in Synopsys logic %s reference.

DESCRIPTION

The system does not find user's specified power and ground reference, so it is using the Synopsys built in logic references.

WHAT NEXT

Specify the source for power and ground, or let the system use the Synopsys built in power and ground source.

EDFO-47 (warning) File %s, line %d: '%s' '%s' cannot change to existing '%s' '%s'.

DESCRIPTION

The system is detecting that there are two different objects with the same name.

WHAT NEXT

Ensure that your design does not contain multiple objects with the same name.

ELAB-3 (warning) %s Extraneous argument for system function/task %s ignored.

DESCRIPTION

If you provide more arguments than the compiler requires when you make a system function or task call, the compiler ignores the extraneous arguments.

WHAT NEXT

This is a warning message only and requires no action on your part.

SEE ALSO

elaborate (2).

ELAB-5 (warning) %s Encountered extra ’dc_script_begin’ pragma.

DESCRIPTION

The **read** command or **elaborate** command issues this warning code when an extra ’dc_script_begin’ is encountered in the vhdl design.

For e.g. -- pragma dc_script_begin -- set_dont_touch find (net, N1) false -- pragma dc_script_end -- pragma dc_script_begin <<-- extra ’dc_script_begin’ pragma.

WHAT NEXT

Locate the extra ’dc_script_begin’ in the vhdl design at the specified line number. Then either provide corresponding ’dc_script_end’ pragma or remove it, as intended.

SEE ALSO

elaborate (2), **read** (2).

ELAB-6 (warning) %s Encountered extra ’dc_script_end’

pragma.

DESCRIPTION

The **read** command or **elaborate** command issues this warning code when an extra 'dc_script_end' is encountered in the vhdl design.

For e.g. -- pragma dc_script_begin -- set_dont_touch find (net, N1) false -- pragma dc_script_end -- pragma dc_script_end <<-- extra 'dc_script_end' pragma.

WHAT NEXT

Locate the extra 'dc_script_end' in the vhdl design at the specified line number. Then either provide corresponding 'dc_script_begin' pragma or remove it, as intended.

SEE ALSO

elaborate (2), **read** (2).

ELAB-7 (error) %s Disable Presto features in Verification Friendly DC Mode

DESCRIPTION

If you use multiple dimension array in Verication Friendly DC Mode, this error message will happen.

WHAT NEXT

Rewrite RTL source codes or remove special Presto directives.

SEE ALSO

elaborate (2), **read** (2).

ELAB-8 (warning) %s Disable Presto features in verification

friendly mode

DESCRIPTION

If you use enum directive and label directive in Verication Friendly DC Mode, this warning message will happen.

WHAT NEXT

Rewrite RTL source codes or remove special Presto directives.

SEE ALSO

elaborate (2), **read** (2).

ELAB-9 (warning) %s Manual resource sharing pragmas will be ignored.

DESCRIPTION

This warning message occurs when the **hdlin_disable_manual_resource_sharing** variable is set to true. All of the manual resource sharing pragmas are ignored. The default value of the variable is false.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, you can use manual resource sharing by setting the **hdlin_disable_manual_resource_sharing** variable to false.

SEE ALSO

hdlin_disable_manual_resource_sharing(3)

ELAB-28 (warning) %s SCALARED keywords are ignored.

DESCRIPTION

You receive this warning to let you know that for synthesis purposes, the compiler ignores the scalared keyword.

WHAT NEXT

This is a warning only and requires no action on your part.

SEE ALSO

elaborate (2).

ELAB-33 (warning) %s SV Assertions are ignored for synthesis since %s is not set to true.

DESCRIPTION

This warning message issues once for each module elaboration where the Presto HDL Compiler encounters a labelled assertion or assertion severity system task call that must be ignored due to the tcl environment variable setting cited in the message. Because SystemVerilog Assertions (SVA) allow synthesis' optimizers to recognize more "don't care" conditions than otherwise specified by the RTL, they are not applied by default but must be enabled - both as a product feature and also by certifying that individual assertions have proven to be unreachable prior to synthesizing this RTL.

WHAT NEXT

This is only a warning message. No action is required.

However, if you want the construct to be either exploited or ignored with no warnings, you must set **hdlin_enable_assertions** to true and also establish its assertion label (with lexical scope) as an element of the **confirmed_SVA()** environment array giving this a true or false value.

SEE ALSO

analyze(2)
elaborate(2)
hdlin_enable_assertions(3)

ELAB-65 (warning) %s Always block that has both a timing control statement as well as embedded event (@) expression is not supported by synthesis.

DESCRIPTION

You receive this warning when an always block has both a timing control statement

and an embedded event (@) expression, a situation that Synthesis does not support.

WHAT NEXT

Change the always block description by removing either the timing control statement or the embedded event (@) expression. Then invoke the compiler again.

SEE ALSO

elaborate (2).

ELAB-66 (warning) %s The event depends on both edge and nonedge expressions, which synthesis does not support.

DESCRIPTION

You receive this warning message because you have assigned to an event both edge and nonedge expressions, which Synthesis does not support.

WHAT NEXT

Modify your description so that the event depends on either an edge expression or a nonedge expression, but not both.

SEE ALSO

elaborate (2).

ELAB-67 (warning) %s Only simple variables are allowed in the sensitivity list for synthesis.

DESCRIPTION

You receive this warning because you have not included simple variables in the sensitivity list. Synthesis supports only simple variables in the sensitivity list.

WHAT NEXT

Use simple variables in the sensitivity list. Then invoke the compiler again.

SEE ALSO

elaborate (2).

ELAB-68 (warning) %s The event depends on two edges of the same variable, which synthesis does not support.

DESCRIPTION

You receive this warning because you have assigned to an event two edges of the same variable, which synthesis does not support.

WHAT NEXT

Modify your description so that the event depends on only one edge of the variable. Then invoke the compiler again.

SEE ALSO

elaborate (2).

ELAB-69 (warning) %s In the event expression with ’posedge’ or ’negedge’ qualifier, synthesis allows only simple variables.

DESCRIPTION

You receive this warning to let you know that synthesis allows only simple variables in an event expression with a ’posedge’ or ’negedge’ qualifier. If the event expression in your description contains no simple variables, you receive this warning.

WHAT NEXT

Modify your description to include only simple variables in the event expression.

SEE ALSO

elaborate (2).

ELAB-90 (error) %s Always block that has both a timing control

statement as well as embedded event (@) expression is not supported by synthesis.

DESCRIPTION

You receive this error message when an always block has both a timing control statement and embedded event (@) expression, which synthesis does not support.

WHAT NEXT

Change the always block description by removing either the timing control statement or the embedded event (@) expression. Then invoke the compiler again.

SEE ALSO

elaborate (2).

ELAB-91 (error) %s The event depends on both edge and nonedge expressions, which synthesis does not support.

DESCRIPTION

You receive this error message because you have assigned to an event both edge and nonedge expressions, which Synthesis does not support.

WHAT NEXT

Modify your description so that the event depends on either an edge expression or a nonedge expression, but not both.

SEE ALSO

elaborate (2).

ELAB-92 (warning) %s Only simple variables are allowed in the sensitivity list for synthesis.

DESCRIPTION

You receive this warning message because you have not included simple variables in

the sensitivity list. Synthesis supports only simple variables in the sensitivity list.

WHAT NEXT

Use simple variables in the sensitivity list. Then invoke the compiler again.

SEE ALSO

elaborate (2).

ELAB-93 (error) %s Events that depend on two edges of the same variable are not supported by synthesis.

DESCRIPTION

You receive this error message because you have put in the event expression both 'posedge' and 'negedge' of the same variable. Synthesis supports only one edge of a variable in the event expression.

WHAT NEXT

Review your design description and decide which edge you want to use. Then invoke the **elaborate** command again.

SEE ALSO

elaborate (2).

ELAB-94 (error) %s In the event expression with 'posedge' or 'negedge' qualifier, synthesis allows only simple variables.

DESCRIPTION

You receive this error message because you did not specify simple variables only under a 'posedge' or 'negedge' qualifier in the event expression. Synthesis supports only simple variables under those qualifiers.

WHAT NEXT

Review your design description and make the appropriate changes, using only simple variables under 'posedge' or 'negedge'. Then invoke the compiler again.

SEE ALSO

elaborate (2).

ELAB-95 (error) %s Unsupported expressions appear in the sensitivity list.

DESCRIPTION

You receive this error message because unsupported expressions appear in the sensitivity list with posedge or negedge. Only simple variables, or variables indexed by a constant or a constant expression as offset, are allowed in the sensitivity list with posedge or negedge, by synthesis policy. For example:

```
parameter p=5;
 always @(posedge a[p+2])
```

WHAT NEXT

Change the expression following posedge or negedge so it conforms to the above synthesis policy.

SEE ALSO

elaborate (2).

ELAB-100 (warning) %s Variable '%s' is a legacy of HDL Compiler. For Presto HDL compiler, please use '%s' instead.

DESCRIPTION

This is an old HDLC variable.

WHAT NEXT

ELAB-101 (error) %s %s in constant function is illegal.

DESCRIPTION

Illegal action inside constant function.

WHAT NEXT

ELAB-102 (warning) %s %s in constant function will be ignored.

DESCRIPTION

The action inside constant function will be ignored.

WHAT NEXT

ELAB-103 (error) %s Try to get value of parameter before the declaration of the parameter.

DESCRIPTION

Try to get value of parameter before the declaration of the parameter!.

WHAT NEXT

ELAB-104 (warning) %s Symbol '%s' is not included in modport.

DESCRIPTION

This symbol is not included in modport.

WHAT NEXT

ELAB-105 (error) %s The name '%s' is not a modport of the interface instance actually provided on port '%s'.

DESCRIPTION

This issues during the elaboration of an module or interface one of whose formal ports requires a modport with the specified name to be supplied as the actual port of the instantiation. The actual interface provided on the indicated port did not satisfy that expectation. Either an interface instance was provided with no such modport defined, or a modport of a different name was passed by mistake.

WHAT NEXT

Check the spelling of the modport name vs the modports declared by the interface type of the instance being provided on this port.

ELAB-106 (warning) %s A symbol named '%s' is already defined differently in the receiving scope.

DESCRIPTION

This warning message issues in SystemVerilog contexts when a problem arises merging two copies of a well-known scope. It indicates that two or more reuses of a common definition are not actually in perfect agreement about its authorship or meaning.

SystemVerilog modules and interfaces share access to global "compilation unit" scopes such as $unit (formerly known as $root) and to SV package scopes. When they are separately analyzed, each module's or interface's .pvl file, and each package's .pvk file holds a replica of selected entities within these scopes. Package imports, interface instantiations, and type parameterizations expect to share these common definitions. So as the separate parts are recombined, the SystemVerilog compiler applies a "trust-but-verify" protocol before accepting the equivalence of a foreign definition to its local homograph. If the declaration, scope, and provenance (i.e., source code location) of the two symbols match up perfectly, they can become identified with each other. When this protocol fails, compilation proceeds by accepting both homographs.

The message is only a warning, because both definitions survive after the merger and continue to support all their existing referents. References to the foreign definition that arrive alongside it continue to refer to the foreign definition. References to the name in the receiving scope are bound to its lexically local definition. But future mergers of the receiving scope with any others can cause multiple repeats of the warning. Also, the existence of two meanings for one name may make some compiler output ambiguous. The presence of type homographs can result in strict datatype mismatches and unexpected results from type comparison operations.

WHAT NEXT

Locate the relevant declaration(s) of this name. If the name is not one you declared (e.g. it looks like it might be a compiler temporary), it usually belongs to a struct or enum type declaration which you might know by one or more typedef'ed names. The internal name for a struct or enum type becomes visible in instantiation reports when the type is passed as a type parameter; experiments using that feature can help to locate these.

The location info in this report may point either to the semantic action which merges scopes, or to one of the homograph declarations. Merge actions can occur deeply nested in the actual receiving scope, so be sure to consider the name's definition in all parent scopes of the reported line number, too. If the declaration sites are not all within the source file currently being analyzed or read, consider

how they come to be included in this compilation. There must be just one lexical occurrence of the declaration of any strong data type. Function, task and named block declarations must be reproduced verbatim, and ideally should be acquired by file inclusion or package reference.

The problem may be related to ‘include file revisions, to ‘include’ing one file into several scopes, or to an attempt to pass a type parameter or refer to a package between incompatible compilations of the same application. Occasionally this warning also arises due to imperfections in DC SystemVerilog’s ability to match up copies of enum types, or certain types of generated names. If you suspect this to be the case, contact Synopsys support.

Check that files ‘included by both compilation units are the same version of the same file, and that they use the same basename for the file, even if the directory paths differ. Some matching criteria are sensitive to line location and token sequencing. Note that macro expansion outcomes can differ due to the ‘define namespace of separate analyze commands, or the prevailing ‘defines at different points of inclusion. One file, analyzed with different releases of the dc_shell tool, may be incompatible with itself; although analyses done on distinct hosts or even operating systems with the same release level of dc_shell should be interchangeable. ELAB-106 is extra sensitive to many subtle kinds of miscoordination between separately compiled components. If you are integrating subprojects for their first time, you will need to establish uniform ways of preparing any infrastructure they share.

SEE ALSO

http://en.wiktionary.org/wiki/homograph (external **link), http://en.wikipedia.org/wiki/Graph_isomorphism_problem** (external **link), analyze** (2), **read** (2), **hdlin_sv_packages** (3), **VER-21** (n), **VER-930** (n), **VER-934** (n).

ELAB-107 (error) %s Wrong slice size .

DESCRIPTION

Wrong slice size.

WHAT NEXT

ELAB-108 (error) %s Attempt to operate %s on null string.

DESCRIPTION

Attempt to operate on null string.

WHAT NEXT

ELAB-109 (error) %s Type query specifies nonexistent dimension.

DESCRIPTION

Type query specifies nonexistent dimension.

WHAT NEXT

ELAB-110 (error) %s Invalid hierarchical modport port.

DESCRIPTION

Invalid hierarchical modport port.

WHAT NEXT

ELAB-111 (error) %s Unsupported operation on double: %s.

DESCRIPTION

Unsupported operation on double.

WHAT NEXT

ELAB-112 (error) %s Multiple sequential assignment.

DESCRIPTION

Multiple sequential assignment.

WHAT NEXT

ELAB-113 (error) %s Non-standard synchronous coding style not supported.

DESCRIPTION

```
Non-standard synchronous coding style not supported.
```

WHAT NEXT

ELAB-114 (warning) %s Variable %s has an invalid value: %s.

DESCRIPTION

WHAT NEXT

ELAB-115 (error) %s RTL Netlist found.

DESCRIPTION

```
RTL Netlist found.
```

WHAT NEXT

ELAB-116 (warning) %s Variable %s is not supported in Incremental Mode.

DESCRIPTION

WHAT NEXT

ELAB-117 (error) %s Array of GTECH_* instances is not

supported yet.

DESCRIPTION

Array of GTECH_* instances is not supported yet.

WHAT NEXT

ELAB-118 (error) %s Unsupported resource : %s .

DESCRIPTION

WHAT NEXT

ELAB-119 (error) %s Array length should be positive integer.

DESCRIPTION

This message issues because you have provided a zero or negative value when specifying an array length.

EXAMPLE

When you try to convert an integer to an array type in VHDL, you might write

```
...
CONV_UNSIGNED(A, 0)
...
```

which requests an empty vector of bits - the zero here is not correct. Or in SystemVerilog you might use a C-style declaration to declare

```
byte lcd_text[N];
...
```

which can provoke this error if N = -42.

WHAT NEXT

Correct the values of the array length in your design.

ELAB-120 (warning) %s %s does not exist, resource declaration will be ignored.

DESCRIPTION

This warning message will happen when the operator does not have the operator label in resouce declaration, or the opearator is optimized away. Then the resource declaration will be ignored.

WHAT NEXT

If the user wants to use resouce declaration, please add the operator label for the operator.

ELAB-130 (warning) %s The initial value for signal '%s' is not supported for synthesis. Presto ignores it.

DESCRIPTION

You receive this warning message if the signal is assigned an initial value when it is declared. Presto VHDL ignores initial values for signals. If the only assignment to a signal is from the initial value declaration, the signal will be treated as an undriven net for synthesis. Any nets that remain undriven will be tied to zero during optimization. This will cause a simulation-synthesis mismatch if the initial value is not zero.

WHAT NEXT

You may ignore this warning, if the declaration initialization is not the only assignment to this signal. However, if the declaration initialization is the only assignment to this signal, then either a second assignment to the signal should be added, or a constant should be used instead. Leaving the declaration initialization as the only the assignment to the signal will likely cause a simulation-synthesis mismatch.

ELAB-160 (error) %s Redeclaration of port '%s' is not allowed.

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the Presto HDL Compiler has detected that the same port is declared twice inside the same function, task, or module. Following is an example that illustrates this type of error:

```
function f;
 input a;
 input a;      // redeclaration of already declared port
  ...
endfunction;
```

WHAT NEXT

Remove or rename as appropriate one of these ports.

SEE ALSO

analyze (2), **read** (2).

ELAB-182 (error) %s Task call %s should not have parentheses unless it has a parameter.

DESCRIPTION

You receive this error message because the task declaration you wrote has an empty parameter list.

The following example shows a task declaration that would generate this error:

```
task foo();
...
endtask
```

The correct task declaration is

```
task foo;
...
endtask
```

WHAT NEXT

Rewrite the task declaration as shown in the example, removing the parentheses.

SEE ALSO

analyze (2), **read** (2).

ELAB-190 (warning) %s Constructs from STD.TEXTIO are not

supported for synthesis, they will be ignored. %s

DESCRIPTION

You receive this warning from the **read** command or the **elaborate** command, either of which issues this message when constructs from STD.TEXTIO package are in use. The details of the error appear in the message.

WHAT NEXT

To avoid receiving this warning message in the future, remove the constructs from STD.TEXTIO package. This warning message can be safely ignored.

SEE ALSO

elaborate (2), **read** (2). **hdlin_ignore_textio_constructs** (3).

ELAB-191 (error) %s Constructs from STD.TEXTIO package are not supported. %s

DESCRIPTION

You receive this error from the **read** command or the **elaborate** command, either of which issues this message when constructs from STD.TEXTIO package are in use. The details of the error appear in the message.

WHAT NEXT

To avoid receiving this error message in the future, remove the constructs from STD.TEXTIO package.

SEE ALSO

elaborate (2), **read** (2). **hdlin_ignore_textio_constructs** (3).

ELAB-192 (warning) %s There are nonblocking assignments inside TASK that set output/inout port '%s'; this may introduce

simulation mismatch.

DESCRIPTION

This warning message occurs when TASK has nonblocking assignments that set the output or inout ports. This may introduce simulation mismatch, for example:

```
module ShiftR (Out, In);
output Out;
input In;
reg Out;
always@(In)
     tShift(Out, In );
task tShift(output Q, input D);
      Q <= D ;
endtask
endmodule
```

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid receiving this warning message, do not set the output or inout port of TASK using a nonblocking assignment. You can change the output or inout port as a global variable. The above example can be rewritten as follows:

```
module ShiftR (Out, In);
output Out;
input In;
reg Out;
always@(In)
     tShift(In);
task tShift(input D);
      Q <= D ;
endtask
endmodule
```

SEE ALSO

elaborate(2)
read(2)

ELAB-201 (warning) %s Unconnected output ’%s’ in function

call tied to ground.

DESCRIPTION

Presto has found that the named output is not driven by any logic for this instance of function call. Sometimes this represents an issue in your design and sometimes it doesn’t. You should review your source code to ensure that this will not translate into incorrect outputs.

Presto has grounded the logic that may depend on these function outputs.

An example of this situation happens in the following code:

```
procedure elab_201_example(in1: in std_logic;
                           out1: out std_logic;
                           undriven_out : out std_logic_vector)
begin
    out1 := ’0’;
end procedure elab_201_example;
```

WHAT NEXT

ELAB-207 (error) %s Malformed specify block in Verilog source code.

DESCRIPTION

You receive this error message because your Verilog source code contains an invalid use of a specify block.

The following example, containing two specify blocks in the same module (an invalid instance), illustrates this type of error.

```
module m;
  ...
  specify
   ...
  endspecify
  ...
  specify
   ...
  endspecify
  ...
endmodule;
```

WHAT NEXT

Modify your Verilog source code to remove the inavlid usage.

SEE ALSO

analyze (2), **read** (2).

ELAB-210 (Error) %s integer overflow occurs.

DESCRIPTION

You receive this error message because there is an integer overflow in an arithmetic operation.

For example, the following code causes the error message because the operation 2**32 overflows in the range of integers.

```
   module M (a,d);
   input [31:0] a;
   output [31:0] d;
   reg [31:0] d;

   always begin
     d = 2**32 - a;
     $display ("d = %d
", d);
   end

   endmodule
```

Another possible integer overflow case is introduced by verilog shifter. By verilog language standard, the right operand of a shifter is always treated as an unsigned number. The constant '-1' (32'b11111111111111111111111111111111) in the following example is interpreted as unsigned number, which causes the integer overflow.

```
   module m (input [1:0] in1, output [1:0] out1);
   assign out1 = (in1 << -1);
   endmodule
```

WHAT NEXT

Check the operand of the operator, on the line indicated by the error message, to ensure that the result is within integer range, or use a Verilog number vector to represent a large value.

SEE ALSO

elaborate (2), **read** (2).

ELAB-229 (error) %s 0-repeat concat not supported in generate expressions.

DESCRIPTION

This error message occurs because an expression in generate block contains a 0-repeat concat operation that Presto HDL Compiler does not support.

WHAT NEXT

Rewrite your source code to remove the occurance of 0-repeat concats and try again.

SEE ALSO

elaborate (2), **read** (2).

ELAB-230 (error) %s Multiple blocks have been named '%s' in a scope.

DESCRIPTION

You get this error when two (or more) blocks with the same name are declared in the same local scope.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

ELAB-231 (error) %s %s declaration redeclares symbol '%s'.

DESCRIPTION

You see this message because you have assigned a function or task declaration to a symbol that has already been defined.

In the following example, which demonstrates such a situation, the symbol *f* is

declared twice: first as a register and then as a function:

```
reg f;          // initial declaration of 'f'

function f;     // illegal redeclaration of 'f'
...
endfunction
```

The example elicits the VER-106 message.

WHAT NEXT

Rename either the function declaration or the other declaration and all corresponding uses of the symbol.

SEE ALSO

analyze (2), **read** (2).

ELAB-255 (error) %s Internal error in %s at line %d.

DESCRIPTION

You receive this error message because an internal compiler error has occurred, related to the indicated position in the source code.

The nature of this error prevents availability of more specific information about it.

WHAT NEXT

Please file a star against Presto with your testcase if it's possible.

SEE ALSO

elaborate (2), **read** (2).

ELAB-256 (error) %s %s call violation: %s.

DESCRIPTION

You receive this error because the RTL power constructs were used incorrectly. The RTL power constructs include power, isolate and retain calls. The reason can be incorrect number of parameters, unsupported parameter types, width mismatch or the wrong place to call the functions.

WHAT NEXT

For details on how to use RTL power constructs, please refer to the Power Compiler User Guide, chapter "Implementing Multivoltage Designs Using RTL Isolation and Power Constructs", and section "Multivoltage Elements: $isolate and $power".

SEE ALSO

elaborate (2), **read** (2).

ELAB-275 (error) %s You must specify a named block with infer_mux when used outside a case statement.

DESCRIPTION

You receive this error message because you have used the Synopsys *infer_mux* pragma outside of a *case* statement without specifying the label of a named block on which MUX inference is to be applied.

WHAT NEXT

Using *infer_mux*, specify the label of the named block on which you want to apply MUX inference. Then invoke the compiler again.

SEE ALSO

elaborate (2).

ELAB-276 (warning) %s All symbols and listed symbols are designated as %s set/reset in block '%s'; using the all designation.

DESCRIPTION

You receive this warning because you have designated incompatible conditions, which the compiler has to resolve:

• You have explicitly marked a symbol as a set/reset signal in a list of symbols annotated with the Synopsys set/reset pragma.

• You have implicitly marked the symbol as a set/reset signal using the Synopsys

pragma that applies set/reset inferencing to all symbols.

Under these circumstances, the compiler uses set/reset inferencing on all symbols (not just the listed symbols), and this warning informs you of that fact.

WHAT NEXT

This warning is for your information and requires no action on your part.

elaborate (2).

ELAB-277 (warning) %s More than one multibit pragma specified for symbol '%s'; using '%s'.

DESCRIPTION

You receive this warning message from the **elaborate** or **read** command if there are two multibit pragmas on one variable. The message informs you about which pragma is being used.

WHAT NEXT

Remove the pragma you do not want to use, and reexecute the command.

SEE ALSO

elaborate (2), **read** (2).

ELAB-278 (warning) %s The pragma '%s' for object '%s' will be ignored because the object could not be found.

DESCRIPTION

You receive this warning because you tried to place a pragma on an object that does not exist.

WHAT NEXT

Inspect your design and make sure it is correct and that there are no errors in the spelling of objects and other components.

ELAB-280 (warning) %s Signal on port %d renamed from ’%s’ to ’%s’ in ’%s’.

DESCRIPTION

You receive this warning when the name of a signal on a port, such as on the second port in the following example,

```
  module test(x, \x[0] );
     input [0:0] x;
output \x[0] ;
assign \x[0] = x[0];
  endmodule
```

is different in the output netlist than it would usually be, because of a name conflict, such as a conflict with the name of a component of a bus.

In this example, the output signal on the second port will be renamed from "x[0]" to "x[0]1".

ELAB-281 (error) %s Default branch isn’t the last branch in the case statement.

DESCRIPTION

You receive this error message because you have specified a default branch that is not the last branch in the *case* statement, which is must be.

WHAT NEXT

Review your design and make sure the default branch you specify is the last branch in the *case* statement.

ELAB-282 (warning) %s Parameter range specification is only meaningful to synthesis, not simulation, which might result in

different behavior.

DESCRIPTION

Providing a range (size) for a parameter is only used during synthesis. You might see different behavior between synthesis and simulation if you have explicitly sized parameters.

WHAT NEXT

Review your design description and make appropriate changes.

SEE ALSO

elaborate (2).

ELAB-283 (warning) %s Function '%s' is mapped to module '%s' but body is not empty and will be ignored.

DESCRIPTION

You receive this warning because you specified a function whose body contains code. When you use the *map_to_module* pragma, because calls to that function are mapped to the specified module, the body of the function is not used. This warning lets you know that your design has such a function and its body contains code and will be ignored.

WHAT NEXT

This warning is informational only and requires no action on your part.

SEE ALSO

elaborate (2).

ELAB-284 (error) %s Return port name '%s' conflicts with names of function input parameters.

DESCRIPTION

You receive this error message because a function description in your design

contains an output port that has the same name as one of the input ports, an invalid condition. This occurred in connection with your use of the *map_to_module* or *map_to_operator* pragmas. Following is an example of a description that would elicit this error message. The **return_port_name** is specified as **o** and so is one of the input ports.

```
function f;
          // synopsys map_to_module ADDER
          // synopsys return_port_name "o"
input o;
input p;
endfunction
```

WHAT NEXT

Change the name of the port whose name duplicates the name of another port. Then invoke the command again.

ELAB-285 (error) %s Conversion function on formal port is not supported.

DESCRIPTION

You receive this error message because conversion function is called with formal port as argument while port mapping, which is not supported.

```
    begin
        U1 : TEST_E
    port map ( Cone(A) => Ctwo(TA), Z => TZ );
```

WHAT NEXT

Remove the conversion functions on port formals and try again

ELAB-286 (error) %s Type conversion on formal port is not supported.

DESCRIPTION

You receive this error message because port formals have Type conversion on them, while port mapping which is not supported by Presto.

WHAT NEXT

Remove the type conversion on formal port and try again.

ELAB-287 (error) %s Incorrect specification of port formals.

DESCRIPTION

You receive this error message because a syntax error is detected on port formals during port mapping.

WHAT NEXT

Please check the correct syntax of specifying port formals during port mapping and try again.

ELAB-288 (error) %s synthesis_on and synthesis_off directives are not used in pair within current design unit.

DESCRIPTION

You receive this error message because either synthesis_on or synthesis_off is missed within current design unit.

WHAT NEXT

Please follow the error message to complete the synthesis_off/on pair and try again.

ELAB-289 (error) %s A synthesis_off or translate_off object has been used in an expression.

DESCRIPTION

You receive this error message because a synthesis_off or translate_off object has been used in an expression.

WHAT NEXT

Please follow the error message to check if the synthesis_off/on translate_on/off pragma has been put at a wrong place.

ELAB-290 (error) %s The synthesis_on/synthesis_off or translate_on/translate_off attribute is inconsistent on arg #%d.

DESCRIPTION

You receive this warning message because the synthesis_on/synthesis_off or translate_on/translate_off is inconsistent between the formal and actual argument.

WHAT NEXT

Please follow the warning message to check if the synthesis_off/on translate_on/off pragma is put at a wrong place or is missing.

ELAB-292 (warning) %s '%s' is being read, but does not appear in the sensitivity list of the block.

DESCRIPTION

You receive this warning message if not all the signals that are read appear in the sensitivity list of the block. This may result in simulation-synthesis mismatches.

Consider the following example:

For Verilog:

```
always @(in1)
   myout = in1 | in2 ;
```

For VHDL:

```
entity e is
   port(in1, in2: in bit; myout: out bit);
end;

architecture a of e is
begin
   process(in1) begin
      myout <= in1 or in2;
   end process;
end;
```

This example will result in an OR gate whose inputs are *in1* and *in2*, and whose output is *myout*. The output of the OR gate will potentially change whenever *in1* or *in2* changes. However, in simulations of the original description, *myout* will change only when *in1* changes, because *in1* is the only signal to appear in the sensitivity list of the block.

WHAT NEXT

Add the signal specified in the warning to the sensitivity list of the block.

SEE ALSO

elaborate (2), **read** (2).

ELAB-293 (warning) %s Variable %s is read before being assigned; the synthesized result may not match simulations.

DESCRIPTION

You receive this warning message because a variable that is local to a function or task was read before being assigned. When the **hdlin_infer_function_local_latches** variable is set to **false**, the Presto HDL Compiler does not preserve variable values across separate calls to a task or function, unlike a simulator. Any bits of the variable that are not assigned before being used are given the value 0. No latches are inferred for variables local to a subprogram.

When the **hdlin_infer_function_local_latches** variable is set to **true**, the compiler matches the simulator's behavior. This may result in additional latches in your design.

WHAT NEXT

If you intended to use a value set during a previous call, set **hdlin_infer_function_local_latches** to **true** in order to preserve the value across calls.

If you did not intend to use a value across calls, check your design to verify that you assigned all local variables before using them.

SEE ALSO

elaborate(2)
read(2)

ELAB-294 (warning) %s Floating pin '%s' connected to ground.

DESCRIPTION

You receive this warning message when a previously unconnected pin has been connected to ground. This message reminds you to check whether the behavior resulting from connecting the pin to ground conforms to your expectations.

WHAT NEXT

Verify that connecting the specified pin to ground results in the desired behavior.

SEE ALSO

elaborate (2), **read** (2).

ELAB-295 (error) %s Number of actual arguments in task or function call does not match the number of formals.

DESCRIPTION

You receive this error message because the number of actual arguments in a function or task call does not match the number of formal arguments expected by the corresponding function or task.

WHAT NEXT

Identify the offending parameters and add or remove them accordingly. See the function or task definition to determine which parameters are required.

SEE ALSO

elaborate (2), **read** (2).

ELAB-296 (error) %s Index bounds '%s' for vector '%s' are wrong.

DESCRIPTION

You receive this error message because the bounds of a vector declaration are not an integer type or sized parameter value is overflow. The following example shows the compiler attempting to use a real number as a vector bound.

```
...
reg [3.0:0] x;      // error: "3.0" is not a valid array bound
...
```

The following example shows the compiler attempting to override sized parameter, the new value is overflow for the given size.

```
module test (a, b, c);
parameter WIDTH = 8;
```

```
input [WIDTH-1:0] a, b;
output [WIDTH-1:0] c;
bottom  #(.W(WIDTH)) U1 (a, b ,c ); // W has 3 bits, but 8 need 4 bits.
endmodule

module bottom (a, b, c);
parameter [2:0] W = 4;
input [W-1:0] a, b;
output [W-1: 0] c;
assign c = a + b;
endmodule
```

WHAT NEXT

Modify each part select so that it uses only integer bounds. In the example, you would replace "3.0" with "3". Modify sized parameter definiton or new parameter value.

SEE ALSO

elaborate (2), **read** (2).

ELAB-297 (error) %s '%s' is a task and not a function.

DESCRIPTION

You receive this error message because a function call is attempting to enable a task. A function call can only enable functions. The symbol a function call refers to must be defined by a function declaration.

A function returns a value; thus, a function call must be used as an expression.

WHAT NEXT

Check that you did not attempt to enable a task. If you did not, either change the function call to a task, or rewrite the task to a function.

SEE ALSO

elaborate (2), **read(2).**

ELAB-298 (error) %s Array index out of bounds %s.

DESCRIPTION

You receive this error message because the index used to access the array is not within the range of valid indices defined by the array declaration.

In the following example, the valid array indices must be in the range 0:1 because of the way the array is declared. Attempting to access location 2 outside the valid range, as in the following example, results in this error.

```
reg [1:0] a;
...
a[2] = 1'b1;        // error: index out of bounds
```

WHAT NEXT

Modify the array index so that it is within the valid index range given by the array declaration.

SEE ALSO

elaborate (2), **read** (2).

ELAB-299 (error) %s Array index out of bounds %s.

DESCRIPTION

You receive this error message because the index used to access the array is not within the range of valid indices defined by the array declaration. In the following example, the array index must be within the range 0:1 because of the way the array is declared. Attempting to access location 2, which is outside the valid range, results in this error message.

```
reg [1:0] a;
...
x = a[2];        // error: index out of bounds
```

WHAT NEXT

Modify the array index so that it is within the valid index range given by the array declaration.

SEE ALSO

elaborate (2), **read** (2).

ELAB-300 (error) %s Cannot test variable '%s' because it was not in the event expression or with wrong polarity.

DESCRIPTION

You receive this error message when the outermost if statement in the always block tests some other variable that does not appear in a *posedge* or *negedge* expression or with wrong polarity. When an always block's sensitivity list contains more than one *posedge* or *negedge* expression, the Presto HDL Compiler assumes that one expression represents the clock, and any remaining expressions represent asynchronous sets or resets. For each set or reset condition, the always block should contain an if statement that tests it.

WHAT NEXT

Modify your rtl to meet the above requirements. See the *HDL Compiler for Verilog Reference Manual* or the *VHDL Compiler Reference Manual* for information on how the compiler infers flip-flops.

SEE ALSO

elaborate (2), **read** (2).

ELAB-301 (warning) %s Only constant-valued subscripts are checked in the sensitivity list; other subscripted expressions are ignored.

DESCRIPTION

You receive this warning message because Presto HDL Compiler does not perform sensitivity list checking on variable subscripts.

Sensitivity list checking verifies that all signals read by a combinational always block are in its sensitivity list.

WHAT NEXT

Remove the variable subscript from the sensitivity list.

SEE ALSO

elaborate (2), **read** (2).

ELAB-302 (error) %s The statements in this ’always’ block are outside the scope of the synthesis policy. Only an ’if’ statement is allowed at the top level in this always block.

DESCRIPTION

You receive this error message when the statement at the top level of the always block is not an if statement.

WHAT NEXT

See the *HDL Compiler for Verilog Reference Manual* and the *VHDL Compiler Reference Manual* for ways to infer flip-flops and latches from always blocks with an if statement.

SEE ALSO

elaborate (2), **read** (2).

ELAB-303 (error) %s The expression in the reset condition of the ’if’ statement in this ’always’ block can only be a simple identifier or its negation.

DESCRIPTION

You receive this error message when the reset condition of the *if* statement is not a simple identifier or a negation of the simple identifier. Presto HDL Compiler only supports an identifier or its negation as the reset condition.

WHAT NEXT

Modify the reset condition so that it is either a simple identifier or a negation of the simple identifier. The following example shows how to modify the RTL code.

Original RTL code:

```
if (~reset || jt_cbits[6]) ec_mode <= 1’b0;
else ec_mode <= 1’b1;
```

Modified RTL code:

```
if (~reset) ec_mode <= 1’b0;
else if (jt_cbits[6]) ec_mode <= 1’b0;
else ec_mode <= 1’b1;
```

SEE ALSO

elaborate (2), **read** (2).

ELAB-304 (warning) %s Case- or If-statement or ?: operator has an infer_mux attribute and a default branch or incomplete mapping. This can cause nonoptimal logic if a mux is inferred. %s.

DESCRIPTION

This warning message may be displayed when mux inference has been requested for a case statement, if statement or ?: operator.

You receive this warning when a case statement does not have all the values of the case variable explicitly enumerated. Instead, a default branch is used (explicitly or implicitly) to represent a lot of them together as in the following example.

```
case(c) // synopsys infer_mux
  2'b00: out = in1 ;
  2'b01: out = in2;
  default: out = in2;
endcase
```

A MUX_OP is not the optimal hardware for this representation. You will not receive this warning if you delete the default branch and explicity add labels for 2'b10 and 2'b11.

You also receive this warning when an if statement has a final else branch or the control variable is not compared against all possible values, as in the following example:

```
if (sel == 2'b00) // synopsys infer_mux
  dout <= a;
else if (sel == 2'b01)
  dout <= b;
else
  dout <= in2;
```

You will not receive this warning if you change this code by:

```
if (sel == 2'b00) // synopsys infer_mux
  dout <= a;
else if (sel == 2'b01)
  dout <= b;
else if (sel == 2'b10)
  dout <= in2;
else if (sel == 2'b11)
  dout <= in2;
```

For the ?: operator, in the current version you will always receive this warning. Change this operator by a case statement to avoid the warning message.

Finally, you may receive many ELAB-304 warning messages when you set the variable hdlin_infer_mux to all because this is equivalent to use the infer_mux pragma or attribute in any case, if or ?:.

WHAT NEXT

To avoid this warning message, remove the infer_mux pragma or recode by a case or if statement where all possible values are enumerated.

SEE ALSO

elaborate (2), **read** (2). **hdlin_infer_mux** (3).

ELAB-305 (error) %s Clock %s used as data.

DESCRIPTION

You receive this error message because Presto HDL Compiler does not allow clock signals to be used for purposes other than clocking.

WHAT NEXT

Remove the unsupported code from your design.

SEE ALSO

elaborate (2), **read** (2).

ELAB-306 (error) %s Illegal use of tristate value.

DESCRIPTION

You receive this error message when a tristate value is used in an expression in a way that Presto does not support, as in the following example.

```
out = in & 1'bz
```

This error is also issued when a variable assigned to a tristate value is used in an expression, as in the following example.

```
if(c) tmp = 1'bz;
else tmp = in1 ;
```

```
out = tmp & in2
```

WHAT NEXT

Remove the unsupported portion of code.

SEE ALSO

elaborate (2), **read** (2).

ELAB-307 (error) %s Case labels are not parallel in %s at line %d. A MUX_OP cannot be inferred.

DESCRIPTION

You receive this error message because Presto HDL Compiler does not infer a MUX_OP for the case statements that are not parallel. A case is parallel when all its branches are mutually exclusive.

WHAT NEXT

Remove the "infer_mux" pragma from this case statement, or if the branches really will be mutually exclusive, prepend a "unique" qualifier to the case statement in SystemVerilog or add a "parallel_case" pragma in traditional Verilog.

SEE ALSO

elaborate (2), **read** (2).

ELAB-308 (warning) %s Mismatch between simulation and synthesis may occur due to three-state value.

DESCRIPTION

You receive this warning message when the design contains a variable that is conditionally assigned to a three-state value, and the variable is read in the same always block in which it is conditionally assigned. Reading such a variable in the HDL source code generates logic that uses the output of a three-state buffer, which may cause a mismatch between simulations and synthesis.

In the following example, *tmp* is assigned to a three-state value and assigned to out when both *c* and *in1* are false.

```
if(c)
   tmp = 1'bz ;
else if (in1)
   tmp = in2 ;

out = tmp ;
```

WHAT NEXT

Modify the code so that the design does not read a variable that is not conditionally assigned to *z*.

SEE ALSO

elaborate (2), **read** (2).

ELAB-309 (warning) %s Cannot infer a MUX_OP in %s at line %d.

DESCRIPTION

You receive this warning message if a MUX_OP cannot be inferred for an if or case statement because one or more of the following requirements were not met:

• Because variable hdlin_infer_mux was set to "none" .

• For the case statement, all case labels must be constants.

• For the if statement, all control expressions must be simple comparisons that are constants compared with a common variable.

• The number of case labels must be greater than or equal to the value of the **hdlin_mux_size_min** variable.

• The number of case labels must be less than or equal to the value of the **hdlin_mux_size_limit** variable.

• The ratio of case label number to branch number must be less than or equal to the value of the **hdlin_mux_oversize_ratio** variable.

WHAT NEXT

Modify the if or case statement so that it meets the above requirements.

elaborate (2), **read** (2); **hdlin_mux_oversize_ratio** (3), **hdlin_mux_size_limit** (3), **hdlin_mux_size_min** (3).

ELAB-310 (warning) %s Comparison against '?', 'x', or 'z' values is always false. It may cause simulation/synthesis mismatch.

DESCRIPTION

You receive this warning when any operand in a comparison expression has *xfp or z* values. The result of such expressions are always determined to be false, and the corresponding branch is never executed.

In the following example, 'then-branch' of the if-conditional is never executed.

```
if(2'b0x) begin
   out = in1;       /* Will never fire */
end
else begin
   out = in2;       /* Will always fire */
end
```

In the following example, the case branch condition that contains *x* or *z* values are never reached.

```
case(c)
  1'bx : out = in1 ;  /* Will never fire */
  1'b0 : out = in2 ;
endcase
```

WHAT NEXT

Rewrite the design to eliminate the occurance of *x* or *z* from conditional expressions, or convert the case into a casex or casez statement.

SEE ALSO

elaborate (2), **read** (2).

ELAB-311 (warning) %s DEFAULT branch of CASE statement

cannot be reached.

DESCRIPTION

You receive this warning message when you execute the **read** or **elaborate** command and your design contains a case statement in which the default branch can never be executed. This warning is issued when the compiler detects that at least one of the other branches will always be executed.

```
case(c)
  1'b1 : out = in1 ;
  1'b0 : out = in2 ;
  default: out = in2 ;
endcase
```

WHAT NEXT

Verify that your case statement is written as you intended. If so, delete the default branch.

SEE ALSO

elaborate (2), **read** (2).

ELAB-312 (warning) %s Out of bounds bit select replaced with X.

DESCRIPTION

You receive this warning message when you apply a subscript to a bit vector, and the bit vector attempts to access a bit that is out of range of the vector.

WHAT NEXT

Modify the subscript so that it attempts to access a bit that is within range of the vector.

SEE ALSO

elaborate (2), **read** (2).

ELAB-313 (error) %s Repetition multiplier in a concatenation is not constant expression.

DESCRIPTION

You receive this error message because you have specified a repetition multiplier in a concatenation that is not a constant expression, which is not allowed. The repetition multiplier in a concatenation must be a constant. For example, {i{x}} is not allowed if *i* is a varying expression.

WHAT NEXT

Review your design and make appropriate corrections.

SEE ALSO

elaborate (2).

ELAB-314 (warning) %s Case branch %s is unreachable.

DESCRIPTION

You receive this warning message when one or more branches in a case statement are unreachable due to stronger branch conditions in earlier branches.

For example, in the following Verilog code the first branch of the case statement is always taken. As a result, all subsequent case branches are unreachable.

```
module m (a, b, y);
 input a, b;
 output reg y;

 reg t0, t1;

 always begin
  case (1'b1)
    1'b1: y = a;
    b: y = ~a;
    default: y = b;
  endcase
 end

endmodule // m
```

WHAT NEXT

Dead case branches might indicate a design error. Examine the case statement and verify that the unreachable branches are intentional.

SEE ALSO

elaborate(2)
read(2)

ELAB-315 (error) %s A statement in your design description tried to read a three-state value.

DESCRIPTION

You receive this error message because a statement in your source code tried unsuccessfully to read a **Z** value. Synthesis does not support **Z** values.

WHAT NEXT

Rewrite your description to change or eliminate the value or values in question.

ELAB-316 (error) %s A statement in your design description tried to read an 'x', '?', or three-state value.

DESCRIPTION

You receive this error message because a statement in your source code tried unsuccessfully to read an **x**, **?**, or **Z** value. Synthesis does not support these values.

WHAT NEXT

Rewrite your description to change or eliminate the value or values in question.

ELAB-317 (error) %s A statement in your design description tried to read an 'x', '?', or three-state value in a case expression.

DESCRIPTION

You receive this error message because a statement in your source code tried

unsuccessfully to read an **x**, **?**, or **Z** value in a case expression. Synthesis does not support these values in a case expression.

WHAT NEXT

Rewrite your description to change or eliminate the value or values in question.

ELAB-318 (error) %s Unable to read from modfile %s: %s

DESCRIPTION

You receive this error message because your intermediate file could not be read, a situation that might be caused by restricted directory permission or by disk corruption.

WHAT NEXT

Change the directory permission to allow access. Then invoke the **analyze** command again to analyze the corrupted module file and attain a modfile that is not corrupted.

SEE ALSO

analyze (2), **elaborate** (2).

ELAB-319 (information) %s Reading module %s from file %s.

DESCRIPTION

Reading module from the corresponding .pvl file.

WHAT NEXT

No action is necessary.

SEE ALSO

elaborate (2), **read** (2).

ELAB-320 (warning) %s File %s for module %s cannot be

found.

DESCRIPTION

You receive this warning message because the corresponding intermediate files, such as .pvl, .syn, and etc for the module could not be found.

WHAT NEXT

Reanalyze the module.

ELAB-321 (error) %s Number of ports on reference design '%s' is inconsistent with specified instance '%s'.

DESCRIPTION

You receive this error message because the number of ports on reference design is inconsistent with specified instance.

WHAT NEXT

Rewrite your description to make the number of ports on reference design is consistent with specified instance.

ELAB-322 (error) %s Width of port '%s' on reference design '%s' is inconsistent with specified instance '%s'.

DESCRIPTION

You receive this error message because the width of port on reference design is inconsistent with specified instance.

WHAT NEXT

Rewrite your description to make the width of port on reference design is consistent with specified instance.

ELAB-323 (error) %s Too many ports found on gate

instantiation

DESCRIPTION

Too many ports found on gate instantiation

WHAT NEXT

Check that the correct number of ports has been specified on the gate instantiation.

SEE ALSO

elaborate (2), **read** (2).

ELAB-324 (error) %s Too many ports passed to instance %s

DESCRIPTION

Too many ports passed to instance

WHAT NEXT

Check that the correct number of ports has been passed to the instance listed above.

SEE ALSO

elaborate (2), **read** (2).

ELAB-325 (error) %s Unknown port %s in instance %s in module %s

DESCRIPTION

Unknown port in instance in module

WHAT NEXT

Check that the offending port listed above has been specified correctly.

SEE ALSO

elaborate (2), **read** (2).

ELAB-326 (error) %s module data file %s revision mismatch: Expected %d, got %d

DESCRIPTION

module data file revision mismatch.

WHAT NEXT

analyze the rtl file again using new version.

ELAB-327 (error) %s Cannot resolve pin %s on cell %s:%s.

DESCRIPTION

Cannot resolve pin on cell.

WHAT NEXT

modify rtl source to make sure the module instanitation agree with submodule declaration.

ELAB-328 (error) %s Replication constant contains ’x’ or ’z’.

DESCRIPTION

The repeat count of this replication operator is a constant expression that contains ’x’ or ’z’. It is unusable for elaborate-time replication of the data or assignment pattern. The following example will trigger this error:

```
x = { 3’bx11 { y } };
```

WHAT NEXT

Replace the replication constant by a constant expression resolvable to 0s and 1s. Or, if this constant was meant to produce ’x’ or ’z’ data values in the result, insert a comma after the constant so that it parses as a list element and not as a

replication operator.

SEE ALSO

elaborate (2), **read** (2).

ELAB-329 (warning) %s A ’disable’ statement for block ’%s’ appears outside the block and is being ignored.

DESCRIPTION

You receive this warning message because a disable statement appears outside of the block it attempts to disable, as in the following example:

```
   always begin
      begin : block_a
 y = 1'b1;
      end
      disable block_a;
   end
```

A disable statement must appear with the block to be disabled; otherwise, the disable statement has no effect and is ignored.

WHAT NEXT

Examine your code to verify the block you want to disable, and revise the code so that the disable statement appears inside the block to be disabled.

SEE ALSO

elaborate (2), **read** (2).

ELAB-330 (error) %s Attempt to disable block ’%s’ out of function scope is not supported.

DESCRIPTION

You receive this error message when a disable statement inside a function refers to a block that is either outside the function or that does not contain the disable statement. The Presto HDL Compiler for Verilog supports only disable statements that refer to a block inside the current function.

WHAT NEXT

Change the design so that all disable statements are within the block they disable, and that all disable statements refer to blocks within the same function or task.

SEE ALSO

elaborate (2), **read** (2).

ELAB-331 (error) %s Attempt to disable block '%s' out of task scope is not supported.

DESCRIPTION

You receive this error message when a disable statement inside a task refers to a block that is either outside the task or that does not contain the disable statement. The Presto HDL Compiler of Verilog supports only disable statements that refer to a block inside the current task.

WHAT NEXT

Change the design so that all disable statements are within the block they disable, and that all disable statements refer to blocks within the same function or task.

SEE ALSO

elaborate (2), **read** (2).

ELAB-332 (warning) %s Concatenations cannot have unsized numbers; assuming 32 bits.

DESCRIPTION

You receive this warning message when a concatenation contains an unsized constant. The compiler cannot calculate the correct size of the concatentation. The size is assumed to be 32 bits.

This construction is disallowed by the IEEE Verilog standard, but is permitted by the compiler for backward compatibility.

The following two concatenations will trigger this warning:

```
x = { 0, a };
z = { b, 'hf, c };
```

WHAT NEXT

Avoid this style. Use an explicit size on all constants within concatenations.

SEE ALSO

elaborate (2), **read** (2).

ELAB-333 (warning) %s This SV Assertion is ignored for synthesis since %s is not set to true.

DESCRIPTION

This warning message issues when the Presto HDL Compiler finds a labelled assertion or assertion severity system task call whose usage is not confirmed by the tcl environment variable setting cited in the message. Because SystemVerilog Assertions (SVA) can lead synthesis to using a larger set of "don’t care" conditions during optimization, you must separately certify that these assertions have proven to be unreachable prior to synthesizing this RTL.

WHAT NEXT

This is only a warning message. No action is required.

However, if you do not want the construct to be ignored, you must set hdlin_enable_assertions to true and also set an element of the confirmed_SVA environment array to true whose element name identifies the label and lexical scope of the applicable assertion. The most specific form of its element name is used in the warning message when hdlin_enable_assertions is already true.

The recommended way to confirm assertions is to assemble a separate tcl file to source into your dc_shell before elaborating the design elements which use SVA. This same file should then be sourced into fm_shell when formally verifying the results of this elaboration.

SEE ALSO

analyze(2)
elaborate(2)
confirmed_SVA(3)
hdlin_enable_assertions(3)

ELAB-334 (error) %s Part-select direction does not match declared direction of symbol ’%s’ (declared [%d:%d], part-select

is [%d:%d]).

DESCRIPTION

You receive this error message when a part-select statement on a variable conflicts with the variable's declaration. If the variable is declared with the left bound greater than the right bound, then the part-select must also use a left bound greater than a right bound, and vice versa.

For example, the following code will trigger this error because the part-select 'x[1:2]' does not match the declared direction of 'x'.

```
    module test(x, y);
input  [2:0] x;
output [1:0] y;

    assign y = x[1:2];

    endmodule
```

WHAT NEXT

Correct the part-select statement so that the bounds are compatible with the variable's declaration.

SEE ALSO

elaborate (2), **read** (2).

ELAB-335 (warning) %s 'Case' statement is full and has only one nontrivial branch; it will be inlined.

DESCRIPTION

You receive this warning message because a case statement in the design either is marked as a full case by the user, or is proved to be a full case by the compiler, and has only one useful branch. Because in a the full case, at least one branch must execute, the single branch of the case statement will always be executed. The compiler has detected this situation and will skip generating logic to test the case condition, executing the code in the body as if it were not surrounded by the case statement.

Most commonly, this message arises when case statements have one normal branch, and a default branch that only assigns variables to 'bx. For example:

```
    module test(a,y);

       input  a;
       output y;
       reg  y;

       always
  case (a)
    1'b1: y = 1'b1;
            default: y = 1'bx;
  endcase
    endmodule
```

In this case, the presence of the default branch means that the case statement is full (that is, one branch will always be taken.) Then, Because the default branch only assigns variables to 1'bx, it can be optimized away, and the resulting single-branch case can be simplified to unconditionally assign y = 1'b1.

In the next example, the // synopsys full_case directive tells the compiler that all possible values of *x* are handled in the case statement. However, there is only one branch. The compiler concludes that *a* must always be 1. Thus, the branch will always be executed.

```
    module test(a,y);

       input  a;
       output y;
       reg  y;

       always
  case (a) // synopsys full_case
    1'b1: y = 1'b1;
  endcase
    endmodule
```

This second example is an uncommon coding style. The compiler issues this warning to remind you to verify that the case statement is as you intended it.

WHAT NEXT

Verify that the case statement implements the behavior you intended.

SEE ALSO

elaborate (2), **read** (2).

ELAB-336 (error) %s Presto does not support processes with

multiple event statements.

DESCRIPTION

You receive this error message because Presto Compiler does not support multiple event statements in the same process.

WHAT NEXT

Change the source code to remove the use of multiple event in the same process.

SEE ALSO

elaborate (2), **read** (2).

ELAB-337 (warning) %s Assignment to supply0/1 variable '%s' is ignored.

DESCRIPTION

You receive this warning message if you attempt to make an assignment to a variable declared as 'supply0' or 'supply1'. These variables always have values of 0 and 1, respectively; any assignments you attempt are ignored.

WHAT NEXT

Remove the specified assignment, then reexecute the command.

SEE ALSO

elaborate (2), **read** (2).

ELAB-338 (warning) %s Module '%s' contains a supply%d variable '%s'. Replacing with wire driven by a continuous assignment to %d.

DESCRIPTION

You receive this warning message when a supply0 or supply1 variable appears in your design.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

elaborate (2), **read** (2).

ELAB-339 (warning) %s Symbol '%s', declared as an enum, may be assigned non-enum values.

DESCRIPTION

A variable declared using the 'synopsys enum' pragma may be assigned to a value that is not a member of the enum. An enumerated type declaration represents an assertion by the user that a variable can only be assigned a certain set of values; if the design assigns a value that is not part of the user-declared enum, results may be unpredictable.

The compiler is not always able to determine conclusively when an expression will evaluate to a value listed in the enum. For example, the compiler cannot determine the possible values of input ports. Another case occurs when a symbol declared as an enum is assigned the result of an arithmetic or logical expression that cannot be evaluated to a constant at compile time.

In the following example, the expression 'current_state + 2'b01' will trigger this error. By examining the code, you can determine that the expression evaluates to a value that is contained in the enumerated type, except when 'current_state' is equal to 'last_state'. Since it is only executed when 'current_state' is not 'last_state', it would be safe to leave this code as is.

```
    module test (clock);

      input clock;

      parameter [1:0] /* synopsys enum states */ first_state = 2'b00,
second_state = 2'b01, last_state = 2'b10;

      reg [1:0] /* synopsys enum states */ current_state, next_state;

      always @(posedge clock) begin
 if (current_state == last_state)
   next_state = first_state;
 else
   next_state = current_state + 2'b01;
      end
    endmodule
```

However, if the 'always' block were replaced with:

```
    assign next_state = current_state + 2'b01;  // result is 2'b11 when
                                                // current_state == last_state
```

then 'next_state' could be assigned 2'b11. This contradicts the user-declared enum, and could have unpredictable results and cause simulation/synthesis mismatches.

WHAT NEXT

If you receive this warning, make certain that the symbol is ONLY assigned a values that are listed in the enumerated type declaration.

If the variable is assigned to the value of an input port, make sure that the port will only be assigned to values within the enum. If that is the case, declare the port as a member of the same enumerated type using the 'synopsys enum' pragma.

If the variable is assigned to an expression result, make sure that expression can never evaluate to a non-enum value.

If you cannot determine that the value assigned will be a member of the declared enumerated type, you must remove the enum declaration from the variable.

ELAB-340 (warning) %s Enumerated type '%s' is not compatible with type of symbol '%s'.

DESCRIPTION

You receive this error message because the specified enumerated type is not compatible with the specified symbol type. This error occurs at elaboration when parameters in the size specifications are resolved.

In the following example, the variable **current_state** has bounds of [0:SIZE], which resolves to [0:3], but the enumerated type states has bounds of [0:SIZE2], which resolves to [0:2].

```
parameter SIZE = 3;
parameter SIZE2 = 2;

parameter [0:SIZE] /* synopsys enum states */ state1 = 4'd0, state2 = 4'd1;
reg [0:SIZE2] /* synopsys enum states */ current_state;
```

WHAT NEXT

If it is a typo, modify the design so that the symbol and the enumerated type share the same type.

If user intends to let the symbol and the enumerated type have different type, the user have to make sure that the synthesis behavior is what the user wants.

SEE ALSO

elaborate (2), **read** (2).

ELAB-341 (error) %s The number of enum encodings given does not match the number of literals.

DESCRIPTION

You receive this error message when, in an enumerated type declaration, there is a different number of literals and encodings.

WHAT NEXT

Fix the design so that the number of encodings and literals is the same.

SEE ALSO

elaborate (2), **read** (2).

ELAB-342 (error) %s Expression involving %s operator cannot have a real operand.

DESCRIPTION

You receive this error message because the specified operator does not support real operands. Real operands are not supported for synthesis.

WHAT NEXT

If your design is intended for synthesis only, remove real operands from the design.

SEE ALSO

elaborate (2), **read** (2).

ELAB-343 (error) %s Source file for '%s' was not analyzed by

this release of the compiler; re-analyze it.

DESCRIPTION

Your **read, analyze,** or **elaborate** command requires data about the specified entity, module, or package that was stored by a previous **analyze** command. A file of such data was found, but it had been produced by an incompatible version of the Presto HDL compiler. The file cannot be read in its current version.

WHAT NEXT

Reanalyze all design source files needed for this compilation using **this release** of Design Compiler - on any platform. Or adjust your working directory settings to use the environment that contains the properly analyzed sources.

When the analyzed data files are in synch with the compiler release you are using, reexecute the failed command.

SEE ALSO

analyze (2), **elaborate** (2), **read** (2).

ELAB-344 (error) %s File '%s' does not contain an analyzed design.

DESCRIPTION

You receive this error message when you execute the **read** or **elaborate** command and specify a file that does not contain an analyzed design. The compiler was expecting a file that is an analyzed design. The Presto HDL Compiler stores pre-analyzed designs in disk files.

WHAT NEXT

Re-analyze the module or entity you are elaborating or reading and specify a file that contains an analyzed design.

SEE ALSO

elaborate (2), **read** (2).

ELAB-345 (error) %s Symbol '%s' is a function that is being

called as a task.

DESCRIPTION

You receive this error message when a function in your design is being called as a task. A task call is a stand-alone statement, whereas a function call generates a value.

WHAT NEXT

Modify the design so that the function is called only in places where an expression is expected.

SEE ALSO

elaborate (2), **read** (2).

ELAB-346 (error) %s Variable ’%s’ must be non-negative.

DESCRIPTION

You receive this error message when a variable that controls the Presto HDL Compiler has a negative value. Only non-negative values are supported.

WHAT NEXT

Identify the variable that has a negative value and change it to a non-negative value. See the manual page of the variable for valid values.

SEE ALSO

elaborate (2), **read** (2).

ELAB-347 (warning) %s Division by 0 evaluates to ’x’.

DESCRIPTION

You receive this warning message because an expression contains a division by 0, which evaluates to ’x’ in Verilog.

WHAT NEXT

Verify that you intended to write an expression with 0 as the divisor.

SEE ALSO

elaborate (2), **read** (2).

ELAB-348 (error) %s Incorrect datatype for variable '%s'.

DESCRIPTION

You receive this error message when a variable that controls the behavior of the Presto HDL Compiler has a value that is the wrong datatype. This occurs when a non-numeric value is assigned to a variable that should contain a string, or when a variable that should be *true* or *false* has a numeric value, or contains another string.

WHAT NEXT

Use the correct datatype in interactive use, and correct any scripts that set the variable. To determine what type of value the variable should have, see the manual page of the appropriate variable.

SEE ALSO

elaborate (2), **read** (2).

ELAB-349 (warning) %s Potential simulation-synthesis mismatch if index exceeds size of array '%s'.

DESCRIPTION

You receive this warning message if the bit-width of the index expression is larger than the bit-width of the array bounds, or if an array has bounds that cannot be expressed as [0 : 2^n-1] or vice versa.

An array in the program is indexed by an expression that can evaluate to an out-of-bounds index, and the compiler cannot determine if the index will evaluate to a legal subscript.

If the index does evaluate to an out-of-bounds value, the synthesized result may not match Verilog simulations. Assigning to, or reading from, an out-of-bounds location may have unpredictable results.

For example, in the following Verilog module, a register is indexed by the input port 'addr'. If 'addr' ever has the value 3'd7, then the register will be accessed out-of-bounds, but the correct logic can be generated.

```
module test(addr, data, write);
  input [2:0] addr;
  input data, write;
  reg [6:0] mem;

always @(addr or data or write)
  if (write)
    mem[addr] = data;

endmodule
```

For example, in the following Verilog module, a register is indexed by the input port 'addr'. If 'addr' ever is more than the value 4'd6, then the register will be accessed out-of-bounds, and the bad logic will be generated. When 'addr' ever has the value 4'd8, it will access mem[0], not mem[8].

```
module test(addr, data, write);
  input [3:0] addr;
  input data, write;
  reg [6:0] mem;

always @(addr or data or write)
  if (write)
    mem[addr] = data;

endmodule
```

WHAT NEXT

Verify that the index expression cannot evaluate to an out-of-bounds value.

SEE ALSO

elaborate (2), **read** (2).

ELAB-350 (error) %s Can't resolve constant expression for symbol '%s'.

DESCRIPTION

In certain circumstances, the Presto HDL compiler may not evaluate constant expressions with operands larger than 32 bits. To work around this problem, pre-compute such expressions in your design, or use HDL Compiler to elaborate that design. This problem will be fixed in an upcoming release.

WHAT NEXT

Either pre-compute the value, or use HDL Compiler on this design.

ELAB-351 (warning) %s Comparison against 'unknown' value is always false; may cause simulation/synthesis mismatch.

DESCRIPTION

You receive this message because the result of a comparison, by definition, can produce only one result. In the following example, the body of the first IF statement always executes, and the body of the second IF statement never executes. All comparisons against the uninitialized value *U* fail because the result of an equality comparison against *U* is always false, and the result of a disequality comparison against *U* is always true.

```
IF(A2 /= "U") THEN
   ONE_2 <= '1';              -- SHOULD ALWAYS FIRE
 END IF;

 IF(A2 = "U") THEN
   ZERO_2 <= '1';             -- SHOULD NEVER FIRE
 END IF;
```

WHAT NEXT

Ensure that you intended to compare against *U*; and, if not, correct the comparison.

ELAB-352 (error) %s Operator '%s' not found in synthetic library.

DESCRIPTION

You receive this message because the operator defined by a *map_to_operator* attribute is not described in any of the synthetic libraries in the **synthetic_library** variable (and is not found in **standard.sldb**).

WHAT NEXT

To use the synthetic library operator, ensure that it can be found in the files defined by the **synthetic_library** variable.

SEE ALSO

synthetic_library (3).

ELAB-353 (error) %s Width of the actual at the port '%s' does not match. %s

DESCRIPTION

You receive this message because a temporary signal/variable does not have a proper bit width.

The following example shows that a *temp_out* signal connected to a *Y* port is too wide or too narrow when represented in hardware.

```
architecture A of E is
component C1
   port (A : integer range 0 to 15;
         Y : integer range 0 to 15);
end component;
signal temp_in : integer range 0 to 15;
signal temp_out : integer range 0 to 31;
begin
U1: C1 port map (A => temp_in, Y => temp_out);
end A;
```

WHAT NEXT

Define a temporary signal/variable with the proper bit width. The following example is a modification of the one above to provide a proper bit width for the *temp_out* signal.

```
architecture A of E is
component C1
   port (A : integer range 0 to 15;
         Y : integer range 0 to 15);
end component;
signal temp_in : integer range 0 to 15;
signal temp_out : integer range 0 to 31;
signal temp : integer range 0 to 15;
begin
temp_out <= temp;
U1: C1 port map (A => temp_in, Y => temp);
end A;
```

ELAB-354 (error) %s Cannot read architecture file %s: %s.

DESCRIPTION

You receive this message because during a read or elaborate command, the Presto HDL compiler cannot open or read a file describing the source language (and, for VHDL, the architecture) of the module or entity being elaborated.

You also receive this message if the module or entity has not yet been analyzed or if the module or entity name is misspelled.

WHAT NEXT

Ensure that the module or entity being elaborated has already been analyzed, and that the entity or module name is correctly specified.

SEE ALSO

elaborate (2), **read** (2).

ELAB-355 (information) %s Elaborating module '%s'.

DESCRIPTION

You automatically receive this message for each module elaborated during a read or elaborate command.

WHAT NEXT

No action is necessary.

SEE ALSO

elaborate (2), **read** (2).

ELAB-356 (error) %s No modules exist in the analyzed file.

DESCRIPTION

You receive this message because the Presto HDL compiler finds no modules or entities in the file being read from the **read** command using a **verilog** or **vhdl** format. The error is reported by the **read** command.

WHAT NEXT

Ensure that the file being read contains at least one module or entity.

SEE ALSO

read (2).

ELAB-357 (error) %s Module '%s' cannot be found for elaboration.

DESCRIPTION

You receive this message because the Presto HDL compiler cannot find the module to be elaborated. The error is reported by the **elaborate** command.

WHAT NEXT

Ensure that the module to be elaborated has been analyzed.

SEE ALSO

elaborate (2), **analyze** (2).

ELAB-358 (error) %s Mismatching number of connections in module/component instantiation.

DESCRIPTION

The number of port connections of the module/component instantiation does not match the number of ports in the module/component declaration. Either you specified too many or not enough connections to the module/component.

WHAT NEXT

Check against the module/component declarations to find out which ports are unconnected or whether you specified too many connections.

SEE ALSO

ELAB-359 (error) %s The procedure/task %s cannot be mapped to %s because it has an inout port (%s).

DESCRIPTION

HDL Compiler issues this error when, during the activity of the **read** command or **elaborate** command, the compiler encounters a procedure or task that has a map-to-entity or map-to-operator or map_to_module directive and also has an inout port or signal port. HDL Compiler does not support inout or signal ports on mapped procedures.

WHAT NEXT

Remove the inout port from the mapped function or procedure, and issue the command again.

SEE ALSO

elaborate (2), **read** (2).

ELAB-360 (error) %s The REAL data type is not supported for synthesis.

DESCRIPTION

HDL Compiler does not support the use of the REAL data type when synthesizing VHDL.

WHAT NEXT

Rewrite your design so that it does not use the REAL data type.

SEE ALSO

elaborate (2), **read** (2).

ELAB-361 (error) %s Unable to open standard synthetic

libraries; check for correct installation.

DESCRIPTION

The Presto HDL Compiler could not open the standard synthetic library file, standard.sldb, or the standard GTECH library, gtech.db. This probably indicates that Design Compiler is not installed correctly.

WHAT NEXT

Verify the successful completion of the the installation of Design Compiler.

SEE ALSO

elaborate (2), **read** (2).

ELAB-362 (error) %s Cannot find port '%s' on synthetic operator '%s'.

DESCRIPTION

The Presto HDL Compiler cannot find a port it expected to find on a synthetic operator. This usually indicates that a function that uses the map-to-operator pragma has incorrect parameter names for the synthetic operator that it is mapped to.

WHAT NEXT

Verify that any functions mapped to synthetic operators use the correct port (parameter) names.

SEE ALSO

elaborate (2), **read** (2).

ELAB-363 (error) %s Incorrect value for hdlin_infer_mux: '%s'; possible values are 'all', 'default', or 'none'.

DESCRIPTION

Allowed values for the **hdlin_infer_mux** variable are *all*, *none*, and *default*. When *all*

is the value, HDL Compiler attempts to infer a MUX_OP for a signal or variable assigned in a case statement. When *none* is the value, HDL Compiler does not attempt to infer any MUX_OPs for a Verilog or VHDL design.

When *default* (the default value) is the value, HDL Compiler attempts to infer a MUX_OP for a signal or variable assigned in a case statement or if statement, if the statement is either marked with the **infer_mux** directive, or is in a process associated with the **infer_mux** attribute or directive. A MUX_OP cannot be inferred if it violates the **hdlin_mux_size_limit** variable.

For details, see the *HDL Compiler for Verilog Reference Manual* or the *VHDL Compiler Reference Manual*.

To determine the current value of this variable, type **list hdlin_infer_mux**. For a list of hdl variables and their current values, type **list -variables hdl**.

WHAT NEXT

Set **hdlin_infer_mux** to one of the values *all*, *default*, or *none*.

SEE ALSO

elaborate (2), **read** (2); **hdlin_infer_mux** (3).

ELAB-364 (warning) %s Replication constant {%d{...}} is non-standard.

DESCRIPTION

The replication factor applied to a Verilog concatenation or a System Verilog assignment pattern must be either positive (Verilog-2001 and earlier) or non-negative (Verilog-2005 and later).

The setting of hdlin_vrlg_std at the time the (System)Verilog source is analyzed determines which definition of the replication operator is provided when elaborating zero replications. When supported as an extension, negative replication constants are also issued this warning; then they are handled using the prevailing definition of zero replication.

Non-standard replications analyzed when hdlin_vrlg_std <= 2001 return 1'b0. This is compatible with an extension made by Synopsys Verilog products of that era. Replications analyzed when hdlin_vrlg_std >= 2005 whose elaboration-time constant is zero or (with this warning) negative cause the repeated expressions to elaborate once (for their side-effects), but not to contribute result values to a surrounding concatenation or assignment pattern. Verilog 2005 permits such empty replication results only within an otherwise non-empty concatenation.

WHAT NEXT

Make sure you intend to use a negative number (or zero) as the repeat count in your concatenation. Check the setting of hdlin_vrlg_std used when the elaborated module was analyzed and align this with your choice for whether 1'b0 or an empty result is intended. If you need more choices of behavior when migrating legacy codes to current standards, contact Synopsys.

SEE ALSO

analyze (2), **elaborate** (2), **read** (2).

ELAB-365 (warning) %s Net '%s' or a directly connected net is driven by more than one process or block.

DESCRIPTION

You receive this warning when a 'reg' variable is driven by more than one always block or a 'wire' variable is driven by more than one continuous assignment and you have also set the variable **hdlin_prohibit_nontri_multiple_drivers** to *false*.

Note: This warning is issued because an invalid design could result.

In simulation, if a 'reg' variable is driven by more than one always block, the definition, in effect, depends on which block executed most recently. In synthesis, since all blocks are concurrently executing at all times, this is not the case, and invalid designs can result if the drivers are simply shorted together. However, when the **hdlin_prohibit_nontri_multiple_drivers** variable is set to *false*, multiple drivers of 'reg' variables are permitted.

A multiple-driven 'wire' variable is prohibited by the Verilog standard. Although some simulators permit this behavior, HDL Compiler issues the ELAB-366 error if it occurs. However, when **hdlin_prohibit_nontri_multiple_drivers** is set to *false*, multiple drivers are permitted. **Note** that this variable setting might cause the generation of invalid designs.

The compiler permits multiple drivers on nets declared as 'tri', although it issues a warning if all the drivers are not three-state devices.

WHAT NEXT

An invalid design might result when this warning is issued. Multiple driver nets are only generated because the **hdlin_prohibit_nontri_multiple_drivers** variable is set to *false*.

Consider modifying your design, to avoid driving a variable from more than one always block or continuous assignment.

SEE ALSO

elaborate (2), **read** (2).

ELAB-366 (error) %s Net '%s' or a directly connected net is driven by more than one source, and not all drivers are three-state.

DESCRIPTION

You receive this error message when a 'reg' variable is driven by more than one always block or a 'wire' variable is driven by more than one continuous assignment or input port and not all of the drivers are three-state.

In simulation, if a 'reg' variable is driven by more than one always block, the definition, in effect, depends on which block executed most recently. In synthesis, since all blocks are concurrently executing at all times, this behavior is not possible, and invalid designs can result if the drivers are simply shorted together. Therefore, HDL Compiler issues an error if any bits of any variable are driven by more than one process.

A multiply-driven net declared as 'wire' is not supported in synthesis and Presto HDL Compiler issues the ELAB-366 error if it occurs. If you want the compiler to permit such behavior, set the **hdlin_prohibit_nontri_multiple_drivers** variable to *false*. **Note** that this variable setting might cause the generation of invalid designs.

The compiler permits multiple drivers on nets declared as 'tri', although it issues a warning if all the drivers are not three-state devices.

COMMON ISSUES

Sharing the same loop index variable between processes is a common source of this error. At the end of each process or always block, the loop index variable is driven by the last value it had during the loop.

```
integer i;
always begin
  if (c)
    for (i = 0; i < N; i = i + 1)
      x[i] = ~x[i];
end
always begin
  if (c)
    for (i = 0; i < N; i = i + 1)
      y[i] = ~y[i];
```

```
  end
```

To avoid this situation, use different variables in the different always blocks or declare the loop index variables locally, as in the following example.

```
always begin: x_block
  integer i;
  if (c)
    for (i = 0; i < N; i = i + 1)
      x[i] = ~x[i];
end
always begin: y_block
  integer i;
  if (c)
    for (i = 0; i < N; i = i + 1)
      y[i] = ~y[i];
end
```

In some cases the compiler can determine that the variable **i** is never read before being assigned in the block, and in those cases the error is not issued.

Previous versions of HDL Compiler treated loop variables as a special case and did not allow them to be read after the loop. However, the Presto HDL Compiler treats loop variables as full-fledged program variables, which can lead to this situation.

WHAT NEXT

Modify your design to avoid driving a variable from more than one always block or continuous assignment. Or if all drivers of the variable are three-state devices, change the declaration of the variable to 'tri', which permits multiple drivers.

Another alternative is to set **hdlin_prohibit_nontri_multiple_drivers** to *false*. **Note** that this setting might allow the generation of invalid designs to be generated. For that reason, it is not recommended.

SEE ALSO

elaborate (2), **read** (2); **hdlin_prohibit_nontri_multiple_drivers** (3).

ELAB-367 (error) %s Clock expression must be one bit wide.

DESCRIPTION

An expression you use as a clock signal must be one bit wide. If you use an expression that is wider than one bit, you receive this error message. In Verilog,

you specify the clock using an event statement, such as "@(posedge clock)". In VHDL, you specify a clock event using "if (clock'event and clock = '1')".

WHAT NEXT

Modify your design so that all clock expressions are one bit wide.

SEE ALSO

elaborate (2), **read** (2); **hdlin_infer_mux** (3).

ELAB-368 (error) %s Net '%s', or a directly connected net, is driven by more than one source, and at least one source is a constant net.

DESCRIPTION

You receive this error when a 'reg' variable is driven by more than one always block, or a 'wire' variable is driven by more than one continuous assignment or input port, and at least one of the drivers is a constant. This is an error because an invalid design results when the output of a gate is connected directly to the Logic0 or Logic1 nets.

In simulation, if a 'reg' variable is driven by more than one always block, the definition, in effect, depends on which of the blocks executed most recently. In synthesis, since all blocks are concurrently executing at all times, this behavior is not possible, and invalid designs can result if the drivers are simply shorted together. Therefore, HDL Compiler issues an error if any bits of any variable are driven by more than one process.

A multiply-driven 'wire' variable is prohibited by the Verilog standard. Although some simulators permit this behavior, HDL Compiler issues the ELAB-366 or ELAB-368 error in this situation. If you wish to permit this behavior, you may set **hdlin_prohibit_nontri_multiple_drivers** to *false*. **Note** that this variable setting may cause the generation of invalid designs.

Ordinarily, multiple drivers are permitted on nets declared as 'tri'; however, constant nets are an exception to this rule because the implementation would result in an invalid design.

COMMON ISSUES

A common source of this error message is sharing the same loop index variable between processes. At the end of each process or always block, the loop index variable is driven by the last value it had during the loop.

```
integer i;
always begin
  if (c)
    for (i = 0; i < N; i = i + 1)
      x[i] = ~x[i];
end
always begin
  if (c)
    for (i = 0; i < N; i = i + 1)
      y[i] = ~y[i];
end
```

To avoid this situation, either use different variables in the different always blocks, or declare the loop index variables locally, as in the following example.

```
always begin
  integer i;
  if (c)
    for (i = 0; i < N; i = i + 1)
      x[i] = ~x[i];
end
always begin
  integer i;
  if (c)
    for (i = 0; i < N; i = i + 1)
      y[i] = ~y[i];
end
```

In some cases the compiler can determine that the variable **i** is never read before being assigned in the block, and in those cases the error is not issued.

Previous versions of HDL Compiler treated loop variables as a special case, and did not allow them to be read after the loop; however, the Presto HDL Compiler treats loop variables as full-fledged program variables, which can lead to this situation.

WHAT NEXT

Modify your design to avoid driving a variable from more than one always block or continuous assignment.

When none of the drivers is a constant net, another alternative is to set **hdlin_prohibit_nontri_multiple_drivers** to *false*. However, when one of the drivers is a constant net, an error is always generated, because the result would be an invalid design.

SEE ALSO

elaborate (2), **read** (2), **hdlin_prohibit_nontri_multiple_drivers** (3).

ELAB-369 (error) %s The width of port %s on instance %s of design %s is inconsistent with other instantiations of the same design.

DESCRIPTION

You receive this error message when a module is instantiated in your design more than once, but the width of the ports is inconsistent among all of the instances.

In the following example, the module named *foo* is instantiated twice, but the ports named *a* and *b* have different widths, causing the error message.

```
module E (a, b, out1, out2);
input [2:0] a;
input [3:0] b;
output [3:0] out1, out2;

foo U1 (a, out1);
foo U2 (b, out2);
endmodule
```

The instance for which this error is reported may not be the actual instance that uses the wrong width. Since the design is not yet linked, the compiler cannot check which of the instances is correct and can only report the inconsistency.

In the example above, the error is reported for instance U2, because instance U1 has already been seen and uses a different width. As the first in the list, the module named *foo* might require a 3-bit port, a 4-bit port, or another size. Errors that affect all instances equally are checked during linking instead of during elaboration.

WHAT NEXT

Correct the width of the ports so that they are consistent, and then invoke the compiler again.

SEE ALSO

elaborate(2)

ELAB-370 (warning) %s No MUX_OP inferred for the case because it might lose the benefit of resource sharing.

DESCRIPTION

You receive this warning message because the compiler did not infer the MUX_OP you specified for the case statement, because the case statement would lose the benefit of resource sharing.

WHAT NEXT

This is a only a warning and requires no action on your part.

ELAB-371 (warning) %s Pragmas has been removed in compiling.

DESCRIPTION

The tool issues this warning when pragmas are removed in the specified location during compilation, usually in rewriting intermediate language code.

For example, when inferring carryin for the following statement, one of the two adders will be removed, along with the label pragma associated with that adder.

```
a = a1 + //synopsys label adder1
    a2 + //synopsys label adder2
    cin;
```

WHAT NEXT

No action is required on your part. However, if you want to avoid the removal of pragmas, change your Verilog code.

SEE ALSO

elaborate (2), **read** (2).

ELAB-372 (warning) %s Unsupported use of user-encoded

enumeration type as array index.

DESCRIPTION

You receive this error message because synthesis does not support user-encoded enumeration types used as an array index. A user-encoded enumeration type is one that has an associated ENUM_ENCODING attribute.

During synthesis, enumeration values are implemented by choosing a binary encoding. VHDL requires that the meaning of an enumeration value used as an index is the position of the enumeration value in the enumeration type definition. Since the encoded value and the position are usually different values, correct synthesis would require the insertion of inefficient decoding logic.

EXAMPLE

The following declaration of A1 is not supported because the index type ENUM1 is an user-encoded enumerated type.

```
  ...
attribute ENUM_ENCODING : string;
attribute ENUM_ENCODING : string;
type ENUM1 is (M1, M2, M3, M4);
attribute ENUM_ENCODING of
    ENUM1 : type is "0010 1000 1001 1111";

type A1 is array (ENUM1 range <>) of BOOLEAN;
  ...
```

WHAT NEXT

Rewrite the source code so that it does not use arrays with user-encoded enumeration types as an index. The tool allows the use of the enumeration type with default encoding as an array index type.

SEE ALSO

elaborate (2), **read** (2).

ELAB-373 (warning) %s Potential overflow which may cause synthesis and simulation mismatch in operator '%s'.

DESCRIPTION

This warning message occurs when the tool detects a potential overflow in an operator (such as exponent or abs) of the expression.

For example, in the following expression if *tmp* is less than zero, there will be an integer overflow.

```
2 ** (31 - tmp)
```

In the following expression, if *tmp* is the minimum integer, there will be an integer overflow.

```
abs(tmp)
```

WHAT NEXT

This is a warning message only. No action is required on your part. However, it is good practice to remove the overflow exponent or abs from the expression.

SEE ALSO

elaborate (2), **read** (2).

ELAB-374 (information) %s Inferred unloaded sequential element for %s.

DESCRIPTION

You receive this message when the Presto HDL Compiler infers a sequential element that is not required for proper functioning of the design being elaborated, but whose inference was requested by the user.

An RTL-level design description in Verilog or VHDL may contain variables that ordinarily would create a sequential cell (either because they are assigned under a clock edge, or because they are conditionally assigned) but whose values are never read, or whose values are not used in computing any output of the design. Because the their values are not used (that is, they have no loads, or no path to the the outputs), by default HDL Compiler (Presto) will not create sequential cells for these variables.

In some circumstances designers wish to retain these sequential cells. Unloaded sequential cells can be inferred by two methods. First, if hdlin_preserve_sequential is TRUE, then a sequential cell will be inferred for any variable that is conditionally assigned or assigned under a clock, regardless of whether its value is used or not. Second, if hdlin_preserve_sequential is not set, but some variables are marked with the "preserve_sequential" pragma, only those variables will receive sequential cells even if they have no loads.

WHAT NEXT

Examine the set of variables for which unloaded sequential cells are inferred.

If you do not want any unloaded sequential cells, make sure that hdlin_preserve_sequential is FALSE and no pragmas appear in your HDL source files.

If you do intend to infer some unloaded sequential cells, but some unwanted cells also appear, and the variable hdlin_preserve_sequential is TRUE, consider using the pragma method for finer control over the inference.

Otherwise, no action is required on your part.

SEE ALSO

hdlin_preserve_sequential (3), **elaborate** (2), **analyze** (2), **read** (2), **read_file** (2), **hdlin_preserve_sequential** (3).

ELAB-375 (error) %s Could not resolve hierarchical reference '%s'.

DESCRIPTION

You receive this message when the object referred to by a hierarchical identifier could not be found.

WHAT NEXT

Find the object that the hierarchical identifier was meant to refer to and fix the hierarchical name to correctly refer to this object.

SEE ALSO

elaborate (2), **analyze** (2), **read** (2), **read_file** (2),

ELAB-376 (Error) %s elaborating interface '%s'.

DESCRIPTION

This error message occurs if you attempt to elaborate a SystemVerilog interface, because that is not supported in synthesis.

WHAT NEXT

Refer to the SystemVerilog User Guide for recommended use models.

SEE ALSO

elaborate (2).

ELAB-377 (warning) %s The resolution function '%s' is not marked with a resolution method directive. It is being ignored.

DESCRIPTION

The tool issues this warning message if any function that is used as a resolution function is not marked with one of the following resolution method directives:

```
-- synopsys resolution_method wired_and
-- synopsys resolution_method wired_or
-- synopsys resolution_method wired_three_state
```

The tool does not support arbitrary resolution functions. Only *wired_and*, *wired_or*, and *three_state* functions are allowed. The tool requires that all resolution functions are marked with one of the resolution method directives indicating the kind of resolution being performed.

This resolution function will be ignored.

WHAT NEXT

This is a warning message only. No action is required on your part. However, if you do not want the resolution function to be ignored, add one of the following resolution method directives to the resolution function:

```
-- synopsys resolution_method wired_and
-- synopsys resolution_method wired_or
-- synopsys resolution_method wired_three_state
```

SEE ALSO

elaborate (2), **read** (2).

ELAB-378 (Error) %s the content %s is not defined in interface instance %s.

DESCRIPTION

You receive this error message when you are accessing the content of the interface through an instance, but the content is not defined in the interface. The following example results in the error message.

```
interface simple_bus;
logic a;
endinterface;

module top(i, o);
input i;
output o;

simple_bus sb();

assign o = i & o.b;   //b is not defined in the interface

endmodule
```

WHAT NEXT

Correct the interface content access or add the content definition in the corresponding interface and run the command again.

SEE ALSO

elaborate (2), **read** (2).

ELAB-379 (Error) %s value of double type is not supported in synthesis.

DESCRIPTION

You receive this error message because you are attempting to synthesize a real, float, or double data type, which synthesis does not support.

WHAT NEXT

Do not use real, float, or double data types for synthesis. Correct the data type and run the command again.

SEE ALSO

elaborate (2).

ELAB-380 (Error) %s name of port %s is inconsistent with

module definition or other instances.

DESCRIPTION

You receive this error message because the specified port name is inconsistent with module definition or other module instances having the named port connection. One of the ports is an interface or modport instance in the module instantiation.

In the following example, the *foo* module is instantiated with a named port connection. It uses the named ports *a*, *o* and *ifc*, and *ifc* is an interface instance. However, *a* is not in the port list of the *foo* module, so the error message occurs.

```
interface ifc;
logic x,y;
endinterface

module E (a, out1);
input [2:0] a;
output [3:0] out1;
iface ifc();
foo U1 (.a(a), .o(out1), .ifc(ifc));
endmodule

module foo(input [2:0] i, output [3:0] o, iface ifc);
endmodule
```

WHAT NEXT

Correct the names of the ports so that they are consistent, and then invoke the compiler again.

SEE ALSO

elaborate (2).

ELAB-381 (error) %s interface/modport port %s in an instantiation is incompatible with corresponding module definition or interface definition.

DESCRIPTION

This error message occurs when the specified port name in an instantiation is incompatible with the corresponding module definition or interface definition in one of the following cases:

- Connecting an interface/modport instance to a non interface/modport port
- Connecting a non interface/modport instance to an interface/modport port
- Connecting an interface instance to a different interface port
- Connecting a modport instance to a different modport
- Connecting a modport instance to a different interface port
- Connecting an interface instance to a modport port
- Connecting a modport instance to a different modport port.

In the following example, the module named *foo* is instantiated with the ports named *a*, *out1*, and *ifc*. The *ifc* port is an interface instance that is connected to the output port named *o2*. However, the *o2* port is not a compatible interface port. This causes the error message.

```
interface iface;
logic x,y;
modport MP(input x, output y);
endinterface

module E (a, out1);
input [2:0] a;
output [3:0] out1;
iface ifc();
foo U1 (ifc.MP);
endmodule

module foo(output o2);
endmodule
```

Another example that results in the error message is when you attempt to connect a modport of an interface instance to a different modport port.

```
interface iface;
wire x,y;
modport MP1(input x, output y);
modport MP2(input x, output y);
endinterface

module E (a, out1);
input [2:0] a;
output [3:0] out1;
iface ifc();
foo U1 (ifc.MP1);
endmodule

module foo(iface.MP2 ifc);
endmodule
```

Attempting to connect an interface instance to a modport port is not allowed in synthesis due to the separate compilation constraint. The following example results in the error message.

```
interface iface;
wire x,y;
modport MP(input x, output y);
endinterface

module E (a, out1);
input [2:0] a;
output [3:0] out1;
iface ifc();
foo U1 (ifc);
endmodule

module foo(iface.MP ifc);
endmodule
```

WHAT NEXT

Correct the ports in the module instantiation and the module definition so that they are consistent and then invoke the compiler again.

SEE ALSO

elaborate(2)

ELAB-382 (error) %s Module %s was not elaborated because it contains the generic interface as port.

DESCRIPTION

You receive this error message because you are elaborating a module with generic interface as port.

WHAT NEXT

Specify the interface in elaboration or elaborate the upper designs containing instantiations of this module.

SEE ALSO

elaborate (2).

ELAB-383 (error) %s Too many elements in assignment pattern expression list

DESCRIPTION

The elements listed in an aggregate expression must be in one-to-one correspondence with the members of the structure type or the elements of the array type into which the aggregate expression is being assigned, aggregated, or cast.

EXAMPLE

In the following example, structures of type *shoe* have just two members. Since *shoe* is not declared to be a *packed* structure, lists enclosed within curly braces that are assigned to *shoe*s are interpreted according to the rules for aggregate expressions. Thus, lists longer than than two elements are rejected, even if they would be valid as (packed array) concatenations.

```
typedef struct {
  logic [3:0]heel;
  logic [3:0]toe;
} shoe;

shoe left, right;
shortint tongue;

left = { right.toe, 4'b1111, tongue };      // Shoe is too small
right= { 1'b1, left.heel[2:0], left.toe };  // Not a Verilog concat
```

WHAT NEXT

Check for a mismatch between the structure declaration and its uses, due to incompatible versions of two source files.

If concatenation was intended where an unpacked aggregate expression is now parsed, consider changing the structure declaration to *packed*, or regrouping the elements to correspond to the structure members as declared.

ELAB-384 (error) %s Too few elements in assignment pattern expression list

DESCRIPTION

The elements listed in an aggregate expression must be in one-to-one correspondence with the members of the structure type or the elements of the array type into which the aggregate expression is being assigned, aggregated, or cast.

EXAMPLE

In the following example, structures of type *shoe* have just two members. Since *shoe* is not declared to be a *packed* structure, lists enclosed within curly braces that are assigned to *shoe*s are interpreted according to the rules for aggregate expressions. Thus, lists with less than two elements are rejected, even if they would be valid as (packed array) concatenations.

```
typedef struct {
  bit [3:0] sole;
  bit [3:0] tongue;
} shoe;

shoe left, right;
byte heel;

left = { right.sole }; // Shoe is too big
right= { heel };       // Not a Verilog concat
```

WHAT NEXT

Check for a mismatch between the structure declaration and its uses, due to incompatible versions of two source files.

If concatenation was intended where an aggregate expression is now parsed, check that the structure declaration is *packed*, or try decomposing and regrouping the listed elements to correspond to the structure members as declared.

ELAB-385 (Error) %s interface '%s' cannot be found.

DESCRIPTION

This error message occurs because the Presto HDL compiler cannot find the intermediate files of the interface.

WHAT NEXT

Ensure that the interface has been analyzed and the intermediate files are in the working directory, and then run the compiler again.

SEE ALSO

analyze (2), **elaborate** (2), **read** (2).

ELAB-386 (error) %s Name clash on net '%s'.

DESCRIPTION

You receive this error message because your two names in your design cause a name clash in the netlist. The name clash can be between to same named objects or two similar named objects in conjunction with a naming style.

Eg. when choosing net naming style "%n_%d" the following declarations can create a name clash:

```
// net naming style set to "%s_%d"

// nameclash regarding r_0:
reg r_0;
reg [0:3] r;  // will result in r_0, r_1, r_2 and r_3
```

WHAT NEXT

Ensure that all object names in your design are unamibiguous, considering the naming style you are using.

SEE ALSO

elaborate (2), **read** (2), **analyze** (2).

ELAB-387 (error) %s The '%s' attribute is supported only if that attribute is used in conformance with the style described in the Synopsys manual for the VHDL Compiler.

DESCRIPTION

You receive this error message when an attribute usage is not in conformance with the style described in the Synopsys manual for the VHDL Compiler.

You might have used the attribute as the RHS expression of blocking assignment, non-blocking assignment, or, in the return expression of function, etc.

WHAT NEXT

See the *HDL Compiler for VHDL Reference Manual* for ways to use the attributes.

SEE ALSO

elaborate (2), **read** (2).

ELAB-388 (warning) %s X and/or Z bits occur in an actual parameter to the '%s' design template.

DESCRIPTION

This warning message occurs when you create an instance of a parameterized subdesign using a constant value that contains X or Z bits.

In classical synthesis, these bits are zeroed to form ordinary integer or string constants. However, in the current operating mode, the full four-state parameter value is used as written when the subdesign is elaborated. If the subdesign uses it as a casex or casez statement label, there may be a mismatch between synthesis and simulation results.

Synthesis results will also differ from HDL Compiler, from versions of Presto HDL up to and including 2004.06, and from Presto synthesis results obtained with the **hdlin_allow_4state_parameters** variable set to false.

Don't care bits in parameters do not indicate wildcard matching within the design libraries.

WHAT NEXT

Convert the casex item into a literal or convert the casex statement into a case statement.

For more information, see the **-parameters** option on the **elaborate** command man page.

SEE ALSO

elaborate(2)
hdlin_allow_4state_parameters(3)

ELAB-389 (warning) %s X and Z bits in parameters of subdesign '%s' are set to zero.

DESCRIPTION

You are creating an instance of a parameterized subdesign using a constant value which contains x or z bits. In classical synthesis coding styles, parameters are integer or string constants. In the current operating mode, 4-state parameter values are being cast to 2-state values (by setting x and z bits to zero) before the subdesign is elaborated. If the subdesign uses this parameter as a casex or casez statement label, there may be a mismatch between synthesis and simulation results.

Don't-care bits in parameters do not indicate wildcard matching within the design libraries.

WHAT NEXT

Try to convert the casex item into a literal or convert the casex statement into a case statement.

SEE ALSO

elaborate -parameter **(2), hdlin_allow_4state_parameters.**

ELAB-390 (warning) %s Variable or function call in casex item is a potential simulation/synthesis mismatch.

DESCRIPTION

You receive this warning message when a variable or function call is used in a casex item. Even if an x bit is assigned to a variable or returned by a function call, the value of the case item will not match both 0 and 1, as it would for an x bit in a literal in a casex item. For example:

```
b = 2'b1x ;
casex (a)
  b : ... // in this case, 2'b1x only matches 2'b10
endcase
```

A full example:

```
module m( o1 , o2 );
output o1, o2 ;
reg o1, o2 ;

  function f ;
  input [1:0] R ;
  casex (2'b11)
    R : f = 1'b0 ;
    default : f = 1'b1 ;
  endcase
  endfunction

  always begin
   o1 = f(2'b1x) ;
  end

  reg [1:0] R;
  always begin
   R = 2'b1x;
   casex (2'b11)
     R : o2 = 1'b0 ;
     default: o2 = 1'b1 ;
```

```
      endcase
    end

  endmodule
```

WHAT NEXT

Convert the casex item into a literal or convert the casex statement into a case statement.

SEE ALSO

elaborate(2)
read(2)

Convert the casex item into a literal or convert the casex statement into a case statement.

SEE ALSO

elaborate(2)
read(2)

ELAB-391 (warning) %s Variable %s may be read before being assigned; the synthesized result may not match simulations.

DESCRIPTION

You receive this warning message because a variable that is local to a function or task may be read before being assigned. When the **hdlin_infer_function_local_latches** variable is set to **false**, the Presto HDL Compiler does not preserve variable values across separate calls to a task or function, unlike a simulator. Any bits of the variable that are not assigned before being used are given the value 0. No latches are inferred for variables local to a subprogram.

When the **hdlin_infer_function_local_latches** variable is set to **true**, the compiler matches the simulator's behavior. This may result in additional latches in your design.

WHAT NEXT

If you intended to use a value set during a previous call, set **hdlin_infer_function_local_latches** to **true** in order to preserve the value across calls.

If you did not intend to use a value across calls, check your design to verify that you assigned all local variables before using them.

SEE ALSO

elaborate(2)
read(2)

ELAB-392 (warning) %s Value of function %s may be used before being assigned; the synthesized result may not match simulations.

DESCRIPTION

A Verilog function definition implicitly declares a variable, internal to the function, with the same name as the function. You receive this warning message when the function may return without the variable having been assigned or when the variable may be read by the function body before the variable is assigned.

When the **hdlin_infer_function_local_latches** variable is set to *false*, the Presto HDL Compiler does not preserve variable values across separate calls to a task or function, unlike a simulator. Any bits of the variable that are not assigned before being used are given the value 0. No latches are inferred for variables local to a subprogram.

When the variable **hdlin_infer_function_local_latches** is set to *true*, the compiler matches the simulator's behavior. This may result in additional latches in your design.

WHAT NEXT

If you intended to use a return value set during a previous call, set **hdlin_infer_function_local_latches** to *true* in order to preserve the value across calls.

If you did not intend to use a return value across calls, check your design to verify that a meaningful value is returned by the function.

SEE ALSO

elaborate(2)
read(2)

ELAB-393 (warning) %s Value of function '%s' is used before being assigned; the synthesized result may not match

simulations.

DESCRIPTION

A Verilog function definition implicitly declares a variable, internal to the function, with the same name as the function. You receive this warning message when the function returns without the variable having been assigned or when the variable is read by the function body before the variable is assigned.

When the variable **hdlin_infer_function_local_latches** is set to *false*, the Presto HDL Compiler does not preserve variable values across separate calls to a task or function, unlike a simulator. Any bits of the variable that are not assigned before being used will be given the value 0. No latches will be inferred for variables local to a subprogram.

When the variable **hdlin_infer_function_local_latches** is set to *true*, the compiler will match the simulator's behavior. This might result in additional latches in your design.

WHAT NEXT

If you intended to use a return value set during a previous call, set **hdlin_infer_function_local_latches** to *true* in order to preserve the value across calls.

If you did not intend to use a return value across calls, check your design to verify that a meaningful value is returned by the function.

SEE ALSO

elaborate (2), **read** (2).

ELAB-394 (error) %s Specified resoure sharing (label %s) is not realizable. There is conflict among the operations.

DESCRIPTION

You receive this error message when the specified resource sharing is not realizable. For example:

```
module ppf (cond, cond2, a,b, c, d, z, y); input cond, cond2; input [3:0] a, b, c,
d; output [3:0] z, y; reg [3:0] z, y;

always @(a or b or c or d) begin : b1 /* synopsys resource r0 : ops = "a0 a1",
map_to_module = "DW01_add", implementation = "rpl", add_ops="false";*/

if (cond) begin z = a + /* synopsys label a0 */ b; y = c + /* synopsys label a1 */
```

```
d; end else z = a + c; end

endmodule

Resoure r0 can not be shared by a0 and a1.
```

WHAT NEXT

Modify resource sharing pragma, make sure the specified resources can be shared.

SEE ALSO

elaborate (2), **read** (2).

ELAB-395 (warning) %s Latch inferred in design %s read with 'hdlin_check_no_latch'

DESCRIPTION

The variable hdlin_check_no_latch directs the read command to ensure no latch is inferred in the HDL file.

WHAT NEXT

Check whether the value of hdlin_check_no_latch is correct or HDL file contains error hence latches are inferred unexpectedly.

SEE ALSO

elaborate (2), **read** (2).

ELAB-396 (warning) %s Floating net '%s' connected to ground.

DESCRIPTION

You receive this warning message when a previously unconnected net has been connected to ground. This message reminds you to check whether the behavior resulting from connecting the net to ground conforms to your expectations.

WHAT NEXT

Verify that connecting the specified net to ground results in the desired behavior.

SEE ALSO

elaborate (2), **read** (2).

ELAB-397 (error) %s The module or interface '%s' needs to be analyzed.

DESCRIPTION

This error message occurs when the Presto HDL Compiler fails to read the intermediate file after analyzing.

WHAT NEXT

Ensure that the module or interface is analyzed before running the command.

SEE ALSO

elaborate(2)
read(2)

ELAB-398 (error) %s Synthesis does not support implicit ref port '%s'.

DESCRIPTION

You receive this error message when you pass an **interface instance** to a **module instantiation** and the interface declares a variable. According to section 19.2.2 of the System Verilog LRM, such variables pass to the module as implicit ports whose direction is **ref**. However, ref ports are not supported in synthesis.

The port name cited in the message is constructed from the interface's port or instance name, followed by an underscore and the variable name.

In the following example, *s* is a logic variable in the *I* interface that becomes a ref port for module test, and causes the error message.

```
interface I();
logic s;
endinterface

module test(I i);
endmodule
```

```
module top();
I i;
test t (i);  // Error: ... implicit ref port 'i_s' (ELAB-398)
endmodule
```

WHAT NEXT

Change the variable to *net*, or refer to a *modport* of the interface which imposes a synthesizable port direction for this variable.

SEE ALSO

elaborate(2)
read(2)

ELAB-399 (error) %s Type query %s on undefined expression or type.

DESCRIPTION

You receive this error message because the tool detected an error when querying on an undefined expression or type.

In the example below, the argument of $bits is undefined, which causes the error message to be issued.

```
module top(i, o);
input [$bits(t)-1:0] i;
output [$bits(t)-1:0] o;
endmodule
```

WHAT NEXT

Correct the query argument and run the command again.

SEE ALSO

elaborate(2)
read(2)

ELAB-400 (error) %s Type query %s requires an array

reference as the first argument.

DESCRIPTION

This error message occurs when you attempt an array query on a non-array type.

In the following example, the $left argument does not have an array type, so the error message is issued.

```
typedef logic t;

module top(i, o);
input [$left(t)-1:0] i;
output [$left(t)-1:0] o;
endmodule
```

WHAT NEXT

Correct the query argument and run the command again.

SEE ALSO

elaborate(2)
read(2)

ELAB-401 (warning) %s Comparisons to don’t-care or to unknown literals are always treated as being false. This may cause simulation to disagree with synthesis.

DESCRIPTION

This warning message occurs because comparisons in hardware are inherently different than in the simulator. Digital hardware comparators can only distinguish between ones and zeros. As a result, it does not make sense to synthesize comparisons to three-state, don’t-care, or unknown literals. Since signals are assumed to carry a value of one or zero, equality tests to non-one or zero values always return false in synthesis.

WHAT NEXT

This is only a warning message. No action is required.

If the comparison was used only for simulation purposes you do not need to modify your HDL. For example, if you want to print a message when an input port is in the high-impedance state, it is acceptable to compare its value to z.

If you are using the comparison to affect the state of your circuit, you should consider recoding your HDL. For example, if you need a four-state state machine, do not declare a single-bit variable and use 0, 1, x, and z as your states. In hardware, each bit only holds two useful states: 1 and 0.

SEE ALSO

elaborate(2)

ELAB-403 (warning) %s Presto uses shift to implement signed division.

DESCRIPTION

You receive this warning message when Presto HDL Compiler uses shift to implement signed division. The result does not match the simulation result, but it is the same behavior as the HDL Compiler and Formality.

If you want to match simulation behavior, set the **hdlin_signed_division_use_shift** variable to **false**, which is the default value.

WHAT NEXT

This is only a warning message. No action is required.

However, you can perform the verification and change the value of the **hdlin_signed_division_use_shift** variable to **false** to match the simulation result.

SEE ALSO

analyze(2)
elaborate(2)
read(2)
read_file(2)
hdlin_signed_division_use_shift(3)

ELAB-404 (error) %s Unpacked type used as index.

DESCRIPTION

You receive this error message when an unpacked type is used as an index for a subscription or a vector part-select.

WHAT NEXT

Change the type of index expression or cast it to packed types and run the command again.

SEE ALSO

elaborate(2)
read(2)

ELAB-405 (warning) %s Net %s or a directly connected net may be driven by more than one process or block.

DESCRIPTION

You receive this warning message when a **reg** variable is driven by more than one always block, or a **wire** variable could be driven by more than one continuous assignment, and you have also set the **hdlin_prohibit_nontri_multiple_drivers** variable to **false**.

This warning message is issued because an invalid design could result.

In the following example, the assignment in the module could cause multidriven issues for wire t.

```
module M(input i, output o);
wire t = i;
assign t = o;
endmodule
```

The compiler permits multiple drivers on nets declared as **tri**, but it issues a warning if one of the drivers is not a three-state device.

WHAT NEXT

This is only a warning message.

An invalid design may result when this warning is issued. Multiple driver nets are only generated because the **hdlin_prohibit_nontri_multiple_drivers** variable is set to **false**.

Consider modifying the design to avoid driving a variable from more than one always block or continuous assignment.

SEE ALSO

elaborate(2)
read(2)

ELAB-406 (warning) %s The binding of %s is ignored.

DESCRIPTION

You receive this message from the **elaborate** or **read** command when the compiler eliminates binding of the specified signal. The bindings are usually made by assignments. The reason for the elimination is that there is no reference to the specified signal before the next binding.

For example:

```
always @* begin
  t = 1;
  t = 2;
end
```

The binding of the first assignment to t is overwritten by the second assignment. The message warns you that the first assignment is eliminated.

The following is another example:

```
module M (input i, output o);
reg t;
always @* begin
  t = 1;
end
endmodule
```

The binding of t is not used anywhere else, so you are warned when it is eliminated.

WHAT NEXT

This is only a warning message.

However, if the elimination is unexpected, modify the code and run the tool again.

SEE ALSO

analyze(2)
read(2)

ELAB-407 (error) %s All edge events in a single process must

depend on the same signal.

DESCRIPTION

This error message occurs when a process contains more than one event wait (in VHDL), or when an always block contains more than one edge expression (in Verilog or SystemVerilog). All of the waits must be for an edge on the same signal.

WHAT NEXT

Recode the design so that all event waits depend on the same variable.

SEE ALSO

elaborate(2)
read(2)

ELAB-408 (error) %s Only some paths through the process contain event waits; waits must occur on all or no paths through a process.

DESCRIPTION

This error message occurs when a process contains any event wait (in VHDL), or when an always block contains any edge expression (in Verilog or SystemVerilog). All paths through that block must reach at least one event wait. It must be impossible to execute the process or block without triggering a wait.

WHAT NEXT

Recode the design so that all paths reach an event wait.

SEE ALSO

elaborate(2)
read(2)

ELAB-409 (error) %s Edge expression being tested is not a

simple edge.

DESCRIPTION

This error message occurs when a process contains any event wait (in VHDL), or when an always block contains any edge expression (in Verilog or SystemVerilog). The event the system is waiting for must be a simple edge expression.

WHAT NEXT

Recode the design so that all event waits are for simple edge expressions.

SEE ALSO

elaborate(2)
read(2)

ELAB-410 (error) %s Processes with both 'wait' statements and 'if' statements that test events are not currently supported.

DESCRIPTION

This error message occurs when a process contains an event wait, and an if statement in the same process contains an event as part of the condition. This process type is not supported by Presto.

WHAT NEXT

Recode the design so that it contains only event waits or an if statement that tests an event condition.

SEE ALSO

elaborate(2)
read(2)

ELAB-411 (error) %s Processes or always blocks with multiple events are disallowed when hdlin_allow_multiple_waits is false.

DESCRIPTION

This error message occurs when the Presto HDL Compiler encounters a process

containing more than one event wait when reading or elaborating a Verilog or VHDL design.

Presto supports the read and elaborate processes, except when the **hdlin_allow_multiple_waits** variable is set to false. The default value is true.

The most common reason for setting **hdlin_allow_multiple_waits** to false is as part of a range of settings that ensure that designs can be elaborated by the Formality RTL readers.

WHAT NEXT

Either set **hdlin_allow_multiple_waits** to true, or recode the design so that it contains only a single event wait or an if statement that tests an event condition.

SEE ALSO

elaborate(2)
read(2)

ELAB-412 (error) %s Wait or event statements that do not depend on edge events are not supported.

DESCRIPTION

This error message occurs when the design being read or elaborated contains a process with a wait statement that does not depend on an edge event, or an always block that does not depend on a posedge or negedge expression.

This error also occurs when SystemVerilog designs contain special-form always blocks, such as always_comb or always_ff, and also contain a sensitivity list. Designs containing any of these statements are not supported.

WHAT NEXT

Recode the design so that it contains only event waits.

SEE ALSO

elaborate(2)
read(2)

ELAB-413 (error) %s Processes containing more than one ’if’

statement that tests an event expression are not supported.

DESCRIPTION

This error message occurs because a process that contains more than one if statement that tests an event expression is not supported.

WHAT NEXT

Recode the design so that each process contains no more than one if statement that tests an event expression in each process.

SEE ALSO

elaborate(2)
read(2)

ELAB-414 (warning) %s Ignoring %s - too complex for synthesis to utilize.

DESCRIPTION

This warning message issues when the Presto HDL Compiler finds a labelled assertion or assertion severity system task call whose logical structure lies outside the current synthesis subset.
• Generally, the asserted expression should compare only one variable or signal to a compile-time constant, or else

• It should make a $onehot or $onehot0 claim about a collection of signal wires.

• It must not have any statements in its action_block.

• It should use bitwise NOT (~) of the complete argument, rather than reduction NOT (!) of each bit when forming a $onehot() argument to assert a one-cold relationship.

Consult the SystemVerilog User Guide for the exact definition of the subset currently supported by this release.

WHAT NEXT

This is only a warning message. No action is required.

However, if you do not want the construct to be ignored, you must simplify it, perhaps into several separate relations.

SEE ALSO

elaborate(2)
confirmed_SVA(3)
hdlin_enable_assertions(3)

ELAB-420 (warning) %s Invalid symbol '%s' or expression in a signal name list of a pragma or assertion. It is being ignored.

DESCRIPTION

This warning message occurs when the Presto HDL Compiler finds an invalid symbol or expression in the list of signal names submitted to a Verilog or VHDL compiler pragma or in a SystemVerilog assertion. This can be caused by one of the following:

• The type of the signal or expression is invalid for the pragma or asserted condition.

• If the signal or its expression is an array, its index or bounds should be a constant expression. No function call is allowed, including a constant function call.

• The type of the signal or the expression accessing it cannot involve a union type.

• For one_hot and one_cold pragmas or $onehot and $onehot0 system functions, the signal name list can only contain signals that are ports.

WHAT NEXT

This is only a warning message. No action is required.

However, if you do not want the symbol and/or its expression to be ignored in this context, correct the symbol name and/or its expression and analyze the RTL again.

SEE ALSO

analyze(2)
elaborate(2)
read(2)

ELAB-425 (error) %s Found expression without known width in

context that requires one

DESCRIPTION

You receive this error when you use an expression that cannot have a width or whose width cannot be determined in a context that requires an expression with a well-defined width.

An example from SystemVerilog:

```
interface IFC;
  logic a, b;
  assign b = a;
  modport mp(output a, input b);
endinterface

module test(output out, input in);
  IFC ifc();
  bot bot(ifc.mp, out, in);
endmodule

module bot (IFC.mp ifc, output out, input in);
  assign out = ifc; // Error -- intended ifc.b, not just ifc
  assign ifc.a = in;
endmodule
```

WHAT NEXT

Make sure that you have not written an expression without a well-defined width.

SEE ALSO

elaborate (2), **read** (2).

ELAB-490 (error) %s Variable or function call in casex item is a potential simulation/synthesis mismatch.

DESCRIPTION

You receive this error message in verification friendly mode when a variable or function call is used in a casex item. Even if an x bit is assigned to a variable or returned by a function call, the value of the case item will not match both 0 and 1, as it would for an x bit in a literal in a casex item. For example:

```
b = 2'b1x ;
```

```
      casex (a)
        b : ... // in this case, 2'b1x only matches 2'b10
      endcase
```

A full example:

```
   module m( o1 , o2 );
   output o1, o2 ;
   reg o1, o2 ;

     function f ;
     input [1:0] R ;
     casex (2'b11)
       R : f = 1'b0 ;
       default : f = 1'b1 ;
     endcase
     endfunction

     always begin
      o1 = f(2'b1x) ;
     end

     reg [1:0] R;
     always begin
      R = 2'b1x;
      casex (2'b11)
        R : o2 = 1'b0 ;
        default: o2 = 1'b1 ;
      endcase
     end

   endmodule
```

WHAT NEXT

Convert the casex item into a literal or convert the casex statement into a case statement.

SEE ALSO

elaborate(2)
read(2)

ELAB-491 (warning) %s Embedded configuration statements

are not supported for synthesis. They are ignored.

DESCRIPTION

This warning is issued when the design on which the **elaborate** or **read** command is invoked includes embedded configuration statement. Embedded configuration statements are not supported, and is ignored.

WHAT NEXT

Rewrite the design using configuration blocks and try again.

SEE ALSO

elaborate (2), **read** (2).

ELAB-495 (error) %s Variable or function call in case-inside item is a potential simulation/synthesis mismatch.

DESCRIPTION

You receive this error message in when a variable or function call is used in a case-inside item. Even if an x bit is assigned to a variable or returned by a function call, the value of the case-inside item will not match both 0 and 1, as it would for an x bit in a literal in a case-inside item. For example:

```
b = 2'b1x ;
case (a) inside
  b : ... // in this case, 2'b1x only matches 2'b10
endcase
```

A full example:

```
module m( o1 , o2 );
output o1, o2 ;
reg o1, o2 ;

  function f ;
  input [1:0] R ;
  case (2'b11) inside
    R : f = 1'b0 ;
    default : f = 1'b1 ;
  endcase
  endfunction
```

```
    always begin
     o1 = f(2'b1x) ;
    end

    reg [1:0] R;
    always begin
     R = 2'b1x;
     case (2'b11) inside
       R : o2 = 1'b0 ;
       default: o2 = 1'b1 ;
     endcase
    end

  endmodule
```

WHAT NEXT

Convert the case-inside item into a literal or convert the case-inside statement into a case statement.

SEE ALSO

elaborate(2)
read(2)

ELAB-500 (warning) %s No Design Compiler license, Presto optimization: %s can not be enabled.

DESCRIPTION

Presto advanced optimizations need check Design Compiler (DC) license. If no DC license, the optimizations will not be enabled and this warning message will be generated.

WHAT NEXT

Get DC license.

ELAB-501 (error) %s defparam assignment for %s was ignored.

DESCRIPTION

Defparam assignment to task, function or block parameters are ignored for synthesis.

WHAT NEXT

Recode the design using named parameter assignments and try again.

ELAB-510 (information) %s Presto preserved an unloaded net '%s'.

DESCRIPTION

You receive this information message when Presto HDL Compiler preserves a net that may not be driving any loads.

WHAT NEXT

Check your design for possible misconfiguration of port directions or port connections and try again. You may ignore this information if the connections are part of the required design specifications.

ELAB-600 (error) %s Pre-analyzed files for module '%s' not found.

DESCRIPTION

You receive this message because the Presto HDL compiler cannot find the pre-analyzed files for the given module during elaboration.

WHAT NEXT

Ensure that the module to be elaborated has been analyzed with the variable hdlin_sv_ieee_assignment_patterns set to a value of 2 or higher.

SEE ALSO

elaborate (2), **analyze** (2).

ELAB-601 (error) %s %s is not supported for %s.

DESCRIPTION

The combination of array of instances and assignment patterns on ports on a module

instantiation is not supported for synthesis.

WHAT NEXT

Please recode to remove either the array of instances, or the assignment pattern on the ports construct and try again.

SEE ALSO

elaborate (2), **analyze** (2).

ELAB-800 (error) %s The loop variable is not initialized to a constant.

DESCRIPTION

You receive this error message when your loop variable is not initialized to a constant, as required by Presto synthesis. The following example results in the error message.

```
for(i = non_constant ; i< 64 ; i = i+1)
 begin
   loop_body
 end
```

WHAT NEXT

Rewrite the loop so that the loop variable is initialized to a constant. The previous example can be rewritten as follows if non_constant is positive:

```
for (j = 0; j<64; j = j+1)
 begin
   i = j + non_constant;
   if ( i < 64 )
      loop_body
 end
```

SEE ALSO

elaborate (2), **read** (2);

ELAB-801 (warning) %s BDD result may not be complete.

DESCRIPTION

You receive this error message because the BDD memory limit has been reached. The BDD result may not be complete, so the QOR (Quality of Results) may be worse than expected. The default BDD memory limit is 6M.

WHAT NEXT

Use the hidden variable **hdlin_bdd_memory_limit** to increase the memory limit.

SEE ALSO

elaborate (2), **read** (2);

ELAB-802 (warning) %s The port default value in entity declaration for port '%s' is not supported. Presto ignores it.

DESCRIPTION

You receive this warning message because port default values in entity declaration are ignored by Presto VHDL.

In the following example, the port default values '1' and 'Z' for the ports A and Z will be ignored:

```
entity test is
  port (A: in std_logic := '1';
        EN: in std_logic;
        Z: out std_logic := 'Z'
       );
end;
```

WHAT NEXT

Verify if it implements the behavior you intended after ignoring the port default values, and modify your code if needed.

SEE ALSO

elaborate (2), **read** (2).

ELAB-803 (warning) %s There is a name conflict between the instance '%s' and an existing cell. The name of the instance is being renamed to '%s'.

DESCRIPTION

This warning message occurs when you specify an instance name of a module instantiation that has already been used by another existing cell. The message may be caused by the following circumstances:

• There is a name conflict between your instance name and another instance name generated in FOR-GENERATE statement. In this case, if the original instance name in the FOR-GENERATE statement is *mod_name*, the tool may generate a series of instance names based on it in the form: *mod_name*, *mod_name_1*, *mod_name_2*, etc.

• There is a name conflict between your instance name and another instance name in your code.

WHAT NEXT

If you want the instance name to be renamed to the new name indicated in the warning message, no action is required on your part. However, if you want to keep the instance name unchanged, you can resolve the conflict by modifying the name of the conflicting instance name in your code, and then run the tool again.

SEE ALSO

elaborate (2), **read** (2).

ELAB-804 (error) %s error found for parameters value near token '%s'.

DESCRIPTION

This error message occurs when there is an error in the parameter value list given by the module or component instantiation or by the **elaborate** command.

Presto VHDL adds support for the following types:

integer

```
   bit
   bit_vector
   std_ulogic
   std_ulogic_vector
   std_logic
   std_logic_vector
   signed
   unsigned
```

Presto Verilog adds support for parameters with Verilog numbers and strings.

Presto SVerilog adds support for parameters with Verilog numbers, strings, and type parameters.

The parameter specification is a list of values separated by commas, based on parameter order (for example, "3,4,5") or parameter names (for example, "N=>8,M=>16").

WHAT NEXT

Correct the error in the parameter value list and run the command again. See the man page for the **elaborate** command for information on the accepted parameter list syntax.

SEE ALSO

elaborate(2)

ELAB-820 (error) %s This use of clock'event specification not supported

DESCRIPTION

This error occurs if you use more than one **if clock'event** expression in a process or if you embed the **clock'event** expression inside a subprogram or loop.

The following example shows a positive- and negative-edge trigger in the same process.

```
entity test is
  port(clock, a: in bit; z1, z2: out bit);
end;

architecture a of test is
begin
  process (clock)
  begin
    if(clock'event and clock = '1') then
      z1 <= a;
```

```
    end if;

    if(clock'event and clock = '0') then -- ERROR
      z2 <= a;
    end if;
  end process;
end;
```

WHAT NEXT

Restructure your code to have a single "if clock'event" construct at the start of the process.

The previous example can be fixed by splitting the process into two processes.

```
entity test is
  port(clock, a: in bit; z1, z2: out bit);
end;

architecture a of test is
begin
  process (clock)
  begin
    if(clock'event and clock = '1') then
      z1 <= a;
    end if;
  end process;

  process (clock)
  begin
    if(clock'event and clock = '0') then
      z2 <= a;
    end if;
  end process;
end;
```

ELAB-832 (warning) %s Undriven register '%s' is connected to primary output '%s'.

DESCRIPTION

This warning message occurs when Presto determines that the listed register is not driven in the source code. The cause might be an issue in your design. Review your source code to ensure that this will not translate to incorrect outputs.

Normally, Presto grounds undriven registers, but the listed register will not be grounded because it is connected to a primary output.

An example of this situation happens in the following code:

```
module example(input [1:0] x, input y, output reg [1:0] z);
  always @* begin
    z[2*x]= y;
  end
endmodule
```

For z[1], Presto normally creates the register z_reg[1], but it can never be assigned because 2*x will never be 1. Therefore, z_reg[1] is an undriven register and it is not created. The output z[1] is also undriven.

WHAT NEXT

Modify your code to drive the listed register properly.

SEE ALSO

ELAB-833n

ELAB-833 (warning) %s Register '%s' is undriven.

DESCRIPTION

This warning message occurs when Presto determines that the listed register is not driven in the source code. The cause might be an issue in your design. Review your source code to ensure that this will not translate to incorrect outputs.

An example of this situation happens in the following code:

```
module example(input [1:0] x, input y, output reg z);
  reg [1:0] t;
  always @* begin
    t[2*x]= y;
    z= &t;
  end
endmodule
```

For t[1], Presto normally creates the register t_reg[1], but it can never be assigned because 2*x will never be 1. Therefore, t_reg[1] is an undriven register and it is not created.

Note that Presto grounds automatically undriven registers that are not connected to primary outputs. In the example Presto handles t[1] as constant 0 because it is not directly connected to output z. The output z is 0.

For undriven registers connected to primary outputs, Presto issues a warning with the ELAB-832 message.

WHAT NEXT

Modify your code to drive the listed register properly.

SEE ALSO

ELAB-832(n)

ELAB-900 (error) %s Loop exceeded maximum iteration limit.

DESCRIPTION

You receive this error message when your loop runs on forever, or is designed to run some number of times greater than the iteration limit. When the compiler processes loops, the loop condition must fail at some point.

WHAT NEXT

Set the **hdlin_while_loop_iterations** variable to a higher number.

SEE ALSO

elaborate (2), **read** (2); **hdlin_while_loop_iterations** (3).

ELAB-901 (error) %s Function call stack exceeded maximum depth.

DESCRIPTION

This error message occurs when the depth of the function call stack exceeds the maximum depth currently supported by Presto to prevent runaway function call chains.

The most probable cause of this error is that your design has an infinite recursion.

Note that this message may be shown for recursive functions that finish in simulation, but are infinite in synthesis. One example of infinite recursion, and thus unsupported, is this design:

```
module fact (input [3:0] n, output [40:0] z);

  function [40:0] f;
  input [3:0] k;
  begin
    if (k==0)
```

```
        f = 1;
      else
        f = k * f(k-1);
    end
    endfunction

    assign z = f(n);
  endmodule
```

This example will not finish in synthesis because the terminating condition depends on a port and therefore is never a proper constant.

WHAT NEXT

Check your design for an infinite recursion and then run the command again.

SEE ALSO

elaborate(2)
read(2)

ELAB-902 (warning) %s In the call to '$display', the '%%%c' format specifier is not supported.

DESCRIPTION

You receive this warning message when you execute the **elaborate** or the **read** command with a format specifier that is not supported. The following specifiers are supported, and the rest are ignored:

WHAT NEXT

Reexecute the **elaborate** or **read** command with a format specifier that is supported.

SEE ALSO

elaborate (2), **read** (2).

ELAB-903 (warning) %s Insufficient pins supplied to array of

modules for instance '%s' of design '%s'.

DESCRIPTION

You receive this warning message when the wires you specify for a given port do not meet the following requirements:

1) Wires must match the width of the port on the module.

2) The wires must be an integer multiple of the width of the port.

WHAT NEXT

Respecify the wires so that they meet the above requirements.

SEE ALSO

elaborate (2), **read** (2).

ELAB-904 (error) %s When instantiating '%s' array of modules, the implementation design '%s' must be available.

DESCRIPTION

You receive this error message when you execute the **elaborate** or **read** command and specify an array of modules that contain a black box.

Because of the strict nature of the port connections for instantiating an array of modules, the design to be instantiated cannot be a black box; you must provide the complete design.

WHAT NEXT

Verify that the implementation design is available. Also check to see that there is not a typo in the name of the module to be instantiated.

SEE ALSO

elaborate (2), **read** (2).

ELAB-906 (error) %s Too many parameters passed to module

instance %s.

DESCRIPTION

You receive this message because the list of parameter override values exceeds the number of parameters declared in the module. This is a list of parameter override values that can be supplied when instantiating a module.

WHAT NEXT

Ensure that the number of parameters passed to a module instance matches the number of parameters declared in the module.

ELAB-908 (error) %s Exponentiation is only supported if the base is a power of 2 or the exponent is 2.

DESCRIPTION

You receive this error message because one of these situations exist. Either

1. The base of an exponentiation expression is variable and the exponent is not 2.

or

2. The exponent is not 2.

WHAT NEXT

Correct the expression so that its base is constant or its exponent is not 2.

SEE ALSO

elaborate (2) ~

ELAB-909 (warning) %s Case statement is not a full case.

DESCRIPTION

You receive this warning message because you used the "// synopsys full_case" directive for this case statement and you set the **hdlin_check_user_full_case** variable to **true**. However, the case statement is not a full case statement.

WHAT NEXT

No action is necessary on your part. However, you can verify that the case statement implements the behavior you intended, try to make the case statement full, or set the **hdlin_check_user_full_case** variable to **false**.

SEE ALSO

elaborate (2), **read** (2).

ELAB-910 (warning) %s Case statement is not a parallel case.

DESCRIPTION

You receive this warning message because you used the "// synopsys parallel_case" directive for this case statement and you set the **hdlin_check_user_parallel_case** variable to **true**. However, this case statement is not parallel. A case is parallel when all of its branches are mutually exclusive.

WHAT NEXT

Try to make the case statement parallel, or set the **hdlin_check_user_parallel_case** variable to **false**.

SEE ALSO

elaborate (2), **read** (2).

ELAB-911 (error) %s Can not find return port name of type function '%s'.

DESCRIPTION

You receive this error message because this type function does not have the required return port name.

WHAT NEXT

Define a return port name for the type function by using -- pragma **return_port_name**.

SEE ALSO

elaborate (2).

ELAB-912 (error) %s Negative exponent.

DESCRIPTION

You receive this error message when the tool detects a negative exponent.

The exponent might be entered directly or might be the result of an expression. For example, the expression (2**(M-N)) has a negative exponent when both M and N are constant, and N is larger than M.

WHAT NEXT

Remove the negative exponent from the expression.

SEE ALSO

elaborate (2).

ELAB-913 (error) %s Divide by zero.

DESCRIPTION

You receive this error message when the tool detects division by a constant value, which is zero in a VHDL file.

The zero might be entered directly or it might be the result of an expression. For example, the expression (WIDTH/(M-N)) divides by zero if both M and N are equal constants.

WHAT NEXT

Remove the division by zero from the expression.

SEE ALSO

elaborate (2).

ELAB-914 (error) %s Direction (’to’ or ’downto’) does not agree

with ’first’ and ’last’ values in range.

DESCRIPTION

You receive this error message because you specified a direction that conflicts with the position in the range.

• Use the keyword **downto** when the first value in the range is greater than the last value.

• Use the keyword **to** when the first value in the range is less than the last value.

WHAT NEXT

Rewrite your descriptions using **downto** and **to** as described above. In the following example, the direction is **downto**, because 15 is greater than 0.

```
VHDL:
   signal my_bus : bit_vector ( 15 to 0 );
```

SEE ALSO

elaborate (2).

ELAB-915 (error) %s Expected value but was supplied unknown

DESCRIPTION

You receive this error message because a case statement contains "unknown" instead of a value.

For example, the tool issues the message if an enumeration literal with a U encoding is supplied to a case statement.

WHAT NEXT

Change the case choice to avoid an unknown value.

SEE ALSO

elaborate (2).

ELAB-916 (error) %s Can not find definition for %s .

DESCRIPTION

You receive this error message if the declared function, operator, or procedure cannot be found in the VHDL libraries or packages.

WHAT NEXT

Include the correct library or package.

SEE ALSO

elaborate (2), **read** (2).

ELAB-917 (error) %s Type of port '%s' is unconstrained.

DESCRIPTION

You receive this error message if the port type is unconstrained.

WHAT NEXT

Do not use unconstrained for the port type.

SEE ALSO

elaborate (2), **read** (2).

ELAB-918 (warning) %s Physical types are not supported. Presto ignores it.

DESCRIPTION

You receive this warning message because physical types are not supported by Presto VHDL. Presto ignores physical types.

WHAT NEXT

No action is required on your part. Use caution when physical types are used.

SEE ALSO

elaborate (2), **read** (2).

ELAB-919 (error) %s Unsupported range type used in array declaration.

DESCRIPTION

You receive this error message because the range type you specified in the array declaration is not supported. For example, std_logic is not supported as the range of an array.

WHAT NEXT

Rewrite the array declaration using a supported range type.

SEE ALSO

elaborate (2), **read** (2).

ELAB-920 (warning) %s OPS entry '%s' is already included in another resource. Entry ignored.

DESCRIPTION

You receive this warning message because during **elaborate** or **read** command activity, the compiler detected a label that appears in the ops list of more than one resource, which is invalid.

The following example shows the invalid entry:

```
synopsys resource r0 : ops = "op1 op2";    //op2 appears twice
synopsys resource r1 : ops = "op2 op3";
```

WHAT NEXT

Correct your code so that each label appears in the ops list of only one resource.

SEE ALSO

elaborate (2), **read** (2).

ELAB-921 (error) %s Built-in %s currently is not supported yet.

DESCRIPTION

The built-in used is not supported yet. Changes to VHDL sources may be needed.

WHAT NEXT

Change your VHDL source file to avoid using the built-in.

SEE ALSO

elaborate (2), **read** (2).

ELAB-922 (error) %s Constant value required.

DESCRIPTION

This error message occurs because an expression in the indicated line of your RTL description does not evaluate to a constant value, as required by the language.

In the example below, the expression in the generate case statement is required to evaluate to a constant value at elaboration time. The use of an input port in that expression violates this requirement.

```
module m (a);
  input a;

  generate
    case (a)        // error: not constant
    ...
  endgenerate
endmodule
```

WHAT NEXT

Change your source file to use a constant value and run the command again.

SEE ALSO

elaborate (2), **read** (2).

ELAB-923 (error) %s Potential glitch on net '%s': A signal/

variable can’t be synchronously and asynchronously assigned within the same process.

DESCRIPTION

This error is issued when the design on which the **elaborate** or **read** command is invoked is not supported for synthesis because there is a potential glitch on a net. This is caused by the order in which multiple sequential statements that assign to the same net are executed.

In the following example, the if statements are executed sequentially.

```
architecture RTL of E is
begin
  process (CLK, RST)
  begin
    if (CLK’event and CLK =’1’) then
      Q <= D;
    end if;
    if (RST = ’1’) then
      Q <= ’0’;
    end if;
  end process;
end RTL;
```

In the event that the conditions on both if statements evaluate to TRUE, Q will momentarily be assigned the value of D before being assigned ’0’, resulting in a possible glitch.

To avoid this situation, if a D flip-flop with an asynchronous reset is desired, the rtl can be rewritten as shown.

```
architecture RTL of E is
begin
  process (CLK, RST)
  begin
    if (RESET = ’1’) then
      Q <= ’0’;
    elsif (CLK’event and CLK =’1’) then
      Q <= D;
    end if;
  end process;
end RTL;
```

WHAT NEXT

Modify the design to avoid a potential glitch on a net and ensure that the design accurately specifies the desired functionality. Invoke the compiler again.

SEE ALSO

elaborate (2), **read** (2).

ELAB-924 (warning) %s Signal assignment delays are not supported for synthesis. They are ignored.

DESCRIPTION

This warning is issued when a signal assignment statement in the design on which the **elaborate** or **read** command is invoked includes delay information. The delay is not supported and is ignored.

WHAT NEXT

No modification is required. Ensure the delay that is ignored is not integral to the functionality of the design.

SEE ALSO

elaborate (2), **read** (2).

ELAB-925 (error) %s Attribute %s is not supported for synthesis.

DESCRIPTION

This error is issued when the compiler encounters an attribute that is not supported for synthesis in the design on which the **elaborate** or **read** command is invoked.

WHAT NEXT

Remove the attribute that is causing the error and rerun the compiler.

SEE ALSO

elaborate (2), **read** (2).

ELAB-926 (error) %s %s types are not supported for synthesis.

DESCRIPTION

This error is issued when the compiler encounters a physical, access, or file type in the design on which the **elaborate** or **read** command is invoked. These types are not supported for synthesis.

WHAT NEXT

Avoid using unsupported types in the design.

SEE ALSO

elaborate (2), **read** (2).

ELAB-927 (error) %s cannot find architecture %s of entity %s in library %s.

DESCRIPTION

This error message occurs when the compiler is unable to find a specific entity or architecture pair in a library.

WHAT NEXT

Ensure that all entity and architecture names are specified correctly. Remove any special characters that may be problematic.

SEE ALSO

elaborate (2), **read** (2).

ELAB-928 (error) %s An if statement containing a clock event has an illegal else branch and is not supported for synthesis.

DESCRIPTION

This error occurs when a value is assigned on the "else" part of an "if clock’event".

An example of RTL that is not synthesizable because an assignment does not depend on a clock edge is shown:

```
entity test is
  port(clock, a, b: in bit; z: out bit);
end;

architecture a of test is
begin
  process (clock, a, b)
  begin
    if(clock'event and clock = '1') then
      z <= a;
    else
      z <= b; -- ERROR
    end if;
  end process;
end;
```

The following example shows RTL that is not synthesizable because assignments occur on multiple clock edges:

```
entity test is
  port(clock, a, b: in bit; z: out bit);
end;

architecture a of test is
begin
  process (clock, a, b)
  begin
    if(clock'event and clock = '1') then
      z <= a;
    elsif(clock'event and clock = '0') then
      z <= b; -- ERROR
    end if;
  end process;
end;
```

A variable can receive both asynchronous and synchronous assignments, but the asynchronous assignment must take precedence. That is, there must be a Boolean condition that enables the asynchronous part and disables the synchronous part.

WHAT NEXT

Use an "if" statement to ensure that either that the asynchronous or synchronous assignments fire in any execution of the process. Make sure that the condition controlling this "if" (the asynchronous reset condition) is level sensitive, not edge sensitive.

SEE ALSO

elaborate (2), **read** (2).

ELAB-929 (error) %s Illegal use of unpacked type %s.

DESCRIPTION

This error message occurs because the RTL code uses an unpacked type in a location where unpacked types are illegal, as shown in the following example.

```
     struct {int i;} ctrl;   // unpacked structure
     ...
     y = ctrl ? a:b;  //
 error: control expression not allowed to be of unpacked type
```

WHAT NEXT

Change the unpacked type to a packed type and run the command again.

SEE ALSO

elaborate (2), **read** (2).

ELAB-930 (error) %s Incompatible types %s.

DESCRIPTION

This error message occurs because the language standard requires the equivalence of two types in the indicated context, but the actual provided types are not equivalent, as shown in the example below.

```
   // two non equivalent structures
   struct {int i;} a;
   struct {char c;} b;
   ...
   y = c ? a : b;  // error: types of both conditional branches must be equivalent
```

The precise rules for type compatibility are given in section 5.8 of the *SystemVerilog LRM*. Incompatibility can arise due to differences in vector widths, packed versus unpacked dimensions, unpacked structures that come from different declaration sites, or other inconsistencies between two data types where they are required to correspond.

WHAT NEXT

The end of the error message indicates the kind of construction that requires the type equivalence, which is usually an assignment, an aggregate construction, or a relational operator.

Identify the part of the cited line that corresponds to the indicated language feature. Determine the source of the two types that are involved. Correct the data accesses or their type declarations so that equivalent types are used and run the command again.

SEE ALSO

elaborate(2)
read(2)

ELAB-931 (warning) %s implicit truncation caused by range overflow.

DESCRIPTION

This warning message occurs when a value is truncated by the CONV_SIGNED or CONV_UNSIGNED function, because the value overflows the range specified by SIZE.

WHAT NEXT

This is a warning message only. No action is required on your part. However, be aware that some information may be lost because of the truncation.

SEE ALSO

elaborate (2), **read** (2).

ELAB-932 (Error) %s %s type as range type is not supported.

DESCRIPTION

You receive this error message because the range type you specified in the array declaration or loop parameter is not supported. For example, std_logic/bit/boolean is not supported as the range of an array. or std_logic/bit/boolean is not supported as the discrete range in the loop parameter.

WHAT NEXT

Rewrite the array declaration or loop parameter range using a supported range type.

SEE ALSO

elaborate (2), **read** (2).

ELAB-933 (warning) %s REM operator is synthesized differently in this version of HDL Compiler.

DESCRIPTION

This warning message occurs when a REM operator with a potentially negative first operand is encountered.

Previous versions of HDL Compiler synthesized the REM operation as a MOD operation, resulting in a potential synthesis and simulation mismatch.

The Presto engine within HDL Compiler handles a REM operation with a negative first operand correctly and does not translate it as a MOD operation. Therefore, Presto HDL Compiler does not produce the same result as previous versions of HDL Compiler.

WHAT NEXT

This is a warning message only. No action is required on your part.

If a REM operation is intended, be aware that the synthesis results may differ from that of older versions of HDL Compiler. However, if a MOD operation is intended, modify the source code to use a MOD operator.

To suppress further instances of this warning, add ELAB-933 to the list of error codes specified by the suppress_errors variable.

SEE ALSO

elaborate (2), **read** (2).

ELAB-934 (error) %s Architecture '%s' of design '%s' cannot be found.

DESCRIPTION

This error occurs when the specified architecture for a design cannot be found.

WHAT NEXT

Ensure the desired architecture exists and has been specified correctly.

SEE ALSO

elaborate (2), **read** (2).

ELAB-935 (warning) %s the direction (to or downto) does not agree with the values first and last in the range.

DESCRIPTION

This warning message occurs when you specify a direction that conflicts with the position in the range.

• Use the keyword **downto** when the first value in the range is greater than the last value.

• Use the keyword **to** when the first value in the range is less than the last value.

WHAT NEXT

This is a warning message only. No action is required.

Ignore the warning message if the code is unreachable. However, if the code does not reflect the design you intended, make the necessary corrections and rerun the command.

SEE ALSO

elaborate(2)

ELAB-936 (warning) %s Attribute %s is not supported for synthesis and will be ignored.

DESCRIPTION

This warning is issued when the compiler encounters an attribute that is not supported in the design on which the **elaborate** or **read** command is invoked.

WHAT NEXT

No user action is required. However, be aware that the attribute will be ignored.

SEE ALSO

elaborate (2), **read** (2).

ELAB-937 (error) %s Constant expression too complex.

DESCRIPTION

You are receiving this error message because in a context requiring a constant expression you are using an expression that is not constant or too complex to be handeled by the compiler. This can be a restriction of the language or the compiler.

Example:

```
  module (in);
  input [0:3] in;
  parameter p = 2;

  generate
    if (in[p])    // error: in[p] is not a constant expression
      ...
  end generate
```

WHAT NEXT

Simplify the constant expression so the compiler can determine the value at compile time.

SEE ALSO

elaborate (2), **read** (2).

ELAB-938 (error) %s An order based parameter was specified after a name based parameter for the module instance %s.

DESCRIPTION

This error happens when the argument to the elaborate command includes a combination of order-based and name-based parameter values, and all the order-based parameters are not specified before name-based parameters.

WHAT NEXT

Modify the arguments to the elaborate command so that all order-based parameters occur before name-based parameters.

SEE ALSO

elaborate (2).

ELAB-939 (error) %s The system function '%s' is not supported for synthesis.

DESCRIPTION

This error message occurs when a system function called in the design is not implemented for synthesis.

WHAT NEXT

Remove the specified system function call in your design and reread or reanalyze it.

SEE ALSO

elaborate(2)
read(2)

ELAB-940 (warning) %s real types are ignored.

DESCRIPTION

This warning message occurs when a real type is encountered in the design. Real types are not supported by the compiler and are ignored.

WHAT NEXT

This is a warning message only. No action is required.

However, be aware the portion of the design that involves real types will not be implemented.

SEE ALSO

elaborate(2)
read(2)

ELAB-941 (error) %s attribute %s of prefix %s cannot be found.

DESCRIPTION

This error message occurs when the attribute specification of the named attribute in the attribute reference is nonexistent or is defined in an invalid scope.

WHAT NEXT

Ensure that the attribute specification of the desired attribute is defined in the current scope and then rerun the command.

SEE ALSO

elaborate(2)
read(2)

ELAB-942 (Error) %s %s of physical types are not supported in synthesis.

DESCRIPTION

You receive this error message because physical types are not supported by Presto VHDL as procedure or function parameters, entity or block ports types, etc.

WHAT NEXT

Remove the procedure or function parameters, or the entity or block ports that are assuming physical types and rerun the command.

SEE ALSO

elaborate(2)
read(2)

ELAB-943 (warning) %s Generic %s does not have a default value.

DESCRIPTION

You receive this warning message because the generic default value is not specified.

WHAT NEXT

Set the default value for the given generic and run the command again.

SEE ALSO

elaborate(2)
read(2)

ELAB-944 (warning) %s Non-standard coding style used to implement a sequential element.

DESCRIPTION

You receive this warning message when the design contains a non-standard coding style to describe a sequential element. Non-standard coding styles can lead to problems during simulation and may not be supported by other tools.

The following example contains a non-standard coding style to infer a sequential element with asynchronous reset. Two separate if statements are used to describe the synchronous part and the asynchronous reset. This can cause a problem during simulation.

```
entity e is
 port (d: in bit;
       q: out bit;
       clk: in bit;
       r: in bit
      );
end;

architecture a of e is
 signal t: bit;
begin

 p: process (clk) is
 begin
  if (clk'event and clk = '1') then
    t <= d;
  end if;
  if (r = '1') then
    t <= '0';
  end if;
 end process;

 q <= t;

end;
```

The next example shows a standard way to describe the sequential element:

```
entity e is
 port (d: in bit;
       q: out bit;
       clk: in bit;
       r: in bit
      );
end;

architecture a of e is
 signal t: bit;
begin

 p: process (clk) is
 begin
  if (r = '1') then
    t <= '0';
  else if (clk'event and clk = '1') then
    t <= d;
  end if;
 end process;

 q <= t;

end;
```

WHAT NEXT

This is only a warning message. No action is required.

If you are willing to accept potential simulation problems, you can leave the code unchanged.

If you want to avoid possible simulation problems, refer to the *HDL Compiler (Presto Verilog) Reference Manual* or *HDL Compiler (Presto VHDL) Reference Manual* for the recommended coding style.

SEE ALSO

elaborate(2)
read(2)

ELAB-945 (error) %s Attribute not supported with index value

different from ’1’.

DESCRIPTION

You receive this error because the VHDL attribute is used with an index value different from ’1’. The attribute is only supported for index value ’1’.

WHAT NEXT

Rewrite your VHDL code so it doesn’t use the attribute with an index value different from ’1’.

SEE ALSO

elaborate(2)
read(2)

ELAB-946 (error) %s Assignment to %s overflows declared bounds.

DESCRIPTION

This error message occurs when a variable is assigned a value whose size is larger than the declared bounds of the variable.

WHAT NEXT

Fix the offending assignment and try again.

SEE ALSO

elaborate (2), **read** (2).

ELAB-950 (error) %s out of bounds index [%d] into scope array ’%s’.

DESCRIPTION

This error message occurs when the index value specified is not within the declared range of the scope array. For example:

```
generate
 genvar i;
 for (i=3; i>0; i=i-1) begin : forlbl
   always @(posedge clk) begin : alwlbl
       reg tmp;
       o[i] = tmp;
       forlbl[i+1].alwlbl.tmp = b[i] & a[i];  // Error on accessing forlbl[4]
   end
 end
endgenerate
```

WHAT NEXT

Rewrite your design to change or eliminate the illegal access and run the command again.

SEE ALSO

elaborate(2)
read(2)

ELAB-951 (error) %s Indexed access to %s not allowed.

DESCRIPTION

This error message occurs when an indexed access is made into a scope that does not support indexed operation.

WHAT NEXT

Rewrite your design to change or eliminate the illegal access and try again.

SEE ALSO

elaborate(2)
read(2)

ELAB-952 (error) %s The genvar '%s' has been assigned the value '%s' repeatedly.

DESCRIPTION

This error message occurs when the same **genvar** variable is assigned more than one time. According to the Verilog LRM this is illegal. Only one assignment to each **genvar** variable is allowed.

WHAT NEXT

Rewrite the Verilog RTL code so that there is only one assignment to each **genvar** variable.

SEE ALSO

elaborate(2)
read(2)

ELAB-953 (error) %s Array of scopes '%s' cannot be referenced without an index.

DESCRIPTION

This error message occurs when your Verilog RTL code contains a hierarchical reference to an object inside a generate loop scope. The hierarchical reference must specify which iteration of the for loop it refers to. This is accomplished by subscripting the for loop scope name with the value of the **genvar** variable specific to this loop iteration, as shown in the following example:

```
module m (y);
  output [0:3] y;
  genvar i;

  generate
    for (i=0; i<4; i=i+1) begin : blk
      wire t;
    end
  endgenerate

  assign y = blk[1].t;    // subscript 'blk' with genvar value '1'
endmodule
```

WHAT NEXT

Rewrite your Verilog RTL code so that the hierarchical name uses subscripts to access specific generate loop iterations.

SEE ALSO

elaborate(2)
read(2)

ELAB-954 (warning) %s Nonstandard generate block outside of

generate conditional or generate loop.

DESCRIPTION

This warning message occurs because the Verilog standard no longer permits generate blocks that do not belong to the branches of a generate conditional or a generate loop.

Presto Verilog still handles singleton generate blocks for backward compatibility, but other tools may not.

The following example shows a singleton generate block that causes this warning message:

```
module m ();

 begin : blk    // deprecated singleton generate block
 end

end
```

WHAT NEXT

This is only a warning message.

You can eliminate this warning message by using a generate block that is associated with a generate conditional or a generate loop.

SEE ALSO

elaborate(2)
read(2)

ELAB-955 (warning) %s State register '%s': changing state encoding from gray to binary.

DESCRIPTION

This warning message indicates that the requested FSM encoding style "gray" cannot be implemented because the number of states is not a power of 2. In this case the encoding is changed to binary.

WHAT NEXT

This is only a warning message. The state machine will still be implemented, but with binary encoding.

SEE ALSO

elaborate(2)
read(2)

ELAB-956 (Warning) %s Unknown FSM encoding '%s' requested.

DESCRIPTION

You are receiving this warning message because you set the Presto option "hdlin_force_fsm_encoding" to an unknown value. The permitted values are: one_hot, binary, gray, none.

In case of an unknown value, the value 'none' is assumed.

WHAT NEXT

Change the value of the option "hdlin_force_fsm_encoding" to one of the permitted values.

SEE ALSO

elaborate (2), **read** (2).

ELAB-957 (Error) %s Generate construct not inside generate region.

DESCRIPTION

You are receiving this error message because the Verilog standard requires that generate constructs must occur inside a generate region (generate regions are indicated by the keywords 'generate...endgenerate'). The generate construct at the indicated source location is not inside a generate region.

WHAT NEXT

Add a generate region, by surrounding generate constructs with the keywords 'generate...endgenerate'.

SEE ALSO

elaborate (2), **read** (2).

ELAB-958 (Error) %s Generate loop requires named begin block.

DESCRIPTION

You are receiving this error message because the Verilog 2001 standard requires that loop generate constructs contain a named begin block. Your RTL either does not contain a begin block or the begin block is not named. Please note that the 2005 update of the Verilog standard all

WHAT NEXT

Add a named block to the loop generate construct.

SEE ALSO

elaborate (2), **read** (2).

ELAB-959 (error) %s Illegal value assigned to a genvar variable.

DESCRIPTION

This error message occurs when any bit of of a genvar variable is set to an X or Z. Genvar values with X or Z are not supported in Synthesis.

WHAT NEXT

Rewrite the Verilog RTL code such that genvar variables are assigned legal values and try again.

SEE ALSO

elaborate(2)
read(2)

ELAB-960 (error) %s Constant value not supported in given context.

DESCRIPTION

This error message occurs when any bit of a constant value is an X or Z, and the context in which it is used does not allow for such values in the constant.

WHAT NEXT

Rewrite the Verilog RTL code such that the constant value does not evalutate to bits with X or Z, and try again.

SEE ALSO

elaborate(2)
read(2)

ELAB-961 (error) %s Constant expression (%s) not supported in given context.

DESCRIPTION

This error message occurs the reported operation is not supported in evaluation context.

WHAT NEXT

Rewrite the Verilog RTL code such that the reported operation does not happen in the given context, and try again.

SEE ALSO

elaborate(2)
read(2)

ELAB-968 (error) %s The width=%s of the indexed part-select is less than 1.

DESCRIPTION

You receive this message because the width of the indexed part-select is not at least 1.

WHAT NEXT

Modify code to resolve this issue.

/TH messages n "Sept 2002"

ELAB-971 (error) %s Assignment of NULL waveforms not supported

You receive this error when you assign a null waveform to a signal. This is currently not supported by the tool.

Make sure you do not have any such statements in your code. Assign proper i.e. non-null value to a signal.

elaborate (2), **read** (2).

/TH messages n "Sept 2002"

ELAB-972 (error) %s Construct %s.%s not supported

This error is seen if the package/Unit definition is not present.

In case of Package definition missing you must replace the code that makes use of this package by one that uses packages that have already been defined.

elaborate (2), **read** (2).

ELAB-973 (error) %s Only selected types are supported for generics.

DESCRIPTION

Currently only the following types are supported for generics:

Integer, std_logic_vector, std_logic, bit, bit_vector.

WHAT NEXT

Change the source code to remove the usage of the generics types that are not supported.

SEE ALSO

elaborate (2), **read** (2).

ELAB-974 (warning) %s Netlist for always_comb block contains a latch%s.

DESCRIPTION

This warning message occurs during **read** or **elaborate** command activity to advise you that a latch is inferred for an always_comb block.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

If combinational logic is intended, you can rewrite the always_comb block.

If combinational logic is not intended, you can remove the always_comb keyword.

SEE ALSO

elaborate(2)
read(2)

ELAB-975 (warning) %s Netlist for always_latch block does not contain a latch.

DESCRIPTION

This warning message occurs during **read** or **elaborate** command activity to advise you that the netlist for an always_latch block does not contain a latch. This may be because the always_latch block represents combinational logic or because all latches could be optimized away.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

If latched logic is intended, determine whether the body of the always_latch block represents latched logic. If it does not, then a design problem in the always_latch block has been detected. However, if the always_latch block does represent latched logic, then a coding simplification opportunity may have been detected.

If latched logic is not intended, you can replace the always_latch keyword.

SEE ALSO

elaborate(2)
read(2)

ELAB-976 (warning) %s Netlist for always_ff block does not

contain a flip-flop.

DESCRIPTION

This warning message occurs during **read** or **elaborate** command activity to advise you that the netlist for an always_ff block does not contain a flip-flop. This may be because the always_ff block does not actually represent sequential logic or because all of the flip-flops could be optimized away.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

If sequential logic is intended, determine whether the body of the always_ff block represents sequential logic. If not, then a design problem in the always_ff block has been detected. However, if the always_ff block does represent sequential logic, then a coding simplification opportunity may have been detected.

If sequential logic is not intended, you can replace the always_latch keyword.

SEE ALSO

elaborate(2)
read(2)

ELAB-977 (warning) %s Netlist for always_latch block contains a flip-flop.

DESCRIPTION

This warning message occurs during **read** or **elaborate** command activity to advise you that a flip-flop is inferred for an always_latch block.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

If latched logic is intended, you can rewrite the always_latch block.

If latched logic is not intended, you can replace the always_latch keyword. Complete your changes and run the command again.

SEE ALSO

elaborate(2)
read(2)

ELAB-978 (warning) %s Netlist for always_ff block contains a latch.

DESCRIPTION

This warning message occurs during **read** or **elaborate** command activity to advise you that a latch is inferred for an always_ff block.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

If sequential logic is intended, you can rewrite the always_ff block.

If sequential logic is not intended, you can replace the always_ff keyword.

SEE ALSO

elaborate(2)
read(2)

ELAB-979 (warning) %s Netlist for always_comb block contains a flip-flop.

DESCRIPTION

This warning message occurs during **read** or **elaborate** command activity to advise you that a flip-flop is inferred for an always_comb block.

WHAT NEXT

This is only a warning message. You can eliminate the warning message by following the instructions below.

If combinational logic is intended, you can rewrite the always_comb block.

If combinational logic is not intended, you can remove the always_comb keyword.

SEE ALSO

elaborate(2)
read(2)

ELAB-980 (error) %s Real type signal is not supported.

DESCRIPTION

This error message occurs because the Presto HDL Compiler does not support the real type signal. Currently, only the real type constant is supported.

WHAT NEXT

Declare a real type constant instead of the real type signal, and run the command again.

SEE ALSO

elaborate(2)
read(2)

ELAB-981 (error) %s Real type variable is not supported.

DESCRIPTION

This error message occurs because the Presto HDL Compiler does not support the real type variable. Currently, only the real type constant is supported.

WHAT NEXT

Declare a real type constant instead of the real type variable, and run the command again.

SEE ALSO

elaborate(2)
read(2)

ELAB-982 (warning) %s Netlist for always_comb block is

empty.

DESCRIPTION

This warning message occurs during **read** or **elaborate** command activity to advise you that no logic is inferred for an always_comb block, because none of the signals driven from that block are needed to compute the outputs of the module. For example:

```
module test(input  logic in,
            output logic out);
logic tmp;
assign out = in ;
always_comb begin
    tmp = in;
end
endmodule
```

WHAT NEXT

If combinational logic is intended, determine whether the body of the always_comb block represents combinational logic. If not, then a design problem in the always_comb block has been detected.

However, if the always_comb block does represent combinational logic, then either the signals driven by this block are not connected as intended or a coding simplification opportunity has been detected and the always_comb block can be removed.

SEE ALSO

elaborate(2)
read(2)

ELAB-983 (warning) %s Netlist for always_latch block is empty.

DESCRIPTION

This warning message occurs during **read** or **elaborate** command activity to advise you that no logic is inferred for an always_latch block, because none of the signals driven from that block are needed to compute the outputs of the module. For example:

```
module test(input  logic clk,
            input  logic in,
            output logic out);
logic tmp;
always_latch begin
  if(clk)
```

```
    tmp <= in;
end
endmodule
```

WHAT NEXT

If latched logic is intended, determine whether the body of the always_latch block represents latched logic. If not, then a design problem in the always_latch block has been detected.

However, if the always_latch block does represent latched logic, then either the signals driven by this block are not connected as intended or a coding simplification opportunity has been detected and the always_latch block can be removed.

SEE ALSO

elaborate(2)
read(2)

ELAB-984 (warning) %s Netlist for always_ff block is empty.

DESCRIPTION

This warning message occurs during **read** or **elaborate** command activity to advise you that no logic is inferred for an always_ff block, because none of the signals driven from that block are needed to compute the outputs of the module. For example:

```
module test(input  logic clk,
            input  logic in,
            output logic out);
logic tmp;
always_ff @(posedge clk) begin
    tmp <= in;
end
endmodule
```

WHAT NEXT

If sequential logic is intended, determine whether the body of the always_ff block represents sequential logic. If not, then a design problem in the always_ff block has been detected.

However, if the always_ff block does represent sequential logic, then either the signals driven by this block are not connected as intended or a coding simplification opportunity has been detected and the always_ff block can be removed.

SEE ALSO

elaborate(2)
read(2)

ELAB-985 (warning) %s Netlist for always block is empty.

DESCRIPTION

This warning message occurs during **read** or **elaborate** command activity to advise you that no logic is inferred for a SystemVerilog always block with an implicit or explicit sensitivity list, because none of the signals driven from that block are needed to compute the outputs of the module. For example:

```
module test(input  logic in,
            output logic out);
logic tmp;
assign out = in ;
always @* begin
    tmp = in;
end
endmodule
```

WHAT NEXT

Either the signals driven by this block are not connected as intended or a coding simplification opportunity has been detected and the always block can be removed.

SEE ALSO

elaborate(2)
read(2)

ELAB-989 (error) %s Packed union members must be of the same size.

DESCRIPTION

You receive this error message because a packed union has been declared with members of different sizes. The *Language Reference Manual* (LRM) specifies that "A packed union shall contain members that must be packed structures, or packed arrays or integer data types all of the same size".

For example:

```
module test #(parameter OFFSET_BITSIZE = 16,
              parameter PAGE_BITSIZE = 16);
  union packed {
    int numeric;
    struct packed {
      bit [OFFSET_BITSIZE-1:0] offset;
      bit [PAGE_BITSIZE-1:0] page;
    } vaddress;
  } one_union;
endmodule
```

If the module test is going to be instantiated with parameter values other than the defaults, they must add 32, in order for the bit width of the packed structure vaddress to be of the same size than the integer numeric (32).

WHAT NEXT

Modify your source file so that all union members have the same bit width.

ELAB-990 (error) %s Width of distributed port expression does not equal width of declared type of structure of instances.

DESCRIPTION

You receive this message because a distributed port expression, such as .p(<expr>), in a structure of instances does not have the same number of bits as the type declared for the structure of instances.

WHAT NEXT

Modify code so that the distributed port expression has the same number of bits as the declared type of the structure of instances.

ELAB-991 (warning) %s The type of a <distributed port expression> is not equivalent to the structured <type> of these instances.

DESCRIPTION

You receive this message because a distributed port expression, such as .p(<expr>) in a structure of instances, does not have the declared type for the structure of instances. For example, the type declared for the structure of instances might be a packed structure, while the type of the distributed port expression might be a simple bit-vector type of the same length.

WHAT NEXT

If the expression bit width of each distributed port matches the number of instances, they will be distributed anyway. However, as a precaution, you should examine the RTL code to make sure that the distributed port expression's type is actually intended to align with the instance structure in a bit-streamed order. If so, consider using an explicit cast of the port expression to clarify that this is what you intend.

ELAB-992 (error) %s The lhs width=%s does not match the rhs width=%s of the assignment statement.

DESCRIPTION

You receive this message because the assignment statement has a width mismatch problem.

WHAT NEXT

Modify code to resolve this issue.

ELAB-993 (warning) %s Synthesis/simulation mismatch for multiplier.

DESCRIPTION

You receive this error message because the multiplier is optimized assuming no result truncation. Verilog/VHDL semantics require result truncation to be taken into account. In most cases assuming no result truncation results result in the intended behaviour and better QOR. If the design relies on multiplier truncation, this message indicates bad logic. When you see this message, there may be a synthesis/ simulation mismatch.

Strict Verilog/VHDL semantics can be forced by setting the following option:

```
set hdlin_idxopt_optimize_mul false
```

This will resolve the synthesis/simulation mismatch, but can result in QOR degradation.

WHAT NEXT

Modify code to reolve this issue.

ELAB-994 (warning) %s Found an unknown pragma '%s'; it will be ignored.

DESCRIPTION

You receive this warning message from the **elaborate** or **read** command, if there is an unknown pragma. The unknown pragma will be ignored.

WHAT NEXT

Check the spelling of the unknown pragma and correct it if necessary; otherwise consider to remove the unknown pragma.

SEE ALSO

elaborate (2), **read** (2).

ELAB-995 (error) %s Real to integer conversion is not supported.

DESCRIPTION

This error message occurs because the Presto HDL Compiler does not support the real to integer conversion currently.

WHAT NEXT

Modify the code to remove the error source.

SEE ALSO

elaborate(2)
read(2)

ELAB-996 (error) %s WAIT statement inside FOR loop is not supported.

DESCRIPTION

This error message occurs because the Presto HDL Compiler does not support WAIT statements inside FOR loops.

WHAT NEXT

Modify the code to remove the error source.

SEE ALSO

elaborate(2)
read(2)

ELAB-997 (error) %s Multidimensional part-select is not supported.

DESCRIPTION

This error message occurs because the Presto HDL Compiler does not support part-select operators (+: and -:) with multidimensional arrays.

WHAT NEXT

Modify the code to remove the error source.

SEE ALSO

elaborate(2)
read(2)

ELAB-998 (error) %s The rhs width does not match the lhs width of the logical operator statement.

DESCRIPTION

You receive this message because the logical operator statement has a width mismatch problem.

WHAT NEXT

Modify code to resolve this issue.

ELAB-999 (error) %s Width of actual parameter does not match

the formal parameter '%s'.

DESCRIPTION

You received this error message because width of the actual parameter does not match the mismatch the actual parameter, given by module/component instantiation or by elaborate command.

WHAT NEXT

Modify formal or actual parameter type to match the width.

ELAB-1000 (error) %s Overflow in a conversion of a real type number: %s.

DESCRIPTION

You receive this message because there is an overflow in a conversion of a real type number.

WHAT NEXT

Modify code to resolve this issue.

ELAB-1001 (error) %s Overflow in a real type number or calculation.

DESCRIPTION

You receive this message because there is an overflow in a real type number or calculation. The number/result is greater than REAL'HIGH = 1.0e+38 or smaller than REAL'LOW = -1.0e+38.

WHAT NEXT

Modify code to resolve this issue.

ELAB-1002 (warning) %s Real types with ranges are not

supported and will be ignored.

DESCRIPTION

You receive this message because there is a real type with a range defined. This is not supported. A real type without ranges will be used.

WHAT NEXT

This is a warning message only. No action is required.

However, be aware the portion of the design that involves real types with ranges could behave differently.

ELAB-1010 (error) %s Complex usage of multiple events statements is not supported.

DESCRIPTION

This error message occurs because the Presto HDL Compiler does not support complex multiple events in an verilog always block or a VHDL process.

WHAT NEXT

Modify the code to have only one event per always or process.

SEE ALSO

elaborate(2)
read(2)

ELAB-1011 (warning) %s Comparison operator always returns '%s' when comparing values with different widths.

DESCRIPTION

This warning message occurs when the tool detects that there is a comparison with values of different width which evaluates always as unequal.

This can result in never reached statements within a comparison branch.

WHAT NEXT

Resolve the potential problem.

SEE ALSO

elaborate (2), **read** (2).

ELAB-1012 (error) %s The width (%d %s) is too big.

DESCRIPTION

This error message occurs when the tool detects a width that exceeds the supported range.

WHAT NEXT

Decrease the used width and run the command again.

SEE ALSO

elaborate(2)
read(2)

ELAB-1013 (error) %s PORT/GENERIC declaration in BLOCK header is not supported.

DESCRIPTION

Declaration and use of generics and ports in a block header is not supported.

WHAT NEXT

Remove port and generic declarations from the block header and adapt the block statements if necessary.

SEE ALSO

elaborate (2), **read** (2).

ELAB-1014 (warning) %s The lhs width=%s does not match the

rhs width=%s of the comparison.

DESCRIPTION

This warning message occurs when the tool detects that there is a comparison with values of different widths.

WHAT NEXT

Correct the widths so that they are the same and run the command again.

SEE ALSO

elaborate(2)
read(2)

ELAB-1015 (warning) %s Ignoring SystemVerilog checker '%s' instantiation: '%s'.

DESCRIPTION

This warning message occurs when the SystemVerilog *checker* construct and its instantiations are ignored.

WHAT NEXT

This is only a warning message. No action is required.

SEE ALSO

elaborate(2)
read(2)

ELAB-1016 (error) %s Port %s is not declared by this module or interface.

DESCRIPTION

This error message occurs when a port name used in a module or interface instantiation, or used in an **elaborate -parameter** command and argument is not declared as a port by that module or interface.

In the following example, the *foo* module is instantiated with a named port connection. It uses the named ports *a*, *o* and *state*. However, *state* is not in the port list definition of the *foo* module, so the error message occurs.

```
module E (a, out1, state);
input [2:0] a;
output [3:0] out1;
output state;
foo U1 (.a(a), .o(out1), .state(state));
endmodule

module foo(input [2:0] i, output [3:0] o, output status);
endmodule
```

WHAT NEXT

Correct the names of the ports so that they are consistent with the module definition, and then invoke the compiler again.

SEE ALSO

elaborate(2)
link(2)

ELAB-1060 (error) %s Symbol '%s' results in multiple objects.

DESCRIPTION

The named symbol results in creation of objects that conficts with each other. The most likely cause of this error is importing of symbols from interfaces or classes into a module. During the import phase, homographs are created that in most cases can be automatically resolved, however in some cases such as this, automatic resolution is not possible.

WHAT NEXT

Look for ELAB-106 warnings for the symbol in question, and rename or resolve the homographs.

SEE ALSO

ELAB-106 (n),

ELAB-2000 (error) %s Incorrect value for hdlin_infer_ram: '%s';

possible values are ’all’, ’default’, or ’none’.

DESCRIPTION

Allowed values for the **hdlin_infer_ram** variable are *all*, *none*, and *default*. When *all* is the value, HDL Compiler attempts to infer a RAM_OP for a 2-dimensional register. When *none* (the default value) is the value, HDL Compiler does not attempt to infer any RAM_OPs for a Verilog or VHDL design.

When *default* is the value, HDL Compiler attempts to infer a RAM_OP for a 2-dimensional register, only if the register is marked with the **infer_ram** directive,

For details, see the *HDL Compiler for Verilog Reference Manual* or the *VHDL Compiler Reference Manual*.

To determine the current value of this variable, type **list hdlin_infer_ram**. For a list of hdl variables and their current values, type **list -variables hdl**.

WHAT NEXT

Set **hdlin_infer_ram** to one of the values *all*, *default*, or *none*.

SEE ALSO

elaborate (2), **read** (2), **hdlin_infer_ram** (3).

ELAB-2001 (warning) %s Ignored infer_ram pragma value ’%s’ on register ’%s’.

DESCRIPTION

You receive this message because, during **elaborate** or **read** command activity, the compiler has detected invalid synopsys infer_ram pragma value on the memory element.

Currently supported values are none, auto, distrubuted and no_rw_check. These values specify the implementation of memory.

For details, see the *HDL Compiler for Verilog Reference Manual* or the *VHDL Compiler Reference Manual*.

SEE ALSO

elaborate (2), **read** (2), **hdlin_infer_ram** (3).

ELAB-2002 (warning) %s The design '%s' has no parameters. The parameters '%s' has been ignored.

DESCRIPTION

You receive this message because, during **elaborate** or **read** command activity, the compiler has detected that cell has be instantiated with the parameter. But the down design to which this cell is linked does not take any parameters.

SEE ALSO

elaborate (2), **read** (2).

ELAB-2004 (warning) %s Signal %s has %s attribute, but is %s. A possible mismatch of attribute and behavior.

DESCRIPTION

You receive this warning message because one_hot signal is used in an active low situation while one_hot attribute indicates the signal should be active high, or a one_cold signal is used in an active high situation while one_cold attribute indicates the signal should be active low.

This warning reminds the designer to keep the attribute of the signal consistent with the behavior of the signal.

WHAT NEXT

This is a only a warning and requires no action on your part.

ELAB-2008 (information) %s Complex logic will not be considered for set/reset inference.

DESCRIPTION

You receive this information when, during **elaborate** or **read** command activity, some possible set/reset logics have been excluded from consideration for set/reset inference, because they were estimated to be too complex, for example, because they were driven by another instance.

If the hdlin_infer_complex_set_reset is set to TRUE, if the control logic is complex and that drives the data pin of register to zero, the control logic gets moved to

the reset line;and any control logic that drives the data pin to one, gets moved to the set line. And if hdlin_infer_complex_set_reset is set to FALSE (default), no complex control logic gets moved to the set/reset lines and it will stay on the data line.

Usually excluding these complex possibilities leads both to better quality of result and to better runtime. Hence this message is not a warning, but only informational. Occasionally, however, the designer knows reasons why it would be good for the compiler to consider additional, more complex, possibilities. When this is so, it can be communicated to the compiler by overriding to true the default value of the hdlin_infer_complex_set_reset variable.

SEE ALSO

elaborate (2), **read** (2), **hdlin_infer_complex_set_reset** (3).

ELAB-2010 (error) %s Size mismatch in the assignment.

DESCRIPTION

This error message occurs when right hand side of the assignment is not the same as left hand size.

WHAT NEXT

Fix the offending assignment and try again.

SEE ALSO

elaborate (2), **read** (2).

ELAB-2015 (warning) %s illegal tristate driver '%s' on the wired types. may cause simulation/synthesis mismatch.

DESCRIPTION

You receive this message because Output of the tristate is used to drive more than one wired net. These nets may be driven directly by the tristate, or might be driven indirectly through another wired net.

WHAT NEXT

Check the assignments on wired type, to fix the error

ELAB-2016 (error) %s Found illegal tristate driver/drivers on the wired types.

DESCRIPTION

You receive this message because Output of the tristate is used to drive more than one wired net. These nets may be driven directly by the tristate, or might be driven indirectly through another wired net. To overide this error message set hdlin_error_illegal_driver_on_wired_type to FALSE. Overring this error might cause

WHAT NEXT

To overide this error message set hdlin_error_illegal_driver_on_wired_type to FALSE. Overring this error might cause simulation/synthesis mismatch.

ELAB-2017 (warning) %s Ignoring ’infer_onehot_mux’ pragma because case not marked %s.

DESCRIPTION

You receive this message because the case statement marked as "infer_onehot_mux" is not marked as "full_case" or "parallel_case". Both pragmas "full_case" and "parallel_case" are required for the "infer_onehot_mux" pragma to be honored by the compiler.

WHAT NEXT

Make sure the case statement is really "full" and "parallel", then add the "full_case" and "parallel_case" pragmas to the "infer_onehot_mux" pragma.

ELAB-2018 (error) %s Conflicting pragmas ’%s’ and ’%s’ cannot be applied simultaneously.

DESCRIPTION

You receive this message because you applied to conflicting pragmas simultaneously. The pragmas are either conflicting or the tool does not support the application of both pragmas.

WHAT NEXT

Keep the pragma that was intended to be used and remove the conflicting other pragma.

ELAB-2020 (error) %s %s.

DESCRIPTION

This error message occurs when Presto VHDL detects the following semantic error when running the **analyze** command.

WHAT NEXT

Fix the error and reanalyze this file.

SEE ALSO

elaborate(2)
read(2)

ELAB-2024 (warning) %s Clock %s used as data.

DESCRIPTION

You receive this warning message because Presto HDL Compiler detected clock signals used for purposes other than clocking.

WHAT NEXT

Modify the design to avoid using clock for purposes other than clocking.

SEE ALSO

elaborate (2), **read** (2).

ELAB-2025 (error) %s Call to impure function '%s' is not

supported.

DESCRIPTION

You receive this error message because Presto VHDL does not support calls to Impure functions.

SEE ALSO

elaborate (2), **read** (2).

ELAB-2028 (error) %s Default value of the sized parameter '%s' has been overridden with an expression whose self-determined type is not as wide as the parameter.

DESCRIPTION

You receive this warning message when the default value of a sized parameter '%s' has been overridden with an expression whose self-determined type is not as wide as the parameter.

In synthesis the expression used in a parameter override is evaluated in a self-determined context, so in the following example, parameter P in the instantiation "bot1" is overridden with an expression that is evaluated with 1-bit width precision.

But in simulation, because the width of the sized parameter P in the module BOT is 2, the expression would be evaluated with 2-bit width precision. As in this example, the difference in precision can lead to different results between simulation and synthesis.

```
`define E 1'b1 + 1'b1
module TOP (output test_bit);
  wire [1:0] w1, w2;
  assign test_bit = (w1 == w2);
  BOT#(.P(`E)) bot1(w1);
  BOT bot2(w2);
endmodule

module BOT #(parameter [1:0] P = `E) (output [1:0] o);
  assign o = P;
endmodule
```

WHAT NEXT

Either reduce the size of the parameter or override the parameter with an expression whose self-determined type is as least as wide as the parameter.

ELAB-2029 (warning) %s Default value of the sized parameter '%s' has been overridden with an expression whose self-determined type is not as wide as the parameter.

DESCRIPTION

You receive this warning message when the default value of a sized parameter '%s' has been overridden with an expression whose self-determined type is not as wide as the parameter.

In synthesis the expression used in a parameter override is evaluated in a self-determined context, so in the following example, parameter P in the instantiation "bot1" is overridden with an expression that is evaluated with 1-bit width precision.

But in simulation, because the width of the sized parameter P in the module BOT is 2, the expression would be evaluated with 2-bit width precision. As in this example, the difference in precision can lead to different results between simulation and synthesis.

```
`define E 1'b1 + 1'b1
module TOP (output test_bit);
  wire [1:0] w1, w2;
  assign test_bit = (w1 == w2);
  BOT#(.P(`E)) bot1(w1);
  BOT bot2(w2);
endmodule

module BOT #(parameter [1:0] P = `E) (output [1:0] o);
  assign o = P;
endmodule
```

WHAT NEXT

Either reduce the size of the parameter or override the parameter with an expression whose self-determined type is as least as wide as the parameter.

ENV-001 (error) Value for %s cannot be larger than the %s value.

DESCRIPTION

Some commands work in pairs, specifying a max and min value. The min value must be less than the max value. For example, never specify a **min_capacitance** which is larger than the **max_capacitance** for the same design or port.

WHAT NEXT

Remove the old value or use a different value.

ENV-1 (error) Variable '%s' is not defined.

DESCRIPTION

WHAT NEXT

ENV-002 (warning) Invalid value '%s' for variable '%s'. %s

DESCRIPTION

You received this message because you specified an invalid value for the specified variable. The message should provide valid values for the variable.

WHAT NEXT

If the message did not provide valid values for the variable, refer to the manual page for the variable. Reset the variable with a valid value, then reexecute the command.

ENV-003 (Information) Using automatic %s wire load selection

group ’%s’%s.

DESCRIPTION

Automatic wire load selection by area is being performed on the design or on a hierarchical cell. The specified selection group is used to determine which wire load model to apply to hierarchical cells at and below this cell or design, based on their cell area. There might be a different selection group for max and min conditions.

WHAT NEXT

To see which wire load models are set, you can use the **report_wire_load** command.

EQN-1 (error) Undefined variable on or near line %d at or near ’%s’.

DESCRIPTION

WHAT NEXT

EQN-2 (error) Undefined operator on or near line %d at or near ’%s’.

DESCRIPTION

This error is generated when an undefined operator or command has been specified.

WHAT NEXT

Check for a spelling error in the command name and reinvoke the command. Type "list -commands" to see a list of the available commands.

EQN-3 (error) Incorrect number of operands on or near line %d at or near ’%s’.

DESCRIPTION

WHAT NEXT

EQN-4 (error) Operator can not process operand of this type on or near line %d at or near ’%s’.

DESCRIPTION

This error is generated when the operand for the given operator can not accept the given operand.

WHAT NEXT

Check and correct operands, then reissue the current command.

Comparison Operators: ==, !=, <, <=, >, >= takes two operands from float, integer, string, and list. Arithmetic Operators: *, / takes two operands from float and integer. Special arithmetic Operator plus: + takes two operands from float, integer, string, and lists. Arithmetic operator minus: - takes two operands from float, integer, and list. Assignment Operator: '=' operator in a = b, a and b must be the same operand type and can be float, integer, string, and list. Redirect operators: > and >>. For example a > b where operand a is a string expression and b is a file name.

EQN-5 (error) Evaluation error on or near line %d at or near '%s'.

DESCRIPTION

WHAT NEXT

EQN-6 (error) Internal error.

DESCRIPTION

WHAT NEXT

EQN-7 (error) Evaluation error on or near line %d at or near '%s'.

DESCRIPTION

WHAT NEXT

EQN-8 (error) Error on or near line %d at or near '%s'

DESCRIPTION

WHAT NEXT

EQN-9 (error) Operator used in bad context on or near line %d at or near ’%s’.

DESCRIPTION

WHAT NEXT

EQN-10 (warning) Defining new variable ’%s’.

DESCRIPTION

WHAT NEXT

EQN-11 (error) Could not write file ’%s’.

DESCRIPTION

WHAT NEXT

EQN-12 (error) Break statement not enclosed in loop on or near

line %d.

DESCRIPTION

WHAT NEXT

EQN-13 (error) Continue statement not enclosed in loop on or near line %d.

DESCRIPTION

WHAT NEXT

EQN-14 (error) Can’t execute command ’%s’ in this context on or near line %d.

DESCRIPTION

WHAT NEXT

EQN-15 (error) Can’t divide by zero on or near line %d at or near ’%s’.

DESCRIPTION

WHAT NEXT

EQN-16 (error) Operand must be positive on or near line %d at

or near ’%s’.

DESCRIPTION

WHAT NEXT

EQN-17 (error) The abbreviated option ’%s’ matches more than 1 argument for this command.

DESCRIPTION

This error message is generated when there is more than one options whose abbreviation is the same.

WHAT NEXT

Type command -help and look for the availability option of the command. Then reinvoke the command.

EQN-18 (error) Unexpected argument ’%s’.

DESCRIPTION

WHAT NEXT

EQN-19 (error) %s required for the ’%s’ argument.

DESCRIPTION

WHAT NEXT

EQN-20 (error) Arithmetic overflow or exception encountered.

DESCRIPTION

WHAT NEXT

EQN-21 (warning) Function ’%s’ leaked %d allocations for %d bytes.

DESCRIPTION

WHAT NEXT

EQN-22 (information) Additional information in file ’%s’.

DESCRIPTION

WHAT NEXT

EQN-23 (error) That is an invalid name for a user defined

function.

DESCRIPTION

User-function names must be simple strings or identifiers.

WHAT NEXT

Choose a different name for this user function.

EQN-24 (error) define_function cannot be used to redefine the builtin '%s' command.

DESCRIPTION

The define_function command can only be used to define new user functions. It cannot be used to change the definition of a builtin command.

WHAT NEXT

Choose a name for this user function that does not conflict with the name of a builtin command.

EQN-25 (error) The %s command cannot be used outside of a user defined function.

DESCRIPTION

The **get_parameter** command retrieves values from the invocation line of the currently executing user-defined function. It can only be used when defining a user function.

The **return** command returns values from a currently executing user-defined function. It can only be used when defining a function.

WHAT NEXT

Use this command only from within a user-defined function.

EQN-26 (error) Cannot use both -remainder and -option for the

get_parameter command on line %d.

DESCRIPTION

The "-option" option to the get_parameter command fetches a single option for the argument list. The "-remainder" option fetches the entire remaining list of parameters to this user function. These options cannot be used together.

WHAT NEXT

Decide which use is more appropriate, or use the get_parameter command twice, once with -option, once with -remainder.

EQN-27 (error) Type '%s' is not a valid variable type for %s call on line %d.

DESCRIPTION

The variable types that are acceptable for the **get_parameter** command and the **create_variable** command are *integer*, *float*, *string*, *list*, and *object*.

The **get_parameter** command also accepts the type *flag* for dash options that do not have a following value.

WHAT NEXT

Use one of the predefined variable types.

EQN-28 (error) Variable '%s' cannot be redefined by %s on line %d.

DESCRIPTION

The **get_parameter** command returns the user function parameter value in a newly created local variable. The **get_parameter** command cannot be used to change an existing local variable.

The **create_variable** command creates a new variable either globally or locally to a user function. **create_variable** cannot be used to overwrite an existing variable.

WHAT NEXT

Choose a different name for the variable that returns the parameter value, or remove the variable from the local scope by using the **remove_variable** command before calling **get_parameter**.

Call **remove_variable** to remove the previous definition of the variable before creating a new one with **create_variable**.

EQN-29 (error) A value is required for the '%s' option of user function '%s' on line %d. get_parameter call on line %d fails.

DESCRIPTION

Most parameters to user functions are of the form -*option value*. It is an error to specify the option -*option* without following it with the option value *value*.

WHAT NEXT

Call the user function with the value following the option.

EQN-30 (error) Argument %s is required for calls to user function '%s' on line %d. get_parameter call on line %d fails.

DESCRIPTION

Required parameters to a user function are defined using **get_parameter** without the -*default* option. If the defined parameter is not present when calling the user-defined function, this error occurs.

WHAT NEXT

Call the user function with the required parameter. Or redefine the user function making this parameter's options by using the -*default* option to **get_parameter**.

EQN-31 (error) Cannot convert value %s to type %s, %s call on

line %d.

DESCRIPTION

The value given to the user function call cannot be converted to the type specified in the **get_parameter** or **create_variable** command.

WHAT NEXT

When calling the user function, use the correct type for that option. When creating variables, try not to use type conversion for the variable's initial value.

EQN-32 (error) User function "%s

DESCRIPTION

The user function identified is not currently defined.

WHAT NEXT

Either the function has not yet been defined, the given function name was typed incorrectly, or the function is a built-in command.

EQN-33 (error) Specify only one of -local and -global.

DESCRIPTION

A variable can only be removed from one scope at a time. The **remove_variable** command can accept an argument of *-local* to remove a variable local to the current executing function or *-global* to remove a variable from the global variable list. By default, the command first checks the local variable list, then checks the global variable list.

The **variable_exists** command normally checks the local scope first (if currently in a user-defined function), then the global scope. Defining both *-local* and *-global* is redundant.

WHAT NEXT

Try the command without using either the *-local* or *-global* options, or just use one option.

EQN-34 (error) Variable %s not defined in %s scope.

DESCRIPTION

The defined variable was not found in the named scope (local or global). Either the **remove_variable** command was invoked with the incorrect scope flag (*-local* or *-global*) or the variable does not exist in the scope.

WHAT NEXT

Try removing the variable from the other scope. Perhaps the variable was never created, or it had already been removed.

EQN-35 (error) Variable %s not defined.

DESCRIPTION

The named variable is not defined.

WHAT NEXT

Perhaps the variable was never created, or perhaps it had already been removed.

EQN-36 (error) Variable '%s' is protected.

DESCRIPTION

This variable was defined in the system **synopsys_dc.setup** file. These system variables are protected and cannot be removed.

WHAT NEXT

Use another variable.

EQN-37 (error) Specify either a default value, or a variable type.

DESCRIPTION

The **create_variable** command determines what type of variable to create by using the given type, or by using the same type as the initial value for the variable. One of

these two options must be defined.

WHAT NEXT

Use the *-type* option to **create_variable**, or define an initial value.

EQN-38 (error) Cannot list builtin command '%s'.

DESCRIPTION

The **list_function command cannot list built-in commands.**

WHAT NEXT

Use the **list_function** command only on user-defined functions.

EQN-39 (error) Cannot remove builtin command '%s'.

DESCRIPTION

The **remove_function** command cannot remove built-in commands.

WHAT NEXT

Use the **remove_function** command only on user-defined functions.

EQN-40 (warning) Undefined command name '%s' encountered.

DESCRIPTION

WHAT NEXT

EQN-41 (warning) Syntax or context checking is not supported

for ’%s’.

DESCRIPTION

This message indicates that the syntax or context checking is not supported for this user-defined function created by the define_funtion command.

WHAT NEXT

EQN-42 (error) Argument ’%s’ has been specified more than once.

DESCRIPTION

You have specified an argument multiple times, when only one is allowed.

WHAT NEXT

Remove the redundant argument.

Sometimes this error can occur as a result of command aliasing. If you can only see one specification of the argument, try using the alias command to see whether your command has an alias which includes the extra argument. If so, you can use the unalias command to remove the alias.

EQNI

EQNI-1 (error) Illegal left hand side at line %d.

DESCRIPTION

WHAT NEXT

EQNI-2 (error) Illegal function at line %d.

DESCRIPTION

WHAT NEXT

EQNI-3 (error) Invalid use of '?' in token '%s' at line %d.

DESCRIPTION

WHAT NEXT

EQNI-4 (error) Design name must be specified at line %d.

DESCRIPTION

WHAT NEXT

EQNI-5 (error) Signal ?%s set a second time at line %d.

DESCRIPTION

WHAT NEXT

EQNI-6 (error) Signal %s set a second time at line %d.

DESCRIPTION

WHAT NEXT

EQNI-7 (error) Invalid use of ’?’ in input ’%s’.

DESCRIPTION

WHAT NEXT

EQNI-8 (error) Port %s declared twice at line %d.

DESCRIPTION

WHAT NEXT

EQNI-9 (error) Invalid use of ’?’ in output ’%s’.

DESCRIPTION

WHAT NEXT

EQNI-10 (warning) Unknown command "%s

DESCRIPTION

WHAT NEXT

EQNI-11 (error) Can’t read file "%s

DESCRIPTION

WHAT NEXT

EQNO

EQNO-0 (error) Invalid design to write out as equations.

DESCRIPTION

WHAT NEXT

EQNO-1 (error) Cannot write out design with non-combinational cell(s).

DESCRIPTION

WHAT NEXT

EQNO-2 (error) Cannot write out design with INOUT ports.

DESCRIPTION

WHAT NEXT

EQNO-3 (error) Cannot write out design with ports with unknown direction.

DESCRIPTION

WHAT NEXT

EQNO-4 (warning) The value of variable ’equationout_%s’ isn’t

valid--using ’%s’.

DESCRIPTION

WHAT NEXT

EST-1 (warning) The ’%s’ command is not supported by Estimator. The command is skipped.

DESCRIPTION

The command listed in this error message is not supported by Estimator. Estimator prints this warning message and skips the command. The command does not affect the execution of Estimation.

WHAT NEXT

No action by user is required.

EST-2 (Error) Estimator cannot proceed without an Estimation license.

DESCRIPTION

An Estimation license ought to have been checked out before reaching this point in the execution. But a license check determined that the Estimation license was not checked out.

WHAT NEXT

Check your license server. Report problem to Synopsys Hotline / Support Center.

EST-3 (Error) Invalid value ’%s’ for the ’estimate_resource_preference’ variable.

DESCRIPTION

Valid values for the ’estimate_resource_preference’ variable are "fast" and "small". The default is "fast".

WHAT NEXT

Please set the ’estimate_resource_preference’ variable to a valid value and

continue.

EST-4 (Error) Invalid value '%s' for the 'estimate -resource_preference' option.

DESCRIPTION

Valid values for the '-resource_preference' option to the 'estimate' command are "fast" and "small". The default is "fast".

WHAT NEXT

Please use a valid value for the '-resource_preference' option and continue.

EST-5 (Error) The design '%s' has not been read in.

DESCRIPTION

Please read in the design before running the estimate command.

WHAT NEXT

EST-6 (Error) The current design is not defined.

DESCRIPTION

This error is generated when the current design is not defined when running the estimate command.

WHAT NEXT

Use **list_designs** commands to see whether there is any design in memory or use **read** command to read a design in. Then invoke the **current_design** command to set the desired current design.

EST-7 (error) Estimation terminated with errors.

DESCRIPTION

This message indicates that estimation was terminated and did not write the intermediate design back to the database. Because the design was not written back to the database, the **current_design** is unchanged. The explanation for abnormal termination should have appeared in an error message previous to this one.

WHAT NEXT

Resolve errors and rerun estimation.

EST-8 (error) Estimation of synthetic parts failed.

DESCRIPTION

This message indicates that the estimation of synthetic parts failed. A more detailed explanation for the failure should have appeared in an error message previous to this one.

WHAT NEXT

Resolve errors and rerun estimation.

EST-9 (error) Cannot run the '%s' command on the design '%s' because it is an estimated design.

DESCRIPTION

The current design (or one of it's sub-designs) is an estimated design - i.e. it was generated by the 'estimate' command, or it was generated by using (V)HDL Compiler functionality with only an Estimator license. Certain operations are not permitted on estimated designs. The current command is one of those unpermitted operations.

WHAT NEXT

EST-10 (Error) Estimator does not support FPGA libraries.

DESCRIPTION

Estimator does not support FPGA libraries.

WHAT NEXT

EST-11 (warning) Estimator does not support FPGA-specific Library Component optimization. FPGA-specific optimization disabled.

DESCRIPTION

This warning message occurs when your library contains components whose use requires FPGA-specific optimization. Estimation will proceed with the FPGA-specific optimization disabled.

WHAT NEXT

EST-12 (warning) The effort level for ’flattening’ was automatically reduced from ’high’ to ’medium’.

DESCRIPTION

Estimator does not allow a high effort setting for flattening. The effort level is automatically reduced to medium.

WHAT NEXT

EST-13 (warning) The design ’%s’ will be marked as an estimated design after ungrouping because one or more of its

sub-designs are estimated.

DESCRIPTION

One or more of the subdesigns of the specified design are estimated. The system needs to keep track of which designs are estimated because certain actions are allowed or disallowed on estimated designs.

When cells in a design are ungrouped, the design is marked as estimated if any of its subdesigns are estimated.

WHAT NEXT

EST-14 (error) Cannot write out an estimated design in non-db format.

DESCRIPTION

The current design (or one of its subdesigns) is an estimated design. For example, it was generated by the 'estimate' command, or it was generated by using (V)HDL Compiler functionality with only an Estimator license. Writing out of netlists is not permitted on estimated designs.

WHAT NEXT

EST-15 (warning) The gtech design generated from this HDL compilation can be used for Estimation only.

DESCRIPTION

This design was analyzed/elaborated using only an Estimator license. Since a (V)HDL Compiler License was not used, the resulting gtech design from high-level compile will be allowed as input to Estimation only. This design cannot be used as input to the compile command (Design Compiler).

WHAT NEXT

EST-16 (warning) The current design is an estimated design :

The ATPG vectors will not be saved.

DESCRIPTION

The current design is an estimated design. You may run ATPG (i.e. the create_test_patterns command) in order to estimate the fault coverage that can be obtained. However, the vectors generated by the ATPG run will not be saved.

WHAT NEXT

EST-17 (error) Illegal operation if an Estimator key is not checked out.

DESCRIPTION

The software attempted an operation which is legal only if an Estimator key is already checked out. If an Estimator key was not checked out, the software exits.

WHAT NEXT

Contact the Synopsys support line.

EST-18 (warning) Power constraints will be ignored during Estimation.

DESCRIPTION

The design has power constraints. These will not be taken into consideration during Estimation. You can analyze power (with the report_power command) on the estimated design after Estimation has completed.

Power analysis on estimated designs is supported. However, power optimization during estimation is not supported.

WHAT NEXT

No action is required. You may analyze power (with the report_power command) after Estimation has completed.

EST-19 (error) The security handshake for Estimator failed.

DESCRIPTION

This is an internal error. The security handshake between HDL Advisor and Estimator failed.

WHAT NEXT

Contact the Synopsys support line.

EST-20 (error) Cannot run Estimator stand-alone. It must be run through Chip Architect.

DESCRIPTION

Estimator can only be run after a security handshake with Chip Architect. Estimator must be run through Chip Architect. It cannot be run stand-alone.

WHAT NEXT

EXPT_7 (error) %s '%s' in design '%s' has no symbol library.

DESCRIPTION

WHAT NEXT

EXPT-1 (error) The variable '%s' isn't defined.

DESCRIPTION

WHAT NEXT

EXPT-2 (error) The variable '%s' is of an unsupported external export option type.

DESCRIPTION

WHAT NEXT

EXPT-3 (error) Unknown export format '%s'.

DESCRIPTION

This error is generated when the **write** command encounters an invalid write (export) format.

WHAT NEXT

Invoke the **write** -help command for valid write (export) formats. Identify and correct format, then reinvoke the **write** command.

EXPT-4 (error) Can’t open export file ’%s’.

DESCRIPTION

WHAT NEXT

EXPT-5 (error) Cannot execute ’%s’.

DESCRIPTION

WHAT NEXT

EXPT-6 (warning) Library ’%s’ used which wasn’t created by %s interface.

DESCRIPTION

WHAT NEXT

EXPT-8 (error) Unable to find an external scale attribute for schematic ’%s’.

DESCRIPTION

WHAT NEXT

EXPT-9 (error) The external scales in libraries ’%s’ and ’%s’

aren’t equal.

DESCRIPTION

WHAT NEXT

EXPT-10 (error) The route grids in libraries ’%s’ and ’%s’ aren’t equal.

DESCRIPTION

WHAT NEXT

EXPT-11 (information) %s name ’%s’ changed to ’%s’.

DESCRIPTION

This message is for information only and indicates that an object in the design database has had its name changed. The name change could have happened automatically (for example, if the name was not compliant with the target syntax) or manually (for example, if a user executed the **change_names** command.

WHAT NEXT

Because this is a message for information only, no further action is indicated.

EXPT-12 (information) Design ’%s’ had %d name changes.

DESCRIPTION

WHAT NEXT

EXPT-13 (error) Schematic ’%s’ was created with an invalid

setting for the variable '%s'.

DESCRIPTION

WHAT NEXT

EXPT-14 (warning) The %s name '%s' is corrupted.

DESCRIPTION

WHAT NEXT

EXPT-15 (warning) The name of net '%s' in design '%s' can't be changed to the name of both ports '%s' and '%s' to which it's connected.

DESCRIPTION

WHAT NEXT

Because multiple ports are connected to the same net, to avoid this problem, the design must be modified with the **compile** command to insert enough extra logic.

Set *compile_fix_multiple_port_nets* to *true*, execute the **compile** command, and execute the **create_schematic** command again. Then execute the edif format **write** command again. If you are going to execute the edif format **write** command with the *-hierarchy option*, be sure to execute the **create_schematic** command with the *-hierarchy* option.

For future use, set *compile_fix_multiple_port_nets* to *true* in your initialization.

EXPT-16 (error) One of the %s has no name.

DESCRIPTION

WHAT NEXT

EXPT-17 (error) The schematic is corrupted or is an old version.

DESCRIPTION

WHAT NEXT

EXPT-18 (error) %s '%s' is corrupted.

DESCRIPTION

WHAT NEXT

EXPT-19 (error) Schematic '%s' was created with incompatible values for the variables '%s'
and '%s'.

DESCRIPTION

WHAT NEXT

EXPT-20 (error) Ripper symbol '%s' in library '%s'
is corrupted; it does not have the attribute 'ripped_pin'.

DESCRIPTION

WHAT NEXT

FEAS-001 (error) You do not have the necessary license key.

DESCRIPTION

The user does not have the necessary license key to run the given feature.

WHAT NEXT

Check the location of the keyfile, either the default location or at $SYNOPSYS_KEY_FILE. Check the key file to see if the feature exists. If the user does not have the feature in the key file, then the user cannot run this feature. It could also be that all the licenses are in use.

FEAS-002 (warning) High Fanout Synthesis has not been performed

DESCRIPTION

High Fanout Synthesis has not been performed on this design.

WHAT NEXT

User should run high fanout synthesis before running this command. Otherwise, the result may not be accurate.

FEAS-003 (warning) Zero Path Margin is given but adjustments for Zero Path violating endpoints not enabled. Margin not enabled if adjustments not enabled

DESCRIPTION

The design has been given a Zero Path margin value, but margin adjustments for Zero Path violating endpoints have not been enabled. Thus, the margin adjustments will not performed.

WHAT NEXT

User should turn on Zero Path adjustments if this is intended, or remove the Zero Path margins.

FEAS-004 (warning) Zero Wire Load Margin is given but adjustments for Zero Wire Load violating endpoints not enabled. Margin not enabled if adjustments not enabled

DESCRIPTION

The design has been given a Zero Wire Load margin value, but margin adjustments for Zero Wire Load violating endpoints have not been enabled. Thus, the margin adjustments will not performed.

WHAT NEXT

User should turn on Zero Wire Load adjustments if this is intended, or remove the Zero Wire Load margins.

FEAS-005 (warning) compare mode is set to 1. It overwrites all other margin value settings

DESCRIPTION

Compare mode is turned on and overwrites all given margin values.

WHAT NEXT

FEAS-006 (error) Please specify at least one type of adjustment

DESCRIPTION

The get_adjusted_endpoints command is called without specifying the type of adjusted endpoints. Please specify at least one type.

WHAT NEXT

get_adjusted_endpoints(2)

FEAS-007 (warning) %s value should be negative... ignoring.

DESCRIPTION

The value provided should be a negative number. Please provide a negative number to the option.

WHAT NEXT

set_feasibility_options(2) report_feasibility_options(2) get_adjusted_endpoints(2)

FEAS-008 (warning) path group %s does not exist... ignoring.

DESCRIPTION

The path group provided does not exist in the design and/or scenario. Please make sure that the specified path group has already been defined before setting the slack threshold on this path group.

WHAT NEXT

set_feasibility_options(2) report_feasibility_options(2) get_adjusted_endpoints(2)

FEAS-009 (error) path group slack threshold not given

DESCRIPTION

The path group slack threshold is not provided even though the path group(s) are given. Please provide the value using the -path_group_slack_threshold option.

WHAT NEXT

set_feasibility_options(2) report_feasibility_options(2) get_adjusted_endpoints(2) report_adjusted_endpoints(2)

FEAS-010 (error) path group(s) not given

DESCRIPTION

The path group slack threshold is provided but no path groups are specified. Please

provide the path groups using the -slack_threshold_path_groups option.

WHAT NEXT

set_feasibility_options(2) report_feasibility_options(2) get_adjusted_endpoints(2) report_adjusted_endpoints(2)

FEAS-100 (warning) Found zero path (ZP), startpoint %s (arrival time %.2f), endpoint %s (required time %.2f, delta setup %.2f), with slack %.2f.

DESCRIPTION

This is a Zero Path, meaning that the required time at endpoint is less than the arrival time at the start time, so there is not enough time for the signal to propagate to the endpoint. Zero Path violations are independent of the physical layout of the circuit. In other words, it is impossible for the design to meet timing on this path.

WHAT NEXT

Check the constraints and clocks on this path and make corresponding changes to relax timing window.

FEAS-101 (warning) Found zero wireload path (ZWL), startpoint %s (arrival time %.2f), endpoint %s (required time %.2f, delta setup %.2f), with slack %.2f.

DESCRIPTION

A Zero Wire Load Path has been found. The zero wire load delay of this path is the delay through the path assuming zero wire load at every output pin of cells in this path. In other words, this is the best case timing possible for this path. A Zero Wire Load path (or a Zero Wire Load violating path) is one where the arrival time at the startpoint plus to zero wire load delay of this path is more than the required time of the endpoint. This means that there is not enough time for the signal to propagate through this path and meet timing.

WHAT NEXT

Check the design constraints and logic structure for this path. Fix constraints if there is error. Consider changing logics or use multicycle path if timing is

impossible to meet.

FEAS-102 (information) Zero endpoint %s: start arrival = %f, required time = %f, library setup adjustment = %f, margin = %f.

DESCRIPTION

This information shows the margin adjustment applied to a zero path endpoint. A Zero Path is a timing path where the required time at endpoint is less than the arrival time at the start point, so there is not enough time for the signal to propagate to the endpoint, even when the interconnect delay on the path is ignored. Zero Path violations are independent of the physical layout of the circuit. In other words, it is impossible for the design to meet timing on this path.

The different items printed are:

start arrival. This is the arrival time at the start point of the path.

required time. This is the required time at the end point of the path.

library setup **adjustment.** This is an adjustment the tool adds to the calculation in order to take into consideration that the transition time to the end point will be different from the current transition, thereby resulting in a different delay.

The required time for an endpoint depends on the setup time of the endpoint flip-flop, and this setup time depends on its input transition. Before any optimization, the input transition is very likely to be very bad and unrealistic compared to the input transition for a properly optimized design. This results in a very unrealistic setup time for the endpoint flip-flop in the early stage of the design where feasibility flow is being used. However, it is expected that optimization will fix the input transition and setup time. Hence, the library setup adjustment represents the expected change in the setup time after the transition time is fixed. This adjustment is a characteristic of the cell and the library and the tool calculates this adjustment automatically when considering the margin values to adjust.

margin. This is the margin that the tool applies to the end point for this path. The margin is calculated as follows:

> ZP violation = (required time + library setup adjusment) - start arrival
> margin applied = (1 + ZP_MARGIN/100) * ZP violation
> where ZP_MARGIN is the zero path margin (in percentage) the user has set using the set_feasibility_options command.

EXAMPLE

Suppose the user has set the ZP_MARGIN to 25% and the tool gave the following message:

Information: Zero endpoint DSP/top0/x_top/reg/r_reg_10_/D: start arrival = 4.50000, required time = 4.390979, library setup adjustment = 0.002595, margin = -0.13303250.

(FEAS-102)

This means that the endpoint DSP/top0/x_top/reg/r_reg_10_/D has a zero path violation. The zero path violation is (required time + library setup adjustment) - (start arrival) = (4.390979 + 0.002595) - 4.50000 = -0.106426

Therefore, the margin will be (1 + 25/100) * ZP violation = 1.25 * (-0.106426) = -0.13303250

WHAT NEXT

see set_feasibility_options

FEAS-103 (information) Zero wireload endpoint %s: start arrival = %f, required time = %f, zero wireload delay = %f, library setup adjustment = %f, margin = %f.

DESCRIPTION

This information shows the margin adjustment applied to an endpath with zero wireload violation. A Zero Wireload Path (or Zero Wireload violating path) is a timing path where the required time at endpoint is less than the arrival time at the start point plus the delay through the path assuming zero wireload at each cell, so there is not enough time for the signal to propagate to the endpoint, even when the interconnect delay on the path is ignored. Zero Wireload violations are independent of the physical layout (i.e. placement) of the circuit, and depends only on the cell characteristics and constraints on the path. In other words, it is highly impossible for the design to meet timing on this path.

The different items printed in this message are:

start arrival. This is the arrival time at the start point of the path.

required time. This is the required time at the end point of the path.

zero wireload **delay.** This is the total delay through the path, assuming zero wireload at each output pin of cells. In other words, this is a best-case timing through the path.

library setup **adjustment.** This is an adjustment the tool adds to the calculation in order to take into consideration that the transition time to the end point will be different from the current transition, thereby resulting in a different delay.

The required time for an endpoint depends on the setup time of the endpoint flip-flop, and this setup time depends on its input transition. Before any optimization, the input transition is very likely to be very bad and unrealistic compared to the input transition for a properly optimized design. This results in a very unrealistic setup time for the endpoint flip-flop in the early stage of the design where feasibility flow is being used. However, it is expected that optimization will fix

the input transition and setup time. Hence, the library setup adjustment represents the expected change in the setup time after the transition time is fixed. This adjustment is a characteristic of the cell and the library and the tool calculates this adjustment automatically when considering the margin values to adjust.

margin. This is the margin that the tool applies to the endpoint for this path. The margin is calculated as follows:

> ZWL violation = (required time + library setup adjusment) - (start arrival + zero wireload delay)
> margin applied = (1 + ZWL_MARGIN/100) * ZWL violation
> where ZWL_MARGIN is the zero wireload margin (in percentage) the user has set using the set_feasibility_options command.

EXAMPLE

Suppose the user has set the ZWL_MARGIN to be 0% and the tool gave the following message:

Information: Zero wireload endpoint DSP/top0/x_top/r_reg_10_/D: start arrival = 0.000000, required time = 4.389008, zero wireload delay = 4.458447, library setup adjustment = 0.004813, margin = -0.064625 (FEAS-103)

This means that the endpoint DSP/top0/x_top/reg/r_reg_10_/D has a zero path violation. The zero path violation is (required time + library setup adjustment) - (start arrival + zero wireload delay) = (4.389008 + 0.004813) - (0.000000 + 4.458447) = -0.064626

Therefore, the margin will be (1 + 0/100) * ZWL violation = -0.064626

If the ZWL_MARGIN was set to 25%, then the margin will be (1 + 25/100) * ZWL violation = -0.0807825

WHAT NEXT

see set_feasibility_options

FEAS-110 (information) Summary: %s

DESCRIPTION

Gives a summary of the number of timing vioations, zero paths, and/or zero wire load paths of a path group.

WHAT NEXT

None.

FEAS-201 (warning) Detected net '%s' has bigger fanout number than 500.

DESCRIPTION

This message occurs because the net fanout number is bigger than the fanout threshold. **place_opt_feasibility** flow will detect this issue before optimization.

This feature is meant to provide better behavior during optimization for high-fanout nets that cannot be decomposed by buffering (for example, because they are dont_touch) or give user information about the net which may cause trouble.

WHAT NEXT

Set the net to ideal net.

SEE ALSO

place_opt_feasibility(2)
set_ideal_net(2)
set_ideal_network(2)

FEAS-202 (warning) Performing automatic 'set_ideal_net' on '%d' nets.

DESCRIPTION

This message occurs because **place_opt_feasibility** flow detect some net with fanout number bigger than the fanout threshold before timing optimization.

This feature is meant to provide better behavior during optimization for high-fanout nets that cannot be decomposed by buffering (for example, because they are dont_touch).

WHAT NEXT

Change the attribute of the nets reported as message id FEAS-201 to allow tool optimize it during some stage such as HFS.

SEE ALSO

place_opt_feasibility(2)
set_ideal_net(2)
set_ideal_network(2)
FEAS-201(n)

FILE

FILE-1 (error) Can’t open file ’%s’.

DESCRIPTION

WHAT NEXT

FILE-2 (error) Can’t create file ’%s’.

DESCRIPTION

WHAT NEXT

FILE-3 (error) Can’t close file ’%s’.

DESCRIPTION

WHAT NEXT

FILE-4 (error) Can’t close file stream for ’%s’.

DESCRIPTION

WHAT NEXT

FILE-5 (error) Invalid data format encountered.

DESCRIPTION

WHAT NEXT

FILE-6 (error) Alias ’%s’ depends on itself.

DESCRIPTION

WHAT NEXT

FILE-7 (error) Invalid history syntax.

DESCRIPTION

WHAT NEXT

FILE-8 (error) There is no previous command.

DESCRIPTION

WHAT NEXT

FILE-9 (error) Command ’%d’ not found; out of range.

DESCRIPTION

WHAT NEXT

FILE-10 (error) ’%s’ not found in history.

DESCRIPTION

WHAT NEXT

FILE-11 (error) Can’t find file ’%s’.

DESCRIPTION

WHAT NEXT

FLIPCHIP-001 (Error) The input file is not of AIF type, but %s.

DESCRIPTION

You get this message because the input file is not AIF file.

WHAT NEXT

Please check the input file and make sure the line of file type is TYPE=AIF.

FLIPCHIP-002 (Error) The input file does not specify distance in the unit of um, but %s.

DESCRIPTION

You get this message because the units in the given file is not um.

WHAT NEXT

Please check the given file and make sure the line setted units is UNITS=um or UNITS=UM.

FLIPCHIP-003 (Error) The width of die(%f) is not legal.

DESCRIPTION

You get this message because the width of die in the input file is not legal.

WHAT NEXT

Please check the input file and make sure the width of die is positive.

FLIPCHIP-004 (Error) The hight of die(%f) is not legal.

DESCRIPTION

You get this message because the hight of die in the input file is not legal.

WHAT NEXT

Please check the input file and make sure the hight of die is positive.

FLIPCHIP-005 (Error) The type of input file is unspecified.

DESCRIPTION

You get this message because the type of input file is unspecified.

WHAT NEXT

Please specify the type of the file as TYPE=AIF.

FLIPCHIP-006 (Error) The unit of input file is unspecified.

DESCRIPTION

You get this message because the unit of input file is unspecified.

WHAT NEXT

Please specify the unit of the file as UNITS=um.

FLIPCHIP-007 (Error) Failed to open file %s.

DESCRIPTION

You get this message because the input file can’t open.

WHAT NEXT

Please make sure the input file is existent.

FLIPCHIP-008 (Error) Must specify exactly one physical lib cell.

DESCRIPTION

You get this message because specify more than one physical lib cell.

WHAT NEXT

Please make sure only one physical li cell is specified.

FLIPCHIP-009 (Error) Can not find physical lib cell.

DESCRIPTION

You get this message because can’t find phsical lib cell.

WHAT NEXT

Please make sure the physical lib cell specified is right.

FLIPCHIP-010 (Error) Bump cell %s does not exist, can’t create without -physical_lib_cel specified.

DESCRIPTION

You get this message because can’t create bumps without phyical lib cell.

WHAT NEXT

Please use the option -physical_lib_cel to specify bump’s physical lib cell.

FLIPCHIP-011 (Warning) String %s is not a net Name.

DESCRIPTION

You get this message because one net name is not correct.

WHAT NEXT

Please check the net name and make sure it is a net name.

FLIPCHIP-012 (Error) String %s is not a bump cell inst name but other cell inst name.

DESCRIPTION

You get this message because one name in the input file isn’t a bump cell name but other cell name.

WHAT NEXT

Please check the string and make sure it is a bump cell inst name.

FLIPCHIP-013 (Error) No verion type in aif or version isn’t 2.0.

DESCRIPTION

You get this message because there’s no verion type in aif or version type isn’t 2.0.

WHAT NEXT

Please check the input file and make sure the version type is VERSION=2.0.

FLIPCHIP-020 (Error) No net to merge.

DESCRIPTION

You get this message because there’s no flat net in the from net list.

WHAT NEXT

Please make sure there’s at least one flat net in the from list.

FLIPCHIP-021 (Error) The net %s is not the same type as the

first net.

DESCRIPTION

You get this message because all the net type is not the same.

WHAT NEXT

Please make sure all the from net type is the same.

FLIPCHIP-022 (Error) Net %s has been already existent.

DESCRIPTION

You get this message because the to net is existent.

WHAT NEXT

Please reassign the to net which is not existent or add the net to the from net list.

FLIPCHIP-023 (Error) Not enough bumps for this personality type, skipping...

DESCRIPTION

You get this error because there are not enough bump cell to complete the net assignment of a certain personality type. The tool will skip net assignment for this personality type.

WHAT NEXT

Check the log to see which personality type it is processing while this error message is issued. To resolve this issue, you can 1) Instantiate more bump cells of this personality type 2) Adjust the number of driver or bump cells of this personality type 3) Specify a different -uniquify option(default is 1), the larger the -uniquify option, the less bumps cell will be needed.

FLIPCHIP-024 (Error) Bump %s port inst %s is power or ground, but the driver %s port inst %s isn’t match the bump’s port inst

type.

DESCRIPTION

You get the message because PG bump can’t be assigned to driver which is not the same type. Power bump should be connected to power driver and ground bump should be connected to ground driver. Signal bump can be connected all type of drivers.

WHAT NEXT

You can use the command set_flip_chip_type to regroup drivers and bumps. Make sure that PG bumps are in the group of PG drivers. If the driver has all types of flip chip port inst, it must be in the group of signal bumps.

FLIPCHIP-025 (Error) Cannot find reference lib cell %s for creating bump %s.

DESCRIPTION

You get the message because can’t find reference lib cell for creating bump.

WHAT NEXT

Please check the reference lib cell specified by -physical_lib_cel option and your library setting. If fc_aif_ref_lib_cell is set to 1, please check the REF_LIB_CELL column of the input AIF file.

FLIPCHIP-125 (Error) License check failed.

DESCRIPTION

You get the message because you don’t have the flip chip license.

WHAT NEXT

Please make sure you have the flip chip license.

FLIPCHIP-126 (Error) Must specify exactly one filler cell.

DESCRIPTION

You get the message because you specified more than one filler cells or no filler cell specified.

WHAT NEXT

Please make sure you specify one filer cell.

FLIPCHIP-127 (Warning) Can not specify more than 5 pairs of personality constraints.

DESCRIPTION

You get the message because you specify more than 5 pairs of personality constraints in the command.

WHAT NEXT

Please make sure specify no more than five personality constraints in the command.

FLIPCHIP-128 (Warning) Unknown option, ignored.

DESCRIPTION

You get the message because there’s an unkown option in the command.

WHAT NEXT

To refer to the man page of the command and check the command option.

FLIPCHIP-129 (Error) No bumps or drviers to dump.

DESCRIPTION

You get the message because there’s no bump or driver in the design.

WHAT NEXT

To check whether there’s some bumps and some drivers in the design.

FLIPCHIP-130 (Error) The option -num_extra_spacing and -extra_spacing must be used together.

DESCRIPTION

The option -num_extra_spacing and -extra_spacing should be used together.

WHAT NEXT

Check whether -num_extra_spacing and -extra_spacing use together in the command.

FLIPCHIP-131 (Error) Not enough slot to place all bumps.

DESCRIPTION

When the bump_number specified is too big, so there’s no slot to place all bumps.

WHAT NEXT

The option -num is optional, if you don’t know the precise number of bumps, you may not specify the -num option.

FLIPCHIP-132 (Error) Flip chip grid is not defined or is not valid in DB.

DESCRIPTION

Flip chip grid should be in DB.

WHAT NEXT

Please check whether set grid correctly. If there’s no flip chip grid, you can use the command set_flip_chip_grid to creates equally spaced grid points for driver placement.

FLIPCHIP-133 (Warning) Too many reserved locations.

DESCRIPTION

You get the message because the number of reserved_for_cell slot exceed the max number(500). ICC will ignore the specified reserved slots after the first 500.

WHAT NEXT

Please check the option -reserved_for_cell, make sure the reserved slot is no more than 500.

FLIPCHIP-134 (Warning) invalid row or col index.

DESCRIPTION

You get the message because row or col index which you specify exceeds driver row or col size. ICC will skip the row or col or slot.

WHAT NEXT

Please check the row and col index in the command, make sure they are all no more than the driver row and col size.

FLIPCHIP-135 (Error) Can’t find any matching cell site.

DESCRIPTION

You get the message because there’s no slot in the option -flip_chip_site.

WHAT NEXT

Please make sure there’re some cell site in the option -flip_chip_site.

FLIPCHIP-136 (Error) Must specify bbox in standard format {{llx

lly} {urx ury}}.

DESCRIPTION

You get the message because the option -outer_ring isn’t correctly specified.

WHAT NEXT

Make sure specify the lower-left coordinate {llx lly} and up-right coordinate {urx ury} of the bounding box of the outermost ring in the format of {{llx lly} {urx ury}}. Please refer to the command man page.

FLIPCHIP-137 (Error) Not enough space to place all the rings.

DESCRIPTION

You get the message because the specified boundary box is full, there’s no space to place all the rings.

WHAT NEXT

Please increase the ring boundary size or decrease the ring number, so all the rings can be placed.

FLIPCHIP-138 (Error) Must specify at least 2 moveable flip chip cells.

DESCRIPTION

This error message occurs because the tool requires at least 2 moveable flip chip cells to be specified. The object(s) with the given name may not exist in the Milkyway library.

WHAT NEXT

Check that the specified object is spelled correctly, and that it exists in the library or design. Check the command man page to verify the correct syntax.

FLIPCHIP-139 (Error) Fail to read driver or bump %s personality

type

DESCRIPTION

You get the message because there’s no personality type in the driver or bump.

WHAT NEXT

You can use the command set_flip_chip_type to set personality type for the driver or bump.

FLIPCHIP-140 (Warning) Master %s has no flipchip port defined. skip.

DESCRIPTION

You get this message because the cell is defined as "flip_chip_driver" but none of its port is defined as "FlipChip" type port.

WHAT NEXT

Check your library setting to see if this is intended.

FLIPCHIP-141 (Error) Driver %s and driver %s are overlapping.

DESCRIPTION

You get the message because the two divers are overlapping.

WHAT NEXT

You can use gui to check whether they are overlapping and move one of them.

FLIPCHIP-142 (Error) Failed to open file %s for write.

DESCRIPTION

You get this message because tool cannot open a file for write.

WHAT NEXT

Check whether the working directory is writable, and whether there exist an unwritable file with the same name.

FLIPCHIP-143 (Warning) must specify reserved locations in {{cell_ref {col_index row_index}...} {cell_ref {col_index row_index}...} ...} format.

DESCRIPTION

You get the message because the format of reserved locations is not right.

WHAT NEXT

You can refer to the man page of the command and check the format of reserved locations.

FLIPCHIP-144 (Error) Cannot open the FRAM view of cell %s.

DESCRIPTION

You get this message because the tool cannot open the FRAM view of the library cell you specified in option -reserved_for_cell.

WHAT NEXT

please check your library setting.

FLIPCHIP-145 (Warning) Can’t set %s for island type cell site %s, skipping

DESCRIPTION

You get the message because island cell site can’t set personality types.

WHAT NEXT

Please check whether the site is a island type cell site.

FLIPCHIP-146 (Error) Can’t specify option -phy_lib_cel when tcl variable fc_read_write_non_aif_format is set to 1.

DESCRIPTION

You get the message because you specify option -phy_lib_cel when tcl variable fc_read_write_non_aif_format is set to 1.

WHAT NEXT

If you want to no aif format, set fc_read_write_non_aif_format 1, and not specify option -phy_lib_cel. If you want to aif format, set fc_read_write_non_aif_format 0, and you can specify option -phy_lib_cel.

FLIPCHIP-147 (Warning) Can’t set %s for non-island type cell site %s, skipping

DESCRIPTION

You get the message because non-island cell site can’t set personality constraints and reserved slots.

WHAT NEXT

Please check whether the site is a island type cell site.

FLIPCHIP-148 (Warning) MT-pin aware: terminals assigned to bump %s exceed the maximum number 8

DESCRIPTION

You get the message because more than 8 terminals are assigned to a certain bump. Net assignment can still completes but the tool will not record the terminal infomation for the extra terminals. This might affect the RDL routing QoR.

WHAT NEXT

Adjust the -uniquify option you used in assign_flip_chip_nets. Specify 1 or any positive interger less than 8 should solve this problem.

FLIPCHIP-149 (Error) MT-pin aware: failed to create MT pin matching property on bump cell %s

DESCRIPTION

You get the message because tool failed to create MT pin matching property on a certain bump cell.

WHAT NEXT

FLIPCHIP-150 (Warning) Port number on ref cel %s exceeds the maximum limit of %d

DESCRIPTION

You get the message because there are too many flip chip ports on a certain ref cel. This is mostly likely due to improper use of -multiple_terminal_pin option.

WHAT NEXT

FLIPCHIP-151 (Error) Option -terminal_names cannot be used together with -multiple_terminal_pin or -terminal_layers option.

DESCRIPTION

You get the message because the 2 options being specified is exlusive to each other. You can use only one of them at the same time.

WHAT NEXT

FLIPCHIP-152 (Error) Option -terminal_layers can only be used together with -multiple_terminal_pin option.

DESCRIPTION

You get the message because of improper option usage. The -terminal_layers option can only be specified when -multiple_terminal_pin is specified.

WHAT NEXT

FLIPCHIP-153 (Error) Cannot find pin %s by name.

DESCRIPTION

You get the message because the specified pin cannot be found by name. Make sure it is correctly specified in -terminal_names option.

WHAT NEXT

FLIPCHIP-153 (Error) Wrong format of terminal name specified in -terminal_names option.

DESCRIPTION

You get the message because the terminal name is not correctly specified thus the tool is unable to parse the name string. The name string must be specified in -terminal_names option in the following format: "cell_name/pin_name:terminal_name"

WHAT NEXT

FLT-002 (information) Errors preprocessing compiled filter.

DESCRIPTION

This is a summary message generated after a filter expression has successfully parsed, but unsuccessfully processed because of an unknown identifier, type mismatch in a relation, or invalid operator in a relation.

WHAT NEXT

Look at previous error messages to determine the problem with the filter expression. Correct the problems, and retry the operation.

FLT-003 (error) while parsing filter expression: %s at '%s'

DESCRIPTION

A filter expression could not be successfully parsed, typically because of a syntax error. The point in the expression that caused the failure is shown along with the remainder of the expression.

WHAT NEXT

Look at the man pages for filter expression syntax, and verify that your expression conforms to the syntax. Ensure that supported relation and logical operators are in use, that the expression is constructed of a series of relations separated by logical operations, etc.

FLT-005 (error) Unknown attribute '%s'.

DESCRIPTION

Filters are evaluated within a context. Given the current context, an attribute which you entered is unknown.

A relation in a filter expression is very simple. For example, "area <= 2.4". In this case, the attribute is "area". If you were applying the filter to a pin collection, since "area" is not a valid pin attribute, this error would occur.

WHAT NEXT

Look at the man pages for the given command, and ascertain the valid values for attributes.

FLT-006 (error) Type mismatch between '%s' and '%s'.

DESCRIPTION

A relation in a your filter expression has an identifier and value with inconsistent types. The following simple rules apply:

Identifier Type mismatch generates:when value is: ---------- ---------- stringn/a - never an error numeric literalstring, true, false boolean numeric literal, string

Note some important distictions: the boolean words TRUE and FALSE are interpretted as strings in a string relation, or as boolean in a boolean relation. Simlilarly, the numeric literal 2.4E-9 is interpretted as a string in a string relation, or as a number in a numeric relation.

WHAT NEXT

Re-enter the filter with valid identifier/value relations.

FLT-007 (error) Invalid operator '%s' for '%s' and '%s'.

DESCRIPTION

A relation in a your filter expression has an identifier and value with consistent types but an invalid operator. The following simple rules apply:

Type: Invalid operators: ---------- ----------- string None. All operators ok. numeric literal=~, !~ boolean=~, !~, <, >, >=, <=

WHAT NEXT

Re-enter the filter with a valid operator for the failed relation.

FMLINK-1 (warning) Error code %d encountered while writing SVF file:
%s
Operation aborted.

DESCRIPTION

dc_shell encountered an internal error while writing out the Formality verification setup (SVF) file. This may cause the SVF file to be incomplete.

WHAT NEXT

Please contact the Synopsys Support Center for assistance.

SEE ALSO

set_svf(2)

FOPT-001 (error) Please specify only one focal area.

DESCRIPTION

You receive this error message because you have specified more than one focal metric for focal opt. The tool is expecting exactly one focal metric specified in one iteration of focal opt. continue to optimize.

WHAT NEXT

Specify only one of the following option with focal_opt: -hold_endpoints -setup_endpoint -drc_nets

SEE ALSO

focal_opt (2),

FOPT-002 (error) Can’t find file %s.

DESCRIPTION

You receive this error message because you have specified a file that does not exist.

WHAT NEXT

Please verify the file location.

SEE ALSO

focal_opt (2),

FOPT-003 (error) Invalid specification for %s switch.

DESCRIPTION

The current specification for that switch is not valid one.

WHAT NEXT

Please use one of valid specification for the switch. To find out the valid specifications, please refer man page of focal_opt.

SEE ALSO

focal_opt (2)

FOPT-004 (Information) Using user defined cost priority %s, -priority switch is ignored in focal_opt.

DESCRIPTION

This message informs you that -prioritize switch in focal_opt is ignored because user has pre-defined cost priority settings. The user defined cost prioity is coming from set_cost_priority command.

WHAT NEXT

No action is needed if user need to tool to respect user-defined cost priority settings. If this is not inteneded, then user need to remove the cost priority settings and run focal_opt with -prioritize option.

SEE ALSO

focal_opt (2), **set_cost_priority** (2)

FOPT-005 (Information) Setting endpoint margin(setup) %f for endpoint %s.

DESCRIPTION

This message informs user that the tool is overwriting the slack value for the specific endpoint with the value in the file that is specified with the -setup_endpoints option when running focal_opt.

WHAT NEXT

No action is needed if user intend to overwrite the slack value for the endpoint. If this is not desired, user can change the behavior with the focalopt_endpoint_margin variable.

SEE ALSO

focal_opt (2), **focalopt_endpoint_margin** (3)

FOPT-006 (Information) Setting endpoint margin(hold) %f for endpoint %s.

DESCRIPTION

This message informs user that the tool is overwriting the slack value for the specific endpoint with the value in the file that is specified with the -hold_endpoints option when running focal_opt.

WHAT NEXT

No action is needed if user intend to overwrite the slack value for the endpoint. If this is not desired, user can change the behavior with the focalopt_endpoint_margin variable.

SEE ALSO

focal_opt (2), **focalopt_endpoint_margin** (3)

FOPT-007 (error) Failed to set endpoint margin (%s) %f to pin %s or same margin has already been set on endpoint.

DESCRIPTION

You receive this error message because the tool has encountered an error when setting the endpoint margin on the endpoint.Or the same margin has already been set on the specific endpoint.

WHAT NEXT

Please double check if endpoint margin has already been set on the endpoint. If not, then please verify the validity of the endpoint and refer to the focal_opt(2) man page for the accepted format of the endpoint margin file.

SEE ALSO

focal_opt (2),

FOPT-008 (error) Fail to find endpoint %s from %s endpoint file.

DESCRIPTION

You receive this error message because the tool cannot find the specified endpoint in the design.

WHAT NEXT

Please verify the validity of the endpoint in the design or the spelling and update the endpoint file accordingly.

SEE ALSO

focal_opt (2),

FOPT-009 (error) Endpoint file format not supported for the following input:
%s.

DESCRIPTION

You receive this error message because the specified line provided in the endpoint file does not follow the format the tool recognize.

WHAT NEXT

Please refer to the focal_opt man page for the accepted format.

SEE ALSO

focal_opt (2),

FOPT-010 (error) Invalid scenario name %s specified in INPUT file %s. Endpoint %s will be optimized without margin.

DESCRIPTION

You receive this error message because you have specified an invalid scenario name in the endpoint file. The specified endpoint will stil be optimized by focal_opt.

However, the specified endpoint margin will not be set for the specified endpoint.

WHAT NEXT

Please verify the scenario name and edit the endpoint file accordingly.

SEE ALSO

focal_opt (2),

FOPT-011 (error) Endpoint %s does not have valid endpoint margin specified.

DESCRIPTION

You receive this error message because the endpoint margin specified for the endpoint does not follow the format that the tool supports.

WHAT NEXT

Please refer to the focal_opt man page for the accepted format.

SEE ALSO

focal_opt (2),

FOPT-012 (warning) Additional endpoint margin is not set on endpoint %s because given slack is the same as the tool’s slack.

DESCRIPTION

You receive this error message because the endpoint margin specified is the same or very close to the margin that has already been set on the endpoint.

WHAT NEXT

None.

SEE ALSO

focal_opt (2),

FOPT-013 (warning) No endpoint margin set on endpoint %s because positive slack is specified in %s endpoint file.

DESCRIPTION

You receive this error message because the endpoint margin specified in the input file is of positive slack. Therefore, no margin is set on the endpoint and the current slack value for the endpoint remains unchanged.

WHAT NEXT

SEE ALSO

focal_opt (2),

FOPT-014 (error) Failed to remove endpoint margin(%s) for endpoint %s.

DESCRIPTION

You receive this error message because the tool has encountered an error when removing the endpoint margin on the endpoint.

WHAT NEXT

Please double check if endpoint margin has already been set on the endpoint.

SEE ALSO

focal_opt (2),

FOPT-015 (Information) Removing endpoint margin(%s) for endpoint %s.

DESCRIPTION

This message informs user that the tool is removing the endpoint margin that was previously set for the specified endpoint.

WHAT NEXT

No action is needed if user intend to remove the previous set endpoint margin for the endpoint after focal_opt.

SEE ALSO

focal_opt (2), **focalopt_endpoint_margin** (3)

FOPT-016 (warning) Additional endpoint margin is not set on endpoint %s because given slack is larger than the tool's slack.

DESCRIPTION

You receive this error message because the endpoint margin specified for the endpoint is larger than the tool's slack. No action is taken on the endpoint.

WHAT NEXT

SEE ALSO

focal_opt (2),

FP-1 (error) Unsupported combination of options specified.

DESCRIPTION

You received this error message because you specified an invalid option combination.

[-control_type aspect_ratio] cannot be combined with one or more of "-core_width", "-core_height", "-keep_io_place", "-core_aspect_ratio".
[-control_type width_and_height] cannot be combined with one or more of "-core_aspect_ratio", "-core_utilization", "-keep_io_place", "-num_rows".
[-control_type boundary] cannot be combined with one or more of "-core_aspect_ratio", "-core_utilization","-core_width", "-core_height", "-num_rows", "pad_lim".

WHAT NEXT

Re-run the command with legal combination of options.

FP-2 (error) Invalid value specified for the option

DESCRIPTION

You received this error message because you specified an invalid value for the option.

WHAT NEXT

Refer to man page for acceptable values and re-run the command with correct option values.

FPCCI-001 (Warning) Command '%s' is obsolete. Please use '%s' instead.

DESCRIPTION

This warning message occurs when you use a certain command which is obsolete and will be removed in later release.

WHAT NEXT

Please use the new command proponed in the warning message.

FPCCI-002 (Warning) Design constraints have been removed. You need to re-apply design constraints on current design.

DESCRIPTION

This warning message occurs because merge_fp_hierarchy deletes all design constraints from the cell.

WHAT NEXT

Please re-apply design constraints using read_sdc command.

FPCCI-003 (Warning) fp_set_pin_constraints is called without any option.

DESCRIPTION

This warning message occurs because fp_set_pin_constraints is called without any option.

WHAT NEXT

Please use fp_remove_pin_constraints to apply default values for pin constraints.

FPCCI-004 (Warning) Original sdc file is not provided. Couldn’t update sdc file. This may cause constraints mismatch with new logical hierarchy.

DESCRIPTION

This warning message occurs because sdc file is not providing while using command merge_fp_hierarchy.

WHAT NEXT

Please provide an sdc file or manually check/modify sdc for the new logical hierarchy.

FPCCI-005 (Error) Please specify correct UPF supply net for option -net_name.

DESCRIPTION

This error message occurs because command connect_virtual_pg_net fail to get flat net name from UPF supply net object.

WHAT NEXT

Please provide correct UPF supply net object.

FPCCI-006 (Error) Fail to find lib cell name from power switch %s .

DESCRIPTION

This error message occurs because command fail to get lib cell name from specified power switch.

WHAT NEXT

Please use map_power_switch to provide correct lib cell list.

FPCCI-007 (Error) Cannot find voltage area %s.

DESCRIPTION

This error message occurs because fail to get voltage area object with specified name.

WHAT NEXT

Please use report_voltage_area to check the voltage area.

FPCCI-008 (Error) Cannot find %s in design hierarchy.

DESCRIPTION

This error message occurs because fail to get specified hierarchy module in voltage area.

WHAT NEXT

Please use report_voltage_area to check hierarchy modules in the voltage area.

FPCCI-009 (Error) Cannot find hierachy modules in voltage area %s.

DESCRIPTION

This error message occurs because fail to get hierarchy modules list in specified voltage area.

WHAT NEXT

Please use report_voltage_area to check hierarchy modules in the voltage area.

FPCCI-010 (Error) Specified hierarchy module %s inconsistent

with voltage area %s.

DESCRIPTION

This error message occurs because specified hierarchy module is not under specified voltage area.

WHAT NEXT

Please use report_voltage_area to check hierarchy modules in the voltage area.

FPCCI-011 (Error) The specified shielding width is less than or equal to the minimum DB unit!

DESCRIPTION

This is a user error caused by specifying a shielding width that is significantly smaller than any legal width.

WHAT NEXT

Examine your specification of shielding width and make sure that it is at least as large as any layer’s minimum width.

FPCCI-012 (Error) The specified shielding width (%.3f) is less than the minimum width for %s (%.3f)!

DESCRIPTION

This is a user error caused by specifying a shielding width that is smaller than one or more of the specified metal layers’ minimum width.

WHAT NEXT

Examine your specification of shielding width and make sure that it is at least as large as any specified layer’s minimum width.

FPCCI-013 (Error) Failed to get base unit!

DESCRIPTION

This is an internal error.

WHAT NEXT

Contact your Synopsys representative.

FPCCI-014 (Warning) Object %s is not a logical cell instance

DESCRIPTION

remove_mim_property only accepts logical cell instances as input

WHAT NEXT

see remove_mim_property man page

FPCCI-015 (Error) Unable to remove MIM property successfully from %s

DESCRIPTION

This is an internal error.

WHAT NEXT

Contact your Synopsys representative.

FPCCI-016 (Error) %s failed in %s

DESCRIPTION

This is an internal error.

WHAT NEXT

Contact your Synopsys representative.

FPCCI-017 (Warning) %s does not belong to any MIM group

DESCRIPTION

The logical cell instance above does not share the same reference (master) cell with any other logical cell instance in the design. In addition, no MIM property has been attached by the user to designate it as belonging to an MIM group. See man page for uniquify_fp_mw_cel option -store_mim_property for more information regarding MIM property.

FPCCI-018 (Warning) The scan chains in the design will be deleted, please input your scandef file for scan design.

DESCRIPTION

This is a warning message that existing scan chains will be deleted prior to proceeding.

FPCCI-019 (Error) Object %d is not a softMacro

DESCRIPTION

This is a User error.

WHAT NEXT

Make sure that objects specified for uncommit are soft macro objects.

FPCCI-020 (Warning) Multiply instantiated soft macros detected.
uncommit_fp_soft_macros does not support multiply instantiated macros
The results of this command may be invalid

DESCRIPTION

User has specified a soft macro which belongs to a MIM group of soft macros. uncommit_fp_soft_macros currently does not support unommitting MIM group soft macros.

WHAT NEXT

Run uncommit_fp_soft_macros with this soft macro removed from the list to be uncommitted.

FPCCI-021 (Warning) Hier. cell instance %s does not have MIM property

DESCRIPTION

This hier. cell instance has not been assigned MIM property, or the MIM property may have been previously removed.

WHAT NEXT

see remove_mim_property man page Also see man page for uniquify_fp_mw_cel -store_mim_property

FPCCI-022 (Warning) MIM property for %s has been removed

DESCRIPTION

The MIM property for this instance has been removed because this is the lone instance which has the MIM property. By definition this instance is no longer an MIM and so the MIM property was removed. This condition arises probably because the MIM property of all other instances that were previously assigned as an MIM group together (with uniquify_fp_mw_cel -store_mim_property) had been earlier removed.

WHAT NEXT

see remove_mim_property man page Also see man page for uniquify_fp_mw_cel -store_mim_property

FPCCI-023 (Error) No plan groups selected!

DESCRIPTION

No plan groups were selected in either create_fp_plan_group_padding or remove_fp_plan_group_padding

WHAT NEXT

see create_fp_plan_group_padding man page or remove_fp_plan_group_padding man page.

FPCCI-024 (Warning) fp_create_plan_group_padding is deprecated, please use create_fp_plan_group_padding

DESCRIPTION

fp_create_plan_group_padding is an antiquated command name. Please begin to use create_fp_plan_group_padding.

WHAT NEXT

see create_fp_plan_group_padding man page

FPCCI-025 (Warning) fp_remove_plan_group_padding is deprecated, please use remove_fp_plan_group_padding

DESCRIPTION

fp_remove_plan_group_padding is an antiquated command name. Please begin to use remove_fp_plan_group_padding.

WHAT NEXT

see remove_fp_plan_group_padding man page

FPCCI-026 (Info) create_fp_block_shielding is running in -block_level mode. The options -inside_boundary, -outside_boundary, and any object collection will be ignored in

this command session

DESCRIPTION

This is an information message. When in block_level mode, this command can only be used to create block shielding around the cell boundary. All other options are still functional.

WHAT NEXT

See the man page for create_fp_block_shielding.

FPCCI-027 (Warning) create_fp_block_shielding option - tie_to_net takes a collection of 1 net. More than one net was found in the collection. The command will use only the 1st net in the collection for tieing to the created shielding.

DESCRIPTION

This is an warning message about improper arguments to the option "tie_to_net". This option takes only 1 net object in the collection. The command encountered more than one net specified in the collection. The command will interepret the first net in the collection as the net to use.

WHAT NEXT

See the man page for create_fp_block_shielding.

FPL-001 (error) Internal error, %s:%d

DESCRIPTION

The application encountered an internal error at the specified file and line.

WHAT NEXT

Report the problem.

FPL-002 (error) Iterating %s failed

DESCRIPTION

Iterating objects of specified type failed.

WHAT NEXT

This usually indicates database corruption. Check the database.

FPL-003 (error) Cells are not placed. Run create_fp_placement first!

DESCRIPTION

The shape_fp_blocks command requires cells to be placed before it can run.

WHAT NEXT

Place the cells using create_fp_placement command before running this command.

FPL-004 (error) No cell open!

DESCRIPTION

No Milkyway cell is open. The command is supposed to operate on the currently opened cell.

WHAT NEXT

Open the cell you want the command to act on.

FPL-005 (error) -adjust_channels option is incompatible with every other option except for -constraint_file.

DESCRIPTION

When running the shape_fp_blocks command, the -adjust_channels option can not be invoked together with any other option except for the -constraint_file option.

WHAT NEXT

Remove other options.

FPL-006 (error) Global route/Placement congestion map doesn’t exist. Please generate one before running this command.

DESCRIPTION

When running the shape_fp_blocks with the -incremental congestion_driven option, the command relies on congestion map to determine the appropriate channel widths. Without the congestion map, the command can not run.

WHAT NEXT

Generate congestion map (for example, run global route) before running this command.

FPL-007 (error) No object available for shaping!

DESCRIPTION

The command shapes non-fixed plan groups and/or soft macros. There were none in the currently opened design.

WHAT NEXT

If there are plan groups/soft macros that you want to shape, unfix them. If there are none, do not run this command.

FPL-008 (error) Cannot find %s in the file used for the incremental run

DESCRIPTION

This error occurs because the object mentioned does not exist in the file.

The -incremental option of the **shape_fp_blocks** command is designed to repeat the last floorplan (that is, to keep the same relative locations of plan groups and soft macros), while making appropriate adjustments for some changes that might have occurred. This could include changes such as increasing or decreasing target utilization of plan groups and soft macros, changing core size and shape, or adding blockages. However, changing which objects are to be shaped makes it impossible to create the same relative locations, so it is not allowed. The first time the command is run, it stores the floorplan decisions in a file. When the command is run using the **-incremental** option, it reads this file and attempts to follow the same decisions. This error indicates that the object mentioned does not exist in the file, which means that it did not exist when the command was previously run.

WHAT NEXT

Run the command without specifying the **-incremental** option.

FPL-099 (error) %s

DESCRIPTION

See error message.

WHAT NEXT

See error message.

FPL-101 (warning) No macros to pack

DESCRIPTION

The command is supposed to pack macros; there were none provided.

WHAT NEXT

Choose some macros to pack. Note that the command will not pack fixed macros, so if the macros you want packed are fixed, unfix them first.

FPL-102 (warning) %s is not a macro cell, skipping it

DESCRIPTION

The macro packing command is given a standard cell to pack; those will be skipped.

WHAT NEXT

Make sure that the objects provided to the command are macro cells.

FPL-103 (warning) Macros will not be packed for group %s, since it is not inside the core

DESCRIPTION

The mentioned plan group provided to the command was outside core. The macro packing works only inside core area.

WHAT NEXT

Make sure that the plan groups provided to the command are inside core.

FPL-104 (warning) Preplaced macro %s is in MIM plan group,

marking it not preplaced

DESCRIPTION

The command does not support preplaced macros inside multiply instantiated plan groups (MIMs); in order for the command to proceed, the preplaced macro is marked not preplaced.

WHAT NEXT

This usually happens when the placement command is initially run in the flat mode (this causes large macros to be preplaced) and later a hierarchy is chosen where large macros become part of MIMs. It may be better to specify the hierarchy in the initial placement.

FPL-105 (warning) Fixed macro inside MIM plan group %s, will be ignored

DESCRIPTION

The command does not support fixed macros inside multiply instantiated plan groups (MIMs); in order for the command to proceed, the fixed macro’s connection to the plan group will be ignored.

WHAT NEXT

Unfix macros belonging to MIMs.

FPL-106 (warning) Global route congestion map doesn’t exist. Will use placement congestion map instead.

DESCRIPTION

When running the shape_fp_blocks with the -incremental congestion_driven option, the command relies on congestion map to determine the appropriate channel widths. It attempts to find the global route congestion map; this warning indicates that it could not find it, and that it will use (generally less accurate) placement congestion map instead.

WHAT NEXT

If more accurate results are needed, run global route before running this command.

FPL-107 (warning) not enough space for channels in %s

DESCRIPTION

The shaping command produced channels that are narrower than the initial estimated requirement. This is typically due to perceived lack of space, as the command tries to make sure that the blocks stay within their target utilization.

WHAT NEXT

At this stage, the channel size have to be roughly estimated by the command. Channels can be more accurately set by using "shape_fp_blocks -incremental congestion_driven" command after a congestion map has been generated.

FPL-108 (warning) Channels in %s may be smaller than initial estimated requirement

DESCRIPTION

The shaping command produced channels that are narrower than the initial estimated requirement. This is typically due to perceived lack of space, as the command tries to make sure that the blocks stay within their target utilization.

WHAT NEXT

At this stage, the channel size have to be roughly estimated by the command. Channels can be more accurately set by using "shape_fp_blocks -incremental congestion_driven" command after a congestion map has been generated.

FPL-109 (warning) Large number of fixed standard cells detected, may be unable to avoid overlapping them with macros.

DESCRIPTION

When too many standard cells are fixed, it may be difficult or impossible to place macros without overlapping those fixed cells. Placement can place macros while ignoring overlaps with fixed standard cells. This behavior is controlled by the overlap_ignore_fixed_stdcells_count parameter. If a design has more then this number of fixed standard cells, then macro to standard cell overlaps will be allowed. If a design has less than this number of fixed standard cells, then macro to standard cells overlaps will be avoided. Note that even if macro to standard cells overlaps are avoided, there still may be some overlaps if the placement problem is difficult.

WHAT NEXT

Determine which standard cells really need to be fixed and unfixed the remaining. To have macro placement avoid the remaining fixed standard cells, set overlap_ignore_fixed_stdcells_count parameter to a value larger than the number of fixed standard cells (note that this may produce macros overlapping each other). The syntax for this is:

```
set_fp_placement_strategy -name overlap_ignore_fixed_stdcells_count -value number
```

FPL-110 (warning) Soft macro %s does not have its own congestion map, will use global congestion map instead.

DESCRIPTION

When runing shape_fp_blocks -incremental congestion_driven, the command tries to use congestion map inside soft macros to help estimate their size. This warning means that it failed to find a congestion map inside a soft macro and will use the top level congestion map instead.

WHAT NEXT

If there is a possibility that the size of the soft macro needs to increase to avoid internal congestion, generate congestion map inside the soft macro before running this command.

FPL-199 (warning) %s

DESCRIPTION

See warning message.

WHAT NEXT

See warning message.

FPOPT-002 (error) one or more macros are not fixed, optimize_fp_timing cannot continue.

DESCRIPTION

Command optimize_fp_timing requires all macros have fixed location.

WHAT NEXT

mark all macros as fixed location.

FSM_IN-0 (error) Compiler cannot read the file %s.

DESCRIPTION

You receive this message because the finite-state machine (FSM) compiler cannot open the file %s.

WHAT NEXT

Ensure that the file name is correct.

SEE ALSO

read (2).

FSM_IN-1 (warning) Compiler found illegal command %s (line: %d).

DESCRIPTION

You receive this message because once the finite-state machine (FSM) compiler starts reading rows, the **.encoding** and **.field** commands are the only ones allowed.

FSM_IN-2 (error) Input port %s is declared twice (line: %d).

DESCRIPTION

You receive this message because the input port is declared multiple times.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-3 (error) Output port %s is declared twice (line: %d).

DESCRIPTION

You receive this message because the output port specified in the message is declared multiple times.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-4 (warning) Only one %s command is allowed (line: %d).

DESCRIPTION

You receive this message because the finite-state machine (FSM) compiler has already read a clock signal.

WHAT NEXT

The FSM compiler ignores the clock signal read on the line specified in the message.

FSM_IN-5 (error) Name %s is missing (line: %d).

DESCRIPTION

You receive this message because the line specified in the message is missing a clock signal name.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-6 (error) %s signal %s is not an input port (line: %d).

DESCRIPTION

You receive this message because the signal connect to the clock pin is not an input

signal.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-7 (error) Invalid %s sense %s exists (line: %d).

DESCRIPTION

You receive this message because the clock sense or reset sense specified in the message is invalid. The clock sense is "rising_edge" rather than "falling_edge," or the reset sense is "rising" rather than "falling."

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-8 (error) The compiler cannot write the file named %s.

DESCRIPTION

You receive this error message because the finite state machine (FSM) compiler cannot open the named file and write out the state encoding information for Formality.

WHAT NEXT

Ensure that the disk is not full and that you have write permission for the file and its directory. After making the necessary changes, run the command again.

SEE ALSO

fsm_export_formality_state_info(3)

FSM_IN-10 (error) The state %s is not a state in the state table (line: %d).

DESCRIPTION

You receive this message because, during reading of the the .st file, a state was

read that is not in the state table. You must ensure that the reset state is a valid state.

WHAT NEXT

Abandon .st file read.

SEE ALSO

read (2).

FSM_IN-11 (error) State %s is used multiple times in .encoding (line: %d).

DESCRIPTION

You receive this message because the specified state has already been used in the .encoding section.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-13 (error) Binary encoding %s is used multiple times (%s at line %d and %s at line %d).

DESCRIPTION

You receive this message because the same encoding is used multiple times. For example, this could occur when encoding ’001’ is used to represent both state ’S0’ and state ’S2.’

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-15 (error) A clock must be specified for the state table.

DESCRIPTION

You receive this message because a clock must be specified for each state table.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-16 (error) The state table must have at least one %s.

DESCRIPTION

You receive this message because a state table must have at least one output.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-17 (error) A mismatched number of %s exists.

DESCRIPTION

You receive this message because the number of inputs in .inputnames is not equal to the number of declared inputs.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-19 (error) The clock and reset cannot be on the same input port.

DESCRIPTION

You receive this message because the clock and reset are connected to the same input port.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-21 (error) Too few binary inputs exist (line: %d).

DESCRIPTION

You receive this message because the number of binary input variables is less than the number of input columns in the state table.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-22 (error) Too many binary inputs exist (line: %d).

DESCRIPTION

You receive this message because the number of binary input variables is larger than the number of input columns in the state table.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-23 (error) Binary input has the invalid character %c (line: %d).

DESCRIPTION

You receive this message because the binary input is the specified invalid character. The only valid values are **0**, **1** and **-**.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-24 (error) The compiler cannot read the present state

(line: %d).

DESCRIPTION

You receive this message because the compiler cannot read the present state from the state table file.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-25 (error) Illegal present state %s exists (line: %d).

DESCRIPTION

You receive this message because an illegal present state representation exists. In other words, the specified invalid state representation is **-**, **&**, or **~**.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-26 (error) Compiler cannot read the next state (line: %d).

DESCRIPTION

You receive this message because the finite-state machine (FSM) compiler cannot read the next state from the state table file.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-27 (warning) The next state, %s, is illegal (line: %d).

DESCRIPTION

You receive this message because the next state representation is an illegal

representation. The state specified in the message is **+** or *****.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-28 (error) Compiler cannot read binary outputs (line: %d).

DESCRIPTION

You receive this message because the finite-state machine (FSM) compiler cannot read the binary outputs from the state table file.

WHAT NEXT

Abandon the FSM load.

FSM_IN-29 (error) Too few binary outputs exist (line: %d).

DESCRIPTION

You receive this message because the number of binary output variables is less than the number of the output columns in the state table.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-30 (error) Too many binary outputs exist (line: %d).

DESCRIPTION

You receive this message because the number of binary output variables is larger than the number of output columns in the state table.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_IN-31 (error) Binary output has an invalid character %c (line: %d).

DESCRIPTION

You receive this message because the binary output specified in the message is an illegal representation. It is a character other than **-** or **~**.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_UI-32 (error) Design %s is not a state table.

DESCRIPTION

You receive this message because there is no state table in the design specified in the message.

WHAT NEXT

The finite-state machine (FSM) logic optimization, state minimization, or redundant state removal cannot be completed.

FSM_OUT-32 (error) Design %s is not a state table.

DESCRIPTION

You receive this message because there is no state table in the design specified in the message.

WHAT NEXT

Abandon dumping the finite-state machine (FSM).

FSM_EX-34 (error) The design must have only input and output

ports.

DESCRIPTION

You receive this message because the port type of the design must be input or output and cannot be inout and three-state.

WHAT NEXT

Abandon the finite-state machine (FSM) extraction.

SEE ALSO

extract (2).

FSM_OUT-34 (error) The design can have only input and output ports.

DESCRIPTION

You receive this message because the finite-state machine (FSM) can have only input and output ports. It cannot have any inout or three-state ports.

WHAT NEXT

Abandon dumping the FSM.

FSM_COMP-36 (warning) All existing encodings are ignored for the %s encoding style.

DESCRIPTION

You receive this message because the finite-state machine (FSM) compiler is using the state encoding style set up by the **set_fsm_encoding_style** command.

SEE ALSO

set_fsm_encoding_style (2).

FSM_COMP-37 (warning) Number of state bits is reset to %d to encode %d states for the %s encoding style.

DESCRIPTION

You receive this message because the size of the state vector does not match the number of state bits.

WHAT NEXT

The finite-state machine (FSM) compiler automatically makes up a new state vector.

FSM_COMP-38 (warning) Length of specified encodings is extended to match number of state bits.

DESCRIPTION

You receive this message because the number of bits of the state vector is larger than the number of bits of the existing encodings.

WHAT NEXT

Pad the encodings with zeros.

FSM_COMP-39 (warning) The number of state bits is reset to the length of the specified encodings.

DESCRIPTION

You receive this message because the number of bits of the state vector is too small.

WHAT NEXT

Make a new state vector with the same number of bits as the existing encodings.

FSM_COMP-40 (error) Cannot perform the %s encoding on

more than 30 bits.

DESCRIPTION

You receive this message because the number of bits of the encoding is larger than 30, and the encoding style is not **one_hot**.

WHAT NEXT

Abandon the finite-state machine (FSM) extraction.

SEE ALSO

extract (2).

FSM_EX-47 (error) Cannot extract the design when the state vector is partially reset.

DESCRIPTION

You receive this message because some of the sequential elements have reset and some of them have not. In a finite-state machine (FSM), every sequential element should reset, or no sequential elements can enter the rest phase.

WHAT NEXT

Abandon the finite-state machine (FSM) extraction.

SEE ALSO

extract (2).

FSM_EX-48 (error) Invalid reset for the state vector %s.

DESCRIPTION

You receive this message because, for the finite-state machine (FSM), each sequential element can have only one of the asynchronous controls. A generic sequential element has the following four asynchronous controls: **SEQ_F00**,**SEQ_F01**,**SEQ_F10**, and **SEQ_F11**.

WHAT NEXT

Abandon the finite-state machine (FSM) extraction.

SEE ALSO

extract (2).

FSM_EX-49 (error) The multiple clock signals %s and %s are not allowed.

DESCRIPTION

You receive this message because multiple clock signals are not allowed for a finite-state machine (FSM).

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_EX-50 (error) Multiple clock phases are not allowed.

DESCRIPTION

You receive this message because, in a finite-state machine (FSM), all sequential elements should have the same clock phase, whether rising or falling.

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_EX-51 (error) The multiple reset signals %s and %s are

not allowed.

DESCRIPTION

You receive this message because, in a finite-state machine (FSM), all sequential elements should connect the same reset signal.

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_EX-52 (error) Multiple reset phases are not allowed.

DESCRIPTION

You receive this message because, in a finite-state machine (FSM), all sequential elements should have the same rest phase, whether rising or falling.

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_EX-53 (error) The multiple drivers on the %s network are not allowed.

DESCRIPTION

You receive this message because no driver of the multiple driver net is allowed for a finite-state machine (FSM).

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_EX-54 (error) The state vector element %s has illegal %s logic.

DESCRIPTION

You receive this message because a reset or a clock has illegal combinational logic.

WHAT NEXT

Abandon the finite-state machine (FSM) extraction.

SEE ALSO

extract (2).

FSM_EX-55 (error) Net %s on the %s network has no drivers.

DESCRIPTION

This message is not used.

FSM_EX-56 (warning) The state vector for the state table extraction is not specified.

DESCRIPTION

You receive this message because the state vector is not specified.

WHAT NEXT

The state vector is generated directly from the network by searching for all sequential elements in the network, and it uses sequential element names as the elements of the state vector.

FSM_EX-57 (warning) Assuming that all noncombinational cells are the state vector.

DESCRIPTION

You receive this message because all noncombinational cells in the network are the state vector cells.

FSM_EX-58 (error) The design has no flip-flop instances.

DESCRIPTION

You receive this message because the network has no flip-flop.

WHAT NEXT

Abandon the finite-state machine (FSM) extraction.

SEE ALSO

extract (2).

FSM_EX-59 (error) The state vector cell %s is not in the design.

DESCRIPTION

You receive this message because the finite-state machine (FSM) compiler cannot find the state vector cell in the network.

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_GRP-59 (warning) The state vector cell %s is not in the

design.

DESCRIPTION

You receive this message because the finite-state machine (FSM) compiler cannot find the state vector cell in the design.

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_EX-60 (warning) The design has an invalid noncombinational cell %s.

DESCRIPTION

You receive this message because the design (from which the state table is to be extracted) has a noncombinational cell that is neither a latch nor a flip-flop.

WHAT NEXT

If the design was created using the **group** command with the **-fsm** option, use the **ungroup** command to ungroup the design. Next, mark all cells on which this error message was issued with the **dont_touch** attribute. Finally, use **group -fsm** to create a design from which the state table can be successfully extracted.

SEE ALSO

extract (2), **group** (2), **ungroup** (2).

FSM_EX-61 (error) The state vector cell %s is not clocked.

DESCRIPTION

You receive this message because the state vector cell specified in the message is not clocked. There is no cell driver in the clock pin of the sequential element.

WHAT NEXT

Abandon the finite-state machine (FSM) extraction.

SEE ALSO

extract (2).

FSM_EX-62 (error) No state encodings are provided for the design, so the state vector cannot be longer than 8.

DESCRIPTION

You receive this message because state encodings are not provided. When this occurs, the finite-state machine (FSM) compiler generates all possible state encodings and the state vector becomes too large. When the state vector bit size is larger than 8, you should abandon the FSM extraction because 2^8 is too large.

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_EX-63 (warning) No state names are provided for design. They are automatically generated.

DESCRIPTION

You receive this message because no state encoding is provided, so no state names are provided.

WHAT NEXT

The finite-state machine (FSM) compiler automatically generates all state names (for example, S0, S1, S2, ...).

FSM_EX-64 (warning) No state encodings are provided for the design.
All possible state codes are used.

DESCRIPTION

You receive this message because all possible state codes are used.

FSM_EX-65 (error) For extraction, state codes must be specified with the state names.

DESCRIPTION

You receive this message because a state name does not have a state code. Every state must have a specified state code, otherwise the finite-state machine (FSM) cannot be correctly extracted .

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_EX-66 (error) The reset state code %s is not for a valid state.

DESCRIPTION

You receive this message because the reset state code does not represent the code of a valid state.

WHAT NEXT

Abandon the The finite-state machine (FSM) extraction.

SEE ALSO

extract (2).

FSM_VER-68 (error) The two state machines you specified do not have the same number of ports.

DESCRIPTION

You receive this error message because the two finite state machines (FSMs) you specified do not have the same number of ports. The tool requires that each FSM have the identical number of ports.

WHAT NEXT

Abandon this FSM verification.

SEE ALSO

extract (2), **read** (2).

FSM_VER-69 (error) The two state machines specified do not have identical ports.

DESCRIPTION

You receive this error message because the port descriptions of the two finite state machines (FSMs) you specified have to be identical, but they are not. The items in the port descriptions that must be identical are

- The number of the ports on each state machine
- The bus widths
- The port names

WHAT NEXT

Abandon this FSM verification.

SEE ALSO

extract (2), **read** (2).

FSM_VER-70 (error) The two state machines you specified do not have the same number of states.

DESCRIPTION

You receive this error message because you specified two state machines that do not have the same number of states or the states named do not have the same names in each finite state machine (FSM). The FSM verification package supports verification only on state machines that have the identical number of states and identical state names.

WHAT NEXT

Abandon this FSM verification.

SEE ALSO

extract (2), **read** (2).

FSM_VER-71 (error) The two state machines you specified do not have identical states.

DESCRIPTION

You receive this error message because the state names of the two finite state machines (FSMs) you specified are not identical. The tool requires that the state names be identical.

WHAT NEXT

Abandon this FSM verification.

SEE ALSO

extract (2), **read** (2).

FSM_VER-72 (error) The two state machines you specified are not equivalent.

DESCRIPTION

You receive this error message because the two state machines you specified are not equivalent. This do not necessarily mean that the simulation will fail. This might be because the FSM verification package provided with Design Compiler does not support such FSM verification, for example, two FSMs having a different number of states.

WHAT NEXT

Use Formality to verify the designs. Or reimplement the design with option *hdlin_infer_fsm=false*.

SEE ALSO

extract (2), **read** (2).

FSM_VER-73 (information) The two state machines you specified are equivalent.

DESCRIPTION

You receive this message to let you know that the two finite state machines (FSMs) you specified are equivalent and the verification is successful.

WHAT NEXT

This message is for your information only and does not require any further action on your part.

FSM_EX-74 (error) Compiler cannot convert flip-flops to generic FFGEN.

DESCRIPTION

You receive this message because the finite-state machine (FSM) compiler cannot convert flip-flops into generic FFGEN. For the FSM extraction, all flip-flops must be converted to generic FFGEN, which means that all synchronous controls are

converted into combinational logic.

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_EX-75 (error) The specified state encodings are inconsistent with the length of state vector.

DESCRIPTION

You receive this message because the length of all encodings must be consistent with the length of the state vector.

WHAT NEXT

Abandon the finite-state machine (FSM) extraction.

SEE ALSO

extract (2).

FSM_COMP-76 (error) Encoding length of %d bits is too few to encode %d states.

DESCRIPTION

You receive this message because the (**number_of_encoding_bit**)^2 is less than **number_of_states**. For example, if a finite-state machine (FSM) has nine states, but the encoding is only 3-bit, the 3-bit encoding cannot represent nine states.

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_COMP-77 (warning) State assignment used %d bits and is truncating the state vector.

DESCRIPTION

You receive this message because the length of the resultant encoding is less than the maximum number of the state vector bits.

WHAT NEXT

Truncate the state vector.

FSM_IN-78 (error) Unknown port %s in .field statement (line: %d).

DESCRIPTION

You receive this message because the finite-state machine (FSM) compiler cannot find the port name specified in the message in the 'input_set' and 'input_set' generated from 'stdb_get_input_port_order' and 'stdb_get_input_port_order.

WHAT NEXT

Abandon the FSM load.

FSM_IN-79 (error) Invalid order of the input and output ports at %s (line: %d).

DESCRIPTION

You receive this message because the order of the input and output ports is not correct. In other words, the input and output are mixed. For example, this occurs in the following designation: **in0 in1 out0 in2 ...**.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_VER-80 (error) Finite state machine %s preprocess failed and may cause verification failure.

DESCRIPTION

The dont cares are failed to be annotated.

WHAT NEXT

Set fsm_auto_inferring to false, or use Formality to verify.

FSM_ENC-81 (error) Encoding %s has an invalid base specification %s.

DESCRIPTION

You receive this message because the encoding base is invalid. It can be only **binary**, **octagon**, **decimal**, or **hexagon**.

WHAT NEXT

Quit dc_shell.

FSM_ENC-82 (error) Encoding %s has an invalid base specification (line: %d).

DESCRIPTION

You receive this message because the encoding base is invalid. It can be only **binary**, **octagon**, **decimal**, or **hexagon**.

WHAT NEXT

Quit dc_shell.

FSM_ENC-83 (error) Encoding %s has an invalid number specification %s with base %s.

DESCRIPTION

You receive this message because the encoding specified in the message has an invalid bit number according to the encoding base. For example, this error occurs if the base is binary and one of the encoding bits is larger than **1**, like **10012**.

WHAT NEXT

Quit dc_shell.

FSM_ENC-84 (error) Encoding %s has an invalid number specification %s with base %s (line: %d).

DESCRIPTION

You receive this message because the encoding specified in the message has an invalid bit number according to the encoding base. For example, this error occurs if the base is binary and one of the encoding bits is larger than **1**, like **10012**. The only difference between this message and **FSM_ENC-84** is that this message indicates the line number.

WHAT NEXT

Quit dc_shell.

FSM_ENC-85 (error) Encoding %s overflow.

DESCRIPTION

You receive this message because an encoding bit is less than 0.

WHAT NEXT

Abandon the finite-state machine (FSM) extraction.

SEE ALSO

extract (2).

FSM_IN-86 (error) Cannot transition to the next state, which is invalid (line: %d).

DESCRIPTION

You receive this message because the next state representation contains one of the invalid characters **+**’ or **&**.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_GRP-87 (error) No state vector is specified for FSM grouping.

DESCRIPTION

You receive this message because no state vector is specified for finite-state machine (FSM) grouping.

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_EX-88 (error) Cannot extract the design with combinational feedback loops.

DESCRIPTION

You receive this message because the finite-state machine (FSM) compiler cannot extract a design with combinational feedback loops.

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_IN-89 (warning) The state table has zero states.

DESCRIPTION

You receive this message because the state table has zero states.

FSM_VER-90 (error) Finite state machine %s postprocess failed and may cause verification failure.

DESCRIPTION

Can not recover the original state encoding.

WHAT NEXT

Set fsm_auto_inferring to false, or use Formality to verify.

FSM_COMP-92 (warning) The design has zero states, so it is entirely combinational.

DESCRIPTION

You receive this message because there is no sequential element in the design.

WHAT NEXT

The design acts as a combinational design.

FSM_COMP-93 (warning) The design has one state that is

removed, and the design becomes entirely combinational.

DESCRIPTION

You receive this message because there is only one state in the design. The design must have at least two states to be a sequential design and must have zero states to be a combinational design. Since it has one state, that state can be removed so the design can become combinational.

WHAT NEXT

The finite-state machine (FSM) compiler automatically removes the state, so the design becomes combinational.

FSM_UI-94 (warning) State minimization found all states equivalent, so the design is entirely combinational.

DESCRIPTION

You receive this message because all states are equivalent, so the finite-state machine (FSM) is only one state. In other words, it is a combinational design.

FSM_VER-96 (error) Design '%s' requires a single reset state for verification.

DESCRIPTION

You receive this message because you did not specify a single reset state, which is necessary for the finite state machine (FSM) verification.

WHAT NEXT

Abandon this FSM verification.

FSM_VER-97 (error) Design '%s' requires a state vector for

verification.

DESCRIPTION

You receive this error message because you did not provide the state vector for the finite state machine (FSM) verification.

WHAT NEXT

Use the **dc_shell** command **set_fsm_state_vector** to specify the state vector. Or abandon this FSM verification.

FSM_EX-98 (error) One or more starting states are required for extraction using reachability.

DESCRIPTION

You receive this message because the reachable option is set in the finite-state machine (FSM) extraction, so at least one starting state is required.

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_IN-103 (error) Ambiguous output values are specified at lines %d and %d.

DESCRIPTION

You receive this message because ambiguous output values occur at the two lines specified in this error message. For example, this could happen with the following two rows from a state table: 10 S0 S1 00 and 10 S0 S0 00.

WHAT NEXT

Abandon the finite-state machine (FSM) load.

FSM_LINT-104 (warning) The next state in design %s is unspecified for some transitions.

DESCRIPTION

You receive this message because the next state is not specified in the state transitions.

FSM_LINT-105 (warning) The next state in design %s is unspecified for some transitions from state %s.

DESCRIPTION

You receive this message because the next state is not specified in the state transitions. The message is same as that in FSM_LINT-104 except that it also indicates the current state name.

FSM_LINT-106 (warning) Some output values are unspecified in design %s.

DESCRIPTION

You receive this message because at least one of the output cubes is not fully specified.

FSM_LINT-107 (warning) The value of output %s in design %s is unspecified for some transitions from state %s.

DESCRIPTION

You receive this message because at least one of the output cubes is not fully specified. The message is same as that in FSM_LINT-106, except that it also indicates the unspecified output name and the current state name.

FSM_LINT-108 (warning) No transitions from some states are

specified in design %s.

DESCRIPTION

You receive this message because at least one dead state exists in the design specified in the message.

FSM_LINT-109 (warning) No transitions from state %s are specified in design %s.

DESCRIPTION

This warning message occurs when the state specified in the message is a dead state in the design specified in the message. This message is similar to FSM_LINT-108, except that this warning also indicates the name of the dead state.

WHAT NEXT

This is a warning message only. No action is required on your part. The finite state machine (FSM) optimization automatically removes the dead state.

SEE ALSO

FSM_LINT-108 (n).

FSM_LINT-110 (warning) No transitions are specified to some states in design %s.

DESCRIPTION

You receive this message because at least one dead state exists in the design specified in the message.

FSM_LINT-111 (warning) No transitions are specified to state %s in design %s.

DESCRIPTION

This warning message occurs when the state specified in the message is one of the

dead states in the design. This message is similar FSM_LINT-110, except that this message also indicates the name of the dead state.

WHAT NEXT

This is a warning message only. No action is required on your part.

SEE ALSO

FSM_LINT-110 (n).

FSM_LINT-112 (warning)The state graph is disconnected in design %s.

DESCRIPTION

You receive this message because the number of processed states is not equal to the number of states in the finite-state machine (FSM), so at least one state is disconnected in the state graph.

FSM_EX-113 (error) The design is already a state table (STDB).

DESCRIPTION

You receive this message because the finite-state machine (FSM) compiler cannot extract a design that is already an STDB.

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_EX-114 (warning) Extraction resulted in a state table with

no rows.

DESCRIPTION

You receive this message because the extracted finite-state machine (FSM) compiler resulted in a state table with no rows.

FSM_IN-115 (warning) The state table contains no rows.

DESCRIPTION

You receive this message because no rows exist in the state table.

FSM_COMP-115 (warning) State table contains no rows.

DESCRIPTION

You receive this message because the state table is empty or the design does not have the st format.

WHAT NEXT

Keep the design unchanged.

FSM_OUT-115 (warning) State table contains no rows.

DESCRIPTION

You receive this message because there are no rows in the state table.

FSM_EX-116 (error) The asynchronous reset signal %s cannot drive the combinational logic of the state machine.

DESCRIPTION

You receive this message because the signal '%s' is an asynchronous signal that is used to reset the state machine to a certain start state, and this signal must fanout only to the state vector elements in the design (from which the state table

is to be extracted).

WHAT NEXT

If the design was created by using the **group** command with the **-fsm** option, use the **ungroup** command to ungroup the design. Next, examine the fanout of the reset signal specified in the message. All combinational gates (in the fanout of this reset signal) that do not transitively fanout to the asynchronous pins of the state vector flops must be marked with the **dont_touch** attribute. Finally, execute **group -fsm** to create a design from which the state table can be successfully extracted.

SEE ALSO

group (2), **ungroup** (2).

FSM_EX-117 (error) The clock signal %s cannot drive the state machine’s combinational logic.

DESCRIPTION

You receive this message because the signal specified in the message must fanout only to the state vector elements in the design.

WHAT NEXT

Abandon the finite-state machine (FSM) extraction.

SEE ALSO

extract (2).

FSM_EX-126 (error) Cannot extract the multiple clocks feeding the state vector element %s.

DESCRIPTION

You receive this message because the "clocked_on_also" must be driven by the same pi as "clocked_on" and must be in inverted phase.

WHAT NEXT

Abandon the finite-state machine (FSM) extraction.

SEE ALSO

extract (2).

FSM_EX-127 (warning) The extraction is too expensive.

DESCRIPTION

You receive this message because the finite-state machine (FSM) compiler cannot build the BDD because the network is too large.

WHAT NEXT

Discard the BDD formulas for the network, and abandon the FSM extraction. See the subsequent FSM_EX-144 message for the name of the finite state machine.

FSM_IN-129 (error) The use of the percent operator has resulted in an ambiguous specification.

DESCRIPTION

You receive this message because the on_set and off_set covers overlap, so the use of the percent operator results in an ambiguous specification.

WHAT NEXT

Abandon the finite-state machine (FSM) PLA build.

FSM_VER-130 (error) The length of the encoding of the initial state of design '%s' is inconsistent with the length of the state vector.

DESCRIPTION

You receive this error message because the number of elements of the state vector you specified is not equal to the number of bits of the initial state encoding. The tool requires that these two numbers be the same.

WHAT NEXT

Abandon this FSM verification.

FSM_IN-131 (warning) Compiler ignores the row at line %d, since previous row(s) containing the percent operator cover all input conditions implied by this row.

DESCRIPTION

You receive this message because the previous row(s) already containing the percent operator (%) provide for all input conditions implied by this row.

FSM_VER-132 (error) The two designs you specified must be netlists for verification.

DESCRIPTION

You receive this error message because you did not specify two designs that are both mapped netlists, which the tool requires for verification. The designs cannot be generic GTECH netlists or statetable.

WHAT NEXT

Abandon this FSM Verification.

FSM_EX-133 (warning) Ignoring missing state vector cell %s.

DESCRIPTION

Cannot find a state vector cell in the network.

WHAT NEXT

Ignore the missing state vector cell.

FSM_EX-134 (error) You must specify the state vector for the

state table extraction.

DESCRIPTION

You receive this message because the state vector must be specified in the extracting design.

WHAT NEXT

Abandon the finite-state machine (FSM) extraction.

SEE ALSO

extract (2).

FSM_VER-135 (error) Design '%s' must have only input and output ports.

DESCRIPTION

You receive this error message because your design contains inout ports or tristate ports, which the tool does not allow. A finite state machine (FSM) can have only input ports and output ports.

WHAT NEXT

Abandon this FSM verification.

FSM_VER-136 (error) Design '%s' contains invalid non-combinational cell '%s'.

DESCRIPTION

You receive this error message because your design contains an invalid noncombinational cell, which the tool does not support. Every sequential element in the network is part of the state vector. An error occurs if any noncombinational cell cannot belong to the state vector set.

WHAT NEXT

Abandon this FSM verification.

FSM_VER-137 (error) Design '%s' contains combinational feedback loops.

DESCRIPTION

You receive this error message because the named design contains combinational feedback loops. The compiler does not allow finite state machines (FSMs) to contain combinational feedback loops.

WHAT NEXT

Abandon this FSM verification.

FSM_VER-138 (warning) Ignoring missing state vector cell '%s' in design '%s'.

DESCRIPTION

You receive this warning because the tool cannot find the named state vector cell in the network. The compiler ignores this cell.

WHAT NEXT

This is a warning only. No further action is required on your part.

FSM_EX-140 (error) State encoding %s is invalid for the state %s.

DESCRIPTION

You receive this message because the state encoding specified in the message must be composed of **0** or **1**.

WHAT NEXT

Abandon the finite-state machine (FSM) extraction.

SEE ALSO

extract (2).

FSM_VER-140 (warning) Optimized netlist with non unique state encoding. State name: '%s'.

DESCRIPTION

You receive this warning because the tool optimized one or more state registers away during the FSM optimization. There is no way to verfiy such netlist for Formilty.

WHAT NEXT

This is a warning only. If you try to verfiy the netlist with Formilty, turn off the FSM optmization with fsm_auto_inferring=false

FSM_LINT-141 (warning) The FSM for design %s is large. Consider partitioning the design for better results.

DESCRIPTION

You receive this message because the finite-state machine (FSM) is too large to be extracted.

WHAT NEXT

Abandon the FSM extraction.

SEE ALSO

extract (2).

FSM_EX-141 (warning) The output function for the state %s is too large to be represented.

DESCRIPTION

You receive this message because the output function for the state specified in the message has too many terms in its sum-of-products representation. For example, a parity function obtained by performing the XOR operation on 32 bits of a 32-bit data-bus would have too many terms.

WHAT NEXT

Try to remove the logic corresponding to the complex function from the netlist used for state machine extraction. In other words, make the state machine simpler.

FSM_EX-142 (warning) The transition function for the state %s is too large to be represented.

DESCRIPTION

You receive this message because the transition function for the state specified in the message has too many terms in its sum-of-products representation. The transition function represents the set of all possible input sequences under which the state machine goes from the state specified in the message to any other state. For example, a parity function obtained by performing the XOR operation on 32 bits of a 32-bit data-bus would have too many terms.

WHAT NEXT

Try to remove the logic corresponding to the complex function from the netlist used for state machine extraction. In other words, make the state machine simpler.

FSM_LINT-142 (warning) The FSM size is large. Consider partitioning your original design.

DESCRIPTION

You receive this message because the finite-state machine (FSM) size is very large. The offset cannot be generated for two-level logic optimization, but the FSM is still extracted.

WHAT NEXT

Consider partitioning your original design.

SEE ALSO

extract (2).

FSM_RED-143 (information) The FSM has %d cubes which

exceeds the limit of %d so the reduce_fsm command is too expensive and is unable to complete execution.

DESCRIPTION

This information message occurs when the combinational logic of the finite state machine (FSM) contains a number of cubes that is too large.

The **reduce_fsm** command cannot complete execution.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

reduce_fsm (2).

FSM_LINT-143 (error) The number of outputs in the state table is %d but the number of outputs in the design is %d.

DESCRIPTION

You receive this message because the state table for the *current design* has a different number of outputs than the design. This inconsistent state might have been caused by unconnected output ports in the design.

WHAT NEXT

Examine all previous finite-state machine (FSM) and FSM_LINT warnings and make necessary changes to the design or script to eliminate them. Abandon the finite-state machine (FSM) extraction.

FSM_EX-144 (information) The finite state machine %s has been extracted.

DESCRIPTION

You receive this message because a finite-state machine (FSM) has been successfully extracted.

FSM_EX-145 (information) The finite state machine %s cannot be extracted.

DESCRIPTION

You receive this message because a finite-state machine (FSM) has not been successfully extracted.

FSM_EX-146 (information) The finite state machine %s has been extracted with the same encoding style.

DESCRIPTION

You receive this message because a finite-state machine (FSM) has been extracted with the same encoding style and is going to be extracted twice.

FSM_EX-147 (warning) FSM auto-optimization skipped.

DESCRIPTION

You see this warning about your design because of one of the following reasons:

o The tool can not find the named state register in the current design.

o All state registers are directly driven by other registers, which only drive state registers. In that case, inferring FSM cannot simplify any next-state function.

o Any state register is a scan register.

WHAT NEXT

If you really need to infer the FSM, use the old FSM extraction flow.

SEE ALSO

fsm_auto_inferring (3).

FSM_LINT-151 (warning) The output port %s has no drivers.

DESCRIPTION

You receive this message because the output port specified in the message is ignored for all finite-state machine (FSM) operations.

FSM_LINT-152 (warning) Please use new developed FSM optimization features, and see the ’man fsm_auto_inferring’ command man page for further details.

DESCRIPTION

This message indicates that the command is obsolete. The new developed FSM package covers this feature.

WHAT NEXT

See the man page, using ’man fsm_auto_inferring’.

SEE ALSO

man fsm_auto_inferring

FV-1 (error) The design to align '%s' is not in the original hierarchy.

DESCRIPTION

The subdesign with the given pathname does not exist in the original design hierarchy.

WHAT NEXT

Refer to the Design Compiler Manual for the correct syntax of all set_compare_design_script options.

FV-2 (warning) These endpoints are driven by combinational feedback loops. They will be set to logic zero during verification.

DESCRIPTION

Verification will fail on an endpoint pair (e1, e2) if a feedback loop drives e1 but not e2 (or vice versa) unless e2 happens to be logic zero. Therefore, the software sets to logic zero any endpoint that is found to be driven by a combinational feedback loop.

WHAT NEXT

Other endpoints in the subdesign will be verified as usual. You should inspect any failures occurring on other endpoints.

FV-3 (info) Setting input port '%s' to logic %s in design %s. The 'test_hold' attribute has value %d.

DESCRIPTION

The **test_hold** attribute is on the input port mentioned. In order to verify the designs in "mission" mode as opposed to test mode, the input port is assigned a constant logic value opposite to the value of the **test_hold** attribute.

WHAT NEXT

If the **test_hold** attribute is present on the original and the optimized designs, then the user can optionally remove the attributes before verification. Thus mission mode and test mode will both be checked for functional equivalence.

FV-4 (error) This message is not currently used.

DESCRIPTION

WHAT NEXT

FV-5 (error) Cannot find cell in original design with name '%s'.

DESCRIPTION

WHAT NEXT

FV-6 (info) Setting JTAG Instruction Register outputs to logic one in design '%s'.

DESCRIPTION

This assignment is done for verification purposes only. It has the effect of logically eliminating the Boundary Scan Registers from the design. The original design is not modified.

WHAT NEXT

Verification distinguishing vectors should not mention BSR source or end points.

FV-7 (info) Ignoring JTAG Test Data Out port in design '%s'.

DESCRIPTION

The test data out port does not appear in the original design.

WHAT NEXT

Verification distinguishing vectors should not mention the Test Data Out end point.

FV-8 (warning) No JTAG Test Data Out port was found.

DESCRIPTION

There is usually exactly one JTAG Test Data Out port. It is allowed for the user to remove it manually.

WHAT NEXT

FV-12 (info) Setting scan input port '%s' to logic %s in design %s.

DESCRIPTION

compare_design is intended to to compare an original design (with no test attributes) against a scanned design with test attributes (the result of **insert_test**).

In this recommended methodology, verification puts the scanned design into "mission" mode, as opposed to test mode, by assigning logical constants to certain input ports. Logic zero is assigned to input ports with the attributes: **test_scan_enable**, **test_scan_clock**, **control_point_enable**. Logic one is assigned to input ports with the attributes: **test_scan_enable_inverted**, **control_point_enable_inverted**. Thus, some test logic is disabled during verification and will not be functionally verified.

Current Limitations: Verification does not verify the clocking logic of LSSD scan registers.

WHAT NEXT

If the user wants to violate the recommended methodology and verify one scanned design against another scanned design, then the test attributes must be removed from both designs. The output ports must be in one-to-one name correspondence, or the **set_compare_design_script -ignore** command must be used to ignore endpoints unique to each design. Verification now compares the two designs for equivalence, including both mission mode and test mode.

Moreover, the user always has the option to apply **set_logic_zero** or **set_logic_one** (before **compare_design**) to selected input ports in order to limit the scope of verification.

FV-13 (warning) Verification failures may be caused by the level_sensitive
or clocked_on_also attribute on port '%s'.

DESCRIPTION

Some verification failures occur because input clock ports have have the **level_sensitive** attribute or the **clocked_on_also** attribute.

For example, if MCK is a clock port (the master clock) then the command **set_signal_type "clocked_on_also" MCK -level_sensitive** sets MCK port attributes. These tell **compile** that the design has MS (Master/Slave) latches. **Compile** transforms all flip-flops into MS latches. Because the **level_sensitive** attribute is set, MCK is their master clock. Inferred clocks are slave clocks.

Associated verification failures involve endpoints that are MS latch "clocked_on" pins or inputs to hierarchical cells leading to "clocked_on" pins.

Compile infers MS latches with inferred clocks connected to "clocked_on" pins and signals identified by **set_signal_type** commands connected to "clocked_on_also" pins. Failures occur because translation switches these connections when **level_sensitive** attributes are set.

The failures should be ignored because they are side-effects of the way compile supports MS latches.

WHAT NEXT

Examine the clock logic with the **Design Analyzer** manually. Signals with set **level_sensitive** attributes should be connected to MS latch "clocked_on" pins.

FV-14 (error) The following involve unconnected endpoints:

DESCRIPTION

In the messages that follow this one, the first endpoint is from the original design and the second is from the optimized design. This error message informs the user that an unconnected endpoint is being compared to a connected endpoint. This causes a verification failure. A connected endpoint is categorized by its net connection. The categories are: connected to ground, connected to power, and connected to non-constant net.

WHAT NEXT

Examine the design for unconnected primary outputs and for unconnected inputs to sequential cells.

FV-15 (error) Could not align these output ports in %s design '%s':

DESCRIPTION

Alignment has failed during **compare_design** to align all output ports of the two designs. This may happen for two reasons.

1) The two designs cannot not be aligned; perhaps one has more output ports than the other. Verification cannot succeed under these conditions.

2) An inout port is being interpreted differently in the two designs being compared. Verification needs to interpret each inout port as either a sourcepoint or an endpoint. It does this by examining the net connected to the inout port.

If some other driver pin is connected to the net, then the port is interpreted as an endpoint.

If the net has no clear driver pin and more than one inout port connection, then the port with least alphabetical name is interpreted as the sourcepoint, and the others are interpreted as endpoints.

If the inout port is the only possible driver pin, then the inout port is interpreted as a sourcepoint.

WHAT NEXT

Check to see if the inout ports are used differently in the two designs. If so, then verification cannot be completed.

If verification is giving an improper interpretation to the inout ports, the user may consider copying the designs and giving explicit port directions to the ports on the copies. The the copies should be verified. Currently, there is no option to allow the user to indicate the interpretation of an inout port.

FV-16 (info) No logical constant assignments were made to JTAG

pins in design '%s'.

DESCRIPTION

WHAT NEXT

FV-17 (error) Could not align subdesign '%s'.

DESCRIPTION

Automatic alignment could not align the subdesign mentioned. During **compare_design -hier** the instance pathnames in the two hierarchies being compared must be the same.

If this message is issued during an ECO Compiler command, then this subdesign should be aligned explicitly with a subdesign in the other design hierarchy.

The **set_eco_align** command applied to a pair of output ports on the two subdesigns will accomplish alignment of the subdesigns.

WHAT NEXT

If **compare_design -hier** cannot not work because instance pathnames in the two design hierarchies are not the same, then non-hierarchical verification may be attempted, using simply **compare_design**.

FV-18 (Warning) Accepting design '%s' because its DB reference design, '%s', is the same in both hierarchies.

DESCRIPTION

The two design hierarchies share some subdesigns. The user may do this intentionally in order to reduce the time for verification.

Most likely, the user did not intend for the hierarchies to share subdesigns. In this case, the script should be modified so that **uniquify -force** is used after reading the first design and before reading the second design.

For instance, if a hierarchical design is saved before and after **compile**, and later read into **dc_shell**, then the hierarchies will share subdesigns after linking, which is not the user's intention. The **uniquify -force** command is needed to separate the hierarchies during linking and subsequent verification.

Beware that this warning will not be issued during non-hierarchical verification. If the hierarchies share subdesigns, then verification may be linking both designs to subdesigns from just one of the hierarchies. Again, **uniquify -force** is a sure solution to avoid this problem.

WHAT NEXT

FV-19 (error) First design '%s' has %0d subdesigns, but second design '%s' has %0d subdesigns.

DESCRIPTION

The subdesigns of the two designs mentioned cannot be aligned, because there are a different numbers of subdesigns. The user may need to use the **ungroup** command to partially flatten one or both of the design hierarchies.

WHAT NEXT

compare_design and **eco_align_design** require that the two design hierarchies be identical from the top-level down to accepted designs.

The accepted designs must have the same source and end points, after **set_compare_design_script -ignore** or **set_compare_design_script -only** has been applied. The designs beneath the accepted designs are automatically accepted and not verified.

FV-20 (error) Could not open file: '%s'.

DESCRIPTION

A command tried to open a file for writing, but failed.

WHAT NEXT

Make sure that you have write permission in this directory. If the file already exists in the directory, make sure that you have write permission for that file.

If the permissions are OK, try NOT using the '~' (tilde) character. Some file manipulation functions do not accept path names that start with the tilde character. Try using absolute paths or relative paths instead.

FV-21 (error) This message is not currently used.

DESCRIPTION

WHAT NEXT

FV-22 (warning) Cell '%s' is an empty subdesign in design '%s'. The inputs of the cell will be ignored, not treated as verification endpoints.

DESCRIPTION

If a cell in a design instantiates an empty subdesign (no cells and no nets) then verification will treat the subdesign as a black-box, whose outputs are considered sourcepoints for downstream endpoints.

The input pins are ignored, not treated as endpoints, because the subdesign is empty and functional differences at the input pins could not affect real design endpoints.

It is likely that verification errors will occur and that the subdesign output pins will be mentioned in the report. The most likely explanation is that only one of the design arguments to **compare_design** contains the empty subdesign. The output pins are effectively undriven nets in one of the designs.

WHAT NEXT

Make sure that you really want to have an empty subdesign present.

If so, restrict yourself to comparing two designs whose empty subdesigns are in one-to-one name correspondence, so that the sourcepoints are alignable during verification.

FV-23 (info) This message is not currently used.

DESCRIPTION

WHAT NEXT

FV-24 (warning) The two designs have the same DB reference.

DESCRIPTION

WHAT NEXT

FV-25 (info) Interpreting ’%s’ in %s design as %s.

DESCRIPTION

The interpretation during verification of the mentioned source or endpoint is determined by its net connection. The interpretation may be unexpected by the user because of the declared direction of the point.

For example, if a net is connected to an output port, to input pins of combinational cells, and has no other driver, then verification interprets the output port as a verification sourcepoint because it is used as the driver of combinational logic. This situation may or may not be erroneous in the user’s opinion.

This message may also be issued in cases where the driver of the net is ambiguous. A pass-thru net is an example of this.

WHAT NEXT

The user should examine the designs being compared and make sure that the input and output ports are used as intended.

FV-26 (error) Scan style ’%s’ not supported in compare_design or compile."

DESCRIPTION

The specified scan style attribute on the mentioned design is not supported.

Currently, verification supports the clocked_scan and the multiplexed_flip_flop styles.

WHAT NEXT

FV-27 (info) Using non-hierarchical verification because of boundary optimization.

DESCRIPTION

If the boundary_optimization attribute is present on any hierarchical block in the design, then **compare_design** flattens both design hierarchies just prior to verification; that is, after applying the **set_compare_design_script** commands. In the event that the script commands cannot be applied, because the design hierarchies are not identical, then the user must apply **ungroup -all** to both designs and re-write the script to apply to the flattened designs.

WHAT NEXT

If the user knows that boundary optimization was only applied to certain designs, then it may be possible to **ungroup** those affected designs; the user can then remove the boundary_optimization attribute from all of the hierarchical blocks in the design, in order to allow hierarchical verification to proceed.

FV-28 (error) Original and optimized designs have different scan styles: '%s' '%s'.

DESCRIPTION

The two designs must either have the same scan style, as determined by **set_test_methodology**, or one design must have no scan style.

WHAT NEXT

FV-29 (info) Using non-hierarchical verification because of scan

insertion.

DESCRIPTION

Scan insertion changes the hierarchical boundaries of subdesigns.

WHAT NEXT

FV-30 (error) This message is not currently used.

DESCRIPTION

WHAT NEXT

FV-31 (error) Cannot find the clock pin on the sequential cell '%s'.

DESCRIPTION

WHAT NEXT

Make sure that every sequential cell in the library has a clock pin designated.

FV-32 (warning) Discarding Dont-Care information on DB subdesign '%s'.

DESCRIPTION

This warning is usually issued when the design arguments to **compare_design** are in the wrong order.

Dont-Care information is sometimes automatically annotated on a DB design by the **read** command. This information is later used during **compile** and verification. **Compare_design** utilizes the Dont-Care information annotated on the first design, called the original design. **Compare_design** discards any Dont-Care information annotated on the second design, called the optimized design.

Compare_design is intended to compare an original design, before **compile**, against an optimized design, the result of **compile**. If the optimized design is a result of

compile, it will have no Dont-Care information on it.

The user is permitted to compare two designs with Dont-Care information, for instance two unoptimized designs, but the Dont-care information on the second design will be discarded. In this case, **compare_design** is effectively checking whether the second design (without its Dont-Cares) is a valid implementation of the first design (considering its Dont-Cares).

WHAT NEXT

Check the order of the arguments to **compare_design**. Switch them if necessary and re-execute.

FV-33 (error) Could not open fv_report file.

DESCRIPTION

WHAT NEXT

FV-34 (error) This message is not currently used.

DESCRIPTION

WHAT NEXT

FV-38 (error) Cannot find port or combinational cell '%s' in design '%s'.

DESCRIPTION

The port does not exist in the specified subdesign.

WHAT NEXT

Check that the pathname of the design is correct in the **set_compare_design_script** command.

FV-39 (error) Null token in pathname '%s'.

DESCRIPTION

A pathname may not contain consecutive slash characters.

WHAT NEXT

Examine the **set_compare_design_script** history for improper pathnames, or the sequential cell instance names (if using **insert_clock_tree**). See the *Design Compiler Family Reference Manual*.

FV-40 (error) Cannot find cell '%s' in design '%s'.

DESCRIPTION

The cell does not exist in the specified design.

WHAT NEXT

Examine the **set_compare_design_script** history for improper pathnames. See the *Design Compiler Family Reference Manual* on pathname specifications for **set_compare_design_script**.

FV-41 (error) Cannot find pin '%s' on hierarchical cell '%s' in design '%s'.

DESCRIPTION

The pin on the hierarchical cell does not exist within the specified design.

WHAT NEXT

Examine the **set_compare_design_script** history for improper pathnames. See the *Design Compiler Family Reference Manual* on pathname specifications for **set_compare_design_script**.

FV-42 (error) The name '%s' is a pathname, not a port,

sequential cell, or cell/pin name.

DESCRIPTION

The name of a verification point must be a port name, sequential cell name, or a hierarchical cell name followed by a slash and a pin name.

WHAT NEXT

See the *Design Compiler Family Reference Manual* on command syntax for **set_compare_design_script**.

FV-43 (error) There are no exact name matches in subdesign '%s' for:

DESCRIPTION

The **-accept** option of **set_compare_design_script** asserts that there is a one-to-one name correspondence between input and output ports of two subdesigns. The **-ignore** and **-only** options may be used earlier in order to eliminate some output ports from consideration.

WHAT NEXT

FV-45 (error) Expecting an instance pathname of subdesign, or '%s';
not '%s'.

DESCRIPTION

The first two names in this **set_compare_design_script** entry must be instance pathnames of subdesigns or the placeholder "null". In the **-only** and **-ignore** options, only one of the pathnames may be null. The placeholder is used to indicate that the option should not be applied to one of the designs being compared.

For the **-accept** option, "null" is not allowed as an instance pathname; the top-level designs may have different names; and, the instance pathnames below the top-level designs must be the same.

WHAT NEXT

If the **-accept** option is failing, make sure that the instance pathnames mentioned in the option exist in both designs.

FV-46 (error) Cannot find design hierarchy '%s'.

DESCRIPTION

The design hierarchy in the following **set_compare_design_script** entry is not a current argument to **compare_design**.

WHAT NEXT

See the *Design Compiler Family Reference Manual* for pathname specifications for **set_compare_design_script**.

FV-47 (error) Cannot find instance '%s' within design '%s'.

DESCRIPTION

The instance does not exist within the specified design.

WHAT NEXT

See the *Design Compiler Family Reference Manual* for pathname specifications for **set_compare_design_script**.

FV-48 (error) List of points to align does not have even number of names.

DESCRIPTION

After the first two pathnames in an **-align** option, the point names should be in pairs. The first point will be aligned with the second point in each pair.

WHAT NEXT

FV-49 (warning) Subdesign '%s' being accepted more than

once.

DESCRIPTION

The **set_compare_design_script history contains a redundant -accept** option for the specified design. This may be caused by a subdesign being accepted that is a descendant of another already accepted design. There is no run time or memory penalty associated with this warning.

WHAT NEXT

Review the script to make sure that all the subdesign comparisons desired will be performed.

FV-50 (error) The list of designs to accept does not have even number of names.

DESCRIPTION

The design pathnames in the **-accept** and **-compare** options should be in pairs. For each pair, the input and output ports of the first (original) design are aligned with the input and output ports of the second (optimized) design.

WHAT NEXT

FV-51 (error) These points appear more than once in following -invert_phase option for design '%s':

DESCRIPTION

A point may not have its phase inverted more than once by the commands in the **compare_design** script. The repetition exists within a single **invert_phase** option list.

WHAT NEXT

FV-52 (error) These points appear more than once in -

invert_phase lists for design ’%s’:

DESCRIPTION

A point may not have its phase inverted more than once by the commands in the **compare_design** script. The repetition involves more than one **invert_phase** option list.

WHAT NEXT

FV-53 (error) Cannot combine an -only script entry with other -only entries or with an -ignore entry.

DESCRIPTION

The **compare_design** script may not contain more than one **-only** option for a given subdesign. If the **compare_design** script contains an **-only** option for a given subdesign, then it may not contain any **-ignore** options for the same subdesign. The **compare_design** script may contain more than one **-ignore** option for a given subdesign, though one is sufficient and easier to manage.

WHAT NEXT

Edit your **compare_design** script so that it does not combine an **-only** entry with another **-only** entry or with an **-ignore** entry. Then re-execute.

FV-56 (error) No pathname specified in the following script entry:

DESCRIPTION

The first two names in the displayed **set_compare_design_script** entry must be pathnames of subdesigns or the placeholder "null". In the **-only**, **-ignore**, options, at most, one of the pathnames may be null.

WHAT NEXT

Edit your **set_compare_design_script** entry so that the pathname is appropriately specified; then re-execute.

FV-57 (error) Two pathnames specified in %s script entry: ’%s’

’%s’.

DESCRIPTION

The first two names in the following **set_compare_design_scriptP entry must be pathnames of subdesigns or the placeholder "null". In the invert_phase**, **-source_phase_assign**, and **-end_phase_assign** options, one of the pathnames must be null.

WHAT NEXT

FV-58 (error) Cannot process script entry:

DESCRIPTION

Read the preceding error messages for an explanation of this error.

WHAT NEXT

FV-59 (info) Not assigning input scan port ’%s’ in second design, because port is connected in first design.

DESCRIPTION

compare_design assigns a logical constant to a connected input scan port (in the second design) only if the port is absent or unconnected in the first design.

WHAT NEXT

FV-60 (error) Attempted to invert phase of sequential cell with non-complementary outputs: ’%s’.

DESCRIPTION

The Q and QN outputs of the specified sequential cell are not complementary. Possible reasons for this are: 1) The library specifies that the outputs are not complementary; 2) The functions driving the force_00 and force_11 inputs of the degenerated sequential cell are not logical zero. For purposes of verification, every sequential cell is degenerated into a primitive sequential cell. The outputs

(sourcepoints) of the primitive are Q and QN. The inputs (endpoints) of the primitive are next_state, force_00, force_01, force_10, force_11, clocked_on, and clocked_on_also (for Master-slave cells only). The functions driving the force endpoints characterize the asynchronous properties of the primitive sequential cell. The library may also contain an attribute asserting that the outputs Q and QN are complementary. The force_01 function represents the conditions under which the Q pin can be driven to zero and the QN driven to 1 simultaneously. The other force inputs have a similar interpretation. When the attribute is not present, verification tries to determine that Q and QN are effectively complementary by establishing that both force_00 and force_11 are logically zero. The exact degeneration process depends on the library characterization of the sequential cell and is not described here.

WHAT NEXT

FV-61 (error) The point to phase invert is not a port or sequential cell: '%s'.

DESCRIPTION

The only verification points that can be phase inverted are primary or hierarchical boundary ports and sequential cells.

WHAT NEXT

If you want to invert all the outputs of a hierarchical subdesign, you must list the outputs individually.

FV-62 (error) Cannot find sequential cell or port '%s' in design '%s'.

DESCRIPTION

The sequential cell does not exist in the specified design.

WHAT NEXT

See the *Design Compiler Family Reference Manual* on pathname specifications for **set_compare_design_script**.

FV-63 (warning) Some black-box cells exist during verification

DESCRIPTION

Black-box cells may arise during verification for several reasons.

Verification can succeed in the presence of black-boxes, as long as the black-boxes appear in both designs being compared, with the same instance names and pin names.

When verification failures occur the user should consider the following possible explanations:

1) The library does not contain a functional model for the cell. Some libraries contain cells that are intended to be treated as black-boxes during **compile**. The user should be aware of such cells in the link_library.

2) The user has intentionally instantiated a black-box in a design.

3) The functional model has been lost or is not accessible by verification, perhaps due to previous linking problems. The user should look for unresolved reference warnings during **link**.

4) An internal **dc_shell** error has occurred. There is a functional model in the library for the cell but it is not accessible during verification. Such an error should be reported to Synopsys.

5) The black-box is an instantiation of a Xilinx XBLOX macro cell. The functionality of these cells is unknown during verification. Resource Sharing may occur on the operators implemented by these XBNOX cells. When this happens verification will fail because there are different numbers so black-boxes in the original and optimized designs. A possible work-around is for the user to create gate-level models for the instances and re-link the designs.

WHAT NEXT

FV-64 (warning) An inout port has different interpretations in verification:

DESCRIPTION

The port is being interpreted differently in the two designs being compared. This discrepancy may cause verification failures or endpoint alignment problems.

Verification needs to interpret each inout port as either a sourcepoint or an endpoint. It does this by examining the net connected to the inout port.

If some other driver pin is connected to the net, then the port is interpreted as an endpoint.

If the net has no clear driver pin and more than one inout port connection, then the port with least alphabetical name is interpreted as the sourcepoint, and the others are interpreted as endpoints.

If the inout port is the only possible driver pin, then the inout port is interpreted as a sourcepoint.

WHAT NEXT

Check to see if the inout ports are used differently in the two designs. If so, then verification cannot be completed.

If verification is giving an improper interpretation to the inout ports, the user may consider copying the designs and giving explicit port directions to the ports on the copies. The the copies should be verified. Currently, there is no option to allow the user to indicate the interpretation of an inout port.

FV-65 (warning) Ignoring %s option for points in original design '%s':

DESCRIPTION

This option can apply only to points in the optimized design.

WHAT NEXT

If you are comparing a design against a copy of itself (each in its own sub-directory), it should be possible just to exchange the first and second names in this option and exchange the design pathname arguments to **compare_design**.

FV-66 (info) In verifying the %s design, these are treated as %s:

DESCRIPTION

Verification needs to interpret each port, sub-design pin, and register pin as either a sourcepoint or an endpoint. Furthermore, verification needs to determine a single driver for each net in the design, in order to perform combinational logic verification. Usually pin or port directions declared in the design are sufficient to determine source and endpoints, but in some cases (such as multiple driver nets and nets connected to inout pins) verification needs to choose a driver (sourcepoint) and make the other connections endpoints. This message informs the user of verification's choices.

WHAT NEXT

FV-69 (error) This message is not currently used.

DESCRIPTION

WHAT NEXT

FV-70 (error) The endpoint to ignore, '%s', is not an output port, a register, or a hierarchical cell of design '%s'.

DESCRIPTION

If the endpoint is a register or hierarchical cell, then all the input pins on the cell are ignored during verification. If the endpoint is a specific input pin on a register or hierarchical cell, then only that pin is ignored.

WHAT NEXT

Check that the instance pathname for the option exists in the design and that the cell and pins names exist in the mentioned design. Then re-execute.

FV-72 (error) The point to check for redundancy, '%s', in design '%s' is not a source point.

DESCRIPTION

The **-redundancy_check** option can be applied only to source points.

WHAT NEXT

See the *Design Compiler Family Reference Manual* on the **-redundancy_check** option.

FV-73 (error) The original design, '%s', was found to have these

scan ports, illegal in verification:

DESCRIPTION

compare_design uses the **test_scan_out** and **test_scan_out_inverted** attributes to determine the dedicated scan ports in the optimized design. The original design must not contain scan ports. **compare_design** is not intended to compare two designs that have both been modified for testability.

WHAT NEXT

Revise your methodology so that you compare the original designs with each other, and compare each original with each test modified version. Ensure that your original designs do not contain scan ports.

FV-74 (error) Failure in applying set_compare_design_script.

DESCRIPTION

This error will occur when verification is not done hierarchically, but there is a pathname to a subdesign in a **set_compare_design_script** command.

Otherwise, read the preceding error messages for an explanation.

WHAT NEXT

If pertinent, use the **compare_design -hier** or the **compile -verify_hier** option so that the pathnames in the script are present during verification.

FV-75 (warning) The following points in design '%s' were aligned more than once:

DESCRIPTION

The user is allowed to align a verification point more than once, but it is not recommended. The last alignment in the script is used during verification.

WHAT NEXT

FV-76 (warning) The following points were aligned more than

once to points in design '%s':

DESCRIPTION

The user is allowed to align a verification point more than once, but it is not recommended. The last alignment in the script is used during verification.

WHAT NEXT

FV-77 (warning) Realigning point '%s' in design '%s' and unaligning point '%s' in design '%s'.

DESCRIPTION

This message is issued during various ECO Compiler commands. The first point, being realigned, has been aligned previously to another point. The second point, being unaligned, was previously aligned to the first point.

WHAT NEXT

Check the **set_eco_align** command history to make sure that no point is aligned more than once.

FV-78 (error) Cannot align these two points: '%s/%s' and '%s/%s'."

DESCRIPTION

This message is issued during various ECO Compiler commands. Design objects can be aligned only if they are of the same type. The allowed types are (subdesign) port, sequential cell, and pin (on hierarchical cell).

Note: combinational cells cannot be aligned. In order to specify the reuse of a combinational cell, see the ECO Advanced Directive command **set_eco_reuse**.

WHAT NEXT

FV-80 (error) Attempted to align design '%s' with both design

’%s’ and design ’%s’."

DESCRIPTION

A design can only be aligned with one other design.

WHAT NEXT

If this message is issued during **compare_design**, then check the **set_compare_design_script** command history to make sure that no design is aligned more than once, via the **-accept** option.

If this message is issued during an ECO command such as **eco_align_design**, then check the **set_eco_align** command history for the current ECO design pair to make sure that no design is aligned more than once.

When two designs or points are aligned, all the designs along the paths from these two designs to their respective top-level designs are automatically aligned.

FV-81 (error) Cannot ’%s’ designs ’%s’ and ’%s’, at different depths in hierarchies.

DESCRIPTION

In order to **-align**, **-accept**, or **-compare** two designs, they must be at the same depth in their respective design hierarchies.

WHAT NEXT

It may be necessary to **ungroup** some designs above the two mentioned designs in order to make the two design hierarchies have identical tree structures. **compare_design** requires that the two design hierarchies be identical from the top-level down to accepted designs. The accepted designs must have the same source and end points, after **-ignore** options have been applied. The designs beneath the accepted designs are automatically accepted and not verified.

FV-83 (error) In %s design %s, cell ’%s’ is an empty subdesign. In %s design %s, you must ungroup unaligned cell ’%s’.

DESCRIPTION

Verification currently treats subdesigns without any cells or nets as empty and ungroups them internally. Such empty designs can result from **compile** if all internal

logic is optimized away.

WHAT NEXT

Unfortunately, you must perform a parallel ungrouping when comparing the pre-compile and post-compile versions. Rerun **compare_design**.

FV-84 (information) In %s design %s there is %s unique to

DESCRIPTION

The purpose of this message is to help you diagnose the cause of a verification miscompare between endpoints.

Following this message is a list of verification sourcepoints that are unique to its fanin. Unique means that there is no path from the sourcepoints to the endpoint in the other design during verification.

The roles of sourcepoint and endpoint can be swapped, indicating that a sourcepoint has unique fanout.

WHAT NEXT

GDM-001 (Error) Could not get %s record with id %d in Milkyway.

DESCRIPTION

You recieve this error message because an error occured while accessing the Milkyway database for the object of the error type.

WHAT NEXT

please verify if any of the previous commands have modified Milkyway. write out a fresh milkyway database and re-read the design. if the message disappear, check for the previous commands. Contact ICC Infrastructure Team for more help.

GDM-002 (Warning) Failed to iterate over %s objects in Milkyway.

DESCRIPTION

You recieve this error message because an error occured while accessing the Milkyway database for the object of the error type.

WHAT NEXT

please verify if objects of the error type are present Milkyway. write out a fresh milkyway database and re-read the design. if the message disappear, check for the previous commands. Contact ICC Infrastructure Team for more help.

GDM-003 (Error) Could not get MW id from DC object (%s)%s.

DESCRIPTION

You recieve this error message because an error occured while accessing the Milkyway database object corresponding to timing model object of the above type.

WHAT NEXT

please verify if object of the type is present in Milkyway. write out a fresh

milkyway database and re-read the design. if the message disappear, check for the previous commands. Contact ICC Infrastructure Team for more help.

GDM-004 (Warning) Milkyway object (%s)%s with id '%d' not presetn in DC.

DESCRIPTION

You recieve this error message because an error occured while accessing the timing model database for the object of the above type.

WHAT NEXT

please verify if objects of the error type are present Milkyway. write out a fresh milkyway database and re-read the design. if the message disappear, check for the previous commands. Contact ICC Infrastructure Team for more help.

GDM-005 (Error) Name of DC object (%s)%s and Milkyway object (%s)%s is not matching.

DESCRIPTION

You recieve this error message because an error occured while comparing the attributes of Milkyway objects and timing model datastructers.

WHAT NEXT

please verify if objects of the error type are present Milkyway. write out a fresh milkyway database and re-read the design. if the message disappear, check for the previous commands. Contact ICC Infrastructure Team for more help.

GDM-006 (Error) Could not find Milkyway object (%s) by name '%s'.

DESCRIPTION

You recieve this error message because an error occured while accessing the Milkyway database for the object of the above type with specified name‘

WHAT NEXT

please verify if objects of the error type are present Milkyway. write out a fresh milkyway database and re-read the design. if the message disappear, check for the previous commands. Contact ICC Infrastructure Team for more help.

GDM-007 (Error) Multiple MW ids of type (%s) have same name '%s'.

DESCRIPTION

You recieve this error message because an error occured while accessing the Milkyway database for the object of the above type.

WHAT NEXT

please verify if objects of the error type are present Milkyway. write out a fresh milkyway database and re-read the design. if the message disappear, check for the previous commands. Contact ICC Infrastructure Team for more help.

GDM-008 (Error) Milkyway object type is not (%s) for DC object (%s)%s.

DESCRIPTION

You recieve this error message because an error occured while comparing Milkyway object and corresponding Timing model datastructures.

WHAT NEXT

please verify if objects of the error type are present Milkyway. write out a fresh milkyway database and re-read the design. if the message disappear, check for the previous commands. Contact ICC Infrastructure Team for more help.

GDSO

GDSO-1 (error) There is no corresponding GDSII ID for layer '%s' in library.
This design cannot be written out.

DESCRIPTION

You receive this error message because there is missing GDSII-related information in the physical library. Therefore, the **write_gds** command cannot write out the routed design in GDSII format.

WHAT NEXT

Add GDSII-related information to the physical library (plib) file, and rerun the **read_lib** command to generate a pdb file.

EXAMPLE MESSAGE

```
Error: There is no corresponding GDSII id for layer 'MET1" in library.
This design cannot be written out. (GDSO-1)
```

SEE ALSO

write_gds (2).

GDSO-2 (error) There is no geometry information in via '%s'.

DESCRIPTION

You receive this warning message because you executed the **write_gds** command and specified a via that is not properly linked to the library. Therefore, the via instance is not written out.

WHAT NEXT

Verify that the via exists in the physical library. Then, reexecute the command.

EXAMPLE MESSAGE

```
Error: There is no geometry information in via '%s'. (GDSO-2)
```

SEE ALSO

write_gds (2).

GDSO-3 (warning) Cannot find the cell reference in library. Instance '%s' is not written out.

DESCRIPTION

You receive this warning message because you executed the **write_gds** command and specified a design that is not properly linked to the library. Therefore, the instance is not written out.

WHAT NEXT

Verify that the library cell exists in the logic library and physical library. Then, reexecute the command.

EXAMPLE MESSAGE

Error: Cannot find reference '%s' in library. Instance '%s' is not written out. (GDSO-3)

SEE ALSO

write_gds (2).

GDSO-4 (warning) Undefined wire rule %s encountered in db. Wire segment ignored.

DESCRIPTION

You receive this warning message because the specified wire rule is not found in the library. Therefore, the **write_gds** command cannot write out the wire segment.

WHAT NEXT

Verify that the wire rule is not defined in the library. Define the wire rule, and reexecute the **write_gds** command.

EXAMPLE MESSAGE

warning: Undefined wire rule %s encountered in db. Wire segment ignored.

SEE ALSO

write_gds (2).

GDSO-5 (error) The file '%s' cannot be written out due to errors.

DESCRIPTION

You receive this error message because you have executed the **write_gds** command and specified a file that contains errors and, therefore, cannot be written out.

WHAT NEXT

Fix the specified errors, then reexecute the **write_gds** command and specify the file to be written out.

SEE ALSO

write_gds (2).

GDSO-6 (warning) There is no '%s' on instance '%s' of reference '%s'.

DESCRIPTION

You receive this warning message because you executed the **write_gds** command and specified an instance that does not have location (is not placed) or orientation. Therefore, the instance is not written out into a GDSII file.

WHAT NEXT

Check the design and verify that the instances are properly placed.

SEE ALSO

write_gds (2).

GDSO-7 (error) The design does not contain physical

information. Abort.

DESCRIPTION

You receive this error message because you executed the **write_gds** command and specified a design that is not a physical design db because it does not contain physical information.

WHAT NEXT

Check the design and verify that it contains post-route data.

SEE ALSO

write_gds (2).

GDSO-8 (warning) Truncate %s '%s' to %d characters.

DESCRIPTION

You received this warning message because you executed the **write_gds** command and specified a string that exceeds the GDSII string length limit.

WHAT NEXT

Reexecute the **write_gds** command and specify a string that does not exceed the GDSII string length limit.

SEE ALSO

write_gds (2).

GDSO-9 (error) There is no corresponding layer '%s' in library. This design cannot be written out.

DESCRIPTION

This error message indicates that there are missing layer specifications in the physical library. Therefore, the **write_gds** command cannot write out routed designs in GDSII format.

WHAT NEXT

Make sure the physical library matches the design.

EXAMPLE MESSAGE

```
Error: There is no corresponding layer 'MET1" in library.
This design cannot be written out. (GDSO-9)
```

SEE ALSO

write_gds (2).

GEN-1 (error) Cell '%s' instance '%s' pin '%s' has same Y coordinate as cell '%s' instance '%s' pin '%s'.

DESCRIPTION

Two pins of the same cell, or different cells in the same column, are found to overlap. This was probably caused by a problem in either the symbol library being used or in schematic generation. Check the identified pins in your symbol library source to see if they are pins of the same cell and if the same Y coordinate has been defined for them. If so, correct the Y coordinates, recompile the symbol library, and rerun the test. If this is not the case, report this as a bug in schematic generation.

WHAT NEXT

GEN-2 (error) Pin '%s' on Cell '%s' does not lie on a grid.

DESCRIPTION

WHAT NEXT

GEN-3 (warning) Creating a symbol for cell '%s' of type '%s'.

DESCRIPTION

This warning is issued when the *gen_show_created_symbols* dc_shell variable is set to "true" and *create_schematic* can not locate the symbol template for a cell in the database or in any of the symbol libraries. In such a case, *create_schematic* automatically generates a rectangular symbol template to use in the schematic. In general, this is done by putting all the input pins on the left side of the symbol and all other pins on the right side. The size of the generated symbol can be controlled by setting the *gen_max_ports_on_symbol_side* variable to an appropriate value.

WHAT NEXT

If this warning is issued for primitive gates, that may indicate that the *symbol_library* or *search_path* variables have not been set properly. This can be resolved by (1) finding the symbol library (a file with a .sdb suffix) to be used

and appending it to the *symbol_library* variable, and (2) appending its directory path to the *search_path* variable.

Libraries usually don't have symbol templates for hierarchical cells, so this warning should be ignored for such cells.

GEN-4 (error) Could not find pin: '%s', in cell: '%s' in schematic library '%s'.

DESCRIPTION

WHAT NEXT

GEN-5 (error) Symbol library doesn't have off-sheet connectors.

DESCRIPTION

WHAT NEXT

GEN-6 (warning) Symbol exceeds sheet size.

DESCRIPTION

This warning is issued when one of the symbol templates *create_schematic* creates exceeds the size of the sheet being used. This may be caused by either the sheet being too small or there being too many pins on the symbol.

This message is only issued for symbols that have so many pins that *create_schematic* creates a smaller square symbol with all the pins equally distributed along the four sides, and even then this symbol exceeds the sheet size.

WHAT NEXT

If this is of concern, use a larger sheet size. Since *create_schematic* will automatically create the smallest symbol possible for the given number of ports when this message is issued, the only way to make the symbol fit the sheet is to use a larger sheet.

GEN-7 (warning) Maximum ports on symbol side limit of '%d'

exceeded.

DESCRIPTION

WHAT NEXT

GEN-8 (warning) Can’t rename off-sheet connector of net ’%s’
to the name of its port ’%s’
because net ’%s’ already exists.

DESCRIPTION

WHAT NEXT

GEN-10 (warning) Couldn’t find all the port symbols in the generic symbol library.

DESCRIPTION

WHAT NEXT

GEN-11 (error) Couldn’t find pin name ’%s’ in ripper symbol ’%s’.

DESCRIPTION

WHAT NEXT

GEN-12 (error) Couldn’t find a ripper symbol for creating a

bussed schematic.

DESCRIPTION

WHAT NEXT

GEN-13 (error) Annotator '%s' has an invalid format specification '%s'.

DESCRIPTION

WHAT NEXT

GEN-14 (error) An unnamed annotator has an invalid format specification '%s'.

DESCRIPTION

WHAT NEXT

GEN-15 (error) Annotator '%s' has more than %d '%%s' specifications
in the format string.

DESCRIPTION

WHAT NEXT

GEN-16 (error) An unnamed annotator has more than %d '%%s'

specifications in the format string.

DESCRIPTION

WHAT NEXT

GEN-17 (error) Annotator '%s' has an invalid expression '%s'.

DESCRIPTION

WHAT NEXT

GEN-18 (error) An unnamed annotator has an invalid expression '%s'.

DESCRIPTION

WHAT NEXT

GEN-19 (warning) The symbol for cell '%s' has a pin off the route grid.
You may be mixing symbol libraries with different route grids.

DESCRIPTION

This warning is issued when one of the schematic symbols is found to have a pin that is located outside the route grid being used by *create_schematic*, i.e., the pin is somewhere in the middle of the square region defined by the four points around it that represent the intersection of vertical and horizontal grids instead of being on one of the edges or corners. This indicates that the schematic may contain symbols from more than one symbol library and that these libraries specify different route grids. In such a case, *create_schematic* picks up the route grid specified in the first symbol library it runs into, and uses that route grid in the schematic. Any symbols coming from libraries whose route grids do not match the one being used by *create_schematic* are not guaranteed to have their pins aligned with the route grid.

WHAT NEXT

If this is a problem in transferring the schematic to some external environment, try using symbol libraries with the same route grid. If this is not possible, try modifying the route grids in your symbol libraries to match each other. This is done by editing the .slib file and changing the argument to the *set_route_grid()* specification and then recompiling that library with the *read_lib* command.

GEN-20 (error) One of the pins or port busses is corrupted.

DESCRIPTION

This error is issued when one of the design ports or pins is found to have a corrupt bus structure. This can happen sometimes because of inconsistent bus creation by different tools in the design. In such a case, the port or pin that is found to have a corrupt bus structure will be drawn unbussed in the schematic, i.e. its bus will be ignored by *create_schematic*.

WHAT NEXT

If there are no other problems with the tool run, this message should be ignored as *create_schematic* automatically ignores the bus objects responsible for corruption.

GEN-21 (error) Cell %s's pin %s is on wrong side.

DESCRIPTION

WHAT NEXT

GEN-22 (error) Net %s connects pins of different widths.

DESCRIPTION

WHAT NEXT

GEN-23 (warning) The netlist contains bus-to-bus connections. Any
nets involved in inter-bus connections will be

displayed as disconnected in the no-ripper schematic.

DESCRIPTION

WHAT NEXT

GEN-24 (error) Could not find the type mapper symbol in the generic symbol library. The generic symbol library is probably old - Please use a new library and recreate the schematic.

DESCRIPTION

GEN-25 (warning) All cells are power/ground or have no connection.

DESCRIPTION

Cells in the current design are all power cells or all ground cells. Or the cells have no pins.

WHAT NEXT

GEN-26 (error) member '%d not found in bus '%s' . Only following members present : '%s'. The design is corrupted.

DESCRIPTION

WHAT NEXT

GEN-27 (warning) Creating a very large schematic. It is approximately %d wide and %d tall.

Must skip the ’improve’ algorithm due to insufficient memory.

DESCRIPTION

You receive this warning when you are trying to create a schematic for a very large design, but there is not sufficient memory available to perform the "improve" algorithm.

WHAT NEXT

You have available three courses of action:

• You can let the schematic creation continue, with the possibility that it will succeed, if there is enough memory.

• You can monitor the performance, using a UNIX utility such as **top**, to see if you are close to running out of address space.

• You can send an interrupt to the application, which terminates the schematic creation at the next check point in the algorithm.

Because large schematics are difficult to work with graphically, consider whether you really want your schematic to be so large. If you have flattened your design, going back to an unflattened design might be more workable and require less address space.

If it is imperative that you produce the schematic, rerun your application using the 64-bit version (if it is available to you), which has a memory address space limit exceeding 4 gigabytes. The process should eventually succeed, providing you have enough swap space on your machine.

SEE ALSO

create_schematic (2).

GEN-28 (warning) Creating a schematic with an extreme number of sheets.
The schematic being created has %d sheets.
Aborting attempt to create schematic.

DESCRIPTION

You receive this warning because you are trying to create a schematic that has too

many sheets, making it impractical to use. The process is terminated.

WHAT NEXT

You can avoid the issue by choosing a larger sheet size, which will result in fewer sheets: -size A is the smallest sheet size, -size B is larger, and so on, up to -size infinite, which is always just one sheet. For more information about sheet sizes, see the man page for the **create_schematic** command.

SEE ALSO

create_schematic (2).

GLO-1 (error) Program Failure

DESCRIPTION

This message indicates that the program produced an internal error that was not caught by other error handling mechanisms. There is no single reason for the failure. It could be the result of a bad installation of your software; more likely it is due to the tool trying to deal with unexpected data within your design DB.

WHAT NEXT

Make sure that the executable and the root installation are from consistent versions and that your software installation succeeded without error. If this is not the source of the failure, please report your problem to Synopsys

GR-1 (warning) Route %% changed to %3.1f for %s route layers.

DESCRIPTION

You receive this message because the routing percentage data specified was not valid, so it has been changed as described in the message. The route percentage values should sum to 100.0 for each group of routing layers with a common route direction.

WHAT NEXT

Change the route percentage data to a valid value in either the technology library or the PDEF file.

GR-2 (warning) Location-based optimizations disabled because Steiner routing cannot be invoked with too few back-annotations on the design.

DESCRIPTION

You receive this message because technology data, such as the R and C coefficients, cannot be derived. This occurs because there is not enough capacitance, delay, and location back-annotation on the design. Steiner routing cannot function without this data. The result is that location-based optimization (LBO) is not activated. Instead, the wire load model (WLM) is used to determine capacitance and delay of new nets.

WHAT NEXT

For Steiner routing to work, all nets in the design must have capacitance and delay values; and locations must be annotated on all cells.

SEE ALSO

read_pdef (2), **read_sdf** (2), **reoptimize_design** (2), **set_cell_location** (2), **set_load** (2).

GR-3 (warning) Location-based optimizations disabled.

DESCRIPTION

You receive this message because location-based optimization is not activated: it has been disabled. The PDEF file read for the current design contains locations for leaf cells. This typically enables location-based optimization (buffer insertion and removal) to occur. In this case, however, location-based optimization has been explicitly disabled by setting one of the following variables to *false*:

- **compile_ok_to_buffer_during_inplace_opt**,
- **lbo_buffer_insertion_enabled**,
- **lbo_buffer_removal_enabled**.

WHAT NEXT

To enable location based optimization, ensure that the variables listed above are set to *true* in the setup file.

SEE ALSO

compile_ok_to_buffer_during_inplace_opt (3), **lbo_buffer_insertion_enabled** (3), **lbo_buffer_removal_enabled** (3).

GR-4 (info) %s - horizontal: %.2g vertical: %.2g

DESCRIPTION

You receive this message to inform you that capacitance or resistance values are used for the horizontal and vertical routing layers. See the **GR-7** man page for additional information on the unit used for these values.

WHAT NEXT

This is an informational message only. No action is required on your part.

GR-5 (information) Using user-specified R and C coefficients.

DESCRIPTION

You receive this message to inform you that the capacitance and resistance values used for horizontal and vertical routing layers have been specified via user environment variables instead of having been calculated.

WHAT NEXT

This is an informational message only. No action is required on your part.

GR-6 (information) Using edge_capacity_x: %g, edge_capacity_y: %g, gcell_size: %d.

DESCRIPTION

You receive this message to inform you of the specified parameters. See the **run_router** man page for a definition of these parameters.

WHAT NEXT

This is an informational message only. No action is required on your part.

GR-7 (info) The distance unit in Capacitance and Resistance is %s micron.

DESCRIPTION

You receive this message because it provides information on the type of units in use. The unit used for capacitance is library capacitance units per micron. The unit used for resistance is library resistance units per micron.

WHAT NEXT

No action is necessary. The result is informative.

GR-8 (information) Using derived R and C coefficients.

DESCRIPTION

You receive this message to inform you that the capacitance and resistance values used for the horizontal and vertical routing layers are derived from the physical library.

WHAT NEXT

This is an informational message only. No action is required on your part.

GR-9 (info) %s is scaled by %5.2f

DESCRIPTION

You receive this message because it provides information on the type of scaling in use. It indicates the scaling factor for maximum or minimum values of capacitance or resistance coefficients.

WHAT NEXT

No action is necessary. The result is informative.

GR-10 (information) Library Derived %s : %.2g

DESCRIPTION

You receive this message to inform you of the library derived value for the vertical or horizontal capacitance or resistance coefficient.

WHAT NEXT

This is an informational message only. No action is required on your part.

GR-11 (information) User-specified %s : %.2g

DESCRIPTION

You receive this message to inform you of the user-specified value for the minimum or maximum, vertical or horizontal, capacitance or resistance coefficient.

WHAT NEXT

This is an informational message only. No action is required on your part.

GR-12 (information) %s used : %.2g

DESCRIPTION

You receive this message to inform you of the value for the minimum or maximum, vertical or horizontal, capacitance or resistance coefficient used for delay

estimation. Delay estimation is used in placement and routing estimation.

WHAT NEXT

This is an informational message only. No action is required on your part.

GR-13 (information) Using region-based R and C coefficients.

DESCRIPTION

You receive this message to inform you that the value is derived from the region for vertical and horizontal, capacitance and resistance coefficients used for delay calculation during placement and routing estimation. A region roughly corresponds to the net bounding box.

WHAT NEXT

This is an informational message only. No action is required on your part.

GR-14 (warning) Inconsistent between library RC data and extraction parameters

DESCRIPTION

You receive this message because there might be an inconsistency between your library RC data and extraction parameters. If you specify optional extraction parameters, the program can derive the RC data from them based on some normal condition assumptions. If this RC data is substantially different from your library RC data, you receive this warning message.

WHAT NEXT

Use the **report_lib** command with the **-physical** option to determine that your physical library numbers are correct. Ensure that you do not model the polysilicon layer as a routable layer. Note that the program uses only normal condition assumptions to derive RC data from the extraction parameters. Therefore, if you know that your numbers are correct, you can ignore this warning message.

SEE ALSO

report_lib (2). **set_delay_estimation_options** (2).

GR-15 (information) The RC model used is : %s

DESCRIPTION

This informational message describes which RC model the tool will use to compute the unit RC.

Valid RC models are as follows (given from the highest priority to the lowest priority):

- user - user-specified RC parameters
- library extractor based - based on extraction parameters
- 2.5D - based on 2.5D parameters and user-specified routing wire model
- library 2.5D - based on 2.5D parameters
- library 1D - based on 1D parameters

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

extract2plib(1)
set_routing_wire_model(2)
set_delay_estimation_options(2)
PSYN-140(n)
PSYN-143(n)

GR-16 (information) The routing wire model used is : %s

DESCRIPTION

This informational message describes which routing wire model the tool uses to compute the unit RC.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

set_routing_wire_model(2)
GR-15(n)

GR-21 (warning) Layer ’%s’ is not in the ignored layer list.

DESCRIPTION

You get this warning because the layer that you want to remove does not exist in the ignored layer list.

WHAT NEXT

Check ignored layer list using command "report_ignored_layers" to get the ignored layer list and only apply those layers in this command.

GR-22 (warning) Layer ’%s’ is set multiple times.

DESCRIPTION

You get this warning because when you run "set_ignored_layers" command, you use one layer name multiple times.

WHAT NEXT

GR-23 (error) Can’t find layer ’%s’ in physical library.

DESCRIPTION

You get this error because you are trying to use a layer that does not exist in physical library.

WHAT NEXT

Run set_ignored_layers to use the existing routing layers from the physical library.

GR-24 (error) Can’t use non-routing layer ’%s’.

DESCRIPTION

You get this error because you are trying to use a non-routing layer in ignored layer list.

WHAT NEXT

Run set_ignored_layers to use the existing routing layers from the physical library.

GR-25 (error) Can’t ignore all horizontal routing layers in RC computation.

DESCRIPTION

You get this error because you are trying to ignore all horizontal routing layers in ignored layer list.

WHAT NEXT

Run set_ignored_layers, but leave at least on horizontal routing layer. To check all horizontal routing layers from a physical library, run report_lib command.

GR-26 (error) Can’t ignore all vertical routing layers in RC computation.

DESCRIPTION

You get this error because you are trying to ignore all vertical routing layers in ignored layer list.

WHAT NEXT

Run set_ignored_layers, but leave at least on vertical routing layer. To check all vertical routing layers from a physical library, run report_lib command.

GR-27 (warning) Routing wire model has higher priority than ignored layers.

DESCRIPTION

You get this warning because you are using user specified routing wire model for RC computation while you are specifying ignored layers. Although you can specify ignored layers, we will not consider ignored layers during RC computation when user-specified routing wire model is used for the design.

WHAT NEXT

GR-28 (error) Can’t find layer ’%s’ in physical library.

DESCRIPTION

You get this error because you are trying to use a layer that does not exist in physical library.

WHAT NEXT

Run set_layer_preferred_direction on existing routing layers from the physical library.

GR-29 (error) Can’t use non-metal layer ’%s’.

DESCRIPTION

You get this error because you are trying to set direction on a non-metal layer in layer list.

WHAT NEXT

Run set_layer_preferred_direction on existing routable metal layers from the physical library.

GR-30 (error) Can’t set all routing layers as horizontal.

DESCRIPTION

You get this error because you are trying to set horizontal direction for all routing layers

WHAT NEXT

Run set_layer_preferred_direction, but leave at least one horizontal routing layer. To check all routing layers direction from a physical library, run report_layer_preferred_direction command.

GR-31 (error) Can’t set all routing layers as vertical.

DESCRIPTION

You get this error because you are trying to set vertical direction for all routing layers.

WHAT NEXT

Run set_layer_preferred_direction, but leave at least one vertical routing layer. To check all routing layers direction from a physical library, run report_layer_preferred_direction command.

GUI

```
### GUI-001.n ###
```

GUI-001 (Error) %s: %s ’%s’ not found.

DESCRIPTION

```
The specified object does not exist.

### GUI-002.n ###
```

GUI-002 (Error) %s: %s name is empty.

DESCRIPTION

```
The name for the relevant object type [toolbar|menu|window type|hotkey,..] is empty.

### GUI-003.n ###
```

GUI-003 (Error) %s: valid %s name cannot consist only of ampersands.

DESCRIPTION

```
Valid name for specified object type cannot consist only of ampersands. The object
type can be a menu, toolbar, window type, hotkey, etc.

### GUI-004.n ###
```

GUI-004 (Error) %s: trailing ’->’ not allowed in menu name ’%s’.

DESCRIPTION

```
Trailing ’->’ not allow in specified menu name.

### GUI-005.n ###
```

GUI-005 (Warning) %s: hotkey '%s' is reserved. Please use another hotkey.

DESCRIPTION

```
Specified hotkey is reserved by application. Please use another hotkey.

### GUI-006.n ###
```

GUI-006 (Warning) %s: hotkey '%s' is not supported.

DESCRIPTION

```
Specified hotkey is not supported. Please check spelling or use another hotkey.
Shift modifier only work with letter or function hotkey. Thus, "Ctrl+Shift+4" is not
supported.

### GUI-007.n ###
```

GUI-007 (Error) %s: hotkey '%s' is invalid. Please check spelling.

DESCRIPTION

```
Specified hotkey is invalid. Please check spelling.

### GUI-008.n ###
```

GUI-008 (Warning) %s: menu item '%s' already exist for %s '%s'.

DESCRIPTION

```
Specified menu item already exist for specified window type.

### GUI-009.n ###
```

GUI-009 (Warning) %s: hotkey '%s' will not be set for menu '%s'.

Hotkey had been used.

DESCRIPTION

Specified hotkey will not be set for specified menu. It had been used by another menu item or tcl command.

GUI-010.n

GUI-010 (Error) %s: anchor offset must be nonzero.

DESCRIPTION

Anchor offset value for specified command must be either a positive or negative integer.

GUI-012.n

GUI-012 (Warning) %s: Specified dock side '%s' is invalid. Top docking side will be used.

DESCRIPTION

Specified dock side is invalid. Valid values include left|top|right|bottom.

GUI-014.n

GUI-014 (Error) %s: menu item '%s' not found for window type '%s'.

DESCRIPTION

Specified menu item not found for specified window type or default window type if not specified.

GUI-015.n

GUI-015 (Warning) %s: hotkey '%s' is already set for tcl

command ’%s’.

DESCRIPTION

Specified hotkey is already set for an existing tcl command.

GUI-016.n

GUI-016 (Warning) %s: hotkey not set, hotkey ’%s’ is already set for menu item ’%s’.

DESCRIPTION

Specified hotkey has already been used by a menu item. Use -replace option to force hotkey to be set.

GUI-017.n

GUI-017 (Warning) %s: hotkey ’%s’ is reserved by system function ’%s’.

DESCRIPTION

Specified hotkey has already been used by an internal system function.

GUI-018 (Error) None of the supported browsers %s are in the path

DESCRIPTION

This error message occurs when the application can not find a browser from the list of supported browsers in your environment.

WHAT NEXT

Please correct the PATH to get one of the supported browsers. Please contact your system administrator to get the location of the browsers.

SEE ALSO

gui_online_browser(3)

GUI-019 (Error) The default browser %s of your choice is not supported

DESCRIPTION

The current browser assigned to the variable gui_online_browser is not supported by your online help system.

WHAT NEXT

Please assign a browser from the the following list %s to the variable gui_online_browser and try to bring up the helpsystem.

SEE ALSO

gui_online_browser(3)

GUI-020 (Info) No %s installation specified with variable %s

DESCRIPTION

The application extension to ICC specified depends on the variable to point to the installation of that tool. The environment variable specified was not set so this extension to ICC will not be loaded.

WHAT NEXT

If you would like to load the ICC extension for that tool, then please setup the variable to point to the appropriate tool installation before running the ICC GUI.

SEE ALSO

GUI-021 (Warning) Extension %s not loaded because extension loading is disabled

DESCRIPTION

The loading of application extensions has been disabled. Therefore the specified extension will not be loaded.

WHAT NEXT

Re-enable extension loading if you want to have extensions loaded.

SEE ALSO

GUI-022 (Error) %s installation directory specified in variable %s is not a directory.
Extension can not be loaded from %s

DESCRIPTION

The installation directory for the extension was not a directory, so the extension could not be loaded.

WHAT NEXT

Correct the setting of the variable to specify the path to the installation of the tool and re-start the ICC GUI to get the extension loaded.

SEE ALSO

GUI-023 (Warning) The %s installation specified does not contain an ICC extension setup file %s

DESCRIPTION

The installation directory for the extension did not contain the expected ICC extension, so the extension could not be loaded.

WHAT NEXT

Correct the setting of the variable to specify the path to the installation of the tool and re-run ICC to get the extension loaded. If this version of the application does not support the ICC extension you may need to update to a newer version of this application.

SEE ALSO

GUI-024 (Info) Loaded %s extension from %s

DESCRIPTION

This message indicates that the ICC extension for the specified application was automatically loaded. The loading of the extension is controlled by the specification of the application installation for this application via a variable.

WHAT NEXT

There are no additional steps required to use this extension.

SEE ALSO

GUI-025 (Error) Error sourcing %s extension setup file %s %s
error_info is:
%s

DESCRIPTION

There was an error detected when loading the ICC extension for the specified application. Please contact the support staff for the application to get assistance in correcting the problem.

WHAT NEXT

Please ensure that the application installation specified is correct. If there is an error in the extension then please contact the support staff for that application to get a fix for their ICC extension.

SEE ALSO

GUI-026 (Info) Visibility is turned %s for cells and cell contents because the task is set to %s

DESCRIPTION

The visibility options for cells and cell contents are turned OFF automatically when the task is set to Design Planning or turned ON automatically when the task is set to Block Implementation or All.

WHAT NEXT

You can set the preference setVisibilityByTask to turn on or turn off this behavior. For example, to turn off this behavior, use the following command:

```
gui_set_pref_value -category layout -key setVisibilityByTask -value false
```

By default, this preference is set to true.

SEE ALSO

HDF

HDF-100 (Error) New Core results in invalid Cell Boundary

DESCRIPTION

New Core results in invalid Cell Boundary

WHAT NEXT

HDF-101 (Error) Create Rows failed

DESCRIPTION

Create Rows failed

WHAT NEXT

HDF-102 (Error) Can not set pin satus

DESCRIPTION

Can not set pin status

WHAT NEXT

HDF-103 (Warning) Some instances of soft macro cell %s are

marked fixed but some are not

DESCRIPTION

WHAT NEXT

HDF-105 (Error) axOpenCell: failed for %s.%s

DESCRIPTION

`axOpenCell failed.`

WHAT NEXT

HDF-106 (Error) Place Pads failed

DESCRIPTION

`Place Pads failed`

WHAT NEXT

HDL-1 (error) Can’t open Synopsys primitive package ’%s’

DESCRIPTION

The compiler for your Verilog HDL or VHDL description could not find the file *verilog.prims* or *vhdl.prims*. This happens when Synopsys software is incorrectly installed on your machine.

WHAT NEXT

Reinstall the Synopsys software.

HDL-2 (error) Corrupt Synopsys primitve package

DESCRIPTION

The compiler for your VHDL or Verilog HDL description could not read in the primitive package *vhdl.prims* or *verilog.prims*. This occurs when the primitive package is from a previous version of the Synopsys software release.

WHAT NEXT

Reinstall the current version of Synopsys software.

HDL-3 (error) Can’t find primitive "%s

DESCRIPTION

This message indicates that an HDL Compiler primitive is missing from the installation of the Synopsys software. It can occur when trying to mix system files from different releases.

WHAT NEXT

Reinstall the Synopsys software.

HDL-4 (error) Condition of ’if’ statement must be a single bit %s

DESCRIPTION

This error occurs when the condition tested in an ’if’ statement does not evaluate to a Boolean (single bit).

WHAT NEXT

Rewrite your description so that the condition tested in the ’if’ statement is a Boolean (single bit).

EXAMPLE

VHDL:

```
process
        variable condition_expr: bit_vector (0 to 3);
begin
        condition_expr := in_value;
        if (condition_expr) then
                -- use of condition_expr is incorrect
                out_value := in_value and previous_value;
        end if;
```

HDL-5 (error) Loop increment is zero %s

DESCRIPTION

An increment of zero prevents a *for* or *while* statement from ever making progress. An infinite loop is not synthesizable.

WHAT NEXT

Rewrite your description so that the loop statement has a non-zero increment.

HDL-6 (warning) Loop body will iterate zero times %s

DESCRIPTION

This warning occurs when the upper bound and lower bound specified for iteration are the same. This specification will cause the loop to iterate zero times.

WHAT NEXT

This is only a warning. Rewrite your description if you intended a non-zero number of iteration for the loop.

HDL-7 (warning) Loop will iterate over 1,000 times. (This will take awhile.) %s

DESCRIPTION

This warning message occurs when the number of iterations specified in a loop statement is greater than 1,000. A large number of iterations can cause slow run times.

WHAT NEXT

This is a warning message only. No action is required on your part.

However, if you did not intend to specify such a large number of iterations for the loop, modify your description and then run the command again.

HDL-8 (error) Illegal exit to block %s

DESCRIPTION

This error can occur when a VHDL "exit" or Verilog "disable" referrs to something other than an enclosing loop.

WHAT NEXT

Modify your HDL Source to "exit" or "disable" an enclosing loop.

HDL-9 (error) Illegal exit to block %s %s

DESCRIPTION

This error can occur when a VHDL "exit" or Verilog "disable" referrs to something other than an enclosing loop.

WHAT NEXT

Modify your HDL Source to "exit" or "disable" an enclosing loop.

HDL-10 (error) Connection to port%s may not be a string %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-11 (error) Connection to port%s must be a variable %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-12 (error) Used constant%s which has not been given a value %s

DESCRIPTION

This error occurs when a declared constant or generic parameter is used before the value has been assigned. Remember that generic parameters can be used in the design name.

WHAT NEXT

Assign a value to the constant where it is declared.

HDL-14 (error) Tried to assign a value to a literal %s

DESCRIPTION

This error can occur when you try to assign a value to a literal. Literals include: numbers such as 567, vectors such as "1101", or enumeration literals as STATE_7. Assignments can be made with assignment statements or output parameters of subroutines.

WHAT NEXT

If the literal is an subroutine actual parameter, change the mode to "out". If the literal lies on the left-hand side of an assignment, move it to the right.

HDL-15 (error) Literal may contain only ’0’, ’1’, ’Z’, ’D’, or ’U’ %s

DESCRIPTION

0, *1*, *Z*, *D*, or *U* are the only values recognized by this compiler. This error occurs when you specify some other value, such as ’X’ (see the example below).

WHAT NEXT

Rewrite your description to use one of the recognized values.

EXAMPLES

VHDL:

```
attribute ENUM_ENCODING: string;

type color is (red, green, blue);
        attribute ENUM_ENCODING of color: type is
"00, 01, 1x";
```

- the specification of X as an encoding in the literal will cause this error.

HDL-16 (error) Type of '%s' is unconstrained %s

DESCRIPTION

This error occurs when reading an unconstrained variable, port, or signal. For synthesis, all values must have a fixed bit width. The error occurs, for example, when you declare an entity port to have the type: *BIT_VECTOR*.

The error can also occur if a function with a **built_in** pragma is invoked before the function body is analyzed. In such a case, the workaround is to define the function and its body before the function is invoked.

WHAT NEXT

Use an array-bound constraint when you declare the object. In the above example, you can change the entity port type to *BIT_VECTOR(1 to N)*, where *N* is a constant, literal, or generic value.

EXAMPLES

```
entity foo is
end foo;

architecture bar of foo is
   function func_with_built_in (i, size: integer)      return bit_vector;

   constant x:bit_vector(31 downto 0) := func_with_built_in(3, 32);

   function func_with_built_in       (i, size: integer)  return bit_vector is
   --  pragma built_in SYN_INTEGER_TO_SIGNED
   begin
      ..
      ..
   end;

  --
  -- workaround will be to move the constant declaration after the
  -- function body
  --

begin
end;
```

HDL-17 (error) Untyped variable%s used %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-18 (error) Tried to read from a block with no direction %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-19 (error) Tried to write to a block with no direction %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-20 (error) Block expects value, but none was supplied %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-21 (error) Block returns value, but was assigned one %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-22 (error) Can’t resolve goto to label ’%s’ %s

DESCRIPTION

This error occurs when you use a VHDL "next" or "exit" statement, or a Verilog "disable" statement and the identifier you uses does not refer to an enclosing loop name.

WHAT NEXT

Change the indentifier in your statement to refer to an enclosing loop name.

HDL-23 (error) Array index out of bounds %s.

DESCRIPTION

This error occurs when any array element is indexed outside the bounds of the specified array.

WHAT NEXT

Modify your description so that access occurs within the specified bounds of the array.

EXAMPLES

Verilog:

```
reg [0:7] bus;

single_bit = bus[8];
```

VHDL:

```
variable bus_array: bit_vector(0 to 7);

single_bit := bus_array(8);
```

HDL-25 (error) Range is unconstrained %s

DESCRIPTION

This error occurs when you use an unconstrained range. The bounds of a range must be fixed before it may be used to specify an array range or declare a new object.

WHAT NEXT

Change your description so that a bound will be placed on the range before it is used.

HDL-26 (error) Found a negative value where a unsigned value was expected %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-27 (error) Constant value required %s

DESCRIPTION

This error occurs when the HDL Compiler requires a constant value, but can not calculate it. For example, the actual parameters in a VHDL generic map or Verilog parameter binding must be constant. This error occurs if you supply a VHDL signal, or Verilog wire value instead.

WHAT NEXT

Change the value to one that can be computed at compile-time. Computable values include: constants, literals, generics, parameters, and expressions that depend only

on these.

HDL-28 (error) Operand is not a value %s

DESCRIPTION

This error occurs where the HDL Compiler expects a value but finds something else (such as a type). Legal values include: constants, variables, signals, regs, wires, strings, and literals.

WHAT NEXT

Change the operand to a value.

HDL-29 (error) Operand is not a type %s

DESCRIPTION

This error occurs where the HDL Compiler expects a type but finds something else (such as a variable).

WHAT NEXT

Change the operand to a type.

HDL-30 (error) Operand is not a string %s

DESCRIPTION

This error occurs where the HDL Compiler expects a string but finds something else (such as a variable).

WHAT NEXT

Change the operand to a string.

HDL-31 (error) Too few input operands on dnode %s

DESCRIPTION

This error occurs when a subroutine is supplied less input arguments than it expects.

WHAT NEXT

Compare the subroutine declaration with the call identified in the error message. Change the arguments in the call to match the definition.

HDL-32 (error) Too many input operands on dnode %s

DESCRIPTION

This error occurs when a subroutine is supplied more input arguments than it expects.

WHAT NEXT

Compare the subroutine declaration with the call identified in the error message. Change the arguments in the call to match the definition.

HDL-33 (error) Too few output operands on dnode %s

DESCRIPTION

This error occurs when a subroutine call supplies less output arguments than are defined.

WHAT NEXT

Compare the subroutine declaration with the call identified in the error message. Change the arguments in the call to match the definition.

HDL-34 (error) Too many output operands on dnode %s

DESCRIPTION

This error occurs when a subroutine call supplies more output arguments than are defined.

WHAT NEXT

Compare the subroutine declaration with the call identified in the error message. Change the arguments in the call to match the definition.

HDL-36 (error) Source type of assignment is unconstrained %s

DESCRIPTION

This error occurs when you try to assign an unconstrained value to something. All arrays must be constrained before you use them.

WHAT NEXT

Place a constraint on the value.

HDL-37 (error) Tried to assign a value to an invalid symbol %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-38 (error) Type mismatch %s.

DESCRIPTION

This message indicates that the target of an assignment is not compatible with the assigned value. In VHDL, you may assign only between closely related types of equal size.

WHAT NEXT

Check the sizes of the source and target of the assignment. If they differ, then make them the same. If they already are the same size, then use a type conversion to change the source type into the target type.

HDL-39 (error) Tried to assign a type to an invalid symbol %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-40 (error) Target %s is incompatible with assigned value %s

DESCRIPTION

This error occurs when the target of an assignment is not compatible with the assigned value. In VHDL, you may assign only between closely related types of equal size.

WHAT NEXT

Check the sizes of the source and target of the assignment. If they differ, then make them the same. If they already are the same size, then use a type conversion to convert the source into the type of the target.

HDL-41 (error) Expected %s but was supplied %s %s

DESCRIPTION

This error occurs when it finds an unexpected argument to a subroutine. For example, if enumeration literal with a "U" encoding is supplied to a boolean function, HDL Compiler will report that a "value" was expected, but an "unknown" was supplied instead.

WHAT NEXT

Check the argument identified in the message, and change it to one the of the expected types.

HDL-42 (error) Port%s has no type %s

DESCRIPTION

This error occurs if you omit the type specification on a port declaration.

WHAT NEXT

Specify the type of the port.

HDL-43 (error) Tried to take a slice out of a non-array %s

DESCRIPTION

This error occurs when you attempt to take a slice out of a non-array.

WHAT NEXT

Modify your description to convert the variable in question into an array.

EXAMPLES

Verilog:

```
wire foo, bar;

assign foo[1:3] = bar;
/* foo is not an array. This will cause the error to occur */
```

HDL-44 (error) Arguments to '%s' are not the same size %s

DESCRIPTION

HDL Compiler reports this error when it detects a difference in the bit-width of the arguments to a boolean operator.

WHAT NEXT

Make the arguments the same width.

HDL-47 (error) Divide by zero %s

DESCRIPTION

This error occurs where HDL Compiler detects division by a constant value: zero. The zero may be entered directly, or, more commonly, it is the result of an expression. For example, the expression: (WIDTH/(M-N)) will divide by zero if both M and N are equal constants.

WHAT NEXT

Remove the divide by zero from the expression.

HDL-48 (error) Negative exponent %s

DESCRIPTION

This error occurs where HDL Compiler detects a negative exponent. The exponent may be entered directly, or, more commonly, it is the result of an expression. For example, the expression: (2**(M-N)) will have a negative exponent when both M and N are constant, and N is a larger than M.

WHAT NEXT

Remove the negative exponent from the expression.

HDL-49 (error) Can't determine the value of the locally static

expression %s

DESCRIPTION

You receive this error message because the HDL Compiler cannot determine the value of the locally static expression. The use of complicated types of static expressions might cause this error message.

WHAT NEXT

Simplify the locally static expression.

SEE ALSO

analyze (2).

HDL-50 (error) Can’t get member of array %s

DESCRIPTION

This error occurs when you use an object as though it were an array, when it was not declared that way.

WHAT NEXT

Either declare the object as an array, or don’t use it like an array.

HDL-51 (error) Indexing into a non-array variable is not supported %s.

DESCRIPTION

This error occurs when you index a non-array variable.

WHAT NEXT

Modify your description to remove the attempt to index into the non-array variable.

EXAMPLES

Verilog:

```
reg foo, bar;

bar = foo[0];
/* Indexing into variable 'foo' is an error */
```

HDL-52 (error) AGG major type must be an array %s

DESCRIPTION

This error occurs when an aggregate is used as a non-array. For example, HDL Compiler will error if you qualify an aggregate with an integer type.

WHAT NEXT

Change the use of the aggregate to be consistent with its array type.

HDL-53 (error) Tried to take a member from a non-array %s

DESCRIPTION

This error occurs when you use an array index construct on an object that was not declared as an array. For example, if X is declared as an INTEGER, the expression (X(1)) will get this error.

This error occurs in Verilog when an object is declared as an enumerated type with the /* synopsys enum */ directive, and is then accessed with a bit select.

WHAT NEXT

Either change the object type to an array, or don't perform an array index directly on it. One way to avoid array indexing is to assign the value to a temporary array and index the temporary.

HDL-54 (error) Subtype in aggregate was not a submember or

subrange %s

DESCRIPTION

Currently, only integer values and integer ranges are supported with named associations in aggregates. This error occurs when something else is used.

WHAT NEXT

Change the aggregate to include only integer values and/or integer ranges.

HDL-55 (error) Source and target of slice assignment are not the same size %s

DESCRIPTION

This error occurs when a slice of an array is assigned an expression that has a different bit-width. Usually this is the result of a problem in expression the calculates the slice range. In the following example, the target is one bit larger than the source:

```
Z(A'width downto 0) <= A;
```

The following shows one way to fix the problem:

```
Z(A'width - 1 downto 0) <= A;
```

WHAT NEXT

Modify either the source or target to make the widths equal.

HDL-56 (error) Not enough args to 'lagg' %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-57 (error) Argument to '%s' is not an array or range %s

DESCRIPTION

This error occurs when an operation that is supported only on arrays and ranges is used on something else. For example, the 'first attribute is supported only on array and ranges. The expression: (STATE'first) would get this error if STATE were declared as an enumerated type. The 'first attribute is not supported for synthesis on enumerated types yet, even though this is legal VHDL.

WHAT NEXT

Change the object declaration to an array or range (integer) type. In the above example, STATE could be changed to an INTEGER subtype.

HDL-58 (error) Argument to '%s' is unconstrained %s

DESCRIPTION

This error occurs when you use an unconstrained range. The bounds of a range must be fixed before it may be used to specify an array range or declare a new object.

WHAT NEXT

Change your description so that a bound will be placed on the range before it is used.

HDL-60 (error) Casted from an unconstrained type %s

DESCRIPTION

This error occurs when you use an unconstrained range. The bounds of a range must be fixed before it may be used to specify an array range or declare a new object.

WHAT NEXT

Change your description so that a bound will be placed on the range before it is used.

HDL-61 (error) Direction ('to' or 'downto') does not agree with

’first’
and ’last’ values in range %s

DESCRIPTION

Use the keyword *downto* when the first value in the range is greater than the last value. Use the keyword *to* when the first value in the range is less than the last value. This error occurs these conditions are not met.

WHAT NEXT

Rewrite your descriptions so the above conditions are met.

EXAMPLES

VHDL:

```
signal my_bus : bit_vector ( 15 to 0 );

-- downto should be used here because 15 is greater than 0
```

HDL-62 (error) ’binned_range’ requires at least one operand %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-63 (error) Last name has no encoding %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-64 (error) %s was assigned values of different sizes %s

DESCRIPTION

This error occurs when an unconstrained value is assigned different sized values on separate branches of an "if" or "case".

WHAT NEXT

Change the assignments so they agree on the bit-width assigned to the unconstrained value.

HDL-65 (error) %s %s

DESCRIPTION

This error prefix is used by the primitive routines that implement the builtin VHDL and Verilog functions.

WHAT NEXT

Find the part of your code that is identified by the message, and change it according to the message.

HDL-66 (error) Was expecting a positive number, got %d instead %s

DESCRIPTION

This error occurs when a function that determines if its input is a positive power of 2 is supplied a number less than or equal to zero.

WHAT NEXT

Modify your description so that the input to this function is a positive number.

HDL-67 (error) Duplicate name in enum definition: ’%s’ %s

DESCRIPTION

This error occurs when identifiers or character literals listed by an enumeration type definition are not distinct.

WHAT NEXT

Modify your HDL description so that each identifier or character literal is used only once in each enumeration type definition.

HDL-68 (error) Encoding ’%s’ for ’%s’ is not valid.

DESCRIPTION

You can specify encoding for enumerated data types using the *enum_encoding* attribute. The encoding must be valid in terms of the values that the attribute specifies for the enumeration. The *enum_encoding* attributemust also be valid in terms of the length of the encoding. This error occurs if either of these conditions is not met.

WHAT NEXT

Modify the encoding specified for the enumeration to meet the above conditions.

EXAMPLES

VHDL:

attribute enum_encoding: string; type color is (red, green); attribute enum_encoding of color: type is *00 1*;

-- the encoding string for *red* is two bits long; it should be one -- bit long.

HDL-69 (error) Can’t find a design or function ’%s’ to overload %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-70 (error) Can’t find lvalue version of design ’%s’ %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-71 (error) Constant value %d overflowed ’%s’ %s

DESCRIPTION

This error occurs when the value assigned to a target is smaller than the lower bound or bigger than the upper bound of the range defined for the target.

WHAT NEXT

Modify your HDL description to make the allowable range larger.

HDL-72 (error) Slice width ’%d’ is not positive %s

DESCRIPTION

This error occurs when the width specified for a slice operation on an array is less than zero.

WHAT NEXT

Rewrite your HDL description so that the width specification is positive.

HDL-73 (error) Can’t overload design ’%s’ uniquely %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-74 (error) At least one argument required for ’%s’ %s

DESCRIPTION

This error occurs when no arguments are specifed for operators such as "and", "or", "xor" or "max".

WHAT NEXT

Modify your HDL description to provide at least one argument to the operator.

HDL-76 (error) ’others’, vhdl range choices, and multiple choices in left-hand-side aggregates must be connected to OPEN%s

DESCRIPTION

This error occurs when an attempt is made to use the ’others’ construct is used as part of an association list on the left hand side of an assignment.

WHAT NEXT

Modify your HDL description to remove this use of ’others’

HDL-77 (error) Tried to change the type of %s %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-78 (error) Tried to assign an unconstrained type to variable%s %s

DESCRIPTION

This error occurs if a variable is declared to be of a type that is unconstrained(such as BIT_VECTOR). The VHDL compiler for synthesis requires that all the type of a variable be constrained.

WHAT NEXT

Modify your HDL description to specify a constraint for the type of the variable.

HDL-79 (error) Illegal open connection to builtin function %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-80 (error) Variable%s has an uninitialized type %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-81 (error) Can’t find a design ’%s’ that has correct

parameter profile
(Could be a type mismatch)%s

DESCRIPTION

If the design reported is called 'indexed-name', an array index in the reported line is non-integer. Enumerated types are not supported. Synopsys supports indices of any type of integer.

```
entity e is
end;
architecture a of e is
TYPE mytype        IS      (first, second );
TYPE my_type_array IS      array (first to second) of integer range 0 to 7;
SIGNAL this_index  :      mytype;
SIGNAL this_array  :      my_type_array;
SIGNAL other_array :      my_type_array;

begin
other_array(first) <= this_array(this_index);   -- this is line 11

end;
```

WHAT NEXT

If the line reported in the error message contains an array whose index is not type integer, modify your VHDL so that the type is integer.

If your VHDL does not have an array indexed by a non-integer type, contact your Synopsys support representative.

SAMPLE MESSAGE

```
Error: Can't find a design 'indexed-name' that has correct parameter profile
(Could be a type mismatch)
in call to 'indexed-name'
called from e line 11 in file 'e.vhd' (HDL-81)
```

HDL-82 (error) Unknown HDL format '%s'

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-83 (error) Can’t open %s primitive package ’%s’

DESCRIPTION

This error occurs if the file "vhdl.prims" (for VHDL descriptions) or "verilog.prims" (for Verilog descriptions) cannot be found. This could be because of an error in installing Synopsys software on your machine.

WHAT NEXT

Check to make sure that the software has been correctly and completely installed.

HDL-84 (error) Was expecting a non-negative number, got %d instead %s

DESCRIPTION

This error occurs when a function that computes the logarithm of a number is supplied a negative number as its argument.

WHAT NEXT

Provide a positive number as an argument for this function.

HDL-85 (error) Subprogram body or architecture for ’%s’ was not defined %s.

DESCRIPTION

This error occurs when a function is specified without specifying the function’s subprogram. This error also occurs when you elaborate a design for which no architecture has been specified.

WHAT NEXT

Provide the appropriate architecture or function body.

HDL-86 (error) Subprogram '%s' was used but has no body defined %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-87 (error) Value cannot be interpreted as a boolean %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-90 (error) Slice direction does not match array direction %s

DESCRIPTION

This error occurs if the direction ('to' or 'downto') specified for a slice operation on an array does not agree with the direction specified in the definition of the array.

WHAT NEXT

Modify the HDL description to correct the direction of the slice.

HDL-91 (warning) Can't find '%s' referred to by the '%s' attribute %s

DESCRIPTION

This error occurs when the object for which an attribute is specified cannot be

found. For example, if the arrival_time attribute for a port is specified and if the port does not exist in the design, then this error would occur.

WHAT NEXT

Check your HDL description to see if you have misspelt the name of the object or specified an attribute for a non-existent object.

HDL-92 (warning) Ignored illegal EQUAL or OPPOSITE attribute %s

DESCRIPTION

This error occurs if an incorrect number of values are specified for the EQUAL or OPPOSITE attributes.

WHAT NEXT

Modify your HDL description to provide exactly two values to these attributes.

HDL-93 (warning) %s %s

DESCRIPTION

This warning prefix is used by the primitive routines that implement the builtin VHDL and Verilog functions.

An example of when this message is issued is if the VHDL compares bit arrays of different widths. VHDL comparisons between bit arrays of different widths generate logic for dictionary order (VHDL LRM 7-4) rather than arithmetic ordering. For instance, "10" is considered greater than "011". Most significant bits are compared first, with missing least significant bits treated as null values (which are less than all other bit values). See "Relational Operators" in the VHDL Compiler Reference manual for more detail and examples.

WHAT NEXT

Find the part of your code that is identified by the message, and change it according to the message.

For comparisons between VHDL bit arrays of different widths, check that lexigraphic ordering (’dictionary order’) is appropriate. If not, one operand should be altered to match the width of the other operand.

EXAMPLE

Example problem for VHDL comparisons between bit arrays of different widths:

```
   signal sigvec : std_logic_vector(2 downto 0);

   ...

   if (sigvec > "00") then
-- even when sigvec is "000", it is greater than "00".
-- this branch will always be taken.
   end if;
```

HDL-94 (error) Aggregate contains too many elements %s.

DESCRIPTION

This error occurs when the number of elements specified for an aggregate is greater than the implicit size of the aggregate.

WHAT NEXT

Modify your description to provide the appropriate number of elements.

EXAMPLES

VHDL:

```
signal my_bus: bit_vector ( 0 to 3);

my_bus <= (0, 1, 1, 0, 1);

-- this is an error because five elements are specified. The aggregate's size is four [0,3}; so four elements should have been specified.
```

HDL-95 (error) Aggregate contains too few elements %s.

DESCRIPTION

This error occurs when the number of elements specified for an aggregate are less than the implicit size of the aggregate.

WHAT NEXT

Modify your description to provide the appropriate number of elements.

EXAMPLES

VHDL:

```
signal my_bus: bit_vector ( 0 to 3);

my_bus <= ('0', '1', '1'); -- this is an error because only three elements are
specified. The aggregate's size is 4 [0,3] so four elements should be specified.
```

HDL-96 (error) Infinite recursion detected %s

DESCRIPTION

A function that calls itself is recursive. Recursive functions call themselves directly, or call others functions that eventually call back. Recursive functions usually check a condition that terminates the recursion. The number of nested calls made before termination is called the depth of the recursion.

The HDL compiler allows recursive functions only if the depth of the recursion can be determined at read time. This error is invoked whenever HDL compiler can not determine the depth of a recursive call.

WHAT NEXT

Modify the recursive function to make the recursive call only under a condition that will eventually prove false after a few nested calls. For example, you can add a parameter to the function that is decremented for each nested call. If you return immediately from the function when the parameter reaches zero, HDL compiler will allow the recursion.

EXAMPLES

```
-- VHDL
entity e is
port(a: in bit; z: out bit);
end;
architecture a of e is
function f(a: in bit) return bit is
begin
return(f(a));   -- Infinite recursive call
end;

begin
      z <= f(a);
end;
```

```
/* Verilog */
module e(a,z);
input a;
output z;
function f;
input a;
f = f(a);     /* Infinite recursive call */
endfunction

assign z = f(a);
endmodule
```

EXAMPLE MESSAGE

```
Error: Infinite recursion detected
  in routine f line 6 in file 't.v'
called from f line 7 in file 't.v'
called from f line 7 in file 't.v'
called from f line 7 in file 't.v'
...
```

HDL-97 (error) Can't determine type of operand %s

DESCRIPTION

This error occurs if the type of an operand cannot be determined.

WHAT NEXT

Modify your to HDL description to qualify the operand with its type.

HDL-98 (error) Non-static loop or event waits in only some branches detected %s

DESCRIPTION

This error occurs in one of two cases: (1) It is an RTL description and a process, loop, or branch within a loop was not broken with *event waits* and (2) It is a behavioral description and elaborated without -s option.

EXAMPLE

The following example is an RTL description that triggers the HDL-98 error message. In the example, the *while* loop is broken with an *event wait*. However, the process

must also be broken with an *event wait*. If enable = '0', the description doesn't have an *event wait* because there isn't one for the process.

VHDL

```
library IEEE;
use IEEE.std_logic_1164.all;

entity HDL_98 is
   port( a      : in std_logic_vector(7 downto 0);
         clk    : in std_logic;
         enable : in std_logic;
         b      : out std_logic_vector(7 downto 0)
   );
end HDL_98;

architecture RTL of HDL_98 is
begin
   process begin
      while (enable = '1') loop
         wait until clk'event and clk ='1';
         b <= a;
      end loop;
   end process;
end RTL;
```

Verilog

```
module HDL_98 (a, clk , b , enable);
input [7:0] a;
input clk, enable;
output [7:0] b;
reg [7:0] b;

   always
      while (enable)
         begin
            @ (posedge clk);
            b <= a;
         end
endmodule
```

WHAT NEXT

If it is an RTL description modify your description to include an *event wait* in each branch and loop in your description. If it is a behavioral description use command *elaborate -s*.

In the following example, the above description is modified to include an *event wait* for the process.

VHDL

```
library IEEE;
use IEEE.std_logic_1164.all;
```

```
entity correct is
   port( a      : in std_logic_vector(7 downto 0);
         clk    : in std_logic;
         enable : in std_logic;
         b      : out std_logic_vector(7 downto 0)
   );
end correct;

architecture RTL of correct is
begin
   process begin
      while (enable = '1') loop
         wait until clk'event and clk ='1';
         b <= a;
      end loop;
      wait until clk'event and clk = '1';  -- this wait is added
   end process;
end RTL;
```

Verilog

```
module correct (a, clk , b , enable);
input [7:0] a;
input clk, enable;
output [7:0] b;
reg [7:0] b;

   always begin
      @ (posedge clk)
      while (enable)
         begin
            @ (posedge clk);
            b <= a;
         end
   end
endmodule
```

EXAMPLE MESSAGE

```
Error: Non-static loop or event waits in only some branches detected
        in routine HDL_98 line 7 in file 'HDL_98.v' (HDL-98)
```

HDL-99 (error) Tried to use the value of an instance which does not return a value %s

DESCRIPTION

This error occurs when a construct that does not return a value is used in an expression. An example of such a construct is the 'task' construct in Verilog and the 'procedure' construct in VHDL.

WHAT NEXT

Modify your HDL description to correct the error.

HDL-100 (error) Aggregate type is an unconstrained array %s

DESCRIPTION

This error occurs if the type of an aggregate is an unconstrained type such as bit_vector.

WHAT NEXT

Modify your HDL description so that the type of the aggregate is a constrained type.

HDL-101 (error) Argument must be a constrained array %s

DESCRIPTION

This error occurs if you attempt to do a slice or index operation on an unconstrained array (such as bit_vector).

WHAT NEXT

Modify your HDL description to make the array constrained.

HDL-103 (warning) Function may be completed without returning a value %s

DESCRIPTION

This warning occurs if (in VHDL) the return statement for a function does not return a value or (in Verilog) a function does not return a value by assigning a value to a variable that has the same name as the function.

WHAT NEXT

Modify your HDL description to ensure that the function returns a value. If you do not need to return a value, use a procedure (in VHDL) or a task (in Verilog).

HDL-104 (error) Can’t get width of port %s %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-105 (error) HDL translation aborted.

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-106 (error) Bits of range driven differently %s

DESCRIPTION

This error occurs when values are assigned to some but not all bits of a variable whose type is a range. This usually happens when the variable is converted into an array and some bits of the array are assigned values. If this array is now converted back into a range and used, this error will occur.

WHAT NEXT

Modify your HDL description so that either all or none of the bits are driven.

HDL-107 (error) Tried to use a synchronized value %s

DESCRIPTION

This error occurs when you assign a value to a variable inside an "if(clock’event)" block, and then attempt to read it after the "end if" statement. In the following example, **temp** is improperly read:

```
entity test is
  port(clock: in bit; toggle: out bit);
end;

architecture a of test is
begin
  process (clock, toggle)
    variable temp: bit;
  begin
    if(clock'event and clock = '1') then
      temp := not temp;
    end if;

    toggle <= temp; -- ERROR
  end process;
end;
```

WHAT NEXT

Move the statement that reads the value into the "if" block, or change the variable into a signal and read the signal outside the process.

The following example shows how to move read of **temp** outside the process of the previous example:

```
entity test is
  port(clock: in bit; toggle: out bit);
end;

architecture a of test is
  signal temp: bit;
begin
  process (clock, toggle)
  begin
    if(clock'event and clock = '1') then
      temp <= not temp;
    end if;
  end process;

  toggle <= temp; -- OK
end;
```

EXAMPLE MESSAGE

Error: Tried to use a synchronized value in routine test line 14 in file 't.v' (HDL-107)

HDL-108 (error) Tried to use a conditionally driven value%s %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact you Synopsys support representative.

HDL-109 (error) This use of clock edge specification not supported %s

DESCRIPTION

This error occurs if you use more than one "if clock'event" expression in a process or if you embed the 'event expression inside a subprogram or loop.

The following example shows a positive- and negative-edge trigger in the same process.

```
entity test is
  port(clock, a: in bit; z1, z2: out bit);
end;

architecture a of test is
begin
  process (clock)
  begin
      if(clock'event and clock = '1') then
        z1 <= a;
      end if;

      if(clock'event and clock = '0') then -- ERROR
        z2 <= a;
      end if;
  end process;
end;
```

WHAT NEXT

Restructure your code to have a single "if clock'event" construct at the start of the process.

The previous example can be fixed by splitting the process into two processes.

```
entity test is
```

```
  port(clock, a: in bit; z1, z2: out bit);
end;

architecture a of test is
begin
  process (clock)
  begin
      if(clock'event and clock = '1') then
        z1 <= a;
      end if;
  end process;

  process (clock)
  begin
      if(clock'event and clock = '0') then
        z2 <= a;
      end if;
  end process;
end;
```

EXAMPLE MESSAGE

```
Error: This use of clock edge specification not supported in routine test line 13 in
file 't.v' (HDL-109)
```

HDL-110 (error) Illegal assignment to '%s'. It depends on a non-edge %s

DESCRIPTION

This error occurs when a value is assigned in the FALSE branch of an "if clock'event". This error can happen if a value is assigned on the "else" part of the "if clock'event", or if a value is assigned before the "if clock'event" and in the TRUE branch.

The first example below shows an illegal assignment in the FALSE branch:

```
entity test is
  port(clock, a, b: in bit; z: out bit);
end;

architecture a of test is
begin
  process (clock, a, b)
  begin
      if(clock'event and clock = '1') then
        z <= a;
      else
        z <= b; -- ERROR
      end if;
```

```
  end process;
end;
```

The second example behaves like the previous one because the assignment from "b" takes effect only when there is no event on the clock.

```
entity test is
  port(clock, a, b: in bit; z: out bit);
end;

architecture a of test is
begin
  process (clock, a, b)
  begin
      z <= b; -- ERROR

      if(clock'event and clock = '1') then
        z <= a;
      end if;
  end process;
end;
```

The behavior of these examples cannot be synthesized by the HDL Compiler. Notice that "z" behaves like a D flip-flop just after each clock event, but whenever a positive or negative transition is on either "a" or "b", the value is asynchronously reset to "b".

A variable can receive both asynchronous and synchronous assignments, but the asynchronous assignments must take precedence. That is, there must be a Boolean condition that enables the asynchronous part *and* disables the synchronous part.

The following example is still illegal since the asynchronous enable condition (reset) does not override the synchronous assignments:

```
entity test is
  port(clock, a, b, reset: in bit; z: out bit);
end;

architecture a of test is
begin
  process (clock, a, b, reset)
  begin
      if(reset = '1') then
        z <= b; -- ERROR, Since the if clock'event is not disabled by reset
      end if;

      if(clock'event and clock = '1') then
        z <= a;
      end if;
  end process;
end;
```

WHAT NEXT

Use an "if" statement to insure that either that the asynchronous or synchronous assignments fire in any execution of the process. Make sure that the condition controlling this "if" (the asynchronous reset condition) is *level sensitive*, not *edge sensitive*. The following examples show how to fix the previous code:

```
entity test is
  port(clock, a, b, reset: in bit; z: out bit);
end;

architecture a of test is
begin
  process (clock, a, b, reset)
  begin
      if(reset = '1') then
        z <= b; -- OK, since the if clock'event won't fire if we get here
      elsif(clock'event and clock = '1') then
        z <= a;
      end if;
  end process;
end;
```

EXAMPLE MESSAGE

```
Error: Illegal assignment to 'z'. It depends on a non-edge in routine test line 12
in file 't.v' (HDL-110)
```

HDL-111 (error) Illegally declared clock edge specification %s.

DESCRIPTION

This error occurs when you use the 'event construct in VHDL, or the positive-edge construct in Verilog, on a value that is not a single-bit simple signal or variable.

WHAT NEXT

Change your code to refer to a single-bit clock signal.

HDL-112 (error) Range (integer) types are illegal on inout (out) signal parameters to procedures %s.

DESCRIPTION

This error occurs when the inout (out) signal parameters of a procedure are of range

(integer) type, which the VHDL Compiler does not support for synthesis.

WHAT NEXT

Convert range type to a bit-vector type. For example, modify "bad.vhdl" to "good.vhdl".

```
-- "bad.vhdl"
package tp is

    subtype i4 is integer range 0 to 3;
    procedure p (signal x: in integer; signal y: inout integer);

end tp;

package body tp is

    procedure p (signal x: in integer; signal y: inout integer) is
    begin
        y <= x + y;
    end;

end tp;

use work.tp.all;

entity bad is
    port (a: in i4;
          b: inout i4;
          clk: in BIT;
          z: out i4);
end bad;

architecture a of bad is
    signal ax, bx : i4;
begin
    process (a, b)
    begin
      if (clk'event and clk = '1') then
        ax <= a;
        bx <= b;
        p(ax, bx);
        z <= bx;
      end if;
    end process;
end a;
```

```
-- "good.vhdl"
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_SIGNED.all;
use IEEE.STD_LOGIC_ARITH.all;

package tp is

    subtype i4 is integer range 0 to 3;
    procedure p (signal x:in integer;
                 signal y:inout STD_LOGIC_VECTOR(0 to 1));

end tp;

package body tp is

    procedure p (signal x:in integer;
                 signal y:inout STD_LOGIC_VECTOR(0 to 1))
    is
    begin
        y <= CONV_STD_LOGIC_VECTOR(x + CONV_INTEGER(y), 2);
    end;

end tp;

library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_SIGNED.all;
use IEEE.STD_LOGIC_ARITH.all;
use work.tp.all;

entity good is
    port (a: in i4;
          b: inout i4;
          clk: in BIT;
          z: out i4);
end good;

architecture a of good is
    signal ax : i4;
    signal bx : STD_LOGIC_VECTOR(0 to 1);
begin
    process (clk, a, b)
    begin
      if (clk'event and clk = '1') then
        ax <= a;
        bx <= CONV_STD_LOGIC_VECTOR(b, 2);
        p(ax, bx);
        z <= CONV_INTEGER(bx);
      end if;
    end process;
end a;
```

HDL-113 (error) Width of port %s is inconsistent with other instances %s

DESCRIPTION

This error occurs if the width of a port is different for different instances of a subdesign (component) in the same parent design.

WHAT NEXT

Modify your HDL description so that the width of the port is consitent across various instances of the instantiated design.

HDL-114 (error) Number of ports of instance is inconsistent with other instances %s

DESCRIPTION

This error occurs when the same subdesign (component) is instantiated with differing number of ports in the same parent design.

WHAT NEXT

Modify your HDL description so that the number of ports is the same for all instances of the instantiated design.

HDL-115 (error) Illegal mixing of named and unnamed port association %s

DESCRIPTION

This error occurs if, in instantiating a subdesign (component), named and positional styles of port association are mixed.

WHAT NEXT

Use either named style of positional style of specifying port assocation.

HDL-116 (error) Parameter%s must be associated with a

constant %s

DESCRIPTION

This error occurs if a paramter (generic) is specified but no value is assigned to it.

WHAT NEXT

Specify a value for the paramter (generic).

HDL-117 (error) Register inference not supported if "hdlin_infer_reg_and_latch" is false %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-118 (error) Single bit value expected %s

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-123 (error) Can’t determine type of aggregate or concat %s

DESCRIPTION

This error occurs when the type of an aggregate or concatenation cannot be determined.

WHAT NEXT

Modify your HDL description to qualify the operation with a type.

HDL-124 (error) Elements of aggregate or string literal are out of bounds, overlap, or do not cover all cases %s

DESCRIPTION

This error occurs when the values specified for an aggregate do not cover all the possible elements or if more than one value is specified for the same element or if the values specified are for elements that are not part of this aggregate.

WHAT NEXT

Modify your HDL description to ensure that there is one to one correspondence between elements of the aggregate and the values specified for it.

HDL-127 (error) Argument to concat has incorrect size %s

DESCRIPTION

The arguments to a VHDL concatenation must either 1) be the same type (two BITs, or two BIT_VECTORS), or 2) one must be an array and the other must be a member of that array (one BIT_VECTOR and one BIT). This error indicates that the arguments to the VHDL concatenation operator are invalid (an array of BITS concatenated with an array of INTEGERS).

WHAT NEXT

Make the concatenation arguments compatible.

HDL-130 (error) Could not find synthetic_library '%s'

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-131 (error) synthetic_library '%s' is not a valid library

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-135 (warning) In resource '%s' %s OPS entry '%s' is already included in resource '%s' %s. Entry ignored.

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the compiler has detected a label that appears in the ops list of more than one resource, which is invalid. Following is an example that illustrates this invalid situation:

```
synopsys resource r0 : ops = "op1 op2";    //op2 appears twice
synopsys resource r1 : ops = "op2 op3";
```

WHAT NEXT

Correct your code so that no label appears in the ops list of more than one resource. For more information about the ops directive, see Chapter 7 of the *HDL Compiler for Verilog Reference Manual*.

SEE ALSO

analyze (2), **read** (2).

HDL-139 (error) %s '%s' could not be found in the search path %s.

DESCRIPTION

This error occurs when the HDL Compiler can't find a file in the search path. The search path lists directories where HDL Compiler should look for source files.

WHAT NEXT

First, check the spelling of the file name. If it is correct, fix your search path to include the directory that holds the file.

HDL-140 (error) Tried to read a %s value%s %s

DESCRIPTION

This error occurs when reading a "threestated" or "don't cared" value. For example:

```
if(ENABLE) then

X := A;

else

X := 'Z'; -- Threestate assignment

end if;

Y := W and X; -- Error: reading a threestated value.
```

WHAT NEXT

Generally, you should read these values in a separate process or always block. If you must read them in the same process or always block, read the value before any don't care or threestate assignments.

HDL-141 (warning) '%s' does not indicate a unique instance or resource in resource '%s' %s

DESCRIPTION

WHAT NEXT

HDL-142 (warning) Instance or resource '%s' not found in

resource ’%s’ %s

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the compiler has detected a label in the ops list of a resource that is not defined in the code. Following is an example that illustrates this invalid condition:

```
always @(a or b or c or s) begin : block
  /* synopsys resource r1 : ops = "op1 op4";
   */
casex (s)
   2’b00: x = a + b;    //synopsys label op1
   2’b01: y = a + c;    //synopsys label op2
   2’b1x: z = b + c;    //synopsys label op3
                        //op 4 is not defined
endcase
```

WHAT NEXT

Be sure to define all labels used in this way.

SEE ALSO

analyze (2), **read** (2).

HDL-143 (warning) Subroutine label ’%s’ is not unique in scope. Label ignored. %s */

DESCRIPTION

WHAT NEXT

HDL-144 (warning) No appropriate operation, procedure or function to which label ’%s’ can be bound

DESCRIPTION

You receive this message because, during **analyze** or **read** activity, the compiler has detected a label that does not follow an entity that can be labeled. Label pragmas must appear after the entity they label. Following is an example that illustrates

this situation:

```
   always @(a or b or c or s) begin : block
     /* synopsys resource r1 : ops = "op1 op2";
      */

      //synopsys label op4        //
op4 does not follow an entity that can be labeled
    casex (s)
      2'b00: x = a + b;    //  synopsys label op1
      2'b01: y = a + c;    //  synopsys label op2
      2'b1x: z = b + c;    //  synopsys label op3
    endcase
   end
```

WHAT NEXT

Correct your code so that op4 labels an entity, or remove op4. For more information about resource and label pragmas, see Chapter 7 of the *HDL Compiler for Verilog Reference Manual*.

SEE ALSO

analyze (2), **read** (2).

HDL-145 (error) Label '%s' used on more than one resource in same scope %s.

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the compiler has detected a label that is applied to two operators, which is invalid. You can apply a label to only one operator. Following is an example that illustrates this invalid situation:

```
   always @(a or b or c or s) begin : block
     /* synopsys resource r0 : ops = "op1 op2";
      */
     casex (s)
       2'b00: x = a + b;     //synopsys label op1
       2'b01: y = a + c;     //synopsys label op2
       2'b1x: z = b + c;     //synopsys label op2 appears twice, invalid
     endcase
   end
```

WHAT NEXT

analyze (2), **read** (2).

HDL-146 (error) Type function '%s' not found %s

DESCRIPTION

This error occurs when the *type function* identified with the **type_function** pragma cannot be found. Used in conjunction with the the **map_to_operator** pragma, the **type_function** pragma defines the return type of the function in which the **type_function** pragma is used.

WHAT NEXT

Provide the function referred to in the **type_function** pragma.

NOTE

Use of *type_function* is discouraged. Use *output_port_type* instead.

HDL-147 (error) Ports of type function '%s' don't match %s

DESCRIPTION

This error occurs when the ports in the function identified by the **type_function** pragma do not match the ports in the function in which the *type_function* is embedded.

WHAT NEXT

Modify the type function so the ports match.

NOTE

Use of *type_function* is discouraged. Use *output_port_type* instead.

HDL-148 (error) Invalid constraint on an enumeration type %s

DESCRIPTION

This error occurs when the subrange of an enumerated type does not match the type declaration. This can occur if the range is out of order or the direction does not match.

WHAT NEXT

Change the subrange expression to match the enumeration declaration.

HDL-149 (error) Synthetic library has no one-bit multiplexor.

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-150 (error) Component implication (map_to_entity) subprogram port ’%s’ has an unconstrained type %s

DESCRIPTION

This error occurs when you use a subroutine with a map_to_entity attribute, and one of the subroutine’s ports is unconstrained. All port types must be constrained before you can use map_to_entity.

WHAT NEXT

Add range constraints to the port type declarations.

HDL-151 (error) You are only allowed to use state vector ’%s’ in one process per design.

DESCRIPTION

This error indicates that the state_vector attribute was used more than once in an entity or module. Each entity or module is allowed a single state vector.

WHAT NEXT

If you need two state vectors (to implement communicating state machines, for

example) put each state machine in a separate entity or module. If you only need one state vector, then remove the extraneous state vector attribute.

HDL-152 (error) Expected an enumeration literal %s

DESCRIPTION

This error occurs when an enumeration literal is expected, but something else is supplied. For example, this can occur in an enumeration subrange where the bounds should be specified by enumeration literals, but are instead specified by integers.

WHAT NEXT

Use an enumeration literal where it is expected.

HDL-153 (warning) Share effort '%s' is not supported. Using 'low' share effort instead.

DESCRIPTION

The hlo_share_effort must be one of 'low', 'medium' or 'high'.

WHAT NEXT

The program will work with 'low' effort. If you want a different effort level, please correct the spelling in your dc_shell script.

HDL-154 (error) Inconsistent port declaration detected for port%s %s

DESCRIPTION

This error occurs when port names in subroutine calls do not match the names in the subroutine definition.

WHAT NEXT

Make sure the subroutine call and subroutine definition port names match.

HDL-155 (error)Index value '%d' is not within array bounds [%d, %d] %s

DESCRIPTION

This error occurs when the index value is not within the bounds specified for the array.

WHAT NEXT

Modify the description so that the index value lies within the array bounds.

EXAMPLES

Verilog:

```
reg [3:0] my_bus;
wire foo;

assign foo = my_bus[4];
/* 4 is outside the array bounds [0,3] */
```

VHDL:

```
variable my_bus: bit_vector (0 to 3);
signal foo: bit;

foo <= my_bus(4);
-- 4 is outside the array bounds [0,3]
```

HDL-156 (error) Index range [%d,%d] is not within array bounds [%d,%d] %s

DESCRIPTION

This error occurs when the index range is not within the bounds defined for the array.

WHAT NEXT

Modify the description so that the index range is within the bounds defined for the array.

EXAMPLES

Verilog:

```
reg [3:0] my_bus;
wire [1:0] foo;

assign foo = my_bus[4:3];
/* 4 is outside the array bounds [0,3] */
```

VHDL:

```
variable my_bus: bit_vector (0 to 3);
signal foo: bit_vector (0 to 1);

foo <= my_bus(4 downto 3);
-- 4 is outside the array bounds [0,3]
```

HDL-158 (warning) State vector '%s' was specified, but is not a valid state vector.

DESCRIPTION

The state vector directive identifies the variable that holds the state of a state machine. See or for more information on the state vector directive.

This error occurs when the variable identified in the directive either does not exist, or did not get a flip-flop to hold its value. For more information on how to get the HDL Compiler to build a flip-flop to hold the value of a variable, see or .

WHAT NEXT

Spell the variable in the state vector directive so it matches the variable declaration. Next, check the inferred devices report (see). If the state variable does not appear in the report, or if the memory device listed is not a flip-flop, modify your description to assign the variable on the edge of a clock.

EXAMPLES

-- VHDL

```
entity e is
port(clock, a: in bit; z: out bit);
end;
architecture a of e is
signal state : bit;
attribute state_vector : string;
attribute state_vector of a:architecture is "state";
```

```
begin
process begin
-- This will fail because the wait is disabled
-- wait until clock'event and clock = '1';
state <= state xor a;
end process;
z <= state;
end;

/* Verilog */
module e(clock, a, z);
input clock, a;
output z;
reg state;
/* The variable name is misspelled */
/* synopsys state_vector statex */
always @(posedge clock) begin
state = state ^ a;
end
assign z = state;
endmodule
```

EXAMPLE MESSAGE

```
Warning: State vector 'statex' was specified, but is not a valid state vector. (HDL-
158)
```

HDL-159 (error) Operator '%s' not found in synthetic library.

DESCRIPTION

The operator defined by a *map_to_operator* attribute was not described in any of the synthetic libraries in the *synthetic_library* variable (and was not found in **standard.sldb**).

WHAT NEXT

If you want to use the synthetic library operator, make sure it can be found in the files defined by *synthetic_library*.

HDL-160 (warning) No synthetic_library specified. Resource sharing is disabled.

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-162 (warning) may_merge_with and dont_merge_with conflict in resource '%s'
may_merge_with ignored %s

DESCRIPTION

This error occurs when you state that two resources may merge and also that they may *not* merge. For example, if you indicate that resource R0 may merge with R1, but that R1 may not merge with R0, you will get this error. For more information see the "User Directive Conflicts" section of the "Resource Sharing" chapters in either of the the reference manuals for VHDL and Verilog compiler.

WHAT NEXT

Modify your directives so that the **may_merge_with** and **dont_merge_with** directives do not disagree.

HDL-163 (error) Resolution function '%s' must be labeled with a "resolution_method" pragma
. Resolution functon ignored %s.

DESCRIPTION

The VHDL Compiler does not support arbitrary resolution functions. It supports *wired_and*, *wired_or* and *three_state* as resolution methods. Any function that is used as a resolution function must include a *resolution_method* pragma that indicates which of the three supported resolution methods is to be used. This error occurs when the *resolution_method* pragma is missing.

WHAT NEXT

Add one of the following *resolution_method* pragma to the resolution function: *wired_and*, *wired_or*, or *three_state*

HDL-164 (error) Resolution function '%s' is not legal for variable or type %s

Use "wired_and", "wired_or", or "three_state" %s.

DESCRIPTION

The VHDL Compiler does not support arbitrary resolution functions. It supports *wired_and*, *wired_or* and *three_state* as resolution methods. Any function that is used as a resolution function must include a *resolution_method* pragma that indicates which of the three supported resolution methods is to used. This error occurs when the *resolution_method* pragma indicates a resolution method other than the three methods supported.

WHAT NEXT

Modify the *resolution_method* pragma for the resolution function to be one of the following: *wired_and*, *wired_or* or *three_state*.

HDL-165 (error) Cannot find resolution function '%s'. Resolution function ignored.

DESCRIPTION

The indicated function could not be found. This happens when the name of the function is spelled incorrectly.

WHAT NEXT

Check to make sure all resolution functions are provided and spelled correctly.

HDL-167 (error) %s contains the invalid string '%s'.

DESCRIPTION

This error occurs when an environment variable should have a string value, but instead the value has some other type.

WHAT NEXT

When you assign the value of the environment variable, you can use double quotes around the value you assign to insure it is a string.

HDL-169 (warning) The state-vector does not fan out. It's flip-flops are being deleted.

DESCRIPTION

HDL Compiler removes all logic which does not eventually fan out to out or inout ports. This warning occurs when the state vector flip flops are deleted due to a lack of fanouts. This does not necessarily indicate an error, but it probably means that the state machine is not hooked up properly.

WHAT NEXT

If you know that the state vector is unused, then you can safely ignore this warning. Otherwise, check the connections in your state machine to be sure the output ports, next-state logic and state vector communicate properly.

HDL-170 (warning) Comparisons to a '%s' are treated as always being false %s
This may cause simulation to disagree with synthesis.

DESCRIPTION

Comparisons in hardware are inherently different than in the simulator. Digital hardware comparators can only distinguish between ones and zeros. Thus, it makes no sense to synthesize comparisons to three-state, don't-care or unknown literals. Since signals are assumed to carry a value of one or zero, equality tests to non-one/zero values always return false in synthesis.

WHAT NEXT

There is probably no need to modify your HDL if the comparison was used for simulation purposes only. For example, if you want to print an message when an input port is in the high-impedance state, it is ok to compare its value to 'z'. If you are using the comparison to affect the state of your circuit, you should consider recoding your HDL. For example, if you need a four-state state-machine, don't declare a single-bit variable and use 0, 1, x, and z as your states. In hardware, each bit only holds two useful states: 1 and 0.

HDL-172 (error) Variable%s, which is assigned using RTL

assignment, cannot accept return values from a task call%s.

DESCRIPTION

You receive this message during the issuance of a **read** command or an **elaborate** command, when a variable that is the target of an RTL assignment is passed to an output or inout argument of a task call.

HDL Compiler does not let you mix RTL (nonblocking) and procedural (blocking) assignments and pass them to a given variable in one process (see VE-57). HDL Compiler treats task arguments of type output or inout as procedural (blocking) assignments. Therefore, you cannot combine them with RTL (nonblocking) assignments to the same variable within a process.

In the following example, *y* is the target of an RTL assignment and is passed to the output argument of task *t*. This code causes HDL Compiler to issue HDL-172.

```
task t;
  input a;
  output z;

  z = ~a;
endtask

always @(posedge ck) begin
  if (reset)
    y <= 0;
  else
    t (x, y);
end
```

WHAT NEXT

Avoid this error by using procedure assignments for variables that must be passed to output or inout arguments of task calls. For example, the always block in the example above could be rewritten like this:

```
always @(posedge ck) begin
  if (reset)
    y = 0;
  else
    t (x, y);
end
```

SEE ALSO

elaborate (2), **read** (2); **VE-57** (n).

HDL-173 (warning) Add_ops attribute value "%s" is not valid for

resource ’%s’.
Attribute value is assumed to be "false".

DESCRIPTION

The value shown is not valid. The value assigned for **add_ops** must be either "true" or "false".

WHAT NEXT

Assign either "true" or "false" for **add_ops**.

HDL-174 (error) Variable%s of type ’wire’ cannot accept return values from a task call%s.

DESCRIPTION

This error occurs when a variable of type *wire* is passed to an output or inout argument of a task call.

WHAT NEXT

Modify your description so that the variable passed to the output or inout argument of the task is of type *reg*.

HDL-175 (error) Clock variable ’%s’ is being used as data %s.

DESCRIPTION

The synthesis policy does not support the use of a value as both clock and data in the same process.

WHAT NEXT

If you need to compute a value that is based on a clock signal (for example, to generated a gated clock), then you must perform the computation outside any process that that is sensitive to the clock edge.

HDL-176 (warning) Variable ’%s’ is being read asynchronously

%s.
This may cause simulation-synthesis mismatches.

DESCRIPTION

This warning occurs in the asynchronous reset part of a process or always block. It occurs when a value not in the sensitivity list or block timing control is read.

This typically occurs when a non-constant value is assigned on the asynchronous reset.

In the following example reset_data is incorrectly read:

```
-- VHDL
entity e is
port(clock, a, reset_enable, reset_data: in bit; z: out bit);
end;
architecture a of e is
begin
process (clock, reset_enable) begin
if(reset_enable = '1') then
z <= reset_data -- WARNING
elsif(clock'event and clock = '1') then
z <= a;
end if;
end process;
end;

/* Verilog */
module e(clock, a, reset_enable, reset_data, z);
input clock, a, reset_enable, reset_data;
output z;
reg z;

always @(posedge clock or posedge reset_enable) begin
if(reset_enable) z = reset_data; /* WARNING */
else z = a;
end
assign z = state;
endmodule
```

The problem with this description is that the simulation model does not react to changes in reset_data while reset_enable is held high.

WHAT NEXT

In VHDL the solution is to add reset_data to the process sensitivity list.

In Verilog, you can't add reset_data to the sensitivity list without breaking the model. Thus, In the above case Synopsys recommends that you verify that your model does not rely on the fact that during reset, the simulator holds z steady even though reset_data changes. The synthesized register will be transparent during

reset.

HDL-177 (warning) Local variable ’%s’ is being read before its value is assigned,
%s.
This may cause simulation not to match synthesis.

DESCRIPTION

HDL Compiler assumes that processes should run whenever doing so would change an output value. If a description is written so that the simulator might not execute a process even though doing so could change an output, HDL Compiler displays a warning. The incomplete sensitivity list warning (see **HDL-179**) tells when a signal is read but it is not on the sensitivity list. A simulation/synthesis mismatch can occur when the signal changes because the synthesized hardware reacts immediately, whereas the simulator waits for an event on the sensitivity list.

This warning is similar to **HDL-179**, but it happens with variables instead of signals. The difference is that you can’t fix the problem by adding to the sensitivity list because variables are not allowed in the sensitivity list.

The following example shows how such a situation can cause a simulation/synthesis mismatch:

```
entity e is
port(a: in bit; z: out bit);
end;

architecture a of e is
begin
process(a)
variable temp: bit;

z <= temp; -- WARNING
temp := a;
end process;
end;
```

HDL Compiler builds a circuit with ’a’ feeding directly to ’z’. The simulator, however, feeds the opposite value. Consider what happens when ’a’ transitions from ’0’ to ’1’. At the start of the process, ’temp’ holds a ’0’, so ’z’ is driven with ’0’. At the end of the process, ’temp’ is assigned ’1’, the new value of a. When ’a’ transitions from ’1’ to ’0’, the process runs a second time, and the ’1’ in temp finally makes it to the output. Notice that ’z’ lags one step behind ’a’. In this case it means that ’z’ is really equal to ’not a’.

WHAT NEXT

You can fix this problem by making default assignments to all variables as the first step in a process. Or you can reorder the computations in the process to read variables only after they have been set.

The following example shows a fixed version of the previous example. Notice that the assignments are reordered.

```
entity e is
port(a: in bit; z: out bit);
end;

architecture a of e is
begin
process(a)
variable temp: bit;
begin
temp := a;
z <= temp;  -- OK
end process;
end;
```

EXAMPLE MESSAGE

Warning: Local variable 'temp' is being read before its value is assigned, in routine e line 7 in file 't.v'. This may cause simulation not to match synthesis. (HDL-177)

HDL-178 (warning) Only simple variables are checked in the sensitivity list. The variable in the sensitivity list on line %d is ignored.

DESCRIPTION

The list of variables to which a process (in VHDL) or an *always block* (in Verilog HDL) is sensitive must contain simple variable names. Lists that contain indexed variables or not-processed variables are ignored.

WHAT NEXT

If possible, rewrite the description so that the sensitivity list contains only simple names. As you rewrite the description, be careful not to introduce errors by making the process or block sensitive to more variables than necessary. The usual workaround is to assign to a temporary variable the required bit or slice of the variable, and to make the process or block sensitive to this temporary variable.

EXAMPLES

VHDL

```
process ( bus(1) ) begin
-- bus(1) is not a simple variable. The workaround follows:

temp := bus(1);
process ( temp ) begin
```

Verilog

```
always @ (bus[1]) begin
// bus[1] is not a simple variable. The workaround follows:

assign temp = bus[1];
always @ ( temp ) begin
```

HDL-179 (warning) Variable ’%s’ is being read %s, but is not in the process sensitivity list of the block which begins there.

DESCRIPTION

Since the hardware generated by the HDL compiler is sensitive to to all inputs, you should normally include all read signals in a process’s sensitivity list. This warning is displayed when you don’t.

The following example shows why it is important to include all read signals in the sensitivity list:

```
entity e is
port(a, b: in bit; z: out bit);
end;

architecture a of e is
begin
process(a) begin
z <= a xor b;
end process;
end;
```

HDL Compiler builds a circuit with an ’xor’ gate reading ’a’ and ’b’, and driving ’z’. Whenever either ’a’ or ’b’ changes, the hardware immediately computes a new value for ’z’.

The simulator, in contrast, executes the process only when ’a’ changes, since ’b’ was left out of the sensitivity list. Thus, while ’a’ keeps a steady value, the simulator does not propagate changes in ’b’ to the output. This can cause a simulation/synthesis mismatch.

WHAT NEXT

It is always safer to include values in the sensitivity list to ensure an accurate modeling of the hardware. If you want to leave values out (for simulation efficiency, for example), you should convince yourself that leaving them out does not change the results computed by the simulator, and then ignore this warning.

If you are not sure whether delaying the execution of a process will affect the results, it is safer to simply add the value to the list.

For example, the above description would be much safer if written:

```
entity e is
port(a, b: in bit; z: out bit);
end;

architecture a of e is
begin
process(a, b) begin
z <= a xor b;
end process;
end;
```

EXAMPLE MESSAGE

Warning: Variable 'b' is being read in routine e line 8 in file 'b.v', but is not in the process sensitivity list of the block which begins there. (HDL-179)

HDL-180 (warning) Variable '%s' is being read %s, but does not occur in the timing control of the block which begins there.

DESCRIPTION

A variable is missing from the timing control, also known as the sensivity list. This warning indicates which variable is missing from the list.

Leaving a variable out of the sensitivity list can cause simulation to disagree with synthesis. Simulation only propagates changes for variables when they appear in the sensivity list. Synthesized hardware will propagate changes even for variables missing from the sensitivity list.

The following example shows the importance of a complete sensitivity list:

```
module e(a, b, z);
input a, b;
output z;
reg z;
always @( a ) begin  /* Incomplete sensitivity list */
```

```
z = a ^ b;
end
endmodule
```

HDL Compiler builds a circuit with an 'xor' gate reading 'a' and 'b', and driving 'z'. Whenever either 'a' or 'b' changes, the hardware immediately computes a new value for 'z'.

The simulator, in contrast, executes the always block only when 'a' changes, since 'b' was left out of the sensivity list. Thus, while 'a' keeps a steady value, the simulator does not propagate changes in 'b' to the output. This situation can cause a simulation/synthesis mismatch.

WHAT NEXT

To ensure an accurate modeling of the hardware, it is always safer to include values in the sensitivity list. If you want to omit values (for simulation efficiency, for example), first verify that leaving them out won't change the results computed by the simulator then ignore this warning.

If you are not sure whether delaying the execution of a block will affect the results, it is safer simply to add the value to the list.

For example, the previous description would be much safer if written

```
module e(a, b, z);
input a, b;
output z;
reg z;
always @( a or b ) begin  /* Much safer */
z = a ^ b;
end
endmodule
```

EXAMPLE MESSAGE

```
Warning: Variable 'b' is being read
        in routine e line 6 in file 'b.v',
        but does not occur in the timing control of the block which begins
        there.   (HDL-180)
```

HDL-183 (error) The multi-bit clock '%s' is not supported %s.

DESCRIPTION

This error occurs when the variable that serves as the clock for a description is greater than 1 bit in width. The clocking variable for a design is the one that is specified in VHDL statements such as: wait until clock'event and clock = '1' ; and in Verilog statements as: always @ (posedge clock)

WHAT NEXT

Rewrite your description to specify a 1-bit wide clock.

HDL-184 (error) Case statement was not fully specified. (There exists no TRUE branch)%s

DESCRIPTION

This error occurs if none of the case statement alternatives match the case expression in a case statement.

WHAT NEXT

Modify your HDL description so that at least one case statement alternative can match the case expression.

HDL-185 (error) Couldn’t find the package ’%s’ in memory.

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-186 (error) An order based parameter was specified after a name based parameter for the template ’%s’ %s

DESCRIPTION

This error happens when the argument to the *elaborate* command includes a combination of order-based and name-based parameter values, and all the order-based parameters are not specified before name-based parameters.

WHAT NEXT

Modify the arguments to the *elaborate* command so that all order-based parameters occur before name-based parameters.

HDL-187 (error) Too many parameters were specified for the template '%s'.

DESCRIPTION

This error occurs when the argument to the *elaborate* command includes more parameter values than the number of generics (parameters) that exist in the design.

WHAT NEXT

Modify the arguments to the *elaborate* command to remove the extra parameters.

HDL-188 (error) The parameter '%s' does not exist on template '%s'.

DESCRIPTION

This error occurs when the argument to the *elaborate* command includes a parameter value for a generic (parameter) that does not exist in the design. This error can also occur when a parameterized design is instantiated in VHDL with a named parameter that does not exist in the intantiated entity.

WHAT NEXT

Remove the incorrect parameter from the arguments to the *elaborate* command.

HDL-189 (error) Couldn't find the template '%s' in memory.

DESCRIPTION

This is a non-fatal internal error.

WHAT NEXT

Contact your Synopsys support representative.

HDL-190 (error) The variable '%s' has an illegal format. Please check documentation.

DESCRIPTION

This error occurs when the format specified for naming the template of a design ("template_name_style") or for naming the architecture of a design (when writing out VHDL) has an invalid character.

WHAT NEXT

See the "Design Compiler Interface" chapter of the VHDL Compiler manual for the correct way to set this variable. Modify the appropriate variable to be of the specified format.

HDL-191 (error) The parameter '%s' is not a valid integer.

DESCRIPTION

This error occurs when the value specified for a generic (parameter in Verilog) is not an integer.

WHAT NEXT

Rerun the elaborate command with the correct value for the parameter.

HDL-192 (warning) '%s' is an invalid argument for variable '%s'.

DESCRIPTION

WHAT NEXT

HDL-193 (information) Building the design '%s'%s.

DESCRIPTION

This information message is issued when a new design is being built as a result of the **read** or **elaborate** command.

WHAT NEXT

HDL-194 (error) Could not find the template %s

DESCRIPTION

This error occurs when the template specified to the *elaborate* or similar commands does not exist or was not found because of incorrect library specification (in VHDL).

WHAT NEXT

Check to see if the name of the template has been correctly spelled. If using VHDL, check to make sure that the libraries have been correctly specified.

HDL-195 (error) Couldn't find the symbol '%s'. This is probably because the %s '%s' is not the same %s that the %s '%s' was analyzed with.

DESCRIPTION

This error can happen if a design unit is analyzed with a package, and then is elaborated with another package. Normally, this will be flagged as an error. However, if both versions of the package were analyzed before the entity was, the timestamp checking will think that this is okay, but if the packages are significantly different, problems may occur.

WHAT NEXT

Re-analyze all of the source code from scratch.

HDL-196 (error) User specified sharing information caused combinational loops in design '%s'.

DESCRIPTION

This error happens if combinational loops are created through user specified sharing

information. The following example shows how such a loop could be created.

```
// synopsys resource r1 : ops = "a0 b1";
// synopsys resource r2 : ops = "a1 b0";

if (s) begin
   tmp = a + b;  // synopsys label a0;
   z = tmp + c;   // synopsys label a1;
end
else begin
   tmp = d + e;  // synopsys label b0;
   z = tmp + f;   // synopsys label b1;
end
```

WHAT NEXT

Check the pragmas in your HDL file and remove the sharing that causes the combinational loop.

HDL-200 (error)'default' clause must be the last clause in a case statement.

DESCRIPTION

In a Verilog HDL case statement, the *default* clause must be the last clause. This error occurs if this condition is not met.

WHAT NEXT

Rewrite your description so that the *default* clause occurs last in the case statement.

HDL-201 (error) Character '%c' is not allowed in the variable '%s'.

DESCRIPTION

This error occurs when the format specified for seperators in the name of a template ("template_seperator_style") contain illegal characters. This error may also occur if the format for naming an architecture (when writing out VHDL) contains illegal characters.

WHAT NEXT

See the "Design Compiler Interface" chapter of the VHDL Compiler manual for the correct way to set this variable. Modify the format so that it contains only legal characters.

HDL-202 (information) Saving the %s ’%s’.

DESCRIPTION

This information message is issued when a design (module, entity, or architecture) or a package is being saved to the disk.

WHAT NEXT

HDL-203 (information) Overwriting the %s ’%s’.

DESCRIPTION

This information message is issued when the new design or package that is being processed overwrites an existing design or package of the same name.

WHAT NEXT

HDL-204 (error) Too many generics were specified%s

DESCRIPTION

This error occurs when more generics are specified as arguments to the "elaborate" command than are specified in the description of the design being elaborated.

WHAT NEXT

Check the design description to find the correct number of generics and rerun the "elaborate" command with the correct number of generics.

HDL-205 (error) The value specified for generic ’%s’ is out of

range%s

DESCRIPTION

This error occurs when the value specified for a generic is bigger than the maximum or smaller than the minimum allowable value for the generic.

WHAT NEXT

Check the description of the design being elaborated to find the allowable value of the generic and rerun the "elaborate" command with the correct value for the generic.

HDL-206 (error) Cannot determine type of the aggregate %s (This error can occur if an aggregate and a generic appear in the same component instantiation.)

DESCRIPTION

This error occurs if a generic map is used and if a port is indexed (or sliced) on the left hand side of a port map clause of a component instantiation statement.

WHAT NEXT

Modify the HDL description to (a) replace the generic with a constant or (b) not slice or index the port on the left hand side of the port map statement.

HDL-207 (error) %s contains the invalid list '%s'.

DESCRIPTION

This error occurs when the dc_shell variable "vhdlout_conversion_functions" is set to an incorrect value.

WHAT NEXT

See the "Design Compiler Interface" chapter of the VHDL Compiler manual for the correct way to set this variable.

HDL-208 (warning) hdlin_source_to_gates_mode set to invalid

value "%s", "off" will be used instead.

DESCRIPTION

This warning occurs when the dc_shell variable "hdlin_source_to_gates_mode" is not set to a valid value.

WHAT NEXT

Set the variable to a correct value.

HDL-209 (warning) The VHDL design ’%s’ contains generics but was treated as a "design." To save as a "template", which can be instantiated with different parameters, use the "analyze" command. This is recommended since this does not require changing HDL code or setting any variables. Alternately reread file(s) with ’%s = "TRUE"’, or insert the synthetic comment "template" in the HDL source.

DESCRIPTION

This warning occurs if a design is read in using the "read" command. Use the "analyze" command if you want to elaborate this design with different values for the generics.

WHAT NEXT

HDL-210 (error) Can’t find port ’%s’ on synthetic operator ’%s’ %s

DESCRIPTION

You receive this message because, during processing of a function that has a

map_to_operator pragma, the compiler has not found a match between the names of formal parameters and the names of input ports of the synthetic operator.

WHAT NEXT

Correct the code so that these two entities contain the same names. For more information about the **map_to_operator** pragma, see Chapter 4 of the *DesignWare Developer Guide*.

SEE ALSO

analyze (2), **read** (2); **compile** (2).

HDL-211 (warning) Configurations are ignored during %s. The %s/%s commands must be used to build a configuration.

DESCRIPTION

VHDL source files that contain configurations must be read in using the **analyze** command. If they are read in using the **read** command, the configuration statements are ignored.

WHAT NEXT

If the configuration statements should not be ignored, read in the VHDL source file using the **analyze -f vhdl** command. You can then build the design by using the **elaborate** command.

HDL-213 (error) The library '%s' is mapped to the directory '%s' which is not writable. The VHDL analyzer can not be invoked.

DESCRIPTION

All library names have a mapping to a UNIX directory in dc_shell. These mappings are done either in your '.synopsys_vss.setup' file or by the dc_shell command 'define_design_lib'.

The 'read -f vhdl' command writes intermediate files to the library WORK. The corresponding UNIX directory was not writable, or did not exist at the time the read command was invoked.

WHAT NEXT

Change the mapping for library WORK either in your .synopsys_vss.setup file or by using the define_design_lib command. Also make sure the corresponding UNIX directory exists and has the necessary permissions.

The .synopsys_vss.setup file is read only once, at program start up. Hence, if you change the mapping here you must re-start dc_shell or design_analyzer for the change to take effect.

Note that there is a search path involved for the .synopsys_vss.setup file. If there is one in the directory where the dc_shell is started it will be used. Else if there is one in your home directory it will be used. Else the one in <synopsys_root>/admin/setup/ will be used. If only some setup information was found in a file outside <synopsys_root>/admin/setup/.synopsys_vss.setup, the next one is read to get the missing information.

HDL-220 (warning) Variable '%s' is driven in more than one process or block in file %s This may cause mismatch between simulation and synthesis.

DESCRIPTION

In simulation, the **always** block last fired up drives the variable (the drivers are multiplexed). In synthesis, the drivers are shorted together. This situation is especially serious if the values driven by two **always** blocks are different constants, since this will short power to ground.

The HDL Compiler does not keep track of individual bits in a bus when issuing this warning. If bits of a bus are driven from different **always** blocks, and each bit is driven from one block only, this warning is still issued even though simulation and synthesis match.

WHAT NEXT

If individual bits of a bus are driven from a single block, you can ignore this warning. Otherwise, move the drivers of the variable into the same **always** block or use a three-state bus. If the problem came from the reuse of a loop variable, declare separate loop variables for each block.

FIRST EXAMPLE

In the following example, the simulator will assign 'C' from either 'A' or 'B', depending on which changed most recently. HDL Compiler simply shorts 'A' and 'B' to 'C'.

```
module VERILOG_EXAMPLE ( A, B, C );
input  A, B;
output C;
reg    C;
    always @( A ) begin
      C = A ;
    end
    always @( B ) begin
C = B;
    end
endmodule
```

EXAMPLE MESSAGE

```
Warning: Variable 'C' is driven in more than one process or block
        in file /home/mine/design/dir/x220.ver
        This may cause mismatch between simulation and synthesis. (HDL-220)
```

SECOND EXAMPLE

In the following example, 'i' is used as a loop index in two **always** blocks. The result is that 'i' is driven in both processes by different constants. Both power and ground are shorted onto 'i'. This is a serious problem that should be fixed by declaring separate loop variables for each block.

```
module VERILOG_EXAMPLE ( A, B, C );
input  [3:0] A, B;
output [3:0] C;
reg    [3:0] C;
integer i;

    always @( A ) begin
      for (i=0; i<=1; i=i+1) C[i] = A[i];
    end
    always @( B ) begin
      for (i=2; i<=3; i=i+1) C[i] = B[i];
    end
endmodule
```

EXAMPLE MESSAGE

```
Warning: Variable 'i' is driven in more than one process or block
        in file t.v
        This may cause mismatch between simulation and synthesis. (HDL-220)
Warning: Variable 'C' is driven in more than one process or block
        in file t.v
        This may cause mismatch between simulation and synthesis. (HDL-220)
```

The first warning in this example is serious because the first block drives a '1' onto 'i', and the second block drives a '3'. The second warning is not serious because different bits of 'C' are driven from each block.

HDL-222 (error) Process %s has both a sensitivity list as well as embedded wait statements.

DESCRIPTION

The use of wait statement in a function or process is mutually exclusive with the use of a sensitivity list.

WHAT NEXT

Remove the sensitivity list or re-write the offending code to not make use of the wait statement.

EXAMPLE

```
entity MULTWAIT_VHDL is
    port( I1, I2: in BIT ;
          CLOCK : in BIT ;
          Out_Port : out BIT );
end MULTWAIT_VHDL;

architecture test_behavior of MULTWAIT_VHDL is
begin
    process ( clock ) begin
      wait until clock'event and clock = '1' ;
      Out_Port <= I1 ;
      wait until clock'event and clock = '1' ;
      Out_Port <= I2 ;
    end process;
end test_behavior;
```

EXAMPLE MESSAGE

```
      wait until clock'event and clock = '1' ;
      ^
**Error: vhdlan,1044 /home/mine/design/dir/x222.vhd(10):
    Wait statement must not appear in a function or a process which has a
    sensitivity list.
      wait until clock'event and clock = '1' ;
      ^
**Error: vhdlan,1044 /home/mine/design/dir/x222.vhd(12):
    Wait statement must not appear in a function or a process which has a
    sensitivity list.
```

HDL-223 (error) Always block %s has both a timing control

statement as well as embedded event (’@’) expressions.

DESCRIPTION

You receive this message to inform you that the always block in your design cannot contain, as it does, both a timing control statement and embedded event (’@’) expressions because the code as written does not accommodate this construction. The example shown illustrates a similar instance:

```
module multwait_V( I1, I2, CLOCK, Out_Port);
input CLOCK;
input   I1, I2;
output  Out_Port;
reg Out_Port ;

always @( posedge CLOCK)
begin  : process_blk
  @(posedge CLOCK)
  Out_Port = I1;
  @(posedge CLOCK)
  Out_Port = I2;
end
endmodule
```

The following example shows the error message that the compiler would issue in response to the above code:

```
Error: Always block
        in routine multwait_V line 7 in file ’/home/mine/design/dir/x223.ver’
        has both a timing control statement as well embedded
        event (’@’) expressions.  (HDL-223)
```

WHAT NEXT

Remove the timing control statement or rewrite the code so that it does not make use of embedded event expressions.

SEE ALSO

analyze (2), **read** (2).

HDL-224 (error) Wait statements in process %s use different clocks or clock edges.

DESCRIPTION

All wait statements in same process must be triggered by same clock edge.

WHAT NEXT

Modify the offending process' wait statements to be triggered by same clock edge.

EXAMPLES

In this example one wait statement is triggered by a rising clock edge while the other is triggered by the falling clock edge.

```
entity MULTWAIT_VHDL is
    port( I1, I2: in BIT ;
          CLOCK : in BIT ;
          Out_Port : out BIT );
end MULTWAIT_VHDL;

architecture test_behavior of MULTWAIT_VHDL is
begin
    process begin
      wait until clock'event and clock = '1' ;
      Out_Port <= I1 ;
      wait until clock'event and clock = '0' ;
      Out_Port <= I2 ;
    end process;
end test_behavior;
```

EXAMPLE MESSAGE

```
Error: Wait statements in process
        in routine MULTWAIT_VHDL line 0 in file '/home/mine/design/dir/x224.vhd'
        use different clocks or clock edges. (HDL-224)
```

HDL-225 (error) Event ('@') expressions in always block %s use different clocks or clock edges.

DESCRIPTION

You receive this message to inform you that the always block in your design cannot contain event expressions ('@') that use different clocks or clock edges.

The example shown illustrates a similar instance, one in which the event expressions are triggered by positive and negative clock edges, respectively.

```
module multwait_V( I1, I2, CLOCK, Out_Port);
input CLOCK;
input   I1, I2;
output  Out_Port;
reg Out_Port ;

always
```

```
begin  : process_blk
  @(posedge CLOCK)
  Out_Port = I1;
  @(negedge CLOCK)
  Out_Port = I2;
end
endmodule
```

The following example shows the error message that the compiler would issue in response to the above code:

```
Error: Event ('@') expressions in always block
        in routine multwait_V line 7 in file '/home/mine/design/dir/x225.ver'
        use different clocks or clock edges. (HDL-225)
```

WHAT NEXT

Modify the offending always block's event ('@') expressions so that they are triggered by same clock edge.

SEE ALSO

analyze (2), **read** (2).

HDL-226 (error) Process %s contains unsupported wait statements.

DESCRIPTION

WHAT NEXT

HDL-227 (error) Always block %s contains unsupported event ('@') expressions.

DESCRIPTION

Event expressions are not supported in subprograms or **for** loops.

WHAT NEXT

Modify subprograms not to contain event expressions or "inline" them. Change **for** loops into **forever** loops.

EXAMPLES

Example of unsupported **for** loop:

```
module V1(a, b, clock, d);
input   [0:3] a, b ;
input   clock ;
output  [0:3] d;
reg d;

integer i;
always begin
  for (i = 32'd0;  /* for-loop enclosing event expression, not supported */
       i < 32'd4;
       i = i + 32'd1)
  begin
    @ (posedge clock)
    d[i] = a[i] & b[i];
  end
end
```

Above example rewritten into supported format:

```
module V2(a, b, clock, d);
input   [0:3] a, b ;
input   clock ;
output  [0:3] d;
reg d;

integer i;
always begin
  i = 32'd0;/* init of loop-invariable */
  forever
  begin : infinite_label
    i = i + 32'd1; /* increment loop-invariable */
    @ (posedge clock)
    d[i] = a[i] & b[i];
    if( i > 32'd4) disable infinite_label; /* loop exit */
  end
end
```

EXAMPLE MESSAGE

```
Error: Always block
        in routine V1 line 9 in file '/home/my/design/x227.ver'
        contains unsupported event ('@') expressions. (HDL-227)
```

HDL-230 (error) '%s' is used as a name for an internal package. Please use

a different name for your package.

DESCRIPTION

You have defined a package name that conflicts with a built-in package. The built-in packages are "vhdl," "verilog," and VHDL's predefined "standard."

WHAT NEXT

Because these packages are built in, they are always present. Hence, the VHDL library clause is of no help here.

You must modify the name of the conflicting package.

EXAMPLES

```
-- VHDL
package standard is
end;
```

EXAMPLE MESSAGE

```
Error: "standard" is used as a name for an internal package. Please use
        a different name for your package. (HDL-230)
```

HDL-231 (warning) The enum encoding '%s' is not a valid state machine encoding.
The state name for the state '%s' will not be saved.

DESCRIPTION

The Synopsys state machine compiler only accepts 0 or 1 encodings for its states. For example, a don't care state is not passed to the state machine compiler during the subsequent extract information. The logic for the state is still treated correctly but the encoding for the state will not be shown by the *report_fsm* command.

For a don't care state, it is possible that every time the state is referenced, it will receive a different encoding.

WHAT NEXT

Be aware that state machine encodings other than 0 or 1 will not not be saved.

HDL-232 (error) The encoding '%s' for state '%s' is invalid.

DESCRIPTION

Valid states that can be passed to the Synopsys state machine compiler are vectors of 0's and 1's. don't care states are parsed and ignored, but no other states are valid.

WHAT NEXT

Change the encoding for the state to a valid encoding.

HDL-233 (warning) The encoding '%s' for state '%s' is a duplicate of state '%s'. This state name will not be saved.

DESCRIPTION

There were two states in your design with identical encodings. The second state name will not be saved.

WHAT NEXT

To avoid this warning, replace all references to the duplicate state name with the original state name and remove the definition for the duplicate state.

HDL-234 (warning) Design '%s' has multiple architectures defined. The first architecture defined ('%s') will be used to build the design.

DESCRIPTION

VHDL allows you to define multiple architectures for one entity. When using the **read** command, however, only one design is built per entity. As a result, only the first architecture encountered is used.

WHAT NEXT

You can use the **analyze** or **elaborate** commands to build architectures other than the

first one defined in your design.

EXAMPLES

```
ENTITY A_VHDL IS
END ;

ARCHITECTURE DOIT OF A_VHDL IS
BEGIN
END ;

ARCHITECTURE DOIT_AGAIN OF A_VHDL IS
BEGIN
END ;
```

EXAMPLE MESSAGE

```
Warning: Design 'A_VHDL' has multiple architectures defined.
        The first architecture defined ('DOIT') will be
        used to build the design. (HDL-234)
```

HDL-235 (error) Could not read 'gtech.db' in the libraries/syn directory.

DESCRIPTION

This error message indicates that your installation of the Synopsys tools has been corrupted. You need to reread "libraries/syn/gtech.db" from your Synopsys release tape.

WHAT NEXT

HDL-236 (warning) Non-constant case-item used in casex or casez.
HDL Compiler assumes the expression is never 'x' or 'z' %s

DESCRIPTION

This warning is not serious unless the expression used in the case-item may take the value 'x' or 'z'. HDL Compiler builds the logic of a casex or casez assuming the case-item expression will yield ones and zeros. Under simulation, when some bits of the expression are 'x' or 'z', they are ignored. This can generate a simulation/ synthesis mismatch in the following example:

```
module e(a, z);
input a;
output z;
reg z;
wire ctl;
assign ctl = a ? 1'b0 : 1'bx;

always @(ctl) begin
casex(1'b1)
ctl:   z = 1'b1;
default: z = 1'b0;
endcase
end
endmodule
```

Under simulation, when 'a' is false, 'ctl' is assigned 'x', and the first branch of the casex always fires making 'z' one.

Under synthesis, the 1'bx is treated as a dont-care, and ?: operation optimizes away leaving 'ctl' always equal to zero ('b' is left unconnected). Since 'ctl' never matches the case expression, the second branch always fires, making 'z' zero.

WHAT NEXT

If you know that the expression in the case-item is never 'x' or 'z', then you may ignore this warning.

You can eliminate the warning by omitting expressions from the case-items of casex and casez statements. If you need an expression as a case-item, use a regular case statement.

EXAMPLE MESSAGE

The code fragment above receives the following message:

Warning: Non-constant case-item used in casex or casez. HDL Compiler assumes the expression is never 'x' or 'z' in routine e line 10 in file 'b.v' (HDL-236)

HDL-240 (error) Pragma map_to_entity is not supported for procedures with INOUT ports.
Port '%s' is defined as an INOUT port '%s'.

DESCRIPTION

Pragma **map_to_entity** is not supported for procedures with IN/OUT ports. When a port is used as input and output at the same clock cycle, a combinational loop results.

Usually, in a circuit with an IN/OUT port, a control (switch) logic determines the

port’s direction in each clock cycle. The use of IN/OUT ports implies multiple-cycle behavior of a procedure, and Synopsys does not support procedures with multiple-cycle behavior.

WHAT NEXT

Change the IN/OUT port to one IN port and one OUT port.

HDL-241 (error) Unable to resolve GTECH reference.

DESCRIPTION

This error message is issued following a LINK error message.

WHAT NEXT

See the LINK error message.

HDL-250 (error) Can not synthesize logic for assignment of UNKNOWN to identifier %s
%s.

DESCRIPTION

There is no hardware device to produce an UNKNOWN signal. The UNKNOWN value is for simulation purpose only.

WHAT NEXT

Use ’-- pragma translate off’ and ’-- pragma translate on’ to direct the VHDL Compiler to skip this assignment.

HDL-260 (warning) The parameter ’%s’ is not a valid integer. Treated as uninitialized when using the get_attribute command.

DESCRIPTION

All parameters must be integers for instantiation. This parameter is treated as uninitialized when using the *get_attribute* command.

WHAT NEXT

Change the parameter to an integer within 32 bits.

HDL-270 (error) An unsupported expression is assigned to constant '%s'
%s.

DESCRIPTION

Synopsys does not synthesize logic for HDL description in a constant declaration. All constants must be computable during HDL compilation. Therefore, the computation in constant declarations is restricted to operations of *integer* type. Moreover, arithmetic operations on integer constants greater than 32 bits is not supported.

WHAT NEXT

Cast constants to *integer* type if you need to perform an arithmetic operation in constant declaration. Otherwise, move the computation outside of constant declaration. For example, you can change the constant to a variable and perform the arithmetic operations on the variable. Note that computations on variables always produce logic.

HDL-272 (warning) Selector for MUX is always logic one - %s

DESCRIPTION

When one selector of a MUX is always one, the selected input is always being transferred to the output. Hence this input could override all other inputs. Such a situation could occur in Verilog if a *casex* statement is used and one of the conditions is *x* in all the bits. This is useful as a default condition, but should not be used along with Synopsys parallel-case directive.

WHAT NEXT

Designers should check their HDL descriptions to confirm their intention to have one selector of a MUX always be logic one. If such is not the intention, the designer should modify the HDL description.

HDL-281 (warning) Signal %s
has the asynchronous set/reset attribute attached but not used

for set/reset in design '%s'.

DESCRIPTION

Check the condition used in branch constructs (for example, "if then else" case). If a branch has an asynchronous set/reset assignment, each variable appearing in the branch's conditional expression must have the asynchronous set/reset attribute. In nested branch constructs, the condition for the *else* branch includes negation for the *if* branch.

WHAT NEXT

HDL-282 (warning) Signal %s has the synchronous set/reset attribute attached but not used for set/reset in design '%s'.

DESCRIPTION

Check the condition used in branch constructs (for example, "if then else" case) inside a clocked process. If a branch has a synchronous set/reset assignment, each variable appearing in the branch's conditional expression must have the synchronous set/reset attribute. In nested branch constructs, the condition for the *else* branch includes negation for the *if* branch.

WHAT NEXT

HDL-283 (warning) Signal '%s' has the asynchronous set/reset attribute attached in process %s but not used for set/reset in that process.

DESCRIPTION

Check the condition used in branch constructs (for example, "if then else" case) inside a process. If a branch has an asynchronous set/reset assignment, each variable appearing in the branch's conditional expression must have the asynchronous set/reset attribute. In nested branch constructs, the condition for the *else* branch includes negation for the *if* branch.

WHAT NEXT

HDL-284 (warning) Signal '%s' has the synchronous set/reset attribute
attached in process %s but not used for set/reset in that process.

DESCRIPTION

Check the condition used in branch constructs (for example, "if then else" case) inside the process. If a branch has a synchronous set/reset assignment, each variable appearing in its conditional expression must have the synchronous set/reset attribute. In nested branch constructs, the condition for the *else* branch includes the negation of that for the *if* branch.

WHAT NEXT

HDL-285 (error) Cannot find matching slave process '%s' for master process %s.

DESCRIPTION

Both master and slave processes must have labels. A master process must be attributed with the label of the slave process. Similarly, a slave process must be attributed with the label of the master process.

WHAT NEXT

Check the labels of master and slave processes, and make sure they match.

HDL-287 (warning) State output of master latch '%s' does not connect
directly to input of salve latch '%s'.

Fail to infer master-slave latch.

DESCRIPTION

A pair of latches defined as a master-slave latch cannot be paired because the data input of the slave latch does not connect directly to the output of the master latch.

WHAT NEXT

HDL-288 (warning) Master latch ’%s’ and slave latch ’%s’ have independent asynchronous-clear controls. Fail to infer master-slave latch.

DESCRIPTION

A pair of latches defined as a master-slave latch cannot be paired because their asynchronous set/reset conditions are not the same.

WHAT NEXT

HDL-289 (warning) Master latch ’%s’ and slave latch ’%s’ have independent asynchronous-set controls. Fail to infer master-slave latch.

DESCRIPTION

A pair of latches defined as a master-slave latch cannot be paired because their asynchronous set conditions are not the same.

WHAT NEXT

HDL-290 (warning) Master latch ’%s’ and slave latch ’%s’ have independent asynchronous-clear/set controls.

Fail to infer master-slave latch.

DESCRIPTION

A pair of latches defined as a master-slave latch cannot be paired because their asynchronous set/reset conditions are not the same.

WHAT NEXT

HDL-291 (warning) State output of master flip-flop '%s' does not connect
directly to input of slave flip-flop '%s'.
Or the input of slave flip-flop is driven by multiple sources including
the state output of master flip-flop.
Fail to infer master-slave flip-flop.

DESCRIPTION

WHAT NEXT

HDL-292 (warning) Master flip-flop '%s' and slave flip-flop '%s' have independent asynchronous-clear controls.
Fail to infer master-slave flip-flop.

DESCRIPTION

A pair of flip-flops defined as a master-slave flip-flop cannot be paired because their asynchronous reset conditions are not the same.

WHAT NEXT

HDL-293 (warning) Master flip-flop '%s' and slave flip-flop '%s' have independent asynchronous-set controls.

Fail to infer master-slave flip-flop.

DESCRIPTION

A pair of flip-flops defined as a master-slave flip-flop cannot be paired because their asynchronous set conditions are not the same.

WHAT NEXT

HDL-294 (warning) Master flip-flop '%s' and slave flip-flop '%s' have independent asynchronous-load controls. Fail to infer master-slave flip-flop.

DESCRIPTION

A pair of flip-flops defined as a master-slave flip-flop cannot be paired because their asynchronous data load conditions are not the same.

WHAT NEXT

HDL-295 (warning) Master flip-flop '%s' and slave flip-flop '%s' have different asynchronous data. Fail to infer master-slave flip-flop.

DESCRIPTION

A pair of flip-flops defined as a master-slave flip-flop cannot be paired because they are loaded with different asynchronous data.

WHAT NEXT

HDL-296 (warning) Master flip-flop '%s' and slave flip-flop '%s' have independent asynchronous-clear/set controls.

Fail to infer master-slave flip-flop.

DESCRIPTION

A pair of flip-flops defined as a master-slave flip-flop cannot be paired because their asynchronous set/reset conditions are not the same.

WHAT NEXT

HDL-297 (warning) Slave flip-flop ’%s’ has synchronous-clear control,
cannot be merged with master flip-flop ’%s’.
Fail to infer master-slave flip-flop.

DESCRIPTION

The only synchronous data loaded on the slave flip-flop must be the state output of the master flip-flop.

WHAT NEXT

HDL-298 (warning) Slave flip-flop ’%s’ has synchronous-set control,
cannot be merged with master flip-flop ’%s’.
Fail to infer master-slave flip-flop.

DESCRIPTION

The only synchronous data loaded on the slave flip-flop must be the state output of the master flip-flop.

WHAT NEXT

HDL-299 (warning) Slave flip-flop ’%s’ has synchronous-toggle control,

cannot be merged with master flip-flop ’%s’.
Fail to infer master-slave flip-flop.

DESCRIPTION

The only synchronous data loaded on the slave flip-flop must be the state output of the master flip-flop.

WHAT NEXT

HDL-300 (warning) State output of master cell ’%s’ drives nets in addition to the input of slave cell ’%s’.
Fail to infer master-slave latch/flip-flop.

DESCRIPTION

Cannot tap off the internal state of a master-slave latch/flip-flop.

WHAT NEXT

HDL-301 (warning) Master latch ’%s’ cannot be merged with slave flip-flop ’%s’.
Fail to infer master-slave latch/flip-flop.

DESCRIPTION

The pair of latches defined as a master-slave latch is not really a master-slave latch.

WHAT NEXT

HDL-302 (warning) Master flip-flop ’%s’ cannot be merged with slave latch ’%s’.

Fail to infer master-slave latch/flip-flop.

DESCRIPTION

The pair of flip-flops defined as a master-slave flip-flop is not really a master-slave flip-flop.

WHAT NEXT

HDL-303 (warning) Master cell ’%s’ cannot find its matching slave cell.

Fail to infer master-slave latch/flip-flop.

DESCRIPTION

A latch (flop-flop) inferred in a master process does not directly drive any latch (flop-flop) in the matching slave process to form a master-slave latch (flip_flop).

WHAT NEXT

HDL-304 (warning) Slave cell ’%s’ cannot find its matching master cell.

Fail to infer master-slave latch/flip-flop.

DESCRIPTION

A latch (flop-flop) inferred in a slave process is not directly driven by any latch (flop-flop) in the matching master process to form a master-slave latch (flip-flop).

WHAT NEXT

HDL-305 (error) ’%s’ is not a port or variable/signal, cannot be used

for asynchronous set/reset control in process %s.

DESCRIPTION

The attributed asynchronous set/reset can be attached only to a port or a variable/signal.

WHAT NEXT

HDL-306 (error) ’%s’ is not a port or variable/signal, cannot be used
for synchronous set/reset control in process %s.

DESCRIPTION

The attributed synchronous set/reset can be attached only to a port or a variable/signal.

WHAT NEXT

HDL-307 (warning) Latch inferred in design ’%s’ read with ’hdlin_check_no_latch’.

DESCRIPTION

The variable *hdlin_check_no_latch* directs the **read** command to ensure no latch is inferred in the HDL file.

WHAT NEXT

HDL-308 (warning) One_hot/one_cold pragma containing ’%s’ and ’%s’
is used to optimize set/reset condition for cell ’%s’.
Make sure there is an assertion for this one_hot/one_cold

pragma.

DESCRIPTION

See VE-109 or VHDL-2252.

WHAT NEXT

HDL-309 (warning) Object '%s' appears in two one_hot directives.
The directive containing this object is ignored.

DESCRIPTION

You receive this message because, during **elaborate** or **read** command activity, the compiler has detected the same signal in the signal name list of two **one-hot** directives, which is invalid. A signal can appear only in the signal name list of one **one-hot** or one **one-cold** directive. Following is an example that illustrates this situation:

```
synopsys one_hot "s1, r1"    //signals s1 and s2 appear twice
synopsys one_hot "s2, r2"
synopsys one_hot "s1, s2"
```

WHAT NEXT

Correct the code so that no signal appears more than once in the signal name list of **one_hot** directives.

elaborate (2), **read** (2).

HDL-310 (warning) Object '%s' appears in two one_cold directives.
The directive containing this object is ignored.

DESCRIPTION

You receive this message because, during **elaborate** or **read** command activity, the compiler has detected the same signal in the signal name list of two **one-cold** directives, which is invalid. A signal can appear only in the signal name list of one **one-hot** or one **one-cold** directive. Following is an example that illustrates this

situation:

```
synopsys one_cold "s1, r1"    //signals s1 and s2 appear twice
synopsys one_cold "s2, r2"
synopsys one_cold "s1, s2"
```

WHAT NEXT

Correct the code so that no signal appears more than once in the signal name lists of **one_cold** directives.

elaborate (2), **read** (2).

HDL-311 (warning) Object '%s' appears in a one_hot directive and a one_cold directive.

The directive containing this object is ignored.

DESCRIPTION

You receive this message because, during **elaborate** or **read** command activity, the compiler has detected the same signal in the signal name list of a **one_hot** directive and a **one_cold** directive, which is invalid. A signal can appear only in the signal name list of one **one_hot** or one **one_cold** directive. Following is an example that illustrates this invalid situation:

```
synopsys one_hot "s1, r1"     //signals s1 and r1 appear twice
synopsys one_cold "s2, r2"
synopsys one_cold "s1, r1"
```

WHAT NEXT

When your code contains **one_hot** and **one_cold** directives, be sure that no signal appears more then once in the signal name list of both directives.

SEE ALSO

elaborate (2), **read** (2).

HDL-312 (warning) The design being compiled contains %d operations.

Because of the large search space, resource sharing may take a long time to complete. You might consider turning

resource
sharing and resource implementation to area only.

DESCRIPTION

Because of the nature of the resource sharing problem, the search space grows quickly as the number of operations increase. When running in timing driven resource sharing mode, this results in a large number of calls to the timing verifier. As a result, this can cause very long run times.

WHAT NEXT

If you turn resource allocation and resource implementation to area only, the performance should increase significantly. This can be done either with the hlo_resource_allocation and hlo_resource_implementation variables, or it can be done with the set_resource_allocation and set_resource_implementation commands on a design by design basis (maybe included in an embedded script for the designs that you wish to run in area based mode).

HDL-320 (warning) Mismatch between simulation and synthesis may occur because of
three-state value %s used %s.

DESCRIPTION

An HDL description similar to the following example may cause a mismatch between RTL simulation and a gate-level simulation of the netlist resuling from synthesis. Discrepancy for the value of 'W' may occur if in simulation cycle *t-1* 'c1' is Logic1, and in simulation cycle *t* both 'c1' and 'c2' are Logic0.

```
if (c1)
  Q = high-impedance;
else if (c2)
  Q = d;

W = Q;
```

The HDL description in the next example may cause a mismatch between RTL simulation and gate-level simulation of the netlist resulitgng from synthesis. Discrepancy for the value of 'W' may occur if in simulation cycle *t-1* both 'c1' and 'c3' are Logic1, and in simulation cycle *t* both 'c1' and 'c3' are Logic0.

```
if (c1)
  Q = high-impedance;
```

```
    else if (c2)
      Q = d1;
    else
      Q = d2;

    if (c3)
      X = Q;

    W = X;
```

WHAT NEXT

Separate the statement into two processes. One process assigns the three-state value and the other process reads the three-state value.

process 1

```
   begin
     if (c1)
       Q = high-impedance;
     else if (c2)
       Q = d;
   end
```

process 2

```
   begin
     W = Q;
   end
```

HDL-321 (error) Assignment to loop index '%s' is beyond synthesis policy
%s.

DESCRIPTION

An HDL description similar to the following example is beyond synthesis policy.

```
  for (i = 0; i<loop_max; i = i + 1)
    begin
```

```
      ...
      i = loop_max; // exit the loop
      ...
    end
```

WHAT NEXT

```
Use "disable" statement to exit a loop.

begin : my_loop
  for (i = 0; i<loop_max; i = i + 1)
    begin
      ...
      disable my_loop; // exit the loop
      ...
    end
end
```

HDL-322 (error) Bad bus_naming_style variable ’%s’ used.

DESCRIPTION

```
The bus_naming_style variable variable has been incorrectly defined. It should be of
the type "%s_%d".
```

WHAT NEXT

```
Define the variable to be something like "%s_%d", or dont define it all and the
default will be used.
```

HDL-325 (error) Constant propagation on constant larger than 32 bits is not supported %s.

DESCRIPTION

```
Synopsys does not support constant propagation on a constant larger than 32 bits.
This error occurs when a constant needs to be expanded to a value greater than 32
bits.

In the following example, constant ’h100 needs to be expanded to 64 bits
```

```
wire [63:0] sum;

assign sum = 127 + 'h100;
```

WHAT NEXT

Use a temporary variable within 32 bits range, such as in the following example:

```
wire [31:0] temp;
wire [63:0] sum;

assign temp = 127 + 'h100;
assign sum = temp;
```

HDL-326 (error) Enumeration type defined in a generate statement is not supported %s.

DESCRIPTION

Synopsys does not support enumeration type definition in a VHDL generate statement.

In the following example, the type definition of *STATE_TYPE* is not supported.

```
architecture a of e is
begin
   G: for copy in 0 to 1 generate
      P : process
         type STATE_TYPE is (S1, S2);
         variable state : STATE_TYPE;
      begin
        if (c = '1') then
           state := S1;
        else
           state := S2;
        end if;
      end process P;
   end generate G;
end a;
```

WHAT NEXT

Move the type definition from the generate statement to the architecture declaration

region, as in the following example:

```
architecture a of e is
type STATE_TYPE is (S1, S2);  -- new location
begin
   G: for copy in 0 to 1 generate
      P : process
         variable state : STATE_TYPE;
      begin
        if (c = '1') then
           state := S1;
        else
           state := S2;
        end if;
      end process P;
   end generate G;
end a;
```

HDL-327 (error) Connection to instance port %s is too wide %s.

DESCRIPTION

In the following example, the signal *temp_out* connected to the port Y is too wide when represented in hardware.

```
architecture A of E is
component C1
   port (A : integer range 0 to 15;
         Y : integer range 0 to 15);
end component;
signal temp_in : integer range 0 to 15;
signal temp_out : integer range 0 to 31;
begin
U1: C1 port map (A => temp_in, Y => temp_out);
end A;
```

WHAT NEXT

Define a temporary signal/variable with the proper bit width.

```
architecture A of E is
component C1
   port (A : integer range 0 to 15;
         Y : integer range 0 to 15);
end component;
signal temp_in : integer range 0 to 15;
signal temp_out : integer range 0 to 31;
```

```
signal temp : integer range 0 to 15;
begin
temp_out <= temp;
U1: C1 port map (A => temp_in, Y => temp);
end A;
```

HDL-328 (error) Connection to instance port %s is too narrow %s.

DESCRIPTION

In the following example, the signal *temp_out* connected to the port Y is too narrow when represented in hardware.

```
architecture A of E is
component C1
   port (A : integer range 0 to 15;
         Y : integer range 0 to 31);
end component;
signal temp_in : integer range 0 to 15;
signal temp_out : integer range 0 to 15;
begin
U1: C1 port map (A => temp_in, Y => temp_out);
end A;
```

WHAT NEXT

Define a temporary signal/variable with the proper bit width.

```
architecture A of E is
component C1
   port (A : integer range 0 to 15;
         Y : integer range 0 to 31);
end component;
signal temp_in : integer range 0 to 15;
signal temp_out : integer range 0 to 15;
signal temp : integer range 0 to 31;
begin
temp_out <= temp;
U1: C1 port map (A => temp_in, Y => temp);
end A;
```

HDL-330 (error) Port name '%s' mismatches names of synthetic operator %s.

DESCRIPTION

The formal parameter names of the subprogram do not match those of the synthetic operator defined by the **map_to_operator** pragma.

WHAT NEXT

When using **map_to_operator**, make sure the formal parameter names of the subprogram matches those of the synthetic operator defined by the **map_to_operator** pragma. The match is also case-sensitive.

To check the port names of a synthetic operator, use the **report_synlib** command.

For example:

```
dc_shell> read standard.sldb
dc_shell> report_synlib standard.sldb


****************************************
Report : library
Library: standard.sldb
Version: v3.1a
Date   : Wed Jun 29 06:50:37 2001
****************************************

Library Type            : Synthetic
Tool Created            : v3.1a
Date Created            : Dec. 16, 1776
Library Version         : 3.1

Operators:

   Operator         Ports    Dir
   ------------------------------------------------------------------------
   ADD_TC_CI_OP     A        in
                    B        in
                    CI       in
                    Z        out

   ADD_TC_OP        A        in
                    B        in
                    Z        out
 . . .
```

HDL-350 (error) %s

in parsing parameter value: %s
for parameter ’%s’

DESCRIPTION

The parameter value is not acceptable in this particular context. The usual cause is a syntax error, value of incorrect type, or value out of bounds.

You may also find that the value being parsed is either shorter of longer than you expect. Perhaps the value reported above was intended to represent two values. In this case, make sure that you separate your parameter values by commas, and make sure that your parentheses and quotes match.

WHAT NEXT

Check the expected parameter type and syntax carefully.

HDL-351 (error) Specified value: %s for parameter ’%s’ has improperly sized array elements

DESCRIPTION

A value was specified for an unconstrained array, but the value is not legal because the number of bits is not a multiple of the array element size.

WHAT NEXT

You must specify a number of bits that is a multiple of the array element size.

HDL-352 (error) Specified value: %s for parameter ’%s’ is not the correct size

DESCRIPTION

The value specified is not legal because it is too large or too small for the parameter’s type.

WHAT NEXT

You must specify a number of bits that exactly fits the type.

HDL-353 (error) Can’t find type information for type ’%s’.

DESCRIPTION

This message indicates that the type is not in VHDL standard package.

WHAT NEXT

You can change the types of the generic parameters to use types in the VHDL standard package.

HDL-354 (error) Can’t find directory ’%s’.

DESCRIPTION

The directory cannot be accessed. It either does not exist or is protected.

WHAT NEXT

Check the value of the dc_shell variable that sets the path to the directory.

HDL-360 (warning) The variable hdlin_files is not supported for releases later than v3.3b.

DESCRIPTION

This warning occurs when the hdlin_files variable is used. This variable is supported for v3.3a and v3.3b but not for subsequent releases. Please refer to the WHAT NEXT section below for the solution.

WHAT NEXT

The variable **hdlin_files** specifies a list of file pathnames to be used by the **read -format vhdl** or **read -format verilog** commands. The files specified in **hdlin_files** are read before files specified in the **read command**. This variable is normally used to list VHDL source files that contain packages used by the **current_design**.

Instead of using **hdlin_files**, use the **analyze** command to analyze any packages currently specified in **hdlin_files**. The **analyze** command is a better solution for the following reasons:

1. You can analyze packages to different design libraries via the **-w** option of **analyze**.

2. When **analyze** is used, packages are not analyzed multiple times, thereby saving time. Any VHDL packages listed in **hdlin_files** are input each time a design is read that uses the package.

HDL-361 (warning) The variable hdlin_source_to_gates_mode is obsolete with v3.3a.

DESCRIPTION

This warning occurs when the **hdlin_source_to_gates_mode** variable is used. This variable is obsolete with v3.3a.

WHAT NEXT

Remove this variable from your script to disable this warning message.

HDL-362 (error) Can’t find design for cell ’%s’ on line %d in ’%s’.

DESCRIPTION

The design symbol corresponding to the cell’s reference can not be found in the symbol table. This may happen if you are using pragmas or synopsys directives, ie. translate_on/off or synthesis_on/off.

WHAT NEXT

Check the pragmas or synopsys directives for typos.

HDL-370 (warning) You are using the full_case directive with a case statement in which not all cases are covered.

DESCRIPTION

HDL Compiler assumes that all the conditions which are not covered cannot occur in practice. This means that these conditions are treated as don’t cares, which may result in mismatches between synthesis and simulation. Following is an example that will result in this mismatch:

```
module test (a, b, c, d);

input a, c, d;
```

```
output   b;
reg    b;

always @( a or d or c)
begin
  case (a)
    1'b0: b = d;
  endcase
  case (a) // synopsys full_case
    1'b1: b = c;
  endcase
end

endmodule
```

The second case statement is indicated as a full case, but the case when a = 1'b0 is not covered. This means that this condition can never occur, so HDL Compiler treats it as a don't care condition. As a result, the first case statement becomes redundant and is optimized out.

The compiler assumes that all the conditions which are not covered cannot occur in practice. This means that these conditions are treated as don't cares which may affect the logic generated by other statements.

WHAT NEXT

Specify all the possible branches in the case statement, if you want to avoid a simulation mismatch.

HDL-371 (warning) You are using the parallel_case directive with a case statement in which some case-items may overlap.

DESCRIPTION

There is more than one case-item that evaluates to true in the case statement with the **parallel_case** directive. This may lead to logic which is not the same as the simulated description. The use of the parallel_case directive under these circumstances is discouraged. Following is an example of this:

```
module test (c[1:0],y);
input [1:0] c;
output y;
reg y;

always@(c)
begin
  case {c[1:0]} //synopsys parallel_case
    2'b1x: y = 0;
    2'bx1: y = 1;
  endcase
```

```
end

endmodule
```

For this case statement, if c = 2'b11, y = 0 in simulation, but in synthesis both case-items are executed, so y = 1. For the condition c = 2'b11, HDL Compiler assumes the output is a don't care.

WHAT NEXT

Rewrite the conditons of this case statement in such a way that the different branches do not overlap any more, or don't use the **parallel_case** directive.

HDL-380 (warning) No MUX_OP inferred for the case %s because it might lose the benefit of resource sharing.

DESCRIPTION

The variable **hdlin_dont_infer_mux_for_resource_sharing** is set to true causing this MUX_OP not to be inferred. This MUX_OP is connected to two or more synthetic operators, which can not be shared by a MUX_OP. (They might be sharable otherwise.)

WHAT NEXT

Set **hdlin_dont_infer_mux_for_resource_sharing** to false, or re-write the case statement as to not share synthetic operators.

HDL-381 (warning) A MUX_OP has been inferred for the case %s which may possibly lose the benefit of resource sharing.

DESCRIPTION

The variable **hdlin_dont_infer_mux_for_resource_sharing** is set to false and a MUX_OP was inferred for a case statement that has two or more synthetic operators.

WHAT NEXT

Set **hdlin_dont_infer_mux_for_resource_sharing** to true, or don't infer a MUX_OP for this case statement.

HDL-382 (warning) A MUX_OP has been inferred for the case

%s which has either a default clause or an incomplete mapping.

DESCRIPTION

A MUX_OP has been inferred for a case statement that has an incomplete specification. Because MUX_OP's are hierarchical (the logic is in a separate level of hierarchy), this may result in a nonoptimal design.

The following five "case" statement coding styles result in this message:

1. Default branch A default branch refers to an "others" statement in a VHDL "case" statement or a "default" statement in a Verilog "case" statement. When a default branch covers more than one possible value, the inputs to the inferred MUX_OP are duplicated for the branches that are not covered in the "case" statement. The logic could be more optimal if a MUX_OP was not inferred. Following are examples of "case" statements that contain default branches covering more than one possible value:

```
Verilog
-------
  case (SEL)
    2'b00: DOUT = DIN[0];
    2'b01: DOUT = DIN[1];
    default: DOUT = DIN[2]; // covers 2'b10 and 2'b11 branches
  endcase

VHDL
----
  case SEL is
    when "00" => DOUT <= DIN(0);
    when "01" => DOUT <= DIN(1);
    when others => DOUT <= DIN(2); -- covers "10" and "11" branches
  end case;
```

2. Missing case branches Missing branches in a "case" statement in Verilog (all "case" statements need to be completely specified in VHDL) result in duplicate inputs to the inferred MUX_OP since all branches of the "case" statement are enumerated. If a MUX_OP is not inferred, the logic can be optimized. This is also true if the "case" statement uses the Synopsys "full_case" directive. Following is an example:

```
Verilog
-------
  case (SEL)                    case (SEL) //synopsys full_case
    2'b00: DOUT <= DIN[0];  2'b00: DOUT <= DIN[0];
    2'b01: DOUT <= DIN[1];         OR  2'b01: DOUT <= DIN[1];
    2'b10: DOUT <= DIN[2];  2'b10: DOUT <= DIN[2];
  endcase                       endcase
```

3. Missing assignments Similar to missing "case" branches, missing assignments in a "case" statement branch result in duplicate inputs to the inferred MUX_OP. If a MUX_OP is not inferred, the logic can be optimized. Following are examples of "case" statements with missing assignments that result in the HDL-382 message. These

examples infer two MUX_OPs, one for the output DOUT and one for DOUT2. Notice, an assignment to DOUT is missing in one of the branches, which results in the HDL-382 message.

Verilog
```
  case (SEL)
    2'b00: begin
            DOUT = DIN[0];
            DOUT2 = DIN[0];
           end
    2'b01: begin
            DOUT = DIN[1];
            DOUT2 = DIN[1];
           end
    2'b10: DOUT2 = DIN[2]; // Missing assignment to DOUT
    2'b11: begin
            DOUT = DIN[0];
            DOUT2 = DIN[0];
           end
  endcase
```

VHDL
```
  case SEL is
    when "00" => DOUT  <= DIN(0);
                 DOUT2 <= DIN(0);
    when "01" => DOUT  <= DIN(1);
                 DOUT2 <= DIN(1);
    when "10" => DOUT2 <= DIN(2); -- Missing assignment to DOUT
    when "11" => DOUT  <= DIN(0);
         DOUT2 <= DIN(0)
    when others => DOUT <= DIN(2);
                   DOUT2 <= DIN(2);
  end case;
```

4. Use of "dont_cares" The use of "dont_cares" ("x") in a "case" statement branch results in duplicate inputs to the inferred MUX_OP. If a MUX_OP is not inferred, the logic can be optimized. Following are examples of "case" statements that result in this message:

Verilog
```
  case (SEL)            case (SEL)
    2'b00: DOUT = DIN[0];  2'b00: DOUT = DIN[0];
    2'b0x: DOUT = DIN[1];      OR  2'b01: DOUT = DIN[1];
    2'b10: DOUT = DIN[2];  2'b10: DOUT = 1'bx;
    2'b11: DOUT = DIN[0];  2'b11: DOUT = DIN[0];
  endcase               endcase
```

VHDL
```
  case SEL is
    when "00" => DOUT <= DIN(0);
```

```
    when "0X" => DOUT <= DIN(1);
    when "10" => DOUT <= DIN(2);
    when "1X" => DOUT <= DIN(0);
    when others => DOUT <= DIN(2);
  end case;
```

5. Nested conditionals Nested conditionals refer to "if" statements inside "case" statements and "case" statements inside "case" statements ("case" statements inside "if" statements are not supported for MUX_OP inference). The inner "if" or "case" condition becomes one of the select lines to the MUX_OP, so data inputs to the MUX_OP are duplicated to size the MUX_OP according to the number of select lines. The logic could be more optimal if MUX_OPs were not inferred for nested conditionals. Following are examples of "if" statements nested in "case" statements:

Verilog

```
  case (SEL)
    2'b00: DOUT <= DIN[0];
    2'b01:
if (DIN[0])
  DOUT <= DIN[1];
else
  DOUT <= DIN[0];
    2'b10: DOUT <= DIN[2];
    2'b11: DOUT <= DIN[0];
  endcase
```

VHDL

```
  case SEL is
    when "00" => DOUT <= DIN(0);
    when "01" =>
if (DIN(0) = '1') then
          DOUT <= DIN(1);
else
          DOUT <= DIN(0);
        end if;
    when "10" => DOUT <= DIN(2);
    when "11" => DOUT <= DIN(0);
    when others => DOUT <= DIN(2);
  end case;
```

WHAT NEXT

Don't infer a MUX_OP for this "case" statement.

HDL-383 (warning) A MUX_OP was not inferred for the case %s because its branching factor of %d is greater than

hdlin_mux_size_limit.

DESCRIPTION

A attempt to infer a MUX_OP from a case statement with a branching factor larger than **hdlin_mux_size_limit** was attempted. This is usually the result of nested if or case statements with disjoint supports. It is best to not infer a MUX_OP in these situations, for then the optimizer will be able to effectivly optimize the assignments.

WHAT NEXT

Increase **hdlin_mux_size_limit**, rewrite the case statement to avoid the large branching factor, or do not infer a MUX_OP.

HDL-384 (warning) A MUX_OP for the case %s was not inferred because the variable hdlin_infer_mux was set to "none."

DESCRIPTION

A **hdlin_infer_mux** setting of "none" will override a local **infer_mux** attribute.

WHAT NEXT

Set **hdlin_infer_mux** to "all" or "default."

HDL-385 (warning) A MUX_OP for the case %s was inferred because the variable hdlin_infer_mux was set to "all."

DESCRIPTION

A **hdlin_infer_mux** setting of "al" will infer a MUX_OP for every possible case statement.

WHAT NEXT

Set **hdlin_infer_mux** to "none" or "default" and use the **infer_mux** directive when necessary.

HDL-386 (error) Number of enumeration encoding values does

not match the number of enumeration values.

DESCRIPTION

The number of enumeration encoding values defined via the ENUM_ENCODING attribute must match the number of enumeration values for the type.

WHAT NEXT

Modify the number of enumeration or enumeration attribute values.

HDL-387 (error) Can’t redefine reference named ’%s’ %s

DESCRIPTION

Certain invalid arguments (like a wire or function name) to pragma **map_to_module** can trigger this error message. The **map_to_module** pragma requires a module or component name as its argument. The following VHDL code demonstrates the problem:

```
function FUNC; //synopsys map_to_module FUNC //synopsys return_port_name DBUS input DBUS;

FUNC = DBUS; endfunction
```

WHAT NEXT

Supply a module name or component name to the appropriate **map_to_module** pragma.

HDL-388 (error) Can’t find declarative scope for component ’%s’

DESCRIPTION

It can happen if the use clause for the package in which the component is declared is surrounded by a synthesis off/on pair

WHAT NEXT

Either remove the synthesis off/on pair enclosing the use clause or do not instantiate the component

HDL-389 (warning) The following design name is very long:

’%s’

DESCRIPTION

This message is issued when a design name exceeds 64 characters. Long design names may be a problem for external downstream tools.

If the design contains parameters (generics), the design name is generated automatically based on the following variable settings:

- template_naming_style
- template_parameter_style
- template_separator_style

WHAT NEXT

If the design name was generated automatically, modify one or more of the variables listed above to reduce its length.

HDL-390 (warning) Statement not accelerated: Line %d, %s

DESCRIPTION

This statement contains HDL constructs that are outside of the "turbo" subset. The statement cannot be accelerated and may result in excessive run time to elaborate the containing module.

WHAT NEXT

Refer to the "turbo" subset document to determine what prevents the statement from being accelerated. Modify the HDL code to adhere to the "turbo" subset.

HDL-391 (error) Naming clash with %s

DESCRIPTION

This error occurs when a net has the same name as an other object in your design (net, instance, etc).

WHAT NEXT

Generally, the culprit is in the bus_naming_style. Choosing a poor bus_naming_style can cause this error: bus_naming_style=%s%d is problematic. Try the default bus_naming_style=%s_%d instead.

HDL-392 (error) Combinational loop found on a sequential element pin (net; %s).

DESCRIPTION

This error occurs when a net coming from (or getting to) a sequential element contains a loop.

WHAT NEXT

Typically, this error signals that some simulation statements remain in the HDL code. For example:

CLK <= not CLK after 10 ns; process(CLK) begin if CLK'event and CLK='1' then B <= A; end if; end process;

will create a loop on the CLK net. The simulation-only statements should be isolated with synthesis_on and off directives, like in:

-- synopsys synthesis_off CLK <= not CLK after 10 ns; -- synopsys synthesis_on

HDL-393 (warning) A MUX_OP was not inferred for the case %s because the ratio of MUX_OP data inputs to unique data inputs is %d, which exceeds the hdlin_mux_oversize_ratio.

DESCRIPTION

A MUX_OP was not inferred for a case statement that had too few unique assignments, as this may have negatively affected elaboration time and quality of results. This

situation arises when many assignments of a case statement are missing or identical. Discrete logic may be more desirable than a MUX_OP.

For a more detailed description of incompletely specified case statements, see HDL-382.

WHAT NEXT

Don’t infer a MUX_OP for this "case" statement.

HDL-394 (warning) Unconditional concurrent assignment to tristate value %s, may not result in hardware.

DESCRIPTION

The following example shows an unconditional concurrent assignment to tristate value in Verilog.

```
module e(m);
output m;
assign m = 1’bz;
endmodule
```

The following example shows an unconditional concurrent assignment to tristate value in VHDL.

```
library IEEE;
use IEEE.std_logic_1164.all;

entity E is
   port(m : out std_logic);
end E;

architecture A of E is
begin
  m <= ’Z’ ;
end A;
```

Since the output port ’m’ is always driven to tristate value, HDL Compiler will leave the port unconnected.

EXAMPLE MESSAGE

```
Warning: Unconditional concurrent assignment to tristate
        in routine e line 6 in file ’b.v’,
        may not result in hardware.   (HDL-394)
```

HDL-395 (warning) The statement %s, is never reached.

DESCRIPTION

HDL Compiler will automatically eliminate unreachable statements.

The following example shows an unreachable statement in Verilog. The statement: 'out1=in2' is never reached. This is because the first condition '(c1 | c2)' will always be true when the condition '(c1 & c2)' is true. Conversely, if '(c1 | c2)' is false, '(c1 & c2)' has to be false.

```
module foo(in1, in2, in3, c1, c2, out1);
input in1, in2, in3, c1, c2;
output out1;
reg out1;

always @(in1 or in2 or in3 or c1 or c2)
begin
if (c1 | c2)
out1=in1;
else if (c1 & c2)
out1=in2;
else
out1=in3;
end
endmodule
```

The following example shows an unreachable statement in VHDL. The statement: 'out1 <= in2' is never reached. This is because the first condition '(c1 or c2)' will always be true when the condition '(c1 and c2)' is true. Conversely, if '(c1 or c2)' is false, '(c1 and c2)' has to be false.

```
entity foo is
    port( in1, in2, in3  : in bit ;
          c1, c2    : in boolean ;
          out1    : out bit );
end foo;

architecture bar of foo is
begin
    process ( in1, in2, in3, c1, c2 )
    begin
      if (c1 or c2) then
out1 <= in1;
      else
if (c1 and c2) then
out1 <= in2;
else
out1 <= in3;
end if;
      end if;
    end process;
```

```
end bar;
```

EXAMPLE MESSAGE

```
Warning: The statement in routine e line 6 in file 'b.v',
        is never reached.   (HDL-395)
```

HDL-396 (warning) The flip-flop/latch %s, has asynchronous feedback.
this feedback will not be removed.

DESCRIPTION

HDL Compiler does not remove the feedbacks for latches or the asynchronous feedbacks for latches.

The following examples illustrate the cases mentioned above. The first has latch whose output is being fed back in its input

```
module foo(in1,c1, c2, out1);
input in1,c1, c2;
output out1;
reg out1;

always @(in1 or c1 or c2)
begin
if (c1)
out1=in1;
else if (c2)
out1=out1;    // This statement results in a feeback in the latch
end
endmodule
```

The second example shows a flip-flop which has an asynchronous feedback

```
module foo(in1,c1, clk, out1);
input in1,c1, clk;
output out1;
reg out1;

always @(posedge clk or posedge reset)
begin
if (reset)
out1=out1     // This statement results in a feeback in the latch;
else
out1=in1;
end
endmodule
```

HDL-397 (warning) A feedback loop found at buffer or inverter '%s'

DESCRIPTION

This error is issued when some buffers or inverters form a combinational feedback loop in boundary logic. For example, the following Verilog description is invalid because the CLK input of the flip-flop has a feedback loop.

```
CLK = ~CLK;
always@(posedge CLK)
begin
    Q = D;
end
```

WHAT NEXT

Check the HDL description and remove the combinational feedback loop.

HDL-398 (error) Loop index %s is not initialized %s

DESCRIPTION

A loop index is used under one set of conditions, but remains uninitialized when used under another set of conditions. This can happen when moving code from a for loop in one "if" branch into the "else" branch.

Once a variable is used as a loop iterator, it is handled as a "loop index" for the rest of its scope.

WHAT NEXT

The most likely cause is code moved outside a for loop. In this situation, the for loop probably needs to be duplicated in both places to properly initialize the loop index.

HDL-399 (warning) NUMERIC_STD.STD_MATCH: L'LENGTH /= R'LENGTH, returning FALSE "%s

DESCRIPTION

This message indicates that parameters to STD_MATCH have different lengths. Result will be FALSE.

WHAT NEXT

HDL-400 (warning) Clock signal is not in the sensitivity list. "%s

DESCRIPTION

This message indicates that clock signal is not in the sensitivity list which could cause a simulation and synthesis mismatch.

WHAT NEXT

HDL-401 (warning) The mode selected for resource implementation is use_fastest. The mode selected for resource allocation is either none or area_only. If timing constraints are not met, the fastest possible implementation will initially be selected for each resource. If you know that timing will be met with the smallest implementations it might save CPU time to set resource implementation to area_only.

DESCRIPTION

The current settings for resource allocation is not constraint-driven, while the resource implementation is set to use_fastest. If timing constraints are not met during the high level optimization phase, the selection of the largest implementation may cost additional CPU time.

WHAT NEXT

If you do not want the fastest implementation to be selected set resource implementation to area_only.

HDL-402 (error) No implementation is available for module %s.

DESCRIPTION

Each synthetic library module (e.g. DW01_add) needs at least one implementation (e.g. rpl) to be usable for synthesis. In this particular case no implementation is available for one module. Possible reasons for this are: dont_use statements have forbidden the use of all implementations that are in the synthetic library or the synthetic library itself is incomplete.

WHAT NEXT

Check dont_use statements in your dc_shell scripts or look at your synthetic library source code, if you are using your own synthetic library.

HDL-403 (error) You cannot use a "for" loop iterator that is more than 32 bits wide.

DESCRIPTION

You receive this message if the **read** or elaborate command detects a "for" loop iterator more than 32 bits wide; these are not currently supported.

WHAT NEXT

Redefine the "for" loop iterator to have a width of 32 bits or fewer, and re-execute the command.

SEE ALSO

elaborate (2), **read** (2).

HDL-404 (error) You cannot use a duplicate count of 0.

DESCRIPTION

You receive this message if the **read** or **elaborate** command detects a duplicate count of 0 (for example, {0{a}}). Duplicate counts of 0 are not supported.

WHAT NEXT

Remove the duplicate operator that has the 0 duplicate count, and re-execute the

command.

SEE ALSO

elaborate (2), **read** (2).

HDL-405 (warning) Local variable %s define %s is being read before it is fully assigned

DESCRIPTION

You receive this message if the **read** or **elaborate** command detects that a local variable may be read before it is assigned. The variable might be local to a sequential block or to a subroutine. An initial value of 0 is assigned to all the uninitialized local variables.

WHAT NEXT

Initialize the local variable.

SEE ALSO

elaborate (2), **read** (2).

HDL-406 (error) Potential overflow which may cause synthesis and simulation mismatch %s

DESCRIPTION

You receive this error message because the HDL Compiler detects a potential overflow in the exponent operator of the expression.

For example, an integer overflow occurs if temp is 0 in the expression 2 ** (31 - tmp).

WHAT NEXT

Remove the overflow exponent from the expression.

SEE ALSO

elaborate (2).

HDL-407 (warning) Potential overflow which may cause synthesis and simulation mismatch %s

DESCRIPTION

You receive this warning message because the HDL Compiler detects a potential overflow in the exponent operator of the expression.

For example, an integer overflow occurs if tmp is 0 in the expression 2 ** (31 - tmp).

WHAT NEXT

No action is required on your part. However, you can remove the overflow exponent from the expression.

SEE ALSO

elaborate (2).

HDL-410 (warning) The design being compiled contains %d operations. Because of the large search space, resource sharing may take a long time to complete. You might consider turning resource allocation to area only.

DESCRIPTION

Because of the nature of the resource sharing problem, the search space grows quickly as the number of operations increases. When running in timing driven resource allocation mode, this results in a large number of calls to the timing verifier. As a result, this can cause very long run times.

WHAT NEXT

If you turn resource allocation to area only, the performance should increase significantly. This can be done either with the hlo_resource_allocation variable, or it can be done with the set_resource_allocation command on a design by design basis (maybe included in an embedded script for the designs that you wish to run in area based mode).

HDL-411 (warning) The design being compiled contains %d operations. Because of the large search space, resource implementation may take a long time to complete. You might consider turning resource implementation to area only.

DESCRIPTION

Because of the nature of the resource implementation problem, the search space grows quickly as the number of operations increases. When running in timing driven resource implementation mode, this results in a large number of calls to the timing verifier. As a result, this can cause very long run times.

WHAT NEXT

If you turn resource implementation to area only, the performance should increase significantly. This can be done either with the hlo_resource_implementation variable, or it can be done with the set_resource_implementation command on a design by design basis (maybe included in an embedded script for the designs that you wish to run in area based mode).

HDL-412 (error) HDL Compiler does not support local register declarations.

DESCRIPTION

You receive this error message because the HDL Compiler does not support register declarations within sequential blocks.

The Presto HDL Compiler handles register declarations within sequential blocks.

Set **hdlin_enable_presto** to **true** to use the Presto HDL Compiler.

WHAT NEXT

Either use the Presto HDL Compiler, or recode your design to use module-scope registers instead of locally declared registers.

SEE ALSO

hdlin_enable_presto(3).

HDL-413 (information) HDL directives for resource sharing/ implementation are ignored.

DESCRIPTION

The support to do resouce sharing/implementation as per manual HDL directives is discontinued since the tool can make better choice with the knowledge of design context.

map_to_module, implementation and resource sharing directives specified using OPS attribute will be ignored.

Implementation specified for synthetic operators using set_implementation **is also ignored.**

WHAT NEXT

Contact your Synopsys support representative.

HDLA-1 (error) Design '%s' does not contain HDL analysis information.

DESCRIPTION

Either of the following cases may apply :

- Your top Verilog HDL or VHDL design was not input using *dc_shell* with **hdlin_enable_analysis_info** or **bc_enable_analysis_info** set to true.

- The *read* or *analyze* command encountered an error in your Verilog HDL or VHDL source file. HDL analysis information is not generated for subsequent designs.

- The program may have found the design in another design file that doesn't contain HDL analysis information. Check your **search_path** variable to ensure that the design loaded by the program is the one you expected.

WHAT NEXT

Fix your syntax errors and use *dc_shell* to *read*/*analyze* your HDL source files and regenerate the GTECH design.

HDLA-2 (error) Errors detected while linking '%s' to '%s'.

DESCRIPTION

The GTECH library, 'gtech.db', is not in the given search path.

WHAT NEXT

Ensure that the GTECH library, 'gtech.db', can be found in the search path.

HDLA-3 (warning) Errors detected while linking '%s' to '%s'.

DESCRIPTION

The program is unable to find a design in the given technology-mapped design file(s) or technology library that correspond to instantiations of that design in higher levels of the design hierarchy.

Information about the design or its instantiations in the technology-mapped design is unavailable.

WHAT NEXT

Ensure that the mapped design files or technology library specified are the same ones generated or used in linking the design. These files are specified using the project variables **gtech_db_files, mapped_db_files**, and **link_library**. The directories for these files are specified in the **search_path** variable.

To ensure that you have correctly linked the design, load the design into **dc_shell**, and execute the **link** command from the top level of the design.

HDLA-4 (warning) Port '%s' of GTECH design '%s' is not found in the mapped design.

DESCRIPTION

This message was generated because a port in the GTECH design does not have an equivalent in the mapped design.

This can happen if any of the following is true:

1. The GTECH and mapped design files contain different designs.
2. The bus naming style used in generating the GTECH design file differs from that used in generating the technology-mapped design file.
3. A **group** or **ungroup** command was performed on the designs in one design file and not the other.
4. A **change_names** command was executed on the designs in one design file and not the other.

WHAT NEXT

In general, ensure that any commands that can change the names or the hierarchical

structure of the design are performed on both design files in the same relative order.

For the previous situations in particular, try the following:

1. Check the design files to ensure that they describe the same designs.

2. Define the **bus_naming_style** variable to be similar to "%s_%d" or allow the default to be used. In either case, ensure that the same variable is used to generate both design files.

3. Perform the **group** or **ungroup** command on both design files in the same relative order.

4. Perform the **change_names** command on both design files in the same relative order.

HDLA-5 (error) Design '%s' is multiply defined.

DESCRIPTION

The design exists in more than one design file.

WHAT NEXT

Check the design files to ensure that a design only occurs once.

HDLA-6 (error) Can't find instance '%s' in design '%s'.

DESCRIPTION

An instance in the GTECH design could not be found in the technology mapped design.

WHAT NEXT

Use *dc_shell* to *read*/*analyze* the HDL source files and *compile* the top level design to generate a new technology mapped design.

HDLA-7 (error) Design '%s' contains repeated instances.

Please use the uniquify or set_dont_touch commands on them.

DESCRIPTION

This message indicates that repeated instances exist in your design. Your design must not contain repeated instances that are indistinguishable from each other.

When a design is used (instantiated) more than once in a design, you must use the **dc_shell** commands **uniquify** or **set_dont_touch** on the instances.

WHAT NEXT

Use one of the three following strategies to address this issue:

1) Load your design into *dc_shell*, link it, and issue the **uniquify** command on the top-level design.

2) Use the **set_dont_touch** command on all repeated instances (places where the same design is instantiated more than once).

3) Modify your design so that it contains no repeated instances.

For more information, refer to the **uniquify**, and **set_dont_touch** manual pages.

HDLA-8 (error) Can’t find design ’%s’.

DESCRIPTION

The design cannot be found in the GTECH design file(s).

WHAT NEXT

Ensure that design exists in the HDL source and that it is spelled correctly in the project file as the value of the **top_design_name** variable.

HDLA-9 (warning) The GTECH design %s does not have HDL analysis information.

DESCRIPTION

This message indicates that the **elaborate** command was used on .syn files that were created by **analyze** in either **dc_shell** or **design_analyzer** with either **hdlin_enable_analysis_info** or **bc_enable_analysis_info** set to false. To view **analyze** in either dc_shell or design_analyzer, but not in ha_shell. In HDL Advisor, to view

links between the GTECH design files and HDL source design files, the design must be both analyzed and elaborated in with these variables set to true.

WHAT NEXT

Set **hdlin_enable_analysis_info** or **bc_enable_analysis_info** to true and input the design using the **analyze** and **elaborate** or **read** commands.

If this message was issued from within *ra_shell*, it is due to either of the following:

- The design was previously analyzed outside *ra_shell*,
  eg. by *dc_shell* without the variables set.

  Analyze the HDL source file that contains the design
  using *ra_shell*.

- A list of files was issued to *ra_shell*'s *analyze*
  command and one or more of the files analyzed before
  the file containing the design had an error.
  for example, analyze -f vhdl { file1.vhdl file2.vhdl file3.vhdl }

  If file1.vhdl has an analyze error, the designs in
  file1.vhdl and the following files will not have
  links between the GTECH design and the
  HDL source files.

  Ensure that all HDL source files analyze without errors.

- The design is a Verilog module, specified in a
  Verilog HDL file that is included by another Verilog HDL file.
  Items specified inside a Verilog HDL 'include file
  cannot be traced. This is a current limitation of HDL analysis
  tools.

  Do not reference a Verilog module using 'include.
  Instead, include it in an analyzed file using the
  verilog_file_list variable or the analyze and
  elaborate command in ra_shell.

HDLA-10 (warning) Design '%s' does not contain HDL analysis

information.

DESCRIPTION

This design does not contain HDL analysis information, and may be one of these:

- a DesignWare part;
- a mapped design,
- a design that was not **read**/**analyze**d using **ra_shell** or **dc_shell**;
- a design that was **read** or **analyze**d after an error was encountered in your Verilog HDL or VHDL source file. (HDL analysis information is not generated for subsequent designs).
- a design that resides in another design file that doesn't contain HDL analysis information. Check your **search_path** variable to ensure that the design loaded by the HDL analysis tool is the one you expected.

WHAT NEXT

If the design is not a DesignWare part, use **ra_shell** or **dc_shell** to reanalyze your design; or check the project file and ensure that the GTECH design files are in the indicated directories.

HDLA-11 (error) Variable '%s' is not set.

DESCRIPTION

The variable specified in the error message has not been set in the project file (by default **.synopsys_analyzer.setup**.)

WHAT NEXT

If you are using the default project file (**.synopsys_analyzer.setup**), edit the project file so that the above variable is set.

If you are creating your own project file, set the variable in your project file and

specify the filename when invoking the tool using the **-f** command line option.

HDLA-12 (warning) Variable '%s' is not set.

DESCRIPTION

The variable specified in the error message has not been set in the project file (by default **.synopsys_analyzer.setup**.)

This variable is not required to bring up RTL Analyzer, but does affect the design files loaded.

WHAT NEXT

If you are using the default project file (**.synopsys_analyzer.setup**), edit the project file so that the above variable is set.

If you are creating your own project file, set the variable in your project file and specify the filename when invoking the tool using the **-f** command line option.

HDLA-13 (error) Can't find '%s' in path '%s'.

DESCRIPTION

The file cannot be found in the given path.

WHAT NEXT

Check that the file is correctly set and spelled in the project file and that the **search_path** variable is correctly set to find that file.

HDLA-14 (error) MainWin environment is not set up.

DESCRIPTION

MainWin files, which control the display of the windows, have not been set up or an incorrect version of MainWin has been set up.

WHAT NEXT

Check with your Synopsys administrator.

HDLA-15 (error) Undefined Synopsys root directory.

DESCRIPTION

The Synopsys root directory is undefined.

WHAT NEXT

Check with your Synopsys administrator.

HDLA-16 (error) '%s' is not a directory.

DESCRIPTION

You have specified an invalid directory; or, the directory or one or more of its parents are read or search protected.

WHAT NEXT

Check your project file to ensure that variables specifying directories are correctly set.

Change your permissions to enable reading and searching of the appropriate directory and all of its parents. For example,

chmod a+rx <dir_name>

HDLA-17 (error) Can't read '%s'.

DESCRIPTION

The file cannot be found, or is read protected.

WHAT NEXT

Check your project file to ensure that the file and path are correctly set, and that variables specifying directories are correctly set.

Change your permissions to enable reading of the appropriate file. For example,

chmod a+r <dir_name>

HDLA-18 (warning) Register or instantiated cell '%s' is missing in the mapped design %s.

DESCRIPTION

There are two possible reasons for the generation of this warning message.

• There might be a naming style mismatch between the GTECH and mapped domains;

• The mapped design might have been generated in **dc_shell** (for example, by executing **change_names**, **group**, or **ungroup**) without the corresponding GTECH design having been generated in **ra_shell**; or vice versa.

WHAT NEXT

Check your **ra_shell** and **dc_shell** scripts and edit them as necessary to correct one or both of the above errors, and try again.

HDLA-19 (warning) Pin '%s' does not exist on the instantiated mapped design %s.

DESCRIPTION

For a user-instantiated design, all pins are expected to exist on the mapped design. This message could be generated if there is a name mismatch between the ports of the user-instantiated design in the GTECH and the ports of the mapped design files.

There are two possible reasons for a name mismatch.

• There might be a naming style mismatch between the GTECH and mapped domains;

• The mapped design might have been generated in dc_shell (for example, by executing **change_names**, **group**, or **ungroup**) without the corresponding GTECH design having been generated in **ra_shell**; or in ha_shell, or vice versa.

WHAT NEXT

Check your **ra_shell** and **dc_shell** scripts and edit them as necessary Check your ha_shell and dc_shell scripts and edit them as necessary to correct one or both of the previous errors and try again.

HDLA-20 (warning) Pin '%s' does not exist on the instantiated library cell %s.

DESCRIPTION

The pin does not exist on a user instantiated library cell. This message could be generated if there is a name mismatch between the pins of the library cells in the GTECH and the mapped design files.

There are two possible reasons for a name mismatch.

- There might be a naming style mismatch between the GTECH and mapped domains;

- The mapped design might have been generated in **dc_shell** (for example, by executing **change_names**, **group**, or **ungroup**) without the corresponding GTECH design having been generated in **ra_shell**; or vice versa.

WHAT NEXT

Check your **ra_shell** and **dc_shell** scripts and edit them as necessary to correct one or both of the above errors, and try again.

HDLA-21 (error) Design '%s' appears multiple times in a hierarchy
or in more than one hierarchy.

DESCRIPTION

The same file was used when linking the GTECH and mapped designs.

WHAT NEXT

Use the original design file for linking GTECH and make a copy of the file for linking mapped designs. See also HDLA-7.

HDLA-22 (warning) Instantiated design '%s' of cell '%s' is

empty.

DESCRIPTION

This warning is generated when the design does not contain any nets, either because the design is empty, or because it is an instantiated library design.

WHAT NEXT

Check the value of the **search_path** variable and the setting of other RTL Analyzer variables to ensure that the correct design has been linked.

HDLA-23 (warning) %s is out of date with respect to %s.

DESCRIPTION

This message indicates that the dependencies between the two specified files are incorrect, probably because the files were not generated by the same **ra_shell** or **dc_shell** session.

WHAT NEXT

Regenerate both files using the same **ra_shell** or **dc_shell** session.

HDLA-24 (warning) Logic Inspector : %s

DESCRIPTION

A message that is specific to the Logic Inspector.

WHAT NEXT

HDLA-25 (information) Sorry: no link to help for that item.

DESCRIPTION

You invoked F1 help for an item, such as a menu item or toolbar button, but there is no link to help for that item.

WHAT NEXT

Try to find help for the item some other way. For example, if the item is a toolbar button or menu item, choose Menus and Toolbar Buttons from the window's help menu and look for the item.

HDLA-26 (information) The selected object can not be linked to the design. Try selecting an output port or assignment statement.

DESCRIPTION

This message is generated when New Logic is executed in the Logic Inspector window but RTL Analyzer unable to find an object in the GTECH design that corresponds to the currently selected object. This situation usually occurs when the selected object is a construct in the HDL source.

WHAT NEXT

Select a related port or assignment statement in the HDL source and re-execute the New Logic command.

HDLA-27 (information) The selected object is not driven by boolean logic. This may be because Logic Inspector does not search through hierarchy boundaries, registers or designWare parts. Try selecting an output port or assignment statement.

DESCRIPTION

Issued when New Logic is executed in the Logic Inspector window but the object in the GTECH design that corresponds to the currently selected object is not driven by boolean logic.

WHAT NEXT

Try selecting a related construct in the HDL source and run the New Logic command again. If the offending construct is a pin of a module/entity instance statement, use HDL Browser's Push In operation to go to the definition of the module or entity-architecture, select the corresponding port construct, and run the New Logic command again. You may have to push in multiple levels of hierarchy to get to a port that is driven by logic.

HDLA-28 (information) Unable to link back to the selected object. Try a lower reduction effort.

DESCRIPTION

Issued by the Logic Inspector when a reduction of the boolean logic leaves it in a state that cannot be displayed.

WHAT NEXT

This usually only happens at the High setting of Reduction Effort. Switch to a lower setting.

HDLA-29 (information) No Design Data

DESCRIPTION

This message is generated when there is no design data. The most common reasons for missing design data are these:

• You requested that the program display data from the mapped design, but only the GTECH design is loaded;

• You requested that the program display power data, but the design does not contain power data.

WHAT NEXT

If the problem is that no mapped design is loaded, do the following:

If you invoked this program from Design Compiler or Design Analyzer, ensure that the current design in that program is mapped, then re-invoke this program.

Otherwise, use Load Mapped Design in the File menu of HDL Browser to load the mapped design.

If the problem is that the design does not contain power data, do the following:

If you invoked this program from Design Compiler or Design Analyzer, use the report_power or report_rtl_power commands to ensure that the current design in that program contains power data, then re-invoke this program.

Otherwise, update your design to include power data, then use Load GTECH Design or Load Mapped Design in the File menu of HDL Browser to load the appropriate design.

HDLA-30 (error) Please enter a value to search for.

DESCRIPTION

Issued by HDL Browser's Find Text dialog when you push the Find Forward, Find Backward, or Find All button but haven't specified a string in the Find What field.

WHAT NEXT

Type a string into the field or click the button to the right of the field and pick a previously found string from the drop down list.

HDLA-31 (information) The string '%s' was not found.

DESCRIPTION

Issued after a Find Text operation in HDL Browser when the specified string was not found in the file being displayed.

WHAT NEXT

Try the search again after changing the string or disabling the Match Case check box.

HDLA-32 (error) The GTECH design doesn't cover all of the constructs in source, .bi, and .id files. Displayed results are probably wrong.

DESCRIPTION

This message is generated by HDL Browser when the data in the GTECH design does not account for all of the constructs in an HDL source file that was just loaded.

WHAT NEXT

Check that the HDL source file and the corresponding **.bi** and **.id** files have not been changed since the file(s) that contain the GTECH design were generated. If

necessary, regenerate the GTECH design files. Contact Synopsys if the problem persists after recreating the GTECH design files.

HDLA-33 (error) Source file out of sync with GTECH design! %s probably was changed since the GTECH design was generated.

DESCRIPTION

This message indicates that HDL Browser attempted to load an HDL source file or the corresponding **.bi** or **.id** file, but found that the file's checksum does not match the value stored in the GTECH design. This situation probably occured because the HDL source file was changed after the GTECH design was generated.

WHAT NEXT

You can continue to use this program, but HDL Browser cannot show this HDL source file. To be able to view this HDL source file, you must re-analyze and re-elaborate the GTECH design and then reload it into this program. If you invoked this program from Design Compiler or Design Analyzer, re-invoke this program after re-analyzing and re-elaborating the GTECH design. Otherwise, re-analyze and re-elaborate the GTECH design using the Build GTECH window or ra_shell, then use Load GTECH Design from the File menu of HDL Browser to reload the design.

HDLA-34 (error) Couldn't read HDL source file: %s

DESCRIPTION

This message indicates that HDL Browser was unable to find or read the requested HDL source file.

WHAT NEXT

Ensure that the file exists in one of the directories specified by the **search_path** variable and that the file is readable.

HDLA-35 (error) Couldn't read .bi file:

%s

DESCRIPTION

This message indicates that HDL Browser was unable to find or read the specified **.bi** file. (There is a .bi file that corresponds to each HDL source file.)

WHAT NEXT

Ensure that the file exists in one of the directories specified by the **search_path** variable and that the file is readable.

HDLA-36 (error) The data in .bi file: is not consistent with the text in HDL source file: The HDL source file may have been changed since the .bi file was created.

DESCRIPTION

This message indicates that the data in the specified HDL source file is inconsistent with the data in the corresponding **.bi** file.

WHAT NEXT

Determine whether the HDL design file has been changed since the **.bi** file was created, and re-create the **.bi** and GTECH design files if necessary. If the problem persists, contact Synopsys.

HDLA-37 (information) Stopped search after finding %d occurrence(s) of '%s'. Search again from a different starting location to find any additional occurrences.

DESCRIPTION

This message indicates that HDL Browser has stopped searching because it has reached the limit of number of occurrences that can be found in one operation. Limiting the number of occurrences per operation (currently 1000) allows a Find All operation to take place in a reasonable length of time.

WHAT NEXT

To find more occurrences, position the last found occurrence at the top of the window and then repeat the Find All operation.

HDLA-38 (information) Found %d occurrence(s) of '%s'.

DESCRIPTION

This message indicates the number of occurrences found by HDL Browser during a Find All operation.

WHAT NEXT

Click OK to dismiss the the dialog, then scroll or use Find Next and Find Previous to view all the found occurrences.

HDLA-39 (information) Unable to find a path to or through the selected point.

DESCRIPTION

This message indicates that a Worst GTECH or Worst Mapped command was issued but Path Browser was unable to find a path to or through the currently selected object.

WHAT NEXT

Select a different object and re-issue the command.

HDLA-40 (error) The selected object is not a design, cell, pin or port.

DESCRIPTION

This message indicates that you issued a command to display a new path or object, but the currently selected object is not a design, cell, pin, or port.

WHAT NEXT

Select an object that is a design, cell, pin, or port, and re-execute the command.

If you selected a construct in HDL Browser, use the flying box and Hot Cursor window to find a related construct that functions adequately.

HDLA-41 (error) No Path Displayed.

DESCRIPTION

This message indicates that you have issued the Worst Current Start/End Points GTECH command when Path Browser is not displaying a path. This command displays the worst GTECH path that has the same start and end points as the currently displayed path; therefore, you must display a path before issuing this command.

WHAT NEXT

Use an appropriate Path Browser command to display a path, and reissue the Worst Current Start/End Points command.

HDLA-42 (error) Unable to map the start and end points of the current path to equivalent objects in the GTECH design.

DESCRIPTION

This message indicates that you have issued the Worst Current Start/End Points GTECH command, but Path Browser is unable to find objects in the GTECH design that correspond to the start and end points of the currently displayed path. This situation can arise if the currently displayed path was traced interactively in the mapped design, so that the start or end point is a gate for which there is no exact equivalent in the GTECH design.

WHAT NEXT

Ensure that the start and end points of the current path are registers, ports of the overall design, or ports of hierarchy blocks that exist in both the GTECH and mapped versions of the design. Then reissue the Worst Current Start/End Points command.

HDLA-43 (information) db file not loaded.

DESCRIPTION

This message indicates that you directed the tool to display data from the mapped design, but only the GTECH design, and not the mapped design, is loaded.

WHAT NEXT

If you invoked RTL Analyzer from dc_shell (via the rtl_analyzer command), make sure that when you invoked RTL Analyzer, the current design was a mapped design (i.e. compiled).

If you executed RTL Analyzer directly, choose Edit Project Settings and specify the mapped design. Save the project then choose Load Mapped Design.

HDLA-44 (error) Not available in this mode.

DESCRIPTION

This message, issued by Profiler, indicates that you attempted to enable Follow Selected while Profiler was in Timing mode. Follow Selected is not supported in Timing mode.

WHAT NEXT

To see the worst path through or to an object, select the object in any window and then choose View->Show Selected (or push the Find Selected toolbar button) in Profiler.

HDLA-45 (error) Project variable %s not set.

DESCRIPTION

This message indicates that the project variable is not set that specifies the directory or directories containing the on-line help topic files. This variable is normally set in the system-level **.synopsys_analyzer.setup** file and is not changed by users.

WHAT NEXT

Ask your system administrator to check the tool installation. If the installation is correct, contact Synopsys.

HDLA-46 (error) Help error: %s

DESCRIPTION

This message indicates that a help topic is missing, unreadable, or contains an error. For example, the topic specified for a jump point could not be found.

Examples:

Help error: bad query command
Help error: Couldn’t load file: <filename>
Help error: Couldn’t find marker: <markername>

WHAT NEXT

Have your system administrator check the tool installation. Contact Synopsys if the installation is correct.

HDLA-47 (error) Could not open help context map file.

DESCRIPTION

This message indicates that the tool was unable to read the file that specifies the help topic to be displayed for each menu item and toolbar button using F1 help.

WHAT NEXT

Have your system adminstrator determine whether the file **cntxtmap.qdh** exists in the on-line help directory and is readable.

HDLA-48 (information) Mapped domain of design ’%s’ is not loaded.

DESCRIPTION

This message indicates that the mapped domain of the design was not loaded.

WHAT NEXT

If you invoked RTL Analyzer from dc_shell (via the rtl_analyzer command), make sure that when you invoked RTL Analyzer, the current design was a mapped design (i.e. compiled).

If you executed RTL Analyzer directly, choose Edit Project Settings and specify the mapped design. Save the project then choose Load Mapped Design.

HDLA-49 (warning) '%s' is not a directory.

DESCRIPTION

You have specified an invalid directory; or, the directory or one or more of its parents are read or search protected.

WHAT NEXT

Check your (**search_path** variable or a project file that you may have created) to ensure that variables specifying directories are correctly set.

Change your permissions to enable reading and searching of the appropriate directory and all of its parents. For example,

```
chmod a+rx <dir_name>
```

HDLA-50 (warning) Command line option '%s' is not unique. Possible completions are { %s }.

DESCRIPTION

A prefix of a command line option was used. However, two or more valid command line options share the same prefix.

WHAT NEXT

Use a larger substring of the appropriate command line option to insure that its prefix is unique.

HDLA-51 (warning) The '%s' command is not supported in ra_shell.

DESCRIPTION

This message indicates that the command you issued, while valid in **dc_shell**, is not supported in **ra_shell**, the RTL Analyzer shell user interface. For example, **compile** is supported only in **dc_shell**, and is ignored in **ra_shell**. The command is ignored.

WHAT NEXT

If you need to use the command, issue it from within **dc_shell** and not **ra_shell**.

HDLA-52 (information) Couldn’t find a path to or through the selected point.

DESCRIPTION

Issued by Profiler when a New Path command failed to find any path to or through the currently selected object.

WHAT NEXT

Select a different object and try the command again.

HDLA-53 (error) %s is not the name of a valid host.

DESCRIPTION

The given hostname is not the name of a valid host. This could be due to a typo in your project file.

WHAT NEXT

Edit the project file and ensure that the variable is set to a valid hostname.

HDLA-54 (error) Project variable ’%s’ is not one of the following valid values : %s.

DESCRIPTION

The value of the variable is not valid. This could be due to a typo in the project file.

WHAT NEXT

Edit the project file and ensure that the variable is set to one of the valid values.

HDLA-55 (error) Could not invoke %s on %s.

DESCRIPTION

The given program could not be invoked on the given host. This may be due to an incorrect hostname, incorrect executable name, or problems with the network.

WHAT NEXT

Ensure that the host exists, the host is alive, via the UNIX 'ping' command, and the executable exists for the architecture of the given host .

HDLA-56 (warning) Could not find or execute %s.

DESCRIPTION

The given program could not be found or is not executable.

WHAT NEXT

HDLA-57 (error) Load Design failed. See error messages.

DESCRIPTION

The Load Design operation failed.

WHAT NEXT

Check the error messages to find out why the load failed. Some common problems are: incorrect values specified in the Load Design dialog, missing files, and files unreadable due to permissions.

HDLA-58 (error) Estimator terminated due to a fatal error.

DESCRIPTION

The Estimator process terminated due to a fatal error.

WHAT NEXT

Report this to Synopsys.

HDLA-59 (error) Estimator terminated due to an error. No Estimator results are available.

DESCRIPTION

The Estimator process terminated due to an error.

WHAT NEXT

Check the messages in the Estimator window to find out why the Estimator run failed to produce an estimated design.

HDLA-60 (information) Reload not needed.

DESCRIPTION

The latest versions of the designs that you requested to be loaded (GTECH, Mapped, or both) are already loaded.

WHAT NEXT

HDLA-61 (error) Unable to load the Estimated design.

DESCRIPTION

One or more errors occurred while attempting to load the estimated design.

WHAT NEXT

Check error messages to see what failed. If you are able to correct the problem, you can use the Load Design dialog to attempt to load the estimated design.

HDLA-62 (information) Estimator not enabled.

To enable, ensure that an Estimator license is available and reinvoke RTL Analyzer with the -estimate command line option or with project variable enable_estimation set to TRUE.

DESCRIPTION

You tried to display the Estimator window, but the Estimator is not enabled for this RTL Analyzer run.

WHAT NEXT

To enable the Estimator, ensure that an Estimator license is available and reinvoke RTL Analyzer with the -estimate command line option or with project variable enable_estimation set to TRUE.

HDLA-63 (error) Could not change working directory to

DESCRIPTION

You tried to change the current working directory to the specified directory, but the program was unable to do so.

WHAT NEXT

Check that the specified path is valid and that all permissions are correct.

HDLA-64 (warning) %s is not a valid command line option.

DESCRIPTION

The given option is invalid.

WHAT NEXT

Check the User's Guide or invoke *-help* command line option to see a list of valid command line options.

HDLA-65 (warning) Design %s is empty. It will be treated as an

unresolved reference during link.

DESCRIPTION

The program uniquifies a design after loading it in. If any design in the hierarchy is empty, then this design is not uniquified, leading to multiple instantiation of this design. To get around this problem the program treats empty designs as black boxes, which are unresolved references during link.

WHAT NEXT

The user should confirm that the design being warned about is really intended to be empty. If so, then there is no problem and the later LINK-5 warning about any unresolved references to this design can also be ignored.

HDLA-66 (warning) %s was removed in version %s.

DESCRIPTION

The given variable or command was removed in the aforementioned version.

WHAT NEXT

Check the Reference Manual for alternate commands.

HDLA-67 (warning) %s will be removed in version %s.

DESCRIPTION

The given variable or command will be removed in the aforementioned version.

WHAT NEXT

Check the Reference Manual for alternate commands.

HDLA-68 (warning) %s was made obsolete in version %s.

Please use %s.

DESCRIPTION

The given variable or command was removed in the aforementioned version. Please use the given alternate variable or command.

WHAT NEXT

Check the Reference Manual for alternate commands.

HDLA-69 (warning) %s will be obsolete in version %s. Please use %s.

DESCRIPTION

The given variable or command will be removed in the aforementioned version. Please use the given alternate variable or command.

WHAT NEXT

Check the Reference Manual for alternate commands.

HDLA-70 (error) Build GTECH terminated due to a fatal error.

DESCRIPTION

The Build GTECH process terminated due to a fatal error.

WHAT NEXT

Report this to Synopsys.

HDLA-71 (error) Build GTECH terminated due to an error. No Build GTECH results are available.

DESCRIPTION

The Build GTECH process terminated due to an error.

WHAT NEXT

Check the messages in the Build GTECH window to find out why the Build GTECH run failed to produce a gtech design.

HDLA-72 (error) Unable to load the built GTECH design.

DESCRIPTION

One or more errors occurred while attempting to load the GTECH design.

WHAT NEXT

Check error messages to see what failed. If you are able to correct the problem, you can use the Load Design dialog to attempt to load the built gtech design.

HDLA-73 (warning) Directory '%s' is not writable.

DESCRIPTION

You do not have write permission to the given directory.

WHAT NEXT

Use the UNIX 'chmod' command to add write permission or specify a different directory.

HDLA-74 (error) The current path is not in the mapped design.

DESCRIPTION

This message indicates that you issued the Worst Current Start/End Points GTECH command when the Path Browser is not displaying a path in the mapped design. This command is used to display the worst path in the GTECH design that corresponds to a path in the mapped design. Therefore, Path Browser must be displaying a path in the mapped design when this command is executed.

WHAT NEXT

Use an appropriate Path Browser command to display a path in the mapped, then reissue the Worst Current Start/End Points GTECH command.

HDLA-75 (error) Unable to correlate the path in the mapped design to a corresponding path in the GTECH design.

DESCRIPTION

This message occurs when you issue the Worst Current Start/End Points GTECH command, but Path Browser is unable to correlate the currently displayed path in the mapped design to a corresponding path in the GTECH design. This situation can arise if the currently displayed path was traced interactively in the mapped design, so that the start or end point is a gate for which there is no exact equivalent in the GTECH design.

WHAT NEXT

Ensure that the start and end points of the current path are registers, ports of the overall design, or ports of hierarchy blocks that exist in both the GTECH and mapped versions of the design. Then reissue the Worst Current Start/End Points command.

HDLA-76 (warning) %s is not a valid RTL Analyzer or BCView variable.

DESCRIPTION

A variable was set in an RTL Analyzer or BCView project file which is not a valid variable name for the tool.

WHAT NEXT

Check the spelling of the variable.

HDLA-77 (warning) %s are incompatable variables. Choosing '%s'.

DESCRIPTION

A set of incompatable RTL Analyzer or BCView variables have been set. The tool has chosen a compatable subset of them.

WHAT NEXT

Delete one or more of the variables to make a compatable set of RTL Analyzer or

BCView variables.

HDLA-78 (error) Design '%s' contains multiple instances. Please use the 'set_dont_touch' or 'uniquify' dc_shell commands to resolve this problem.

DESCRIPTION

The given design contains multiple instances of a subdesign. To resolve this problem, either uniquify the design, which will make each instance a separate subdesign; or use the 'set_dont_touch' command to put a synopsys dont_touch attribute on the appropriate subdesign(s).

WHAT NEXT

To dont_touch the design, place the appropriate 'set_dont_touch' command(s) in a dc_shell-compatable script file and specify the name of this file as the value of the 'constraints_include_file' RTL Analyzer variable and restart Build Gtech, or if you invoked RTL Analyzer from dc_shell, include the 'set_dont_touch' command in dc_shell and re-run the 'rtl_analyzer' dc_shell command.

To uniquify the design, place the 'uniquify' command in a dc_shell-compatable script file and specify the name of this file as the value of the 'constraints_include_file' RTL Analyzer variable and restart Build Gtech, or if you invoked RTL Analyzer from dc_shell, include the 'uniquify' command in dc_shell and re-run the dc_shell 'rtl_analyzer' command.

HDLA-79 (warning) No combinational loop found in circuit.

DESCRIPTION

This message is issued when you select "Combinational Loop" on the Data menu in the Path Browser and there are no combinational loops in the circuit.

WHAT NEXT

Nothing. This is good news!

HDLA-80 (warning) Combinational loop found in circuit. Use "Data->Combinational Loop" in Path Browser to display the

loop.

DESCRIPTION

You have combinational loops in your gtech circuit.

WHAT NEXT

Go to the Path Browser. Select "Combinational Loop" under the Data menu. The GTECH path comprising the loop will be shown in the path browser. Select elements in the path and look in HDL Browser to identify constructs in your RTL code that causes the path.

HDLA-81 (warning) Could not change directory to '%s'

DESCRIPTION

The program could not change directory to the specified directory. This directory might not exist.

WHAT NEXT

Ensure that the directory exists.

HDLA-82 (warning) The command '%s" has been unaliased.

DESCRIPTION

The name of an user specified alias clashed with a shell command. The alias was automatically unaliased.

WHAT NEXT

Remove this alias from the .synopsys_dc.setup file and any of the script files or use another name for the alias.

HDLA-83 (error) Files '%s' and '%s' have the same basename.

DESCRIPTION

Having 2 HDL files with the same basename confuses this tool because it only uses the basename to identify an HDL file to allow moving files between directories.

WHAT NEXT

Ensure that no 2 HDL files in the project file have the same basename. On UNIX you can do this without renaming files by using links.

HDLA-84 (warning) Rebuild design '%s' to obtain enhanced HDL tracing information. This design was built by Synopsys release '%s'.

DESCRIPTION

In the v1997.08 release, the following tracing capabilites have been added:

- Tracing of elements inside VHDL Entity/Architecture pairs that reside in different files.

- Tracing elements inside subprogram calls (such as VHDL functions and procedures or Verilog functions and Tasks).

- Tracing iteration-specific elements within the scope of finite loops (such as VHDL and Verilog for loops).

- Tracing elements inside a VHDL package or VHDL package_body.

- Improvements in tracing elements inside conditional statements (such as VHDL condition signal assignments, VHDL if statements, VHDL case statements, Verilog if statements, Verilog case statements and Verilog ?: constructs).

This message was generated because the design does not contain enhanced tracing information. This design was built using a previous release of RTL Analyzer. This might be due to one of the following reasons.

- the design was not generated by the current Synopsys release of

RTL Analyzer or **ra_shell**,

- the hdl source files were analyzed by a previous Synopsys release of **ra_shell**,

- when elaborating an hierarchical design containing an instance of design 'foo', the file 'foo.ra' was loaded instead of regenerating design 'foo'. The design file, 'foo.ra', was not generated by the current Synopsys release.

WHAT NEXT

Use the Current Synopsys release of **Build GTECH** window in RTL Analyzer or **ra_shell** to regenerate your design. If you are running RTL Analyzer from within **dc_shell**, then be sure to set the variable hdlin_enable_analysis_info = true in **dc_shell** before reading in your design.

SEE ALSO

hdlin_enable_analysis_info(3)

HDLA-85 (error) Dependency loop involving files '%s' and '%s' and the definition of '%s' detected.

DESCRIPTION

There are files in the list specified in the variables 'vhdl_file_list' or 'verilog_file_list', which use definitions from each other. This creates a dependency loop.

WHAT NEXT

Check your source files and eliminate the dependency loop.

HDLA-86 (error) Parsing of '%s' failed with the following message: '%s'.

DESCRIPTION

There is a syntax error in the reported file.

WHAT NEXT

If the parser reports a macro usage without prior definition, the problem can be fixed by defining a macro in each file where it is used. This creates some warning messages during analyze, but these can be ignored. RTL Analyzer build can currently not handle macros used in a file and defined in another file.

HDLA-87 (error) Dependency loop involving the design '%s' detected.

DESCRIPTION

The mentioned module instantiates other modules, which in turn instantiate again this module. Thus, a loop is created, which does not allow to process the design.

WHAT NEXT

Check your source files and eliminate the dependency loop.

HDLA-88 (warning) The design files define two differnt modules ('%s' and '%s') with the same name but only different spelling.

DESCRIPTION

If the design consists of Verilog and VHDL files, this can lead to problems, since the decision of which module to use for an instantiation might depend on the order of analysis.

WHAT NEXT

Check your source files and give the modules a unique name.

HDLA-89 (warning) Calculation of HDL tracing information has been disabled.

DESCRIPTION

Due to errors in the HDL source files, further calculation of HDL tracing information has been disabled. The resulting designs will not have the necessary information to allow other Synopsys Analysis tools to trace elements of those

designs to the HDL source. This will affect you if :

• You are analyzing multiple HDL files. Designs in the files analyzed after this message appears will not contain HDL information.

• You have multiple designs in one file. Designs that are analyzed after this message appears will not contain HDL information.

WHAT NEXT

Fix your syntax errors and use *dc_shell* to *read*/*analyze* your HDL source files and regenerate the GTECH design. Ensure that you have set hdlin_enable_analysis_info=true for RTL designs or bc_enable_analysis_info=true for behavioral designs.

SEE ALSO

hdlin_enable_analysis_info(3) bc_enable_analysis_info(3)

HDLA-90 (warning) The design %s does not have tracing information linking it to its HDL source. It might have not been processed with bc_enable_analysis_info set to true.

DESCRIPTION

This message indicates that

1)the **elaborate** command was used
on .syn files that were created by the **analyze** command without the variable **bc_enable_analysis_info** set to **true**,
or
2)the **bc_check_design/schedule** command was used
on .db files that were created by the **elaborate** command without the variable **bc_enable_analysis_info** set to **true**.

In Synopsys HDL analysis tools, in order to view links between designs and their HDL source files, the designs must be processed with the variable **bc_enable_analysis_info** set to **true**.

WHAT NEXT

From within dc_shell set the variable **bc_enable_analysis_info** to **true** while processing designs to be analyzed in Synopsys HDL analysis tools.

SEE ALSO

bc_enable_analysis_info(3).

HDLA-91 (information) You invoked this tool from Design Compiler or Design Analyzer. Please re-analyze and re-elaborate your design there and then reload it using the items in the File menu of HDL Browser.

DESCRIPTION

This tool was invoked through a command in Design Compiler or Design Analyzer. The Build GTECH window invokes ra_shell which will result in a Synopsys db file that is protected. This file cannot be read into Design Compiler or Design Analyzer. Hence, we have disabled the Build GTECH Design from HDL Source window.

WHAT NEXT

Re-analyze and re-elaborate your design in Design Compiler or Design Analyzer and use the Load items in the File menu of the HDL Browser to reload your design.

HDLA-92 (information) bc_view launched successfully with process-id %s. Please refer to the log
in the xterm window titled 'bc_view' for further details.

DESCRIPTION

WHAT NEXT

SEE ALSO

bc_view(2)

HDLA-93 (information) Reload done successfully in the existing bc_view with process-id %s.
Please refer to the log in the xterm window titled 'bc_view' for further details.

DESCRIPTION

WHAT NEXT

SEE ALSO

bc_view(2)

HDLA-94 (warning) The design '%s' is not in a stage that bc_view can analyze.

DESCRIPTION

This warning tells you that the design in question cannot be analyzed with the **bc_view** command because the dc_shell variable **bc_enable_analysis_info** was not set as *true* when you ran **analyze** or **elaborate** on the design. Thus, there is no tracing information in the design and it cannot be analyzed with **bc_view**.

WHAT NEXT

Set **bc_enable_analysis_info** as *true* and again perform **analyze**, **elaborate -s**, and **schedule** or **bc_check_design**, depending on the stage the design was in when you tried to run **bc_view**.

SEE ALSO

bc_view (2), **schedule** (2), **bc_check_design** (2); **analyze** (3), **elaborate** (3).

HDLA-95 (error) No license to analyze SystemC designs can be obtained.

DESCRIPTION

You receive this message because the **bc_view** command was unable to obtain an SC-Schedule license at the current time. You must have a valid SC-Schedule license to analyze SystemC designs with the **bc_view** command.

WHAT NEXT

Wait until an SC-Schedule feature becomes available and attempt to load your design again.

SEE ALSO

bc_view (2).

HDLA-96 (error) No license to analyze HDL designs can be obtained.

DESCRIPTION

You receive this message because the **bc_view** command was unable to obtain a BC-Schedule license at the current time. You must have a valid BC-Schedule license to analyze HDL designs with the **bc_view** command.

WHAT NEXT

Wait until a BC-Schedule feature becomes available and attempt to load your design again.

SEE ALSO

bc_view (2).

HDLA-97 (fatal) Your license file does not contain any of the features needed to run this application.

DESCRIPTION

You receive this message because your license file does not contain the features required to run BCView. The required features depend on the language of your design source code. For VHDL or Verilog, you must have the BC-Schedule feature. For SystemC, you must have the SC-Schedule feature.

WHAT NEXT

Upgrade your licenses, and try running BCView again.

HDLA-100 (error) The command bc_view is no longer supported.

Please use the report_schedule command instead.

DESCRIPTION

The **report_schedule** command should be used to analyze the results after scheduling, instead of **bc_view** which is no longer supported.

WHAT NEXT

Do a man **report_schedule** to see the analysis capabilites of the command.

SEE ALSO

HDLOUT-1 (warning) Expect to see the member name but found %s.

DESCRIPTION

When hdlout_internal_busses is set to TRUE, it will parse the bus member names to form a range of a bus. This process only happen after doing compile while all the data are bit-blasted.

This warning tells that the name might contain range or some form that causes parsing failure.

WHAT NEXT

HFS-059 (Error) HFS failed for driver %s

DESCRIPTION

The 'create_buffer_tree' command was not able to produce a valid buffer tree for one of the subtrees of the specified driver. This usually happens when some sink pins are so isolated that no clustering can be made without violating the design rules even using low fanouts, or there is no enough space to place a buffer.

WHAT NEXT

Try to use a different buffer with higher drive strength ("set_cbt_options -references").

HFS-064 (Warning) HFS could not detect any bufferable fanout driven by pin %s.

DESCRIPTION

The reported pin does not have any fanout in the current netlist.

WHAT NEXT

HFS-122 (Warning) Pin %s/%s is inside a hierarchicall cell %s marked dont_touch.

DESCRIPTION

You receive this message because a high fanout tree in your design traces to the reported pin, which is found within a subdesign protected by the dont_touch attribute. High Fanout Synthesis ignores this sub-tree, because a dont_touch subdesign cannot be modified.

WHAT NEXT

Remove the **dont_touch** attribute from the subdesign represented by the specified hierarchical cell as follows.

1. Execute the **report_cell** command for the hierarchical cell specified by this message. This provides you with the name of the corresponding subdesign.

2. Use the **current_design** command to set this subdesign to be the *current_design*.

3. Remove the **dont_touch** attribute from the *current_design*.

4. Set the *current_design* back to the one you work on.

5. Uniquify the design.

SEE ALSO

current_design (2), **report_cell** (2).

HFS-196 (Error) Insufficient free sites to place buffer.

DESCRIPTION

No empty space (site not covered by a placement blockage, a block or a fixed cell) was found for buffer inserted during HFS, so synthesis of the high fanout net was not completed for this reason.

WHAT NEXT

Please check placement obstructions and placement regions.

HFS-701 (Information) Buffering net %s.

DESCRIPTION

WHAT NEXT

HFS-702 (Warning) Skipping net %s marked dont_touch.

DESCRIPTION

WHAT NEXT

HFS-703 (Information) Skipping net %s - inside SILM.

DESCRIPTION

WHAT NEXT

HFS-710 (Error) The design’s max_fanout value is not valid (%2.0f). Ignoring it.

DESCRIPTION

WHAT NEXT

HFS-720 (Information) Buffer tree break point: %s ’%s’ %s

DESCRIPTION

There are several reasons that a buffer tree will be broken into a set of trees during the high-fanout synthesis in **create_buffer_tree** and **place_opt**. Here are the reasons and suggestions for removing the break points:

The buffer/inverter cell has the **dont_touch** attribute.

The buffer/inverter cell has the **size_only** attribute.

The hierarchical pin has a clock attribute.

The hierarchical pin has a timing constraint attribute.

The hierarchical pin is on a Voltage Area interface.

The hierarchical pin is on an operating condition interface.

The hierarchical pin is on an ILM interface.

The pin or its net is in a **dont_touch** module.

The hierarchical pin drives a dont_touch net.

The hierarchical pin is **dont_touch** on both nets.

The pin is on a hier cell list of -preserve_boundary.

The hierarchical pin is entering the top and variable compile_no_new_cells_at_top_level = true.

The hierarchical pin is exiting on the top and variable compile_no_new_cells_at_top_level = true.

WHAT NEXT

If the **dont_touch**, **size_only**, clock attributes or timing constraint are not needed, then remove them and re-run.

The Voltage Area and ILM break points cannot be removed.

For pins on operating condition interface, please make sure that all needed Voltage Areas are defined for the different operating conditions set on the design.

HFS-721 (Information) Connection class conflict: keep buffer tree with driver '%s' (%s) and load pin '%s' (%s)

DESCRIPTION

This message indicates that Automatic High-Fanout Synthesis (AHFS) during **place_opt** or **create_buffer_tree** is keeping the buffer tree driven by the named pin because the buffer tree has a load pin with a conflicting connection class.

WHAT NEXT

HFS-722 (Warning) %s %s

DESCRIPTION

This message indicates that a driver pin or net is being skipped in **remove_buffer_tree** for one of these reasons:

"Skipping net that does not have exactly one driver: " Multi-driver nets do not have their buffer trees removed.

"Skipping net that has no driver: " The net has no driver.

"Skipping driver with no net connection: " The driving pin in the object_list does not have any net attached.

"Skipping driver whose net does not have exactly one driver: " Multi-driver nets do not have their buffer trees removed.

"Skipping pin that is not a driver: " The pin in the object_list is not an output or inout pin.

WHAT NEXT

HFS-800 (Information) Total number of removal drivers is %d.

DESCRIPTION

This message indicates that Automatic High-Fanout Synthesis (AHFS) during **place_opt** or **create_buffer_tree** is removing the specified number of old buffer trees.

WHAT NEXT

HFS-801 (Information) Total number of insertion drivers is %d.

DESCRIPTION

This message indicates that Automatic High-Fanout Synthesis (AHFS) during **place_opt** or **create_buffer_tree** is inserting the specified number of new buffer trees.

WHAT NEXT

HFS-802 (Information) Automatic high-fanout synthesis deletes %d cells.

DESCRIPTION

This message indicates that Automatic High-Fanout Synthesis (AHFS) during **place_opt** or **create_buffer_tree** has deleted the specified number of buffer or inverter cell instances.

WHAT NEXT

HFS-803 (Error) Setting option %s is not allowed for the current value of option -optimize_buffer_trees.

DESCRIPTION

The current value of option -optimize_buffer_trees determines which other options are relevant and which are not allowed to be set.

When -optimize_buffer_trees is TRUE, these options are not allowed: -hf_threshold -mf_threshold -remove_effort

When -optimize_buffer_trees is FALSE, these options are not allowed: -skip_for_hfs

WHAT NEXT

First set the value of -optimize_buffer_trees and then set the other allowed options.

It is not recommended to switch the value of -optimize_buffer_trees in a single script. If the user does switch the value of -optimize_buffer_trees in a single script, then the non-relevant options values will be ignored during AHFS.

HFS-804 (Warning) Ignoring buffer or inverter in -skip_for_hfs

list '%s' (%s)",

DESCRIPTION

The -skip_for_hfs option does not allow buffers or inverters (without dont_touch and size_only) to be listed.

Buffers and inverters (without dont_touch and size_only) may be driven (indirectly) from other drivers.

If that happens then the entire buffer tree is going to be re-built and the skip has no effect. That is why CCC disallows "skip" on regular buffers.

When using -skip_for_hfs, the user should think of skipping entire trees, not parts of trees.

WHAT NEXT

HFS-805 (Error) There are no driver pins or ports in the -from <object_set>.

DESCRIPTION

The -from option on **remove_buffer_tree** is expecting a set of ports, pins, or nets with at least one driver pin or input port.

Note that power and ground nets are not supported unless this option has been already set: **set_ahfs_options** -constant_nets true.

Nets with multiple drivers are not allowed.

Look for HFS-722 warnings in the log.

WHAT NEXT

Make sure that the collection passed to the -from option contains a driver pin or port, or that the nets have driver pins.

HFS-808 (Warning) Connection class conflicts exist in the buffer tree driven by '%s'

"
 ,

DESCRIPTION

Some pins in the buffer tree are connected with connection class conflicts. Pins should not be connected to each other if they do not share any classes in common. The "universal" class can be connected to any other pin.

You can use **set_ahfs_options -default_reference <buffer_type_list>** to limit the buffer (or inverter) types used during **create_buffer_tree**.

If you want to avoid connection class conflicts, you may need to remove the buffer tree and rebuild it using buffers whose pin classes are compatible with the driver and loads of the high-fanout net.

WHAT NEXT

Make sure that the connection_class attributes on the lib_pin objects are correct. Use **report_constraints -connection_class -all_violators** for details of all nets with connection class violations.

Use **report_buffer_tree -break_points -from <driver_pin>** to see details of the connection class conflicts.

HLS-1 (error)The invokation '%s' of function '%s' constrains the function input '%s' to be smaller than its default. This is not currently supported when elaborating for scheduling.

DESCRIPTION

If the actual constrains passed in is smaller then default then this error occurs. For example : function [7:0] A; input [7:0] IN; ... endfunction function [20:0] B ; reg [5:0] TEMP; ... A(TEMP); <---- error here ... endfunction

WHAT NEXT

Changed the constrains to be the same as the default.

HLS-2 (error) The task '%s' on line %d contains an inout parameter. This is not currently supported when the task is being preserved using the preserve_function pseudo-comment.

DESCRIPTION

Tasks with inout parameters cannot be preserved using the preserve_function compiler directive.

WHAT NEXT

Either do not preserve the task, by removing the preserve_function compiler directive, or rewrite the task to not use inout parameters.

HLS-3 (error) The call to preserved procedure '%s' on line %d, contains a complicated expression specified

for parameter ’%s’.

DESCRIPTION

```
The call to a procedure contains a complicated expression
 (this includes sliced busses).
 This is not currently supported when the procedure
 is being preserved using the preserve_function pragma
 and when the parameter is an out or inout parameter.
```

WHAT NEXT

```
Either do not preserve the procedure, by removing its
 preserve_function pragma, or do not use complex expressions
 as parameters, when calling it.
```

HLS-4 (error) Could not link call to function ’%s’ at line %d.

DESCRIPTION

```
Could not find a design to implement the called function. This can happen for a
number of reasons. For example, the types of the parameters in the call to the
function do not match the types of the parameters in the function declaration. Or,
for example, the function name may be misspelled.
```

WHAT NEXT

```
Verify that the function is being called with the correct parameter types.
```

HLS-5 (error) No suitable process for HLS

DESCRIPTION

```
The current design has no process that can be processed by HLS
```

WHAT NEXT

```
Set the current design or add a process that is suitable for HLS
```

HLS-6 (error) '%s' is not a valid %s. Valid options are %s

DESCRIPTION

The flag you used is not among the acceptable options.

WHAT NEXT

Choose one of the valid options.

HLS-7 (error) Negative HLS timing constraint

DESCRIPTION

The specified delay parameter on the set_cycle family of commands is negative. This is an invalid input.

WHAT NEXT

Specify a positive value for the delay.

HLS-8 (error) Unrecognized HLS datapath topology identifier

DESCRIPTION

The topology identifier you have used is not in the currently supported set.

WHAT NEXT

The topology tags we support are documented in the HLS manual. You may have to quote the tag you use, if it contains special (nonalphanumeric) characters.

HLS-9 (error) No schedule data available

DESCRIPTION

For some reason there is no scheduling information available in the current design.

WHAT NEXT

The current design has no scheduling data present. This will usually happen because the design has not been scheduled, or scheduling failed for some reason.

HLS-10 (error) No scheduled process

DESCRIPTION

There is no scheduled process in the current design.

WHAT NEXT

The current design has no scheduled process. This situation happens because the design contains no suitable process, the process has not been scheduled, or scheduling failed for some reason.

HLS-11 (error) Timing constraint across hierarchy

DESCRIPTION

The timing constraint refers to two or more objects that are at different levels of hierarchy, or that have different ancestries.

WHAT NEXT

You cannot constrain the objects directly. Instead, you can constrain the outermost object to the boundary of the hierarchical element that contains the innermost object; then constrain the innermost with regard to the boundary. Note that as the number of hierarchical levels crossed by the desired constraint increases, the number of these new constraints also increases.

HLS-12 (error) Timing constraint across loop(s)

DESCRIPTION

The timing constraint refers to two or more objects that are on different sides of a loop.

WHAT NEXT

You cannot constrain the objects directly. Instead, you can constrain the first with

regard to the beginning of the loop, and the second with regard to the end of the loop; and then constrain the loop. Note, however, that a constraint from beginning to end of a loop governs the number of cycles in one pass of the loop. Think about the number of passes that may be made and what that implies for your overall constraint.

HLS-13 (Warning) The loop at line %d in file '%s' is not needed, so it was deleted.

DESCRIPTION

Because none of the signals driven in the loop fanned out to the outputs, the loop was unnecessary and was removed.

WHAT NEXT

Check the loop for errors. If there are no errors, the loop is not needed and can be removed.

HLS-14 (error) non-block common schedule

DESCRIPTION

The objects designated are not the proper type to share a schedule.

WHAT NEXT

Only function and procedure calls can have their schedules shared. In the worst case, you can rewrite your input HDL so that otherwise identical functions have different names.

HLS-15 (error) Chained unrelated ops

DESCRIPTION

The objects designated are not in the same execution sequence.

WHAT NEXT

You cannot chain two operations that are in different branches of a conditional. Check the operation names that you are using. In particular, pay close attention to

the hierarchical decomposition of your design (loops, for example, are separate levels of hierarchy) and its effect on naming.

HLS-16 (error) inconsistent clock net ID

DESCRIPTION

The object designated as the clock net in the *clock* declaration does not match the clock net you used in the HDL.

WHAT NEXT

Create the proper net as the clock. Check for the name being a bit different due to hierarchical naming effects. Use **find net** to see what the names really are.

HLS-17 (error) No clock exists

DESCRIPTION

The HLS process could not find the clock signal.

WHAT NEXT

Use **create_clock** to create a known clock signal. The clock signal should agree with the clock you used in *wait* statements in the HDL text (if you used *wait* statements).

HLS-18 (warning) no reset net

DESCRIPTION

There is no designated reset net.

WHAT NEXT

There is no reset net for this design. This condition means that the design may power on in some unknown state, and never be properly initialized.

HLS-19 (error) non-unique path between locked operations

DESCRIPTION

The objects designated as being locked together do not have a unique timing relationship to one another.

WHAT NEXT

This situation occurs when there is a conditional branch in the execution path from one operation to the next. You cannot lock the objects, but you can constrain them. Use **set_max_cycles** and **set_min_cycles** to define an acceptable envelope. If you need a rigid timing relationship, you must rewrite the HDL to eliminate the conditional or move it away from the locked operations.

HLS-20 (error) Indeterminate path length

DESCRIPTION

The objects designated do not have a statistically determined time interval between them, so the constraint is not enforceable.

WHAT NEXT

Break down the constraint so that the part of the path that isn’t determinate (for example, a loop) has a separate constraint that tells how many cycles the loop can take for one iteration. The constraint can then be enforced.

HLS-21 (error) Lock across lexical scopes

DESCRIPTION

The objects designated are at different levels of the design hierarchy, or they are in different subtrees.

WHAT NEXT

You cannot lock these with respect to one another. You can, however, lock them with respect to the boundaries of the hierarchical subtrees they are contained within and then lock the subtrees with respect to one another.

HLS-22 (error) Lock with nonunique path source

DESCRIPTION

The set of objects designated does not contain a single state common ancestor.

WHAT NEXT

For a lock to be meaningful there must be a single state in which the lock begins. Your lock specification contains two or more operations that are on separate execution paths. But each of these operations "begins" the lock. Ask yourself what you want this constraint to enforce. If you really want both operations, replace the constraint with a set of independent constraints, each having only one beginning.

HLS-23 (error) Overconstrained timing.

DESCRIPTION

The system of timing constraints you have given has no solution.

WHAT NEXT

Analysis of your constraints indicates an internal inconsistency. You have asked that no more than four cycles take place between two operations, but these two operations are also constrained elsewhere to be no less than five cycles apart. Somewhere there is a constraint that you must relax.

HLS-24 (error) The named reset net does not exist

DESCRIPTION

The net you have designated as the reset net does not exist, or it is invisible in the current context.

WHAT NEXT

If you are not at the top of the design hierarchy, the net is probably not visible. Otherwise, the net you have named does not exist. Perhaps the name of the net inside the compiler is not the same as the name you gave it. To see what nets are visible, use **find net**.

HLS-25 (error) Could not find an architecture for entity '%s'.

DESCRIPTION

When elaborating a design for scheduling, you must designate an architecture.

WHAT NEXT

If you designated an architecture, and there are errors, correct the errors. If you did not designate an architecture, do so now.

HLS-26 (error) You specified variable '%s' as being mapped to a memory
but the variable was never used.

DESCRIPTION

A resource was declared that mapped the defined variable to a memory to be scheduled by behavioral synthesis. But the variable was never used.

WHAT NEXT

Either remove the variable from the resource, or make sure that the variable is used.

HLS-27 (error) The signal or port '%s' was mapped to a memory. Only variables can be mapped to a memory.

DESCRIPTION

Behavioral synthesis requires that only variables be mapped to memories.

WHAT NEXT

Change the declaration of the signal to a variable.

HLS-28 (warning) The variable '%s' was specified multiple times

on the resource ’%s’.

DESCRIPTION

In the variable declaration for the designated resource, the named variable was declared more than once.

WHAT NEXT

Declare the variable once only.

HLS-29 (error) The variable ’%s’ was mapped to a memory, but its type
is not an array type.

DESCRIPTION

Variables mapped to memories must be arrays.

WHAT NEXT

Declare the variable as an array.

HLS-30 (error) Binding %s of operator %s for processor %s (instance %s) not found

DESCRIPTION

When instantiating an operation instance, a binding cannot be found for the operator type on the designated processor.

WHAT NEXT

Make sure that the appropriate synthetic library .sldb is specified, and that the processor named actually exists in the .sldb libraries in memory.

HLS-31 (error) Illegal use of variable ’%s’ in function ’%s’./n

Memory slices are not supported.

DESCRIPTION

Your behavioral description has an array that’s mapped to a memory or register file. Your array access does not use the full data word length, rather, it uses just a bit slice. We only support memory array access accessing not slices.

WHAT NEXT

Assign the full data word length to a temporary variable and then read the bit slice

HLS-32 (error) Illegal use of variable ’%s’ in design ’%s’. Memory assignments without indexing are not supported.

DESCRIPTION

Currently we only support memory members accessing not slices or the whole array.

WHAT NEXT

Use the loop to do this type of assignments.

HLS-33 (error) Unanalyzable, unsatisfiable timing constraints.

DESCRIPTION

Detected an unsatisfiable timing constraint (as specified by set_cycles, set_min_cycles or set_max_cycles). Unfortunately, this error is unanticipated and Behavioral Compiler does not generate information to allow you to analyze the error using BCView.

WHAT NEXT

Unsatisfiable timing constraints usually result from maximum timing constraints being too tight with respect to minimum timing constraints. Maximum timing constraints are created by set_max_cycles and set_cycles commands, and minimum timing constraints are created by data flow dependencies, set_min_cycles, and set_cycles commands.

If you are unable to proceed based on the information provided by Behavioral Compiler and this manual page, please contact Synopsys support. We apologize for the inconvenience.

HLS-34 (Information) The output of preserved function %s at line %d
has type[%d:0].

DESCRIPTION

You receive this message to inform you that the output type of the specified preserved function has been assigned as specified.

Currently, in Behavioral Compiler, the output type of a preserved function in a Verilog design is determined by each consumer, even if the output type has been specified otherwise. In the following example, the output type of the preserved function foo will be [6:0] even though the function foo is specified to be [9:0], because the consumer x has the type [6:0].

```
module test(....)

reg [6:0] x;
reg [9:0] data1;
reg [9:0] data2;
reg [5:0] data3;

function [9:0] foo;
input [9:0] a;
input [9:0] b;
//synopsys preserve_function
   begin
     foo = a + b
   end

endfunction

always begin: reset_loop
    ....
    x = foo(data1, data2) + data3;
```

WHAT NEXT

If you can accept the type of the specified preserved function as described in the message, no action is required on your part. However, if you want to ensure a certain output type, create a temporary variable that contains the intended preserved function output type. Then, the entire output will propagate correctly.

For example, the following code creates a temporary variable foo_var with value [9:0], and assigns foo() to foo_var. Thus, the output of the preserved function has type [9:0].

```
module test(....)

reg [6:0] x;
reg [9:0] data1;
```

```
reg [9:0] data2;
reg [5:0] data3;
reg [9:0] foo_var;

function [9:0] foo;
input [9:0] a;
input [9:0] b;
//synopsys preserve_function
   begin
     foo = a + b
   end

endfunction

always begin: reset_loop
    ....
    foo_var = foo(data1, data2);
    x = foo_var  + data3;
```

HLS-35 (Warning) Unrolling the loop results in a large number of operations, this may increase search space and slow down run time%s

DESCRIPTION

BC unrolled the for loops by default and sometimes unrolling for loops causes slow donw the tool since it will have large number of operations. To speed up the tool, for loops can be kept unroll using dont_unroll attributes.

WHAT NEXT

Please use dont_unroll attribute to keep the loop in rolled.

HLS-36 (Error) The %s argument is obsolete. Please use the write_rtl command instead.

DESCRIPTION

You receive this error message because the **-rtl_script** argument to the **write** command is obsolete. Equivalent functionality is available through the **write_rtl** command.

The **-rules_name** option is no longer necessary.

WHAT NEXT

Use the **write_rtl** command to generate a synthesizable RTL model.

SEE ALSO

write_rtl (2).

HLS-37 (error) No time to evaluate condition

DESCRIPTION

A conditional branch is trying to create two initial states in the state graph. This conditional cannot be evaluated in time to create the proper conditional transitions. This situation probably occurred because you began a loop inside a conditional in the first state of a process.

WHAT NEXT

Insert a *wait* to give the machine time to evaluate the condition before it tries to enter the loop. Or move the condition inside the loop.

HLS-38 (error) chained loop begins (fixed i/o timing)

DESCRIPTION

Two loop beginnings occur in the same state, which is illegal in fixed I/O timing mode.

WHAT NEXT

To allow time to evaluate the *exit* condition of the outer loop, separate the loop **begins** by one or more *wait* statements.

HLS-39 (information) All wait statements are followed by an exit. A global synchronous reset with %s polarity has been inferred

for %s.

DESCRIPTION

When all *wait* statements are followed by an *exit* from the main loop, the exits are treated as a global synchronous reset. This treatment allows a more efficient implementation for the exit logic.

WHAT NEXT

This is an information message. No further action is required.

HLS-40 (information) All clock transitions are followed by a disable statement.
A global synchronous reset with %s polarity has been inferred for %s.

DESCRIPTION

When all clock transitions are followed by an exit from the main loop, the exits are treated as a global synchronous reset. This allows a more efficient implementation for the exit logic.

WHAT NEXT

This is an information message. No further action is required.

HLS-41 (error) Port '%s' was assigned to using a non-RTL assignment at line %d. Use the RTL assignment operator '<=' for
assignments to ports.

DESCRIPTION

Behavioral synthesis requires that the transitions of all ports be synchronized to clock boundaries. As a result, the RTL assignment operator must be used to assign to ports.

WHAT NEXT

Change the "=" assignment operator to a "<=" every time the port is written to.

HLS-42 (error) The exit statement on line %d in file %s is illegal. Only global reset exits are allowed to cross loop boundaries.

DESCRIPTION

Currently, the only exits that are allowed to cross loop boundaries are global resets.

WHAT NEXT

Change the invalid statement.

HLS-43 (error) A write operation at the end of '%s' (%s) conflicts with the I/O at the beginning of the loop (%s). When running in super state mode, please insert a wait statement after the last write in the loop.

DESCRIPTION

When running behavioral synthesis in "super-state" mode, the scheduler is required to make sure that writes in the super-state happen at the end of the super-state, and reads of I/O happen before the writes (and after the writes of the previous super-state). This helps to match simulation behavior.

However, consider the following pseudo-code fragment:

```
while ( <cond> )
    out <= ...
    <<< clock boundary >>>
    out <= ...
end
```

When the loop executes for the second time, the write to port "out" at the end of the loop will conflict with the write to port "out" at the beginning of the loop. In the simulation of the behavioral code, the out at the end of the loop will be over-written by the out at the beginning of the loop. However, because the scheduler will need to insert more states between the beginning and end of the loop, the behavior of the RTL machine generated would be different. The write to port "out" at the end of the loop would then be visible to the outside world for a few cycles.

To avoid this simulation/synthesis mis-match, it is required that there is a clock boundary between writes at the end of the loop and I/O at the beginning.

WHAT NEXT

Insert a clock boundary (wait in VHDL or always @ in verilog) at the end of the loop (after the last write in the loop).

HLS-44 (error) The write operation '%s' conflicts with I/O at the beginning of '%s' (%s). When running in super state mode, please make sure that the I/O is broken by a clock boundary (e.g. just before the loop).

DESCRIPTION

When running behavioral synthesis in "super-state" mode, the scheduler is required to make sure that writes in the super-state happen at the end of the super-state, and reads of I/O happen before the writes (and after the writes of the previous super-state). This helps to match simulation behavior.

However, consider the following pseudo-code fragment:

```
out <= ...
while ( <cond> )
    out <= ...
```

When simulation the behavioral code, the write to port "out" before the loop will be over-written by the write to port "out" after the loop. When the design is scheduled, however, cycles will be inserted at the beginning of the loop which will cause the first write to port "out" to be visible for a few cycles. This would cause a simulation mis-match.

WHAT NEXT

Insert a clock boundary (wait in VHDL or always @ in verilog) just before the loop.

HLS-45 (error) The write operation '%s' before the loop '%s' conflicts with I/O that occurs after the loop (%s).

DESCRIPTION

When running behavioral synthesis in "super-state" mode, the scheduler is required to make sure that writes in the super-state happen at the end of the super-state, and reads of I/O happen before the writes (and after the writes of the previous super-state). This helps to match simulation behavior.

However, consider the following pseudo-code fragment:

```
out <= ...
while ( <cond> )
    ...
end
out <= ...
```

When the behavioral code is simulated, when "cond" is FALSE, the write to port "out" after the loop will over-write the write before the loop. However, the scheduler will have to insert cycles to see whether or not the loop needs to be evaluated. As a result, the write to port "out" before the loop will become visible to the outside world for a cycle or two.

To prevent this simulation/synthesis mis-match, a clock boundary needs to be inserted to make sure that the two writes to port "out" will not happen in the same cycle in the behavioral code.

WHAT NEXT

Insert a clock boundary (wait in VHDL or always @ in verilog) either just before the loop, or just after the loop.

HLS-46 (error) Write operations occur inside '%s' just before an exit (%s) that conflict with I/O that happens after

the loop (%s).

DESCRIPTION

When running behavioral synthesis in "super-state" mode, the scheduler is required to make sure that writes in the super-state happen at the end of the super-state, and reads of I/O happen before the writes (and after the writes of the previous super-state). This helps to match simulation behavior.

However, consider the following pseudo-code fragment:

```
while ( <cond> )
    ...
    if ( <cond2> )
        out <= ...
        exit;
    end if
    ...
end
out <= ...
```

When simulating the behavioral code, the write to port "out" just before the exit will over-write the write to port "out" after the loop. However, if the scheduler were to insert cycles between the two writes to port "out", the simulation behavior would be different.

WHAT NEXT

The easiest thing to do is to insert a clock boundary (wait in VHDL or always @ in verilog) after the end of the loop.

The other option would be to insert a clock boundary before every exit from the loop.

HLS-47 (error) The design contains parallel paths where one path is broken by clock boundaries, and another path is not. This is not allowed in super-state mode. The paths start from the if/case statement on line%s in file %s.

A wait statement is located on line %d in file %s.

DESCRIPTION

Consider the following code fragment:

```
if ( <cond> )
    <<< clock boundary >>>
end
```

The conditional clock boundary causes problems because the scheduler is not able to divide the circuit up into "super-states". The I/O that happens before the "if" statement may or may not occur in the same cycle as the I/O that happens after the "if" statement.

WHAT NEXT

Either remove the clock boundaries (wait in VHDL or always @ in verilog) along the parallel paths that contain them, or else insert clock boundaries in the paths where they are missing.

HLS-48 (error) Missing clocks in design.

DESCRIPTION

A clock, and a clock period, must be defined for each behavioral process before a design is scheduled. This is necessary in order to determine if an operation can fit into one cycle, or multiple cycles, or if multiple operations can fit into a single cycle.

WHAT NEXT

Make certain every signal which "clocks" a behavioral process (by virute of being used in the wait statements of the process) has been used in a create_clock command after the design has been elaborated. The create_clock command specifies the signal that is the clock and the clock period.

HLS-49 (error) No license for behavioral synthesis.

DESCRIPTION

Could not find a license for behavioral syntheis.

WHAT NEXT

Make certain that you have a license and that the license is properly installed before next trying to use the behavioral synthesis product.

HLS-50 (Warning) Reset declarations of user and HDL clash: non-equivalent simulation may result.

DESCRIPTION

The user has declared a reset net, and there is (apparently) a reset net implicit in the HDL text: the user’s reset net will be used.

WHAT NEXT

The reset net declared by the Design Compiler command will override any automatic inference of reset net and reset sense (true high or low) that can be derived from the HDL description. However, this may cause a clash between the behaviors of the synthesized design and the original HDL, particularly in the case where a true-low or negated signal is used. In any case, the user encountering this warning should make up his or her mind as to which reset methodology is to be used: and then either (1) declare an implicit reset net and delete all references to it from the architecture of the HDL, or else (2) make sure that there is a conditional main-loop exit after each and every wait of the HDL, and delete all references to the reset net from the Design Compiler session and/or script. It is mixing these two strategies that causes the warning to be issued.

HLS-51 (error) Unsatisfiable Timing Constraints

DESCRIPTION

Detected an unsatisfiable timing constraint (as specified by set_cycles, set_min_cycles or set_max_cycles).

WHAT NEXT

Unsatisfiable timing constraints usually result from maximum timing constraints being too tight with respect to minimum timing constraints. Maximum timing constraints are created by set_max_cycles and set_cycles commands, and minimum timing constraints are created by data flow dependencies, set_min_cycles, and set_cycles commands.

HLS-52 (error) Fixed IO schedule is unsatisfiable

DESCRIPTION

Two or more fixed operations in the HDL source have too much summed path delay between them to be scheduled in fixed i/o mode. Move the operations, add waits, or relax the clock.

WHAT NEXT

In fixed IO mode, the wait statements in HDL source code specify partial schedules for input/output operations and loop begins and ends. If the critical path between two fixed events is longer than the distance between them, then a satisfactory schedule cannot be constructed. You can either insert wait statements, or relax your clock period, to increase the amount of time available to perform the operations you have specified.

HLS-53 (error) Error in building synthetic operators.

DESCRIPTION

An error occured in building the operators is this design. Since the operator timings are needed for behavioral synthesis, this results in an abort of the scheduling of the design.

WHAT NEXT

Check your synthetic library variables and licenses.

HLS-54 (error) Clock sense is incompatible with HDL text.

DESCRIPTION

Somewhere in the HDL text you have said that the active clock edge is either rising or falling. Then you issued a command to set the active clock edge. But the command did not agree with the text.

WHAT NEXT

Get your story straight and try again. You don’t have to specify the edge in both the HDL and in Design Compiler; try just doing it in one place or the other. But if you must do both, at least get it consistent.

HLS-55 (error) At line %d, a clock event is being checked using an ’if’ statement. Checking for clock edges using if statements is not supported when elaborating for scheduling. Please use wait statements instead.

DESCRIPTION

When elaborating a design for scheduling, users are not allowed to check for clock edges using if statements. For example, the following is not supported:

```
process ( clk ) begin
    if ( clk’event and clk = ’1’ ) then
.
.
.
    end if;
end process;
```

Instead, you should use something like the following:

```
process begin
    wait until clk’event and clk = ’1’;
.
.
.
end process;
```

WHAT NEXT

Change the "if (clk’event)" to a "wait until clk’event".

HLS-56 (error) The always block at line %d checks a clock edge in its timing control. When elaborating a design for scheduling, you are not allowed to check clock edges in the timing control of always blocks. Instead, clock edges should be checked for in

the body of the block.

DESCRIPTION

When elaborating for scheduling, you are only allowed to check for clock edges inside the body of the block. For example, the following form is illegal:

```
always @ ( posedge clk ) begin
.
.
.
end
```

Instead, please use the following format:

```
always begin

    @ ( posedge clk )
.
.
.
end
```

WHAT NEXT

Modify the verilog source to test the clock edge inside the body instead of inside the block’s timing control.

HLS-57 (error) When elaborating for scheduling, instantiated components are not supported. An instantiated component was found on line %d in file ’%s’

DESCRIPTION

Instantiated components are not allowed inside designs that are being elaborated for scheduling.

WHAT NEXT

Either remove the instantiated component, or move the component to a higher level design (i.e. the design that instantiates the behavioral design).

HLS-58 (error) When elaborating a design for scheduling, there only one block is allowed. The design '%s' contains blocks at lines %d and %d.

DESCRIPTION

Designs that are elaborated for scheduling are only allowed to have one block (i.e. one process in VHDL and one always block in verilog).

WHAT NEXT

Either split the blocks into multiple designs, or merge the blocks together.

HLS-59 (error) The block at line %d has multiple clocks (%s and %s). Multiple clocks are not supported when elaborating for scheduling.

DESCRIPTION

A block that is elaborated for scheduling can only be triggered by a single clock.

WHAT NEXT

Remove one of the clocks from the block.

HLS-60 (error) When elaborating for scheduling, clocks must be single-bit ports. At line %d, variable %s

is used as a clock.

DESCRIPTION

Clocks when elaborating for scheduling must be single bit ports.

WHAT NEXT

Remove the illegal clock statement, and replace it with a clock that is triggered by a port.

HLS-61 (error) When elaborating for scheduling, clocks must be single-bug ports. The multi-bit port '%s' was used in design '%s'.

DESCRIPTION

It is illegal to use a multi-bit port as a clock when elaborating for scheduling.

WHAT NEXT

Use a single-bit port as the clock.

HLS-62 (error) The wait statement at line %d is not supported when elaborating for scheduling.

DESCRIPTION

WHAT NEXT

HLS-63 (error) The port '%s' at line %d in design '%s' is an inout port.

Inout ports are not supported when elaborating for scheduling.

DESCRIPTION

Inout ports are not currently supported by scheduling.

WHAT NEXT

In verilog, change the port from an inout to either an input or an output port. For VHDL, change the port to either buffer, in, or out.

HLS-64 (error) The edge specification used on line %d is not supported when elaborating for scheduling.

DESCRIPTION

When elaborating for scheduling, only positive or negative edges are supported.

WHAT NEXT

Change the edge specification.

HLS-65 (error) The variables that are mapped onto memory '%s' contain indices that overlap. Currently, variable indices are not allowed to overlap.

DESCRIPTION

When multiple variables are mapped onto the same memory, the indices of the variables must be non-overlapping. In future releases, we may support re-mapping of array indices, but currently the indices specified by the user are the ones that are used.

WHAT NEXT

Change the array indices so that they are non-overlapping.

HLS-66 (error) Indexes into array types must be done using an integer
index. The access to variable ’%s’ (resource ’%s’)
at line %d is not an integer.

DESCRIPTION

Accesses to arrays must be done using integer types.

WHAT NEXT

Change the index into the array to be an integer type.

HLS-67 (error) Specified clock period is insufficient.
Available clock period(%.1f) = specified clock period(%.1f) - margin(%.1f).

DESCRIPTION

The clock period specified is insufficient. Behavioral Compiler must reserve a part of the clock period to account for FSM delay, FF setup and register clock-to-Q delay. This reserved part is called the margin. The available clock period is the specified clock period minus the margin. Datapath operations are scheduled in the available clock period.

This error message is generated if the margin exceeds the specified clock period, leaving no available clock period in which operations can be scheduled.

WHAT NEXT

Please make sure the clock period specified (using the create_clock command) is a positive value and is larger than the margin that Behavioral Compiler reserves. The margin can viewed and adjusted using the bc_margin command.

HLS-68 (error) Scheduled designs must have exactly one clock signal.

%d were found.

DESCRIPTION

A process to be scheduled is allowed to have exactly one clock signal. Any other number is wrong and will cause scheduling to exit.

WHAT NEXT

Either declare a clock using create_clock, or don't declare so many clocks. Be careful, if you have used explicit references to a clock in wait statements, that the clock you declare is the same as the clock in all of your wait statements.

HLS-69 (error) Failed to Find a Legal Schedule

DESCRIPTION

Scheduling has failed to find a legal schedule. An illegal schedule is one in which operations bound to the same architectural resource (e.g., read/write operations on the same RAM) are scheduled into overlapping csteps, or operations are scheduled into skipped csteps (e.g., csteps between an exit and loop-end). This usually happens due to low scheduling effort, or due to tight timing constraints.

WHAT NEXT

First, make sure that the number of cycles specified allows sequential scheduling of operations bound to the same resource. Second, use timing constraints to guide scheduling (e.g., use "set_cycles" to sequence operations bound to the same resource). Third, try a higher scheduling effort level and/or a higher number of cycles.

HLS-70 (error) The process at line %d is inside of a generate statement.
This is not allowed when elaborating for scheduling.

DESCRIPTION

Processes are not allowed inside of generate statements.

WHAT NEXT

Remove the generate statement.

HLS-71 (error) The design has already been scheduled.

DESCRIPTION

You have passed a design to scheduling that has already been scheduled. Essential data has been stripped off the design.

WHAT NEXT

You should re-elaborate the design.

HLS-72 (error) The design has no schedule report information.

DESCRIPTION

You have asked for a report on the scheduling of a design that does not have any scheduling report data attached to it.

WHAT NEXT

Most likely you have asked for a scheduling report after changing the current design or after loading a .db file that was not created by scheduling. That is, the file and/or design is simply not annotated with the scheduling information. You should check the file and how it was generated. If necessary, re-run scheduling to generate a new db file.

HLS-73 (error) Failed to allocate hardware for '%s'.

DESCRIPTION

You receive this message because Behavioral Compiler is unable to allocate hardware for the design. The most likely cause of this failure is that incompatible operations have been constrained to the same processor. Synthesis libraries do not have any one component that can execute all of these operations.

An example of a pair of incompatible operations is an addition and a memory read operation. A memory usually cannot perform an addition and so the two operations cannot be executed on the same processor.

WHAT NEXT

Review your synthesis script for commands that constrain operations and variables to the same hardware resource. Examples of such commands are **set_common_resource** and **set_exclusive_use**.

Review the output of these commands in your synthesis log to verify any incompatible operations that are being constrained and remove those constraints.

Use the **bc_set_implementation** command with the **-list_valid** option to list hardware that can implement the operations you attempted to constrain.

SEE ALSO

bc_set_implementation (2), **set_common_resource** (2), **set_exclusive_use** (2).

HLS-74 (Error) Unable to schedule loop '%s'.

DESCRIPTION

You receive this error message because the **schedule** command is unable to schedule the specified loop. The loop violates a scheduling restraint.

For further information about interpreting the report, refer to the one of the following user and modeling guides:

- *Behavioral Compiler VHDL User and Modeling Guide*
- *Behavioral Compiler Verilog User and Modeling Guide*
- *SystemC Compiler User and Modeling Guide*

WHAT NEXT

Resolve the scheduling constraint violation by modifying your behavioral source code or synthesis script so that the number of required clock cycles is less than or equal to the number of available clock cycles.

Study the contributing constraints or relationships listed in the constraint violation table. Your modifications to the behavioral source code and synthesis script will need to reconcile these constraints.

The constraints and relationships are described below. They are listed alphabetically based on the name of the constraint or relationship as it appears in the constraint violation table.

assigned clock cycle The **schedule** command has scheduled the two operations to occur the specified number of clock cycles apart.
Use the **set_cycles**, **set_min_cycles**, and **set_max_cycles** commands to control how these operations are scheduled relative to one another.

conflicting array accesses The two operations might access the same array location, causing the array accesses conflict. In order to prevent the conflict, the accesses must not occur in the same clock cycle.
For more information about conflicting array accesses, refer to the man pages for the **bc_report_memories** command if your array is mapped to a memory, or the man pages for the **bc_report_arrays** command if your array is mapped to a register file.

control dependency Operations inside an *if* or *case* conditional branch must be executed after the conditional branch is evaluated and before the conditional branch ends.

data dependency A data dependency exists between two operations if the output of one operation is the input of a second operation.

inferred clock cycle (cycle fixed mode) In cycle-fixed I/O scheduling mode, the **schedule** command counts the number of clock statements between I/O-related operations in your behavioral source code, and executes the operations in exact clock cycles.
The types of I/O-related operations are

- Reads and writes of I/O ports
- Reads and writes of signals
- Loop boundaries (begin, end, continue, exit).

inferred constraint The **schedule** command has inferred a dependency to prevent the operations from being scheduled in inappropriate clock cycles.
Modify other constraints and relationships to accommodate the inferred constraint.

inner pipelined loop latency This constraint reflects the latency you specified for a pipelined loop.

loop latency This constraint is the number of clock cycles needed to execute one iteration of the loop.
Modify the loop latency using the **set_cycles**, **set_min_cycles**, or **set_max_cycles** command to constrain the beginning and end of the loop.

loop pipelining exit requirement Exits from a pipelined loop must occur within the initiation interval to ensure their occurrence before the next iteration of the loop starts.

loop pipelining flush requirement After exiting a pipelined loop, the FSM controller waits for all remaining iterations of the pipeline to finish. The number of clock cycles for completion depends upon the latency and the initiation interval.

loop pipelining latency This constraint reflects the latency you specified for a pipelined loop.

loop precedence Operations inside a loop must execute after the loop begins and before it ends.

multicycled combinational delay The operation has a combinational delay that exceeds the available clock period. The available clock period is specified with the **create_clock** command minus the clock cycle margin.

pipelined loop carried dependency Loop carried dependencies are data dependencies that span successive iterations of a loop. The producer of the data is in one iteration and the consumer is in another.
The pipelined loop carried dependency ensures that the producer is executed at a clock cycle equal to or earlier than the clock cycle of the consumer.

precedence This constraint indicates a precedence between the two operations that requires the first operation to occur earlier or at the same clock cycle as the

second operation.

registered control You have a conditional expression whose value must be computed at least one clock cycle before operations within the conditional branches can be executed.
This occurs under one of the following conditions:

• You have used the **register_control -outputs** command to specify that the generated FSM controller for your design must have registered outputs.

• The operation in a conditional branch is a multicycled operation. The condition must be held in a register for the duration of the operation.

• The operation in a conditional branch is mapped to a synthetic operator whose inputs are required to be held stable over a clock cycle. Properties of operator inputs are specified in the synthetic library containing the operator.

registered input The inputs of the second operation must be computed one clock cycle earlier.
This occurs under one of the following conditions:

• You have used the **register_control -inputs** command to specify that the generated FSM controller for your design must have its inputs registered.

• The second operation is a multicycled operation. The inputs to the operation must be held stable for the duration of the operation.

• The operation is mapped to a synthetic operator whose specification in the synthetic library requires it to have stable inputs.

required clock cycle The **schedule** command has inferred a dependency to prevent the operations from being scheduled in inappropriate clock cycles.
Modify other constraints and relationships to accommodate these requirements.

resource capacity dependency One or more of the operations are mapped to synthetic operators bound to synthetic components with resource capacity limits. In order to satisfy the resource capacity limits, the two operations must be executed in different clock cycles.
An example is an array that is mapped to a single-port memory. All array accesses are mapped to memory access operators and these are implemented on memory ports. Since the memory has only one port, no two array accesses can be executed in the same clock cycle.
The constraint or relationship string contains information regarding the component instance name and the specific resource provided by that component that is limited.

sequential operation state transition An operation is mapped to a synthetic operator (for example, mult_2_stage_UNS_OP) implemented on a sequential component (for example, DW02_mult_2_stage). This constraint indicates that the two stages of the sequential component must be executed in separate clock cycles.

superstate i/o ordering This constraint reflects the relationships between read and write to I/O ports or signals in superstate-fixed I/O scheduling mode.

• All read and write operations in one superstate occur at least one clock cycle before those in the next superstate.

• All write operations belonging to the same superstate execute in the clock cycle corresponding to the trailing superstate boundary (clock statement).

• All read operations belonging to the same superstate execute at least one clock cycle after the leading superstate boundary (clock statement) and at or before the trailing superstate boundary (clock statement).

superstate ordering Consecutive clock statements (superstates) in your code are executed at least one clock cycle apart.

unchainable The first operation produces data that is used by the second operation. The two operations cannot be executed in the same clock cycle because the cumulative delay through the synthetic components that implement them exceeds the available clock period. The available clock period is specified with the **create_clock** command minus the clock cycle margin.

unchainable across loop iterations The second operation produces data that is used by the first operation in the next iteration of the loop. The two operations cannot be executed in the same clock cycle because the cumulative delay through the synthetic components that implement them exceeds the available clock period. The available clock period is specified with the **create_clock** command minus the clock cycle margin.

unchainable(memory read) The operations feeding data to or getting data from the memory read operation cannot be executed in the same clock cycle as the memory read. This requirement is defined by the synthetic library description of the memory implementing the memory read.

unchainable(memory write) The operations feeding data to the memory write operation cannot be executed in the same clock cycle as the memory write.
This requirement is by the synthetic library description of the memory implementing the memory write.

user 'chain_operations' This reflects a constraint set with the **chain_operations** command.

user 'dont_chain_operations' This reflects a constraint set with the **dont_chain_operations** command.

user 'set_cycles' This reflects a constraint set with the **set_cycles** command.

user 'set_max_cycles' This reflects a constraint set with the **set_max_cycles** command.

user 'set_min_cycles' This reflects a constraint set with the **set_min_cycles** command.

user 'set_common_resource' This reflects a constraint set with the **set_common_resource** command. In order to satisfy the resource capacity limit specified, the two operations must be scheduled in different clock cycles.

SEE ALSO

schedule (2).

HLS-75 (Error) Unable to schedule loop '%s'.

DESCRIPTION

You receive this message because the **schedule** command has encountered a scheduling constraint violation and is unable to complete scheduling the loop.

Scheduling constraints are caused by behavioral code constructs and synthesis commands. The HLS-74 man page lists the various scheduling constraints.

The report that immediately precedes this error message contains details about the violation.

WHAT NEXT

In most cases, this error is caused by operations or code constructs that are forced to execute in the same clock cycle.

Use scheduling constraint commands such as **set_cycles**, **set_min_cycles**, and **set_max_cycles**, to force the operations or code constructs to be executed in different clock cycles.

For further information about resolving scheduling constraint violations, see the HLS-74 man page.

SEE ALSO

HLS-74 (n).

HLS-78 (error) The requested FSM table file cannot be opened.

DESCRIPTION

You have asked for a file that contains data on the FSM state table and output pin assignments. The file name you have given cannot be opened.

WHAT NEXT

Check write permissions on the directory in question. Check for the existence of a file of the same name with no write permission. Check disk quotas and availability.

HLS-79 (error) Internal error: no next state.

DESCRIPTION

Something has gone seriously wrong inside the scheduler’s control unit generator. It has created a state that has no next state under any circumstances.

WHAT NEXT

File a bug report. Try rewriting your HDL with different loop exits, continues, and nesting structures.

HLS-80 (error) Cannot open schedule report file

DESCRIPTION

I cannot open the desired file for some reason.

WHAT NEXT

Try another file name, another disk, another directory, or making some space on your current disk. Check protection on the current directory.

HLS-81 (error) Current design is not for HLS

DESCRIPTION

The current design is not set up properly for HLS.

WHAT NEXT

The current design may not be the top level design, it may not have been elaborated using the proper scheduling flag, or it may simply be inappropriate as a scheduling target.

HLS-82 (error) The reg ’%s’ is driven in block ’%s’ and in block ’%s’. Currently, when elaborating for

scheduling, a reg may only be driven in a single block.

DESCRIPTION

There are two always blocks that both drive the same reg. This is currently not supported when elaborating for scheduling.

WHAT NEXT

Re-write the source code so that the reg is only driven in a single block.

HLS-83 (error) The signal '%s' is driven in process '%s' and in process '%s'. Currently, when elaborating for scheduling, a signal may only be driven in a single process.

DESCRIPTION

There are two processes that both drive the same signal. This is currently not supported when elaborating for scheduling.

WHAT NEXT

Re-write the source code so that the signal is only driven in a single process.

HLS-84 (warning) No area information for operation %s.

DESCRIPTION

No area estimate is available for the operation. This can adversely impact overall quality of results.

WHAT NEXT

Area estimates are derived from cached model entries that are generated before scheduling.

Specify a cache read directory that has entries for the operations that are contained in the behavioral description, or specify a (writeable) cache write directory and .

HLS-85 (warning) Unknown annotation style.

DESCRIPTION

Known styles are "pre" and "post".

WHAT NEXT

This is not normally set by the user. "Pre" means that there will be a register between the control unit outputs and the datapath control inputs. "Post" means this will not be present. In some cases it may be necessary to override the user’s choice to assure functional correctness. The default is "post".

HLS-86 (error) Operator name ’%s’ not found in Synthetic Libraries

DESCRIPTION

The specified operator name is not defined in any of the current synthetic libraries.

WHAT NEXT

Add the appropriate synthetic library to the list, synthetic_library.

HLS-87 (error) No schedulable process

DESCRIPTION

There is no process of that name that can be scheduled.

WHAT NEXT

The process(es) you have named (or the default processes if you did not name any) is not schedulable. Hence the command you have issued is not appropriate. If you are not sure what the proper process is, try ’find’. If you didn’t use the -s flag in elaborate, you must elaborate with the -s flag.

HLS-88 (error) Bad edge constraint

DESCRIPTION

You cannot constrain a loop without using either the from_begin, from_end, to_begin, or to_end flags.

WHAT NEXT

Review the design and reissue the constraint using a flag that means what you want. The default for ordinary operations is to constrain with respect to the beginning; but no such default exists with loop or other structured operations.

HLS-89 (error) Bad hierarchy

DESCRIPTION

The constraint algorithm has encountered an unexpected situation in the hierarchy of your design.

WHAT NEXT

It appears that the object you wish to constrain is not contained within (i.e. it is not a cell of) any other object. As such, it is impossible to constrain it. If you wish to constrain the outermost loop of a process, which contains all of the behavior of the process, you should constrain the process itself.

HLS-90 (error) No load enable register in the standard synthetic library.

DESCRIPTION

There is no load enable register in the standard synthetic library. This register is necessary to calculate the area costs of registers for behavioral synthesis.

WHAT NEXT

Since this register description should be in the standard synthetic library, this error is most likely due to an improper installation of the Synopsys tools. Please contact your system administrator.

HLS-91 (warning) Inconsistent pipelined loop (simulation may not match)

DESCRIPTION

A pipelined loop has been given one number of cycles by implicit scheduling using fixed i/o timing mode, and another number of cycles by a user command that establishes loop pipelining initiation interval and latency. The result is that you should not expect simulation of the scheduled and unscheduled designs to match.

WHAT NEXT

If this really matters to you, you should probably rewrite your HDL so that the fixed i/o mode interpretation will match the loop pipeline parameters you have given. You could also use superstate-fixed mode.

HLS-92 (error) No reset signal polarity

DESCRIPTION

There is a reset signal but whether it is true high or true low has not been specified.

WHAT NEXT

Use the set_implicit_reset_signal command to state the proper polarity.

HLS-93 (error) No ending endpoint for timing constraint

DESCRIPTION

You must use a "to", "to_begin", or "to_end", or you must state a valid cell at which the constraint can end.

WHAT NEXT

Use the find cell command to find an appropriate cell to begin the constraint; then use the appropriate flag to state which timing edge of the cell you want to specify. If the cell is a single-cycle operation, it doesn’t matter which you use.

HLS-94 (error) No beginning endpoint for timing constraint

DESCRIPTION

You must use a "from", "from_begin", or "from_end", or you must state a valid cell from which the constraint can begin.

WHAT NEXT

Use the find cell command to find an appropriate cell to begin the constraint; then use the appropriate flag to state which timing edge of the cell you want to specify. If the cell is a single-cycle operation, it doesn’t matter which you use.

HLS-95 (error) Multiple conflicting constraint endpoints

DESCRIPTION

The constraint has multiple from or to endpoints that are in conflict with one another.

WHAT NEXT

Use multiple constraint commands to accomplish this kind of goal. You aren’t allowed to use more than one of each kind of endpoint specifier (from or to) in one constraint command.

HLS-96 (error) No target library

DESCRIPTION

I am unable to find a target library.

WHAT NEXT

The DC variable "target_library" should be set to the name of the desired technology library.

HLS-97 (warning) The delay specified on the write to signal ’%s’ on line %d is %d which is not an exact multiple of the cycle time %d.

%d cycles will be used for the delay.

DESCRIPTION

When using the after statement with the Behavioral Compiler, the delay specified must be an exact multiple of the clock period.

WHAT NEXT

Modify the delay in the hdl source to be an exact multiple of the clock period.

HLS-98 (error) The delay on the write to signal '%s' at line %d causes the assignment to be pushed outside of the enclosing loop. In order for synthesis to match simulation, this requires loop pipelining. However, the enclosing loop contains exits, and loop pipelining is not currently allowed in loops with exits.

DESCRIPTION

When a signal is delayed such that its assignment occurs outside of the enclosing loop, the loop must be pipelined in order to match simulation. However, in the current release, loop pipelining is only allowed inside of loops with no exit statements.

WHAT NEXT

If you do not want pipelining, either decrease the delay on the signal or add more waits inside of the loop. If you do want pipelining, you will have to remove the exits in the loop (note that while loops have an implicit exit).

HLS-99 (error) The delay on the write to signal '%s' at line %d causes the assignment to be pushed outside of the enclosing block In order for synthesis to match simulation, this requires loop pipelining. However, the enclosing block

is not a loop so no loop pipelining can occur.

DESCRIPTION

If a delayed write causes the assignment to be pushed outside of a preserved function call, it is an error as there is no way to match simulation.

WHAT NEXT

Either add more wait statements to the function, or decrease the delay on the assignment.

HLS-100 (information) The delay on the write to signal '%s' at line %d causes the assignment to be pushed outside of the enclosing block In order for synthesis to match simulation, this requires loop pipelining. The loop will be pipelined with an initiation interval of %d and a latency of %d.

DESCRIPTION

When a signal is delayed such that its assignment occurs outside of the enclosing loop, the loop must be pipelined in order to match simulation. The loop will be automatically pipelined in order to match simulation.

WHAT NEXT

HLS-101 (warning) The %s is delayed by %d cycles. However, delayed assignments are only supported for fixed-I/O mode. The delay will be ignored.

DESCRIPTION

Delayed assignments are supported only during fixed I/O scheduling.

WHAT NEXT

If the hdl code depends on the delay, either use fixed I/O scheduling, or rewrite the hdl so that it no longer depends on the delayed assignment.

HLS-102 (error) Object to be extruded is not a cell

DESCRIPTION

You cannot extrude any object except a cell.

WHAT NEXT

Check that the arguments you are passing to the **extrude** command are in fact cells.

Be careful that the design owning the cells you are extruding is not used in another design or that it has already got dummy pins with the correct names. Otherwise a link error will occur.

HLS-103 (error) Must have a Design Compiler Expert license to compile a design
for behavioral synthesis.

DESCRIPTION

Behavioral Compiler requires a Design Compiler Expert license to time the design (before scheduling), as well as when mapping a design that has been scheduled to gates.

WHAT NEXT

HLS-104 (information) Set loop '%s' to have initiation interval of %d cycles and latency of %d cycles.

DESCRIPTION

Executing the command "pipeline_loop"

WHAT NEXT

HLS-105 (error) Loop ’%s’ cannot be set to latency of %d cycles because
its member node %s is fixed at %d cycles after the loop begins.

DESCRIPTION

WHAT NEXT

HLS-106 (error) Loop ’%s’ cannot be loop-pipelined because it contains exits

DESCRIPTION

WHAT NEXT

HLS-107 (error) Loop ’%s’ cannot be set to initiation interval of %d cycles and latency of %d cycles because %d is not an even multiple of %d

DESCRIPTION

WHAT NEXT

HLS-108 (error) Loop ’%s’ cannot be loop pipelined because it

contains nested loop ’%s’

DESCRIPTION

WHAT NEXT

HLS-109 (warning) Delayed assignments require the transport keyword in order for synthesis to match simulation. The transport keyword is missing on line %d in file %s.

DESCRIPTION

Delayed assignments are supported when elaborating for behavioral synthesis, but the delay is synthesized as a "transport delay" instead of the default "intertial delay". The syntax of the tranport delay is:

```
out <= transport f(in) after 100 ns;
```

WHAT NEXT

Add the transport keyword to the delayed assignment.

HLS-110 (warning) The loop ’%s’ was specified multiple times as dont_unroll.

DESCRIPTION

This warning message occurs when multiple resources are declared that specify the named loop as being *dont_unroll*.

For example:

```
/* synopsys resource R1 : dont_unroll = "L1 L1"; */
```

WHAT NEXT

Remove the named loop.

HLS-111 (warning) A dont_unroll attribute was specified for a loop
named ’%s’, but the loop could not be found.

DESCRIPTION

This warning message indicates that the user attempted to set a *dont_unroll* attribute on a loop that doesn’t exist.

WHAT NEXT

Do one of the following: correct the *dont_unroll* attribute to point to an existing loop; create the specified loop; or remove the *dont_unroll* attribute.

HLS-112 (error) A reset has already been inferred from the HDL by elaborate

DESCRIPTION

The stated reset signal conflicts with one already inferred from the HDL text.

WHAT NEXT

Check the name of the reset signal in the HDL text. The name may be different for different processes, so you must identify which process you mean. If you insist on the reset signal you gave in the command, you may have to change the name in the HDL text.

HLS-113 (error) Reset signal polarity clash

DESCRIPTION

The reset signal polarity clashes with that given in the HDL description.

WHAT NEXT

It may be necessary to correct this condition on a process-by-process basis. Check the HDL text as well; something may be happening that you did not intend to cause.

HLS-114 (error) Inconsistent reset signal polarity

DESCRIPTION

The reset cannot be both true high and true low.

WHAT NEXT

Use either high or low for this flag, but not both.

HLS-115 (error) Either true or false

DESCRIPTION

The reset signal must be declared "asynchronous" or "not asynchronous."

WHAT NEXT

The default is synchronous (false). If you want to set or reset this flag, you must use the flag value (asynchronous is TRUE or FALSE).

HLS-116 (error) Invalid i/o mode flag

DESCRIPTION

The valid options are *cycle_fixed*, *superstate_fixed*.

WHAT NEXT

The reference manual describes what each option means.

HLS-117 (Information) Design has already been timed.

DESCRIPTION

Because the design has already been timed for Behavioral Compiler, it will not be timed again unless the **bc_time_design -force** command is used.

WHAT NEXT

The **bc_time_design -force** command should be used if the technology or synthetic libraries have changed since the design was last timed.

HLS-118 (warning)The for loop on line %d uses the iterator '%s' that is larger than necessary to cover the range of the loop. '%s' is defined on line %d with a bit-width of %d. The range of the loop is %d to %d which only requires the iterator to have a bit-width of %d. This will create inefficient logic if the for loop is not unrolled when elaborating for Behavioral Compiler.

DESCRIPTION

Consider the following example:

```
integer i;
.
.
.
for ( i = 0 ; i < 10 ; i = i + 1 ) begin : for1
    .
    .
    .
end
```

Note that "i" is declared to be an integer, which is defined as a 32-bit value. Because the *for* loop is not unrolled, it builds an adder and a comparator inside the loop to increment the iterator and to check the bounds of the iteration. With a 32-bit iterator, the incrementor and the comparator are built larger than necessary. In the above example, if the "integer i" was replaced with "reg [3:0] i", only a 4-bit adder and incrementor would be built.

Note that if the *for* loop is unrolled (always in regular elaboration, and the default in elaboration for Behavioral Compiler), this problem does not exist. When unrolling the loop, the iterator is treated as a series of constants, and the size of the iterator is irrelevant.

WHAT NEXT

To reduce the size of the arithmetic operators used inside the *for* loop, the size of the iterator can be reduced to the designated value.

Be aware, though, that if the iterator is used in other sections of the code, these other sections may be relying on the larger size of the variable. In such a case, you may want to declare a dedicated variable that will be used only in the *for* loop.

HLS-119 (warning) The iterator '%s' is used in the for loops on lines %s that are not being unrolled. The bit-widths required by the loops (%s) are different, and it might be more efficient to declare separate iteration variables for each for loop.

DESCRIPTION

Consider the following example:

```
reg [9:0] i;
.
.
.
for ( i = 0 ; i < 10 ; i = i + 1 ) begin : for1
    .
    .
    .
end
.
.
.
for ( i = 0 ; i < 1023 ; i = i + 1 ) begin : for2
    .
    .
    .
end
```

The first *for* loop requires only a 4-bit iterator, and the second *for* loop requires a 10-bit iterator. Because the same iterator is used for both loops, however, 10-bit arithmetic operations are built in the first loop.

Note that this is relevant only when elaborating for Behavioral Compiler and when the *for* loops are not unrolled.

WHAT NEXT

Defining a separate iterator for each loop allows the first loop to use 4-bit

arithmetic units. This may create more efficient logic (however, if the registers and arithmetic units are shared between the two loops, it might not really matter).

HLS-120 (error) The for loop on line %d uses the iterator '%s', which is too small to cover the range of the loop. '%s' is defined on line %d with a bit width of %d. The range of the loop is %d to %d, which requires the iterator to have a bit width of at least %d.

DESCRIPTION

Consider the following example:

```
        reg [1:0] i;
        .
        .
        .
        for ( i = 0 ; i < 10 ; i = i + 1 ) begin : for1
            .
            .
            .
        end
```

Note that *i* is declared to be only 2 bits wide, but *i* must be able to store integers as high as 10. The iterator variable *i* must be declared to have at least 4 bits so that it can store all of the possible values of the *for* loop.

A special case is the condition where the range of the *for* loop exactly covers the range of the iterator. Consider the following example:

```
reg [3:0] i;
.
.
.
for ( i = 0 ; i <= 15 ; i = i + 1 ) begin : for1
    .
    .
    .
end
```

At first glance, it appears that the variable *i* has been declared wide enough to cover the range of the *for* loop. A *reg* that is declared [3:0] can represent numbers in the range of 0 to 15.

However, a closer look at the example reveals that the above *for* loop will never terminate. The loop will terminate only when the value of *i* is greater than 15. Because the *reg i* can represent values in the range of only 0 to 15, *i* will never be greater than 15, and the loop will not terminate.

WHAT NEXT

Declare the bit width of the iterator variable to be large enough to store a value of at least 1 + the loop range.

HLS-121 (error) Could not write data file

DESCRIPTION

The data file that is normally passed from the shell to the scheduling process could not be written.

WHAT NEXT

Check the write permissions and the hierarchical structure of the design. You may have loaded a bad design.

HLS-122 (warning) License cannot be recovered

DESCRIPTION

The behavioral license you checked out manually has been lost.

WHAT NEXT

If you need it, you must check it out again manually.

HLS-123 (error) The memory '%s' is being passed in as an argument to routine '%s' at line %d. This is not allowed when elaborating for scheduling.

DESCRIPTION

Users are not allowed to pass whole memories as arguments to functions or procedures.

However, users can access the variable directly inside of the function or procedure. This means that the function must be declared in the scope of the variable that represents the memory. In VHDL, this means declaring the function inside the

declarative region of the process (the same place where variables are defined). In Verilog, this simply means defining the variable and the subprogram at the same level.

WHAT NEXT

Either rewrite the code to access the memory directly (moving the definition of the function to the scope of the variable if necessary) or restructure the code so that the memories are not accessed inside of subprograms.

HLS-124 (warning) The operator '%s' and the module '%s' are connected by more than one sequential binding, one of which is the binding '%s'.

DESCRIPTION

Behavioral Compiler uses the first sequential binding it encounters for a given combination of operator and module. All other bindings are ignored.

WHAT NEXT

Prune the sequential bindings down to a single binding for each operator/module pair, so that you know which binding is being used.

HLS-125 (warning) The check_bindings command cannot verify the sequential binding '%s' of module '%s'

DESCRIPTION

The **check_bindings** command is restricted to combinational bindings. The aforementioned sequential binding will be skipped.

WHAT NEXT

Sequential bindings must be checked manually.

HLS-126 (Warning) Cannot merge output registers of multi-

cycle operations.

DESCRIPTION

Multicycle operations are resource-shared, but their outputs fan out to more than one register. This condition may lead to long compile times because of the high numbers of multicycle timing constraints required.

WHAT NEXT

HLS-127 (Warning) Edge %s may be driven by operations of different cycle delays

DESCRIPTION

An edge may be driven by several operations because of conditional assignments. If these operations have different cycle delays, different multicycle timing paths may be created from one register to another. This situation adversely affects the quality of results for logic synthesis.

WHAT NEXT

HLS-128 (Warning) Loop %s has no exit Operations and/or transfers following it are dead code and will be pruned.

DESCRIPTION

In the design, there is a loop that has "no exit." And there is code after the loop. This dead code cannot be executed, and it will be pruned from the design.

WHAT NEXT

Check the source HDL: the named loop has "no exit" but still has code after it.

HLS-129 (Warning) Post-scheduling uniquify failed

DESCRIPTION

Automatic uniquification after scheduling failed. The design must be uniquified manually before **compile**.

WHAT NEXT

HLS-130 (error) The process%s at line %d does not contain any wait statements. Behavioral Compiler requires that each process being elaborated for scheduling have at least one wait statement. This is necessary to determine the clock and clock edge to use for the process.

DESCRIPTION

Behavioral Compiler requires that every process being run through behavioral synthesis have at least one wait statement.

WHAT NEXT

Add a wait statement to the process.

HLS-131 (error) The always block%s at line %d does not contain any posedge or negedge statements. Behavioral Compiler requires that each always block being elaborated for scheduling have at least one edge statement. This is necessary to determine

the clock and clock edge to use for the block.

DESCRIPTION

Behavioral Compiler requires that every **always** block being run through behavioral synthesis have at least one *posedge* or *negedge* statement.

WHAT NEXT

Add a *posedge* or *negedge* statement to the process.

HLS-132 (error) The process%s at line %d contains waits that check
both positive edges and negative edges of clocks. The wait at line %d checks the positive edge of the clock, and the wait at line %d checks the negative edge. Checking both edges is not
supported.

DESCRIPTION

A process is allowed to check only one edge of the clock.

WHAT NEXT

Change all of the "waits" to check either the positive or negative edge of the clock.

HLS-133 (error) The always block%s at line %d contains both posedge and negedge declarations. There is a posedge declaration at line %d and a negedge declaration at line %d. It is illegal to check both edges of a clock within a single

always block.

DESCRIPTION

An **always** block is allowed to check one edge of the clock.

WHAT NEXT

Change all of the edge declarations to be either all *posedge* or all *negedge*.

HLS-134 (error) Design has not been timed for Behavioral Compiler

DESCRIPTION

The design has not been timed for Behavioral Compiler. Delay estimates, chaining delay estimates, and area costs are not available.

WHAT NEXT

Make certain that the design was elaborated with the *-schedule* switch and then perform the command **bc_time_design**.

HLS-135 (Error) Clock period is too small for operation '%s' which requires a minimum clock period of '%f'.

DESCRIPTION

The clock period is too small for the internal delay of a sequential operation.

WHAT NEXT

HLS-136 (information) The clock transitions being checked at lines
%d and %d are different. No synchronous reset will be inferred

for the %s at line %d.

DESCRIPTION

Behavioral Compiler infers a synchronous reset only if all clock transitions in a process are identical.

WHAT NEXT

If a synchronous reset is desired, check the clock transitions to ensure they are compatible.

HLS-137 (information) The clock transition at line %d is not followed by an if statement. No synchronous reset will be inferred for the %s at line %d.

DESCRIPTION

To infer a synchronous reset, every single clock transition must be followed by a condition that checks the reset condition and exits the block if the condition is true. The clock transition mentioned in the message is not followed by a condition.

WHAT NEXT

If an inferred synchronous reset is desired, add a check for the reset condition after the specified clock transition.

HLS-138 (information) The clock transition at line %d is followed by an if statement, but the contents of the if block is not a single exit statement. In order to infer a synchronous reset, the if block can only contain a single statement that exits from the block. No synchronous reset will be inferred for the %s at line %d.

DESCRIPTION

The contents of an *if* statement that is an inferred synchronous reset can only be a

single statement that terminates the entire **process** or **always** block (exit statement in VHDL and disable statement in Verilog).

WHAT NEXT

Check the *if* statement that follows the defined clock transition. If a synchronous reset is desired, make sure that the content of the *if* statement is simply an exit from the entire block.

HLS-139 (information) The clock transition at line %d is followed by an if statement with a single exit statement, but the exit statement does not reset the entire block (process in VHDL, always block in verilog). No synchronous reset will be inferred for the %s at line %d.

DESCRIPTION

The contents of an *if* statement that is an inferred synchronous reset can only be a statement that terminates the entire **process** block or **always** block (exit statement in VHDL and disable statement in Verilog).

WHAT NEXT

Check the *if* statement that follows the defined clock transition. If a synchronous reset is desired, make sure that the content of the *if* statement is simply an exit from the entire block.

HLS-140 (information) The clock transitions at lines %d and %d are both followed by a conditional that exits the main block. However, the conditions for the two exits are different. No synchronous reset

will be inferred for the %s at line %d.

DESCRIPTION

For a synchronous reset to be inferred, all of the conditions on the conditional **exits** that follow clock transitions must be identical.

WHAT NEXT

If a synchronous reset is desired, check the conditions following the two mentioned *wait* statements. The conditions need to be identical.

HLS-141 (error) The chain_operations and dont_chain_operations commands require two or more operations as arguments.

DESCRIPTION

Chaining is the process of scheduling multiple operations in the same cycle. Therefore, more than one operation must be defined.

WHAT NEXT

Define two or more operations for this command.

HLS-142 (information) The clock transition at line %d is followed by an if statement, but the if statement has multiple branches. In order to infer a synchronous reset, the if statement can only contain a single branch with a statement that exits from the block. No synchronous reset will be inferred for the %s at line %d.

DESCRIPTION

The contents of an *if* statement that is an inferred synchronous reset can be only a single branch with a statement that terminates the entire **process** block and **always** block (*exit* statement in VHDL and *disable* statement in Verilog).

WHAT NEXT

If a synchronous reset is desired, make sure that the *if* clause that follows the clock transition has only a single branch.

HLS-143 (error) The variable ’%s’ was attributed as being a %s in resource %s on line %d. However, the variable is not defined in the process at line %d. If it is not a shared memory the variable should be defined, and if it is a shared memory it should set "bc_allow_shared_memories = true".

DESCRIPTION

The variables that are defined in a memory (or registerfile) specification must be defined in the same process as the resource that specified the memory (or registerfile). The only exception is a memory shared by processes, in which "bc_allow_shared_memories" should be set "true".

WHAT NEXT

Check that the resource was defined properly or "bc_allow_shared_emmories" was set to "true". If it was, make sure that the corresponding variable is defined in the process or "bc_allow_shared_memories" is set to "true".

HLS-144 (error) The variable ’%s’ was attributed as being a %s in resource %s on line %d. However, the variable is not defined in the scope of the always block at line %d.

DESCRIPTION

The variables that are specified in a memory (or registerfile) specification must be defined in the same always block as the resource that specified the memory (or registerfile). Memories are not allowed to span accross multiple always blocks, so the variable definition must be given inside the scope of the always block.

WHAT NEXT

Check that the resource was defined properly. If it was, make sure that the corresponding variable is defined inside of the always block.

HLS-145 (error) Multiple operations have been defined as an endpoint for a timing offset

DESCRIPTION

Only one operation can be identified as an endpoint of the timing offset.

WHAT NEXT

Do not specify more than one operation as an endpoint for a timing offset.

HLS-146 (error) The for loop at line %d contains the loop at line %d and the for loop is being unrolled. For loops are not allowed to contain other loops if they are being unrolled.

DESCRIPTION

A *for* loop that is being unrolled is not allowed to contain other loops (with the exception of other *for* loops that are being unrolled).

WHAT NEXT

Either remove the loop from inside the *for* loop or mark the *for* loop as being "dont_unroll"ed (done with the *dont_unroll* attribute in VHDL and with the *dont_unroll* field of a resource in Verilog).

HLS-147 (error) The command '%s' is only valid on designs that have been elaborated for scheduling, but have not been scheduled yet. The design '%s' is not valid.

DESCRIPTION

This command operates only on designs that have been elaborated for scheduling.

WHAT NEXT

Make sure the design being passed in to this command has been elaborated for scheduling.

HLS-148 (error) The command '%s' is not valid on designs that have been elaborated for scheduling and have not been scheduled yet. The design '%s' is not valid.

DESCRIPTION

This command does not work on designs that have not been scheduled yet.

WHAT NEXT

Schedule the design before trying to use this command.

HLS-149 (Error) Found scheduling template containing resource contention.

DESCRIPTION

WHAT NEXT

HLS-150 (error) Loop '%s' cannot be loop-pipelined because

the branches of the conditional at line %s are unbalanced.

DESCRIPTION

WHAT NEXT

HLS-151 (error) You cannot chain fewer than two operations

DESCRIPTION

You must give two or more operations as arguments to the **chain** command.

WHAT NEXT

HLS-152 (information) Scheduling '%s' ...

DESCRIPTION

WHAT NEXT

HLS-153 (information) Allocating hardware for '%s' ...

DESCRIPTION

WHAT NEXT

HLS-154 (error) Variable '%s' is not initialized for operation '%s'

DESCRIPTION

The variable specified in the error message is used by the operation before it has been written to or initialized.

WHAT NEXT

Ensure that your behavioral description initializes or writes to the variable before it is used by an operation.

HLS-155 (warning) Variable '%s' is read before being written or initialized. This will cause a simulation-synthesis mismatch.

DESCRIPTION

In your behavioral description a variable is read before being initialized or written to. This will cause unpredictable synthesis results.

The behavior of the synthesized design will not match that of your behavioral description.

If you do not initialize a variable, its initial value will be unknown and a simulation-synthesis mismatch may occur for the first iterations of your design until the variable is written for the first time.

If you rely on the variable value to be preserved after a design reset you will experience a simulation-synthesis mismatch. To avoid this situation the variable has to be written before being read in the same run of the design the read operation happens.

An instance were you can safely ignore this warning message is when you use a rolled loop to initialize your variable - insuficient loop index information may cause false warnings.

WHAT NEXT

Initialize or write to the variable before reading its value. Do not assume the current value of a variable will be preserved upon a design reset.

HLS-156 (Information) Operation %s is activated by gate %s

DESCRIPTION

WHAT NEXT

HLS-157 (warning) Ignoring multi-cycle delay for operation '%s'

DESCRIPTION

When bc_enable_multi_cycle is set to false (The default value is true.), BC is forced to make operations single cycle, even if their propagation delays are greater than the clock period. If BC is forced to treat it as a single cycle operation, the user may have problems meeting timing during compile. Normally, the clock cycle time should be greater than or equal to the sum of operation execution time and the margin (sum of clock_to_Q delay and setup time) to execute the operation in one cycle. If you don't like to have multicycle operations, try to contstrain the synthetic library to force bc_time_design to select a faster component. In addition, use bc_time_design -fatest to use the fastest available implementation for each synthetic operation.

WHAT NEXT

Please set bc_enable_multi_cycle to true if you want to let BC infer multicycle synthetic operations from the propagation delays and clock cycle periods. To change the margin amount, please use bc_margin command.

HLS-158 (warning) Logic group '%s' has propagation delay of '%f',
which is longer than the clock period of '%f'

DESCRIPTION

This warns if logic delay is longer than the real clock period. The real clock period is defined as: the original period - the margin. The margin is the sum of the clk_to_Q delay and setup time. You may change the margin by using bc_margin command.

WHAT NEXT

When bc_enable_multi_cycle is set to true, BC will infer multicycle operations when the progation delay is greater than the real period. To force bc_time_design to use the fastest available implementation available in the library, please use

"bc_time_design -fastest".

HLS-159 (Error) Failed to schedule pipelined loop '%s' under initiation interval of %d and loop delay of %d

DESCRIPTION

WHAT NEXT

HLS-160 (Error) Detected Inconsistent Sequential Bindings. In module '%s', for operator '%s', Binding '%s' has %d states, but binding '%s' has %d states

DESCRIPTION

When there are more than one sequential binding for the same operator and same module, all sequential bindings must have the same number of states, and use the same resources in each corresponding state.

WHAT NEXT

HLS-161 (Error) Detected Inconsistent Sequential Bindings. In module '%s', for operator '%s', State '%d' of binding '%s' uses %d resources, but state '%d' of binding '%s' uses %d resources

DESCRIPTION

When there is more than one sequential binding for the same operator and same module, all sequential bindings must have the same number of states and use the same resources in each corresponding state.

WHAT NEXT

HLS-162 (Error) Detected Inconsistent Sequential Bindings.

In module ’%s’, for operator ’%s’,
State ’%d’ of binding ’%s’ uses resource ’%s’,
but state ’%d’ of binding ’%s’ does not use that resource

DESCRIPTION

When there is more than one sequential binding for the same operator and same module, all of the sequential bindings must have the same number of states and use the same resources in each corresponding state.

WHAT NEXT

HLS-163 (Error) Inconsistent FSM registration flags.

DESCRIPTION

The flag *-none* is incompatible with the flags *-inputs* and *-outputs*.

WHAT NEXT

HLS-164 (Warning) one of the allowed flags must be used.

DESCRIPTION

The flags *-inputs*, *-outputs*, or *-none* must be used.

WHAT NEXT

HLS-165 (error) The %s ’%s’ is accessed globally in subprogram ’%s’
at line %d in file %s.
This is not supported when elaborating for scheduling.

DESCRIPTION

When elaborating for scheduling, an error occurs when a VHDL signal or Verilog

register is accessed globally inside a function or procedure (that is, it is accessed inside the function but is not one of the parameters of the function).

Note that VHDL variables and Verilog reg variables declared inside the scope of the **always** block are legal.

WHAT NEXT

Either remove the access to the signal or reg or pass the signal or reg in as a parameter to the function or procedure.

HLS-166 (warning) The subprogram '%s' contains a %s statement at line %d in file %s. No synchronous reset will be inferred.

DESCRIPTION

If a clock transition is checked within a subprogram, there is no way to reset the design when the reset signal is set. Thus, if a clock transition is checked inside of a subprogram, no synchronous reset will be inferred.

WHAT NEXT

Either remove the clock transition from inside of the subprogram or remove all checks for the reset signal; and then use the **set_behavioral_reset** command to define the reset signal.

HLS-167 (error) The subprogram '%s' at line %d in file '%s' contains loops. This is not supported when elaborating for scheduling.

DESCRIPTION

The only loop allowed inside a subprogram is an unrolled *for* loop. All other loops are illegal when elaborating for scheduling.

WHAT NEXT

Rewrite your source HDL code so that the subprogram does not contain any illegal loops.

HLS-168 (error) Cannot find legal binding for %s of operator type %s

DESCRIPTION

Allocation failed because the operation cited does not have a legal binding in the synthetic library. Check unconnected inputs and outputs of the operation, which may make certain synthetic bindings illegal for the operation.

WHAT NEXT

HLS-169 (error) It is illegal to use a 'wire' variable inside of an always block. The wire variable '%s' is used as an iterator in a for loop at line %d in file %s.

DESCRIPTION

In Verilog, it is illegal to use a *wire* inside of an **always** block.

WHAT NEXT

Change the *wire* declaration to a reg declaration.

HLS-170 (Error) %s constraint involving '%s' and '%s' is illegal because it crosses levels in the design hierarchy.

DESCRIPTION

With respect to cells, a timing constraint must be placed in the same level of design hierarchy.

WHAT NEXT

HLS-171 (Error) Failed to schedule loop named '%s'

DESCRIPTION

Behavioral Compiler has failed to schedule the named loop because of timing constraint violations. This aborts the scheduling of the rest of the design.

WHAT NEXT

Relax timing constraints for the named loop. Note that implicit timing constraints are created for signal/port reads and writes in super-state io mode.

HLS-172 (error) You cannot specify common resource for fewer than two operations

DESCRIPTION

You must give two or more operations as arguments to the **set_common_resource** command.

WHAT NEXT

Please reissue the **set_common_resource** command using two or more operations as arguments.

HLS-173 (error) You must specify a unique process

DESCRIPTION

The command requires an explicitly named process if more than one schedulable process is present in your design.

WHAT NEXT

Reissue the last command using the **-process** *process* option and argument.

HLS-174 (Warning) Conditional action on reset transition.

DESCRIPTION

There is a conditional action before the first wait of the design. This results in a conditional being executed when the reset pulse forces the design to transition the beginning of the process. However, there is no way to assure that the conditions upon which the conditional depends are valid at the time of the reset; this may result in simulation failures.

WHAT NEXT

Move the conditional(s) to after the first wait of the process.

HLS-175 (Warning) Read operation %s for signal %s is redundant because
the value is not used.

DESCRIPTION

A read operation on a signal or port is identified as redundant because the read value is never used. This situation can arise when the operations that make use of the read values can never be exercised.

WHAT NEXT

If the read operation is really unnecessary in the design, then delete it; otherwise modify the design so that the read values are used.

HLS-176 (Error) Write operation %s for signal %s is redundant because
it is in dead code or the value has not been initialized.

DESCRIPTION

A write operation on a signal or port has been identified as redundant because the written value has not been assigned. This situation can arise because the write operation is in a block of code that is never executed, because of uninitialized variables, or because operations that assign the values are never exercised.

WHAT NEXT

Check the design for the offending write operation, and either delete this write operation, or ensure that values are assigned.

HLS-177 (Warning) Operation %s outputs are not used.

DESCRIPTION

Combinational data path operation outputs are never used. This can happen when certain operations are never exercised, then values consumed by these operations will never get used. Array write operation is an exception.

WHAT NEXT

Check operations that use values produced by the named operation, and make sure that these operations can be exercised.

HLS-178 (Error) Cannot schedule operations %s and %s on a common resource.

DESCRIPTION

The two named operations have inconsistent internal resources and therefore cannot be scheduled on a common resource. This situation arises when **set_common_resource** is used to group combinational operations with sequential operations, or to group sequential operations that cannot be implemented on the same modules.

WHAT NEXT

Change the set_common_resource commands so that sequential operations are grouped only with sequential operations on the same module types.

HLS-179 (error) The always block at line %d contains references to the variable '%s'. This variable is defined as a Behavioral Compiler memory in the always block at line %d. See Behavioral Compiler User Guide to find out how to share

memories between blocks.

DESCRIPTION

Behavioral Compiler supports memories that are shared by different blocks. It is accomplished by setting "bc_allow_shared_memories = true" and specifying the list of address port names to be used in each block by "address_port_name". See Behavioral Compiler User Guide for details.

WHAT NEXT

Modify the design so that the memory is only accessed inside of a single design or use the rule for shared memory feature.

HLS-180 (error) The for loop on line %d uses the iterator '%s' On line %d, the iterator '%s' is redefined. This is currently not supported when elaborating for scheduling.

DESCRIPTION

Consider the following example:

```
for i in a'range loop
    ...
    for i in b'range loop
...
    end loop;
    ...
end loop;
```

If the outer for loop is not unrolled, and the inner for loop uses an iterator with the same name, this will generate an error.

WHAT NEXT

Rename the iterator on one of the two for loops.

HLS-181 (error) Cannot pipeline loop '%s' with initiation interval

%d. A path has a timing path whose length is too long.

DESCRIPTION

This error indicates that Behavioral Compiler is unable to pipeline a loop with the initiation interval specified because a loop-carry dependency (LCD) conflicts with a path within the loop.

We explain this situation in detail with an example below.

In the loop below, assume that the addition operations are multi-cycled operations that require 1 clock cycle to complete and that the operations do not chain.

```
loop_begin
    a :=  v2 + in_j;  -- add_1
    b :=  a  + in_m;  -- add_2
    v2 := v1;         -- carry forward past output of add_2
    v1 := b;          -- carry forward current output of add_2
loop_end
```

Furthermore, assume that you have set a "set_min_cycles 3" constraint from add_1 to add_2.

```
If:
    x = clock cycle at which add_1 is scheduled and
    y = clock cycle at which add_2 is scheduled,
then,
    y - x >= min_delay, or
    y     >= min_delay + x            --- (Equation 1)
```

Now consider loop pipelining. If the loop is pipelined with initiation interval of 1 clock cycle, successive iterations are launched every clock cycle and overlap as shown in the figure below:

```
 iteration 1     iteration 2    iteration 3
 ------------------------------------------
 add_1
 .               add_1
 .               .              add_1
 add_2           .              .
                 add_2          .
                                add_2
```

A loop-carry dependency (LCD) occurs when data generated by an operation in a loop iteration is used by an operation in one of the succeeding loop iterations.

In our example, this occurs since the add_2 operation in iteration 1 produces data that is carried forward two iterations using the variables v1 and v2 and is eventually used by the add_1 operation in iteration 3.

Clearly, add_2 of iteration 1 must complete prior to the clock cycle in which add_1 of iteration 3 is executed for the data dependency to be met. This is an LCD constraint.

If:

```
    delay(add_2) = execution time for add_2
    #iter        = number of iterations between
                   producer add_2 (iteration 1) and
                   consumer add_1 (iteration 3)
    ii           = initiation interval in clock cycles,
```

then, the LCD constraint specifies:

```
    (completion cycle of producer) <= (start cycle of consumer)
```

which can be expressed as:

```
    y + delay(add_2) <= (#iter * ii) + x
    y                <= (#iter * ii) + x - delay(add_2)   --- (Equation 2)
```

Combining Equation 1 and Equation 2, we get:

```
    (min_delay + x)  <=  y  <=  (#iter * ii) + x - delay(add_2)
```

For this to be consistent, we need:

```
    min_delay + x  <=  (#iter * ii) - delay(add_2) + x
    min_delay      <=  (#iter * ii) - delay(add_2)        --- (Equation 3)
```

In our example,

```
    #iter        = 2
    ii           = 1
    delay(add_2) = 1

    (#iter * ii) - delay(add_2) = 1
    min_delay                   = 3
```

This does not satisfy Equation 3. Behavioral Compiler complains of an LCD violation and generates a report which elaborates on the path, operations, and delays that are causing the error.

WHAT NEXT

From Equation 3 above, the LCD can be met if:

```
    min_delay  <=  (#iter * ii) - delay(add_2)
```

Recommended fix:

- Increase ii, the initiation interval to 2.

Other possible fixes are:

(i) Use a different component for add_2, if delay(add_2) is large.

(ii) Reduce the minimum delay between add_1 and add_2 from 3 to 1, by eliminating

unnecessary paths (dependencies) within an iteration on the loop.

HLS-182 (error) Loop '%s' cannot be loop-pipelined with initiation interval %d because '%s' will occur after '%s' of the next iteration There is a minimum timing constraint of %d cycles from %s to %s. Try changing initiation interval to %d.

DESCRIPTION

In loop pipelining, for each signal/port, Behavioral Compiler requires that read's in one iteration happen before writes in the next iteration, and that writes in one iteration happen 1 cycle before read and writes in the next iteration.

WHAT NEXT

Increase initiation interval.

HLS-183 (error) Loop '%s' cannot be loop-pipelined with initiation interval %d because memory read/write on %s will be permuted. '%s' may occur at the same time or after '%s' of the next iteration since there is a minimum timing constraint of %d cycles from %s to %s. Try changing initiation interval to %d.

DESCRIPTION

In loop pipelining, for each RAM, Behavioral Compiler requires that memory read and writes in one iteration happen 1 cycle before memory writes in the next iteration, and that memory writes in one iteration happen 1 cycle before memory reads in the next iteration.

WHAT NEXT

Increase initiation interval.

HLS-184 (error) Loop ’%s’ cannot be loop-pipelined with initiation interval %d
because operation ’%s’ has a delay of %d cycles.
Try changing initiation interval to %d.

DESCRIPTION

In loop pipelining, each operation is repeatedly executed at the rate of the initiation interval. For multi-cycle operations, Behavioral Compiler requires that its cycle delay be less than or equal to the initiation interval.

WHAT NEXT

Increase initiation interval.

HLS-185 (error) Loop ’%s’ cannot be loop-pipelined with initiation interval %d
because operation ’%s’ uses sequential binding ’%s’ where state %d and %d
both use internal resource ’%s’.
Try increasing initiation interval.

DESCRIPTION

In loop pipelining, each operation is repeatedly executed at the rate of the initiation interval. For sequential operations that reserve internal resources in different states, Behavioral Compiler requires that the initiation interval not cause conflicts on the internal resources.

WHAT NEXT

Increase initiation interval.

HLS-186 (error) Cannot pipeline loop ’%s’ with initiation interval

%d. A path has a minimum length that is too long.

DESCRIPTION

This error indicates that Behavioral Compiler is unable to pipeline a loop with the initiation interval specified because a loop-carry dependency (LCD) conflicts with a path within the loop.

We explain this situation in detail with an example below.

Let us consider a loop with 4 add operations and let us assume each add operation needs its own clock cycles. The add operations in the loop below are executed in successive clock cycles.

```
loop_begin
    a :=  v2 + in_j;  -- add_1
    b :=  a  + in_k;  -- add_2
    c :=  b  + in_l;  -- add_3
    d :=  c  + in_m;  -- add_4
    v2 := v1;         -- carry forward past output of add_4
    v1 := d;          -- carry forward current output of add_4
loop_end
```

As we can see, the path from add_1 to add_4, via add_2 and add_3, requires at least 3 cycles between add_1 and add_4.

```
If:
    x = clock cycle at which add_1 is scheduled and
    y = clock cycle at which add_4 is scheduled,
then,
    y - x >= min_delay, or
    y     >= min_delay + x            --- (Equation 1)
```

Now consider loop pipelining. If the loop is pipelined with initiation interval of 1 clock cycle, successive iterations are launched every clock cycle and overlap as shown in the figure below:

```
 iteration 1     iteration 2    iteration 3
 ------------------------------------------
 add_1
 add_2           add_1
 add_3           add_2          add_1
 add_4           add_3          add_2
                 add_4          add_3
                                add_4
```

A loop-carry dependency (LCD) occurs when data generated by an operation in a loop iteration is used by an operation in one of the succeeding loop iterations.

In our example, this occurs since the add_4 operation in iteration 1 produces data that is carried forward two iterations using the variables v1 and v2 and is eventually used by the add_1 operation in iteration 3.

Clearly, add_4 of iteration 1 must complete prior to the clock cycle in which add_1 of iteration 3 is executed for the data dependency to be met. This is an LCD constraint.

If:

```
    delay(add_4) = execution time for add_4
    #iter        = number of iterations between
                   producer add_4 (iteration 1) and
                   consumer add_1 (iteration 3)
    ii           = initiation interval in clock cycles,
```

then, the LCD constraint specifies:

```
    (completion cycle of producer) <= (start cycle of consumer)
```

which can be expressed as:

```
    y + delay(add_4) <= (#iter * ii) + x
    y                <= (#iter * ii) + x - delay(add_4)   --- (Equation 2)
```

Combining Equation 1 and Equation 2, we get:

```
    (min_delay + x)  <=  y  <=  (#iter * ii) + x - delay(add_4)
```

For this to be consistent, we need:

```
    min_delay + x  <=  (#iter * ii) - delay(add_4) + x
    min_delay      <=  (#iter * ii) - delay(add_4)        --- (Equation 3)
```

In our example,

```
    #iter        = 2
    ii           = 1
    delay(add_4) = 1

    (#iter * ii) - delay(add_4) = 1
    min_delay                   = 3
```

This does not satisfy Equation 3. Behavioral Compiler complains of an LCD violation and generates a report which elaborates on the path, operations, and delays that are causing the error.

WHAT NEXT

From Equation 3 above, the LCD can be met if:

```
    min_delay  <=  (#iter * ii) - delay(add_4)
```

Recommended fix:

- Increase ii, the initiation interval to 2.

Other possible fixes are:

(i) Use a different component for add_4, if delay(add_4) is large.

(ii) Reduce the minimum delay between add_1 and add_4 from 3 to 1, by eliminating unnecessary paths (dependencies) within an iteration on the loop.

HLS-187 (error) Cannot pipeline loop '%s' with initiation interval %d. A path with fixed nodes has a minimum length that is too long.

DESCRIPTION

This error indicates that Behavioral Compiler is unable to pipeline a loop with the initiation interval specified because a loop-carry dependency (LCD) conflicts with a path within the loop. The path in the loop passes through two nodes that are a fixed distance from one another. There need not be a data-dependency between these two nodes.

We explain this situation in detail with an example below.

Let us use the following loop and, to simplify the explanation, assume: (a) the I/O scheduling mode is cycle fixed, (b) each addition operation requires its own clock cycle, and (c) there is no chaining.

```
loop_begin
    a :=  v2 + j;              -- add_1
    out_a <= a;                -- io_write
    wait/@posedge              -- clock_edge
    b := in_b;                 -- io_read
    d :=  b + k;               -- add_2
    v2 := v1;                  -- carry forward past output of add_2
    v1 := d;                   -- carry forward current output of add_2
loop_end
```

The operations add_1 to add_2 have no data-dependence. However io_write is data-dependent on add_1 and add_2 is data-dependent on io_read. The operations io_write and io_read are fixed 1 clock cycles apart by the semantics of cycle-fixed I/O scheduling mode.

There is a transitive, minimum-delay path from add_1 to add_2 through io_write and io_read of length 3.

```
If:
    x = clock cycle at which add_1 is scheduled and
    y = clock cycle at which add_2 is scheduled,
then,
    y - x >= min_delay, or
    y     >= min_delay + x            --- (Equation 1)
```

Now consider loop pipelining. If the loop is pipelined with initiation interval of 1 clock cycle, successive iterations are launched every clock cycle and overlap as

shown in the figure below:

```
 iteration 1     iteration 2    iteration 3
 ------------------------------------------
 add_1
 io_write        add_1
 io_read         io_write       add_1
 add_2           io_read        io_write
                 add_2          io_read
                                add_2
```

A loop-carry dependency (LCD) occurs when data generated by an operation in a loop iteration is used by an operation in one of the succeeding loop iterations.

In our example, this occurs since the add_2 operation in iteration 1 produces data that is carried forward two iterations using the variables v1 and v2 and is eventually used by the add_1 operation in iteration 3.

Clearly, add_2 of iteration 1 must complete prior to the clock cycle in which add_1 of iteration 3 is executed for the data dependency to be met. This is an LCD constraint.

If:

```
    delay(add_2) = execution time for add_2
    #iter        = number of iterations between
                   producer add_2 (iteration 1) and
                   consumer add_1 (iteration 3)
    ii           = initiation interval in clock cycles,
```

then, the LCD constraint specifies:

```
    (completion cycle of producer) <= (start cycle of consumer)
```

which can be expressed as:

```
    y + delay(add_2) <= (#iter * ii) + x
    y                <= (#iter * ii) + x - delay(add_2)   --- (Equation 2)
```

Combining Equation 1 and Equation 2, we get:

```
    (min_delay + x)  <=  y  <=  (#iter * ii) + x - delay(add_2)
```

For this to be consistent, we need:

```
    min_delay + x  <=  (#iter * ii) - delay(add_2) + x
    min_delay      <=  (#iter * ii) - delay(add_2)        --- (Equation 3)
```

In our example,

```
    #iter        = 2
    ii           = 1
    delay(add_2) = 1

    (#iter * ii) - delay(add_2) = 1
```

```
    min_delay                   = 3
```

This does not satisfy Equation 3. Behavioral Compiler complains of an LCD violation and generates a report which elaborates on the path, operations, and delays that are causing the error.

WHAT NEXT

From Equation 3 above, the LCD can be met if:

```
    min_delay  <=  (#iter * ii) - delay(add_2)
```

Recommended fix:

- Increase ii, the initiation interval to 2.

Other possible fixes are:

(i) Use a different component for add_2, if delay(add_2) is large.

(ii) Reduce the minimum delay between add_1 and add_2 from 3 to 1, by eliminating unnecessary paths (dependencies) within an iteration on the loop.

HLS-188 (error) Unable to find scheduling data in FSM-style format.

DESCRIPTION

This message indicates that the **db** file you have loaded does not have the correct annotations for FSM-style reporting of schedule information, perhaps because an early software version was used. With versions earlier than v3.3b, **schedule** was not set up to annotate files for FSM-style reporting.

WHAT NEXT

To annotate the file with FSM information, re-execute **schedule** using v3.3b or a later version. However, even without the annotations, you can still use **report_schedule -variables** and report_schedule -operations.

HLS-189 (information) Register ’%s’ will be inferred as multibit module.

DESCRIPTION

During compile, the register will be inferred as multibit module.

WHAT NEXT

To trun off this property, set **bc_infer_multibit** to *false* or set **bc_minimum_multibit_componet_width** to a larger one.

HLS-190 (error) No multiplexors in the standard synthetic library.

DESCRIPTION

There is no multiplexor in the standard synthetic library. This is necessary to calculate the area costs for behavioral synthesis.

WHAT NEXT

Since this multiplexor description should be in the standard synthetic library, this error is most likely due to an improper installation of the Synopsys tools. Please contact your system administrator.

HLS-191 (information) Binding '%s' to '%s' for timing.

DESCRIPTION

WHAT NEXT

HLS-192 (information) Selected '%s' to implement '%s'.

DESCRIPTION

WHAT NEXT

HLS-193 (information) Using wordlevel timing to calculate

chaining of ’%s’.

DESCRIPTION

WHAT NEXT

HLS-195 (error) Loop %s cannot be loop-pipelined with initiation interval %d
because the memory operation ’%s’ must be no later than %d cycles after the operation ’%s’. This implies a minimum delay of %d
cycles from %s to %s. However, this violates the timing constraint of

DESCRIPTION

WHAT NEXT

HLS-196 (error) Loop %s cannot be loop-pipelined with initiation interval %d
because the memory operation ’%s’ must be no later than %d cycles after the operation ’%s’.
This implies a minimum delay of %d cycles from %s to %s
However, this is unsatisfiable because %s

is fixed at cycle %d, and %s is fixed at cycle %d.

DESCRIPTION

WHAT NEXT

HLS-197 (error) Loop %s cannot be loop-pipelined with initiation interval %d
because the signal read/write operation ’%s’ must be no later than %d
cycles after ’%s’. This implies a minimum delay of %d
cycles from %s to %s. However, this violates the timing constraint of

DESCRIPTION

WHAT NEXT

HLS-198 (error) Loop %s cannot be loop-pipelined with initiation interval %d
because the signal read/write operation ’%s’ must be no later than %d cycles
after ’%s’. This implies a minimum delay of %d
cycles from %s to %s. However, this is unsatisfiable because %s

is fixed at cycle %d, and %s is fixed at cycle %d.

DESCRIPTION

WHAT NEXT

HLS-199 (error) Speculative execution must be either true or false

DESCRIPTION

The variable "enable_speculative_execution" must have the value "true" or "false" in order to be correctly interpreted.

WHAT NEXT

Set it to "true" or "false". The default setting is "true".

HLS-200 (error) State chaining must be either true or false

DESCRIPTION

The variable "enable_state_transition_chaining" must have the value "true" or "false" in order to be correctly interpreted.

WHAT NEXT

Set it to "true" or "false". The default setting is "true".

HLS-201 (error) BC FSM coding style is not in the valid set

DESCRIPTION

The valid options are "one_hot_coding", "two_hot_coding", "counter_based", and "use_fsm_compiler". The default is "two_hot_coding".

WHAT NEXT

Set the desired coding style. Notice that the option "use_fsm_compiler" results in a minimum-length state assignment; notice also that this is incompatible with state transition chaining.

HLS-202 (error) FSM compiler and state transition chaining are incompatible

DESCRIPTION

The use of FSM compiler to generate a state coding is not compatible with the use of state transition chaining.

WHAT NEXT

Either choose an alternative state coding or disable state transition chaining. Set the alternative coding using the variable "bc_fsm_coding_style"; disable state transition chaining using the variable "enable_state_transition_chaining".

HLS-203 (error) Unable to create attributes for BC

DESCRIPTION

This is an internal error. Attributes necessary for running Behavioral Compiler cannot successfully be created.

WHAT NEXT

Reanalyze and reelaborate the design. That should take care of it.

HLS-204 (error) No reference for memory cell

DESCRIPTION

The cell has no reference.

WHAT NEXT

Check your synthetic libraries and link the design.

HLS-205 (error) Cannot use the memory master as a cell

DESCRIPTION

The cell you have named is the memory master. It is needed for internal purposes but it is not subject to being constrained.

WHAT NEXT

Find the memory read operation or memory write operation you want using find -h cell.

HLS-206 (error) Not a memory cell

DESCRIPTION

The ignore_precedence commands only work on memory read and write operations.

WHAT NEXT

The ignore_precedence commands only work on memory read and write operations. Check the names of the operations and reissue the command, if you want to ignore the constraints of memory operations. If you want to eliminate constraints on other kinds of operations, you must change your source code to eliminate constraints of data and control precedence.

HLS-207 (error) Fixed schedule (%s at cstep %d) produces a state transition cycle
 at loop begin named %s

DESCRIPTION

A combinational cycle around the named loop begin is created by the fixed schedule

WHAT NEXT

HLS-208 (error) The named stall pin does not exist.

DESCRIPTION

The net you designated as the stall pin does not exist or it is invisible in the current context.

WHAT NEXT

If you are not at the top of the design hierarchy, the net is probably not visible. Otherwise, the net you have named does not exist. Perhaps the name of the net inside the compiler is not the same as the name you gave it. To see what nets are visible, use **find net**.

HLS-209 (Warning) There already exists a timing constraint between these two operations. The new timing constraint will be applied and replace the old one.

DESCRIPTION

There is already a timing constraint between the two operations you specified. The old constraint will be removed and the new one applied in its place.

WHAT NEXT

This is a warning. No further action is needed.

HLS-210 (information) To enable this feature, you may also use a Behavioral Compiler license (BC-VHDL, BC-HDL).

DESCRIPTION

The feature reported to be not available in the previous error message can also be enabled by using one of the Behavioral Compiler licenses: BC-VHDL or BC-HDL.

WHAT NEXT

If you want to use a Behavioral Compiler license to enable the feature, call **get_license** BC-HDL or **get_license** BC-VHDL.

HLS-211 (error) Inappropriate reporting data for condition reporting

DESCRIPTION

The DB file is either generated by an old version of scheduling or is not the result of scheduling.

WHAT NEXT

The conditional branch information may be retrievable if you set the dc-shell variable bc_fsm_coding_style to "use_fsm_compiler". To do this successfully you will also have to turn off state transition chaining by setting the variable enable_state_transition_chaining to "false".

HLS-212 (error) Compilation of user defined Design Ware parts failed.

DESCRIPTION

WHAT NEXT

HLS-213 (error) Unconditional loop exit at line %s is not allowed.

DESCRIPTION

All exit statements in a loop must have conditions under which they exit. Otherwise, it causes a problem when the exit and loop_continue are scheduled in the same control step for execution.

WHAT NEXT

If there is an exit statement in a loop, it occurs only when its exit condition is true; An unconditional exit is not allowed in the middle of loop.

HLS-214 (Information) Determine default margin.

DESCRIPTION

When bc_estimate_timing_effort is set to high, during bc_time_design the default margin will be determined if margin is not set yet. This default margin will be used during schedule.

WHAT NEXT

If user want to set the margin, user can call the command "bc_margin". If user does not want to set the margin at all, set bc_estimate_timing_effort medium/low/zero.

HLS-215 (information) Delete variable '%s' in process '%s'.

DESCRIPTION

The intermediate variable has been removed. To maintain the variable, use set_exclusive_use command.

WHAT NEXT

This is an information message only. You do not need to take any further action. To find out about how to maintain the variable, please see man page for the set_exclusive_use command.

HLS-216 (information) Set cycle margin to %.2f .

DESCRIPTION

Set cycle margin. The margin includes clk2q, setup delay for register, mux (4X1) delay which locates in fron of register, fsm decoding delay as well as clock uncertainty if specified. The margin can be specified through command bc_margin or BC will determine the default margin during bc_time_design.

WHAT NEXT

User can specifiy the margin in various ways using different options. Please see the man page for bc_margin.

HLS-217 (error) Need a Behavioral Compiler license to enable

this feature.

DESCRIPTION

Could not find a license for csa transformation

WHAT NEXT

Make certain that you have a license and that the license is properly installed before trying to use the behavioral synthesis product again.

HLS-218 (error) All Behavioral Compiler licenses are already in use.

DESCRIPTION

The command attempted requies a Behavior Compiler license. All available licenses of this type at your site are currently in use.

WHAT NEXT

Wait until a license of this type at your site is freed.

HLS-219 (warning) The command ’%s’ will be obsoleted in the next release.
Please use the command ’%s’ instead.

DESCRIPTION

The command will be replaced by new command in the next release. In the next release, to get the same behavior, users should replace the command by the new one.

WHAT NEXT

Replace the old command by the new command.

HLS-220 (error) The command ’dont_chain_operations’ has been obsoleted.

Please use the command ’set_min_cycles’ instead.

DESCRIPTION

WHAT NEXT

HLS-221 (error) bc_allocation_effort must be one of ’default’, ’zero’, ’low’, ’medium’, ’high’.

DESCRIPTION

You set the variable **bc_allocation_effort** to an incorrect value. If you set **bc_allocation_effort** to default, allocation will be done using the same effort as defined in the **schedule** command.

WHAT NEXT

HLS-222 (error) bc_bit_level_muxing must be either ’true’ or ’false’.

DESCRIPTION

WHAT NEXT

HLS-223 (error) clock signal ’%s’ drives multi-cycle operation ’%s’.

DESCRIPTION

WHAT NEXT

HLS-224 (error) Error: connection ’%s’ on function ’%s’ is a signal. This is not currently supported when

elaborating for scheduling.

DESCRIPTION

Try to use varialbes instead of signals.

e.g. procedure A(... signal A : std_logic ....) <---- error

procedure A(... varialbe A : std_logic ...) <---- suggested

WHAT NEXT

HLS-225 (error) No address port of shared memory is specified in process '%s';

At least one port of the shared memory is specified.

DESCRIPTION

Address ports of shared memory is specified as Addr_port_i_name, ...

WHAT NEXT

Only the address ports specified are used in the process.

HLS-226 (error) Syntax error in address port specification '%s' of shared memory in process '%s'.

DESCRIPTION

Address ports of shared memory is specified as Addr_port_i_name, ...

WHAT NEXT

Only the address ports specified are used in the process.

HLS-227 (error) The specified address port '%s' of shared

memory ’%s’ in process ’%s’ is not found.

DESCRIPTION

See the .sl file of the shared memory to find all the address port names.

WHAT NEXT

HLS-228 (error) Unable to create attributes for BC

DESCRIPTION

This is an internal error. Attribute BSDB_BC_ALLOW_SHARED_MEMORY_ATTR necessary for running Behavioral Compiler cannot successfully be created.

WHAT NEXT

Reanalyze and reelaborate the design. That should take care of it.

HLS-229 (error) Loop ’%s’ cannot be pipelined with initiation interval of 1
because of the registered controller outputs.

DESCRIPTION

Behavioral Compiler can not pipeline a loop with initiation interval of 1 if the command ’register_control -outputs’ has been called.

WHAT NEXT

Increase the initiation interval to 2 or remove the register_control -outputs command

HLS-230 (Error) Unrecoverd error has occured. This error might be cured via using a different type of fsm compiler. Try set

"bc_use_fsm_compiler = false" in dc_shell and rerun.

DESCRIPTION

This case is not supported in current fsm model. But the other fsm model supports this case.

WHAT NEXT

Set "bc_use_fsm_compiler = false" in dc_shell and run schedule again.

HLS-231 (error) The subprogram '%s' contains a %s statement which fails to preserve the function.

DESCRIPTION

One of the following constructs will fail to preserve function: 1. unrolled loops. 2. memory read operations. 3. memory write operations. 4. signal read opreations. 5. signal write operations. 6. wait statments 7. perserved functions. Example to show all the illegal construncts within functions or procedures(tasks):
try1_loop:while(tmp < 10)loop -- unrolled loop wait until clk'event and clk = '1' ; -- wait statement mem(addr) := "00001111"; -- memory write and signal addr read. -- mem and addr are declared inside of process, -- but not inside of this function. addr := func1(addr); -- illegal if func1 is another preserved function. end loop;

WHAT NEXT

Avoid using the illegal constructs mentioned above for the preserved function.

HLS-232 (information) Checking '%s' ...

DESCRIPTION

WHAT NEXT

HLS-233 (error) The design contains parallel paths where one path is broken
by clock boundaries, and another path is not.

This is not allowed in cycle-fixed mode.
The paths start from the if/case statement on line%s in file %s.
A wait statement is located on line %d in file %s.

DESCRIPTION

WHAT NEXT

Either remove the clock boundaries (wait in VHDL or always @ in verilog) along the parallel paths that contain them, or else insert clock boundaries in the paths where they are missing.

HLS-234 (warning) '%s' can not chain with '%s', chain_operations will be ignored.

DESCRIPTION

You have attempted to use the chain_operations command on operations that cannot be chained together either because they are unrelated or chaining them in the same clock cycle will violate the clock period constraints. You can specify chaining only for operations in the same execution sequence that have data flow dependencies among them. If the operations are related, it may still not be possible to chain them into the same clock cycle as the total delay thorough them is greater than the specified clock period.

WHAT NEXT

If you want to specify constraints between unrelated operations use the set_min_cycles, set_max_cycles or the set_cycles commands instead. If the operations are related and you see this warning increase the clock period or use components with less delay(s) by using the bc_time_design -fastest command.

HLS-235 (error) The output of operation '%s', which has the attribute "carry_port_name", is connected to another operation. This violates the rule that all outputs of the operation must be

connected to an output port on the design.

DESCRIPTION

When we want to generate a csa tree without a final adder in "transform_csa", we need to set the attribute "carry_port_name" with the specified port name on the root (add/sub/mult) operation of original expression. It is assumed that before the transformation, the outputs of the root operation are connected to one port on the design, and the specified carry port is driven by logic zero.

An example of a legal expression looks like (in vhdl):

```
sum <= A + B + C * B; -- 'sum' and 'carry' are ports on the design  carry <=
"00000000";
```

An example of setting the attribute is:

```
set_attribute add_363 "carry_port_name" "carry" -type string
```

NOTE: This transformation assumes that the "sum/carry" ports on the design are only used by the parent design by adding them together. Any other use of these ports may result in incorrect logic.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-236 (error) The output of operation '%s', which has the attribute "carry_port_name", has multiple fan-out. This violates the rule that all outputs of the operation must be connected to the same port on the design.

DESCRIPTION

When we want to generate a csa tree without a final adder in "transform_csa", we need to set the attribute "carry_port_name" with the specified port name on the root (add/sub/mult) operation of original expression. It is assumed that before the transformation, the outputs of the root operation are connected to one port on the design, and the specified carry port is driven by logic zero.

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"00000000";
```

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```
set_attribute add_363 "carry_port_name" "carry" -type string
```

NOTE: This transformation assumes that the "sum/carry" ports on the design are only used by the parent design by adding them together. Any other use of these ports may result in incorrect logic.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-237 (error) The operation '%s' has a "carry_port_name" attribute referencing port '%s'. This port is not driven by logic zero which is required in order to use the "carry_port_name" attribute.

DESCRIPTION

When we want to generate a csa tree without a final adder in "transform_csa", we need to set the attribute "carry_port_name" with the specified port name on the root (add/sub/mult) operation of original expression. It is assumed that before the transformation, the outputs of the root operation are connected to one port on the design, and the specified carry port is driven by logic zero.

An example of a legal expression looks like (in vhdl):

```
sum <= A + B + C * B; -- 'sum' and 'carry' are ports on the design  carry <=
"00000000";
```

An example of setting the attribute is:

```
set_attribute add_363 "carry_port_name" "carry" -type string
```

NOTE: This transformation assumes that the "sum/carry" ports on the design are only used by the parent design by adding them together. Any other use of these ports may result in incorrect logic.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-238 (error) Could not find operations CSA_UNS_OP and CSA_TC_OP.
This is probably because the synthetic library dw01.sldb is missing from
the synthetic_library variable specification.

DESCRIPTION

The transform_csa command needs to be able to find the synthetic operations "CSA_UNS_OP" and "CSA_TC_OP" in the libraries specified by the synthetic_library variable.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-239 (error) Could not find operations MULT2_UNS_OP and MULT2_TC_OP.
This is probably because the synthetic library dw02.sldb is missing from
the synthetic_library variable specification.

DESCRIPTION

The transform_csa command needs to be able to find the synthetic operations "MULT2_UNS_OP" and "MULT2_TC_OP" in the libraries specified by the synthetic_library variable.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-240 (error) Cell '%s' is part of multiple resource constraints.

DESCRIPTION

If you use the **set_common_resource** command, you have to make sure that you bind every cell to only one resource.

WHAT NEXT

Review the set_common_resource constraints that you have applied to the design and remove constraints that apply to more than one cells.

HLS-241 (error) Forcing the operations '%s' to share resources created a false combinational loop.

DESCRIPTION

If you use the **set_common_resource** command, you have to make sure that you do not force the creation of a false combinational loop. This can happen, e.g. if the operations of two different chains are forced to share resources. Consider the following example, where i1 and i2 are input ports, o1 and o2 are output ports:

```
wait until clk'event and clk = '1'; o1 <= (i1 + a) * b; wait until clk'event and clk = '1'; o2 <= c + (i2 * d); wait until clk'event and clk = '1';
```

If the multiplications are forced to be executed on resorce MULT and the additions are forced to share the adder ADD, there is a path ADD -> MULT -> ADD with no register in between.

WHAT NEXT

HLS-242 (Error) Forcing the operations '%s' and '%s' to share resources would result in a false path that is longer than the cycle time.

DESCRIPTION

The application of **set_common_resource** can create a false path that is longer than the clock period. By default, BC will not create such a path.

WHAT NEXT

HLS-243 (warning) Forcing the operations ’%s’ and ’%s’ to share resources will result in a false path that is longer than the cycle time.

DESCRIPTION

WHAT NEXT

HLS-244 (error) The option ’force_sharing’ can only be used in combination with ’max_count’.

DESCRIPTION

WHAT NEXT

HLS-245 (error) The ’allow_false_path’ option can only be used in combination with the ’force_sharing’ option.

DESCRIPTION

WHAT NEXT

HLS-246 (error) ’min_count’ must be less or equal than

’max_count’.

DESCRIPTION

WHAT NEXT

HLS-247 (error) Can not apply set_common_resource to memory access ’%s’.

DESCRIPTION

WHAT NEXT

HLS-248 (error) Variable power_gated_clock_logic has incorrect value.

DESCRIPTION

The variable power_gated_clock_logic may only have specific values (see manual/ specification) which must fit to the argument of the set_clock_gate command.

WHAT NEXT

HLS-249 (error) Variable power_test_enable has incorrect value.

DESCRIPTION

The variable power_test_enable must be either ’true’ or ’false’.

WHAT NEXT

Set the variable to have the correct value.

HLS-250 (error) Variable power_test_obs_logic has incorrect value.

DESCRIPTION

The variable power_test_obs_logic must be either ’true’ or ’false’.

WHAT NEXT

Set the variable to have the correct value.

HLS-251 (error) Variable power_test_obs_logic_depth has incorrect value.

DESCRIPTION

The variable power_test_obs_logic_depth must have a value greater than 0.

WHAT NEXT

Set the variable to have the correct value.

HLS-252 (error) Variable power_reg_size_threshold has incorrect value.

DESCRIPTION

The variable power_reg_size_threshold must have a value greater than 0.

WHAT NEXT

Set the variable to have the correct value.

HLS-253 (error) Reg ’%s’ was assigned in a blocking assignment in
other process but was read using the continue assignment at

line ’%d’.

DESCRIPTION

Behavioral synthesis requires that the transitions of all ports be synchronized to clock boundaries. As a result, the RTL assignment operator must be used to assign to ports.

WHAT NEXT

Use reg declaration and non-blocking assignment.

HLS-254 (information) Operations ’%s’ and ’%s’ were not merged into CSA operations because of upper-bit truncation between them.

DESCRIPTION

When a addition/subtraction/multiplication tree is transformed into a CSA tree, the intermediate values of the original tree do not exist in the transformed tree. As a result, if there is a truncation being performed in the tree, the same truncation would not be able to be performed in the CSA tree. Since transform_csa will not alter the bit-accurate behavior of the design, the truncation blocks the transformation.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-255 (information) Operations ’%s’ and ’%s’ were not merged into CSA operations because of upper-bit or lower-bit truncation between them.

DESCRIPTION

When a addition/subtraction/multiplication tree is transformed into a CSA tree, the intermediate values of the original tree do not exist in the transformed tree. As a

result, if there is a truncation being performed in the tree, the same truncation would not be able to be performed in the CSA tree. Since transform_csa will not alter the bit-accurate behavior of the design, the truncation blocks the transformation.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-256 (information) Operation '%s' has multiple fan-out. It was duplicated creating upto %d extra operation(s) to allow the CSA transformation to be performed.%s

DESCRIPTION

The operation has multiple fan-out. In order to transform the operation with its successor(s) into CSA operations, the operation needs to be duplicated, which causes extra CSA operation(s). This may increase area, but should reduce the delay.

WHAT NEXT

If the transformed tree is not on the critical path, then it may be better not to duplicate the operation. This can be done either by not specifying the -duplicate switch, or by putting a "dont_duplicate_csa" attribute on the operations that should not be duplicated.

HLS-257 (information) Operation '%s' has multiple fan-out and was not duplicated. See the man page for transform_csa to find out how to duplicate the operation to reduce delay at the expense of extra area.%s

DESCRIPTION

The operation has multiple fan-out. In order to transform the operation with its

successor(s) into CSA operations, the operation needs to be duplicated, which causes extra CSA operation(s). This may increase area, but should reduce the delay.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-258 (error) Unable to create attributes for BC

DESCRIPTION

This is an internal error. Attribute BSDB_BC_CONSTRAIN_SIGNAL_MEMORIES_ATTR necessary for running Behavioral Compiler cannot successfully be created.

WHAT NEXT

Report to BC R&D or CAE.

HLS-259 (warning) Command "transform_csa" cannot be applied to the scheduled design ’%s’.

DESCRIPTION

The command can only be applicable to the design which has not been scheduled.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-260 (warning) The timing of design ’%s’ was invalidated by "transform_csa".

DESCRIPTION

The timing of design is invalidated by tramsform_csa if the design was timed and transform_csa transformed the design.

WHAT NEXT

```
The transform_csa command is obsolete. Please use compile_ultra or
set_ultra_optimization instead.
```

HLS-261 (warning) Operation ’%s’ has both of the attributes "transform_csa" and "dont_transform_csa" with "true" values. The attribute "dont_tranaform_csa" is not honored.

DESCRIPTION

```
Becuase "transform_csa" and "dont_transform_csa" with "true" values are conflict, we
choose "transform_csa" to be honored and ignore the other attribute.
```

WHAT NEXT

```
The transform_csa command is obsolete. Please use compile_ultra or
set_ultra_optimization instead.
```

HLS-262 (warning) Operation ’%s’ has both of the attributes "duplicate_csa" and "dont_duplicate_csa" with "true" values. The attribute "dont_tranaform_csa" is not honored.

DESCRIPTION

```
Becuase "duplicate_csa" and "dont_duplicate_csa" with "true" values are conflict, we
choose "duplicate_csa" to be honored and ignore the other attribute.
```

WHAT NEXT

```
Set only one of them to be "true".
```

HLS-263 (error) bc_schedule_branches_asap must be either

’true’ or ’false’.

DESCRIPTION

WHAT NEXT

HLS-264 (error) %s must be either ’true’ or ’false’.

DESCRIPTION

The environment variable mentioned above is a boolean variable. The only values accepted are either ’true’ or ’false’.

WHAT NEXT

Rest the specified variable to have only boolean values.

HLS-265 (warning) There exist a path from ’%s’ to ’%s’ having no timing information.

DESCRIPTION

WHAT NEXT

HLS-266 (information) Memory instance ’%s’ was declared as a shared memory and
was used by processes %s.

DESCRIPTION

The memory instance can be accessed by one or more than one process. This message lists the processes that were detected as using this memory.

WHAT NEXT

This is an information message. No further action is needed.

HLS-267 (information) Memory instance '%s' was declared as a shared memory, but
was used by one process '%s'.

DESCRIPTION

The shared memory can be accessed by one or more than one process. In your design, only one process accesses the memory.

WHAT NEXT

This is an information message. No further action is needed.

HLS-268 (warning) Ports of memory '%s' are not fully utilized.
Mapping of bindings %s requires
%d %s resources, but only %d resources are available.

DESCRIPTION

In order to maximally utilize the ports of memory, the resource counts, which is specified in .sl file, must be increased.

WHAT NEXT

Change the resource count of the resouce in .sl file to the required number.

HLS-269 (error) Detected an inconsisteny among %s bindings in memory module '%s':
For Bindings '%s' and '%s' are pipelined, but their
initiation intervals are different.

DESCRIPTION

For a multi-port memory, the pattern of resource usage for each binding of same access type (read or write) must be uniform. Specifically, All bindings of same access type must be non-pipelined, or all of them can be pipelined, but must have same initiation intervals.

WHAT NEXT

Change the specification of resource use of the states of bindings in .sl file so that the patterns of resource use among the states be uniform.

HLS-270 (error) The node '%s' is part of conflicting timing constraints.

DESCRIPTION

WHAT NEXT

HLS-271 (error) Unable to create attributes for BC

DESCRIPTION

This is an internal error. Attribute BSDB_BC_DETECT_MEMORY_ACCESSES_ATTR necessary for running Behavioral Compiler cannot successfully be created. If "bc_detect_memory_accesses = true", the attribute must be created with true value and included in each (top) process design. Otherwise, the attribute is not created.

WHAT NEXT

Reanalyze and reelaborate the design. That should take care of it.

HLS-272 (warning) Detected an inconsistency of bindings in memory '%s'.
Binding '%s' is nonpipelined and binding '%s'
is pipelined. Using this memory can cause a suboptimal schedule.

DESCRIPTION

The use of memory with both pipelined and nonpipelined binding for the same access type (such as read access or write access) is also allowed in Behavorial Compiler, but might not find an optimal schedule for the memory accesses.

WHAT NEXT

Adjust the resource names in the resource_use fields of the bindings in .sl file to make them nonpipelined or pipelined with same initiation intervals.

HLS-273 (error) Loop has exits but loop continue %s does not have any condition.

DESCRIPTION

The loop has both exits and loop continue but there is no distinguishable condition on thess two operation. It means there is transition ambiguity between loop continue and loop exit.

WHAT NEXT

Look for source code and check that there is a condition for loop exit. If so, check that the condition is set the proper way.

HLS-274 (Error) The memory resource '%s' at line '%d' is not supported for multi-processes.

DESCRIPTION

There are some memory resources declared in the architecture level.

WHAT NEXT

Move those declaration into each process.

NAM

HLS-275 (error) Memory module '%s' cannot be found in the synthetic libraries.

DESCRIPTION

The memory module name specified in the design source file cannot be found in the available synthetic libraries.

WHAT NEXT

Change the module name into one in the current syntatic library set or add the synthetic library which defines the module to synthetic library set.

HLS-276 (error) Command "bc_report_memories" cannot be applied to design ’%s’ which was not elaborated for behavioral synthesis.

DESCRIPTION

The **bc_report_memories** command processes only the designs elaborated for behavioral synthesis.

WHAT NEXT

Elaborate the design again with the -s option.

HLS-277 (error) Command "bc_report_memories" cannot be applied to the scheduled design ’%s’.

DESCRIPTION

The command can only be applicable to the design which has not been scheduled.

WHAT NEXT

Apply the command before schedule, but after elaboration.

HLS-278 (error) Read memory access of ’%s’ in process ’%s’ cannot be performed because module ’%s’ does not have either a read only or read/write port.

DESCRIPTION

The memory module cannot be used for read access because there is no port for read.

WHAT NEXT

Change the memory module into one which can be read.

HLS-279 (error) Write memory access of '%s' in process '%s' cannot be performed because module '%s' does not have either a write only or read/write port.

DESCRIPTION

The memory module cannot be used for write access because there is no port for write.

WHAT NEXT

Change the memory module into one which can be written.

HLS-280 (warning) User Constraint was given to ignore memory precendences between '%s' and '%s' in process '%s', in which their accesses conflict.

DESCRIPTION

You put an ignore_memory_precendences constraint between two memory accesses which conflict. This can cause siumulation mismatch due to generation of incorrect logics.

WHAT NEXT

Do not use the constraint or check that the constraint does not produce incorrect logics.

HLS-281 (warning) User Constraint was given to ignore memory loop precendences between '%s' and '%s' in process '%s',

in which their accesses across iterations of loop conflict.

DESCRIPTION

You put an ignore_memory_loop_precendences constraint between two memory accesses, which conflict. This can cause siumulation mismatch due to generation of incorrect logics.

WHAT NEXT

Do not use the constraint or check that the constraint do not produce incorrect logics.

HLS-282 (warning) The node '%s references design '%s' which does not drive output '%s'. Please check the state binding in your .sl file.

DESCRIPTION

WHAT NEXT

HLS-283 (error) Because options -dont_split, -round_bits #, and -truncate_bits # conflict with each other, choose only one. See the man page for transform_csa to find out how to control operation spliting.

DESCRIPTION

Operation spliting occurs when lower-bits of output of driving cell does not used in the loaded cell. There are three options for controlling operation spliting:

-dont_split means that transform_csa does not allow operation spliting.
-truncate_bits # means that transform_csa allow operation
spliting up to # bits and used the last carry out bit.
-round_bits # means that transform_csa allow operation spliting
up to # bits and used the last carry out and the most significant bit.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-284 (error) The variable bc_allocation_effort is no longer supported. Please use the option -allocation_effort for the schedule command.

DESCRIPTION

The shell variable **bc_allocation_effort** has been replaced by the **-allocation_effort** option of the **schedule** command and is no longer supported.

WHAT NEXT

To control the allocation effort of behavioral synthesis, please use the **-allocation_effort** option of the **schedule** command.

SEE ALSO

schedule(2)

HLS-285 (information) Operations '%s' and '%s' were not merged into CSA operations. See the man page for this command to find out how to use distributive rule to decrease delay at the expense of extra area.

DESCRIPTION

The corresponding expression in source file is a * (b + ...). It can be changed into a * b + a * ... so that CSA transformation can be applied. This might increase area, but can reduce the delay. This might be beneficial if there is a constant term on the addition expression. But, it needs to examine operations which are connected to the addition to see that the operations together with the addition can merge into CSA operations.

WHAT NEXT

Change the expression of the form a * (b + ...) into a * b + a * ...

HLS-286 (information) Operations '%s' and '%s' were not merged into CSA operations because '-dont_split' option was asserted. See the man page for transform_csa to find out how the operations can be merged by spliting operation.

DESCRIPTION

Operation spliting occurs when lower bits of output of the driving cell are not used in the loaded cell. There are three options for controlling operation spliting:

1. '-dont_split' means that transform_csa does not allow operation spliting.
2. '-truncate_bits #' means that transform_csa allows operation spliting up to # bits and uses the last carry out bit.
3. '-round_bits #' means that transform_csa allows operation spliting up to # bits and uses the last carry out and the most significant bit.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-287 (warning) Designware Foundation license is not avaiable during transform_csa.

DESCRIPTION

The tranform_csa command can be performed without Designware Foundation license, but can cause an error afterwards.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-288 (warning) Due to the transformation of operations with lower bit rounding,
simulation mismatch can occur. See man pages to find out how simulation
mismatch can be avoided on transform_csa.

DESCRIPTION

Simulation mismatch occurs when -round_bits n or -truncate_bits n is used. With -round_bits, simulation mismatch always occurs with -truncate_bits. It occurs when its value is small enough not to take into the result of operation of the least significat bits of inputs.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-289 (information) The direction of port '%s' will be input.

DESCRIPTION

WHAT NEXT

HLS-290 (warning) Could not find memory '%s' in synthetic libraries which is
to be accessed by '%s' of instance '%s'.

DESCRIPTION

The memory used in design is not available in synthetic library. Note that memory name is case sensitive.

WHAT NEXT

Include the memory in synthetic library.

HLS-291 (information) cell '%s' will be chained if possible.

DESCRIPTION

A positive delay has been specified with **set_memory_output_delay** command. BC will try to chain the specified memory read operations with subsequent operations.

WHAT NEXT

No further action is required. This is simply an informational message to indicate that the **set_memory_output_delay** command was successfuly applied.

HLS-292 (error) You cannot specify a zero delay with the set_memory_output_delay command.

DESCRIPTION

A zero delay has been specified with **set_memory_output_delay** command.

WHAT NEXT

The delay sould be positive non zero number. To infer a register, specify a delay equal to the clock period.

HLS-293 (information) the design '%s' has been already timed. The timing table will be automatically update.

DESCRIPTION

This is an informational message. The current design has been already timed. The set_memory_output_delay(set_memory_input_delay) command will automatically update the current timing to take into account the delay specified with **set_memory_output_delay** or **set_memory_input_delay**.

WHAT NEXT

This is an information message. No further action is needed.

HLS-294 (error) Could not find memory name '%s' in synthetic library.

DESCRIPTION

The memory instance name specified in -name list does not exist in any of the synthetic libraries listed in the synthetic_library dc_shell variable.

WHAT NEXT

Make sure that the synthetic_library dc_shell variable includes a synthetic library that contains a memory where name matches the one specified. The command **bc_report_memories** can be used to get a list of memories available in the currently speficied synthetic libraries or a list of memories used in the current design.

HLS-295 (error) Negative delays are not allowed with the set_memory_output_delay command.

DESCRIPTION

You have specified a negative delay with the **set_memory_output_delay** command. This is not allowed.

WHAT NEXT

Specify a delay greather than zero with the **set_memory_output_delay** command.

HLS-296 (error) STABLE = TRUE on a memory output port was detected this is inconsistant with positive internal delays

DESCRIPTION

This command is inconsistent when a STABLE attribute on
the output port of the memory in the .sl file is TRUE
and a positive internal delay is specified.

WHAT NEXT

Check your memory output STABLE attribute in the .sl file. or make sure that the internal delay is 0.

HLS-297 (warning) Due to the pipelining of loop '%s', the unbalanced branches of the conditional at line %s will get scheduled in the same number of control steps.

DESCRIPTION

Pipelining requires the loop body to be executed in the same number of control steps independently of the conditional branches being executed.

In your behavioral description, you have specified a conditional statement with different numbers of clock statements in the different branches. The loop that contains this conditional statement has been specified for pipelining.

In the synthesized design, in order to pipeline the loop, each of the branches will be executed in the same number of clock cycles.

WHAT NEXT

No further action is needed.

However, in simulation, the synthesized design may behave differently from your behavioral description due to the additional clock cycles inserted in some of the branches of the conditional statement.

If necessary, modify your behavioral description to have the same number of clock statements in all branches of the conditional statement.

HLS-298 (error) bc_force_balanced_branches has an illegal value.

Please use one of never, always, wait_based.

DESCRIPTION

WHAT NEXT

HLS-299 (information) Evaluation of an exit condition of loop '%s' needs %d extra clock cycles after the loop to preserve timing when exiting.

DESCRIPTION

When exiting loop, the evaluation of condition takes some amout of clock cycles. If state transition is not allowed, at least one clock cycle is needed after loop because the exit transition should be preserved across the loop. For cycle-fixed mode, the number of clock cycles is strictly required while for other modes, the clock cycles are added if not sufficient in source file by user. It could be an error if an i/o operation occurs during the period of clock cycles after loop because the exit is not completed at that period.

WHAT NEXT

For cycle-fixed mode, add more wait/@posedge after loop if not enough and for superstate-fixed, make sure that the extra clock cycles are used for exit transition.

HLS-300 (error) Current design is not defined.

DESCRIPTION

WHAT NEXT

HLS-301 (error) synthetic_library variable is not defined.

DESCRIPTION

"bc_report_memories" cannot work with undefined synthetic_library.

"set_memory_output_delay" cannot work with undefined synthetic_library.
"set_memory_input_delay" cannot work with undefined synthetic_library.

WHAT NEXT

Define synthetic_library variable before using the command.

HLS-302 (information) Only ’-synthetic_libraries’ or ’-bindings’ are applied
because current design is not defined.

DESCRIPTION

"-synthetic_libraries" and/or "-bindings" work even though current design is not defined. But, for the other options to work design should be defined.

WHAT NEXT

HLS-303 (information) Multi-stage multiplication ’%s’ is not applicable to transformation.

DESCRIPTION

Because multi-stage multiplication is not combinational, transform_csa does not transform the operation. Note that after transform_csa to combinational multiplication, "optimize_registers" command to compiled gate-level design can help you generate a design of pipelined stage of the multiplication automatically. This mean that "transform_csa" and then "optimize_registers" flow can generate pipelined design automatically.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-304 (information) No addition/subtraction/multiplication

tree was found.

DESCRIPTION

The tree structure to be transformed is of the form in which if it is a single-node tree the node must be multiplication, and if is a multi-node tree non-leaf nodes must not be multiplication. In addition, note that addition/subtraction/ multiplication to be transformed must be purely combinational.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-305 (errro) Because options '-balance_only' and '-chain_only' are conflict,
choose only one of them. See the man page for transform_csa to
find out the applications.

DESCRIPTION

-balance_only transforms an operation tree into a balanced addition tree. -chain_only transforms an operation tree into a chained addition tree. In BC-flow, -balance_only is intended for reducing timing while -chain_only is indended for reducing area.

WHAT NEXT

HLS-306 (warning) '-duplicate' option cannot be appiled together with '%s'
option. '-duplicate' was ignored.

DESCRIPTION

-balance_only transforms an operation tree into a balanced addition tree. -chain_only transforms an operation tree into a chained addition tree. In BC-flow, -balance_only is intended for reducing timing while -chain_only is indended for reducing area. Note that -duplicate is meaningful only for transform an operation tree into CSA operation (not additions).

WHAT NEXT

HLS-307 (error) ’%s’ is an invalid logic grouping size. Use one of ’zero’, ’small’, ’medium’, and ’large’.

DESCRIPTION

WHAT NEXT

HLS-308 (warning) Negative value ’%d’ of option ’%s’ is not allowed. The option was ignored.

DESCRIPTION

Values of -round_bits and -truncate_bits shound be zero or positive integers.

WHAT NEXT

Specify non-negative number.

HLS-309 (warning) Memory module ’%s’ uses binding ’%s’ which has no state information. This can cause a fatal error in schedule.

DESCRIPTION

Each binding defined in memory module should have non-empty state infarmation.

WHAT NEXT

Add state information inside of the binding.

HLS-310 (information) Operations '%s' extended input bit-width %s
to generate MULT2 operation without output extension. It increases area,
but can reduce the delay.

DESCRIPTION

Currently, extending output of mult2 doen not gaurantee the correctness of simulation when the extended output is used as a input of csa tree. Therefore, we extened the input width of mult so that when decompoed into mult2 there is no need to extend its outputs.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-311 (warning) memory_address_port attributes were found in processes %s.
But, bc_allow_shared_memories is not set. The memory is assumed to be
non-shared.

DESCRIPTION

Shared memory feature is effective only when bc_allow_shared_memories = "true". Otherwise, BC considers the memory as a non-shared memory. Use bc_report_memories command to find out the detail information of the memory used in scheduling.

WHAT NEXT

Set bc_allow_shared_memories to be true to apply the shared memory feature.

HLS-312 (error) Could not find operations MULTP_UNS_OP and MULTP_TC_OP.
This is probably because the synthetic library dw02.sldb is

missing from
 the synthetic_library variable specification or the dw02.sldb does not contain
 the modules..

DESCRIPTION

The transform_csa command needs to be able to find the synthetic operations "MULT2_UNS_OP" and "MULT2_TC_OP" in the libraries specified by the synthetic_library variable.

WHAT NEXT

The transform_csa command is obsolete. Please use compile_ultra or set_ultra_optimization instead.

HLS-313 (error) Multiple %s bindings were defined in address port '%s' of memory '%s'.

DESCRIPTION

For each port of memory, only one read/write binding must be defined.

WHAT NEXT

Check the bindings of the memory.

HLS-314 (error) Reset signal came from synthetic operation or sequential operation.

DESCRIPTION

Reset signal must come from either combinational logic or port.

WHAT NEXT

Redefine reset signal.

HLS-315 (error) Number of cycles '%d' constrained to graph '%s' by set_cycles command exceeds the minimum number of cycles %d required for the graph.

DESCRIPTION

Note that the cycles specified by set_cycle command to the graph must be greater than or equal to the required minimum number of cycles.

WHAT NEXT

Reset the number of cycles.

HLS-316 (error) Because preserve function '%s' contains %s %s the function cannot be treated as a designware. See the man page to find out the usage of preserve function attribute.

DESCRIPTION

A preserve function can be treated as a designware part if it does not contains - loop construct - sequential operation - wait/posedge statement - memory access operation, or - signal access operation

Use preserve "sequential" function attribute if the function want to be treated as a schedulable component rather than a designware component.

WHAT NEXT

Remove the illegal statemet from the design description or use preserve sequential function attribute.

HLS-317 (error) Negative delays are not allowed with the

set_memory_input_delay command.

DESCRIPTION

You have specified a negative delay with the **set_memory_input_delay** command. This is not allowed.

WHAT NEXT

Specify a delay greather than zero with the **set_memory_input_delay** command.

HLS-318 (error) You cannot specify a zero delay with the set_memory_input_delay command.

DESCRIPTION

A zero delay has been specified with **set_memory_input_delay** command.

WHAT NEXT

The delay sould be positive non zero number.

HLS-319 (error) Cannot find variable '%s' in design '%s'. set_exclusive_use will be ignored.

DESCRIPTION

The variable specified could not be found in the design.

WHAT NEXT

Check in your HDL, whether the variable really exists. If you tried applying this command on a db that has already been timed, you might want to try specifying this constraint right after elaboration.

HLS-320 (error) Precompiled design '%s' has not been created

in the Behavioral Compiler flow.

DESCRIPTION

To avoid inconsistencies, **bc_time_design** requires that precompiled parts that represent preserved functions have to be generated from within **bc_time_design**.

WHAT NEXT

Please call **bc_time_design** again using the **cache_user_dw** option.

HLS-321 (information) Writing preserved function '%s' to file '%s'
in library '%s' which is mapped to '%s'.

DESCRIPTION

The preserved function has been written into the design library as directed by the option **cache_user_dw** specified with **bc_time_design**.

WHAT NEXT

When you call **bc_time_design** again you can reuse the precompiled part by providing the name of the **design_library** for the **use_chached_user_dw** option of **bc_time_design**. However, please make sure that you only use this mechanism as long as the HDL code for all the preserved functions have not changed. Otherwise, you will observe simulation mismatches between the pre- and post scheduling versions of your design.

HLS-322 (warning) Reading precompiled version of preserved function '%s' from library '%s'.

DESCRIPTION

WHAT NEXT

HLS-323 (warning) Cannot find precompiled version of preserved function '%s'

in library '%s'. The preserved function will get compiled.

DESCRIPTION

bc_time_design was not able to find the precompiled function in the designated library. Therefore, **bc_time_design** has to compile the preserved function.

WHAT NEXT

HLS-324 (warning) test

DESCRIPTION

WHAT NEXT

HLS-325 (error) Behavioral Compiler does currently not support data dependencies from the inside of a pipelined loop to the outside of that loop, unless the producer of the data is scheduled in the initiation interval.

DESCRIPTION

WHAT NEXT

HLS-326 (information) register '%s' has a reset value '%s'

DESCRIPTION

This is an information message to warn that a reset value has been assigned to this register. The set/reset pin of this register will be directly connected to the reset signal of the design.

WHAT NEXT

Since the reset/set pin of the considered register are directly
connected to the reset signal of the design. You should expect
a difference cycle behavior between signal A and B in the following example:

```
RstL: loop
 A <= "1011";
 B <= In1 + 4;
 wait until Clk'event and CLK ='1';
 exit reset_loop when reset = '1';

 MainL: loop
 ....
 end loop MainL;
end loop RstL;
```

A will get the value "1011" when the reset is sampled true. B will get the fisrt value in the following rising edge.

HLS-327 (error) Negative external delays are not allowed with the set_memory_output/input_delay command.

DESCRIPTION

You have specified a negative delay with the **-external** option of the **set_memory_input_delay** command or the **set_memory_output_delay** command. This is not allowed.

WHAT NEXT

Specify a delay greather than zero with the **-external** option.

HLS-328 (information) An old delay '%f' has been found on cell '%s'

DESCRIPTION

This is to inform you that cell '%s' had already an old delay value
Since no delay has been specified with set_memory_output/input_delay
command. The old delay is taken into account.

WHAT NEXT

To override the old delay specify a new one with the -delay option
of set_memory_output/input_delay.

HLS-329 (information) An old external delay '%f' has been found on cell '%s'

DESCRIPTION

This is to inform you that cell '%s' had already an old external delay value
Since no external delay has been specified with set_memory_output/input_delay
command. The old external delay is taken into account.

WHAT NEXT

To override the old delay specify a new one with the -external option
of set_memory_output/input_delay.

HLS-330 (error) no memory found in synthetic libraries.

DESCRIPTION

No memory is declared in synthetic libraries

WHAT NEXT

check your synthetic libraries or your synthetic_library dc_shell variable if it includes the desired synthetic library.

HLS-331 (warning) no clock has been yet defined on the current design

DESCRIPTION

The delays specified with **set_memory_input_delay** and **set_memory_output_delay** must not exceed the effective clock period.

However, we cannot check this since the clock has not yet been created for your design.

WHAT NEXT

When you do create a clock, make sure that the delays specified with **set_memory_input_delay** and **set_memory_output_delay** do not exceed the effective clock period.

The effective clock period is the clock period you specify with the **create_clock** command minus the clock cycle margin computed by the **bc_margin** command or the **bc_time_design** command.

HLS-332 (error) The total delay '%f' exceeds the clock period '%f'

DESCRIPTION

The sum of the delays specified with **set_memory_input_delay** or **set_memory_output_delay** commands exceeds the clock period already specified.

WHAT NEXT

Check your delays and/or your clock period and make sure that the sum of the delays does not exceed the clock period.

HLS-333 (information) Please use "bc_clears_all_registers" rather than "reset_clears_all_bc_registers" next time.

DESCRIPTION

The official variable name is bc_clears_all_registers even though BC still supportreset_clears_all_bc_registers for a while.

WHAT NEXT

Replace reset_clears_all_bc_registers by bc_clears_all_registers.

HLS-334 (information) Nothing to report for given range in this

process.

DESCRIPTION

No operations or variables are scheduled in given range. During **report_schedule**, -start or -finish options are generated out of range.

WHAT NEXT

Do **report_schedule** to find out proper range.

HLS-335 (warning) The dont_unroll loop %s is missing.

DESCRIPTION

The dont_unroll attribute is specified but there’s no loop has that name.

WHAT NEXT

Examine the source code to make sure the dont_unroll attribute is the correct name.

HLS-336 (warning) Direct reset is turned off because the command control_register -outputs is on.

DESCRIPTION

The direct reset (default mode) will keep reset signals from appearing in the datapath. However, the feature will not work if the command control_register -output and the reset signal will appear on datapath.

WHAT NEXT

use set_behavioral_reset -fsm to allow reset signal in the datapath.

HLS-337 (error) The command ’%s’ is only valid on designs that have
been timed for scheduling, but have not been scheduled yet.

The design ’%s’ is not valid.

DESCRIPTION

This command operates only on designs that have been timed for scheduling.

WHAT NEXT

Make sure the design being passed in to this command has been timed for scheduling.

HLS-338 (error) The ’area’ option for the schedule command has been renamed in ’extend_latency’.

DESCRIPTION

Due to the confusion the name of the ’area’ option created, it has been renamed into ’extend_latency’.

WHAT NEXT

Call the **schedule** command using the ’extend_latency’ option.

HLS-339 (information) the design ’%s’ has been already timed.

DESCRIPTION

This is an information message. The current design has been already timed.

WHAT NEXT

Rerun **bc_time_design** to update the timing table before scheduling.

HLS-340 (warning) Port ’%s’ drives node ’%s’.

DESCRIPTION

When a port has been constrained using **bc_dont_register_input_port**, it is recommended that the port drives all consumers directly. Consider the example given

below where it is assumed that the port data_in has been marked as not requiring a register.

```
  -- This is bad, a register might get allocated for tmp
  tmp := data_in;
  loop
    a := b + tmp;
    ...
  end loop;

  -- This is correct
  loop
    a := b + data_in;
    ...
  end loop;
```

WHAT NEXT

Check whether you can rewrite the HDL to avoid the unintentional allocation of registers.

HLS-341 (error) Design %s is already compiled for bc_time_design.

DESCRIPTION

This design has been already compiled for **bc_time_design**.

WHAT NEXT

To recompile the design, use the -force option.

HLS-342 (error) no cluster was found in %s

DESCRIPTION

No cluster was found in %s.

WHAT NEXT

Make sure that you already clustered random logic using the **bc_group_logics** or the **bc_time_design** commands.

HLS-343 (warning) %s attribute is set true on design %s

DESCRIPTION

This is a warning message. A %s attribute is set true on design %s. This design will not be compiled.

WHAT NEXT

Refer to the **bc_time_design** or the **bc_time_groups** man pages for more information.

HLS-344 (error) Design %s is not a cluster of random logic

DESCRIPTION

The **bc_time_groups** command is only applied on random logic groups that are clustered. This design is not a cluster of random logic.

WHAT NEXT

Make sure that all designs specified with **bc_time_groups** are clusters of random logic. For more informations on clustering random logic refer to **bc_time_design** and **bc_group_logics** commands.

HLS-345 (information) The delay on the write to signal '%s' at line %d
causes the assignment to be scheduled %d cycles after the beginning of the enclosing loop.

DESCRIPTION

The signal identified in the message has been specified as being delayed in the HDL. In order for synthesis to match simulation, Behavioral Compiler might have to pipeline the loop.

WHAT NEXT

This is an information message. No further action is necessary.

HLS-346 (warning) The design has a comparison operation on line %d that compares values of type std_logic_vector. This is ambiguous.

DESCRIPTION

BC is not able to map to any operator for this type of comparison operation. This is because the type of variables that are compared is not clearly defined for comparison. For example, BC will not figure out what kind of comparator should be used for std_logic_vector variables, because the values could be interpreted as signed or as unsigned. This might cause simulation mismatches!

If for example a and b are defined as std_logic_vector, then the following statement is ambiguous

```
if (a < b) then
```

change it into e.g.

```
if (signed(a) < signed(b)) then
```

WHAT NEXT

Check the hdl code for the types of variables used in comparison operations. The type have to be clear such as signed or unsigned. ~

HLS-347 (warning) All dont_care nets will become logic zero nets.

DESCRIPTION

If a design has dont_care signals, BC will treat them as logic zero. For example, VHDL code

```
CS_Z <= '-';
```

will be translated into

```
CS_Z <= '0';
```

In other words, BC will generate the same design as the variable hdlin_make_dc_zero set to true.

WHAT NEXT

Providing a specific value for each signal is recommended. Rewrite your HDL code so

that it does not contain any dont care signals.

HLS-348 (error) The variable feeding input %s of operation %s is not initialized.

DESCRIPTION

Behavioral Compiler detected that an input variable to the operation described has never been initialized.

WHAT NEXT

Please make sure, that all variables in your HDL code are initialized appropriately.

HLS-349 (Error) Design %s contains a subdesign %s which does not drive a used output %s

DESCRIPTION

You can receive this message if you have a subdesign whose outputs are never used by designs higher in the hierarchy. Behavioral Compiler disconnects the cells driving these outputs. However, if designs higher in the hierarchy have operations to which these outputs are connected, Behavioral Compiler reports this error.

This can happen if there is unreachable code in the input behavioral description.

In the example below, the line "y := b + 16;" is never reached because main_loop is never exited. Behavioral Compiler will not drive the "b" output of subdesign "main_loop_design", but the output "b" is connected to an adder in subdesign "reset_loop_design", generating this error message.

```
reset_loop : loop

x <= x_in

wait until clk'event and clk='1' if reset='1' then exit reset_loop; end if;

main_loop : loop

a := 1 + x; b := a * 5;

wait until clk'event and clk='1' if reset='1' then exit reset_loop; end if;

end loop main_loop;

y := b + 16; -- dead code
```

```
end loop reset_loop;
```

WHAT NEXT

Examine your design for code that uses the undriven output that was reported. Remove any unreachable code that uses the undriven output.

HLS-350 (warning) Operation ’%s’ has been turned into a multicycle operation.

DESCRIPTION

The margin time is set to take clock-to-Q delay and signal setup time into account. Even though the execution time of an operation is less than the clock period, if the sum of the margin and the executition time of an operation is bigger than the clock period, then the operation cannot be executed within a single cycle. Therefore, the operation is transformed into a multicycle operation. This warning message informs the user that this operation has been turned into a multicycle operation.

WHAT NEXT

- To disable multicycle operation, set bc_enable_multi_cycle = false - To change the margin amount, use bc_margin command - For a multicycle operation of ’n’ cycles, the available execution time is effectively: ’n’ * clock_period - margin_amount.

HLS-351 (information) Using precompiled version of preserved function ’%s’ from library ’%s’.

DESCRIPTION

The subdesign for the preserved function identified in the message will be taken from the cached version in the specified library. This cached version replaces the subdesign previously linked to the main design.

WHAT NEXT

This is an information message. No further action is necessary.

HLS-352 (error) The variable %s is no longer supported.

Please use %s instead.

DESCRIPTION

The following variables are removed: - bc_connect_reset It is replaced by the default mode of the new reset implementation. To enforce the default setting, please use set_behavioral_reset without any argument. - bc_no_reset_on_datapath It used to be the same variable as "bc_connect_reset". So it’s now replaced by "set_behavioral_reset". - bc_clears_all_registers It used to be used to clear all registers to zeros. Now you can you set_behavioral_reset with -all option to obtain the same behavior.

For the current release, it is an error because we want to make sure that users use the new command and variables. After that, when users may define these variable if they want to. Please modify your script to use the new command: set_behavioral_reset with new options.

WHAT NEXT

Also note that the following commands were also removed or modified: set_behavioral_async_reset, set_behavioral_reset.

HLS-353 (error) There must be a main (infinite) loop inside the reset loop, if you are using the direct reset connection.

DESCRIPTION

You receive this message if you are using the direct reset connection and your design description has a reset loop that contains no main (infinite) loop. If you executed **set_behavioral_reset** without the **-fsm** option, by default you are using the direct reset connection.

Behavioral Compiler expects each process to be structured with the reset loop as the outermost loop, and the main loop as the next outermost loop. In this case, expected reset behavior might not be fully achieved.

Thus, Behavioral Compiler does not perform any strict checking for reset loop coding style when there is no nested infinite loop structure.

WHAT NEXT

Rewrite your code so that it has a nested loop structure with the reset loop as the outermost loop and the main (infinite) loop directly within the outermost loop, then re-execute. For an explanation of the recommended Behavioral Compiler coding style, see the manual page for the **set_behavioral_reset** command, or the *Behavioral Compiler User’s Guide*.

SEE ALSO

set_behavioral_reset (2), *Behavioral Compiler User's Guide*.

HLS-354 (error) You cannot use a rolled loop before the first clock statement inside the reset loop block, if you are also using the direct reset connection. Add a clock statement before the rolled loop inside the reset loop block, or use set_behavioral_reset -fsm.

DESCRIPTION

You receive this message if you are using the direct reset connection and used a rolled loop before the first clock statement inside the reset loop block. If you executed **set_behavioral_reset** without the **-fsm** option, by default you are using the direct reset connection.

A construction where a conditional execution appears in the reset loop, especially before the first clock statement, makes the reset behavior unpredictable.

"for" loops are unrolled by default; no error message is issued if there is a "for" loop before the first clock statement. However, when you specify "dont_unroll" of a certain "for" loop, an error message is issued if a "for" loop with the "dont_unroll" attribute appears before the first clock statement, as in the following example:

```
    --- code fragment
    attribute dont_unroll of f1:label is TRUE;
    begin
D <= "00001";
E <= "11111";


        f1: for i in C'range loop
            C(i) <= A(i) and B(i);
            wait until clk'event and clk = '1';
        end loop;

    end process;
    -- end of code fragment
```

WHAT NEXT

Insert a clock statement before the rolled loop, then re-execute. For an explanation of the recommended Behavioral Compiler coding style, see the manual page for the **set_behavioral_reset** command, or the *Behavioral Compiler User's Guide*.

Alternatively, you can use **set_behavioral_reset -fsm**; there are no coding style restrictions in this case. However, when the FSM reset is used, reset link checking is turned off and there might be a performance penalty.

SEE ALSO

set_behavioral_reset (2), *Behavioral Compiler User's Guide*.

HLS-355 (warning) No signal assignments appear before the first clock statement in the reset loop; therefore, the reset signal cannot be directly connected to any signals.

DESCRIPTION

You receive this message if you are using the direct reset connection and a clock statement appears in the reset loop before any signal operation. If you executed **set_behavioral_reset** without the **-fsm** option, by default you are using the direct reset connection.

The message warns you that currently no signals in your design can be connected to the reset signal. Signal registers are reset only if their signal assignments appear before the first clock statement in the reset loop. Otherwise, no signal registers can be directly connected to the reset signal.

In Behavioral Compiler, variable assignments are delayed until they are really necessary, which means that even though the HDL description shows some variable assignments, it is possible that Behavioral Compiler will not see any assignments before the first clock statement. Also, checking for reset loop coding style is carried out on the portion of the reset loop before the first clock statement. In this case, checking for reset loop coding style is effectively not carried out because there is no statement before the first clock statement.

WHAT NEXT

Remove the clock statement from the description; it does not perform any meaningful function. For an explanation of the recommended Behavioral Compiler coding style, see the manual page for the **set_behavioral_reset** command, or the *Behavioral Compiler User's Guide*.

Alternatively, you can use **set_behavioral_reset -fsm**; there are no coding style restrictions in this case. However, when the FSM reset is used, checking for reset loop coding style is turned off and there might be a performance penalty.

SEE ALSO

set_behavioral_reset (2), *Behavioral Compiler User's Guide*.

HLS-356 (error) You cannot use a reset loop that contains a conditional (if) statement before the first clock statement, if you are also using the direct reset connection. Add a clock statement before the conditional statement inside the reset loop block, or use set_behavioral_reset -fsm.

DESCRIPTION

You receive this error message if you are using the direct reset connection and your reset loop block contains a conditional (if) statement before the first clock statement. If you executed **set_behavioral_reset** without the **-fsm** option, by default you are using the direct reset connection.

In the direct reset connection, Behavioral Compiler directly connects the reset signal to the preset/clear pin of the register to be reset. If there is a conditional statement in the reset loop before the first clock, the assignment inside the conditional might not be reset in the first cycle. In addition, the reset value cannot be determined until run time.

Another structure that is not allowed is a rolled loop before the first clock statement in the reset loop; any rolled loop must have at least one clock statement.

WHAT NEXT

Insert a clock statement before the conditional statement, then re-execute. For an explanation of the recommended Behavioral Compiler coding style, see the manual page for the **set_behavioral_reset** command, or the *Behavioral Compiler User's Guide*.

Alternatively, you can use **set_behavioral_reset -fsm**; there are no coding style restrictions in this case. However, when the FSM reset is used, checking for reset loop coding style is turned off and there might be a performance penalty.

SEE ALSO

set_behavioral_reset (2), *Behavioral Compiler User's Guide*.

HLS-357 (information) The reset signal will be directly connected to the preset or clear pin of registers.

DESCRIPTION

This message informs you that the reset signal is being directly connected to the preset/clear pin of those registers that need to be reset. If you executed **set_behavioral_reset** without the **-fsm** option, by default you are using the direct

reset connection.

During **compile** (by Design Compiler), when the register is mapped to a filp-flop without a preset or clear pin, an equivalent implementation is realized with the reset signal hooked up to the D-pin of the mapped flip-flop. But as long as there is a reset pin in the mapped flip-flop, the reset signal is directly connected to it. The reset value for each register to be reset must be known, or an error messsage is generated.

Alternatively, you can let the FSM generate the reset signal as it generates other control signals, by executing **set_behavioral_reset -fsm**. In that case, the reset signal is fed into the FSM, and the reset signal is generated from the FSM. There are no coding style restrictions when the FSM reset is used; however, checking for reset loop coding style is turned off and there might be a performance penalty.

WHAT NEXT

If you intended for the reset signal to be directly connected to the preset or clear pin of registers, with no intervening logic, no action is required on your part. In this default direct reset connection mode, certain coding restrictions apply. For more information, see the manual page for the **set_behavioral_reset** command, or the *Behavioral Compiler User's Guide*.

Otherwise, use **set_behavioral_reset -fsm** as previously described.

SEE ALSO

set_behavioral_reset (2), *Behavioral Compiler User's Guide*.

HLS-358 (information) The reset signal will be generated from the FSM.

DESCRIPTION

This message informs you that the reset signal is being generated from the FSM, because you have executed **set_behavioral_reset -fsm**. The reset signal from the FSM can be regarded as a control signal normally generated from the FSM, and goes through glue logic in the datapath instead of being directly connected to preset/ clear pin of registers. Since reset is a control signal, the main advantage of using this style of reset is that any general structures (for example, as conditionals and rolled loops) are allowed in the reset loop before the first clock statement. Also, when the FSM reset is used, checking for reset loop coding style is turned off. The main disadvantage is that it takes time to calculate the reset signal in the FSM, and there is additional delay when the reset functions as a select signal for some of MUXes to select the reset value over the normal data value.

Alternatively, you can let the reset signal be directly connected to the preset/ clear pin of those registers that need to be reset, by executing **set_behavioral_reset** without the **-fsm** option.

WHAT NEXT

If you intended for the reset signal to be generated from the FSM, no action is required on your part. Otherwise, to enable the default direct reset connection re-execute **set_behavioral_reset** without the **-fsm** option.

SEE ALSO

set_behavioral_reset (2).

HLS-359 (information) The reset of the scheduled design has been set to %s.

DESCRIPTION

You receive this message to inform you that the reset of the scheduled design has been set to either synchronous or asynchronous, as specified in the message. The synchronous setting is the default; if you want the design's reset to be asynchronous, you must execute **set_behavioral_reset -async**.

WHAT NEXT

If the reset has been set to asynchronous and you want to keep this setting, no action is required on your part.

If the reset has been set to asynchronous and you want to change it to synchronous, execute **set_behavioral_reset** without the **-async** option.

If the reset has been set to synchronous and you want to change it to asynchronous, execute **set_behavioral_reset -async**.

If the reset has been set to synchronous and you want to keep this setting, then to avoid generating errors, follow these guidelines:

- Place an "if" statement after each clock statement.
- Ensure that the "if" block does not have an "else" path.
- Ensure that the "if" block does not have multiple exit paths.
- Ensure that the polarity and condition of the "if" block
  is the same for every occurrence.
- Ensure that in the "if" block, the exit block is
  outside the main loop, so that execution of the current]
  block is terminated when the branch is taken.
- Ensure that all reset jumps jump to the same exit block.

For example, if(reset = '1') then exit reset_loop; end if;
The destination block of the 'exit' should be the same.

SEE ALSO

set_behavioral_reset (2).

HLS-360 (warning) You have executed set_behavioral_reset without arguments; setting all reset options to their default values.

DESCRIPTION

This message informs you that you have executed **set_behavioral_reset** with no options, and therefore all default values will be used.

The default for the **-port** option is to use the reset port specified in the HDL code. If none is specified, an error message is generated.

Defaults for the other options are as follows:

-process (all)
-active (high)
-fsm (false)
-async (false)
-all (false)

NOTE: By using the default reset, you can get fast and simple implementation of reset, but there are restrictions in the coding style, which could generate warning or error messages for nonconformance. For information about the coding style restrictions, see the manual page for the **set_behavioral_reset** command or the *Behavioral Compiler User's Guide*.

Alternatively, to avoid coding restrictions, you can use **set_behavioral_reset -fsm**. However, when the FSM reset is used, checking for reset loop coding style is turned off and there might be a performance penalty.

WHAT NEXT

If the default values are acceptable to you, no action is required on your part. Otherwise, re-execute **set_behavioral_reset** with appropriate options.

SEE ALSO

set_behavioral_reset (2). *Behavioral Compiler User's Guide*.

HLS-361 (information) Checking for reset loop coding style will be performed on the reset loop.

DESCRIPTION

This message informs you that checking for reset loop coding style will be performed on the reset loop. Checking is performed if one of the following is true:

• You have executed the **set_behavioral_reset** command without the **-fsm** option; or

• You have executed the **schedule** command and it detects that checking for reset loop coding style has not been done (for example, if you have not executed **set_behavioral_reset**). In this case, **schedule** checks for reset loop coding style as one of the preliminary steps before the actual scheduling.

The default mode is a simple and intuitive way to implement the reset connections in the design. The following is a VHDL example of a desirable coding style for the default reset connection:

```
    architecture behav of design_name is
      begin
process
reset_loop: loop
signal or variable assignments;
clk statement
main_loop: loop

main functional description

end main_loop;
end reset_loop;
end process;
     end behav;
```

The following is a similar Verilog example:

```
     module
always begin: reset_loop
signal or variable assignments;
clk statement

forever begin: main_loop

main functional description

end // main_loop
end // reset_loop
     end module
```

WHAT NEXT

If you want checking for reset loop coding style to be performed on the reset loop, no action is required on your part. Otherwise, to disable this checking, execute **set_behavioral_reset** with the **-fsm** option.

SEE ALSO

schedule (2), **set_behavioral_reset(2),** *Behavioral Compiler User's Guide*.

HLS-362 (warning) Multiple rolled loops appear in the reset loop.

DESCRIPTION

You receive this message if you are using the direct reset connection and your design description has multiple rolled loops in the reset loop. If you executed **set_behavioral_reset** without the **-fsm** option, by default you are using the direct reset connection.

It is not recommended to have multiple loops in the reset loop. Sometimes the behavioral description inevitably has several rolled loops inside the reset loop. For example, if there is a big "for" loop to initialize a big array, it is preferable to keep it rolled. But in most other cases, it is preferable to have a single rolled loop (main loop) inside the reset loop.

WHAT NEXT

Rewrite your code so that it has a single rolled loop inside the reset loop, then re-execute. For an explanation of the recommended Behavioral Compiler coding style, see the manual page for the **set_behavioral_reset** command, or the *Behavioral Compiler User's Guide*.

Alternatively, you can use **set_behavioral_reset -fsm**; there are no coding style restrictions in this case. However, when the FSM reset is used, checking for reset loop coding style is turned off and there might be a performance penalty.

SEE ALSO

set_behavioral_reset (2), *Behavioral Compiler User's Guide*.

HLS-363 (error) The reset port was not specified either with set_behavioral_reset -port or in the HDL description. Cannot

define reset characteristic.

DESCRIPTION

You receive this message if you attempt to use a reset characteristic but Behavioral Compiler cannot find a specification of the reset port. If you do not define the reset port using **set_behavioral_reset -port**, the default is to use the reset port specified in the HDL code. If none is specified, this error message is generated.

WHAT NEXT

Specify the reset port, either by using **set_behavioral_reset -port**, or by adding the reset port specification to your HDL description.

SEE ALSO

set_behavioral_reset (2).

HLS-365 (warning) Multiple clock statements appear in the reset loop.

DESCRIPTION

You receive this warning message if you are using the default direct reset connection and have multiple clock statements in the reset loop. If you executed **set_behavioral_reset** without the **-fsm** option, by default you are using the direct reset connection.

Multiple clock statements in the reset loop are not recommended, because the reset actions either might not take place in the same clock cycle simultaneously, or might introduce additional delays in executing reset actions.

Also, with the direct reset connection, each rolled loop inside the reset loop should have at least one clock statement.

WHAT NEXT

If possible, rewrite your code so that only one clock statement appears in the reset loop. For an explanation of the recommended Behavioral Compiler coding style, see the manual page for the **set_behavioral_reset** command, or the *Behavioral Compiler User's Guide*.

If you must have multiple clock statements in the reset loop, you can use **set_behavioral_reset -fsm**; there are no coding style restrictions in this case. However, when the FSM reset is used, checking for reset loop coding style is turned off and there might be a performance penalty.

SEE ALSO

set_behavioral_reset (2), *Behavioral Compiler User's Guide*.

HLS-366 (error) Input port '%s' is updated inside function '%s'.

DESCRIPTION

You receive this message if the specified input port, which is an input to the specified function, is being modified within the function. You cannot modify a signal within a function if that signal is defined as an input to the function.

The following is an example of code that would generate this error message. The input port coin_count is modified in the "if" block of the function.

```
    task coin_return_task;
    // synopsys preserve_schedule_subprogram
        input  [7:0] coin_count ;
        reg  [7:0] coin_count_var ;

        begin
        if (coin_count > 7'b0) begin
            coin_count = coin_count  - 4'b1010;
             .
             .
             .
```

WHAT NEXT

Define a local variable and use that local variable inside the function, as in the following example.

```
    task coin_return_task;
    // synopsys preserve_schedule_subprogram
        input  [7:0] coin_count ;
        reg  [7:0] coin_count_var ;

        begin
        coin_count_var = coin_count;
if (coin_count_var > 7'b0) begin
    coin_count_var = coin_count_var  - 4'b1010;
     .
     .
     .
```

HLS-367 (Warning) The reset of the scheduled design has been changed to %s, overriding the previously specified %s reset.

DESCRIPTION

You receive this message to inform you that the reset of the scheduled design has been changed from synchronous to asynchronous, or vice versa. Normally, this would happen as a result of your executing **set_behavioral_reset** with or without the **-async** option.

When a synchronous reset has been inferred from the code and then you execute **set_behavioral_reset -async**, you receive this message saying that the reset has been changed to asynchronous, overriding the previous synchronous setting.

When an asynchronous reset has been specified by executing **set_behavioral_reset -async** and then you execute **set_behavioral_reset** without the **-async** option, you receive this message saying that the reset has been changed to synchronous, overriding the previous asynchronous setting.

WHAT NEXT

If the specified change is what you intended, no action is required on your part. Otherwise, you can re-execute **set_behavioral_reset** with or without the -async option, to reverse the specification.

SEE ALSO

set_behavioral_reset (2).

HLS-368 (error) You cannot specify %s without also specifying %s.

DESCRIPTION

You receive this message if you execute **set_behavioral_reset** and use one, but not both, of the **-port** and -active options. These options must always be used together.

Of course, you can omit both options. In that case, the defaults are used.

WHAT NEXT

Re-execute **set_behavioral_reset** using either both the **-port** and **-active** options, or neither of those options.

SEE ALSO

set_behavioral_reset (2).

HLS-369 (error) This constraint is illegal because it crosses the subprogram hierarchy.

DESCRIPTION

You receive this message from **set_cycles**, **set_min_cycles**, or **set_max_cycles** if you attempt to place timing constraints on operations that are not in the same level of hierarchy and the same instance of the subprogram. You can place timing constraints only on operations that are in the same level of hierarchy and in the same instance of the subprogram.

WHAT NEXT

Review the design, and reissue the command using a set of constraints that apply to each subprogram instance.

HLS-370 (error) Failed to rebind multiple sequential bindings.

DESCRIPTION

You receive this message if the **schedule** command cannot find valid bindings for an operation that has multiple sequential binding choices; for example, multi-port memory.

WHAT NEXT

Contact Synopsys Technical Support.

HLS-371 (error) Superstate mode violation detected at loop-continue

of %s

DESCRIPTION

When running behavioral synthesis in "super-state" mode, the scheduler is required to make sure that writes in the super-state happen at the end of the super-state, and reads of I/O happen before the writes (and after the writes of the previous super-state). This helps to match simulation behavior.

However, consider the following pseudo-code fragment:

```
while ( <cond> )
    out <= ...
    <<< clock boundary >>>
    out <= ...
end
```

When the loop executes for the second time, the write to port "out" at the end of the loop will conflict with the write to port "out" at the beginning of the loop. In the simulation of the behavioral code, the out at the end of the loop will be over-written by the out at the beginning of the loop. However, because the scheduler will need to insert more states between the beginning and end of the loop, the behavior of the RTL machine generated would be different. The write to port "out" at the end of the loop would then be visible to the outside world for a few cycles.

To avoid this simulation/synthesis mis-match, it is required that there is a clock boundary between writes at the end of the loop and I/O at the beginning.

WHAT NEXT

Insert a clock boundary (wait in VHDL or always @ in verilog) at the end of the loop (after the last write in the loop).

HLS-372 (error) Superstate mode violation detected at loop-entry
of %s

DESCRIPTION

When running behavioral synthesis in "super-state" mode, the scheduler is required to make sure that writes in the super-state happen at the end of the super-state, and reads of I/O happen before the writes (and after the writes of the previous super-state). This helps to match simulation behavior.

However, consider the following pseudo-code fragment:

```
out <= ...
while ( <cond> )
    out <= ...
```

When simulation the behavioral code, the write to port "out" before the loop will be over-written by the write to port "out" after the loop. When the design is scheduled, however, cycles will be inserted at the beginning of the loop which will cause the first write to port "out" to be visible for a few cycles. This would cause a simulation mis-match.

WHAT NEXT

Insert a clock boundary (wait in VHDL or always @ in verilog) just before the loop.

HLS-373 (information) The reset signal will clear all registers.

DESCRIPTION

You receive this information because you have used the **-all** option with the **set_behavioral_reset** command prior to running **schedule** or **bc_check_design**.

When a reset is applied to the synthesized design, all of the registers in the design are cleared.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

set_behavioral_reset (2).

HLS-400 (error) Variable '%s' used in preserve_schedule_subprogram '%s' was not defined locally.

DESCRIPTION

All variables used in preserve_schedule_subprogram should be defined locally. But, signals can be used globally.

```
e.g. CASE1: reg [4:0] tmp; task A; input [4:0] p, q; output [4:0] x; //synopsys
preserve_schedule_subprogram x = p + q + tmp ; <---- error: tmp has not passed in.

CASE2: task A; input [4:0] p, q, tmp; output [4:0] x; //synopsys
preserve_schedule_subprogram x = p + q + tmp ; <---- ok

CASE3: input [4:0] a; task A; input [4:0] p, q; output [4:0] x; //synopsys
preserve_schedule_subprogram x = p + q + a; <---- ok because 'a' is signal

CASE4: output [4:0] o; task A; input [4:0] p, q; //synopsys
preserve_schedule_subprogram o <= p + q; <---- ok because 'o' is signal
```

WHAT NEXT

HLS-401 (error)can not create two preserve (sequential) function with same nane'%s'

DESCRIPTION

When preserve (sequential) function is used, it is treated as a design. We can not have two different design with the same name.

WHAT NEXT

HLS-402 (error) illegal memory usage '%s' in the preserve schedule subprogram '%s'.

DESCRIPTION

When preserve schedule subprogram is shared(Only allowed in Verilog), the memory needs to be sharabled. i.e. It needs to be declared as the same name and same memory type and same address port.

```
module test ( a, b, c, o1, o2, clk, reset );

reg [4:0] mem[4:0],mem1[4:0];

task t;

input [4:0] a, b; //synopsys preserve_schedule_subprogram begin @(posedge clk);
mem[0] = a + b; <---- illegal @(posedge clk); mem1[0] = a- b; <--- illegal @(posedge
clk); end

endtask
```

```
always begin : reset_loop

/* synopsys resource Shr_Mem: variables = "mem1", map_to_module = "DW03_ram1_s_d",
memory_address_ports = "addr"; */

@(posedge clk); if ( reset ) disable reset_loop;

t(a, b); o1 <= mem1[0];

end

always begin : reset_loop_2

/* synopsys resource Shr_Mem: variables = "mem", map_to_module = "DW03_ram1_s_d",
memory_address_ports = "addr"; */

@(posedge clk); if ( reset ) disable reset_loop_2;

t(a, b); o2 <= mem[0];

end

endmodule
```

WHAT NEXT

HLS-403 (information) Operations '%s' and '%s' were not merged into CSA operations because of the mismatch of pins or nets connected between them.

DESCRIPTION

When an addition/subtraction/multiplication tree is transformed into a CSA tree, the intermediate values of the original tree do not exist in the transformed tree. As a result, if there is an incomplete or non-regular connection between operations in the tree, the behavior of the connection would not be able to be performed in the CSA tree. Because **transform_csa** will not alter the bit-accurate behavior of the design, the irregular connection blocks the transformation.

transform_csa command is now obsolete.

WHAT NEXT

No thing needs to be done. **transform_csa** command is now obsolete.

HLS-404 (error) Ignoring execution precedence from '%s' to '%s'.

Removal of Read <-> Write precedences can lead to illegal allocation
of memory bindings (ports). Consult your local Behavior Compiler expert
for further information.

DESCRIPTION

When two memory operations, in which one is read access and thea other is write, use a multi-port memory module with at least one read/write port cannot be performed simultaneoulsly. Consequently, ignoring the memory precedence between them can cause a bad logic.

WHAT NEXT

Do not issue ignore memory precedence command between memory read and write operations.

HLS-405 (error) It is not recommended to uniquify Behavioral Compiler designs before scheduling. Of course, uniquify can be used for post-scheduled designs.

DESCRIPTION

The command uniquify changes the name of design which may cause problems during scheduling.

WHAT NEXT

Do not run the uniquify command before scheduling a Behavioral Compiler design.

HLS-406 (error) Not an array cell.

DESCRIPTION

The ignore_precedence commands only work on array read and write operations.

WHAT NEXT

Check the names of the operations and re-issue the command, if you want to ignore the constraints of array operations. If you want to eliminate constraints on other kinds of operations, you must change your source code to eliminate constraints of data and control precedence.

HLS-407 (error) No reference for array cell.

DESCRIPTION

The cell has no reference.

WHAT NEXT

Check your synthetic libraries and link the design.

HLS-408 (error) Cannot use the array master as a cell

DESCRIPTION

The cell you have named is the array master. It is needed for internal purposes but it is not subject to being constrained.

WHAT NEXT

Find the array read operation or array write operation you want using find -h cell.

HLS-409 (warning) '-use_bit_adder' option cannot be appiled together with '%s'
option. '-use_bit_adder' was ignored.

DESCRIPTION

The -balance_only option transforms an operation tree into a balanced addition tree. The -chain_only option transforms an operation tree into a chained addition tree. In BC-flow, -balance_only is intended for reducing timing while -chain_only is indended for reducing area. Note that -use_bit_adder is meaningful only for optimizing timing in bit level.

WHAT NEXT

Use only one of the options.

HLS-410 (warning) Preserved function '%s' has use_netlist pragma.
The netlist will be used rather than the cached version in library '%s'.

DESCRIPTION

There are multiple possible versions of the function design for **bc_time_design** to use. The use_netlist pragma in the HDL will be honored, rather than using the precompiled function in the designated library.

WHAT NEXT

HLS-411 (error) Variable '%s' is used in preserve_function '%s' but is not defined locally.

DESCRIPTION

All variables used in preserved functions should be defined locally.

WHAT NEXT

HLS-440 (warning) No AND or OR gate in the standard synthetic library.

DESCRIPTION

There is no AND or OR gate in the standard synthetic library. At least one of these gates is necessary to calculate the area costs of operand isolation banks for behavioral synthesis.

WHAT NEXT

Since AND/OR gate descriptions should be in the standard synthetic library, this

error is most likely due to an improper installation of the Synopsys tools. Please contact your system administrator.

HLS-483 (error) Loop ’%s’ cannot be loop pipelined with initiation interval %d because array read/write on %s will be permuted. ’%s’ can occur at the same time or after ’%s’ of the next iteration since there is a minimum timing constraint of %d cycles from %s to %s. Try changing initiation interval to %d.

DESCRIPTION

In loop pipelining, for each RAM, Behavioral Compiler requires that array read and writes in one iteration happen 1 cycle before array writes in the next iteration, and that array writes in one iteration happen 1 cycle before array reads in the next iteration.

WHAT NEXT

Increase initiation interval.

HLS-495 (error) Loop %s cannot be loop pipelined with initiation interval %d because the array operation ’%s’ must be no later than %d cycles after the operation ’%s’. This implies a minimum delay of %d cycles from %s to %s. However, this violates the timing constraint of

%d cycles from %s to %s.

DESCRIPTION

WHAT NEXT

HLS-496 (error) Loop %s cannot be loop pipelined with initiation interval %d
because the array operation '%s' must be no later than %d cycles after the operation '%s'.
This implies a minimum delay of %d cycles from %s to %s
However, this is unsatisfiable because %s
is fixed at cycle %d, and %s is fixed at cycle %d.

DESCRIPTION

WHAT NEXT

HLS-497 (Error) %s constraint involving non-loop preserve_schedule_subprogram
'%s' and a cell which is not in the subprogram is not supported.

DESCRIPTION

With respect to cells, a timing constraint must be placed in the same level of design hierarchy.

WHAT NEXT

HLS-498 (warning) Resource '%s' of memory '%s' specified in .sl file
never be maximally utilized. At most %d of the resource can be

used
in parallel by the port bindings.

DESCRIPTION

In order to maximally utilize the resource, increase the number of ports.

WHAT NEXT

HLS-499 (error) All %s licenses are already in use. The %s command needs such a license.

DESCRIPTION

The optimize_registers and pipeline_design commands require license of the type specified in the error message. All available licenses of this type at your site are currently in use.

WHAT NEXT

Wait until a license of this type at your site is freed.

HLS-500 (error) You need a license for %s to enable the %s command.

DESCRIPTION

The optimize_registers and pipeline_design commands require a special license for which no key is available at your site.

WHAT NEXT

If you want to use these features purchase the above mentioned license from Synopsys.

HLS-501 (error) Clock was not defined in binding '%s' of

memory ’%s’.

DESCRIPTION

For each binding of memory, a (single) clock must be defined.

WHAT NEXT

Check the binding of the memory module.

HLS-502 (error) Address port name was not defined in binding ’%s’ of memory ’%s’.

DESCRIPTION

For each binding of memory, the address port name must be defined.

WHAT NEXT

Check the binding of the memory module.

HLS-503 (error) Multiple clocks were defined in binding ’%s’ of memory ’%s’.

DESCRIPTION

For each binding of memory, one and only one clock must be defined.

WHAT NEXT

Check the binding of the memory module.

HLS-504 (error) Operation(s) specified in timing constraints command are signal probe(s).

DESCRIPTION

In **set_cycles**, **set_max_cycles**, or **set_min_cycles**, no schedulable from or to

operation was specified. The specified operation(s) is a signal probe.

WHAT NEXT

Check the operations (cells) used in the timing constraint commands. Check the output of the **find (cell ..)** command if it was used.

HLS-505 (warning) A timing constraint cannot be set on '%s', which is a signal probe.

DESCRIPTION

A timing constraint cannot be set from or to a signal probe when using **set_cycles**, **set_max_cycles**, or **set_min_cycles**. If a signal probe is specified, it is ignored.

WHAT NEXT

Check the operation(s) specified in the **set_cycles**, **set_max_cycles**, or **set_min_cycles** commands. Check the output of the **find (cell, ..)** command if it was used.

HLS-506 (warning) A timing constraint cannot be set on '%s', which is a signal probe.

DESCRIPTION

A signal probe is ignored from the list of specified operations that may or may not be chained using **chain_operations**, **dont_chain_operations**, or **bc_dont_chain**.

WHAT NEXT

Check the operation(s) specified in **chain_operations**, **dont_chain_operations**, and **bc_dont_chain**. Check the output of the **find (cell, ..)** command if it was used.

HLS-507 (error) All operations specified in chain/dont_chain

command are signal probes.

DESCRIPTION

In **chain_operations**, **dont_chain_operations**, or **bc_dont_chain**, no schedulable operations were specified. All specified operations are signal probes.

WHAT NEXT

Check the operations (cells) used in the **chain** and **dont_chain** commands. Check the output of 'find (cell ..)' command, if it were used.

HLS-508 (warning) A timing constraint cannot be set on '%s', which is a signal probe.

DESCRIPTION

A signal probe is ignored from the list of specified operations in **unschedule** and **preschedule** commands.

WHAT NEXT

Check the operation(s) specified in **unschedule** or **preschedule** commands. Check the output of the **find (cell, ..)** command if it was used.

HLS-509 (error) All operations specified in unschedule/ preschedule command are signal probes.

DESCRIPTION

In **unschedule** or **preschedule**, no schedulable operations were specified. All specified operations are signal probes.

WHAT NEXT

Check the operations (cells) used in the **chain** and **dont_chain** commands. Check the output of the **find (cell ..)** command if it was used.

HLS-510 (error) Error in specifying port '%s' of the preserved

function at line ’%d’. ’%s’

DESCRIPTION

There was an error in specifying a port of a preserved function. Possible causes of the error include:

1. The port direction was not specified.
2. The port has multiple definitions.
3. The port is a return value, which cannot be used in preserve functions.

WHAT NEXT

Check the definition of the preserved function.

HLS-511 (error) You cannot specify both "preserved_functions" and "-exclude preserved_functions" at the same time.

DESCRIPTION

You receive this message if you have issued either **compile_preserved_functions** or **read_preserved_function_netlist** and have specified both *preserved_functions* and **-exclude** *preserved_functions*. These two options are mutually exclusive.

WHAT NEXT

Re-issue the command and specify only one of the above options.

SEE ALSO

compile_preserved_functions (2), **read_preserved_function_netlist** (2).

HLS-512 (error) Invalid argument %s specified for command option
-compile_effort.

DESCRIPTION

You receive this message if you execute **compile_preserved_functions** and specify an invalid argument for the **-compile_effort** option. Valid arguments are *low, 1, medium, 2, high, and 3*.

WHAT NEXT

Re-issue **compile_preserved_functions** and use one of the valid arguments for the **-compile_effort** option.

SEE ALSO

compile_preserved_functions (2).

HLS-513 (error) You have specified two or more options that cannot be used together.

DESCRIPTION

You receive this message if you issue **compile_preserved_functions** with two or more options that cannot be used together; these options are as follows:

-compile_effort
-include_script
-no_compile

WHAT NEXT

Re-issue **compile_preserved_functions** and specify only one of the above options.

SEE ALSO

compile_preserved_functions (2).

HLS-514 (warning) No preserved functions were found in ‘%s.’

DESCRIPTION

‘compile_preserved_functions’ or ‘read_preserved_function_netlist’ command will by default process all preserved functions in the current design. However, no preserved functions were found.

WHAT NEXT

Check if ‘preserve_function’ pragma is set on function(s) to be preserved. Also check if ‘use_netlist’ pragma were set, and if there were errors while reading the external netlist.

HLS-515 (warning) The command ‘%s’ with the ’-no_compile’ option has no effect without also specifying the ’-write’ option.

DESCRIPTION

You receive this message if you issue **compile_preserved_function** with the **-no_compile** option, but not with the **-write** option. The **-no_compile** option is intended to be used if you want only to write elaborated or compiled db files of preserved function designs. You must use the **-no_compile** option if you invoke **compile_preserved_functions** after scheduling.

WHAT NEXT

If you want to write an elaborated or compiled db file of a preserved function design without actually compiling it, re-issue **compile_preserved_function** using both the **-no_compile** and **-write** options.

SEE ALSO

compile_preserved_function (2).

HLS-516 (warning) Skipping ‘%s’, because a mapped netlist for this preserved function was detected.

DESCRIPTION

You receive this message if you have issued **compile_preserved_functions** or **read_preserved_function_netlist** and have specified a preserved function whose design in memory is already a mapped netlist. These commands do not replace the existing design of a preserved function in memory if the design is a mapped netlist.

WHAT NEXT

If you receive this warning, do one of the following:

1. Remove the preserved function from the list of objects to be processed, if a list of objects is specified.

2. Specify the preserved function in the list of objects to be excluded.

3. Use the **-force_recompile** or **-force_reload** options to replace the design in the memory.

SEE ALSO

compile_preserved_functions (2), **read_preserved_function_netlist** (2).

HLS-517 (information) Calling '%s' on preserved function '%s'

DESCRIPTION

This message informs you that the **compile_preserved_functions** command is calling the script you specified with the **-include_script** option. Commands in the specified script will be executed on each of the preserved functions currently being processed by the command.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

compile_preserved_functions (2).

HLS-518 (error) The filename option may not be applied to multiple preserved functions.

DESCRIPTION

Behavioral Compiler only supports one netlist per file. Therefore, it is not possible to apply the filename option to more than one preserved function at a time.

WHAT NEXT

If your design contains multiple preserved functions that you want to write out, you have to call compile_perserved_functions for each of those functions seperately.

HLS-519 (information) Designs will be written to design library '%s.'

DESCRIPTION

This message informs you that the **compile_preserved_functions** command is writing the

design to the library you specified with the **-design_library** option, instead of to the default design library. The design can be read from the design library in using the **read_preserved_function_netlist** command.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

compile_preserved_functions (2), **read_preserved_function_netlist** (2).

HLS-520 (error) You cannot use the -force_recompile and -no_compile options together.

DESCRIPTION

You receive this message if you issue **compile_preserved_functions** with both the **-force_recompile** and **-no_compile** options. These options are mutually exclusive.

WHAT NEXT

Re-issue **compile_preserved_functions** and use only one of the two options.

SEE ALSO

compile_preserved_functions (2).

HLS-521 (error) You cannot use the '-include_script' option, because the preserved function '%s' contains an embedded script.

DESCRIPTION

You receive this message if you have issued **compile_preserved_functions** with the **-include_script** option, and the specified preserved function contains an embedded script. The constraints in the two scripts could potentially conflict with each other.

WHAT NEXT

Either remove the embedded script from the preserved function, or re-issue **compile_preserved_functions** without the **-include_script** option.

HLS-522 (warning) Existing design for preserved function

DESCRIPTION

You receive this warning message if your existing design is a mapped netlist and you issue **compile_preserved_functions** with the **-force_recompile** option, or **read_preserved_function_netlist** with the **-force_reload** option.

By default, if the existing design of a preserved function is a mapped netlist, that design is not overwritten. This message warns you that the existing design will be overwritten, because the **-force_recompile** or **-force_reload** option was used to override the default behavior.

WHAT NEXT

If you intended that the existing design for the specified preserved function be overwritten, no action is required on your part. Otherwise, to prevent this warning, do one of the following:

1. If the specified preserved function is on the list of objects to be processed, remove it.

2. Add the specified preserved function to the list of objects to be excluded.

3. Remove the **-force_recompile** or **-force_reload** option.

SEE ALSO

compile_preserved_functions (2), **read_preserved_function_netlist** (2).

HLS-523 (information) Compiling preserved function ‘%s’ with %s effort.

DESCRIPTION

This message informs you that the **compile_preserved_functions** command is using the level of compile effort you specified with the **-compile_effort** option. The default is *medium*.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

compile_preserved_functions (2).

HLS-524 (error) You cannot use the -netlist_file_name and -return_port options if you specify more than one preserved function.

DESCRIPTION

You receive this message if you issue the **read_preserved_function_netlist** command with one or both of the options **-netlist_file_name** and **-return_port**, and more than one preserved function has been specified. You can use these options only for a single preserved function.

Multiple preserved functions would be specified if you did not use the **preserved_functions** option. By default, if you do not specify the *preserved_functions* list, netlists are read for all preserved functions in the current top-level design.

WHAT NEXT

To correct this error, do one of the following:

1. If you want to use the **-netlist_file_name** and/or the **-return_port** options, re-issue the **read_preserved_function** command using the *preserved functions* option to specify a single preserved function.

2. If you want to use multiple preserved functions, re-issue the **read_preserved_function** command and do not use the **-netlist_file_name** and **-return_port** options. In that case, the following default values are used:

-netlist_file_name	*preserved_function_name*.db
-return_port	*preserved_function_name*-return

SEE ALSO

read_preserved_function_netlist (2).

HLS-525 (error) The preserved function ‘%s’ has the same

name as a synthetic operator in the synthetic library.

DESCRIPTION

You receive this message if a preserved function has the same name as that of a synthetic operator in the synthetic library. The name of the preserved function must be unique and unused by any operators in your synthetic library.

WHAT NEXT

If you receive this message, do one or more of the following:

1. Change the name of the preserved function so that it does not conflict with names of operators in your synthetic library.

2. If you are using the map_to_operator **oper** pragma to use a DesignWare component, ensure that **oper** is not a preserved function.

3. Change the synthetic library. Using this solution, however, could cause some operators in the design not to be found, which could cause an error message to be generated.

HLS-526 (error) After scheduling, you cannot invoke ‘compile_preserved_functions’ without using the ‘-no_compile’ option.

DESCRIPTION

You receive this message if you schedule your design and then invoke the **compile_preserved_functions** command without the **-no_compile** option. After scheduling, you cannot recompile the preserved function, because the timing might change and invalidate the current schedule. Thus, after scheduling you can use **compile_preserved_functions** only to write the preserved function’s netlist to a db file. In that case, you must use both the **-no_compile** and **-write** options.

WHAT NEXT

If you receive this message, do one of the following:

1. If you want to write the preserved function’s netlist to a db file, re-issue **compile_preserved_functions** using both the **-no_compile** and **-write** options.

2. If you need to recompile the preserved function, restart with the

elaborated db.

HLS-527 (error) The ‘read_preserved_function_netlist’ command cannot be invoked for preserved function ‘%s’ because the ‘use_netlist’ pragma was used in the latter.

DESCRIPTION

You receive this message if you attempt to read a netlist for a preserved function that has the **use_netlist** pragma. If you use the **use_netlist** pragma to read an external netlist for a preserved function, you cannot use the **read_preserved_function_netlist** command for that preserved function, because there could be a conflict between the two external netlists, and/or parameters (for example, **design_name** and **return_port**).

WHAT NEXT

Remove the **use_netlist** pragma from the preserved function and reanalyze and reelaborate the source file(s). Then reexecute **read_preserved_function_netlist**.

SEE ALSO

read_preserved_function_netlist (2).

HLS-528 (error) Preserved function ‘%s’ specified in the list of preserved functions to be processed or excluded, does not exist in the current top-level design ‘%s.’

DESCRIPTION

You receive this message if you issue the **compile_preserved_functions** or the **read_preserved_function_netlist** command, and one of the functions on the *preserved_functions* list cannot be found in the current top-level design. If you did not use the *preserved_functions* argument, by default the command attempts to process all preserved functions in the current top-level design.

This error could be caused by a misspelling or a typo, or by the presence of the **use_netlist** pragma on the preserved function, accompanied by an error reading the

netlist.

WHAT NEXT

If you receive this message, do one of the following:

1. Verify the correct spelling of the preserved function, and correct it if necessary.

2. Remove the specified preserved function from the list of preserved functions to be processed or excluded.

3. Remove the **use_netlist** pragma from the specified function.

SEE ALSO

compile_preserved_functions (2), **read_preserved_function_netlist** (2).

HLS-529 (error) Unable to read netlist file ‘%s’ in the default design library for preserved function ‘%s.’

DESCRIPTION

You receive this message if the **read_preserved_function_netlist** command cannot find the specified preserved function netlist in the default design library, or if the file is unreadable. This error could be caused by a misspelling or a typo, or by a read protection on the file.

WHAT NEXT

Verify that the specified netlist file exists in the directory to which the default design library is mapped, and is readable. Verify the correct spelling. Then reexecute **read_preserved_function_netlist**.

SEE ALSO

read_preserved_function_netlist (2).

HLS-530 (error) Unable to find design ‘%s’ in netlist file ’%s’

in design_library ’%s’ for preserved function ‘%s.’

DESCRIPTION

You receive this message if a design with the same name as the specified preserved function cannot be found in the netlist file in the specified design library. This error could be caused by a misspelling or a typo.

WHAT NEXT

Ensure that the specified netlist file contains the name of a design that is exactly the same as the name of the specified preserved function. Then reexecute **read_preserved_function_netlist**.

SEE ALSO

read_preserved_function_netlist (2).

HLS-531 (error) Unable to read the file ‘%s’ for preserved function ‘%s’
using design_library ‘%s’ which is mapped to ‘%s’.

DESCRIPTION

You receive this message if the **read_preserved_function_netlist** command cannot find the specified preserved function netlist in the specified design library, or if the file is unreadable. This error could be caused by a misspelling or a typo, or by a read protection on the file.

WHAT NEXT

Verify that the specified netlist file exists in the directory to which the specified design library is mapped, and is readable. Verify the correct spelling. Then reexecute **read_preserved_function_netlist**.

SEE ALSO

read_preserved_function_netlist (2).

HLS-532 (information) Using the design in netlist ‘%s’

in library ‘%s’ for preserved function ‘%s.’

DESCRIPTION

This message informs you that the **read_preserved_functions_netlist** command is reading the design in the netlist file *preserved_function_name*.db, located in the specified design library. The design is expected to be a non-hierarchical mapped netlist.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

read_preserved_function_netlist (2).

HLS-533 (error) Cannot link the external netlist ‘%s.’

DESCRIPTION

You receive this message if **read_preserved_function_netlist** cannot link an external netlist for a preserved function. One of several possible reasons for this error to occur is that the link and target libraries used in the external netlist are not found in the search path of the current top-level design.

WHAT NEXT

Inspect the link and target libraries used in the external netlist, and ensure that they exist in the search path of the current top-level design. Then reexecute **read_preserved_function_netlist**.

SEE ALSO

read_preserved_function_netlist (2).

HLS-534 (error) No %s library is set for the current top-level design ‘%s.’

DESCRIPTION

You receive this message if you execute **read_preserved_function_netlist** and the link

library or the target library is not set for the current top-level design. You set these using the **link_library** and **target_library** variables.

WHAT NEXT

Use the **link_library** or **target_library** variable to set the link or target library for the current top-level design.

SEE ALSO

read_preserved_function_netlist (2); **link_library** (3), **target_library** (3).

HLS-535 (warning) No link or target library is set for the netlist ‘%s.’

DESCRIPTION

You receive this message if you execute **read_preserved_function_netlist** and the link library or the target library is not set for the netlist. This might also imply that the external netlist is unmapped.

WHAT NEXT

Ensure that the external netlist is mapped to a link library or a target library. Use the **link_library** or **target_library** variable to set the link or target library for the netlist.

SEE ALSO

read_preserved_function_netlist (2); **link_library** (3), **target_library** (3).

HLS-536 (error) The library ‘%s’ used by the external netlist ‘%s’ is not used by the current top-level design ‘%s.’

DESCRIPTION

You receive this message from **read_preserved_function_netlist** if the external netlist uses a library not used by the top-level design. In this case, the final physical synthesis of the top-level design might be unsuccessful.

WHAT NEXT

Ensure that the external netlist is mapped only to libraries used by the top-level design. Alternatively, add the additional libraries used by the the external netlist to the libraries used by the top-level design.

SEE ALSO

read_preserved_function_netlist (2).

HLS-537 (error) The external netlist ‘%s’ is %s. It contains a %s ‘%s.’

DESCRIPTION

You receive this message from the **read_preserved_function_netlist** command if the external netlist you specified does not meet one or more of these requirements: The netlist must be nonhierarchical. Its target library must be included in the set of target libraries of the current top-level design. It cannot contain any generic logic components or synthetic operators.

WHAT NEXT

Be sure that the external netlist is correct according to the stated requirements. If the external netlist is not available, you can compile the preserved function using the **compile_preserved_functions** command.

SEE ALSO

compile_preserved_functions (2), **read_preserved_function_netlist** (2).

HLS-538 (information) Writing preserved function ‘%s’ to file ‘%s.’

DESCRIPTION

This message informs you that the **compile_preserved_functions** command is writing the design to a file *preserved_function_name*.db in the default design library, because you specified the **-write** option.

WHAT NEXT

This is an informational message only. No action is required on your part, unless

you want the file to be written to a library other than the default design library. In that case, reexecute **compile_preserved_functions -write** and also use the **-design_library** option.

SEE ALSO

compile_preserved_functions (2).

HLS-539 (information) Using the design in netlist '%s' in the default design library for preserved function '%s.'

DESCRIPTION

This message informs you that the **read_preserved_functions_netlist** command is reading the design in the netlist file *preserved_function_name*.db, located in the default design library. The design is expected to be a non-hierarchical mapped netlist.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

read_preserved_function_netlist (2).

HLS-540 (warning) Cannot specify a return port for preserved function '%s', because it has more than one output port. Ignoring the specified return port '%s'.

DESCRIPTION

You receive this warning message if you use the **-return_port** option of **read_preserved_function_netlist** to specify the return port, but the specified preserved function has more than one output port. In this case, Behavioral Compiler cannot identify the output port whose name is to be changed.

WHAT NEXT

Either re-issue **read_preserved_function_netlist** without the **-return_port** option, or modify the preserved function so that it has only one output port.

SEE ALSO

read_preserved_function_netlist (2).

HLS-541 (information) Using port ‘%s’ from netlist ‘%s’ as return port for preserved function ‘%s.’

DESCRIPTION

This message is issued in ‘read_preserved_function_netlist’ command if the ‘-return_port’ option or ‘return_port_name’ pragma is not used to specify the return port for a preserved function, and the default output port of the function does not match with the output port of the netlist. In this case, the output port of the netlist is used.

WHAT NEXT

You may specify the output port in the netlist as the return port of the preserved function in ‘read_preserved_function_netlist’ command.

HLS-542 (error) Preserved function ‘%s’ could not be compiled using the script ‘%s.’

DESCRIPTION

This message is issued in ‘compile_preserved_functions’ command if the ‘-include_script’ option is used, and if the preserved function is not compiled. After executing commands in the specified script in order to compile the preserved function, a mapped netlist for the latter was not generated. A possible reason for this is an explicit ‘compile’ command was not given in the specified script.

WHAT NEXT

Please make sure that the user-specified script used to compile the preserved function contains a ‘compile’ command. The ‘compile’ command may be invoked in the default mode or with options.

HLS-543 (error) The ‘read_preserved_function_netlist’ command

cannot be invoked after scheduling.

DESCRIPTION

The ‘read_preserved_function_netlist’ command can be invoked after ‘elaborate -schedule’ or ‘bc_time_design,’ but not after scheduling is complete. Replacing the netlist of a preserved function may change its timing which could make the present schedule invalid.

WHAT NEXT

Please do not invoke ‘read_preserved_function_netlist’ after scheduling. If a new netlist for a preserved function must be used, re-start with the timed db of the top-level design, elaborated db, or ‘elaborate -schedule.’

HLS-544 (warning) The ‘use_netlist’ pragma is being phased out, and will not be supported after the v2000.05 release. Please use ‘read_preserved_function_netlist’ instead.

DESCRIPTION

You receive this message if you use the use_netlist pragma in a preserved function to read an external netlist for its design. This pragma is being phased out and will not be supported after the v2000.05 release; it has been replaced by the command **read_preserved_function_netlist**.

WHAT NEXT

To avoid this warning, remove the use_netlist and return_port_name pragmas from the preserved function. After executing **elaborate -schedule** on the top-level design, invoke **read_preserved_function_netlist**, specifying the netlist name and the return port name as command options.

SEE ALSO

elaborate (2), **read_preserved_function_netlist** (2).

HLS-545 (warning) The variable ‘%s’

is no longer supported.

DESCRIPTION

This message is issued when the variable that determines the map/compile effort of preserved functions is set. This variable is no longer supported, and its value will not affect the map effort of preserved functions. In order to compile preserved functions with the desired map effort, a new command ‘compile_preserved_functions’ can be used with the desired compile effort specified as a command option.

WHAT NEXT

To avoid this warning, please remove the above variable from the Synopsys DC setup file and your compilation scripts.

HLS-546 (error) The options ‘-cache_preserved_functions’ and ‘-except’ are no longer supported in ‘bc_time_design.’

DESCRIPTION

This error is reported in ‘bc_time_design’ if any of the above two options to cache a preserved-function design are used. The feature to cache preserved-function designs during ‘bc_time_design’ is now obsolete. Please use the new command ‘compile_preserved_functions’ to compile and write a netlist for a preserved function, and ‘read_preserved_function_netlist’ to read a pre-compiled netlist.

WHAT NEXT

Please remove ‘-cache_preserved_functions’ and/or ‘-except’ from ‘bc_time_design.’

HLS-547 (error) The options ‘-use_cached_preserved_functions’ and ‘-recompile’ are no longer supported in ‘bc_time_design.’

DESCRIPTION

This error is reported in ‘bc_time_design’ if any of the above two options to read a cached preserved-function design are used. The feature to cache preserved-function designs during ‘bc_time_design’

is now obsolete. Please use the new command
'compile_preserved_functions' to compile and write a netlist for a
preserved function, and 'read_preserved_function_netlist' to read a
pre-compiled netlist.

WHAT NEXT

Please remove '-use_cached_preserved_functions' and/or '-recompile'
from 'bc_time_design.'

HLS-548 (warning) The design has a comparison operation that compares values of type std_logic_vector. This is ambiguous. For more specific line information, please re-analyze with "bc_enable_analysis_info = true".

DESCRIPTION

BC is not able to map to any operator for this type of comparison operation. This is because the type of variables that are compared is not clearly defined for comparison. For example, BC will not figure out what kind of comparator should be used for std_logic_vector variables, because the values could be interpreted as signed or as unsigned. This might cause simulation mismatches!

If for example a and b are defined as std_logic_vector, then the following statement is ambiguous

```
if (a < b) then
```

change it into e.g.

```
if (signed(a) < signed(b)) then
```

WHAT NEXT

Check the hdl code for the types of variables used in comparison operations. The type have to be clear such as signed or unsigned. ~

HLS-549 (error) Failed to compile preserved functions.

DESCRIPTION

You receive this error message because the **compile_preserved_functions** command failed to complete.

WHAT NEXT

The output of the **compile_preserved_functions** command contains other warnings and errors that identify the problem. Refer to the man pages for those warnings and errors to solve the problem.

SEE ALSO

compile_preserved_functions (2).

HLS-550 (error) Can’t find %s port ’%s’ for design ’%s’.

DESCRIPTION

Behavioral Compiler couldn’t find a port with the given name in the design.

WHAT NEXT

Please specify a valid choice.

HLS-551 (error) Port ’%s’ of design ’%s’ has unsupported type inout.

DESCRIPTION

Behavioral Compiler does currently not support pipelined netlists with inout ports.

WHAT NEXT

Please modify the netlist such that it does not contain inout ports.

HLS-552 (error) Port ’%s’ of design ’%s’ has unknown type.

DESCRIPTION

Behavioral Compiler currently only supports pipelined netlists with input and output ports. Behavioral Compiler is not able to determine the type of the port that is mentioned in the error message.

WHAT NEXT

Please check the netlist and make sure that all port types are specified appropriately.

HLS-553 (error) You may not specify %s without specifying %s.

DESCRIPTION

Some options may only be used in combination with others.

WHAT NEXT

Please make sure that you only use valid combinations of command options.

HLS-554 (error) %s has to be %s.

DESCRIPTION

The value you specified for the option is illegal.

WHAT NEXT

Please specify a legal value.

HLS-555 (error) Inconsistent stage count for %s ’%s’.

DESCRIPTION

Behavioral Compiler found an output port or a sequential element that can be reached from two different input ports through paths containing different numbers of sequential elements. Behavioral Compiler currently only supports those kinds of pipelined parts where the number of stages from every input to every output is the same.

WHAT NEXT

Please create a pipelined component that satisfies Behavioral Compiler’s requirements.

HLS-556 (error) Found loop containing cell '%s'.

DESCRIPTION

Behavioral Compiler found a loop in the pipelined component. This is currently not supported.

WHAT NEXT

Please create a pipelined component that satisfies Behavioral Compiler's requirements.

HLS-557 (error) Inconsistent number of pipeline stages in netlist %s.

DESCRIPTION

Behavioral Compiler found two output ports, that can be reached from input ports using different numbers of sequential elements. THis is in conflict with Behavioral Compiler's requirements for pipelined components that all inputs have to be available at the same time and that all outputs have to be computet at the same time.

WHAT NEXT

Please create a pipelined component that satisfies Behavioral Compiler's requirements.

HLS-558 (error) Found control register '%s' in netlist '%s'.

DESCRIPTION

Behavioral Compiler found a sequential element, that is not part of the datapath. Behavioral Compiler only supports netlists without any internal control.

WHAT NEXT

Please create a pipelined component that satisfies Behavioral Compiler's requirements.

HLS-559 (error) The %s '%s' doesn't match name of the %s '%s' defined for netlist '%s'.

DESCRIPTION

Behavioral Compiler found conflicting specifications for the clock port of the pipelined netlist. This can happen if a port of the netlist (e.g. clock1) has been specified as being a clock port using the create_clock command, while the clock_port_name option specifies another port.

WHAT NEXT

Please make sure that you provide Behavioral Compiler with a consistent clock specification.

HLS-560 (error) Cannot find clock port %s for design %s.

DESCRIPTION

Behavioral Compiler did not find the clock port you specified.

WHAT NEXT

Please make sure that you provide Behavioral Compiler with a valid name for the clock port.

HLS-561 (error) Clock port %s for design %s is not an input port.

DESCRIPTION

The port you specified as being the clock port is not an input port.

WHAT NEXT

Please make sure that you provide Behavioral Compiler with a valid name for the clock port.

HLS-562 (error) Cannot find reset port %s for design %s.

DESCRIPTION

Behavioral Compiler did not find the reset port you specified.

WHAT NEXT

Please make sure that you provide Behavioral Compiler with a valid name for the reset port.

HLS-563 (error) Reset port %s for design %s is not an input port.

DESCRIPTION

The port you specified as being the reset port is not an input port.

WHAT NEXT

Please make sure that you provide Behavioral Compiler with a valid name for the reset port.

HLS-564 (error) You may specify only one of %s.

DESCRIPTION

You specified two incompatible options.

WHAT NEXT

Please make sure that you provide Behavioral Compiler with compatible options.

HLS-565 (warning) Assuming clock type is positive edge.

DESCRIPTION

Since the type of the clock has not been specified, Behavioral Compiler will assume that the sequential elements of your design are being triggered by the positive edge of the clock.

WHAT NEXT

Please make sure that the assumptions of Behavioral Compiler meet your requirements.

HLS-566 (error) The pipelining properties of netlist %s have already
been determined. You may not specify any pipelining options.

DESCRIPTION

The netlist you are reading in for the preserved function has already been attributed with all the necessary pipelining properties. Behavioral Compiler is not able to handle - potentially conflicting - pipelining directives provided at the command line.

WHAT NEXT

Please call read_preserved_function_netlist again without any option regarding pipelining, ie. without clock_port_name, clock_edge, sync_reset_name, async_reset_name or reset_polarity.

HLS-567 (error) You specified pipelining options even though netlist
%s does not contain any sequential elements.

DESCRIPTION

The netlist read by Behavioral Compiler does not contain any sequential element. This conflicts with the pipelining options you specified, ie. at least one of clock_port_name, clock_edge, sync_reset_name, async_reset_name or reset_polarity,

WHAT NEXT

Please call read_preserved_function_netlist again without any pipelining related options.

HLS-568 (warning) Skipping netlist %s, it already contains

sequential elements.

DESCRIPTION

The netlist contains sequential elements. This is not allowed when pipelining Behavioral Compiler using the compile_preserved_functions command.

WHAT NEXT

Please read in the original, combinatorial netlist and apply compile_preserved_functions to it.

HLS-569 (warning) No clock period has been specified, pipelining %s for minimum clock period.

DESCRIPTION

You did not specify a clock period to be used for pipelining the preserved function. Behavioral Compiler also did not find a clock at either the top level design or at the preserved function. Therefore, the pipelined component will be built to achieve the minimum clock period.

WHAT NEXT

If you would like the preferved function to be pipelined for a particular clock period, please create a clock for the design or specify the period option for the compile_preserved_functions command.

HLS-570 (Information) Netlist %s is pipelined component with %d stages.

DESCRIPTION

Behavioral Compiler identified the netlist as being a pipelined component.

WHAT NEXT

No further action is required.

HLS-571 (Error) No clock port has been specified for sequential netlist %s.

DESCRIPTION

Behavioral Compiler determined that the netlist contains sequential elements. To be able to check the pipelining properties of the netlist you have to specify the clock port as well as the reset port if applicable.

WHAT NEXT

Please specify the clock port and reset port using the command options.

HLS-572 (warning) The reset synchronicity of sequential component %s is different from the one of the design.

DESCRIPTION

This message is issued when the sequential component from preserve function has a synchronous reset and BC design has an asynchronous reset or vice versa.

WHAT NEXT

Please check the reset synchronicity is defined correctly.

HLS-573 (warning) The reset polarity of sequential component %s is different from the one of the design.

DESCRIPTION

This message is issued when the sequential component from preserve function has an active high reset and BC design has an active low reset or vice versa.

WHAT NEXT

Please check the reset polarity of either sequential component or the design.

HLS-574 (warning) The clock polarity of sequential component

%s is different from the one of the design.

DESCRIPTION

This message is issued when the sequential component from preserve function has a rising edge clock and BC design has a falling edge clock or vice versa.

WHAT NEXT

Please check clock polarity of either sequential component or the design.

HLS-575 (error) When selecting any pipelining related option, you may specify neither ’include_script’ nor ’no_compile’.

DESCRIPTION

The pipelining features of compile_preserved_functions require Behavioral Compiler to compile the netlist to be pipelined. Therefore, it is not possible to use pipelinineg related options together with the no_compile option. There are two ways to pipeline a netlist using compile_preserved_functions. You can either use a pipelining option or use an include script that calls the pipeline_design command. You may not combine those two approaches.

WHAT NEXT

Please call compile_preserved_functions with options that do not conflict with each other.

HLS-576 (error) The filename may not be hierarchical.

DESCRIPTION

When using the filename option of compile_preserved_functions or read_preserved_function_netlist, the name provided may not be hierarchical. Behavioral Compiler uses the design_library option to determine the directory of a file.

WHAT NEXT

Please call compile_preserved_functions or read_preserved_function_netlist again using a non-hierarchical filename.

HLS-577 (error) You may not specify an input_delay or output_delay when selecting the include_script option.

DESCRIPTION

When specifying an include_script, all constraints you want to apply to the preserved function have to be specified as part of the include_script.

WHAT NEXT

Please add the commands for applying input and output delay constraints to the include_script.

HLS-578 (error) No clock period defined for design %s.

DESCRIPTION

You receive this message because you invoked the **compile_preserved_functions** command without an *-include_script* argument. In this situation, Behavioral Compiler requires that you specify the clock period for the design.

WHAT NEXT

Use the **create_clock** command first before you invoke the **compile_preserved_functions** command.

SEE ALSO

compile_preserved_functions (2), **create_clock** (2), **compile** (2), **pipeline_design** (2), **create_port** (2).

HLS-579 (error) Cannot find the behavioral %s '%s' in the library '%s'.

DESCRIPTION

You receive this message because the behavioral design unit given is not in the library specified, and therefore could not be found for behavioral elaboration.

WHAT NEXT

You can use the **report_design_lib** command to determine the contents of a library.

If the design unit is not present, reanalyze the design unit by using the **analyze** command with the **-library** or **-work** option.

This problem also arises if you have set the dc_shell **hdlin_enable_presto** variable to *true* prior to running the **analyze** command on files containing behavioral design units. Set the dc_shell **hdlin_enable_presto** variable to *false* or use the **analyze** command with the **-schedule** option when analyzing files containing behavioral design units.

SEE ALSO

analyze (2), **report_design_lib** (2), ,B hdlin_enable_presto (3).

HLS-580 (error) Behavioral subprogram body or architecture for '%s' was not defined %s.

DESCRIPTION

You receive this message because, during elaboration for scheduling,
a subprogram is called in the design, but the subprogram body is missing.

This error also occurs when you elaborate a design for which no architecture
has been specified.

WHAT NEXT

Include the missing subprogram body or design architecture and
re-analyze the design files.

This problem also arises if you have set the dc_shell
hdlin_enable_presto variable to *true* prior to running
the **analyze** command on files containing behavioral design units.
Set the dc_shell **hdlin_enable_presto** variable to *false*
or use the **analyze** command with the **-schedule** option
when analyzing files containing behavioral design units.

SEE ALSO

analyze (2), **hdlin_enable_presto** (3).

HLS-581 (information) Possibly you did not analyze the missing %s with 'analyze -schedule'.

DESCRIPTION

You receive this message because the behavioral design unit given is not in the library specified; or it has not been analyzed with the option **-schedule** and, therefore, could not be found for behavioral analysis.

WHAT NEXT

You can use the **report_design_lib** command to determine the content of a library. If the design unit is not present, reanalyze the design unit by using the **analyze** command with the **-schedule** option and either the **-library** option or the **-work** option. Instead of using the **analyze** command described above, you can set the dc_shell **hdlin_enable_presto** variable to *false*.

SEE ALSO

analyze (2), **report_design_lib** (2), **hdlin_enable_presto** (3).

HLS-582 (error) Failed to compute timing margin.

DESCRIPTION

You receive this error message because the **bc_margin** command failed to compute the timing margin.

WHAT NEXT

The output of the **bc_margin** command contains other warnings and errors that identify the problem. Refer to the man pages for those warnings and errors to solve the problem.

SEE ALSO

bc_margin (2).

HLS-600 (error) Design '%s' is not a top-level behavioral design.

DESCRIPTION

The command you are trying to execute works only when your current design is a top-level behavioral module, elaborated with the **elaborate -s** command or the **compile_systemc** command.

Your current design is not a top-level behavioral module.

WHAT NEXT

From your behavioral source file, get the name of your behavioral module. Use the **current_design** command to set the current design to the name of that module.

Use the **list_designs** command to view a list of all designs contained in dc_shell.

SEE ALSO

current_design (2), **list_designs** (2).

HLS-601 (error) Design '%s' contains constructs not supported for FPGA synthesis.

DESCRIPTION

You tried to target your behavioral design for synthesis to an FPGA. However, your design contains constructs the tool does not support for synthesis to FPGA. These constructs include:

- Arrays mapped to register files
- Operations that are implemented in non-Synopsys synthetic libraries
- RTL processes

WHAT NEXT

Rewrite your behavioral description to remove these constructs.

Instead of mapping arrays to register files, map them to memories. Memories are more efficiently implemented on FPGAs.

In place of non-Synopsys components, use the components available to you in the Synopsys DesignWare libraries.

Move RTL processes outside your behavioral module. For example, implement an RTL module that contains your RTL processes and that also instantiates your behavioral module. This is equivalent to your original description.

SEE ALSO

set_fpga (2).

HLS-602 (error) Unable to link design '%s'.

DESCRIPTION

The command you tried to execute is unable to link your design, which indicates that the command was unable to find implementations for all the components and subdesigns your design uses.

WHAT NEXT

Be sure that implementations of all the components and subdesigns are present.

Use the **list_designs** command to view the designs currently in dc_shell, which will tell you if you inadvertently removed a subdesign.

Be sure that the value of the **link_library** variable and the **synthetic_library** variable contains all of the libraries that contain components your design uses.

SEE ALSO

list (2), **list_designs** (2), **list_libraries** (2); **link_library** (3), **synthetic_library** (3).

HLS-603 (information) Targeted design '%s' to FPGA target='%s' device='%s' speed='%s'.

DESCRIPTION

You successfully targeted your design to the FPGA you specified. Your design is now configured for behavioral synthesis targeting this FPGA.

WHAT NEXT

This is an information message. You do not need to take any action.

SEE ALSO

set_fpga (2).

HLS-604 (error) Unable to find a valid version of FPGA Compiler II.

DESCRIPTION

You tried to target to an FPGA your behavioral design for synthesis. However, a valid version of FPGA Compiler II was not found on your operating system's search path, such as the PATH environment variable on UNIX systems.

WHAT NEXT

Behavioral synthesis targeting FPGAs requires version 3.6 or later of the Synopsys FPGA Compiler II. Please be sure that your search path includes the path to the **fc2_shell** executable contained in your FPGA Compiler II installation.

The version of FPGA Compiler II is important. Version 3.5 or earlier does not enable behavioral synthesis to FPGAs.

SEE ALSO

set_fpga (2).

HLS-605 (error) Incomplete specification. FPGA %s has not been specified.

DESCRIPTION

You used dc_shell variables to target your behavioral design for synthesis to FPGAs. But your specification is incomplete because you did not set one or more of three necessary variables.

WHAT NEXT

Make sure that you specify a legal FPGA specification with the following three dc_shell variables.

- bc_fpga_target
- bc_fpga_device
- bc_fpga_speed

SEE ALSO

bc_fpga_device (3), **bc_fpga_speed** (3), **bc_fpga_target** (3).

HLS-606 (error) Specified FPGA %s '%s' is not supported.

DESCRIPTION

You tried to target your behavioral design for synthesis to an FPGA. But the FPGA you specified is not supported.

WHAT NEXT

Behavioral synthesis targets only FPGAs that are supported by version 3.6 or later of the Synopsys FPGA Compiler II.

See the FPGA Compiler II documentation to be sure that your FPGA is supported.

SEE ALSO

set_fpga (2).

HLS-607 (error) Unable to launch FPGA Compiler II located at %s.

DESCRIPTION

Behavioral synthesis was unable to launch your installation of the Synopsys FPGA Compiler II.

WHAT NEXT

To target FPGAs, behavioral synthesis must be able to launch the **fc2_shell** executable in your FPGA Compiler II installation.

The most likely cause for this error is an incorrect operating system configuration or incorrect installation of FPGA Compiler II.

Verify that your operating system is compliant with the requirements in the manual *Installing and Licensing Synopsys Software*. Noncompliant operating system versions and patches can prevent the **fc2_shell** executable being launched.

Ensure that your FPGA Compiler II installation is set up correctly. The **fc2_shell** executable might be absent or might not launch if the setup is incorrect. See the FPGA Compiler II documentation for further information.

SEE ALSO

set_fpga (2).

HLS-608 (error) Unable to communicate with FPGA Compiler II launched from %s.

DESCRIPTION

Behavioral synthesis successfully launched FPGA Compiler II but is unable to communicate with it.

WHAT NEXT

To target FPGAs, behavioral synthesis must be able to launch and communicate with the **fc2_shell** executable in your FPGA Compiler II installation. This error indicates that communication was lost.

The most likely cause for this error is an incorrect operating system configuration or incorrect installation of FPGA Compiler II.

Verify that your operating system is compliant with the requirements in the manual *Installing and Licensing Synopsys Software*. Noncompliant operating system versions and patches can prevent the **fc2_shell** executable being launched.

Be sure that your FPGA Compiler II installation is set up correctly. The **fc2_shell** executable might be absent or might not launch if the set up is incorrect. See the FPGA Compiler II documentation for further information.

Another possible cause is a transient operating system or network anomaly. Test this possibility by rerunning your behavioral synthesis task.

SEE ALSO

set_fpga (2).

HLS-609 (error) Unable to create temporary workspace for FPGA synthesis %s.

DESCRIPTION

Behavioral synthesis is unable to create a temporary directory to house intermediate files during FPGA synthesis.

WHAT NEXT

Behavioral synthesis must be able to create a temporary workspace in which to place intermediate files during synthesis targeting FPGAs.

Be sure that the permissions settings in the directory in which you are running **dc_shell** let you create subdirectories and files.

SEE ALSO

set_fpga (2).

HLS-610 (error) The target technology for design '%s' cannot be changed. %s

DESCRIPTION

You tried, with the **set_fpga** command, to target a behavioral design for synthesis to an FPGA. Or you tried to remove such a specification with the **unset_fpga command**.

However, the state the design is in prevents the tool performing such a retargeting of technology. Some technology-specific tasks, for example timing or synthesis, have already been performed on the design.

WHAT NEXT

Remove the current behavioral design from **dc_shell** memory with the **remove_design** command.

Restart behavioral synthesis from the analysis and elaboration stage, or read in a .db file containing an elaborated design.

The design must not have been processed with any of the following commands:

- **schedule**

- **bc_time_design**
- **bc_margin**
- **compile_preserved_functions**

SEE ALSO

read (2), **remove_design** (2), **set_fpga** (2), **unset_fpga** (2), **write** (2).

HLS-611 (error) Unable to find an implementation for operator '%s' in a Synopsys DesignWare library. The operator is used by operations '%s' in design '%s'.

DESCRIPTION

You receive this error message because your design for behavioral synthesis targeting FPGAs contains operations that use components that Synopsys DesignWare does not own or support.

The only exceptions are memory read and write operators defined in a synthetic library that contains the implementation of memory wrappers used for memories inferred in your behavioral description, which Synopsys DesignWare does support.

WHAT NEXT

Remove from the **synthetic_library** variable synthetic libraries that Synopsys DesignWare does not support, noting the exceptions described in the previous paragraph. Replace the removed components with components found in the Synopsys DesignWare libraries.

SEE ALSO

set_fpga (2); **synthetic_library** (3).

HLS-612 (error) Design '%s' maps the array variables '%s' to register files, which are not supported for FPGA synthesis.

DESCRIPTION

You receive this error message because you have in your design arrays that have been

mapped to register files using the *map_to_registerfiles* compiler directive or the **dc_shell** variable **bc_use_registerfiles**. Register files are not supported in behavioral synthesis targeting FPGAs.

WHAT NEXT

Remove the mapping of arrays to register files.

Alternately, map array variables to memories instead, by using the *map_to_module* compiler directive.

For more information about mapping arrays to memories, see the *Behavioral Compiler User Guide* or the *SystemC Compiler User Guide*.

SEE ALSO

set_fpga (2).

HLS-613 (error) Design '%s' contains a non-behavioral process %s.

DESCRIPTION

Your behavioral module contains a register-transfer level (RTL) process. Behavioral modules with both behavioral and RTL processes are not supported for behavioral synthesis targeting FPGAs.

WHAT NEXT

Move your RTL processes out of your behavioral module. You can create an RTL module that contains your RTL processes and also instantiates your behavioral module. By connecting your RTL processes to your behavioral module you create a hierarchical description that is equivalent to your current description.

SEE ALSO

set_fpga (2).

HLS-614 (error) Unable to target design '%s' to specified FPGA.

DESCRIPTION

You receive this error message because you tried unsuccessfully to target to an FPGA your design for behavioral synthesis.

WHAT NEXT

This error message is always preceded by an error message detailing the specific reason your attempt was unsuccessful. Refer to the man page for that error message for more details.

SEE ALSO

set_fpga (2).

HLS-615 (error) An error occurred during processing of design %s, using the synthetic libraries specified by the user.

DESCRIPTION

You receive this error message because the compiler did not find the synthetic libraries you specified in your design. It looks for the standard set of Synopsys-specific synthetic libraries.

WHAT NEXT

Check to see if the the **dc_shell** variable **synthetic_library** lists all of the required synthetic libraries to support the operators in your design.

Preceding this error message, you might also see another error message that gives the specific reason for the failure. See the man page for that error message for more details.

SEE ALSO

synthetic_library (3).

HLS-616 (error) FPGA %s has not been specified, resulting in incomplete specification.

DESCRIPTION

You receive this error message because, in using the **set_fpga** command to target your behavioral design for synthesis to FPGAs, your specification is incomplete. One or more settings for the FPGA target, device, or speed is missing. These settings are options to the **set_fpga** command.

WHAT NEXT

Set the necessary options (-target, -device, and -speed) to the **set_fpga** command. Then run the command again.

SEE ALSO

set_fpga (2).

HLS-617 (error) Option %s is unsupported for behavioral synthesis to FPGA.

DESCRIPTION

You receive this error message because the command option you tried to execute has no effect on a design that has been configured for behavioral synthesis targeting an FPGA.

WHAT NEXT

Do not use the option when invoking the command on a design configured for behavioral synthesis to an FPGA.

SEE ALSO

set_fpga (2).

HLS-618 (error) File '%s' does not contain an implementation of preserved function '%s' that targets an FPGA.

DESCRIPTION

You receive this error message because you tried to use the **read_preserved_function_netlist** command to read in an implementation for a preserved function configured for behavioral synthesis targeting an FPGA.

However, the .db file you are reading from was not generated by running the **compile_preserved_function** command (with the **-write** option) on a design configured for behavioral synthesis targeting an FPGA. Therefore, the implementations the file contains are not valid for behavioral synthesis to an FPGA.

WHAT NEXT

• If you have a valid .db file, that is, one that was generated with **compile_preserved_function -write** on a design configured for behavioral synthesis to FPGA with the **set_fpga** command, specify that .db file as the file to read from.

• If you want to use the current .db file, do not configure the file for synthesis to FPGA. Use the **unset_fpga** command to remove your prior configuration.

SEE ALSO

compile_preserved_functions (2), **read_preserved_function_netlist** (2), **set_fpga** (2), **unset_fpga** (2).

HLS-619 (error) Preserved function '%s' and the corresponding design in file '%s' target different FPGAs.

DESCRIPTION

You receive this error message because you tried to read in an implementation for a preserved function using the **read_preserved_function_netlist** command. The preserved function is configured for behavioral synthesis targeting an FPGA.

The **read_preserved_function_netlist** command has found in the file you are reading from a design with the same name as the preserved function. However, this design is not mapped to the same FPGA as the design the preserved function is targeting.

WHAT NEXT

• If you have a .db file containing a design for the preserved function that targets the same FPGA, specify that file as the one to read from.

• Use the **set_fpga** command to retarget the preserved function to the FPGA that the design in the .db file targets.

SEE ALSO

read_preserved_function_netlist (2), **set_fpga** (2).

HLS-620 (error) The operation %s requires multiple clock cycles to execute. Multicycled operations are not supported in FPGA

synthesis.

DESCRIPTION

You receive this error message because the operation you specify takes multiple clock steps to execute, and FPGA synthesis does not support multicycled operations. An operation takes multiple clock steps if the delay its execution requires is larger than the clock period available.

Behavior synthesis reserves a part of the clock period, called the "margin," to provide for FSM delay, register setup, and clock-to-Q delay. The clock period available to execute the datapath operations is the specified clock period, minus the margin.

To avoid multicycled operations, the available clock period for the design must be larger than the delay of the slowest operation in the design, plus the margin.

Another way to avoid multicycled operations, instead of increasing the clock period, is to try to use faster components for synthesis, such as the **bc_time_design** command with the **-fastest** option, or by manually selecting faster components from the Synopsys DesignWare libraries.

WHAT NEXT

Here is a summary of ways to avoid multicycled operations:

- Increase the clock period, using the **create_clock** command.
- Reduce the margin, using the **bc_margin** command.
- Use bc_time_design -fastest to select the fastest components for synthesis.
- Use a pipelined component to implement the operation.
- Use the preserved function methodology to generate a faster component to implement the operation.

For more details, see the *Cocentric SystemC Compiler/Behavior Compiler User Guide*.

SEE ALSO

bc_margin (2), **bc_time_design** (2), **create_clock** (2), **compile_preserved_functions** (2).

HLS-621 (information) Removed FPGA specification from design '%s'.

DESCRIPTION

The named design was previously configured for behavioral synthesis targeting an FPGA. You ran a command, such as **unset_fpga** that removed the configuration.

WHAT NEXT

This message is informational only and requires no action on your part.

SEE ALSO

set_fpga (2), **unset_fpga** (2).

HLS-622 (error) Design library '%s' does not exist.

DESCRIPTION

You receive this error message because you tried to use the **-design_library** option of the **compile_preserved_function** command to write to disk the preserved functions in your design. But the design library you specified in the option does not exist.

WHAT NEXT

Use the **define_design_library** command to map a physical directory on your disk to a logical design library of the name you specified. Then invoke **compile_preserved_functions** again.

Or you can correct the design library name you specified and then invoke **compile_preserved_functions** again.

SEE ALSO

compile_preserved_functions (2), **define_design_lib** (2).

HLS-623 (error) Design library '%s' is mapped to disk location

’%s’ that is not a directory or is not writable.

DESCRIPTION

You receive this error message because you tried to use the **-write** option of the **compile_preserved_function** command to write to disk the preserved functions in your design. The design library into which you want the preserved functions to be written is not writable for one of the following reasons:

• The location to which the design library is mapped is not a directory.

• The directory to which the design library is mapped does not have permissions that allow the creation of files within it. For example, on a UNIX platform the directory must have write and execute permissions.

WHAT NEXT

Use the **define_design_library** command to map a writable physical directory on your disk to a logical design library of the name you specified. Then invoke **compile_preserved_functions**.

Or you can change the design library you specify to one that is mapped to a writable physical directory, and then invoke **compile_preserved_functions** again.

SEE ALSO

compile_preserved_functions (2), **define_design_lib** (2).

HLS-624 (error) Unable to create a file named ’%s’ in design library ’%s’ that is mapped to physical directory ’%s’.

DESCRIPTION

You receive this error message because you tried to use the **-write** option of the **compile_preserved_function** command to write to disk the preserved functions in your design. Behavioral synthesis tried to create a file on your disk into which to place the netlists of the compiled preserved functions. However, it is unable to do this for one of the following reasons:

• A directory with the same name as the specified (or default) filename already exists in the physical directory to which the design library is mapped.

• A file with the same name already exists, but the file permissions do not allow

the file to be overwritten. For example, on a UNIX platform the file must have write permissions.

WHAT NEXT

You can fix the problem by doing one of the following:

• Use the **-filename** option of the **compile_preserved_function** command to specify the name of the file you want to write into. Ensure that you are able to create and write into a file of this name.

• Change the permissions of the existing file to allow it to be overwritten.

• Change the design library into which you are writing and ensure that no file name in the physical location of that design library conflicts with the file name in the error message.

SEE ALSO

compile_preserved_functions (2), **report_design_lib** (2).

HLS-625 (error) Unable to write preserved function '%s'.

DESCRIPTION

You receive this error message because you tried, but failed, to use the **-write** option of the **compile_preserved_function** command to write to disk the preserved functions in your design.

WHAT NEXT

This error message is always preceded by one that gives details of the specific failure that occurred. See the man page for that error for more information.

SEE ALSO

compile_preserved_functions (2).

HLS-626 (warning) The dc_shell variable '%s' has no effect on

a design configured for behavioral synthesis to FPGAs.

DESCRIPTION

You receive this warning because you assigned to a **dc_shell** variable a value that has no effect on behavioral synthesis of a design configured with the **set_fpga** command to target FPGAs.

WHAT NEXT

To eliminate the warning message, remove the variable or restore it to its default value. See the man page for the variable, to determine what its default value should be.

SEE ALSO

set_fpga (2), **unset_fpga** (2).

HLS-627 (warning) Design '%s' does not target an FPGA.

DESCRIPTION

You receive this warning because you tried to use the **unset_fpga** command to remove a previous configuration of the named design to target FPGAs in behavioral synthesis.

However, the named design was never configured with the **set_fpga** command to target FPGAs.

WHAT NEXT

This warning indicates that the **unset_fpga** command has no effect on this design. No further action on your part is necessary.

However, this might indicate an earlier error in your synthesis script. For example, an earlier call to the **set_fpga** command may have failed.

SEE ALSO

set_fpga (2), **unset_fpga** (2).

HLS-628 (error) Design '%s' is a behavioral module synthesized for an FPGA implementation. You cannot use the '%s' command

to perform logic synthesis. Use FPGA Compiler II instead.

DESCRIPTION

You receive this error message because you tried to invoke a logic synthesis command, such as **compile** or **reoptimize_design**, on your current design. The design is a behavioral module that was configured with the **set_fpga** command to target an FPGA implementation.

Therefore, you must use FPGA Compiler II, not Design Compiler, to perform logic synthesis on your design.

WHAT NEXT

Write out a synthesizable RTL model of your design. Also create an FPGA Compiler II synthesis script, using the **write_rtl** command,

For example,

```
dc_shell> write_rtl -format verilog \
                    -output my_design.v \
                    -rtl_script my_design.fc2
```

Then invoke FPGA Compiler II from your UNIX command line to perform logic synthesis.

```
unix% fc2_shell -f my_design.fc2
```

SEE ALSO

set_fpga (2).

HLS-629 (error) FPGA %s cannot be set to '%s' for behavioral synthesis.

DESCRIPTION

You receive this error message because you tried to set an FPGA target, device, or speed to a value that is invalid for behavioral synthesis.

The FPGA specification must identify a fully defined FPGA. For example,

```
dc_shell> set_fpga -target APEX20K -device EP20K400FC672 -speed -3
```

You cannot use an unrestricted FPGA specification, such as the following:

```
dc_shell> set_fpga -target APEX20K -device AUTO -speed FASTEST
```

WHAT NEXT

Change your FPGA specification to identify a fully defined FPGA.

You can use the **-list** option of the **set_fpga** command to view the available FPGAs for behavioral synthesis.

For example,

```
dc_shell> set_fpga -target APEX20K -device "*" -speed "*"
```

SEE ALSO

set_fpga (2).

HLS-630 (error) Preserved function '%s' targets an FPGA and the corresponding design in file '%s' does not.

DESCRIPTION

You receive this error message because you tried to read in an implementation for a preserved function using the **read_preserved_function_netlist** command. The preserved function was not configured for behavioral synthesis targeting an FPGA with the **set_fpga** command.

The **read_preserved_function_netlist** command found a design with the same name as the preserved function in the file from which you are reading. However, this design was mapped to an FPGA using the **set_fpga** command.

You cannot use the design from the file to implement the preserved function.

WHAT NEXT

Do one of the following actions:

• If you have a .db file containing a design for the preserved function that targets the same technology, specify that file as the one to read from.

• Use the **compile_preserved_functions -write** command to compile a new implementation for the preserved function. The **-write** option writes the new implementation to disk so that in future sessions you can read in the new implementation using the **read_preserved_function_netlist** command.

• Use the **set_fpga** command to retarget the design containing the preserved function to the FPGA that the design in the .db file targets.

SEE ALSO

set_fpga (2), **read_preserved_function_netlist** (2), **compile_preserved_functions** (2).

HLS-631 (warning) The synthetic component '%s' cannot be timed; operation '%s' will have zero delay.

DESCRIPTION

You receive this warning because the synthetic component '%s' on your design configured for behavioral synthesis targeting an FPGA cannot be timed. This happens for DesignWare that is not from Synopsys and for components the FPGA Compiler II does not recognize.

Scheduling is still possible, but all operations using this component will have zero delay, and other operations will be able to chain into or from it.

WHAT NEXT

Use Synopsys DesignWare components instead. Use the command **set_implementation** to specify an implementation.

If you continue with your currently configured design, you need to take into account timing requirements for this component and set proper scheduling timing constraints on the operations that make use of the component. Use the **dont_chain_operations** command to control chaining into and out of the operation. Use the **set_cycles** command to specify timing for the operation.

SEE ALSO

dont_chain_operations (2), **set_cycles** (2), **set_implementation** (2).

ICCSH-001 (information) License queuing is enabled.

DESCRIPTION

You receive this message because you have enabled licensing queuing.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

ICCSH-002 (information) Successfully checked out feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE in icc_shell.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

ICCSH-003 (information) Started queuing for feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE in icc_shell.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

ICCSH-004 (information) Still waiting for feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE in icc_shell.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

ICCSH-005 (information) Timeout while waiting for feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE in icc_shell.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

IFS-001 (error) Unit conflict found: constraints %s unit is '%s'; Main Library %s unit is '%s'.

DESCRIPTION

You receive this message because unit in SDC or design constraints is different from the unit in current Main Library. The Main Library is the first logical db library specified in link_library set.

WHAT_NEXT

Please check the logical library setting, search_path and link_library should already specified before reading the design or SDC file. Refer to report_lib command to report the Main Library units.

An alternative is to edit the SDC file to match the units of your current library settings. After changing the SDC, please remove the set_units command in the SDC file or change the set_units command to has all the same units as Main Library units.

If the DDC/CEL is the design input, please make sure the library setting is the same with the setting when the DDC/CEL file is saved.

If the DDC/CEL is copied from other Design Library to this Design Library, please make sure the Design Library units are the same between the two libraries. Refer to report_units command to report the Design Library units.

SEE ALSO

report_units report_lib

IFS-002 (error) One or more design constraints unit is conflicting with Main Library unit, '%s' failed.

DESCRIPTION

You receive this error because tool detects design constraints unit confict with Main Library unit. This means the unit of constraints saved in DDC/CEL or specified in SDC file are conflicting with unit in current Main Library.

Refer to detail unit conflict issued in previous IFS-001 message.

WHAT_NEXT

Please check the logical library setting, search_path and link_library should already specified before reading the design or SDC file. Refer to report_lib command to report the Main Library units.

An alternative is to edit the SDC file to match the units of your current library settings. After changing the SDC, please remove the set_units command in the SDC file or change the set_units command to has all the same units as Main Library units.

If the DDC/CEL is the design input, please make sure the library setting is the same with the setting when the DDC/CEL file is saved.

If the DDC/CEL is copied from other Design Library to this Design Library, please make sure the Design Library units are the same between the two libraries. Refer to report_units command to report the Design Library units.

SEE ALSO

report_units report_lib

IFS-003 (error) Unrecognized %s unit: %s.

DESCRIPTION

You receive this message because unrecoginized unit set in set_units command.

WHAT_NEXT

check set_units command for correct syntax and supported units.

SEE ALSO

report_units set_units(2).

IFS-004 (error) Unit conflict found: current design constraints %s unit is %s; previous design constraints %s unit is %s.

DESCRIPTION

You receive this message because power/current/voltage units in SDC or DDC/CEL are different from the units of power/current/voltage constraints set and saved previously.

WHAT_NEXT

An alternative is to edit the SDC file to match the units of your current library settings. After changing the SDC, please remove the set_units command in the SDC file or change the set_units command to has all the same units previously set.

SEE ALSO

report_units

IFS-005 (warning) Unit conflict found: Design Library %s unit is %s; Main Library %s unit is %s.

DESCRIPTION

You receive this message because the unit saved in Design Library is different from the unit in current Main Library. The Design Library is MW design library. The Main Library is the first logical db library specified in link_library set.

WHAT_NEXT

Please check the logical library setting, search_path and link_library should already be specified before opening the Design Library and the CEL. The link_library set should be consistent with link_library set during the creation time of Design Library and saving of MW CEL. If link_library set is modified, make sure the Main Library units are consistant between old setting and new setting.

Refer to report_units command to report the Design Library units . Refer to report_lib command to report the Main Library units. The units reported by these 2 commands must be consistent

If the CEL is copied from other Design Library to this Design Library, please make sure the Design Library units are the same between the two libraries. Refer to report_units command to report the Design Library units.

SEE ALSO

report_units report_lib

IFS-006 (error) One or more Design Library unit is conflicting

with Main Library unit.

DESCRIPTION

You receive this error because tool detects Design Library unit confict with Main Library unit. This means the unit of constraints saved in Design Library are conflicting with unit in current Main Library.

Refer to detail unit conflict issued in previous IFS-005 message.

WHAT_NEXT

Please check the logical library setting, search_path and link_library should already be specified before opening the Design Library and the CEL. The link_library set should be consistent with link_library set during the creation time of Design Library and saving of MW CEL. If link_library set is modified, make sure the Main Library units are consistant between old setting and new setting.

Refer to report_units command to report the Design Library units . Refer to report_lib command to report the Main Library units. The units reported by these 2 commands must be consistent

If the CEL is copied from other Design Library to this Design Library, please make sure the Design Library units are the same between the two libraries. Refer to report_units command to report the Design Library units.

SEE ALSO

report_units

IFS-007 (warning) Conflict unit found: MW tech file %s unit is %s; Main Library %s unit is %s.

DESCRIPTION

You receive this message because the unit in MW technology file is different from the unit in current Main Library. The Main Library is the first logical db library specified in link_library set.

WHAT_NEXT

Please check the tech file units and the logical library setting, search_path and link_library should be set before opening the library and the CEL. Units in tech file and units in main library should be the same.

Refer to report_lib to report main library units.

SEE ALSO

report_units report_lib.

IFS-008 (warning) No valid link library found, please specify link_library.

DESCRIPTION

You receive this error because logical link library is not set up.

WHAT_NEXT

Please set search_path and link_library. Check if the search_path and link_library settings are correct.

SEE ALSO

IFS-009 (warning) %s has been removed on design %s.

DESCRIPTION

You receive this message because the unit has been removed on the design.

WHAT_NEXT

SEE ALSO

ILM-01 (error) Could not read model back from '%s' for design '%s'.

DESCRIPTION

You receive this message if **create_ilm** cannot read back an extracted model file that was created by writing the output of **create_ilm** to a user-specified file.

Once ILM extraction is completed, the extracted model is written to the specified output db file, which is subsequently read back in as the current design. If the file cannot be read, this error message is generated.

Some possible reasons why the file cannot be read back could include the following:

• The model was not written to the file specified by the **-output** option of **create_ilm**, either because you did not have write permission for the file or the directory, or because there was insufficient disk space.

• You do not have read permission for the directory that contains the extracted model file.

WHAT NEXT

Ensure that you direct the output db file to a directory with sufficient disk space, in which you have both read and write privileges. Then reexecute the **create_ilm** command and generate the output file.

SEE ALSO

create_ilm (2).

ILM-02 (warning) Could not adjust location for cell: %s.

DESCRIPTION

During ILM extraction, the **create_ilm** command attempts to adjust the cell and port locations so that the (x,y) coordinates are relative to the origin of the block. You receive this message if **create_ilm** could not adjust the location of the specified cell. The most probable reason for the failure is that cells or ports have not been placed prior to ILM extraction.

WHAT_NEXT

Execute **report_cell -physical** and **report_port -physical** and ensure that all cells (except spare cells) and ports have locations. If they do not have locations, you must place them before executing the **create_ilm** command.

SEE_ALSO

create_ilm (2), **report_cell** (2), **report_port** (2).

ILM-03 (error) Design '%s' contains cluster information. You cannot use the tool to extract ILM when clusters are present.

DESCRIPTION

This error occurs because you used the **create_ilm** command from within the shell to extract an interface logic model (ILM) on a design that contains clusters. The **create_ilm** command in the shell does not accept designs that contain clusters.

WHAT NEXT

Do not attempt to execute the **create_ilm** command from within the shell.

SEE ALSO

create_ilm(2)

ILM-04 (error) Interface logic has not been identified for design: %s

DESCRIPTION

You receive this message if you attempt to execute the extract step of **create_ilm** command on a design for which the interface logic has not been identified or tool has failed to identify interface logic. This interface logic is preserved in the Interface Logic Model (ILM). You cannot do extract ILM step unless you have previously identified the interface logic using the **create_ilm** command.

WHAT_NEXT

The most likely cause of this error is incorrect usage or other error conditions

occured during **create_ilm** command. If you are using **-identify_only** and/or **-extract_only** options of **create_ilm**, make sure **create_ilm -identify_onlyP is executed successfully without any errors before executing create_ilm -extract_only**.

SEE_ALSO

create_ilm (2).

ILM-05 (error) The core area has not been defined for design: %s.

DESCRIPTION

You receive this message if you execute **create_ilm**, but the core area for the specified block has not been defined. If you use the default options, you must have previously defined the core area.

WHAT NEXT

Do the following:

1. Specify the core area in the floorplan.

2. Use the **set_placement_area** command to define the core area.

Then, reexecute **create_ilm** .

SEE ALSO

create_ilm(2), set_placement_area (2).

ILM-06 (error) The parent block %s of ILM block %s is not an ILM.

DESCRIPTION

You receive this message if you attempt to execute the optimization command on a design that contains an interface logic model (ILM) block, but the parent block of the ILM block is not an ILM. You cannot perform top-level optimization on a design that contains an ILM block within a non-ILM hierarchical block.

WHAT NEXT

If your design has a hierarchical block that contains an ILM sub-block, use the **create_ilm** command to create an ILM for the hierarchical block also. Nested ILM blocks are permitted as long as the outermost ILM is directly at the top level.

SEE ALSO

create_ilm (2),

ILM-07 (Information) Port '%s' belongs to the ignore list because it fans
out to %d%% of the registers on the design.

DESCRIPTION

You receive this message if you execute the **create_ilm** command with the **-auto_ignore** option, and the fanout of the specified input port has a larger percentage of the total number of registers than the percentage specified by the current value of the **ilm_ignore_percentage** variable (default 25). (For example, for the default value of 25, a port's fanout is ignored if the port fans out to 25% or more of the total number of registers in the design.) This message informs you that the specified port's fanout will be ignored.

WHAT NEXT

This is an informational message only; if it is acceptable to you that the specified port is on the ignore list, no action is required on your part. Otherwise, you can query the current value of the **ilm_ignore_percentage** variable by executing the following:

psyn_shell **printvar ilm_ignore_percentage**

If you want to set the variable to a higher or lower threshold percentage, execute the following:

psyn_shell **set ilm_ignore_percentage** *new_value*

SEE ALSO

create_ilm (2); **ilm_ignore_percentage** (3).

ILM-08 (error) Cannot specify '%s' with '%s'.

DESCRIPTION

The listed command options are exclusive. Only one of them can be specified.

WHAT NEXT

Look at the manpage for this command for more information on command options.

ILM-09 (error) The orientation of the ILM block %s is not legal.

DESCRIPTION

You receive this message if the orientation of the ILM block in the top level floorplan is not legal. Only 0, 180,0-mirror, 180-mirror orientations are supported for ILM blocks.

WHAT NEXT

Change the orientation of the ILM block to one of the legal orientations and run optimization command again.

SEE ALSO

ILM-10 (error) Unable to propagate attributes for ILM cell %s

DESCRIPTION

You receive this message during propagate_ilm when the attributes are not loaded from the cells of the ILM design to the instance of the top level design.

SEE ALSO

propagate_ilm (2).

ILM-11 (error) Unable to find the location of ILM block %s

DESCRIPTION

You receive this message during propagate_ilm if the location of the ILM block is missing from the top level floorplan.

WHAT_NEXT

Check if the pdef contains the location information for ILM block. If no location is specified for the ILM blocks, update floorplan with location specified for ILM block.

SEE ALSO

propagate_ilm (2). **physopt** (2).

ILM-12 (Error) Cell '%s' not an ILM block.

DESCRIPTION

The cell provided as argument on the command line is not an ILM block. This command can be used to propagate information for ILM blocks only. If you are using this command to propagate placement information for a non-ILM block, please use the **propagate_placement** command instead.

WHAT NEXT

Please remove any non-ILM cells from cell list or use the **propagate_placement** command.

SEE ALSO

propagate_ilm(2), propagate_placement(2).

ILM-13 (Error) Cell '%s' not a hierarchical cell.

DESCRIPTION

The cell provided as argument on the command line is not a hierarchical cell. This command works only on hierarchical cells.

WHAT NEXT

Please specify only hierarchical cells in the cell list.

SEE ALSO

propagate_placement(2), propagate_ilm(2).

ILM-14 (error) Location not found for ILM leaf cell %s reference %s.

DESCRIPTION

You receive this error message because a leaf cell inside an ILM block does not have its location specified. All leaf cells inside an ILM block must have locations. The locations of the ILM leaf cells will be automatically propagated when the ILMs are linked at the top level design. You need not use **propogate_ilm** command.

WHAT NEXT

To check if all leaf cells inside ILM block have locations, you can set current design as the reference design of the ILM block instance, and then run the **report_cell -physical** command.

To ensure that all ILM leaf cells have locations, create ILM for the block after the block has been placed.

If you found that this cell instance does not exist in original block or ILM, this could have been incorrectly added by one of the previous optimization commands. Trace back to the actual command causing this problem. If any of the previous optimization commands have abnormally terminated, restart the session.

SEE ALSO

create_ilm (2), **report_cell** (2).

ILM-15 (error) Invalid options. Must specify '%s' option with '%s'.

DESCRIPTION

The listed command options are dependant. -keep_macros option requires -physical option.

WHAT NEXT

Look at the manpage for this command for more information on command options.

ILM-16 (error) Cell/Port '%s' does not have a location.

DESCRIPTION

You receive this message if **create_ilm** cannot find the locations of all the cells and ports of the design.

WHAT NEXT

Ensure that the design is placed and all the cells and ports of the current design have valid locations and then rerun **create_ilm**.

SEE ALSO

create_ilm (2).

ILM-17 (error) Design '%s' has sequential elements but there are no clocks defined on it.

DESCRIPTION

You receive this message if **create_ilm** cannot find any clocks defined on the design, but the design has sequential elements.

WHAT NEXT

Ensure that there are clocks defined on the design and then rerun **create_ilm**. Use the **create_clock** command to create the clocks.

SEE ALSO

create_ilm (2), **create_clock** (2).

ILM-18 (information) Design '%s' has no sequential elements.

DESCRIPTION

You receive this message if **create_ilm** cannot find any sequential elements in the design in which case the ILM generated will be of the same size as the original design.

WHAT NEXT

This is information message only. No action needed.

SEE ALSO

create_ilm (2).

ILM-19 (error) Found non-uniquified hierarchy '%s'. Run uniquify command before running this command.

DESCRIPTION

You receive this error message if the **create_ilm** command finds one or more non-uniquified designs. Uniquify the designs before running this command.

WHAT NEXT

Run the **uniquify** command before running this command. In addition, you can remove don't touch attributes using the **set_dont_touch** command before running **uniquify** to reduce the resultant ILM size.

If you want to remove all don't touch attributes and run **create_ilm**, use the following set of commands:

```
psyn_shell-t> set_dont_touch [get_designs *] FALSE
psyn_shell-t> uniquify
psyn_shell-t> create_ilm
```

SEE ALSO

create_ilm(2)
set_dont_touch(2)
uniquify(2)

ILM-20 (warning) Preserving the %s hierarchy '%s' completely. This may increase ILM size.

DESCRIPTION

You receive this message if the **create_ilm** command finds one or more don't touch designs or ununiquified designs. If **create_ilm** finds a don't touch design or ununiquified design it retains the design completely in ILM. This can potentially increase the size of the ILM.

WHAT NEXT

Remove the don't touch attributes using the **set_dont_touch** command and run the **uniquify** command before running **create_ilm**. For example, if you want to remove the don't touch attribute for all designs, use the commands:

```
psyn_shell-t> set_dont_touch [get_designs *] FALSE
psyn_shell-t> uniquify
psyn_shell-t> create_ilm
```

SEE ALSO

create_ilm(2)
set_dont_touch(2)
uniquify(2)

ILM-21 (error) The current design '%s' has ILM blocks in it. compile_physical does not support ILMs.

DESCRIPTION

The compile_physical command does not support designs with instances of ILMs in it.

WHAT NEXT

Instead of ILMs instantiate the entire block.

SEE ALSO

compile_physical(2).

ILM-22 (warning) Side_load type has been changed from '%s' to

’all’ since -keep_parasitics option is specified.

DESCRIPTION

You will see this message if you specify **none** or **boundary** for **-include_side_load** when **-keep_parasitics** option is specified. For accurate Interface Logic Model creation it is recommended to use **-include_side_load all** when **-keep_parasitics** option is used. Thus the tool automatically adjusts the **-include_side_load** setting.

WHAT NEXT

This automatic setting can not be over ruled. No action is required.

SEE_ALSO

create_ilm (2).

ILM-23 (error) ILM ’%s’ does not have required parasitics (%s) file.

DESCRIPTION

You will see this message if the reported ILM view does not have required parasitics file. The RC parasitics file is attached to the ILM during ILM creation if the design is partially or fully routed. This file is needed to combine block-level and top-level post-route parasitics. This file is required during top-level extraction when the top-level design is partially or fully routed.

By default, The CC parasitics file is attached to the ILM during ILM creation a. if -include_xtalk option is used for create_ilm b. SI option(s) are turned ON.

If design is neither track assigned nor detail routed, the CC parasitics file will not be attached with ILM.

These files get generated when extraction runs successfully during ILM creation. ILM-29 information message is printed if these files are successfully generated and attached.

For example,
• If RC parasitic file is missing for A.ILM, you will get "ILM ’A’ does not have required parasitics (RC) file" error message.
• If CC parasitic file is missing for A.ILM, you will get "ILM ’A’ does not have required parasitics (CC) file" error message.

WHAT NEXT

Check the options and output of **create_ilm** command that is used to create the reported ILM. Check if ILM-29 message is printed. Watch out for ILM-90 and ILM-92 message. Re-run with the correct settings.

SEE_ALSO

create_ilm (2), **ILM-29** (n), **ILM-90** (n), **ILM-92** (n).

ILM-24 (error) Missing parasitics data for routed design '%s'.

DESCRIPTION

You will see this message if the top-design is routed but neither **extract_rc command is run nor parasitics present in the corresponding PARA view.**

WHAT NEXT

Check/set TLUPlus file settings, run **extract_rc** and run the command again.

SEE_ALSO

set_tlu_plus_files (2), **extract_rc** (2), **propagate_ilm** (2).

ILM-25 (error) Missing parasitics data. '%s' option has failed.

DESCRIPTION

You will see this message during **create_ilm** if **extract_rc** command is not run on the design and PARA view does not contain parasitics file. Parasitics data is required for running **-keep_parasitics** option of **create_ilm**.

WHAT NEXT

Check/set TLUPlus file settings, run **extract_rc** and run **create_ilm** again.

SEE_ALSO

set_tlu_plus_files (2), **extract_rc** (2), **create_ilm** (2).

ILM-26 (information) Using parasitics (%s) file from '%s.ILM'

DESCRIPTION

You will see this message during top-level flow when ILM parasitics are used to stitch with the top-level parasitics.

WHAT NEXT

This is informative message. No action required.

SEE_ALSO

set_tlu_plus_files (2), **extract_rc** (2), **create_ilm** (2).

ILM-27 (information) Using parasitics (%s) from PARA view for design '%s'

DESCRIPTION

You will see this message during **create_ilm** if the parasitics are being used from corresponding PARA view.

WHAT NEXT

This is informative message, no action is required.

SEE_ALSO

set_tlu_plus_files (2), **extract_rc** (2), **create_ilm** (2).

ILM-28 (error) Failed to save parasitics (%s) file for design '%s'

DESCRIPTION

You will see this message during **create_ilm** if RC extraction has failed.

WHAT NEXT

Check if any error issued by RC extraction. Check/set tlu_plus file settings, run **extract_rc** and run **create_ilm** again.

SEE_ALSO

set_tlu_plus_files (2), **extract_rc** (2), **create_ilm** (2).

ILM-29 (information) Generated and attached parasitics (%s) file to '%s.%s'.

DESCRIPTION

This message is issued by create_ilm to indicate successful generation and storage of parastics in ILM view. RC indicates parasitic file for timing while CC indicates coupling cap parasitics.

WHAT NEXT

This is informative message, no action is required.

SEE_ALSO

set_tlu_plus_files (2), **extract_rc** (2), **create_ilm** (2).

ILM-30 (error) Failed to generate or attach parasitics for ILM '%s'

DESCRIPTION

You will see this message if parasitics generation or saving them to MW has failed.

WHAT NEXT

Check if any error messages issued by RC extraction, create_ilm to find out possible causes. Check/set TLUPlus file settings, run **extract_rc** and run **create_ilm** again.

SEE_ALSO

set_tlu_plus_files (2), **extract_rc** (2), **create_ilm** (2).

ILM-31 (information) Generated and attached SI aggressor info

file to %s.%s.

DESCRIPTION

This message is issued by create_ilm to indicate successful generation and storage of SI aggressor info file to the ILM.

WHAT NEXT

This is informative message, no action is required.

SEE_ALSO

set_tlu_plus_files (2), **extract_rc** (2), **create_ilm** (2).

ILM-32 (error) ILM ’%s’ does not have required (%s) file.

DESCRIPTION

You will see this message if one or more of the ILM instances do not have SI aggressor info file in the associated ILM view. This could be due to, not using **-include_xtalk** option of **create_ilm** or some errors occured during **create_ilm -include_xtalk**. All ILMs will need to have SI aggressor info files in the respective ILM views for top-level SI analysis to consume SI information from ILM. This command will however continue without the SI aggressor file but the SI analysis may be inaccurate due to not accounting for aggressors from removed logic during ILM creation.

WHAT NEXT

Check the options and output of **create_ilm** command used to create the reported ILM. Re-run with the corrected settings.

SEE_ALSO

create_ilm (2).

ILM-33 (error) Failed to save SI aggressor info file for design

’%s’

DESCRIPTION

You will see this message during **create_ilm** if RC extraction has failed.

WHAT NEXT

Check if any error issued by RC extraction. Check/set TLUPlus file settings. Check if the design has been routed. Check if the si_options are properly set using the set_si_options command. Check if hierarchical SI flow has been enabled using the enable_hier_si variable. Check if the necessary licenses are available.

SEE_ALSO

set_tlu_plus_files (2), **extract_rc** (2), **create_ilm** (2).

ILM-34 (error) Invalid options. Cannot specify ’%s’ option with ’%s’.

DESCRIPTION

The listed command options are dependant. -keep_macros can not be specified with -no_physical option.

WHAT NEXT

Look at the manpage for this command for more information on command options.

ILM-35 (Warning) Master cell of macro %s is not %s.FRAM.

DESCRIPTION

You will see this message during **propagate_ilm** if the block does not have a FRAM view or even if the block has a FRAM view, but the master of the instance is not the FRAM view. Block boundary will be read from ILM view. All metal layers over the block will be blocked for top-level routes.

WHAT NEXT

Create a FRAM view for the macro block if it does not exist. Change the master of the macro instance to FRAM view using the command **change_macro_view**.

SEE_ALSO

change_macro_view (2), **create_ilm** (2).

ILM-36 (error) TLUPlus files (for parasitic corner #%d) did not match between Top design and ILM.
Top design: %s
ILM (%s): %s

DESCRIPTION

You are seeing this message because the TLUPlus files for the Top design and the reported ILM did not match. This can happen, if the total number or names of TLUPlus files used for active scenarios when the ILM is created do not match with the total number or names of TLUPlus files used when extract_rc is run at the top-level.

WHAT NEXT

Review the scenarios and TLUPlus settings used for create_ilm and top-level to check if they are according to the ILM/MCMM flow usage recommendations.

SEE_ALSO

set_tlu_plus_files (2) **report_tlu_plus_files(2) ILM-37(n) ILM-68(n) ILM-69(n)**

ILM-37 (warning) Potential mismatch of TLUPlus files (for parasitic corner #%d) for Top design and the ILM since they are from two different directories:
Top design: %s,
ILM(%s): %s

DESCRIPTION

You are seeing this message because the TLUPlus files used for the top design and the reported ILM have same names but are residing in two different directories. ILM/MCMM flow requires the consistent use of TLUPlus files at the block level when ILM was created and at the top-level when ILM was used. The difference of directory may actually mean a different TLUPlus file being used for create_ilm and top-level extract_rc and can lead to inconsistent use of RC for ILM nets.

WHAT NEXT

Review the TLUPlus files reported and make sure they are actually represent the same parasitic corner. If the TLUPlus file names meant for different corner happen to have the same name, rename the TLUPlus file so that file names are unique.

Review the scenarios and TLUPlus settings used for create_ilm and top-level to check if they are according to the ILM/MCMM flow usage recommendations.

SEE_ALSO

set_tlu_plus_files (2) **report_tlu_plus_files** (2) **ILM-36(n) ILM-68(n) ILM-69(n)**

ILM-38 (warning) %s nets do not have delays calculated. Running extract_rc to extract RC and calculate delays.

DESCRIPTION

This warning message occurs when some nets do not have delays calculated. This scenario can occur due to use of some commands that remove delays from nets like remove_annotated_delay, set_delay_calculation, remove_sdc commands. create_ilm command checks for nets not having delays and runs extract_rc estimate and extract_rc (if the design is routed) commands as a corrective measure to calculate the delays.

WHAT NEXT

Review the commands that were run prior to create_ilm to find out the reason for some nets not having delays. Run recommended commands like extract_rc to calculate the delays. No action is required if the corrective action of running extract_rc estimate and extract_rc is sufficient for the flow.

SEE ALSO

ILM-39 (error) Failed to save TLUPlus signature file for design '%s'

DESCRIPTION

You will see this message during **create_ilm** if saving the TLUPlus signature file has failed. TLUPlus signature file is different from TLUPlus files. TLUPlus signature file has a mapping between the extraction data and the TLUPlus files and temperature used for extraction. For example: If there are two TLUPlus files TLUP1, TLUP2 and extraction is done using TLUP1 for temperatures 25,40 and extraction is done using

TLUP2 for temperatures 25, 40 and 80, the TLUPlus signature file has extraction data mapped to each of the (TLUP1,25), (TLUP1,40), (TLUP2,25), (TLUP2,40), (TLUP2,80) pairs. This mapping information is needed to match the extraction data from ILM with top-level and successfully stitch the ILM RC with top-level RC data. This file is automatically generated by the tool when extraction runs successfully. This error may happen because of attached TLUPlus file.

WHAT NEXT

Set the TLUPlus files using the **set_tlu_plus_files** command after linking the deisgn. Run **create_ilm** again and watch out for RCEX-046 message.

SEE_ALSO

set_tlu_plus_files (2), **extract_rc** (2), **create_ilm** (2), **RCEX-046(n).**

ILM-40 (information) %s to include the netlist from the ILMs into current_design.

DESCRIPTION

You will see this message as information of start or end of flattening during **create_ilm** when netlist from the ILMs will be included into the current_design.

WHAT NEXT

This is informative message. No action required.

SEE_ALSO

create_ilm (2).

ILM-41 (Error) Cell '%s' an ILM block.

DESCRIPTION

The cell provided as argument on the command line is an ILM block. This command can be used to propagate information for non-ILM blocks only. If you are using this command to propagate placement or annotated delay information for an ILM block, please use the **propagate_ilm** command instead.

WHAT NEXT

Please remove any ILM cells from cell list or use the **propagate_ilm** command.

SEE ALSO

propagate_ilm(2), propagate_annotated_delay_up(2). propagate_placement(2).

ILM-42 (Error) This command is obsolete, use propagate_ilm.

DESCRIPTION

This command is obsolete. If you are using this command to propagate delay information for an ILM block, please use the **propagate_ilm** command instead.

WHAT NEXT

Use the **propagate_ilm** command.

SEE ALSO

propagate_ilm(2).

ILM-43 (error) No ILM sub-designs in current design.

DESCRIPTION

You are trying to run a command which works on Interface Logic Model sub-designs in the current design. As there are none, this command is issuing this error.

WHAT NEXT

Please read in db files for the ILM sub-designs, link the design and try this command again.

SEE_ALSO

propagate_ilm (2), **propagate_placement** (2).

ILM-44 (warning) Nested ILM sub-design %s has dont_touch

attribute.

DESCRIPTION

You receive this message if **create_ilm** command has detected nested ILM blocks having dont_touch attribute. During ILM extraction, the **create_ilm** command will retain all logic in blocks with dont_touch attribute so this can cause the extracted ILM to contain unnecessary extra logic.

WHAT_NEXT

For each ILM sub-design nested in the current design, set the current design to the nested ILM sub-design and execute **set_dont_touch [current_design] false** command. Then, with the current design set to the original top design, run the **create_ilm** command.

SEE_ALSO

create_ilm (2).

ILM-45 (Error) Interface logic of design '%s' has already been identified.

DESCRIPTION

The interface logic of the design has already been identified. The **create_ilm** command was already executed on this design perhaps with a different set of options. This command should not be executed multiple times on the same design.

WHAT NEXT

Read in the original design and then run the **create_ilm** command with the appropriate options.

SEE ALSO

create_ilm(2), propagate_ilm(2).

ILM-46 (Error) The -output option of create_ilm command is

obsolete, use write command to save ILM.

DESCRIPTION

The -output option of create_ilm commands is obsolete and no longer supported. Instead use **write** command to save ILM into a file.

WHAT NEXT

Use **write** command to save ILM into a file.

Suppose, your script has following lines: create_ilm -output block_ilm.db

the following change is required. create_ilm write -f db -hier -output block_ilm.db

If you are running the tool in XG mode, you can save the created ILM to the Milkyway design library, for example:

create_ilm write_milkyway -output block

Refer to the latest Application Notes for more details of ILM flow when using XG mode.

SEE ALSO

create_ilm(2), write(2), write_milkyway(2).

ILM-47 (error) Missing -ilm_core option.

DESCRIPTION

You receive this message if you execute **create_ilm** or **create_ilm** with the **-optimizable** option, but the **-ilm_core** option is ommited. If you use the **-optimizable** option, you must specify a ilm_core file used for saving core design for later merging.

WHAT NEXT

Specify file name for storing ilm_core file using -ilm_core option.

SEE ALSO

create_ilm(2), merge_ilm(2).

ILM-48 (warning) Assigned (0,0) location to Port '%s'. Reason: Either dangling port or PG port with no location.

DESCRIPTION

You receive this message in either of the following cases: if a PG port's location is missing or if a dangling non-PG port's location is missing. Dangling port is a port which is not connected to any other cell inside the block. In general, all ports and cells will need to have physical location to run create_ilm and avoid problems in top-level.

WHAT NEXT

Review the floorplan and set port location accordingly and rerun create_ilm

SEE ALSO

create_ilm (2). **ILM-16** (n)

ILM-49 (warning) Failed to find mw_id information for %s : '%s' to associate RC information while using ILMs.

DESCRIPTION

You will see this message if current command fails to find mw_id information for net or pin while trying to associate RC data while using ILMs. This can happen for multiple reasons:

1) This may be a dummy/floating or constant net where RC is not available/not required. In this case you may ignore this message. 2) The pin/net does not exist in ILM and for some reason started showing up at the top-level. In this case the most likely cause would be one of the optimization commands run prior to this command have inserted a net/cell into ILM. 3) Some command in the flow has abnormally terminated. In such a case you can fix the issue and re-start the flow with good version of database.

WHAT NEXT

Watch for the RCEX-060 messages later in the flow. If you find RCEX-060, check the routing and RC data of reported nets at the block-level and at the top-level. In case of boundary nets, ensure that both portions of the net (inside and outside the ILM) are routed. In case this error is issued due to abnormal termination of some prior command, fix the reported issue of that command and re-start the flow with good version of database.

SEE_ALSO

extract_rc (2), **create_ilm** (2).

ILM-50 (warning) ILM design or sub-design %s in file %s has same name as another design. Renamed it as %s.

DESCRIPTION

You will see this message if any ILM design or sub-design is renamed. If the **link** command detects multiple ILM designs or sub designs with same name in the link_library, the link automatically renames the design and then updates the instances in the ILM file containing the design, to refer to the renamed design (**ILM-51**).

WHAT NEXT

If **link** has chosen the design you want to use, you do not need to take any action.

SEE_ALSO

ILM-51 (n), **link** (2).

ILM-51 (warning) Instance '%s' in design '%s' is updated to refer to renamed design '%s'.

DESCRIPTION

You will see this message if any ILM design or sub-design is renamed. If the **link command detects multiple ILM designs or sub designs with same name in the link_library, the link** automatically renames the design (**ILM-50**) and then updates the instances in the ILM file containing the design, to refer to the renamed design.

WHAT NEXT

If **link** has chosen the design you want to use, you do not need to take any action.

SEE_ALSO

ILM-50 (n), **link** (2).

ILM-52 (Error) The specified cel name (%s) does not match with current design name (%s). Failed to save ILM to Milkyway.

DESCRIPTION

The MW cel name specified for ILM storage does not match with the ILM design name. This mismatch can lead to "link" errors when top-design and ILMs are being linked for top-level optimization.

WHAT NEXT

Specify the ILM design name as MW cel name for storing ILM.

Suppose, your ILM design name is 'foo', use the following command to store ILM to milkyway.

psyn_shell-t> current_design foo psyn_shell-t> write -format milkyway -output foo

SEE ALSO

write (2), **read_file** (2).

ILM-53 (Warning) The design name (%s) of the loaded ILM does not match with the cel name (%s). This can potentially lead to "link" errors later.

DESCRIPTION

The design name of the ILM loaded from Milkyway does not match with the cel name. This can potentially lead to "Unresolved references" errors when top-design and ILMs are being linked for top-level optimization.

WHAT NEXT

Rename the design if you see problems during "link".

SEE ALSO

write (2), **read_file** (2), **ILM-52** (n).

ILM-54 (error) Found feed-through or multiple-port net '%s'. This

net must be buffered before creating ILM.

DESCRIPTION

This error message occurs when the design has a net connected to more than one port and you are trying to create ILM for that design. The reported net could be a net driving multiple output ports or it could be a feed-through net connecting input and output ports (feed-through pins) directly. These nets must be buffered to make them connect only one port before creating the ILM.

WHAT NEXT

Use **set_fix_multiple_port_nets** command to fix these nets so that no net is connected to more than one port. Rerun the command after fixing the reported nets.

SEE ALSO

set_fix_multiple_port_nets(2).

ILM-55 (error) Failed to check top and ILM TLUPlus consistency.

DESCRIPTION

You will see this error if the tool has failed to check if TLUPlus settings are consistently used between the top-level and the ILM.

WHAT NEXT

Review the errors issued prior to this error and fix the reported problem.

Review the scenarios and TLUPlus settings used for create_ilm and top-level to check if they are according to the ILM/MCMM flow usage recommendations.

SEE ALSO

report_tlu_plus_files(2), set_tlu_plus_files(2), ILM-39(n).

ILM-56 (error) ILM ’%s’ does not have required TLUPlus

signature file.

DESCRIPTION

You will see this error if the TLUPlus signature file attached to the reported ILM is not found. TLUPlus signature file is different from TLUPlus files. TLUPlus signature file has a mapping between the extraction data and the TLUPlus files and temperature used for extraction. For example: If there are two TLUPlus files TLUP1, TLUP2 and extraction is done using TLUP1 for temperatures 25,40 and extraction is done using TLUP2 for temperatures 25, 40 and 80, the TLUPlus signature file has extraction data mapped to each of the (TLUP1,25), (TLUP1,40), (TLUP2,25), (TLUP2,40), (TLUP2,80) pairs. This mapping information is needed to match the extraction data from ILM with top-level and successfully stitch the ILM RC with top-level RC data. This file is automatically generated by the tool when extraction runs successfully. Most likely there are one or more errors during create_ilm in generating the TLUPlus signature file.

WHAT NEXT

Set the TLUPlus files for the block using the **set_tlu_plus_files** command after linking the design. If the design uses MCMM scenarios, review the scenarios and TLUPlus settings. Recreate ILM for that block. Watch for RCEX-046 and ILM-39 messages. Use the the newly created ILM at the top-level.

SEE ALSO

report_tlu_plus_files(2), set_tlu_plus_files(2), create_ilm(2), ILM-39(n), RCEX-046(n).

ILM-57 (error) Mismatch of total number of TLUPlus files used in ILM %s and Top.,Äù

DESCRIPTION

You will see this error if the total number of TLUPlus files used for extraction is different for the reported ILM and Top design.

WHAT NEXT

Review the TLUPlus file settings used for the reported ILM and make sure that they match between the top design and the ILM.

Review the scenarios and TLUPlus settings used for create_ilm and top-level to check if they are according to the ILM/MCMM flow usage recommendations.

SEE ALSO

report_tlu_plus_files(2), set_tlu_plus_files(2).

ILM-58 (error) Level shifter pin %s is not connected to any other leaf load/driver pin. check_mv_design at top-level may fail.

DESCRIPTION

You will see this error if level shifter pin is not connected to any other leaf load/driver pin or it is connected to logic hierarchy. If the level shifter pin is connected to logic hierarchy and have the operating condition defined on that logic hierarchy then such connenction may not exists at top level. This is because logic hierarchy is retained only if it is a non-empty hierarchy.

WHAT NEXT

You may need to attach the level shifter pin to some load and re-run the create_ilm.

SEE ALSO

create_ilm(2), check_mv_design(2).

ILM-60 (error) Design is a route-cache.

DESCRIPTION

The design being used is a route-cache. Using a route-cache with this flow is not supported. A real design, loaded from a Milkyway design library, on disk, is required to continue.

WHAT NEXT

To continue you need to write the design to disk using the **write_milkyway** command. After this is done, you may proceed as usual.

SEE ALSO

write_milkyway(2).

ILM-61 (error) Design contains data from previous optimization/

extract_rc run.

DESCRIPTION

The design that you are trying to run On-Route optimization/extract_rc on has data from a previous run. This might have occured due to interruption of a previous run of the command.

WHAT NEXT

ILM-62 (error) Could not read ILM '%s.%s'.

DESCRIPTION

This error occurs because the tool was unable to open the specified interface logic model (ILM) so it cannot proceed. This could be due to several reasons, such as insufficient permissions for reading or the design being locked.

WHAT NEXT

Ensure that The ILM block specified is the one that should be read and that it is readable. (It requires sufficient UNIX permissions.) Ensure that the block and design are not locked.

ILM-63 (error) Could not get block location/offset for block '%s'.

DESCRIPTION

This error occurs because the tool was unable to retrieve either the location or offset of this block or both. These values must be set before On-Route optimization can proceed.

WHAT NEXT

You should read the location for the block from the top-level Design Exchange Format (DEF) or Physical Design Exchange Format (PDEF) file or set it by using the **set_cell_location** command.

SEE ALSO

set_cell_location(2)

ILM-64 (error) Die/core area not defined for '%s'.

DESCRIPTION

This error occurs because the tool was unable to retrieve either the die area or the core area of the specified block or both. These are necessary in order to proceed.

WHAT NEXT

You can read the block die and core areas from the Design Exchange Format (DEF) or Physical Design Exchange Format (PDEF) file or use the **set_die_area** and **set_placement_area** commands to manually set them.

SEE ALSO

set_die_area(2)
set_placement_area(2)

ILM-65 (error) ILM block '%s' does not contain route data.

DESCRIPTION

The specified ILM block contains no routing data. For On-Route optimization to proceed, an ILM of the routed block is required.

WHAT NEXT

Make sure that the CEL view of the block is routed, read it in using **read_milkyway**, and re-create the ILM using the **create_ilm** command.

SEE ALSO

create_ilm(2), read_milkyway(2).

ILM-66 (error) Invalid or absent layer information.

DESCRIPTION

This error occurs when the tool is unable to retrieve the physical information for one or more layers.

WHAT NEXT

Ensure that the layer data is present in the library, and then rerun the last command.

ILM-67 (error) Could not get data for port '%s' from the Milkyway database.

DESCRIPTION

This error occurs because the tool was unable to retrieve data for the specified interface logic model (ILM) port from the Milkyway database. Without this information, On-Route optimization cannot continue.

WHAT NEXT

Ensure that all the port data for the block is included in the ILM and that this data is stored in the ILM view of the block.

ILM-68 (error) Mismatch in '%s' TLUPlus setting between Top design and ILM in scenario '%s'
Top TLUPlus file : '%s'
Block ('%s') TLUPlus file: '%s'

DESCRIPTION

You will see this error if the TLUPlus file name setting for the given condition (e.g. min or max) is different between the top-level and the given ILM in a particular scenario.

WHAT NEXT

Review the TLUPlus file settings used for the reported scenario make sure that they match between the top design and the ILM.

Review the scenarios and TLUPlus settings used for create_ilm and top-level to check if they are according to the ILM/MCMM flow usage recommendations.

SEE ALSO

create_ilm(2), report_tlu_plus_files(2), set_tlu_plus_files(2). ILM-69(n)

ILM-69 (warning) Potential mismatch in '%s' TLUPlus setting between Top design and ILM in scenario '%s' since they are from two different directories.
Top design: %s,
ILM (%s): %s

DESCRIPTION

You are seeing this message because the TLUPlus files used for the top design and the reported ILM have same names but are residing in two different directories. ILM/MCMM flow requires the consistent use of TLUPlus files at the block level when ILM was created and at the top-level when ILM was used. The difference of directory may actually mean a different TLUPlus file being used for create_ilm and top-level extract_rc and can lead to inconsistent use of RC for ILM nets.

WHAT NEXT

Review the TLUPlus files reported and make sure they are actually represent the same parasitic corner. If the TLUPlus file names meant for different corner happen to have the same name, rename the TLUPlus file so that file names are unique.

Review the scenarios and TLUPlus settings used for create_ilm and top-level to check if they are according to the ILM/MCMM flow usage recommendations.

SEE ALSO

create_ilm(2), report_tlu_plus_files(2), set_tlu_plus_files(2). ILM-68(n)

ILM-70 (error) Scenario '%s' is not available in %s

DESCRIPTION

You will see this error if the scenarios present in the top-level design does not match with the scenarios present in ILM by name. ILM can have additional scenarios which are not defined in the top-level design.

WHAT NEXT

To fix this error, you must create the scenario for the given(sub)design. Note that if you are changing the set of scenarios in an ILM, you must load the entire block-level design, define scenarios as appropriate, and then recreate the ILM for that block using the **create_ilm** command.

SEE ALSO

create_ilm(2), create_scenario(2), remove_scenario(2).

ILM-71 (Warning) Unconnected pin '%s' has different case values across scenarios. set_case_analysis are applied automatically to this ILM pin. These should be made available at the top level using propagate_constraints. Details: %s

DESCRIPTION

You will see this message if there is some pin in the block for which you are creating an ILM, which has different case values across scenarios. For example, a given pin might have a case value '0' in scenario 'scene1' and case value '1' in scenario 'scene2'. The case_values on the reported pin might have been as a result of user case settings on ports or other pins and propagated to this pin. At the unconnected pins, which are as a result of logic removal, create_ilm uses the case values to create logic0/1 cells based on the case_value at this pin. In case of conflicting values, it applied set_case_analysis constraint instead of creating logic0/1 cell connections for this pin. Note that these values will **not** be available at the top level unless you use the **propagate_constraints -case_analysis** command.

WHAT NEXT

Use the propagate_constraints -case_analysis command at the top level to propagate these values to top-level.

SEE ALSO

create_ilm(2), propagate_constraints(2).

ILM-72 (error) Multi-mode/Multi-corner flow is not supported with ILMs.

DESCRIPTION

You will see this error if your try to create an ILM for a design which has multiple scenarios. Concurrent Multi-mode and Multi-corner optimization are currently not supported in the ILM flow.

WHAT NEXT

Support for mutliple modes/corners will be added in an upcoming release.

SEE ALSO

create_ilm(2).

ILM-73 (error) Inconsistent use of ILM %s in MCMM flow. %s has scenarios defined while %s does not have scenarios defined.

DESCRIPTION

You receive this message if the top-design has scenarios defined and the reported ILM does not have scenarios defined or vice versa.

WHAT NEXT

If you intend to use MCMM flow with ILM, make sure that you create scenarios in top level as well as ILM as per the recommended flow. If you are using non MCMM flow make sure that there are no scenarios in either ILM or TOP. Mixing non-MCMM top with MCMM ILM is not allowed and mixing MCMM top with non-MCMM ILM is also not allowed .

SEE ALSO

ILM-74 (warning) ILM does not contain required information related to MCMM. Re-generate the ILM with latest image.

DESCRIPTION

You receive this message if you have created ILM with an older version of IC compiler. The tool did not find required information from this ILM You need to recreate the ilms. If you are using non-MCMM flow you may safely ignore this warning.

WHAT NEXT

Recreate the ilm.

ILM-75 (error) Unable to find location of the cell %s. Failed to propagate.

DESCRIPTION

You receive this message if the tool is not able to find and propagate the location information of a cell from ILM to top-level design.

WHAT NEXT

To check if all leaf cells inside ILM block have locations, you can set current design as the reference design of the ILM block instance, and then run the **report_cell -physical** command.

To ensure that all ILM leaf cells have locations, create ILM for the block after the block has been placed.

If you find that this cell instance does not exist in original block or ILM, this could have been incorrectly added by one of the previous optimization commands. Trace back to the actual command causing this problem. If any of the previous optimization commands have abnormally terminated, restart the session.

ILM-76 (warning) Scenario %s is not active and will not be saved in the ILM.

DESCRIPTION

You receive this message if there are some scenarios which are not active during ILM creation. **create_ilm** saves scenario data of only active scenarios.

WHAT NEXT

Activate the scenarios which are not active by using the command **set_active_scenarios** and run **create_ilm** again.

SEE_ALSO

set_active_scenarios (2), **create_ilm** (2).

ILM-77 (error) create_ilm command cannot be run on an

auto_cel CEL.

DESCRIPTION

You receive this message if the current_mw_cel is an auto_cel.

WHAT NEXT

Save the current_mw_cel to a valid cel using the command save_mw_cel with the -as option. Then run create_ilm.

ILM-78 (error) ILM loading failed because latest version of %s.%s is more recent than the latest version of %s.%s.

DESCRIPTION

You receive this message if you have modified the CEL view after creating the ILM. This check is to prevent loading an outdated ILM.

WHAT NEXT

Check your create_ilm/block-level script and avoid save_mw_cel after create_ilm. Alternatively recreate the ILM and load it at the top-level.

ILM-79 (error) Option -in_context can be used only with -compact <output/all> option.

DESCRIPTION

You receive this message if you are using -in_context without the -compact <output/all> option in create_ilm_models command. The option -in_context generates compact ILMs that are in context with the top level timing.

WHAT NEXT

Use -compact <output/all> along with -in_context option of create_ilm_models.

SEE_ALSO

create_ilm_models (2),

ILM-80 (Error) Unconnected pin '%s' has different case values across scenarios. Recommend re-creating ILM with '-case_controlled_ports' or '-compact none -traverse_disabled_arcs' to avoid the problem.

DESCRIPTION

You will see this message if there is some pin in the block for which you are creating an ILM, which has different case values across scenarios. For example, a given pin might have a case value '0' in scenario 'scene1' and case value '1' in scenario 'scene2'. The case_values on the reported pin might have been as a result of user case settings on ports or other pins and propagated to this pin. At the unconnected pins, which are as a result of logic removal, create_ilm uses the case values to create logic0/1 cells based on the case_value at this pin. In case of conflicting values, it can not create such logic0/1 cell to connect to unconnected input pin. You can avoid this problem by re-creating ILM with additional '-case_controlled_ports' or '-compact none -traverse_disabled_arcs' options.

WHAT NEXT

Recreate ILM with the recommended options.

SEE ALSO

create_ilm(2).

ILM-81 (information) Skipping net %s for ILM preprocessing as it is %s net.

DESCRIPTION

This message is generated while preprocessing ILMs for high fanout synthesis. You will see this information message if a buffer can not be inserted in net.

The current preprocessing of ILMs does not insert buffers if the net is . an ideal . dont touch . three state bus . tristate . drc disabled . multiple driver . constant

WHAT NEXT

This is an information. No action required.

SEE ALSO

ILM-82 ILM-83

ILM-82 (information) Inserted buffer on net %s for isolating ILM pin %s.

DESCRIPTION

This message is generated while preprocessing ILMs for high fanout synthesis. You will see this information message when the preprocessing step inserts a buffer to isolate the ILM pin.

WHAT NEXT

This is an information. No action required.

SEE ALSO

ILM-81 ILM-83

ILM-83 (error) No suitable buffer found for isolating %s pin.

DESCRIPTION

This message is generated while preprocessing ILMs for high fanout synthesis. You are seeing this message because preprocessing step was not able to find a suitable buffer in the library to isolate the ILM pin.

WHAT NEXT

Make sure that you have buffer definitions in the library and rerun the high fanout synthesis command.

SEE ALSO

ILM-81 ILM-82

ILM-85 (error) No current design found. Please open the top

level design.

DESCRIPTION

You receive this message if you are using create_ilm_models -in_context without opening any top level design. The option -in_context needs a top level design which has been linked with existing ILM blocks.

WHAT NEXT

Use open_mw_cel to open the top design and rerun the create_ilm_models commands.

SEE_ALSO

create_ilm_models (2),

ILM-86 (error) No ILMs found in the design.

DESCRIPTION

You receive this message if you are using create_ilm_models -in_context on a design that has not been linked with existing ILMs.

WHAT NEXT

Create the ILMs using create_ilm_models or create_ilm. Open the top design and link them with ILMs created in the previous step. Now run create_ilm_models -in_context to create the in_context ILMs.

SEE_ALSO

create_ilm_models (2),

ILM-87 (error) Failed to open temporary file:%s for write

DESCRIPTION

An error has occurred while the tool was trying to write the file.

WHAT NEXT

Please make sure that the disk has enough space for the file to be written. Please

check the write permissions for the the file and directory and rerun the command.

SEE_ALSO

ILM-88 (error) ILM '%s' does not have required 'min' TLUPlus setting/data.

DESCRIPTION

You will see this message if the reported ILM does not have required 'min' corner parasitics. To use 'min' corner parasitics at the Top-level, the ILM must be extracted with 'min' TLUPlus setting. Otherwise the top-level extraction fails.

WHAT NEXT

Use report_tlu_plus_files and report_ilm commands to check the tluplus settings of TOP and ILM. If you do not intend to use 'min' corner, you may remove the min_tlu_plus option of the set_tlu_plus_files commands. Alternatively, you can re-create the ILM with both max and min TLUPlus settings and re-run commands at the top-level.

SEE_ALSO

create_ilm (2), **report_ilm** (2), **report_tlu_plus_files** (2), **set_tlu_plus_files** (2).

ILM-89 (error) Top design does not have required 'min' TLUPlus setting/extracted data to combine with ILM %s 'min' extracted data.

DESCRIPTION

You will see this message if the Top design does not have required 'min' corner extracted parasitics and one of the ILMs has such setting/data. To combine ILM and top-level extracted parasitics correctly either both ILM and TOP need to use 'min' TLUPlus setting or both should not use. Otherwise the top-level extraction fails.

Note that if you specify 'min' TLUPlus at the Top level then each of the ILMs are expected to have 'min' TLUPlus settings/data.

WHAT NEXT

Use report_tlu_plus_files and report_ilm commands to check the TLUplus settings of

TOP and ILM. If you do not intend to use 'min' corner, you may remove the min_tlu_plus option of the set_tlu_plus_files commands. Alternatively, you can re-create the ILM with corrected TLUPlus settings and re-run commands at the top-level.

SEE_ALSO

create_ilm (2), **report_ilm** (2), **report_tlu_plus_files** (2), **set_tlu_plus_files** (2).

ILM-90 (warning) The -include_xtalk option can't be used if design is '%s'. The coupling capacitance can be included only if design is either track assigned or detailed routed.

DESCRIPTION

You are seeing this message because the command expects the design to be either track assigned or detail routed for including the coupling capacitance and SI effective aggressor information in the ILM.

WHAT NEXT

Remove the -include_xtalk option while running create_ilm. Alternatively you can perform track assignment or detailed routing and run the create_ilm with -include_xtalk option.

SEE ALSO

create_ilm(2), route_global (2) **route_opt** (2)

ILM-91 (error) Found '%s.ILM' generated with older version of the tool. Please re-generate the ILM using latest version of the tool.

DESCRIPTION

You are seeing this message because the ILM used was generated with older version of the tool. Due to a backward compatibility issue, the older ILM is no longer usable in the later versions of the tool.

WHAT NEXT

Re-create the ILM with latest version of the tool. Check and ensure correct TLUPlus

settings before running create_ilm.

SEE ALSO

create_ilm(2),

ILM-92 (warning) The -keep_parasitics option can’t be used if design is not routed. The ILM creation will be continued without -keep_parasitics option.

DESCRIPTION

You are seeing this message because the command expects the design to be routed (either partially or fully) for including the RC tree information in the ILM. The ilm creation will be continued without -keep_parasitics option.

WHAT NEXT

If you want to include detailed RC parasitic information in ILM, then perform routing and run the create_ilm command.

SEE ALSO

create_ilm(2), route_global (2) **route_opt** (2)

ILM-93 (warning) Found ’%s.ILM’ generated with older version of the tool. The tool will automatically process the TLUPlus signature file attached to the ILM to maintain backward compatibility.

DESCRIPTION

You are seeing this message because the ILM used was generated with older version of the tool. TLUPlus signature file has a mapping between the extraction data and the TLUPlus files and temperature used for extraction. For example: If there are two TLUPlus files TLUP1, TLUP2 and extraction is done using TLUP1 for temperatures 25,40 and extraction is done using TLUP2 for temperatures 25, 40 and 80, the TLUPlus signature file has extraction data mapped to each of the (TLUP1,25), (TLUP1,40), (TLUP2,25), (TLUP2,40), (TLUP2,80) pairs. The tool automatically detects and takes corrective action to appropriately use the extraction related data from the ILM. This is to maintain supporting backward compatibility of reading older ILMs.

WHAT NEXT

This is a warning message and it will not affect the flow since the tool automatically detects and takes corrective action. Optionally, you can re-create the ILM with latest version of the tool to avoid this message.

SEE ALSO

create_ilm(2)

ILM-95 (error) Could not find TLUPlus signature file attached to top level '%s'

DESCRIPTION

You will see this error if the TLUPlus signature file attached to the top-level design is not found. TLUPlus signature file is different from TLUPlus files. TLUPlus signature file has a mapping between the extraction data and the TLUPlus files and temperature used for extraction. For example: If there are two TLUPlus files TLUP1, TLUP2 and extraction is done using TLUP1 for temperatures 25,40 and extraction is done using TLUP2 for temperatures 25, 40 and 80, the TLUPlus signature file has extraction data mapped to each of the (TLUP1,25), (TLUP1,40), (TLUP2,25), (TLUP2,40), (TLUP2,80) pairs. This mapping information is needed to match the extraction data from ILM with top-level and successfully stitch the ILM RC with top-level RC data. This file is automatically generated by the tool when top-level extraction runs successfully.

WHAT NEXT

If the design is is non-MCMM, please make sure setting TLUPlus files using **set_tlu_plus_files** command. If the design uses MCMM scenarios, review the scenarios and TLUPlus settings used. Please check for RCEX-046 warning messages and make sure you are not using any attached TLUPlus files. Make sure **set_tlu_plus_files** command is applied after design is linked.

SEE ALSO

report_tlu_plus_files(2), set_tlu_plus_files(2), RCEX-046(n).

ILM-96 (warning) Top level TLUPlus file name %s matches with more than one TLUPlus file names in ILM %s. The details of ILM

TLUPlus files: %s

DESCRIPTION

You will see this message during top level if the top level TLUPlus file name matches with more than one TLUPlus file names in ILM. For matching the top level TLUPlus file name with ILM TLUPlus file name, the tool considers only the basename of the TLUPlus file name. If you have two different TLUPlus files with same basename but in different directories, it will cause this warning.

WHAT NEXT

Check or set TLUPlus file settings to avoid such situation, rename the TLUPlus file to make them distinct and run **create_ilm** again.

SEE_ALSO

set_tlu_plus_files (2), **extract_rc** (2), **create_ilm** (2).

ILM-97 (warning) At the top level, in scenario %s TLUPlus file %s is associated with emulation TLUPlus file %s. In some other scenario, the same emulation TLUPlus file %s is associated with different TLUPlus file %s. Only the first association will be honored.

DESCRIPTION

This is happening for MCMM case and may be scenario are using conflicting TLUPlus setting across scenario.

WHAT NEXT

Correct the TLUPlus setting to avoid the conflicts. Check or set TLUPlus file properly and re-run the top level flow.

SEE_ALSO

set_tlu_plus_files (2), **extract_rc** (2), **create_ilm** (2).

ILM-98 (warning) At the top level, in scenario %s the emulation

TLUPlus file %s is associated with TLUPlus file %s. In some other scenario, the same TLUPlus file %s is associated with different emulation TLUPlus file %s. Only the first association will be honored.

DESCRIPTION

This is happening for MCMM case and may be scenario are using conflicting TLUPlus setting across scenario.

WHAT NEXT

Correct the TLUPlus setting to avoid the conflicts. Check or set TLUPlus file properly and re-run the top level flow.

SEE_ALSO

set_tlu_plus_files (2), **extract_rc** (2), **create_ilm** (2).

ILM-99 (error) Top level TLUPlus file %s does not have corresponding data in ILM %s. RC stitching of top and ILM will fail.

DESCRIPTION

You will see this message during top level if the top level TLUPlus does not have corresponding data in ILM. This may happen because of improper setting of TLUPlus files at the block or top level.

WHAT NEXT

Watch for ILM-97 and ILM-98 and review TLUPlus plus setting at block and top level.

SEE_ALSO

set_tlu_plus_files (2), **extract_rc** (2), **create_ilm** (2), **ILM-97(n), ILM-98(n).**

ILM-100 (Error) ICC ILM flow is not supported in DC-T in

2008.09.

DESCRIPTION

You receive this message when you use the ICC ILM flow in DCT in B2008.09 release.

WHAT NEXT

SEE ALSO

write_milklyway (2)

ILM-101 (Information) Loading link library %s.ILM from Milkyway library %s ...

DESCRIPTION

You receive this information message if you have ICC generated ILMs specified in your link_library variable. When you have ILM names specified in the link_library, the **link** command loads specified ILM from the MW design library or MW reference library. If you are loading ILM in IC Compiler, the recommended method is to use auto-load of ILMs by not specifying ILMs in the link_library variable.

WHAT NEXT

This is information message. If you are using IC Compiler, please remove the ILM from the link_library to allow the tool to auto load the ILM. If you are using other tools, no action is needed.

SEE ALSO

ILM-102(n)

ILM-102 (Information) Auto loading %s.ILM from Milkyway library %s ...

DESCRIPTION

You receive this information message if you have a cell instance in the design which is not linked to any of the library cells or designs specified in the link_library, and the tool has searched and loaded matching ILM from the MW design library or MW

reference library. If you are loading ILM in IC Compiler, this is the recommended method of ILM loading.

WHAT NEXT

This is information message. No action is needed.

SEE ALSO

create_ilm(2)

ILM-103 (Information) Saving ILM to milkyway view %s.ILM

DESCRIPTION

You receive this information message when ILM gets saved to Milkyway with the name specified in the information message.

WHAT NEXT

If you intend to save ILM with a different name, use appropriate command after **create_ilm** to save the design along with all the views to the name desired.

SEE ALSO

create_ilm(2),
save_mw_cel(2)
write_milkyway(2)

ILM-104 (Error) Unable to find %s of the ILM cell %s

DESCRIPTION

You receive this message when the location or dimension of the specified ILM cell cannot be found out. This can be due to missing location in the floorplan or not reading the floorplan. This will result in not propagating the physical information from the corresponding ILM.

WHAT NEXT

Check the floorplan of the design or check/set location on the reported cell. You may run **propagate_ilm -keepout -placement** after correcting the cell location to force tool to propagate the physical information from the ILMs. If you are using IC Compiler the physical information gets propagated automatically.

SEE ALSO

propagate_ilm (2)

ILM-105 (Error) The physical library has not been initialized.

DESCRIPTION

You receive this message if you have not specified the physical library to the tool or the tool failed to get physical information from the library.

WHAT NEXT

Follow the tool recommendation to provide the information of physical library. Check your physical library for any problems.

SEE ALSO

ILM-106 (Error) Failed to propagate keepouts from ILM

DESCRIPTION

You receive this message when the tool failed to propagate keepouts from the ILM.

WHAT NEXT

Check for any error messages issued prior to this message to get detailed information of the problem. Re-run this command after correcting the problem.

SEE ALSO

propagate_ilm(2).

ILM-107 (Error) Unable to find die area or core area of the design %s.

DESCRIPTION

You receive this message if die area or core area could not be obtained for the reported design/block.

WHAT NEXT

Check your floorplan data to find out why core area and die area are missing. Correct your floorplan data and re-run the flow with corrected design.

SEE ALSO

set_placement_area(2)
set_die_area(2)

ILM-108 (Warning) ILM will not contain physical information. Use -physical switch to create ILM with physical information.

DESCRIPTION

You receive this message if ILM is not created with physical information.

WHAT NEXT

Use -physical switch to create ILM with physical information.

SEE ALSO

create_ilm(2)

ILM-109 (Error) Cannot use include_xtalk option since hierarchical-SI feature is not enabled.

DESCRIPTION

You receive this message if you run **create_ilm -include_xtalk** but have the hierarchical-SI feature disabled by setting **set enable_hier_si false**.

WHAT NEXT

Please check your script to remove setting of **enable_hier_si** variable. The hierarchical-SI feature is ON by default and you need not set **enable_hier_si** variable to enable it.

SEE ALSO

enable_hier_si(3)

ILM-110 (error) Cannot specify '%s' without specifying '%s'.

DESCRIPTION

The listed command options are to be given together. Please use both options to avoid this error.

WHAT NEXT

Look at the manpage for this command for more information on command options.

ILM-111 (error) Net %s does not have extracted parasitics information.

DESCRIPTION

You will see this message if reported net don't have extracted parasitics during create_ilm. This could be due to reasons that include design is not routed or tool is not run as per recommended methodology or some other error occurred prior to this message. In general, the design must be routed prior to generating ILM with post-route extraction data. The nets having driver(s) or having connection to more than one pin are checked for existence of parasitics.

WHAT NEXT

Run extract_rc prior to create_ilm and save parasitics in SPEF format to isolate the problem.

SEE_ALSO

extract_rc (2), **write_parasitics** (2).

ILM-112 (information) Total %s (%s) nets have extracted parasitics information.

DESCRIPTION

The message indicate that total number of nets having extracted parasitics. Only the nets having a driver or having connection to more than one pin are considered for this reporting. If there are some nets not having extracted parasitics, this could be due to reasons that include design is not routed or tool is not run as per recommended methodology or some other error occurred prior to this message.

WHAT NEXT

To debug the nets with missing parasitics run extract_rc prior to create_ilm and save parasitics in SPEF format to isolate the problem.

SEE ALSO

extract_rc (2), **write_parasitics** (2).

ILM-121 (Error) %s attribute incorrectly set to false on ILM %s '%s'.

DESCRIPTION

The specified ILM instance or design has dont_touch attribute set to false. Ideally, all the ILM instances in the top-level needs to have dont_touch attribute set to true.

WHAT NEXT

Set the dont_touch attribute on the specified ILM to true and rerun the command.

SEE ALSO

set_dont_touch(2), all_dont_touch(2).

ILM-122 (Error) dont_touch value incorrectly set to false on %s '%s' inside ILM hierarchy '%s'.

DESCRIPTION

The specified cell or net inside the specified ILM hierarchy has dont_touch value set to false. Ideally, all the cells and nets inside ILM hierarchy needs to have dont_touch value set to true.

WHAT NEXT

Remove the dont_touch attribute on the specified cell or net or set the dont_touch attribute to true on the specified cell or net and rerun the command.

SEE ALSO

set_dont_touch(2), all_dont_touch(2), remove_attribute(2), ILM-121(n).

ILM-123 (Error) Mismatch in case_analysis setting on the ILM boundary pin '%s' between ILM '%s' and top-level design '%s'%s : block-level value: %s, top-level value: %s

DESCRIPTION

There is a mismatch in the case analysis value set on the ILM boundary pin from the top-level and the case analysis value set on the corresponding port in the block from which ILM was created. This mismatch is scenario specific in case of MCMM designs. Ideally both the case analysis value should match unless while creating the ILM, the particular port was specified in the port list for the case_controlled_ports option of **create_ilm** command.

WHAT NEXT

Either change the case analysis value on the specified pin in the top-level or change the case analysis value in the block for the corresponding port and recreate ILM.

SEE ALSO

set_case_analysis(2), remove_case_analysis(2), report_case_analysis(2), create_ilm(2).

ILM-125 (Error) Net '%s' is not clock tree synthesized.

DESCRIPTION

You receive this error message if the specified clock net is not clock tree synthesized. Clock tree synthesis for all clock trees had not been done in the block prior to ILM creation.

WHAT NEXT

If you need to use the ILM for top-level clock_opt, perform clock tree synthesis in the block, recreate ILM using **create_ilm** and use it in the top-level.

ILM-126 (Warning) The libraries from which ILM and %s are loaded are different for ILM instance %s. ILM Library: %s; %s Library: %s.

DESCRIPTION

You receive this warning message if the ILM and FRAM/CEL view for the specified ILM instance are present in different libraries. The difference in libraries means that there is a potential opportunity for the usage of inconsistent versions of ILM, FRAM/CEL views.

WHAT NEXT

Ensure that the required ILM, FRAM/CEL views from the required libraries are provided to the tool.

SEE ALSO

report_ilm (2), **ILM-129** (n).

ILM-128 (Error) Top-level PG connection is not made to ILM PG pin %s.

DESCRIPTION

You receive this error message if the top-level PG connection is not made to the specified ILM PG pin. This PG pin may in turn drives signal pins inside the ILM. With incomplete pg connection, the reported timing/delay is invalid since the signal pins will not get the propagated logic_0/logic_1.

WHAT NEXT

Create top-level PG connections to the specified ILM PG pin.

SEE ALSO

check_mv_design (2), **verify_pg_nets** (2), **derive_pg_connection** (2).

ILM-129 (Warning) Port %s in %s %s does not have matching

port in %s view.

DESCRIPTION

You receive this warning message if the specified port in ILM/FRAM/CEL view does not have a matching port in one of the other ILM/FRAM/CEL views as specified in the message. This can cause port connectivity issues.

WHAT NEXT

Ensure that the ports in ILM/CEL/FRAM views are consistent with each other. Ensure that the required version of ILM/FRAM/CEL is used by the tool.

SEE ALSO

get_ports (2), **ILM-126** (n).

ILM-130 (warning) Scenario %s is not part of scenario list used for create_ilm and this scenario will not be saved in the ILM.

DESCRIPTION

You receive this message if a scenario is not part of scenario list used during ILM creation. **create_ilm** saves scenario data of only scenarios provided in scenario list using -scenarios switch to create_ilm.

WHAT NEXT

Add the missing scenarios in the sceanrio list and run **create_ilm** again.

SEE_ALSO

create_ilm (2).

ILM-150 (error) Top-level extract_rc has extracted for more temperatures %s for TLUPlus file %s compared to ILM.
Top-level: TLUPlus file: %s, Temperatures: %s

ILM (%s) : TLUPlus file: %s, Temperatures: %s

DESCRIPTION

You will see this error message if the top level has additional set_operating_conditions applied compared to reported ILM. This leads to extract_rc not finding matching RC data in ILM for it to successfully stitch the ILM RC with top-level RC data. RC data between Top and ILM is matched by combination of TLUPlus file name and Temperature. If you have used emulation TLUPlus files at the top-level but not at the block-level or vice versa, tool will automatically match based any of TLUPlus file name or emulation TLUPlus file name. In such a case it is mandatory to specify both TLUPlus files and emulation TLUPlus files using set_tlu_plus_files command.

WHAT NEXT

Please verify the set_operating_conditions and set_tlu_plus_files settings at the top-level and block-level and make sure the settings used at the top-level are used while creating each of the ILMs. Correct the settings at the top-level and/or block-level. Re-create the ILM if block-level settings are changed.

SEE ALSO

report_tlu_plus_files(2), set_tlu_plus_files(2), report_lib(2), set_operating_conditions(2),

ILM-160 (Information) ILM design '%s' has some set_case_analysis constraints automatically set by create_ilm. Use propagate_constraints -case_analysis at top level.

DESCRIPTION

You will see this message if there is some pin in the block (for which you are creating an ILM), has different case values across scenarios. For example, a given pin might have a case value '0' in scenario 'scene1' and case value '1' in scenario 'scene2'. The case_values on such pin might have been as a result of user case settings on ports or other pins and propagated to this pin. At the unconnected pins, which are as a result of logic removal, create_ilm uses the case values to create logic0/1 cells based on the case_value at this pin. In case of conflicting values, it applied set_case_analysis constraint instead of creating logic0/1 cell connections for this pin. Note that these values will **not** be available at the top level unless you use the **propagate_constraints -case_analysis** command.

WHAT NEXT

Use the propagate_constraints -case_analysis command at the top level to propagate

these values to top-level.

SEE ALSO

create_ilm(2), propagate_constraints(2).

ILM-161 (information) Using mixed RC for boundary nets of ILM %s.

DESCRIPTION

You will see this message during top-level flow when Mixed RC is used for boundry nets of ILM.

WHAT NEXT

This is informative message. No action required.

SEE_ALSO

set_tlu_plus_files (2), **extract_rc** (2), **create_ilm** (2).

ILM-300 (Error) ICC ILM is temporarily not supported in this version of 2008.09 Design Compiler Release.

DESCRIPTION

You receive this message when you use the ICC ILM flow in DCT in B2008.09 release.

WHAT NEXT

For further details on support of ICC ILMs please contact Synopsys Support Center by using Enter A Call at http://solvnet.synopsys.com/EnterACall.

SEE ALSO

write_milklyway (2)

ILM-301 (error) The %s.ILM’s data model version is newer than

what is supported by this application.

DESCRIPTION

This ILM was created with an application using a newer data model version. You are attempting to open the ILM using an application that uses an older and incompatible version of the data model.

The data model version is not a user accessible attribute.

WHAT NEXT

Use a newer version of the application to open the ILM.

ILM-302 (error) The %s.ILM’s data model version is older than what is supported by this application. User must re-create the ILM using this version of the application.

DESCRIPTION

The ILM was created with an application using an older data model version. In order to open this ILM, the ILM must be updated to the current application’s data model version.

The data model version is not a user accessible attribute.

WHAT NEXT

Use the latest version of the application to re-create the ILM.

ILM-303 (information) The ILM %s was created using the command:%s

DESCRIPTION

This message will report the options using which the ILMs were created through the command create_ilm.

WHAT NEXT

This is an informative message. No action requierd.

SEE ALSO

ILM-301 ILM-302

ILM-305 (Warning) Option -keep_macros is not supported for DC netlist.

DESCRIPTION

You receive this message if you issue -keep_macros on a netlist that has been created using compile in non DC Topographical mode.

Please use this command with DC Topographical netlist.

WHAT NEXT

Please run compile_ultra in DC Topographical before you use -keep_macro

SEE ALSO

create_ilm(2)

ILM-351 (warning) Paths to/from port: %s %s (%s) are unconstrained. Retaining worst paths based on arrival time.

DESCRIPTION

Paths reaching to or starting from port %s %s (%s) are unconstrained. Compact ILM retain worst paths based on the slack value computation. Since the path reaching or starting from reported port is unconstrained slack value computation is not possible so compact ILM will retain paths based on the arrival times. The unconstrained paths can be due to SDC constraints like set_false_path, missing set_input_delay/ set_output_delay, missing clocks etc.

WHAT NEXT

Check the constraints applied on the design. Correct the SDC constraints and recreate the ILM. If you do not have SDC file or the SDC file is incomplete/ incorrect, please use ’-compact none’.

ILM-352 (warning) No clocks found in design %s. Creating non-

compact ILM.

DESCRIPTION

You will see this message if the design has no clocks defined and create_ilm is attempting to create a compact ILM (default). Compact ILM retains critical path based logic based on timing analysis. If the SDC is not provided or SDC is incomplete/incorrect it can produce inaccurate model. To avoid this problem, the tool has automatically switched to non-compact ILM.

No clock is defined in the design %s. Compact ILM retains logic based on timing analysis. Since no clock is present in the design, timing analysis cannot be done accuratly. For the accuracy of model non-compact ILM will be created for the design.

WHAT NEXT

Create clocks in the design.

ILM-353 (error) Option '-traverse_disabled_arcs' cannot be used with option '-compact all/output'. Use '-case_controlled_ports' instead.

DESCRIPTION

The option '-traverse_disabled_arcs' is incompatible with option '-compact all/output' in **create_ilm** command. The option '-traverse_disabled_arcs' disables the case_analysis. Disabling the case analysis values effect the timing critical paths. Since only four timing critical paths are retained from each port in case of compact ILM (all/output), this option is not applicable for '-compact all/output'. Note that '-compact all' is default option for **create_ilm** command.

Use '-case_controlled_ports' in place of '-traverse_disabled_arcs' if you want to create case independent ILM.

WHAT NEXT

To create case independent compact ILM use '-case_controlled_ports' in place of '-traverse_disabled_arcs'.

SEE ALSO

create_ilm(2).

ILM-351 (warning) Paths to/from port: %s (%s) are disabled or not present. No path retained to/from this port

DESCRIPTION

Paths reaching to or starting from port %s (%s) are either disabled or not present. Since the paths are not present or disabled so compact ILM will not retain any path from/to this port.

WHAT NEXT

Check the physical connection and constraints applied on this port. Correct the connectivity or constraints and recreate the ILM.

ILM-361 (information) UPF power domains are found in the design. Creating ILM with '-compact none -traverse_disabled_arcs'.

DESCRIPTION

You will see this message if the design has UPF power domains and create_ilm is being run. In order to generate a correct model, tool automatically add the options '-compact none -traverse_disabled_arcs'.

WHAT NEXT

This is information message. No action is needed.

SEE ALSO

create_ilm(2)

ILM-401 (Information) Found an ILM for %s (Reference: %s) in MW library %s. Checking link_library files for matching library cells...

DESCRIPTION

You receive this information message if a MW design library or MW reference library has an ILM view present for a macro cell instance of a MW design. For such

instances, all the link libraries will be scanned to find out if there is a library cell present for them. If library cells are not found then these instances are considered as a candidate to be linked to ILMs later.

WHAT NEXT

This is information message. No action is needed.

SEE ALSO

create_ilm(2)

ILM-402 (Information) Cell %s (Reference: %s) will be linked to an ILM from MW library %s.

DESCRIPTION

You receive this information message if a MW design library or MW reference library has an ILM view present for a macro cell instance of a MW design and for such instances there is no matching library cell present in any of the specified link libraries. All such instances are considered as a candidate to be linked to ILMs later.

WHAT NEXT

This is information message. No action is needed.

SEE ALSO

create_ilm(2)

ILM-403 (Information) Cell %s (Reference: %s) will not be linked to an ILM. Matching library cell found in the link_library '%s' file.

DESCRIPTION

You receive this information message if a MW design library or MW reference library has an ILM view present for a macro cell instance of a MW design but for such instances there is also a matching library cell present in one of the specified link libraries. Such instances will not be considered as candidates to be linked to ILMs later.

WHAT NEXT

This is information message. No action is needed.

SEE ALSO

create_ilm(2)

IMPT

IMPT-1 (error) The variable '%s' isn't defined.

DESCRIPTION

WHAT NEXT

IMPT-2 (error) The variable '%s' is of an unsupported external import option type.

DESCRIPTION

WHAT NEXT

IMPT-3 (error) Unknown import format '%s'.

DESCRIPTION

This error is generated when the **read** command encounters an invalid read (import) format.

WHAT NEXT

Invoke the **read** -help command for valid read (import) formats. Identify and correct format, then reinvoke the **read** command.

IMPT-4 (error) Cannot execute '%s'.

DESCRIPTION

WHAT NEXT

IMPT-5 (warning) The variable 'edifin_lib_%s_symbol' isn't

defined.

DESCRIPTION

WHAT NEXT

IMPT-12 (error) Expected a list. Found ’%s’.

DESCRIPTION

WHAT NEXT

IMPT-13 (error) Each list must contain three elements: sheet name, orientation and symbol name.

DESCRIPTION

WHAT NEXT

IMPT-14 (error) Sheet orientation must be ’landscape’ or ’portrait’. ’%s’ is invalid.

DESCRIPTION

WHAT NEXT

INFO-100 (information) Variable '%s' is obsolete and is being ignored.

DESCRIPTION

This version does not support the requested variable. This variable is being ignored.

WHAT NEXT

SEE ALSO

INFO-101 (information) Use of Variable '%s' is not recommended. This variable will be obsolete in a future release.

DESCRIPTION

Although this version support the requested variable. This variable will be obsolete in a future release.

WHAT NEXT

SEE ALSO

INFO-102 (information) Command '%s' is obsolete and is being ignored.

DESCRIPTION

This version does not support the requested command. This command is being ignored.

WHAT NEXT

SEE ALSO

INFO-103 (information) Use of command ’%s’ is not recommended. This command will be obsolete in a future release.

DESCRIPTION

Although this version support the requested command. This command will be obsolete in a future release.

WHAT NEXT

SEE ALSO

INFO-104 (information) This option "-cts_mode" is obsolete, use report_clock_tree for clocktree related information.

DESCRIPTION

If you wish to obtain clock network delay (clock latency) to any clock sink in CTS context, use report_clock_tree -to option.

WHAT NEXT

SEE ALSO

INFO-105 (information) Variable ’%s’ does not have any effect in compile_ultra.

DESCRIPTION

This variable is only applicable in **compile**.

WHAT NEXT

SEE ALSO

INFO-106 (information) Command '%s' does not have any effect in compile_ultra.

DESCRIPTION

This command is only applicable in **compile**.

WHAT NEXT

SEE ALSO

INFO-107 (information) Command '%s' is not available in '%s'.

DESCRIPTION

This message occurs when the specified command is not available. The requested command is only available in dc_shell.

WHAT NEXT

This is only an information message. No action is required.

INFO-108 (information) Variable '%s' has been consolidated under the variable '%s'.

DESCRIPTION

This information message advises you that the specified variable has been consolidated under another variable in this version. See the man page for the variable under which the consolidation occurred for details.

WHAT NEXT

This is an information message only. No action is required.

INFO-109 (information) Use of option '%s' is not recommended. This option will be removed in a future release. See the man page for more information.

DESCRIPTION

This information message advises you that although this option is supported in this version of the tool, it is considered obsolete and will be removed in a future release.

WHAT NEXT

Consult the man page for the command for further information.

INFO-110 (information) Option '%s' is obsolete and is being ignored.

DESCRIPTION

This information message occurs because this version does not support the requested option. The option is ignored.

WHAT NEXT

This is only an information message. No action is required.

INFO-111 (information) Command '%s' is obsolete and is being aliased to '%s'.

DESCRIPTION

This information message occurs when the requested command is not supported. The specified command is aliased to a newer command.

WHAT NEXT

This is an information-only message. No action is required.

INT

INT-1 (fatal) Unknown interrupt signal ’%d’ encountered.

DESCRIPTION

WHAT NEXT

INT-2 (information) Interrupting current command.

DESCRIPTION

WHAT NEXT

INT-3 (information) One more interrupt will exit process.

DESCRIPTION

WHAT NEXT

INT-4 (information) Process terminated by interrupt.

DESCRIPTION

WHAT NEXT

INT-5 (information) Preparing to interrupt optimization...

DESCRIPTION

This message indicates that a Control-c (SIGINT) was received by the process during the trials phase of compile, and compile is preparing to either print out a menu (interactive mode) or to write a checkpoint file (background mode). Compile must finish the current transform before the menu or checkpoint file can be written. It

may take a few minutes to finish the current transform, so please wait until you see that the checkpoint file has been written before hitting Ctrl-C again.

WHAT NEXT

No action is required on your part. If you want to abort the current compile, hit Control-c twice.

INT-6 (information) Aborting optimization...

DESCRIPTION

This message indicates that two Control-c signals (SIGINT) were received by the process after the Delay Optimization phase of compile, so compile will abort. **compile** will end optimization and return the design in its current state.

WHAT NEXT

No action is required on your part. If you want to abort the process, press Control-c three times.

INT-7 (information) Ignoring interrupt signal since the design is being mapped. One more interrupt will abort optimization without transferring the design...

DESCRIPTION

This message indicates that one Ctrl-C signal (SIGINT) was received by the process before the Delay Optimization phase of compile. Since the design is being mapped, compile will ignore the first interrupt signal. The second Ctrl-C will abort compile and not write out the design.

If you want to abort the process, then hit Ctrl-C three times in a row.

WHAT NEXT

INT-8 (information) Aborting optimization without transferring

the design...

DESCRIPTION

This message indicates that two Ctrl-C signals (SIGINT) were received by the process before the Delay Optimization phase of compile, so compile is going to abort. Compile will end optimization but not return the design in its current state because the design has not been fully mapped.

If you want to abort the process, then hit Ctrl-C three times in a row.

WHAT NEXT

LBDB-1 (error) The ’%s’ function requires %d arguments.

DESCRIPTION

This message indicates that the number of arguments passed to the specified function or the complex attribute is wrong. The Library Compiler expects a specific number of arguments for various functions and complex attributes. For example, the define_cell_area and the capacitive_load_unit require two arguments. A common cause of this error is the argument’s syntax definition. For example, the pin_equal complex attribute requires one quoted string as an argument instead of multiple strings

```
pin_equal("Q", "XQ");wrong
pin_equal("Q" "XQ");wrong
pin_equal("Q XQ");correct
```

WHAT NEXT

Change the technology library to correct the number of arguments. Refer to the "Library Compiler Reference Manual" for the syntax description.

EXAMPLES

```
/* Try the wrong number of arguments to these functions. */
define_cell_area(my_area,pad_slots,extra_junk);
capacitive_load_unit(1, pf, pf);
```

EXAMPLE MESSAGE

```
Error: Line 23, The ’define_cell_area’ function requires 2 arguments. (LBDB-1)
```

LBDB-2 (error) The value of argument %d of the ’%s’ function is of the wrong type. A value of ’%s’ type is required.

DESCRIPTION

This message indicates that the wrong value type has been set to the specified function argument. A common cause of this error is the alteration of argument order. For example, the capacitive_load_unit attribute expects a floating-point value then a unit of string type.

```
capacitive_load_unit( pf, 1);    wrong
capacitive_load_unit( 1, pf);    correct
```

WHAT NEXT

Change the technology library to correct the arguments. Refer to the "Library Compiler Reference Manual" for the syntax description.

EXAMPLES

```
  capacitive_load_unit( pf, 1);
```

In this case, the arguments of the capacitive_load_unit need to be switched.

EXAMPLE MESSAGE

```
Error: Line 17, The value of argument 1 of the 'capacitive_load_unit' function
is of the wrong type. A value of 'floating-point' type is required. (LBDB-2)
```

LBDB-3 (error) The '%s' value is invalid for the '%s' attribute. Its valid values are %s.

DESCRIPTION

This message indicates that the specified string value is not included in the list of accepted values. This error is often caused by a typo in the valid enumerated string value.

WHAT NEXT

Change the technology library to correct the invalid value.

EXAMPLES

```
  default_wire_load_mode : enclose;
```

In this case, the value should be 'enclosed'.

EXAMPLE MESSAGE

```
Error: Line 15, The 'enclose' value is invalid for the 'default_wire_load_mode'
attribute.
        Its valid values are top, segmented and enclosed. (LBDB-3)
```

LBDB-4 (error) The %s '%s' cannot be specified during

the update_lib command.

DESCRIPTION

Only library-level group statements can be added to an existing library using the update_lib command.

This message indicates that an invalid data (function, attribute, or group) has been found in the library to be added.

WHAT NEXT

Check the "Library Compiler User Guide" for valid data that can be added to existing libraries. Change the library to be updated appropriately.

EXAMPLES

Existing library

```
  default_wire_load_mode      : top;
```

You cannot specify the default_wire_load_mode attribute to be added to an existing library.

EXAMPLE MESSAGE

```
Error: Line 8, The group 'default_wire_load_mode' cannot be specified during
the update_lib command. (LBDB-4)
```

LBDB-5 (error) The library already has a '%s' attribute. It cannot be overwritten during the update_lib command.

DESCRIPTION

Only library-level group statements can be added to an existing library using the update_lib command.

This message indicates that an attribute has been found in the library to be added.

WHAT NEXT

Remove the existing attribute from the technology file.

LBDB-6 (error) The library already has a '%s' group; it cannot be overwritten during the update_lib command because it is permanent.

DESCRIPTION

This message indicates that an existing group is being overwritten in the library; the existing group is permanent. You cannot overwrite existing groups because their definitions might already have affected subsequent group declarations in the library. You can, however, add new ones.

WHAT NEXT

Change the library file to either remove the group or modify its name.

EXAMPLES

```
wire_load("05x05") {
    resistance : 0 ;
    capacitance : 1 ;
    area : 0 ;
    slope : 0.186 ;
    fanout_length(1,0.39) ;
}
```

EXAMPLE MESSAGE

```
Error: Line 1, The library already has a '05x05' group; it cannot be
       overwritten during the update_lib command because it is permanent. (LBDB-6)
```

LBDB-8 (information) The %s '%s' group has been successfully %s in the library.

DESCRIPTION

The **update_lib** command updates library groups in a given library. This message is for information purposes only and concerns cell and operating_conditions groups. However, if a wire-load model group is updated in a library, designs using that wire-load model must be reassigned a wire-load model.

WHAT NEXT

Use **set_wire_load_model** to set the wire-load model on designs using the modified

wire-load models.

EXAMPLE MESSAGE

```
Information: Line 1, The operating_conditions 'BCMIL' group has been successfully a
dded
             in the library. (LBDB-8)
Information: Line 8, The cell 'lbdb8' group has been successfully added
             in the library. (LBDB-8)
```

LBDB-11 (warning) The same '%s' attribute is defined twice and is ignored the second time.

DESCRIPTION

This message indicates that an attribute has been registered twice. The Library Compiler ignores the second value.

WHAT NEXT

Make sure that the attribute is defined only once.

LBDB-12 (warning) The '%s' attribute is the wrong type for the '%s' object.

DESCRIPTION

This message indicates that an attribute's value had a wrong type. The Library Compiler ignores the value.

WHAT NEXT

Make sure that the attribute's value is of the correct type.

LBDB-13 (warning) The '%s' enum has been defined twice and is being ignored.

DESCRIPTION

This message indicates that an enumeration value registered with an attribute has

been defined twice.

WHAT NEXT

Make sure that the enumeration value is defined only once.

LBDB-14 (error) The library already has a '%s' group; the library cannot be overwritten unless the -overwrite option is specified.

DESCRIPTION

This message indicates that a group has already been added by the **update_lib** command, and you are trying to overwrite it using the **update_lib** command again without specifying the -overwrite option.

WHAT NEXT

Either specify the -overwrite option to the update_lib command if you want to overwrite the same group or change the name of the group.

EXAMPLE MESSAGE

```
Error: Line 2, The library already has a 'lbdb14' group; the library
cannot be overwritten unless the -overwrite option is specified. (LBDB-14)
```

LBDB-16 (warning) Found a duplicate %s attribute. Using the latest value.

DESCRIPTION

This message indicates an attribute has been defined twice. The first definition is ignored.

WHAT NEXT

Remove the duplicate definition of the attribute.

EXAMPLES

```
    pin(Q) {
      direction : output;
      function : "1";
      function : "1";
```

```
    }
```

EXAMPLE MESSAGE

```
Warning: Line 59, Found a duplicate function attribute. Using the latest value. (LB
DB-16)
```

LBDB-17 (error) The library already has a type named '%s'. Type groups can never be overwritten.

DESCRIPTION

This message indicates that a type group already exists in the original library, and you are trying to overwrite it using the **update_lib** command again.

WHAT NEXT

Either remove the type group from the added library or change the name of the group in the file used for update.

EXAMPLES

```
type(bus2) {
  base_type : array;
  data_type : bit;
  bit_width : 2;
  bit_from : 0;
  bit_to : 1;
  downto : false;
}
```

The type named bus2 is defined in the library to be updated and the file used to update.

EXAMPLE MESSAGE

```
Error: Line 1, The Library already has a type named 'bus2'. Type
       groups can never be overwritten. (LBDB-17)
```

LBDB-18 (warning) In the '%s' library, the environment attribute

%s’s value is out of range.

DESCRIPTION

This message indicates that the nominal source voltage value defined in the library using nom_voltage attribute is less than 0. The library compiler ignores the value and takes the default nominal voltage. For a CMOS library, the default nominal voltage value is 5 volts.

WHAT NEXT

Change the value of the nom_voltage attribute to be greater than zero.

EXAMPLES

```
    nom_voltage : -5;
```

EXAMPLE MESSAGE

```
Warning: Line 29, In the library ’lbdb18’, the environment attribute
        nom_voltage’s value is out of range. (LBDB-18)
```

LBDB-19 (warning) Can’t find a pin named ’%s’ in the ’%s’ cell.

DESCRIPTION

This message indicates that one of the pin names in the list of the **pin_equal** or **pin_opposite** attribute or **gate_leakage** group is not defined in the cell. This often happens when there is a typo in the pin name.

WHAT NEXT

Check to see if there is a typo in the pin name. Otherwise, declare the pin in the technology library.

EXAMPLES

```
  cell(lbdb19) {
    area : 13;
    pin_opposite("Q","XQ");
    pin(Q, YQ) {
direction : output;
function : "1";
    }
  }
  cell(lbdb19_1) {
    area : 13;
```

```
    pin(Q, YQ) {
        direction : input;
        function : "1";
    }
    leakage_current() {
       gate_leakage(XQ) {
         input_high_value : 7.1;
         input_low_value : -8.7;
       }
    }
  }
```

EXAMPLE MESSAGE

```
Warning: Line 28, Can't find a pin named 'XQ' in the 'lbdb19' cell. (LBDB-19)
Warning: Line 218, Can't find a pin named 'XQ' in the 'lbdb19_1' cell. (LBDB-19)
```

LBDB-20 (warning) Cannot process 'pin_opposite' for the '%s' cell.

DESCRIPTION

This message indicates that the pins used in the list of the **pin_opposite** attribute are not found in the cell.

WHAT NEXT

Fix the pin names in the list of the pin_opposite attribute.

EXAMPLES

```
  cell(lbdb20) {
    area : 13;
    pin_opposite("Q","XQ");
    pin(Q, YQ) {
direction : output;
function : "1";
    }
    pin(YQ) {
direction : output;
function : "0";
    }
  }
```

In this case, the pins defined in the cell are 'Q' and 'YQ'. However, the pins listed in the pin_opposite attribute are 'Q' and 'XQ'.

EXAMPLE MESSAGE

```
Warning: Line 28, Can’t process ’pin_opposite’ for the ’lbdb20’ cell. (LBDB-20)
```

LBDB-23 (error) There is a missing timing arc between pins ’%s’ and ’%s’ in the ’%s’ cell.

DESCRIPTION

This message indicates there is a missing timing arc from an input or inout pin to an output pin.

For a combinational cell, the Library Compiler checks that

* An output port with a function statement has timing arcs to all functionally related inputs
* An output port with a three_state attribute has timing arcs to all three_state related inputs
* If all timing arcs are conditional, a default timing arc without any condition is required.

WHAT NEXT

Add the missing timing group between the two pins.

EXAMPLES

```
  cell(lbdb23) {
    area : 1;
    pin(A) {
      direction : input;
      capacitance : 1;
    }
    pin(B) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "(A B)’";
      timing() {
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "A";
      }
    }
```

```
  }
```

In this case, a timing arc is missing between the pin ’Z’ and ’B’. To fix the problem, add the following timing group:

```
      timing() {
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "B";
      }
```

EXAMPLE MESSAGE

Error: Line 12, There is a missing timing arc between pins ’A’ and ’Z’ in the ’lbdb23’ cell. (LBDB-23)

LBDB-24 (warning) The ’%s’ symbol is used but is not defined.

DESCRIPTION

This message indicates that in a symbol library, you assigned an undefined symbol name to a special symbol.

WHAT NEXT

Either define the symbol assigned to the special symbol, or correct the name if it is wrong.

EXAMPLES

```
  logic_1_symbol : "mylogic_1";
```

In this example, the symbol ’my_logic_1’ is not defined. To fix the problem, define the symbol:

```
  symbol(mylogic_1) {
    line(0,0,0,1.5);
    line(0,1.5,.5,2);
    line(0,1.5,-.5,2);
    pin(a,0,0,RIGHT);
  }
```

EXAMPLE MESSAGE

Warning: Line 38, The ’mylogic_1’ symbol is used but is not defined. (LBDB-24)

LBDB-27 (error) An invalid attribute is found.

DESCRIPTION

This error message occurs when a bus **function**, **three_state**, or **state_function** attribute value is not valid.

This message is also used to notify you when the **level_shifter_enable_pin** attribute is not specified for the input pin of a level shifter cell, or when the **isolation_cell_enable_pin** attribute is not specified for the input pin of an isolation cell.

WHAT NEXT

Correct the value of the attribute and rerun the command.

LBDB-28 (error) The ’%s’ attribute is supplied with %d arguments.
Only %d arguments are expected.

DESCRIPTION

This message indicates that a command or an attribute got the wrong number of arguments.

WHAT NEXT

Fix the arguments of the attribute.

EXAMPLES

```
define("lbdb28", "library", "string", "integer");
```

EXAMPLE MESSAGE

```
Error: Line 61, The ’define’ attribute is supplied with 4 arguments.
Only 3 arguments are expected. (LBDB-28)
```

LBDB-29 (warning) The ’%s’ attribute is already defined for %s groups.

It cannot be redefined.

DESCRIPTION

This message indicates that the user's defined attribute has been already defined. The Library Compiler ignores the second definition.

WHAT NEXT

Remove the redundant definition or rename the second definition.

EXAMPLES

```
  define("lbdb29", "pin", "string");
  define("lbdb29", "pin", "integer");
```

EXAMPLE MESSAGE

```
Warning: Line 62, The 'lbdb29' attribute is already defined for pin groups.
         It cannot be redefined. (LBDB-29)
```

LBDB-30 (warning) There is a sequential timing arc with the %s non-clock pin for a related_pin attribute.

DESCRIPTION

This message warns you if you specified any setup, hold, skew, removal, or edge-triggered timing arcs relative to a nonclock signal.

WHAT NEXT

Make sure the related_pin value is a clock pin, or modify the timing group.

EXAMPLES

```
  cell(lbdb30) {
    area : 9;
    pin(D) {
      direction : input;
      capacitance : 1;
      min_pulse_width_high : 1.0;
      min_pulse_width_low : 1.0;
      timing () {
timing_type : rising_edge;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
```

```
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "CD";
      }
    }
    pin(CP) {
      direction : input;
      capacitance : 1;
    }
    pin(CD) {
      direction : input;
      capacitance : 1;
    }
    ff("IQ","IQN") {
      next_state : "D";
      clocked_on : "CP";
      clear   : "CD'";
    }
  }
```

EXAMPLE MESSAGE

```
Warning: Line 1828, There is a sequential timing arc with the
'CP' non-clock pin for a related_pin attribute. (LBDB-30)
```

LBDB-31 (information) The %s group has been successfully %s in the library.

DESCRIPTION

This message informs you that a group has been successfully added or overwritten in a library using the **update_lib** command.

WHAT NEXT

No action is required.

EXAMPLE MESSAGE

```
Information: Line 1, The type group has been successfully added
in the library. (LBDB-31)
```

LBDB-32 (warning) The '%s' group has been defined multiple times in

the ’%s’ library. Using the last definition encountered.

DESCRIPTION

The library contains more than one definition of a group. The Library Compiler issues this error message, ignores the previous definitions, and takes into consideration the last definition encountered.

WHAT NEXT

Change the group name if it is wrong, or delete the second definition.

EXAMPLES

```
wire_load_selection(lbdb32) {
  wire_load_from_area(27,100,"10x10");
  wire_load_from_area(10,25,"05x05");
}
wire_load_selection(lbdb32) {
  wire_load_from_area(27,10,"10x10");
  wire_load_from_area(27,100,"10x10");
  wire_load_from_area(0,28,"05x05");
  wire_load_from_area(2,10,"15x10");
}
```

EXAMPLE MESSAGE

Warning: Line 50, The ’lbdb32’ group has been defined multiple times in the ’lib’ library. Using the last definition encountered. (LBDB-32)

LBDB-34 (error) There is a syntax error in the related_bus_pins attribute’s value.

DESCRIPTION

This message indicates there is a syntax error in the value of the related_bus_pins attribute. This might be caused by a typo.

WHAT NEXT

Check the "Library Compiler User Guide" for the correct syntax of the value, and fix the technology library source file.

EXAMPLES

```
          related_bus_pins : {ADDR} ;
```

In this case, the ’ADDR’ name is between parentheses. To fix the error, place the name between quotes.

EXAMPLE MESSAGE

```
Error: Line 164, There is a syntax error in the related_bus_pins attribute’s value.
 (LBDB-34)
```

LBDB-35 (warning) Missing a timing arc of timing_type ’three_state_disable’ between ’%s’ and ’%s’ pins in the ’%s’ cell.

DESCRIPTION

To describe the transition from 0->Z or 1->Z, use the timing arc with timing_type of **three_state_disable** for the pin with a three_state attribute.

WHAT NEXT

Add the missing timing group between the two pins.

EXAMPLES

```
  cell(BTS4)  {
        area : 3.0;
    pin(Z)  {
      direction : output;
      function : "A";
      three_state : "E";
      timing()  {
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "A";
      }
      timing()  {
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "E";
      }
    }
    pin(A)  {
      direction : input;
        capacitance : 1.0;
    }
```

```
    pin(E)  {
      direction : input;
        capacitance : 1.0;
    }
  }
```

EXAMPLE MESSAGE

```
Warning: Line 110, Missing a timing arc of timing_type 'three_state_disable'
between 'E' and 'Z' pins in the 'lbfb35' cell. (LBDB-35)
```

LBDB-36 (error) The '%s' specifies two variable names.

DESCRIPTION

This error indicates that you specified wrong variable names for a ff, ff_bank, latch, latch_bank, or a statetable group. Examples of wrong variable names are:

- The group name
- An empty string

WHAT NEXT

Check the "Library Compiler User Guide" for the correct syntax, and fix the variable names of the group in the technology library.

EXAMPLES

```
statetable("A", "statetable") {
ff("IQ", "") {
```

EXAMPLE MESSAGE

```
Error: Line 213, The 'statetable' specifies two variable names. (LBDB-36)
```

LBDB-37 (warning) The '%s' layer is defined multiple times: Deleting the old definition.

DESCRIPTION

The symbol library contains more than one definition of a layer. The Library Compiler issues this warning message, deletes the previous definition, and takes into consideration the last definition encountered.

WHAT NEXT

In the symbol library file, change the layer name if it is wrong, or delete the second definition.

EXAMPLES

```
library("ds.sdb") {

  layer(lbdb37_layer) {
    set_font ("1_25.font");
    visible : TRUE ;
    line_width : 1 ;
    red : 65000 ;
    green : 33000 ;
    blue : 0 ;
  }

  layer(lbdb37_layer) {   /* A duplicate layer. */
    set_font ("1_25.font");
    visible : TRUE ;
    line_width : 1 ;
    red : 65000 ;
    green : 33000 ;
    blue : 0 ;
  }
 }
```

EXAMPLE MESSAGE

```
Warning: Line 32, The 'lbdb37_layer' layer is defined multiple times:
        Deleting the old definition. (LBDB-37)
```

LBDB-39 (error) The '%s' symbol is defined multiple times.

DESCRIPTION

The symbol library contains more than one definition of a symbol. The Library Compiler issues this error message and deletes all the definitions.

WHAT NEXT

Change the symbol name if it is wrong, or delete the second definition.

EXAMPLES

```
  symbol(lbdb39_dot) {
    line( -.25,-.25,.25,-.25);
    line(.25,.25,.25,-.25);
```

```
    line(.25,.25,-.25,.25);
    line( -.25,.25,-.25,-.25);
    line( -.25,-.25,.25,.25);
    line(.25,-.25,-.25,.25);
  }

  symbol(lbdb39_dot) {
    line( -.25,-.25,.25,-.25);
    line(.25,.25,.25,-.25);
    line(.25,.25,-.25,.25);
    line( -.25,.25,-.25,-.25);
    line( -.25,-.25,.25,.25);
    line(.25,-.25,-.25,.25);
  }
```

EXAMPLE MESSAGE

```
Error: Line 58, The 'lbdb39_dot' symbol is defined multiple times. (LBDB-39)
```

LBDB-40 (error) In the '%s' symbol, the '%s' and '%s' pins both have the '%s' direction and the same Y location.

DESCRIPTION

The symbol library contains more than one pin with the same direction and the same Y location.

WHAT NEXT

Change the direction or the Y location of any of the pins.

EXAMPLES

```
  symbol("lbdb40") {
    set_minimum_boundary(0 , 0 , 8000, 12000);
    pin("P0", 1000, 10000, LEFT);
    pin("P1", 8000, 10000, LEFT);
    pin("P2", 8000, 10000, LEFT);
    line(0, 0, 0, 12000);
    line(0, 12000, 8000, 12000);
    line(8000, 12000, 8000, 0);
    line(8000, 0, 0, 0);
  }
```

EXAMPLE MESSAGE

```
Error: Line 15, In the 'lbdb40' symbol, the 'P2' and 'P0' pins both
have the 'LEFT' direction and the same Y location. (LBDB-40)
```

LBDB-41 (error) In the '%s' symbol, the '%s' and '%s' pins both have the '%s' direction and the same X location.

DESCRIPTION

The symbol library contains more than one pin with the same direction and the same X location.

WHAT NEXT

Change the direction or the X location of any of the pins.

EXAMPLES

```
symbol("lbdb41") {
  set_minimum_boundary(0 , 0 , 8000, 12000);
  pin("P0", 10000, 1000, DOWN);
  pin("P1", 10000, 8000, DOWN);
  pin("P2", 10000, 8000, DOWN);
  line(0, 0, 0, 12000);
  line(0, 12000, 8000, 12000);
  line(8000, 12000, 8000, 0);
  line(8000, 0, 0, 0);
}
```

EXAMPLE MESSAGE

Error: Line 15, In the 'lbdb41' symbol, the 'P2' and 'P0' pins both have the 'DOWN' direction and the same X location. (LBDB-41)

LBDB-42 (error) In the '%s' symbol, the '%s' pin '%s' and the '%s' pin '%s' are uncorrectly positioned.

DESCRIPTION

This error indicates that one of the problems is encountered:

- Both pin P1 and P2 have same direction and same X and Y locations.
- The pin P1 has a LEFT direction, the pin P2 has RIGHT direction, and P1 and P2 have the same Y location. However the X location of P2 is less or equal than to the X location of P1.
- The pin P1 has a UP direction, the pin P2 has DOWN direction, and P1 and P2 have the same X location. However the Y location of P2 is greater or equal than to the Y location of P1.

WHAT NEXT

Change the direction or the locations of any of the pins.

EXAMPLES

```
symbol("lbdb41") {
  set_minimum_boundary(0 , 0 , 8000, 12000);
  pin("P0", 10000, 1000, DOWN);
  pin("P1", 10000, 8000, DOWN);
  pin("P2", 10000, 8000, DOWN);
  line(0, 0, 0, 12000);
  line(0, 12000, 8000, 12000);
  line(8000, 12000, 8000, 0);
  line(8000, 0, 0, 0);
}
```

EXAMPLE MESSAGE

```
Error: Line 41, In the symbol 'lbdb42', the 'DOWN' pin 'P2' and
the 'DOWN' pin 'P1' are uncorrectly positioned. (LBDB-42)
```

LBDB-43 (error) The '%s' pin is defined multiple times in the '%s' symbol.

DESCRIPTION

The symbol library contains more than one definition of a pin in the specified symbol. The Library Compiler issues this error message and deletes all the definitions.

WHAT NEXT

Change the pin name if it is wrong, or delete the second definition.

EXAMPLES

```
symbol("lbdb43") {
  set_minimum_boundary(0 , 0 , 8000, 12000);
  pin("P0", 10000, 1000, DOWN);
  pin("P0", 10000, 1000, DOWN);
  line(0, 0, 0, 12000);
  line(0, 12000, 8000, 12000);
  line(8000, 12000, 8000, 0);
  line(8000, 0, 0, 0);
}
```

EXAMPLE MESSAGE

Error: Line 44, The ’P0’ pin is defined multiple times in the ’lbdb43’ symbol. (LBD B-43)

LBDB-46 (error) Found an invalid rotation.

DESCRIPTION

This message indicates that the specified string value for the pin’s rotation is not included in the list of accepted values. This error is often caused by a typo in the valid enumerated string value.

WHAT NEXT

Change the symbol library to correct the invalid rotation value. The valid values of the rotation are ANY_ROTATION, LEFT, RIGHT, UP, or DOWN.

LBDB-47 (error) The ’%s’ cell’s pin ’%s’ has a timing arc that has %d matched timing arcs on the scaled_cell(%s,%s).

DESCRIPTION

Each timing arc in the regular cell should have a matched timing arc on the same pin in the scaled_cell group. This message indicates that more than one such matching timing arc has been found in the library source.

WHAT NEXT

Find the duplicate timing group you do not need, and delete it.

EXAMPLES

```
library(lbdb47) {
    operating_conditions(WCCOM) {
process : 1.5 ;
        temperature : 70 ;
voltage : 4.75 ;
tree_type : "worst_case_tree" ;
    }

    cell(AND) {
      area : 1;
      pin(A B) {
```

```
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "A B";
timing() {
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A B";
}
      }
    }

    scaled_cell(AND,WCCOM) {
      area : 1;
      pin(A B) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "A B";
timing() {
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A";
}
timing() {
  intrinsic_rise : 0.3;
  intrinsic_fall : 0.3;
  rise_resistance : 0.3;
  fall_resistance : 0.3;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A ";
        }
      }
    }
  }
```

In this case, The timing arc between 'Z' and 'A' is defined once in the 'AND' cell and twice in the 'AND' scaled_cell. To fix the problem, remove one the timing arcs.

EXAMPLE MESSAGE

```
Error: Line 42, The 'AND' cell's pin 'Z' has a timing arc that has
```

```
       2 matched timing arcs on the scaled_cell(AND,WCCOM). (LBDB-47)
```

LBDB-48 (error) The ’%s’ pin has a %s group whose related_pin is the port itself.

DESCRIPTION

It is not possible to have a timing arc or a power table whose starting point and ending point are the same.

WHAT NEXT

Check the timing arc or the internal power group, and make the appropriate correction.

EXAMPLES

```
    cell(lbdb48) {
      area : 1.0;
      pin ( O ) {
direction : output;
function : "1";
timing() {
  timing_sense : non_unate;
  related_pin : "O";
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  intrinsic_rise : 5.0;
          intrinsic_fall : 0.0;
       }
     }
    }
```

EXAMPLE MESSAGE

```
Error: Line 43, The ’O’ pin has a timing group whose related_pin
       is the port itself. (LBDB-48)
```

LBDB-49 (error) No ’%s’ attribute has been specified for the library. This attribute is needed in %s libraries.

DESCRIPTION

This message indicates that you did not specify any of the following attributes in the physical library.

```
* distance_unit
* capacitance_unit
* resistance_unit
```

WHAT NEXT

Add the missing attribute to the library source file.

EXAMPLES

Add any of the following examples of attributes to the library:

```
    distance_unit : "1um";
```

EXAMPLE MESSAGE

```
Warning: No 'distance_unit' attribute has been specified for the
         library. This attribute is needed in technology libraries. (LBDB-49)
```

LBDB-50 (error) In the '%s' cell, the '%s' input pin has a 'function' attribute.

DESCRIPTION

This message indicates that a pin declared as an input, implicitly by omitting the direction or explicitly where the direction is set to input, has a function attribute. Only output and inout ports can have a function attribute.

WHAT NEXT

Either change the direction of the port or remove the function attribute.

EXAMPLES

```
    pin(Q) {
function : "1";
    }
```

In this case, the direction of 'Q' is set implicitly to 'input' and 'Q' has a function statement defined. To fix the problem, either set the direction explicitly to 'output' or 'inout', or delete the function attribute.

EXAMPLE MESSAGE

```
Error: Line 55, In the 'lbdb50' cell, the 'Q' input pin has a 'function' attribute.
 (LBDB-50)
```

LBDB-51 (warning) No ’%s’ attribute has been specified for the %s library. It is set to default value ’%s’.

DESCRIPTION

This message indicates that you did not specify any of the following attributes in the physical library. And a default value has been assigned.

* time_unit

WHAT NEXT

Make sure the default value is the desired value.

EXAMPLES

Add any of the following examples of attributes to the library:

```
distance_unit : 1um ;
```

EXAMPLE MESSAGE

```
Warning: No ’time_unit’ attribute has been specified for the
         library. It is set to default value ’1ns’. (LBDB-51)
```

LBDB-53 (error) The ’%s’ attribute, which expects values of %s type,
is being supplied a value of %s type.

DESCRIPTION

This message indicate that the attribute has been supplied with the wrong value. Library Compiler ignores the value.

WHAT NEXT

Check the "Library Compiler User Guide" for the correct type of attribute, and change the value accordingly.

EXAMPLES

```
    dont_touch : 1;
```

In this case, the 'dont_touch' attribute expects a boolean value such as true or false.

EXAMPLE MESSAGE

```
Error: Line 53, The 'dont_touch' attribute, which expects values of boolean  type,
       is being supplied a value of integer type. (LBDB-53)
```

LBDB-54 (error) The define attribute has an invalid '%s' type. The valid types are 'string', 'integer', 'float', and 'boolean'.

DESCRIPTION

This message indicates that an invalid type is specified for the define attribute. Library Compiler ignores the invalid type.

WHAT NEXT

Change the type to string, integer, float, or boolean in the library.

EXAMPLES

```
library(lbdb54) {
  define( "glorp","library","my_type" );
}
```

EXAMPLE MESSAGE

```
Error: Line 2, The define attribute has an invalid 'my_type' type.
       The valid types are 'string', 'integer', 'float', and 'boolean'. (LBDB-54)
```

LBDB-55 (error) The '%s' technology license is not installed.

DESCRIPTION

This message indicates that the specified technology license is missing during a read_lib command. Given the technology, the missing license feature is matched as follows:

* CMOS technology needs a Design-Compiler feature.
* FPGA technology needs an FPGA-Compiler feature.

If your site is without a valid technology license, the library is read in, and all functional information is removed. All cells are black boxes, and optimization with this library is disabled.

WHAT NEXT

Make sure that you have a license and that the license is properly installed before next trying to read the specified technology library.

EXAMPLE MESSAGE

Error: Line 2, The 'cmos' technology license is not installed. (LBDB-55)

LBDB-57 (error) The 'generic' technology can only be read by Synopsys.

DESCRIPTION

The generic technology library supplies simple combinational and sequential cells that are useful for technology-independent component instantiation. This message indicates that you specified 'generic' as the technology type in the technology library source file. This technology type is reserved for Synopsys generic technology library. Only Synopsys is allowed to compile a generic technology library.

WHAT NEXT

Do not use 'generic' as the technology type in your technology library source. Choose the correct technology type from current supporting types, for example, CMOS or FPGA.

LBDB-58 (warning) The '%s' pin is a multicell_pad_pin, but it has no connection_class information.

DESCRIPTION

This message indicates that you have a pin in a multicell pad with the multicell_pad_pin attribute defined but the connection_class attribute is missing.

If your library uses multicell pads, Design Compiler needs to know which pins on the various cells to connect to implement the pad properly. Two attributes give this information:

* The multicell_pad_pin attribute identifies the pins to
  connect to create a working multicell pad. Use this
  attribute to flag all the pins to connect on a pad or an
  auxiliary pad cell.
* The connection_class attribute indicates the pins
  to be connected to pins on other cells.

WHAT NEXT

Add the connection_class attribute to the specified pin.

EXAMPLES

```
    cell (lbdb58) {
      pad_cell : true;
      area : 0.0;
      pin (A) {
direction : input;
capacitance : 1.0;
fanout_load : 1.0;
      }
      pin (GZ) {
direction : input;
capacitance : 1.0;
fanout_load : 1.0;
      }
      pin(Y) {
direction : output;
capacitance : 1.0;
driver_type : open_drain;
is_pad : true;
multicell_pad_pin : true;
slew_control : low;
drive_current : 1.0;
output_voltage  : STD_CMOS;/* defined in the library */
function : "A";
three_state : "GZ";
timing () {
  intrinsic_rise   : 0.0;
  rise_resistance  : 0.0;
  intrinsic_fall   : 1.0;
  fall_resistance  : 0.1;
  related_pin      : "A";
}
timing () {
  intrinsic_rise   : 0.0;
  rise_resistance  : 0.0;
  intrinsic_fall   : 1.0;
  fall_resistance  : 0.1;
  related_pin      : "GZ";
}
max_transition : 0.1;
      }
    }
```

In this case, the 'Y' pin has the multicell_pad_pin attribute defined. To fix the problem, add the connection_class attribute.

EXAMPLE MESSAGE

Warning: Line 41, The 'Y' pin is a multicell_pad_pin, but

has no connection_class information. (LBDB-58)

LBDB-59 (error) The '%s' found in the %s attribute is invalid.

DESCRIPTION

This message indicates that the specified pin, bus, or bundle name defined in a related_inputs or related_outputs attribute does not exist in the library.

WHAT NEXT

Add the port definition if it is missing in the library, or fix the name if it is a typographical error.

EXAMPLES

```
/* Specify non-existence output pin */
internal_power(lbdb59) {
  values("0.1, 1.2, 0.3, 0.4");
  related_outputs : "X";
}
```

EXAMPLE MESSAGE

Error: Line 46, The 'X' found in the related_inputs or related_outputs attribute is invalid. (LBDB-59)

LBDB-60 (warning) The wire_load or wire_load_table '%s' group has no '%s'. Using the default value of (%d, %3.1f).

DESCRIPTION

This message indicates that the specified attribute is not specified in the wire_load or wire_load_table group. The default value of the attribute is used. The missing attribute can be

* A fanout_length
* A fanout_capacitance
* A fanout_resistance
* A fanout_area

WHAT NEXT

If you do not want to apply the default to the attribute indicated in the warning message, specify the attribute in the indicated group.

EXAMPLES

```
  wire_load_table("lbdb60") {
      fanout_length(1, 0.2) ;
      fanout_resistance(1, 0.17) ;
      fanout_area(1, 0.2) ;
    }
```

In this case, the fanout_capacitance is missing in the wire_load_table. If you do not want the default value, add the following attribute:

```
      fanout_capacitance(1, 0.15);
```

EXAMPLE MESSAGE

Warning: Line 10, The wire_load or wire_load_table ’lbdb60’ group has no ’fanout_capacitance’. Using the default value of (1, 0.0). (LBDB-60)

LBDB-61 (warning) Template ’%s’ is defined in old library syntax.

DESCRIPTION

This message indicates that a special symbol in the symbol library file is written using an old library syntax.

WHAT NEXT

Check the "Library Compiler User Guide" for the correct syntax of symbols.

LBDB-62 (error) The ’%s’ symbol is a duplicate ’%s’ template.

DESCRIPTION

This message indicates that the specified symbol is a duplicate symbol in the symbol library file. Library Compiler ignores the duplicate symbol.

WHAT NEXT

Remove the duplicate symbol from the symbol library, or change the name if it is a typo.

LBDB-66 (error) The '%s' attribute cannot be supplied a nonpositive value (%f).

DESCRIPTION

This message indicates that the specified attribute cannot have a nonpositive value.

WHAT NEXT

Change the value of the attribute to positive in the technology library file.

EXAMPLES

```
    capacitive_load_unit( -1,pf );
```

EXAMPLE MESSAGE

```
Error: Line 18, The 'capacitive_load_unit' attribute cannot be supplied a
       nonpositive value (-1.000000). (LBDB-66)
```

LBDB-69 (error) Missing a %s name.

DESCRIPTION

This message indicates that a group name is missing in the technology or symbol library file. The Library Compiler ignores the library.

WHAT NEXT

Add the group name to the technology or symbol library file.

EXAMPLES

```
  cell() {
    area : 9;
  }
```

EXAMPLE MESSAGE

```
Error: Line 63, Missing a cell name. (LBDB-69)
```

LBDB-70 (error) The '%s' group name is defined multiple times for the '%s' parent.

DESCRIPTION

The technology library contains more than one definition of a define_group attribute with the same name. The Library Compiler issues this error message and deletes all the definitions.

WHAT NEXT

Change the group name if it is wrong, or delete the second definition.

EXAMPLES

```
    define_group(lbdb70, cell);
    define_group(lbdb70, cell);
```

EXAMPLE MESSAGE

```
Error: Line 58, The 'lbdb70' group name is defined multiple times for the 'cell' pa
rent. (LBDB-70)
```

LBDB-72 (error) Undefined module_pin '%s' referenced in pin_association '%s' in %s '%s'.

DESCRIPTION

The name given to a pin_association group within a binding group or a state group names a pin that must be defined by a pin group within the module. This error arises when the name given to the pin_association group does not have a corresponding pin group on the module. For example, in the following synthetic library, the pin_association group named 'MY_B' attempts to bind the operator pin 'B' to the module pin 'MY_B'. However, the pin 'MY_B' is not defined for the module, which causes an error to occur.

```
library (example.sldb) { module (my_module) { design_library : "MYLIB";
parameter(width) { hdl_parameter : TRUE; } pin (MY_A) { direction : input; bit_width
```

```
: "width"; } pin (MY_Z) { direction : output; bit_width : "width"; } binding (b1) {
bound_operator : "ADD_UNS_OP"; pin_association(MY_A) { oper_pin : A ; }

/* The following line creates an error: */ pin_association(MY_B) { oper_pin : B ; }

pin_association(MY_Z) { oper_pin : Z ; } } } }
```

In this case you can fix the error by adding a pin group to the module:

```
pin (MY_B) { direction : input; bit_width : "width"; }
```

WHAT NEXT

Remove the pin_association group that refers to the nonexistent module pin. Alternately, you can add a module pin group with the name of the referenced pin in the pin_association group.

LBDB-73 (error) The '%s' cell has more than one sequential function (seq, latch, or ff) declaration.

DESCRIPTION

This message indicates there is more than one declaration of a sequential function group.

WHAT NEXT

Leave only one sequential function group declaration; remove the rest of the declarations.

LBDB-74 (error) The %s value, '%s', is either not defined or it is defined after this line.

DESCRIPTION

This error message occurs when the **default_operating_conditions** or **default_wire_load** attribute refers to an undefined the operating_conditions or wire_load group name in the library.

This message can also report the **related_power_rail** attribute references and the undefined power_rail values in the power_supply group.

The following example shows the 05x05 wire_load group defined after the **default_wire_load** attribute and the resulting error message:

```
    default_wire_load : 05x05;
    wire_load("05x05") {
      resistance : 0 ;
      capacitance : 1 ;
      area : 0 ;
      slope : 0.186 ;
      fanout_length(1,0.39) ;
    }
```

```
Error: Line 57, The default_wire_load value, '05x05',
has not been defined or it is defined after this line. (LBDB-74)
```

WHAT NEXT

Check your library to determine if you have defined the group name. If the group name exists in the library, make sure it is defined before it is used.

LBDB-75 (warning) There is an extra timing arc between '%s' and '%s' pins in the '%s' cell.

DESCRIPTION

Timing arcs are allowed for pins that are related to each other. To be related to each other, the input pin has to be in the **function** or **three_state** attribute of the output/input pin. This message is issued if the timing arc identified between pins does not fall into the categories described previously. In addition, the VHDL generator fails and the timing verifier times through this timing arc, which you probably do not intend.

WHAT NEXT

Check your library to see whether you have generated the timing group by mistake, whether the related_pin field is wrong or the function attribute value is not recognized.

EXAMPLES

```
    pin(Z) {
      direction : output;
      function : "B";
      timing() {
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "A";
      }
```

```
  }
```

In this case, you defined a timing arc between the ’A’ and ’Z pins, even though the ’A’ pin is not functionally related to the ’Z’ pin. Either remove the timing arc or change the function statement of ’Z’ to include ’A’.

EXAMPLE MESSAGE

```
Warning: Line 73, There is an extra timing arc between ’A’ and
        ’Z’ pins in the ’lbd75’ cell. (LBDB-75)
```

LBDB-76 (error) The ’%s’ %s cannot be specified here.

DESCRIPTION

This message indicates that you specified an attribute outside its context. When processing the current context, Library Compiler flags invalid attributes.

It can also be used to indicate that you have specified an attribute/groups which conflicts with the other attributes/groups of the object. For example, if you specify ’io_type’ attribute on a cell in the FPGA library which is based on fpga_isd information, the LBDB-76 will be issues and the ’io_type" attribute should be removed.

WHAT NEXT

Change the technology library source file to either delete the specified attribute or move the attribute to its correct context.

EXAMPLES

```
pin(D) {
  direction : input;
  capacitance : 1.0;
  current_unit : "1mA";
}
```

In this case, the ’current_unit’ attribute is defined at the pin level. To fix the problem, move the attribute to the library context.

EXAMPLE MESSAGE

```
Error: Line 69, The ’current_unit’ attribute cannot be specified here. (LBDB-76)
```

LBDB-79 (error) The ’ripped_pin’ name is not defined.

DESCRIPTION

This message indicates that you specified an undefined pin name for the ripped_pin attribute in a symbol library file.

WHAT NEXT

Change the symbol library to either define the pin name before you use it in the ripped_pin attribute or fix the pin name if it is a typo.

EXAMPLES

```
  symbol("lbdb79") {
 ripped_pin : "bus_pin" ;
 ripped_bits_property : "EDIF_property" ;
 line(0 , 50, 50, 0);
 line(50, 0, 0, -50);
 line(-50, 0 , 100, 0);
 pin("wire_pin", 100 , 0 , ANY_ROTATION);
  }
```

In this case, the ’bus_pin’ pin is not defined.

EXAMPLE MESSAGE

Error: Line 69, The ’ripped_pin’ name is not defined. (LBDB-79)

LBDB-80 (error) The ’%s’ port name is either undefined or its group definition is invalid.

DESCRIPTION

This message indicates that the specified port name is either not defined in the library source file or Library Compiler did not read the port group definition successfully. This might often be caused by a problem in the pin bus or a bundle group definition.

WHAT NEXT

Change the library source file to define the port.

EXAMPLES

```
  cell (lbdb80) {
```

```
    area : 3.0;
    bus (D) {
      bus_type : BUS4;
      direction : input;
      capacitance : 1.0;
    }
    pin (CK) {
      direction : input;
      capacitance : 1.0;
    }
    ff_bank (IQ,IQN,4) {
      next_state : "D" ;
      clocked_on : "CK";
    }
    pin (Q) {
      direction : output ;
      function : "D[0] CK" ;
    }
  }
```

In this case, the 'BUS4' type is not defined in the library. Thus, the 'D' bus is not recognized, and the next_state value is considered to be not defined. Fix the problem by adding the 'BUS4' type group definition.

EXAMPLE MESSAGE

```
Error: Line 186, The 'D' port name is either undefined or
its group definition is invalid. (LBDB-80)
```

LBDB-81 (error) The base type in the type group is invalid.

DESCRIPTION

This message indicates that the specified base_type name in the type group is invalid. This might be caused by a typo in the name. Library Compiler only supports the **array** base_type.

WHAT NEXT

Check the "Library Compiler User Guide" and fix the name of the base_type.

EXAMPLES

```
  type(bus2) {
    base_type : afrray;
    data_type : bit;
    bit_width : 2;
    bit_from : 0;
    bit_to : 1;
    downto : false;
```

```
  }
```

In this case, there is a typo in the base_type value. change afrray to **array**.

EXAMPLE MESSAGE

Error: Line 30, The base type in the type group is invalid. (LBDB-81)

LBDB-82 (error) The data type in the type group is invalid.

DESCRIPTION

This message indicates that the specified data_type name in the type group is invalid. This might be caused by a typo in the name. Library Compiler only supports the **bit** data_type.

WHAT NEXT

Check the "Library Compiler User Guide" and fix the name of the data_type.

WHAT NEXT

EXAMPLES

```
type(bus2) {
  base_type : array;
  data_type : int;/* wrong */
  bit_width : 2;
  bit_from : 0;
  bit_to : 1;
  downto : false;
}
```

In this case, the data_type value is invalid. change int to **bit**.

EXAMPLE MESSAGE

Error: Line 30, The data type in the type group is invalid. (LBDB-82)

LBDB-83 (warning) The width value in the type group is invalid.

It is corrected.

DESCRIPTION

This message indicates that the specified **bit_width** value in the type group is invalid. This might be caused by a typo in the value. The Library Compiler ignores the invalid value and computes the real value from the bit_from and bit_to fields.

WHAT NEXT

Change the library file, and fix the value of the bit_width.

EXAMPLES

```
type(bus2) {
  base_type : array;
  data_type : bit;
  bit_width : 3;
  bit_from : 0;
  bit_to : 1;
  downto : false;
}
```

In this case, the bit_width value is 3. To fix the problem, change it to 2 (bit_to - bit_from + 1).

EXAMPLE MESSAGE

```
Error: Line 30, The width value in the type group is invalid.
It is corrected. (LBDB-82)
```

LBDB-86 (warning) The downto value in the type group is invalid.

It is corrected.

DESCRIPTION

This message indicates that the specified **downto** value in the type group is invalid. This might be caused by a typo in the value. The Library Compiler ignores the invalid value and computes the real value from the bit_from and bit_to fields.

WHAT NEXT

Change the library file, and fix the value of the downto field.

EXAMPLES

```
type(bus2) {
  base_type : array;
  data_type : bit;
  bit_width : 2;
  bit_from : 0;
  bit_to : 1;
  downto : ffalse;
}
```

In this case, the downto value has a typo, ffalse. To fix the problem, change ffalse to false. The Library Compiler corrects the value by setting to false bit_from value is less than the bit_to value. Otherwise, it is set to true.

EXAMPLE MESSAGE

```
Warning: Line 35, The downto value in the type group is invalid.
It is corrected. (LBDB-86)
```

LBDB-87 (error) The type group is missing its ’data_type’ field.

DESCRIPTION

This message indicates that the data_type field is missing in the type group.

WHAT NEXT

Change the library file, and add the data_type field to the type group.

EXAMPLES

```
type(bus2) {
  base_type : array;
  bit_width : 2;
  bit_from : 0;
  bit_to : 1;
  downto : false;
}
```

To fix the problem, add the data_type statement to the type group.

```
  data_type : bit;
```

EXAMPLE MESSAGE

```
Error: Line 28, The type group is missing its ’data_type’ field. (LBDB-87)
```

LBDB-88 (error) The type group is missing its ’base_type’ field.

DESCRIPTION

This message indicates that the base_type field is missing in the type group.

WHAT NEXT

Change the library file, and add the base_type field to the type group.

EXAMPLES

```
  type(bus2) {
    data_type : bit;
    bit_width : 2;
    bit_from : 0;
    bit_to : 1;
    downto : false;
  }
```

To fix the problem, add the base_type statement to the type group.

```
    base_type : array;
```

EXAMPLE MESSAGE

Error: Line 28, The type group is missing its ’base_type’ field. (LBDB-88)

LBDB-89 (error) The ’%s’ library attribute must be defined to specify a %s value.

DESCRIPTION

This message indicates that an attribute needed by another group is missing in the library. Examples of attributes are

* The input_voltage value needs the voltage_unit attribute
          defined.
* The slew_control value needs the time_unit attribute
          defined.
* The drive_current value needs the current_unit attribute
          defined.

WHAT NEXT

Add the missing attribute to the library.

EXAMPLES

```
  input_voltage(CMOS) {
    vil         : 0.8 ;
    vih         : 2.0 ;
    vimin       : -0.3 ;
    vimax       : VDD + 0.3 ;
   }
    cell(lbdb89) {
      area : 0.0;
      dont_touch : false;
      dont_use   : false;
      pad_cell : true;
      pin(PAD ) {
is_pad : true;
input_voltage : CMOS;
direction   : input;
capacitance : 3.0;
fanout_load : 0.0;
      }
      pin(Y ) {
direction   : output;
function    : "PAD";
max_fanout  : 16.0;
timing() {
  intrinsic_fall  : 4.0;
  intrinsic_rise  : 4.0;
  fall_resistance : 0.0;
  rise_resistance : 0.0;
  related_pin  :"PAD ";
}
      }
    }
```

In this case, add the voltage_unit to the library as follows:

```
voltage_unit : "1V";
```

EXAMPLE MESSAGE

```
Error: Line 14, The 'voltage_unit' library attribute must be defined
       to specify a input_voltage value. (LBDB-89)
```

LBDB-90 (error) The type group is defined multiple times.

DESCRIPTION

This message indicates that the type group is defined multiple times in the technology library. This might be caused by a typo.

WHAT NEXT

Change the library file by either removing the multiple definitions but one or renaming the type groups.

EXAMPLES

```
type(bus2) {
  base_type : array;
  data_type : bit;
  bit_width : 2;
  bit_from : 0;
  bit_to : 1;
  downto : false;
}
type(bus2) {
  base_type : array;
  data_type : bit;
  bit_width : 2;
  bit_from : 1;
  bit_to : 0;
  downto : true;
}
```

In this case, rename the second type group to bus2_down.

EXAMPLE MESSAGE

Error: Line 36, The type group is defined multiple times. (LBDB-90)

LBDB-91 (warning) The bus naming style format is invalid. Using the default format.

DESCRIPTION

This message indicates that you specified an invalid bus_naming_style format. The value must include %s and %d. Library Compiler ignores the invalid value and uses the default style "%s[%d]".

WHAT NEXT

Check the "Library Compiler User Guide" for the correct format of the bus_naming_style and fix the value.

EXAMPLES

```
bus_naming_style : "%s$%s";
```

EXAMPLE MESSAGE

```
Warning: Line 28, The bus naming style format is invalid.
Using the default format. (LBDB-91)
```

LBDB-92 (error) The bus subscript is out of bounds.

DESCRIPTION

This message indicates that you specified a bus element whose index value falls outside the declared index range of the bus type.

The accessed bus element with an index outside the bus bounds is specified in function, three_state, ff, or latch statements.

WHAT NEXT

Either change the bounds of the bus definition so that all subelements that are accessed fall within the range, or correct any bus indexing errors in the source library.

```
  type(bus2) {
    base_type : array;
    data_type : bit;
    bit_width : 2;
    bit_from : 0;
    bit_to : 1;
    downto : false;
  }
  cell (lbdb92) {
    area : 31.0;
    bus (D) {
      bus_type : bus2;
      direction : input ;
      capacitance : 1.0 ;
    }
    pin (CK) {
      direction : input ;
      capacitance : 1.0 ;
    }
    ff_bank (IQ,IQN,2) {
      next_state : "D[3]" ;
      clocked_on : "CK" ;
    }
    bus (SO) {
      bus_type : bus2;
      direction : output ;
      function : "IQ" ;
    }
  }
```

In this case, the ’D[3]’ value assigned to next_state falls outside the bus2 range.

EXAMPLE MESSAGE

Error: Line 186, The bus subscript is out of bounds. (LBDB-92)

LBDB-93 (error) The bus type is invalid.

DESCRIPTION

This message indicates that you specified a bus name whose bus_type is invalid. This might be caused by an invalid base_type in the type group or a typo in the name. Library Compiler only supports the **array** base_type for bus groups.

WHAT NEXT

Check the "Library Compiler User Guide" and fix the name of the base_type in the type group, or change the bus type name.

EXAMPLES

```
type(bus2) {
  base_type : list;
  data_type : bit;
  bit_width : 2;
  bit_from : 0;
  bit_to : 1;
  downto : false;
}
cell (lbdb93) {
  area : 31.0;
  bus (D) {
    bus_type : bus2;
    direction : input ;
    capacitance : 1.0 ;
  }
  pin (CK) {
    direction : input ;
    capacitance : 1.0 ;
  }
}
```

In this case, the ’list’ base_type of the ’bus2’ type is invalid. Fix the problem by changing the ’list’ to ’array’.

EXAMPLE MESSAGE

Error: Line 177, The bus type is invalid. (LBDB-93)

LBDB-94 (warning) The ':' character is used in this bus naming style;
this makes it impossible to specify ranges of buses using ':'.

DESCRIPTION

This message indicates that you specified a ':' in the string of the bus_naming_style. Library Compiler gets confused because the ':' is used to specify ranges of buses.

WHAT NEXT

Change the value of the bus_naming_style attribute in the technology library.

EXAMPLES

```
bus_naming_style : "%s:%d";
```

EXAMPLE MESSAGE

```
Warning: Line 28, The ':' character is used in this bus naming style;
         this makes it impossible to specify ranges of buses using ':'. (LBDB-94)
```

LBDB-95 (error) Buses have incompatible widths.

DESCRIPTION

This message indicates that you specified a function or a three_state attribute of a group of buses with a different width.

WHAT NEXT

Change the library source file to make sure that all buses have the same width.

EXAMPLES

```
cell (lbdb95) {
  area : 3.0;
  bus (D) {
    bus_type : bus2;
    direction : input;
    capacitance : 1.0;
  }
  pin (CK) {
    direction : input;
```

```
      capacitance : 1.0;
    }
    ff_bank (IQ,IQN,4) {
      next_state : "D";
      clocked_on : "CK";
    }
    pin (SO) {
      direction : output;
      function : "D[0] CK";
    }
  }
```

In this case, the number of bits in the ff_bank, which is 4, is different from the width of the 'D' bus, which is 2. Make sure that both values are the same.

EXAMPLE MESSAGE

```
Error: Line 186, Buses have incompatible widths. (LBDB-95)
```

LBDB-96 (error) The bus type name is missing.

DESCRIPTION

This message indicates that you specified a bus with an invalid a bus_type.

WHAT NEXT

Check the library source file, and correct the bus_type to the bus in the library.

LBDB-97 (error) The bus type of a subelement is missing.

DESCRIPTION

This message indicates that you specified a subelement whose parent is missing a bus type.

WHAT NEXT

Change the library, and fix the bus type.

LBDB-98 (error) The type group name is not defined.

DESCRIPTION

This message indicates that you specified a bus group with an undefined bus_type name in the technology library. This might be caused by a typo.

WHAT NEXT

Change the library file by adding the named type group.

EXAMPLES

```
  cell (lbdb98) {
    area : 3.0;
    bus (D) {
      bus_type : bus2;
      direction : input;
      capacitance : 1.0;
    }
   }
```

In this case, the 'bus2' is not defined in the library. To fix the problem, add the following type group:

```
  type(bus2) {
    base_type : array;
    data_type : bit;
    bit_width : 2;
    bit_from : 0;
    bit_to : 1;
    downto : false;
  }
```

EXAMPLE MESSAGE

Error: Line 177, The type group name is not defined. (LBDB-98)

LBDB-99 (error) The pin direction is inconsistent with the bus or the bundle parent direction.

DESCRIPTION

This message indicates that you specified a member of a bus or a bundle whose direction is different from its parent's direction.

WHAT NEXT

Change the library to fix the direction of the element, the bus, or the bundle.

EXAMPLES

```
    bundle(nets) {
      members(n0, n1, n2, n3);
      direction : inout;
      pin (n0) {
direction : output;
      }
    }
```

In this case, the 'nets' direction is 'inout', but the 'n0' direction is 'output'.

EXAMPLE MESSAGE

```
Error: Line 199, The pin direction is inconsistent with the bus or
the bundle parent direction. (LBDB-99)
```

LBDB-101 (error) The piece number in piecewise linear mode is negative.

DESCRIPTION

This message indicates that you specified a negative piece number in either delay intercept attributes or pin resistance attributes in CMOS piecewise linear delay model library.

WHAT NEXT

Modify the piece number to match the number of ranges in the piece_define attribute.

EXAMPLES

```
  piece_define("0 8 15");
...
  rise_delay_intercept(-11, "2.2");
```

In this case, the -11 piece number is invalid. To fix the problem, make the piece number 0, 1, or 2 as defined by the piece_define attribute.

EXAMPLE MESSAGE

```
Error: Line 172, The piece number in piecewise linear mode is negative. (LBDB-101)
```

LBDB-102 (warning) The '%s' piece is multiply defined. Using the first one encountered.

DESCRIPTION

This message indicates that you specified either delay intercept attributes or pin resistance attributes for the same piece number multiple times in a CMOS piecewise linear delay model library. Library Compiler ignores the later definitions.

WHAT NEXT

Modify the piece number if it is a typo, or remove the second definition.

EXAMPLES

```
rise_delay_intercept(1, "2.2");
rise_delay_intercept(1, "2.2");
```

EXAMPLE MESSAGE

```
Warning: Line 173, The 'rise_delay_intercept(1)' piece is multiply
defined. Using the first one encountered. (LBDB-102)
```

LBDB-103 (warning) The piece number is greater than the number defined with piece_define.

DESCRIPTION

This message indicates that in a CMOS piecewise-linear delay model library you specified a piece number in either delay intercept attributes or pin resistance attributes greater than the number defined in the piece_define attribute.

WHAT NEXT

Modify the piece number to match the number of ranges in the piece_define attribute.

EXAMPLES

```
  piece_define("0 8 15");
...
  rise_delay_intercept(3, "2.2");
```

In this case, the 3 piece number is invalid. To fix the problem, make the piece

number 0, 1, or 2 as defined by the piece_define attribute.

EXAMPLE MESSAGE

```
Warning: Line 174, The piece number is greater than the number
defined with piece_define. (LBDB-103)
```

LBDB-104 (warning) The piecewise linear model is multiply defined. Using the first one encountered.

DESCRIPTION

This message indicates that you specified the **piece_define** attribute multiple times in a CMOS piecewise linear delay model library. Library Compiler ignores the later definitions.

WHAT NEXT

Remove the second definition of the attribute.

EXAMPLES

```
piece_define("0 8 15");
piece_define("0 8 15 25");
```

EXAMPLE MESSAGE

```
Warning: Line 13, The piecewise linear model is multiply defined.
Using the first one encountered. (LBDB-104)
```

LBDB-105 (warning) The timing arc has a negative %s specified. Using the default value.

DESCRIPTION

This message indicates that you specified a negative drive resistance value of pin resistance attributes in a CMOS piecewise linear delay model library. Library Compiler assigns the **default_rise_pin_resistance** or the **default_fall_pin_resistance** value to the timing arc or the value 0.0 if no default value exists.

WHAT NEXT

Make the drive resistance value positive in the pin resistance attribute.

WHAT NEXT

EXAMPLES

```
rise_pin_resistance(0, "-11.1");
```

EXAMPLE MESSAGE

```
Warning: Line 183, The timing arc has a negative rise_pin_resistance(0)
specified. Using the default value. (LBDB-105)
```

LBDB-107 (warning) The %s '%s' is defined multiple times in the library. Using the last one encountered.

DESCRIPTION

This message indicates that the same name has been used for more than one object (for example, cells in a library or pins in a cell). Each object must have a unique name within its scope. In the case of a name conflict, Library Compiler ignores all except the last name encountered during the compilation. The compiled database contains the last object only.

WHAT NEXT

Update the library to give each object a unique name within its scope. Quite often, a typo is responsible for the name conflict.

EXAMPLES

```
      statetable ( "D GN", "Q QB") {
table : "L/H L : - - : L/H H/L,\

        -   H : - - : N   N";
      }

      statetable ( "D GN", "Q QB") {
table : "L/H L : - - : L/H H/L,\

        -   H : - - : N   N";
      }
```

EXAMPLE MESSAGE

```
Warning: Line 987, The group 'statetable' is defined multiple times
        in the library. Using the last one encountered. (LBDB-107)
```

LBDB-110 (warning) In the piecewise linear model, the first piece must have 0 length.

DESCRIPTION

This message indicates that you specified the first piece range, in the piece_define attribute, not starting from zero. Library Compiler ignores the value, and resets it to zero.

WHAT NEXT

Change the first piece range to zero.

EXAMPLES

```
piece_define("1 8 15");
```

EXAMPLE MESSAGE

```
Warning: Line 12, In the piecewise linear model, the first piece must
have 0 length. (LBDB-110)
```

LBDB-111 (warning) In the piecewise linear model, a piece length smaller than that of the previous piece has been found.

DESCRIPTION

This message indicates that in the piece_define attribute you specified a piece length smaller than the previous one. The Library Compiler ignores the value and resets it to the previous value.

WHAT NEXT

Change the piece ranges to be in ascending order.

EXAMPLES

```
piece_define("0 18 15");
```

EXAMPLE MESSAGE

```
Warning: Line 12, In the piecewise linear model, a piece length
smaller than that of the previous piece has been found. (LBDB-111)
```

LBDB-112 (error) The timing arc has only one segment of '%s'. It must have at least two if piece_define has more than one piece.

DESCRIPTION

This message indicates that in a CMOS piecewise linear delay model library you specified only one segment in either delay intercept attributes or pin resistance attributes. However, the **piece_define** defines more than one piece.

WHAT NEXT

Modify the piece number to match the number of ranges in the piece_define attribute.

EXAMPLES

```
piece_define("0 8 15");
...
rise_delay_intercept(0, "2.2");
```

In this case, only one rise_delay_intercept attribute is defined. To fix the problem, add two more rise_delay_intercept for piece 1 and 2.

```
rise_delay_intercept(1, "3.3");
rise_delay_intercept(2, "4.4");
```

WHAT NEXT

EXAMPLE MESSAGE

```
Error: Line 169, The timing arc has only one segment of
       'rise_delay_intercept'. It must have at least two if
piece_define has more than one piece. (LBDB-112)
```

LBDB-117 (error) A list does not belong here.

DESCRIPTION

This message indicates that you specified a list to an attribute whose type is not a list.

WHAT NEXT

Correctthe value of the specified attribute.

EXAMPLES

```
library(lbdb117) {
  cell(c) {
    area : 1.0;
    pin( a ) {
      direction : input;
      capacitance : 1.0;
    }
    pin( b ) {
      direction : output;
      timing() {
        intrinsic_rise : 0.48;
        intrinsic_fall : 0.77;
        rise_resistance : 0.1443;
        fall_resistance : {0.0523,0.0523};
        slope_rise : 0.0;
        slope_fall : 0.0;
        related_pin : "a";
      }
    }
  }
}
```

In this case, the ’fall_resistance’ attribute has a value of type list. Fix the problem by assigning a single value to the attribute.

EXAMPLE MESSAGE

Error: Line 14, A list does not belong here. (LBDB-117)

LBDB-119 (error) The ’%s’ pin on the %s could not be found on

the %s. There must be a one-to-one match.

DESCRIPTION

Each pin in the regular cell needs a matched pin in the scaled_cell group. This message indicates that a pin could not be matched in the library source.

WHAT NEXT

Add the missing pin in the regular cell, or remove the extra pin in the scaled_cell.

EXAMPLES

```
library(lbdb119) {
    operating_conditions(WCCOM) {
process : 1.5 ;
        temperature : 70 ;
voltage : 4.75 ;
tree_type : "worst_case_tree" ;
    }
    cell(AND) {
      area : 1;
      pin(A B) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "A B";
timing() {
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A B";
}
      }
    }

    scaled_cell(AND,WCCOM) {
      area : 1;
      pin(A B C) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "A B";
timing() {
  intrinsic_rise : 0.1;
```

```
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A B";
}
      }
    }
  }
```

In this case, the ’C’ pin exists in the scaled_cell but not in the parent cell.

EXAMPLE MESSAGE

```
Error: Line 100, The ’C’ pin on the scaled_cell could not be found on
       the parent cell. There must be a one-to-one match. (LBDB-119)
```

LBDB-120 (warning) Layers are ignored inside symbols.

DESCRIPTION

For a symbol library, Library Compiler ignores layer information within a symbol.

WHAT NEXT

Remove the layer information from the symbol.

EXAMPLES

```
  symbol(lbdb-120) {
    line( - flag_width / 2, - flag_height / 2, \

 - flag_width / 2, flag_height / 2) ;
    line( - flag_width / 2, flag_height / 2, \

 flag_width / 2, flag_height / 2) ;
    line( flag_width / 2, flag_height / 2, \

 flag_width / 2, - flag_height / 2) ;
    line( flag_width / 2, - flag_height / 2, \

 - flag_width / 2, - flag_height / 2) ;
    text( "Area", - string_length / 2 - char_width / 3, \

 - 0.75 / 2, "constraint_layer") ;
  }
```

In this case, the constraint_layer is used in the symbol.

EXAMPLE MESSAGE

```
Warning: Line 3453, Layers are ignored inside symbols. (LBDB-120)
```

LBDB-126 (error) The ’%s’ construct is not valid in ’%s’ libraries.

DESCRIPTION

This message indicates that the specified construct is not valid in the specified library. In Library Compiler, certain constructs are valid only in certain types of libraries. For example, pin resistances are not valid when specified on timing arcs in nonlinear (table_lookup) libraries.

WHAT NEXT

Remove the invalid construct from the library source file

EXAMPLES

```
library(lbdb126) {
  delay_model : "generic_cmos";
  piece_define("0 8 15");

  cell(INVERTER) {
    area : 5.0;
    cell_power : 1.0;
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
  }
}
```

In this case, the ’cell_power’ construct is not valid in piecewise_cmos libraries.

EXAMPLE MESSAGE

```
Error: Line 155, The ’cell_power’ construct is not valid
        in ’piecewise_cmos’ libraries. (LBDB-126)
```

LBDB-132 (error) In the ’%s’ cell, the %s pin ’%s’ cannot have

a ’%s’ attribute.

DESCRIPTION

This message indicates that you specified a **clock** or a **prefer_tied** attribute on a inout pin.

WHAT NEXT

Remove the specified attribute, or change the direction of the pin to input.

EXAMPLES

```
  cell(lbdb132) {
    area : 1;
    pin(A B C) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : inout;
      function : "A B";
      three_state : "C";
      clock : true;
      timing() {
intrinsic_rise : 0.1;
intrinsic_fall : 0.1;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "A B C";
      }
      timing() {
timing_type : three_state_disable;
intrinsic_rise : 0.1;
intrinsic_fall : 0.1;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "C";
      }
    }
  }
```

In this case, the ’Z’ pin whose direction is inout has a clok attribute set.

EXAMPLE MESSAGE

```
Error: Line 219, In the ’lbdb132’ cell, the inout pin ’Z’ cannot have
a ’clock’ attribute. (LBDB-132)
```

LBDB-136 (warning) The '%s' attribute on the '%s' pin in the '%s' cell is not valid on %s pins. The attribute is ignored.

DESCRIPTION

This message indicates that the attribute on the specified pin is invalid. The attribute is ignored.

WHAT NEXT

Refer to the "Library Compiler User Guide" to determine the reason why the attribute is not valid. Make the correction.

EXAMPLES

```
    cell(lbdb136) {
      area : 9;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(CP) {
direction : input;
capacitance : 1;
      }
      pin(CD) {
direction : input;
capacitance : 2;
      }
      ff("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
clear   : "CD'";
      }
      pin(Q) {
direction : output;
function : "IQ";
min_period : 0;
      }
```

In this case, the min_period attribute is defined for an output pin.

EXAMPLE MESSAGE

```
Warning: Line 1848, The  'min_period'  attribute on the 'Q' pin in
the 'lbdb136' cell is not valid on output pins.
The attribute is ignored. (LBDB-136)
```

LBDB-138 (warning) The timing arc is missing the piecewise data value for ’%s’. The value is interpolated if possible. Otherwise, the default value is used if it exists.

DESCRIPTION

This message indicates that you did not specify the definition of either delay intercept attributes or pin resistance attributes of piece number in a CMOS piecewise linear delay model library.

WHAT NEXT

Add the missing attribute to the specified piece number.

EXAMPLES

```
library(test) {
  delay_model : "generic_cmos";
  piece_define("0 8 15");

  cell(lbdb138) {
    area : 5.0;
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
    pin(Z) {
      direction : output;
      function : "A’";

      timing() {
intrinsic_rise : 5.0;
intrinsic_fall : 2.0;
slope_rise : 1.0;
slope_fall : 2.0;

        rise_delay_intercept(0, "1.1");
rise_delay_intercept(1, "2.2");
rise_delay_intercept(2, "3.3");

fall_delay_intercept(0, "1.1");
fall_delay_intercept(1, "2.2");
fall_delay_intercept(2, "3.3");

rise_pin_resistance(0, "1.1");
rise_pin_resistance(1, "2.2");

fall_pin_resistance(0, "4.4");
fall_pin_resistance(1, "4.4");
```

```
related_pin : "A";
      }
    }
  }
}
```

In this case, the value of the rise_pin_resistance attribute is missing for index 2.

EXAMPLE MESSAGE

```
Warning: Line 165, The timing arc is missing the piecewise data value
for 'rise_pin_resistance(2)'. The value is interpolated if possible
Otherwise, the default value is used if it exists. (LBDB-138)
```

LBDB-139 (error) Invalid delay model for the given technology.

DESCRIPTION

This message indicates that you specified an invalid value in the delay_model attribute.

WHAT NEXT

Refer to the "Library Compiler User Guide" for supported delay models. Change the value of the delay_model attribute to a valid one.

EXAMPLES

```
delay_model : "lbdb139";
```

EXAMPLE MESSAGE

```
Error: Line 3, Invalid delay model for the given technology. (LBDB-139)
```

LBDB-140 (warning) The '%s' cell contains circular timing arcs. The '%s' pin is in one of the cycles.

DESCRIPTION

The pin in the library cell has circular timing arcs. A circular timing arc occurs when an inout or output pin is related to itself through other inout or output pins. A change in one pin belonging to a circular timing arc continually loops around.

Circular timing arcs do not make sense and are probably mistakes. Therefore, the

Library Compiler flags them with warnings.

WHAT NEXT

Check the library source file, and verify the questionable circular timing arcs.

EXAMPLES

```
    cell(lbdb140) {
      area : 9;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(CP) {
direction : input;
capacitance : 1;
      }

      ff("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
      }
      pin(Q) {
direction : output;
function : "IQ";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "CP";
}
      }
      pin(Q2) {
direction : output;
function : "IQ";
timing() {
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "Q3";
}
      }
      pin(Q3) {
direction : output;
function : "IQ";
timing() {
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
```

```
  related_pin : "Q2";
}
      }
    }
```

EXAMPLE MESSAGE

```
Warning: Line 263, The 'lbdb140' cell contains circular timing arcs.
The 'Q2' pin is in one of the cycles. (LBDB-140)
```

LBDB-141 (warning) The timing arc is missing the piecewise data value for '%s'. The default value is used if it exists.

DESCRIPTION

This message indicates that you did not specify the definition of either delay intercept attributes or pin resistance attributes of the piece number defined in the piece_define in a CMOS piecewise linear delay model library.

WHAT NEXT

Add the missing attribute to the specified piece number.

EXAMPLES

```
library(test) {
  delay_model : "generic_cmos";
  piece_define("0");

  cell(lbdb138) {
    area : 5.0;
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
    pin(Z) {
      direction : output;
      function : "A'";

      timing() {
intrinsic_rise : 5.0;
intrinsic_fall : 2.0;
slope_rise : 1.0;
slope_fall : 2.0;

        rise_delay_intercept(0, "1.1");
```

```
rise_pin_resistance(0, "1.1");
fall_pin_resistance(0, "4.4");

related_pin : "A";
      }
    }
  }
```

In this case, the value of the fall_delay_intercept attribute is missing for index 2.

EXAMPLE MESSAGE

```
Warning: Line 170, The timing arc is missing the piece wise data value for
         'fall_delay_intercept(0)'. The default value is used if it exists. (LBDB-
141)
```

LBDB-142 (error) '%s' is an invalid value for the '%s' enumerated type attribute.

DESCRIPTION

This message indicated that you specified a value that is not part of the enumerated literals for the specified attribute.

WHAT NEXT

Refer to the "Library Compiler User Guide", and fix the invalid value.

EXAMPLES

```
  voltage_unit : "1";
```

EXAMPLE MESSAGE

```
Error: Line 19, '1' is an invalid value for the 'voltage_unit'
enumerated type attribute. (LBDB-142)
```

LBDB-143 (error) An invalid string is provided. The invalid string is either a blank string or a string that begins with a digit

that is unquoted.

DESCRIPTION

A string begining with a digit must be enclosed in double quotes (""). In addition, blank strings are not valid in Library Compiler.

WHAT NEXT

Check the library and correct the string. If the string begins with a digit, enclose the string in quotes. Remove any blank strings. For details on Library Compiler string rules, refer to the "Library Compiler Reference Manual".

EXAMPLES

```
type(111) {
  base_type : array;
  data_type : bit;
  bit_width : 2;
  bit_from : 1;
  bit_to : 0;
  downto : true;
}
```

In this case, the 111 type name starts with a digit. To fix the problem, add quotes.

EXAMPLE MESSAGE

```
Error: Line 29, An invalid string is provided. The invalid string is
either a blank string or a string that begins with a digit
that is unquoted. (LBDB-143)
```

LBDB-144 (error) The '%s' pin name does not match the '%s' bus name.

DESCRIPTION

This message indicates that you specified a bus element name different from the bus name given in the bus_naming_style. Library Compiler cannot extract the element name properly.

WHAT NEXT

Make sure that the bus_naming_style string matches the specified bus name.

LBDB-145 (warning) The ’direction’ attribute is missing in the %s ’%s’.

DESCRIPTION

This message indicates that the direction attribute is missing in the bus or bundle group.

WHAT NEXT

Add the direction attribute to the bus or bundle port in the technology library.

EXAMPLES

```
    bundle(Q) {
      members(XQ, Q1);
/*      direction : output; */
      function : "1";
    }
```

EXAMPLE MESSAGE

Warning: Line 53, The ’direction’ attribute is missing in the ’Q’ bundle. (LBDB-145)

LBDB-146 (error) The value for the update attribute must be "true" or "false".

DESCRIPTION

This message indicates that, in a symbol library, you specified an invalid value to the **update** attribute in either an **annotate_symbol** or an **annotate** group. This might be caused by a typo because the Library Compiler expects a quoted string.

WHAT NEXT

Check your symbol library file, and correct the value of the update attribute.

EXAMPLES

```
    annotate_symbol() {
      value( "ANN_PAGE_NUM", "ANN_NUM_PAGES") ;
      format : "sheet:  %s of %s" ;
      x : RIGHT_X ;
      y : LOW_Y ;
      layer_name : "template_text_layer" ;
```

```
      update : true;
    }
```

EXAMPLE MESSAGE

```
Error: Line 95, The value for the update attribute must be "true" or "false". (LBDB-
146)
```

LBDB-147 (error) A value must be specified for the annotate or the annotate_symbol group.

DESCRIPTION

This message indicates that, in a symbol library, you did not specify a value to either the **annotate** or the **annotate_symbol** group.

WHAT NEXT

Check your symbol library file, and add the value attribute.

EXAMPLES

```
    annotate_symbol() {
      format : "sheet:  %s of %s" ;
      x : RIGHT_X ;
      y : LOW_Y ;
      layer_name : "template_text_layer" ;
    }
```

In this case, the value attribute is missing. To fix the problem, add the attribute,

```
      value( "ANN_PAGE_NUM", "ANN_NUM_PAGES") ;
```

EXAMPLE MESSAGE

```
Error: Line 89, A value must be specified for the annotate or
the annotate_symbol group. (LBDB-147)
```

LBDB-148 (error) The '%s' pin is not found in the annotate_symbol group.

DESCRIPTION

This message indicates that, in a symbol library, you specified an invalid pin_name

value for the **pin_name** attribute in an **annotate_symbol**. This might be caused by a typo.

WHAT NEXT

Check your symbol library file, and correct the value of the pin_name attribute.

EXAMPLES

```
symbol("lbdb148") {
  set_minimum_boundary(0 , 0 , 8000, 12000);
  pin("P0", 10000, 1000, DOWN);

  line(0, 0, 0, 12000);
  line(0, 12000, 8000, 12000);
  line(8000, 12000, 8000, 0);
  line(8000, 0, 0, 0);
  annotate_symbol() {
    value( "ANN_PAGE_NUM", "ANN_NUM_PAGES") ;
    pin_name : "P2";
    format : "sheet:  %s of %s" ;
    x : RIGHT_X ;
    y : LOW_Y ;
    layer_name : "template_text_layer" ;
  }

}
```

In this case, the ’P2’ name does not exist in the ’lbdb148’ symbol. Change the name to P0.

EXAMPLE MESSAGE

Error: Line 89, The ’P2’ pin is not found in the annotate_symbol group. (LBDB-148)

LBDB-149 (error) The X value is invalid in the annotate or the annotate_symbol group.

DESCRIPTION

This message indicates that, in a symbol library, you specified an invalid value to the **X** attribute in either an **annotate** or **annotate_symbolf group. This might be caused by a typo.**

WHAT NEXT

Check your symbol library file, and correct the value of the X attribute.

EXAMPLES

```
symbol("lbdb148") {
  set_minimum_boundary(0 , 0 , 8000, 12000);
  pin("P0", 10000, 1000, DOWN);

  line(0, 0, 0, 12000);
  line(0, 12000, 8000, 12000);
  line(8000, 12000, 8000, 0);
  line(8000, 0, 0, 0);
  annotate_symbol() {
    value( "ANN_PAGE_NUM", "ANN_NUM_PAGES") ;
    format : "sheet:  %s of %s" ;
    x : "";
    y : LOW_Y ;
    layer_name : "template_text_layer" ;
  }

}
```

EXAMPLE MESSAGE

```
Error: Line 89, The X value is invalid in the annotate or
the annotate_symbol group. (LBDB-149)
```

LBDB-150 (error) The format specification cannot have more than %d %%s specifications.

DESCRIPTION

This message indicates that, in a symbol library, the format attribute has more than 10 string specifications. Library Compiler accepts only 10.

WHAT NEXT

Check your symbol library file, and reduce the number of specification in the format attribute.

EXAMPLES

```
  annotate_symbol() {
    value( "A1","A2","A3","A4","A5","A6","A7","A8","A9","A10" ) ;
    format : "sheet:  %s of %s %s of %s %s of %s %s of %s %s of %s %s of %s " ;
    x : RIGHT_X ;
    y : LOW_Y ;
    layer_name : "template_text_layer" ;
  }
```

EXAMPLE MESSAGE

```
Error: Line 101, The format specification cannot have more than 10 %s specification
s. (LBDB-150)
```

LBDB-151 (error) The format specification has %d %%s specification(s), but only %d value(s) is/are specified.

DESCRIPTION

This message indicates that, in a symbol library, the format specification does not match the number of values provided to either the **annotate** or the **annotate_symbol** group. This might be caused by a typo.

WHAT NEXT

Check your symbol library file, and correct the value of either the value attribute or the format attribute.

EXAMPLES

```
annotate_symbol() {
  value( "ANN_PAGE_NUM") ;
  format : "sheet:  %s of %s" ;
  x : RIGHT_X ;
  y : LOW_Y ;
  layer_name : "template_text_layer" ;
}
```

In this case, the value attribute has only the string value, but the format refers to two %s. To fix the problem, either add the second string value in the value attribute or remove the second %s in the format attribute.

EXAMPLE MESSAGE

```
Error: Line 89, The format specification has 2 %s specification(s),
but only 1 value(s) is/are specified. (LBDB-151)
```

LBDB-152 (error) The '%s' object type is invalid in the annotate

or the annotate_symbol group.

DESCRIPTION

This message indicates that, in a symbol library, you specified an invalid object type for the **object_type** attribute in either an **annotate** or **annotate_symbolf group. This might be caused by a typo. Library Compiler accepts the following object types:**

* pin
* design
* port
* cell
* net

WHAT NEXT

Check your symbol library file, and correct the value of the object_type attribute.

EXAMPLES

```
symbol("lbdb152") {
  set_minimum_boundary(0 , 0 , 8000, 12000);
  pin("P0", 10000, 1000, DOWN);

  line(0, 0, 0, 12000);
  line(0, 12000, 8000, 12000);
  line(8000, 12000, 8000, 0);
  line(8000, 0, 0, 0);
  annotate_symbol() {
    value( "ANN_PAGE_NUM", "ANN_NUM_PAGES") ;
    format : "sheet:  %s of %s" ;
    x : "RIGHT_X";
    y : LOW_Y ;
    layer_name : "template_text_layer" ;
    object_type : "library";
  }

}
```

EXAMPLE MESSAGE

```
Error: Line 89, The 'library' object type is invalid in the annotate
or the annotate_symbol group. (LBDB-152)
```

LBDB-153 (error) A syntax error is found before the library or phys_library group.

The compilation is terminated.

DESCRIPTION

This message follows lexical and syntax error messages issued when reading a library.

WHAT NEXT

Fix all lexical and syntax errors.

EXAMPLES

```
          related_bus_pins : { ADDR";
```

In this case, a lexical error is encountered in the related_bus_pins value. Substitute the '{' for a '"'.

EXAMPLE MESSAGE

```
Error: A syntax error is found before the library or phys_library group.
The compilation is terminated. (LBDB-153)
```

LBDB-155 (warning) The %s_cell for the '%s' cell with '%s' operating_conditions is defined multiple times in the library. Using the last one encountered.

DESCRIPTION

This message indicates that a scaled_cell with the same operating_conditions is defined multiple times in the library. This might be caused by a typo in the name of the operating_conditions. Library Compiler uses the last cell encountered.

WHAT NEXT

Delete all the redundant scaled_cell groups, or fix the library if it is a typo.

EXAMPLES

```
library(lbdb155) {
    operating_conditions(WCCOM) {
process : 1.5 ;
        temperature : 70 ;
voltage : 4.75 ;
tree_type : "worst_case_tree" ;
```

```
    }
    cell(IVV) {
      area : 1;
      pin(A) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "A'";
timing() {
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A";
}
      }
    }

    scaled_cell(IVV,WCCOM) {
      area : 1;
      pin(A) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "A'";
timing() {
  intrinsic_rise : 0.3;
  intrinsic_fall : 0.3;
  rise_resistance : 0.3;
  fall_resistance : 0.3;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A";
}
      }
    scaled_cell(IVV,WCCOM) {
      area : 1;
      pin(A) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "A'";
timing() {
  intrinsic_rise : 0.3;
  intrinsic_fall : 0.3;
  rise_resistance : 0.3;
  fall_resistance : 0.3;
```

```
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A";
}
      }
    }
  }
```

EXAMPLE MESSAGE

```
Warning: Line 327, The scaled_cell for the 'AND' cell with 'WCCOM'
         operating_conditions is defined multiple times in the library.
         Using the last one encountered. (LBDB-155)
```

LBDB-156 (error) The LSI rounding digit and cutoff attributes have incompatible values.

DESCRIPTION

This message indicates that you specified invalid values for either the **lsi_rounding_digit** or the **lsi_rounding_cutoff** attribute. Library Compiler issues this error when the lsi_rounding_digit value is greater than the lsi_rounding_cutoff value multiplied by 10.01 or the lsi_rounding_cutoff value is greater than the lsi_rounding_digit value.

WHAT NEXT

Check the library, and fix either the value of the lsi_rounding_digit or the lsi_rounding_cutoff attribute.

EXAMPLES

```
   lsi_rounding_digit : 0.1;
   lsi_rounding_cutoff : 0.003;
```

In this case, the lsi_rounding_digit 0.1 is greater than (0.003 * 10.01). To fix the problem, assign the value 0.01 to lsi_rounding_digit.

```
   lsi_rounding_digit : 0.01;
```

EXAMPLE MESSAGE

```
Error: Line 10, The LSI rounding digit and cutoff attributes
have incompatible values. (LBDB-156)
```

LBDB-157 (error) The '%s' cell name defined in the scaled_cell

is not found.

DESCRIPTION

This message indicates that the technology library has a scaled_cell defined without a parent cell defined. Library Compiler uses the scaled_cell group to supply an alternate set of values for an existing cell. The choice is based on the set of operating conditions used.

WHAT NEXT

Add the parent cell for the scaled_cell, or fix the scaled_cell name if it is a typo.

EXAMPLES

```
library(lbdb157) {
    operating_conditions(WCCOM) {
process : 1.5 ;
        temperature : 70 ;
voltage : 4.75 ;
tree_type : "worst_case_tree" ;
    }

cell(IV) {
  area : 1;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A'";
    timing() {
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
scaled_cell(IVV,WCCOM) {    /* Typo in the cell name. */
  area : 1;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
```

```
    function : "A'";
    timing() {
      intrinsic_rise : 0.3;
      intrinsic_fall : 0.3;
      rise_resistance : 0.3;
      fall_resistance : 0.3;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
}
```

EXAMPLE MESSAGE

```
Error: Line 101, The 'IVV' cell name defined in the scaled_cell is not found. (LBDB-157)
```

LBDB-158 (error) The '%s' operating conditions is not found.

DESCRIPTION

This message indicates that the technology library has a scaled_cell with an undefined operating conditions.

WHAT NEXT

Add the operating_conditions group if it is missing, or fix the operating_conditions name if it has a typo.

EXAMPLES

```
library(lbdb158) {
    operating_conditions(WCCOM) {
process : 1.5 ;
        temperature : 70 ;
voltage : 4.75 ;
tree_type : "worst_case_tree" ;
    }

cell(IV) {
  area : 1;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
```

```
    function : "A'";
    timing() {
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
scaled_cell(IV,WCCOM1) {    /* Typo in the operating_conditions name. */
  area : 1;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A'";
    timing() {
      intrinsic_rise : 0.3;
      intrinsic_fall : 0.3;
      rise_resistance : 0.3;
      fall_resistance : 0.3;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
}
```

EXAMPLE MESSAGE

```
Error: Line 305, The 'WCCOM1' operating conditions is not found. (LBDB-158)
```

LBDB-159 (error) Incomplete EDIF properties are specified in the '%s' symbol.
Specify 'edif_cell_name', 'edif_view_name', and 'edif_name_property'.

DESCRIPTION

This message indicates that, in a symbol library, you specified incomplete attributes of the view identifier properties of the symbol for a cell. These attributes are **edif_cell_name**, **edif_view_name**, and **edif_name_property**. If Library

Compiler encounters a symbol with any of these attributes, it must have all three of them declared.

WHAT NEXT

Change the symbol definition for the cell in the source text file of the symbol library. Either delete the view identifier property attributes that are there so that the symbol has none of those attributes or add appropriate view identifier property attributes, so that the symbol has all three of those attributes.

EXAMPLES

```
  symbol("lbdb159") {
    set_minimum_boundary(0 , 0 , 8000, 12000);
    pin("P0", 10000, 1000, DOWN);

    line(0, 0, 0, 12000);
    line(0, 12000, 8000, 12000);
    line(8000, 12000, 8000, 0);
    line(8000, 0, 0, 0);
    edif_cell_name : "edifcell";
    edif_name_property : " edifproperty";
  }
```

In this case, the edif_view_name attribute is missing. To fix the problem, add

```
    edif_view_name : "edifview";
```

EXAMPLE MESSAGE

```
Error: Incomplete EDIF properties are specified in the 'lbdb159' symbol.
       Specify 'edif_cell_name', 'edif_view_name', and 'edif_name_property'. (LBDB-
159)
```

LBDB-160 (error) It is not acceptable to set the technology to '%s' after it has been set to '%s'. The two technologies are incompatible.

DESCRIPTION

This message indicates that you specified incompatible values for the technology attribute and the delay_model attribute.

WHAT NEXT

Check The Library Compiler User Guide Manual for compatible combinations, and fix either the value of the technology or the delay_model attribute.

EXAMPLES

```
library(lbdb160) {
    /* wrong technology and delay model combination */
    technology("cmos");
    delay_model : generic_ecl;
}
```

EXAMPLE MESSAGE

```
Error: Line 4, It is not acceptable to set the technology to
'generic_ecl' after it has been set to 'cmos'. The two
technologies are incompatible. (LBDB-160)
```

LBDB-161 (error) The '%s' bus needs to have its bus_type specified first.

The %s '%s' was found before the bus_type.

DESCRIPTION

This message indicates that you specified a bus without its bus_type attribute, or Library Compiler rejected the bus_type value and considered it as not defined.

WHAT NEXT

Add the bus_type attribute to the library, or fix the value of the attribute.

EXAMPLES

```
    bus (D) {
/*    bus_type : bus2; *//* remove the comment to fix the problem */
      direction : input;
      capacitance : 1.0;
    }
```

EXAMPLE MESSAGE

```
Error: Line 179, The 'D' bus needs to have its bus_type specified first.
       The attribute 'direction' was found before the bus_type. (LBDB-161)
```

LBDB-162 (error) An invalid area range is found in the

wire_load_from_area attribute.

DESCRIPTION

This message indicates that you specified an invalid area range. The problem is caused by any of these reasons:

* The min_area value is greater than the max_area value.
* The min_area value is less than zero.
* The max_area value is less or equal to zero.

WHAT NEXT

Check the area values, and fix the problem.

EXAMPLES

```
wire_load("05x05") {
  resistance : 0 ;
  capacitance : 1 ;
  area : 0 ;
  slope : 0.186 ;
  fanout_length(1,0.39) ;
}
wire_load_selection(test) {
  wire_load_from_area(27,10,"10x10");/* problem */
  wire_load_from_area(27,100,"10x10");
  wire_load_from_area(0,28,"05x05");
  wire_load_from_area(2,10,"15x10");
}
```

In this case, the minimum area value 27 is greater than the maximum area value 10.

EXAMPLE MESSAGE

```
Error: Line 51, An invalid area range is found in the wire_load_from_area attribute
. (LBDB-162)
```

LBDB-163 (warning) The '%s' attribute value is %s (%3.1f). Using %3.1f instead.

DESCRIPTION

This message indicates that you specified an attribute value that is out of the accepted range. The value is either less than the minimum value or greater than the maximum value.

WHAT NEXT

Change the attribute value to satisfy the value range.

EXAMPLES

```
     k_volt_internal_power : -111.0;
```

In this case, the k_volt_internal attribute’s value -111.0 is less than the minimum accepted value -100.0.

EXAMPLE MESSAGE

```
Warning: Line 9, The ’k_volt_internal_power attribute’ attribute value is
 less than the minimum allowed  (-100.0). Using 0.0 instead. (LBDB-163)
```

LBDB-164 (error) The ’wire_load_from_area’ range overlaps the range in line %d.

DESCRIPTION

This message indicates that you specified an overlapping area range in two **wire_load_from_area** attributes.

WHAT NEXT

Change the area range in the second **wire_load_from_area** attribute.

EXAMPLES

```
    wire_load("05x05") {
    resistance : 0 ;
    capacitance : 1 ;
    area : 0 ;
    slope : 0.186 ;
    fanout_length(1,0.39) ;
  }

  wire_load_selection(test) {
    wire_load_from_area(0,20,"05x05");
    wire_load_from_area(10,25,"05x05");
  }
```

In this case, the area range [0,20] overlaps the area range [10,25].

EXAMPLE MESSAGE

```
Error: Line 12, The 'wire_load_from_area' range overlaps
        the range in line 13. (LBDB-164)
```

LBDB-165 (warning) A range gap is found in the 'wire_load_selection'. The 'min_area' is extended from %f to %f.

DESCRIPTION

The wire_load_selection specified in this library has a gap. It means that two adjacent selector items are not overlapped. Library Compiler uses its built-in algorithm to fill the gap. It extends the lower bound of the selector that covers the bigger area toward the upper bound of the other selector item.

WHAT NEXT

Ignore the warning if the Library Compiler's algorithm satisfies your modeling requirement. Otherwise, fix the library source code to match your wire_load_selection model.

EXAMPLES

```
    wire_load("05x05") {
    resistance : 0 ;
    capacitance : 1 ;
    area : 0 ;
    slope : 0.186 ;
    fanout_length(1,0.39) ;
  }

  wire_load_selection(test) {
    wire_load_from_area(0,20,"05x05");
    wire_load_from_area(25,50,"05x05");
  }
```

In this case, there is a gap in area range from 20 to 25. Library Compiler corrects the problem as if you had the declaration

```
    wire_load_from_area(20,50,"05x05");
```

EXAMPLE MESSAGE

```
Warning: Line 13, A range gap is found in the 'wire_load_selection'.
        The 'min_area' is extended from 25.000000 to 20.000000. (LBDB-165)
```

LBDB-166 (warning) A range does not start with 0.0 in the 'wire_load_selection'.
The 'min_area' is extended from %f to 0.0.

DESCRIPTION

The min_area value in the specified wire_load_selection attribute in this library does not start with 0.0. Library Compiler extends the lower bound of the selector to 0.0.

WHAT NEXT

Fix the library source code to set the min_area to 0.0.

EXAMPLES

```
wire_load("05x05") {
  resistance : 0 ;
  capacitance : 1 ;
  area : 0 ;
  slope : 0.186 ;
  fanout_length(1,0.39) ;
}

wire_load_selection(test) {
  wire_load_from_area(10,25,"05x05");
}
```

EXAMPLE MESSAGE

```
Warning: Line 48, A range does not start with 0.0 in the 'wire_load_selection'.
        The 'min_area' is extended from 10.000000 to 0.0. (LBDB-166)
```

LBDB-167 (error) The '%s' scaling factors group is not found.

DESCRIPTION

The message indicates that you specified an invalid name for the scaling_factors group. This might be caused either by a typo in the name or by the group not being defined.

WHAT NEXT

Add the scaling_factors group to the library, or correct the value of the scaling_factors if it is a typo.

EXAMPLES

```
    scaling_factors("IO_PAD_SCALING") {
        k_volt_intrinsic_rise : 0.846 ;
    }
    cell (lbdb167) {
       area : 0 ;
       scaling_factors : IO_PAD_SCALE ;
    }
```

In this case, there is a typo in the name.

EXAMPLE MESSAGE

```
Error: Line 20, The 'IO_PAD_SCALE' scaling factors group is not found. (LBDB-167)
```

LBDB-168 (error) The %s timing constraint has only one value. Only one 'intrinsic_rise' or 'intrinsic_fall' can be specified.

DESCRIPTION

You specified invalid values for intrinsic_rise and intrinsic_fall in a timing group that describes a **recovery** or **removal** timing constraint. Library Compiler complains if each of these two constraints has

* Both intrinsic_rise and intrinsic_fall values are assigned to zero.
* Both intrinsic_rise and intrinsic_fall values are not specified.
* Both intrinsic_rise and intrinsic_fall values are not zero.

WHAT NEXT

Inspect the datasheet of the cell in question. If the asynchronous control signal is high-active, define the recovery and the removal constraints as the intrinsic_fall. If the asynchronous control signal is low-active, define the recovery and the removal constraints as the intrinsic_rise. Remove the other field (intrinsic_rise or intrinsic_fall) from the library source file.

EXAMPLES

```
    pin(CD) {
      direction : input;
      capacitance : 2;
      timing() {
timing_type : recovery_rising;
/* both values are 0.0 */
intrinsic_rise : 0.0;
intrinsic_fall : 0.0;
related_pin : "CP";
```

```
      }
      timing() {
timing_type : removal_rising;
/* both values not specified */
related_pin : "CP";
      }
    }
```

EXAMPLE MESSAGE

```
Error: Line 56, The Recovery timing constraint has only one value.
        Only one 'intrinsic_rise' or 'intrinsic_fall' can be specified. (LBDB-168)
```

LBDB-169 (error) An invalid 'three_state_disable' timing type appears
on the timing arc. Its parent output pin has no 'three_state' attribute.

DESCRIPTION

This message indicates that you specified a **three_state_disable** timing_arc on a port that has no **three_state** attribute.

WHAT NEXT

Either delete the timing arc or correct the port group definition to add the three_state attribute.

EXAMPLES

```
  cell(AND) {
    area : 1;
    pin(A B) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "A B";
      timing() {
intrinsic_rise : 0.1;
intrinsic_fall : 0.1;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "A B" ;
      }
      timing() {
```

```
timing_type : three_state_disable;
intrinsic_rise : 0.1;
intrinsic_fall : 0.1;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "A";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 44, An invalid 'three_state_disable' timing type appears
on the timing arc. Its parent output pin has no 'three_state' attribute. (LBDB-169)
```

LBDB-170 (warning) The '%s' attribute's value is %s (%3.1f). Removing it.

DESCRIPTION

This message indicates that you specified an attribute value that is out of the accepted range. The value is either less than the minimum value or greater than the maximum value. Library Compiler ignores the value because it does not find a default value to replace it.

WHAT NEXT

Change the attribute value to satisfy the value range.

EXAMPLES

```
    pin(A) {
      direction : input;
      capacitance : 1;
      min_fanout : -1;
    }
```

In this case, the min_fanout attribute's value -1 is less than the minimum accepted value 0.0.

EXAMPLE MESSAGE

```
Warning: Line 283, The 'min_fanout' attribute value is
         less than the minimum allowed (0.0). Removing it. (LBDB-170)
```

LBDB-171 (error) The ’%s’ wire load model is not defined, or it is defined after this line.

DESCRIPTION

This message indicates that you specified a "wire_load_from_area" that refers to a "wire_load" group that is not defined or has been defined in the library after the current line.

WHAT NEXT

Check your library to see if you have defined the group. If you have done that, also check its position within the library to make sure it is defined before it is used.

EXAMPLES

```
wire_load("05x05") {
  resistance : 0 ;
  capacitance : 1 ;
  area : 0 ;
  slope : 0.186 ;
  fanout_length(1,0.39) ;
}

wire_load_selection(test) {
  wire_load_from_area(27,100,"10x10");
  wire_load_from_area(10,25,"05x05");
}
```

EXAMPLE MESSAGE

Error: Line 47, The ’10x10’ wire load model is not defined, or
it is defined after this line. (LBDB-171)

LBDB-172 (warning) The ’%s’ attribute is not specified. Using %4.2f.

DESCRIPTION

This message indicates that an attribute is missing, and Library Compiler is reporting the default floating point or integer value it is setting. This message affects attributes with default values.

WHAT NEXT

Either add the missing attribute to the technology library or ignore the message.

EXAMPLES

```
pin(D) {
  direction : input;
}
```

EXAMPLE MESSAGE

Warning: Line 52, The ’capacitance’ attribute is not specified. Using 0.00. (LBDB-172)

LBDB-173 (error) The ’%s’ group requires one or more names.

DESCRIPTION

This message indicates you specified no name for a group that requires at least one name.

WHAT NEXT

Change your library to add the group name.

EXAMPLES

```
pin() {
  direction : input;
  capacitance : 1.0;
}
```

In this case, a pin name is required.

EXAMPLE MESSAGE

Error: Line 286, The ’pin’ group requires one or more names. (LBDB-173)

LBDB-174 (error) The ’%s’ group requires %d names.

DESCRIPTION

This message indicates that you specified a group without its required number of names. This might be caused by a typo.

WHAT NEXT

Refer to the "Library Compiler User Guide" for the correct syntax of the specified group, and match the number of group names.

EXAMPLES

```
      ff(IQ,IQN, 2)
```

In this case, the ’ff’ group requires 2 names. To fix the problem, either remove the last element 2 or if it is a typo change ff to ff_bank.

EXAMPLE MESSAGE

Error: Line 87, The ’ff’ group requires 2 names. (LBDB-174)

LBDB-175 (warning) The bus_naming_style contains characters that are also used as delimiters in function, three_state, and related_pin attributes. Be sure to put spaces around the characters in the [%s] set when supplying values for attributes of the types mentioned. Also, surround subscripted pin names with double quotes in pin groups.

DESCRIPTION

This message indicates that you specified delimiter characters in the **bus_naming_style** attribute such as "/
/ \

WHAT NEXT

Change the delimiter character, or follow the rules specified in the message.

EXAMPLES

```
  bus_naming_style : %s&%d;
```

EXAMPLE MESSAGE

```
Warning: Line 28, The bus_naming_style contains characters that
        are also used as delimiters in function, three_state, and related_pin
        attributes. Be sure to put spaces around the characters in the [&] set
        when supplying values for attributes of the types mentioned.
        Also, surround subscripted pin names with double quotes in pin groups. (LBD
B-175)
```

LBDB-176 (error) Invalid bus syntax is detected in '%s'.

DESCRIPTION

This message indicates that you specified an invalid bus element. Library Compiler fails to extract the bus element information using the bus_naming_style attribute value.

WHAT NEXT

Change the library by either fixing the bus_naming_style value or fixing the bus element representation.

LBDB-177 (warning) The attribute '%s' is not specified Using '%s'.

DESCRIPTION

This message indicates that an attribute is missing, and Library Compiler is reporting the default string value it is setting. This message affects attributes with default values.

WHAT NEXT

Either add the missing attribute to the technology library or ignore the message.

LBDB-179 (error) The '%s' group requires the '%s' attribute. Either the attribute is missing or the attribute has an invalid

value.

DESCRIPTION

This message indicates you specified a group without one of its required attributes. Library Compiler rejects the attribute definition if the attribute exists and has an invalid value.

WHAT NEXT

Change the library file by adding the missing attribute to the group.

EXAMPLES

```
memory() {
  type : random;
  address_width : 10;
  word_width : 8;
}
```

In this case, the ’type’ has an invalid value. To fix the problem, assign ’rom’ or ’ram’ to the type.

EXAMPLE MESSAGE

```
Error: Line 27, The ’memory’ group requires the ’type’ attribute.
Either the attribute is missing or the attribute has an invalid value. (LBDB-179)
```

LBDB-180 (error) The ’%s’ attribute requires both ’clear’ and ’preset’ attributes.

DESCRIPTION

This message indicates that you specified the ’clear_preset_var1’ or the ’clear_preset_var2’ attribute or both in a sequential model group without specifying both the ’clear’ and the ’preset’ attributes.

WHAT NEXT

Add the missing attribute to the group.

EXAMPLES

```
      ff("IQ","IQN") {
next_state : "D";
```

```
clocked_on : "CP";
clear : "CD'";
clear_preset_var1: "L";
      }
```

In this case, the 'preset' attribute is missing in the ff group.

EXAMPLE MESSAGE

```
Error: Line 98, The 'clear_preset_var1' attribute requires both
'clear' and 'preset' attributes. (LBDB-180)
```

LBDB-181 (error) The '%s' group, with both 'clear' and 'preset' attributes, requires 'clear_preset_var1' and/or 'clear_preset_var2' attributes.

DESCRIPTION

This message indicates that you specified both the 'clear' and the 'preset' attribute in a sequential model group without specifying both the 'clear_preset_var1' or the 'clear_preset_var2' attributes.

WHAT NEXT

Add either 'clear_preset_var1' or 'clear_preset_var2' to the sequential group.

EXAMPLES

```
      ff("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
preset : "SD'";
clear : "CD";
```

In this case, the 'clear_preset_var1' and or 'clear_preset_var2' attributes are missing.

EXAMPLE MESSAGE

```
Error: Line 93, The 'ff' group, with both 'clear' and 'preset' attributes,
        requires 'clear_preset_var1' and/or 'clear_preset_var2' attributes. (LBDB-
181)
```

LBDB-182 (error) Invalid %s name '%s' is detected. This name must be unique among all pin names, bus names, bundle names, and rail connection names.

DESCRIPTION

This message indicates a duplicate pin, bus, bundle, or a rail_connection name in the library.

WHAT NEXT

Change the name of the pin, bus, bundle, rail_connection in the technology library.

EXAMPLES

```
pin(D) {
  direction : input;
  capacitance : 1.0;
}
pin(D) {
  direction : input;
  capacitance : 1.0;
}
```

EXAMPLE MESSAGE

```
Error: Line 56, Invalid pin name 'D' is detected. This name must be
        unique among all pin names, bus names, and bundle names. (LBDB-182)
```

LBDB-186 (error) Invalid '%s' pin name is detected in the '%s' bundle.

DESCRIPTION

This message indicates that you specified an invalid pin name in a bundle group.

WHAT NEXT

Change the library source file by correcting the pin name.

LBDB-187 (error) The ’%s’ bundle needs to have its ’members’ specified first.
The ’%s’ %s is found before a ’members’.

DESCRIPTION

This message indicates that you specified the members attribute in a bundle group after another attribute. The **members** attribute has to be first in the bundle group.

WHAT NEXT

Change the library source file by specifying the members attribute first in the bundle group.

EXAMPLES

```
      bundle (DD) {
direction : input;
members(D1, D2);
capacitance : 1;
      }
```

EXAMPLE MESSAGE

```
Error: Line 94, The ’DD’ bundle needs to have its ’members’ specified first.
       The ’direction’ attribute is found before a ’members’. (LBDB-187)
```

LBDB-188 (error) The ’members’ attribute is defined multiple times.

DESCRIPTION

This message indicates that you specified the **members** attribute in a bundle group more than once. Library Compiler expects only one **members** attribute in the bundle group.

WHAT NEXT

Change the library source file by specifying only one members attribute in a bundle group.

EXAMPLES

```
      bundle (DD) {
```

```
direction : input;
members(D1, D2);
members(D3, D4);
capacitance : 1;
      }
```

EXAMPLE MESSAGE

```
Error: Line 95, The 'members' is defined multiple times. (LBDB-188)
```

LBDB-189 (warning) Level shifters are required for this library. A level shifter is a buffer or inverter with differing connection_class values specified between input and output pins. Design Compiler cannot produce valid designs using this library if a level shifter component is not provided.

DESCRIPTION

This warning message occurs when your library contains connection classes that cannot be used without level shifters. Design Compiler uses these components to shift a net from one connection class to another and does so to remove connection class violations from your design. Multi-input or multi-output cells with differing connection classes on inputs and outputs are not considered level shifters. Following this warning message, a list appears of those connection classes that do not have valid shifters between them.

This warning alerts you to situations where Design Compiler might not be able to validate your design for connection class. For example, suppose that Library Compiler warns that you are missing a level shifter with an input connection class of "a" and an output connection class of "b". If there is a pin or port in your design with a connection class of "b" connected to a driver with a connection class of "a", Design Compiler might be unable to validate this connection without a level shifting component that converts voltage levels from an input connection class of "a" to an output connection class of "b".

There are cases where this message can be too restrictive. For example, consider the case where you, the designer, know that all inputs to your design will only have connection class "a" and that all outputs will only have connection class "c". Meanwhile, for the purposes of our example, assume that all "internal" logic in the design will have connection class "b". If you defined a library with two level shifters (one with "a" on the input and "b" on the output, and the other with "b" on the input and "c" on the output), Design Compiler can validate the design because it can convert voltage levels from the inputs at level "a" to internal logic at level "b", and from internal logic at level "b" to the outputs at level "c". In this case, the warnings that you receive about missing level shifters would be too restrictive. However, you have an output that is at level "a", and is driven by internal logic at level "b", Design Compiler is not be able to validate the design unless it can replace the component driving the output port with a component that has level "a" on

its output pin.

Be aware of the current limitations in the connection class validation and be advised that you can construct a library with connection rule restrictions that are too difficult for Design Compiler to solve. Future versions of the software might remove these restrictions, but Library Compiler currently informs you of the limitations on validating a design for connection class violations.

WHAT NEXT

If this message appeared because you omitted some level shifting components from your library, add the components.

EXAMPLES

```
    cell(lbdb189) {
      /* Should only be connected to IO Cells only */
      area : 0.0;
      dont_touch : false;
      dont_use   : false;
      pad_cell : true;
      pin(PAD ) {
is_pad : true;
input_voltage : CMOS;
direction   : input;
capacitance : 1.0;
fanout_load : 0.0;
      }
      pin(Y ) {
connection_class : "iopcl";
direction   : output;
function    : "PAD";
max_fanout  : 1.0;
timing() {
  intrinsic_fall  : 1.0;
  intrinsic_rise  : 1.0;
  fall_resistance : 0.0;
  rise_resistance : 0.0;
  related_pin  :"PAD ";
}
      }
    }
```

EXAMPLE MESSAGE

```
Warning: Line 1, Level shifters are required for this library.
A level shifter is a buffer or inverter with differing
connection_class values specified between input and output
pins. Design Compiler cannot produce valid designs using this
library if a level shifter component is not provided. (LBDB-189)
```

LBDB-190 (warning) %s level shifter with input connection class '%s' and output connection class '%s' is needed.

DESCRIPTION

This message indicates that a (noninverting or inverting) level shifter is needed between the two connection classes. See the man page for error LBDB-189 for more information on how this message can occur.

WHAT NEXT

If you obtained this message because you omitted a level shifting component from your library, add the level shifting component.

EXAMPLES

```
    cell(IOPCLBUF) {
      /* Should only be connected to IO Cells only */
      area : 0.000000;
      dont_touch : false;
      dont_use   : false;
      pad_cell : true;
      pin(PAD ) {
is_pad : true;
input_voltage : CMOS;
direction   : input;
capacitance : 35.000000;
fanout_load : 0.000000;
      }
      pin(Y ) {
connection_class : "iopcl";
direction   : output;
function    : "PAD";
max_fanout  : 16.000000;
timing() {
  intrinsic_fall  : 3.925000;
  intrinsic_rise  : 3.925000;
  fall_resistance : 0.000000; /* delay included in intrinsic */
  rise_resistance : 0.000000; /* delay included in intrinsic */
  related_pin  :"PAD ";
}
      }
    }
```

EXAMPLE MESSAGE

Warning: Line 1, Noninverting level shifter with input connection class 'iopcl' and output connection class 'default' is needed. (LBDB-190)

LBDB-191 (error) The inout ’%s’ pin, bus, or bundle has no ’three_state’ function.

DESCRIPTION

The pin whose direction is specified as ’inout’ has only a ’function’ statement. The ’three_state’ statement is also required by an "inout" pin.

WHAT NEXT

If the pin is actually an output pin, change the direction attribute to ’output’. Otherwise, add the ’three_state’ statement to the pin.

EXAMPLES

```
pin(Z) {
  direction : inout;
  function : "A B";
}
```

EXAMPLE MESSAGE

Error: Line 356, The inout ’Z’ pin, bus, or bundle has
no ’three_state’ function. (LBDB-191)

LBDB-192 (error) Illegal interdependence data specified in pin "%s".

DESCRIPTION

timing arc with "interdependence_id" attribute is treated as interdependence data in pin. they are used for setup/hold pessimism reduction. There are some rules to specified the id for interdependence data (These rules applies to timing arcs with same condition):

1. Interdependece data can not be the first timing arc in this pin. This it to prevent potential backward compatibility issue.

2. Interdependece data should be in pair. That is, if there is a setup_rising interdependence data with id = 1 in the pin, a hold_rising interdependence data with same id = 1 is needed. Same case for timing type = setup_falling / hold_falling.

3. For one timing_type arcs, the interdependence id should be unique. E.g. If there are two setup_rising interdependence data with same id = 1, this error is issued.

4. The interdependence id starts from 1, and if multiple interdependence data

defined for the pin, the id should be consecutive. E.g. id = 1,2,3 is okay, but 1, 2, 4 is not.

WHAT NEXT

Check the id value for interdependence data in the pin group, make sure all above requirments are satisfied.

EXAMPLES

```
    pin(D) {
      direction : input;
timing() {
    timing_type : setup_rising;
    fall_constraint("template") {
    ...
    }
    rise_constraint("template") {
    ...
    }
    related_in: "CLK";
}
timing() {
    timing_type : setup_rising;
    interdependence_id : 1;
    fall_constraint("template") {
    ...
    }
    rise_constraint("template") {
    ...
    }
    related_in: "CLK";
}
timing() {
    timing_type : hold_rising;
    fall_constraint("template") {
    ...
    }
    rise_constraint("template") {
    ...
    }
    related_in: "CLK";
}
timing() {
    timing_type : hold_rising;
    interdependence_id : 2;
    fall_constraint("template") {
    ...
    }
    rise_constraint("template") {
    ...
    }
    related_in: "CLK";
}
```

```
    }
```

EXAMPLE MESSAGE

```
Error: Line 356, Illegal interdependence data specified in pin "D".(LBDB-192)
```

LBDB-193 (error) Interdependence data is defined for wrong timing type arc in pin "%s".

DESCRIPTION

Timing group with "interdependence_id" attribute is treated as interdependence data in pin. they are used to for setup/hold pessimism reduction. For now, It’s only supported for these timing types: setup_rising, hold_rising, setup_falling, hold_falling.

WHAT NEXT

Check the interdependence data in the pin group, make sure they are defined for constraint arcs with right timing type.

EXAMPLES

```
    pin(D) {
      direction : input;
timing() {
    timing_type : setup_rising;
    fall_constraint("template") {
    ...
    }
    rise_constraint("template") {
    ...
    }
    related_in: "CLK";
}
timing() {
    timing_type : skew_rising; // not support type
    interdependence_id : 1;
    fall_constraint("template") {
    ...
    }
    rise_constraint("template") {
    ...
    }
    related_in: "CLK";
}
timing() {
    timing_type : hold_rising;
    fall_constraint("template") {
```

```
    ...
    }
    rise_constraint("template") {
    ...
    }
    related_in: "CLK";
}
timing() {
    timing_type : hold_rising;
    interdependence_id : 2;
    fall_constraint("template") {
    ...
    }
    rise_constraint("template") {
    ...
    }
    related_in: "CLK";
}
    }
```

EXAMPLE MESSAGE

```
Error: Line 356, Interdependence data is defined for wrong timing type arc in pin "
D".(LBDB-193)
```

LBDB-200 (error) The cell has both the ’pad_cell’ and the ’auxiliary_pad_cell’ attributes.

DESCRIPTION

This message indicates that you specified both the **pad_cell** and the auxiliary_pad_cell attributes in the same cell.

WHAT NEXT

Remove either the pad_cell attribute or the auxiliary_pad_cell attribute.

EXAMPLES

```
    cell(lbdb200){
      area : 0.000000;
      pad_cell : true;
      auxiliary_pad_cell : true;
    }
```

EXAMPLE MESSAGE

```
Error: Line 3577, The cell has both the 'pad_cell' and the 'auxiliary_pad_cell' att
ributes. (LBDB-200)
```

LBDB-201 (error) A nonpad '%s' cell has a '%s' attribute.

DESCRIPTION

This message indicates that you specified a pad_type attribute in a nonpad cell.

WHAT NEXT

Check the "Library Compiler User Guide" for information on pad cells. Either remove the invalid attribute or add the pad_type, the pad_cell, or the auxiliary_pad_cell attribute.

EXAMPLES

```
  cell(lbdb201){
      area : 0.0;
      pad_type : clock;
      pin(Z)  {
        direction : output
        function : "A"
      }
      pin(A) {
direction : input;
capacitance : 1.0;
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 3577, A nonpad 'lbdb201' cell has a 'pad_type' attribute. (LBDB-201)
```

LBDB-202 (error) A nonpad '%s' cell has a '%s' pin with a '%s' attribute.

DESCRIPTION

This message indicates that you specified a pad pin attribute in a nonpad cell.

WHAT NEXT

refer to the "Library Compiler User Guide" for information on pad cells. Either remove the invalid attribute or add the pad_cell attribute.

EXAMPLES

```
  cell(lbdb202){
      area : 0.0;
      pin(Z)  {
        is_pad : true;
        direction : output
        drive_current : 2.0;
        function : "A"
      }
      pin(A) {
direction : input;
capacitance : 1.0;
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 3581, A nonpad 'lbdb202' cell has a 'Z' pin
       with a 'is_pad' attribute. (LBDB-202)
```

LBDB-203 (error) The nonpad '%s' pin has a '%s' attribute.

DESCRIPTION

This message indicates that you specified a pad cell with pad_type and pad_cell attributes defined and a nonpad pin with a hysteresis attribute.

WHAT NEXT

Refer to the "Library Compiler User Guide" for information on pad cells. Either remove the pad cell attributes or add the pad pin attributes.

EXAMPLES

```
  cell(lbdb203){
    area : 0.0;
    pad_type : clock;
    pad_cell : true;
    pin(Z)  {
      direction : output;
      hysteresis : true;
      function : "A";
    }
```

```
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 3584, The nonpad ’Z’ pin has a ’hysteresis’ attribute. (LBDB-203)
```

LBDB-204 (error) The ’%s’ %s pin cannot have a ’%s’ attribute.

DESCRIPTION

This message indicates that you specified a pad pin attribute on a pin with an invalid direction.

WHAT NEXT

Refer to the "Library Compiler User Guide" for information on pad cells. Either change the pin’s direction or move the attribute to the correct pin.

EXAMPLES

```
  cell(lbdb204){
    area : 0.0;
    pad_cell : true;
    pin(Z)  {
      direction : output;
      is_pad : true;
      hysteresis : true;
      function : "A";
    }
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 3584, The ’Z’ output pin cannot have a ’hysteresis’ attribute. (LBDB-
204)
```

LBDB-205 (warning) The ’%s’ pad pin is missing a ’%s’ attribute.

DESCRIPTION

This message indicates that you specified an output or inout pad pin without a **drive_current** attribute.

WHAT NEXT

Refer to the "Library Compiler User Guide" for information on pad cells and pins. Add the missing attribute to the pin.

EXAMPLES

```
cell(lbdb205){
  area : 0.0;
  pad_cell : true;
  pin(Z)  {
    direction : output;
    is_pad : true;
    hysteresis : true;
    function : "A";
  }
  pin(A) {
    direction : input;
    capacitance : 1.0;
  }
}
```

EXAMPLE MESSAGE

Warning: Line 3596, The ’Z’ pad pin is missing a ’drive_current’ attribute. (LBDB-205)

LBDB-206 (error) The ’%s’ pad cell has no pad pins.

DESCRIPTION

This message indicates that you specified a pad cell with pad_type and pad_cell attributes defined but you did not specify pad pin attributes associated with any pin in the cell.

WHAT NEXT

Refer to the "Library Compiler User Guide" for information on pad cells. Remove either the pad cell attributes or add the pad pin attributes.

EXAMPLES

```
cell(lbdb206){
  area : 0.0;
  pad_type : clock;
  pad_cell : true;
  pin(Z)  {
    direction : output
    function : "A"
  }
  pin(A) {
    direction : input;
    capacitance : 1.0;
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 3575, The 'lbdb206' pad cell has no pad pins. (LBDB-206)
```

LBDB-207 (warning) The '%s' pad cell has more than one pad pin.

DESCRIPTION

This message indicates that you specified more than one pad pin in a pad cell.

WHAT NEXT

Refer to the "Library Compiler User Guide" for information on pad cells.

EXAMPLES

```
cell(lbdb207) {
  area : 0.0;
  pad_cell : true;
  bond_pads : 1;
  driver_sites : 1;
  pin(PAD ) {
    direction : input;
    is_pad : true;
    input_voltage : CMOS;
    capacitance : 1.0;
  }
  pin(PAD1 ) {
    direction : input;
    is_pad : true;
```

```
      input_voltage : CMOS;
      capacitance : 1.0;
    }
    pin(Y ) {
      direction : output;
      function : "PAD PAD1";
      timing() {
intrinsic_fall : 1.0;
intrinsic_rise : 1.0;
fall_resistance : 0.50;
rise_resistance : 0.50;
related_pin :"PAD PAD1";
      }
    }
  }
```

In this case, there are two pad pins: ’PAD’ and ’PAD1’.

EXAMPLE MESSAGE

```
Warning: Line 33, The ’lbdb207’ pad cell has more than one pad pin. (LBDB-207)
```

LBDB-208 (error) The %s ’%s’ pad cell cannot be a ’clock’ pad.

DESCRIPTION

This message indicates you specified an output pad pin with the is_pad attribute on a clock pad. Library Compiler accepts clock pads only on input pins.

WHAT NEXT

Refer to the "Library Compiler User Guide" for information on pad cells. Check the library source file, and specify the is_pad attribute to an input pin.

EXAMPLES

```
  cell(lbdb208) {
    area : 0.0;
    pad_cell : true;
    pad_type : clock;
    pin(PAD ) {
      direction : input;
      capacitance : 1.0;
    }
    pin(Y ) {
      direction : output;
      is_pad : true;
      function : "PAD";
      output_voltage : CMOS_OUT;
      timing() {
```

```
intrinsic_fall : 1.0;
intrinsic_rise : 1.0;
fall_resistance : 0.0;
rise_resistance : 0.0;
related_pin :"PAD";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 65, The output 'lbdb208' pad cell cannot be a 'clock' pad. (LBDB-208)
```

LBDB-209 (error) A '%s' attribute cannot be specified on a pin unless a pull_up or pull_down driver_type is specified.

DESCRIPTION

This message indicates that you specified a **pulling_resistance** or a **pulling_current** attribute on a pin without specifying the pullup or pulldown driver type.

WHAT NEXT

Change the library file by either adding the driver_type attribute to the specified pin or removing the pulling_resistance or pulling_current attribute.

EXAMPLES

```
    pin(A) {
      direction : output;
      pulling_resistance : 100;
      ...
    }
```

In this case, the driver_type is missing. To fix the problem, add the statement,

```
   driver_type : pull_up;
```

EXAMPLE MESSAGE

```
Error: Line 355, A 'pulling_resistance' attribute cannot be specified on a
       pin unless a pull_up or pull_down driver_type is specified. (LBDB-209)
```

LBDB-210 (error) The pulling_current value cannot be 0.0.

DESCRIPTION

This message indicates that you specified a zero value for the **pulling_current** attribute.

WHAT NEXT

Change the value of the attribute to a nonzero value.

EXAMPLES

```
      pulling_current : 0.0;
```

EXAMPLE MESSAGE

```
Error: Line 357, The pulling_current value cannot be 0.0. (LBDB-210)
```

LBDB-211 (error) The '%s' driver_type cannot be specified on a pin that already has a %s driver_type specified.

DESCRIPTION

This message indicates that you specified an incompatible set of driver types on a pin. Library Compiler fails if the driver_type value includes the following combinations:

* pull_up and pull_down
* pull_up and bus_hold
* pull_down and bus_hold
* open_drain and open_source
* open_drain and bus_hold
* open_source and bus_hold

WHAT NEXT

Refer to the "Library Compiler User Guide" for driver_type information. Remove the incompatible values of the driver_type attribute.

EXAMPLES

```
  cell(lbdb211) {
    area : 2;
    pin(A) {
      direction : input;
```

```
      capacitance : 1.0;
    }
    pin(Z2) {
      direction : output;
      function : "A";
      driver_type : "pull_up pull_down";
      timing() {
intrinsic_rise : 0.1;
intrinsic_fall : 0.1;
related_pin : "A";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 84, The 'pull_down' driver_type cannot be specified on a
       pin that already has a 'pull_up' driver_type specified. (LBDB-211)
```

LBDB-212 (error) The 'open_%s' driver_type cannot be specified on an input pin.

DESCRIPTION

This message indicates that you specified an invalid **open_source** or **open_drain** driver_type value on an input_pin.

WHAT NEXT

Refer to the "Library Compiler User Guide" for driver_type information. Remove the invalid value of the driver_type attribute.

EXAMPLES

```
  cell(lbdb212) {
    area : 2;
    pin(A) {
      direction : input;
      capacitance : 1.0;
      driver_type : "open_drain";
    }
    pin(Z2) {
      direction : output;
      function : "A";
      timing() {
intrinsic_rise : 0.1;
intrinsic_fall : 0.1;
```

```
related_pin : "A";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 78, The 'open_drain' driver_type cannot be specified on
       an input pin. (LBDB-212)
```

LBDB-213 (error) The '%s' area attribute cannot be specified on a pin of a cell that is not a pad cell.

DESCRIPTION

This message indicates that you specified a user-defined cell area value for pad cells and applied it to a nonpad cell.

WHAT NEXT

Change the library file, and either make the cell a pad cell or remove the pad information from the cell.

EXAMPLES

```
define_cell_area(my_area,pad_slots);

cell(NON_PAD_CELL) {
  area : 1;
  my_area : 10;
}
```

EXAMPLE MESSAGE

```
Error: Line 29, The 'my_area' area attribute cannot be specified
       on a pin of a cell that is not a pad cell. (LBDB-213)
```

LBDB-214 (error) The '%s' area attribute of '%s' type cannot be specified on a pin of a cell that is not a pad cell

or an auxiliary pad cell.

DESCRIPTION

This message indicates that you specified a user-defined cell area value for pad cells or auxiliary pad cells and applied it to a nonpad cell.

WHAT NEXT

Change the library file and either make the cell a pad cell or remove the pad information from the cell.

EXAMPLES

```
define_cell_area(your_area,pad_driver_sites);

cell(NON_PAD_CELL) {
  area : 1;
  your_area : 10;
}
```

EXAMPLE MESSAGE

```
Error: Line 29, The 'your_area' area attribute of 'pad_driver_sites' type
       cannot be specified on a pin of a cell that is not a pad cell
       or an auxiliary pad cell. (LBDB-214)
```

LBDB-215 (error) The '%s' attribute cannot be specified on the '%s' input pin.

DESCRIPTION

This message indicates that you specified an invalid attribute on an input pin. Library Compiler fails if the following attributes are associated with an input pin.

* A driver_type attribute whose value is bus_hold
* A slew_control attribute
* An edge_rate_rise attribute
* An edge_rate_fall attribute
* An edge_rate_rise_load attribute
* An edge_rate_fall_load attribute
* A reference_resistance attribute

WHAT NEXT

Check the library source file, and delete the invalid attribute from the input pin.

EXAMPLES

```
pin(B) {
   direction : input;
   capacitance : 1.0;
   fanout_load : 1.0;

   edge_rate_breakpoint_r0 : 0.000;
   edge_rate_breakpoint_f0 : 0.000;
   edge_rate_breakpoint_r1 : 0.010;
   edge_rate_breakpoint_f1 : 0.010;

   edge_rate_rise : 1.0;
   edge_rate_load_rise : 1.0;
   edge_rate_fall     : 1.0;
   edge_rate_load_fall : 1.0;
}
```

EXAMPLE MESSAGE

```
Error: Line 110, The 'edge_rate_rise' attribute cannot be specified
       on the 'B' input pin. (LBDB-215)
```

LBDB-216 (error) The '%s' scaled_cell's '%s' pin has a different number of timing arcs than the corresponding pin on the '%s' cell.

DESCRIPTION

This message indicates that a timing group is missing in one of the output pins of either the specified cell or the scaled_cell.

WHAT NEXT

Add the missing timing group to the specified output pin in either the cell or the scaled_cell.

EXAMPLES

```
library(lbdb216) {
    operating_conditions(WCCOM) {
process : 1.5 ;
        temperature : 70 ;
voltage : 4.75 ;
tree_type : "worst_case_tree" ;
    }
    cell(IVV) {
      area : 1;
```

```
      pin(A) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "A'";
timing() {
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A";
}
      }
    }

    scaled_cell(IVV,WCCOM) {
      area : 1;
      pin(A) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "A'";
      }
    }
  }
```

In this case, add the following timing group to the 'Z' pin in the scaled_cell to fix the problem.

```
timing() {
  intrinsic_rise : 0.3;
  intrinsic_fall : 0.3;
  rise_resistance : 0.3;
  fall_resistance : 0.3;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A";
}
```

EXAMPLE MESSAGE

```
Error: Line 40, The 'WCCOM' scaled_cell's 'Z' pin has a different
       number of timing arcs than the corresponding pin on the 'IVV' cell. (LBDB-
216)
```

LBDB-217 (error) The '%s' cell's '%s' pin has a timing arc

without
a counterpart on the scaled_cell(%s,%s).

DESCRIPTION

Each timing arc in the regular cell needs a matched timing arc on the same pin in the scaled_cell group. This message indicates that a matching timing arc is not found in the library source file.

WHAT NEXT

Find the missing timing group in the scaled_cell and add it, or remove one of the extra timing groups in the cell.

EXAMPLES

```
library(lbdb217) {
    operating_conditions(WCCOM) {
process : 1.5 ;
        temperature : 70 ;
voltage : 4.75 ;
tree_type : "worst_case_tree" ;
    }
    cell(AND) {
      area : 1;
      pin(A B) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "A B";
timing() {
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A B";
}
      }
    }

    scaled_cell(AND,WCCOM) {
      area : 1;
      pin(A B) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
```

```
direction : output;
function : "A B";
timing() {
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A";
}
timing() {
  intrinsic_rise : 0.3;
  intrinsic_fall : 0.3;
  rise_resistance : 0.3;
  fall_resistance : 0.3;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A ";
        }
      }
    }
  }
```

In this case, The timing arc between ’Z’ and ’A’ is defined once in the ’AND’ cell and twice in the ’AND’ scaled_cell. To fix the problem, remove one of the timing arcs.

EXAMPLE MESSAGE

```
Error: Line 42, The ’AND’ cell’s ’Z’ pin has a timing arc without
       a counterpart on the scaled_cell(AND,WCCOM). (LBDB-217)
```

LBDB-218 (warning) The ’direction’ of the ’%s’ scaled_cell pin does not match that of the same pin name on the ’%s’ cell. Resetting the scaled_cell pin’s direction to match both directions.

DESCRIPTION

This message indicates that a direction attribute of a scaled_cell pin is different from the same pin on the primary cell. Library Compiler matches the direction of the scaled_cell pin to the direction of the primary pin.

WHAT NEXT

Check the library source file, and make sure the directions are the same.

EXAMPLES

```
  cell(AND) {
    area : 1;
    pin(A B C) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : inout;
      function : "A B";
      three_state : "C";
      timing() {
intrinsic_rise : 0.1;
intrinsic_fall : 0.1;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "A B C";
      }
      timing() {
timing_type : three_state_disable;
intrinsic_rise : 0.1;
intrinsic_fall : 0.1;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "C";
      }
    }
    }
    scaled_cell(AND,WCCOM) {
      area : 1;
      pin(A B C) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "A B";
timing() {
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A B";
}
      }
   }
```

EXAMPLE MESSAGE

```
Warning: Line 313, The 'direction' of the 'Z' scaled_cell pin
         does not match that of the same pin name on the 'AND' cell.
         Resetting the scaled_cell pin's direction to match both directions. (LBDB-
```

218)

LBDB-219 (error) The (%s,%s) scaled_cell has duplicate timing arcs for the '%s' pin. It is unclear which arc corresponds to the arcs in the '%s' cell.

DESCRIPTION

This message indicates that a scaled_cell has duplicate timing arcs between two pins. Library Compiler fails to recognize the equivalent timing arc in the primary cell.

WHAT NEXT

Check the library source file, and remove the second timing arc.

LBDB-220 (error) The '%s' %s_voltage group has no '%s' attribute specified. This attribute is essential in defining valid voltages.

DESCRIPTION

This message indicates that an input_voltage or an output_voltage group has one of its attributes missing. For an input_voltage group, Library Compiler fails if any of the vil, vih, vimin, or vimax attributes is missing. For an output_voltage group, Library Compiler fails if any of the vol, voh, vomin, or vomax attributes is missing.

WHAT NEXT

Check the library source file, and add the missing attribute to the voltage group.

EXAMPLES

```
output_voltage(CMOS_OUT) {
  vil : 1.5;
  vih : 3.5;
  vimin : -0.3;
  vimax : VDD + 0.3;
}
```

In this case, either there is a typo where the output_voltage is specified instead of input_voltage, or the vol, voh, vomin, and vomax are not specified for the

output_voltage.

EXAMPLE MESSAGE

```
Error: Line 31, The 'CMOS_OUT' output_voltage group has no 'vol' attribute
       specified. This attribute is essential in defining valid voltages. (LBDB-220)
```

LBDB-221 (warning) The '%s' %s_voltage group has a %s value, which is %s %s.

DESCRIPTION

This message indicates that an **input_voltage** or an **output_voltage** has inconsistent values for its attributes. Library Compiler issues warnings in these cases:

* vil value is less than vimin value.
* vih value is greater than vimax value.
* vol value is less than vomin value.
* voh value is greater than vomax value.

WHAT NEXT

Change the specified attribute value to be consistent with the minimum or the maximum values.

EXAMPLES

```
  input_voltage(CMOS) {
    vil : -1.5;
    vih : 3.5;
    vimin : -0.3;
    vimax : VDD + 0.3;
  }
```

In this case, the vil value is less than the vimin value.

EXAMPLE MESSAGE

```
Warning: Line 25, The 'CMOS' input_voltage group has a vil value,
        which is less than vimin. (LBDB-221)
```

LBDB-222 (error) The fpga_family attribute is required when

the fpga_cell_type attribute is specified.

DESCRIPTION

This message indicates that in an fpga cell you specified an **fpga_cell_type** attribute without the **fpga_family** attribute.

WHAT NEXT

Add the missing fpga_family attribute to the cell.

EXAMPLES

```
    cell( lbdb222 ) {
area : 1;
fpga_cell_type : CLB;

pin( K ) {
    direction : input;
    capacitance : 0.0;
}
...
    }
```

In this case, to fix the problem, add the statement to the cell.

```
fpga_family : "x4000";
```

EXAMPLE MESSAGE

```
Error: Line 28, The fpga_family attribute is required when
the fpga_cell_type attribute is specified. (LBDB-222)
```

LBDB-223 (error) The fpga_cell_type attribute is required when the fpga_family attribute is specified.

DESCRIPTION

This message indicates that in an fpga cell you specified an **fpga_family** attribute without the **fpga_cell_type** attribute.

WHAT NEXT

Add the missing fpga_cell_type attribute to the cell.

EXAMPLES

```
    cell(lbdb223) {
area : 1;
fpga_family : "x4000";

pin( K ) {
    direction : input;
    capacitance : 0.0;
}
...
    }
```

In this case, to fix the problem, add the statement to the cell.

```
fpga_cell_type : CLB;
```

EXAMPLE MESSAGE

```
Error: Line 28, The fpga_cell_type attribute is required when
the fpga_familyattribute is specified. (LBDB-222)
```

LBDB-224 (error) The fpga_timing_type is required on all arcs when fpga_cell_type and fpga_family are specified.

DESCRIPTION

This message indicates that you did not specify **fpga_timing_type** groups in a cell with the **fpga_family** and the **fpga_cell_type** attributes.

WHAT NEXT

Add the missing fpga_timing_type groups to all the pins of the cell.

EXAMPLES

```
    cell(INV) {
      fpga_family : "x4000";
      fpga_cell_type : CLB;
      area : 1;
      pin(X) {
function : "A'";
direction : output;
timing() {
  intrinsic_rise  : 0.1;
  intrinsic_fall  : 0.1;
  rise_resistance : 1.0;
  fall_resistance : 1.0;
  related_pin : "A";
```

```
}
      }
      pin(A) {
direction : input;
capacitance :  0.1;
fanout_load :  0.1;
      }
    }
```

To fix the problem, add the attribute to the timing group.

```
timing() {
  fpga_timing_type : ICK;
  intrinsic_rise  : 0.1;
  intrinsic_fall  : 0.1;
  rise_resistance : 1.0;
  fall_resistance : 1.0;
  related_pin : "A";
}
```

EXAMPLE MESSAGE

```
Error: Line 208, The fpga_timing_type is required on all arcs
when fpga_cell_type and fpga_family are specified. (LBDB-224)
```

LBDB-225 (error) The fpga_timing_type is invalid when the fpga_cell_type and the fpga_family attributes are not defined on a cell.

DESCRIPTION

This message indicates that you specified fpga_timing_type in a timing group of a pin without defining the fpga_family and the fpga_cell_type attributes at the cell level.

WHAT NEXT

Add the missing attribute to the library file.

EXAMPLES

```
    cell(lbdb225) {
      area : 1;
      pin(X) {
function : "A'";
direction : output;
timing() {
  fpga_timing_type : ICK;
```

```
  intrinsic_rise  : 0.1;
  intrinsic_fall  : 0.1;
  rise_resistance : 1.0;
  fall_resistance : 1.0;
  related_pin : "A";
}
      }
      pin(A) {
direction : input;
capacitance :  0.1;
fanout_load :  0.1;
      }
    }
```

To fix the problem, add the sample statements at the cell level.

```
      fpga_family : "x4000";
      fpga_cell_type : CLB;
```

EXAMPLE MESSAGE

```
Error: Line 30, The fpga_timing_type is invalid when the fpga_cell_type
and the fpga_family attributes are not defined on a cell. (LBDB-225)
```

LBDB-226 (error) The FPGA CLB cell type from the x2000 family requires A, B, C, D, K, X, and Y pins.

DESCRIPTION

This message indicates that you specified an incomplete CLB FPGA cell with missing pins from the x2000 family.

WHAT NEXT

Add the missing pins to the cell.

EXAMPLES

```
    cell(lbdb226) {
      fpga_family : "x2000";
      fpga_cell_type : CLB;
      area : 1;
      pin(X) {
function : "A'";
direction : output;
timing() {
  fpga_timing_type : ICK;
```

```
  intrinsic_rise  : 0.1;
  intrinsic_fall  : 0.1;
  rise_resistance : 1.0;
  fall_resistance : 1.0;
  related_pin : "A";
}
      }
      pin(A) {
direction : input;
capacitance :  0.1;
fanout_load :  0.1;
      }
    }
```

EXAMPLE MESSAGE

```
Error: Line 22, The FPGA CLB cell type from the x2000 family requires
        A, B, C, D, K, X, and Y pins. (LBDB-226)
```

LBDB-227 (error) The FPGA IOB cell type from the x2000 family requires
O, T, K, I, and PAD pins.

DESCRIPTION

This message indicates that you specified an incomplete IOB FPGA cell with missing pins from the x2000 family.

WHAT NEXT

Add the missing pins to the cell.

EXAMPLES

```
    cell(lbdb227) {
      fpga_family : "x2000";
      fpga_cell_type : IOB;
      area : 1;
      pin(X) {
function : "A'";
direction : output;
timing() {
  fpga_timing_type : ICK;
  intrinsic_rise  : 0.1;
  intrinsic_fall  : 0.1;
  rise_resistance : 1.0;
  fall_resistance : 1.0;
  related_pin : "A";
```

```
}
      }
      pin(A) {
direction : input;
capacitance :  0.1;
fanout_load :  0.1;
      }
    }
```

EXAMPLE MESSAGE

```
Error: Line 22, The FPGA IOB cell type from the x2000 family requires
        O, T, K, I, and PAD pins. (LBDB-227)
```

LBDB-228 (error) The FPGA CLB cell type from the x3000 family requires A, B, C, D, E, K, EC, DI, RD, X, Y, and GSR pins.

DESCRIPTION

This message indicates that you specified an incomplete CLB FPGA cell with missing pins from the x3000 family.

WHAT NEXT

Add the missing pins to the cell.

EXAMPLES

```
    cell(lbdb228) {
      fpga_family : "x3000";
      fpga_cell_type : CLB;
      area : 1;
      pin(X) {
function : "A'";
direction : output;
timing() {
  fpga_timing_type : ICK;
  intrinsic_rise  : 0.1;
  intrinsic_fall  : 0.1;
  rise_resistance : 1.0;
  fall_resistance : 1.0;
  related_pin : "A";
}
      }
      pin(A) {
direction : input;
capacitance :  0.1;
```

```
fanout_load :  0.1;
      }
    }
```

EXAMPLE MESSAGE

```
Error: Line 22, The FPGA CLB cell type from the x3000 family requires
        A, B, C, D, E, K, EC, DI, RD, X, Y, and GSR pins. (LBDB-228)
```

LBDB-229 (error) The FPGA IOB cell type from the x3000 family requires
O, T, IK, OK, I, Q, PAD, and GSR pins.

DESCRIPTION

This message indicates that you specified an incomplete IOB FPGA cell with missing pins from the x3000 family.

WHAT NEXT

Add the missing pins to the cell.

EXAMPLES

```
    cell(lbdb229) {
      fpga_family : "x3000";
      fpga_cell_type : IOB;
      area : 1;
      pin(X) {
function : "A'";
direction : output;
timing() {
  fpga_timing_type : ICK;
  intrinsic_rise  : 0.1;
  intrinsic_fall  : 0.1;
  rise_resistance : 1.0;
  fall_resistance : 1.0;
  related_pin : "A";
}
      }
      pin(A) {
direction : input;
capacitance :  0.1;
fanout_load :  0.1;
      }
    }
```

EXAMPLE MESSAGE

```
Error: Line 22, The FPGA IOB cell type from the x3000 family requires
        O, T, IK, OK, I, Q, PAD, and GSR pins. (LBDB-229)
```

LBDB-230 (error) The FPGA CLB cell type from the x4000 family requires F1-F4, G1-G4, C1-C4, K, X, Y, XQ, YQ, GSR, CIN, and COUT pins.

DESCRIPTION

This message indicates that you specified an incomplete CLB FPGA cell with missing pins from the x4000 family.

WHAT NEXT

Add the missing pins to the cell.

EXAMPLES

```
    cell(lbdb230) {
      fpga_family : "x4000";
      fpga_cell_type : CLB;
      area : 1;
      pin(X) {
function : "A'";
direction : output;
timing() {
  fpga_timing_type : ICK;
  intrinsic_rise  : 0.1;
  intrinsic_fall  : 0.1;
  rise_resistance : 1.0;
  fall_resistance : 1.0;
  related_pin : "A";
}
      }
      pin(A) {
direction : input;
capacitance :  0.1;
fanout_load :  0.1;
      }
    }
```

EXAMPLE MESSAGE

```
Error: Line 22, The FPGA CLB cell type from the x4000 family requires
        F1-F4, G1-G4, C1-C4, K, X, Y, XQ, YQ, GSR, CIN, and COUT pins. (LBDB-230)
```

LBDB-231 (error) The FPGA IOB cell type from the x4000 family requires
O, T, IK, OK, I1, I2, PAD, and GSR pins.

DESCRIPTION

This message indicates that you specified an incomplete IOB FPGA cell with missing pins from the x4000 family.

WHAT NEXT

Add the missing pins to the cell.

EXAMPLES

```
    cell(lbdb231) {
      fpga_family : "x4000";
      fpga_cell_type : IOB;
      area : 1;
      pin(X) {
function : "A'";
direction : output;
timing() {
  fpga_timing_type : ICK;
  intrinsic_rise  : 0.1;
  intrinsic_fall  : 0.1;
  rise_resistance : 1.0;
  fall_resistance : 1.0;
  related_pin : "A";
}
      }
      pin(A) {
direction : input;
capacitance :  0.1;
fanout_load :  0.1;
      }
    }
```

EXAMPLE MESSAGE

```
Error: Line 22, The FPGA IOB cell type from the x4000 family requires
        O, T, IK, OK, I1, I2, PAD, and GSR pins. (LBDB-231)
```

LBDB-235 (error) This %s voltage or power supply group is not

defined.

DESCRIPTION

This message indicates the specified voltage or the power supply associated with the signal level is not defined in the library source file. The voltage can either be input or output.

WHAT NEXT

Add the missing voltage or the power supply to the library file.

EXAMPLES

```
      pin(PAD ) {
is_pad : true;
input_voltage : lbdb235;
direction   : input;
capacitance : 35.000000;
fanout_load : 0.000000;
      }
      pin(PAD1 ) {
is_pad : true;
input_signal_level : VDD1;
direction   : input;
capacitance : 35.000000;
fanout_load : 0.000000;
      }
```

In this case, the 'lbdb235' input_voltage is not defined. To fix the problem, add the following input_voltage:

```
  input_voltage(lbdb235) {
    vil         : 0.8 ;
    vih         : 2.0 ;
    vimin       : -0.3 ;
    vimax       : VDD + 0.3 ;
   }
```

In addition, the 'VDD1' input_signal_level is not defined. To fix the problem, add the following power_supply group:

```
  power_supply() {
    default_power_rail : VDD0;
    power_rail (VDD1, 5.0);
   }
```

EXAMPLE MESSAGE

```
Error: Line 23, This input voltage or power supply group is not defined. (LBDB-235)
Error: Line 30, This input voltage or power supply group is not defined. (LBDB-235)
```

LBDB-236 (error) An %s pin cannot specify an %s attribute.

DESCRIPTION

This message indicates that there is a mismatch between the direction of a pin and the voltage attribute. Library Compiler fails if you specify an input_voltage to an output pin and an output_voltage to an input pin.

WHAT NEXT

Check the library source file, and fix the invalid attribute, either the direction of the pin or the voltage attribute.

EXAMPLES

```
  cell(lbdb236) {
    area : 0.0;
    pad_cell : true;
    pad_type : clock;
    pin(PAD ) {
      direction : input;
      is_pad : true;
      input_voltage : CMOS;
      capacitance : 1.0;
    }
    pin(Y ) {
      direction : output;
      is_pad : true;
      function : "PAD";
      input_voltage : CMOS;
      timing() {
intrinsic_fall : 1.0;
intrinsic_rise : 1.0;
fall_resistance : 0.1;
rise_resistance : 0.1;
related_pin :"PAD";
      }
    }
  }
```

In this case, the ’Y’ pin has an input_voltage specified. To fix the problem, change the voltage to an output_voltage attribute.

EXAMPLE MESSAGE

Error: Line 71, An output pin cannot specify an input_voltage attribute. (LBDB-236)

LBDB-238 (warning) No ’%s’ attribute has been specified for the

library. This attribute is needed in %s libraries.

DESCRIPTION

This message indicates that you did not specify any of the following attributes in the technology library.

* time_unit
* capacitance_load_unit
* pulling_resistance_unit
* voltage_unit
* current_unit

WHAT NEXT

Add the missing attribute to the library source file.

EXAMPLES

Add any of the following examples of attributes to the library:

```
capacitive_load_unit(0.042000,pf) ;
voltage_unit  : "1V";
current_unit  : "1mA";
pulling_resistance_unit : "1kohm";
time_unit : "1ns";
```

EXAMPLE MESSAGE

```
Warning: No 'capacitive_load_unit' attribute has been specified for the
         library. This attribute is needed in technology libraries. (LBDB-238)
```

LBDB-239 (error) The '%s' driver_type cannot coexist with the '%s' attribute on the '%s' pin.

DESCRIPTION

The **driver_type** specified in the pin cannot coexist with the attribute on the same pin. For example, a pin with a **bus_hold driver_type** is tied to a DC source. A function attribute or **three_state** attribute cannot be specified on a **bus_hold** pin.

WHAT NEXT

Check the specification of the cell, and make the appropriate change to the **driver_type** attribute or other attributes in the faulty pin group.

EXAMPLES

```
  cell(lbdb239) {
    area : 2;
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
    pin(Z2) {
      direction : output;
      function : "A";
      driver_type : "bus_hold";
      timing() {
intrinsic_rise : 0.1;
intrinsic_fall : 0.1;
related_pin : "A";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 84, The  'bus_hold' driver_type cannot coexist
        with the 'function' attribute on the 'Z2' pin. (LBDB-239)
```

LBDB-240 (error) The '%s' cell area attribute has already been defined.

DESCRIPTION

This message indicates that the user-defined cell area is specified twice.

WHAT NEXT

Remove the second definition of the cell area attribute.

EXAMPLES

```
    define_cell_area(my_area,pad_slots);
    define_cell_area(my_area,pad_slots);
```

EXAMPLE MESSAGE

```
Error: Line 24, The 'my_area' cell area attribute has already been defined. (LBDB-
240)
```

LBDB-241 (warning) Multiple cell area definitions (%s, %s) map onto the same '%s' area. Using the last one encountered.

DESCRIPTION

This message indicates that you specified multiple defined_cell_area attributes with the same area kind. Library Compiler uses the last one encountered.

WHAT NEXT

Delete the redundant define_cell_area definitions.

EXAMPLES

```
define_cell_area(my_area,pad_slots);
define_cell_area(your_area,pad_slots);
```

EXAMPLE MESSAGE

```
Warning: Line 24, Multiple cell area definitions (your_area, my_area) map
onto the same 'pad_slots' area. Using the last one encountered. (LBDB-241)
```

LBDB-242 (warning) This '%s' timing arc has the same timing_type and related_pin attributes as the timing arc on the line %d.

DESCRIPTION

This message indicates that on the same pin you defined two timing groups with the same timing_type and related_pin attributes. Design Compiler considers the timing arcs as two separate arcs.

WHAT NEXT

If it is a typo, change the library file, and delete the redundant timing groups.

EXAMPLES

```
pin(QN) {
  direction : output;
  function : "IQN";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
```

```
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 2.0;
      intrinsic_fall : 2.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP P";
    }
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
```

In this case, the 'QN' pin has the 'CP' related_pin and the 'rising_edge' timing_type multiply defined.

EXAMPLE MESSAGE

```
Warning: Line 591, This 'QN' timing arc has the same timing_type and
         related_pin attributes as the timing arc on the line 583. (LBDB-242)
```

LBDB-243 (warning) The '%s' combinational cell has a '%s' pin with a sequential timing arc containing the '%s' timing_type.

DESCRIPTION

This message indicates that you specified one of the cell's timing arcs as sequential, while the function of this cell is combinational. Library Compiler warns you if any of the following timing types is defined on a combinational cell:

* rising_edge
* falling_edge
* preset
* clear
* setup_rising
* setup_falling
* hold_rising
* hold_falling
* recovery_rising

```
* recovery_falling
* skew_rising
* skew_falling
* removal_rising
* removal_falling
```

WHAT NEXT

Change the library source file, and fix the timing_type of the specified pin.

EXAMPLES

```
  cell(lbdb243) {
    area : 1;
    pin(A B) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "A B";
      timing() {
timing_type : rising_edge;
intrinsic_rise : 0.1;
intrinsic_fall : 0.1;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "A B";
      }
    }
  }
```

In this case, the ’Z’ pin has an invalid ’rising_edge’ timing_type.

EXAMPLE MESSAGE

```
Warning: Line 84, The ’lbdb243’ combinational cell has a ’Z’ pin with
         a sequential timing arc containing the ’rising_edge’ timing_type. (LBDB-
243)
```

LBDB-246 (warning) The default_wire_load_selection is not defined.
By default, the ’%s’ wire_load_selection group is used.

DESCRIPTION

The **default_wire_load_selection** attribute is undefined in this library. The **default_wire_load_selection** attribute is required when multiple wire_load_selection

groups are specified in a library. If there is only one wire_load_selection group defined in a library, Library Compiler automatically sets the **default_wire_load_selection** attribute to the only available wire_load_selection group.

WHAT NEXT

Set the **default_wire_load_selection** attribute to avoid this warning message, or ignore this message.

EXAMPLES

```
wire_load("05x05") {
  resistance : 0 ;
  capacitance : 1 ;
  area : 0 ;
  slope : 0.186 ;
  fanout_length(1,0.39) ;
}
wire_load_selection(test) {
  wire_load_from_area(27,10,"10x10");
  wire_load_from_area(27,100,"10x10");
  wire_load_from_area(0,28,"05x05");
  wire_load_from_area(2,10,"15x10");
}
```

EXAMPLE MESSAGE

```
Warning: Line 50, The default_wire_load_selection is not defined.
        By default, the 'test' wire_load_selection group is used. (LBDB-246)
```

LBDB-247 (error) The default_wire_load_selection is not defined.
The default_wire_load_selection attribute is required when more than one
wire_load_selection group is specified.

DESCRIPTION

The **default_wire_load_selection** attribute is undefined in this library. Library Compiler requires this attribute because there is more than one wire_load_selection group specified.

WHAT NEXT

Set the **default_wire_load_selection** attribute to be one of the wire_load_selection

groups.

EXAMPLES

```
  wire_load("05x05") {
    resistance : 0 ;
    capacitance : 1 ;
    area : 0 ;
    slope : 0.186 ;
    fanout_length(1,0.39) ;
  }

  wire_load_selection(test) {
    wire_load_from_area(0,25,"05x05");
  }
  wire_load_selection(test1) {
    wire_load_from_area(0,27,"05x05");
  }
```

To fix the problem, add this statement to the library:

```
  default_wire_load_selection : test;
```

EXAMPLE MESSAGE

```
Error: Line 0, The default_wire_load_selection is not defined.
        The default_wire_load_selection attribute is required when more than one
        wire_load_selection group is specified. (LBDB-247)
```

LBDB-250 (warning) The ’%s’ pin already has a ’pulling_resistance’ value.
The ’pulling_current’ causes the ’pulling_resistance’ value to be overwritten.

DESCRIPTION

This message indicates you specified both the **pulling_resistance** and the **pulling_current** attributes on the same pin. Library Compiler uses the pulling_current value and the nominal voltage to overwrite the pulling_resistance value.

WHAT NEXT

If you do not want the pulling_resistance value overwritten, delete the pulling_current attribute.

EXAMPLES

```
      pin(Y) {
direction : output;
capacitance : 1.0;
driver_type : pull_up;
is_pad : true;
slew_control : low;
drive_current : 1.0;
output_voltage  : CMOS_OUT;
function : "A";
three_state : "GZ";
pulling_resistance : 1000;
pulling_current : 10;
     }
```

EXAMPLE MESSAGE

```
Warning: Line 93, The 'Y' pin already has a 'pulling_resistance' value.
The 'pulling_current' causes the 'pulling_resistance' value to be overwritten. (LBD
B-250)
```

LBDB-251 (warning) The '%s' pin has a 'hysteresis' attribute but no 'input_voltage' attribute. Both attributes are needed.

DESCRIPTION

This message indicates that you specified the hysteresis attribute, but you did not specify the input_voltage attribute in a pad cell.

WHAT NEXT

Add the input_voltage attribute to the pin in the pad cell.

EXAMPLES

```
    pin(PAD ) {
      direction : input;
      is_pad : true;
      hysteresis : true;
      capacitance : 1.0;
    }
```

To fix the problem, add this statement to the 'PAD' pin:

```
     input_voltage : CMOS; /* CMOS is defined in the library */
```

EXAMPLE MESSAGE

```
Warning: Line 53, The 'PAD' pin has a 'hysteresis' attribute but
no 'input_voltage' attribute. Both attributes are required. (LBDB-251)
```

LBDB-252 (error) The '%s' %s group already exists and cannot be overwritten.

DESCRIPTION

This message indicates that you multiply defined either an input_voltage or an output_voltage group. Library Compiler does not allow the overwriting of existing voltage groups.

WHAT NEXT

Delete the second specification of the voltage group.

EXAMPLES

```
input_voltage(CMOS) {
  vil : 1.5;
  vih : 3.5;
  vimin : -0.3;
  vimax : VDD + 0.3;
}

input_voltage(CMOS) {
  vil : 2.5;
  vih : 4.5;
  vimin : -0.3;
  vimax : VDD + 0.3;
}
```

EXAMPLE MESSAGE

```
Error: Line 31, The 'CMOS' input_voltage group already exists and
       cannot be overwritten. (LBDB-252)
```

LBDB-253 (error) The '%s' pin does not have all the %s slew rate attributes defined. The '%s' attribute is missing. All %s slew-rate attributes must be specified together as a

group.

DESCRIPTION

This message indicates that not all slew rate attributes are specified in a pin. Library Compiler expects the following rise slew rate attributes defined together:

* rise_current_slope_before_threshold
* rise_time_before_threshold
* rise_current_slope_after_threshold
* rise_time_after_threshold

and the following fall slew rate defined together:

* fall_current_slope_before_threshold
* fall_time_before_threshold
* fall_current_slope_after_threshold
* fall_time_after_threshold

WHAT NEXT

Check the library source file, and add the missing slew rate attribute.

EXAMPLES

```
  cell(lbdb253) {
    area : 0.0;
    pad_cell : true;
    bond_pads : 1;
    driver_sites : 1;
    pin(PAD) {
      is_pad : true;
      direction : output;
      output_voltage : CMOS_OUT;
      function : "Y ";
      drive_current : 1.0;
      slew_control : high;
      rise_time_before_threshold : 1.0;
      rise_current_slope_after_threshold : -0.1;
      rise_time_after_threshold : 1.0;
      fall_current_slope_before_threshold : -0.1;
      fall_time_before_threshold : 1.0;
      fall_current_slope_after_threshold : 0.1;
      fall_time_after_threshold : 1.0;
      timing() {
intrinsic_fall : 1.0;
intrinsic_rise : 1.0;
fall_resistance : 0.1;
rise_resistance : 0.1;
related_pin :"Y";
      }
    }
```

```
    pin(Y ) {
      direction : input;
      capacitance : 1.0;
    }
  }
```

In this case, the ’rise_current_slope_before_threshold’ attribute is not specified for the ’PAD’ pin.

EXAMPLE MESSAGE

```
Error: Line 88, The ’PAD’ pin does not have all the rise slew rate attributes
defined. The ’rise_current_slope_before_threshold’ attribute is missing.
All rise slew-rate attributes must be specified together as a group. (LBDB-253)
```

LBDB-254 (error) The ’%s’ edge rate related attribute cannot be specified on the ’%s’ output pin.

DESCRIPTION

This message indicates that you specified an edge rate attribute on an output pin.

WHAT NEXT

Delete the attribute from the output pin group.

EXAMPLES

```
         pin(Z) {
            direction : output;
            function : "(A & B)";
            max_fanout : 25;

            edge_rate_breakpoint_r0 : 0.0;
            edge_rate_breakpoint_f0 : 0.0;
            edge_rate_breakpoint_r1 : 0.1;
            edge_rate_breakpoint_f1 : 0.1;

            edge_rate_rise : 1.0;
            edge_rate_load_rise : 1.0;
            edge_rate_fall : 0.1;
            edge_rate_load_fall : 1.0;
}
```

EXAMPLE MESSAGE

```
Error: Line 120, The ’edge_rate_breakpoint_r0’ edge rate related attribute
```

cannot be specified on the ’Z’ output pin. (LBDB-254)

LBDB-255 (error) The ’vhdl_name’ attribute of ’%s’ is invalid VHDL or conflicts with another ’vhdl_name’ attribute.

DESCRIPTION

This message indicates that the cell or port **vhdl_name** attribute is either invalid VHDL (reserved VHDL name) or another cell or port has already been set to the same name.

WHAT NEXT

If the attribute is invalid VHDL, change the library by fixing the value of the vhdl_name attribute. If the value of the attribute is redundant, either delete the second attribute or change its value.

EXAMPLES

```
  cell(lbdb255) {
    area : 2;
    pin(A) {
      vhdl_name : "pinvhdl";
      direction : input;
      capacitance : 1;
    }
    pin(B) {
      vhdl_name : "pinvhdl" ;
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "A^B";
      timing() {
timing_sense : positive_unate;
intrinsic_rise : 0.1;
intrinsic_fall : 0.1;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "A";
      }
      timing() {
timing_sense : non_unate;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
```

```
related_pin : "A B";
      }
    }
  }
```

In this case, both the ’A’ and ’B’ pin have the same value in the vhdl_name attribute.

EXAMPLE MESSAGE

```
Error: Line 93, The ’vhdl_name’ attribute of ’pinvhdl’ is invalid VHDL or
        conflicts with another ’vhdl_name’ attribute. (LBDB-255)
```

LBDB-256 (warning) The ’vhdl_name’ attribute of ’%s’ is invalid VHDL or conflicts with another ’vhdl_name’ attribute. Renamed to ’%s’.

DESCRIPTION

This message indicates that the cell or port ’vhdl_name’ attribute is either invalid VHDL or another cell or port has already been set to the same name.

Because this is an update_lib cell, the name is automatically renamed to a valid one.

WHAT NEXT

Change the file to update by changing the value of the vhdl_name attribute if you are not satisfied with the renamed value.

EXAMPLES

```
cell (lbdb256) {
  area : 1;
  pin(IN) {
    vhdl_name : "port_X";
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    vhdl_name : "port_X";/* rename after warning */
    direction : output;
    function : "IN’";
    timing () {
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      rise_resistance : 0.1;
```

```
      fall_resistance : 0.1;
      related_pin : "IN";
    }
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 9, The 'vhdl_name' attribute of 'port_X' is invalid VHDL or
        conflicts with another 'vhdl_name' attribute. Renamed to 'port_Xb'. (LBDB-
256)
```

LBDB-257 (warning) The '%s' wire_load_selection group has been specified while the default_wire_load_mode is %s 'top'. This causes the 'wire_load_selection' group to work only for the top-level design.

DESCRIPTION

The 'default_wire_load_mode' is defined as, or defaults to, 'top', which causes the 'wire_load_selection' group to only work for the top-level design.

WHAT NEXT

Set the default_wire_load_mode to 'segmented' or 'enclosed' modes to work with wire_load_selection group.

EXAMPLES

```
  default_wire_load_mode : 'top';
  wire_load_selection(test) {
    wire_load_from_area(27,100,"10x10");
    wire_load_from_area(10,25,"05x05");
  }
```

EXAMPLE MESSAGE

```
Warning: The 'test' wire_load_selection group has been specified
        while the default_wire_load_mode is default to 'top'. This causes
        the 'wire_load_selection' group to work only for the top-
level design. (LBDB-257)
```

LBDB-258 (error) The '%s' driver_type cannot be specified

on a inout pin without a three_state attribute.

DESCRIPTION

This message indicates that you specified a pull_up or a pull_down driver_type on an inout pin lacking a three_state attribute.

WHAT NEXT

Either delete the driver_type or add the three_state attribute.

EXAMPLES

```
pin(A) {
  direction : inout;
  driver_type : pull_up;
  capacitance : 1;
  pulling_resistance : 100;
}
```

EXAMPLE MESSAGE

```
Error: Line 354, The 'pull_up' driver_type cannot be specified
        on a inout pin without a three_state attribute. (LBDB-258)
```

LBDB-259 (error) The '%s' refers to a nonexistent or empty '%s'.

DESCRIPTION

This message indicates that you specified a nonexistent or empty template group on a propagation delay in a nonlinear delay library.

WHAT NEXT

Check the library source file, and either add the lu_table_template group if it is missing or correct the template name if it is a typo.

EXAMPLES

```
fall_propagation(lbdb259_template) {
values ("1, 2, 3, 4", "5, 6, 7, 8", \

"9, 10, 11, 12", "13, 14, 15, 16");
}
```

To fix the problem, add the following group to the library file,

```
lu_table_template(lbdb259_template) {
    variable_1 : input_net_transition;
    variable_2 : output_net_length;
    index_1 ("0.1, 1.2, 2.3, 3.4");
    index_2 ("0.1, 1.2, 2.3, 3.4");
}
```

EXAMPLE MESSAGE

```
Error: Line 111, The 'lbdb259_template' refers to a nonexistent or empty 'lu_table_
template'. (LBDB-259)
```

LBDB-260 (error) The '%s' in '%s' and '%s' in '%s' of the '%s' lu_table_template represent the same unallowable meaning.

DESCRIPTION

This message indicates that the two variables in the lu_table_template represent the same unallowable meaning. Library Compiler fails if both the values of variable_1 and variable_2 are from the following set:

* total_output_net_capacitance
* output_net_length
* output_net_wire_cap
* output_net_pin_cap

WHAT NEXT

Check the lu_table_template, and make the correction to either variable_1 or variable_2.

EXAMPLES

```
lu_table_template(lbdb260) {
    variable_1 : output_net_length;
    variable_2 : total_output_net_capacitance;
    index_2 ("0.1, 1.2, 2.3, 3.4");
}
```

EXAMPLE MESSAGE

```
Error: Line 57, The 'output_net_length' in variable_1 and 'total_output_net_capacit
ance'
in variable_2 of the 'lbdb260' lu_table_template represent
the same unallowable meaning. (LBDB-260)
```

LBDB-261 (error) The ’%s’ has already been specified for ’%s’.

DESCRIPTION

This message indicates that routing track or look-up table information is specified multiple times. Library Compiler does not allow duplicate information.

WHAT NEXT

Check the library source file, and, if there is a duplicate, change the name of either group or delete one group.

EXAMPLES

```
lu_table_template(lbdb261_template) {
    variable_1 : constrained_pin_transition;
    variable_2 : related_pin_transition;
    index_1 ("0.1, 1.2, 2.3, 3.4");
    index_2 ("0.1, 1.2, 2.3, 3.4");
    index_2 ("0.1, 1.2, 2.3, 3.4");
}
```

EXAMPLE MESSAGE

Error: Line 43, The ’index_2’ has already been specified for ’lbdb261_template’. (LBDB-261)

LBDB-261w (warning) The ’%s’ has already been specified for ’%s’.

DESCRIPTION

This message indicates that routing track or look-up table information is specified multiple times. Library Compiler does not allow duplicate information.

WHAT NEXT

Check the library source file, and, if there is a duplicate, change the name of either group or delete one group.

EXAMPLES

```
lu_table_template(lbdb261_template) {
    variable_1 : constrained_pin_transition;
    variable_2 : related_pin_transition;
    index_1 ("0.1, 1.2, 2.3, 3.4");
```

```
      index_2 ("0.1, 1.2, 2.3, 3.4");
      index_2 ("0.1, 1.2, 2.3, 3.4");
  }
```

EXAMPLE MESSAGE

```
Warning: Line 43, The 'index_2' has already been specified for 'lbdb261_template'.
(LBDB-261w)
```

LBDB-262 (error) The '%s' attribute has an invalid sequence of data '%f , %f'. The values must be in monotonically increasing order.

DESCRIPTION

This message indicates that the set of data is not specified in monotonically increasing order.

WHAT NEXT

Check your library and correct the order of the values.

EXAMPLES

```
  lu_table_template(one_dimension) {
      variable_1 : input_net_transition;
      variable_2 : output_net_length;
      index_1 ("0.1");
/* index does not in monotically increasing order */
      index_2 ("0.1, 4.2, 2.3, 3.4");
  }
```

EXAMPLE MESSAGE

```
Error: Line 22, The 'index_2' attribute has an invalid sequence of
data '4.200000 , 2.300000'. The values must be in
monotonically increasing order. (LBDB-262)
```

LBDB-263 (error) The '%s' attribute has a value '%f', which is less than '%f', the minimum required value

of this attribute.

DESCRIPTION

The value specified is less than the required minimum value for this attribute.

WHAT NEXT

Check the library source file and correct the problem. Find the minimum value for this attribute in the error message or in the Library Compiler reference manual.

EXAMPLES

```
  lu_table_template(invalid_template) {
      variable_1 : constrained_pin_transition;
      variable_2 : output_net_length;
/* index value can not be less than zero */
      index_1 ("-0.1, 1.2, 2.3, 3.4");
      index_2 ("0.1, 1.2, 2.3, 3.4");
  }
```

EXAMPLE MESSAGE

```
Error: Line 35, The 'index_1' attribute has a value '-0.100000',
which is less than '0.000000', the minimum required value
of this attribute. (LBDB-263)
```

LBDB-264 (error) The '%s' is invalid in this look-up table.

DESCRIPTION

This message indicates that the specified index is not allowed in the current table because the current table is one dimensional.

WHAT NEXT

Check the library source file to determine whether you have the **variable_2** attribute specified before **index_2** or whether you are specifying **index_2** in a one-dimensional table or template.

EXAMPLES

```
  lu_table_template(lbdb264) {
      variable_1 : constrained_pin_transition;
      index_2 ("0.1, 1.2, 2.3, 3.4");
  }
```

To fix the problem, change index_2 to index_1.

EXAMPLE MESSAGE

Error: Line 46, The 'index_2' is invalid in this delay look-up table. (LBDB-264)

LBDB-265 (error) You cannot mix a cell delay table with a propagation delay table in the same timing group.

DESCRIPTION

You can define cell delay table or propagation delay table within a timing group, but you cannot mix them together. For example, **cell_rise** and **propagation_fall** cannot be defined in a timing group. The same applies to **cell_fall** and **propagation_fall**.

WHAT NEXT

Make your selection, and use either a cell delay table or a propagation delay table.

EXAMPLES

```
  cell (INVB) {
    area : 0.1;
    pin(Q) {
      direction : output;
      function :  "!A";
      timing() {
related_pin : "A";
rise_transition(fivebyfive) {
  index_1("0.000,0.200,0.400,0.600,0.800");
  index_2("0.100,0.200,0.300,0.400,0.500");
  values("0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000");
}
cell_rise(fivebyfive_prime) {
  index_1("0.000,0.200,0.400,0.600,0.800");
  values("-0.100000, -0.200000, 0.300000, 0.400000, 0.500000");
}
rise_propagation(fivebyfive_prime) {
  index_1("0.000,0.200,0.400,0.600,0.800");
  values("-0.100000, -0.200000, 0.300000, 0.400000, 0.500000");
}
```

```
fall_transition(fivebyfive) {
  index_1("0.000,0.200,0.400,0.600,0.800");
  index_2("0.100,0.200,0.300,0.400,0.500");
  values("0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000");
}
cell_fall(fivebyfive) {
  index_1("0.000,0.200,0.400,0.600,0.800");
  index_2("0.100,0.200,0.300,0.400,0.500");
  values("0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000");
}
      }
      max_transition : 1.0;
    }
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 1110, You cannot mix a cell delay table with
a propagation delay table in the same timing group. (LBDB-265)
```

LBDB-266 (error) The ’%s’ attribute is needed in the specification.
No default can be applied to this attribute.

DESCRIPTION

This error message occurs when the identified attribute is missing in the specification.

WHAT NEXT

Check your library, add the missing attribute, and run the command again.

For example, the **index_1** attribute is missing from the following specification:

```
lu_table_template(lbdb266_template) {
 variable_1 : constrained_pin_transition;
 index_2 ("0.1, 1.2, 2.3, 3.4");
}
```

In the following example, since the **va_rise_constraint** is referring to a template that contains the **related_out_total_output_net_capacitance** related output loading variable, the **related_output_pin** attribute is required under the timing group.

```
lu_table_template(va_sup_hld_1) {
  variable_1 : related_out_total_output_net_capacitance;
  index_1("2.0, 3.0");
  variable_2 : constrained_pin_transition;
  index_2("3.0, 4.0");
}
   timing () {
      timing_based_variation() {
        va_parameters(var1, var2);
        nominal_va_values(10.0, 20.0);
        va_rise_constraint(va_sup_hld_1) {
                        va_values(10.0, 19.0);
              ...
        }
...}
```

LBDB-267 (error) The '%s' is missing for this timing arc.

DESCRIPTION

All four delay look-up tables

* rise_propagation/cell_rise
* fall_propagation/cell_fall
* rise_transition
* fall_transition

are required in the timing arc if the **delay_model** is **table_lookup**. If the **timing_type** is 'clear', define both fall tables. Defining the rise tables is optional. If the **timing_type** is 'preset', define both rise tables. Defining the fall tables is optional.

WHAT NEXT

Check the library source file to see if you missed the look-up table or put it in the wrong place.

EXAMPLES

```
    pin ( Y )    {
      direction : output;
      function : " (A+B)' ";
      timing ()      {
        related_pin : A ;
        rise_propagation(prop) {
          values("0.100000, 0.100000, 0.100000",  \

 "0.100000, 0.100000, 0.100000",  \

                 "0.100000, 0.100000, 0.100000",  \

                 "0.100000, 0.100000, 0.100000",  \

                 "0.100000, 0.100000, 0.100000");
        }
        rise_transition(tran) {
          values("0.000000, 0.10000");
        }
        fall_transition(tran) {
          values("0.000000, 0.100000");
        }
      }
    }
```

To fix the problem, add the attribute to the timing group,

```
        fall_propagation(prop) {
          values("0.100000, 0.100000, 0.100000",  \

 "0.100000, 0.100000, 0.100000",  \

                 "0.100000, 0.100000, 0.100000",  \

                 "0.100000, 0.100000, 0.100000",  \

                 "0.100000, 0.100000, 0.100000");
        }
```

EXAMPLE MESSAGE

```
Error: Line 144, The 'fall_propagation' is missing for this timing arc. (LBDB-267)
```

LBDB-268 (error) The '%s' cannot be specified in a timing arc with

the ’%s’ timing_type.

DESCRIPTION

This message indicates that the timing arc with the indicated timing_type is not compatible with a **table_lookup** delay model.

EXAMPLES

```
rise_constraint(basic_template) {
values ("1, 2, 3, 4", "5, 6, 7, 8", \

"9, 10, 11, 12", "13, 14, 15, 16");
}
```

EXAMPLE MESSAGE

```
Error: The ’rise_constraint’ cannot be specified in a timing arc with
the ’combinational’ timing_type. (LBDB-268)
```

LBDB-269 (error) You have both ’%s’ and ’%s’ specified in this timing group.

DESCRIPTION

You cannot specify both cell delay and propagation delay information in a timing group as indicated in the error message. For example, **cell_rise** and **propagation_fall** cannot be defined in a timing group. The same applies to **cell_fall** and **propagation_fall**.

You can use **intrinsic_rise** and **intrinsic_fall** to define default delay values when the delay model is a table_lookup.

WHAT NEXT

Make your selection to use either a cell delay table or a propagation delay table.

EXAMPLES

```
  cell (INVB) {
    area : 0.1;
    pin(Q) {
      direction : output;
      function :  "!A";
      timing() {
related_pin : "A";
rise_transition(fivebyfive) {
```

```
  index_1("0.000,0.200,0.400,0.600,0.800");
  index_2("0.100,0.200,0.300,0.400,0.500");
  values("0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000");
}
cell_rise(fivebyfive_prime) {
  index_1("0.000,0.200,0.400,0.600,0.800");
  values(
 "-0.100000, -0.200000, 0.300000, 0.400000, 0.500000");
}
rise_propagation(fivebyfive_prime) {
  index_1("0.000,0.200,0.400,0.600,0.800");
  values(
 "-0.100000, -0.200000, 0.300000, 0.400000, 0.500000");
}
fall_transition(fivebyfive) {
  index_1("0.000,0.200,0.400,0.600,0.800");
  index_2("0.100,0.200,0.300,0.400,0.500");
  values("0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000");
}
cell_fall(fivebyfive) {
  index_1("0.000,0.200,0.400,0.600,0.800");
  index_2("0.100,0.200,0.300,0.400,0.500");
  values("0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \

 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000");
}
      }
      max_transition : 1.0;
    }
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
```

```
}
```

EXAMPLE MESSAGE

```
Error: Line 1110, You have both 'rise_propagation' and 'cell_rise'
specified in this timing group. (LBDB-269)
```

LBDB-270 (error) The '%s' has a count of %d, which does not match
the size %d specified.

DESCRIPTION

The specification of the index implied the size of each axis of the look-up table. The syntax of **values** complex attribute should be organized in groups of floating-point values equal to the size of index_2. The total number of groups should be equal to the size of index_1. For a one-dimensional table, the size of index_2 is **1**.

WHAT NEXT

Check the library source file, and correct the problem by grouping the values together in the required format.

EXAMPLES

```
lu_table_template(basic_template) {
    variable_1 : input_net_transition;
    variable_2 : output_net_length;
    index_1 ("0.1, 1.2, 2.3, 3.4");
    index_2 ("0.1, 1.2, 2.3, 3.4");
}

rise_propagation(basic_template) {
    values ("1, 2, 3, 4", "5, 6, 7, 8", \

          "9, 10, 11", "13, 14, 15, 16");
}
```

EXAMPLE MESSAGE

```
Error: Line 160, The 'values' have a count of 3, which does not match
the size 4 specified. (LBDB-270)
```

LBDB-271 (error) The ’%s’ has zero elements.

DESCRIPTION

This message indicates that one of the lu_table_template index complex attributes contains no value.

WHAT NEXT

Check the library source file, and either add the missing value to the index attribute or delete the attribute if it is not used.

EXAMPLES

```
  lu_table_template(missing_index) {
variable_1 : output_net_length;
index_1("");
  }
```

EXAMPLE MESSAGE

Error: Line 64, The ’index_1’ has zero elements. (LBDB-271)

LBDB-272 (warning) The ’%s’ attribute has a ’%f’ value, which is less than ’%f’ the minimum recommended value of this attribute.

DESCRIPTION

This message indicates that the value assigned for the specified attribute is lower than the recommended minimum value. However, Library Compiler will maintain the values as is.

WHAT NEXT

Check the library source file, and make sure the value is correct. Refer to the "Library Compiler Reference Manual" for the attribute value requirements.

EXAMPLES

```
  lu_table_template(basic_template) {
      variable_1 : input_net_transition;
      variable_2 : output_net_length;
      index_1 ("0.1, 1.2, 2.3, 3.4");
      index_2 ("0.1, 1.2, 2.3, 3.4");
```

```
  }
  ...
fall_transition(basic_template) {
values ("-1, 2, 3, 4", "5, 6, 7, 8", \

"9, 10, 11, 12", "13, 14, 15, 16");
}
```

EXAMPLE MESSAGE

```
Warning: Line 123, The 'values' attribute has a '-1.000000' value,
which is less than '0.000000' the minimum recommended value of
      this attribute. (LBDB-272)
```

LBDB-273 (error) The fanout_length complex attribute allows only 2 or 5 arguments, and you specified %d arguments.

DESCRIPTION

This message indicates that the **fanout_length** complex attribute has an invalid number of arguments. The attribute can have either the two standard arguments,

* fanout
* length

or five arguments created automatically from the back-annotation information,

* fanout
* length
* average capacitance
* standard deviation
* number of nets

WHAT NEXT

Refer to the "Library Compiler User Guide" manual for more information about the fanout_length attribute. Check the library source file, and correct the format of the attribute.

EXAMPLES

```
  wire_load("05x05") {
    resistance : 0 ;
    capacitance : 1 ;
    area : 0 ;
    slope : 0.186 ;
    fanout_length(1,0.39, 0.1) ;
```

```
  }
```

EXAMPLE MESSAGE

```
Error: Line 43, The fanout_length complex attribute allows only 2
        or 5 arguments, and you specified 3 arguments. (LBDB-273)
```

LBDB-274 (warning) The ’%s’ attribute has a ’%f’ value, which is less than ’%f’ the minimum required value of this attribute. The value is changed to the minimum value.

DESCRIPTION

This message indicates that the value assigned for the specified attribute is lower than the required minimum value. Therefore, Library Compiler uses the minimum value for the attribute.

WHAT NEXT

Check the library source file, and correct the value if the minimum value is not acceptable. Refer to the "Library Compiler Reference Manual" for the attribute value requirements.

EXAMPLES

```
  lu_table_template(basic_template) {
      variable_1 : output_pin_transition;
      variable_2 : connect_delay;
      index_1 ("0, 1");
      index_2 ("0, 1");
  }
  ...
fall_transition_degradation(basic_template) {
values ("-1, 2", "5, 8");
}
```

EXAMPLE MESSAGE

```
Warning: Line 123, The ’values’ attribute has a ’-1.000000’ value,
which is less than ’0.000000’ the minimum required value of
this attribute. The value is changed to the minimum value. (LBDB-274)
```

LBDB-275 (warning) The ’%s’ attribute has size 1, which is not

used for any purpose with its associated variable.

DESCRIPTION

This message indicates that the size of one of the **lu_table_template** attributes has size 1. Library Compiler expects the size of each dimension to be larger than **1**.

WHAT NEXT

Check the library source file, and delete this dimension if it is not needed.

EXAMPLES

```
lu_table_template(lbdb275) {
     variable_1 : input_net_transition;
     variable_2 : output_net_length;
     index_1 ("0.1");
     index_2 ("0.1, 0.2, 0.3, 0.4");
 }
```

EXAMPLE MESSAGE

```
Warning: Line 20, The 'index_1' attribute has size 1, which is not
used for any purpose with its associated variable. (LBDB-275)
```

LBDB-276 (error) The '%s' refers to an invalid '%s'.

DESCRIPTION

This message indicates that the specified name refers to an invalid **lu_table_template** group. First, Library Compiler issues all the errors that make the group invalid and issues this message when the template is used.

WHAT NEXT

Check the library source file, and correct the errors in the look-up table template to which this table refers.

EXAMPLES

```
lu_table_template(lbdb276_template) {
    variable_1 : constrained_pin_transition;
    variable_2 : output_net_length;
    index_1 ("-0.1, 1.2, 2.3, 3.4");
    index_2 ("0.1, 1.2, 2.3, 3.4");
}
```

```
  rise_transition(invalid_template) {
      values ("1, 2, 3, 4", "5, 6, 7, 8", \

             "9, 10, 11, 12");
  }
```

In this case, the index_1 value is less than zero, so the look-up table becomes invalid. The rise_transition timing information refers to an invalid table.

EXAMPLE MESSAGE

```
Error: Line 165, The 'lbdb276_template' refers to an invalid 'lu_table_template'. (
LBDB-276)
```

LBDB-278 (error) The 'timing' group with '%s' timing_type needs at least one look-up table.

DESCRIPTION

This message indicates that in a nonlinear delay library, you did not specify a look-up table (rise_constraint or fall_constraint) for timing checks in a timing group. To be complete, Library Compiler expects at least one look-up table for the timing check groups.

WHAT NEXT

Check the library source file, and correct the timing group. Add either a rise_constraint or fall_constraint table to the group.

EXAMPLES

```
  pin ( D )    {
      direction : input;
      capacitance : 1;
      timing ()      {
        related_pin : CK ;
        timing_type : setup_rising ;
      }
  }
```

To fix the problem, define the template group and the rise_constraint group to the timing group,

```
  lu_table_template(constraint) {
    variable_1 : constrained_pin_transition;
    index_1("0, 1, 2, 3, 4");
    variable_2 : related_pin_transition;
```

```
    index_2("0, 1, 2, 3, 4");
  }
  pin ( D )    {
      direction : input;
      capacitance : 1;
      timing () {
        related_pin : CK ;
        timing_type : setup_rising ;
rise_constraint(constraint) {
          values("1.0000, 1.0000, 1.0000, 1.0000, 1.0000",  \

 "1.0000, 1.0000, 1.0000, 1.0000, 1.0000",  \

 "1.0000, 1.0000, 1.0000, 1.0000, 1.0000",  \

 "1.0000, 1.0000, 1.0000, 1.0000, 1.0000",  \

 "1.0000, 1.0000, 1.0000, 1.0000, 1.0000");
 }
      }
  }
```

EXAMPLE MESSAGE

```
Error: Line 63, The 'timing' group with 'setup_rising' timing_type
needs at least one look-up table. (LBDB-278)
```

LBDB-279 (error) The 'timing' group with '%s' timing_type needs one look-up table.

DESCRIPTION

This message indicates that you specified more than one table for the specified timing group. This group needs only one table, either **constraint_rise** or **constraint_fall**.

WHAT NEXT

Check the library source file, and correct the timing group. Delete from the group either the **constraint_rise** table or the **constraint_fall** table.

EXAMPLES

```
    pin(cd) {
      direction : input;
      capacitance : 0.065
      timing() {
related_pin : "cp";
timing_type : recovery_rising;
```

```
rise_constraint(constraint_template) {
  values("1, 2", "3, 4");
}
fall_constraint(scalar) {
  values("1");
}
      }
    }
```

In this case, the ’cd’ pin has both the rise_constraint and fall_constraint attribute. To fix the problem, delete the fall_constraint table.

EXAMPLE MESSAGE

Error: Line 61, The ’timing’ group with ’recovery_rising’ timing_type needs one look-up table. (LBDB-279)

LBDB-280 (error) The ’%s’ look-up table cannot use ’%s’ as its template. The look-up table is not compatible with the template.

DESCRIPTION

This message indicates that the specified look-up table is not compatible with the specified template. Variable types described in a look-up table template must be compatible with the usage of that template. For example, a template references variable types used for constraint checking (’related_pin_transition’ and ’constrained_pin_transition’) cannot be referenced in a cell delay description (’cell_rise’ or ’cell_fall’).

WHAT NEXT

Refer to the "Library Compiler User Guide" for more information about look-up tables. Change the library source file by referencing a different template in the look-up table description.

EXAMPLES

```
  lu_table_template(basic_template) {
    variable_1 : input_net_transition;
    index_1("0, 1, 2, 3, 4");
    variable_2 : output_net_length;
    index_2("0, 1, 2");
  }
  lu_table_template(constraint) {
    variable_1 : constrained_pin_transition;
    index_1("0, 1, 2, 3, 4");
    variable_2 : related_pin_transition;
```

```
    index_2("0, 1, 2, 3, 4");
  }

rise_constraint(basic_template) {
values ("1, 2, 3, 4", "5, 6, 7, 8", \

"9, 10, 11, 12", "13, 14, 15, 16");
}
```

To fix the problem, change the template value of the rise_constraint group from basic_template to constraint.

EXAMPLE MESSAGE

```
Error: Line 126, The 'rise_constraint' look-up table cannot use
'basic_template' as its template. The look-up table is not
compatible with the template. (LBDB-280)
```

LBDB-281 (error) The '%s' template has variables which should not be used together.

DESCRIPTION

This message indicates that you specified two incompatible variables in the same template.

WHAT NEXT

Refer to the "Library Compiler User Guide" for more information on defining CMOS nonlinear timing model templates. Check the library source file to see if you made a mistake when you entered the variables strings.

EXAMPLES

```
  lu_table_template(invalid_template) {
      variable_1 : constrained_pin_transition;
      variable_2 : output_net_length;
      index_1 ("0.1, 0.2, 0.3, 0.4");
      index_2 ("0.1, 0.2, 0.3, 0.4");
  }
```

EXAMPLE MESSAGE

```
Error: Line 32, The 'invalid_template' template has variables which
should not be used together. (LBDB-281)
```

LBDB-282 (error) The ’%s’ attribute has a ’%f’ value that is larger than the maximum allowed value of ’%f’.

DESCRIPTION

This message indicates that for the specified attribute, you defined a value that is larger than the maximum allowed value. The error message includes the maximum value for this attribute.

WHAT NEXT

Refer to the "Library Compiler User Guide" for the maximum value required for the attribute, and correct the value in the library source file.

EXAMPLES

```
default_min_porosity : 91.0;
```

EXAMPLE MESSAGE

Error: Line 53, The ’default_min_porosity’ attribute has a ’91.000000’ value that is larger than the maximum allowed value of ’90.000000’. (LBDB-282)

LBDB-283 (error) The ’%s’ layer name is invalid.

DESCRIPTION

This message indicates that you specified an invalid name for the current attribute or function. The name should match a name previously defined in the resource group.

If the value is in the related_layer attribute and the layer is not valid. It may be because it is not one of the neighboring contact layer.

WHAT NEXT

Check your library to see if you have an error in either previous layer definition or the current attribute / function.

EXAMPLES

```
same_net_min_spacing(dummy, metal1, 0.1, TRUE);
```

EXAMPLE MESSAGE

```
Error: Line 104, The 'dummy' layer name is invalid.  (LBDB-283)
```

LBDB-284 (error) Missing 'routing_layers' attribute for this library which is needed for specifying 'routing_track'.

DESCRIPTION

This message indicates that you specified a **routing_track** group without specifying the **routing_layers** attribute. Library Compiler expects the **routing_layers** complex attribute to be defined before you can specify the **routing_track** group. The **routing_track** group has a name to refer to a specific routing layer in the **routing_layers** complex attribute.

WHAT NEXT

Check the library source file to see if you are missing the **routing_layers** attribute, which should be placed in the library before the **routing_track** group can be identified.

EXAMPLES

```
   routing_track(metal2) {
        tracks : 2;
        total_track_area : 0.2;
   }
```

To fix the problem, add the attribute to the library,

```
    routing_layers(metal1,metal2);
```

EXAMPLE MESSAGE

```
Error: Line 65, Missing 'routing_layers' attribute for this library,
which is needed for specifying 'routing_track'. (LBDB-284)
```

LBDB-285 (error) In this 'routing_track' group, 'tracks' is 0 and 'total_track_area' is %f, which is inconsistent.

DESCRIPTION

This message indicates that for a **routing_track** group, you specified the

total_track_area attribute without specifying the **tracks** attribute. If you do not have tracks in a routing layer, you cannot have **total_track_area** for that layer either.

WHAT NEXT

Check your library to see if it is missing the **tracks** attribute in this group. Do not have the **total_track_area** other than '0', or this group is not needed.

EXAMPLES

```
   routing_layers(metal1,metal2);

   routing_track(metal2) {
/* missing tracks */
        total_track_area : 1.5;
   }
```

To fix the problem, add the tracks attribute to the routing_track group,

```
        tracks : 1;
```

EXAMPLE MESSAGE

```
Error: Line 266, In this 'routing_track' group, 'tracks' is 0 and
'total_track_area' is 1.500000, which is inconsistent. (LBDB-285)
```

LBDB-286 (error) No 'routing_track' information in the '%s' library.

DESCRIPTION

This message indicates that, in the library, you specified the **default_min_porosity** attribute without specifying the **routing_track** group in any of the cells.

WHAT NEXT

Remove the **default_min_porosity** attribute or add **routing_track** information into the library.

EXAMPLE MESSAGE

```
Error: Line 1, No 'routing_track' information in the 'lbdb286' library. (LBDB-286)
```

LBDB-287 (warning) No routability information in the '%s' %s.

DESCRIPTION

This message indicates that one of the two cases occurred:

* You have the **routing_layers** attribute in a library and do not have **routing_track** group in the cell.
* You have the **default_min_porosity** attribute in a library and do not have the **routing_track** information in a cell.

WHAT NEXT

Check the library source file to remove the **routing_layers** attribute if the warning fits the first case. For the second case, check the cell to make sure it does not have any **routing_track** information on all routing layers (all of them are completely obstructed in this cell) when you have the **default_min_porosity** attribute.

EXAMPLES

```
    default_min_porosity : 0.0;
    routing_layers(metal1,metal2);

cell(AN2) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A B";
    timing() {
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "A";
    }
    timing() {
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "B";
    }
  }
```

```
}
```

In this case, The library has the **default_min_porosity** attribute, but the 'AN2' cell has no **routing_track** information.

EXAMPLE MESSAGE

```
Warning: Line 63, No routability information in the 'AN2' cell. (LBDB-287)
```

LBDB-288 (error) The '%f' 'total_track_area' value is larger than the '%f' cell area value.

DESCRIPTION

This message indicates that you specified a larger value for the **total_track_area** than the **cell area** value. The **total_track_area** value of a particular routing layer cannot be larger than the **cell area** value.

WHAT NEXT

Check to see if you have entered the wrong information for either of these two attributes.

EXAMPLES

```
cell(IVP) {
  area : 1;
   routing_track(metal2) {
tracks : 1;
        total_track_area : 1.5;
   }
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A'";
    timing() {
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
```

```
}
```

EXAMPLE MESSAGE

```
Error: Line 242, The 1.500000 'total_track_area' value is larger than
the '1.000000' cell area value. (LBDB-288)
```

LBDB-289 (error) '%s' has been used more than one time in the specification.

DESCRIPTION

This message indicates that you specified the same routing layer name more than once in the routing_layers attribute. Library Compiler expects unique names.

WHAT NEXT

Check to see if you entered the wrong information for this attribute.

EXAMPLES

```
    routing_layers(metal2,metal2);
```

EXAMPLE MESSAGE

```
Error: Line 55, 'metal2' has been used more than one time in the
specification. (LBDB-289)
```

LBDB-290 (error) '%s' should have at least one entry in it.

DESCRIPTION

This message indicates that you specified an attribute without any entries. This complex attribute must contain at least one entry.

WHAT NEXT

Check to see if you have entered the required information for this complex attribute.

EXAMPLES

```
    routing_layers();
```

EXAMPLE MESSAGE

Error: Line 18, 'routing_layers' should have at least one entry in it. (LBDB-290)

LBDB-291 (warning) No routability information for the '%s' layer. It is assumed to be completely obstructed.

DESCRIPTION

The **routing_track** group of the indicated layer is not in the cell. It is assumed to be completely obstructed.

WHAT NEXT

If the previous statement is not true, enter the **routing_track** information for the indicated layer. Otherwise, it is all right.

EXAMPLES

```
library(small_cmos1) {
    default_min_porosity : 0.0;
    routing_layers(metal1,metal2);

    cell(AN2) {
       area : 2;
       routing_track(metal2) {
         tracks : 2;
         total_track_area : 0.2;
       }
       pin(A) {
         direction : input;
         capacitance : 1;
       }
       pin(B) {
         direction : input;
         capacitance : 1;
       }
       pin(Z) {
         direction : output;
         function : "A B";
         timing() {
            intrinsic_rise : 0.1;
    intrinsic_fall : 0.1;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "A";
 }
         timing() {
            intrinsic_rise : 0.1;
    intrinsic_fall : 0.1;
```

```
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "B";
         }
       }
    }
}
```

In this case, ’metal1’ is not used in any routing_track group.

EXAMPLE MESSAGE

```
Warning: Line 240, No routability information for the ’metal1’ layer.
It is assumed to be completely obstructed. (LBDB-291)
```

LBDB-292 (error) The ’%s’ should be the %d%s attribute in the library.

DESCRIPTION

This message indicates that you specified the technology and delay_model in unacceptable order. For the Library Compiler to work correctly, the defined attribute must appear in this library at the indicated place in the error message.

WHAT NEXT

Modify the library source file to move the defined attribute to the correct place, as indicated in the error message.

EXAMPLES

```
library(lib) {
  technology : "cmos";
  delay_model : "generic_cmos";
}
```

In this case, the delay_model attribute comes after the technology attribute. To fix the problem, switch the order of definition of the two attributes.

EXAMPLE MESSAGE

```
Error: Line 5, The ’delay_model’ should be the 1st attribute in the library. (LBDB-
292)
```

LBDB-293 (error) In this ’routing_track’ group, the ’tracks’ value

is %d and the ’total_track_area’ value is ’0.0’. This is inconsistent.

DESCRIPTION

This message indicates that you specified the **tracks** attribute without specifying the **total_track_area** attribute in a **routing_track** group. If you have tracks in a routing layer, you need to have the **total_track_area** for that layer too.

WHAT NEXT

Check the library source file to see if it is missing the **total_track_area** attribute in this group, and add it. Otherwise, set the **tracks** value to 0 or remove the routing_track group.

EXAMPLES

```
   routing_track(metal2) {
        tracks : 2;
/* missing total_track_area */
   }
```

EXAMPLE MESSAGE

```
Error: Line 205, In this ’routing_track’ group, the ’tracks’ value
is 2 and the ’total_track_area’ value is ’0.0’. This is
inconsistent. (LBDB-293)
```

LBDB-294 (warning) The UP or DOWN X pin coordinate does not lay on a grid.

DESCRIPTION

This warning message appears when the library symbol has a pin that is not on a grid and is off by 0.01.

WHAT NEXT

Check the symbol library file, and correct the X coordinate.

EXAMPLES

```
library(lbdb294) {
 SCALE = 1.0 / 8.0;
```

```
  symbol("gndsym") {
    set_minimum_boundary(0 * SCALE, 0 * SCALE, 40 * SCALE, 40 * SCALE);
    line(5 * SCALE, 10 * SCALE, 35 * SCALE, 10 * SCALE);
    line(0 * SCALE, 20 * SCALE, 40 * SCALE, 20 * SCALE);
    line(15 * SCALE, 2 * SCALE, 25 * SCALE, 2 * SCALE);
    line(20 * SCALE, 20 * SCALE, 20 * SCALE, 40 * SCALE);
    pin("gnd", 20 * SCALE, 40 * SCALE, ANY_ROTATION);
  }
}
```

In this case, the "gnd" pin has the Y coordinate off the grid.

EXAMPLE MESSAGE

```
Warning: Line 24, The UP or DOWN X pin coordinate does not lay on a grid. (LBDB-294)
```

LBDB-295 (warning) The LEFT or RIGHT Y pin coordinate does not lay on a grid.

DESCRIPTION

This warning message appears when the library symbol has a pin that is not on a grid and is off by 0.01.

WHAT NEXT

Check the symbol library file, and correct the Y coordinate.

EXAMPLES

```
library(lbdb295) {
 SCALE = 1.0 / 8.0;

  symbol("gnd") {
    set_minimum_boundary(0 * SCALE, 0 * SCALE, 40 * SCALE, 40 * SCALE);
    line(5 * SCALE, 10 * SCALE, 35 * SCALE, 10 * SCALE);
    line(0 * SCALE, 20 * SCALE, 40 * SCALE, 20 * SCALE);
    line(15 * SCALE, 2 * SCALE, 25 * SCALE, 2 * SCALE);
    line(20 * SCALE, 20 * SCALE, 20 * SCALE, 40 * SCALE);
    pin("Z", 128 * SCALE, 4 * SCALE, ANY_ROTATION);
    pin("gnd", 20 * SCALE, 40 * SCALE, ANY_ROTATION);
  }
}
```

In this case, the "Z" pin has the Y coordinate off the grid.

EXAMPLE MESSAGE

```
Warning: Line 24, The LEFT or RIGHT Y pin coordinate does not lay on a grid. (LBDB-
295)
```

LBDB-296 (warning) The '%s' pin of the '%s' auxiliary pad cell should not have a function attribute.

DESCRIPTION

This message indicates that you specified a function attribute on a auxiliary pad cell.

Cells with a 'auxiliary_pad_cell' attribute are used together with other cells with a 'pad_cell' attribute to build a logical pad. They can also provide the pull-up, pull-down, buffer, or inverter functionality. They should not have real 'logic'. Design Compiler will not work correctly if you decompose your pad cell this way.

WHAT NEXT

Check the technology source library. Either

1. remove the 'function' attribute from the cell under the following conditions:

* If the cell is a buffer, no action is required.
* If the cell is an inverter, invert the functionality of your 'pad_cell', which is to be connected to this cell to form a pad cell, accordingly.

or

2. remove the 'auxiliary_pad_cell' attribute, and model this cell as a regular cell but with the right 'connection_class' on the pin so it can be connected to the 'pad_cell' to form a pad as intended.

EXAMPLES

```
cell(lbdb296) {
  auxiliary_pad_cell : true;
  area : 1;
  general_drivers : 0;
  input_drivers : 8;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A'";
    timing() {
      intrinsic_rise : 0.1;
```

```
          intrinsic_fall : 0.1;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "A";
        }
      }
    }
```

EXAMPLE MESSAGE

```
Warning: Line 64, The 'Z' pin of the 'lbdb296' auxiliary pad cell
should not have a function attribute. (LBDB-296)
```

LBDB-297 (error) The '%s' pin is reserved and should not be used as a pin name.

DESCRIPTION

Library Compiler uses several keywords internally for a sequential cell. The keywords are

* next_state
* clocked_on
* clocked_on_also
* data_in
* enable
* enable_also
* preset
* clear
* force_00
* force_01
* force_10
* force_11
* the variable1 and variable2 used in ff/latch/ff_bank/latch_bank

WHAT NEXT

Modify your library to change the name of the pin.

EXAMPLES

```
  pin(preset) {
    direction : input;
    capacitance : 1;
  }
```

EXAMPLE MESSAGE

```
Error: Line 182, The 'preset' pin is reserved and should not be used as a pin name.
 (LBDB-297)
```

LBDB-298 (error) The '%s' attribute has a value %d, which is less than the minimum required value of this attribute %d.

DESCRIPTION

This message indicates that the value specified is less than the required minimum value for this attribute.

WHAT NEXT

Check the library source file, and correct the value of the attribute. If the minimum value for this attribute is not displayed in the error message, refer to the **Library Compiler User Guide Manual** for minimum attribute values.

EXAMPLES

```
    wire_load_table("40x40") {
      fanout_area(-11, 0.1);
   }
```

EXAMPLE MESSAGE

```
Error: Line 84, The 'fanout_area' attribute has a value -11, which is
less than the minimum required value of this attribute 1. (LBDB-298)
```

LBDB-300 (error) The '%s' related_outputs for the internal_power group has been specified. A duplicate is not allowed.

DESCRIPTION

This message indicates that you include the same output pin in more than one internal_power group.

WHAT NEXT

Check the library source file, and delete the duplicate information from one of the internal_power groups.

EXAMPLES

```
internal_power(test_input) {
 values("0.1, 1.2, 2.3, 3.4");
 related_outputs : "Z";
}
internal_power(test_input) {
 values("0.1, 1.2, 2.3, 3.4");
 related_outputs : "Z";
}
```

EXAMPLE MESSAGE

```
Error: Line 41, The 'Z' related_outputs for the internal_power group has
been specified. A duplicate is not allowed. (LBDB-300)
```

LBDB-301 (information) No internal_power information for the '%s' cell.

DESCRIPTION

This message indicates that you did not define an internal_power group for the specified cell. Library Compiler expects at least one internal_power group so the internal power of the cell can be calculated.

WHAT NEXT

If you want to include the internal power of this cell in your design, add the required information into the library.

EXAMPLES

```
cell(lbdb301) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A B";
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
```

```
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A B";
    }
  }
  cell_leakage_power : 1;
}
```

In this case, the 'lbdb301' cell is missing the internal_power group. To fix the problem, add this statement:

```
  internal_power(output_by_cap_and_trans) {
     values(" 5.000000 ,  15.000000 ,  0.300000 ", \

            " 1.000000 ,  5.000000 ,  0.000000 ", \

            " 0.000000 ,  0.000000 ,  0.000000 ");
     related_outputs : "Z";
     related_inputs : "A B";
  }
```

EXAMPLE MESSAGE

```
Information: Line 191, No internal_power information for the 'lbdb301' cell. (LBDB-301)
```

LBDB-302 (error) The '%s' specified in the '%s' is an %s pin.

DESCRIPTION

This message indicates that you specified either an input pin in a **related_outputs** attribute or an output pin in a **related_inputs** attribute.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell(lbdb302) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
```

```
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A B";
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A B";
    }
  }
  cell_leakage_power : 1;
  internal_power(output_by_cap_and_trans) {
     values(" 5.000000 ,  15.000000 ,  0.300000 ", \

             " 1.000000 ,  5.000000 ,  0.000000 ", \

    " 0.000000 ,  0.000000 ,  0.000000 ");
     /* bad related port */
     related_outputs : "A";
     related_inputs : "Z B";
  }
}
```

In this case, both the related_outputs and the related_inputs attributes have a wrong pin name. To fix the problem, change the name from ’A’ to ’Z’ in the related_outputs attribute and ’Z’ to ’A’ in the related_inputs attribute.

EXAMPLE MESSAGE

```
Error: Line 272, The ’A’ specified in the ’related_outputs’ is an
input pin. (LBDB-302)
Error: Line 273, The ’Z’ specified in the ’related_inputs’ is an
output pin. (LBDB-302)
```

LBDB-303 (error) You cannot specify more than one input pin or one bit of a bus or bundle input pin in the ’related_input’.

DESCRIPTION

This message indicates that you specified more than one input pin or one bit of an input pin, in the case of bus and bundle groups, in the **related_input** attribute. Library Compiler allows only one input pin or one bit of a bus or bundle in the attribute.

WHAT NEXT

Check the "Library Compiler User Guide" for more information on power analysis, and correct the problem. Make sure that the related_input attribute has only one input pin or one bit of an bus or bundle input pin and the related_inputs attribute has more than one pin.

EXAMPLES

```
cell(lbdb303) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A+B";
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A B";
    }
  }
  cell_leakage_power : 1;
  internal_power(output_by_cap_and_trans) {
     values(" 5.000000 ,  15.000000 ,  0.300000 ", \

            " 1.000000 ,  5.000000 ,  0.000000 ", \

            " 0.000000 ,  0.000000 ,  0.000000 ");
     related_outputs : "Z";
     /* more than one related input */
     related_input : "A B";
  }
}
```

In this case, the related_input attribute has two ’A’ and ’B’ input pins.

EXAMPLE MESSAGE

```
Error: Line 315, You cannot specify more than one input pin or one bit
of a bus or a bundle input pin in the ’related_input’. (LBDB-303)
```

LBDB-304 (error) You can specify '%s' but not both, because they are mutually exclusive.

DESCRIPTION

This message indicates that you specified a **related_input** attribute with a **related_outputs** attribute in an internal_power group. Library Compiler allows either a **related_input** attribute or the pair **related_outputs**, **related_inputs** attributes, but not both, since the information provided is mutually exclusive. Library Compiler supports the related_input, related_inputs, and the related_outputs attributes in the table as follows:

* A one dimensional table uses only related_outputs.
* A one dimensional table uses only related_input.
* A one dimensional table uses both related_inputs and related_outputs.
* A two dimensional table uses both related_inputs and related_outputs.

WHAT NEXT

Check the library and correct the related_inputs attribute if it is a typo or delete the unnecessary information from the library.

EXAMPLES

```
cell(lbdb304) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A+B";
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A B";
    }
  }
  cell_leakage_power : 1;
  internal_power(output_by_cap_and_trans) {
```

```
     values(" 5.000000 ,  15.000000 ,  0.300000 ", \

            " 1.000000 ,  5.000000 ,  0.000000 ", \

            " 0.000000 ,  0.000000 ,  0.000000 ");
     related_outputs : "Z";
     related_input : "A B";
  }
}
```

In this case, there is a typo. To fix the problem, add the character s to the related_input attribute name.

EXAMPLE MESSAGE

Error: Line 309, You can specify ’related_outputs/related_inputs or related_input’ but not both, because they are mutually exclusive. (LBDB-304)

LBDB-305 (error) In the context, the ’%s’ valid value of the ’%s’ template is ’%s’. You specified ’%s’.

DESCRIPTION

This message indicates that you specified an invalid value for the variable_1 in the power_lut_template given the specified information in the internal_power group. Library Compiler expects

* A related_input attribute in an internal_power group for a input_transition_time value in variable_1 of the corresponding power_lut_template
* A related_outputs attribute in an internal_power group for a total_output_net_capacitance value in variable_1 of the corresponding power_lut_template

WHAT NEXT

Refer to the "Library Compiler Reference Manual Volume 1" for more information on power modeling and analysis. Correct the attribute’s value or its reference in the library.

EXAMPLES

```
  power_lut_template(lbdb305_input) {
    variable_1 : input_transition_time;
    index_1 ("1.0, 2.0");
  }
```

```
cell(lbdb305) {
  internal_power(lbdb305_input) {
    index_1("1.0, 2.0");
    values("1.0, 2.0");
    related_outputs : "Z";
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 27, In the context, the 'variable_1' valid value of the
'lbdb305_input' template is 'total_output_net_capacitance'.
You specified 'input_transition_time'. (LBDB-305)
```

LBDB-306 (warning) The '%s' preferred input voltage does not exist in this library.

DESCRIPTION

This message indicates that you specified a input_voltage name to the **preferred_input_pad_voltage** attribute that is not described in the library or is defined after this attribute.

WHAT NEXT

Check the preferred input pad voltage to be sure it is correct. If the input_voltage exists, make sure that the attribute is defined before the preferred_input_pad_voltage attribute. Otherwise, add the preferred input pad voltage to the library description.

EXAMPLES

```
  preferred_input_pad_voltage : "lbdb306";
  input_voltage(lbdb306) {
    vil : 1.5;
    vih : 3.5;
    vimin : -0.3;
    vimax : VDD + 0.3;
  }
```

in this case, the 'lbdb306' input_voltage is defined after the preferred_input_pad_voltage attribute.

EXAMPLE MESSAGE

```
Warning: Line 25, The 'lbdb306' preferred input voltage does not exist in this libr
ary. (LBDB-306)
```

LBDB-307 (warning) The '%s' preferred output voltage does not exist in this library.

DESCRIPTION

This message indicates that you specified an output_voltage name to the **preferred_output_pad_voltage** attribute that is not described in the library or is defined after this attribute.

WHAT NEXT

Check the preferred output pad voltage to be sure it is correct. If the output_voltage exists, make sure that the attribute is defined before the preferred_output_pad_voltage attribute. Otherwise, add the preferred output pad voltge to the library description.

EXAMPLES

```
preferred_output_pad_voltage : "lbdb307" ;
output_voltage(lbdb307) {
  vol : 1.5;
  voh : 3.5;
  vomin : -0.3;
  vomax : VDD + 0.3;
}
```

in this case, the 'lbdb307' output_voltage is defined after the preferred_output_pad_voltage attribute.

EXAMPLE MESSAGE

```
Warning: Line 24, The 'lbdb307' preferred output voltage does not exist in this lib
rary. (LBDB-307)
```

LBDB-308 (warning) Incomplete set of pads to support the '%s' preferred output pad slew rate control.

DESCRIPTION

This message indicates that in the library you specified the **preferred_output_pad_slew_rate_control** attribute but you did not define a complete set of pads to support it. Library Compiler expects at least one of the following set of pad cells in the library with the given slew rate control value:

* One output pad
* One bidirectional pad

* One three state pad

WHAT NEXT

Check the preferred output pad slew rate control to be sure it is correct, and add pads to the library containing the preferred output pad slew rate control value.

EXAMPLES

```
library (lbdb308) {
  preferred_output_pad_slew_rate_control : high;
  output_voltage(GENERAL) {
    vol          : 0.33 ;
    voh          : 3.7 ;
    vomin        : -0.3 ;
    vomax        : VDD + 0.3 ;
  }
  cell(OUTBUF) {
    area : 0.000000;
    dont_touch : false;
    dont_use   : false;
    pad_cell : true;
    pin(D ) {
      direction   : input;
      capacitance : 1.0;
    }
    pin(PAD ) {
      is_pad : true;
      output_voltage : GENERAL;
      drive_current : 4.0;
      slew_control : high;
      direction   : output;
      function    : "D";
      timing() {
        intrinsic_fall  : 1.0;
        intrinsic_rise  : 1.0;
        fall_resistance : 0.1;
        rise_resistance : 0.1;
        related_pin  :"D";
      }
    }
  }
  cell(BBHS) {
    area : 0.000000;
    dont_touch : false;
    dont_use   : false;
    pad_cell : true;
    pin(E D ) {
      direction   : input;
      capacitance : 1.0;
    }
    pin(Y ) {
      direction   : output;
      timing() {
```

```
        intrinsic_fall  : 1.0;
        intrinsic_rise  : 1.0;
        fall_resistance : 0.1;
        rise_resistance : 0.1;
        related_pin  :"PAD ";
      }
    }
    pin(PAD ) {
      is_pad : true;
      input_voltage : CMOS;
      output_voltage : GENERAL;
      drive_current : 4.0;
      slew_control : high;
      direction   : inout;
      function    : "D";
      three_state : "E'";
      timing() {
        intrinsic_fall  : 1.0;
        intrinsic_rise  : 1.0;
        fall_resistance : 0.1;
        rise_resistance : 0.1;
        related_pin  :"E D";
      }
    }
  }
}
```

In this case, the 'lbdb308' library has an output pad cell and a bidirectional pad cell, but it is missing a three_state pad cell.

EXAMPLE MESSAGE

```
Warning: Line 2, Incomplete set of pads to support the 'high'
preferred output pad slew rate control. (LBDB-308)
```

LBDB-309 (warning) In the '%s' gate, cannot degenerate the '%s' output due to excessive function size.

DESCRIPTION

This message appears when the Library Compiler has determined that degenerating the given output is potentially too difficult. This determination is based on an evaluation of the function complexity at this output port.

WHAT NEXT

Either remove the **fpga_complex_degenerate** attribute from the library cell in question, or set the **fpga_degenerate_output** attribute to FALSE on this particular output. In either case, these actions delete the warning; they do not cause the

degeneration software to attempt to degenerate the gate.

LBDB-310 (information) Degenerating %d-input gates from '%s' component of the '%s' output.

DESCRIPTION

This message indicates that the Library Compiler is starting to create degenerate functions based on the component named.

WHAT NEXT

No action is required.

EXAMPLES

```
  cell(lbdb310) {
    area : 1.0;
    fpga_complex_degenerate : true ;
    pin(D0 D1 D2 D3 S00 S01 S10 S11) {
      direction   : input;
      capacitance : 1.0;
    }
    pin(Y) {
      direction : output;
      function : "(D0!(S00&S01)+D1(S00&S01))!(S10+S11)+(D2!(S00&S01)+D3(S00&S01))(S
10+S11)";
      timing() {
rise_resistance : 0.5;
fall_resistance : 0.5;
        related_pin  :  "D0 D1 D2 D3 S00 S01 S10 S11" ;
      }
    }
  }
```

EXAMPLE MESSAGE

```
Information: Degenerating 2-input gates from the 'lbdb310' component
of the 'Y' output. (LBDB-310)
```

LBDB-311 (information) Degenerated %d %d-input gates from the '%s' component. A total of %d components have been degenerated from the '%s'

output.

DESCRIPTION

This message indicates that the Library Compiler has finished creating n-input degenerate functions based on the component and output named. The message tells you how the library size is growing and how long the degeneration process is taking.

WHAT NEXT

No action is required.

EXAMPLES

```
  cell(lbdb311) {
    area : 1.0;
    fpga_complex_degenerate : true ;
    pin(D0 D1 D2 D3 S00 S01 S10 S11) {
      direction   : input;
      capacitance : 1.0;
    }
    pin(Y) {
      direction   : output;
      function : "(D0!(S00&S01)+D1(S00&S01))!(S10+S11)+(D2!(S00&S01)+D3(S00&S01))(S
10+S11)";
      timing() {
rise_resistance : 0.5;
fall_resistance : 0.5;
        related_pin  :  "D0 D1 D2 D3 S00 S01 S10 S11" ;
      }
    }
  }
```

EXAMPLE MESSAGE

```
Information: Degenerated 2 1-input gates from the 'lbdb311' component.
A total of 2 components have been degenerated from the 'Y' output. (LBDB-311)
```

LBDB-312 (warning) Unable to do fpga complex degeneration on the '%s' gate because it %s.

DESCRIPTION

This message occurs when you have defined **fpga_complex_degenerate** on a component for which this feature is not currently supported. Library Compiler issues this message for the following cells:

* Sequential devices: latches and flip flops
* I/O pads
* Cells with dont_use attribute
* Cells with three_state attribute

WHAT NEXT

Remove the **fpga_complex_degenerate** attribute for this component, or set the attribute to FALSE.

LBDB-315 (error) The '%s' attribute is incorrectly specified in the context.

DESCRIPTION

The attribute indicated in the error message is not valid, because it is not compatible with the template to which this internal_power group refers. For example, the **related_input** attribute cannot be specified in a two-dimensional table.

WHAT NEXT

Refer to the Library Compiler manuals and the Design Power Reference manual for power modeling and analysis. Modify the library to correct the problem.

EXAMPLES

```
power_lut_template(output_by_cap_and_trans) {
  variable_1 : total_output_net_capacitance;
  variable_2 : input_transition_time;
  index_1 ("0.0, 5.0, 20.0");
  index_2 ("0.1, 1.00, 5.00");
}

cell(lbdb315) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A+B";
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
```

```
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A B";
    }
  }
  cell_leakage_power : 1;
  internal_power(output_by_cap_and_trans) {
     values(" 5.000000 ,  15.000000 ,  0.300000 ", \

            " 1.000000 ,  5.000000 ,  0.000000 ", \

            " 0.000000 ,  0.000000 ,  0.000000 ");
     related_outputs : "Z";
     related_input : "A";
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 315, The 'related_input' attribute is incorrectly specified in the cont
ext. (LBDB-315)
```

LBDB-316 (error) Arithmetic overflow or exception is encountered on the '%s' attribute with the '%s' value.

DESCRIPTION

This message indicates that you specified an attribute's value that causes an arithmetic overflow or an exception. Library Compiler cannot handle the value.

WHAT NEXT

Check the library source file, and correct the problem.

EXAMPLES

```
fall_propagation ( table4x6 ) {
   index_1 ("2.00e+02 2.50e+02 3.50e+02 4.00e+02 ") ;
   index_2 ("4.48e-02 8.96e-02 1.34e-01 1.79e-01 2.24e-01 2.69e-01 ");
   values ("7.45e+01 9.56e+01 1.15e+02 1.34e+02 1.52e+02 1.71e+02 ", \

   "9.38e+01 1.20e+02 1.45e+02 1.67e+02 1.89e+02 2.10e+02 ", \

   "1.01e+02 1.32e+02 1.58e+02 1.83e+02 2.07e+02 2.29e+02 ", \
```

```
   "1.04e+02 1.43e-93 1.43e-93 1.43e-93 2.75e+226 9.30e+254 " ) ;
}
```

EXAMPLE MESSAGE

```
Error: Line 85, Arithmetic overflow or exception is encountered
on the 'values' attribute with the '2.75e+226' value. (LBDB-316)
```

LBDB-317 (error) It is invalid to specify the '%s' attribute on a pin within the bus or bundle group.

DESCRIPTION

This message indicates that you specified a function attribute on a pin within a bus or a bundle group.

WHAT NEXT

Check the library source file, and correct the problem.

EXAMPLES

```
  bundle (qn) {
    members(qn2);
    direction : output;
    function : "iq";
    pin (qn2) {
      function : "q2";
    timing() {
       related_pin   : "q2";
       intrinsic_rise :  0.1;
       intrinsic_fall :  0.1;
       rise_resistance : 1.0;
       fall_resistance : 1.0;
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 67, It is invalid to specify the 'function' attribute
on a pin within the bus or bundle group. (LBDB-317)
```

LBDB-350 (error) The '%s' cell has the interface_timing attribute,

but is not a black box.

DESCRIPTION

This library cell has the **interface_timing** attribute set to TRUE. The interface timing specification ITS policy requires that no pin on this cell has the function attribute defined for it. In addition, the ff group cannot be defined for such cells.

WHAT NEXT

Remove the function attribute defined for any output pin of the cell. Also remove the ff group from the cell description if it is specified.

EXAMPLES

```
  cell (lbdb350) {
    area    :   0.0;
    interface_timing : TRUE;
    pin (I1)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
    }
    pin(Q){
      direction   :   output;
      function : "I1'";
      timing () {
intrinsic_rise   : 1.0;
rise_resistance  : 0.1;
intrinsic_fall   : 1.0;
fall_resistance  : 0.1;
related_pin      : "I1";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 6, The 'lbdb350' cell has the interface_timing attribute,
but is not a black box. (LBDB-350)
```

LBDB-353 (warning) A nonsequential timing arc is specified with

respect to the '%s' clock pin.

DESCRIPTION

The cell has the **interface_timing** attribute set to TRUE. The interface timing policy requires that all timing arcs defined with respect to a clock pin be sequential (noncombinational) in nature.

WHAT NEXT

Make sure that all arcs with a clock pin as a related_pin are sequential.

EXAMPLES

```
  cell (lbdb353) {
    area    :   0.0;
    interface_timing : TRUE;
    pin (I1)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      timing () {
timing_type : setup_rising;
intrinsic_rise : 1.0;
intrinsic_fall :  1.0;
related_pin : "CLK";
      }
      timing () {
timing_type : hold_rising;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
related_pin : "CLK";
      }
    }
    pin (CLK)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      clock : true;
      timing () {
timing_type : skew_rising;
intrinsic_rise : 1.0;
related_pin : "CLK1";
      }
    }

    pin (CLK1)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      timing () {
timing_type : skew_falling;
```

```
intrinsic_rise : 1;
related_pin : "CLK";
      }
    }
    pin(Q){
      direction   :   output;
      timing () {
intrinsic_rise   : 1.0;
rise_resistance  : 0.1;
intrinsic_fall   : 1.0;
fall_resistance  : 0.1;
related_pin      : "CLK";
      }
    }
  }
```

In this case, the ’Q’ pin is missing the timing_type attribute in its timing group.

EXAMPLE MESSAGE

```
Warning: Line 62, A nonsequential timing arc is specified with
respect to the ’CLK’ clock pin. (LBDB-353)
```

LBDB-354 (warning) A sequential timing arc is specified with respect to the ’%s’ nonclock pin.

DESCRIPTION

The cell has the **interface_timing** attribute set to TRUE. The interface timing policy requires that all sequential timing arcs (except for clear and preset) be defined with respect to a pin that is labeled as a clock.

WHAT NEXT

Make sure that all sequential arcs are defined with respect to a clock pin.

EXAMPLES

```
  cell (lbdb354) {
    area    :   0.0;
    interface_timing : TRUE;
    pin (I1)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      timing () {
timing_type : setup_rising;
```

```
intrinsic_rise : 1.0;
intrinsic_fall :  1.0;
related_pin : "CLK";
      }
      timing () {
timing_type : hold_rising;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
related_pin : "CLK";
      }
    }
    pin (CLK)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      clock : true;
      timing () {
timing_type : skew_rising;
intrinsic_rise : 1.0;
related_pin : "CLK1";
      }
    }

    pin (CLK1)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      timing () {
timing_type : skew_falling;
intrinsic_rise : 1;
related_pin : "CLK";
      }
    }
    pin(Q){
      direction   :   output;
      timing () {
intrinsic_rise   : 1.0;
rise_resistance  : 0.1;
intrinsic_fall   : 1.0;
fall_resistance  : 0.1;
related_pin      : "CLK";
      }
    }
  }
```

In this case, the ’CLK’ pin has a timing group with a timing_group value skew_rising related to the ’CLK1’ pin.

EXAMPLE MESSAGE

```
Warning: Line 40, A sequential timing arc is specified with respect
to the ’CLK1’  nonclock pin. (LBDB-354)
```

LBDB-355 (warning) A skew constraint is specified for the nonclock ’%s’ pin.

DESCRIPTION

A skew constraint is specified for a pin that is not a clock. All clock pins must have the **clock** attribute set to TRUE.

WHAT NEXT

Make sure that skew constraints are defined for clock pins only. Check the library source file, and either set the **clock** attribute to TRUE on the pin, or remove the skew constraint.

EXAMPLES

```
  cell (lbdb355) {
    area    :   0.0;
    interface_timing : TRUE;
    pin (I1)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      timing () {
timing_type : setup_rising;
intrinsic_rise : 1.0;
intrinsic_fall :  1.0;
related_pin : "CLK";
      }
      timing () {
timing_type : hold_rising;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
related_pin : "CLK";
      }
    }
    pin (CLK)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      clock : true;
      timing () {
timing_type : skew_rising;
intrinsic_rise : 1.0;
related_pin : "CLK1";
      }
    }

    pin (CLK1)    {
      direction   :   input;
      capacitance :   1.0;
```

```
      fanout_load :   1.0;
      timing () {
timing_type : skew_falling;
intrinsic_rise : 1;
related_pin : "CLK";
      }
    }
    pin(Q){
      direction   :   output;
      timing () {
intrinsic_rise   : 1.0;
rise_resistance  : 0.1;
intrinsic_fall   : 1.0;
fall_resistance  : 0.1;
related_pin      : "CLK";
      }
    }
  }
```

In this case, the ’CLK1’ pin has skew constraint timing group on the nonclock ’CLK’ pin. Because Library Compiler failed to recognize the ’CLK’ pin.

EXAMPLE MESSAGE

Warning: Line 52, A skew constraint is specified for the nonclock ’CLK1’ pin. (LBDB-355)

LBDB-356 (warning) Multiple %s constraints are specified between the ’%s’ pin and the ’%s’ clock pin.

DESCRIPTION

Design Compiler takes the worst case constraint when multiple constraints are specified.

WHAT NEXT

PrimeTime supports multiple setup/hold constraints.

EXAMPLES

```
  cell (lbdb356) {
    area    :   0.0;
    interface_timing : TRUE;
    pin (I1)    {
      direction   :   input;
      capacitance :   1.0;
```

```
      fanout_load :   1.0;
      timing () {
timing_type : setup_rising;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
related_pin : "CLK";
      }
      timing () {
timing_type : hold_rising;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
related_pin : "CLK";
      }
      timing () {
timing_type : hold_falling;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
related_pin : "CLK";
      }
    }
    pin (CLK)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      clock : true;
    }
    pin(Q){
      direction   :   output;
      timing () {
timing_type      : rising_edge;
intrinsic_rise   : 1.0;
rise_resistance  : 0.1;
intrinsic_fall   : 1.0;
fall_resistance  : 0.1;
related_pin      : "CLK";
      }
    }
  }
```

In this case, the ’I1’ pin has two hold constraints.

EXAMPLE MESSAGE

```
Warning: Line 31, Multiple setup or hold constraints are specified
between the ’I1’ pin and the ’CLK’ clock pin. (LBDB-356)
```

LBDB-357 (warning) The ’%s’ cell has the interface_timing attribute,

but has no clock pin.

DESCRIPTION

According to interface timing specification policy, a library cell with the interface timing attribute set to TRUE must have at least one pin labeled as a clock.

WHAT NEXT

If the cell is combinational, remove the **interface_timing** attribute set on the cell. If the cell is sequential in nature, add the **clock** attribute to all clock pins of the cell. If the cell does not have a clock pin (like a RAM), choose the control pin with respect to which setups and holds are measured, and label it as a clock.

EXAMPLES

```
  cell (lbdb357) {
    area    :   0.0;
    interface_timing : TRUE;
    pin (I1)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
    }
    pin(Q){
      direction   :   output;
      function : "I1'";
      timing () {
intrinsic_rise   : 1.0;
rise_resistance  : 0.1;
intrinsic_fall   : 1.0;
fall_resistance  : 0.1;
related_pin      : "I1";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Warning: Line 6, The 'combo' cell has the interface_timing attribute,
but has no clock pin. (LBDB-357)
```

LBDB-358 (error) It is not legal to specify the attribute '%s' in

the ’%s’ group in this context.

DESCRIPTION

The indicated attribute cannot be specified in the indicated group because of the context. This situation can arise if the group can have several types and the attribute can only appear when the group is of specific type.

WHAT NEXT

Check your library to see if you have specified the wrong information for the group or if the attribute should be deleted from the group.

LBDB-370 (error) The library contains a ’%s’ group, but has no contain ’%s’ group.

DESCRIPTION

This message indicates that you specified only one transition degradation table in the library. Libraries that contain transition degradation tables must have tables for both rise and fall transitions.

WHAT NEXT

Add the missing table group to the library description.

EXAMPLES

```
rise_transition_degradation(trans_deg) {
values("0.0, 0.6",
       "1.0, 1.6");
}
```

In this case, the ’fall_transition_degradation’ group is missing. To fix the problem, add this group to the library,

```
fall_transition_degradation(trans_deg) {
values("0.0, 0.8",
       "1.0, 1.8");
}
```

EXAMPLE MESSAGE

Error: Line 46, The library contains a ’rise_transition_degradation’ group, but has no ’fall_transition_degradation’ group. (LBDB-370)

LBDB-371 (error) The '%s' lut group is missing the mandatory '%s' attribute.

DESCRIPTION

This message indicates that you specified a lut group without the input_pins attribute in a FPGA library.

WHAT NEXT

Check the library source file, and add the missing attribute.

EXAMPLES

```
  cell(lut5) {
    area : 1.0;
    lut(lbdb371) {
      /*      input_pins : "a b c d e"; */
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
    pin(o) {
      direction : output;
      function : "lbdb371";
      timing() {
related_pin : "a b c d e";
      }
    }
  }
```

EXAMPLE MESSAGE

Error: Line 98, The 'lbdb371' lut group is missing the mandatory 'input_pins' attribute. (LBDB-371)

LBDB-372 (error) The '%s' lut group attribute has an invalid '%s' value.

DESCRIPTION

This message indicates that you specified a lut group with an invalid value for the input_pins attribute in a FPGA library.

WHAT NEXT

Check the library source file, and correct the value of the input_pins attribute.

EXAMPLES

```
  cell(lut5) {
    area : 1.0;
    lut(R) {
    input_pins : "";
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
related_pin : "a b c d e";
      }
    }
  }
```

EXAMPLE MESSAGE

Error: Line 98, The ’input_pins’ lut group attribute has an invalid ’’ value. (LBDB-372)

LBDB-373 (error) The ’%s’ cell has more than one lut group defined.

DESCRIPTION

This message indicates that you specified more than one lut group in the FPGA library.

WHAT NEXT

Check the library source file, and delete the extra lut groups.

EXAMPLES

```
  cell(lbdb373) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e";
    }
```

```
    lut(R1) {
      input_pins : "a b c d e";
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
related_pin : "a b c d e";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 96, The 'lbdb373' cell has more than one lut group defined. (LBDB-373)
```

LBDB-374 (error) The '%s' input port is not in the '%s' lut.

DESCRIPTION

This message indicates that you did not specify an input port in lut group.

WHAT NEXT

Check the library source file, and either add the input port to the lut group or delete the port.

EXAMPLES

```
  cell(lbdb374) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e";
    }
    pin(a b c d e f) {
      direction : input;
      capacitance : 0.0;
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
related_pin : "a b c d e";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 101, The ’f’ input port is not in the ’lbdb374’ lut. (LBDB-374)
```

LBDB-375 (error) The ’%s’ port is incorrectly listed as an input in the ’%s’ lut.

DESCRIPTION

This message indicates that you specified a noninput port in the lut group.

WHAT NEXT

Check the library source file, and delete the noninput port from the lut group.

EXAMPLES

```
  cell(lbdb375) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e o";
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
related_pin : "a b c d e";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 98, The ’o’ port is incorrectly listed as an input in the
’lbdb375’ lut. (LBDB-375)
```

LBDB-376 (error) The ’%s’ port is invalid in a cell containing a

lut group.

DESCRIPTION

This message indicates that you specified an invalid port in a cell containing a lut group. Ports in a cell with a lut are either input or output.

WHAT NEXT

Check the library source file, and correct the direction of the port.

EXAMPLES

```
  cell(lbdb376) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e ";
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
    pin(f) {
      direction : inout;
      capacitance : 0.0;
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
related_pin : "a b c d e";
      }
    }
  }
```

EXAMPLE MESSAGE

Error: Line 105, The ’f’ port is invalid in a cell containing a lut group. (LBDB-376)

LBDB-377 (error) The ’%s’ lut group is invalid in a multiple output cell.

DESCRIPTION

This message indicates that you specified more than one output port in a cell containing a lut group.

WHAT NEXT

Check the library source file, and delete the extra output ports.

EXAMPLES

```
  cell(lbdb377) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e ";
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
    pin(f) {
      direction : output;
      function : "R";
      timing() {
related_pin : "a b c d e";
      }
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
related_pin : "a b c d e";
      }
    }
  }
```

In this case, both ’f’ and ’o’ are output ports.

EXAMPLE MESSAGE

Error: Line 98, The ’R’ lut group is invalid in a multiple output cell. (LBDB-377)

LBDB-378 (error) The ’%s’ lut group is invalid in a cell with no outputs.

DESCRIPTION

This message indicates that you did not specify any output port in a cell containing a lut group.

WHAT NEXT

Check the library source file, and either add the output port or delete the lut group.

EXAMPLES

```
cell(lbdb378) {
  area : 1.0;
  lut(R) {
    input_pins : "a b c d e ";
  }
  pin(a b c d e) {
    direction : input;
    capacitance : 0.0;
  }
}
```

In this case, the 'lbdb378' has no output port.

EXAMPLE MESSAGE

Error: Line 98, The 'R' lut group is invalid in a cell with no outputs. (LBDB-378)

LBDB-379 (error) The '%s' output port on the '%s' cell has no function attribute, or the function attribute is invalid with the lut group on this cell.

DESCRIPTION

This message indicates that either you specified an invalid function attribute on the output port a cell containing a lut group, or you did not define the function attribute.

WHAT NEXT

Check the library source file, and either add or correct the function attribute.

EXAMPLES

```
cell(lbdb379) {
  area : 1.0;
  lut(R) {
    input_pins : "a b c d e ";
  }
  pin(a b c d e) {
    direction : input;
    capacitance : 0.0;
  }
  pin(o) {
    direction : output;
    timing() {
```

```
related_pin : "a b c d e";
      }
    }
  }
```

In this case, The function attribute is missing in the ’o’ port. To fix the problem, add the statement

```
     function : "R";
```

EXAMPLE MESSAGE

```
Error: Line 113, The ’o’ output port on the ’lbdb379’ cell has no
function attribute, or the function attribute is invalid with
the lut group on this cell. (LBDB-379)
```

LBDB-380 (error) The ’%s’ name is invalid for a lut group in the ’%s’ cell because a port on the design has the same name.

DESCRIPTION

This message indicates that there is a name conflict between the specified lut group name and a port name. The names of the lut groups must be unique and must not conflict with existing port names.

WHAT NEXT

Change the name of the lut group so that it is unique.

EXAMPLES

```
  cell(lbdb380) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e";
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
    pin(R) {
      direction : output;
      function : "R";
      timing() {
related_pin : "a b c d e";
```

```
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 98, The 'R' name is invalid for a lut group in the 'lbdb380'
cell because a port on the design has the same name. (LBDB-380)
```

LBDB-381 (error) The '%s' lut cell has %d input port(s). A lut cell must have at least 1 but no more than 9 input ports.

DESCRIPTION

This message indicates that the specified lut cell has either too many or too few input ports. lut cells must have at least 1 but not more than 9 input ports.

WHAT NEXT

Edit the lut cell description in your library so that the cell has at least 1 but not more than 9 input ports.

EXAMPLES

```
  cell(lbdb381) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e f g h i j";
    }
    pin(a b c d e f g h i j) {
      direction : input;
      capacitance : 0.0;
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
related_pin : "a b c d e f g h i j";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 98, The 'lbdb381' lut cell has 10 input port(s). A lut
cell must have at least 1 but no more than 9 input ports. (LBDB-381)
```

LBDB-382 (error) The ’%s’ cell is an invalid lut cell. Only simple combinational cells are valid.

DESCRIPTION

This message indicates that the specified cell is not a simple combinational cell, which is the only valid type of lut cell.

WHAT NEXT

Remove the lut construct from this cell description, or modify the cell so that it is a simple combinational cell.

EXAMPLES

```
  cell(lbdb382) {
    area : 1.0;
    lut(R) {
      input_pins : "D CP";
    }
    pin(D CP ) {
      direction : input;
      capacitance : 0.0;
    }
    ff("IQ","IQN") {
      next_state : "D";
      clocked_on : "CP";
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
related_pin : "D CP";
      }
    }
  }
```

EXAMPLE MESSAGE

Error: Line 96, The ’lbdb382’ cell is an invalid lut cell. Only simple combinational cells are valid. (LBDB-382)

LBDB-383 (error) The ’%s’ attribute is invalid on

the ’%s’ lut cell.

DESCRIPTION

This message indicates that the specified attribute is not valid on the specified lut cell.

WHAT NEXT

Remove the offending attribute from the lut cell.

EXAMPLES

```
cell(lbdb383) {
    area : 1.0;
    fpga_lut_output : true;
    lut(R) {
      input_pins : "A B C D";
    }
    pin(A B C D) {
direction : input;
capacitance : 0.0;
    }
    pin(Z) {
direction : output;
function : "R";
timing() {
    intrinsic_rise : 5.0;
    intrinsic_fall : 5.0;
    related_pin : "A B C D";
}
    }
}
```

EXAMPLE MESSAGE

```
Error: Line 25, The ’fpga_lut_output’ attribute is invalid on
the ’lbdb383’ lut cell.  (LBDB-383)
```

LBDB-384 (error) The lut marker cell attribute ’%s’ is invalid on the ’%s’ cell.

DESCRIPTION

This message indicates that a lut marker cell attribute has been found on the specified cell, identifying it as a lut marker cell. However, the cell is not a valid candidate for a lut marker cell because it is not a single output buffer cell

with 0 area.

Lut marker cells delimit the boundaries of luts and must be single-output buffer cells with 0 area.

WHAT NEXT

Either remove the lut marker cell attribute from the cell, or edit the cell description to make it a valid marker cell; that is, a single output buffer cell with 0 area.

EXAMPLES

```
  cell(lbdb384) {
    area : 0.0;
    fpga_lut_insert_before_sequential : true;
    pin(A) {
      direction : input;
      capacitance : 0.0;
    }
    pin(Z) {
      direction : output;
      function : "A";
      timing() {
intrinsic_rise : 0.0;
intrinsic_fall : 0.0;
related_pin : "A";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 126, The lut marker cell attribute
'fpga_lut_insert_before_sequential' is invalid on the 'lbdb384' cell. (LBDB-384)
```

LBDB-385 (error) The lut marker '%s' cell is functionally invalid. Lut marker cells must be single output buffers.

DESCRIPTION

This message indicates that the specified marker cell is not a single output buffer, which is the only valid lut marker cell type.

WHAT NEXT

Remove the marker cell attribute from the cell, or change the cell's functionality so that it is a single output buffer.

EXAMPLES

```
  cell(lbdb385) {
    area : 0.0;
    fpga_lut_output : true;
    pin(A) {
      direction : input;
      capacitance : 0.0;
    }
    pin(Z1) {
      direction : output;
      function : "A";
      timing() {
intrinsic_rise : 0.0;
intrinsic_fall : 0.0;
related_pin : "A";
      }
    }
    pin(Z2) {
      direction : output;
      function : "A";
      timing() {
intrinsic_rise : 0.0;
intrinsic_fall : 0.0;
related_pin : "A";
      }
    }
  }
```

In this case, there are two output ports in the cell.

EXAMPLE MESSAGE

```
Error: Line 143, The lut marker 'lbdb385' cell is functionally invalid.
Lut marker cells must be single output buffers. (LBDB-385)
```

LBDB-386 (warning) The lut marker '%s' cell has a nonzero '%s' attribute. Marker cells must have zero area and zero delay.

DESCRIPTION

This message indicates that the specified area or delay value in the library is nonzero, which is invalid for lut marker cells.

WHAT NEXT

Change the offending nonzero value (area or delay, as appropriate) to zero.

EXAMPLES

```
  cell(lbdb386) {
    area : 0.0;
    fpga_lut_output : true;
    pin(A) {
      direction : input;
      capacitance : 0.0;
    }
    pin(Z) {
      direction : output;
      function : "A";
      timing() {
intrinsic_rise : 1.0;
intrinsic_fall : 0.0;
related_pin : "A";
      }
    }
  }
```

In this case, the 'intrinsic_rise' value is 1.0. Change the value to zero to fix the problem.

EXAMPLE MESSAGE

```
Warning: Line 169, The lut marker 'lbdb386' cell has a nonzero
'intrinsic rise delay' attribute. Marker cells must have
zero area and zero delay. (LBDB-386)
```

LBDB-387 (warning) The '%s' library has more than one lut output marker cell.

DESCRIPTION

This message indicates that the specified library has too many lut output marker cells. Each library can have only one lut output marker cell.

WHAT NEXT

Check the library source file, and remove the duplicate output marker cells.

EXAMPLES

```
library(lbdb387) {
  ...
  cell(marker1) {
    area : 0.0;
    fpga_lut_output : true;
    pin(A) {
```

```
      direction : input;
      capacitance : 0.0;
    }
    pin(Z) {
      direction : output;
      function : "A";
      timing() {
intrinsic_rise : 0.0;
intrinsic_fall : 0.0;
related_pin : "A";
      }
    }
  }

  cell(marker2) {
    area : 0.0;
    fpga_lut_output : true;
    pin(A) {
      direction : input;
      capacitance : 0.0;
    }
    pin(Z) {
      direction : output;
      function : "A";
      timing() {
intrinsic_rise : 0.0;
intrinsic_fall : 0.0;
related_pin : "A";
      }
    }
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 56, The 'lbdb387' library has more than one lut output marker cell. (
LBDB-387)
```

LBDB-388 (error) The '%s' attribute cannot be specified in a timing arc that is not a timing constraint.

DESCRIPTION

This message indicates that an attribute has been incorrectly specified. The specified attribute is allowed only on timing arcs that are timing constraints (for example, setup and hold).

WHAT NEXT

Check the library source file, and make the appropriate correction. For example, change the timing type to be a timing constraint.

EXAMPLES

```
    pin(Q) {
      direction : output;
      function : "IQ";
      timing() {
        timing_type : falling_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
when_end : "D0";
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "CK2";
      }
    }
```

In this case, the ’falling_edge’ timing_type value is not a constraint.

EXAMPLE MESSAGE

```
Error: Line 94, The ’when_end’ attribute cannot be specified in a
timing arc that is not a timing constraint. (LBDB-388)
```

LBDB-389 (error) This timing arc has either ’%s’ or ’%s’ attribute but not both.

DESCRIPTION

This message indicates that in a timing group, you defined only one attribute from the following sets:

* when attribute and sdf_cond attribute
* when_start attribute and sdf_cond_start attribute
* when_end attribute and sdf_cond_end attribute

To define a state dependent timing arc, Library Compiler expects both attributes defined.

WHAT NEXT

Complete your specification by adding appropriate attributes to the timing group.

EXAMPLES

```
      pin(Z) {
direction : output;
function : "A^B";
timing() {
  when : "B'";
  timing_sense : positive_unate;
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "A";
}
```

In this case, only the 'when' attribute is specified. To fix the problem, add the statement,

```
  sdf_cond : "!B";
```

EXAMPLE MESSAGE

```
Error: Line 88, This timing arc has either 'when' or 'sdf_cond'
        attribute but not both. (LBDB-389)
```

LBDB-390 (warning) The when and/or sdf_cond attributes in this timing arc are ignored.

DESCRIPTION

This message indicates that you specified, in addition to the **when_start**, **when_end**, **sdf_cond_start**, or **sdf_cond_end** attributes in the timing (constraint) group, the **when** and **sdf_cond** attributes. Library Compiler ignores the **when** and **sdf_cond** attributes.

WHAT NEXT

Remove the redundant **when** and/or **sdf_cond** attributes from the timing group.

EXAMPLES

```
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      sdf_edges : start_edge;
      when : " CD * SD ";
```

```
      sdf_cond : " SIG_2 == 1'b1 ";
      when_end : " CD * SD * Q' ";
      sdf_cond_end : " SIG_0 == 1'b1";
      related_pin : "CP";
    }
```

In this case, both the when and sdf_cond pair and the when_end and sdf_cond_end are specified.

EXAMPLE MESSAGE

```
Warning: Line 836, The when and/or sdf_cond attributes in this
timing arc are ignored. (LBDB-390)
```

LBDB-391 (warning) The '%s' attribute on pin '%s' is not valid. The attribute is ignored.

DESCRIPTION

This message indicates that the attribute on the specified pin is invalid. The attribute is ignored. This situation occurs when other information specified on the same pin is incompatible with the attribute. For example, the **min_period** attribute is ignored if the **minimum_period** group is also specified on the same pin.

WHAT NEXT

Refer to the **Library Compiler Reference Manual** to determine the reason why the attribute is not valid. Change the library source file and make the correction.

EXAMPLES

```
pin (CLK) {
  direction : input ;
  capacitance : 0 ;
  min_pulse_width_low  : 3 ;
  min_pulse_width_high : 3 ;
  min_period : 5.0;
  minimum_period() {
    constraint : 1.0;
    when : "D PRE";
    sdf_cond : "cond_1 == 1'b1";
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 183, The 'min_period' attribute on the 'CLK' pin is not valid.
The attribute is ignored. (LBDB-391)
```

LBDB-392 (error) The ECL Technology is obsolete with v3.4b. Compilation terminated abnormally.

DESCRIPTION

This error occurs when the ECL Technology is used. This technology is supported up to v3.4a but not for subsequent releases.

WHAT NEXT

Use the supported technologies.

EXAMPLES

```
library(lbdb392) {
  technology(ecl);
  delay_model : "generic_ecl" ;
}
```

EXAMPLE MESSAGE

Error: The ECL Technology is obsolete with v3.4b. Compilation terminated abnormally . (LBDB-392)

LBDB-393 (error) Too many values entered for the driver_type attribute.

DESCRIPTION

This error occurs when more than two values entered for a driver_type attribute in defining a simple attribute.

WHAT NEXT

Only inout pin allows for two driver_type values. Other pins can have only one value. During passing, we first catch the case where more than two are entered.

EXAMPLES

```
    pin(y) {
      direction : inout;
      function : 1;
      three_state : "a";
      driver_type : "open_source pull_down resistive";
      timing() {
```

```
        timing_type : three_state_disable;
        related_pin : "a";
      }
      timing() {
        related_pin : "a";
      }
    }
```

In the driver_type line, three driver_types are specified for this pin.

EXAMPLE MESSAGE

Error: Line 458, Too many values entered for the driver_type attribute. (LBDB-393)

LBDB-394 (error) The driver type %s is incompatible with the %s pin %s.

DESCRIPTION

Valid driver-type (programmable or non-programmable) and pin combinations (Y means valid):

non-programmable input output inout programmable
========== pull_up Y Y Y pull_up_function pull_down Y Y Y pull_down_function open_drain N Y Y open_drain_function open_source N Y Y open_source_function bus_hold N N Y bus_hold_function resistive N Y Y resistive_function resistive_0 N Y Y resistive_0_function resistive_1 N Y Y resistive_1_function open_drain_with_pull_up N N Y open_drain_with_pull_down N N Y open_source_with_pull_up N N Y open_source_with_pull_down N N Y
==========

WHAT NEXT

When single pull_up/down applys to an inout pin, it is for the input behavior; other single types applying to an inout pin are for the output behavior. Always comply with the above rules.

EXAMPLES

```
    pin(a) {
      direction : input;
      capacitance : "1";
      driver_type : "open_source pull_up";
    }
```

EXAMPLE MESSAGE

```
Error: Line 177, The driver type open_source_with_pull_up is incompatible
        with the input pin a. (LBDB-394)
```

EXAMPLES

```
 pin(A3) {
  direction : input;
  pull_up_function : "!A1 * !A2 * !A3";
  pull_down_function : "A1 * A2 * !A3";
  bus_hold_function : "A1 * !A2 * !A3";
  open_drain_function : "!A1 * A2 * !A3";
  open_source_function : "!A1 * !A2 * A3";
  resistive_function : "A1 * A2 * A3";
  resistive_0_function : "A1 * !A2 * A3";
  resistive_1_function : "!A1 * A2 * A3";
  ...
 }
```

In this case, only pull_up_function and pull_down_function can be specified under an input pin. To avoid the error, please remove the rest of 6 programmable driver types.

EXAMPLE MESSAGE

```
Error: Line 217, The driver type open_drain_function is incompatible with the input
 pin A3. (LBDB-394)
```

LBDB-395 (warning) The timing arc with timing_type '%s' can only be specified on a pin with 'input' or 'inout' direction.

DESCRIPTION

The timing_type non_seq_setup_rising, non_seq_setup_falling, non_seq_hold_rising and non_seq_hold_falling can only be specified on a timing arc on the input or the inout pins.

WHAT NEXT

Check the timing arc and make the correction to either the direction of the pin or delete the timing arc or move it to the appropriate place.

EXAMPLES

```
pin(Z) {
  direction : output;
  timing() {
          timing_type : non_seq_setup_rising;
```

```
    ...
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 144, The timing arc with timing_type 'non_seq_setup_rising' can only
be specified on a pin with 'input' or 'inout' direction. (LBDB-395)
```

LBDB-396 (warning) The 'related_output_pin' attribute is only needed when the delay table refers to a template which uses the output loading of the related_output_pin in one of its dimension.

DESCRIPTION

```
This can happen when the 'related_output_pin' is not needed in this timing arc or
the template name used by this table is wrong or the template itself should use the
output loading of the related_output_pin in one of its dimension.
```

WHAT NEXT

```
Check the table or the template to see if the related_output_pin attribute is
actually needed here. If not, just delete the attribute.
```

EXAMPLES

```
lu_table_template(prop) {
        variable_1 :  output_net_length;
        index_1 ("1, 5, 10");
}

cell(A) {

  pin(O) {
    timing() {
            related_output_pin : "Z";
      rise_propagation(prop) {
        ...
      }
    }
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 144, The 'related_output_pin' attribute is only needed when the delay
table refers to a template which uses the output loading of the related_output_pin
in one of its dimension. (LBDB-396)
```

```
The timing arc is a rise_propagation table which refers to the template 'prop'. In
the template, the only variable it depends on is the loading of the output pin.
There is not dependency on the loading of pin 'Z' and there is no need to put the
'related_output_pin' in the timing group.
```

LBDB-397 (error) There can only be one pin in the 'related_output_pin' attribute and the pin should be single bit.

DESCRIPTION

```
The "related_output_pin" attribute is used for figuring out the output loading to
index into the table. It is not possible to determine which output pin to use for
this purpose if there is more than one pin specified in the attribute. Multiple bits
specification also have the same problem.
```

WHAT NEXT

```
Check the 'related_output_pin' attribute and make the correction according to the
real electrical characteristics.
```

EXAMPLES

```
timing() {
        related_output_pin : "Z1 Z2";
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 144, There can only be one pin in the 'related_output_pin' attribute and
the pin should be single bit. (LBDB-397)
```

```
There are two pins, Z1 and Z2, in the related_output_pin attribute. It is not
possible to figure out which pin should be used to figuring out the loading to index
into the timing table.
```

LBDB-398 (error) The pin '%s' specified in the

’related_output_pin’ attribute is not an output or inout pin.

DESCRIPTION

The pin specified in the ’related_output_pin’ attribute should have the direction ’output’ or ’inout’.

WHAT NEXT

Check the ’related_output_pin’ attribute to see if you have put the wrong pin in it or you forgot to put the correct pin direction on the pin specified in the ’related_output_pin’ attribute.

EXAMPLES

```
pin(A) {
  direction : input;
  ...
}
pin(B) {
  timing() {
    related_output_pin : "A";
    ...
  }
}
```

EXAMPLE MESSAGE

Error: Line 144, The pin ’A’ specified in the ’related_output_pin’ attribute is not an output or inout pin. (LBDB-398)

Pin ’A’ is an input pin and cannot be put into the ’related_output_pin’ attribute.

LBDB-399 (error) The timing_type ’%s’ is not supported with the ’related_output_pin’ attribute.

DESCRIPTION

The timing_type supported with the ’related_output_pin’ attribute are: ’setup_rising’, ’setup_falling’, ’hold_rising’, ’hold_falling’, ’non_seq_setup_rising’, ’non_seq_setup_falling’, ’non_seq_hold_rising’, ’non_seq_hold_falling’, ’skew_rising’, ’skew_falling’, ’removal_rising’, ’removal_falling’, ’recovery_rising’ and ’recovery_falling’.

WHAT NEXT

You may either put the wrong timing_type for the timing group or delete the timing group if it is not supported or the 'related_output_pin' attribute is not needed.

EXAMPLES

```
timing() {
  timing_type : rising_edge;
  related_output_pin : "A";
  ...
}
```

EXAMPLE MESSAGE

Error: Line 144, The timing_type 'rising_edge' is not supported with the 'related_output_pin' attribute.. (LBDB-399)

LBDB-400 (warning) The '%s' operating condition has been defined multiple times in the '%s' library. Design Compiler will use the first definition only.

DESCRIPTION

The library contains more than one definition of an operating condition. Library Compiler issues this error message, records all definitions, but Design Compiler will only use the first definition encountered.

WHAT NEXT

Change the operating condition name if it is wrong, or delete all extra definitions.

EXAMPLES

```
  operating_condition(P1V1) {
    ...
  }
  operating_condition(P1V1) {
    ...
  }
```

EXAMPLE MESSAGE

```
Warning: Line 50, The 'P1V1' operating condition has been defined
multiple times in the 'sample-library' library.
Design compiler will use the first one only. (LBDB-400)
```

LBDB-401 (error) The '%s' is missing for this timing check.

DESCRIPTION

Both rise and fall constraint values are required in the nochange timing check.

WHAT NEXT

Check the library source file to see if you missed the rise or fall constraint value. Otherwise, use setup or hold check instead.

EXAMPLES

```
    pin ( EN )    {
      direction : input;
      timing ()      {
timing_type : nochange_high_high;
        related_pin : CP ;
        rise_constaint(cons) {
          values("0.100000, 0.100000, 0.100000",  \

 "0.100000, 0.100000, 0.100000",  \

                 "0.100000, 0.100000, 0.100000",  \

                 "0.100000, 0.100000, 0.100000",  \

                 "0.100000, 0.100000, 0.100000");
        }
      }
    }
```

To fix the problem, add the attribute to the timing group,

```
        fall_constraint(cons) {
          values("0.100000, 0.100000, 0.100000",  \

 "0.100000, 0.100000, 0.100000",  \

                 "0.100000, 0.100000, 0.100000",  \

                 "0.100000, 0.100000, 0.100000",  \

                 "0.100000, 0.100000, 0.100000");
        }
```

EXAMPLE MESSAGE

```
Error: Line 104, The 'fall_constraint' is missing for this timing check. (LBDB-401)
```

LBDB-402 (error) The '%s' is missing for this internal_power group.

DESCRIPTION

Internal_power groups require specification of either (1) both the rise_power and fall_power attributes; or (2) the power attribute.

WHAT NEXT

Check the library source file to see if you missed the rise_power, fall_power, or power attribute.

EXAMPLES

```
    pin ( EN )    {
      direction : input;
      internal_power ()      {
        rise_power(power_1d_temp) {
          values("0.100000, 0.100000, 0.100000");
        }
      }
    }
```

To fix the problem, add the attribute to the internal_power group.

```
        fall_power(power_1d_temp) {
          values("0.100000, 0.100000, 0.100000");
        }
```

EXAMPLE MESSAGE

```
Error: Line 104, The 'fall_power' is missing for this internal_power group. (LBDB-
402)
```

LBDB-403 (error) The '%s' and '%s' attributes are both defined for this

internal_power group.

DESCRIPTION

Internal_power groups require specification of either (1) both the rise_power and fall_power attributes; or (2) the power attribute.

However, it is an error to mix style (1) and (2).

WHAT NEXT

Check the library source file to make sure that the previous requirement is met.

EXAMPLES

```
    pin ( EN )    {
      direction : input;
      internal_power ()      {
        power(power_1d_temp) {
          values("0.100000, 0.100000, 0.100000");
        }
        rise_power(power_1d_temp) {
          values("0.100000, 0.100000, 0.100000");
        }
      }
    }
```

To fix the problem, remove the rise_power attribute from the internal_power group, or remove power attribute and add the following fall_power attribute from the internal_power group.

```
        fall_power(power_1d_temp) {
          values("0.100000, 0.100000, 0.100000");
        }
```

EXAMPLE MESSAGE

```
XXX
Error: Line 104, The 'rise_power' and 'power' attributes are both defined for this
       internal_power group. (LBDB-403)
```

LBDB-404 (error) The '%s' lookup table in the input-associated internal_power group cannot use '%s' as its template.

DESCRIPTION

The rise_power, fall_power, or power lookup tables in a input-associated

internal_power group must use 1-dimensional template with input_transition_time as its variable.

WHAT NEXT

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

EXAMPLES

```
  power_lu_template(ok_temp) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
  }
  power_lu_template(err_temp) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");
  }

power(err_temp) {
values ("1, 2, 3, 4");
}
```

To fix the problem, change the template value of the power attribute from err_temp to ok_temp.

EXAMPLE MESSAGE

```
Error: Line 126, The 'power' lookup table in the input-associated
       internal_power group cannot use 'err_temp' as its template. (LBDB-404)
```

LBDB-405 (error) The 1-dimensional '%s' lookup table in the inout-associated internal_power group cannot use '%s' as its template.

DESCRIPTION

The 1-dimensional rise_power, fall_power, or power lookup tables in an inout-associated internal_power group must use a template with input_transition_time or total_output_net_capacitance as its variable.

WHAT NEXT

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

EXAMPLES

```
power_lu_template(ok_temp) {
  variable_1 : input_transition_time;
  index_1("0, 1, 2, 3");
}
power_lu_template(ok2_temp) {
  variable_1 : total_output_net_capacitance;
  index_1("0, 1, 2, 3");
}
power_lu_template(err_temp) {
  variable_1 : output_net_length;
  index_1("0, 1, 2, 3");
}

      power(err_temp) {
              values ("1, 2, 3, 4");
      }
```

To fix the problem, change the template value of the power attribute from err_template to ok_temp or ok2_temp.

EXAMPLE MESSAGE

```
Error: Line 126, The 1-dimensional 'power' lookup table in the
      inout-associated internal_power group cannot use
'basic_template' as its template. (LBDB-405)
```

LBDB-406 (error) The 1-dimensional '%s' lookup table in the %s-associated internal_power group cannot use '%s' as its template.

DESCRIPTION

The 1-dimensional rise_power, fall_power, or power lookup tables in an output-associated internal_power group must use a template with total_output_net_capacitance as its variable.

WHAT NEXT

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

EXAMPLES

```
power_lu_template(err_temp) {
```

```
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
  }
  power_lu_template(ok_temp) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");
  }

        power(err_temp) {
                values ("1, 2, 3, 4");
        }
```

To fix the problem, change the template value of the power attribute from err_template to ok_temp.

EXAMPLE MESSAGE

```
Error: Line 126, The 1-dimensional 'power' lookup table in the
output-associated internal_power group cannot use 'err_temp' as its template. (LBDB-
406)
```

LBDB-407 (error) The 2-dimensional '%s' lookup table in the %s-associated internal_power group cannot use '%s' as its template.

DESCRIPTION

The 2-dimensional rise_power, fall_power, or power lookup tables in an output-associated internal_power group must use a template with input_transition_time and total_output_net_capacitance as its variables.

WHAT NEXT

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

EXAMPLES

```
  power_lu_template(ok_temp) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
    variable_2 : total_output_net_capacitance;
    index_2("0, 1, 2, 3");
  }
  power_lu_template(err_temp) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");
```

```
    variable_2 : constrained_pin_transition;
    index_2("0, 1, 2, 3");
  }

power(err_temp) {
values ("1, 2, 3, 4", "5, 6, 7, 8", \

"9, 10, 11, 12", "13, 14, 15, 16");
}
```

To fix the problem, change the template value of the power attribute from err_temp to ok_temp.

EXAMPLE MESSAGE

```
Error: Line 126, The 2-dimensional 'power' lookup table in the
output-associated internal_power group cannot use 'err_temp' as its template. (LBDB-
407)
```

LBDB-408 (error) The 3-dimensional '%s' lookup table in the %s-associated internal_power group cannot use '%s' as its template.

DESCRIPTION

The 3-dimensional rise_power, fall_power, or power lookup tables in an output-associated internal_power group must use a template with input_transition_time, total_output_net_capacitance and equal_or_opposite_output_net_capacitance as its variables.

WHAT NEXT

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

EXAMPLES

```
  power_lu_template(ok_temp) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2");
    variable_2 : total_output_net_capacitance;
    index_2("0, 1, 2");
    variable_3 : equal_or_opposite_output_net_capacitance;
    index_3("0, 1, 2");
  }
  power_lu_template(err_temp) {
    variable_1 : total_output_net_capacitance;
```

```
    index_1("0, 1, 2");
    variable_2 : constrained_pin_transition;
    index_2("0, 1, 2");
    variable_3 : equal_or_opposite_output_net_capacitance;
    index_3("0, 1, 2");
  }

        power(err_temp) {
                values ("1,  2,  3",  "4,  5,  6",  "7, 8, 9", \

                        "10, 11, 12", "13, 14, 15", "16, 17, 18", \

"19, 20, 21", "22, 23, 24", "25, 26, 27");
        }
```

To fix the problem, change the template value of the power attribute from err_temp to ok_temp.

EXAMPLE MESSAGE

```
Error: Line 126, The 3-dimensional 'power' lookup table in the
output-associated internal_power group cannot use 'err_temp' as its template. (LBDB-
408)
```

LBDB-409 (error) The %d-dimensional template used in '%s' lookup table
is incompatible with the template used in '%s' lookup table.

DESCRIPTION

Both rise_power and fall_power lookup tables must have the same dimension. One exception is when the internal_power is an arc from a tri-state pin (that is related_pin is a tri-state pin), the dimension of rise_power and fall_power can be different.

WHAT NEXT

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

EXAMPLES

```
  power_lu_template(1d_temp) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");

  power_lu_template(2d_temp) {
```

```
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
    variable_2 : total_output_net_capacitance;
    index_2("0, 1, 2, 3");
  }

rise_power(1d_temp) {
                values ("1, 2, 3, 4");
        }
        fall_power(2d_temp) {
                values ("1, 2, 3, 4", "5, 6, 7, 8", \

                        "9, 10, 11, 12", "13, 14, 15, 16");
        }
```

To fix the problem, use 1-dimensional or 2-dimensional lookup tables on both rise_power and fall_power attributes.

EXAMPLE MESSAGE

```
Error: Line 126, The %d-dimensional template used in '%s' lookup table
is incompatible with the template used in '%s' lookup table. (LBDB-409)
```

LBDB-410 (error) The '%s' attribute is missing from the internal_power group.

DESCRIPTION

The related_pin or related_bus_pins attributes are required in an internal_power group with a 2-dimensional or 3-dimensional lookup table. The equal_or_opposite_output attribute is required in an internal_power group with a 3-dimensional look-up table.

WHAT NEXT

Change the library source file by specifying related_pin, related_bus_pins, or equal_or_opposite_output attribute in the internal_power group as needed.

EXAMPLES

```
    internal_power() {
      power(power_2d) {
values ("1, 2, 3, 4", "5, 6, 7, 8", \

"9, 10, 11, 12", "13, 14, 15, 16");
      }
    }
```

To fix the problem, add the following line into the internal_power group.

```
related_pin : "A";
```

EXAMPLE MESSAGE

```
Error: Line 126, The 'related_pin or related_bus_pins' attribute is missing
from the internal_power group. (LBDB-410)
```

LBDB-411 (error) The internal_power group associated with pin '%s' cannot coexist with the cell-associated internal_power group in line %d.

DESCRIPTION

It is not allowed to use cell-associated and pin-associated internal_power group for the same pin.

WHAT NEXT

Refer to the *Library Compiler User Guide* for more information about power modeling. Change the library source file by using either the cell-associated style or pin-associated style internal_power on the specified pin.

EXAMPLES

```
    cell(AN2) {
internal_power(power_1d_temp) {
    related_input : "A";
            values("0.100000, 0.100000, 0.100000");
}
      pin (A) {
    direction : input;
    internal_power () {
        power(power_1d_temp) {
              values("0.100000, 0.100000, 0.100000");
        }
    }
}
        ...
    }
```

To fix the problem, remove internal_power group associated with cell group or pin group.

EXAMPLE MESSAGE

```
Error: Line 126, The internal_power group associated with pin 'A'
cannot co-exist with the cell-associated internal_power group in line 120. (LBDB-
411)
```

LBDB-412 (error) There is a missing internal_power relation between pins '%s' and '%s' in the '%s' cell.

DESCRIPTION

This message indicates there is a missing internal_power relation from an input or inout pin to an output pin.

For a combinational cell, the Library Compiler checks that

* An output port with a function statement has internal_power relation to all functionally related inputs
* An output port with a three_state attribute has timing arcs to all three_state related inputs

However, Library Compiler will not check if internal_power information is completely missing in this output.

WHAT NEXT

Add the missing internal_power group between the two pins.

EXAMPLES

```
  cell(AN2) {
    pin(A, B) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "A B";
      internal_power () {
power (power_2d_temp) {
            values ("1, 2, 3, 4", "5, 6, 7, 8", \

                    "9, 10, 11, 12", "13, 14, 15, 16");
        }
related_pin : "A";
      }
      timing() {
...
```

```
      }
    }
  }
```

In this case, an internal_power group is missing between the pin ’Z’ and ’B’. To fix the problem, add the following internal_power group:

```
      internal_power () {
        power (power_2d_temp) {
            values ("1, 2, 3, 4", "5, 6, 7, 8", \

                    "9, 10, 11, 12", "13, 14, 15, 16");
        }
        related_pin : "B";
      }
```

EXAMPLE MESSAGE

```
Error: Line 12, There is a missing internal_power relation between
pins ’B’ and ’Z’ in the ’AN2’ cell. (LBDB-412)
```

LBDB-413 (error) There is an extra internal_power group between ’%s’ and ’%s’ pins in the ’%s’ cell.

DESCRIPTION

Internal_power groups are allowed for pins that are related to each other. To be related to each other, the input pin has to be in the **function** or **three_state** attribute of the output or input pin. This message is issued if the internal_power group identified between pins does not fall into the categories previously described.

WHAT NEXT

Check your library to see whether you have generated the internal_power group by mistake, whether the related_pin field is wrong, or the function attribute value is not recognized.

EXAMPLES

```
    pin(Z) {
      direction : output;
      function : "B";
      internal_power () {
        power (power_2d_temp) {
            values ("1, 2, 3, 4", "5, 6, 7, 8", \
```

```
                    "9, 10, 11, 12", "13, 14, 15, 16");
        }
        related_pin : "A B";
      }
      timing() {
...
      }
   }
```

In this case, you defined a internal_power group between the ’A’ and ’Z pins, even though the ’A’ pin is not functionally related to the ’Z’ pin. Remove the internal_power group or change the function statement of ’Z’ to include ’A’.

EXAMPLE MESSAGE

Warning: Line 73, There is an extra internal_power group between ’A’ and ’Z’ pins in the ’AN2’ cell. (LBDB-413)

LBDB-414 (error) In this internal_power group, the ’%s’ output pin in the ’%s’ attribute is not functionally equivalent or opposite to the ’%s’ pin.

DESCRIPTION

If an output is specified in the related_pin, related_bus_pins, or equal_or_opposite_output attributes, this output must be functionally equivalent or opposite of the output pin which owns the internal_power.

WHAT NEXT

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

EXAMPLES

```
  cell(AN2) {
    pin(A, B) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "A B";
```

```
      internal_power () {
        power (power_3d_temp) {
                values ("1, 2, 3", "4, 5, 6", "7, 8, 9", \

                        "10, 11, 12", "13, 14, 15", "16, 17, 18", \

                        "19, 20, 21", "22, 23, 24", "25, 26, 27");
        }
        related_pin : "A B";
equal_or_opposite_output : "Y";
      }
      timing() {
        ...
      }
    }
    pin(Y) {
      direction : output;
      function : "A + B";
      timing() {
        ...
      }
    }
  }
```

To fix the problem, remove equal_or_opposite_output attribute from the internal_power group and use 2-dimensional lookup table; or make sure 'Y' is functionally equivalent or opposite to 'Z'.

EXAMPLE MESSAGE

```
Error: Line 126, In this internal_power group, the 'Y' output pin in
the 'equal_or_opposite_output' attribute is not functionally equivalent
or opposite to the 'Z' pin. (LBDB-414)
```

LBDB-415 (error) The '%s' attribute cannot be specified in this internal_power group.

DESCRIPTION

This message indicates you specified an attribute outside its context.

(1) An internal_power group with 1-dimensional look-up tables cannot specify related_pin, related_bus_pins, or equal_or_opposite_output attributes.
(2) An internal_power group with 2-dimensional look-up tables cannot specify an equal_or_opposite_output attribute.

One exception is when the internal_power is an arc from a tri-state pin (that is related_pin is a tri-state pin), the checker is diabled.

WHAT NEXT

Change the technology library source file to delete the specified attribute or move the attribute to its correct context.

EXAMPLES

```
    internal_power() {
        power(power_1d_temp) {
                values ("1, 2, 3, 4");
        }
related_pin : "A";
    }
```

In this case, the ’related_pin’ attribute is not allowed in 1-dimensional lookup table. To fix the problem, remove the related_pin attribute from internal_power group.

EXAMPLE MESSAGE

Error: Line 69, The ’related_pin or related_bus_pins’ attribute cannot be specified in this internal_power group. (LBDB-415)

LBDB-416 (error) The ’%s’ cell is missing cell_leakage_power attribute.

DESCRIPTION

This message indicates there is one or more state-dependent leakage_power attribute, but no cell_leakage_power attribute specified as default value. When at least one state-dependent leakage power is specified in a cell, the cell must have also cell_leakage_power attribute defined.

WHAT NEXT

Add the missing timing group between the two pins.

EXAMPLES

```
  cell(AN2) {
      leakage_power () {
when : "A";
value : 1.0;
      }
      ...
  }
```

In this case, a cell_leakage_power attribute is missing. To fix the problem, add the

following attribute to the cell group:

```
      cell_leakage_power : 0.5;
```

EXAMPLE MESSAGE

```
Error: Line 12, The 'AN2' cell is missing cell_leakage_power attribute. (LBDB-416)
```

LBDB-417 (error) Pin '%s' has a timing arc that appears on only one of
the scaled cell (%s,%s) and the cell '%s'.

DESCRIPTION

Timing arcs with the same pin pair and type must match by number between the scaled cell and the regular cell.

WHAT NEXT

Find the timing group in the scaled_cell and remove the extra timing groups or add more timing groups in the parent cell.

EXAMPLES

```
library(alib) {
    operating_conditions(WCCOM) {
process : 1.5 ;
        temperature : 70 ;
voltage : 4.75 ;
tree_type : "worst_case_tree" ;
    }
    cell(AND) {
      area : 1;
      pin(A B) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "A B";
timing() {
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A B";
```

```
}
      }
    }

    scaled_cell(AND,WCCOM) {
      area : 1;
      pin(A) {
direction : input;
capacitance : 1;
      }
      pin(B) {
direction : input;
capacitance : 1;
timing() {
  intrinsic_rise : 0.3;
  intrinsic_fall : 0.3;
  rise_resistance : 0.3;
  fall_resistance : 0.3;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A";
        }
      }
      pin(Z) {
direction : output;
function : "A B";
timing() {
  intrinsic_rise : 0.3;
  intrinsic_fall : 0.3;
  rise_resistance : 0.3;
  fall_resistance : 0.3;
  slope_rise : 0.0;
  slope_fall : 0.0;
  related_pin : "A B";
        }
      }
    }
  }
```

In this case, The timing arc between 'B' and 'A' is defined only on the 'AND' scaled cell and not on the 'AND' scaled_cell. To fix the problem, remove one of the timing arcs.

EXAMPLE MESSAGE

```
Error: Ling 30, Pin 'A' has a timing arc that appears on only one of
the scaled cell (AND,WCCM) and the cell 'AND'. (LBDB-417)
```

LBDB-418 (warning) The cell_degradation constraint is missing

in this timing group in cell ’%s’.

DESCRIPTION

This message informs the user that Library Compiler finds the cell_degradation constraint being described in at least one, but not all, timing arcs of the cell. If the cell_degradation constraint is specified in a cell, all timing arcs of the following types should specify cell_degradation constraint: combinational rising_edge falling_edge clear preset three_state_enable However, the cell_degradation constraint should not be defined in timing groups of the following timing types: setup_rising setup_falling hold_rising hold_falling recovery_rising recovery_falling removal_rising removal_falling skew_rising skew_falling non_seq_setup_rising non_seq_setup_falling non_seq_hold_rising non_seq_hold_falling nochange_high_high nochange_high_low nochange_low_high nochange_low_low

WHAT NEXT

Do either one of the following modification to the cell description: (1) Remove all cell_degradation constraints specified in the cell. (2) Make sure all delay arcs of the above timing types specify cell_degradation constraints.

EXAMPLES

```
cell (DFF) {
  pin (D) {
    direction : input;
    ...
    timing () {  /* no warning */
      timing_type : setup_rising;
      related_pin : CP;
      rise_constraint (constr) {
        ...
      }
      rise_constraint (constr) {
        ...
      }
    }
  }
  pin (CP) {
    direction : input;
    ...
  }
  pin (Q) {
    direction : output;
    timing () {  /* cell_degradation is defined */
      related_pin : CP;
      timing_type : rising_edge;
      cell_degradation (celldeg) {
...
      }
      cell_rise (delay) {
        ...
```

```
      }
      cell_fall (delay) {
        ...
      }
      ...
    }
    ...
  }
  pin (QN) {
    direction : output;
    timing () {  /* cell_degradation is NOT defined  --- LIBG-206 --- */
      related_pin : CP;
      timing_type : rising_edge;
      cell_rise (delay) {
        ...
      }
      cell_fall (delay) {
        ...
      }
      ...
    }
    ...
  }
  ...

}
```

In this case, the warning message will be issued on CP-to-QN timing arc.

EXAMPLE MESSAGE

```
Warning: Line 202, The cell_degradation constraint is missing
 in this timing group in cell 'DFF'. (LBDB-418)
```

LBDB-419 (warning) Found the obsolete and unsupported 'state' group in the'%s' cell; please use 'ff' group or 'latch' group or 'statetable' instead.

DESCRIPTION

The **state** group is not supported after v3.0. Instead, the sequential function should now be described in **ff** or **latch** group or **statetable**.

WHAT NEXT

If you have access to the technology library source file change the **state** group to **ff** or **latch** group. Otherwise contact the vendor and inform them about the problem.

EXAMPLE MESSAGE

```
Warning: Line 159, Found the obsolete and unsupported 'state' group in the 'lbdbl41
9' cell;
        please use 'ff' group or 'latch' group or 'statetable' instead. (LBDB-419)
```

LBDB-420 (error) The index number '%d' must be less than the address width '%d'.

DESCRIPTION

This message indicates an index in the column_address or row_address attribute is greater than the address_width value.

WHAT NEXT

Correct the index in the technology library.

EXAMPLES

```
memory() { /* Indicate this is a memory cell */
  type : ram;
  address_width : 4;
  word_width : 2;
  column_address : "0 6 "; /* index 6 > addr_width 4 */
}
```

EXAMPLE MESSAGE

```
Error: Line 127, The index number '6' must be less than
        the address width '4'.  (LBDB-420)
```

LBDB-421 (error) The column or row address width '%d' must be less than or equal to the address width '%d'.

DESCRIPTION

This message indicates the width of the column_address or row_address attribute is greater than the address_width value.

WHAT NEXT

Reduce the number of indices in the column_address or row_address or correct the address_width value in the technology library.

EXAMPLES

```
memory() { /* Indicate this is a memory cell */
  type : ram;
  address_width : 4;
  word_width : 2;
  column_address : "0:4 "; /* col width 5 > addr_width 4 */
}
```

EXAMPLE MESSAGE

```
Error: Line 127, The column/row address width ’5’ must be less than or
       equal to the address width ’4’.  (LBDB-421)
```

LBDB-423 (error) Address pins are not all used by column_address and row_address attributes.

DESCRIPTION

This message indicates not all indices in the column_address and row_address attributes are used.

WHAT NEXT

Correct the index in the technology library.

EXAMPLES

```
memory() { /* Indicate this is a memory cell */
  type : ram;
  address_width : 4;
  word_width : 2;
  column_address : "0 1";
  row_address : "3";              /* missing the index 2 */
}
```

EXAMPLE MESSAGE

```
Error: Line 122, Address pins are not all used by column_address and row_address at
tributes. (LBDB-423)
```

LBDB-424 (warning) The number of address pins that overlap between column and row is ’%d’.

DESCRIPTION

This message indicates that there are overlapping indices in the column_address and row_address attributes.

WHAT NEXT

Correct the index overlapping in the technology library.

EXAMPLES

```
memory() { /* Indicate this is a memory cell */
  type : ram;
  address_width : 4;
  word_width : 2;
  column_address : "0:2";
  row_address : "2:3";            /* the index 2 is overlapping */
}
```

EXAMPLE MESSAGE

```
Warning: Line 122, The number of address pins that overlap between column and row i
s 1. (LBDB-424)
```

LBDB-425 (warning) Removing duplicate indices in the attribute.

DESCRIPTION

This message indicates an index in the column_address or row_address attribute is duplicated.

WHAT NEXT

Correct the index in the technology library.

EXAMPLES

```
memory() { /* Indicate this is a memory cell */
  type : ram;
  address_width : 4;
  word_width : 2;
```

```
        column_address : "0 3 3";
      }
```

EXAMPLE MESSAGE

```
Warning: Line 126, Removing duplicate indices in the attribute.  (LBDB-425)
```

LBDB-426 (error) The '%s' is missing for this inout pin.

DESCRIPTION

Both input_signal_level and the output_signal_level values are required in an inout pin.

WHAT NEXT

Check the library source file to see if you missed the input_signal_level or the output_signal_level attributes. Otherwise, change the direction of the pin to input or output.

EXAMPLES

```
    pin ( BIDIR )    {
      direction : inout;
      input_signal_level : VDD1;
      }
    }
```

To fix the problem, add the attribute to the pin group,

```
        output_signal_level : VDD2;
```

EXAMPLE MESSAGE

```
Error: Line 104, The 'output_signal_level' is missing for this inout pin. (LBDB-426)
```

LBDB-427 (error) All power supplies defined in the power_supply group must exist in this operating_conditions group.

DESCRIPTION

This message indicates that one or more power_rail attributes are missing in an operating_conditions group even though they were defined in the power_supply group.

WHAT NEXT

Check the library source file to see if you missed a power_rail attribute and correct it.

EXAMPLES

```
    power_supply() {
        default_power_rail : VDD0;
        power_rail(VDD1, 5.0);
        power_rail(VDD2, 3.3);
    }


    operating_conditions(MPSS) {
        process : 1.5 ;
        temperature : 70 ;
        voltage : 4.75 ;
        tree_type : "worst_case_tree" ;
        power_rail(VDD2, 2.9);
    }
```

To fix the problem, add the attribute to the operating_conditions group,

```
        power_rail(VDD1, 4.9);
```

EXAMPLE MESSAGE

```
Error: Line 14, All power supplies defined in the power_supply group
        must exist in this operating_conditions group. (LBDB-427)
```

LBDB-428 (error) All the pins in the '%s' cell with multiple power supplies must have signal level attributes.

DESCRIPTION

Either the input_signal_level or the output_signal_level attribute is missing in a pin within a multiple power supply cell.

WHAT NEXT

Check the library source file to see if you missed the input_signal_level or the output_signal_level attributes.

EXAMPLES

```
    power_supply() {
        default_power_rail : VDD0;
        power_rail(VDD1, 5.0);
        power_rail(VDD2, 3.3);
    }

cell(lbdb428) {
  area : 2;
  pad_cell : true;
  rail_connection(PV1, VDD1);
  rail_connection(PV2, VDD2);
  pin(A) {
    direction : input;          /* missing input_signal_level attribute */
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A";
    output_signal_level : VDD2;
    timing() {
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
}
```

To fix the problem, add the attribute to the 'A' pin group,

```
        input_signal_level : VDD1;
```

EXAMPLE MESSAGE

```
Error: Line 96, All the pins in the 'lbdb428' cell with multiple power supplies
must have signal level attributes. (LBDB-428)
```

LBDB-429 (warning) The timing arc from '%s' to '%s' is dormant.

DESCRIPTION

A timing arc from an input pin to an output pin is dormant if the signal change on the input pin can never cause the change on the output without simultaneous changes on any other input pins.

WHAT NEXT

This is caused by the input sharing between 'function', 'three_state', and 'x_function'. The signal transition is not physically possible and generally the timing arc should not be specified.

EXAMPLES

```
cell(a_cell) {
  pin(y) {
    function : "!a b"
    three_state : "!a !b | a b"
    timing() {
      related_pin : a;
    }
  }
}
```

In this example, if only pin 'a' is changed, pin 'y' will not have the signal transitions between '0' and '1'. The combinational timing arc between 'a' and 'y' is dormant.

EXAMPLE MESSAGE

Warning: Line 50000, The timing arc from 'a' to 'y' is dormant. (LBDB-429)

LBDB-430 (error) The '%s' rail_connection in a cell with multiple power supplies is missing an internal_power table.

DESCRIPTION

This error message indicates that an output pin, regardless of the output_signal_level value, is missing an internal_power table for designated rail_connection.

WHAT NEXT

Check the library source file to see if you missed the power_level attribute or there is a typo in the name of the power_supply.

EXAMPLES

```
power_supply() {
    default_power_rail : VDD0;
    power_rail(VDD1, 5.0);
    power_rail(VDD2, 3.3);
```

```
    }

cell(lbdb428) {
  area : 2;
  pad_cell : true;
  rail_connection(PV1, VDD1);
  rail_connection(PV2, VDD2);
  pin(A) {
    direction : input;
    capacitance : 1;
    input_signal_level : VDD1;
    internal_power () {
      power_level : VDD1;
      power(power_out1_d) {
        values (" 0.693418, 0.691911, 0.689730, 0.691771, 0.695229, 0.696524");
      }
    }
  }
  pin(Z) {
    direction : output;
    function : "A";
    output_signal_level : VDD2;
    internal_power () {
      power_level : VDD2;
      power(power_out1_d) {
        values (" 0.693418, 0.691911, 0.689730, 0.691771, 0.695229, 0.696524");
      }
    }
    timing() {
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
}

To fix the problem, add the internal_power to the 'Z' pin.

    internal_power () {
      power_level : VDD1;
      power(power_out1_d) {
        values (" 0.693418, 0.691911, 0.689730, 0.691771, 0.695229, 0.696524");
      }
    }
```

EXAMPLE MESSAGE

```
Error: Line 96,  The 'VDD1' rail_connection in a cell with multiple power
supplies is missing an internal_power table. (LBDB-430)
```

LBDB-431 (error) The value for attribute ’%s’ is empty.

DESCRIPTION

This error message indicates that an value field is null or empty.

WHAT NEXT

Check the library source file to see if you missed giving the value. If so, fill it up with appropriate value.

EXAMPLES

```
cell(GND_G_A) {
  area             : 1 ;
  cell_footprint   : GND_G ;
  dont_touch       : true ;
  dont_use         : true ;
  cell_leakage_power : 0.00;

  pin(PAD) {
    direction            : output ;
    function             : "0" ;
    capacitance          : 0.000000 ;

    max_capacitance      : 999.989990 ;
  }

  internal_power(POWER_IO_A) {
    values ("0.00000  ,0.00000  ",
            "0.00000  ,0.00000  ");
    related_inputs  : "";
    related_outputs : "PAD";
  }
}
```

To fix the problem, fill up value for related_inputs or remove related_inputs.

```
    internal_power () {
      values ("0.00000  ,0.00000  ",
           "0.00000  ,0.00000  ");
related_inputs  : "";
related_outputs : "PAD";
      }
```

EXAMPLE MESSAGE

```
Error: Line 722,  The value for attribute ’related_outputs’ is
empty. (LBDB-431)
```

LBDB-432 (error) The non-Zero %d scalar value is not allowed in internal_power
group within a cell group.

DESCRIPTION

This error message indicates that a non zero scalar value was defined in an internal_power group within a cell group.

WHAT NEXT

Check the library source file to see if it was a typo. If so, change the value to zero for no power consumption or move the internal power to a pin group.

EXAMPLES

```
cell(LBDB-432) {
  area             : 1 ;

  internal_power(scalar) {
values("2.0");
related_input : "";
  }

   ....
}
```

To fix the problem, change the values to zero or move the internal_power to a pin group.

```
    internal_power (scalar) {
      values ("0.00000");
related_input  : "";
      }
```

EXAMPLE MESSAGE

Error: Line 174, The non-Zero 2.0 scalar value is not allowed in internal_power group within a cell group. (LBDB-432)

LBDB-433 (error) The '%s' integrated gated clock cell has a '%s' pin with

a combinational timing arc containing the ’%s’ timing_type.

DESCRIPTION

This message indicates that you specified one of the cell’s timing arcs as either combinational or sequential which should be the opposite, while the function of this cell is integrated clock gated cell.

WHAT NEXT

Change the library source file, and fix the timing_type of the specified pin.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "none_posedge";
  dont_use : true;
  pin(EN) {
    direction : input;
    capacitance : 0.017997;
    clock_gate_enable_pin : true;
    timing() {
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "EN";
    }
    timing() {
      intrinsic_rise : 0.22;
      intrinsic_fall : 0.22;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "CP";
    }
  }
  pin(CP) {
    direction : input;
    capacitance : 0.031419;
    clock_gate_clock_pin : true;
    min_pulse_width_low  : 0.319;
  }
  pin(Z) {
    direction : output;
    function : "CP + EN’";
    max_capacitance : 0.500;
    clock_gate_out_pin : true;
```

```
    timing() {
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "EN";
    }
    timing() {
      intrinsic_rise : 0.22;
      intrinsic_fall : 0.22;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "CP";
    }
    internal_power (){
      rise_power(li4X3){
        index_1("0.0150, 0.0400, 0.1050, 0.3550");
        index_2("0.050, 0.451, 1.501");
        values("0.141, 0.148, 0.256",
        "0.162, 0.145, 0.234",
        "0.192, 0.200, 0.284",
        "0.199, 0.219, 0.297");
      }
      fall_power(li4X3){
        index_1("0.0150, 0.0400, 0.1050, 0.3550");
        index_2("0.050, 0.451, 1.500");
        values("0.117, 0.144, 0.246",
        "0.133, 0.151, 0.238",
        "0.151, 0.186, 0.279",
        "0.160, 0.190, 0.217");
      }
      related_pin : "CP EN" ;
    }
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The 'CGNP' integrated gated clock cell has a 'Z' pin with
        a combinational timing arc containing the 'combinational' timing_type. (LBD
B-433)
```

LBDB-434 (error) The '%s' integrated gated clock cell has a '%s' pin with

a sequential timing arc containing the ’%s’ timing_type.

DESCRIPTION

This message indicates that you specified one of the cell’s timing arcs as sequential, while the function of this cell is integrated clock gated cell. Library Compiler issues an error if any of the following timing types is defined on this cell:

* rising_edge
* falling_edge
* preset
* clear
* setup_rising
* setup_falling
* hold_rising
* hold_falling
* recovery_rising
* recovery_falling
* skew_rising
* skew_falling
* removal_rising
* removal_falling

WHAT NEXT

Change the library source file, and fix the timing_type of the specified pin.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "none_posedge";
  dont_use : true;
  pin(EN) {
    direction : input;
    capacitance : 0.017997;
    clock_gate_enable_pin : true;
    timing() {
      timing_type : nochange_high_low;
      intrinsic_rise : 0.4;
      intrinsic_fall : 0.4;
      related_pin : "CP";
    }
    timing() {
      timing_type : nochange_low_low;
      intrinsic_rise : 0.4;
      intrinsic_fall : 0.4;
      related_pin : "CP";
    }
  }
  pin(CP) {
```

```
  direction : input;
  capacitance : 0.031419;
  clock_gate_clock_pin : true;
  min_pulse_width_low  : 0.319;
}
pin(Z) {
  direction : output;
  function : "CP + EN'";
  max_capacitance : 0.500;
  clock_gate_out_pin : true;
  timing() {
    timing_type : nochange_high_low;
    intrinsic_rise : 0.4;
    intrinsic_fall : 0.4;
    related_pin : "CP";
  }
  timing() {
    timing_type : nochange_low_low;
    intrinsic_rise : 0.4;
    intrinsic_fall : 0.4;
    related_pin : "CP";
  }
  timing() {
    intrinsic_rise : 0.48;
    intrinsic_fall : 0.77;
    rise_resistance : 0.1443;
    fall_resistance : 0.0523;
    slope_rise : 0.0;
    slope_fall : 0.0;
    related_pin : "EN";
  }
  timing() {
    intrinsic_rise : 0.22;
    intrinsic_fall : 0.22;
    rise_resistance : 0.1443;
    fall_resistance : 0.0523;
    slope_rise : 0.0;
    slope_fall : 0.0;
    related_pin : "CP";
  }
  internal_power (){
    rise_power(li4X3){
      index_1("0.0150, 0.0400, 0.1050, 0.3550");
      index_2("0.050, 0.451, 1.501");
      values("0.141, 0.148, 0.256",
      "0.162, 0.145, 0.234",
      "0.192, 0.200, 0.284",
      "0.199, 0.219, 0.297");
    }
    fall_power(li4X3){
      index_1("0.0150, 0.0400, 0.1050, 0.3550");
      index_2("0.050, 0.451, 1.500");
      values("0.117, 0.144, 0.246",
      "0.133, 0.151, 0.238",
      "0.151, 0.186, 0.279",
```

```
        "0.160, 0.190, 0.217");
      }
      related_pin : "CP EN" ;
    }
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The 'CGNP' integrated gated clock cell has a 'Z' pin with
        a sequential timing arc containing the 'nochange_high_low' timing_type. (LB
DB-434)
```

LBDB-435 (error) The '%s' integrated gated clock cell has a '%s' pin without specified timing arcs.

DESCRIPTION

This message indicates that you specified one of the cell's pin without timing arcs, while the function of this cell is integrated clock gated cell.

WHAT NEXT

Change the library source file, and add the missing timing arc of the specified pin.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "none_posedge";
  dont_use : true;
  pin(EN) {
    direction : input;
    capacitance : 0.017997;
    clock_gate_enable_pin : true;
  }
  pin(CP) {
    direction : input;
    capacitance : 0.031419;
    clock_gate_clock_pin : true;
    min_pulse_width_low  : 0.319;
  }
  pin(Z) {
    direction : output;
    function : "CP + EN'";
    max_capacitance : 0.500;
```

```
    clock_gate_out_pin : true;
    timing() {
      timing_type : nochange_high_low;
      intrinsic_rise : 0.4;
      intrinsic_fall : 0.4;
      related_pin : "CP";
    }
    timing() {
      timing_type : nochange_low_low;
      intrinsic_rise : 0.4;
      intrinsic_fall : 0.4;
      related_pin : "CP";
    }
    timing() {
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "EN";
    }
    timing() {
      intrinsic_rise : 0.22;
      intrinsic_fall : 0.22;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "CP";
    }
    internal_power (){
      rise_power(li4X3){
        index_1("0.0150, 0.0400, 0.1050, 0.3550");
        index_2("0.050, 0.451, 1.501");
        values("0.141, 0.148, 0.256",
        "0.162, 0.145, 0.234",
        "0.192, 0.200, 0.284",
        "0.199, 0.219, 0.297");
      }
      fall_power(li4X3){
        index_1("0.0150, 0.0400, 0.1050, 0.3550");
        index_2("0.050, 0.451, 1.500");
        values("0.117, 0.144, 0.246",
        "0.133, 0.151, 0.238",
        "0.151, 0.186, 0.279",
        "0.160, 0.190, 0.217");
      }
      related_pin : "CP EN" ;
    }
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The 'CGNP' integrated gated clock cell has a 'Z' pin without
        specified timing arcs. (LBDB-435)
```

LBDB-436 (error) Illegal timing_model_type value '%s'.

DESCRIPTION

Currently the timing_model_type attribute can only take the value "stamp".

WHAT NEXT

Change or delete the attribute.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  timing_type_model : stml;
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, Illegal timing_model_type value 'stml'. (LBDB-436)
```

LBDB-437 (warning) The generated_clock(%s) group is defined multiple times.

DESCRIPTION

This message indicates that you specified the same generated_clock group multiple times. Only the last one is retained.

WHAT NEXT

Change the group name, or delete the duplicated group.

EXAMPLES

```
cell(CGNP) {
  area : 1;
```

```
  generated_clock(clock_A) {
    ...
  }
  generated_clock(clock_A) {
    ...
  }
  ...
}
```

EXAMPLE MESSAGE

```
Warning: Line 206, The generated_clock(clock_A) group is defined
multiple times. (LBDB-437)
```

LBDB-438 (error) The master pin is not specified in the generated_clock group.

DESCRIPTION

The master_pin attribute must be specified for a generated clock.

WHAT NEXT

Add the master_pin attribute.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  generated_clock(clockA) {
    clock_pin : CK;
    divided_by : 2;
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The master pin is not specified in the generated_clock
group. (LBDB-438)
```

LBDB-439 (error) The clock pin is not specified in the generated_clock
group.

DESCRIPTION

The clock_pin attribute must be specified for a generated clock.

WHAT NEXT

Add the clock_pin attribute.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  generated_clock(clockA) {
    master_pin : CK;
    divided_by : 2;
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The clock pin is not specified in the generated_clock
group. (LBDB-439)
```

LBDB-440 (error) The generated_clock divisor is less than 1.

DESCRIPTION

The divisor in the generated_clock group must be an integer greater than or equal to 1.

WHAT NEXT

Change the divisor value.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  generated_clock(clockA) {
```

```
    clock_pin : CLK1;
    master_pin : CLK;
    divided_by : 0;
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The generated_clock divisor is less than 1. (LBDB-440)
```

LBDB-441 (error) The generated_clock multiplier is less than 1.

DESCRIPTION

The multiplier in the generated_clock group must be an integer greater than or equal to 1.

WHAT NEXT

Change the multiplier value.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  generated_clock(clockA) {
    clock_pin : CLK1;
    master_pin : CLK;
    multiplied_by : 0;
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The generated_clock multiplier is less than 1. (LBDB-441)
```

LBDB-442 (error) The generated_clock edge is less than 0.

DESCRIPTION

The edge1, edge2, and edge3 parameter in the edges complex attribute in the generated_clock group must be non-negative integers.

WHAT NEXT

Change the violating edge value.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  generated_clock(clockA) {
    clock_pin : CLK1;
    master_pin : CLK;
    edges(-1, 2, 3);
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The generated_clock edge is less than 0. (LBDB-442)
```

LBDB-443 (warning) The mode_definition(%s) group is defined multiple times.

DESCRIPTION

This message indicates that you specified the same mode_definition group multiple times. Only the last one is retained.

WHAT NEXT

Change the group name, or delete the duplicated group.

EXAMPLES

```
cell(CGNP) {
  area : 1;

  mode_definition(rw) {
    ...
  }
  mode_definition(rw) {
    ...
  }
  ...
}
```

EXAMPLE MESSAGE

```
Warning: Line 206, The mode_definition(rw) group is defined
multiple times. (LBDB-443)
```

LBDB-444 (error) The mode definition '%s' has no values defined.

DESCRIPTION

A mode_definition group must have at least one mode value defined.

WHAT NEXT

Define the mode values.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  mode_definition(read) {
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The mode definition 'read' has no values defined. (LBDB-444)
```

LBDB-445 (warning) The mode_value(%s) group is defined multiple times.

DESCRIPTION

This message indicates that you specified the same mode_value group multiple times. Only the last one is retained.

WHAT NEXT

Change the group name, or delete the duplicated group.

EXAMPLES

```
cell(CGNP) {
  area : 1;

  mode_definition(rw) {
    mode_value(read) {
      when : R;
      sdf_cond : "R == 1";
    }
    mode_value(read) {
      when : !R;
      sdf_cond : "R == 0";
    }
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 206, The mode_value(read) group is defined
multiple times. (LBDB-445)
```

LBDB-446 (error) The sdf_cond attribute is not specified for the mode condition.

DESCRIPTION

This message indicates that you specified the when condition for the mode value, but did not specify the sdf_cond attribute.

WHAT NEXT

Add the missing sdf_cond attribute.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  mode_difinition(rw) {
    mode_value(read) {
      when : R;
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The sdf_cond attribute is not specified for the
mode condition. (LBDB-446)
```

LBDB-447 (information) The mode instance is defined multiple times for the same timing arc.

DESCRIPTION

This message indicates that you specified multiple mode instances for a timng arc.

WHAT NEXT

Please make sure that it is your real attention to have multiple modes that apply to the timing arc.

EXAMPLES

```
cell(CGNP) {
  area : 1;

  pin (y) {
    timing() {
      mode(rw, read);
      mode(rw, write);
    }
  }
}
```

EXAMPLE MESSAGE

```
Information: Line 206, The mode instance is defined multiple times
for the same timing arc. (LBDB-447)
```

LBDB-448 (error) The Boolean condition overlaps with the condition

specified at line %d.

DESCRIPTION

The two Boolean conditions must be mutually exclusive.

WHAT NEXT

Check the conditions and make them mutually exclusive.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  mode_definition(rw) {
    mode_value(read) {
      when : R;
      sdf_cond : "R == 1";
    }
    mode_value(write) {
      when : R;
      sdf_cond : "R == 1";
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The Boolean condition overlaps with the condition
        specified at line 202. (LBDB-448)
```

LBDB-449 (error) The mode instance mode(%s, %s) is invalid.

DESCRIPTION

The mohe instance delaration must be referring to a mode_definition and one of its mode_value

WHAT NEXT

Check for consistency between mode group and mode value definitions, and mode instance declarations.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  mode_definition(rw) {
    mode_value(read) {
      ...
    }
    mode_value(werite) {
      ...
    }
  }
  pin (y) {
    timing () {
      mode(rw, latching);
      ...
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The mode instance mode(rw, latching) is invalid. (LBDB-449)
```

LBDB-450 (error) Mismatched quotes in the sdf_cond string.

DESCRIPTION

In the sdf_cond string, a double quoting is mismatched.

WHAT NEXT

Add the missing quote or delete the extra quote.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  mode_definition(rw) {
    mode_value(read) {
      when : R;
      sdf_cond : "R == 1 && C ==
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, Mismatched quotes in the sdf_cond string. (LBDB-450)
```

LBDB-451 (error) Undefined variable '%s'.

DESCRIPTION

The variable in the sdf_cond string must be a port or bus name.

WHAT NEXT

Eliminate undefined varibable.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  mode_definition(rw) {
    mode_value(read) {
      when : R;
      sdf_cond : "read == 1";
    }
  }
  pin (R) {
    ...
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, Undefined variable 'read'. (LBDB-451)
```

LBDB-452 (error) Fewer than two ports are specified in the short list.

DESCRIPTION

A short complex attribute must have more than one parameter.

WHAT NEXT

Add the missing port names.

EXAMPLES

```
cell (c) {
  ...
  short(A);
  pin (A) {...}
  pin (Y) {...}
}
```

EXAMPLE MESSAGE

```
Error: Line 206, Fewer than two ports are specified in the
short list. (LBDB-452)
```

LBDB-453 (error) The parameter '%s' in the short list is not a port or bus name.

DESCRIPTION

The short complex attribute must take port or bus name as parameters.

WHAT NEXT

Eliminate undefined varibable.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  short(R, T);

  pin(R) {...}
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The parameter 'T' in the short list is not a
port or bus name. (LBDB-453)
```

LBDB-454 (error) Unequal bus widths in the short list. specified

timing arcs.

DESCRIPTION

All members of a short list must be of the same width. That is, they must all be simple ports, or all be buses of the same width.

WHAT NEXT

Use the same width members.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  short(A, B);
  bus(A) {
    bus_type : bus4;
  }
  bus(B) {
    bus_tyep : bus8;
  }
  ...
}
```

EXAMPLE MESSAGE

Error: Line 206, Unequal bus widths in the short list. (LBDB-454)

LBDB-455 (error) Multiple drive arcs are defined on port %s.

DESCRIPTION

A port can have at most one drive arc defined.

WHAT NEXT

Eliminate the extra ones.

EXAMPLES

```
pin(Y) {
  timing () {
    drive_arc : true;
    ...
  }
```

```
  timing () {
    drive_arc : true;
    ...
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, Multiple drive arcs are defined on port Y. (LBDB-455)
```

LBDB-456 (error) The drive arc is not combinational.

DESCRIPTION

Drive arc must be combinational.

WHAT NEXT

Change the drive arc to combinational or delete it.

EXAMPLES

```
pin(Z) {
    direction : output;
    timing() {
        timing_type : nochange_high_low;
        drive_arc : true;
        ...
    }
    ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The drive arc is not combinational. (LBDB-456)
```

LBDB-457 (error) Related pin is found on the drive arc.

DESCRIPTION

Drive arc cannot have related pins.

WHAT NEXT

Remove the related_pin attribute or unlabel the timing arc.

EXAMPLES

```
pin(Z) {
    direction : output;
    timing() {
        timing_type : nochange_high_low;
        drive_arc : true;
        related_pin : A;
        ...
    }
    ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, Related pin is found on the drive arc. (LBDB-457)
```

LBDB-458 (error) Cell rise or fall table is missing on the drive arc.

DESCRIPTION

Drive arc requires cell rise and fall tables.

WHAT NEXT

Add the missing tables.

EXAMPLES

```
pin(Z) {
    direction : output;
    timing() {
        timing_type : nochange_high_low;
        drive_arc : true;
        cell_rise(table1) {
          ...
        }
    }
    ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, Cell rise or fall table is missing on the
drive arc. (LBDB-458)
```

LBDB-459 (error) The drive arc has tables that are not 1-D function of total_output_capacitance.

DESCRIPTION

Drive arc requires delay tables to be 1-D function of total output capacitance.

WHAT NEXT

Add the missing tables.

EXAMPLES

```
pin(Z) {
    direction : output;
    timing() {
        timing_type : nochange_high_low;
        drive_arc : true;
        cell_rise(table2D) {
          values("0.1, 0.2", "0.5, 0.8");
        }
    }
    ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The drive rc has tables that are not 1-D function
of total_output_capacitance. (LBDB-459)
```

LBDB-460 (error) Multiple tlatch groups are defined on pin '%s'.

DESCRIPTION

This message indicates that you specified multiple tlatch groups on a pin.

WHAT NEXT

Delete the duplicated group.

EXAMPLES

```
pin(D) {

  tlatch(EN) {
    ...
  }
  tlatch(E) {
    ...
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, Muliple tlatch groups are defined on
pin 'D'.  (LBDB-460)
```

LBDB-461 (error) The edge type is not specified for the tlatch.

DESCRIPTION

A tlatch group must have the edge_type attribute specified.

WHAT NEXT

Add the missing attribute.

EXAMPLES

```
pin(D) {

  tlatch(EN) {
    tdisable : TRUE;
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The edge tyep is not specified for the tlatch. (LBDB-461)
```

LBDB-462 (error) Pin ’%s’ referred to in tlatch does not exist.

DESCRIPTION

The tlatch group name must be the name of an existing enable pin.

WHAT NEXT

Add the missing attribute.

EXAMPLES

```
cell (c) {
  pin(D) {
    tlatch(EN) {
      edge_type : rising;
    }
  }
  ...
  /* No such pin as EN */
}
```

EXAMPLE MESSAGE

Error: Line 206, Pin ’EN’ referred to in tlatch does not exist. (LBDB-462)

LBDB-463 (warning) The related pin ’%s’ for the non-sequential setup/hold timing check is labeled a clock.

DESCRIPTION

If the related pin for the non-sequential constraint arc is labeled a clock, then timing analysis will not propagate a clock signal through the cell.

WHAT NEXT

Delete the "clock : true;" declaration in the pin group.

EXAMPLES

```
cell (c) {
  pin(D) {
    timing() {
      timing_type : non_seq_setup_falling;
      related_pin : OSC;
```

```
      ...
    }
  }
  pin(OSC) {
    clock : true;
    ...
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 206, The related pin 'OSC' for the non-sequential
setup/hold timing check is labeled a clock. (LBDB-463)
```

LBDB-464 (error) The '%s' cell is a non-pad cell with x_function, which is not supported by Library Compiler.

DESCRIPTION

Library Compiler only supports x_function on pad cells. Library Compiler issues this error message if a non-pad cell defines x_function on one or more ports.

WHAT NEXT

Remove the x_function attribute defined for any output pin of the cell.

EXAMPLES

```
  cell (lbdb464) {
    area    :   0.0;
    pin (D, CLK)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
    }
    pin(Q){
      direction   :   output;
      function : "IQ";
      x_function : CLK';
      timing () {
      timing_type : rising_edge;
intrinsic_rise   : 1.0;
rise_resistance  : 0.1;
intrinsic_fall   : 1.0;
fall_resistance  : 0.1;
related_pin      : "CLK";
      }
    }
```

```
    ff (IQ, IQN) {
      next_state : D;
      clocked_on : CLK;
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 6, The 'lbdb464' cell is a non-pad cell with x_function,

which is not supported by Library Compiler. (LBDB-464)
```

LBDB-465 (error) The '%s' attribute is missing from the electromigration group.

DESCRIPTION

The **related_pin** or **related_bus_pins** attribute is required in an electromigration group with a two-dimensional lookup table.

WHAT NEXT

Change the library source file by specifying the **related_pin** or the **related_bus_pins** attribute in the electromigration group as needed.

EXAMPLES

```
    electromigration() {
      em_max_toggle_rate(em_2d) {
values ("1, 2, 3, 4", "5, 6, 7, 8", \

"9, 10, 11, 12", "13, 14, 15, 16");
      }
    }
```

To fix the problem, add the following line into the electromigration group:

```
related_pin : "A";
```

EXAMPLE MESSAGE

```
Error: Line 126, The 'related_pin or related_bus_pins' attribute is missing
from the electromigration group. (LBDB-465)
```

LBDB-466 (error) The '%s' attribute cannot be specified in this electromigration group.

DESCRIPTION

This message indicates that you specified an attribute outside its context. An electromigration group with one-dimensional lookup tables cannot specify **related_pin** or **related_bus_pins** attributes.

WHAT NEXT

Change the technology library source file to delete the specified attribute or move the attribute to its correct context.

EXAMPLES

```
    electromigration() {
        em_max_toggle_rate(em_1d_temp) {
                values ("1, 2, 3, 4");
        }
related_pin : "A";
    }
```

In this case, the **related_pin** attribute is not allowed in the one-dimensional lookup table. To fix the problem, remove the **related_pin** attribute from the electromigration group.

EXAMPLE MESSAGE

```
Error: Line 69, The 'related_pin or related_bus_pins' attribute cannot be
specified in this electromigration group. (LBDB-466)
```

LBDB-467 (error) The '%s' lookup table in the input-associated electromigration group cannot use '%s' as its template.

DESCRIPTION

The em_max_toggle_rate lookup table in an input-associated electromigration group must use a one-dimensional template with **input_transition_time** as its variable.

WHAT NEXT

For more information about lookup tables, see the *Library Compiler User Guide*. Change the library source file by referencing a different template in the lookup table description.

EXAMPLES

```
  em_lut_template(ok_temp) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
  }
  em_lut_template(err_temp) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");
  }

em_max_toggle_rate(err_temp) {
values ("1, 2, 3, 4");
}
```

To fix the problem, change the template value of the **em_max_toggle_rate** attribute from *err_temp* to *ok_temp*.

EXAMPLE MESSAGE

```
Error: Line 126, The 'em_max_toggle_rate' lookup table in the input-associated
       electromigration group cannot use 'err_temp' as its template. (LBDB-467)
```

LBDB-468 (error) The one-dimensional '%s' lookup table in the inout-associated electromigration group cannot use '%s' as its template.

DESCRIPTION

The one-dimensional em_max_toggle_rate lookup table in an inout-associated electromigration group must use a template with **input_transition_time** or **total_output_net_capacitance** as its variable.

WHAT NEXT

For more information about lookup tables, see the *Library Compiler User Guide*. Change the library source file by referencing a different template in the lookup table description.

EXAMPLES

```
  em_lut_template(ok_template) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
  }
  em_lut_template(ok2_template) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");
```

```
  }
  em_lut_template(err_template) {
    variable_1 : output_net_length;
    index_1("0, 1, 2, 3");
  }

        em_max_toggle_rate(err_template) {
                values ("1, 2, 3, 4");
        }
```

To fix the problem, change the template value of the **em_max_toggle_rate** attribute from err_template to ok_template or ok2_template.

EXAMPLE MESSAGE

```
Error: Line 126, The 1-dimensional 'em_max_toggle_rate' lookup table in the
      inout-associated electromigration group cannot use
'err_template' as its template. (LBDB-468)
```

LBDB-469 (error) The one-dimensional '%s' lookup table in the %s-associated electromigration group cannot use '%s' as its template.

DESCRIPTION

The one-dimensional em_max_toggle_rate lookup table in an output-associated electromigration group must use a template with **total_output_net_capacitance** as its variable.

WHAT NEXT

For more information about lookup tables, see the *Library Compiler User Guide*. Change the library source file by referencing a different template in the lookup table description.

EXAMPLES

```
  em_lut_template(err_template) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
  }
  em_lut_template(ok_template) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");
  }

        em_max_toggle_rate(err_template) {
```

```
                values ("1, 2, 3, 4");
        }
```

To fix the problem, change the template value of the **em_max_toggle_rate** attribute from *err_template* to *ok_template*.

EXAMPLE MESSAGE

```
Error: Line 126, The 1-dimensional 'em_max_toggle_rate' lookup table in the
output-
associated electromigration group cannot use 'err_template' as its template. (LBDB-
469)
```

LBDB-470 (error) The two-dimensional '%s' lookup table in the %s-associated electromigration group cannot use '%s' as its template.

DESCRIPTION

The two-dimensional em_max_toggle_rate lookup table in an output-associated electromigration group must use a template with **input_transition_time** and **total_output_net_capacitance** as its variables.

WHAT NEXT

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

EXAMPLES

```
  em_lut_template(ok_template) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
    variable_2 : total_output_net_capacitance;
    index_2("0, 1, 2, 3");
  }
  em_lut_template(err_template) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");
    variable_2 : constrained_pin_transition;
    index_2("0, 1, 2, 3");
  }

em_max_toggle_rate(err_template) {
values ("1, 2, 3, 4", "5, 6, 7, 8", \

"9, 10, 11, 12", "13, 14, 15, 16");
```

```
}
```

To fix the problem, change the template value of the **em_max_toggle_rate** attribute from err_template to ok_template.

EXAMPLE MESSAGE

```
Error: Line 126, The 2-dimensional 'em_max_toggle_rate' lookup table in the
output-
associated electromigration group cannot use 'err_template' as its template. (LBDB-
470)
```

LBDB-471 (error) The '%s' port has %d electromigration tables. Only one table is allowed. Path-dependent electromigration is not supported.

DESCRIPTION

Library Compiler only supports non path-dependent electromigration. Library Compiler issues this error message if more than one electromigration is defined within a pin.

WHAT NEXT

Change the library source file by removing any extra electromigration tables within the pin group.

EXAMPLES

```
    pin(Q){
      ...
      electromigration() {
      em_max_toggle_rate(em_2d) {
values ("1, 2, 3, 4", "5, 6, 7, 8", \

"9, 10, 11, 12", "13, 14, 15, 16");
      }
related_pin : "A";
      }
      electromigration() {
      em_max_toggle_rate(em_2d) {
values ("21, 22, 23, 24", "25, 26, 27, 28", \

"29, 30, 31, 32", "33, 34, 35, 36");
      }
related_pin : "B";
      }
  }
```

To fix the problem, remove one of the electromigration tables and include both pins 'A' and 'B' in the related_pin.

```
    pin(Q){
      ...
      electromigration() {
      em_max_toggle_rate(em_2d) {
values ("41, 42, 43, 44", "45, 46, 47, 48", \

"49, 50, 51, 52", "53, 54, 55, 56");
      }
related_pin : "A B";
      }
  }
```

EXAMPLE MESSAGE

```
Error: Line 6, The 'Q' port has 2 electromigration tables.
Only one table is allowed. Path dependent electromigration is not supported. (LBDB-
471)
```

LBDB-472 (warning) The timing type of the timing arc from '%s' to '%s' is changed from '%s' to '%s'.

DESCRIPTION

The functional relationships between the pin and the related pin(s) dictate that this timing arc is non-rising or non-falling. This is due to the input sharing between function, three_state, and x_function.

WHAT NEXT

Change the library source file so that expected timing types are entered. In case of an error, change the functional description.

EXAMPLES

```
  pin(io){
      direction : output;
      function : "!ap & !an";
      three_state : "ap & !an";
      x_function : "!ap & an";
```

```
      timing() {
        related_pin : "ap an";
        timing_type : three_state_disable;
        ...
      }
      ...
  }
```

To fix, change functions or change timing_types.

```
  pin(io){
      ...
      timing() {
        related_pin : "ap an";
        timing_type : three_state_disable_rise;
        ...
      }
      ...
  }
```

EXAMPLE MESSAGE

```
Warning: Line 9, The timing type of the timing arc from 'ap' to
'io' is changed from 'three_state_disable' to
'three_state_disable_rise'. (LBDB-472)
```

LBDB-473 (error) The timing label '%s' is already used for another timing arc in the same cell.

DESCRIPTION

You receive this error message when the given timing label is invalid because it was already used by another timing arc in the cell. Duplicate timing labels are not allowed within a cell.

WHAT NEXT

Edit the timing label list so that there is not a label in the list that is used in another timing group in the cell.

LBDB-474 (error) The timing group has incorrect number of

labels.

DESCRIPTION

You receive this error message when the timing group at the specified line has either too many or too few specified labels.

WHAT NEXT

Edit the timing label list in your library so that the timing group has the right number of labels specified.

LBDB-475 (error) The port '%s' is missing the attribute '%s'.

DESCRIPTION

You receive this error message when the **rise_capacitance** attribute or the **fall_capacitance** attribute for a port is missing and the other attribute is specified. Both or neither of the attributes must be specified.

WHAT NEXT

Specifiy the missing attribute, or remove the specified attribute.

LBDB-476 (warning) The port '%s' does not have the attribute '%s' specified. The value %f will be assigned to the attribute.

DESCRIPTION

You receive this error message when the **rise_capacitance** and **fall_capacitance** attributes are specified for a port, and the **capacitance** attribute is not. The maximum value between **rise_capacitance** and **fall_capacitance** will be assigned to the attrribute.

WHAT NEXT

If you accept the value assigned to the attribute referenced in the error message, no action is required on your part. If not, assign a value to the attribute.

LBDB-477 (error) The table %s has invalid intermediate_values

entry.

DESCRIPTION

This message indicates that a intermediate_values table contain invalid values. The values have to be between zero and the corresponding values from the values table attribute.

WHAT NEXT

Edit the intermediate_values table so that it doesn’t have invalid values any more.

LBDB-478 (error) The intermediate_values cannot be used with current setting of output delay threshold voltages.

DESCRIPTION

This message indicates that the output delay threshold voltages are not valid for intermediate_values table. intermediate_values table values are used to specify the values from first slew point to the output delay point. The assumption is that the output delay point lies between the two slew points. This error message will be issued when Library Compiler detects that the output delay point does not lie between the two slew points, and intermediate_values table was used.

WHAT NEXT

Stop using intermediate_values table, or edit the library level attributes for threshold voltages (for delay and slew).

LBDB-479 (error) when ’%s’ is specified ’%s’ has to be given as well.

DESCRIPTION

This message indicates that a rise net delay table was given without fall net delay table (or vice versa). Both tables are expected by the wire delay estimator.

WHAT NEXT

Edit the library source file to add in the missing table or delete the incomplete table for the file to compile.

LBDB-480 (error) Missing a timing arc of timing_type ’three_state_disable’ between the ’%s’ and ’%s’ pins in the ’%s’ cell.

DESCRIPTION

To describe the transition from 0->Z or 1->Z, use the timing arc with a timing_type of **three_state_disable** for the pin with a **three_state** attribute.

WHAT NEXT

Add the missing timing group between the two pins. To change the message to a warning, set the environment variable **timing_check_all_errors** to 0.

EXAMPLES

```
cell(BTS4)  {
      area : 3.0;
  pin(Z)  {
    direction : output;
    function : "A";
    three_state : "E";
    timing()  {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "A";
    }
    timing()  {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "E";
    }
  }
  pin(A)  {
    direction : input;
      capacitance : 1.0;
  }
  pin(E)  {
    direction : input;
      capacitance : 1.0;
  }
}
```

EXAMPLE MESSAGE

Error: Line 110, Missing a timing arc of timing_type ’three_state_disable’

between ’E’ and ’Z’ pins in the ’lbfb35’ cell. (LBDB-480)

LBDB-481 (warning) Port %s has multiple default timing arcs. Only one arc is used as the default arc.

DESCRIPTION

You receive this message because a port has multiple default timing arcs in the case of State Dependent Timing. This is probably due to two conditions: First, a timing arc with no WHEN statement has been given as a default arc. Second, one timing arc with a condition has been specified as a default timing arc by having its **default_timing** attribute set for the arc.

WHAT NEXT

Examine the library source file, and remove all but one default timing arc.

LBDB-482 (error) Port %s has multiple timing arcs with default_timing attribute set.

DESCRIPTION

You receive this message because a port has multiple timing arcs with the **default_timing** attribute set. A port with State Dependent Timing should have only one timing arc. A library with this error does not compile.

WHAT NEXT

Examine the library source file, and reset all but one timing arc of the **default_timing** attribute for the port.

LBDB-483 (error) Cannot find include file ’%s’.

DESCRIPTION

You receive this message because the **include()** attribute has been used to include a file but the file could not be located in the search path.

WHAT NEXT

Add the missing include file.

LBDB-484 (error) No variables statement is specified in the '%s' poly_template.

DESCRIPTION

You receive this message because you did not define a variables statement in the specified poly_template group. Library Compiler expects you to define one variables statement there.

WHAT NEXT

Define a variables statement for the specified poly_template.

EXAMPLES

The following example shows a poly_template named *p1* that is missing a variables statement:

```
poly_template(p1) {
  variable_1_range("1,2");
  variable_2_range("3,4");
}
```

To correct the problem in the example above, insert the following statement in the *p1* poly_template group:

```
  variables("temperature, total_output_net_capacitance");
```

EXAMPLE MESSAGE

Error: Line 191, No variables statement is specified in the 'p1' poly_template. (LB DB-484)

LBDB-485 (error) Incompatible variable '%s' is used in the '%s' poly_template.

DESCRIPTION

You receive this message because you defined an invalid variable in the variables statement in the poly_template group.

WHAT NEXT

Define a variable name for the specified poly_template.

EXAMPLES

In the following example, the *whatever* variable value is not valid in the *p1* poly_template.

```
poly_template(p1) {
  variables("whatever, total_output_net_capacitance");
  variable_1_range("1,2");
  variable_2_range("3,4");
}
```

To correct the problem in the example above, insert the following statement in the *p1* poly_template group:

```
  variables("temperature, total_output_net_capacitance");
```

EXAMPLE MESSAGE

Error: Line 191, Incompatible variable 'whatever' is used in the 'p1' poly_template. (LBDB-485)

LBDB-486 (warning) Variable range outside variable dimension is defined in '%s' poly_template.

DESCRIPTION

You receive this message because you have defined a variable range outside the dimension of the poly_template.

WHAT NEXT

Remove the statement for the variable range that is not in use.

EXAMPLES

The following example shows a **variable_2_range** variable value that cannot be used in the *p1* poly_template.

```
poly_template(p1) {
  variables("total_output_net_capacitance");
  variable_1_range("1,2");
  variable_2_range("3,4");
}
```

Correct it by removing the **variable_2_range** statement.

EXAMPLE MESSAGE

```
Warning: Line 191, Variable range outside variable
      dimension is defined in 'p1' poly_template. (LBDB-486)
```

LBDB-487 (error) No range information defined for variable_%d in 'p1' poly_template.

DESCRIPTION

You receive this message because you have not defined the range for one of the variables used in the poly_template.

WHAT NEXT

Add the **variable_n_range** statement for the specified variable.

EXAMPLES

The following example shows a *p1* poly_template that is missing the **variable_1_range** statement.

```
poly_template(p1) {
  variables("temperature, total_output_net_capacitance");
  variable_2_range("3,4");
}
```

Correct it by adding the following statement in the poly_template group:

```
  variable_1_range("1,2");
```

EXAMPLE MESSAGE

```
Error: Line 191, No range information defined for variable_1 in
      'p1' poly_template. (LBDB-487)
```

LBDB-488 (error) No variables statement specified in '%s'

domain of ’%s’ poly_template.

DESCRIPTION

You receive this message because you have not defined a variables statement in this domain of the poly_template group.

WHAT NEXT

Define a variables statement for this domain in the poly_template.

EXAMPLES

The following example shows a domain named *d1* in a poly_template named *p1* that is missing the variables statement:

```
poly_template(p1) {
  ......
  domain (d1) {
    variable_1_range("1,2");
    variable_2_range("3,4");
  }
}
```

Correct it by adding the following statement in the poly_template group:

```
  variables("temperature, total_output_net_capacitance");
```

EXAMPLE MESSAGE

```
Error: Line 191, No variables statement specified in ’d1’

      domain of ’p1’ poly_template. (LBDB-488)
```

LBDB-489 (error) Incompatible variable ’%s’ used ’%s’ domain of ’%s’ poly_template.

DESCRIPTION

You receive this message because you defined an invalid variable in the variables statement of this domain in the poly_template.

WHAT NEXT

Examine the name of the specified variable to determine the cause.

EXAMPLES

The following example shows an invalid variable named *whatever* in the *p1* poly_template.

```
poly_template(p1) {
  ......
  domain(d1) {
    variables("whatever, total_output_net_capacitance");
    variable_1_range("1,2");
    variable_2_range("3,4");
  }
}
```

Correct it by adding the following statement in the domain group:

```
  variables("temperature, total_output_net_capacitance");
```

EXAMPLE MESSAGE

Error: Line 191, Incompatible variable 'whatever' used in 'd1' domain of 'p1' poly_ template. (LBDB-489)

LBDB-490 (warning) Variable range outside variable dimension is defined in '%s' domain of '%s' poly_template.

DESCRIPTION

You receive this message because you have defined a variable range outside the dimension of the specified domain of the poly_template.

WHAT NEXT

Remove the variable range statement not in use.

EXAMPLES

The following example shows a **variable_2_range** statement that is useless in the *d1* domain of the *p1* poly_template.

```
poly_template(p1) {
  ......
  domain(d1) {
    variables("total_output_net_capacitance");
    variable_1_range("1,2");
    variable_2_range("3,4");
  }
}
```

Correct it by removing the **variable_2_range** statement.

EXAMPLE MESSAGE

Warning: Line 191, Variable range outside variable dimension is defined in 'd1' domain of 'p1' poly_template. (LBDB-490)

LBDB-491 (error) No range information defined for variable_%d in 'p1' domain of '%s' poly_template.

DESCRIPTION

You receive this message because you have not defined a range for the specified variable used in this domain of the poly_template.

WHAT NEXT

Add a **variable_n_range** statement (substituting the specified variable number for **n**).

EXAMPLES

The following example shows the *d1* domain of the *p1* poly_template with the **variable_1_range** statement missing.

```
poly_template(p1) {
  ......
  domain(d1) {
    variables("temperature, total_output_net_capacitance");
    variable_2_range("3,4");
  }
}
```

Correct it by adding the following statement:

```
  variable_1_range("1,2");
```

EXAMPLE MESSAGE

Error: Line 191, No range information defined for variable_1 in 'd1' domain of 'p1' poly_template. (LBDB-491)

LBDB-492 (error) Power rail mapping information missing in

’%s’ poly_template.

DESCRIPTION

You receive this message because you have not defined the power rail mapping information for the **voltage2** variable in the poly_template.

WHAT NEXT

Add the mapping statement in the poly_template.

EXAMPLES

The following example shows the *p1* poly_template with the mapping statement missing.

```
poly_template(p1) {
  variables("temperature, voltage2, total_output_net_capacitance");
  ......
}
```

Correct it by adding the following statement:

```
  mapping("voltage2, VDD");
```

EXAMPLE MESSAGE

Error: Line 191, Power rail mapping information missing in ’p1’ poly_template. (LBDB-492)

LBDB-493 (error) Power rail mapping information missing in ’%s’ domain of ’%s’ poly_template.

DESCRIPTION

You receive this message because you have not defined the power rail mapping information for the voltage2 variable in the specified domain of the specified poly_template.

WHAT NEXT

Add the mapping statement in this domain of the poly_template.

EXAMPLES

The following example shows the *d1* domain of the *p1* poly_template with the mapping

statement missing.

```
poly_template(p1) {
  ......
  domain(d1) {
    variables("temperature, voltage2, total_output_net_capacitance");
    ......
  }
}
```

Correct it by adding the following statement:

```
  mapping("voltage2, VDD");
```

EXAMPLE MESSAGE

```
Error: Line 191, Power rail mapping information missing in 'd1' domain of 'p1'
poly_template. (LBDB-493)
```

LBDB-495 (error) Invalid number of dimensions in '%s' poly_template.

DESCRIPTION

You receive this message because the number of variables you have defined in the poly_template is invalid.

WHAT NEXT

Examine the variables statement to determine why the number of variables is invalid.

EXAMPLES

The following example shows a variables statement that defines the wrong number of variables in the *p1* poly_template.

```
poly_template(p1) {
  variables("");
  ......
}
```

Correct it by changing the variables statement in the poly_template group to the following:

```
  variables("temperature, total_output_net_capacitance");
```

EXAMPLE MESSAGE

```
Error: Line 191, Invalid number of dimensions in 'p1' poly_template. (LBDB-495)
```

LBDB-496 (error) Invalid number of dimensions in '%s' domain of '%s' poly_template.

DESCRIPTION

You receive this message because the number of variables you have defined in the specified domain of the specified poly_template is invalid.

WHAT NEXT

Examine the variables statement to determine why the number of variables is invalid.

EXAMPLES

The following example shows a variables statement that defines the wrong number of variables in the *d1* domain of the *p1* poly_template.

```
poly_template(p1) {
  ......
  domain (d1) {
    variables("");
    ......
  }
}
```

Correct it by changing the variables statement in this domain of the poly_template group to the following:

```
  variables("temperature, total_output_net_capacitance");
```

EXAMPLE MESSAGE

```
Error: Line 191, Invalid number of dimensions in 'd1' domain of 'p1' poly_template.
(LBDB-496)
```

LBDB-497 (error) Incomplete range of variable in '%s'

poly_template.

DESCRIPTION

You receive this message because the variable statement of the specified poly_template has an incomplete range.

WHAT NEXT

Examine all **variable_n_range** statements (substituting each existing variable number for **n**) of the specified poly_template to determine those that have an incomplete range.

EXAMPLES

The following example shows the *p1* poly_template with an incomplete **variable_1_range** statement.

```
poly_template(p1) {
  variables("temperature, total_output_net_capacitance");
  variable_1_range("1");
  ......
}
```

Correct it by changing the **variable_1_range** statement in the poly_template group to the following:

```
  variable_1_range("1,2");
```

EXAMPLE MESSAGE

Error: Line 191, Incomplete range of variable in 'p1' poly_template. (LBDB-497)

LBDB-498 (error) Incomplete range of variable in '%s' domain of '%s' poly_template.

DESCRIPTION

You receive this message because the variable statement in the specified domain of the specified poly_template has an incomplete range.

WHAT NEXT

Examine all **variable_n_range** statements (substituting each existing variable number for **n**) in the specified domain of the specified poly_template to determine those

that have an incomplete range.

EXAMPLES

The following example shows *d1* domain of the *p1* poly_template with an incomplete **variable_1_range** statement.

```
poly_template(p1) {
  ......
  domain (d1) {
    variables("temperature, total_output_net_capacitance");
    variable_1_range("1");
    ......
  }
}
```

Correct it by changing the **variable_1_range** statement in the *d1* domain of the poly_template group to the following:

```
  variable_1_range("1,2");
```

EXAMPLE MESSAGE

```
Error: Line 191, Incomplete range of variable in 'd1' domain of 'p1' poly_template.
(LBDB-498)
```

LBDB-499 (error) No orders information defined for the polynomial.

DESCRIPTION

You receive this message because you have not defined the **orders** statement for the polynomial.

WHAT NEXT

Add the **orders** statement before the **coefs** statement.

EXAMPLES

The following example shows a poly timing group with a missing **orders** statement.

```
  rise_constraint(constraint) {
    coefs("1.2095, 0.2281, 0.0225, -0.0001, 0.0678, -0.0002, 0.0000, 0.0000");
  }
```

Correct it by adding the following statement before the **coefs** statement:

```
  orders("1,1,1");
```

EXAMPLE MESSAGE

```
Error: Line 191, No orders information defined for the polynomial. (LBDB-499)
```

LBDB-500 (error) No orders information defined for ’%s’ domain of the polynomial.

DESCRIPTION

You receive this message because you have not defined the **orders** statement for this domain of the polynomial.

WHAT NEXT

Add the **orders** statement before the **coefs** statement.

EXAMPLES

The following example shows the *d1* domain of a poly timing group with a missing **orders** statement.

```
  rise_constraint(constraint) {
    ......
    domain (d1) {
      coefs("1.2095, 0.2281, 0.0225, -0.0001, 0.0678, -0.0002, 0.0000, 0.0000");
    }
  }
```

Correct it by adding the following statement before the **coefs** statement:

```
  orders("1,1,1");
```

EXAMPLE MESSAGE

```
Error: Line 191, No orders information defined for ’d1’ domain of the polynomial.
(LBDB-500)
```

LBDB-501 (error) No coefs information defined for the

polynomial.

DESCRIPTION

You receive this message because you have not defined the **coefs** statement for the polynomial.

WHAT NEXT

Add the **coefs** statement after the **orders** statement.

EXAMPLES

The following example shows a poly timing group with a missing **coefs** statement.

```
  rise_constraint(constraint) {
    orders("1,1,1");
  }
```

Correct it by adding the following statement after the **orders** statement:

```
  coefs("1.2095, 0.2281, 0.0225, -0.0001, 0.0678, -0.0002, 0.0000, 0.0000");
```

EXAMPLE MESSAGE

```
Error: Line 191, No coefs information defined for the polynomial. (LBDB-500)
```

LBDB-502 (error) No coefs information defined for '%s' domain of the polynomial.

DESCRIPTION

You receive this message because you have not defined the **coefs** statement for the specified domain of the polynomial.

WHAT NEXT

Add the **coefs** statement for the specified domain after the **orders** statement.

EXAMPLES

The following example shows the *d1* domain of a poly timing group with a missing **coefs** statement.

```
  rise_constraint(constraint) {
```

```
    ......
    domain (d1) {
      orders("1,1,1");
    }
  }
```

Correct it by adding the following after the **orders** statement:

```
  coefs("1.2095, 0.2281, 0.0225, -0.0001, 0.0678, -0.0002, 0.0000, 0.0000");
```

EXAMPLE MESSAGE

```
Error: Line 191, No coefs information defined for 'd1' domain of the polynomial.
(LBDB-502)
```

LBDB-503 (Error) The low range setting is equal to or greater than the high range setting in %s.

DESCRIPTION

This warning message tells you that the values specified for the variable range setting statement are incorrect. Only temperature, voltages, and generic parameters can have the same low range and high range.

EXAMPLES

The following example shows the p1 poly_template with an incomplete variable_1_range statement.

```
poly_template(p1) {
  variables("temperature, total_output_net_capacitance");
  variable_1_range("100,1");
  ......
}
```

Correct it by changing the variable_1_range statement in the poly_template group to the following:

```
  variable_1_range("1,100");
```

EXAMPLE MESSAGE

```
Error: Line 191, The low range setting is equal to or greater than the high range
setting in variable_1_range. (LBDB-503)
```

LBDB-504 (warning) Range setting in domain at

variable_%d_range conflicts with template setting. Use the template setting instead.

DESCRIPTION

This warning tells you that the variable range setting statement has a range that conflicts with the range set previously in the template.

WHAT NEXT

Examine all variable_*n*_range statements. Substitute each existing variable number for *n* in the specified poly_template to determine the statements that conflict with each other.

EXAMPLES

The following example shows the p1 poly_template with an incorrect variable_1_range statement in the domain.

```
poly_template(p1) {
  variables("temperature, total_output_net_capacitance");
  variable_1_range("1,50");
  domain (d1) {
    variable_1_range("2,100");
  }
  ......
}
```

Correct it by changing the variable_1_range statement in the domain to the following:

```
  variable_1_range("2,40");
```

The value 40 can be any number less than or equal to 50.

EXAMPLE MESSAGE

Warning: Line 191, Range setting conflicts with template setting. (LBDB-504)

LBDB-505 (error) Variable %s is not a voltage. Can only map voltages to a power rail.

DESCRIPTION

This error message tells you that the first variable in mapping is not a voltage. Only voltages can be mapped to a power rail.

WHAT NEXT

Check the variables in the mapping and replace the first variable with a voltage.

EXAMPLES

The following example shows the p1 poly template with an incorrect mapping statement.

```
poly_template(p1) {
  variables("temperature, voltage,total_output_net_capacitance");
  variable_1_range("20,150");
  variable_2_range("1.2,3.2");
  variable_3_range("10,30");
  mapping(temperature,VDD1);
  ......
}
```

Fix the mapping statement by changing the variable_1_range statement in the domain to the following:

```
  mapping(voltage,VDD1);
```

EXAMPLE MESSAGE

Error: Line 191, Variable temperature is not a voltage (LBDB-505).

LBDB-506 (error) Variable %s is not defined in the %s.

DESCRIPTION

This error message tells you that the first variable in mapping is not defined in the template.

WHAT NEXT

Define the variable in the template, or change the variable_1_range statement in the domain.

EXAMPLES

The following example shows the p1 poly_template with an incorrect mapping statement.

```
poly_template(p1) {
  variables("temperature, voltage,total_output_net_capacitance");
  variable_1_range("20,150");
  variable_2_range("1.2,3.2");
```

```
  variable_3_range("10,30");
  mapping(voltage1,VDD1);
  ......
}
```

Correct it by changing the variable_1_range statement in the domain to the following:

```
  mapping(voltage,VDD1);
```

EXAMPLE MESSAGE

```
Error: Line 191, Variable voltage1 is not defined in the template (LBDB-506).
```

LBDB-507 (error) Attempting to map to %s, which is defined in power_supply group. However, power_supply group is missing.

DESCRIPTION

This error message tells you that you have not defined a power_supply group before using its information.

WHAT NEXT

Add a power_supply group before the templates.

EXAMPLES

The following example shows the p1 poly_template with the mapping statement missing.

```
poly_template(p1) {
  variables("temperature, voltage2, total_output_net_capacitance");
  mapping("voltage2, VDD");
  ......
}
```

Correct it by adding the following statement before the template:

```
  power_supply() {
    default_power_rail : VDD ;
  }
```

EXAMPLE MESSAGE

```
Error: Line 191, Power_supply group missing but trying to map to %s, which is
supposed to be defined in a power_supply group. (LBDB-507)
```

LBDB-508 (error) The ’%s’ port has hyperbolic low groups. Only input pin or bidirectional pin can have hyperbolic low groups.

DESCRIPTION

Library Compiler issues this error message if one hyperbolic low group is defined within an output pin.

WHAT NEXT

Change the library source file by removing the hyperbolic low groups within the output pin group.

EXAMPLES

```
    pin(Q){
      direction : output;
      ...
      hyperbolic_noise_low() {
        ...
      }
  }
```

To correct the problem, remove one of the hyperbolic low groups.

```
    pin(Q){
      direction : output;
      ...
  }
```

EXAMPLE MESSAGE

```
Error: Line 6, The ’Q’ port has hyperbolic groups.
Only input pin or bidirectional pin can have hyperbolic low groups. (LBDB-508)
```

LBDB-509 (error) The ’%s’ port has hyperbolic high groups. Only input pin or bi-directional pin can have hyperbolic high groups.

DESCRIPTION

Library Compiler issues this error message if one hyperbolic high group is defined within a output pin.

WHAT NEXT

Change the library source file by removing the hyperbolic high groups within the output pin group.

EXAMPLES

```
    pin(Q){
      direction : output;
      ...
      hyperbolic_noise_high() {
      }
  }
```

To fix the problem, remove one of the hyperbolic high groups.

```
    pin(Q){
      direction : output;
      ...
  }
```

EXAMPLE MESSAGE

Error: Line 6, The 'Q' port has hyperbolic groups.
Only input pin or bi-directional pin can have hyperbolic high groups. (LBDB-509)

LBDB-510 (error) The '%s' port has hyperbolic above_high groups.
Only input pin or bi-directional pin can have hyperbolic above_high groups.

DESCRIPTION

Library Compiler issues this error message if one hyperbolic above_high group is defined within a output pin.

WHAT NEXT

Change the library source file by removing the hyperbolic above_high groups within the output pin group.

EXAMPLES

```
    pin(Q){
```

```
      direction : output;
      ...
      hyperbolic_noise_above_high() {
      }
  }
```

To fix the problem, remove one of the hyperbolic above_high groups.

```
    pin(Q){
      direction : output;
      ...
  }
```

EXAMPLE MESSAGE

```
Error: Line 6, The 'Q' port has hyperbolic groups.
Only input pin or bi-directional pin can have hyperbolic above_high groups. (LBDB-
510)
```

LBDB-511 (error) The '%s' port has hyperbolic below_low groups.
Only input pin or bi-directional pin can have hyperbolic below_low groups.

DESCRIPTION

Library Compiler issues this error message if one hyperbolic below_low group is defined within a output pin.

WHAT NEXT

Change the library source file by removing the hyperbolic below_low groups within the output pin group.

EXAMPLES

```
    pin(Q){
      direction : output;
      ...
      hyperbolic_noise_below_low() {
      }
  }
```

To fix the problem, remove one of the hyperbolic below_low groups.

```
    pin(Q){
      direction : output;
      ...
  }
```

EXAMPLE MESSAGE

```
Error: Line 6, The 'Q' port has hyperbolic groups.
Only input pin or bi-directional pin can have hyperbolic below_low groups. (LBDB-
511)
```

LBDB-512 (error) The '%s' port has noise hyperbolic groups. Only one input/bi-directional port can have noise hyperbolic groups.

DESCRIPTION

Library Compiler issues this error message if more than one noise hyperbolic is defined within a timing.

WHAT NEXT

Change the library source file by removing any extra noise hyperbolic groups within the pin group.

EXAMPLES

```
    pin(Q){
      direction : output;
      ...
      noise_hyperbolic_low() {
        ...
      }
  }
```

To fix the problem, remove one of the noise hyperbolic groups.

```
    pin(Q){
      direction : output;
      ...
  }
```

EXAMPLE MESSAGE

```
Error: Line 6, The 'Q' port has noise hyperbolic groups.
Only input/bi-directional ports can have noise hyperbolic groups. (LBDB-512)
```

LBDB-513 (error) The '%s' port has repeated noise hyperbolic groups. Only one such group is allowed.

DESCRIPTION

Library Compiler issues this error message if more than one of the same noise hyperbolic group is defined within a timing.

WHAT NEXT

Change the library source file by removing any extra noise hyperbolic groups within the timing group.

EXAMPLES

```
    pin(Q){
      ...
      noise hyperbolic_low() {
        ...
      }
      noise hyperbolic_low() {
        ...
      }
  }
```

To correct the problem, remove extra noise hyperbolic groups.

```
    pin(Q){
      ...
      noise hyperbolic_low() {
        ...
      }
  }
```

EXAMPLE MESSAGE

```
Error: Line 6, The 'Q' port has repeated noise hyperbolic groups.
Only one such group is allowed. (LBDB-513)
```

LBDB-514 (error) The constraint timing arc has noise immunity groups.
Only non-constraint timing arc can specify such info.

DESCRIPTION

Library Compiler issues this error message if noise immunity info is defined within a constraint timing arc.

WHAT NEXT

Remove the noise immunity tables/polys.

EXAMPLES

```
    pin(Q){
      direction : output;
      ...
      timing() {
 timing_type: setup_rising;
         ...
         noise_immunity_low() {
           ...
         }
      }
  }
```

To fix the problem, remove the noise immunity tables/polys.

```
    pin(Q){
      direction : output;
      ...
      timing() {
 timing_type: setup_rising;
         ...
      }
  }
```

EXAMPLE MESSAGE

```
Error: Line 6, The timing arc has noise immunity groups.
Only non-constraint timing arc can specify such info. (LBDB-514)
```

LBDB-515 (error) The '%s' port has repeated noise immunity

groups inside timing group. Only one such group is allowed.

DESCRIPTION

Library Compiler issues this error message if more than one noise immunity is defined within a timing group.

WHAT NEXT

Change the library source file by removing any extra noise immunity tables or polys within the timing group.

EXAMPLES

```
    pin(Q){
      ...
      timing() {
         ...
         noise_immunity_low() {
           ...
         }
         noise_immunity_low() {
           ...
         }
      }
  }
```

To correct the problem, remove extra noise immunity groups.

```
    pin(Q){
      ...
      timing() {
      ...
        noise_immunity_low() {
        ...
        }
      }
  }
```

EXAMPLE MESSAGE

Error: Line 6, The 'Q' port has repeated noise immunity groups inside timing group. Only one such group is allowed. (LBDB-515)

LBDB-516 (error) The '%s' group uses

template ’%s’ which does not contain ’iv_output_voltage’ as its variable.

DESCRIPTION

The iv characteristics group must use a 1-d iv characteristics template with **iv_output_voltage** as its variable.

WHAT NEXT

Change the library source file by including ’iv_output_voltage’ in the template.

EXAMPLES

```
    iv_lut_template(ok_temp){
        variable_1 : iv_output_voltage;
        index_1("0.5,1.0,1.5,2.0,2.5");
    }
    iv_lut_template(err_temp){
        variable_1 : input_transition_time;
        index_1("0.5,1.0,1.5,2.0,2.5");
    }
    ...
 steady_state_current_high(err_temp) {
values("1.385,2.554,3.722,4.891,6.059");;
}
```

To fix the problem, change the template value of the **steady_state_current_high** attribute from *err_temp* to *ok_temp*.

EXAMPLE MESSAGE

```
Error: Line 126, The ’steady_state_current_high’ group in the timing
       group cannot use ’err_temp’ as its template. (LBDB-516)
```

LBDB-517 (error) The ’%s’ lookup table in the timing group cannot use ’%s’ as its template.

DESCRIPTION

The noise characteristics group must use a 2-d noise characteristics template with **input_noise_width, total_output_net_capacitance** as its variables.

WHAT NEXT

Change the library source file by including 'input_noise_width' and 'total_output_net_capacitance' in the template.

EXAMPLES

```
    noise_lut_template(ok_temp){
        variable_1 : input_noise_width;
        variable_2 : total_output_net_capacitance;
        index_2("1.0,2.0,4.0,6.0,10.0");
        index_2("0.5,1.0,1.5,2.0,2.5");
    }
    noise_lut_template(err_temp){
        variable_1 : input_net_transition;
        variable_2 : total_output_net_capacitance;
        index_2("1.0,2.0,4.0,6.0,10.0");
        index_2("0.5,1.0,1.5,2.0,2.5");
    }
    ...
 noise_immunity_high(err_temp) {
                values("0.733,1.073,1.412,1.752,2.092",
                           "0.873,1.214,1.554,1.894,2.234",
                           "1.095,1.442,1.787,2.132,2.477",
                           "1.298,1.648,1.996,2.343,2.691",
                           "1.703,2.060,2.414,2.766,3.119");
}
```

To fix the problem, change the template value of the **noise_immunity_high** attribute from *err_temp* to *ok_temp*.

EXAMPLE MESSAGE

```
Error: Line 126, The 'noise_immunity_high' lookup table in the timing
       group cannot use 'err_temp' as its template. (LBDB-517)
```

LBDB-519 (error) The timing arc has steady_state_resistance_low/high/above_high/below_low attribute specified.

Only combo, enable, disable, rising_edge, falling_edge, clear and preset timing arc can specify such attributes.

DESCRIPTION

Library Compiler issues this error message if any steady_state_resistance_low/high/above_high/below_low attribute is defined within a timing arc which is not combo, disable or enable.

WHAT NEXT

Change the library source file by removing such attributes inside the timing() group.

EXAMPLES

```
    pin(Q){
      ...
      timing() {
timing_type : setup_rising;
...
        steady_state_resistance_high() {
           ...
        }
      }
  }
```

To fix the problem, remove the steady_state_resistance attributes.

```
    pin(Q){
      ...
      timing() {
timing_type : setup_rising;
        ...
      }
  }
```

EXAMPLE MESSAGE

```
Error: Line 6, The timing arc has steady_state_resistance_low/high/above_high/
below_low attribute specified.
Only combo, enable, disable, rising_edge, falling_edge, clear and preset timing arc
 can specify such attributes. (LBDB-519)
```

LBDB-520 (error) The timing arc has steady_state_current_high/low specified. Only combo, rising_edge, falling_edge, preset and clear timing arcs can specify such info.

DESCRIPTION

Library Compiler issues this error message if any steady_state_current_high/low group is defined within a timing group which is not combo, disable or enable.

WHAT NEXT

Change the library source file by removing such groups inside the timing() group.

EXAMPLES

```
    pin(Q){
      ...
      timing() {
timing_type : setup_rising;
...
        steady_state_current_high(iv1x5) {
           ...
        }
      }
  }
```

To fix the problem, remove the steady_state_current_high group.

```
    pin(Q){
      ...
      timing() {
timing_type : setup_rising;
        ...
      }
  }
```

EXAMPLE MESSAGE

```
Error: Line 6, The timing arc has steady_state_current_high/low specified.
Only combo, rising_edge, falling_edge, preset and clear timing arcs can specify suc
h info. (LBDB-520)
```

LBDB-521 (error) The timing arc has steady_state_current_tristate specified. Only enable or disable timing arc can specify such info.

DESCRIPTION

Library Compiler issues this error message if any steady_state_current_tristate group is defined within a timing group which is not disable or enable.

WHAT NEXT

Change the library source file by removing such groups inside the timing() group.

EXAMPLES

```
    pin(Q){
      ...
      timing() {
timing_type : setup_rising;
...
        steady_state_current_tristate(iv1x5) {
           ...
        }
      }
  }
```

To fix the problem, remove the steady_state_current_tristate group.

```
    pin(Q){
      ...
      timing() {
timing_type : setup_rising;
        ...
      }
  }
```

EXAMPLE MESSAGE

```
Error: Line 6, The timing arc has steady_state_current_tristate specified.
Only enable or disable timing arc can specify such info. (LBDB-521)
```

LBDB-522 (error) The '%s' group in the timing arc cannot use '%s' as its template.

DESCRIPTION

The noise characteristics group must use a 3-d noise characteristics template with **input_noise_width, input_noise_height, total_output_net_capacitance** as its variables.

WHAT NEXT

Change the library source file by including 'input_noise_width', 'input_noise_height' and 'total_output_net_capacitance' in the template.

EXAMPLES

```
    ...
    propagation_lut_template(ok_temp){
```

```
        variable_1 : input_noise_width;
        variable_2 : input_noise_height;
        variable_3 : total_output_net_capacitance;
        index_1("1.0,2.0,4.0,6.0,10.0");
        index_2("0.5,1.0,1.5,2.0,2.5");
        index_3("0.5,1.0,1.5,2.0,2.5");
    }
    noise_lut_template(err_temp){
        variable_1 : input_net_transition;
        variable_2 : input_noise_height;
        variable_3 : total_output_net_capacitance;
        index_1("1.0,2.0,4.0,6.0,10.0");
        index_2("0.5,1.0,1.5,2.0,2.5");
        index_3("0.5,1.0,1.5,2.0,2.5");
    }
    ...
 propagation_noise_width_high(err_temp) {
                values("0.733,1.073,1.412,1.752,2.092",
                           "0.873,1.214,1.554,1.894,2.234",
                           "1.095,1.442,1.787,2.132,2.477",
                           "1.298,1.648,1.996,2.343,2.691",
   ...
                           "1.703,2.060,2.414,2.766,3.119");
}
```

To fix the problem, change the template value of the **propagation_noise_width_high** attribute from *err_temp* to *ok_temp*.

EXAMPLE MESSAGE

```
Error: Line 126, The 'propagation_noise_width_high' group in the timing
       arc cannot use 'err_temp' as its template. (LBDB-522)
```

LBDB-523 (error) The related '%s' group is not specified for the %s' group in the timing arc.

DESCRIPTION

The noise propagation width and height group must coexist for the same region(low, high, below_low, above_high).

WHAT NEXT

Add the missiong propagation group in the timing group.

EXAMPLES

```
      ...
timing() {
```

```
      propagation_noise_width_high(ok_temp) {
                values("0.733,1.073,1.412,1.752,2.092",
                           "0.873,1.214,1.554,1.894,2.234",
                           "1.095,1.442,1.787,2.132,2.477",
                           "1.298,1.648,1.996,2.343,2.691",
   ...
                           "1.703,2.060,2.414,2.766,3.119");
}
      propagation_noise_width_low(ok_temp) {
                values("0.733,1.073,1.412,1.752,2.092",
                           "0.873,1.214,1.554,1.894,2.234",
                           "1.095,1.442,1.787,2.132,2.477",
                           "1.298,1.648,1.996,2.343,2.691",
   ...
                           "1.703,2.060,2.414,2.766,3.119");
      propagation_noise_height_low(ok_temp) {
                values("0.733,1.073,1.412,1.752,2.092",
                           "0.873,1.214,1.554,1.894,2.234",
                           "1.095,1.442,1.787,2.132,2.477",
                           "1.298,1.648,1.996,2.343,2.691",
   ...
                           "1.703,2.060,2.414,2.766,3.119");
}
...
```

To fix the problem, add the *propagation_noise_width_high* group in the timing group.

EXAMPLE MESSAGE

Error: Line 126, The related 'propagation_noise_height_high' group is not specified for the 'propagation_noise_width_high' group in the timing arc. (LBDB-523)

LBDB-524 (error) Invalid variable '%s' is used in the '%s' poly_template refered by %s group.

DESCRIPTION

You receive this message because you defined an invalid variable in the variables statement in the poly_template group refered by leakage_power or pin_capacitance group. The valid variables can only be temperature voltage, and power_rails.

WHAT NEXT

Define a variable name for the specified poly_template.

EXAMPLES

In the following example, the *whatever* variable value is not valid in the *p1*

```
poly_template.

poly_template(p1) {
  variables("temperature, total_output_net_capacitance");
  variable_1_range("1,2");
  variable_2_range("3,4");
}
```

To correct the problem in the example above, insert the following statement in the *p1* poly_template group:

```
  variables("temperature, voltage");
```

EXAMPLE MESSAGE

```
Error: Line 191, Invalid variable 'total_output_net_capacitance' is used in the 'p1'
poly_template refered by leakage_power group.(LBDB-524)
```

LBDB-525 (error) Only polynomial format is supported for '%s' group.

DESCRIPTION

You receive this message because you defined an non-polynomial group, such as pin_capacitance() group, leakagage_power() group.

WHAT NEXT

Please redefine these groups using polynomials.

LBDB-600 (error) The '%s' direction cannot be specified on a pin.

DESCRIPTION

This message indicates that you specified an incompatible direction value on a pin. Library Compiler fails if the direction value includes the following combinations:

* tristate

WHAT NEXT

Refer to the "Library Compiler User Guide" for direction information. Remove the incompatible values of the direction attribute.

EXAMPLES

```
  cell(lbdb600) {
    area : 2;
    pin(A) {
      direction : tristate;
      capacitance : 1.0;
    }
    ...
  }
```

EXAMPLE MESSAGE

```
Error: Line 84, The 'tristate' direction cannot be specified on a
       pin. (LBDB-600)
```

LBDB-601 (error) related_pin is illegal in the timing group. Timing arc info is missing.

DESCRIPTION

This message indicates that you specified an illegal related_pin in a timing group.

WHAT NEXT

Refer to the "Library Compiler User Guide" for related_pin information.

EXAMPLES

```
           timing() {
                /* noise immunity */
                noise_immunity_high(noise5x5){
                    index_2("0.362,0.725,1.087,1.449,1.812");
                    values("0.733,1.073,1.412,1.752,2.092",
                           "0.873,1.214,1.554,1.894,2.234",
                           "1.095,1.442,1.787,2.132,2.477",
                           "1.298,1.648,1.996,2.343,2.691",
                           "1.703,2.060,2.414,2.766,3.119");
                }
related_pin: "a";
            }
```

EXAMPLE MESSAGE

```
Error: Line 120, related_pin is illegal in the timing group.
 Timing arc info is missing.  (LBDB-601)
```

LBDB-602 (warning) The units of time, capacitance, voltage and current are not consistent.

DESCRIPTION

This message indicates that you specified an inconsistent units in the library.

WHAT NEXT

Refer to the "Library Compiler User Guide" for unit information. Modify the realted unit values to make them consistent.

EXAMPLES

```
library (mi333) {
    ...
   time_unit                    : "1ns";
   voltage_unit                 : "1mV";
   current_unit                 : "1mA";
   pulling_resistance_unit      : "1kohm";
   capacitive_load_unit  (1, pf);
    ...
```

EXAMPLE MESSAGE

```
Warning: Line 120, The units of time, capacitance, voltage and current are not cons
istent. (LBDB-602)
```

LBDB-603 (error) The ’%s’ attribute cannot be supplied a nonpositive value (%d).

DESCRIPTION

This message indicates that the specified attribute cannot have a nonpositive value.

WHAT NEXT

Change the value of the attribute to positive in the technology library file.

EXAMPLES

```
    orders ( 0, 2, 3 );
```

EXAMPLE MESSAGE

```
Error: Line 18, The 'orders' attribute cannot be supplied a
       nonpositive value (0) (LBDB-603)
```

LBDB-604 (error) '%s' attribute should be less than '%s' attribute.

DESCRIPTION

This message indicates that the specified attributes are not consistent.

WHAT NEXT

Change the value of the attributes to be consistent in the technology library file.

EXAMPLES

```
   slew_lower_threshold_pct_rise: 80.0
   slew_upper_threshold_pct_rise: 20.0
```

EXAMPLE MESSAGE

```
Error: Attribute 'slew_lower_threshold_pct_rise' should be less
       than 'slew_upper_threshold_pct_rise'. (LBDB-604)
```

LBDB-605 (warning) The attribute '%s' is not specified.

DESCRIPTION

This message indicates that an attribute is missing.

WHAT NEXT

Either add the missing attribute to the technology library or ignore the message.

EXAMPLES

```
   slew_lower_threshold_pct_rise: 20.0
```

EXAMPLE MESSAGE

```
Warning: Line 18, The attribute 'slew_lower_threshold_pct_rise' is not specified. (
LBDB-605)
```

LBDB-606 (error) The invalid ’%s’ value is encountered on the ’%s’ attribute.

DESCRIPTION

This message indicates that you specified an invalid attribute’s value . Library Compiler cannot handle the value.

WHAT NEXT

Check the library source file, and correct the problem.

EXAMPLES

```
fall_propagation ( table4x6 ) {
   index_1 ("2.00e+02 2.50e+02 3.50e+02 4.00e+02 ") ;
   index_2 ("4.48e-02 8.96e-02 1.34e-01 1.79e-01 2.24e-01 2.69e-01 ");
   values ("Look.here 9.56e+01 1.15e+02 1.34e+02 1.52e+02 1.71e+02 ", \

   "9.38e+01 1.20e+02 1.45e+02 1.67e+02 1.89e+02 2.10e+02 ", \

   "1.01e+02 1.32e+02 1.58e+02 1.83e+02 2.07e+02 2.29e+02 ", \

   "1.04e+02 1.43e-93 1.43e-93 1.43e-93 2.75e+226 9.30e+254 " ) ;
}
```

EXAMPLE MESSAGE

```
Error: Line 85, The invalid ’Look.here’ value is encountered
on the ’values’ attribute. (LBDB-606)
```

LBDB-607 (warning) The pin ’%s’ does not have a internal_power group.

DESCRIPTION

For an input pin, we must have one internal_power table matching the input_signal_level value. The rest of the rail connections are optional.

WHAT NEXT

Add the relative internal_power table matching the input_signal_level value.

EXAMPLES

```
 cell ( cell1 ) {
     rail_connection(PV1, VDD1);
     rail_connection(PV2, VDD2);

     pin(A) {
...
     }
     pin(B) {
...
     }
     pin ( CP ) {
         direction : input ;
         input_signal_level : VDD1;
 ...
      }
      ...
```

To fix the problem, add the relative internal_power group matching the input_signal_level value to pin(CP). internal_power() { power_level : VDD1 ; when : "A !B"; power (power_ramp) { values ("1.934150, 2.148130, 2.449420, 3.345050, 4.305690"); } }

EXAMPLE MESSAGE

Warning: Line 126, The pin ’CP’ does not have a internal_power group. (LBDB-607)

LBDB-608 (Warning) Library cell ’%s’ has a valid function-id, but it has also been annotated with the user_function_class attribute. Resolving this conflict by ignoring the user_function_class attribute for this library cell.

DESCRIPTION

The specified cell has been annotated with the **user_function_classr** attribute even though it has a valid function-id. Library Compiler can generate a function-id for most cells in a technology library. However, there may be a few complex sequential or combinational cells that Library Compiler cannot successfully generate a function-id for. In addition, some black-box cells in the library do not have any function information. The **user_function_class** attribute is intended for such cells that otherwise would not have a function-id. The **user_function_class** attribute is not intended for library cells that already have a valid function-id.

WHAT NEXT

This warning message indicates that the **user_function_class** attribute for this library cell will be ignored. No further action is required. To turn off this

warning message in the future, make sure that a **user_function_class attribute** is not set on this library cell.

LBDB-609 (Warning) Library cells '%s' and '%s' have different pin information, but they have been assigned the same user_function_class. Resolving this conflict by ignoring the user_function_class attribute on the latter library cell.

DESCRIPTION

Two library cells that are assigned the same **user_function_class** attribute should have the exact same pin information. That is, they must have the same number of pins and the same pin names. This requirement is necessary so that Design Compiler can establish pin-to-pin correspondence between two cells in the same **user_function_class** when it replaces a reference to one library cell by a reference to the other library cell.

This warning message indicates that an inconsistency was found between the pin information of two library cells in the same **user_function_class**. To resolve this conflict, the **user_function_class** attribute for the second library cell will be ignored.

WHAT NEXT

This warning message indicates that the **user_function_class** attribute for the second library cell will be ignored. No further action is required. To turn off this warning message in the future, make sure that all library cells in a given **user_function_class** attribute have the same pin information.

LBDB-610 (warning) The units of %s are not consistent.

DESCRIPTION

This message indicates that you specified an inconsistent units in the library.

WHAT NEXT

Refer to the "Library Compiler User Guide" for unit information. Modify the realted unit values to make them consistent.

EXAMPLES

```
library (mi333) {
```

```
  ...
 time_unit                    : "1ns";
 voltage_unit                 : "1V";
 current_unit                 : "1mA";
 resistance_unit      : "1kohm";
 capacitive_load_unit  (1, pf);
  ...
```

EXAMPLE MESSAGE

```
Warning: Line 120, The units of time, capacitance, resistance are not consistent. (
LBDB-610)
```

LBDB-611 (warning) The ’%s’ %s group is not used by any %s pin in the library.

DESCRIPTION

This message indicates that the library pins does not use the defined input/output voltage groups.

WHAT NEXT

For input_voltage group, add "input_voltage" attrribute to input library pins. For output_voltage group, add "output_voltage" attrribute to output library pins.

EXAMPLES

```
input_voltage(CMOS) {
  vil : 1.5;
  vih : 3.5;
  vimin : -0.3;
  vimax : VDD + 0.3;
}

input_voltage(CMOS) {
  vil : 2.5;
  vih : 4.5;
  vimin : -0.3;
  vimax : VDD + 0.3;
}
```

EXAMPLE MESSAGE

```
Error: Line 31, The ’CMOS’ input_voltage  group is not used by any input pin in the
 library. (LBDB-611)
```

LBDB-612 (information) The ’%s’ attribute value is %s (%3.1f).

DESCRIPTION

This message indicates that you specified an attribute value that maybe out of the accepted range. The value is either less than the minimum value or greater than the maximum value. Unlike LBDB-163, it does not reset the value.

WHAT NEXT

EXAMPLES

```
height_coefficient : -0.01;
```

In this case, the height_coefficient’s value -0.01 is less than the minimum accepted value 0.0. However, it is not reset.

EXAMPLE MESSAGE

```
Warning: Line 109, The ’height_coefficient’ attribute value is
 less than 0.0. (LBDB-612)
```

LBDB-613 (error) The ’%s’ group requires the ’%s’ %s. Either the attribute(or group) is missing or the attribute(or group) has an invalid value.

DESCRIPTION

This message indicates you specified a group without one of its required attributes(or groups). Library Compiler rejects the attribute(group) definition if the attribute(group) exists and has an invalid value.

WHAT NEXT

Change the library file by adding the missing attribute(or group) to the group.

EXAMPLES

```
memory() {
  type : random;
  address_width : 10;
  word_width : 8;
```

```
      }
```

In this case, the ’type’ has an invalid value. To fix the problem, assign ’rom’ or ’ram’ to the type.

EXAMPLE MESSAGE

```
Error: Line 27, The ’memory’ group requires the ’type’ attribute.
Either the attribute is missing or the attribute has an invalid value. (LBDB-179)
```

LBDB-614 (error) The ’%s’ has a count of %d, which does not match the number of "%s" specified.

DESCRIPTION

The specification of the variables implied the number of indices of a template (or template domain).

WHAT NEXT

Check the library source file, and make the number of variables and indices to the same.

EXAMPLES

```
  lu_table_template(basic_template) {
      variable_1 : input_net_transition;
      index_1 ("0.1, 1.2, 2.3, 3.4");
      index_2 ("0.1, 1.2, 2.3, 3.4");
  }
```

EXAMPLE MESSAGE

```
Error: Line 160, The ’index_*’ have a count of 2, which does not match
the number of ’varible_*’ specified. (LBDB-614)
```

LBDB-615 (warning) Connect pin ’%s’ to the default_power_supply ’%s’

defined in the power_supply() group in library.

DESCRIPTION

Either the input_signal_level or the output_signal_level attribute is missing in a pin within a multiple power supply cell. By default, LC connect this pin to the default_power_supply defined in the power_supply() group in library.

WHAT NEXT

Check the library source file to see if you missed the input_signal_level or the output_signal_level attributes.

EXAMPLES

```
    power_supply() {
        default_power_rail : VDD0;
        power_rail(VDD1, 5.0);
        power_rail(VDD2, 3.3);
    }

cell(lbdb428) {
  area : 2;
  pad_cell : true;
  rail_connection(PV1, VDD1);
  rail_connection(PV2, VDD2);
  pin(A) {
    direction : input;          /
* missing input_signal_level attribute, will use default VDD0 */
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A";
    output_signal_level : VDD2;
    timing() {
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
}
```

EXAMPLE MESSAGE

```
Warning: Line 96, Connect pin 'A' to the default_power_supply 'VDD0'
       defined in the power_supply() group in library. (LBDB-615)
```

LBDB-616 (error) Found the timing arc '%s' has lookup table or poly template
which is more than %s dimensional in a '%s' timing group in the library

DESCRIPTION

In the timing group reported, since the related_pin and constraint_pin are the same, there can not be a two-dimension or more lookup table/poly template based on related_pin_transition and constraint_pin_transition because they are the same pin and one pin can not have two different values at the same time.

Specially, for min_pulse_width timing group, since the arc can be indexed by the output load, thus it can be 1D or 2D.

WHAT NEXT

Modify the timing arc based on a one-dimensional lookup table or poly template.

EXAMPLES

```
lu_table_template  (table_2)   {
   variable_1  :  constrained_pin_transition  ;
   variable_2  :  related_pin_transition  ;
   index_1 ("0.00, 0.25, 0.50") ;
   index_2 ("0.00, 0.50, 2.00") ;
}
```

```
    timing() {
      related_pin : CP ;
      timing_type : min_pulse_width ;
      rise_constraint(table_2) {
          index_1 ("0.00, 1.00, 2.50") ;
          index_2 ("0.00, 1.00, 2.50") ;
          values (\n
                  "4.0, 5.0, 6.0"\n
                  "4.2, 5.2, 6.2"\n
                  "4.4, 5.4, 6.4"\n
          );
      }
      fall_constraint(table_2) {
          index_1 ("0.00, 1.00, 2.50") ;
          index_2 ("0.00, 1.00, 2.50") ;
          values (\n
```

```
                "4.0, 5.0, 6.0"\n
                "4.2, 5.2, 6.2"\n
                "4.4, 5.4, 6.4"\n
        );
    }
```

EXAMPLE MESSAGE

```
Error: Line 160, Found the timing arc 'rise_constraint' has lookup table or poly te
mplate


which is more than one dimensional in a min_pulse_width timing group in the library
 (LBDB-616)
```

LBDB-617 (warning) The related pin in a '%s' timing group is specified as '%s', not the pin '%s' itself. It is reset to pin '%s'.

DESCRIPTION

In the timing group reported, since the related_pin and constraint_pin are the same, the related_pin attribute is optional and has be to set to the pin itself.

WHAT NEXT

Either delete the related_pin attribute or set the attribute to the pin's name.

EXAMPLES

```
pin(CP) {
 ...
  timing() {
    related_pin : D ;
    timing_type : min_pulse_width ;
    rise_constraint(table_2) {
        index_1 ("0.00, 1.00, 2.50") ;
        index_2 ("0.00, 1.00, 2.50") ;
        values (\n
                "4.0, 5.0, 6.0"\n
                "4.2, 5.2, 6.2"\n
                "4.4, 5.4, 6.4"\n
        );
    }
    fall_constraint(table_2) {
        index_1 ("0.00, 1.00, 2.50") ;
        index_2 ("0.00, 1.00, 2.50") ;
```

```
          values (\n
                  "4.0, 5.0, 6.0"\n
                  "4.2, 5.2, 6.2"\n
                  "4.4, 5.4, 6.4"\n
          );
      }
  }
```

need to delete related_pin attribute or set it as
related_pin : CP ;

EXAMPLE MESSAGE

Warning: Line 160, The related pin in a min_pulse_width timing group is specified a
s 'D', not

the pin 'CP' itself. It is reset to pin 'CP'. (LBDB-617)

LBDB-618 (error) The min/max_clock_tree_path timing arc contains illegal rise/fall_propagation group.

DESCRIPTION

In a min/max_clock_tree_path timing arc, only cell_rise group or cell_fall group or
both are allowed

WHAT NEXT

Delete the illegal rise/fall_propagation group

EXAMPLES

```
  pin(CP) {
   ...
    timing() {
      related_pin : CLK ;
      timing_type : min_clock_tree_path ;
      rise_propagation(table_2) {
          index_1 ("0.00, 1.00, 2.50") ;
          values (\n
                  "4.0, 5.0, 6.0"\n
          );
      }
      fall_propagation(table_2) {
          index_1 ("0.00, 1.00, 2.50") ;
          index_2 ("0.00, 1.00, 2.50") ;
          values (\n
                  "4.0, 5.0, 6.0"\n
```

```
          );
      }
  }
```

need to delete both rise_propagation and fall_propagation lookup table and replace with
cell_rise and cell_fall lookup tables

EXAMPLE MESSAGE

Warning: Line 160, the min/max_clock_tree_path timing arc containts illegal rise/ fall_progagation group (LBDB-618)

LBDB-619 (error) The '%s' attribute cannot be specified on the %s %s.

DESCRIPTION

This error message occurs when you specify an invalid attribute for an object. As shown in the following example, the **output_signal_level_high** attribute is invalid for a pin object, causing the error message:

```
cell(lbdb600) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1.0;
    output_signal_level_high : 1.2;
    ...
  }
  ...
}
```

```
   Error: Line 84, The 'output_signal_level_high' attribute cannot be specified on the
          pin 'A'. (LBDB-619)
```

WHAT NEXT

Remove the attribute from the pin and rerun the command.

LBDB-620 (warning) The lookup table domain '%s' is defined multiple times

within ’%s’. Using the last one encountered.

DESCRIPTION

This message indicates that the same lookup table domain has been defined for multiple times within one timing/power arc. In the case of a domain conflict, Library Compiler ignores all except the last domain encountered during the compilation. The compiled database contains the last domain only.

WHAT NEXT

Make sure that only define one lookup table for each domain for each timing/power arc.

EXAMPLES

```
cell_rise(li7X7){
  domain(D1) { ... }
  domain(D1) { ... }
  domain(D2) { ... }
}
```

EXAMPLE MESSAGE

```
Warning: Line 987, The lookup table domain ’D1’ is defined multiple times
         within ’cell_rise’. Using the last one encountered. (LBDB-620)
```

LBDB-621 (error) Invalid calc_mode ’%s’ is detected. This name must be unique among domains within one lu_table_template.

DESCRIPTION

This message indicates a duplicate calc_mode defined among domains within one lu_table_template.

WHAT NEXT

Change the name of the pin, bus, bundle, rail_connection in the technology library.

EXAMPLES

```
lu_table_template(li7X7){
  domain(D1) {
    calc_mode : "CM1";
```

```
    . . .
  }
  domain(D2) {
    calc_mode : "CM1";
    . . .
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 56, Invalid calc_mode 'CM1' is detected. This name must be
       unique among domains within one lu_table_template. (LBDB-621)
```

LBDB-622 (error) The '%s' attribute is missing for the %s %s.

DESCRIPTION

This error message occurs because either the **max_input_noise_width** or the **min_input_noise_width** attribute is missing when both attributes are required.

This message also occurs when **input_signal_level** and **output_signal_level** are not defined in the input/output pin of a level shifter or isolation cell.

WHAT NEXT

Check the library source file, and add the missing attribute.

LBDB-623 (error) The '%s' attribute is larger than the %s '%s' %sfor the %s %s.

DESCRIPTION

This error message occurs when the **min_input_noise_width** attributed value is larger than the max_input_noise_width attribute value. Library Compiler requires that the **min_input_noise_width** value be no larger than the **max_input_noise_width** value.

The following example shows **min_input_noise_width** set at a higher value than **max_input_noise_width** and the resulting error message.

```
pin(S) {
  min_input_noise_width : 2.0;
  max_input_noise_width : 1.0;
  ...
  }
```

```
   Error: Line 18, The 'min_input_noise_width' attribute is larger than
   the 'min_input_noise_width' attribute for the pin '%s'.  (LBDB-623)
```

This error message also occurs when any of the following are true:

- The value of **output_signal_level_high** is greater than **output_signal_level_low**.
- The value of **output_signal_level_high** is greater than output_signal_level.
- The value of **input_signal_level_high** is greater than **input_signal_level_low**.
- The value of **input_signal_level_high** is greater than **input_signal_level**.

WHAT NEXT

Change all related values to conform to the requirement and rerun the command.

LBDB-624 (error) The output/inout pin '%s' has illegal 'tied-off' timing arcs.

DESCRIPTION

If a output pin is not tied to "high"(the function attribute is set to "1") or "low"(the function attribute is set to "0"), its time arcs should not set the 'tied-off' attribute to true.

WHAT NEXT

Delete the 'tied-off' attribute.

EXAMPLES

```
  pin(S) {
   function : "A B";
   ...
    timing() {
      tied_off : true;
      steady_state_current_high(table_1) {
          index_1 ("0.00, 1.00, 2.50") ;
          values (\n
                  "4.0, 5.0, 6.0"\n
  ...
          );
      }
      ...
  }
```

need to delete the 'tied-off' attribute.

EXAMPLE MESSAGE

Warning: Line 160, The output pin 'S' has illegal 'tied-off' timing arcs. (LBDB-624)

LBDB-625 (error) The output/inout pin '%s' has a 'tied-off' timing arc containing illegal '%s' %s.

DESCRIPTION

If a output pin is tied to "high"(the function attribute is set to "1"), only steady_state_current_high group is allowed in its timing arc whose 'tied_off' attribute is set to true.

WHAT NEXT

Delete the illegal noise_immunity/noise_propagation groups.

EXAMPLES

```
  pin(S) {
   function : "1";
   ...
    timing() {
      tied_off : true;
      steady_state_current_high(table_1) {
          index_1 ("0.00, 1.00, 2.50") ;
          values (\n
                  "4.0, 5.0, 6.0"\n
  ...
          );
      }
      ...
  }
```

need to delete the 'steady_state_current_high' table.

EXAMPLE MESSAGE

Warning: Line 160, The output pin 'S' has a 'tied-
off' timing arc containing illegal 'steady_state_current_high' group. (LBDB-625)

LBDB-626 (error) The ’tied-off’ timing arc contains illegal noise_immunity/noise_propagation group.

DESCRIPTION

In a timing arc whose tied_off attribute is set to true, for noise information, only steady_state_current_low group or steady_state_current_high group is allowed

WHAT NEXT

Delete the illegal noise_immunity/noise_propagation groups.

EXAMPLES

```
  pin(CP) {
   ...
    timing() {
      tied_off : true;
      noise_immunity_high(table_1) {
          index_1 ("0.00, 1.00, 2.50") ;
          index_2 ("0.00, 1.00, 2.50") ;
          values (\n
                  "4.0, 5.0, 6.0"\n
  ...
          );
      }
      ...
  }
```

need to delete the ’noise_immunity_high’ table.

EXAMPLE MESSAGE

Warning: Line 160, the ’tied-off’ timing arc containts illegal noise_immunity/ noise_propagation group (LBDB-626)

LBDB-627 (error) The ’%s’ group of the ’%s’ timing arc is not referencing the compatible template.

DESCRIPTION

In the min_pulse_width timing arc reported, the only valid templates are as follows: 1. "constrained_pin_transition" (1-dimentional) 2. "related_pin_transition" (1-dimentional) 3. "constrained_pin_transition" + "related_out_total_output_net_capacitance" 4. "related_pin_transition" +

"related_out_total_output_net_capacitance"

WHAT NEXT

Change the variable in the template accordingly.

EXAMPLES

```
lu_table_template  (table_1)   {
   variable_1  :  related_pin_transition  ;
   index_1 ("0.10, 0.25, 0.50") ;
}
lu_table_template  (table_2)   {
   variable_1  :  related_out_total_output_net_capacitance;
   index_1 ("0.10, 0.25, 0.50") ;
}
```

```
    timing() {
      related_pin : CP ;
      timing_type : min_pulse_width ;
      rise_constraint(table_2) {
          index_1 ("0.50, 1.00, 2.50") ;
          values (\n
                  "4.0, 5.0, 6.0"\n
          );
      }
      fall_constraint(table_1) {
          index_1 ("0.50, 1.00, 2.50") ;
          values (\n
                  "4.0, 5.0, 6.0"\n
          );
      }
```

change the template table_2 to

```
lu_table_template (table_2) { variable_1 : constrained_pin_transition ; index_1
("0.10, 0.25, 0.50") ; }
```

EXAMPLE MESSAGE

```
Error: Line 160, The 'rise_constraint' group of the 'min_pulse_width' timing arc

      is not referencing the compatible template.  (LBDB-627)
```

LBDB-628 (error) The value of timing_sense attribute is invalid for
the timing arc whose timing_sense should be ’%s’ instead.

DESCRIPTION

The timing arc with feed_through_type attribute must have ’positive_unate’ timing_sense.

WHAT NEXT

Check the timing arc and make the correction accordingly.

EXAMPLES

```
...
        pin(Z) {
          direction : inout;
          timing() {
            feed_through_type : short;
    timing_sense : negative_unate;
            ...
          }
        }
...
```

In this case, the timing sense should be "positive_unate".

EXAMPLE MESSAGE

Error: Line 256, The value of timing_sense attribute is invalid for the timing arc whose timing_sense should be ’positive_unate’ instead. (LBDB-628)

LBDB-629 (error) The parent ’%s’ of the user-defined attribute is not defined.

DESCRIPTION

For define(name, parent, type), parent must be the name of a user-defined group or a predefined library group.

WHAT NEXT

Either change the parent name or define a new user-defined group with the parent name.

EXAMPLES

```
    library(test) {
      define(a, test, string);
...
    }
```

Since "test" is not defined, we can define a new user-defined group call "test" by adding the following statement: define_group(test, library);

EXAMPLE MESSAGE

```
Error: Line 256, The parent 'test' of the user-
defined attribute is not defined. (LBDB-629)
```

LBDB-630 (error) The 'user_parameters' group is not specified.

DESCRIPTION

This message indicates that the 'user_parameters' group is not specified. Library Compiler errors out because some generic parameters(parameter1..5) are used in either poly_template or power_poly_template, and the 'user_parameters' must be defined to contain the definition of those generic parameters.

WHAT NEXT

Add the missing attribute to the 'user_parameters' group. the message.

EXAMPLES

```
    user_parameters() {
      parameter1 : 0.80;
    }
```

EXAMPLE MESSAGE

```
Error: Line 52, The 'user_parameters' group is not specified. (LBDB-630)
```

LBDB-631 (error) The '%s' attribute in the 'user_parameters'

group is not specified.

DESCRIPTION

This message indicates that an attribute is missing, and Library Compiler errors out because this attribute is used in either poly_template or power_poly_template.

WHAT NEXT

Add the missing attribute to the 'user_parameters' group. the message.

EXAMPLES

```
user_parameters() {
  parameter1 : 0.80;
}
```

EXAMPLE MESSAGE

Error: Line 52, The 'parameter2' attribute in the 'user_parameters' group is not s
pecified. (LBDB-631)

LBDB-632 (error) The power rail name '%s' is invalid.

DESCRIPTION

This message indicates that you specified an invalid name for the current power rail. The name should not conflict with the generic parameters(parameter1..paramter5).

WHAT NEXT

User a different name that is not conflicting with parameter1..paramter5.

EXAMPLES

```
 power_supply() {
         default_power_rail : VDD0;
 power_rail(parameter1, 4.95);
}
```

EXAMPLE MESSAGE

Error: Line 104, The power rail name 'parameter1' layer name is invalid. (LBDB-632)

LBDB-633 (error) The %s value, '%s', has not been defined in the %s.

DESCRIPTION

This message indicates that the referred value is undefined in the library.

WHAT NEXT

Add the referred value in the library.

EXAMPLES

```
  part(a) {
    valid_speed_grades ("A","B","C");
    valid_step_levels ("step0","step1","step3");
    default_step_level : "step0";
    speed_grade("D") {
step_level("step0");
    }
  }
```

In this case, the "D" valid_speed_grade is not defined.

EXAMPLE MESSAGE

```
Error: Line 57, The valid_speed_grade value, 'D',
       has not been defined in the part. (LBDB-74)
```

LBDB-634 (error) The "variables" definition is conflicting with the main template.

DESCRIPTION

This message indicates that you specified an invalid 'variables' for the current poly template domain. It's required that a poly template define the same 'variables' as that of its main poly template.

WHAT NEXT

User the same 'variables' definition as that of its main poly template.

EXAMPLES

```
  poy_template(T3) {
```

```
      variables (input_net_transition, voltage, temperature);
      . . .
   domain(D1) {
      variables (input_net_transition, voltage);
      . . .
   }
}
```

EXAMPLE MESSAGE

```
Error: Line 124, The "variables" definition is conflicting with its main template.
(LBDB-634)
```

LBDB-635 (error) The ’tied-off’ timing arc contains illegal related_pin attribute.

DESCRIPTION

In a timing arc whose tied_off attribute is set to true, related_pin attribute is not allowed.

WHAT NEXT

Delete the related_pin attribute.

EXAMPLES

```
pin(CP) {
 ...
  timing() {
    tied_off : true;
    ...
    related_pin : A;
    }
    ...
}
```

need to delete the ’related_pin’ attribute.

EXAMPLE MESSAGE

```
Warning: Line 160, the ’tied-
off’ timing arc containts illegal related_pin attribute. (LBDB-635)
```

LBDB-636 (error) The ’%s’ attribute value is invalid for the timing

arc.

DESCRIPTION

This message indicates for a timing arc that the attribute value is invalid. For example, clock_gate_check attribute can only be defined to "true" for the setup/hold/nochange timing arcs.

WHAT NEXT

Remove the attribute from the timing arc.

LBDB-637 (error) The %s-associated '%s' lookup table cannot use '%s' as its template.

DESCRIPTION

This message can be used as generic error message template. For frequency-base max_cap, it means that: 1. the max_cap lookup table in an input-associated max_cap group must use a one-dimensional template with **frequency** as its variable. 2. the max_cap lookup table in an ouput-associated max_cap group must use a one-dimensional template with **frequency** as its variable, or a two-dimensional template with **frequency** and **total_output_net_capacitance** as its variables with **frequency** being the first variable.

WHAT NEXT

For more information about lookup tables, see the *Library Compiler User Guide*. Change the library source file by referencing a different template in the lookup table description.

EXAMPLES

```
  maxcap_lut_template(ok_temp) {
    variable_1 : frequency;
    index_1("0, 1, 2, 3");
  }
  maxcap_lut_template(err_temp) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
  }

max_cap(err_temp) {
values ("1, 2, 3, 4");
}
```

To fix the problem, change the template value of the **max_cap** attribute from *err_temp*

to *ok_temp*.

EXAMPLE MESSAGE

```
Error: Line 126, The input-associated 'max_cap' lookup table
       cannot use 'err_temp' as its template. (LBDB-637)
```

LBDB-638 (error) It is invalid to specify the '%s' %s on an %s pin.

DESCRIPTION

This message indicates that you specified a invalid group on a pin.

WHAT NEXT

Check the library source file, and correct the problem.

EXAMPLES

```
pin (p) {
  direction : input;
  ...
  max_cap (test) {
    ...
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 67, It is invalid to specify the 'max_cap' group
on an input pin. (LBDB-638)
```

LBDB-639 (warning) The '%s' %s in this timing arc are ignored.

DESCRIPTION

This message indicates that you specified a redundant attribute or group for the sequential half-nate timing arcs.

In the following example, both the cell_fall group and the fall_transition group are redundant for the sequential half-unate timing arc.

```
 timing() {
   timing_type : rising_edge;
   timing_sense : positive_unate;
   cell_rise( f_ocap ){
     index_1 ( "0.0000, 1.0000, 512.0000, 7999.9995, 15999.9990, 31999.9980, 63999.
9961");
     values ( "25.0000, 35.0000, 5145.0000, 80024.9922, 160024.9844, 320024.9688, 6
40024.9375");
   }
   rise_transition( f_ocap ){
     index_1 ( "0.0000, 1.0000, 512.0000, 7999.9995, 15999.9990, 31999.9980, 63999.
9961");
     values ( "15.0000, 25.0000, 5135.0000, 80014.9922, 160014.9844, 320014.9688, 6
40014.9375");
   }
   cell_fall( f_ocap ){
     index_1 ( "0.0000, 1.0000, 512.0000, 7999.9995, 15999.9990, 31999.9980, 63999.
9961");
     values ( "25.0000, 35.0000, 5145.0000, 80024.9922, 160024.9844, 320024.9688, 6
40024.9375");
   }
   fall_transition( f_ocap ){
     index_1 ( "0.0000, 1.0000, 512.0000, 7999.9995, 15999.9990, 31999.9980, 63999.
9961");
     values ( "15.0000, 25.0000, 5135.0000, 80014.9922, 160014.9844, 320014.9688, 6
40014.9375");
   }
 }

 Warning: Line 639, The cell_fall group in this
    timing arc are ignored. (LBDB-390)
 Warning: Line 639, The fall_transition group in this
    timing arc are ignored. (LBDB-390)
```

WHAT NEXT

Remove the redundant groups from the timing arc and rerun the command.

LBDB-640 (error) The ’%s’ attribute %s in this %s group.

DESCRIPTION

This message indicates you need to specify or remove an attribute from the group according to the template it references as follows: 1. 1-dimentional template does not allow the ’related_pin’ attribute. 2. 2-dimentional template requires the ’related_pin’ attribute.

WHAT NEXT

Change the technology library source file to add or delete the specified attribute.

EXAMPLES

```
        max_cap(maxcap_1d_template) {
                values ("1, 2, 3, 4");
        related_pin : "A";
        }
```

In this case, the 'related_pin' attribute is not allowed in 1-dimensional lookup table. To fix the problem, remove the related_pin attribute from the max_cap group.

EXAMPLE MESSAGE

```
Error: Line 69, The 'related_pin' attribute cannot be specified
in this max_cap group. (LBDB-640)
```

LBDB-641 (error) The '%s' %s has some %s groups missing the %s attribute.

DESCRIPTION

This message indicates there is one or more leakage_power(internal) groups without the power_level attribute. When at least one leakage_power(internal_power) is specified with the power_level attribute in a cell(pin), all the leakage_power(internal_power) in the cell must also have the power_level attribute defined.

It can also be used to notify a user that teh related_pg_pin attribute is missing in the leakage_power/internal_power groups.

WHAT NEXT

Add the missing attribute for the leakage_power group.

EXAMPLES

```
  cell(AN2) {
      leakage_power () {
power_level : VDD1;
value : 1.0;
      }
      leakage_power () {
/* power_level : VDD2; */
value : 2.0;
      }
```

```
    ...
  }
```

In this case, the power_level attribute is missing for the 2nd leakage_power. To fix the problem, add the attribute to the leakage_power group:

```
  cell(AN2) {
      leakage_power () {
        power_level : VDD1;
        value : 1.0;
      }
      leakage_power () {
        power_level : VDD2;
        value : 2.0;
      }
      ...
  }
```

EXAMPLE MESSAGE

```
Error: Line 12, The 'AN2' cell has some leakage_power groups
missing the power_level attribute. (LBDB-641)
```

LBDB-642 (warning) The group '%s' is defined multiple times in group '%s'. Using the last one encountered.

DESCRIPTION

Some groups require that no more than one same group be defined in their scope.

Some groups require when statement, and only one of them can be defined without when statement in their scope.

WHAT NEXT

Remove the extra objects.

EXAMPLES

```
   pin_capacitance ()  {
     rise_capacitance_range() { ... }
     rise_capacitance_range() { ... }
   }
```

EXAMPLE MESSAGE

```
Warning: Line 987, The group 'rise_capacitance_range' is defined multiple times
        in group 'pin_capacitance'. Using the last one encountered. (LBDB-642)
```

EXAMPLES

```
cell(test) {
...
leakage_current ()  {
  when : A;
  pg_current(VDD) {
    value : 5.3;
  }
}
leakage_current ()  {
  when : A1;
  pg_current(VDD) {
    value : 15.3;
  }
}
...
leakage_current ()  {
  pg_current(VDD) {
    value : 0.3;
  }
}
leakage_current ()  {
  pg_current(VDD) {
    value : 8.3;
  }
}
...
```

Only one of leakage_current groups with no 'when' statement can be defined under a cell. If there are more than one group with no 'when' statement defined, then they are duplicated groups.

The rule is applied to intrinsic_parasitic and va_leakage_current groups as well. q

For va_leakage_current, if two of va_leakage_current groups are under the same cell_based_variation and both have same va_value and with no state condition, then they are duplicated groups.

```
cell(test) {
...
power_cell_type : macro;
intrinsic_parasitic() {
 when : "!A1 & !A2 & !ZN";
 total_capacitance(V2) {
    value : 9.0;
 }
 total_capacitance(G1) {
    value : 62.2;
 }
 total_capacitance(G2) {
    value : 31.47;
 }
}
intrinsic_parasitic() {
```

```
    when : "!A1 & A2 & !ZN";
    total_capacitance(V2) {
       value : 9.0;
    }
    total_capacitance(G1) {
       value : 62.2;
    }
    total_capacitance(G2) {
       value : 31.47;
    }
  }

   ...
```

If power_cell_type is macro, then only one intrinsic_parasitic can be specified under a cell. In this case, there are two intrinsic_parasitic groups under cell "test", which is wrong. The first intrinsic_parasitic will be removed, and only the second one will be kept.

EXAMPLE MESSAGE

```
Warning: Line 138, The group 'leakage_current' is defined multiple times
        in group 'cell'. Using the last one encountered. (LBDB-642)
```

LBDB-643 (error) '%s' is used more than once inside cell '%s'.

DESCRIPTION

This error message occurs when unique **power_gating_pin** attribute value is specified more than once within a cell.

The following example shows power_pin_1 specified twice within a cell and the resulting error message:

```
     cell (BUF) {
       pin(A) {
         power_gating_pin (power_pin_1, "0") ;
         direction : input;
       }
       pin(B) {
         power_gating_pin (power_pin_1, "0") ;
         direction : output;
       }
     }

   Error: Line 56, 'power_pin_1' is used more than once inside cell 'BUF'.
   (LBDB-643)
```

WHAT NEXT

Make sure that each unique **power_gating_pin** value is specified only once.

LBDB-644 (warning) The cell_leakage_power attribute of the '%s' cell is redundant and not used in the leakage_power modeling.

DESCRIPTION

This message indicates one of the following two cases are true: 1. there is power_level specific leakage_power groups in the cell 2. the cell has no power_level specific leakage_power groups, and it has default leakage_power group(leakage_power group without 'when' statement).

WHAT NEXT

Remove the 'cell_leakage_power' from the cell.

EXAMPLES

```
  cell(AN2) {
      cell_leakage_power : 0.5;
      leakage_power () {
power_level : VDD1;
when : "A";
value : 1.0;
      }
      ...
  }
```

In this case, the cell has power_level specific leakage_power groups, thus the cell_leakage_power attribute is redundant. To fix the problem, remove the attribute from the cell group.

EXAMPLES

```
  cell(AN2) {
      cell_leakage_power : 0.5;
      leakage_power () {
        when : "A";
        power(LKP_T) {
           orders ("1, 1");
           coefs  ("1, 1, 1, 1");
           domain (D1) {
                 orders ("1, 1");
                 coefs  ("1, 1, 1, 1");
   }
```

```
}
      }
      ...
  }
```

In this case, a cell_leakage_power attribute is redundant. To fix the problem, remove the attribute from the cell group:

```
Warning: Line 12, The cell_leakage_power attribute of the 'AN2' cell is redundant
and not used in the leakage_power modeling. (LBDB-644)
```

LBDB-645 (error) Cannot find the '%s' %s in the %s.

DESCRIPTION

This error message occurs when a power_rail name attached to a **related_power_rail** or **rail_value** attribute does not exist in the power_supply.

This error message also occurs when the **default_power_rail** attribute is not defined in the power_supply group.

The following code does not contain VDD4 in the power_supply, which results in the error message.

```
     library(libg5) {
       ...
       power_supply(pw) {
         default_power_rail : VDD;
          power_rail (VDD1, 2.0);
          power_rail (VDD2, 2.5);
          power_rail (VDD3, 3.0);
          power_rail (VSS1, 3.0);
          power_rail (VSS2, 3.0);

          mapping(VSS1) {
                  related_power_rail : "VDD1 VDD2";
          }
          mapping(VSS2) {
                  related_power_rail : "  VDD4 VDD3       ";
          }
        }

    }

   Error: Line 403, Cannot find the 'VDD4' power_rail in the power_supply.
   (LBDB-645)
```

WHAT NEXT

Check your library for an incorrect power_rail name, correct the name, and run the

command again.

LBDB-646 (error) No %s information is defined before the %s '%s'.

DESCRIPTION

This error message occurs when you have not defined the power_supply statement for the power_level.

This message also occurs when the power_supply group is missing for a cell rail_connections because some pins of the cell do not define the **input_signal_level** (for an input pin) or the **output_signal_level** (for an output pin).

The following example shows a library with a missing power_supply statement before the cell containing the power_level attribute and the resulting error message.

```
library(lib) {
 ...
 cell (A)
   ...
   leakage_power() {
  power_level : "VDD";
   ...
   }
   ...
}
```

```
Error: Line 191, No power_supply information is defined before the
power_level 'VDD'. (LBDB-646)
```

WHAT NEXT

Add the power_supply statement before the cell statement that contains the power_level, as shown in the following example:

```
 power_supply() {
       default_power_rail : VDD;
       power_rail (VDD, 2.0);
  ...
 }
```

LBDB-647 (warning) Found the obsolete and unsupported '%s'

%s in the '%s' cell; use '%s' instead.

DESCRIPTION

The **rail_connection** attribute is not supported after 2004.12 Beta version. Instead, the information should now be described in the power_pin group.

The following is an example of the error message:

```
Warning: Line 159, Found the obsolete and unsupported 'rail_connection'
attribute in the 'sample' cell; use 'power_pin' group instead. (LBDB-647)
```

WHAT NEXT

If you have access to the technology library source file, change the **rail_connection** attribute to power_pin group. Otherwise, contact the vendor and inform them of the problem.

LBDB-648 (error) The power_pin definitions of cell '%s' do not follow the mapping rules specified in the power_supply group.

DESCRIPTION

This error message occurs when the definitions of the power_pins do not follow the mapping rules in the power_supply group. The following is an example of this error message:

```
Warning: Line 159, The power_pin definitions of cell '%s' do not follow
the mapping rules in the power_supply group. (LBDB-648)
```

WHAT NEXT

Either change the mapping rules in the power_supply group or redefine the power_pins and run the command again.

LBDB-649 (error) The '%s' domain's power rail mapping information conflicts with its main template.

DESCRIPTION

This error message occurs when the power rail mapping information is incorrectly

defined in the domain of the poly_template. The information in poly_template domain must be exactly the same as the poly_template.

The following example shows the *d1* domain of the *p1* poly_template with the incorrect mapping statement and the resulting error message:

```
poly_template(p1) {
  ...
  mapping(voltage1, VDD1);
  mapping(voltage, VDD0);
  ...
  domain(d1) {
    ...
    mapping(voltage1, VDD2);
    mapping(voltage, VDD0);
    ...
  }
}
```

```
Error: Line 191, The 'd1' domain's power rail mapping information
conflicts with its main template. (LBDB-649)
```

WHAT NEXT

Modify the mapping statements in this domain of the poly_template to match those of the poly_template.

The following example shows the correct *d1* domain mapping statements:

```
    mapping(voltage1, VDD1);
    mapping(voltage, VDD0);
```

LBDB-650 (error) The '%s' cell is not a valid %s.

DESCRIPTION

This error message occurs when the level shifter or isolation cell is incorrectly modeled. A level shifter or an isolation cell must satisfy one of the following sets of conditions:

• It has 3 pins, including 1 input pin, 1 level_shifter_enable_pin/ isolation_cell_enable_pin, 1 output pin.

• It has 2 pins, including 1 input pin and 1 output pin.

The following example shows the level shifter with the incorrect modeling and the resulting error message:

```
 cell(LS) {
is_level_shifter : true;
...
pin(a) {
     ...
}
pin(b) {
     ...
}
pin(c) {
     ...
}
pin(d) {
     ...
}
}
Error: Line 191, The 'LS' cell is not a valid level shifter. (LBDB-650)
```

WHAT NEXT

Correct the modeling information of the level shifter or isolation cell to satisfy the requirements.

You could correct the modeling in the previous example by removing one of the pins specified in the cell.

LBDB-651 (error) The %s%s '%s' contains the conflicting '%s'/'%s' values.

DESCRIPTION

This error message occurs when the **input_signal_level** and **output_signal_level** values are modeled incorrectly for the level shifter or isolation cell.

For a level shifter, **input_signal_level** in input pin can't be the same as **output_signal_level** in output pin. Meaning that the rail names can't be the same in a level shifter.

For an isolation cell, the value of **input_signal_level** in input pin can't be different from the value of **output_signal_level** in output pin. Meaning that the rail values can't be difference in an isolation cell.

EXAMPLES

The following example shows the level shifter with the incorrect modeling and the resulting error message:

```
cell(LS) {
```

```
 is_level_shifter : true;
 ...
 pin(in) {
      ...
input_signal_level : VDD2
 }
 pin(out) {
      ...
output_signal_level : VDD2
 }
}
```

```
Error: Line 191, The pins of level shifter 'LS' contain the
conflicting 'input_signal_level'/'output_signal_level' values. (LBDB-651)
```

WHAT NEXT

Modify the modeling information of the level shifter to meet the requirements.

To correct the modeling of the example above, make the **input_signal_level** string "VDD1" of the input pin different from the **output_signal_level** string "VDD2" of the output pin as follows:

```
   cell(LS) {
    is_level_shifter : true;
    ...
    pin(in) {
           ...
           input_signal_level : VDD1
    }
    pin(out) {
           ...
           output_signal_level : VDD2
    }
   }
```

EXAMPLES

The following example shows the isolation cell with the incorrect modeling and the resulting error message:

```
library(libdb651) {
  ...
  /* operation conditions */
  operating_conditions(5v_1v) {
    ...
    power_rail (VDDH, 5);    /* high power */
    power_rail (VDDL, 1);    /* low power */
    ...
  }
```

```
  ...
  default_operating_conditions : 5v_1v;

  ...
cell(ISO) {
 is_isolation_cell : true;
 ...
 pin(in) {
        ...
        input_signal_level : VDDH
 }
 pin(out) {
        ...
        output_signal_level : VDDL
 }
}
```

```
Error: Line 191, The pins of isolation cell 'ISO' contain the
conflicting 'input_signal_level'/'output_signal_level' values. (LBDB-651)
```

WHAT NEXT

Modify the modeling information of the isolation cell to meet the requirements.

To correct the modeling of the example above, make the **input_signal_level** value "5" of the input pin same as the **output_signal_level** value "1" of the output pin. You can assiged both to the same pin like "VDDH", so that both will refer to same value "5" in operating_conditions as follows.

```
   library(libdb651) {
     ...
     /* operation conditions */
     operating_conditions(5v_1v) {
       ...
       power_rail (VDDH, 5);    /* high power */
       power_rail (VDDL, 1);    /* low power */
       ...
     }
     ...
     default_operating_conditions : 5v_1v;

     ...
   cell(ISO) {
    is_isolation_cell : true;
    ...
    pin(in) {
           ...
           input_signal_level : VDDH
    }
    pin(out) {
           ...
           output_signal_level : VDDH
    }
```

```
}
```

SEE ALSO

LBDB-747

LBDB-652 (error) The %s '%s' has incompatible '%s' and '%s'.

DESCRIPTION

This error message occurs when the user specified attributes are incompatible. For example, specifying both **pulse_clock** and **generated_clock** inside a cell.

```
Error: Line 159, The cell 'A' has incompatible 'pulse_clock'
and 'generated_clock'.  (LBDB-652)
```

WHAT NEXT

Either remove the **pulse_clock**attribute or the **generated_clock** group for the cell.

LBDB-653 (error) The index of '%s' can define only one value.

DESCRIPTION

This error message occurs because the specified index cannot contain more than one value. This restriction applies to the dimension input_net_transition, and total_output_net_capacitance in the vector group.

The following example shows an index with more than one value and the resulting error message.

```
output_current_template(CCS_T) {
  variable_1 : input_net_transition;
  variable_2 : total_output_net_capacitance;
  variable_3 : time;
}
vector(CCS_T) {
 reference_time : 0.5;
      index_1 ("0.12");
 index_2 ("0.1, 1.2");
 index_3 ("0.01, 0.02, 0.03");
 values (" ... ");
}
```

```
   Error: Line 46, The index of 'total_output_net_capacitance' can
   only define one value. (LBDB-653)
```

To correct the error, change index_2 to ("0.1");

WHAT NEXT

Check the library source file and remove the extra values in the index definition.

LBDB-654 (error) The values of '%s' and '%s' are not consistent in %s '%s'.

DESCRIPTION

This error message occurs when the values of the **reference_time** and **input_net_transition** attributes are inconsistent inside the output_current_rise or output_current_fall group. Inside each output_current_rise or output_current_fall group, only the same pair of **reference_time** and **inout_net_transition** values is allowed.

Note: In 2007.03 release, the message is enhanced to also report inconsistent input_voltage_range and output_voltage_range values in a level shifter. Assuming that a level shifter defines the following information: level_shifter_type : <lst_val>; input_voltage_range(<<ivrl_val>, <ivrh_val>); output_voltage_range(<ovrl_val>, <ovrh_val>); then it must satisfy the following requirements: - if <lst_val> = HL, then <ivrh_val> > <ovrl_val>. - if <lst_val> = LH, then <ivrl_val> < <ovrh_val>. Otherwise, LC will issue LBDB-654 error.

The following is an example of inconsistent **reference_time** and **input_net_transition** values and the resulting error message:

```
  output_current_template(CCT) {
   variable_1 : input_net_transition;
   variable_2 : total_output_net_capacitance;
   variable_3 : time;
  }
  . . .
  output_current_rise() {
    vector(CCT) {
       reference_time : 0.11; <=== reference_time = 0.11 with input_net_transition
= 0.1
       index_1 ("0.1");
       index_2 ("1");
       index_3 ("1, 2, 3");
       values ("1, 2, 3");
    }
     vector(CCT) {
       reference_time : 0.12; <=== reference_time = 0.12 with input_net_transition
= 0.1
```

```
      index_1 ("0.1");
      index_2 ("2");
      index_3 ("1, 2, 3");
      values ("1, 2, 3");
   }
 }
```

```
Error: Line 98, The values of 'reference_time' are not consistent in
group 'output_current_rise'. (LBDB-654)
```

WHAT NEXT

Check the library source file, and correct the values of the **reference_time** attribute.

LBDB-655 (error) The vectors are not dense in group '%s'.

DESCRIPTION

This error message occurs because Library Compiler requires a vector for each input_net_transition and total_output_net_capacitance pair inside each output_current_rise or output_current_fall group.

The following example shows an output_current_rise group without a dense vector and resulting error message.

```
output_current_template(CCT) {
 variable_1 : input_net_transition;
 variable_2 : total_output_net_capacitance;
 variable_3 : time;
}
. . .
output_current_rise() {
  vector(CCT) {
     reference_time : 0.11;
     index_1 ("0.1");
     index_2 ("1");
     index_3 ("1, 2, 3");
     values ("1, 2, 3");
  }
   vector(CCT) {
     reference_time : 0.11;
     index_1 ("0.2");
     index_2 ("2");
     index_3 ("1, 2, 3");
     values ("1, 2, 3");
  }
  /* need vectors for (0.1, 2) and (0.2, 1) */
}
```

```
Error: Line 198, The vectors are not dense in group 'output_current_rise'.
(LBDB-655)
```

WHAT NEXT

Check the library source file and add a vector for each input_net_transition and total_output_net_capacitance pair.

LBDB-656 (error) The lu_table_template '%s' referred by '%s' in line %d is invalid.

DESCRIPTION

This error message occurs because the variable of the referred lu_table_template can only include the **input_net_transition** variable for the pin based receiver model. For the timing arc based receiver model, the variable of the referred lu_table_template can include **input_net_transiton** and **total_output_net_capacitance**.

The following example shows an invalid lu_table_template reference and the resulting error message:

```
lu_table_template(T1) {
 variable_1 : input_net_transition;
 variable_2 : total_output_net_capacitance;
 . . .
}
. . .
pin(A) {

receiver_capacitance() {
  receiver_capacitance1_rise(T1) {
     index_1 ("0.1, 0.1");
     index_2 ("1, 2");
     values ("1, 2", "2.5, 3");
  }
  . . .
}

Error: Line 298, The lu_table_template 'T1' referred by
 'receiver_capacitance1_rise' in line 1239 is invalid. (LBDB-656)
```

WHAT NEXT

Check the library source file, and correct the variable(s) of the corresponding lu_table_template.

LBDB-657 (error) Conflicting receiver model found in pin '%s' (pin-based) and in timing arc '%s-%s' (arc-based).

DESCRIPTION

This error message occurs because when an input (or inout) pin A defines a receiver_capacitance() group, then no timing arc whose from pin is A, can define receiver_capacitance1_rise/receiver_capacitance1_fall/ receiver_capacitance2_rise/ receiver_capacitance2_fall.

The following is an example of an incorrect definition and the resulting error message:

```
pin(A) {
  direction : input;
  receiver_capacitance() { . . .}
  . . .
}
pin(Y) {
  direction : output;
  timing() {
    receiver_capacitance1_rise(T1) { . . .}
    receiver_capacitance1_fall(T1) { . . .}
    receiver_capacitance2_rise(T1) { . . .}
    receiver_capacitance2_fall(T1) { . . .}
    . . .
  }
  . . .
}
```

```
Error: Line 398, Conflicting receiver model found in pin 'A' (pin-based) and in
timing arc 'A-Y' (arc-based). (LBDB-657)
```

WHAT NEXT

Check the library source file and remove the duplicated receiver model. Usually it is best practice to use the timing arc based receiver model.

LBDB-658 (error) Both variable and range of poly_template '%s' should be defined before domain '%s' is defined.

DESCRIPTION

You receive this message a domain can't be defined because either the variable or range statement of the main poly_template is missing.

WHAT NEXT

Make sure that **variables** and all **variable_n_range** statements exist before defining domains.

EXAMPLES

The following example shows the *p1* poly_template is missing both variable and range information.

```
poly_template(p1) {
 poly_template(PT)  {
  domain(D1)  {
    variables("temperature, total_output_net_capacitance");
    variable_1_range(0, 40);
    variable_2_range(1, 2);
  }
  ......
}
```

Correct it by add **variablesfp, variable_1_range** and **variable_2_range** statement in the poly_template group.

EXAMPLE MESSAGE

Error: Line 191, Both variable and range of poly_template 'PT' should be defined before domain 'D1' is defined. (LBDB-658)

LBDB-659 (error) The %s %s cannot coexist with the '%s' %s on the '%s' pin.

DESCRIPTION

The first specified attribute/group in the pin cannot coexist with the second specified attribute/group on the same pin. For example, the **is_three_state** attribute cannot be specified on a pin with **three_state** attribute.

WHAT NEXT

Check the specification of the cell, and make the appropriate change to the **driver_type** attribute or other attributes in the faulty pin group.

EXAMPLES

```
  cell(lbdb239) {
    area : 2;
    pin(A) {
```

```
      direction : input;
      capacitance : 1.0;
    }
    ...

    pin(Z) {
      direction : output;
      function : "A";
      three_state : "B"

      is_three_state : false; /* error */
      ...
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 84, The  "false" 'is_three_state' attribute cannot coexist
        with the 'three_state' attribute on the 'Z' pin. (LBDB-659)
```

LBDB-660 (error) It is invalid to specify the '%s' %s on the '%s' %s%s.

DESCRIPTION

This message indicates that you specified an invalid attribute/group on a cell.

WHAT NEXT

Check the library source file, and correct the problem. For example, in order to specify the "clocked_cell" attribute, the cell needs to satisfy the following 2 conditions: - has only 1 clock pin whose "clock" attribute is set to "true". - has at least 1 timing arc between the clock pin and an output pin.

EXAMPLES

```
  cell (p) {
    clocked_cell : rising_edge;
    pin(clk) {
      clock : true;
    }

    pin(out) {
      function : "clk";
    }
  }
```

To solve this issue, we need to add "combinational" timing arcs between "clk" pin and "out" pin.

EXAMPLE MESSAGE

```
Error: Line 67, It is invalid to specify the 'clocked_cell' attribute
on the 'p' cell. (LBDB-660)
```

LBDB-661 (error) The 'generic' integrated clock gating cell should not define the 'statetable' group. It should use 'ff' group or 'latch' group instead.

DESCRIPTION

This message indicates that you specified the 'generic' integrated gating clock cell with 'statetable' definition, You should define 'ff/latch' group instead.

WHAT NEXT

Change the library source file, and replace the statetable group with the ff/latch group of the specified cell.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "generic";

  statetable(" CP EN ", "IQ ") {
     table : " L  L  : - : L ,
               L  H  : - : H ,
               H  -  : - : N ";
  }
  ...
}
```

The modified cell description should be :

```
cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "generic";

  latch("IQ","IQN") {
    enable : "CP'";
    data_in : "EN";
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The 'generic' integrated clock gating cell should not define the '
statetable' group.
It should use 'ff' group or 'latch' group instead. (LBDB-661)
```

LBDB-662 (warning) The %s is not defined. operating_conditions "nom_pvt" is created and set as the default_operating_conditions.

DESCRIPTION

This warning message occurs when the **default_operating_conditions** is undefined and there is eith no operating_conditions groups defined or multiple operating_conditions defined.

WHAT NEXT

If you do not want Library Compiler to create the default operating_conditions for you, please check your library to define the relative operating_condition group and set it as the default_operating_conditions with the library-level attribute "default_operating_conditions".

LBDB-663 (warning) The %s is not defined. operating_conditions '%s' is set as the default_operating_conditions.

DESCRIPTION

This warning message occurs when the **default_operating_conditions** is undefined and there is extactly 1 operating_conditions group defined in the library.

WHAT NEXT

If you do not want Library Compiler to automatically set the default operating_conditions for you, please check your library to define the relative operating_condition group and set it as the default_operating_conditions with the library-level attribute "default_operating_conditions".

LBDB-664 (error) The '%s' attribute of the '%s' has a value '%g',

which should be %s for the %s.

DESCRIPTION

The value specified is less than/larger than/equal to a threshold value 0.0 for the attribute.

WHAT NEXT

Check the library source file and correct the problem.

EXAMPLES

```
      output_current_rise(current_template_8x7) {
        vector(current_template_8x7) {
           reference_time : 0.0140609;
           index_1("0");
           index_2("0.019368");
           index_3("0.1462, 0.175, 0.19, 0.205, 0.235, 0.25, 0.265, 0.275, 0.29, 0.
305, 0.32, 0.35, 0.406591");
           values("-
0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3");
        }
      }
```

EXAMPLE MESSAGE

Error: Line 35, The ’values’ attribute of the ’vector’ has a value ’-0.100000’, which should be positive for the output_current_rise vector. (LBDB-664)

LBDB-665 (error) The %s value of the ’%s’ attribute of the ’%s’ is the peak value.

DESCRIPTION

The frist value specified in the specified attribute is a peak value, i.e., the maximun value for the values attribute of the vector of an output_current_rise group, or the minimum value for the values attribute of the vector of an output_current_fall group.

WHAT NEXT

Check the library source file and correct the problem.

EXAMPLES

```
      output_current_rise(current_template_8x7) {
        vector(current_template_8x7) {
           reference_time : 0.0140609;
           index_1("0");
           index_2("0.019368");
           index_3("0.1462, 0.175, 0.19, 0.205, 0.235, 0.25, 0.265, 0.275, 0.29, 0.
305, 0.32, 0.35, 0.406591");
           values("1.8, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3"
);
        }
      }
```

EXAMPLE MESSAGE

```
Error: Line 35, The first value of the 'values' attribute of the 'vector' is the pe
ak value. (LBDB-665)
```

LBDB-666 (warning) The '%s' has the same %s %g as the '%s' at line %d,
but the %s does not increase(from %g to %g)
with increasing %s (from %g to %g).

DESCRIPTION

For a timing arc, within each output_current_rise/fall group. for a given total_output_net_capacitance(load), teh reference_times should increase with the increasing input_transition_time(slew). This check is only useful for the signoff timing analysis with the 2004.12 and the relative sevice pack releases of PrimeTime.

WHAT NEXT

Check the library source file and correct the problem.

EXAMPLES

```
output_current_rise(current_template) {
...
       vector(current_template) {
                  reference_time : 0.0140609;
                  index_1("0.1"); /* load */
                  index_2("0.019368"); /* slew */
                  index_3("0.1462, 0.175, 0.19, 0.205, 0.235, 0.25, 0.265, 0.275, 0
.29, 0.305, 0.32, 0.35, 0.406591");
                  /* LBDB-664 */
                  values("0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.
2, 1.3");
```

```
               }
               vector(current_template) {
                  reference_time : 0.0319875;
                  index_1("0.1"); /* load */
                  index_2("0.049573"); /* slew */
                  index_3("0.160795, 0.185, 0.2, 0.23, 0.24, 0.255, 0.27, 0.285, 0.
295, 0.31, 0.325, 0.34, 0.355, 0.37, 0.4
175");
                  values("0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.
2, 1.3");
               }
...
}
```

EXAMPLE MESSAGE

```
Warning : Line 357, The 'vector' has the same total_output_net_capacitance 0.000000
 as the 'vector' at line 364,
but the reference_time does not increase(from 0.031987 to 0.026168)
with increasing input_net_transition (from 0.049573 to 0.094881). (LBDB-666)
```

LBDB-667 (error) The '%s' of the '%s' is %g, which should be positive.

DESCRIPTION

The reference_times in the vectors of output_current_rise/fall groups should NOT be zero or negative.

WHAT NEXT

Check the library source file and correct the problem.

EXAMPLES

```
      output_current_rise(current_template) {
...
        vector(current_template) {
           /* reference_time : 0.0961844; */
           reference_time : 0.0;  /* LBDB-667 */
           index_1("0");
           index_2("0.170393");
           index_3("0.254379, 0.295, 0.31, 0.325, 0.34, 0.355, 0.385, 0.4, 0.415, 0
.43, 0.445, 0.475, 0.543056");
           values("0.1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0");
        }
...
    }
```

EXAMPLE MESSAGE

```
Error : Line 373, The 'reference_time' of the 'vector' is 0.000000,
which should be positive. (LBDB-667)
```

LBDB-668 (warning) The final signal voltage of the %s is %g, which does not reach within the 5 percent of the rail voltage %g.

DESCRIPTION

For each output_current_rise/fall vector, the final signal voltage must be within the 5% of the final rail voltage. This can be descibed with the following formulas:

If output_signal_level_low and output_signal_level_high are specified, volt_low = output_signal_level_low; volt_high = output_signal_level_high; Else volt_low = VSS; volt_high = VDD;

1. For the output_current_rise vector, Vfinal = volt_low + (0.5/Cout)*(I2+I1)*(T2-T1)+...+(0.5/Cout)*(In+In-1)*(Tn-Tn-1) and fabs(Vfinal - volt_high) must NOT be greater than 0.02 (volt_high - volt_low) 2. For the output_current_fall vector, Vfinal = volt_high + (0.5/Cout)*(I2+I1)*(T2-T1)+...+(0.5/Cout)*(In+In-1)*(Tn-Tn-1) and fabs(Vfinal - volt_low) must NOT be greater than 0.02 (volt_high - volt_low)

WHAT NEXT

Check the library source file and correct the problem.

EXAMPLE MESSAGE

```
Error : Line 373, The final signal voltage of the vector is 1.200000, which does no
t reach within the 5 percent
of the rail voltage 1.000000. (LBDB-668)
```

LBDB-669 (error) The final signal voltage of the %s is %g and it does not reach beyond the 2nd slew threshold voltage, which is %g for the %s.

DESCRIPTION

For each output_current_rise/fall vector, the final signal voltage must reach the 2nd slew threshold(i.e., the maximum of the slew thresholds for the output_current_rise vectors, and the minimum of the slew thresholds for the output_current_fall vectors) This can be described with the following formulas:

If output_signal_level_low and output_signal_level_high are specified, volt_low = output_signal_level_low; volt_high = output_signal_level_high; Else volt_low = VSS; volt_high = VDD;

1. For the output_current_rise vector, Vfinal = volt_low + (0.5/Cout)*(I2+I1)*(T2-T1)+...+(0.5/Cout)*(In+In-1)*(Tn-Tn-1) Verr = volt_low + MAX(slew_lower_threshold_pct_rise, slew_upper_threshold_pct_rise, output_threshold_pct_rise) * (volt_high-volt_low) * 0.01

Vfinal must NOT be less than Verr. 2. For the output_current_fall vector, Vfinal = volt_high + (0.5/Cout)*(I2+I1)*(T2-T1)+...+(0.5/Cout)*(In+In-1)*(Tn-Tn-1) Verr = volt_low + MAX(slew_lower_threshold_pct_fall, slew_upper_threshold_pct_fall, output_threshold_pct_fall) * (volt_high-volt_low) * 0.01

Vfinal must NOT be greater than Verr.

WHAT NEXT

Check the library source file and correct the problem.

EXAMPLE MESSAGE

Error : Line 373, The final signal voltage of the vector is 0.800000 and it does no
t reach beyond the 2nd
slew threshold voltage, which is 1.000000 for the output_current_fall vector. (LBDB-669)

LBDB-670 (information) The '%s' has '%s' %s, which has less than %d significant digits.

DESCRIPTION

The values in the current/receiver_capacitance tables should have at least 4 significant digits. The value of intrinsic_resistance and intrinsic_capacitance should have at least 2 significant digits if there is no off channel resistance (i.e. greater than 1Mohm) in the library.

WHAT NEXT

Check the library source file and correct the problem.

EXAMPLES

```
      output_current_rise(current_template) {
...
        vector(current_template) {
           reference_time : 0.0961844;
           index_1("0");
```

```
           index_2("0.170393");
           index_3("0.254379, 0.295, 0.31, 0.325, 0.34, 0.355, 0.385, 0.4, 0.415, 0
.43, 0.445, 0.475, 0.543056");
           values("0.1234, 0.2345, 0.3456, 0.4567, 0.5678, 0.6789, 0.7890, 0.7891,
0.0001, 0.7892, 0.7893, 0.7894, 0.7895");
        }
...
    }
```

EXAMPLE MESSAGE

```
Information : Line 373, The 'vector' has 'values' 0.4,
which has less than 4 significant digits. (LBDB-670)
```

LBDB-671 (warning) The '%s' has %s adjacent '%s' (%.8g, %.8g).

DESCRIPTION

The adjacent 'values' in the vectors fo the outpur_current_rise/fall tables are identical.

WHAT NEXT

Check the library source file and correct the problem.

EXAMPLES

```
      output_current_rise(current_template) {
...
        vector(current_template) {
           reference_time : 0.0961844;
           index_1("0");
           index_2("0.170393");
           index_3("0.254379, 0.295, 0.31, 0.325, 0.34, 0.355, 0.385, 0.4, 0.415, 0
.43, 0.445, 0.475, 0.543056");
           values("0.1234, 0.2345, 0.2345, 0.4567, 0.5678, 0.6789, 0.7890, 0.7891,
0.0001, 0.7892, 0.7893, 0.7894, 0.7895");
        }
...
    }
```

EXAMPLE MESSAGE

```
Error : Line 373, The 'vector' has identical adjacent 'values' (0.2345, 0.2345). (L
BDB-671)
```

LBDB-672 (information) There are more than 1 operating_conditions defined in the library.

DESCRIPTION

The message is to notify users that there are more than 1 operating_conditions defined in the library. For each library, only 1 operating_condtions group is necessary since it defined the pvt used for characterizing the library, and this operating_condtion is also the "default_operating_conditions" of the library.

LBDB-673 (warning) The timing arc does not have full receiver modeling information.

DESCRIPTION

This message indicates that the timing arc does not have all the following receiver modeling information: receiver_capacitance1_rise, receiver_capacitance1_fall, receiver_capacitance2_rise, receiver_capacitance2_fall

Although it is usually valid to specify only half of the receiver modeling information for the half-nate timing arcs. However, in some corner cases, we may need the full receiver modeling information.

In the following example,the receiver_capacitance1_fall group and the receiver_capacitance2_fall group are not specified for the half-unate timing arc.

```
 timing() {
   timing_type : rising_edge;
   timing_sense : positive_unate;
   ...
   receiver_capacitance1_rise(basic_template_8x7) {
                index_1 ("0, 0.00081298, 0.0188997, 0.0460298, 0.0912466, 0.18168,
0.452981, 0.905149");
                index_2 ("0.019368, 0.049573, 0.0948806, 0.170393, 0.321418, 0.7744
94, 1.52962");
                values ("0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211
, 0.00166425, 0.00167038",
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211, 0.0
0166425, 0.00167038",
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211, 0.0
0166425, 0.00167038",
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211, 0.0
0166425, 0.00167038",
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211, 0.0
0166425, 0.00167038",
```

```
                  "0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211, 0.0
0166425, 0.00167038",
                  "0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211, 0.0
0166425, 0.00167038",
                  "0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211, 0.0
0166425, 0.00167038");
   }
   receiver_capacitance2_rise(basic_template_8x7) {
               index_1 ("0, 0.00081298, 0.0188997, 0.0460298, 0.0912466, 0.18168,
0.452981, 0.905149");
               index_2 ("0.019368, 0.049573, 0.0948806, 0.170393, 0.321418, 0.7744
94, 1.52962");
               values ("0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211
, 0.00166425, 0.00167038",
                  "0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211, 0.0
0166425, 0.00167038",
                  "0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211, 0.0
0166425, 0.00167038",
                  "0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211, 0.0
0166425, 0.00167038",
                  "0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211, 0.0
0166425, 0.00167038",
                  "0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211, 0.0
0166425, 0.00167038",
                  "0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211, 0.0
0166425, 0.00167038",
                  "0.00165664, 0.00165664, 0.00165936, 0.00166126, 0.00166211, 0.0
0166425, 0.00167038");
   }
   ...
 }

 Warning: Line 673, The timing arc does not have full receiver modeling information
. (LBDB-390)
```

WHAT NEXT

If possoble, add the missing receiver modeling information in the library.

LBDB-674 (information) The 1st %s/%s index of timing arc '%s' are %g, %g which are larger than recommended %g, %g.

DESCRIPTION

This information occurs when the 1st index values of the timing arc are larger than the recommended values.

WHAT NEXT

Make sure the 1st index values are not larger than the recommended.

EXAMPLES

```
cell_rise(template) {
    index_1("1.0 ,2.0,4.0,6.0,10.0"); /* total_output_net_capacitance */
    index_2("0.362,0.725,1.087,1.449,1.812"); /* input_transition_time */
    ...
}
```

EXAMPLE MESSAGE

```
Information: Line 20068, The 1st total_output_net_capacitance/
input_transition_time index of timing arc
       'cell_rise' are 1.0, 0.362 which are larger than recommended 0, 0.  (LBDB-
674)
```

LBDB-675 (information) The 1st %s index of timing arc '%s' is %g, which is larger than recommended %g.

DESCRIPTION

This information occurs when the 1st index value of the timing arc is larger than the recommended value.

WHAT NEXT

Make sure the 1st index value is not larger than the recommended.

EXAMPLES

```
cell_rise(template) {
    index_1("1.0 ,2.0,4.0,6.0,10.0"); /* total_output_net_capacitance */
    ...
}
```

EXAMPLE MESSAGE

```
Information: Line 20068, The 1st total_output_net_capacitance index of timing arc
       'cell_rise' is 1.0, which is larger than recommended 0.  (LBDB-675)
```

LBDB-676 (information) The significant digits of values in timing arc '%s' is %d,

which is less than recommended %d.

DESCRIPTION

This information occurs when the significant digits of values in the specified table is less than the recommended number.

WHAT NEXT

Make sure the significant digits is not less than the recommended.

EXAMPLES

```
cell_rise(template) {
    ...
    values("0.459,0.651,0.843,1.034,1.225",
    ...);
}
```

EXAMPLE MESSAGE

```
Information: Line 454, The significant digits of values in timing arc 'cell_rise' i
s 4,
       which is less than recommended 5. (LBDB-676)
```

LBDB-677 (warning) The table size of timing arc '%s' is %dx%d, which is less than recommended %dx%d.

DESCRIPTION

This information occurs when the table size is less than the recommended number.

WHAT NEXT

Make sure the table size is not less than the recommended.

EXAMPLES

```
cell_rise(template) {
    index_1("1.0 ,2.0,4.0,6.0,10.0"); /* total_output_net_capacitance */
    index_2("0.362,0.725,1.087,1.449,1.812"); /* input_transition_time */
    ...
}
```

EXAMPLE MESSAGE

```
Warning: Line 446, The table size of timing arc 'cell_rise' is 5x5,
        which is less than recommended 7x7. (LBDB-677)
```

LBDB-678 (warning) The table size of timing arc '%s' is %d, which is less than recommended %d.

DESCRIPTION

This information occurs when the table size is less than the recommended number.

WHAT NEXT

Make sure the table size is not less than the recommended.

EXAMPLES

```
  cell_rise(template) {
      index_1("1.0 ,2.0,4.0,6.0,10.0"); /* total_output_net_capacitance */
      ...
  }
```

EXAMPLE MESSAGE

```
Warning: Line 446, The table size of timing arc 'cell_rise' is 5,
        which is less than recommended 7. (LBDB-678)
```

LBDB-679 (error) Can not find the %s of the %s pin '%s'.

DESCRIPTION

This information occurs when pin's max_capacitance/min_capacitance or the related_pin's max_transition information can not be found.

WHAT NEXT

Make sure the max_transition/max_capacitance/min_capacitance information are defined in the source .lib file.

EXAMPLES

```
  cell ( INV ) {
    area : 1 ;
```

```
    pin ( A ) {
      direction : input ;
      capacitance : 1 ;
      fanout_load : 1 ;
      ...
    }
    pin ( Z ) {
      related_pin :  A ;
      direction : output ;
      capacitance : 1 ;
      fanout_load : 1 ;
      ...
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 446, Can not find the max_transition of the input pin 'A'. (LBDB-679)
Error: Line 446, Can not find the min_capacitance of the  pin 'Z'. (LBDB-679)
Error: Line 446, Can not find the max_capacitance of the  pin 'Z'. (LBDB-679)
```

LBDB-680 (warning) The max value of %s index of group '%s' is %g,
which is less than max %s of pin '%s', %g.

DESCRIPTION

This information occurs when the max value of the specified index is less than the max constraint for the pin.

WHAT NEXT

Make sure the max index value is not less than the constraint.

EXAMPLES

```
   pin(y) {
     direction   : input;
     min_capacitance : 0.361;
     max_capacitance : 1.813;
     max_transition : 0.5;
     cell_rise(template) {
       index_2("0.362,0.725,1.087,1.449,1.812"); /* total_out_net_cap  */
       ...
     }
     ...
   }
```

EXAMPLE MESSAGE

```
Warning: Line 762, The max value of total_out_net_cap index of timing arc 'cell_ris
e' is 1.812,
        which is less than max total_out_net_cap of pin 'y', 1.813. (LBDB-680)
```

LBDB-681 (warning) The min value of %s index of timing arc '%s' is %g,
which is bigger than min %s of pin '%s', %g.

DESCRIPTION

This information occurs when the min value of the specified index is larger than the min constraint for the pin.

WHAT NEXT

Make sure the min index value is not larger than the constraint.

EXAMPLES

```
pin(y) {
  direction   : input;
  min_capacitance : 0.361;
  max_capacitance : 1.813;
  max_transition : 0.5;
  cell_rise(template) {
    index_2("0.362,0.725,1.087,1.449,1.812"); /* total_out_net_cap  */
    ...
  }
  ...
}
```

EXAMPLE MESSAGE

```
Warning: Line 762, The min value of total_out_net_cap index of timing arc 'cell_ris
e' is 0.362,
        which is larger than min total_out_net_cap of pin 'y', 0.361. (LBDB-681)
```

LBDB-682 (warning) The values in timing arc '%s' are non monotonous %g, %g,

when %s = %g.

DESCRIPTION

This information occurs when the delay values in specified table do not increase monotonously with increasing capacitance.

WHAT NEXT

Make sure the delay values increase monotonously with increasing capacitance.

EXAMPLES

```
  cell_rise(template) {
      index_1("1.0 ,2.0,4.0,6.0,10.0"); /* input_transition_time */
      index_2("0.362,0.725,1.087,1.449,1.812"); /* total_output_net_capacitance */
      values ("1.405, 1.116...")
  }
```

EXAMPLE MESSAGE

```
Warning: Line 762, The values in timing arc 'cell_rise' are non monotonous 1.405, 1
.116,
        when input_net_transition = 1.   (LBDB-682)
```

LBDB-683 (warning) The table is a load independent table.

DESCRIPTION

This information occurs when the template of one table do not have the total_output_net_capacitance index where it is needed.

WHAT NEXT

Make sure the table use the correct template which is with total_output_net_capacitance index.

EXAMPLES

```
 lu_table_template(transition1x5){
    variable_1 : input_net_transition;
    index_1("0.5,1.0,1.5,2.0,2.5");
 }
 ...
 cell (AND) {
   pin(y) {
     ...
```

```
    cell_rise(transition1x5) {
      index_1("0.362,0.725,1.087,1.449,1.812"); /* input_net_transition  */
      ...
    }
    ...
  }
  ...
}
```

EXAMPLE MESSAGE

```
Warning: Line 762, The table is a load independent table. (LBDB-683)
```

LBDB-684 (warning) The table is a scalar table.

DESCRIPTION

This information occurs when the template of one table do not have any index where it is needed.

WHAT NEXT

Make sure the table use the correct template which is with index.

EXAMPLES

```
lu_table_template(scalar_template){
}
...
cell (AND) {
  pin(y) {
    ...
    cell_rise(scalar_template) {
       values ("...");
    }
    ...
  }
  ...
}
```

EXAMPLE MESSAGE

```
Warning: Line 762, The table is a scalar table. (LBDB-684)
```

LBDB-685 (warning) The voltage range of %s is %g->%g,

which is less than recommended %g->%g.

DESCRIPTION

This information occurs when the range of voltage index for IV curves is less than the recommended.

WHAT NEXT

Make sure the voltage range is not less than the recommended.

EXAMPLES

```
     ...
   iv_lut_template ("LUT_TEMPLATE_13570_t") {
variable_1 : "iv_output_voltage";
index_1("-1.500000, -0.611850, -
0.019800, 0.009900, 0.246750, 0.868350, 1.016400, 1.578900, 2.526300, 3.000000");
   }
     ...
    timing () {
      steady_state_current_low ("LUT_TEMPLATE_13570_t") {
                  values("-1.500000, -0.611850, -
0.019800, 0.009900, 0.246750, 0.868350, 1.016400, 1.578900, 2.526300, 3.000000");
      }
    }
```

EXAMPLE MESSAGE

```
Warning: Line 780, The voltage range of steady_state_current_low is -1.5->3,
        which is less than recommended -5->10. (LBDB-685)
```

LBDB-686 (warning) There is potential extrapolation problem %s[%g, %g, %g]=%g (> %g).

DESCRIPTION

This information occurs when the noise value extrapolated with the boundary values is larger than the recommended zero value.

WHAT NEXT

Make sure the boundary values in the table correct.

EXAMPLES

```
  propagated_noise_width_below_low(my_noise_propagation){
      index_1("0.00250, 0.00500, 0.01000, 0.01500, 0.02500, 0.03750, 0.05000"); /
*total_output_net_capacitance*/
      index_2("0.400,1.000,1.500,2.000"); /*input_noise_width*/
      index_3("0.36000,0.54000,0.72000,0.90000");
      values("0.025, 0.024, 0.010, 0.013",
             "1.071, 0.342, 0.121, 0.222",
             "0.489, 0.565, 0.789, 0.750",
             "0.282, 0.021, 0.279, 0.118",
             "0.034, 0.042, 0.009, 0.015",
             "1.068, 0.346, 0.121,...");
  }
```

EXAMPLE MESSAGE

```
Warning: Line 215, There is potential extrapolation problem
        Width[0.05, 1, 0]=0.376 (> 0.1). (LBDB-686)
```

LBDB-687 (warning) There is potential extrapolation problem %s[%g, %g]=%g (> %g).

DESCRIPTION

This information occurs when the noise value extrapolated with the boundary values is larger than the recommended zero value.

WHAT NEXT

Make sure the boundary values in the table correct.

EXAMPLES

```
  propagated_noise_width_below_low(my_noise_propagation){
      index_1("0.400,1.000,1.500,2.000"); /*input_noise_width*/
      index_2("0.36000,0.54000,0.72000,0.90000");
      values("0.025, 0.024, 0.010, 0.013",
             "1.071, 0.342, 0.121, 0.222",
             "0.489, 0.565, 0.789, 0.750",
             "0.282, 0.021, 0.279, 0.118");
```

```
  }
```

EXAMPLE MESSAGE

```
Warning: Line 215, There is potential extrapolation problem
        Width[1, 0]=2.529 (> 0.1). (LBDB-687)
```

LBDB-688 (warning) The curve is curling upwards at the end. when total_output_net_capacitance=%g.

DESCRIPTION

This information occurs when the immunity curve curls upwards at the end of the curve.

WHAT NEXT

Make sure each last 2 values with the same total_output_net_capacitance index are almost identical.

EXAMPLES

```
  noise_immunity_high (my_noise_reject) {
    values ("1.3, 0.8, 0.7, 0.6, 0.55",
            "1.5, 0.9, 0.8, 0.65, 0.6",
            "1.5, 0.9, 0.8, 0.65, 0.6",
            "1.5, 0.9, 0.8, 0.65, 0.6",
            "-1.5, 1.9, 0.8, 0.65, 0.6") ;
  }
```

EXAMPLE MESSAGE

```
Warning: Line 178, The curve is curling upwards at the end.
        when total_output_net_capacitance=0.1. (LBDB-688)
```

LBDB-689 (warning) The curve is not leveling off at the end. when total_output_net_capacitance=%g.

DESCRIPTION

This information occurs when the immunity curve is not leveling off at the end.

WHAT NEXT

Make sure each last 2 values with the same total_output_net_capacitance index are almost identical.

EXAMPLES

```
  noise_immunity_high (my_noise_reject) {
    values ("1.3, 0.8, 0.7, 0.6, 0.55",
            "1.5, 0.9, 0.8, 0.65, 0.6",
            "1.5, 0.9, 0.8, 0.65, 0.6",
            "1.5, 0.9, 0.8, 0.65, 0.6",
            "-1.5, 1.9, 0.8, 0.65, 0.6") ;
  }
```

EXAMPLE MESSAGE

```
Warning: Line 178, The curve is not leveling off at the end.
        when total_output_net_capacitance=0. (LBDB-689)
```

LBDB-690 (error) The current polarity is reversed.

DESCRIPTION

This information occurs when the current polarity is reversed.

WHAT NEXT

Make sure the skew of the current at middle point is correct.

EXAMPLES

```
  steady_state_current_low(my_current_low) {
    values("0.1, 0.05, 0, -0.1, -0.25, -1, -1.8");
  }
```

EXAMPLE MESSAGE

```
Error: Line 198, The current polarity is reversed. (LBDB-690)
```

LBDB-691 (error) There is negative values in the table.

DESCRIPTION

This information occurs when the value in the table is negative where it should be

positive.

WHAT NEXT

Make sure the values in the table are positive.

EXAMPLES

```
  propagated_noise_height_below_low(my_noise_propagation){
  ...
  values ("-1.4 ..");
```

EXAMPLE MESSAGE

```
Error: Line 198, There is negative values in the table. (LBDB-691)
```

LBDB-692 (warning) The max height of the noise table %s is %g, which is less than recommended %g.

DESCRIPTION

This information occurs when the max height of the noise table is less than the recommended.

WHAT NEXT

Make sure the max height is not less than the recommended.

EXAMPLES

```
   propagated_noise_height_below_low(my_noise_propagation){
                index_1("0.00250, 0.00500, 0.01000, 0.01500, 0.02500, 0.03750, 0.05
000");
                index_2("0.400,1.000,1.500,2.000");
                index_3("0.36000,0.54000,0.72000,0.90000"); /*input_noise_height*/
```

EXAMPLE MESSAGE

```
Warning: Line 248, The max height of the noise table propagated_noise_height_below_
low is 0.9,
        which is less than recommended 5. (LBDB-692)
```

LBDB-693 (warning) The max width of the noise table %s is %g,

which is less than recommended %g.

DESCRIPTION

This information occurs when the max width of the noise table is less than the recommended.

WHAT NEXT

Make sure the max width is not less than the recommended.

EXAMPLES

```
   propagated_noise_height_below_low(my_noise_propagation){
                index_1("0.00250, 0.00500, 0.01000, 0.01500, 0.02500, 0.03750, 0.05
000");
                index_2("0.400,1.000,1.500,2.000"); /*input_noise_width*/
                index_3("0.36000,0.54000,0.72000,0.90000");
```

EXAMPLE MESSAGE

```
Warning: Line 281, The max width of the noise table propagated_noise_width_low is 2,
        which is less than recommended 4. (LBDB-693)
```

LBDB-694 (warning) The width range of %s is %g->%g, which is less than recommended %g->%g.

DESCRIPTION

This information occurs when the width index does not have enough range.

WHAT NEXT

Make sure the width index have the enough range.

EXAMPLES

```
  noise_immunity_above_high (my_noise_reject_outside_rail) {
    index_1("0, 0.1, 2"); /*input_noise_width*/
    values ("1, 0.8, 0.5",
            "1, 0.8, 0.5",
            "1, 0.8, 0.5");
  }
```

EXAMPLE MESSAGE

```
Warning: Line 192, The width range of noise_immunity_above_high is 0->2,
        which is less than recommended 2->4. (LBDB-694)
```

LBDB-695 (error) The pin '%s' misses DC noise margin.

DESCRIPTION

This information occurs when one pin does not DC noise margin information.

WHAT NEXT

Make sure there is DC noise margin information defined in one pin if no other noise information.

EXAMPLES

```
pin(a) {
            direction   : input;
            capacitance : 1.000;
}
```

EXAMPLE MESSAGE

```
Error: Line 794, The pin 'a' misses DC noise margin. (LBDB-695)
```

LBDB-696 (warning) The timing arc misses noise %s information.

DESCRIPTION

This information occurs when the timing arc does not have specified noise information.

WHAT NEXT

Make sure there is complete noise information defined in the timing arc.

EXAMPLE MESSAGE

```
Warning: Line 137, The timing arc misses noise propagated_noise_width_high informat
ion. (LBDB-696)
```

LBDB-697 (warning) The timing arc %s->%s misses noise %s_%s information.

DESCRIPTION

This information occurs when the timing arc does not have specified noise information.

WHAT NEXT

Make sure there is complete noise information defined in the timing arc.

EXAMPLE MESSAGE

```
Warning: Line 137, The timing arc DA[0]-
>QB[0] misses noise propagated_noise_width_above_high information. (LBDB-697)
```

LBDB-698 (warning) The values in noise table '%s' are non monotonous
%g, %g, when %s = %g, %s = %g.

DESCRIPTION

This information occurs when the delay values in specified table do not decrease monotonously with increasing capacitance.

WHAT NEXT

Make sure the delay values decrease monotonously with increasing capacitance.

EXAMPLES

```
            propagated_noise_width_below_low(my_noise_propagation){
                index_1("0.00250, 0.00500, 0.01000, 0.01500, 0.02500, 0.03750, 0.05
000");
                index_2("0.400,1.000,1.500,2.000");
                index_3("0.36000,0.54000,0.72000,0.90000");
                values("0.000, 0.024, 0.010, 0.013",
                        "1.071, 0.342, 0.121, 0.222",
                        "0.489, 0.565, 0.789, 0.750",
                        "0.282, 0.021, 0.279, 0.118",
                        "1.000, 0.042, 0.009, 0.015",
                        "1.068, 0.346, 0.121, 0.248",
                        "0.497, 0.584, 0.786, 0.777",
                        "0.271, 0.029, 0.281, 0.120",
```

```
                    "0.055, 0.074, 0.008, 0.017",
                    "1.076, 0.356, 0.121, 0.306",
                    "0.481, 0.612, 0.783, 0.778",
                    "0.257, 0.045, 0.288, 0.103",
                    "0.072, 0.102, 0.006, 0.018",
                    "1.098, 0.367, 0.121, 0.359",
                    "0.506, 0.646, 0.779, 0.770",
                    "0.248, 0.057, 0.295, 0.105",
                    "0.102, 0.161, 0.002, 0.018",
                    "1.162, 0.392, 0.118, 0.437",
                    "0.571, 0.707, 0.775, 0.763",
                    "0.238, 0.076, 0.311, 0.107",
                    "0.142, 0.202, 0.002, 0.059",
                    "0.389, 0.426, 0.102, 0.541",
                    "0.673, 0.775, 0.772, 0.768",
                    "0.235, 0.094, 0.329, 0.109",
                    "0.180, 0.246, 0.005, 0.071",
                    "0.434, 0.463, 0.090, 0.644",
                    "0.705, 0.835, 0.758, 0.783",
                    "0.235, 0.108, 0.345, 0.111");
          }
```

EXAMPLE MESSAGE

```
Warning: Line 248, The values in noise table 'propagated_noise_height_below_low' ar
e non monotonous
        0.025, 1.000, when input_noise_width = 0.4, input_noise_height = 0.36. (LBD
B-698)
```

LBDB-699 (error) The 'generic' integrated clock gating cell '%s' should only have at most 1 inout/output pin with attribute 'clock_gate_out_pin' set to true.

DESCRIPTION

This message indicates that you specified the 'generic' integrated gating clock cell can only have 1 inout/output pin with 'clock_gate_out_pin : true'.

WHAT NEXT

Change the library source file.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "generic";
  ...
```

```
  pin(O1) {
                direction : output;
                clock_gate_out_pin : true;
...
  }
  pin(O2) {
                direction : output;
                clock_gate_out_pin : true;
...
  }
  ...
}

The modified cell description can be :

cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "generic";
  ...
  pin(O1) {
                direction : output;
                clock_gate_out_pin : true;
...
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The 'generic' integrated clock gating cell 'CGNP' should only have
 at most 1 inout/output pin with

attribute 'clock_gate_out_pin' set to true. (LBDB-699)
```

LBDB-700 (error) The pin '%s' of the 'generic' integrated clock gating cell '%s' can not define attribute 'state_function'. It should use attribute 'function" instead.

DESCRIPTION

```
This message indicates that you specified attribute 'state_function' in the
'generic' integrated gating clock cell. It should be changed as 'function'.
```

WHAT NEXT

```
Change the library source file by replacing "state_function" to "function".
```

EXAMPLES

```
cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "generic";
  ...
  pin(O1) {
                direction : output;
state_function : "!(IQ + SE) * CP_IN"
...
  }
  ...
}
```

The modified cell description can be :

```
cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "generic";
  ...
  pin(O1) {
                direction : output;
function : "!(IQ + SE) * CP_IN"
...
  }
  ...
}
```

EXAMPLE MESSAGE

Error: Line 206, The pin ’O1’ of the ’generic’ integrated clock gating cell ’CGNP’ can not define

attribute ’state_function’. It should use attribute ’function" instead. (LBDB-700)

LBDB-701 (error) The %scell ’%s’ can not define pin functions of both ’%s’ and ’%s’.

DESCRIPTION

Assume the integrated clock gating cell is modeled as :

... clock_gating_integrated_cell : "generic"; latch("IQ", "IQN") { data_in : "EN1 * EN2" ; enable : "CLK’" ; } ...

This message indicates that you specified pin functions for either one of the following 2 cases, which is invalid: 1. the same pin function with both IQ and IQN. for example, pin(Y1) { function : "IQ * (A + IQN)"; ... }

2. the different pin functions involved with IQ and IQN. for example, pin(Y1) {

```
function : "IQ * A"; ... } pin(Y2) { function : "IQN * A"; ... }
```

WHAT NEXT

Change the library source file by replacing "IQN" to "IQ'".

EXAMPLE MESSAGE

```
Error: Line 206, The integrated clock gating cell '%s' can not define pin functions
 of both '%s' and '%s'. (LBDB-701)
```

LBDB-702 (error) The cell should not define the 'statetable' group.
It should use 'ff' group or 'latch' group instead.

DESCRIPTION

This message indicates that you specified statetable and the pin function of "...IQ..." or "...IQN..."(excluding "IQ" and IQN", where IQ and IQN are the outptut of sequential element. You should define 'ff/latch' group instead.

WHAT NEXT

Change the library source file, and replace the statetable group with the ff/latch group of the specified cell.

EXAMPLES

```
cell(A) {
  area : 1;
  ...
  statetable(" CP EN ", "IQ ") {
     table : " L  L  : - : L ,
               L  H  : - : H ,
               H  -  : - : N ";
  }

  pin(Y) {
function : "IQ * CP";
...
  }
  ...
}
```

The modified cell description should be :

```
cell(A) {
```

```
  area : 1;

  latch("IQ","IQN") {
    enable : "CP'";
    data_in : "EN";
  }
  ...
  pin(Y) {
function : "IQ * CP";
...
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The cell should not define the 'statetable' group.
It should use 'ff' group or 'latch' group instead. (LBDB-702)
```

LBDB-703 (error) An invalid %s '%s' is found in the '%s' group.

DESCRIPTION

The message is to notify users that either the attribute/group should not be defined in the relative parent group, or the value of the attribute/group need to be corrected.

WHAT NEXT

Remove the attribute/group or correct the value of the attribute/group and rerun the command.

LBDB-704 (error) The standard cells '%s' and '%s' does not have the same pg_pin configuration.

DESCRIPTION

The message is to notify users that all the standard cells(cells having 1 primary_power pg_pin and 1 primary_ground pg_pin) should have exactly the same pg_pin configuration: - all the primrary_power pg_pins of these cells have the same "voltage_name" - all the primrary_ground pg_pins of these cells have the same "voltage_name"

WHAT NEXT

Correct the "voltage_name" attribute values of the pg_pins of the standard cells and rerun the command.

LBDB-705 (warning) The '%s' %s group has been defined multiple times in the '%s' %s group. Using the last definition encountered.

DESCRIPTION

The library contains more than one definition of a group. The Library Compiler issues this error message, ignores the previous definitions, and takes into consideration the last definition encountered.

WHAT NEXT

Change the group name if it is wrong, or delete the second definition.

EXAMPLES

```
    cell(sample) {
...
pg_pin(A) {
  ...
}
pg_pin(A) {
  ...
}
...
    }
```

EXAMPLE MESSAGE

Warning: Line 50, The 'A' pg_pin group has been defined multiple times in the 'sample' cell group. Using the last definition encountered. (LBDB-705)

LBDB-706 (error) Cell '%s', pin '%s', the CCS Noise data cannot be compiled successfully.

DESCRIPTION

This error message occurs when the CCS Noise data defined cannot be compiled successfully for the Synopsys timing tools to perform the CCS Noise computation.

WHAT NEXT

Change the CCS Noise data accordingly.

LBDB-707 (information) Compiling CCS Noise data --- %%d...

DESCRIPTION

This message is for information purposes only and it is to show the process of compiling CCS Noise data.

EXAMPLE MESSAGE

```
Information: Compiling CCS Noise data --- 10%... (LBDB-707)
Information: Compiling CCS Noise data --- 20%... (LBDB-707)
Information: Compiling CCS Noise data --- 100%... (LBDB-707)
```

LBDB-708 (error) The timing arc has ’%s’ timing_sense, which is not consistent with the "is_inverting" attribute value(s) of its ccsn_first_stage/ ccsn_last_stage group(s).

DESCRIPTION

This message is to indicate that the "is_inverting" attribute value of the ccsn_first_stage/ccsn_last_stage group(s) defined in the timing arc is not consistent with the timing_sense of the arc.

The correct configuration should be: 1. If the timing sense is "positive_unate", then it can only contain either 1 ccsn_first_stage with "FALSE" "is_inverting" attribute, or 1 ccsn_first_stage with "TRUE" "is_inverting" attribute and 1 ccsn_last_stage with "TRUE" "is_inverting" attribute, or 1 ccsn_first_stage with "FALSE" "is_inverting" attribute and 1 ccsn_last_stage with "FALSE" "is_inverting" attribute. 2. If the timing sense is "negative_unate", then it can only contain either 1 ccsn_first_stage with "TRUE" "is_inverting" attribute, or 1 ccsn_first_stage with "TRUE" "is_inverting" attribute and 1 ccsn_last_stage with "FALSE" "is_inverting" attribute, or 1 ccsn_first_stage with "FALSE" "is_inverting" attribute and 1 ccsn_last_stage with "TRUE" "is_inverting" attribute.

EXAMPLE MESSAGE

```
Error: Line 50, The timing arc has ’negative_unate’ timing_sense, which is not
consistent with the "is_inverting" attribute values of its ccsn_first_stage/
ccsn_last_stage group(s). (LBDB-708)
```

LBDB-709 (error) The sequential timing arc cannot define the '%s' group.

DESCRIPTION

This message is to indicate that a sequential timing arc cannot have ccsn_first_stage/ccsn_last_stage group.

EXAMPLE MESSAGE

Error: Line 50, The sequential timing arc cannot define the 'ccsn_first_stage' group. (LBDB-709)

LBDB-710 (error) The table size of '%s' is %dx%d, which is less than the required %dx%d.

DESCRIPTION

This information occurs when the table size is less than the required number.

WHAT NEXT

Make sure the table size is not less than the recommended.

EXAMPLES

```
dc_current(template) {
    index_1("1.0") ; /* input_voltage */
    index_2("0.362"); /* output_voltage */
    ...
}
```

EXAMPLE MESSAGE

```
Warning: Line 446, The table size of 'dc_current' is 5x5,
        which is less than the required 6x6. (LBDB-710)
```

LBDB-711 (error) Cell '%s', pin '%s', a %s pin cannot specify the

’%s’ %s.

DESCRIPTION

This error message occurs when there is a mismatch between the direction of a pin and the CCS Noise data. Library Compiler fails if the following rules are not satisfied:

1. An input pin can only specify at least 1 ccsn_first_stage group.

2. An inout pin can specify both ccsn_first_stage group and ccsn_last_stage group.

3. An output pin can only specify ccsn_last_stage group.

WHAT NEXT

Check the library source file and fix either the invalid CCS Noise data, or the direction of the pin.

EXAMPLES

The following is an example of incorrect input that causes this error message:

```
cell(lbdb711) {
  ...
  pin(Y ) {
    direction : output;
    ...
    ccsn_first_stage() {
...
    }
  }
}
```

In this case, the Y pin has the ccsn_first_stage group specified. To fix the error, change ccsn_first_stage to ccsn_last_stage.

LBDB-712 (warning) an %s pin should either specify at least one non-static
’%s’ in the pin group or specify noise data for all of its timing

arcs.

DESCRIPTION

This warning message occurs because an inout or output pin should have at least 1 non-static ccsn_last_stage group in the pin group or define non-static ccs noise last stage data for all of its timing groups.

A static CCS noise model captures the behaviors of a static CCB (channel connected block). A static CCB refers to a CCB that does not have any input terminal or the voltage level at the input terminal does not affect the output current of the CCB. For example, a static CCS noise model can be characterized for a CMOS NAND gate when both inputs are tied to ground. Such static CCS noise models can be used in noise analysis with case analysis, but they cannot be used for propagating crosstalk delay or noise waveforms through the cell under study. See the *Make CCS Noise User Guide* for detailed information.

WHAT NEXT

This is only a warning message. No action is required.

However, you can do any of the following:

• Check the library source file and fix either the invalid CCS Noise data, or the direction of the pin.

• Safely ignore this warning if the following three categories of cells are identified in a library:

• inverters: A cell always has 1 input pin and 1 output pin with the function as "!input" or "input’"

• NAND: A cell always has 2 input or more and 1 output pin with the function as "!(input1 * input2 * ... input(n))" or "(input1 * input2 * ... input(n))’"

• NOR: A cell always has 2 input or more and 1 output pin with the function as "!(input1 + input2 + ... input(n))" or "(input1 + input2 + ... input(n))’"

Ignore this warning if the current cell belongs to the three categories of cells above.

EXAMPLES

The incorrect input below causes this warning message:

```
cell(good) {
  ...
  pin(Y ) {
    direction : output;
    ...
    ccsn_last_stage() {
```

```
      ...
         }
         }
       }
     }
     cell(lbdb712) {
       ...
       pin(Y ) {
         /* no ccs noise information inside the pin group */
         direction : output;
         ...
         /* not all timing arcs inside the pin group has ccs noise data */
       }
     }
```

In this example, the Y pin does not have the ccsn_last_stage group specified. To fix the problem, add the ccsn_last_stage group into the pin group.

LBDB-713 (error) The ’%s’ group wth %s ’%s’ attribute cannot specify ’%s’ %s.

DESCRIPTION

This message can be used to indicate that if a ccsn_first_stage/ccsn_last_stage group has ’is_needed’ attribute set to FALSE, then it is not valid to specify the following CCS Noise data: stage_type, is_inverting, miller_cap_rise, miller_cap_fall, dc_current, output_voltage_rise, output_voltage_fall, propagated_noise_low, propagated_noise_high.

WHAT NEXT

Check the library source file, and remove the redundant CCS Noise data.

EXAMPLES

```
  cell(bad) {
    ...
    pin(Y ) {
      direction : output;
      ...
ccsn_last_stage() {
is_needed : FALSE;
stage_type : both
...
}
      }
    }
  }
```

In this case, the ’Y’ pin does not have the ’ccsn_last_stage’ group specified. To fix the problem, add the ’ccsn_first_stage’ group into the pin group.

EXAMPLE MESSAGE

Error: Line 71, The ’ccsn_last_stage’ group with FALSE ’is_needed’ attribute cannot specify ’stage_type’ attribute. (LBDB-713)

LBDB-714 (error) The ’%s’ group cannot specify the ’%s’ attribute with value ’%s’.

DESCRIPTION

This message can be used to indicate that the output pin of a tie-off cell(pin function= "1" | "0", or driver_type = "pull_up" | "pull_down") specify incorrect value for the stage_type attribute of the ccsn_first_stage/ccsn_last_stage groups defined on the pin, which must satisfy the following rules: 1. If the driver pin with driver_type = pull_up or function = "1", then its ccsn_first_stage/ ccsn_last_stage group must have the stage_type attribute with value "PULL_UP". 2. If the driver pin with driver_type = pull_down or function = "0", then its ccsn_first_stage/ccsn_last_stage group must have the stage_type attribute with value "PULL_DOWN".

WHAT NEXT

Check the library source file, and correct the incorrect ’stage_type’ value.

EXAMPLES

```
  cell(bad) {
    ...
    pin(Y ) {
        direction : output;
        function : 1;
driver_type : "pull_up";
      ...
ccsn_last_stage() {
is_needed : FALSE;
stage_type : "pull_down";
...
}
      }
    }
  }
```

In this case, the ’Y’ pin specify ’pull_down’ stage_type attribute in its ’ccsn_last_stage’ group. To fix the problem, change the ’pull_down’ to ’pull_up’.

EXAMPLE MESSAGE

```
Error: Line 71, The 'ccsn_last_stage' group cannot specify the 'stage_type' attribu
te with value 'PULL_DOWN'. (LBDB-714)
```

LBDB-715 (error) The '%s' attribute has an invalid sequence of data '%g , %g'. The values must be in %s increasing order.

DESCRIPTION

This message indicates that the set of data is not specified in increasing order.

WHAT NEXT

Check your library and correct the order of the values.

EXAMPLES

```
  dc_current(template) {
/* index does not in monotically increasing order */
      index_1 ("0.1, 4.2, 2.3, 3.4");
      index_2 ("0.1, ...");
...
  }
```

EXAMPLE MESSAGE

```
Error: Line 22, The 'index_1' attribute has an invalid sequence of
data '4.200000 , 2.300000'. The values must be in
monotonically increasing order. (LBDB-715)
```

LBDB-716 (error) The %s %g of '%s' attribute is %s %s = %g.

DESCRIPTION

This message indicates that the first/last/some value of the specific attribute is greater than the upper bound value, or lower than the lower bound value.

WHAT NEXT

Check your library and correct the value.

LBDB-717 (error) The value %g of '%s' attribute is %s %g.

DESCRIPTION

This message indicates that the value of the specific attribute is greater than the upper bound value, or less than the lower bound value.

WHAT NEXT

Check your library and correct the value.

LBDB-718 (warning) The %s %g of '%s' attribute is %s %s = %g.

DESCRIPTION

This message indicates that the first/last/some value of the specific attribute is greater than the upper bound value, or lower than the lower bound value. Note that this is just a warning, not an error.

WHAT NEXT

Check your library and correct the value.

LBDB-719 (error) The cell must have at least 1 'primary_ground' pg_pin and at least 1 'primary_power' pg_pin.

DESCRIPTION

This error message occurs when a primary_ground pg_pin or a primary_power pg_pin is missing. Cell in the following list could occurs this message, if it doesn't have at least 1 primary_ground pg_pin and at least 1 primary_power pg_pin. (1) The cell is a macro cell. (2) The cell has function info. (except function ,Äú0,Äù or ,Äú1,Äù for tie-off cell) (3) The cell has timing/noise/power info.

WHAT NEXT

Add the missing primary_ground pg_pin or primary_power pg_pin and run the command again.

LBDB-720 (error) The ’%s’ %s cannot be specified in the library based on pg_pin.

DESCRIPTION

This message indicates that you specified the syntax(power_supply, rail_connection, input/output_signal_level, power_level, etc.) which is incompatible with the syntax based on pg_pin such as voltage_map, pg_pin, related_power/ground_pin, related_pg_pin).

WHAT NEXT

Refer to the "Library Compiler User Guide" for related information and emove the incompatible values,

EXAMPLES

```
cell(lbdb720) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1.0;

    input_signal_level : VDD;

    related_power_pin : VDD;
    related_ground_pin : VSS;

  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 84, The ’input_signal_level’ attribute cannot be specified in the libra
ry
based on pg_pin. (LBDB-720)
```

LBDB-721 (warning) The value %f of ’nom_voltage’ is not the same as the value %f of ’voltage’ of the default operating_conditions ’%s’.

DESCRIPTION

This message indicates that the nom_voltage valye is not equal to the value of "voltage" attribute of the default operating_conditions group of the library.

WHAT NEXT

Correct the nominal_voltage value to make it the same as the value of the voltage attribute of the default operating_conditions group.

EXAMPLES

```
nom_voltage     : 1.09;

operating_conditions(sample) {
  process     : 1;
  temperature : 85;
  voltage     : 1.08;
  tree_type   : balanced_tree
}
```

EXAMPLE MESSAGE

Warning: Line 52, The value 1.09 of 'nom_voltage' is not the same as the value 1.08 of 'voltage' of the default operating_conditions '%s'. (LBDB-721)

LBDB-722 (error) The voltage value %f of the 1st voltage_map '%s' is not the same as the value of 'voltage' of the default operating_conditions '%s'.

DESCRIPTION

This message indicates the 1st specified voltage_map attribute specifiy the different voltage value from that of the 'voltage' of the default operating_consitions group. They should be equal.

WHAT NEXT

Correct the voltage value of the 1st voltage_map.

EXAMPLES

```
voltage_map(VDD, 1.2);
voltage_map(VSS, 0);
operating_conditions(sample) {
process     : 1;
temperature : 85;
voltage     : 1.08;
tree_type   : balanced_tree
}
default_operating_conditions : sample;
```

In this case, the voltage value of the 1st voltage_map 'VDD1' voltage_map is 1.2, while the voltage valye of default operating_conditions 'sample' is 1.08. To Fix the problem, update the voltage_map 'VDD' as follows:

```
voltage_map(VDD, 1.08);
voltage_map(VSS, 0);
operating_conditions(sample) {
  process     : 1;
  temperature : 85;
  voltage     : 1.08;
  tree_type   : balanced_tree
}
default_operating_conditions : sample;
```

EXAMPLE MESSAGE

```
Error: Line 23, The voltage value 1.2 of the 1st voltage_map 'VDD' is not the same as

      the value of 'voltage' of the default operating_conditions 'sample'. (LBDB-722)
```

LBDB-723 (error) The last variable '%s' is '%s', which is wrong. The value must be "time".

DESCRIPTION

This message indicates that the value of the last variable can only be "time" in pg_current_template. pg_current_template can have one variable up to 4 variables, and input_net_transition, time, and total_output_net_capacitance are 3 avaiable values can be assigned. No matter what size of template is, the last variable must be "time".

WHAT NEXT

If the last variable is not "time", change the variable, which is assigned to "time", to the last.

EXAMPLES

```
pg_current_template(basic_template) {
  variable_1 : input_net_transition;
  variable_2 : time;
  variable_3 : total_output_net_capacitance;
  variable_4 : total_output_net_capacitance;
}
```

To fix the problem, exchange the values between variable_2 and variable_4.

EXAMPLE MESSAGE

```
Error: Line 388, The last variable variable_4 is total_output_net_capacitance,
        which is wrong.  The value must be "time". (LBDB-723)
```

LBDB-724 (error) There is no voltage_map defined for ground voltage value 0.

DESCRIPTION

This message indicates the library does not define the voltage_map for the ground voltage value 0. In the libraries based on the new power modeling syntax (voltage_map, pg_pin, ..., etc.), this condition myst be satisfied.

WHAT NEXT

Add the voltage_map for the ground voltage value 0.

EXAMPLES

```
      voltage_map(VDD, 1.08);
      voltage_map(VDD1, 1.1);

      operating_conditions(sample) {
      process     : 1;
      temperature : 85;
      voltage     : 1.08;
      tree_type   : balanced_tree
      }
      default_operating_conditions : sample;
```

In this case, there is no voltage_map defined for ground voltage value 0. To fix the problem, add the following voltage_map attribute at the library level:

```
      voltage_map(VDD, 1.08);
      voltage_map(VDD1, 1.1);
      voltage_map(VSS, 0);

      operating_conditions(sample) {
        process     : 1;
        temperature : 85;
        voltage     : 1.08;
        tree_type   : balanced_tree
      }
      default_operating_conditions : sample;
```

EXAMPLE MESSAGE

```
Error: Line 23, There is no voltage_map defined for ground voltage value 0. (LBDB-
724)
```

LBDB-725 (warning) Connect pin '%s' to the default %s pg_pin '%s'.

DESCRIPTION

Either the related_power_pin or the related_ground_pin attribute is missing in a pin within a multiple power supply cell. By default, LC connect this pin to the default related_power_pin/related_ground_pin.

WHAT NEXT

Check the library source file to see if you missed the related_power_pin or the related_ground_pin attributes.

EXAMPLES

```
   voltage_map(VDD0, 1.8);
   voltage_map(VDD1, 1.9);
   voltage_map(VDD2, 23);
   voltage_map(VSS, 0);

cell(lbdb428) {
  area : 2;
  pad_cell : true;
  pg_pin(PV1) {
    voltage_name : VDD1;
    pg_type : primary_power;
  }
  pg_pin(PV2) {
    voltage_name : VDD2;
    pg_type : primary_power;
  }
  pg_pin(VSS) {
    voltage_name : VSS;
    pg_type : primary_ground;
  }
  pin(A) {
    direction : input;
    capacitance : 1;
    /* missing related_power_pin attribute, will use default PV1 */
    related_ground_pin : VSS;
  }
  pin(Z) {
    direction : output;
    function : "A";
```

```
    related_power_pin : PV1;
    related_ground_pin : VSS;
    timing() {
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 96, Connect pin 'A' to the default power pg_pin 'PV1'. (LBDB-725)
```

LBDB-726 (error) All the pins in the '%s' cell with more than 2 %s pg_pins must have '%s' attribute.

DESCRIPTION

The related_power_pin (or the related_ground_pin) attribute is missing in a pin within a cell with more than 2 power pg_pins (or ground pg_pins) respectively.

WHAT NEXT

Check the library source file to see if you missed the related_power_pin or the related_ground_pin attributes.

EXAMPLES

```
   voltage_map(VDD0, 1.8);
   voltage_map(VDD1, 1.9);
   voltage_map(VDD2, 23);
   voltage_map(VSS, 0);

cell(lbdb428) {
  area : 2;
  pad_cell : true;
  pg_pin(PV1) {
    voltage_name : VDD1;
    pg_type : primary_power;
  }
  pg_pin(PV2) {
    voltage_name : VDD2;
```

```
    pg_type : primary_power;
  }
  pg_pin(VSS) {
    voltage_name : VSS;
    pg_type : primary_ground;
  }
  pin(A) {
    direction : input;
    capacitance : 1;
    /* missing related_power_pin attribute, will use default PV1 */
    related_ground_pin : VSS;
  }
  pin(Z) {
    direction : output;
    function : "A";
    related_power_pin : PV1;
    related_ground_pin : VSS;
    timing() {
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
```

To fix the problem, add the attribute to the 'A' pin group,

```
        related_power_pin : VDD1;
```

EXAMPLE MESSAGE

Error: Line 96, All the pins in the 'lbdb726' cell with more than 2 power pg_pins must have 'related_power_pin' attribute. (LBDB-726)

LBDB-727 (error) The %s%s '%s' contains the conflicting %s '%s' for pin '%s' and %s '%s' for pin '%s'.

DESCRIPTION

This error message occurs when the **input_signal_level** , **output_signal_level**, or **related_power_pin** values is modeled incorrectly for the level shifter or isolation cell. See detail checking as described below.

In Liberty, we support two kinds (old and new) of pg syntax.

Rule for a level shifter in old syntax : The rail name of **input_signal_level** in

input pin can’t be the same as rail name of **output_signal_level** in output pin.

Rule for a level shifter in new syntax : If **input_signal_level** and **related_power_pin** both present in input pin, then Library Compiler will choose the value of **input_signal_level** for comparison. Either **input_signal_level** or **related_power_pin** in input pin can’t refer to the same voltage name as what **related_power_pin** refers to in output pin.

Rule for an isolation cell in old syntax : The rail value of **input_signal_level** in input pin shall be the same as the rail value of **output_signal_level** in output pin.

Rule for an isolation cell in new syntax : The value of either **input_signal_level** or **related_power_pin** in input pin shall refer to the same voltage value as what **related_power_pin** refers to in output pin.

EXAMPLES

The following example shows the level shifter with the incorrect modeling and the resulting error message in new pg syntax:

```
library (test) {
voltage_map( VSS, 0.0);
voltage_map( VDDH, 0.9);
voltage_map( VDDL, 0.7);
cell(LS) {
pg_pin(GND) {
voltage_name : VSS;
pg_type : primary_ground;
}
pg_pin(VDD2) {
voltage_name : VDDH;
pg_type : primary_power;
}
pg_pin(VDD1) {
voltage_name : VDDL;
pg_type : primary_power;
}

 is_level_shifter : true;
 ...
 pin(in) {
      ...
        input_signal_level : VDDL;
related_power_pin : VDD1;  /* discard */
related_ground_pin : GND;
 }
 pin(out) {
      ...
related_power_pin: VDD1;
related_ground_pin : GND;
 }
}
```

In this case, input_signal_level "VDDL", which is the same voltage name as what related_power_pin "VDD1" is referring to.

Error: Line 191, The level shifter 'LS' contain the conflicting input_signal_level 'VDDL' for pin 'in' and related_power_pin 'VDD1' for pin 'out'. (LBDB-727)

WHAT NEXT

Modify the modeling information of the level shifter to meet the requirements.

To correct the modeling of the example above, make the **input_signal_level** value of the input pin different from the **related_power_pin** value of the output pin as follows:

```
cell(LS) {
 is_level_shifter : true;
 ...
 pin(in) {
        ...
        input_signal_level : VDDL;
   related_power_pin: VDD1;
   related_ground_pin : GND;
 }
 pin(out) {
        ...
   related_power_pin: VDD2;
   related_ground_pin : GND;
 }
}
```

EXAMPLES

The following example shows the isolation cell with the incorrect modeling and the resulting error message in new pg syntax:

```
library (libdb727) {
voltage_map( VDD, 0.7);
voltage_map(VDDH, 0.80); /* high power */
voltage_map(VDDL, 0.4); /* low power */
voltage_map(VSS, 0.0);   /* primary ground */
cell(ISO) {
pg_pin(VDD1) {
voltage_name : VDDH;
pg_type : primary_power;
}
pg_pin(VDD2) {
voltage_name : VDDL;
pg_type : primary_power;
}
```

```
 is_isolation_cell : true;
 ...
 pin(in) {
        ...
        related_power_pin : VDD1;
        related_ground_pin : GND;
 }
 pin(out) {
        ...
        related_power_pin: VDD2;
        related_ground_pin : GND;
 }
}
```

In this case, related_power_pin 'VDD1' is referred to voltage value 0.8 and related_power_pin 'VDD2' is referred to voltage value 0.4. So, the valtage value 0.8 in input pin is different from valtage value 0.4 in output pin, which is wrong.

```
Error: Line 191, The isolation cell 'ISO' contain the conflicting related_power_pin
        'VDD1' for pin 'in' and related_power_pin 'VDD2' for pin 'out'. (LBDB-727)
```

WHAT NEXT

Modify the modeling information of the isolation cell to meet the requirements.

To correct the modeling of the example above, make the **related_power_pin** value of the input pin same as the **related_power_pin** value of the output pin as follows:

```
   library (libdb727) {
   voltage_map( VDD, 0.7);
   voltage_map(VDDH, 0.80); /* high power */
   voltage_map(VDDL, 0.4); /* low power */
   voltage_map(VSS, 0.0);   /* primary ground */
   cell(ISO) {
   pg_pin(VDD1) {
   voltage_name : VDDH;
   pg_type : primary_power;
   }
   pg_pin(VDD2) {
   voltage_name : VDDL;
   pg_type : primary_power;
   }

    is_isolation_cell : true;
    ...
    pin(in) {
           ...
           related_power_pin : VDD1;
           related_ground_pin : GND;
    }
    pin(out) {
           ...
```

```
            related_power_pin: VDD1;
            related_ground_pin : GND;
     }
    }
```

EXAMPLES

The following example shows the level shifter with the incorrect modeling and the resulting error message in old pg syntax:

```
cell(LS) {
 is_level_shifter : true;
 ...
 pin(in) {
      ...
input_signal_level : VDD2

 }
 pin(out) {
      ...
output_signal_level : VDD2

 }
}
```

Error: Line 191, The level shifter ’LS’ contain the conflicting input_signal_level ’VDD2’ for pin ’in’ and output_signal_level ’VDD2’ for pin ’out’. (LBDB-727)

WHAT NEXT

Modify the modeling information of the level shifter to meet the requirements.

To correct the modeling of the example above, make the **input_signal_level** string of the input pin different from the **output_signal_level** string "VDD2" of the output pin as follows:

```
   cell(LS) {
    is_level_shifter : true;
    ...
    pin(in) {
            ...
            input_signal_level : VDD1
    }
    pin(out) {
            ...
            output_signal_level : VDD2
    }
```

```
   }
```

EXAMPLES

The following example shows the isolation cell with the incorrect modeling and the resulting error message in old pg syntax:

```
library(libdb727) {
  ...
  /* operation conditions */
  operating_conditions(5v_1v) {
    ...
    power_rail (VDDH, 5);    /* high power */
    power_rail (VDDL, 1);    /* low power */
    ...
  }
  ...
  default_operating_conditions : 5v_1v;

  ...
cell(ISO) {
 is_isolation_cell : true;
 ...
 pin(in) {
        ...
        input_signal_level : VDDH
 }
 pin(out) {
        ...
        output_signal_level : VDDL
 }
}
```

```
Error: Line 191, The isolation cell 'ISO' contain the conflicting input_signal_leve
l 'VDDH' for pin 'in' and output_signal_level 'VDDL' for pin 'out'. (LBDB-727)
```

WHAT NEXT

Modify the modeling information of the isolation cell to meet the requirements.

input_signal_level 'VDDH' is referred to voltage value '5' and output_signal_level 'VDDL' is referred to voltage value '1'. The voltage value is '5' in input pin and the voltage value is '1' in output pin, which is wrong.

To correct it, you can assiged both to the same voltage like "VDDH", so that both will refer to same value "5" in operating_conditions as follows.

```
   library(libdb727) {
```

```
    ...
    /* operation conditions */
    operating_conditions(5v_1v) {
      ...
      power_rail (VDDH, 5);    /* high power */
      power_rail (VDDL, 1);    /* low power */
      ...
    }
    ...
    default_operating_conditions : 5v_1v;

    ...
  cell(ISO) {
   is_isolation_cell : true;
   ...
   pin(in) {
          ...
          input_signal_level : VDDH
   }
   pin(out) {
          ...
          output_signal_level : VDDH

   }
  }
```

SEE ALSO

LBDB-747

LBDB-728 (error) You can not specify the same pin '%s' twice in '%s'.

DESCRIPTION

This message indicates that you specified the same pin more than one in either **related_inputs** or **related_outputs**. Each pin can be only specifed once.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell(lbdb728) {
  area : 2;
  pin(A) {
    direction : input;
```

```
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }

  pin(Z) {
    direction : output;
    function : "A B";
    timing() {
     ...
    }
  }
  dynamic_current() {
    when : "A";
    related_inputs : "B B";
    related_outputs : "Z Z"
    typical_capacitances(0.3 0.4);
    switching_group() {
     ...
    }
  }
  ...
}
```

In this case, both related_outputs and related_inputs, have specified the same pin name twice. To fix the problems, change the name from 'Z Z' to 'Z' in the related_outputs, change the name from 'B B' to 'B' in the related_inputs.

EXAMPLE MESSAGE

```
Error: Line 272, You can not specify the same pin 'Z' twice
in 'related_outputs'. (LBDB-728)
Error: Line 572, You can not specify the same pin 'B' twice
        in 'related_inputs'. (LBDB-728)
```

LBDB-729 (error) You can't specify the same pin '%s' in different related_output attributes which are under the same intrinsic_parasitic group.

DESCRIPTION

If there are more than one **intrinsic_resistance** group under a **intrinsic_parasitic** group, then no **related_output** can have the same pin. However, the rule does not apply to closed channel, where the value specified in **intrinsic_resistance** group is greater than 1M Ohm.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
library(my) {
  /* unit attributes */
  time_unit : "1ns";
  capacitive_load_unit (1.0,pf);
  ...
 cell(lbdb729) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }
  intrinsic_parasitic() {
    /* default state */
    intrinsic_resistance(<pg_name>) {
       related_output : "ZN";
       value : 9.0;
    }
    intrinsic_resistance(<pg_name>) {
       related_output : "ZN";
       value : 920.0;
    }
    intrinsic_resistance(<pg_name>) {
       related_output : "ZN";
       value : 1001.0;
    }
    intrinsic_capacitance(<pg_name>) {
       value : 8.2;
    }
  }
  ...
 }
}
```

Based on timing and capacitance unit, we know the resistance unit is kilo. In this case, all intrinsic_resistance groups under a intrinsic_parasitic have same related_output 'ZN'. To fix the problem, change the name 'ZN' to 'Z' in either the group which has value '9.0' or the group which has value '920.0' because both are

opened channel. No need to change the name in the group which has value '1001.0' because it is greater than 1M ohm, which is closed channel.

EXAMPLE MESSAGE

Errorr Line 272, You can't specify the same pin 'ZN' in different related_output attributes which are under the same intrinsic_parasitic group. (LBDB-729)

LBDB-730 (error) The pin '%s' specified in the '%s' is neither an %s pin nor an inout pin.

DESCRIPTION

This message indicates that direction of the pin you specified in a **related_inputs**, **related_outputs**, **related_output**, **index_output** or **gate_leakage** is wrong.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell(lbdb730) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A B";
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A B";
    }
  }
  leakage_current() {
     when : "A & !B & Z";
     pg_current(V1) {
```

```
      ...
     }
     ...
     gate_leakage(Z) {  /* must be input or inout pin */
       input_high_value : 2.1;
       input_low_value : -1.7;
     }
  }
  dynamic_current() {
    when : "A";
    related_inputs : "Z";
    related_outputs : "B"
    typical_capacitances(0.3);
    switching_group() {
      input_switching_condition(fall);
      output_switching_condition(rise);
      pg_current(<pg_name>) {
        vector(<lu_template_name>) {
          reference_time : 93.2;
          index_output : "A";
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
      }
     ...
    }
  }
  intrinsic_parasitic() {
    /* default state */
    intrinsic_resistance(<pg_name>) {
       related_output : "B";
       value : 9.0;
    }
    intrinsic_capacitance(<pg_name>) {
       value : 8.2;
    }

  }
  ...
}
```

In this case, all related_output, related_outputs, related_inputs, index_output and gate_leakage have a wrong pin name. To fix the problems, change the name from ’Z’ to either ’A’ or ’B’ in the related_inputs, change the name from ’B’ to ’Z’ in the related_outputs, change the name from ’A’ to ’Z’ in the index_output, change the name from ’B’ to ’Z’ in the related_output and change the name from ’Z’ to either ’A’ or ’B’ in the gate_leakage.

EXAMPLE MESSAGE

```
Error: Line 272, The pin ’Z’ specified in the ’related_inputs’ is neither
        an input pin nor an inout pin. (LBDB-730)
Error: Line 471, The pin ’B’ specified in the ’related_outputs’ is neither
```

```
        an output pin nor an inout pin. (LBDB-730)
Error: Line 526, The pin 'A' specified in the 'index_output' is neither
        an output pin nor an inout pin. (LBDB-730)
Error: Line 890, The pin 'B' specified in the 'related_output' is neither
        an output pin nor an inout pin. (LBDB-730)
Error: Line 749, The pin 'Z' specified in the 'gate_leakage' is neither
        an input pin nor an inout pin. (LBDB-730)
```

LBDB-731 (error) The pin '%s' specified in the '%s' can not be found in '%s'.

DESCRIPTION

Whatever the pin you specified in **index_output** must be matched to one of pins that you specified in **related_outputs**.

This message indicates that the pin you specified in a **index_output** is wrong because it can not be found in **related_outputs** which is defined under the same dynamic_current group as where **index_output** is defined.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell(lbdb731) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }
  dynamic_current() {
    when : "A";
    related_inputs : "B";
    related_outputs : "Z"
    typical_capacitances(0.3);
```

```
    switching_group() {
      input_switching_condition(fall);
      output_switching_condition(rise);
      pg_current(<pg_name>) {
        vector(<lu_template_name>) {
          reference_time : 93.2;
          index_output : "ZN";
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
      }
     ...
    }
  }
  ...
}
```

In this case, index_output have a wrong pin 'ZN' because it does not match the pin 'Z', which is specified in related_outputs. To fix the problem, change the name from 'ZN' to 'Z' in index_output.

EXAMPLE MESSAGE

```
Error: Line 272, The pin 'ZN' specified in the 'index_output' can not
be found in 'related_outputs'. (LBDB-731)
```

LBDB-732 (error) You cannot specify more than one output pin or one bit of a bus or bundle output pin in the '%s'.

DESCRIPTION

Only single output pin is allowed to be specified in a **index_output** and a **related_output**.

This message indicates that you specified multiple pins either in a **index_output** or in a **related_output**.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell(lbdb732) {
  area : 2;
```

```
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }

  dynamic_current() {
    when : "A";
    related_inputs : "B";
    related_outputs : "Z ZN"
    typical_capacitances(0.3 0.4);
    switching_group() {
      input_switching_condition(fall);
      output_switching_condition(rise fall);
      pg_current(<pg_name>) {
        vector(<lu_template_name>) {
          reference_time : 93.2;
          index_output : "Z ZN";
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
      }
     ...
    }
  }
  ...
  intrinsic_parasitic() {
    /* default state */
    intrinsic_resistance(<pg_name>) {
       related_output : "Z ZN";
       value : 9.0;
    }
    intrinsic_capacitance(<pg_name>) {
       value : 8.2;
    }

  }

}
```

In this case, index_output and related_output have specified "Z ZN" which is wrong. To fix the problem, remove either ’Z’ or ’ZN’ from "Z ZN".

EXAMPLE MESSAGE

```
Error: Line 272, You cannot specify more than one output pin or one bit
of a bus or bundle output pin in the 'index_output'. (LBDB-732)
Error: Line 262, You cannot specify more than one output pin or one bit
of a bus or bundle output pin in the 'related_output'. (LBDB-732)
```

LBDB-733 (warning) An %s pin '%s' should specify at least 1 non-static '%s' %s.

DESCRIPTION

This message indicates that the following rule is not satisfied: an input/inout pin should have at least 1 non-static ccsn_first_stage group in the pin group if it is referred as the related_pin in a timing arc and the timing arc does not have non-static ccsn_first_stage group.

A static CCS noise model captures the behaviors of a static CCB (channel connected block). A static CCB refers to a CCB that does not have any input terminal or the voltage level at the input terminal does not affect the output current of the CCB. For example, a static CCS noise model can be characterized for a CMOS NAND gate when both inputs are tied to ground. Such static CCS noise models can be used in noise analysis with case analysis, but they cannot be used for propagating crosstalk delay or noise waveforms through the cell under study. Please refer to "CCS Noise Library Characterization Guide" for detailed information.

WHAT NEXT

Check the library source file, and fix either the invalid CCS Noise data, or the direction of the pin.

EXAMPLES

```
  cell(good) {
    ...
    pin (A) {
direction : input;
    }

    pin(Y ) {
      direction : output;
      ...
      ccsn_last_stage() {
...
      }

      timing () {
related_pin : A;
cell_rise() {
...
```

```
}
rise_transition() {
...
}
cell_fall() {
...
}
fall_transition() {
...
}
      }
    }
  }
```

In this case, the timing arc A->Y does not have 'ccsn_first_stage' group specified, and the 'A' pin does not have the 'ccsn_first_stage' group specified. To fix the problem, add the non-static 'ccsn_first_stage' group into the pin 'A'.

EXAMPLE MESSAGE

Warning: Line 71, An input/inout pin 'A' should specify at least 1 non-static 'ccsn_first_stage' group. (LBDB-733)

LBDB-734 (warning) an %s pin should specify at least 1 non-static '%s' groups.

DESCRIPTION

This warning message occurs when an input or inout pin does not have non-static ccsn_first_stage group in the pin group and there are no related timing arcs referring this pin as the related_pin.

A static CCS noise model captures the behaviors of a static CCB (channel connected block). A static CCB refers to a CCB that does not have any input terminal or the voltage level at the input terminal does not affect the output current of the CCB. For example, a static CCS noise model can be characterized for a CMOS NAND gate when both inputs are tied to ground. Such static CCS noise models can be used in noise analysis with case analysis, but they cannot be used for propagating crosstalk delay or noise waveforms through the cell under study. See the *Make CCS Noise User Guide* for detailed information.

WHAT NEXT

Check the library source file and fix either the invalid CCS Noise data, or the direction of the pin.

EXAMPLES

The following is an example of incorrect input that causes this warning message:

```
cell(sample) {
  ...
  pin (A) {
 direction : input;
  }

  pin(Y ) {
    direction : output;
    ...
    ccsn_last_stage() {
 ...
    }

  }
}
```

In this example, the A pin does not have the ccsn_first_stage group specified, and there are no associated timing arcs specifying ccs_first_stage groups. To fix the problem, add the non-static ccsn_first_stage group into pin A.

LBDB-735 (error) ’%s’ can’t be specified in ’%s’ if power cell type is macro.

DESCRIPTION

Currently in Liberty syntax, we support two power cell types for CCS power model. One is ’stdcell’ and another is ’macro’. For a ’macro’ cell type, there is one restriction. You can not specify **related_outputs** in **dynamic_current** group and **output_switching_condition** in **switching_group** group if cell type in CCS power is ’macro’.

This message indicates that you either specified **related_outputs** or **output_switching_condition** when cell type is ’macro’.

WHAT NEXT

Check the library source file, and make the necessary correction. You can remove **output_switching_condition** or **related_outputs** attribute to avoid the error if you specify any of them.

EXAMPLES

```
cell(lbdb735) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
```

```
  }
    ...
  power_cell_type : macro;
  dynamic_current() {
    ...
    related_outputs : "Z ZN";               /* remove this */
    typical_capacitances(0.3 0.4);
    switching_group() {
      input_switching_condition(fall);
      output_switching_condition(rise fall); /* remove this */
      pg_current(<pg_name>) {
        vector(<lu_template_name>) {
        ...
        }
        ...
      }
     ...
    }
  }
  ...
}
```

In the case above, related_outputs and output_switching_condition are sepcified when cell type is 'macro', which is wrong. To fix the problem, we shall remove both attributes.

EXAMPLE MESSAGE

```
Error: Line 272, 'related_outputs' can't be specified in 'dynamic_current' if power
 cell type is macro. (LBDB-735)
Error: Line 292, 'output_switching_condition' can't be specified in 'switching_grou
p' if power cell type is macro. (LBDB-735)
```

LBDB-736 (error) Size of '%s' must be the same as size of related_outputs.

DESCRIPTION

Size of **output_switching_condition** specified in **switching_group** and size of **related_outputs** specified in **dynamic_current**, they must be identical, which is the same for **typical_capacitances**. Meaning that size of **typical_capacitances** specified in **dynamic_current** must be the same size as what **related_outputs** has.

This message indicates that either size is different between **related_outputs** and **typical_capacitances** or size is different between **related_outputs** and **output_switching_condition**.

WHAT NEXT

Check the library source file, and make the necessary correction. Size of **output_switching_condition**, **related_outputs** and **typical_capacitances** must be identical.

EXAMPLES

```
cell(lbdb736) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }

  dynamic_current() {
    when : "A";
    related_inputs : "B";
    related_outputs : "Z";
    typical_capacitances(0.3 0.4);
    switching_group() {
      input_switching_condition(fall);
      output_switching_condition(rise fall);
      pg_current(<pg_name>) {
        vector(<lu_template_name>) {
          ...
      }
     ...
    }
  }
  ...
  }
}
```

In this case, size of related_outputs is 1 ("Z"), but size of typical_capacitances is 2 (0.3 and 0.4) and size of output_switching_condition is 2 (rise and fall) as well. To fix the problem, you can increase size of related_outputs to 2. You can change "Z" to "Z ZN".

EXAMPLE MESSAGE

```
Error: Line 272, Size of 'typical_capacitances' must be the same as size of related
```

```
_outputs. (LBDB-736)
Error: Line 282, Size of 'output_switching_condition' must be the same as size of r
elated_outputs. (LBDB-736)
```

LBDB-737 (error) '%s' is required in '%s' if index_output is specified
in one of pg_current groups.

DESCRIPTION

For expanded ccs power, if **index_output** is specified in one of **vector** groups, then all of the **vector** groups under the same **pg_current** group must define an **index_output**.

For compact ccs power, if **index_output** is specified in one of **compact_ccs_power** groups, then all of the **compact_ccs_power** groups under the same **pg_current** group must define an **index_output**.

In the case like this, **typical_capacitances** attribute is required in **dynamic_current** group.

This message indicates that there no **typical_capacitances** attribute can be found in **dynamic_current** when **index_output** is defined.

WHAT NEXT

Check the library source file, and make the necessary correction. Add **typical_capacitances** attribute to avoid the error.

EXAMPLES

```
cell(lbdb737) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }
```

```
  dynamic_current() {
    when : "A";
    related_inputs : "B";
    related_outputs : "Z ZN"
    switching_group() {
      ...
      pg_current(<pg_name>) {
        vector(<lu_template_name>) {
          reference_time : 93.2;
          index_output : "Z";
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
        ...
      }
     ...
    }
  }
  ...
}
```

In this case, index_output is specified, but no typical_capacitances attribute is specified. To fix the problem, add the line like this typical_capacitances(0.1); in the dynamic_current group.

EXAMPLE MESSAGE

```
Error: Line 272, 'typical_capacitances' is required in 'dynamic_current' if index_o
utput is specified
       in one of pg_current groups. (LBDB-737)
```

LBDB-738 (error) In '%s' group, size of '%s' must be larger than one
if index_output is defined in one of pg_current groups.

DESCRIPTION

For expanded ccs power, if **index_output** is specified in one of **vector** groups, then all of the **vector** groups under the same **pg_current** group must define an **index_output** attribute.

For compact ccs power, if **index_output** is specified in one of **compact_ccs_power** groups, then all of the **compact_ccs_power** groups under the same **pg_current** group must define an **index_output** attribute.

In the case like this, the size of **related_outputs** must be larger than 1.

This message indicates that the size of **related_outputs** is less than 2, when **index_output** is defined.

WHAT NEXT

Check the library source file, and make the necessary correction. Increase the size of **related_outputs** up to at least 2 to avoid the error.

EXAMPLES

```
cell(lbdb738) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }

  dynamic_current() {
    related_outputs : "Z"
    ...
    switching_group() {
      ...
      pg_current(<pg_name>) {
        vector(<lu_template_name>) {
          reference_time : 93.2;
          index_output : "Z";
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
        ...
      }
     ...
```

In this case, size of related_outputs is 1 ("Z"), when index_output is defined, which is wrong. To fix problem, we shall increase size of related_outputs. We can change "Z" to "Z ZN".

EXAMPLE MESSAGE

```
Error: Line 272, In 'dynamic_current' group, size of 'related_outputs' must be larg
er than one
       if index_output is defined in one of pg_current groups. (LBDB-738)
```

LBDB-739 (error) '%s' attribute is required for this '%s' group.

DESCRIPTION

For expanded ccs power, all **vector** groups under the same **pg_current** group must specify the same template. If there is no any **index_output** attribute specified in these **vector** groups and template used for these **vector** groups contains only one total_output_net_capacitance, then **related_outputs** attribute is required in **dynamic_current**.

For expanded ccs power, all **compact_ccs_power** groups under the same **pg_current** group must specify the same template. If there is no any **index_output** attribute specified in these **compact_ccs_power** groups and template used for these **compact_ccs_power** groups contains only one total_output_net_capacitance, then **related_outputs** attribute is required in **dynamic_current**.

This message indicates that you must specify **related_outputs** attribute in **dynamic_current** because the above rule is applied.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
pg_current_template(test_2) {
   variable_1 : input_net_transition;
   variable_2 : total_output_net_capacitance;
   variable_3 : time;
   index_1("0.6 0.9");
   index_2("0.6 0.9");
   index_3("0.3 4.7");
}
cell(lbdb739) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
```

```
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }

  dynamic_current() {
    when : "A";
    related_inputs : "B";
    ...
    switching_group() {
      input_switching_condition(fall);
      output_switching_condition(rise fall);
      pg_current(<pg_name>) {
        vector(test_2) {
          reference_time : 93.2;
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
        ...
      }
     ...
    }
  }
  ...
}
```

In this case, there is no index_output specified in any vector under a pg_current group. Also, the template (test_2) that vector referred to contains only one total_output_net_capacitance (variable_2). In the case like this a related_outputs attribute is required to be defined in dynamic_current group. To fix the problem, we need to add a related_outputs attribute within a dynamic_current group.

EXAMPLE MESSAGE

```
Error: Line 272, 'related_outputs' attribute is required for this 'dynamic_current'
 group. (LBDB-739)
```

LBDB-740 (error) Size of '%s' in this '%s' group must be two.

DESCRIPTION

For expanded ccs power, all **vector** groups under the same **pg_current** group refer to the same **pg_current_template**.

For compact ccs power, a **compact_ccs_power** group refers to a **compact_lut_template**.

In the pg_current_template or compact_lut_template, if there are two

total_output_net_capacitance, then size of **related_outputs** in **dynamic_current** must be two.

This message indicates that the size of **related_outputs** is not two.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
pg_current_template(test_1) {
   variable_1 : input_net_transition;
   variable_2 : total_output_net_capacitance;
   variable_3 : total_output_net_capacitance;
   variable_4 : time;
   index_1("0.6 0.9");
   index_2("0.6 0.9");
   index_3("0.3 4.7");
   index_4("4.5 6.7 7.2");
}
cell(lbdb740) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }

  dynamic_current() {
    when : "A";
    related_inputs : "B";
    related_outputs : "Z"
    switching_group() {
      ...
      pg_current(<pg_name>) {
        vector(test_1) {
          reference_time : 93.2;
          index_1("5.1");
          index_2("0.3");
          index_3("0.3");
          index_4("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
```

```
        }
        ...
      }
    ...
```

In this case, template 'test_1' contains two total_output_net_capacitance values, but size of related_outputs is 1 ("Z"), which is wrong. To fix the problem, you might want to increase size of related_outputs to two. You can change "Z" to "Z ZN".

EXAMPLE MESSAGE

Error: Line 262, Size of 'related_outputs' in this 'dynamic_current' group must be two. (LBDB-740)

LBDB-741 (error) Two switching_group groups in line %d and %d are overlapping.

DESCRIPTION

If either min_input_switching_count or max_input_switching_count specified in switching groups, and the switching count number they covered are overlapping, then these **switching_group** groups are considered overlapped.

If there is no min_input_switching_count or max_input_switching_count, then two **switching_group** groups are considered overlapped if both **input_switching_condition** and **output_switching_condition** are overlapped.

If one of followings are true, then **output_switching_condition** is considered to be overlapping condition : + **output_switching_condition** is undefined on both **switching_group** groups. + **output_switching_condition** is defined on both **switching_group** groups and values of them are indentical.

If one of followings are true, then **input_switching_condition** is considered to be overlapping condition : + **input_switching_condition** is undefined on both **switching_group** groups. + **input_switching_condition** is defined on both **switching_group** groups and values of them are indentical. + values of them are difference, but one **input_switching_condition** is undefined, and another has value either "rise" or "fall".

This message indicates that two **switching_group** groups are overlapped because **input_switching_condition** and **output_switching_condition** both are in overlapping condition.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell(lbdb741) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }
  power_cell_type : stdcell;
  dynamic_current() {
    when : "A";
    related_inputs : "B";
    related_outputs : "Z ZN"
    typical_capacitances(0.3 0.4);
    switching_group() {
      input_switching_condition(fall);
      output_switching_condition(rise fall);
     ...
    }
    switching_group() {
      output_switching_condition(rise fall);
     ...
    }

  }
  ...
```

In this case, both switching_group have same output_switching_condition, and one input_switching_condition has value "fall" and another is undefined. input_switching_condition is overlapping and which is same as output_switching_condition, so two switching_group groups are overlapped. To fix the problem, you might want to change the value to "fall fall" in one of output_switching_condition groups.

```
type(bus6) {
  base_type : array ;
  data_type : bit ;
  bit_width : 6 ;
  bit_from : 5 ;
  bit_to : 0 ;
  downto : true ;
}
```

```
cell(lbdb741) {
  bus(sel) {
    bus_type : bus6 ;
    direction : input ;
    capacitance : 2 ;
    related_power_pin : V1;
    related_ground_pin : G1;
  }

  bundle(C) {
    members(Cx, Cy, Cz);
    direction : input;
    capacitance : 2 ;
    related_power_pin : V1;
    related_ground_pin : G1;

  }
  area : 2;
  pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
     pg_type : backup_power;
  }
  pg_pin(G1) {
     voltage_name : GND1;
     pg_type : primary_ground;
  }
  pg_pin(G2) {
     voltage_name : GND2;
     pg_type : backup_ground;
  }
  power_cell_type : macro;
  dynamic_current() {
    related_inputs : "C sel";
    switching_group() {
      min_input_switching_count : 1;
      max_input_switching_count : 6;
      ...
    }
    switching_group() {
      min_input_switching_count : 5;
      max_input_switching_count : 9;
      ...
    }
    ...
  }
}
```

In this case, the min_input_switching_count and max_input_switching_count are specified in "macro" cell type. If that is the case, we need to check if the number they covered are overlapping. We don’t worry about input_switching_condition or output_switching_condition here because these attributes can’t be sepcified

if either min_input_switching_count or max_input_switching_count is sepcified.

'C' is 6 bits bus and 'sel' is 3 bits bundle. The total bits are 9.
For the first switching_group, the switching count is from 1 to 6, and for the second switching_group, the switching count is from 5 to 9. The number 5 and 6 are covered in both groups, which means the two groups are overlapping. To fix the problem, please change number 5 to 7 in the second switching_group or change number 6 to 4 in the first switching_group.

SH EXAMPLE MESSAGE

```
Error: Line 100, Two switching_group groups in line 170 and 189 are
       overlapping. (LBDB-741)
```

LBDB-742 (error) Only one total_output_net_capacitance is allowed for the template specified in this %s.

DESCRIPTION

For expanded ccs power, if **index_output** is specified in one of **vector** groups, then all of the **vector** groups under the same **pg_current** group must define an **index_output** attribute.

For compact ccs power, if **index_output** is specified in one of **compact_ccs_power** groups, then all of the **compact_ccs_power** groups under the same **pg_current** group must define an **index_output** attribute.

In the case like this, the template , which these **vector**/**compact_ccs_power** groups referred to, must contains only one total_output_net_capacitance.

This message indicates that the template contains either more than one or less than one total_output_net_capacitance.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
pg_current_template(test_1) {
   variable_1 : input_net_transition;
   variable_2 : total_output_net_capacitance;
   variable_3 : total_output_net_capacitance;
   variable_4 : time;
   index_1("0.6 0.9");
   index_2("0.6 0.9");
   index_3("0.3 4.7");
```

```
   index_4("4.5 6.7 7.2");
}

pg_current_template(test_2) {
   variable_1 : input_net_transition;
   variable_2 : total_output_net_capacitance;
   variable_3 : time;
   index_1("0.6 0.9");
   index_2("0.6 0.9");
   index_3("0.3 4.7");
}
cell(lbdb742) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }

  dynamic_current() {
    when : "A";
    related_inputs : "B";
    related_outputs : "Z ZN";
    typical_capacitances(0.3 0.4);
    switching_group() {
      input_switching_condition(fall);
      output_switching_condition(rise fall);
      pg_current(<pg_name>) {
        vector(test_1) {
          reference_time : 93.2;
          index_output : "Z";
          index_1("5.1");
          index_2("0.3");
          index_3("0.3");
          index_4("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
      }
     ...
```

In this case, index_output is specified in vector, and the vector is referred to template 'test_1', which contains two total_output_net_capacitance values. That is wrong. To fix the problem, we can change referred template to 'test_2'.

EXAMPLE MESSAGE

```
Error: Line 272, Only one total_output_net_capacitance is allowed for the
       template specified in this vector. (LBDB-742)
```

LBDB-743 (error) All %s under a pg_current group must specify same template.

DESCRIPTION

All **vector** or **compact_ccs_power** groups under the same **pg_current** group must specify the same template.

This message indicates that you specified different templates in /fBvector or **compact_ccs_power** groups, which are all under same **pg_current**.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
pg_current_template(test_1) {
   variable_1 : input_net_transition;
   variable_2 : total_output_net_capacitance;
   variable_3 : total_output_net_capacitance;
   variable_4 : time;
   index_1("0.6 0.9");
   index_2("0.6 0.9");
   index_3("0.3 4.7");
   index_4("4.5 6.7 7.2");
}

pg_current_template(test_2) {
   variable_1 : input_net_transition;
   variable_2 : total_output_net_capacitance;
   variable_3 : time;
   index_1("0.6 0.9");
   index_2("0.6 0.9");
   index_3("0.3 4.7");
}
cell(lbdb743) {
  area : 2;
  ...
  dynamic_current() {
     ...
    switching_group() {
      ...
      pg_current(<pg_name>) {
        vector(test_2) {
```

```
          reference_time : 93.2;
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
        vector(test_1) {
          reference_time : 93.2;
          index_1("5.1");
          index_2("0.3");
          index_3("0.3");
          index_4("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
        ...
      }
     ...
```

In this case, two vectors refer to different templates, one is 'test_1', and another is 'test_2'. This is wrong. To fix the problem, change 'test_1' to 'test_2' in second vector.

EXAMPLE MESSAGE

```
Error: Line 272, All vectors under a pg_current group must specify
       same template. (LBDB-743)
```

LBDB-744 (error) index_output is required for all %s in this pg_current group.

DESCRIPTION

For expanded ccs power, if **index_output** is specified in one of **vector** groups, then all of the **vector** groups under the same **pg_current** group must define an **index_output** attribute.

For compact ccs power, if **index_output** is specified in one of **compact_ccs_power** groups, then all of the **compact_ccs_power** groups under the same **pg_current** group must define an **index_output** attribute.

This message indicates that **index_output** attribute is not defined in all **vector**/ **compact_ccs_power** groups under a **pg_current**.

Also to see, LBDB-737, LBDB-738, and LBDB-742.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell(lbdb744) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }

  dynamic_current() {
    when : "A";
    related_inputs : "B";
    related_outputs : "Z ZN"
    typical_capacitances(0.3 0.4);
    switching_group() {
      input_switching_condition(fall);
      output_switching_condition(rise fall);
      pg_current(VDD) {
        vector(<lu_template_name>) {
          reference_time : 93.2;
          index_output : "ZN";
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
         vector(<lu_template_name>) {
          reference_time : 93.2;
          index_output : "Z";
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
        vector(<lu_template_name>) {
          reference_time : 93.2;
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
      }
     ...
```

```
    }
  }
  ...
```

In this case, index_output is not specified in third vector, which is wrong. All vectors under pg_current(VDD) must specify index_output, because index_output has beed defined in one of vectors. To fix the problem, add index_output attribute to the third vector.

EXAMPLE MESSAGE

```
Error: Line 272, index_output is required for all vectors in this
       pg_current group. (LBDB-744)
```

LBDB-745 (error) Under this dynamic_current, pin '%s' is specified in '%s' and '%s'.

DESCRIPTION

/fBwhen, **related_outputs**, and **related_inputs** can't specify the same pin if they are under the same **dynamic_current** group.

This message indicates that you specified the same pin for two of following attributes : /fBwhen, **related_outputs**, and **related_inputs**

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell(lbdb745) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
```

```
    ...
  }
  pin(ZN1) {
    direction : output;
    ...
  }
  dynamic_current() {
    when : "B + ZN'";
    related_inputs : "B";
    related_outputs : "Z ZN"
    typical_capacitances(0.3 0.4);
    switching_group() {
  ...
}
```

In this case, pin B is specified in both when and related_inputs, which is wrong. Same for pin ZN, which is specified in both when and related_outputs. To fix the problem, change "B" to "A" in related_inputs, and change "Z ZN" to "Z ZN1" in related_outputs.

EXAMPLE MESSAGE

```
Error: Line 272, Under this dynamic_current, pin 'B' is specified in

       'related_inputs' and 'when'. (LBDB-745)
Error: Line 272, Under this dynamic_current, pin 'ZN' is specified in

       'related_outputs' and 'when'. (LBDB-745)
```

LBDB-746 (error) The %s of cell '%s' should be specified before the %s '%s' is defined.

DESCRIPTION

You receive this message because the switch_cell_type is not defined before specifying the attributes related to switch cells.

WHAT NEXT

Make sure that **switch_cell_type** attribute exists before defining other attributes related switch cells.

EXAMPLES

The following example shows the *switch_cell_type* is missing.

```
cell(sample) {
 pin(Y)  {
switch_function : "sp";
```

```
...
 }
  ......
}
```

Correct it by add **fBswitch_cell_typefp attribute in the cell group.**

EXAMPLE MESSAGE

Error: Line 191, The switch_cell_type attribute of cell 'sample' should be specified before the switch_function 'sp' is defined. (LBDB-746)

LBDB-747 (warning) %s on input pin and %s on output pin have same power rail value but different rail name.

DESCRIPTION

This message will only be applied for an isolation cell.

In Liberty, we support two kinds (old and new) of pg syntax. If **input_signal_level** and **related_power_pin** both presented in new syntax, then **input_signal_level** will be chosen, and **related_power_pin** will be discarded.

If you are in new pg syntax, the message indicates that voltage name of either **input_signal_level** or **related_power_pin** in input pin is different from voltage name of **related_power_pin** in ouput pin, but both are referring to the same voltage value.

If you are in old pg syntax, the message indicates that rail name of **input_signal_level** in input pin is different from rail name of foutput_signal_level in ouput pin, but both rail names are referring to the same voltage value.

WHAT NEXT

Check the library source file, and make the necessary correctiorn if it is needed.

EXAMPLES

```
/* This is an example of old pg syntax. */
library(libdb747) {
 ...
   power_supply() {
        default_power_rail : VDD;
        power_rail (VDDH, 3); /* high power */
        power_rail (VDDL, 3); /* low power */
        power_rail (VSS, 0.0);   /* primary ground */
  }
  ...
  /* operation conditions */
  nom_process   : 1;
```

```
  nom_temperature       : 25;
  nom_voltage   : 1.0;
  operating_conditions(3v_3v) {
    process     : 1;
    temperature : 25;
    voltage     : 1.0;
    tree_type   : balanced_tree
    power_rail (VDDH, 3);    /* high power */
    power_rail (VDDL, 3);    /* low power */
    power_rail (VSS, 0.0);   /* primary ground */
  }
  default_operating_conditions : 3v_3v;

 ...
cell (LVLHLEHX2M) {
  ...
  rail_connection (VDD, VDDL);
  area : 2.600000;
  is_isolation_cell : true;
  pin(A) {
    direction : input;
    input_signal_level : VDDH;
    capacitance : 0.1859;
    internal_power() {
    ...
  }
  pin(Y) {
    direction : output;
    output_signal_level : VDDL;
    capacitance : 0.0;
    function : "(A & EN)";
    internal_power() {
      power_level : VDDL;
   ...
```

In this case, input_signal_level in input pin "A" is specified "VDDH" as power rail, which is different from "VDDL" specified in output_signal_level in output pin "Y". However, both "VDDH" and "VDDL" are referring to same voltage value "3" as defined in operating_conditions group.

EXAMPLE MESSAGE

```
Warning: Line 100, input_signal_level on input pin and output_signal_level on outpu
t pin
have same power rail value but different rail name. (LBDB-747)
```

EXAMPLES

```
/* This is an example of new pg syntax */
library (libdb747) {
```

```
voltage_map( VDD, 0.7);
voltage_map(VDDH, 0.8); /* high power */
voltage_map(VDDL, 0.8); /* low power */
voltage_map(VSS, 0.0);   /* primary ground */
cell(ISO) {
pg_pin(VDD1) {
voltage_name : VDDH;
pg_type : primary_power;
}
pg_pin(VDD2) {
voltage_name : VDDL;
pg_type : primary_power;
}

 is_isolation_cell : true;
 ...
 pin(in) {
        ...
        input_signal_level : VDDH;
        related_power_pin : VDD1;  /* discard */
        related_ground_pin : GND;
 }
 pin(out) {
        ...
        related_power_pin: VDD2;
        related_ground_pin : GND;
 }
}
```

In this case, input_signal_level 'VDDH' is referred to voltage value 0.8 and related_power_pin 'VDD2' is referred to voltage value 0.8, too. The voltage value 0.8 in input pin is same as valtage value in output pin, but their voltage names are different, one is VDDH, and the other is VDDL.

EXAMPLE MESSAGE

```
Warning: Line 100, input_signal_level on input pin and related_power_pin on output
pin
        have same power rail value but different rail name. (LBDB-747)
```

SEE ALSO

LBDB-727

LBDB-748 (error) There are less than 4 vectors specified in

group ’%s’.

DESCRIPTION

This error message occurs because Library Compiler requires at least 4 vectors inside each output_current_rise or output_current_fall group.

The following example shows an output_current_rise group without a dense vector and resulting error message.

```
    output_current_template(CCT) {
     variable_1 : input_net_transition;
     variable_2 : total_output_net_capacitance;
     variable_3 : time;
    }
    . . .
    output_current_rise() {
      vector(CCT) {
         reference_time : 0.11;
         index_1 ("0.1");
         index_2 ("1");
         index_3 ("1, 2, 3");
         values ("1, 2, 3");
      }
      /* need at least additional 3 vectors to compile */
    }
```

```
   Error: Line 198, There are less than 4 vectors specified in group ’output_curren
t_rise’.  (LBDB-748)
```

WHAT NEXT

Check the library source file and add additional vectors.

LBDB-749 (error) The size of %s should be at least %d.

DESCRIPTION

The specification of the size of the index is less than the minim index size.

WHAT NEXT

Check the library source file, and correct the problem by inceasing the size of the specified index.

EXAMPLES

```
  lu_table_template(basic_template) {
variable_1 : input_net_transition;
index_1 ("1");
  }

  receiver_capacitance1_rise(basic_template) {
index_1 ("500");
values ("1.3401");
  }
```

EXAMPLE MESSAGE

```
Error: Line 160, The size of index_1 should be at least 2. (LBDB-749)
```

LBDB-750 (warning) Overwrite '%s' by default '%s' value %f defined in 'operating_conditions'.

DESCRIPTION

There are two pg pin syntaxes in liberty: one is old syntax such as power_rail or rail_connection, another is new syntax such as voltage_map or pg_pin.

If new pg_pin syntax has been defined in .lib file , all PVT (process, voltage and temperature) defined in default_operating_conditions will be copied over to nom PVT.

The warning message indicates that whatever default nom PVT values you defined have been overwritten by values of default_operating_conditions.

EXAMPLES

```
library(libdb750) {
 ...
  nom_process : 1.3
  nom_temperature : 20.0;
  nom_voltage : 4.0;

  operating_conditions ( TYPICAL ) {
    process : 1.0 ;
    temperature : 22.0 ;
    voltage : 3.0 ;
    tree_type : balanced_tree ;
  }
  default_operating_conditions :  TYPICAL;
   ...
  voltage_map(VDD1, 4.0); /* new pg pin syntax */
  voltage_map(VDD2, 4.5);
```

```
  ...
cell (and2) {
  ...
pg_pin(V1) { /* new pg pin syntax */
   voltage_name : VDD1;
   pg_type : primary_power;
}
pg_pin(V2) {
   voltage_name : VDD2;
   pg_type : backup_power;
}
...
```

In this case, nom_process will be overwritten by "process" value 1.0, which is defined in default operating_conditions group. nom_temperature will be overwritten by "temperature" value 22.0, which is defined in default operating_conditions group. nom_voltage will be overwritten by "voltage" value 3.0, which is defined in default operating_conditions group.

EXAMPLE MESSAGE

```
Warning: Line 100, Overwrite 'nom_process' by default 'process' value 1.0 defined
in 'operating_conditions'. (LBDB-750)
Warning: Line 100, Overwrite 'nom_temperature' by default 'temperature' value 22.0
defined
in 'operating_conditions'. (LBDB-750)
Warning: Line 100, Overwrite 'nom_voltage' by default 'voltage' value 3.0 defined
in 'operating_conditions'. (LBDB-750)
```

LBDB-751 (error) The %s group with name '%s', has not been defined in the %s.

DESCRIPTION

This message indicates that the referred group name is undefined in the library.

WHAT NEXT

Add the referred group in the library. Or remove the reference

EXAMPLE MESSAGE

```
Error: Line 57, The base_curves group with name 'AND2",
       has not been defined in the library.(LBDB-751)
```

LBDB-752 (error) The '%s' attribute is missing in compressed_lut_template '%s'.

DESCRIPTION

This message indicates that the attribute is not defined in the compressed_lut_template group.

WHAT NEXT

Add the attribute in compressed_lut_template.

EXAMPLE MESSAGE

Error: Line 58, The 'base_curves_group' attribute is missing in compressed_lut_template 'LTT3'.(LBDB-752)

LBDB-753 (error) The '%s' base curve parameter is missing in compressed_lut_template '%s' index_3.

DESCRIPTION

For ccs timing base curves, these six elementary curve parameters are must needed: init_current, peak_current, peak_voltage, peak_time, left_id, right_id. Additional parameters are also allowed, the index_3 value list can contains more than six parameters.

WHAT NEXT

Add the missing elementary curve parameter in compressed_lut_template index_3.

EXAMPLES

```
    compressed_lut_template(LTT3) {
variable_1 : input_net_transition;
variable_2 : total_output_net_capacitance;
variable_3 : curve_parameters;
index_1 ("0.1, 0.2");
index_2 ("1.0, 1.2");
index_3 ("init_current, peak_current, peak_voltage, left_id, right_id");
    }
```

EXAMPLE MESSAGE

Error: Line 60, The 'peak_time' base curve parameter is missing in compressed_lut_t

emplate ’LTT3’ index_3.(LBDB-753)

LBDB-754 (error) Redudant curve_x defined in base_curves ’%s’.

DESCRIPTION

In a base_curves group, only one curve_x definition is allowed, otherwise it brings confusing to users.

WHAT NEXT

Remove redudant curve_x definition in base curves group, left one curve_x is enough.

EXAMPLES

```
    base_curves(AND2_BC) {
base_curve_type : ccs_timing_half_curve;
curve_x ("0.1, 0.5, 0.9");
curve_x ("0.2, 0.5, 0.8");
curve_y (1, "0.8, 0.5, 0.2");
curve_y (2, "0.85, 0.5, 0.15");
...
    }
```

EXAMPLE MESSAGE

Error: Line 62, Redudant curve_x defined in base_curves ’AND2_BC’.(LBDB-754)

LBDB-755 (error) Illegal base curve data is specified in ’%s’.

DESCRIPTION

The syntax of base_curves group: base_curves("name") { base_curve_type : ccs_half_curve; curve_x ("float..., float"); curve_y (curve_id, "float..., float"; ... }

Following are rules for base curve data: For curve data specified in curve_x: 1. At least 3 points are specified; 2. The value should between 0 and 1; 3. The values should be monotonic increasing;

For curve_data specified in curve_y: 1. number of points should be same as as that in curve_x; 2. curve_y should be defined after curve_x; 3. valid boundary is [-inf, 1] for both compact CCS timing and compact CCS power.

WHAT NEXT

Check base curve data according these rules, fix error.

EXAMPLES

```
    base_curves(AND2_BC) {
base_curve_type : ccs_timing_half_curve;
curve_x ("0.1, 0.5, 1.1");
curve_y (1, "0.8, 0.5, 0.2, 0.1");
curve_y (2, "0.85, 0.5, 0.15");
...
    }
```

EXAMPLE MESSAGE

```
Error: Line 63, Illegal base curve data is specified in 'curve_x'.(LBDB-755)
Error: Line 64, Illegal base curve data is specified in 'curve_y'.(LBDB-755)
```

LBDB-756 (error) No curve_x definition found before curve_y in the base_curves '%s'.

DESCRIPTION

In a base_curves group, Only and Must have one curve_x defined before curve_y.

WHAT NEXT

Add the curve_x definition before the curve_y, otherwise, the base curve data is incomplete.

EXAMPLES

```
    base_curves(AND2_BC) {
base_curve_type : ccs_timing_half_curve;
curve_y (1, "0.8, 0.5, 0.2");
curve_y (2, "0.85, 0.5, 0.15");
...
    }
```

EXAMPLE MESSAGE

```
Error: Line 65, No curve_x definition found before curve_y in the base_curves 'AND2
_BC'.(LBDB-756)
```

LBDB-757 (error) No curve_y definition found in the base_curves '%s'.

DESCRIPTION

In a base_curves group, base curves are demonstrated by curve_x and curve_y together. curve_y can't be absent.

WHAT NEXT

Add the curve_y definition after the curve_x, in the base curves group.

EXAMPLES

```
    base_curves(AND2_BC) {
base_curve_type : ccs_timing_half_curve;
curve_x ("0.1, 0.5, 0.9");
    }
```

EXAMPLE MESSAGE

Error: Line 63, No curve_y definition found in the base_curves 'AND2_BC'.(LBDB-757)

LBDB-758 (error) Duplicate or negative curve_id '%d' is specified.

DESCRIPTION

In a base_curves group, the curve_id in curve_y should satisfy following rules: 1. curve_id should be an interger that greater than 0; 2. curve_id should be unique in the base_curves group;

WHAT NEXT

Check rules above, correct the curve_id data in curve_y.

EXAMPLES

```
    base_curves(AND2_BC) {
base_curve_type : ccs_timing_half_curve;
curve_x ("0.1, 0.5, 1.1");
curve_y (-1, "0.8, 0.5, 0.2, 0.1");
curve_y (2, "0.85, 0.5, 0.15");
curve_y (4, "0.8, 0.5, 0.2, 0.1");
curve_y (4, "0.85, 0.5, 0.15");
```

```
...
    }
```

EXAMPLE MESSAGE

```
Error: Line 63, Duplicate or negative curve_id '-1' is specified.(LBDB-758)
Error: Line 60, Duplicate or negative curve_id '4' is specified.(LBDB-758)
```

LBDB-759 (error) Bad init_current value '%g' is specified in '%s'.

DESCRIPTION

Init_current is one of six parameters to model compressed ccs timing base curve. In compressed_ccs_rise group, the init_current values should >= 0; And in compressed_ccs_fall group, the init_current values should <= 0;

WHAT NEXT

According the rule above, correct the init_current value.

EXAMPLES

```
library(name) {
  ...
  base_curves (ctbct1){
    base_curve_type : ccs_timing_half_curve;
    curve_x("0.2, 0.5, 0.8");
    curve_y(1, "0.8, 0.5, 0.2");
    curve_y(2, "0.75, 0.5, 0.35");
    curve_y(3, "0.85, 0.5, 0.15");
    curve_y(4, "0.85, 0.5, 0.15");
  }
  compressed_lut_template(LTT3) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : curve_parameters;
    index_1 ("0.1, 0.2");
    index_2 ("1.0, 2.0");
    index_3 ("init_current, peak_current, peak_voltage, peak_time, left_id, right_i
d");
    base_curves_group: "ctbct1";
  }

  cell(cell_name) {
    pin(pin_name) {
timing() {
    compressed_ccs_rise("LTT3") {
      values("0, 0.5, 0.6, 0.8, 1, 3",
     "-0.15, 0.55, 0.65, 0.85, 2, 4",
     "0.2, 0.6, 0.7, 0.9, 3, 2", <HardSpace
```

```
                "0.25, 0.65, 0.75, 0.95, 4, 1");
    } /* end of compressed_ccs_rise */
}
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 1163, Bad init_current value '-
0.15' is specified in 'compressed_ccs_rise'.(LBDB-759)
```

SEE ALSO

LBDB-753

LBDB-760 (error) Bad peak_current value '%g' is specified in '%s'.

DESCRIPTION

peak_current is one of six parameters to model compressed ccs timing base curve. In compressed_ccs_rise group, the peak_current values should > 0; And in compressed_ccs_fall group, the peak_current values should < 0;

WHAT NEXT

According the rule above, correct the peak_current value.

EXAMPLES

```
library(name) {
  ...
  base_curves (ctbct1){
    base_curve_type : ccs_timing_half_curve;
    curve_x("0.2, 0.5, 0.8");
    curve_y(1, "0.8, 0.5, 0.2");
    curve_y(2, "0.75, 0.5, 0.35");
    curve_y(3, "0.85, 0.5, 0.15");
    curve_y(4, "0.85, 0.5, 0.15");
  }
  compressed_lut_template(LTT3) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : curve_parameters;
    index_1 ("0.1, 0.2");
```

```
    index_2 ("1.0, 2.0");
    index_3 ("init_current, peak_current, peak_voltage, peak_time, left_id, right_i
d");
    base_curves_group: "ctbct1";
  }

  cell(cell_name) {
    pin(pin_name) {
timing() {
    compressed_ccs_rise("LTT3") {
      values("0.1, 0, 0.6, 0.8, 1, 3",
     "0.15, -0.55, 0.65, 0.85, 2, 4",
     "0.2, 0.6, 0.7, 0.9, 3, 2", <HardSpace
                 "0.25, 0.65, 0.75, 0.95, 4, 1");
    } /* end of compressed_ccs_rise */
}
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 1163, Bad peak_current value ’0’ is specified in ’compressed_ccs_rise’.
(LBDB-760)
Error: Line 1163, Bad peak_current value ’-
0.55’ is specified in ’compressed_ccs_rise’.(LBDB-760)
```

SEE ALSO

LBDB-753

LBDB-761 (error) Non-integer base curve id ’%s’ is specified in ’%s’.

DESCRIPTION

Curve_id should be integers because it is defined with integer data type.

For compact ccs timing, curve_id is the data corresponding to left_id or right_id in compressed_ccs_rise/compressed_ccs_fall group.

For compact ccs power, curve_id is the data corresponding to bc_id* in compact_ccs_power group.

WHAT NEXT

According the rule above, correct the left_id/right_id value in compressed_ccs_rise/

compressed_ccs_fall group, or the bc_id* value in compact_ccs_power group.

EXAMPLES

```
library(name) {
  ...
  base_curves (ctbct1){
    base_curve_type : ccs_timing_half_curve;
    curve_x("0.2, 0.5, 0.8");
    curve_y(1, "0.8, 0.5, 0.2");
    curve_y(2, "0.75, 0.5, 0.35");
    curve_y(3, "0.85, 0.5, 0.15");
    curve_y(4, "0.85, 0.5, 0.15");
  }
  compressed_lut_template(LTT3) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : curve_parameters;
    index_1 ("0.1, 0.2");
    index_2 ("1.0, 2.0");
    index_3 ("init_current, peak_current, peak_voltage, peak_time, left_id, right_i
d");
    base_curves_group: "ctbct1";
  }

  cell(cell_name) {
    pin(pin_name) {
timing() {
    compressed_ccs_rise("LTT3") {
      values("0.1, 0, 0.6, 0.8, 1, 3",
     "0.15, -0.55, 0.65, 0.85, 2, 4",
     "0.2, 0.6, 0.7, 0.9, 3, 2", <HardSpace
                 "0.25, 0.65, 0.75, 0.95, 4, 1");
    } /* end of compressed_ccs_rise */
}
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 1163, Non-integer curve_id(lef_id/
right_id) ’3.5’ is specified in ’compressed_ccs_rise’.(LBDB-761)
Error: Line 1163, Non-integer curve_id(lef_id/
right_id) ’2.0’ is specified in ’compressed_ccs_rise’.(LBDB-761)
```

SEE ALSO

LBDB-753

LBDB-762 (error) Undefined base curve id '%d' is referenced in '%s'.

DESCRIPTION

Curve_id must be predefined in previous base_curve group.

For compact ccs timing, curve_id is the data corresponding to left_id or right_id in compressed_ccs_rise/compressed_ccs_fall group.

For compact ccs power, curve_id is the data corresponding to bc_id* in compact_ccs_power group.

WHAT NEXT

According the rule above, correct the left_id/right_id value in compressed_ccs_rise/ compressed_ccs_fall group, or the bc_id* value in compact_ccs_power group.

EXAMPLES

```
library(name) {
  ...
  base_curves (ctbct1){
    base_curve_type : ccs_timing_half_curve;
    curve_x("0.2, 0.5, 0.8");
    curve_y(1, "0.8, 0.5, 0.2");
    curve_y(2, "0.75, 0.5, 0.35");
    curve_y(3, "0.85, 0.5, 0.15");
    curve_y(4, "0.85, 0.5, 0.15");
  }
  compressed_lut_template(LTT3) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : curve_parameters;
    index_1 ("0.1, 0.2");
    index_2 ("1.0, 2.0");
    index_3 ("init_current, peak_current, peak_voltage, peak_time, left_id, right_i
d");
    base_curves_group: "ctbct1";
  }

  cell(cell_name) {
    pin(pin_name) {
timing() {
    compressed_ccs_rise("LTT3") {
      values("0.1, 0, 0.6, 0.8, 1, 31",
     "0.15, -0.55, 0.65, 0.85, 7, 4",
     "0.2, 0.6, 0.7, 0.9, 3, 2", <HardSpace
                 "0.25, 0.65, 0.75, 0.95, 4, 1");
    } /* end of compressed_ccs_rise */
}
```

```
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 1163, Undefined curve_id(lef_id/
right_id) '31' is referenced in 'compressed_ccs_rise'.(LBDB-762)
Error: Line 1163, Undefined curve_id(lef_id/
right_id) '7' is referenced in 'compressed_ccs_rise'.(LBDB-762)
```

SEE ALSO

LBDB-753

LBDB-763 (error) Incompatible %s data specified in %s.

DESCRIPTION

For ccs timing and power data, there are two models that can be used. One is expanded model, the other is compact model.

Expanded ccs timing model is specified by output_current_{rise|fall}. Compact ccs timing model is specified by compact_ccs_{rise|fall}. Expanded ccs power model is specified by vector under pg_current group. Compact ccs power model is specified by compact_ccs_power under pg_current group.

Currently, only one model is supported in one library. If both of them are used in the library, the error is issued.

Users can't specify expanded ccs timing/power model for some cells in the library, while compact ccs timing/power model for other cells.

WHAT NEXT

Keep only one ccs timing/power model in the library.

EXAMPLES

```
library(name) {
  ...

  cell(cell_name1) {
    pin(pin_name) {
timing() {
    output_current_rise() {
      vector("CT3") {
```

```
...
      }
      ...
    }
    output_current_fall() {
      vector("CT3") {
...
      }
      ...
    }
}
    }
  }
  cell(cell_name2) {
    pin(pin_name) {
timing() {
    compact_ccs_rise("LTT3") {
      values("..."..., "...");
    }
    compact_ccs_fall("LTT3") {
      values("..."..., "...");
    }
}
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 1, Un-Compatible CCS timing data specified in timing arc.(LBDB-763)
```

LBDB-764 (error) Redundant base_curves group '%s' with '%s' type defined in library.

DESCRIPTION

Since the compressed ccs data (for the time being, it only support compressed ccs timing) is consumed by PT, to ensure the performance of PT, guarantee the ccs accuracy and ease the implementation of PT support and implementation, we only support one base curve group with specific base curve type.

WHAT NEXT

Remove the base_curves group or combine same base curve type groups into one base_curves group if possible. Leave only one base_curves group with the base curve type.

EXAMPLES

```
library(name) {
  ...

  base_curves(bct1) {
    base_curve_type : ccs_timing_half_curve;
    curve_x ("0.1, 0.5, 0.9");
    curve_y (1, "0.2, 0.5, 0.8");
    ...
  }
  base_curves(bct2) {
    base_curve_type : ccs_timing_half_curve;
    curve_x ("0.1, 0.5, 0.9");
    curve_y (1, "0.33, 0.55, 0.88");
    ...
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 165, Redundant base_curves group 'bct2' with 'ccs_timing_half_curve' ty
pe defined in library.(LBDB-764)
```

LBDB-765 (error) Bad peak_voltage value '%g' is specified in '%s',
Legal vale should be in range of [%g, %g].

DESCRIPTION

peak_voltage is one of six parameters to model compact ccs timing base curve. In [va_]compact_ccs_rise/fall group, the peak_voltage values should less than Vdd of this port.

Note that the ways to define VDD are different between pg pin library, power-rail library, non-pg pin library. details may need to refer to application notes for pg pin supporting.

WHAT NEXT

According the rule above, correct the peak_voltage value.

EXAMPLES

```
library(name) {
  ...
```

```
  operating_conditions(typical) {
    process: 1;
    temperature: 25;
    voltage: 1.0;
    tree_type: balanced_tree
  }
  default_operating_conditions : typical;

  base_curves (ctbct1){
    base_curve_type : ccs_timing_half_curve;
    curve_x("0.2, 0.5, 0.8");
    curve_y(1, "0.8, 0.5, 0.2");
    curve_y(2, "0.75, 0.5, 0.35");
    curve_y(3, "0.85, 0.5, 0.15");
    curve_y(4, "0.85, 0.5, 0.15");
  }
  compressed_lut_template(LTT3) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : curve_parameters;
    index_1 ("0.1, 0.2");
    index_2 ("1.0, 2.0");
    index_3 ("init_current, peak_current, peak_voltage, peak_time, left_id, right_i
d");
    base_curves_group: "ctbct1";
  }

  cell(cell_name) {
    pin(pin_name) {
timing() {
    compact_ccs_rise("LTT3") {
      values("0.1, 0, 0.6, 0.8, 1, 3",
     "0.15, 1.55, 0.65, 0.85, 2, 4",
     "0.2, 0.6, 0.7, 0.9, 3, 2", <HardSpace
                 "0.25, 0.65, 0.75, 0.95, 4, 1");
    } /* end of compressed_ccs_rise */
}
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 1163, Bad peak_voltage value ’1.55’ is specified in ’compact_ccs_rise’,
Legal value should be in range of [0, 1.0].(LBDB-765)
```

SEE ALSO

LBDB-753

LBDB-766 (warning) The '%s' attribute of %s '%s' overwrites the value specified in the '%s' attrbiute.

DESCRIPTION

This message indicates that the latest value overwrites the previous value defined for the same attribute.

WHAT NEXT

Make sure that it is what have been expected.

EXAMPLE MESSAGE

```
Error: Line 100, The 'retention_pin' attribute of pin 'A' overwrites the value spec
ified
in the 'map_to_logic' attrbiute. (LBDB-766)
```

LBDB-767 (error) No mandatory attribute '%s' defined in sensitization group '%s'.

DESCRIPTION

sensitization group is to describe the complete state patterns (by vector attributes) for a specific list of pins (by pin_names attribute). vector and pin_names are mandatory attributes in the group.

WHAT NEXT

According to message, add pin_names or vector to make the sensitization group complete.

EXAMPLES

```
library(name) {
  ...
  sensitization (my_sensitization){
    pin_names("A, B, Y");
  }

  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 11, No mandatory attribute 'vector' defined in sensitization group 'my_
sensitization'.(LBDB-767)
```

LBDB-768 (error) Duplicate pin name '%s' specified in '%s'.

DESCRIPTION

This error is issued when duplicate pin name specified in sensitization group pin_names, or cell/timing group pin_name_map attribute. Pin names in the attribute are used to generate stimuli from sensitization group for timing arc.

WHAT NEXT

Correct the duplicate pin name definition, if the number of pin is changed because of the fix, other sensitization related attributes may also need to be updated.

EXAMPLES

```
library(name) {
  ...
  sensitization (my_sensitization){
    pin_names("A, B, B, Y");
    vector (0, "0 0 0 0");
    vector (1, "0 0 0 1");
    ...
  }

  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 12, Duplicate pin name 'B' specified in 'pin_names'.(LBDB-768)
```

LBDB-769 (error) %s id (%d) specified sensitization vector.

DESCRIPTION

This error is issued when duplicate or negative vector id specified in vector attribute. The vector attribute is composed by: vector(vector_id, vector_string); The vector id should greater than or equal to zero, and unique in current sensitization group.

WHAT NEXT

Correct the vector id in the vector attribute, according to the rule above.

EXAMPLES

```
library(name) {
  ...
  sensitization (my_sensitization){
    pin_names("A, B, C, Y");
    vector (0, "0 0 0 0");
    vector (1, "0 0 0 1");
    vector (1, "0 0 1 1");
    vector (-1, "0 0 1 0");
    ...
  }

  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 14, Duplicate id (1) specified in sensitization vector.(LBDB-769)
Error: Line 15, Negative id (-1) specified in sensitization vector.(LBDB-769)
```

LBDB-770 (error) No pin_names attribute defined before the vector.

DESCRIPTION

In sensitization group, pin_names attribute should be declared before all vectors. The error is issued when processing vector but find no pin_names attribute defined before in the sensitization group.

WHAT NEXT

Add pin_names attribute if it’s missing, or reorder the pin_names attribute to the first declaration in the sensitization group.

EXAMPLES

```
library(name) {
  ...
  sensitization (my_sensitization){
    vector (0, "0 0 0 0");
    pin_names("A, B, C, Y");
    vector (1, "0 0 0 1");
```

```
    vector (2, "0 0 1 0");
    vector (3, "0 0 1 1");
    ...
  }

  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 13, No pin_names attribute defined before the vector.(LBDB-770)
```

LBDB-771 (error) Number of elements in the vector string (%d) is different from number of pin (%d).

DESCRIPTION

This error is issued when the number of elements in vector string is different the number of pins defined in pin_names attribute. The vector attribute is composed by: vector(vector_id, vector_string);

WHAT NEXT

Correct the vector string in the vector attribute, make it’s elements number equal to number of pin in pin_names.

EXAMPLES

```
library(name) {
  ...
  sensitization (my_sensitization){
    pin_names("A, B, C, Y");
    vector (0, "0 0 0 0");
    vector (1, "0 0 0 1");
    vector (2, "0 0 1 0");
    vector (3, "0 1 1");
    ...
  }

  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 17, Number of elements in the vector string (3) is different from numbe
r of pins (4).(LBDB-771)
```

LBDB-772 (error) Number of pins (%d) in the %s pin_name_map is different from that (%d) in sensitization master '%s'.

DESCRIPTION

This error is issued when run into following situations: 1. Number of pin in cell->pin_name_map is different from that in cell->sensitization_master->pin_names. 2. Number of pin in timing->pin_name_map is different from that in timing->sensitization_master->pin_names. 3. When there is timing->pin_name_map defined, but there is only cell->sensitization_master attribute, Number of pin in timing->pin_name_map is different from that in cell->sensitization_master->pin_names.

When there is pin_name_map defined in cell or timing, pins in the attribute is used to generate stimuli for characterization, instead of pin_names in sensitization master. but the number of pins should be the same, otherwise vectors in the sensitization_master can not be mapped to these pins properly.

WHAT NEXT

Correct the vector string in the vector attribute, make it's elements number equal to number of pin in pin_names.

EXAMPLES

```
library(name) {
  ...
  sensitization (my_sensitization){
    pin_names("A, B, C, Y");
    vector (0, "0 0 0 0");
    vector (1, "0 0 0 1");
    vector (2, "0 0 1 0");
    vector (3, "0 0 1 1");
    ...
  }

  cell (my_cell) {
    sensitization_master : my_sensitization;
    pin_name_map("A, B, Z");
    pin (A) {
...
    }
    ...
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 1170, Number of pins (3) in the cell pin_name_map
is different from that (4) in sensitization master 'my_sensitization'.(LBDB-772)
```

LBDB-773 (error) Illegal pin name '%s' specified in %s level sensitization attribute.

DESCRIPTION

This error is issued when pin name specified in cell/timing level sensitizaiotn attribute is an illegal(undefined) pin in the cell: This screener rule checks following pin names: 1. pin names specified in cell->pin_name_map attribute. 2. when there is no cell->pin_name_map, pin_names in cell->sensitization_master. 3. pin names in timing->pin_name_map attribute. 4. when there is no timing->pin_name_map, pin_names in timing->sensitization_master.

WHAT NEXT

Check pin names in the sensitization attributes(pin_name_map, or pin_names in sensitization_master), make sure all pin names are real pin in the cell.

EXAMPLES

```
library(name) {
  ...
  sensitization (my_sensitization){
    pin_names("A, B, C");
    vector (0, "0 0 0");
    vector (1, "0 0 1");
    vector (2, "0 1 0");
    vector (3, "0 1 1");
    ...
  }

  cell (my_cell) {
    sensitization_master : my_sensitization;
    pin_name_map("A, B, Z");
    pin (A) {
...
    }
    pin (B) {
...
    }
    pin (Y) {
...
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 1170, Illegal pin name 'Z' specified in cell level sensitization attrib
ute.(LBDB-773)
```

LBDB-774 (error) Incomplete sensitization info in the timing arc.

DESCRIPTION

This error is issued when there is wave_rise/wave_fall attribute defined in the timing group, but none of following attributes found: 1. pin_name_map attribute in current timing group. 2. sensitization_master attribute in current timing group. 3. pin_name_map attribute in current cell. 2. sensitization_master attribute in current cell.

Since there is no way to get the pin names for the wave_rise/wave_fall, the sensitization information for the timing is incomplete.

WHAT NEXT

Define pin_name_map or sensitization_master attribute either in the timing arc or in the cell, make sure the sensitization information in this timing group is complete.

EXAMPLES

```
library(name) {
  ...
  sensitization (my_sensitization){
    pin_names("A, B, C");
    vector (0, "0 0 0");
    vector (1, "0 0 1");
    vector (2, "0 1 0");
    vector (3, "0 1 1");
    ...
  }

  cell (my_cell) {
    ...
    pin (A) {
timing() {
    wave_rise (1, 3);
    wave_fall (2, 0);
    /* other timing arc data */
}
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 1170, Incomplete sensitization info in the timing arc.(LBDB-774)
```

LBDB-775 (warning) No sensitization_master defined, sensitization vector is derived from vector id in the timing arc.

DESCRIPTION

This warning is issued when there is wave_rise/wave_fall attribute defined in the timing group, But no sensitization_master attribute defined either in the timing group or current cell.

This is a simplified usage model of sensitization, that sensitization vector used to get from sensitization group by vector id, but is derived from vector id and number of pin in pin_name_map by binary scale directly in such cases.

Example: timing() { pin_name_map("A, B, C, Z"); wave_rise (5, 8, 15); }

Here ’5’ implies vector string of "0 1 0 1", ’8’ implies vector string of "1 0 0 0", and so on.

WHAT NEXT

If this is what the users wanted, just ignore this warning. otherwise, specify valid sensitization_master attribute in the timing group or current cell.

EXAMPLES

```
library(name) {
  ...

  cell (my_cell) {
    ...
    pin (A) {
timing() {
    pin_name_map("A, B, Y");
    wave_rise (1, 3);
    wave_fall (2, 0);
    /* other timing arc data */
}
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Warning: Line 1170, No sensitization_master defined, sensitization vector is derive
d from vector id in the timing arc.(LBDB-775)
```

LBDB-776 (error) Vector id (%d) in '%s' is undefined in sensitization group '%s'.

DESCRIPTION

When there is sensitization master defined for the timing arc, Vector id specified in wave_rise and wave_fall should be predefined in the sensitization group, otherwise, this error is issued.

WHAT NEXT

Modify vector id in the wave_rise/wave_fall, make sure every vector id is predefined in sensitization master group.

EXAMPLES

```
library(name) {
  sensitization (my_sensitization){
    pin_names("A, B, C");
    vector (0, "1 0 0");
    vector (1, "0 0 1");
    vector (2, "1 1 0");
    vector (3, "0 1 1");
  }
  ...

  cell (my_cell) {
    ...
    pin (A) {
timing() {
    sensitization_master : my_sensitization;
    pin_name_map ("A, B, Y");
    wave_rise (1, 3);
    wave_fall (2, 4);
    /* other timing arc data */
}
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 1181, Vector id (4) in 'wave_fall' is undefined in sensitization group
'my_sensitization'(LBDB-776)
```

LBDB-777 (error) Vector id (%d) for implied vector string in '%s' is out of range (0~%d).

DESCRIPTION

When there is no sensitization master defined either in the timing group or current cell, Vector string is implied by vector id and number of pin in pin_name_map. So the vector id should greater than or equal to zero, and less than 2^(number of pin in pin_name_map).

For example: timing() { pin_name_map("A, B, C, Z"); wave_rise (5, 8, 17); } Here number of pin in pin_name_map is 4, the vector id should < (2^4 = 16), so the vector id = 17 is out of range, and is not allowed.

WHAT NEXT

Modify vector id in the wave_rise/wave_fall, make sure every vector id is in the legal range.

EXAMPLES

```
library(name) {
  ...
  cell (my_cell) {
    ...
    pin (A) {
timing() {
    sensitization_master : my_sensitization;
    pin_name_map ("A, B, Y");
    wave_rise (1, 7);
    wave_fall (2, 8);
    /* other timing arc data */
}
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 1181, Vector id (8) for implied vector string in 'wave_fall' is out of
range (0~7)(LBDB-777)
```

LBDB-778 (error) index (%d) specified in '%s' is out of range (1~%d).

DESCRIPTION

The wave_rise_sampling_index/wave_fall_sampling_index is to define from which transition, (instead of default last transition) to the transition of the output pin, the delay is measured.

If the number of elements in wave_rise/wave_fall is N, then The index value should between (1 ~ N-1).

WHAT NEXT

Modify sampling index accordingly, make sure it's in the legal range.

EXAMPLES

```
library(name) {
  ...
  cell (my_cell) {
    ...
    pin (A) {
timing() {
    sensitization_master : my_sensitization;
    pin_name_map ("A, B, Y");
    wave_rise (1, 4, 7);
    wave_fall (2, 5, 8);
    wave_rise_sampling_index : 3;
    /* other timing arc data */
}
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 1181, index (3) specified in 'wave_rise_sampling_index' is out of range
 (1~2)(LBDB-778)
```

LBDB-779 (error) Number of elements (%d) specified in '%s' is

out of range (1~%d).

DESCRIPTION

The wave_rise_timing_interval/wave_fall_timing_interval attributes are for special cases that customers want to control the time interval between transitions. which is used to characterize some special-purpose cells and pessimistic timing characterization.

If the number of elements in wave_rise/wave_fall is N, then Number of elements in these two attributes should between (1 ~ N-1);

WHAT NEXT

Modify the wave_rise_timing_interval/wave_fall_timing_interval attribute values, accordingly to the rule above.

EXAMPLES

```
library(name) {
  ...
  cell (my_cell) {
    ...
    pin (A) {
timing() {
    sensitization_master : my_sensitization;
    pin_name_map ("A, B, Y");
    wave_rise (1, 4, 7);
    wave_fall (2, 5, 8);
    wave_rise_timing_interval(0.0, 0.5, 1.0);
    /* other timing arc data */
}
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 1181, Number of elements (3) specified in 'wave_rise_sampling_index' is
 out of range (1~2)(LBDB-779)
```

LBDB-780 (error) The '%s' %s is not %s '%s' %s.

DESCRIPTION

This error message occurs when you specify an invalid 'std_cell_main_rail' pg_pin in

a level shifter not satisfying one of the following constraints: - the pg_pin must be a ’primary_power’ or ’primary_ground’ pg_pin. - if the pg_pin is ’primary_power’, the pg_pin must be specified as the "related_power_pin" of one of the signal pins of the level shifter. - if the pg_pin is ’primary_ground’, the pg_pin must be specified as the "related_ground_pin" of one of the signal pins of the level shifter.

As shown in the following example, the ’VDD’ pg_pin is invalid because it is not a ’primary power’ pg_pin.

```
     cell(ls) {
       is_level_shifter : true;

       pg_pin(VDD) {
       voltage_name : VDDL;
      pg_type : backup_power;

      std_cell_main_rail : true;
       }
       ...
     }
```

```
   Error: Line 84, The ’VDD’ pg_pin is not a ’primary_power’ pg_pin. (LBDB-780)
```

WHAT NEXT

Modify the cell accordingly to satisfy the constraints.

LBDB-781 (error) The timing arc with feed_through_type ’%s’ %s specify the CCS Timing Current waveform vectors.

DESCRIPTION

The timing arc with feed_through_type attribute must satisfy the following requirements: 1. if the feed_through_type attribute is "short", then the timing arc must not have CCS Timing current waveform vectors. 2. if the feed_through_type attribute is "wire" or "gate", then the timing arc must have CCS Timing current waveform vectors.

WHAT NEXT

Check the timing arc and make the correction accordingly.

EXAMPLES

```
pin(Z) {
  direction : output;
  timing() {
    /* no ccs information defined in the timing arc */
```

```
    feed_through_type : wire;
    ...
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 144, The timing arc with feed_through_type 'short' cannot specify the
CCS Timing Current waveform vectors. (LBDB-781)
```

LBDB-782 (error) The pin '%s' should be an 'inout' pin because of the associated timing arc with feed_through_type attribute.

DESCRIPTION

The timing arc with feed_through_type attribute can only be specified between inout pins.

WHAT NEXT

Check the timing arc and make the correction accordingly.

EXAMPLES

```
pin (A) {
  direction : output;
  ...
}
pin(Z) {
  direction : output;
  timing() {
          feed_through_type : short;
    ...
    related_pin : "A";
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 144, The pin 'A' should be an 'inout' pin because of the associated
timing arc with feed_through_type attribute. (LBDB-782) Error: Line 148, The pin 'Z'
should be an 'inout' pin because of the associated timing arc with feed_through_type
attribute. (LBDB-782)
```

LBDB-783 (error) In cell '%s', the %s timing arc from pin '%s' to '%s' with feed_through_type '%s'
 does not have the required timing arc from pin '%s' to '%s' of the same timing_type
 , timing_sense and feed_though_type.

DESCRIPTION

The timing arc with feed_through_type attribute 'short' or 'wire' must have the relative backward timing arc with the same timing_type and feed_through_type for the same cell.

WHAT NEXT

Check the timing arcs and make the correction accordingly.

EXAMPLES

```
     cell(T) {
...
pin(Z) {
  direction : output;
  /* no timing arc Z-
>A with timing_type = combinational and feed_through_type= wire exists in the cell
T */
  timing() {
    timing_type : combinational;
    feed_through_type : wire;
    ...
    related_pin "A";
  }
}
...
     }
```

EXAMPLE MESSAGE

```
Error: Line 144, In cell 'T', the combinational timing arc from pin 'A' to 'Z' with
feed_through_type '%s'
      does not have the required timing arc from pin 'Z' to 'A' of the same
timing_type , timing_sense and feed_though_type. (LBDB-783)
```

LBDB-784 (error) The %s value of the '%s' attribute is %g,

which is %s the required value %g.

DESCRIPTION

The minimum/maximum value of the attribute is less/greater than the required value.

WHAT NEXT

Check the library source file and correct the problem.

EXAMPLES

```
  ...
  current_unit : "1mA" ;
  ...
  dc_current (ccsn_dc_29x29) {
index_1 ("...");
index_2 ("...");
/* current unit = 1mA, and the max value = 0.005 */
values ("0.0005, ...., 0.00091);
  }
```

EXAMPLE MESSAGE

```
Error: Line 35, The maximum value of the 'values' attribute is 0.0005,
which is less than required value 0.001. (LBDB-784)
```

LBDB-785 (warning) The '%s' attribute is not defined in the library.
Using %f as the default value.

DESCRIPTION

You receive this message because the relative attribute is not defined in the library, so LC will create the attribute with the predefined default value.

WHAT NEXT

Examine the library source file, and add the correct value for the attribute.

EXAMPLE MESSAGE

```
Warning: Line 85, The 'nom_voltage' attribute is not defined in the library. Using 5
```

as the default value. (LBDB-785)

LBDB-786 (error) The attribute valus is not a switch pin.

DESCRIPTION

The value of related_switch_pin must be referring to either a switch pin or an internal pin as defined below.

switch pin : switch_pin attribute is set to "true" within a pin. internal pin : related_pin attribute is referred to a switch pin.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
dc_current (ccsn_dc_29x29) {
   related_switch_pin : D;
   ...
}
pin(CTL) { /* this is a switch pin as switch_pin is set to "true" */
   capacitance : 0.5;
   direction : input;
   switch_pin : true;
   ...
}
pin(int_1) { /* this is an internal pin, which refers to a switch pin by
                related_pin attribute */
   direction : internal;
   timing () {
     related_pin : CTL;
     ...
   }
   ...
}
pin(D) {
   capacitance : 0.5;
   direction : input;
   ...
 }
```

In this case, related_switch_pin is pointing to pin "D", which is not either an internal pin or a switch pin. The way to correct it is to specify related_switch_pin to either pin "CTL" or pin "int_1".

EXAMPLE MESSAGE

```
Error Line 272, The attribute valus is not a switch pin. (LBDB-786)
```

LBDB-787 (error) Cell(%s): The ’internal_node’ in the ’%s’ port can’t be specified because no statetable is allowed in generic type of clock gating integrated cell.

DESCRIPTION

If attribute ’clock_gating_integrated_cell’ is generic, then no statetable is allowed. ’internal_node’ attribute must match one of the internal node names in statetable. Since there is no statetable is allowed, there is no ’internal_node’ attribute can be specified in a port, either.

WHAT NEXT

Remove the internal_node attribute to fix the problem.

EXAMPLES

```
cell(ldbd-787) {
    ...
  cell_leakage_power : 0.023529479 ;
  clock_gating_integrated_cell : "generic" ;
    ...

  pin(Q) {
    direction : internal;
    internal_node : "Q1";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.34;
      intrinsic_fall : 1.54;
      rise_resistance : 0.0718;
      fall_resistance : 0.0347;
      related_pin : "CP";
    }
  }
}
```

In this case, Q1 in internal_node attribute shall not be specified because there is no statetable in the cell.

EXAMPLE MESSAGE

```
Error: Line 139, Cell(lbdb-787): The ’internal_node’ in the ’Q’ port
```

can’t be specified because no statetable is allowed in generic type of clock gating integrated cell. (LBDB-787)

LBDB-788 (warning) No default ’%s" group defined in ’%s’.

DESCRIPTION

This warning is issued when there is some default group is missing in library, but no default can be assumed to it.

For example, if there is no default driver waveform specified, This warning will be reported.

WHAT NEXT

Check the library source file, add default group.

EXAMPLE MESSAGE

Warning Line 10, No default ’normalized_driver_waveform" group defined in ’library’ .(LBDB-788)

LBDB-789 (warning) The ’%s’ attribute in the ’%s’ table has less than %d ’%s" points,that is point between %g to %g.

DESCRIPTION

The values of the corresponding attribute has no enough type of points.

For example, the normalized voltage points for driver waveform need at lease 1 start points(0~0.05) and end points(0.95~1.0) for accuracy.

WHAT NEXT

Check the library source file, add some example points for the attribute.

EXAMPLES

```
normalized_driver_waveform (dw01) {
   index_1 ("1.0");/* input net transition */
   index_2 ("0.1, 0.3, 0.5, 0.7, 0.9"); /* normalized voltage*/
   ...
}
```

In this case, the index_2 of normalized_driver-waveform is normalized_voltage, It would be better to supply at leat one start points and end points for accuracy purpose.

EXAMPLE MESSAGE

Warning Line 27, The ’index_2’ attribute in the ’normalized_driver_waveform’ table has less than 1 ’start" points, that is between ’0’ to ’0.05’. (LBDB-789)
Warning Line 27, The ’index_2’ attribute in the ’normalized_driver_waveform’ table has less than 1 ’end" points, that is between ’0.95’ to ’1.0’. (LBDB-789)

LBDB-790 (error) ’%s’ only allows single %s pin name.

DESCRIPTION

Only one single pg pin name can be specified in intrinsic_resistance, intrinsic_capacitance and pg_current or only one single pin name can be specified in gate_leakage.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
  pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
     pg_type : backup_power;
  }
  pg_pin(G1) {
     voltage_name : GND1;
     pg_type : primary_ground;
  }
  pg_pin(G2) {
     voltage_name : GND2;
     pg_type : backup_ground;
  }

 pin(A1) {
  direction : input;
  ...
   }
 pin(A2) {
  direction : input;
  ...
```

```
  }
pin(A3) {
 direction : input;
 ...
  }
pin(ZN1) {
 direction : output;
 ...
}
pin(ZN) {
 direction : output;
 ...
}
...
 dynamic_current() {
   when : "A1";
   related_inputs : "A2 A3";
   related_outputs : "ZN ZN1";
   typical_capacitances(0.3 0.4);
   switching_group() {
     input_switching_condition(fall);
     output_switching_condition(rise fall);
     pg_current(V2 G1) {
       vector(test_2) {
         reference_time : 193.2;
         index_output : "ZN1";
         index_1("15.1");
         ...
        }
     ...
    }
   ...
  }

 leakage_current() {
    pg_current(V1) {
      value : 4.5;
    }
    pg_current(G1 G2) {
      value : -4.5;
    }
   ...
    gate_leakage(A2 A3) {
      input_high_value : 1.0;
      input_low_value : -10.0;
    }
    gate_leakage() {
      input_high_value : 3.0;
      input_low_value : -40.0;
    }


 }
 intrinsic_parasitic() {
   when : "A1 & A2 & ZN";
```

```
    intrinsic_resistance(G1 G1) {
       related_output : "ZN";
       value : 9.0;
    }
    intrinsic_resistance(G1) {
       related_output : "ZN1";
       value : 62.2;
    }
    intrinsic_capacitance(G2 G2) {
       value : 31.47;
    }
  }
```

In this case, the pg_current within switching_group has two pg pins, V2 and G1, which is wrong. The pg_current within leakage_current has two pg pins, G1 and G2, which is wrong. The intrinsic_resistance has two pg names, G1 and G1, which is wrong. The intrinsic_capacitance has two pg names, G2 and G2, which is wrong. The first gate_leakage has two pin names A3 and A2, which is wrong, and the second gate_leakage has no name there, which is wrong, too. You might want to change all of them to one PG or pin name to avoid the error.

EXAMPLE MESSAGE

```
Error Line 272, 'pg_current' only allows single pg pin name. (LBDB-790)
Error Line 222, 'gate_leakage' only allows single pin name. (LBDB-790)
```

LBDB-791 (error) pg_pin group is required for ccs power cell.

DESCRIPTION

If the cell is a ccs power cell, which contains dynamic_current, leakage_current or intrinsic_parasitic, then pg_pin group is required.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell (AND3) {
  ...
  power_cell_type : stdcell;
  dynamic_current() {
    when : "A1";
    related_inputs : "A2 A3";
    related_outputs : "ZN ZN1";
    typical_capacitances(0.3 0.4);
    switching_group() {
```

```
    ...
    }
    ...
  } ...
}
```

In this case, cell, AND3, is a ccs power cell. The pg_pin must be specified within cell to fix the error as shown below : cell (AND3) { pg_pin(V1) { voltage_name : VDD1; pg_type : primary_power; } pg_pin(V2) { voltage_name : VDD2; pg_type : backup_power; } pg_pin(G1) { voltage_name : GND1; pg_type : primary_ground; } pg_pin(G2) { voltage_name : GND2; pg_type : backup_ground; }

power_cell_type : stdcell; dynamic_current() { ...

EXAMPLE MESSAGE

Error Line 272, pg_pin group is required for ccs power cell. (LBDB-791)

LBDB-792 (error) leakage current in simplified format must be >= 0.

DESCRIPTION

If there is no pg_current within leakage_current group, we defined that as simplified format. Please refer to users guide for details.

If leakage_current is in simplifed format, then the value of leakage current must be zero or positive floating number.

The same rule is applied to va_leakage_current.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell (OR2) {
  pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(G1) {
     voltage_name : GND1;
     pg_type : primary_ground;
  }
  leakage_current() {
     when : "A1 & !A2 & ZN";
```

```
    value : 3.1;
  }
  leakage_current() {
    when : "A1 & !A2 & !ZN";
    value : 0.0;
  }
  leakage_current() {
    /* default state */
    value : -8.1;
  }
  ...
}
```

In this case, leakage current -8.1 is not allowed. The value must be >= 0 in simplified format.

EXAMPLE MESSAGE

Error Line 272, leakage current in simplified format must be >= 0. (LBDB-792)

LBDB-793 (error) Name specified in '%s' is not a valid %s pin.

DESCRIPTION

You got this message because an invalid PG or signal pin is used.

The pin name specified in intrinsic_capacitance, intrinsic_resistance, or pg_current group must be referred to a valid PG pin defined in cell, and a pg name is required for these groups.

The pin name specified in gate_leakage group must be referred to a valid signal pin defined in cell, and a pin name is required for gate_leakage.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell (AND3) {
  ...
  pg_pin(V1) {
    voltage_name : VDD1;
    pg_type : primary_power;
  }
  pg_pin(V2) {
    voltage_name : VDD2;
    pg_type : backup_power;
  }
  pg_pin(G1) {
```

```
    voltage_name : GND1;
    pg_type : primary_ground;
 }
 pg_pin(G2) {
    voltage_name : GND2;
    pg_type : backup_ground;
 }
...
dynamic_current() {
   when : "A1";
   related_inputs : "A2 A3";
   related_outputs : "ZN ZN1";
   typical_capacitances(0.3 0.4);
   switching_group() {

     input_switching_condition(fall);
     output_switching_condition(rise fall);

     pg_current(V5) {     /* error */
       vector(test_2) {
       ...
     }
     pg_current() {       /* error */
     ...
   ...
 }
  ...
  leakage_current() {
    when : "A1 & !A2 | ZN";
    pg_current(V5) {      /* error */
      value : 4.5;
    }
    pg_current(V2) {
      value : 4.5;
    }
    pg_current(G2) {
      value : -3.5;
    }
    pg_current() {       /* error */
      value : 4.5;
    }
 }
 ...
 intrinsic_parasitic() {
   when : "A1 & A2 & ZN";
   intrinsic_resistance() {    /* error */
      related_output : "ZN";
      value : 9.0;
   }
   intrinsic_resistance(V5) {   /* error */
      related_output : "ZN1";
      value : 62.2;
   }
   intrinsic_capacitance(G2) {
      value : 31.47;
```

```
    }
    intrinsic_capacitance() {    /* error */
       value : 31.47;
    }
    intrinsic_capacitance(V5) {  /* error */
       value : 31.47;
    }
    ...
  }
}
```

Please check the lines marked as 'error'. For these lines, they are either refers to an empty pg name, or refers to a invalid pg pin name, V5. Both are wrong. To fix the problems, please change V5 to a valid pg pin like V1, and also give a valid pg name for the empty ones.

EXAMPLE MESSAGE

Error Line 272, Name specified in 'pg_current' is not a valid PG pin. (LBDB-793)

LBDB-794 (error) The value of pg_current must be '%s'.

DESCRIPTION

This is rule for leakage_current groups. If the PG pin is a power or internal ground pin, then the value of leakage current must be either zero or positive floating number. If the PG pin is a ground or internal power pin, then the value of leakage current must be either zero or negative floating number.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell (AND3_1) {
  pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
     pg_type : backup_power;
  }
  pg_pin(V3) {
     voltage_name : VDD3;
     pg_type : internal_ground;
  }
  pg_pin(G1) {
     voltage_name : GND1;
```

```
      pg_type : primary_ground;
   }
   pg_pin(G2) {
      voltage_name : GND2;
      pg_type : backup_ground;
   }
   pg_pin(G3) {
      voltage_name : GND3;
      pg_type : internal_power;
   }
   leakage_current() {
      when : "A1 & !A2 & ZN";
      pg_current(V1) {
        value : -4.5;
      }
      pg_current(V2) {
        value : -4.5;
      }
      pg_current(G2) {
        value : 4.5;
      }
      pg_current(V3) {
        value : -4.5;
      }
      pg_current(G1) {
        value : 4.5;
      }
      pg_current(G3) {
        value : 4.5;
      }
   }
}
```

In this case, V1, V2 and V3 must be positive or zero, and G1, G2 and G3 must be negative or zero based on the pg_type.

EXAMPLE MESSAGE

Error Line 272, The value of pg_current must be '>=0'. (LBDB-794)

LBDB-795 (error) Only one PG pin can be omitted in %s group.

DESCRIPTION

All the PG pins except one shall be specified in leakage_current. This rule is also applied to va_leakage_current group.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell (AND3) {

  pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
     pg_type : backup_power;
  }
  pg_pin(G1) {
     voltage_name : GND1;
     pg_type : primary_ground;
  }
  pg_pin(G2) {
     voltage_name : GND2;
     pg_type : backup_ground;
  }
  leakage_current() {
     when : "A1 & A2 & !ZN";
     pg_current(V1) {
       value : 4.5;
     }
     pg_current(V2) {
       value : 4.5;
     }
  }
}
```

There are 4 pg pins in the cell AND3, and based on rule only one pg pin can be omitted in leakage_current group. Meaning you have to specify at least three pg pins for this case. However, there are only two pg pins (V1 and V2) specified in leakage_current. To fix the problem, please specify at least one of ground pins for leakage_current as shown below.

```
leakage_current() { when : "!A1 & A2 & ZN"; pg_current(V1) { value : 4.5; }
pg_current(V2) { value : 4.5; } pg_current(G2) { value : -4.5; } }
```

EXAMPLE MESSAGE

```
Error Line 272, Only one PG pin can be omitted in leakage_current group. (LBDB-795)
```

LBDB-796 (error) The leakage current of all PG pins and gate leakage current of all input/inout pins must be summed up to

zero.

DESCRIPTION

This rule applies to leakage_current and va_leakage_current groups if leakage current of all PG pins are specified.

If no gate_leakage are specified, the leakage current of all PG pins should add up to zero. If gate_leakage of all input/inout pins are specified, the leakage current of all PG pins and gate leakage current of all input/inout pins should add up to zero.

The absolute total of leakage current must add up to zero with a tolerance of 1.0e-6 * (total of absolute values of leakage current). The tolerance is calculated as follows:

$$0 <= \frac{| \text{total of leakage current} |}{\text{total of } | \text{leakage current} |} <= 1.0e\text{-}06$$

If |total of leakage current| * (current_unit / Amp) < 1.0e-10, this message won't be issued because the absolute current value is too small.

WHAT NEXT

Check the library source file and make the necessary correction.

EXAMPLES

In the example below, the total of leakage current is -0.000028. Based on the rule above, it will be like | -0.000028 | / 27.000028 = 1.03 * 1.0e-6 The result is greater than 1.0e-6. To fix the problem, we can change the G3 current to -4.500020.

```
cell (AND3_1) {
  pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
     pg_type : backup_power;
  }
  pg_pin(V3) {
     voltage_name : VDD3;
     pg_type : internal_ground;
  }
  pg_pin(G1) {
     voltage_name : GND1;
     pg_type : primary_ground;
  }
  pg_pin(G2) {
     voltage_name : GND2;
```

```
      pg_type : backup_ground;
    }
    pg_pin(G3) {
      voltage_name : GND3;
      pg_type : internal_power;
    }
    leakage_current() {
      when : "A1 & A2 & ZN";
      pg_current(V1) {
        value : 4.5;
      }
      pg_current(V2) {
        value : 4.5;
      }
      pg_current(G2) {
        value : -4.5;
      }
      pg_current(V3) {
        value : 4.5;
      }
      pg_current(G1) {
        value : -4.5;
      }
      pg_current(G3) {
        value : -4.500028;
      }
  }
```

EXAMPLE MESSAGE

```
Error: Line 246, The leakage current of all PG pins and gate leakage
current of all input/inout pins must be summed up to zero. (LBDB-796)
```

LBDB-797 (warning) The leakage_current is in wrong format.

DESCRIPTION

Please also refer to LBDB-798.

The leakage_cuurent only allow either regular or simplified format. The regular format shall contain pg_current group, and the simplified format shall contain value attribute.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
   leakage_current() {
```

```
    when : "A1 & !A2 & !ZN";
  }
```

In this case, leakage_current is neither in regular nor in simplified format. To avoid the warning, please change it to either of followings :

simplified format : leakage_current() { when : "A1 & !A2 & !ZN"; value : 0.0; }

regular format : leakage_current() { when : "A1 & !A2 & !ZN"; pg_current(V1) { value : 0.0; } }

EXAMPLE MESSAGE

Warning Line 272, The leakage_current is in wrong format. (LBDB-797)

LBDB-798 (error) The leakage current groups have mix format.

DESCRIPTION

Please also refer to LBDB-797.

The leakage_cuurent only allow either regular or simplified format. The regular format shall contain pg_current group, and the simplified format shall contain value attribute. And, two formats can not be mixed.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell (test) { ... leakage_current() { pg_current(V1) { value : 4.5; } pg_current(G1) { value : -4.5; } pg_current(G2) { value : -14.5; } pg_current(V2) { value : 14.5; } } leakage_current() { when : "!A1 & !A2 & ZN"; value : 0.0; } ... }
```

In this case, first leakage_current is in regular format and second leakage_current is in simplified format, which is wrong. Two formats can not be mixed under the same cell.

EXAMPLE MESSAGE

Error Line 272, The leakage current groups have mix format. (LBDB-798)

LBDB-799 (error) The multiple PG pins can not be simplified format

in %s.

DESCRIPTION

The simplified format in leakage_current means no pg_current group specified under this leakage_current. If a cell have more than one power or ground pin, then we can not use simplified format for leakage_current.

The rule is also applied to va_leakage_current.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell (test) {
  pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(G1) {
     voltage_name : GND1;
     pg_type : primary_ground;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
     pg_type : backup_ground;
  }
  leakage_current() {
     when : "A1 & !A2 | ZN";
     value : 3.1;
  }
 ...
}
```

In this case, the cell 'test' have more than one power pin, and leakage_current is in simplified format, which is wrong. To fix the problem, please change the simplified format to regular format as shown below.

```
leakage_current() { when : "A1 & !A2 | ZN"; pg_current(V1) { value : 1.1; }
pg_current(G1) { value : -3.1; } pg_current(V2) { value : 2.0; } }
```

EXAMPLE MESSAGE

```
Error Line 272, The multiple PG pins can not be simplified format
in leakage_current group. (LBDB-799)
```

LBDB-800 (error) In group '%s', the number of differnt

’%s’ values in the vectors is %d, which should be at least %d.

DESCRIPTION

This error message occurs because Library Compiler requires the vectors should contain at least 2 different slew values and 2 different load values.

The following example shows an output_current_rise group with vectors containing only 1 slew value, which is 1.

```
output_current_template(CCT) {
 variable_1 : input_net_transition;
 variable_2 : total_output_net_capacitance;
 variable_3 : time;
}
. . .
output_current_rise() {
  vector(CCT) {
     reference_time : 0.11;
     index_1 ("0.1");
     index_2 ("1");
     index_3 ("1, 2, 3");
     values ("1, 2, 3");
  }
   vector(CCT) {
     reference_time : 0.11;
     index_1 ("0.2");
     index_2 ("1");
     index_3 ("1, 2, 3");
     values ("1, 2, 3");
  }
}
```

```
Error: Line 198, In group ’output_current_rise’, the number of differnt
   ’total_output_net_capacitance’ values in the vectors is 1, which should
   be at least %d. (LBDB-800)
```

WHAT NEXT

Check the library source file and add a vector for each input_net_transition and total_output_net_capacitance pair.

LBDB-801 (error) %s and %s attributes must be specified in

pair.

DESCRIPTION

The max_input_switching_count and min_input_switching_count attributes must be defined in pair within a switching_group. Meaning that if max_input_switching_count is defined, then min_input_switching_count must be defined under the same switching_group and vice versa.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
power_cell_type : macro;
dynamic_current() {
  ...
  switching_group() {
    min_input_switching_count : 1;
    ...
  }
...}
```

In this case, min_input_switching_count is defined, but there is no max_input_switching_count, which is wrong. To fix the problem, you can either remove min_input_switching_count from the switching_group or specify max_input_switching_count within switching_group.

EXAMPLE MESSAGE

Error Line 272, min_input_switching_count and max_input_switching_count attributes must be specified in pair. (LBDB-801)

LBDB-802 (error) %s can not be defined within a %s group where %s is defined.

DESCRIPTION

You can only specify either max_input_switching_count and min_input_switching_count or input_switching_condition within a switching_group group. Meaning max_input_switching_count/ min_input_switching_count and input_switching_condition shall not present under the same switching_group group.

ALSO SEE LBDB-801

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
   switching_group() {
      min_input_switching_count : 1;
      max_input_switching_count : 9;
      input_switching_condition(rise);
      ...
   }
```

In this case, min_input_switching_count and max_input_switching_count are defined, and also input_switching_condition is defined under the same switching_group where min_input_switching_count and max_input_switching_count are defined. This is wrong. To fix the problem, please remove either input_switching_condition or min_input_switching_count and max_input_switching_count.

EXAMPLE MESSAGE

```
Error Line 272, input_switching_condition can not be defined within a switching_gro
up
group where min_input_switching_count or max_input_switching_count is defined. (LBD
B-802)
```

LBDB-803 (error) %s and %s are required for all %s groups within this %s group.

DESCRIPTION

If min_input_switching_count and max_input_switching_count are specified in one of switching_group groups within a dynamic_current group, then they must be defined in the rest of switching_group groups.

This message indicates that min_input_switching_count and max_input_switching_count are not defined in all switching_group groups within a dynamic_current.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell(lbdb803) {
    ...
  dynamic_current() {
     ...
```

```
  switching_group() {
     pg_current(V1) {
       vector(test_3) {
         reference_time : 193.2;
         index_1("1.1");
         index_2("18.2 18.3 19.0");
         values("13.78 192.4 1100.1");
        }
       vector(test_3) {
         reference_time : 193.2;
         index_1("1.8");
         index_2("18.2 19.4 19.8");
         values("11.78 112.4 1110.1");
        }
       vector(test_3) {
         reference_time : 193.2;
         index_1("2.1");
         index_2("18.2 19.4 19.8");
         values("12.78 122.4 1120.1");
        }
        ...
      }
   }
  switching_group() {
     min_input_switching_count : 1;
     max_input_switching_count : 9;
     pg_current(V2) {
       vector(test_3) {
        ...
        }
       vector(test_3) {
        ...
        }
        ...
      }
    }
 }
 ...
```

In this case, min_input_switching_count and max_input_switching_count are defined in second switching_group, but not in first switching_group. This is wrong. min_input_switching_count and max_input_switching_count are required for all switching_group groups if they are defined in one of switching_group under the same dynamic_current. To fix the problem, please define min_input_switching_count and max_input_switching_count in first switching_group.

EXAMPLE MESSAGE

```
Errorr Line 272, min_input_switching_count and max_input_switching_count are requir
ed for all switching_group
groups within this dynamic_current group. (LBDB-803)
```

LBDB-804 (error) The switching count shall cover all bits in related_inputs.

DESCRIPTION

The max_input_switching_count and min_input_switching_count attributes defined in a dynamic_current shall cover all bits specified in related_inputs.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
type(bus6) {
  base_type : array ;
  data_type : bit ;
  bit_width : 6 ;
  bit_from : 5 ;
  bit_to : 0 ;
  downto : true ;
}
cell (libdb804) {
  bus(sel) {
    bus_type : bus6 ;
    direction : input ;
    ...
  }
  bundle(C) {
    members(Cx, Cy, Cz);
    direction : input;
    ...
  }
 pin(A1) {
  direction : input;
 ...
   }
 pin(A2) {
  direction : input;
  ...
   }
 pin(A3) {
  direction : input;
   ...
   }
  ...
  power_cell_type : macro;
  dynamic_current() {
    when : "A1";
    related_inputs : "Cx A3 Cy sel[0:3] A2";
    switching_group() {
```

```
      min_input_switching_count : 1;
      max_input_switching_count : 3;
      ...
    }
    switching_group() {
      min_input_switching_count : 5;
      max_input_switching_count : 8;
      ...
    }
  }
```

In this case, total number of bits in related_inputs is 8, so the switching count we specified in min_input_switching_count and max_input_switching_count shall cover number from 1 up to 8. The first switching group covers number from 1 to 3 and second switching group covers number from 5 to 8. The number 4 is not covered by any switching count within the dynamic_current. This is wrong. To fix the problem, we need the third switching_group as following :

switching_group() { min_input_switching_count : 4; max_input_switching_count : 4; ... }

EXAMPLE MESSAGE

Error Line 272, The switching count shall cover all bits in related_inputs. (LBDB-804)

LBDB-805 (error) The value of %s is invalid.

DESCRIPTION

The message indicates that you are breaking one of following rules :

1> The value of min_input_switching_count must be greater than 0. 2> The value of max_input_switching_count must be greater than or equal to min_input_switching_count. 3> The value of max_input_switching_count must be less than or equal to total number of bits in related_inputs

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
type(bus6) {
  base_type : array ;
  data_type : bit ;
  bit_width : 6 ;
  bit_from : 5 ;
  bit_to : 0 ;
```

```
  downto : true ;
}
cell (libdb804) {
  bus(sel) {
    bus_type : bus6 ;
    direction : input ;
    ...
  }
  bundle(C) {
    members(Cx, Cy, Cz);
    direction : input;
    ...
  }
 pin(A1) {
  direction : input;
 ...
   }
 pin(A2) {
  direction : input;
  ...
   }
 pin(A3) {
  direction : input;
   ...
   }
  ...
  power_cell_type : macro;
  dynamic_current() {
    when : "A1";
    related_inputs : "Cx A3 Cy sel[0:3] A2";
    switching_group() {
      min_input_switching_count : 0;
      max_input_switching_count : 9;
      ...
    }
    switching_group() {
      min_input_switching_count : 8;
      max_input_switching_count : 6;
      ...
    }
  }
```

In this case, total number of bits in related_inputs is 8, so the switching count we specified in min_input_switching_count and max_input_switching_count shall cover only from 1 up to 8. 0 in min_input_switching_count is not a valid number, and 9 in max_input_switching_count is not a valid number, either. In the second switching_group, min_input_switching_count is greater than max_input_switching_count, which is wrong.

EXAMPLE MESSAGE

```
Error Line 272, The value of min_input_switching_count is invalid. (LBDB-805)
Error Line 272, The value of max_input_switching_count is invalid. (LBDB-805)
```

LBDB-806 (error) table_lookup is required model in ccs.

DESCRIPTION

The table_lookup is required delay_model for following ccs syntaxes :

ccs timing (driver and receiver), compact ccs timing, ccs noise, and ccs power

The message indicates that either there is no delay_model in your library or the delay_model you defined is not "table_lookup".

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
library(libdb806) {
  ...
  cell(test_1) {
    pin(Z) {
      direction : output;
      timing() {
        compact_ccs_rise(template) {
         ....
      ...}
        compact_ccs_fall(template) {
         ....
      ...}
    ...}
  ...}
}
```

In this case, ccs compact is defined but there is no delay_model specified, which is wrong. This is the fix to avoid the error message.

```
library(libdb806) { delay_model : table_lookup; ... cell(test_1) { ... }
```

EXAMPLE MESSAGE

Error Line 272, table_lookup is required model in ccs. (LBDB-806)

LBDB-807 (error) The power_down_function is not allowed in

test_cell.

DESCRIPTION

The power_down_function attribute can not be specified under test_cell group.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell(libdb807) {
  ...
    test_cell() {
      pin(QN) {
        direction : output;
        power_down_function : "!VDD + VSS";
        function : "IQN";
        signal_type : test_scan_out_inverted;
      }
    }
  ...
}
```

In this case, power_down_function attribute is defined under a test_cell, which is wrong. You can avoid the message by comment out power_down_function attribute.

EXAMPLE MESSAGE

Error Line 272, The power_down_function is not allowed in test_cell. (LBDB-807)

LBDB-808 (error) The %s can’t be specified if %s is not defined.

DESCRIPTION

The nominal tables must be specified if variation-aware tables are there. Meaning the following variation-aware tables can be specified only if the corresponding nominal tables are defined.

va tables : va_compact_ccs_rise , va_compact_ccs_fall va_receiver_capacitance1_rise , va_receiver_capacitance2_rise va_receiver_capacitance1_fall , va_receiver_capacitance2_fall va_rise_constraint, va_fall_constraint and va_leakage_current

corresponding nominal tables : compact_ccs_rise , compact_ccs_fall receiver_capacitance1_rise , receiver_capacitance2_rise receiver_capacitance1_fall , receiver_capacitance2_fall rise_constraint, fall_constraint and leakage_current

For the leakage_current, we need to consider when statement. Meaning that va_leakage_current can be defined only if leakage_current with the same state condition as what va_leakage_current has and it is defined within the same cell as where va_leakage_current is deinfed.

The same rule is applied to gate_leakage. The gate_leakage in va_leakage_current can't be specified if gate_leakage with same pin name is not defined in leakage_current, and both va_leakage_current and leakage_current are under the same state condition.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
pin(QN) {
 ...
 pin_based_variation() {
    va_parameters(var1, var2);
    nominal_va_values(10.0, 20.0);
    va_receiver_capacitance1_rise ( pinTB2INVXC_rise_1 ) {
      va_values(10.0, 21.0);
      values (
        "1.100, 1.100, 1.100");
    }
    ...
  }
}
```

In this case, there is no receiver_capacitance specified within QN pin, so it is wrong to define va_receiver_capacitance1_rise table.

EXAMPLE MESSAGE

Error: Line 341, The va receiver cap can't be specified if nominal receiver cap is not defined. (LBDB-808)

EXAMPLES

```
leakage_current() {
  when : "B1";
  ...
}
leakage_current() {
  when : "C1";
  ...
}
leakage_current() {
  when : "D1";
  ...
}
leakage_current() { /* default */
```

```
    ...
  }
  cell_based_variation() {
     va_parameters(var1, var2);
     nominal_va_values(10.0, 20.0);
     va_leakage_current() {
       when : "A1";
       va_values(10.0, 21.0);
       ...
     }
     ...
   }
 }
```

In this case, there is no "when statement" A1 in leakage_current, but "when : A1" is defined in va_leakage_current, which is wrong.

EXAMPLE MESSAGE

Error: Line 246, The va_leakage_current can’t be specified if leakage_current with the same state condition is not defined. (LBDB-808)

EXAMPLES

```
  leakage_current() {
    when : "A2";
    pg_current(V1) {
      value : 4.5;
    }
    pg_current(G1) {
      value : -4.5;
    }
    gate_leakage(A2) {
      input_high_value : 7.1;
    }
  }
  cell_based_variation() {
     va_parameters(var1);
     nominal_va_values(10.0);
     va_leakage_current() {
       when : "A2";
       va_values(11.0);
       pg_current(V1) {
         value : 4.5;
       }
       pg_current(G1) {
         value : -4.5;
       }
       gate_leakage(A1) {
        input_high_value : 9.3;
        input_low_value : -8.7;
       }
     }
     ...
```

```
    }
  }
```

The gate_leakage "A1" is defined under va_leakage_current, but it is not defined under leakage_current, where va_leakage_current and leakage_current have same state condition (when : "A2"). This violate the rule.

EXAMPLE MESSAGE

Error: Line 161, The gate_leakage in va_leakage_current can’t be specified if gate_ leakage in leakage_current is not defined. (LBDB-808)

LBDB-809 (error) The left_id and right_id must be either defined in pairs or non-defined.

DESCRIPTION

The left_id and right_id are optoinal attributes for variation-aware compact table. If they are defined, then they must be defined in pairs.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
library(libdb809) {
 compact_lut_template(va_test){
  variable_1 : input_net_transition ;
  variable_2 : total_output_net_capacitance ;
  variable_3 : curve_parameters;
  index_1 ( "5.236700e-02, 6.042500e-02, 8.710600e-02" ) ;
  index_2 ( "1.000000e-03, 1.511000e-03" ) ;
  index_3 ("init_current, peak_current, peak_voltage, peak_time, left_id");
  base_curves_group : "tt";
 }
   timing () {
     ...
      timing_based_variation() {
        va_parameters(var1, var2);
        nominal_va_values(10.0, 20.0);
        va_compact_ccs_rise(va_test) {
         va_values(10.0, 21.0);
         values (
            "0.01, 3.45, 3.20, 1.3, 1", "1.01, 2.45, 4.20, 2.3, 1", "2.01, 3.35, 5.
20, 3.3, 1","3.01, 4.45, 6.20, 4.3, 1","4.01, 5.45, 7.20, 5.3, 1", "6.01, 7.45, 8.2
```

```
0, 6.3, 1");
        }
      }
    ...
}
```

In this case, va_compact_ccs_rise is referring to a template, va_test, which has only left_id without right_id. This is wrong. To avoid the error message, you shall either remove left_id from the template or define right_id in the template.

EXAMPLE MESSAGE

```
Error: Line 813, The left_id and right_id must be either defined in
        pairs or non-defined. (LBDB-809)
```

LBDB-810 (error) The %s can’t be empty.

DESCRIPTION

There must be at least one variable specified in va_parameters attribute.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
    pin_based_variation() {
        va_parameters();
        ...
    }
```

In this case, there is no value inside va_parameters, which is wrong. You can specified a list of variables in va_parameters(), and the list can’t be empty.

EXAMPLE MESSAGE

```
Error: Line 1029, The va_parameters can’t be empty. (LBDB-810)
```

LBDB-811 (error) The %s must be defined before %s is defined.

DESCRIPTION

The va_parameters can be defined within library(), timing_based_variation(), pin_based_variation() or cell_based_variation() group.

The va_parameters is referred by nominal_va_values and va_values, and it shall be defined before nominal_va_values and va_values are defined.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
library(libdb811) {
  ...
    pin_based_variation() {
        nominal_va_values(10.0, 20.0);
        ...
        va_receiver_capacitance1_rise ( pinTB2INVXC_rise_1 ) {
         va_values(10.0, 21.0);
         values (
            "1.100, 1.100, 1.100");
        }
    }
  ...
  va_parameters(var1, var2);
}
```

In this case, there is no va_parameters attribute defined inside either library() or pin_based_variation() before nominal_va_values and va_values. To fix the problem, please move va_parameters(var1, var2) to the line above pin_based_variation().

```
library(libdb811) { va_parameters(var1, var2); ... pin_based_variation() {
nominal_va_values(10.0, 20.0); ... va_receiver_capacitance1_rise (
pinTB2INVXC_rise_1 ) { va_values(10.0, 21.0); values (  "1.100, 1.100, 1.100"); } }
... }
```

Or, you can move the va_parameters(var1, var2) to the line above nominal_va_values(10.0, 20.0).

```
library(libdb811) { ... pin_based_variation() { va_parameters(var1, var2);
nominal_va_values(10.0, 20.0); ... va_receiver_capacitance1_rise (
pinTB2INVXC_rise_1 ) { va_values(10.0, 21.0); values (  "1.100, 1.100, 1.100"); } }
... }
```

EXAMPLE MESSAGE

```
Error: Line 626, The va_parameters must be defined before nominal_va_values is defi
ned. (LBDB-811)
Error: Line 638, The va_parameters must be defined before va_values is defined. (LB
DB-811)
```

LBDB-812 (error) The size of %s and %s must be identical.

DESCRIPTION

You can specified a list of values in these attributes : va_parameters, nominal_va_values and va_values.

The size of list in nominal_va_values must be the same as the size of corresponding va_parameters. The same rule is applied to va_values.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
library(libdb821) {
 ...
 va_parameters(var1);
  ...
  pin(a) {
    pin_based_variation() {
        nominal_va_values(10.0, 20.0);
        va_receiver_capacitance1_rise ( pinTB2INVXC_rise_1 ) {
          va_values(10.0, 21.0);
          values (
          "1.100, 1.100, 1.100");
        }
     }
  ...
  }
}
```

In this case, the size of va_parameters is 1, but the size of va_values is 2. They are shall be identical. And, the size of nominal_va_values is 2, which is not the same as the size of va_parameters neither. To fix the problem, please specify two values in va_parameters such as va_parameters(var1, var2).

EXAMPLE MESSAGE

```
Error: Line 761, The size of va_parameters and nominal_va_values must be identical.
 (LBDB-812)
Error: Line 763, The size of va_parameters and va_values must be identical. (LBDB-
812)
```

LBDB-813 (error) The values in %s must be unique.

DESCRIPTION

The variables that you specified in va_parameters must be unique. They can’t have the same name.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
va_parameters(var1, var2, var2, var4);
```

In this case, there are two var2 in va_parameters, which is wrong.

EXAMPLE MESSAGE

Error: Line 363, The values in va_parameters must be unique. (LBDB-813)

LBDB-814 (error) The values in %s must be the same as defined values.

DESCRIPTION

The following predefined parameters can be specified in **va_parameters**:

- The parameters defined in default_operating_conditions, such as process, temperature, and voltage
- The voltage names defined in voltage_map

If these predefined parameters are specified in **va_parameters**, then the values defined in **nominal_va_values** must match the values of the predefined parameters.

If both **default_operating_conditions** and **voltage_map** are defined, and **voltage** is defined in **va_parameters**, then Library Compiler considers **voltage** as a user-defined parameter, an exception to the rule.

WHAT NEXT

Check the library source file, and make sure the values are correct.

In the following example, the predefined parameter **voltage** is specified in **va_parameters**, and the corresponding value in **nominal_va_values** is defined as 15.1.

This value is incorrect because it will be the same value of 9.0 as defined in **default_operating_conditions**, WCCOM. For the **process** predefined parameter, 35.0 in **nominal_va_values** is incorrect, because it is not the same value of 1.5 as defined in **default_operating_conditions**.

```
library(libdb814) {
    operating_conditions(WCCOM) {
        process : 1.5 ;
        temperature : 45 ;
        voltage : 9.0 ;
        tree_type : "worst_case_tree" ;
    }
    default_operating_conditions : WCCOM;
    ...
      timing_based_variation() {
        va_parameters(voltage, var2, process, temperature);
        nominal_va_values(15.1, 25.0, 35.0, 45.0);
        ...
    ...
```

In the example below, both **default_operating_conditions** and **voltage_map** are defined. The **voltage** is user-defined parameter, (not a predefined parameter), which means you can specify any voltage value in **nominal_va_values**. However, VDD is a predefined parameter in **voltage_map**. If you specified it in **va_parameters**, then the corresponding value of 10.0 in **nominal_va_values** will be the same as the value of 9.0 defined in **voltage_map**. The values are not the same, so the error message is generated.

```
library(libdb814) {
    ...
    voltage_map( VDD, 9.0);
    voltage_map(VDDH, 4.91);
    voltage_map(VDDL, 4.80);
    voltage_map(VSS, 0.0);

    operating_conditions(WCCOM) {
        process : 1.5 ;
        temperature : 45 ;
        voltage : 9.0 ;
        tree_type : "worst_case_tree" ;
    }
    default_operating_conditions : WCCOM;
    ...
      timing_based_variation() {
        va_parameters(voltage, var2, VDD, temperature);
        nominal_va_values(15.1, 25.0, 10.0, 45.0);
        ...
    ...
```

LBDB-815 (error) The number of %s in %s must be exactly

twice the number of the values in va_parameters.

DESCRIPTION

This error message occurs when the number of variation tables does not equal twice the number of the values in **va_parameters**.

The following are the possible variation tables that you can specify under **pin_based_variation**:

```
   va_receiver_capacitance1_rise
   va_receiver_capacitance2_rise
   va_receiver_capacitance1_fall
   va_receiver_capacitance2_fall
```

in -25i

The following are the possible variation tables that you can specify under **timing_based_variation**:

```
   va_receiver_capacitance1_rise
   va_receiver_capacitance2_rise
   va_receiver_capacitance1_fall
   va_receiver_capacitance2_fall
   va_rise_constraint
   va_fall_constraint
   va_compact_ccs_rise
   va_compact_ccs_fall
```

The total number of these tables must be exactly twice number of values in **va_parameters**.

WHAT NEXT

Check the library source file, make the necessary corrections, and run the command again.

EXAMPLES

In the following example, there are 5 **va_receiver_capacitance1_rise groups** under **timing_based_variation**. Since the size of va_parameters is 2, var1 and var2, the total number of **va_receiver_capacitance1_rise** groups will be 4 instead of 5.

```
 timing_based_variation() {
  va_parameters(var1, var2);
  nominal_va_values(15.0, 25.0);
  va_receiver_capacitance1_rise ( va_TB2INVXC_rise_1 ) {
    va_values(16.0, 25.0);
    values (
      "1.100, 1.100", "1.100, 1.100", "1.100, 1.100");
  }
  va_receiver_capacitance1_rise ( va_TB2INVXC_rise_1 ) {
```

```
    va_values(14.0, 25.0);
    values (
      "1.200, 1.200", "1.200, 1.200", "1.200, 1.200");
  }
  va_receiver_capacitance1_rise ( va_TB2INVXC_rise_1 ) {
    va_values(15.0, 26.0);
    values (
      "1.300, 1.300", "1.300, 1.300", "1.300, 1.300");
  }
  va_receiver_capacitance1_rise ( va_TB2INVXC_rise_1 ) {
    va_values(15.0, 24.0);
    values (
      "1.400, 1.400", "1.400, 1.400", "1.400, 1.400");
  }
  va_receiver_capacitance1_rise ( va_TB2INVXC_rise_1 ) {
    va_values(15.0, 23.0);
    values (
      "1.400, 1.400", "1.400, 1.400", "1.400, 1.400");
  }
 ...
```

LBDB-816 (error) %s in this group and %s defined in %s shall have identical values on all but one.

DESCRIPTION

The values you specified in va_values and nominal_va_values must be identical except for one value.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
 pin_based_variation() {
  va_parameters(var1, var2, var3, var4);
  nominal_va_values(15.0, 25.0, 35.0, 45.0);
  va_receiver_capacitance1_rise ( pinTB2INVXC_rise_1 ) {
    va_values(15.0, 25.0, 35.0, 45.0);
    values (
      "1.100, 1.100, 1.100");
  }

  va_receiver_capacitance1_rise ( pinTB2INVXC_rise_1 ) {
    va_values(14.0, 25.0, 35.0, 45.0);
    values (
      "1.200, 1.200, 1.200");
  }
```

```
  va_receiver_capacitance1_rise ( pinTB2INVXC_rise_1 ) {
    va_values(15.0, 26.0, 36.0, 45.0);
    values (
      "1.300, 1.300, 1.300");
  }
   ...
```

In the first va_receiver_capacitance1_rise, all values in nominal_va_values and va_values are the same, which is wrong. There must be one value difference.

In the second va_receiver_capacitance1_rise, var1 has different value between va_values and nominal_va_values, which is okay.

In the third va_receiver_capacitance1_rise, var2 and var3 have different values between va_values and nominal_va_values, which is wrong. Only one value is allowed to be different.

EXAMPLE MESSAGE

```
Error: Line 381, va_values in this group and nominal_va_values defined in pin_based
_variation
        shall have identical values on all but one.      (LBDB-816)
```

LBDB-817 (error) For %s groups in %s, one characterization point is required and up to two points are allowed for each parameter.

DESCRIPTION

At least one characterization point is required for each parameter, and only up to two points are allowed. The value of characterization point must be different from the nominal value. If there are two points, then one must be greater than nominal value, and the other must be less than nominal value.

This rule also applies for all va_leakage_current groups under the same state condition.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
timing_based_variation() {
  va_parameters(var1, var2);
  nominal_va_values(15.0, 25.0);
  va_compact_ccs_rise(va_lut) {
```

```
    va_values(16.0, 25.0);
    values ( ... );
  }
  va_compact_ccs_rise(va_lut) {
    va_values(19.0, 25.0);
    values ( ... );
  }
  va_compact_ccs_rise(va_lut) {
    va_values(15.0, 26.0);
    values ( ... );
  }
  va_compact_ccs_rise(va_lut) {
    va_values(15.0, 24.0);
    values ( ... );
  }
  ...
}
```

For the parameter var1, there are two variations (19.0 and 16.0), and both of them are greater than nominal value 15.0, which is wrong.

EXAMPLES

```
      timing_based_variation() {
        va_parameters(var1, var2);
        nominal_va_values(15.0, 25.0);
            va_rise_constraint(va_sup_hld) {
                va_values(16.0, 25.0);
                index_1(" 0.006, 0.04, 0.1, 0.2, 1");
                index_2(" 0.006, 0.04, 0.1, 0.2, 1");
                values( ...);
                }
            va_rise_constraint(va_sup_hld) {
                va_values(14.0, 25.0);
                index_1(" 0.006, 0.04, 0.1, 0.2, 1");
                index_2(" 0.006, 0.04, 0.1, 0.2, 1");
                values( ...);
                }
            va_rise_constraint(va_sup_hld) {
                va_values(16.0, 25.0);
                index_1(" 0.006, 0.04, 0.1, 0.2, 1");
                index_2(" 0.006, 0.04, 0.1, 0.2, 1");
                values( ...);
                }
           va_rise_constraint(va_sup_hld) {
                va_values(15.0, 24.0);
                index_1(" 0.006, 0.04, 0.1, 0.2, 1");
                index_2(" 0.006, 0.04, 0.1, 0.2, 1");
                values( ...);
                }
         ...
```

For parameter var1, there are three variation values (16.0, 14.0 and 16.0 again). This is wrong because only up to 2 points are allowed. For parameter var2, there is only one variation value (24.0), which is okay.

EXAMPLES

```
      cell_based_variation() {
        va_parameters(var1, var2);
        nominal_va_values(15.0, 25.0);
            va_leakage_current() {
                when : "A1";
                va_values(17.0, 25.0);
                 ...
                }
            va_leakage_current() {
                when : "A1";
                va_values(13.0, 25.0);
                 ...
                }
            va_leakage_current() {
                when : "!A1";
                va_values(17.0, 25.0);
                 ...
                }
            va_leakage_current() {
                when : "!A1";
                va_values(15.0, 29.0);
                 ...
                }
            va_leakage_current() {  /* default state */
                va_values(16.0, 25.0);
                 ...
                }
    va_leakage_current() {  /* default state */
                va_values(15.0, 26.0);
                 ...
                }
       } /* end of cell_based_variation */
         ...
```

Under the when statement "A1", there is no characterization point for var2, which is wrong, and var1 have two points (17.0 and 13.0), which are okay. For the cases with state condition "!A1" and without any state condition (default state), both are okay.

EXAMPLE MESSAGE

```
Error: Line 552, For va_rise_constraint groups in timing_based_variation, one chara
cterization point
is required and up to two points are allowed for each parameter. (LBDB-817)
```

LBDB-818 (error) At least, one of the variation-aware groups is

absent.

DESCRIPTION

This message indicates that at least you are missing one of the variation-aware tables. Here is the rule : if both of nominal tables are defined, then either no variation-aware table is required or all variation-aware tablea are required. Meaning that if all nominal tables are defined, then you can’t not just define partial of correspoding variation-aware tables.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
    timing() {
      ...
        fall_constraint(sup_hld) {
           index_1(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1        ");
           index_2(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1        ");
           values( ...
        }
        rise_constraint(sup_hld) {
           index_1(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1        ");
           index_2(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1        ");
           values( ...
        }
        timing_based_variation() {
        ...
           va_rise_constraint(va_sup_hld) {
             ...
             values( ...
        ...}
     ...}
 ,,,}
```

In this case, both nominal tables (fall_constraint and rise_constraint) are defined and only one of variation-aware tables (va_rise_constraint) is defined, which is wrong. To fix the problem, please either add va_fall_constraint :

```
timing() { ... fall_constraint(sup_hld) { index_1(" 0.006 , 0.04 , 0.1 , 0.2 , 1 ");
index_2(" 0.006 , 0.04 , 0.1 , 0.2 , 1 "); values( ... } rise_constraint(sup_hld) {
index_1(" 0.006 , 0.04 , 0.1 , 0.2 , 1 "); index_2(" 0.006 , 0.04 , 0.1 , 0.2 , 1
"); values( ... } timing_based_variation() { ... va_rise_constraint(va_sup_hld) {
... values( ... ...} va_fall_constraint(va_sup_hld) { ... values( ... ...}

...} ...}
```

or remove va_rise_constraint from the timing arc :

```
timing() { ... fall_constraint(sup_hld) { index_1(" 0.006 , 0.04 , 0.1 , 0.2 , 1 ");
```

```
index_2(" 0.006 , 0.04 , 0.1 , 0.2 , 1 "); values( ... } rise_constraint(sup_hld) {
index_1(" 0.006 , 0.04 , 0.1 , 0.2 , 1 "); index_2(" 0.006 , 0.04 , 0.1 , 0.2 , 1
"); values( ... } timing_based_variation() { ... ...} ...}
```

EXAMPLE MESSAGE

```
Error: Line 552 At least, one of the variation-aware groups is absent. (LBDB-818)
```

LBDB-819 (warning) The %s %s is not present, so accuracy can be deteriorated.

DESCRIPTION

You will get the wanring due to the following reason : - If CCS timing driver model is defined, then CCS timing receiver model is expected to be there, too.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
...
 pin(I) {
   direction : input ;
   capacitance : 0.0014397 ;
   rise_capacitance : 0.0013000 ;
   fall_capacitance : 0.0012000 ;
 }
 pin(Z) {
   direction : output ;
   max_capacitance : 0.17890 ;
   function : "I" ;

   timing() {
     related_pin : "I" ;
     timing_sense : positive_unate ;
     cell_rise(delay_template_7x7) {
       ...
     }
     rise_transition(delay_template_7x7) {
       ...
     }
     cell_fall(delay_template_7x7) {
              ...
     }
     fall_transition(delay_template_7x7) {
               ...
     }
```

```
        output_current_fall() {
           ...
        }
        output_current_rise() {
           ...
        }
        ...
      }
    ...
```

In this case, ccs receiver data for pin 'I' is expected because ccs driver model is defined.

EXAMPLE MESSAGE

```
Warning: Line 3186, The CCS receiver data is not present, so
        accuracy can be deteriorated. (LBDB-819)
```

LBDB-820 (error) The %s is preferred pg type.

DESCRIPTION

If the cell is an always_on cell, then for all signal pins, the backup_power is preferred pg_type that related_power_pin shall refer to, and backup_ground is preferred pg_type that related_ground_pin shall refer to.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell(test) {
   always_on : TRUE;
   pg_pin(PWR) {
   voltage_name : VDD;
   pg_type : primary_power;
   }
   pg_pin(GND) {
   voltage_name : VSS;
   pg_type : primary_ground;
   }
   pg_pin(GND1) {
   voltage_name : VSS1;
   pg_type : backup_ground;
   }
   pg_pin(VDDI) {
   voltage_name : VDDH;
   pg_type : backup_power;
   }
```

```
   ...
   pin(A1) {
        always_on : TRUE;
        direction : input;
        related_power_pin : PWR;
        related_ground_pin : GND1;
      ...
   }
   pin(A2) {
        direction : input;
        related_power_pin : VDDI;
        related_ground_pin : GND;
     ...
   }
   ...
}
```

For the always_on pin, A1 , the related_power_pin is pointing to PWR, which is not backup_power. For the non always_on pin, A2, the related_ground_pin is pointing to GND, which is not backup_ground either. Both of them shall connect to backup PG.

EXAMPLE MESSAGE

```
Error: Line 335, The backup_power is preferred pg type. (LBDB-820)
Error: Line 385, The backup_ground is preferred pg type. (LBDB-820)
```

LBDB-821 (error) The always_on pin is required for always_on cells.

DESCRIPTION

An always_on cell requires at least one or more always_on pin under it.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell(test) {
   always_on : TRUE;
   ...
   pin(sp) {
        direction : input;
        related_power_pin : PWR;
        related_ground_pin : GND;
      ...
   }
   pin(a) {
```

```
      ...
   }
   ...
}
```

Since ’test’ cell is an always_on cell, the always_on attribute is required to be specified at least in one of pins under ’test’ cell.

EXAMPLE MESSAGE

```
Error: Line 1548, The always_on pin is required for always_on cells. (LBDB-821)
```

LBDB-822 (error) A pin can only has either non-programmable or programmable driver types.

DESCRIPTION

Under a pin, there can only be either non-programmable driver type or programmable driver types, but not both.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
 pin(ZN) {
  direction : inout;
  pull_up_function : "!A1 * !A2 * !A3";
  pull_down_function : "A1 * A2 * !A3";
  bus_hold_function : "A1 * !A2 * !A3";
  driver_type : pull_up;
  ...
 }
```

In pin ZN, there are three programmable driver types, pull_up_function, bus_hold_function, and pull_down_function. Also, the non-programmable driver type, "driver_type : pull_up", is defined under the same pin, which is wrong. Please remove either programmable driver types or non-programmable driver type from the pin.

EXAMPLE MESSAGE

```
Error: Line 104, A pin can only has either non-programmable or
        programmable driver types. (LBDB-822)
```

LBDB-823 (information) The %s %s is not present, so accuracy can be deteriorated.

DESCRIPTION

You will get the message due to one of following reasons : - ccs model is expected to be defined to improve the data accuracy.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
...
  timing() {
    related_pin : "I" ;
    timing_sense : positive_unate ;
    cell_rise(delay_template_7x7) {
      ...
    }
    rise_transition(delay_template_7x7) {
      ...
    }
    cell_fall(delay_template_7x7) {
             ...
    }
    fall_transition(delay_template_7x7) {
              ...
    }
    ...
  }
```

In this case, there is no ccs timing model but NLDM, and we expected ccs timing models for better accuracy.

EXAMPLE MESSAGE

```
Information: Line 582, The CCS data output_current_rise is not present, so
        accuracy can be deteriorated. (LBDB-823)
Information: Line 582, The CCS data output_current_fall is not present, so
        accuracy can be deteriorated. (LBDB-823)
```

LBDB-824 (error) The %s'%s' group cannot specify the static

’%s’ %s.

DESCRIPTION

This message indicates you specified a static ccsn_*_stage group in a timing arc or input/internal pin, whichis not allowed.

A static CCS noise model captures the behaviors of a static CCB (channel connected block). A static CCB refers to a CCB that does not have any input terminal or the voltage level at the input terminal does not affect the output current of the CCB. For example, a static CCS noise model can be characterized for a CMOS NAND gate when both inputs are tied to ground. Such static CCS noise models can be used in noise analysis with case analysis, but they cannot be used for propagating crosstalk delay or noise waveforms through the cell under study. Please refer to "CCS Noise Library Characterization Guide" for detailed information.

WHAT NEXT

Change the library file by adding the missing non-static ccsn_*_stage group.

EXAMPLE MESSAGE

Error: Line 27, The ’timing’ group cannot specify the static ’ccsn_first_stage’ gro up. (LBDB-824)

LBDB-825 (error) The ’%s’ pin with ’true’ has_pass_gate attribute does not have any timing-level/pin-level ccsn_first_stage/ ccsn_last_stage group with ’true’ is_pass_gate attribute.

DESCRIPTION

This message indicates you specified a pin with ’true’ has_pass_gate, but does not specify ’true’ is_pass_gate attribute in its timing-level/pin-level ccsn_*_stage groups, which causes conflict.

WHAT NEXT

Change the library file by either remove the has_pass_gate attribyte from eh pin or specify ’true’ is_pass_gate attribute for the relative pin-level/timing-level ccsn_first_stage/ccsn_last_stage group inside the pin.

EXAMPLE MESSAGE

```
Error: Line 27, The The 'Z' pin with 'true' has_pass_gate attribute
does not have any timing-level/pin-level ccsn_first_stage/ccsn_last_stage
group with 'true' is_pass_gate attribute. (LBDB-825)
```

LBDB-826w (warning) The %s entry cannot be found for %s(%s) of cell(%s).

DESCRIPTION

This warning message occurs when there is no related entry for pg_pin, rail_connection, or other attributes specified in the map file required by the add_pg_pin_to_db command.

WHAT NEXT

This is only a warning message. No action is required.

However, you can eliminate this warning message by adding the required entry to the map file.

EXAMPLE

The following is an example of this warning message:

```
Warning: The pg_to_voltage_map entry cannot be found for pg_pin(VDD)
of cell(sample). (LBDB-826w)
```

SEE ALSO

add_pg_pin_to_db(2)

LBDB-826 (error) The %s entry cannot be found for %s(%s) of cell(%s).

DESCRIPTION

This message indicates that you do not specify the relative entry in the map file required by add_pg_pin_to_db command.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

```
Error: The pg_to_voltage_map entry cannot be found for pg_pin(VDD) of cell(sample).
 (LBDB-826)
```

LBDB-827 (error) The input library '%s' has not been read in.

DESCRIPTION

This message indicates that the input library has not been read in.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

```
Error: The input library 'a.db' has not been read in. (LBDB-827)
```

LBDB-828 (error) The input library '%s' is pg_pin-based library.

DESCRIPTION

This message indicates that the input library is pg_pin-based.

WHAT NEXT

The input library is already pg_pin based, and no need to be converted by the utility

EXAMPLES

EXAMPLE MESSAGE

```
Error: The input library 'a.db' is pg_pin-based library. (LBDB-828)
```

LBDB-828w (warning) The input library ’%s’ is pg_pin-based library.

DESCRIPTION

This message indicates that the input library is pg_pin-based.

WHAT NEXT

The input library is already pg_pin based, and only incremental update will be performed.

EXAMPLES

EXAMPLE MESSAGE

Warning: The input library ’a.db’ is pg_pin-based library. (LBDB-828w)

LBDB-829 (error) The input library ’%s’ does not have default operating_conditions.

DESCRIPTION

This message indicates that the input library does not have default operating_conditions.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

Error: The input library ’A.db’ does not have default operating_conditions. (LBDB-829)

LBDB-830 (error) The input library ’%s’ does not have ’voltage’

attribute in the default operating_conditions '%s'.

DESCRIPTION

This message indicates that the input library does not have default operating_conditions.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

Error: The input library 'A.db' does not have 'voltage' attribute in trhe default operating_conditions 'nom_pvt'. (LBDB-830)

LBDB-831 (error) The converted voltage_map table is empty.

DESCRIPTION

This message indicates that converted voltage_map table is empty.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

Error: The converted voltage_map table is empty. (LBDB-831)

LBDB-832 (error) The number of pg_pin's generated for cell(%s) is %d, which is less than 2.

DESCRIPTION

This message indicates that the number of generated pg_pin's for the cell is less than the required minimum value (2).

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

```
Error:  The number of pg_pin’s generated for cell(A) is 1, which is less than 2. (L
BDB-832)
```

LBDB-833 (error) The related_pg_pin for %s %s power_level(%s) of cell(%s) cannot be found.

DESCRIPTION

This message indicates that the related_pg_pin entry cannot be found for internal_power/leakage_power group.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

```
Error:  The related_pg_pin for cell-
level internal_power power_level(VDD) of cell(A). (LBDB-833)
```

LBDB-834 (error) The related_pg_pin for %s %s of cell(%s) cannot be found.

DESCRIPTION

This message indicates that the related_pg_pin entry cannot be found for internal_power/leakage_power group.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

```
Error:  The related_pg_pin for cell-level internal_power of cell(A). (LBDB-834)
```

LBDB-835 (error) For cell(%s), the %s(%s) which is the %s of pin(%s) cannot be found.

DESCRIPTION

This message indicates that you do not specify the power/ground pg_pin of a cell in the map file required by add_pg_pin_to_db command.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

```
Error: For cell(sample), the pg_pin(VDD) which is the related_power_pin of pin(A) c
annot be found. (LBDB-835)
```

LBDB-836 (error) Failed to generate %s for pin(%s) of cell(%s).

DESCRIPTION

This message indicates that add_pg_pin_to_db command cannot generated related_powe_pin/related_ground_pin for the specfied signal pin. Please check input map file to make sure that it is specified correctly.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

```
Error: Failed to generate related_ground_pin for pin(A) of cell(sample). (LBDB-836)
```

LBDB-837 (error) The %s for pin(%s) of cell(%s) cannot be found.

DESCRIPTION

This message indicates that the related_power_pin/related_ground_pin cannot be found for the specified pin.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

Error: The related_power_pin for pin(A) of cell(sample) cannot be found. (LBDB-837)

LBDB-838 (error) Failed to find the file name for %s option.

DESCRIPTION

In add_pg_pin_to_db command, some options have dependency and requirement. (1) An output db file name must be specified in -output option and must be different from the input db file. (2) If -mw_library_name is not specified, -pg_map_file must be specified, and vice versa. (3) If the Milkyway library does not cover all cells in db, -pg_map_file must be specified. (4) the map file name must be valid and exists in disk.

WHAT NEXT

Check the options to this command, and specify all the necessary ones.

EXAMPLES

```
add_pg_pin_to_db input.db -output pg_pin.db
```

In this case, neither -pg_map_file nor -mw_library_name is specified. You will get the second error message in the following example.

EXAMPLE MESSAGE

```
Error: Failed to find the file name for -output option. (LBDB-838)
Error: Failed to find the file name for either -pg_map_file or -
mw_library_name. (LBDB-838)
Error: Failed to find the file name for -pg_map_file option. (LBDB-838)
```

LBDB-839 (warning) Partial Milkyway library for the input library file.

DESCRIPTION

In add_pg_pin_to_db command, when you specify -mw_library_name and the Milkyway library does not cover all cells in the input db, this warning will occur. This includes missing cells, as well as missing and mismatched pins. This is shown after check_library command is invoked under the hood, and you will also see Logic vs. physical library check summary: Number of cells missing in logic library: <number of missing cells>

WHAT NEXT

First you need to check if the Milkyway library you specified is the correct one. Otherwise, you should specify mapping in the map file for those cells that do not exist or exist but have missing or mismatched pins in the Milkyway library. Otherwise, later checking in the flow will find such cells are not specified in the map file and pg_pin based db will not be generated. If you want to get a list of the missing cells and/or missing and mismatched pins, run check_library command for logic vs. physical library cross checking with default options. You do not need to use set_check_library_options command to set options. You only need to specify logic and Milkyway library names in check_library command.

EXAMPLES

```
add_pg_pin_to_db input.db -mw_library_name mwlib -pg_map_file pg.map -
output pg_pin.db
```

In this case, Milkyway library mwlib does not cover all cells in input.db.
You will get the second error message in the following example.

EXAMPLE MESSAGE

```
Logic vs. physical library check summary:
Number of cells missing in logic library:       23
Logic library is INCONSISTENT with physical library.
Warning: Partial Milkyway library for the input library file. (LBDB-839)
```

LBDB-840 (warning) No %s found in map file.

DESCRIPTION

In the map file, if any of the following occurs: (1) No BEGIN <section_name> or END <section_name> (2) incorrect <section_name> (3) incorrect key words in title line this message will be printed out. Valid section names include: PG_PIN_MAP PG_TO_VOLTAGE_MAP VOLTAGE_MAP POWER_DOWN_FUNCTION_MAP

Key words in title line include: (1) PG_TO_VOLTAGE_MAP section cell, pg_pin, voltage_name, pg_type and direction where key word direction is optional. (2) PG_PIN_MAP section cell, pin, rail_connection and pg_pin (3) VOLTAGE_MAP section voltage_name and voltage_value (4) POWER_DOWN_FUNCTION_MAP cell, pin and power_down_function

The key words in each title line should be in the above order and delimited by Tab or space(s). Invalid record will be ignored. If BEGIN or END section line or title line is missing, the whole section will be ignored. In the map file, the following lines are legal but will be ignored: (1) a comment line starting with # is a comment line and (2) a blank line

WHAT NEXT

You should correct the syntax errors in the map file.

EXAMPLES

```
BEGIN PG_TO_VOLTAGE_MAP
cell        pg_pin      voltage_name pg_type
ADDFHX1     VDD         VDD     power
ADDFHX1     VSS         VSS     primary_ground
END PG_TO_VOLTAGE_MAP
```

EXAMPLE MESSAGE

```
Warning: Line 14, No END section found in map file. (LBDB-840)
Warning: Line 20, No BEGIN section found in map file. (LBDB-840)
Warning: Line 44, No title line found in map file. (LBDB-840)
```

LBDB-841 (error) Failed to read input library '%s'.

DESCRIPTION

When the input library file does not exist or cannot open for read or the library is not a valid technology library, this message occurs.

WHAT NEXT

Check for the input library file name and location to make sure it exists with read permission. If it does, check if the input library is a valid technology library.

EXAMPLES

EXAMPLE MESSAGE

```
Error: Failed to read input library 'rail.db'. (LBDB-841)
```

LBDB-842 (warning) Number of rail_connections %d for cell '%s' is not equivalent to number of power pins %d in %s.

DESCRIPTION

In cell group in db, rail_connection is used to specify power rails, not ground or internal pins. Therefore, if a rail_connection is for ground, such as VSS in the following example, the rail_connection is not valid.

WHAT NEXT

If you have more rail_connections in db than power pins in Milkyway or map file, check if the extra rail is proper or not. If not, you should remove it from db. Otherwise, there is mismatch between db and Milkyway (or map file if the cell is from map file) and the command will stop conversion for a new pg_pin db.

EXAMPLES

```
    cell (test) {
rail_connection(VDD, VDD);
rail_connection(VDD_AUX, VDD1);
rail_connection(VSS, VSS);
      ...
    }
```

    In Milkyway library, cell test has VDD and VSS, but no VDD1.

EXAMPLE MESSAGE

```
Warning: Number of rail_connections 3 for cell 'test' is not equivalent to number o
f power pins 1 in Milkyway. (LBDB-842)
```

LBDB-843 (error) %s cell '%s' does not have %s pg_pins.

DESCRIPTION

Each cell with NLDM, CCS-T and CCS-N has at least 2 pg_pins (1 power and 1 ground) while a load or pull_up (tieoff high) or pull_down (tieoff low) cell has at least one pg_pin as documented in LC manual. Further, a pull_up cell should have a power

pg_pin while a pull_down cell should have a ground pg_pin.

WHAT NEXT

Check and specify the correct pg_pin in the map file: 1) for a cell with NLDM, CCS-T and CCS-N, check if there are at least 1 power and 1 ground pg_pin's, and 1 power and 1 ground pg_pin's for each signal pin. 2) for a load cell, check if there are at least 1 pg_pin 3) for a pull_up cell, check if there is 1 power pg_pin 4) for a pull_down cell, check if there is 1 ground pg_pin

EXAMPLES

```
BEGIN PG_TO_VOLTAGE_MAP
cell        pg_pin      voltage_name pg_type
tieoff_pullup VDD VDD     primary_power
tieoff_pulldownVSSVSS     primary_power
END PG_TO_VOLTAGE_MAP
```
where tieoff_pulldown cell does not have a ground pg_pin.

EXAMPLE MESSAGE

```
Error: Tieoff cell 'tieoff_pulldown' does not have ground pg_pins. (LBDB-843)
Error: cell 'ADDFHX4' pin 'A' does not have related_power pg_pins. (LBDB-843)
```

LBDB-843w (warning) %s cell '%s' does not have %s pg_pins.

DESCRIPTION

Each cell with NLDM, CCS-T and CCS-N has at least 2 pg_pins (1 power and 1 ground) while a load or pull_up (tieoff high) or pull_down (tieoff low) cell has at least one pg_pin as documented in LC manual. Further, a pull_up cell should have a power pg_pin while a pull_down cell should have a ground pg_pin.

WHAT NEXT

Check and specify the correct pg_pin in the map file: 1) for a cell with NLDM, CCS-T and CCS-N, check if there are at least 1 power and 1 ground pg_pin's, and 1 power and 1 ground pg_pin's for each signal pin. 2) for a load cell, check if there are at least 1 pg_pin 3) for a pull_up cell, check if there is 1 power pg_pin 4) for a pull_down cell, check if there is 1 ground pg_pin

EXAMPLES

```
BEGIN PG_TO_VOLTAGE_MAP
cell        pg_pin      voltage_name pg_type
tieoff_pullup VDD VDD     primary_power
tieoff_pulldownVSSVSS     primary_power
END PG_TO_VOLTAGE_MAP
```

where tieoff_pulldown cell does not have a ground pg_pin.

EXAMPLE MESSAGE

Warning: Tieoff cell 'tieoff_pulldown' does not have ground pg_pins. (LBDB-843w)

LBDB-844 (warning) %s '%s' does not exist in input db. Remove it from map.

DESCRIPTION

When a cell and/or pin specified in the map file does not exist in the input db, it will be ignored and removed from the map. The cell may come from the map file or Milkyway. If it comes from Milkyway, no line number is printed out.

WHAT NEXT

Check if the cell and/or pin is what you want. If so, you need to check the input db for the missing cell. Otherwise, ignore it or remove it from the map file.

EXAMPLES

EXAMPLE MESSAGE

Warning: Line 24, Cell 'test' does not exist in input db. Remove it from map. (LBDB-844)

LBDB-845 (error) %s '%s' is missing in %s.

DESCRIPTION

If a db cell and/or pin is missing in the map file or its Milkyway library, this message will be printed out. You need to add its mapping in the map file to generate a complete pg_pin based db file. For dirty flow and on the fly PG library update, for non-rail_based db's, you need to either input Milkyway library or map data. In the case of incremental update to a PG library, you need to specify map file or tcl file for maps. For dirty flow by add_pg_pin_to_lib, for rail_based lib's, if there is no power_level with voltage value 0. the utility does not assume a default ground pin, so you need to either input Milkyway library or map data.

WHAT NEXT

You need to add the mapping in the map file or specify the correct Milkyway library for the missing cells to generate a complete pg_pin based db file. You can use wild card "*" for all the cells that are not explicitly specified in the map file. For dirty flow and on the fly PG library update, you need to input either Milkyway library or map data for non-rail_based db's.

EXAMPLES

EXAMPLE MESSAGE

Error: Cell 'test' is missing in map file. (LBDB-845)
Error: 'Map data or FRAM' is missing in input. (LBDB-845)

LBDB-845w (warning) %s '%s' is missing in %s.

DESCRIPTION

If a power management attribute is missing in the cell, this message will occur. If a db cell and/or pin is missing in the map file or its Milkyway library, this message will be printed out. You need to add its mapping in the map file to generate a complete pg_pin based db file.

WHAT NEXT

You need to add the missing attribute for power management cells; otherwise, the cells will not be used for UPF. You need to add the mapping in the map file or specify the correct Milkyway library for the missing cells to generate a complete pg_pin based db file. You can use wild card "*" for all the cells that are not explicitly specified in the map file.

EXAMPLES

EXAMPLE MESSAGE

Warning: Cell 'LS16FROM16TO20' 'level_shifter_type' is missing in library'. (LBDB-845w)

LBDB-846 (warning) Cell '%s' has %d %s pins in Milkyway library.

DESCRIPTION

If a cell has multiple power or ground pins in Milkyway and db, you should specify related_power_pin and related_ground_pin for its signal pins.

WHAT NEXT

Check PG_PIN_MAP section in the map file to see if related_power_pin and related_ground_pin's are specified for these cells that have multiple P/G pins. This is only a warning message. In the flow that follows this message, there are other checkings that will catch error if you did not specify related_power_pin and related_ground_pin for these cells.

EXAMPLES

```
BEGIN PG_PIN_MAP
cell    pin rail_connection pg_pin
test    LSI VDD             VDD
test    LSO VDD_AUX         VDD_AUX
test    LSI -               VSS
test    LSO -               VSS
END PG_PIN_MAP
```
where cell test has 2 power pins: VDD and VDD_AUX.

EXAMPLE MESSAGE

Warning: Cell 'test' has 2 power pins in Milkyway library. (LBDB-846)

LBDB-847 (error) Too many values (%d) specified in the table.

DESCRIPTION

This message indicates that there are too many values specified in the table. (number = index1_size * index2_size [* index3_size] [*index4_size]). The number exceed the limit (32767) that Library Compiler current handles.

WHAT NEXT

Split the table, to make each table's size less than the limit.

EXAMPLE MESSAGE

Error: Line 307, Too many values (45000) specified in the table. (LBDB-847)

LBDB-848 (error) There is no ’%s’ %s defined for ’%s’ %s.

DESCRIPTION

This message indicates the library does not define the voltage_map for the voltage_name specified in a pg_pin, or input_signal_level/output_signal_level defined in a pin.

WHAT NEXT

Add the missing voltage_map.

EXAMPLES

```
      voltage_map(VDD, 1.08);
      voltage_map(VDD1, 1.1);
      voltage_map(VSS, 0.0);

...
      cell(sample) {
      pg_pin(VDD) {
voltage_name : VDD2;
...
}
...
      }
      ...
```

In this case, there is no voltage_map defined for voltage_name VDD2. To fix the problem, add the voltage_map attribute for VDD2 at the library level:

```
      voltage_map(VDD, 1.08);
      voltage_map(VDD1, 1.1);
      voltage_map(VDD2, 1.2);
      voltage_map(VSS, 0);

...
      cell(sample) {
      pg_pin(VDD) {
voltage_name : VDD2;
...
}
...
      }
      ...
```

EXAMPLE MESSAGE

Error: Line 23, There is no ’VDD2’ voltage_map defined for ’VDD2’ voltage_name. (LB DB-848)

LBDB-849 (warning) The '%s' group is overwritten by the '%s' group on line %d.

DESCRIPTION

The same group has been defined multiple times and only the last one will be recoded in the library db.

WHAT NEXT

Check the dc_current groups for wrong information and fix.

EXAMPLES

EXAMPLE MESSAGE

Warning: The 'dc_current' group is overwritten by the 'dc_current' group on line 12 0. (LBDB-849)

LBDB-850 (warning) Missing %s value under section %s in map file.

DESCRIPTION

If data entered in map file is incomplete, this message will be printed out. In PG_TO_VOLTAGE_MAP section, there are four fields: cell, pg_pin, pg_type and voltage_name. If one or more fields are left blank, you will see missing data in this section. The same is true for other sections. In VOLTAGE_MAP, for multi-rail library you should specify voltage_map entry with voltage_value = 0. Invalid record will be ignored. In POWER_DOWN_FUNCTION_MAP, if power_down_function values are missing for some cell/pins, the default values !VDD1+!VDD2+...+VSS1+VSS2 will be used where VDDi and VSSi are pg_pins of the cell.

WHAT NEXT

You should enter values for each field in the map file. Do not leave blank in any field except optional direction field in PG_TO_VOLTAGE_MAP section.

EXAMPLES

```
BEGIN PG_TO_VOLTAGE_MAP
cell        pg_pin      voltage_name pg_type
ADDFHX1     VDD         VDD
ADDFHX1     VSS         VSS     primary_ground
END PG_TO_VOLTAGE_MAP
```

EXAMPLE MESSAGE

```
Warning: Line 14, Missing pg_type value under section PG_TO_VOLTAGE_MAP in map file
. (LBDB-850)
Warning: Line 20, Missing voltage value under section VOLTAGE_MAP in map file. (LBD
B-850)
```

LBDB-851 (error) %s section %s in map file.

DESCRIPTION

If the whole map section is missing (neither in map file nor derivable), this message will be printed out. For single-rail library, only PG_TO_VOLTAGE_MAP is required if no Milkyway library. If there is complete Milkyway library to cover all the cells in the input db, no map file is required. In this case, VOLTAGE_MAP will be derived from the input db that includes one voltage_map for nominal voltage and the other one for ground (voltage value = 0). For multi-rail library, PG_PIN_MAP, PG_TO_VOLTAGE_MAP, VOLTAGE_MAP and POWER_DOWN_FUNCTION_MAP sections are all required. If there are rail_connection's, PG_PIN_MAP is required in any case. Please note that invalid entries in the map section are ignored and removed. So even though these entries exist in the map section, the final map table may not include such entries.

WHAT NEXT

Enter the missing section. For multi-rail library, specify all the four map sections with complete data. You can use "*" in cell and/or pin fields for all the others that are not listed in the map section. For single-rail library, specify at least PG_TO_VOLTAGE_MAP section with complete pg_pin, voltage_name and pg_type for each cell.

EXAMPLES

```
BEGIN PG_TO_VOLTAGE_MAP
cell    pg_pin  voltage_name    pg_type
*     VDD     VDD primary_power
*     VSS     VSS primary_ground
*     VSS1    VSS1 backup_ground
END PG_TO_VOLTAGE_MAP
BEGIN POWER_DOWN_FUNCTION_MAP
cell    pin power_down_function
test    test    VSS
*     *       !VDD+VSS+VSS1
END POWER_DOWN_FUNCTION_MAP
```

EXAMPLE MESSAGE

```
Error: Missing section PG_PIN_MAP in map file. (LBDB-851)
Error: Missing section VOLTAGE_MAP in map file. (LBDB-851)
```

LBDB-852 (error) %s found in %s is missing in %s.

DESCRIPTION

This message occurs during cross checking of map sections. (1) PG_PIN_MAP and PG_TO_VOLTAGE_MAP It is two-way checking. It is to check consistency of pg_pin associated with a cell between the two map sections. If a pg_pin for a cell exists in one map section but either the pg_pin or cell is missing in the other section, you will see this message. (2) PG_PIN_MAP and POWER_DOWN_FUNCTION_MAP It is to check signal pin consistency between the two sections. If a pin for a cell exists in POWER_DOWN_FUNCTION_MAP but is missing in PG_PIN_MAP, you will see this message. This checking is for multi-rail library. (3) PG_TO_VOLTAGE_MAP and VOLTAGE_MAP It is to check voltage_name consistency between the two sections. If the voltage_name for the nominal voltage is specified in VOLTAGE_MAP but is missing in PG_TO_VOLTAGE_MAP, you will see a message saying so. Please also refer to LBDB-854. In VOLTAGE_MAP, you can have more entries than necessary.

WHAT NEXT

Check if the missing data (cell, pg_pin or pin) is what is required in the map section or extra data in the section where it exists. In the following example, if it is a multi-rail library and pg_pin VDD1 is what you should need in the library, you should list its entry in PG_TO_VOLTAGE_MAP, in the form of ADDFHX1 VDD1 VDD1 backup_power Otherwise, if it is a single-rail library, you should remove the entry for VDD1 from PG_PIN_MAP.

EXAMPLES

```
BEGIN PG_PIN_MAP
cell    pin rail_connection pg_pin
ADDFHX1 A       -   VSS
ADDFHX1 A       -   VDD
ADDFHX1 A       -   VDD1
END PG_PIN_MAP
BEGIN PG_TO_VOLTAGE_MAP
cell    pg_pin  voltage_name    pg_type
ADDFHX1 VDD     VDD primary_power
ADDFHX1 VSS     VSS primary_ground
END PG_TO_VOLTAGE_MAP
```

EXAMPLE MESSAGE

```
Error: Line 14, Cell 'test' pg_pin 'VDD1' found in PG_PIN_MAP is missing in PG_TO_V
OLTAGE_MAP. (LBDB-852)
```

LBDB-853 (warning) Voltage value %g for voltage_name '%s' is

replaced by %g from input library.

DESCRIPTION

In add_pg_pin_to_db, it takes the data in the input db as higher priority. Therefore, if you defined a voltage_map in the map file while there is a different voltage value in the db for this voltage_name, the user defined value will be replaced by the value from the db, e.g. power_rail. The voltage value from the input db is taken in the following order: 1. If the library db has defined default_operating_conditions, then the specified voltage value in operating_condition will be used as the nominal voltage. 2. Otherwise, nom_voltage value defined at the library level will be used as the nominal voltage.

EXAMPLES

```
BEGIN VOLTAGE_MAP
voltage_name    voltage_value
VDD        1.1
VSS     0.0
END VOLTAGE_MAP
in default_operating_conditions,
   power_rail (VDD, 1.2)
```

EXAMPLE MESSAGE

```
Warning: Voltage value 1.1 for voltage_name 'VDD' is replaced by 1.2 from input lib
rary. (LBDB-853)
```

LBDB-854 (warning) voltage_map for nominal voltage %g not referenced in PG_TO_VOLTAGE_MAP.

DESCRIPTION

If you have specified a voltage_map with the nominal voltage (or in the case of a single-rail or 1P1G library, a default voltage_map for the nominal voltage is automatically derived from the input db), but this voltage_name is not referenced in PG_TO_VOLTAGE_MAP table, you will receive this message.

WHAT NEXT

Check if this nominal voltage and voltage name are correct. If so, add its mapping entry with the nominal voltage in PG_TO_VOLTAGE_MAP. If you have not specified the correct voltage_name for the nominal voltage in VOLTAGE_MAP, please correct the voltage_name. If you have not specified the voltage_map in the map file for the nominal voltage and it is derived by the utility, please specify the voltage_map for the nominal voltage by using the correct voltage_name from PG_TO_VOLTAGE_MAP.

EXAMPLES

```
BEGIN PG_TO_VOLTAGE_MAP
cell    pg_pin  voltage_name   pg_type
test    VDD1    VDD1           primary_power
test    VSS    VSS            primary_ground
END PG_TO_VOLTAGE_MAP

BEGIN VOLTAGE_MAP
voltage_name    voltage_value
VDD        1.2
VDD1        1.08
VSS     0.0
END VOLTAGE_MAP
where 1.2 is nominal voltage.
```

EXAMPLE MESSAGE

```
Warning: voltage_map for nominal voltage 1.2 not referenced in PG_TO_VOLTAGE_MAP. (
LBDB-854)
```

LBDB-855 (warning) Invalid %s found under section %s in map file.

DESCRIPTION

In the map file, if any of the following is incorrect, (1) pg_type (2) pg_pin direction (3) voltage value (4) wild card or - in wrong field (5) incorrect section name or keywords in title line (6) pin direction in POWER_DON_FUNCTION_MAP (7) duplicate data specified on the same cell/pin (8) incorrect rail_connection this message will occur.

Valid pg_type values include: primary_power primary_ground backup_power backup_ground internal_power internal_ground Valid pg_pin direction values include input output inout internal nwell pwell deepnwell deeppwell

Valid voltage values are non-negative floating point numbers. Valid pin directions in POWER_DOWN_FUNCTION_MAP are output or inout. Valid power_down_functions are double quoted strings or unquoted strings if no space within the strings and the strings must contain only the power and ground pin names. rail_connection value should be derived from input .lib/db for the cell. If no rail_connection, please enter -.

Wild cards "*" and "-" can only be entered in some specific fields: (1) PG_PIN_MAP section "*" can be entered in cell and pin fields, and "-" can be entered in pin and rail_connection fields. (2) POWER_DOWN_FUNCTION_MAP section "*" can be entered in cell and pin fields. (3) PG_TO_VOLTAGE_MAP section "*" can be entered in cell field only, and "-" can be entered in optional direction field. (4) VOLTAGE_MAP section No "*" or "-" can be entered in any field in this section. Caret "^" cannot be entered in the first entry of each map section. In checking title lines, the key words and their order should be exactly the same as mentioned in the spec. If an invalid value

is entered or the value is entered in the wrong field in the map file, the whole record will be ignored for all fields except optional field in which only optional value is ignored. For example, if the pg_pin direction value is invalid, only the invalid value in this field is ignored. However, if the value is invalid in other fields, the whole line of record wil be ignored. (5) POWER_MANAGEMENT_ATTRIBUTE_MAP section If you specify duplicate entries on the same cell/pin/attribute, the last one will be ignored. For example, if you specify retention_2 sv retention_pin (save, "1") retention_2 sv retention_pin (restore, "0") you will receive this message and the second entry will be ignored. If you want to specify pin SAVE as both save and restore, specify it in this way, retention_2 sv retention_pin (save_restore, "0")

WHAT NEXT

You should correct the invalid values in the map file. For example, in pg_type field, if you enter power, you will receive this message. The correct pg_type should be primary_power.

EXAMPLES

```
BEGIN PG_TO_VOLTAGE_MAP
cell        pg_pin      voltage_name pg_type
ADDFHX1     VDD         VDD     power
ADDFHX1     VSS         VSS     primary_ground
GEND PG_TO_VOLTAGE_MAP
```

EXAMPLE MESSAGE

```
Warning: Line 14, Invalid pg_type found under section PG_TO_VOLTAGE_MAP in map file
. (LBDB-855)
Warning: Line 20, Invalid wild card found under section PG_PIN_MAP in map file. (LB
DB-855)
```

LBDB-856 (error) For pin(%s) of cell(%s), the %s entry for %s of pin(%s) cannot be found.

DESCRIPTION

This message indicates that you do not specify the relative_power_pin/ related_ground_pin of the signal pin in the PG_PIN_MAP section of the map file used by add_pg_pin_to_db command.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

```
Error: For pin(A) of cell(sample), the pg_pin_map entry for related_power_pin of pi
n(A) cannot be found. (LBDB-856)
```

LBDB-857 (error) Missing %s under section %s.

DESCRIPTION

You will receive this Error if the following occurs: (1) VOLTAGE_MAP for multi-rail library if you do not specify voltage_map entry with voltage_value = 0 (2) POWER_MANAGEMENT_ATTRIBUTE_MAP if you do not specify a complete set of power management attributes in the map file, or the input .lib has partial power management attributes but you do not specify the ones that are missing in the library

WHAT NEXT

You should enter values for each field in the map file. Do not leave blank in any field except optional direction field in PG_TO_VOLTAGE_MAP section. In VOLTAGE_MAP, for multi-rail library you should specify voltage_map entry with voltage_value = 0. In POWER_MANAGEMENT_ATTRIBUTE_MAP, specify the missing power attributes. In converting power_gating_pin, it uses power_pin_class and map_to_logic attributes in DB, and change power_pin_class = 6, 7, 8 to pin class "save", "restore" and "save_restore", respectively, and take the value of map_to_logic as <disable_value>. If the input .lib does not have power_pin_class = 6, 7 or 8, you should specify retention_pin_class as in the example RET_1svretention_pin (save, "0")

EXAMPLES

```
BEGIN VOLTAGE_MAP
voltage_name    voltage_value
VDDlow      1.6
VDDhigh     2.0
VSS     0.1
END VOLTAGE_MAP
```

EXAMPLE MESSAGE

```
Error: Missing voltage value 0 under section VOLTAGE_MAP. (LBDB-857)
Error: Missing power_pin_class for cell ’retention’ pin ’sv’ under section POWER_MA
NAGEMENT_ATTRIBUTE_MAP. (LBDB-857)
```

LBDB-858 (error) The timing arc %s->%s with when condition "%s" doesn’t have ccs noise model.

DESCRIPTION

For every timing arc, there must be one of the followings: (1) arc-based ccs noise model(s) with the same "when" condition as the "when" of the timing arc, (2) pin-based ccs noise models with the same "when" condition as the "when" of the timing arc, or (3) pin-based ccs noise models with default (i.e., no "when") "when" condition.

For example, pin(CO) { timing() { when : "!B&A"; ... ccsn_first_stage() { /* no when condition */ ... } /* qualified model 1 */ }

ccsn_last_stage() { when : "!B&A"; ... } /* qualified model 2 */

ccsn_last_stage() { /* no when condition */ ... } /* qualified model 3 */

... }

when condition "default" means that this timing arc has no "when" attribute.

WHAT NEXT

Add ccs noise model with the qualified "when" condition.

EXAMPLE MESSAGE

Error: The timing arc CI-
>CO with when condition "!B&A" doesn’t have ccs noise model. (LBDB-858)

LBDB-859 (error) There is no cross point in this %s group with input_net_transition %s.

DESCRIPTION

For expanded ccs power, if **pg_current** is represented as a sparse cross table, if there is no *input_net_transition*, then there must be one and only one cross point in one of the vectors. if *input_net_transition* is specified, then one and only one cross point is required for each *input_net_transition*.

For compact ccs power, if **pg_current** is represented as a sparse cross table, then the typical capacitance of the pin specified in "index_output" must be one of the values in index with variable "total_output_net_capacitance".

WHAT NEXT

Add cross point for each input_net_transition.

EXAMPLES

```
  dynamic_current() {
    ...
    related_outputs : "Q QN QN1 QN2";
    typical_capacitances(10.0, 12.0, 14.0, 16.0);
    switching_group() {
      ...
      pg_current(VDD) {
        vector(CCS_power_1) {
          index_output : "QN1";
  index_1 ("0.01");
  index_2 ("14.0"); /* cross point */
  ...
}
vector(CCS_power_1) {
  index_output : "QN2";
  index_1 ("0.02");
  index_2 ("11.0"); /* non cross point */
  ...
}
      }
      ...
    }
  }
```

In this case, pg_current has only two vectors. There is no cross point with input_net_transition 0.02. So error message LBDB-859 will be issued.

EXAMPLE MESSAGE

Error: There is no cross point in this pg_current group with input_net_transition 0 .02. (LBDB-859)

LBDB-860 (error) This cross point vector is inconsistent with a previous one with the same input_net_transition.

DESCRIPTION

If two cross point **vector** groups have the same **index** value of *input_net_transition*, then waveform of the I-t curve and **reference_time** must be the same for both vectors.

Two I-t curve waveforms are "equal" means,

Step1. Use the 1st waveform as a reference. For each time point in the reference waveform, get the current from the 2nd waveform. (may involve linear interpolation).

Step2. Take the sum of absolute difference on currents for each time point at the reference waveform. Assume total num of points in the reference waveform is N.

Step3. Calculate relative waveform difference as Sum_of_difference_on_current / (peak_from_reference * N), which should <= 2%.

Step4. Calculate relative peak difference as ABS (peak_from_2nd - peak_from_reference) / peak_from_reference, which should <= 2%.

WHAT NEXT

Correct one of the cross points to make them consistent.

EXAMPLES

```
  dynamic_current() {
    ...
    related_outputs : "Q QN";
    typical_capacitances(10.0, 12.0);
    switching_group() {
      ...
      pg_current(VDD) {
        vector(CCS_power_1) {
          index_output : "Q";
  reference_time : 0.01;
  index_1 ("0.02"); /* input_net_transition */
  index_2 ("10.0"); /* total_output_net_capacitance */
  index_3 ("0.000, 0.0873, 0.135, 0.764"); /* time */
  values ("0.002, 0.009, 0.134, 0.546");
}
vector(CCS_power_1) {
  index_output : "QN";
  reference_time : 0.04;
  index_1 ("0.02"); /* input_net_transition */
  index_2 ("12.0"); /* total_output_net_capacitance */
  index_3 ("0.000, 0.0873, 0.135, 0.764"); /* time */
  values ("0.002, 0.009, 0.134, 0.546");
}
      }
      ...
    }
  }
```

In this case, pg_current is a sparse cross table, two vectors are represented as cross points, and both have the same input_net_transition 0.02. In such a case, I-t curve waveform and reference_time (0.01 and 0.04, not identical. Error out) must be the same.

EXAMPLE MESSAGE

Error: This cross point vector is inconsistent with a previous one with the same in put_net_transition. (LBDB-860)

LBDB-861 (error) This vector is repeated with a previous one under the same pg_current group.

DESCRIPTION

Under the same **pg_current** group, no two vectors can have the same **index_output** and values of all **index** attributes except for the last **index** (time). Otherwise, this vector will be regarded as repeated.

WHAT NEXT

Correct one of the vectors to make them different.

EXAMPLES

```
      pg_current(VDD) {
        vector(CCS_power_1) {
          index_output : "QN1";
  reference_time : 0.01;
  index_1 ("0.01"); /* input_net_transition */
  index_2 ("14.0"); /* total_output_net_capacitance */
  index_3 ("0.001, 0.003, 0.006"); /* time */
  ...
}
vector(CCS_power_1) {
  index_output : "QN1";
  reference_time : 0.01;
  index_1 ("0.01"); /* input_net_transition */
  index_2 ("14.0"); /* total_output_net_capacitance */
  index_3 ("0.004, 0.007, 0.009"); /* time */
  ...
}
      }
```

In this case, index_output (QN1), input_net_transition (0.01), and total_output_net_capacitance(14.0) are all the same between two vectors. So error message LBDB-861 will be issued.

EXAMPLE MESSAGE

```
Error: This vector is repeated with a previous one under the same pg_current group.
 (LBDB-861)
```

LBDB-862 (error) The dense table under the pg_current group

is incomplete with input_net_transition %s.

DESCRIPTION

If a <template> with two *total_output_net_capacitance* variables is applied to all vectors under a **pg_current** group, then all possible combination of capacitances between two output pins must be specified if all of them have the same *input_net_transition*.

WHAT NEXT

Add vectors to make the dense table complete.

EXAMPLES

```
      pg_current(VDD) {
        vector(CCS_power_dense) {
  reference_time : 0.01;
  index_1 ("0.01"); /* input_net_transition */
  index_2 ("1.0"); /* total_output_net_capacitance */
  index_3 ("2.0"); /* total_output_net_capacitance */
  index_4 ("0.000, 0.0873, 0.135, 0.764"); /* time */
  values ("0.002, 0.009, 0.134, 0.546");
}
        vector(CCS_power_dense) {
  reference_time : 0.01;
  index_1 ("0.01"); /* input_net_transition */
  index_2 ("1.5"); /* total_output_net_capacitance */
  index_3 ("2.5"); /* total_output_net_capacitance */
  index_4 ("0.100, 0.0873, 0.135, 0.764"); /* time */
  values ("0.113, 0.110, 0.243, 0.657");
}
        vector(CCS_power_dense) {
  reference_time : 0.01;
  index_1 ("0.01"); /* input_net_transition */
  index_2 ("1.5"); /* total_output_net_capacitance */
  index_3 ("2.0"); /* total_output_net_capacitance */
  index_4 ("0.000, 0.0873, 0.135, 0.764"); /* time */
  values ("0.224, 0.221, 0.358, 0.769");
}
      }
```

In this case, all possible combinations of (c1, c2) with input_net_transition 0.01 are (1.0, 2.0), (1.5, 2.5), (1.0, 2.5) and (1.5, 2.0). But (1.0, 2.5) is missing. So error message LBDB-862 will be issued.

EXAMPLE MESSAGE

```
Error: The dense table under the pg_current group is incomplete with input_net_tran
sition 0.01. (LBDB-862)
```

LBDB-863 (error) Size or values of total_output_net_capacitance are not identical for output pin %s.

DESCRIPTION

The size and values of *total_output_net_capacitance* for the same output pin or **index_output** (cross type) shall be identical for all vectors which have different *input_net_transition* index values.

In other words, every fixed (without tolerance) input_net_transition needs the same set of total_output_net_capacitance.

In the message, "output pin" means index_output (cross type) or all pins in "related_outputs" (dense type and diagonal type).

WHAT NEXT

Change the size or values of total_output_net_capacitance with a input_net_transition value to make the size and values consistent.

EXAMPLES

```
  dynamic_current() {
    ...
    related_outputs : "Q QN";
    typical_capacitances(10.0, 12.0);
    switching_group() {
      ...
      pg_current(VDD) {
        vector(CCS_power_1) {
          index_output : "Q";
  reference_time : 0.01;
  index_1 ("0.01"); /* input_net_transition */
  index_2 ("5.0"); /* total_output_net_capacitance */
  ...
}
vector(CCS_power_1) {
  index_output : "Q";
  reference_time : 0.01;
  index_1 ("0.01"); /* input_net_transition */
  index_2 ("10.0"); /* total_output_net_capacitance */
  ...
}
vector(CCS_power_1) {
  index_output : "Q";
  reference_time : 0.01;
  index_1 ("0.01"); /* input_net_transition */
  index_2 ("15.0"); /* total_output_net_capacitance */
  ...
}
vector(CCS_power_1) {
```

```
  index_output : "QN";
  reference_time : 0.01;
  index_1 ("0.01"); /* input_net_transition */
  index_2 ("6.0"); /* total_output_net_capacitance */
  ...
}
vector(CCS_power_1) {
  index_output : "QN";
  reference_time : 0.01;
  index_1 ("0.01"); /* input_net_transition */
  index_2 ("12.0"); /* total_output_net_capacitance */
  ...
}
vector(CCS_power_1) {
  index_output : "QN";
  reference_time : 0.01;
  index_1 ("0.01"); /* input_net_transition */
  index_2 ("18.0"); /* total_output_net_capacitance */
  ...
}
vector(CCS_power_1) {
  index_output : "Q";
  reference_time : 0.01;
  index_1 ("0.02"); /* input_net_transition */
  index_2 ("5.0"); /* total_output_net_capacitance */
  ...
}
vector(CCS_power_1) {
  index_output : "Q";
  reference_time : 0.01;
  index_1 ("0.02"); /* input_net_transition */
  index_2 ("11.0"); /* total_output_net_capacitance */
  ...
}
vector(CCS_power_1) {
  index_output : "Q";
  reference_time : 0.01;
  index_1 ("0.02"); /* input_net_transition */
  index_2 ("15.0"); /* total_output_net_capacitance */
  ...
}
vector(CCS_power_1) {
  index_output : "QN";
  reference_time : 0.01;
  index_1 ("0.02"); /* input_net_transition */
  index_2 ("6.0"); /* total_output_net_capacitance */
  ...
}
vector(CCS_power_1) {
  index_output : "QN";
  reference_time : 0.01;
  index_1 ("0.02"); /* input_net_transition */
  index_2 ("12.0"); /* total_output_net_capacitance */
  ...
}
```

```
vector(CCS_power_1) {
  index_output : "QN";
  reference_time : 0.01;
  index_1 ("0.02"); /* input_net_transition */
  index_2 ("18.0"); /* total_output_net_capacitance */
  ...
}
vector(CCS_power_1) {
  index_output : "QN";
  reference_time : 0.01;
  index_1 ("0.02"); /* input_net_transition */
  index_2 ("24.0"); /* total_output_net_capacitance */
  ...
}
      }
      ...
    }
  }
```

When input_net_transition is 0.01 and output pin is Q, total_output_net_capacitance size=3, values = (5.0, 10.0, 15.0). /*group1*/ When input_net_transition is 0.01 and output pin is QN, total_output_net_capacitance size=3, values = (6.0, 12.0, 18.0). /*group2*/ When input_net_transition is 0.02 and output pin is Q, total_output_net_capacitance size=3, values = (5.0, 11.0, 15.0). /*group3*/ When input_net_transition is 0.02 and output pin is QN, total_output_net_capacitance size=4, values = (6.0, 12.0, 18.0, 24.0). /*group4*/ group1 and group3 have different values. group2 and group4 have different sizes. So error message LBDB-863 will be issued.

EXAMPLE MESSAGE

```
Error: Size or values of total_output_net_capacitance are not identical for output
pin Q. (LBDB-863)
Error: Size or values of total_output_net_capacitance are not identical for output
pin QN. (LBDB-863)
```

LBDB-864 (error) The design '%s' has separate intrinsic_parasitic groups.

DESCRIPTION

This error occurs when there are two intrinsic_parasitic groups in the same cell, where the only difference is that one group has only intrinsic_resistance, and the other group has only intrinsic_capacitance.

However, it is allowed that only intrinsic_resistance or intrinsic_capacitance is defined for the intrinsic_parasitic group.

WHAT NEXT

Combine the separate intrinsic_parasitic groups into one group.

EXAMPLES

```
cell (AND3) {
  ...
  intrinsic_parasitic() {
    /* default state */
    intrinsic_resistance(G1) {
       related_output : "ZN";
       value : 9.0;
    }
  }

  intrinsic_parasitic() {
    /* default state */
    intrinsic_capacitance(G2) {
       value : 8.2;
    }
  }
}
```

In this case, cell 'AND3' has both an intrinsic_parasitic group with only intrinsic_resistance and an intrinsic_parasitic group with only intrinsic_capacitance. So error message LBDB-864 will be issued.

EXAMPLE MESSAGE

Error: The design 'AND3' has separate intrinsic_parasitic groups. (LBDB-864)

LBDB-865 (warning) Conductance is negative at input voltage level %g.

DESCRIPTION

The conductance at any index point (input_voltage, output_voltage) is calculated as: at a given input voltage level, G = di/dv, where dv is the voltage difference between two adjacent index points of output voltage, and di is the corresponding current difference.

Conductance calculated from IV curve should be non-negative.

WHAT NEXT

Change output_voltage or current data in dc_current table.

EXAMPLES

```
lu_table_template (c_grain) {
  variable_1 : input_voltage;
  variable_2 : output_voltage;
  index_1("0.0, 0.2, 0.5, 1.08, 4.07");
  index_2("0.0, 0.5, 1.08, 4.0, 5.0");
}
cell (AND3) {
  ...
  dc_current (c_grain) {
    ...
    values ("0.01, 0.02, 0.03, 0.05, 0.06",
            "0.02, 0.03, 0.04, 0.05, 0.06",
            "0.03, 0.04, 0.05, 0.06, 0.07",
            "0.04, 0.05, 0.06, 1.07, 0.08",
            "0.05, 0.06, 0.07, 0.08, 0.09");
  }
}
```

In this case, at input_voltage level 1.08, the conductance is negative when using the current data "1.07" and "0.08". Cond = (0.08-1.07) / (5.0-4.0) < 0. So warning message LBDB-865 will be issued.

EXAMPLE MESSAGE

Warning: Conductance is negative at input voltage level 1.08. (LBDB-865)

SEE ALSO

LBDB-866.n LBDB-867.n

LBDB-866 (warning) The maximum conductance is non-positive.

DESCRIPTION

The conductance at any index point (input_voltage, output_voltage) is calculated as: at a given input voltage level, G = di/dv, where dv is the voltage difference between two adjacent index points of output voltage, and di is the corresponding current difference.

For conductance calculated cross all input voltage and output voltage indices, the largest conductance value should be positive (can’t be zero).

WHAT NEXT

Change output_voltage or current data in dc_current table.

EXAMPLES

```
lu_table_template (c_grain) {
  variable_1 : input_voltage;
  variable_2 : output_voltage;
  index_1("0.0, 0.2, 0.5, 1.08, 4.07");
  index_2("0.0, 0.5, 1.08, 4.0, 5.0");
}
cell (AND3) {
  ...
  dc_current (c_grain) {
    ...
    values ("0.01, 0.01, 0.01, 0.01, 0.01",
            "0.02, 0.02, 0.02, 0.02, 0.02",
            "0.03, 0.03, 0.03, 0.03, 0.03",
            "0.04, 0.04, 0.04, 0.04, 0.04",
            "0.05, 0.05, 0.05, 0.05, 0.05");
  }
}
```

In this case, all conductance is 0.0. So warning message LBDB-866 will be issued.

EXAMPLE MESSAGE

Warning: The maximum conductance is non-positive. (LBDB-866)

SEE ALSO

LBDB-865.n LBDB-867.n

LBDB-867 (warning) Conductance is not monotonically decreasing at input voltage level %g.

DESCRIPTION

The conductance at any index point (input_voltage, output_voltage) is calculated as: at a given input voltage level, G = di/dv, where dv is the voltage difference between two adjacent index points of output voltage, and di is the corresponding current difference.

At any input voltage level, as output voltage increases, the conductance should monotonically decrease.

WHAT NEXT

Change output_voltage or current data in dc_current table.

EXAMPLES

```
lu_table_template (c_grain) {
  variable_1 : input_voltage;
  variable_2 : output_voltage;
  index_1("0.0, 0.2, 0.5, 1.08, 4.07");
  index_2("0.0, 0.5, 1.08, 4.0, 5.0");
}
cell (AND3) {
  ...
  dc_current (c_grain) {
    ...
    values ("0.01, 0.02, 0.03, 0.04, 0.05",
            "0.02, 0.03, 0.04, 0.05, 0.06",
            "0.03, 0.04, 0.05, 0.06, 0.07",
            "0.04, 0.05, 0.06, 1.07, 0.08",
            "0.05, 0.06, 0.07, 0.08, 0.09");
  }
}
```

In this case, at input_voltage level 0.0, the conductance are c1 = (0.02-0.01) / (0.5-0.0) = 0.02 c2 = (0.03-0.02) / (1.08-0.5) = 0.017 c3 = (0.04-0.03) / (4.0-1.08) = 0.0034 c4 = (0.05-0.04) / (5.0-4.0) = 0.1 The values are not monotonically decreasing. So warning message LBDB-867 will be issued.

EXAMPLE MESSAGE

Warning: Conductance is not monotonically decreasing at input voltage level 0.0. (L BDB-867)

SEE ALSO

LBDB-865.n LBDB-866.n

LBDB-868 (warning) The estimated time when output signal reaches VDD level is out of range [%g, %g].

DESCRIPTION

The time when output signal reaches VDD level is estimated as T = reference time + NLDM delay Reference time means the time when input signal reaches VDD level. T has to be within the range of the current waveform (min and max of time in current waveform).

The way to evaluate NLDM delay is to lookup the cell_rise/cell_fall table in the corresponding timing arc with the given input_net_transition and total_output_net_capacitance in the vector.

If the given input_net_transition and total_output_net_capacitance can not be found in the cell_rise/cell_fall table, use the nearest index to get the delay value.

WHAT NEXT

Extend current waveform, or change reference time and delay.

EXAMPLES

```
lu_table_template (table_dodelaycell_rise_0k0aa01m1) {
  variable_1 : total_output_net_capacitance
  variable_2 : input_net_transition
  index_1 (" 0.006404, 0.055194, 0.147118 ");
  index_2 (" 0.060000, 0.400000, 0.800000 ");
}
pg_current_template(t1) {
  variable_1 : input_net_transition;
  variable_2 : total_output_net_capacitance;
  variable_3 : time;
  index_1("0.6 0.9");
  index_2("0.6 0.9");
  index_3("0.3 4.7");
}

cell (AND3) {
  dynamic_current() {
    ...
    related_inputs : "A2 A3";
    related_outputs : "ZN ZN1";
    typical_capacitances(0.3 0.4);
    switching_group() {
      ...
      pg_current(V2) {
        vector(t1) {
          reference_time : 15.6;
          index_output : "ZN1";
          index_1("0.5");
          index_2("0.043");
          index_3("18.2 18.3 19.0");
          values("13.78 192.4 1100.1");
        }
      }
    }
  }

  pin(ZN1) {
    ...
    timing() {
      related_pin : "A1 A2"
      cell_rise( scalar ) {
        values("0.28"); }
      cell_fall( scalar ) {
        values("0.0"); }
      ...
```

```
    }
    timing() {
      related_pin : "A3"
      cell_rise ("table_dodelaycell_rise_0k0aa01m1") {
      values (
        "0.1729, 0.2200, 0.2397 ",
        "0.3494, 0.4012, 0.4273 ",
        "0.6499, 0.7018, 0.7281 "
      );
    }
    cell_fall( scalar ) {
      values("0.0"); }
    }
  }
}
```

In this case, the information on the given current waveform is, (1) the time range is [18.2, 19.0]; (2) reference time is 15.6; (3) input pins are "A2 A3", output pin is ZN1; (4) input_net_transition is 0.5; (5) total_output_net_capacitance is 0.043.

In the section of pin(ZN1), (1) the first timing arc is specified with input pin "A1 A2", overlaped with "A2 A3" in the current waveform. So the delay is needed. delay1 = MAX(0.28, 0.0) = 0.28.

(2) the second timing arc is specified with input pin "A3", overlaped with "A2 A3" in the current waveform. So the delay is needed.

Look up cell_rise table with (input_net_transition=0.5, total_output_net_capacitance=0.043). The nearest index is values[1][1] = 0.4012. delay2 = MAX(0.4012, 0.0) = 0.4012.

max_delay = MAX(delay1, delay2) = 0.4012.

reference_time + max_delay = 15.6+0.4012 = 16.0012. It isn’t within the range [18.2, 19.0]. So warning message LBDB-868 will be issued.

EXAMPLE MESSAGE

Warning: The estimated time when output signal reaches VDD level is out of range [18.2, 19.0]. (LBDB-868)

LBDB-869 (information) Failure rate of the library cells will be overwritten.

DESCRIPTION

Failure rate is a Design-For-Yield concept, it is a integer number, value from 0 ~ 1e9, means the number of failures per billion.

In Liberty syntax, there are two models can describe the cell yield, under the same

cell level group, functional_yield_metric().

cell (my_cell) { ... functional_yield_metric() { /* 1st method */
average_number_of_faults(<template>) { values("float...float"); } /* 2nd method */
critical_area_table(<template>) { defect_type:enum(short, open, short_and_open);
related_layer:<layer_name>; index_1("float...float"); /*particle diameter array*/
values("float...float"); /*critical area values */ } } ... }

Using the 1st method can defined the average failure rate and derive a cell failure rate directly by Library Compiler.

The 2nd method, besides the critical area table in .lib, user need particle distribution function file, using command calculate_caa_based_yield2db to calculate out the failure rate.

This message is reported when the command calculate_caa_based_yield2db is called to calculate the CAA based yield (failure rate), while the failure rate attribute is already exist in the library(db file), regardless the failure rate is calculated by 1st or 2nd method before.

WHAT NEXT

This is just an information to update the status, you can just ignore it.

EXAMPLE MESSAGE

Information: Failure rate of the library cells will be overwritten. (LBDB-869)

LBDB-870 (information) Redundant cross point vector with input_net_transition %s is removed.

DESCRIPTION

If there are more than one cross point vectors with the same input_net_transition under a pg_current group, read_lib will only keep the first one. Others will be removed.

WHAT NEXT

It’s just an information. Change in .lib is not required. However, in order to remove this message, keep only one cross point vector with the specified input_net_transition.

EXAMPLES

```
dynamic_current() {
  ...
  related_outputs : "Q QN QN1 QN2";
```

```
    typical_capacitances(10.0, 12.0, 14.0, 16.0);
    switching_group() {
      ...
      pg_current(VDD) {
        vector(CCS_power_1) {
          index_output : "QN1";
  index_1 ("0.01");
  index_2 ("14.0"); /* cross point */
  ...
}
vector(CCS_power_1) {
  index_output : "QN2";
  index_1 ("0.01");
  index_2 ("16.0"); /* cross point */
  ...
}
      }
      ...
    }
  }
```

In this case, there are two cross points with input_net_transition 0.01. So the second one will be removed.

EXAMPLE MESSAGE

Info: Redundant cross point vectors with input_net_transition 0.01 are removed. (LB DB-870)

LBDB-871 (error) The first point current value(%f) is almost the same as peak point current value(%f).

DESCRIPTION

This error is issued when init current value is numerically identical to the peak current in CCS Timing or Compact CCS Timing data. The tolerance is set to 0.001%, that is: if fabs((I(first_point) - I(peak_point))/I(peak_point)) < 0.001%,

This could potentially cause larger errors in the calculation if data is truncated during reading, when these two values are too close.

WHAT NEXT

Check the library source file and correct the data, most likely, you may need to re-characterize the library cells for CCS timing data.

EXAMPLES

```
      output_current_rise() {
```

```
vector(ccs) {
reference_time : 1.493117e+00;
index_1(2.986235e+00);
index_2(2.500000e+01);
index_3("8.216709e+00, 8.391117e+00, 1.775112e+01, 3.249112e+01, 4.366012e+01, 6.03
3512e+01, 7.932612e+01, 9.818012e+01, 1.184101e+02, 1.420501e+02, 1.728901e+02, 1.8
51275e+02");
values( "4.299772e-01, 4.299781e-01, 4.117592e-01, 3.890655e-01, 3.539464e-
01, 2.690953e-01, 1.685153e-01, 9.581405e-02, 4.934546e-02, 2.188565e-02, 7.340714e-
03, 5.989923e-03");
}
      }
```

EXAMPLE MESSAGE

```
Error: Line 3383, The first point current value(0.429977) is almost
        the same as peak point current value(0.429978). (LBDB-871)
```

SEE ALSO

LBDB-665 LBDB-671

LBDB-872 (warning) Curve parameters in %s are not exact for compact CCS power.

DESCRIPTION

This warning message occurs when the curve parameters are not exact for compact CCS power. If a compact_lut_template is for compact CCS power, the value of the curve_parameters index (the last index) must be the following:

```
   init_time, init_current, bc_id1, point_time1, point_current1, bc_id2,
   [point_time2, point_current2, bc_id3, ...], end_time, end_current
```

This is a pattern instead of a specified series because the compact CCS power table varies in size.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this warning message you can change the values in the curve_parameters index and run the command again.

EXAMPLES

The following example results in this warning message:

```
     compact_lut_template(t1) {
       variable_1 : input_net_transition;
       variable_2 : total_output_net_capacitance;
       variable_3 : curve_parameters;
       index_1 : ("...");
       index_2 : ("...");
       index_3 : ("init_time, init_current, bc_id1");
     }
```

The values in index_3 are not exact for compact CCS power.

SEE ALSO

LBDB-873(n)
LBDB-876(n)
LBDB-877(n)

LBDB-873 (error) Invalid size of data for I-t curve #%d in "values".

DESCRIPTION

In compact ccs power, an I-t curve is always described with the pattern init_time, init_current, bc_id1, point_time1, point_current1, bc_id2, [point_time2, point_current2, bc_id3, ...], end_time, end_current

So the size of data within a pair of quotation (e.g., data for an I-t curve) should be able to reprented as 8+3i (i>=0).

"I-t curve #?" means the order of this curve in "values". For example, "I-t curve #2" means the 2nd curve in "values".

WHAT NEXT

Change size and data in "values".

EXAMPLES

```
  compact_ccs_power(t1) {
    ...
    values("0.0, 1, 0.32, 1.08, 2, 0.87, -
0.33, 3, 1.03, 0.0, 4, 1.50, 0.67", <HardSpace/* size = 13 */
   "0.0, 0.0, 1, 0.28, 0.93, 2, 0.45, 0.28", <HardSpace/* size = 8 */
   "0.0, 0.0, 1, 0.36, 1.05, 2, 0.52, -0.49, 3, 0.88, 0.22", <HardSpace/
* size = 11 */
   "0.0, 0.0, 1, 0.33, 1.31, 2, 0.61, -0.83, 3, 0.96, 0.66" /* size = 11 */);
  }
```

In this example, size of the first line in "values" is 13, which is invalid. Sizes of other lines are valid.

EXAMPLE MESSAGE

Error: Line 388, Invalid size of data for I-t curve #1 in "values". (LBDB-873)

LBDB-874 (error) Time values in I-t curve #%d in "values" should be monotonically increasing.

DESCRIPTION

In compact ccs power, an I-t curve is always described with the pattern init_time, init_current, bc_id1, point_time1, point_current1, bc_id2, [point_time2, point_current2, bc_id3, ...], end_time, end_current

Time values with corresponding parameter "init_time", "point_time*" and "end_time" in an I-t curve should be monotonically increasing.

"I-t curve #?" means the order of this curve in "values". For example, "I-t curve #2" means the 2nd curve in "values".

WHAT NEXT

Change values of time-related data in "values".

EXAMPLES

```
  compact_ccs_power(t1) {
    ...
    values("0.0, 0.0, 1, 1.32, 1.08, 2, 0.87, -
0.33, 3, 1.03, 0.0, 4, 1.50, 0.67", ...
  }
```

In this example, time-related data are {0.0, 1.32, 0.87, 1.03, 1.50}, which are not monotonically increasing.

EXAMPLE MESSAGE

```
Error: Line 388, Time values for I-
t curve #1 in "values" should be monotonically increasing. (LBDB-874)
```

LBDB-875 (warning) %s value %f in I-t curve #%d is too small

and may be reset 0.

DESCRIPTION

In a I-t curve, all time values with corresponding parameter "init_time", "point_time*" and "end_time" can’t be too diverse. Otherwise, small values will be reset 0. Similarly, all current values with corresponding parameter "init_current", "point_current*" and "end_current" can’be too diverse, either. "I-t curve #?" means the order of this curve in "values". For example, "I-t curve #2" means the 2nd curve in "values".

WHAT NEXT

Change time or current values.

EXAMPLES

```
  compact_ccs_power(t1) {
    ...
    values("0.0, 0.0, 1, 1.32, 1.08, 2, 0.87, -
0.33, 3, 1.03, 0.0, 4, 1e+100, 0.67", ...
  }
```

In this example, "end_time" is 1e+100, which will make other non-zero time values 1.32, 0.87 and 1.03 reset 0.

EXAMPLE MESSAGE

```
Warning: Line 388, Time value 1.32 in I-
t curve 1 is too small and may be reset 0. (LBDB-875)
```

LBDB-876 (error) Variables are specified behind indexes in compact_lut_template.

DESCRIPTION

compact_lut_template requires variables are specified before indexes. Other templates don’t have this requirement.

WHAT NEXT

Put all variables in front of indexes.

EXAMPLES

```
  compact_lut_template (t1) {
```

```
    index_1 ("0, 1");
    index_2 ("0, 1");
    index_3 ("init_time, init_current, bc_id1, point_time1, point_current1,
              bc_id2, [point_time2, point_current2, bc_id3, ...],
      end_time, end_current");
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : curve_parameters;
  }
```

EXAMPLE MESSAGE

```
Error: Line 388, Variables are specified behind indexes in compact_lut_template. (L
BDB-876)
```

LBDB-877 (error) Variables in compact_lut_template are invalid.

DESCRIPTION

Variables in compact_lut_template must satisfy, (1) The last variable is "curve_parameters"; (2) The variables before the last one are "input_net_transition" and "total_output_net_capacitance".

If this template is applied in compact ccs timing or va compact ccs timing, (3) There should be exactly one "input_net_transition" and one "total_output_net_capacitance".

If this template is applied in compact ccs power, (3) There should be at most one "input_net_transition" and at most two "total_output_net_capacitance".

WHAT NEXT

Make necessary change in variable and index.

EXAMPLES

```
  compact_lut_template(t1) {
    variable_1 : input_net_transition;
    variable_2 : curve_parameters;
    variable_3 : total_output_net_capacitance;
  }
```

To fix the problem, exchange the values between variable_2 and variable_3.

EXAMPLE MESSAGE

```
Error: Line 388, Variables in compact_lut_template are invalid. (LBDB-877)
```

LBDB-878 (error) One point current value(%f) is almost the same as the adjacent point current value(%f).

DESCRIPTION

This error is issued when current value in one point is numerically identical to that in the adjacent point in Compact CCS Power data. The tolerance is set to 0.001%, that is: if fabs((I(first_point) - I(second_point))/I(second_point)) < 0.001%,

This could potentially cause larger errors in the calculation if data is truncated during reading, when these two values are too close.

WHAT NEXT

Check the library source file and correct the data, most likely, you may need to re-characterize the library cells for CCS power data.

EXAMPLES

```
compact_ccs_power(t1) {
  ...
  values("0.0, 0.0, 1, 0.28, 0.93, 2, 0.45, 0.929999", ...
}
```

EXAMPLE MESSAGE

Error: Line 388, One point current value(0.93) is almost the same as the adjacent p oint current value(0.929999). (LBDB-878)

LBDB-879 (error) Pin ’%s’ can’t be a pll %s pin.

DESCRIPTION

This message is issued because pin direction doesn’t match the required direction of pll reference/feedback/output pin. If a pin is set "is_pll_reference_pin" or "is_pll_feedback_pin" true, it should be an input pin. If a pin is set "is_pll_output_pin" true, it should be an output pin.

WHAT NEXT

Specify the attribute "is_pll_reference_pin", "is_pll_feedback_pin" or "is_pll_output_pin" under another pin with consistent direciton.

EXAMPLES

```
cell (AND2) { is_pll_cell : true; pin (A1) { direction : input; is_pll_output_pin :
true; } ... }
```

EXAMPLE MESSAGE

```
Error: Pin 'A1' can't be a pll output pin. (LBDB-879)
```

LBDB-880 (error) More than one exclusive pll pin attributes are specified in pin '%s'.

DESCRIPTION

In a cell, pll reference pin, pll feedback pin and pll output pin must be different pins. Therefore in a pin group, at most one of the three attributes "is_pll_reference_pin", "is_pll_feedback_pin" and "is_pll_output_pin" can be set true.

WHAT NEXT

Move all pll pin specifications except one to other pins.

EXAMPLES

```
cell (AND2) { is_pll_cell : true; pin (ZN1) { direction : input;
is_pll_reference_pin : true; is_pll_feedback_pin : true; } ... }
```

EXAMPLE MESSAGE

```
Error: More than one exclusive pll pin attributes are specified in pin 'ZN1'. (LBDB-
880)
```

LBDB-881 (error) Pll cell '%s' has wrong pll %s pin defined.

DESCRIPTION

If a cell is specified as a pll cell, then the cell group should contain one and only one pll reference pin, one and only one pll feedback pin, and one or more pll output pins.

WHAT NEXT

Correct pins under the pll cell.

EXAMPLES

```
cell (AND2) { is_pll_cell : true; pin (ZN1) { direction : input;
is_pll_reference_pin : true; } }
```

EXAMPLE MESSAGE

```
Error: Pll cell 'AND2' has wrong pll feedback pin defined. (LBDB-881)
Error: Pll cell 'AND2' has wrong pll output pin defined. (LBDB-881)
```

LBDB-882 (warning) Pll pin tags in non-pll cell '%s' will be ignored.

DESCRIPTION

If a cell is not set "is_pll_cell" true, then pin level attributes "is_pll_reference_pin", "is_pll_feedback_pin" and "is_pll_output_pin" will be ignored.

WHAT NEXT

Remove pll pin tags from the non-pll cell.

EXAMPLES

```
cell (AND2) { pin (ZN1) { direction : input; is_pll_reference_pin : true; } }
```

EXAMPLE MESSAGE

```
Warning: Pll pin tags in non-pll cell 'AND2' will be ignored. (LBDB-882)
```

LBDB-883 (error) More than one physical only cell types are specified in design '%s'.

DESCRIPTION

In a pin group, at most one of the three attributes "is_decap_cell", "is_filler_cell" and "is_tap_cell" can be set true.

WHAT NEXT

Remove all physical only cell type specifications except one.

EXAMPLES

```
cell (S1CAP1) { is_filler_cell : true; is_decap_cell : true; ... }
```

EXAMPLE MESSAGE

Error: More than one physical only cell types are specified in design ’S1CAP1’. (LB DB-883)

LBDB-884 (error) Physical only cell ’%s’ can’t contain I/O pins.

DESCRIPTION

If one of the three attributes "is_decap_cell", "is_filler_cell" and "is_tap_cell" is set true, this cell is a physical only cell. It should contain pg-pin only and has no signal pins in it.

WHAT NEXT

Remove I/O pins in this cell.

EXAMPLES

```
cell (S1CAP1) { is_decap_cell : true; pin(A1) { ... } ... }
```

EXAMPLE MESSAGE

Error: Physical only cell ’S1CAP1’ can’t contain I/O pins. (LBDB-884)

LBDB-885 (error) There is no bias pin named ’%s’ related to this signal pin’s related power or ground pin.

DESCRIPTION

This error message is reported when the association of power/ground pin and bias pin in signal is incorrect.

A signal pin’s related bias pin must one of the related bias pins of this signal pin’s related power/ground pin.

WHAT NEXT

Check if this related bias pin is related to this signal pin’s power pin or ground pin.

EXAMPLE MESSAGE

Error: Line 546, There is no bias pin named vpw related to this signal pin’s related power/ground pin.(LBDB-885)

LBDB-886 (error) Bias pg_pin ’%s’ can not be properly assciated to the pg_pin.

DESCRIPTION

This error message is reported when bias pin %s can not be properly associated to a pg_pin.

Power type pg_ppin should be associated with a nwell type bias pg pin; ground type pg_pin should be associated with a pwell type bias pg pin.

WHAT NEXT

Check the pg_type of the pg_pin to be assoicated and the pg_type of the bias pg_pin.

EXAMPLES

```
pg_pin(PWR) {
  voltage_name : VDD;
  pg_type : primary_power;
  related_bias_pin : "vpw"
}
pg_pin(vpw) {
  voltage_name : VDDL;
  pg_type : pwell;
  bias_connection : routing_pin;
}
```

EXAMPLE MESSAGE

Error: Line 546, Bias pg_pin vpw can not be properly assciated to the pg_pin.(LBDB-886)

LBDB-887 (warning) Only one (P or N)well bias pin exists.

DESCRIPTION

This message is indicates that only one bias pin with pg_type P or N well is exists. Generally, pwell and nwell bias pins should be exsit as a pair.

WHAT NEXT

Delete the odd bias pin or add a new bias pin to be couple with the odd one.

EXAMPLE MESSAGE

Warning: Line 546, Only one (P or N)well bias pin vpw exists.(LBDB-887)

LBDB-888 (error) Bias_connection is associated with a invalid pg_type.

DESCRIPTION

This error message is reported when bias_connection is associted with an invalid pg_type. pg_type of a bias pg pin should be one of the predefined bias types: pwell|nwell|deeppwell|deepnwell.

WHAT NEXT

Check the pg_type of the bias pg pin.

EXAMPLE MESSAGE

Error: Line 546, The pg_type of bias pg pin vpw is incorrect.(LBDB-888)

LBDB-889 (error) The pg_type of bias pg pin '%s' to be related is invalid.

DESCRIPTION

This error message is reported when a bias pg pin is related to a pg_pin or a signal pin, its type_type is not one of the predefined bias types: pwell|nwell|deeppwell|deepnwell.

WHAT NEXT

Check the pg_type of the bias pg pin.

EXAMPLE MESSAGE

```
Error: Line 546, The pg_type of bias pg pin vpw to be related
is invalid.(LBDB-889)
```

LBDB-890 (warning) Isolation cell '%s' contains more than two input pins.

DESCRIPTION

WHAT NEXT

Delete unwanted input pins to keep the input pin number is no less than 2.

EXAMPLES

EXAMPLE MESSAGE

```
Warning: Line 202, Isolation cell 'acell' contains more than two input pins. (LBDB-
890)
```

LBDB-891 (error) Retention cell '%s' has no retention pin.

DESCRIPTION

In a retention cell (identified by retention_cell or power_gating_cell attribute), there should be at leat one control pin (identified by retention_pin or power_gating_pin function).

WHAT NEXT

Add retention pins into the given cell.

EXAMPLES

```
cell(retention_dff) {
  ...
  retention_cell : "my_retention_dff" ;
  clock_gating_integrated_cell : "generic";
```

```
  pin(SAVE) {
    ...
    direction : input;
/*  retention_pin (save, "0") ;*/
  }

  pin(RESTORE) {
    ...
    direction : input;
/*  retention_pin (restore, "0") ;*/
  }
}
```

EXAMPLE MESSAGE

Error: Retention cell ’retention_dff’ has no retention pin. (LBDB-891)

LBDB-892 (error) Pin name ’%s’ is duplicated with pg pin name.

DESCRIPTION

Names of Signal pins should be different with pg pin names and vice-versa.

WHAT NEXT

Change the duplicated signal pin name or pg pin name.

EXAMPLE MESSAGE

Error: Pin name ’VSS’ is duplicated with pg pin name.(LBDB-892)

LBDB-893 (warning) Bad usage to turn on scaling feature.

DESCRIPTION

In order to turn on scaling feature, two environment variables should be set. One is "lc_allow_process_kfactor_scaling" as a switch. Default value is 0 (turn off). Set it as 1 to turn on. The other is "lc_new_process_value" to set the new process value with a float. For example, to load scaled design.db with new process 1.8,

lc_shell> set lc_allow_process_kfactor_scaling 1 lc_shell> set lc_new_process_value 1.8 lc_shell> read_db design.db

This message is issued because only one of the two environment variables is set.

WHAT NEXT

If scaling feature is intended to turn on, set the other variable. Else, ignore this warning.

EXAMPLES

EXAMPLE MESSAGE

Warning: Bad usage to turn on scaling feature. (LBDB-893)

LBDB-894 (warning) No scaling is done in '%s' because nominal process can not be found.

DESCRIPTION

This message is issued because scaling feature is turned on and there is no nominal process defined in the library.

Nominal process is selected in this order of precedence:

(1) if "default_operating_conditions" is specified, nominal process is taken from attribute "process" in the default "operating_conditions" group; (2) nominal process is taken from library-level attribute "nom_process".

WHAT NEXT

Define nominal process in library to continue scaling.

EXAMPLES

EXAMPLE MESSAGE

Warning: No scaling is done because nominal process can not be found. (LBDB-894)

LBDB-895 (warning) "values" in "%s" group won't be scaled because "%s" is not found.

DESCRIPTION

This message is issued because scaling feature is turned on and there is no corresponding k-factor defined for the specified attribute.

Here is the mapping table of supported k-factors and db attributes.

Nominal process is selected in this order of precedence:

k-factor name db_attribute_name k_process_cell_risetiming -> cell_rise -> values k_process_cell_falltiming -> cell_fall -> values k_process_rise_propagationtiming -> rise_propagation -> values k_process_fall_propagationtiming -> fall_propagation -> values k_process_rise_transitiontiming -> rise_transition -> values k_process_fall_transitiontiming -> fall_transition -> values k_process_setup_rise timing -> rise_constraint ->values (when "timing_type" is "setup_rising" or "setup_falling") k_process_setup_falltiming -> fall_constraint ->values (when "timing_type" is "setup_rising" or "setup_falling") k_process_hold_risetiming -> rise_constraint ->values (when "timing_type" is "hold_rising" or "hold_falling") k_process_hold_falltiming -> fall_constraint ->values (when "timing_type" is "hold_rising" or "hold_falling") k_process_recovery_risetiming -> rise_constraint ->values (when "timing_type" is "recovery_rising" or "recovery_falling") k_process_recovery_falltiming -> fall_constraint ->values (when "timing_type" is "recovery_rising" or "recovery_falling") k_process_removal_rise timing -> rise_constraint ->values (when "timing_type" is "removal_rising" or "removal_falling") k_process_removal_falltiming -> fall_constraint ->values (when "timing_type" is "removal_rising" or "removal_falling")

WHAT NEXT

Add corresponding k-factor.

EXAMPLES

EXAMPLE MESSAGE

Warning: "values" in "cell_rise" group won’t be scaled because "k_process_cell_rise " is not found. (LBDB-895)

LBDB-896 (error) Invalid %s found under section %s in map file.

DESCRIPTION

This error message occurs if any the following are incorrect in the map file:

- voltage_name
- voltage value
- power management attributes

A valid voltage_name must be a valid string that starts with either an uppercase character A-Z or a lowercase character a-z.

The voltage_name in the PG_TO_VOLTAGE_MAP section must be the name used in VOLTAGE_MAP. The name could be a rail name, and can be the same as the pg_pin name. You cannot use an invalid value such as "-" or "*" in the voltage_name field in PG_TO_VOLTAGE_MAP or VOLTAGE_MAP section.

Valid voltage values are non-negative floating point numbers, for example, 0.9, that are valid voltage values in the input library.

For valid power management attributes see the *Library Compiler Modeling Timing, Signal Integrity, and Power in Technology Libraries User Guide*. The following are some examples of power management attributes:

- valid switch_cell_type is coarse_grain and fine_grain
- valid level_shifter_type is HL, LH and HL_LH
- always_on pins are related to backup power
- a switch cell has VVDD+VDD or VVSS+VSS and VVDD has pg_function where VVDD is virtual VDD;
- a valid retention_cell must be a sequential cell with retention_cell and retention_pin attributes

WHAT NEXT

Correct the invalid values or voltage_name in the map file. For example, if there is a "-" in the voltage_name field, this message occurs. You must input a valid voltage_name; for example, VDD.

EXAMPLES

The following example shows a "-" in the voltage name field, resulting in the error message:

```
BEGIN PG_TO_VOLTAGE_MAP
cell            pg_pin          voltage_name    pg_type
ADDFHX1         VDD             -               power
ADDFHX1         VSS             VSS             primary_ground
END PG_TO_VOLTAGE_MAP
```

SEE ALSO

add_pg_pin_to_db(2)
add_pg_pin_to_lib(2)

LBDB-897 (error) The input library '%s' has pg_pin's defined as signal pins.

DESCRIPTION

When pg_pin's are as signal pins in the library, this message occurs.

add_pg_pin_to_db abd add_pg_pin_to_lib have limitation. In the above case, the utility will stop generation of map template and pg_pin based .lib/db.

WHAT NEXT

Check the contents of the library to see if there are pg_pin's or rail names or in/output_signal_level as signal pins. If so, remove these pin groups in your .lib and try to rerun the utility add_pg_pin_to_lib.

EXAMPLES

EXAMPLE MESSAGE

Error: The input library 'test.lib' has pg_pin's defined as signal pins. (LBDB-897)

LBDB-898 (error) Cell '%s', pin '%s', both 'stage_type : pull_up' and 'stage_type : pull_down' '%s' groups are specified with an identical or overlapping when condition.

DESCRIPTION

This error message occurs when both "stage_type : pull-up" and "stage_type : pull_down" ccs_first_stage/ccs_last_stage groups are specified with an identical or overlapping when condition.

If a first (last) CCB can physically make both rising and falling output transition under the same side-pin condition, then the stage_type of the CCB should be marked as both. The CCSN data should not be split into two stage_type pull_up/pull_down. Otherwise, the characterized result will not be correct.

WHAT NEXT

Check the library source file and correct the incorrect **stage_type** attribute.

EXAMPLES

The following example shows incorrect usage of the **stage_type** attribute, resulting in the error message:

```
cell(bad) {
  ...
```

```
Pin (A) {
...
ccsn_first_stage() {
     stage_type : PULL_UP;
     when : "B";
      }

ccsn_first_stage() {
     stage_type : PULL_DOWN;
     when : "B";
      }
}

}
```

In this example, pin ’A’ has both "stage_type : pull-up" and "stage_type : pull_down" ccs_first_stage groups specified with an identical or overlapping when condition.

LBDB-899 (warning) Cell ’%s’, there is no CCS Noise information.

DESCRIPTION

This warning message occurs when checking cells for CCS Noise information. The tool determined that there are some cells that have CCS Noise data, but no CCS Noise information is defined for the specified cell.

WHAT NEXT

This is only a warning message. No action is required.

If CCS Noise information is not needed for the cell, you can ignore this message. Otherwise, you can add CCS Noise data for the cell and run the command again.

LBDB-900 (error) The %f value of the power distribution table is not between 0 and 1.

DESCRIPTION

This error message occurs when the values of the power distribution tables are not between 0 and 1.

WHAT NEXT

Modify the values of the power distribution tables to meet the requirements. Make sure the values are between 0 and 1.

SEE ALSO

LBDB-901(n)
LBDB-902(n)
LBDB-903(n)
LBDB-904(n)
LBDB-905(n)
LBDB-906(n)
LBDB-907(n)

LBDB-901 (error) Missing power distribution tables in %s.

DESCRIPTION

This error message occurs when a cell contains one leakage power group with power distribution tables, but not all leakage power groups have power distribution tables, or when a pin contains one internal power group with power distribution tables, but not all internal power groups have power distribution tables.

WHAT NEXT

Make sure that all leakage power groups have power distribution tables in a cell, or that all internal power groups have power distribution tables in a pin. Add the missing distribution tables in the .lib file before reading it in.

SEE ALSO

LBDB-900
LBDB-902
LBDB-903
LBDB-904
LBDB-905
LBDB-906
LBDB-907

LBDB-902 (error) The sum of the values in all the distribution tables

attached to %s table is not equal to 1.

DESCRIPTION

This error message occurs when the sum of all values in the distribution tables are not equal to 1. Each value in the distribution table must be between 0 and 1, and the sum of them should be 1.

WHAT NEXT

Check all the values in all distribution tables attached to the specified leakage power or internal power to make sure that each value is between 0 and 1, and the sum of them is 1. Update the values as needed to meet the requirements.

SEE ALSO

LBDB-900
LBDB-901
LBDB-903
LBDB-904
LBDB-905
LBDB-906
LBDB-907

LBDB-903 (error) In an internal power group, the number of values for power and power distribution tables are not the same.

DESCRIPTION

This error message occurs when the number of values in the paired power and power distribution tables are not the same in the internal power group. For example, there are 5 values in the rise power table, but there are 6 values in the paired rise power distribution table.

WHAT NEXT

Check the internal power group for the number of values between the power group and paired power distribution table, rise power group and paired rise power distribution table, or fall power group and paired fall power distribution table. Make sure the number is the same.

SEE ALSO

LBDB-900

LBDB-901
LBDB-902
LBDB-904
LBDB-905
LBDB-906
LBDB-907

LBDB-904 (error) The %s distribution tables are not paired with the %s tables in the internal power group.

DESCRIPTION

This error message occurs when power, rise, or fall power distribution tables are not paired with the related power group. For example, when the rise power distribution table is found in the internal power group but no rise power table is found, the tool issues this error message.

WHAT NEXT

Check the power distribution tables in the internal power group. When the power, rise power, or fall power distribution tables are found, there must be paired power, rise power, fall power groups. If this is not the case, remove the unpaired power distribution tables or add paired power, rise power, fall power groups before reading in the .lib file.

SEE ALSO

LBDB-900
LBDB-901
LBDB-902
LBDB-903
LBDB-905
LBDB-906
LBDB-907

LBDB-905 (error) Indices for the distribution tables are not matched with the paired rise power, fall power, or power groups.

DESCRIPTION

This error message occurs when the indices for the distribution tables are not

matched with the paired rise power, fall power, or power groups.

WHAT NEXT

In the internal power group, check the power template and indices for distribution tables and its paired rise power, fall power, or power groups. If the power template is used, they should be the same for distribution tables and its paired rise power, fall_power, or power groups. Index_1 and index_2 for distribution tables and its paired rise power, fall power, or power groups should also be the same. If necessary, update the power template and indices to meet the requirements.

SEE ALSO

LBDB-900
LBDB-901
LBDB-902
LBDB-903
LBDB-904
LBDB-906
LBDB-907

LBDB-906 (error) Missing related_ground_pin in the power distribution table.

DESCRIPTION

This error message occurs when no related_ground_pin is specified in the power distribution table.

WHAT NEXT

Check the power distribution table to determine if the related_ground_pin attribute is specified. If necessary, add the missing attribute before reading in the .lib file.

SEE ALSO

LBDB-900
LBDB-901
LBDB-902
LBDB-903
LBDB-904
LBDB-905
LBDB-907

LBDB-907 (error) Invalid ground_pin %s with incorrect pg_type.

DESCRIPTION

This error message occurs when the ground_pin is not a valid PG pin defined for the cell with pg_type of primary_ground, backup_ground, or internal_ground.

WHAT NEXT

Check the pg_type of the related_ground_pin in the power distribution table to see if it is primary_ground, backup_ground, or internal_ground. If the related_ground_pin is not specified as one of the 3 types, it is not a valid ground pin in the power distribution table. Re-specify a valid ground pin for power distribution.

SEE ALSO

LBDB-900
LBDB-901
LBDB-902
LBDB-903
LBDB-904
LBDB-905
LBDB-906

LBDB-908 (error) Cell ’%s’, pin ’%s’, the logic represented by the ’when’ attribute (%s) in the ’%s’ group is a superset of the logic represented by the ’when’ attribute (%s) in the timing group.

DESCRIPTION

This error message indicates that the "when" attribute in the ccsn_first_stage or ccsn_last_stage group is a superset of the "when" attribute in the current timing group.

The "when" condition in the ccsn_first_stage or ccsn_last_stage group can only be a subset of the "when" condition in the current timing group. Otherwise, the characterized result is not correct.

WHAT NEXT

Check the library source file, and correct the incorrect "when" attribute.

EXAMPLES

The following example results in this error. The "when" condition "A+B" in the ccsn_first_stage is a superset of the "when" condition "A" of the timing group.

```
cell(bad) {
   Pin (A) {
      timing () {
         when : "A";
         ccsn_first_stage() {
            when : "A+B";
            ...
         }
         ...
      }
      ...
   }
   ...
}
```

EXAMPLE MESSAGE

```
Error: Cell 'bad', pin 'A', the logic represented by the 'when' attribute (A+B) in
'ccsn_first_stage' group is a superset of the logic represented by the 'when'
attribute (A) in the timing group.
```

LBDB-909 (warning) The cell should have at least 1 primary_ground pg_pin and at least 1 primary_power pg_pin.

DESCRIPTION

This warning message occurs because in the new libraries based on pg_pin, all of the cells must have at least 1 primary_ground pg_pin and at least 1 primary_power pg_pin.

WHAT NEXT

This is only a warning message. No action is required if users do not want to modify the cell pg pin modeling.

However, if users want to avoid this warning message, add the missing primary_ground pg_pin or primary_power pg_pin and run the command again.

LBDB-910 (warning) The cell skips partial PG requirement checking.

DESCRIPTION

This warning message advises you that cells in the specified category skip PG pin requirement checking. The cells could have partial PG pins, meaning the cells are without a primary_power pg_pin or a primary_ground pg_pin. Currently, there is only one type ETM cell in the category.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this warning message, add the missing primary_ground pg_pin or primary_power pg_pin and run the command again.

LBDB-911 (error) The attribute '%s' violates the variation-aware consistence rule.

DESCRIPTION

This warning message advises you that the variation data in the library violates the consistence rule. If any variation attribute contains N/2N data entries, all variation attributes in the same library must also contain N/2N entries at the same N/2N process points (va_values). The number of data entries must be either N or 2N for any variation attribute. This checking rule includes the following models:

- VA Timing Constraint Model
- VA Compact CCS Timing Driver Model
- VA CCS Timing Receiver Model (arc-based and pin-based)

WHAT NEXT

Add the missing variation attribute or correct the process point (va_values). This message appears only once on the first violation entry. Check the other entries in the variation group for violations.

LBDB-912 (error) The variation needs to be consistent across corresponding arcs.

DESCRIPTION

This error message occurs when a variation inconsistency is found among the timing arcs. If the timing_based_variation group exists in a timing arc, all its corresponding timing arcs must also contain the timing_based_variation group. Otherwise, none of the arcs can contain the timing_based_variation group.

WHAT NEXT

Add the missing timing_based_variation in the corresponding timing arcs and run the command again.

LBDB-913 (warning) Cell '%s' is missing '%s' pg_pin so it will become a black box cell for multivoltage functional optimization flow. It is being marked dont_touch, dont_use.

DESCRIPTION

This warning message occurs when a cell has 2 or more power or ground pins, but there is no backup power or backup ground pin.

The following conditions apply to retention and isolation cells:

- If a cell has 2 or more power pins, there must be a backup power pin.
- If a cell has 2 or more ground pins, there must be a backup ground pin.

If the conditions are not met, the tool issues this warning message. The cell is black box for the multivoltage flow and is marked as dont_touch, dont_use (d,u). The black box cannot be recognized during functional optimization by the tools (Power Compiler and IC Compiler).

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, add or correct the backup_ground pg_pin or backup_power pg_pin and run the command again.

LBDB-914 (warning) Cell '%s', pin '%s', is missing

related_power_pin to a '%s' pg_pin, so it will become a black box cell for multivoltage functional optimization flow. It is being marked as dont_touch, dont_use.

DESCRIPTION

This warning message occurs when a cell has no related_power_pin, or when the related_power_pin relates to an incorrect pg_pin.

For retention cells, if save and restore pins exist, they should be related to the backup power or ground, depending on whether backup power or ground is available. All other signal pins should be related to the primary power or ground. For isolation cells, if a backup power pin exists, the output pin must be related to backup power through a related_power_pin.

The cell is black box for the multivoltage flow and is marked as dont_touch, dont_use (d,u). it cannot be recognized during functional optimization by the tools (Power Compiler and IC Compiler).

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, add or correct the related_power_pin and run the command again.

LBDB-915 (warning) Cell '%s', pin '%s', is missing related_ground_pin to a '%s' pg_pin, so it will become a black box cell for multivoltage functional optimization flow. It is being marked dont_touch, dont_use.

DESCRIPTION

This warning message occurs when a cell has no related_ground_pin, or when the related_ground_pin is related to an incorrect pg_pin.

For retention cells, if save and restore pins exist, they should be related to the backup power or ground, depending on whether backup power or ground is available. All other signal pins should be related to the primary power or ground.

The cell is black box for the multivoltage flow and is marked as dont_touch, dont_use (d,u). It cannot be recognized during functional optimization by the tools (Power Compiler and IC Compiler).

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, add or correct the related_ground_pin and run the command again.

LBDB-916 (warning) Cell '%s', pin '%s' and pin '%s' have different related_power_pin settings, so it will become a black box cell for multivoltage functional optimization flow. It is being marked dont_touch/dont_use.

DESCRIPTION

This warning message occurs when the 2 specified pins do not relate to the same **related_power_pin**.

For a level-shifter cell, the enable pin and the output pin must be related to the same power pin.

The cell is black box for the multivoltage flow and is marked as dont_touch, dont_use (d,u). It cannot be recognized during functional optimization by the tools (Power Compiler and IC Compiler).

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, make sure the specified pins have the same **related_power_pin** and run the command again.

LBDB-917 (warning) no pg_pin or signal pin in this pad cell.

DESCRIPTION

This message indicates this pad cell hasn't a signal pin or pg_pin.

WHAT NEXT

Add one signal pin or pg_pin with attribute "is_pad : true".

EXAMPLES

```
  cell(AN2) {
      pad_cell : true;
      ...
  }
```

In this case, the IO cell has no signal pin or pg_pin. To fix the problem, add one signal pin or pg_pin with attribute "is_pad : true".

Warning: Line 12, Cell 'AN2', no pg_pin or signal pin in this pad cell. (LBDB-917)

LBDB-996 (error) The timing arc's fpga_arc_condition attribute contains invalid format '%s.%s'.

DESCRIPTION

This message indicates that you specified invalid <pin_name>.<pin_status> or <fpga_cond_name>.<fpga_cond_value_name> in the fpga_arc_condition attribute of the timing arc.

WHAT NEXT

Modify <A>.<B> to make it as a valid <pin_name>.<pin_status> or <fpga_cond_name>.<fpga_cond_value_name>.

EXAMPLES

```
cell(test) {

  ...
  pin(A) {
      ...
  }
  pin(B) {
      ...
timing() {
...
fpga_arc_condition: "wrong_pin.CONNECTED";
...
}
      ...
  }
  ...
}
```

We can correct it by replace "wrong_pin" with "A".

EXAMPLE MESSAGE

```
Error: Line 206, The timing arc's fpga_arc_condition attribute contains
invalid format 'wrong_pin.CONNECTED'. (LBDB-996)
```

LBDB-997 (warning) The fpga_condition(%s) group is defined multiple times.

DESCRIPTION

This message indicates that you specified the same fpga_condition group multiple times. Only the last one is retained.

WHAT NEXT

Change the group name, or delete the duplicated group.

EXAMPLES

```
cell(CGNP) {
  area : 1;

  fpga_condition(cond1) {
    ...
  }
  fpga_condition(cond1) {
    ...
  }
  ...
}
```

EXAMPLE MESSAGE

```
Warning: Line 206, The fpga_conditino(cond1) group is defined
multiple times. (LBDB-997)
```

LBDB-998 (error) The fpga condition '%s' has no values defined.

DESCRIPTION

A fpga_condition group must have at least one fpga condition value defined.

WHAT NEXT

Define the fpga condition values.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  fpga_condition(cond1) {
  }
  ...
}
```

EXAMPLE MESSAGE

Error: Line 206, The fpga condition ’cond1’ has no values defined. (LBDB-998)

LBDB-999 (warning) The fpga_condition_value(%s) group is defined multiple times.

DESCRIPTION

This message indicates that you specified the same fpga_condition_value group multiple times. Only the last one is retained.

WHAT NEXT

Change the group name, or delete the duplicated group.

EXAMPLES

```
cell(CGNP) {
  area : 1;

  fpga_condition(cond1) {
    fpga_condition_value(normal) {
      fpga_arc_condition : "operation_mode=normal";
    }
    fpga_condition_value(normal) {
      fpga_arc_condition : "operation_mode=arithmetic";
    }
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 206, The fpga_condition_value(normal) group is defined
multiple times. (LBDB-999)
```

LBDB-1000 (error) The fpga_arc_condition attribute is not specified
for the fpga_condition_value.

DESCRIPTION

This message indicates that you have not specified fpga_arc_condition attribute within fpga_condition_value.

WHAT NEXT

Add the missing fpga_arc_condition attribute.

EXAMPLES

```
cell(CGNP) {
  area : 1;
  fpga_condition(cond1) {
    fpga_condition_value(normal) {
      fpga_arc_condition : "operation_mode=normal";
    }
  }
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 206, The fpga_arc_condition attribute is not specified for the
fpga_condition_value. (LBDB-1000)
```

LBDB-1001 (error) Found one or more cells defined before '%s' group.

DESCRIPTION

This message indicates the named group in phys_library is not defined before all cell groups.

WHAT NEXT

Move this group inside the physical library so that it is defined in front of all cell groups.

EXAMPLES

```
    phy_library(test) {
...
macro (cell1) {
 ...
}
resource ( std_cell ) {
        ...
}
    }
```

EXAMPLE MESSAGE

Error: Line 59, Found one or more cells defined before ’resource’ group. (LBDB-1001)

LBDB-1002 (error) The resource name is not supported.

DESCRIPTION

Library Compiler accepts resource with the following names: - std_cell - array

This message indicates the resource group is using a name other than mentioned above.

WHAT NEXT

Change the resource group name to either "std_cell" or "array".

EXAMPLES

```
    phys_library(test) {
...
resource ( wrong_name ) {/* ERROR */
        ...
}
    }
```

EXAMPLE MESSAGE

Error: Line 5, The resource name is not supported. (LBDB-1002)

LBDB-1003 (error) The resource group does not contain any layer definition.

DESCRIPTION

Library Compiler requires that one or more layer definition be defined in the resource group. A layer definition can be one of the following functions / groups: - device_layer - contact_layer - overlap_layer - routing_layer

This message indicates there is none of the above defined in the resource group.

WHAT NEXT

Add layer information into resource group.

EXAMPLES

```
    phys_library(test) {
resource ( std_cell ) {/* ERROR */
}
...
    }
```

EXAMPLE MESSAGE

Error: Line 3, The resource group does not contain any layer definition. (LBDB-1003)

LBDB-1004 (error) The resource group does not contain any site / tile definition.

DESCRIPTION

Library Compiler requires that one or more site / tile groups be defined in the resource group.

This message indicates there is neither any site nor any tile groups defined in the resource group.

WHAT NEXT

Add site information into resource group.

EXAMPLES

```
    phys_library(test) {
```

```
resource ( std_cell ) {/* ERROR */
}
...
    }
```

EXAMPLE MESSAGE

```
Error: Line 3, The resource group does not contain any site /
 tile definition. (LBDB-1004)
```

LBDB-1005 (warning) Found a duplicate %s attribute. Using the first value.

DESCRIPTION

This message indicates an attribute has been defined twice. The second definition is ignored.

WHAT NEXT

Remove the duplicate definition of the attribute.

EXAMPLES

```
    phys_library(test) {
...
macro(and2) {
  ...
}
macro(and2a) {
  ...
}
macro(and2a1) {
          ...
  eq_cell : and2a;
  eq_cell : and2;
  ...
}
    }
```

EXAMPLE MESSAGE

```
Warning: Line 34, Found a duplicate eq_cell attribute. Using the first value. (LBDB-
1005)
```

LBDB-1006 (error) Cannot accept the ’%s’ pin as the logically

equivalent pin.

DESCRIPTION

This message indicates the eq_pin attribute value is an unacceptable pin name. An unacceptable eq_pin is defined as either - a name equivalent to the current pin name; or - a pin that is not already defined.

WHAT NEXT

Check the pin name and change it. Also make sure the pin specified in the eq_pin attribute is pre-defined.

EXAMPLES

```
    phys_library(test) {
...
macro(and2) {
          ...
  pin(a) {
    eq_pin : a1; /* error */
    ...
  }
  pin(a1) {
  }
}
    }
```

EXAMPLE MESSAGE

Error: Line 34, Cannot accept the ’a1’ pin as the logically equivalent pin. (LBDB-1006)

LBDB-1007 (error) The %s name ’%s’ is an undefined layer name.

DESCRIPTION

This message indicates the obs / geometry group name is not a legal layer name.

WHAT NEXT

Use a pre-defined layer name as the name for the obs / geometry group.

EXAMPLES

```
    phys_library(test) {
...
macro(and2) {
          ...
  pin(a) {
    ...
    obs(new_layer) {/* error */
      ...
    }
  }
}
    }
```

EXAMPLE MESSAGE

```
Error: Line 34, The obs name 'new_layer' is an undefined layer name. (LBDB-1007)
```

LBDB-1008 (error) The %s function has inconsistent number of arguments.

DESCRIPTION

This message indicates the path / polygon / rectangle function has wrong number of arguments. In Library Compiler, - a path function requires odd number of arguments no less than 3; - a polygon function requires even number of arguments no less than 8; - a rectangle function requires 4 arguments.

WHAT NEXT

Make sure the right argument is used for each function.

EXAMPLES

```
    phys_library(test) {
...
macro(and2) {
          ...
  pin(a) {
    ...
    obs(new_layer) {
      rectangle(0.1, 0.3);  /* error */
    }
  }
}
    }
```

EXAMPLE MESSAGE

```
Error: Line 34, The rectangle function has inconsistent number of arguments. (LBDB-
1008)
```

LBDB-1009 (error) Non-positive number found in the size function.

DESCRIPTION

This message indicates either the width or the height of the size function is a non-positive number.

WHAT NEXT

Make sure both width or height of the size function are positive numbers.

EXAMPLES

```
    phys_library(test) {
...
macro(and2) {
          ...
  size (-1.5, 2.0); /* error */
}
    }
```

EXAMPLE MESSAGE

```
Error: Line 34, Non-positive number found in the size function. (LBDB-1009)
```

LBDB-1010 (error) The site ’%s’ is not defined in the resource group.

DESCRIPTION

This message indicates name of the site attribute is not a pre-defined site.

WHAT NEXT

Make sure the site attribute uses a pre-defined site.

EXAMPLES

```
    phys_library(test) {
...
macro(and2) {
          ...
  site : new_site;/* error */
}
    }
```

EXAMPLE MESSAGE

```
Error: Line 34, The site 'new_site' is not defined in the resource group. (LBDB-
1010)
```

LBDB-1011 (error) Cannot accept the '%s' macro as the equivalent cell.

DESCRIPTION

This message indicates the eq_cell attribute value is an unacceptable macro name. An unacceptable macro name is defined as either - a name equivalent to the current macro name; or - a macro that is not already defined.

WHAT NEXT

Check the macro name and change it. Also make sure the macro specified in the eq_cell attribute is pre-defined.

EXAMPLES

```
    phys_library(test) {
...
macro(and2a1) {
          ...
  eq_cell : and2;/* error */
  ...
}
macro(and2) {
  ...
}
    }
```

EXAMPLE MESSAGE

```
Error: Line 34, Cannot accept the 'and2' macro as the electrically equivalent cell.
 (LBDB-1011)
```

LBDB-1012 (error) The layer name, '%s', in the '%s' group is not unique.

DESCRIPTION

Each via group can specify up to 3 geometry groups with the 'layer1', 'contact' and 'layer2' groups. The name of each group gives the name of the layer on which all geometry shapes are defined. The 3 geometry groups must be defined on different layers. This error message indicates that 2 or more geometry groups are specified on the same layer.

WHAT NEXT

Check the layer names on the 'layer1', 'contact' and 'layer2' groups and make sure they call for different layer names.

EXAMPLES

```
    phys_library(test) {
...
resource(std_cell) {
          ...
  via (test) {
    ...
    layer1(met1) {
...
    }
    contact(con1) {
...
    }
    layer2(met1) {/* error */
...
    }
  ...
  }
}
    }
```

EXAMPLE MESSAGE

Error: Line 34, The layer name, 'met1', in the 'layer2' group is not unique. (LBDB-1012)

LBDB-1013 (error) The %s function has inconsistent number of

arguments.

DESCRIPTION

This message indicates the via / via_iterate function has wrong number of arguments. In Library Compiler, - a via function requires 3 arguments: a name followed by x / y coordinates; - a via_iterate function requires 7 arguments: 2 integers (for x-iteration and y-iteration), 2 real numbers (for x-spacing and y-spacing), a name and another 2 real numbers for the first x / y coordinates.

WHAT NEXT

Make sure the right argument is used for each function.

EXAMPLES

```
    phys_library(test) {
...
macro(and2) {
          ...
  pin(a) {
    ...
    obs(new_layer) {
      via(0.1, 0.3);  /* error */
    }
  }
}
    }
```

EXAMPLE MESSAGE

Error: Line 34, The via function has inconsistent number of arguments. (LBDB-1013)

LBDB-1014 (error) The via group does not have a ’contact’ group.

DESCRIPTION

Each via group is required to have a ’contact’ group defined for the geometry in the contact layer. This error message indicates that the ’contact’ group is missing from the current via group.

WHAT NEXT

Make sure the ’contact’ group is defined in current ’via’ group.

EXAMPLES

```
    phys_library(test) {
...
resource(std_cell) {
          ...
  via (test) {/* error */
    layer1(met1) {
...
    }
    layer2(met2) {
...
    }
  ...
  }
}
    }
```

EXAMPLE MESSAGE

```
Error: Line 34, The via group does not have a 'contact' group. (LBDB-1014)
```

LBDB-1015 (error) One or more rectangles are required in this group.

DESCRIPTION

The 'layer1', 'contact' and 'layer2' sub-groups inside a 'via' group define the geometry shapes for the via. This error message indicates that the current sub-group has no rectangle specified.

WHAT NEXT

Make sure there are at least 1 rectangle defined in the current sub-group. Otherwise, remove the sub-group altogether.

EXAMPLES

```
    phys_library(test) {
...
resource(std_cell) {
          ...
  via (test) {
    layer1(con1) { }/* error */
    ...
  }
}
    }
```

EXAMPLE MESSAGE

```
Error: Line 34, One or more rectangles are required in this group. (LBDB-1015)
```

LBDB-1016 (error) The routing_grid function has inconsistent number of arguments.

DESCRIPTION

This message indicates the routing_grid function has wrong number of arguments. In Library Compiler, - a routing_grid function requires 6 arguments: x-starting-coordinate, number-of-columns, x-space, y-start-coordinate, number-of-rows, y-space.

WHAT NEXT

Make sure the right arguments are used for each function.

EXAMPLES

```
    phys_library(test) {
      ...
      array(ABC) {
        routing_grid(100, 200);
...
      }
      ...
    }
```

EXAMPLE MESSAGE

```
Error: Line 34, The routing_grid function has inconsistent number of arguments. (LB
DB-1016)
```

LBDB-1017 (error) The floorplan group contains mismatching site_array group.

DESCRIPTION

This message indicates that either: - the default floorplan (with no given name) is missing site_array with "regular" placement_rule; or - the non-default floorplan contains site_array with "regular" placement_rule.

The default floorplan should contain one or more "regular" site_array groups. The non-default floorplan should not contain any "regular" site_array group.

WHAT NEXT

Check all site_array groups under the current floorplan and make sure the above rules are followed.

EXAMPLES

```
    phys_library(test) {
      ...
      array(ABC) {
        floorplan() {
        site_array(new) {
    placement_rule : can_place;
    ...
  }
        }
...
      }
      ...
    }
```

EXAMPLE MESSAGE

Error: Line 34, The floorplan group contains mismatching site_array group. (LBDB-1017)

LBDB-1018 (warning) The floorplan group does not contain can_place/cannot_occupy site_array groups.

DESCRIPTION

This message indicates that the current floorplan group only contain site_array groups with "regular" placement_rule.

WHAT NEXT

Make sure this is the correct physical library technology data.

EXAMPLES

```
    phys_library(test) {
      ...
      array(ABC) {
        floorplan() {
        site_array(new) {
    placement_rule : regular;
```

```
    ...
  }
        }
...
      }
      ...
    }
```

EXAMPLE MESSAGE

```
Warning: Line 34,  The floorplan group does not contain can_place/cannot_occupy
 site_array groups.  (LBDB-1018)
```

LBDB-1019 (error) The array group does not contain base floorplan.

DESCRIPTION

This message indicates that the current array group contain no base floorplan data. An array group must have a base floorplan group - i.e. a floorplan group defined with no given name.

WHAT NEXT

Add base floorplan data into this array group.

EXAMPLES

```
    phys_library(test) {
      ...
      array(ABC) {
        floorplan(NEW) {
    ...
  }
      }
...
      }
      ...
    }
```

EXAMPLE MESSAGE

```
Error: Line 34,  The floorplan group does not contain base floorplan.  (LBDB-1018)
```

LBDB-1020 (error) The '%s' function has inconsistent number of

arguments.

DESCRIPTION

This message indicates the iterate function in the current site_array has wrong number of arguments. In Library Compiler, - a iterate function requires 4 numerical arguments.

WHAT NEXT

Make sure the right arguments are used for each function.

EXAMPLES

```
    phys_library(test) {
      ...
      array(ABC) {
        site_array(test) {
  iterate (100, 200);
  ..
}
...
      }
      ...
    }
```

EXAMPLE MESSAGE

Error: Line 34, The iterate function has inconsistent number of arguments. (LBDB-1020)

LBDB-1021 (error) The resource group does not contain any via definition.

DESCRIPTION

Library Compiler requires that one or more via groups be defined in the resource group.

This message indicates there is no via groups defined in the resource group.

WHAT NEXT

Add via information into resource group.

EXAMPLES

```
    phys_library(test) {
resource ( std_cell ) {/* ERROR */
}
...
    }
```

EXAMPLE MESSAGE

```
Error: Line 3, The via group does not contain any site definition. (LBDB-1021)
```

LBDB-1022 (error) The resource group must be defined before the topological_design_rules group.

DESCRIPTION

Library Compiler requires all physical library plib file to specify the resource group before specifying the topological_design_rules group.

This message indicates there is no resource group defined before the topological_design_rules group.

WHAT NEXT

Add or move the resource group to the front of the topological_design_rules group.

EXAMPLES

```
    phys_library(test) {
topological_design_rules ( ) {/* ERROR */
}
...
    }
```

EXAMPLE MESSAGE

```
Error: Line 2, The resource group must be defined before the
             topological_design_rules group.  (LBDB-1022)
```

LBDB-1023 (warning) No ’%s’ group defined in the

topological_rules group.

DESCRIPTION

There is no specified group information in the current library.

WHAT NEXT

Make sure the library is correct.

EXAMPLES

```
    phys_library(test) {
      resource(std_cell) {
        ...
      }
      topological_rules() {
      }
      ...
    }
```

EXAMPLE MESSAGE

Warning: Line 34, No via_rule group defined in the topological_rules group. (LBDB-1023)

LBDB-1024 (error) The %s function has inconsistent number of arguments.

DESCRIPTION

This message indicates the min_generate_via_size function has wrong number of arguments. In Library Compiler, it requires 2 floating numbers in the min_generated_via_size function.

WHAT NEXT

Make sure the right argument is used for the function.

EXAMPLES

```
    phys_library(test) {
min_generated_via_size (0.1, 0.2, 0.1);
...
    }
```

EXAMPLE MESSAGE

```
Error: Line 2, The min_generated_via_size function has inconsistent number of argum
ents. (LBDB-1024)
```

LBDB-1025 (error) The '%s' function cannot be supplied a nonpositive value.

DESCRIPTION

This message indicates that the specified function cannot have a nonpositive value.

WHAT NEXT

Change all value of the function to positive in the physical library file.

EXAMPLES

```
    min_generate_via_size(-1, 0.3);
```

EXAMPLE MESSAGE

```
Error: Line 18, The 'min_generate_via_size' function cannot be supplied a
       nonpositive value. (LBDB-1025)
```

LBDB-1026 (error) The '%s' function has inconsistent arguments.

DESCRIPTION

This message indicates the same_net_min_spacing function has wrong arguments. In Library Compiler, it requires 2 layer names followed by a floating numbers and a boolean value (TRUE or FALSE) in the same_net_min_spacing function.

WHAT NEXT

Make sure the right argument is used for the function.

EXAMPLES

```
    phys_library(test) {
same_net_min_spacing (metal1, metal2, 0.1);
...
```

```
    }
```

EXAMPLE MESSAGE

```
Error: Line 2, The ’same_net_min_spacing" function has inconsistent arguments. (LBD
B-1026)
```

LBDB-1027 (error) The ’%s’ function has inconsistent arguments.

DESCRIPTION

This message indicates the contact_spacing function has wrong arguments. In Library Compiler, it requires 2 floating numbers in the contact_spacing function.

WHAT NEXT

Make sure the right argument is used for the function.

EXAMPLES

```
    phys_library(test) {
...
contact_spacing (0.1, 0.2);
...
    }
```

EXAMPLE MESSAGE

```
Error: Line 158, The ’contact_spacing" function has inconsistent arguments. (LBDB-
1027)
```

LBDB-1028 (error) The ’%s’ layer name is of invalid layer type. A %s name is expected.

DESCRIPTION

This message indicates that you specified an layer name with wrong type for the current attribute or function. The name should be a routing_layer or contact_layer name as indicated in the error message.

WHAT NEXT

Check your library to see if you have an error in either previous layer definition or the current attribute / function.

EXAMPLES

```
   contact_min_spacing(metal1, contact1, 0.1);
```

EXAMPLE MESSAGE

Error: Line 104, The ’metal1’ layer name is of invalid layer type. A contact_layer name is expected. (LBDB-1028)

LBDB-1029 (error) There is no rectangle defined in the contact_formula group.

DESCRIPTION

There is no rectangle defined in the current contact_formula group. Library Compiler requires at least 1 rectangle being specified in each contact_formula group.

WHAT NEXT

Define the rectangle shape for the contact_formula group.

EXAMPLES

```
    via_rule_generate(GEN1) {
      contact_formula(con1) { /* error */
routing_direction : horizontal;
resistance : 0.2;
      }
    }
```

EXAMPLE MESSAGE

Warning: Line 34, There is no rectangle defined in the contact_formula group. (LBDB-1029)

LBDB-1030 (error) The ’%s’ attribute value is larger than the

'%s' attribute value.

DESCRIPTION

This message indicates that the 'min_wire_width' value is larger than 'max_wire_width' value. Library Compiler requires that the 'min_wire_width' is no larger than 'max_wire_width' value.

WHAT NEXT

Change all related values follow the requirement.

EXAMPLES

```
routing_layer_rule(met1) {
  min_wire_width : 2.0;
  max_wire_width : 1.0;
  ...
}
```

EXAMPLE MESSAGE

Error: Line 18, The 'min_wire_width' attribute value is larger than the 'max_wire_width' attribute value. (LBDB-1030)

LBDB-1031 (error) The wire_rule group is empty.

DESCRIPTION

This message indicates the wire_rule group does not have any layer_rule / via group or same_net_min_spacing function defined. Library Compiler requires that the wire_rule group not be empty.

WHAT NEXT

Make sure the the wire_rule group is not empty.

EXAMPLES

```
wire_rule(rule1) {
}
```

EXAMPLE MESSAGE

Error: Line 34, The wire_rule group is empty. (LBDB-1031)

LBDB-1032 (error) Cannot accept the '%s' pin as the must_join pin.

DESCRIPTION

This message indicates the must_join pin attribute value is an unacceptable pin name. An unacceptable must_join is defined as either - a name equivalent to the current pin name; or - a pin that is not already defined.

WHAT NEXT

Check the pin name and change it. Also make sure the pin specified in the must_join attribute is pre-defined.

EXAMPLES

```
    phys_library(test) {
...
macro(and2) {
          ...
  pin(a) {
    must_join : a1; /* error */
    ...
  }
  pin(a1) {
  }
}
    }
```

EXAMPLE MESSAGE

Error: Line 34, Cannot accept the 'a1' pin as the must_join pin. (LBDB-1032)

LBDB-1033 (error) The '%s' function has inconsistent arguments.

DESCRIPTION

This message indicates the ranged_spacing function has wrong arguments. In Library Compiler, it requires 3 floating numbers in the ranged_spacing function.

WHAT NEXT

Make sure the right argument is used for the function.

EXAMPLES

```
    phys_library(test) {
ranged_spacing (0.1, 0.2);
...
    }
```

EXAMPLE MESSAGE

```
Error: Line 2, The 'ranged_spacing" function has inconsistent arguments. (LBDB-1033)
```

LBDB-1034 (warning) The '%s' %s group already exists and cannot be overwritten. The first definition will be used.

DESCRIPTION

This message indicates that you multiply defined a site group. Library Compiler does not allow the overwriting of existing site groups.

WHAT NEXT

Delete the second specification of the site group.

EXAMPLES

```
site(IOsite) {
 ...
}
site(IOsite) {
 ...
}
```

EXAMPLE MESSAGE

```
Error: Line 31, The 'IOsite' site group already exists and
       cannot be overwritten. The first definition will be used. (LBDB-1034)
```

LBDB-1035 (error) The '%s' array must have '%d' entries.

DESCRIPTION

You receive this message because the specified array has a different size from the one expected.

Where *N* is the number of routing layers, the following criteria are set:

plate_cap array must have ((N * (N-1)) / 2) entries
overlap_wire_ratio must have (N * (N-1)) entries
adjacent_wire_ratio must have N entries
wire_ratio_x must have N entries
wire_ratio_y must have N entries

WHAT NEXT

Correct the values in the specified array.

EXAMPLES

```
plate_cap( "0.05, 0.06, 0.03" );
```

EXAMPLE MESSAGE

Error: Line 127, The 'plate_cap' array must have '6' entries. (LBDB-1035)

LBDB-1036 (error) The sum of values in the '%s' array attribute does not meet the requirement.

DESCRIPTION

You receive this message because the sum of ratios does not match the specified criteria. The following criteria are set:

overlap_wire_ratio: the sum of value[i(N-1)] to value[i(N-1)+(N-2)] must not exceed 100.0 (100 percent); where *N* is the number of routing layers and *i* is the routing layer id in the range of i=0..N-1.

adjacent_wire_ratio: n/a (not applicable);

wire_ratio_x: the sum of all values must equal 100.0 (100 percent);

wire_ratio_y: the sum of all values must equal 100.0 (100 percent).

WHAT NEXT

Correct the values in the specified array.

EXAMPLES

```
wire_ratio_x( "40.1, 20.0, 20.5" );
```

EXAMPLE MESSAGE

```
Error: Line 127, The sum of values in the 'wire_ratio_x' array attribute does not
meet requirement. (LBDB-1036)
```

LBDB-1037 (error) Cannot accept the '%s' as the default_routing_wire_model value.

DESCRIPTION

You receive this message because the default_routing_wire_model attribute value is an unacceptable routing_wire_model name, that is, one that is a routing_wire_model that has not already been defined.

WHAT NEXT

Change the routing_wire_model name. Ensure that the routing_wire_model specified in the default_routing_wire_model attribute is predefined.

EXAMPLES

```
phys_library(test) {
    ...
    resource(...) {
      ...
      default_routing_wire_model : model_1;          /* error */
      ...
      routing_wire_model(model_1) {
      ...
      }
    }
}
```

EXAMPLE MESSAGE

```
Error: Line 34, Cannot accept the 'model_1' as the default_routing_wire_model value.
(LBDB-1037)
```

LBDB-1038 (error) The plate_cap attribute is not predefined.

DESCRIPTION

You receive this message because the **plate_cap** attribute is not predefined. It has not been defined before the routing_wire_model() group is defined.

WHAT NEXT

Ensure that **plate_cap** is defined before the routing_wire_model() group is defined.

EXAMPLES

```
phys_library(test) {
    ...
    resource(...) {
      ...
      routing_wire_model(model_1) { /* error: LBDB-1038 */
      ...
      }
      plate_cap ("0.05, 0.04, 0.06");
    }
}
```

EXAMPLE MESSAGE

Error: Line 34, The plate_cap attribute is not predefined. (LBDB-1038)

LBDB-1039 (error) The '%s' attribute has an out-of-range '%f' ratio.

DESCRIPTION

You receive this message because a percentage ratio in an array attribute is larger than 100.0 (100%) or less than 0 (0%); it has not been accepted.

WHAT NEXT

Ensure that all values are between 0.0 (0%) and 100.0 (100%).

EXAMPLES

```
    phys_library(test) {
        ...
        resource(...) {
          ...
          routing_wire_model(model_1) {
            ...
            wire_ratio_x ("21.3, 305.4, 19.4"); /* error */
            ...
          }
        }
    }
```

EXAMPLE MESSAGE

```
Error: Line 34, The 'wire_ratio_x' attribute has an out-of-range '305.4' ratio.
(LBDB-1039)
```

LBDB-1040 (error) The %s function has an inconsistent number of arguments.

DESCRIPTION

You receive this message because the **obs_clip_box** or **keepout_clip_box** function has the wrong number of arguments. In Library Compiler, the specified command requires four floating numbers in the **obs_clip_box** or **keepout_clip_box** function.

WHAT NEXT

Ensure that the right argument is used for the specified function.

EXAMPLES

```
keepout_clip_box (0.1, 0.2, 0.1);
...
```

EXAMPLE MESSAGE

```
Error: Line 25 The keepout_clip_box function has an inconsistent number of
arguments. (LBDB-1040)
```

LBDB-1041 (error) The %s function has inconsistent arguments.

DESCRIPTION

You receive this message because the **gds2_layer_map** function has the wrong number or type of arguments. In Library Compiler, the specified function requires an integer, a string, and an integer in the **gds2_layer_map** function.

WHAT NEXT

Ensure that the right argument is used for the function.

EXAMPLES

```
gds2_layer_map (0.1, METAL1, 1);
```

EXAMPLE MESSAGE

```
Error: Line 30, The gds2_layer_map function has inconsistent arguments. (LBDB-1041)
```

LBDB-1042 (warning) The dist_conversion_factor value '%d' is not allowed. Using default value '%d'.

DESCRIPTION

You receive this message because you specified a dist_conversion_factor value that either is not a multiple of 100 or may be a nonpositive number.

WHAT NEXT

Examine the library source file, and correct the dist_conversion_factor value.

EXAMPLES

```
dist_conversion_factor : 123;
```

EXAMPLE MESSAGE

```
Warning: Line 85, The dist_conversion_factor value '123' is not allowed. Using
default value '1000'. (LBDB-1042)
```

LBDB-1043 (error) The gds2_conversion_factor value '%d' is not allowed.

DESCRIPTION

You receive this message because you specified a **gds2_conversion_factor** value that is not a multiple of 100s or may be a nonpositive number.

WHAT NEXT

Examine the library source file, and correct the **gds2_conversion_factor** value.

EXAMPLES

```
gds2_conversion_factor : -100;
```

EXAMPLE MESSAGE

```
Warning: Line 85, The gds2_conversion_factor value '-100' is not allowed. (LBDB-
1043)
```

LBDB-1044 (error) The process resource group must be defined after the resource group and the topological design rules group.

DESCRIPTION

This message indicates that there is no resource group and/or topological design rules group defined before the process resource group. Library Compiler requires all physical library plib files to specify the resource group and the topological_design_rules group before specifying the process_resource group.

WHAT NEXT

Add or move the resource group and the topological design rules group to the front of the process resource group.

EXAMPLES

```
    phys_library(test) {
process_resource (...) {/* ERROR */
}
...
    }
```

EXAMPLE MESSAGE

```
Error: Line 2, The process_resource group must be defined after the
             resource group and the topological_design_rules group.  (LBDB-1044)
```

LBDB-1045 (error) The %s name '%s' is an undefined %s

name.

DESCRIPTION

This error message means that the specified process routing layer, process via, or process wire rule name was not predefined.

WHAT NEXT

Use the **read_lib** command and specify a predefined routing layer, via, or process wire rule.

EXAMPLES

```
    phys_library(test) {
resource(...) {
  routing_layer (met1) {
  }
}
process_resource(...) {
  process_routing_layer(METAL1) { /
* ERROR: METAL 1 is not defined.  Use met1 instead */
        }
...
macro(and2) {
          ...
  pin(a) {
    ...
    obs(new_layer) {/* error */
      ...
    }
  }
}
    }
```

EXAMPLE MESSAGE

Error: Line 34, The process_routing_layer name 'METAL1' is an undefined routing_lay er name. (LBDB-1045)

LBDB-1046 (warning) The boundary_layer attribute is not defined in

gds2_extraction_rules.

DESCRIPTION

This warning message tells you that you used the **read_lib** command and specified the **boundary_layer** attribute, but the **boundary_layer** attribute is not defined in gds2_extraction_rules. In Library Compiler, the **boundary_layer** attribute specifies a layer ID for GDSII extraction to look for the designated macro boundary for the macro size in the PLIB file. When this attribute is missing, the macro size in the PLIB file is determined by the bounding box of all geometries.

WHAT NEXT

Make sure you did not intend to specify the boundary layer. If you did intend to specify the boundary layer, define the **boundary_layer** attribute and reexecute the command.

EXAMPLE MESSAGE

Warning: The boundary_layer attribute is not defined in gds2_extraction_rules. (LBDB-1046)

SEE ALSO

read_lib (2).

LBDB-1047 (error) The '%s' function has inconsistent arguments.

DESCRIPTION

This message indicates the lateral_oxide function has wrong arguments. In Library Compiler, it requires 2 floating numbers in the lateral_oxide function.

WHAT NEXT

Make sure the right argument is used for the function.

EXAMPLES

```
lateral_oxide (0.1, 0.2, 0.3);
```

EXAMPLE MESSAGE

```
Error: Line 2, The 'lateral_oxide" function has inconsistent arguments. (LBDB-1047)
```

LBDB-1048 (error) The '%s' permittivity value is less than 1.00.

DESCRIPTION

The permittivity value must be at least 1.00. It also includes the second value in lateral_oxide() complex attribute.

WHAT NEXT

Check your library and use correct permittivity value.

EXAMPLES

```
lateral_oxide ( 3.9, 0.99 );
```

EXAMPLE MESSAGE

```
Error: Line 46, The 'lateral_oxide' permittivity value is less than 1.00.  (LBDB-1048)
```

LBDB-1049 (error) The '%s' thickness value is less than zero.

DESCRIPTION

The thickness value must be positive. It also applies to the first value in lateral_oxide() complex attribute.

WHAT NEXT

Check your library and use correct thickness value.

EXAMPLES

```
lateral_oxide ( -3.9, 3.99 );
```

EXAMPLE MESSAGE

```
Error: Line 46, The 'lateral_oxide' thickness value is less than zero.  (LBDB-1049)
```

LBDB-1050 (error) There is no rectangle defined in the via_contact_layer group.

DESCRIPTION

There is no rectangle defined in the current via_contact_layer group. Library Compiler requires at least 1 rectangle being specified in each via_contact_layer group.

WHAT NEXT

Define the rectangle shape for the via_contact_layer group.

EXAMPLES

```
    default_via_generate(GEN1) {
      via_contact_layer(con1) { /* error */
resistance : 0.2;
      }
    }
```

EXAMPLE MESSAGE

Warning: Line 34, There is no rectangle defined in the via_contact_layer group. (LBDB-1050)

LBDB-1051 (error) The %s attribute is obsolete.

DESCRIPTION

This message indicates the named attribute is obsolete and need to be changed accordingly.

WHAT NEXT

Refer to the Library Compiler User Guide for the newest attribute names.

EXAMPLES

```
      lateral_oxide_thickness : 0.5 ;
```

EXAMPLE MESSAGE

Error: Line 34, The lateral_oxide_thickness attribute is obsolete. (LBDB-1051)

LBDB-1052 (error) The ’layer_antenna_factor’ function has inconsistent arguments.

DESCRIPTION

This message indicates the layer_antenna_factor function has wrong arguments. In Library Compiler, it requires one layer name followed by a floating number in the layer_antenna_factor function.

WHAT NEXT

Make sure the right argument is used for the function.

EXAMPLES

```
    phys_library(test) {
...
layer_antenna_factor (metal1, metal2, 0.1);
...
    }
```

EXAMPLE MESSAGE

Error: Line 25, The ’layer_antenna_factor’ function has inconsistent arguments. (LBDB-1052)

LBDB-1053 (error) The ’%s’ group cotains conflicting layer specification styles, ’%s’ and ’%s’.

DESCRIPTION

This message indicates the gds2 layer id definition styles are found. For example, you should either use obs_layer_map or obs_layer_id to specify geometry layer id and/or data type, but never use both functions in the same plib/pplib file.

WHAT NEXT

Make sure only one style is used in layer id definition.

EXAMPLES

```
    phys_library(test) {
...
```

```
gds2_extraction_rules() {
  obs_layer_map ( "14, 16, 18, 20", "07, 08, 09, 10");
  obs_layer_id (22, 0, 11, 0);
...
    }
```

EXAMPLE MESSAGE

```
Error: Line 25, The 'gds2_extraction_rules' group contains conflicting layer specif
ication styles,
'obs_layer_map' and 'obs_layer_id'. (LBDB-1053)
```

LBDB-1054 (warning) The port '%s' does not have the attribute '%s' specified. The value (%f, %f) will be assigned to the attribute.

DESCRIPTION

You receive this error message when the **rise_capacitance** and **fall_capacitance** attributes are specified for a port, but the **_rise_capacitance_range** and **fall_capacitance_range** attribute are not. (**rise_capacitance**, **rise_capacitance**) will be assigned to attribute **_rise_capacitance_range and (fall_capacitance**, **fall_capacitance**) will be assigned to attribute **fall_capacitance_range** respectively.

WHAT NEXT

If you accept the value assigned to the attribute referenced in the error message, no action is required on your part. If not, assign a value to the attribute.

LBDB-1055 (error) The '%s' function has inconsistent arguments.

DESCRIPTION

This message indicates the contact_min_spacing function, min_overhang function or diff_net_min_spacing function has wrong arguments. In Library Compiler, it requires 2 layer names followed by a floating numbers in the contact_min_spacing function, min_overhang function or diff_net_min_spacing function.

WHAT NEXT

Make sure the right argument is used for the function.

EXAMPLES

```
    phys_library(test) {
...
topological_design_rules() {
  contact_min_spacing (contact1, 0.5);
  min_overhang (metal1, contact1, 0.3);
  diff_net_min_spacing (metal1, contact1, 0.6);
  ...
      }
...
    }
```

EXAMPLE MESSAGE

```
Error: Line 245, The 'contact_min_spacing" function has inconsistent arguments. (LB
DB-1027)
```

LBDB-1056 (warning) The '%s' value '%d' is not allowed. Using default value '%d'.

DESCRIPTION

You receive this message because you specified a conversion factor value that either is not a multiple of 100 or may be a nonpositive number. A conversion factor can be - capacitance_conversion_factor, or - resistance_conversion_factor, or - current_conversion_factor, or - inductance_conversion_factor.

WHAT NEXT

Examine the library source file, and correct the conversion factor value.

EXAMPLES

```
  capacitance_conversion_factor : 123;
```

EXAMPLE MESSAGE

```
Warning: Line 85, The 'capacitance_conversion_factor' value '123' is not allowed.
Using default value '1000'. (LBDB-1056)
```

LBDB-1057 (error) Found milkyway_layer_map group defined

before ’%s’ group.

DESCRIPTION

This message indicates the named group in phys_library is not defined before milkyway_layer_map group.

WHAT NEXT

Move this group inside the physical library so that it is defined in front of milkyway_layer_map group.

EXAMPLES

```
    phy_library(test) {
...
milkyway_layer_group () {
 ...
}
resource ( std_cell ) {
        ...
}
    }
```

EXAMPLE MESSAGE

Error: Line 59, Found milkyway_layer_group defined before ’resource’ group. (LBDB-1001)

LBDB-1058 (error) The ’%s’ color name is invalid.

DESCRIPTION

This message indicates that you specified an invalid color name for the current attribute or function. The color name should match a color name previously defined in the color groups.

WHAT NEXT

Check your library to see if you have an error in either previous color definition or the current attribute / function.

EXAMPLES

```
   color : foo ;
```

EXAMPLE MESSAGE

```
Error: Line 104, The 'foo' color name is invalid.  (LBDB-1058)
```

LBDB-1059 (error) The '%s' '%s' name is invalid.

DESCRIPTION

This message indicates that you specified an invalid line_style/stipple name for the current attribute or function. The color name should match a line_style/stipple name previously defined in the line_style/stipple groups.

WHAT NEXT

Check your library to see if you have an error in either previous line_style/stipple definition or the current attribute / function.

EXAMPLES

```
   stipple : foo ;
```

EXAMPLE MESSAGE

```
Error: Line 104, The 'foo' 'stipple' name is invalid.  (LBDB-1059)
```

LBDB-1060 (error) The tile '%s' is not defined in the resource group.

DESCRIPTION

This message indicates name of the tile attribute is not a pre-defined tile.

WHAT NEXT

Make sure the tile attribute uses a pre-defined tile.

EXAMPLES

```
    phys_library(test) {
...
macro(and2) {
         ...
  in_tile : new_tile;/* error */
}
```

```
    }
```

EXAMPLE MESSAGE

```
Error: Line 34, The tile 'new_tile' is not defined in the resource group. (LBDB-
1060)
```

LBDB-1061 (error) The %s shape has zero area.

DESCRIPTION

This message indicates the path / polygon / rectangle function has zero size. That is not a real geometrical shape.

WHAT NEXT

Make sure it is a real geometry.

EXAMPLES

```
    phys_library(test) {
...
macro(and2) {
          ...
  pin(a) {
    ...
    obs(new_layer) {
      rectangle(0.1, 0.3, 0.1, 0.3);  /* error */
    }
  }
}
    }
```

EXAMPLE MESSAGE

```
Error: Line 34, The rectangle shape has zero area. (LBDB-1061)
```

LBDB-1062 (error) The '%s' via name is invalid.

DESCRIPTION

This message indicates that you specified an invalid name for the current attribute or function. The via name should match a name previously defined in the resource group.

WHAT NEXT

Check your library to see if you have an error in either previous layer definition or the current attribute / function.

EXAMPLES

```
   reference_cut_table( my_template ) {
values ( "via12, via12a, via12b");
   }
```

EXAMPLE MESSAGE

```
Error: Line 104, The 'via12a' via name is invalid.  (LBDB-1062)
```

LBDB-1063 (warning) The argument value %d of the '%s' function is out of range. It is expected to be 0 ot 1.

DESCRIPTION

This message indicates that the out-of-range value has been set to the specified function.

```
  pattern( 0, 1, 0, 1 ); /* correct */
```

WHAT NEXT

Change the physical library to correct the arguments.

EXAMPLES

```
  pattern( 0, 20, 0, 1 ); /* incorrect */
```

EXAMPLE MESSAGE

```
Warning: Line 17, The argument value 20 of the 'pattern' function
is out of range.  It is expected to be 0 or 1.  (LBDB-1063)
```

LBDB-1064 (error) Invalid attribute '%s' value '%d' is detected. The value must be

unique among all ’%s’ objects.

DESCRIPTION

This message indicates a non-unique id is found. - All via are required to have a unique via_id value. - All mask layers (device_layer, poly_layer, routing_layer, cont_layer) must have a unique mw_map id specified in its corresponding stream_layer group.

WHAT NEXT

Make sure the specified id value is unique among all named objects.

EXAMPLES

```
via (via12) {
  via_id : 12 ;
  ...
}
via (via23) {
  via_id : 12 ;
  ...
}
```

EXAMPLE MESSAGE

```
Error: Line 56, Invalid attriute ’via_id’ value ’12’ is detected.  The value must be
        unique among all ’via’ objects. (LBDB-1064)
```

LBDB-1065 (warning) No ’%s’ attribute has been specified for the
%s ’%s’. It is set to default value ’%d’.

DESCRIPTION

This message indicates that the library, perhaps an older PLIB file, does not contain the newly required object id’s and default values are assigned to it. - All via are required to have a unique via_id value, from 1 to 255. - All mask layers (device_layer, poly_layer, routing_layer, cont_layer) must have a unique mw_map id specified in its corresponding stream_layer group. Datatype in mw_map is always default to 0.

WHAT NEXT

Enhance PLIB file to - specify a unique via_id for each via specification; - specify a corresponding stream_layer (with mw_map attribute) for each mask layer. These stream_layer should have unique mw_map layer id among them.

EXAMPLES

```
via (via12) {
  ...
}
```

EXAMPLE MESSAGE

Warning: Line 56, No 'via_id' attribute has been specified for the via 'via12'. It is set to default value '12'. (LBDB-1065)

LBDB-1066 (warning) Cannot locate corresponding layer id and layer datatype for display_layer '%s'. It is set to layer id %d and layer datatype %d.

DESCRIPTION

This message indicates that the library, perhaps an older PLIB file, does not contain the newly required matching stream_layer object and mw_map(id, datatype) attribute values for all display_layer object. A unique mw_map(id, datatype) is automatically assigned to it.

WHAT NEXT

Enhance PLIB file to - specify a corresponding stream_layer (with mw_map attribute) for each display layer. These stream_layer should have unique mw_map(id, datatype) value pair.

EXAMPLES

```
display_layer (m1_pg) {
  ...
}
```

EXAMPLE MESSAGE

Warning: Line 56, Cannot locate corresponding layer id and layer datatype

for display_layer 'm1_pg'. It is set to layer id 23 and layer datatype '3'. (LBDB-1066)

LBDB-1067 (error) The '%s' attribute value(s) is out of range.

DESCRIPTION

This message indicates that the gds_map or mw_map attribute has out-of-range values.

The acceptable value ranges are:

id <= 255 datatype <= 255 where mw_map (id , datatype); gds_map (id, datatype);

WHAT NEXT

Change the attribute value to satisfy the value range.

EXAMPLES

```
mw_map ( 23, 256 );
```

In this case, the datatype value 256 is out of range.

EXAMPLE MESSAGE

Error: Line 912, The 'mw_map' attribute' attribute value is out of range. (LBDB-1067)

LBDB-1068 (warning) Floating-point value %s in '%s' attribute is too precise and will be truncated to %s.

DESCRIPTION

This warning message occurs when the specified floating-point number cannot be completely stored in the database and must be rounded off.

When storing floating-point numbers in the database, the number is scaled by multiplying the floating-point number by dist_conversion_factor. Digits to the right of the decimal point are dropped. When nonzero digits are dropped, this message appears.

WHAT NEXT

This is a warning message only. No action is required.

However, if the result is not what you intended, you can increase the dist_conversion_factor or reduce the number of digits in the floating-point number, and then run the command again.

EXAMPLES

```
     min_width : 0.1155 ;
```

EXAMPLE MESSAGE

```
Warning: Floating-point value 0.11550 in 'min_width' attribute is too precise and
 will be truncated to 0.115. (LBDB-1068)
```

LBDB-1069 (error) The %s object '%s' has a width %d and height %d that is inconsistent with the pattern size %d.

DESCRIPTION

This error message occurs when the pattern length of the specified section does not match the size specified by the pattern width and height. The number of elements in the pattern list must equal the product of the pattern width and height.

WHAT NEXT

Change the width and height attribute values or add or remove Boolean values to the pattern list. After making your changes, run the command again.

EXAMPLES

```
     stipple ( S1 ) {
width : 3 ;
height : 2 ;
pattern ( 1, 1, 0, 0 );
     }
```

EXAMPLE MESSAGE

```
Error: Line 67, Stipple object 'S1'  has a width 3 and height 2
that is inconsistent with the pattern size 4. (LBDB-1069)
```

LBDB-1070 (warning) Layer '%s' has a pitch %.4f that is less than the minimum spacing
and width sum %.4f.

DESCRIPTION

This warning message occurs when the specified Layer section contains an invalid pitch, minimum spacing or minimum width. The pitch must be greater than or equal to the sum of the layer's minimum spacing and minimum width.

WHAT NEXT

This is a warning message only. No action is required.

However, if the result is not what you intended, change the pitch, minimum spacing, or minimum width to meet the requirement that the pitch be greater than or equal to the sum of the layer's minimum spacing and minimum width.

EXAMPLES

```
     layer ( M1 ) {
min_width : 0.10 ;
spacing : 0.12 ;
pitch : 0.15 ;
     }
```

EXAMPLE MESSAGE

```
Warning: Line 24, Layer 'M1' has a pitch 0.1500 that is less than the minimum spaci
ng

      and width sum 0.2200.  (LBDB-1069)
```

LBDB-1071 (warning) Routing_layer '%s' has invalid spacing_table value %.4f.

DESCRIPTION

This warning message occurs when the specified routing_layer contains an invalid spacing_table value. The spacing_table values must be equal to or greater than the routing_layer spacing value.

WHAT NEXT

This is only a warning message. No action is required.

However, it is best practice to change the spacing_table value of the specified routing_layer so the values are equal to or greater than the layer spacing value. After making your changes, run the command again.

EXAMPLES

```
     layer ( M1 ) {
spacing : 0.12 ;
spacing_table (1d_table) {
  values (" 0.1 , 0.15, 0.24" );
}
     }
```

EXAMPLE MESSAGE

Warning: Line 235, Routing_layer ’M1’ has invalid spacing_table value 0.100. (LBDB-1071)

LBDB-1072 (error) Routing_layer ’%s’ has invalid spacing_table value %.4f.

DESCRIPTION

This warning message occurs when the specified routing_layer contains an invalid spacing_table value. The spacing_table values must be equal to or greater than the routing_layer spacing value. And values[0] = spacing.

WHAT NEXT

Change the spacing_table value so the value in the list are equal to or greater than the layer spacing value. After making your changes, run the command again.

EXAMPLES

```
     layer ( M1 ) {
spacing : 0.12 ;
spacing_table (1d_table) {
  values (" 0.1 , 0.15, 0.24" );
}
     }
```

EXAMPLE MESSAGE

Error: Line 235, Routing_layer ’M1’ has invalid spacing_table value 0.100. (LBDB-1072)

LBDB-1073 (warning) Layer '%s' has a pitch %.4f that does not match the recommended
wire-to-via pitch %.4f.

DESCRIPTION

This warning message occurs when the pitch of the specified layer does not match the recommended pitch. The wire-to-via pitch is the recommended pitch and provides the best wire track resources for routing.

The wire-to-wire pitch is more aggressive, the via-to-via is more conservative and neither are recommended. The metal layer pitch must match the wire-to-via pitch in the routing direction.

The horizontal wire-to-via pitch is calculated as follows:

```
    (min spacing) + (min width)/2 + (via metal width)/2
```

The vertical wire-to-via pitch is calculated as follows:

```
    (min spacing) + (min width)/2 + (via metal height)/2
```

The via metal width and height are based on the larger of the lower and upper default contact codes.

WHAT NEXT

This is only a warning message. No action is required.

You can leave the pitch of the specified layer at the current setting, or you can change the pitch of the layer to the recommended pitch.

EXAMPLES

```
     layer ( metal3 ) {
spacing : 1.9;
min_width : 1.8;
pitch : 4.5;
...
     }

     via (via23) {
...
via_layer(metal3) {
  rectangle ( -1.1, -1.1, 1.1, 1.1 );
}
     }
     via (via34) {
```

```
...
via_layer(metal3) {
  rectangle  ( -1.1, -1.1, 1.1, 1.1 );
}
     }
```

EXAMPLE MESSAGE

```
Warning : Line 36, Layer 'metal3' has a pitch 4.500 that does not match the recomme
nded
wire-to-via pitch 3.900. (LBDB-1073)
```

LBDB-1074 (warning) Layer '%s' has a pitch %.4f that is not aligned with bottom layer pitch %.4f.

DESCRIPTION

This warning message occurs when the pitch of the specified layer is not double or triple the pitch of the lower metal layer with the same routing direction. Doubling or tripling the pitch value, maximizes routing resources and minimizes overlap with other metal layers.

WHAT NEXT

This is only a warning message. No action is required.

You can either leave the pitch of the specified layer unchanged, or change the pitch to the doubled or tripled pitch and run the command again.

EXAMPLES

```
     layer ( metal1 ) {
pitch : 1.9;
...
     }
...
     layer ( metal3 ) {
pitch : 3.9;
...
     }
```

EXAMPLE MESSAGE

```
Warning : Line 36, Layer 'metal3' has a pitch 3.900 that is not aligned with
bottom layer pitch 1.900. (LBDB-1074)
```

LBDB-1075 (error) The attribute '%s' has %d entries, which exceeds the maximal allowed 8 entries.

DESCRIPTION

This error message occurs when the specified index array in routing_layer/cont_layer group that is too large. The index array size must be beween 1 and 8 inclusive.

WHAT NEXT

Change the index array so that it does not exceed 8 entries. Then run the command again.

EXAMPLES

```
     layer ( metal1 ) {
spacing_table ( 1d_stable ) {
  index_1 (0.0, 1.3, 2.4, 4.5, 6.6, 7.1, 9.3, 12.2, 25.0, 33.9);
}
...
     }
```

EXAMPLE MESSAGE

```
Warning : Line 36, The attribute 'index_1' has 10 entries, which exceeds the maximal
      allowed 8 entries. (LBDB-1075)
```

LBDB-1076 (warning) The attribute '%s' has invalid threshold values %.4f.

DESCRIPTION

This warning message occurs when the specified table index contains an invalid threshold values. The threshold list must meet the following requirements:

- The first value must be between 0 and the default_routing_width inclusively.
- The second value must be greater than the layer min_width.

WHAT NEXT

This is only a warning message. No action is required.

However, it is best practice to change the index values to meet the above

requirements. After making your changes, run the command again.

EXAMPLES

```
     layer ( metal1 ) {
min_width : 1.5 ;
spacing_table ( 1d_stable ) {
  index_1 (0.0, 1.3, 2.4, 4.5, 6.6, 7.1, 9.3, 12.2, 25.0, 33.9);
  ...
}
...
     }
```

EXAMPLE MESSAGE

```
Warning : Line 36, The attribute 'index_1' has invalid index value 1.3. (LBDB-1076)
```

LBDB-1077 (error) The attribute '%s' has invalid threshold values %.4f.

DESCRIPTION

This warning message occurs when the specified table index contains an invalid threshold values. The threshold list must meet the following requirements:

- The first value must be between 0 and the min_width inclusively.
- The second value must be greater than the layer min_width.

WHAT NEXT

Change the index values to meet the above requirements. After making your changes, run the command again.

EXAMPLES

```
     layer ( metal1 ) {
min_width : 1.5 ;
spacing_table ( 1d_stable ) {
  index_1 (0.0, 1.3, 2.4, 4.5, 6.6, 7.1, 9.3, 12.2, 25.0, 33.9);
  ...
}
...
     }
```

EXAMPLE MESSAGE

```
Error : Line 36, The attribute 'index_1' has invalid index value 1.3. (LBDB-1077)
```

LBDB-1078 (error) Layer '%s' has a default_routing_width value %.4f that is less than its min_width value %.4f.

DESCRIPTION

This error message occurs when the default width or minimum width of the specified Layer section is invalid. The default width (default_routing_width) of each layer must be greater than or equal to its minimum width (min_width).

WHAT NEXT

Change the default_routing_width or min_width of the specified Layer section so that the default_routing_width is greater than or equal to the min_width. After making your changes, run the command again.

EXAMPLES

```
     layer ( metal1 ) {
min_width : 1.5 ;
default_routing_width : 1.3;
  ...
}
...
     }
```

EXAMPLE MESSAGE

```
Error : Line 36, Layer 'metal1' has a default_routing_width value 1.3000 that is le
ss than its
min_width value 1.5000. (LBDB-1078)
```

LBDB-1079 (warning) The attribute '%s' has rounded threshold value %.4f.

DESCRIPTION

This warning message occurs when the threshold value from the index array contains rounded values. It is best practice to avoid ending threshold values with a 0 digit in the most precise position. This practice minimizes the confusion between tools that interpret the thresholds as exclusive, rather than inclusive, lower bounds.

WHAT NEXT

This is only a warning message. No action is required.

However, you can either increase the rounded threshold value by one grid resolution value and run the command again, or you can leave the threshold value at the current setting.

EXAMPLES

```
     layer ( metal1 ) {
spacing_table ( 1d_spacing ) {
  index_1 ( "0.0, 1.500, 3.015" );
  ...
}
...
     }
```

EXAMPLE MESSAGE

```
Warning : Line 36, The attribute 'index_1' has rounded threshold value 1.5000. (LBD
B-1079)
```

LBDB-1080 (warning) Attribute '%s' has insignificant differences between threshold values %.4f and %.4f.

DESCRIPTION

This warning message occurs when the index threshold contains insignificant differences between the threshold values. It is best practice to have thresholds differ by more than half of the min_width and more than ten percent of the greater threshold. If they do not differ by these amounts, then the table values can contain redundant data, be unnecessarily large, and increase router run-time dramatically.

WHAT NEXT

This is only a warning message. No action is required.

However, you can check the table values for redundant data. If you find redundant data, then reduce the index dimension and the number of threshold values. After making your changes, rerun the command.

EXAMPLES

```
     layer ( metal1 ) {
min_width : 1.5;
spacing_table ( 1d_spacing ) {
  index_1 ( "0.0, 1.905, 1.915" );
  ...
}
...
```

```
    }
```

EXAMPLE MESSAGE

```
Warning : Line 36, The attribute 'index_1' has insignificant differences between
threshold values 1.9050 and 1.9150. (LBDB-1080)
```

LBDB-1081 (warning) Routing layer '%s' does not contain positive min_enclosed_area value.

DESCRIPTION

The value of the **minEnclosedArea** attribute for default metal layers should be greater than 0. Other values can affect the quality of the application results and can cause excessive design rule constraint violations during physical verification.

WHAT NEXT

This is only a warning message. No action is required.

However, it is best practice to check the min_enclosed_area or min_enclosed_area_table attribute value of the specified layer, and then change the value to a value greater than 0, if necessary. After making your changes, run the command again.

EXAMPLES

```
    layer ( metal1 ) {
...
    }
```

EXAMPLE MESSAGE

```
Warning : Line 36, Routing layer 'metal1' does not contain positive min_enclosed_ar
ea value. (LBDB-1081)
```

LBDB-1082 (error) The u_shaped_wire_spacing attribute value %.4f in routing layer '%s' is less than spacing value %.4f.

DESCRIPTION

This message indicates that the u_shaped_wire_spacing value is less than the spacing

value, which is not allowed. It is required that u_shaped_wire_spacing attribute value be no less than the spacing attribute value of the same routing layer.

WHAT NEXT

Change u_shaped_wire_spacing value so that it is equal or more than the spacing value. Then run the command again.

EXAMPLES

```
    layer ( metal1 ) {
  spacing : 1.4;
  u_shaped_wire_spacing : 1.0;
  ...
    }
```

EXAMPLE MESSAGE

```
Error : Line 45, The u_shaped_wire_spacing attribute value 1.0000 in routing layer
'metal1'
is less than the spacing attribute value 1.400. (LBDB-1082)
```

LBDB-1083 (error) The same_net_min_spacing attribute value %.4f in routing layer '%s' is more than spacing value %.4f.

DESCRIPTION

This message indicates that the same_net_min_spacing value is more than the spacing value, which is not allowed. It is required that same_net_min_spacing be no more than the spacing attribute value of the same routing layer.

WHAT NEXT

Change same_net_min_spacing value so that it is equal or less than the spacing value. Then run the command again.

EXAMPLES

```
    layer ( metal1 ) {
  spacing : 1.4;
  same_net_min_spacing : 1.7;
  ...
    }
```

EXAMPLE MESSAGE

```
Error : Line 45, The same_net_min_spacing attribute value 1.7000 in routing layer ’
metal1’
is more than the spacing attribute value 1.400. (LBDB-1083)
```

LBDB-1084 (warning) Tile ’%s’ has size %.4f that is not a multiple of %s routing layer pitch %.4f.

DESCRIPTION

This warning message occurs when: - in horizontal floorplan, tile width is not consistent with first vertical routing layer pitch; or - in vertical floorplan, tile height is not consistent with first horizontal routing layer pitch.

It is recommended that the tile dimension lines up with pitch to maximize utilization.

WHAT NEXT

This is a warning message only. No action is required.

However, it is best practice to either change the size value in question to the suggested pitch, or change the specified routing layer pitch to match tile dimension. After making your changes, run the command again.

EXAMPLES

```
     layer ( metal2 ) {
  routing_direction : vertical ;
  pitch : 1.4;
  ...
     }
...
     tile (unit) {
  size ( 1.6, 5.5 );
  ..
     }
```

EXAMPLE MESSAGE

```
Warning : Line 45, Tile ’unit’ has size 1.6000 that is not a multiple of
metal2 routing layer pitch 1.4000. (LBDB-1084)
```

LBDB-1085 (error) Cannot find via defined for contact layer

’%s’.

DESCRIPTION

This error message occurs when there is no via defined with a specific contact layer between 2 metal layers.

At least one via must be defined between 2 metal layers in a library.

WHAT NEXT

Define at least one via for the contact layer. Run the command again.

EXAMPLE MESSAGE

Error : Cannot find via defined for contact layer ’via12’. (LBDB-1085)

LBDB-1086 (warning) The %s attribute value in via ’%s’ specifies non-positive metal enclosure.

DESCRIPTION

This warning message occurs when the specified via section contains non-positive metal enclosure dimensions or non-positive enclosure metal rectangle. If the non-positive metal enclosure values are set intentionally, this warning can be ignored. Otherwise, the values may cause the router to create enclosures that violate design rule constraints, such as completely enclosed spaces or donuts.

WHAT NEXT

This is a warning message only. No action is required.

However, if the zero metal enclosure values are not intentional, you can change either the rectangle coordinates or change enclosure value in via group to avoid potential design rule violations.

EXAMPLES

```
     via ( via12 ) {
via_layer( metal1 ) {
  enclosure ( 0, 0 );
}
     }
```

EXAMPLE MESSAGE

```
Warning : Line 45, The enclosure attribute value in via 'via12' specifies
non-positive metal enclosure. (LBDB-1086)
```

LBDB-1088 (warning) There are more than 255 layers in this library.

DESCRIPTION

This warning message occurs when more than 255 layers are found in the current library. It does not include display layers. Currently Milkyway database can accomodate up to 255 layers. Upper layers exceeding the limit will be ignore in the database.

WHAT NEXT

This is a warning message only. No action is required.

However, it is best practice to make sure that the total number of layers do not exceed the limit. After making your changes, run the command again.

EXAMPLE MESSAGE

```
Warning : There are more than 255 layers in this library. (LBDB-1088)
```

LBDB-1089 (warning) '%s' and '%s' layers in %s attribute are not
adjacent layers.

DESCRIPTION

This warning message occurs when the 2 layers specified in: - same_net_min_spacing - diff_net_min_spacing - contact_min_spacing - corner_min_spacing - min_overhang - min_enclosure - end_of_line_enclosure complex attributes are not adjacent layers.

It is recommended that the 2 layers must be adjacent routing or contact layers.

WHAT NEXT

This is a warning message only. No action is required.

However, it is best practice to follow the above guideline. After making your changes, run the command again.

EXAMPLES

```
diff_net_min_spacing ( met1, met4, 1.4 );
```

EXAMPLE MESSAGE

```
Warning : Line 45, 'met1' and 'met3' layers in diff_net_min_spacing attribute are n
ot
adjacent layers. (LBDB-1089)
```

LBDB-1090 (warning) Cannot find matching stream_layer for layer '%s'.

DESCRIPTION

This warning message occurs when the layer is specified in resource layer section, but no stream_layer with identical name can be found in milkyway_layer_map group.

It is recommended that a stream_layer is defined for each layer found in resource group.

WHAT NEXT

This is a warning message only. No action is required.

However, it is best practice to add stream_layer definition for the specified layer. After making your changes, run the command again.

EXAMPLE MESSAGE

```
Warning : Cannot find matching stream_layer for layer 'metal1'. (LBDB-1090)
```

LBDB-1091 (warning) Reset density value from %4.1f to %4.1f.

DESCRIPTION

Density value defined in density_property in PLIB file should be between 0.0 and 100.0. Else, it will be reset to 0.0 or 100.0.

WHAT NEXT

Revise density value if the reset value is not expected.

EXAMPLE MESSAGE

```
Warning: Line 12, Reset density value from 101.6 to 100.0. (LBDB-1091)
```

LBDB-1092 (warning) Layer '%s' attribute '%s' has a value of %g.

DESCRIPTION

This warning message occurs when the value of the specified layer attribute may not be optimal.

The values can affect the quality of the application results and can cause excessive design rule constraint violations during physical verification.

For a set of rule, completeness of rule parameters should be maintained:

For enclosed via min edge length rule, if enclosed_via_min_edge_length is specified, min_edge_length should be specified, and enclosed_via_min_edge_length > min_edge_length > 0

For U-shape rule, if you specify u_shaped_min_length or u_shaped_wire_spacing, you should also specify u_shaped_min_depth and min_spacing. And u_shaped_wire_spacing > min_spacing.

For multiple min area rule, "min_area" attribute is needed if "min_polygon_area_rule() -> polygon_min_area" is specified and min_polygon_area_rule()->polygon_min_area > min_area. If both "min_polygon_area_rule() -> polygon_min_area" and "min_polygon_area_rule() -> max_edge_length" are specified, "min_length" should be specified. And min_polygon_area_rule() -> max_edge_length >= min_length

For non-preferred direction routing rule, if you specify non_preferred_dir_width, it will satisfy non_preferred_dir_width > default_routing_width. If you specify both non_preferred_dir_width and non_preferred_dir_max_length, it will satisfy non_preferred_dir_max_length > non_preferred_dir_width-default_routing_width.

For min_spacing rule in routing_layer, if you specify min_spacing(x_min_spacing, y_min_spacing), it will satisfy x_min_spacing >= spacing and y_min_spacing >= spacing.

For jog wire corner to corner spacing rule, if you specify aligned_jog_width and unaligned_jog_diag_width, it will satisfy aligned_jog_width >= min_width and unaligned_jog_diag_width >= min_width.

For [x|y]_min_spacing_table, [x|y]_max_spacing_table, the first value, i.e., value[0], will satisfy value[0] >= spacing.

For [x|y]_max_spacing_check_range_table, the first value, i.e., value[0], will satisfy value[0] >= spacing*2 + min_width.

WHAT NEXT

This is only a warning message. No action is required.

However, it is best practice to check the attribute value of the specified layer, and then change the value to a value greater than 0, if necessary. After making your changes, run the command again.

EXAMPLE MESSAGE

WARNING : Layer 'M1' attribute 'polygon_min_area' has a value of 0.03. (LBDB-1092)

LBDB-1093 (warning) Layer '%s' attribute '%s' is missing.

DESCRIPTION

This warning message occurs when the specified section is missing an important attribute. If the attribute is not specified in PLIB file, the default value is 0 for number attributes, or an empty string for string attributes.

For multiple min area rule, "min_area" attribute is needed if "min_polygon_area_rule() -> polygon_min_area" is specified and min_polygon_area_rule()->polygon_min_area > min_area. If both "min_polygon_area_rule() -> polygon_min_area" and "min_polygon_area_rule() -> max_edge_length" are specified, "min_length" should be specified.

For U-shape rule, if you specify u_shaped_min_length or u_shaped_wire_spacing, you should also specify u_shaped_min_depth and min_spacing.

For enclosed via min edge length rule, if enclosed_via_min_edge_length is specified, min_edge_length should be specified, and enclosed_via_min_edge_length > min_edge_length > 0 If both enclosed_via_min_edge_length and min_edge_length are specified, enclosed_via_adjacent_edge_length should be specified.

For 2-line end rule, if end_to_end_min_spacing is specified, end_of_line_metal_max_width should be specified.

For end of line rule, if end_of_line_side_keepout_length is specified, end_of_line_metal_max_width should be specified.

For line end depth rule, if end_of_line_min_length is specified, end_of_line_metal_max_width should be specified.

WHAT NEXT

This is only a warning message. No action is required.

However, if you do not want to use the default value for the attribute, add the attribute with the desired value to the specified section in PLIB file and rerun the command.

EXAMPLE MESSAGE

```
WARNING : Layer 'M1' attribute 'min_area' is missing. (LBDB-1093)
```

LBDB-1094 (error) The table '%s' can supports 'scalar' template only.

DESCRIPTION

This error message is reported for some table groups, that currently only a scalar value is supported for them by our tool. But found they are using a non-scalar template name.

Following two groups are under the restriction for now:
pgate_antenna_ratio(template_name) { } ngate_antenna_ratio(template_name) { }

WHAT NEXT

Modify the plib file accordingly, change the template name to 'scalar' and specify only one value for the table.

Example: antenna_rule("M1_ANTENNA_RULE") ...
pgate_antenna_ratio("antenna_tempalte1") { index_1 ("0.0 1.0 2.0 3.0") values ("200 200 400 600"); } }

Modify the group to: antenna_rule("M1_ANTENNA_RULE") ...
pgate_antenna_ratio("scalar") { values ("200"); } }

EXAMPLE MESSAGE

```
Error: Line 531, The table 'pgate_antenna_ratio' can supports 'scalar' template onl
y. (LBDB-1094)
```

LBDB-1095 (error) The '%s' should coexist with '%s' in '%s' group.

DESCRIPTION

This error message is reported when there is restriction that two tables/functions/ attributes should coexist the group, but only one found.

Example:

In antenna_rule group, the pgate_antenna_ratio table should coexist with ngate_antenna_ratio. If any of the other is not specified when one is present, the

error is reported.

antenna_rule (M1_mode1_d4) { antenna_ratio ("antenna_tempalte") { index_1("0, 0.05 0.06 0.6"); values("100 100 300 500"); } pgate_antenna_ratio("scalar") { values("100"); } layer_antenna_factor("M1", 1.0); }

WHAT NEXT

Modify the plib file accordingly, specify both tables/attributes/functions in the group. or remove the existing one.

EXAMPLE MESSAGE

Error: Line 546, The 'pgate_antenna_ratio' should coexist with 'ngate_antenna_ratio ' in 'antenna_rule' group. (LBDB-1095)

LBDB-1096 (error) There is unsupported antenna data in the group.

DESCRIPTION

This error message is reported when there is unsupported antenna data found in the antenna_rule group. Mainly, the error is issued for following situations:

1. usage of pgate_antenna_ratio and ngate_antenna_ratio pgate_antenna_ratio and ngate_antenna_ratio can't be supported when: antenna_accumulation_calculation_method : accumulative_ratio; with routing_layer_calculation_method : top_area|side_wall_area;

Note that when reading a plib file to Milkyway library, antenna_accumulation_calculation_method is default to accumulative_ratio and routing_layer_calculation_method is default to top_area;

So, if you want to define pgate_antenna_ratio and ngate_antenna_ratio in the antenna_rule group, you can't leave these two attributes undefined, otherwise, this error will be issued too.

2. usage of antenna area rule The antenna_rule group is defined as antenna area rule, when antenna_ratio_calculation_method == total_routing_area. And there is restrcitions to antenna_accumulation_calculation_method and geometry_calculation_method, according to current tool support. Following combinations are supported now, this error will be issued for other combinations. mode 1: calculate metal area ignore all lower layer segments. antenna_accumulation_cm = single_layer, geometry_cm = connected_only; mode 2: calculate metal area includes lower layer segments to input pins. antenna_accumulation_cm = accumulative_area, geometry_cm = connected_only; mode 3: calculate metal area includes all lower layer segments. antenna_accumulation_cm = accumulative_area, geometry_cm = all_geometries;

Besides above three calculation methods, the antenna_ratio should using scalar template and have only one value defined as max allowable antenna area, attribute max_diode_insertion_distance is used to define max allowable distance from inserted diode to gate.

other attributes and groups defined in antenna area rule are totally ignored during read_plib and not stored into database.

WHAT NEXT

Modify the plib file accordingly to rule above.

EXAMPLE MESSAGE

Error: Line 546, There is unsupported antenna data in the group.(LBDB-1096)

LBDB-1097 (error) Layer '%s' attribute '%s' and '%s' are different.

DESCRIPTION

x_min_spacing_table, y_min_spacing_table, x_max_spacing_table, y_max_spacing_table, x_max_spacing_check_range_table, y_max_spacing_check_range_table currently require the content in index_1 and index_2 are the same.

If both exist, the dimension and content in index_1[] in fat_wire_via_keepout_enclosure_table and in fat_wire_via_keepout_edge_table should be the same.

If both exist, the dimension and content in index_1[] in fat_wire_via_keepout_enclosure_table and in fat_wire_via_spacing_threshold_table should be the same.

WHAT NEXT

Unify the different elements.

EXAMPLE MESSAGE

Error : Layer 'M1' attribute 'x_min_spacing/index_1' and 'x_min_spacing/ index_2' are different. (LBDB-1097)

LBDB-1098 (error) Layer '%s' has wrong '%s'.

DESCRIPTION

Values in x_legal_width and y_legal_width should satisfy, (1) the width values are in ascending order; (2) the first value >= min_width; (3) the last value <= max_width if max_width is specified; (4) default_routing_width is among the values.

WHAT NEXT

Re-specify x_legal_width or y_legal_width.

EXAMPLE MESSAGE

Error : Layer 'M1' has wrong 'x_legal_width'. (LBDB-1098)

LBDB-1099 (error) Layer '%s' '%s' and '%s' can't co-exist.

DESCRIPTION

fat_wire_via_keepout_edge_table and fat_wire_via_spacing_threshold_table can't co-exist in a cont_layer.

WHAT NEXT

Remove at least one of the two given attributes/functions/groups.

EXAMPLE MESSAGE

Error : Layer 'M1' 'fat_wire_via_keepout_edge_table' and 'fat_wire_via_spacing_threshold_table' can't co-exist. (LBDB-1099)

LBDB-1100 (information) Dummy cell '%s' defined in the library.

DESCRIPTION

This info message is reported when there is dummy cell defined in an incremental plib file (that is, the library attribute is_incremental_library : true;)

A dummy cell is identified by following features: 1. The cell name has wildcard '*' used, and the '*' is the last character in the cell name, for example, cell name is "*", or "AND*". 2. There is no cell geometries (macro obs, pin port) defined in the cell.

A dummy cell is expected only in an incremental plib file, and it’s used to update cell/pin attributes for FRAM view cells when read plib data to Milkyway database.

WHAT NEXT

Users do not need to do anything.

LBDB-1101 (error) There is geometry data defined in dummy cell ’%s’.

DESCRIPTION

This warning message is reported when there is geometry data defined in the dummy cell.

A dummy cell is identified by following features: 1. The cell name has wildcard ’*’ used, and the ’*’ is the last character in the cell name, for example, "*" or "AND*". 2. There is no cell geometries (macro obs, pin port) defined in the cell.

A dummy cell is expected only in an incremental plib file, and it’s used to update cell/pin attributes for a set of FRAM view cells (pattern matched cells) when read plib data to Milkyway database.

WHAT NEXT

Remove all geometry data from the cell (macro obs, pin port) if users want to use dummy cell to update cell/pin attributes for a set of cells. Otherwise, rename the cell name to avoid it match with dummy cell naming rule.

EXAMPLE MESSAGE

Error: Line 546, There is geometry data defined in dummy cell ’*’.(LBDB-1101)

LBDB-1150 (error) Invalid value in end_of_line_via_wire_rule.

DESCRIPTION

Name the five values in end_of_line_via_wire_rule as layer1, layer2, end_of_line_via_wire_min_width, end_of_line_via_wire_min_spacing, end_of_line_via_ortho_wire_max_threshold, respectively.

Suppose layer1 is routing_layer, and layer2 is cont_layer. default_via is the default via on layer2. Taking min_width and min_spacing specification from layer1, and compute cut_width by the geometry of default_via.

If there is another design rule for this layer pair

min_enclosure (string, string, float); /* layer1, layer2, min_enclosure */

Take min_enclosure from this specification. Otherwise let min_enclosure=0.

Values should satisfy, (1) end_of_line_via_wire_min_width > min_width (2)
end_of_line_via_wire_min_width >= cut_width + 2* min_enclosure (3)
end_of_line_via_wire_min_spacing >= min_spacing + min_enclosure (4)
end_of_line_via_ortho_wire_max_threshold >= minWidth

WHAT NEXT

Change the value to satisfy all the 4 restrictions.

EXAMPLE MESSAGE

Error : Invalid value in end_of_line_via_wire_rule. (LBDB-1150)

LBDB-1151 (error) "%s" has invalid value %f.

DESCRIPTION

same_segment_center_min_spacing, same_net_center_min_spacing,
diff_segment_center_min_spacing, diff_net_center_min_spacing in cont_layer() group
or in topological_design_rules() group should satifsy,
[same|diff]_[segment|net]_center_min_spacing >= min_cut_spacing + cut_width

The value of min_cut_spacing and cut_width is explained as follows.

As for [same|diff]_[segment|net]_center_min_spacing in cont_layer() group, let
"default_via" to be the default via of this cont_layer. Then min_cut_spacing is
taken from contact_spacing specification. Cut_width is taken from the geometry of
default_via.

As for [same|diff]_[segment|net]_center_min_spacing in topological_design_rules()
group, we only check if both layer1 and layer2 are cont_layers. Let "default_via_1"
to be the default via on layer1, "default_via_2" to be the default via on layer2.
min_cut_spacing is taken from the function in topological_design_rule():

contact_min_spacing (layer1, layer2, min_cut_spacing)

Cut_width_1 and cut_width_2 are taken from the geometry of default_via_1 and
default_via_2, respectively. Let cut_width = (cut_width_1+cut_width_2)/2.

WHAT NEXT

Change the value to satisfy the restriction.

EXAMPLE MESSAGE

```
Error : "diff_segment_center_min_spacing" has invalid value 0.12. (LBDB-1151)
```

LBDB-1152 (error) The '%s' attribute has an invalid sequence of data '%g , %g'. The values must be in decreasing order.

DESCRIPTION

This message indicates that the set of data is not specified in decreasing order. Content in "values" in min_metal_spacing_table must be in descending order.

WHAT NEXT

Check your library and correct the order of the values.

EXAMPLE MESSAGE

```
Error: Line 22, The 'values' attribute has an invalid sequence of
data '1.200000 , 2.300000'. The values must be in decreasing order. (LBDB-1152)
```

LBDB-1153 (error) '%s' has 0 or more than %d arguments.

DESCRIPTION

[x|y]_legal_width requires that the argument number is greater than 0 and less than or equal to 16.

WHAT NEXT

Add or reduce arguments into the specified function.

EXAMPLE MESSAGE

```
Error: Line 22, 'x_legal_width' has 0 or more than 16 arguments. (LBDB-1153)
```

LBDB-1154 (error) There is no noise information in the library.

DESCRIPTION

This information occurs when checking library for noise information, but there is no

noise information in the library at all.

WHAT NEXT

If noise information is not needed, cancel the noise checking; If noise information is needed, add I-V characteristics, noise immunity data and noise propagation data.

LBDB-1155 (error) Invalid %s found under section %s in map file.

DESCRIPTION

In the map file, if any of the following is incorrect, (1) voltage_name (2) voltage value (3) power management attributes this message will occur.

Valid voltage_name should be a valid string that starts with a character a-z or A-Z. The voltage_name in PG_TO_VOLTAGE_MAP section should be one in VOLTAGE_MAP. It could be a rail name, and could be the same as pg_pin name. But never input an invalid value such as "-" or "*" in voltage_name field in PG_TO_VOLTAGE_MAP or VOLTAGE_MAP section. Valid voltage values are non-negative floating point numbers, for example, 0.9, that are valid voltage values in the input library. For valid power management attributes, please refer to related documents or user guide. The following are only a few examples: valid switch_cell_type is coarse_grain and fine_grain; valid level_shifter_type is HL, LH and HL_LH; always_on pins are related to backup power; a switch cell has VVDD+VDD or VVSS+VSS, and. VVDD has pg_function where VVDD is virtual VDD.

WHAT NEXT

You should correct the invalid values and/or voltage_name in the map file. For example, in voltage_name field, if you enter "-", you will receive this message. You must input a valid voltage_name, e.g. VDD.

EXAMPLES

```
BEGIN PG_TO_VOLTAGE_MAP
cell        pg_pin      voltage_name pg_type
ADDFHX1     VDD         -     power
ADDFHX1     VSS         VSS     primary_ground
GEND PG_TO_VOLTAGE_MAP
```

EXAMPLE MESSAGE

Error: Line 14, Invalid voltage_name found under section PG_TO_VOLTAGE_MAP in map f ile. (LBDB-1155)

LBO-1 (info) Location based optimization enabled.

DESCRIPTION

Location based optimization feature of IPO is enabled. This feature is enabled whenever location information is back-annotated using a PDEF file (revision 2.0 or later) and sufficient delay and load back-annotations are provided. Enabling of LBO does not imply automatic enabling of LBO tricks. Individual LBO tricks are enabled or disabled by setting independent variables for each LBO trick.

WHAT NEXT

For more information please see LTL users guide.

LBO-2 (info) Location based optimization enabled with obstruction capability.

DESCRIPTION

Location based optimization feature of IPO is enabled with obstruction handling. This feature will not insert cells in areas marked as obstructions in the PDEF file.

WHAT NEXT

For more information please see LTL users guide.

LBO-3 (warning) The pin '%s' has a location '%d %d' which is on an obstruction; fanout optimization will not be performed on the net.

DESCRIPTION

This net's fanout will not be optimized as its pin locations are within areas marked as obstructions.

WHAT NEXT

Please check the PDEF file to see if the locations are correct and reissue the command. Also check the bounding box of a cell marked as an obstruction via the set_obstruction command.

LBO-4 (warning) Cannot estimate load/delay

DESCRIPTION

Cell location is needed to estimate load/delay.

WHAT NEXT

Please obtain the PDEF file with cell location.

LBO-5 (information) reoptimize_design command is recommended for layout sensitive optimization

DESCRIPTION

reoptimize_design command is the new command for layout sensitive optimization. It has better performance and optimization capabilities, such as Location-Based Optimization (LBO), and shares the new flow and techniques introduced in Design Compiler 98.

WHAT NEXT

Please refer to Floorplan Manager manual

LBO-11 (Warning) Cannot mark %s as an obstruction since bounding rectangle is not defined.

DESCRIPTION

The **set_obstruction** command cannot mark cells as placement obstructions if the bounding rectangle for the cell is not defined.

WHAT NEXT

Use the **read_pdef** command to load the bounding box for the cell. For more information, see the *FloorPlan Manager User Guide* and *Synthesis Release Note Version 1999.05*.

LBO-12 (Warning) %s is already marked as an obstruction.

DESCRIPTION

You receive this warning message if the **set_obstruction** command skipped the specified cell because the cell was already marked as an obstruction.

WHAT NEXT

Varify that you are selecting the correct cell to be marked as an obstruction.

LBO-13 (Warning) Cannot mark hierarchical cell %s as an obstruction.

DESCRIPTION

You receive this warning message when the **set_obstruction** command skipped the cell because it is a hierarchical cell. Hierarchical cells cannot be marked as obstructions using the **set_obstruction** command.

WHAT NEXT

Varify that you are selecting the correct cell to be marked as an obstruction.

LBO-15 (error) No physical design information read before set_port_location; unable to set the port location.

DESCRIPTION

You receive this error message if no physical design information is available when you execute the **set_port_location** command.

WHAT NEXT

Use the **read_pdef** command to load the physical design information before using the **set_port_location** command.

SEE ALSO

For more information, see the *FloorPlan Manager User Guide* and the *Synthesis Release Note Version 1999.05*.

LBO-16 (info) Resetting location for the port %s.

DESCRIPTION

The location specified for the port by any previous **set_port_location** command will be deleted from the database. The tool will use the port location specified by the DEF file for any previous **read_def** command (in the incremental mode), if it is available.

WHAT NEXT

If you want to re-annotate the location of the port, use the **set_port_location** command with the **-coordinate** option.

LBO-17 (info) Setting location for port %s: X = %s %s Y = %s %s

DESCRIPTION

The **set_port_location** command successfully annotated the port location. If only one dimension was specified, only that dimension was changed. The location set by the **set_port_location** command will take precedence over any PDEF-based annotation.

WHAT NEXT

To reset the port location, use the **set_port_location** command without the **-X** and the **-Y** options. FloorPlan Manager will then use any value on the design that was annotated using a PDEF file. For more information, see the **read_pdef** man page, and the *Floor Plan Manage User Guide*.

LBO-18 (Error) Unable to find port %s in the current design.

DESCRIPTION

The **set_port_location** command could not find the specified port in the current design.

WHAT NEXT

Check the name of the port specified by the **set_port_location** command. Use the **find** command to get a list of ports in the current design.

LBO-19 (Error) Port %s does not have location information which can be changed.

DESCRIPTION

The **set_port_location** command could not change the specified dimension since the other dimension has not been annotated. If only one dimension is specified, that dimension is changed only if the value for the other dimension is known.

WHAT NEXT

Check the name of the port specified by the **set_port_location** command. Annotate both of the dimensions on the port.

LBO-20 (Error) set_port_location cannot annotate more than one port at a time.

DESCRIPTION

The **set_port_location** command could not annotate port locations because more than one port was specified.

WHAT NEXT

Check the number of ports specified by the **set_port_location** command. Execute the **set_port_location** command for each port location you wish to specify.

LBO-21 (error) Coordinates set must consist of two floating point

values.

DESCRIPTION

The two values are for X coordinate and Y coordinate. They are expected to be in micron unit.

WHAT NEXT

provide correct number of arguments.

LBO-22 (error) Pin location cannot be set without cluster information.

DESCRIPTION

Design does not have cluster information. Cluster information is required to set the pin location on a library cell.

WHAT NEXT

Load the cluster information using the **read_pdef** or **read_clusters** command and then issue **set_port_location** command.

LBO-23 (error) The library cell %s could not be found in the target library.

DESCRIPTION

The library cell specified does not exist in the target library. The cell should exists in the target library in order to set its pin location.

WHAT NEXT

Check the cell name and make sure that this cell exists in the target library.

LBO-24 (error) Pin %s of library cell %s could not be found.

DESCRIPTION

The specified library cell exists in the target library but the specified pin could be found for this library pin.

WHAT NEXT

Specify the correct pin name.

LBO-25 (Warning) Library cell %s does not have any dimensions. The pins of cell %s will be assigned the location of the cell.

DESCRIPTION

You receive this warning message when the orientation of a cell is not North, and the dimensions of its library cell are not known. If the orientation of the cell is not North, it cannot determine the pin location without knowing the library cell dimensions.

WHAT NEXT

Set the library cell dimensions using **set_libcell_dimensions**.

LBO-30 (error) The core is entirely blocked and there is no vacant core space.

DESCRIPTION

You receive this error message when the core is entirely blocked due to fixed cells or obstructions. There is no vacant core space available for optimization.

WHAT NEXT

Review the PDEF file specified with the **read_pdef** command and the obstructions set using **create_obstruction**. Check if any obstructions that were supposed to be routing obstructions have been incorrectly specified as placement obstructions. If you are using Physical Compiler, use the Physical Compiler graphical user interface to view the floorplan.

LBO-31 (error) Port layer name and layer_area must be set together.

DESCRIPTION

To set port geometry, both layer name and layer_area must be specified.

WHAT NEXT

Use -layer and -layer_area option together for **set_port_location** command.

LBO-32 (warning) Missing pin location data in physical library for physical library pin %s on physical library cell %s.

DESCRIPTION

While attempting to calculate the location of a physical only pin, the problem was encountered where the location data for the physical library pin could not be found in the physical library. The location of the owning cell will be used for the location of the pin (for example in the GUI).

WHAT NEXT

It may be possible to obtain an improved physical library for the design which contains location data for all physical library pins.

SEE ALSO

LBO-33 (warning) Missing orientation while trying to calculate the location of pin %s on cell instance %s.

DESCRIPTION

While attempting to calculate the location of a physical only pin, the problem was encountered where the oorientation data for the cell instance could not be determined. The location of the owning cell will be used for the location of the pin (for example in the GUI).

WHAT NEXT

Try setting the orientation of the cell instance.

SEE ALSO

LBR

LBR-0 (error) Cannot find the %s '%s' in the library '%s'.

DESCRIPTION

This error message occurs when the specified design unit cannot be found in the specified library.

WHAT NEXT

Use the **report_design_lib** command to determine the contents of a library. If the design unit is not in the library, reanalyze the design unit using the **analyze** command with the **-library** or the **-work** option.

SEE ALSO

report_design_lib(2)

LBR-1 (warning) Cannot find the %s '%s' in the library '%s'.

DESCRIPTION

This warning message occurs when the specified design unit is not in the specified library.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this warning message, use the **report_design_lib** command to determine the contents of a library. If the design unit is not in the library, reanalyze the design unit using the **analyze** command with the **-library** or the **-work** option.

SEE ALSO

report_design_lib(2)

LBR-2 (error) The library '%s' is mapped to the directory '%s',

which is not %s.

DESCRIPTION

This error message occurs when attempting to read from or write to a library that is mapped to a directory without the required permissions.

WHAT NEXT

Check the permissions on the specified directory and run the command again.

SEE ALSO

read(2)
write(2)

LBR-3 (warning) The %s '%s' is out of date with respect to its source file '%s'.

DESCRIPTION

This warning message occurs when the file containing the design unit has been modified since the last time the design unit was analyzed.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this warning message, reanalyze the file containing the design unit with the **analyze** command.

SEE ALSO

analyze(2)

LBR-4 (error) The %s '%s' is out of date and the source file '%s' cannot be found.

DESCRIPTION

This message indicates that the file that contains the specified design unit cannot be located.

WHAT NEXT

Ensure that the specified file has not been renamed or moved, verify the file name, and run the command again.

LBR-5 (error) The %s '%s' is out of date. Reanalyze it and try again.

DESCRIPTION

This error message indicates that the specified design unit depends on more recently analyzed files.

WHAT NEXT

Use the **analyze** command to reanalyze the file that contains the specified design unit.

SEE ALSO

analyze(2)

LBR-6 (error) The library '%s' is not mapped to a directory.

DESCRIPTION

This message indicates that you attempted to access a library which does not have a valid directory path associated with it.

WHAT NEXT

For information on mapping between design libraries and paths, refer to the **define_design_lib** command manual page. Mapping can also be done via the .synopsys_vss.setup file.

LBR-7 (error) Could not write the file '%s'.

DESCRIPTION

This message indicates that the file could not be opened for writing.

WHAT NEXT

For previously existing files, check the write permissions. When trying to create a new file, check the full directory path for existence, and ensure that the file name is not an existing directory name.

LBR-8 (warning) Library logical name '%s' is not mapped to a host directory.

DESCRIPTION

This warning message occurs when the specified logical name could not be mapped to a physical host directory.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, provide an appropriate mapping to a host directory, make sure the directory exists, and run the command again. If this does not resolve the problem, please contact Synopsys support. For instructions for creating, packaging, and sending a test case, go to http://www.synopsys.com/testcase.

LBR-9 (warning) The .mra file '%s' contains invalid data. The invalid data is being ignored.

DESCRIPTION

This warning message indicates that the .mra file has been incorrectly modified, with extra character(s) after the architecture name, by a source other than this program. The .mra file should only contain a single architecture name per line, directly followed by a new line.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this warning in the future, reanalyze the design. This automatically generates a new .mra file.

SEE ALSO

analyze(2)

LBR-10 (warning) The environment variable '%s' has no value.

DESCRIPTION

This message indicates that the given environment variable has not been set.

WHAT NEXT

Set the environment variable to a legal value.

LBR-11 (warning) Design library name '%s' is reserved, and cannot be defined by the user.

DESCRIPTION

This warning message occurs when the specified library name is predefined by Synopsys. The library name cannot be redefined.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, you can use the **define_design_lib** command to define a new library name and run the command again.

SEE ALSO

define_design_lib(2)

LBR-12 (warning) Logical library name '%s' is reserved, and cannot be mapped by the user.

DESCRIPTION

This warning message occurs when the specified library name has been predefined by Synopsys. The name cannot be remapped.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result it not what you intended, you can use the **define_design_lib**

command to define a new library name.

SEE ALSO

define_design_lib(2)

LBR-13 (warning) Logical library name '%s' cannot be mapped to '%s', which is reserved.

DESCRIPTION

This warning message occurs when the specified library name has been predefined by Synopsys. The specified name cannot be used.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, use the **define_design_lib** command to define a new library name. You can then map the logical library name to that new library name.

SEE ALSO

define_design_lib(2)

LBR-14 (error) '%s' in library '%s' is a %s. A %s was expected.

DESCRIPTION

This message indicates that the given design unit's type in the specified library does not match the expected type, probably because of a naming conflict between two different design unit types.

WHAT NEXT

Ensure that all primary design units in the library have unique names.

LBR-15 (information) Re-analyzing the out of date %s '%s'.

DESCRIPTION

This message indicates that the source file containing the given design unit is out of date, and will be re-analyzed.

WHAT NEXT

This is only an informational message. The design will be re-analyzed automatically.

LBR-16 (error) You cannot overwrite a library file.

DESCRIPTION

This message indicated that you attempted to write a library file to an existing file that has the same name; this is not allowed.

WHAT NEXT

Choose a unique filename for this library information.

LBR-17 (warning) The package '%s' cannot be saved. It will be used for this read, but cannot be used for subsequent reads.

DESCRIPTION

This warning message occurs when you attempt to write to the directory that is mapped to the working library; this directory is not writable.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, see the **write_design_lib_paths** command man page for information about mapping between design libraries and paths.

SEE ALSO

write_design_lib_paths(2)

LBR-18 (error) The variable '%s' is not set. You must use the '-filename' argument.

DESCRIPTION

This error message occurs when the tool cannot determine where to write the results of the **write_design_lib_paths** command.

WHAT NEXT

Set the specified environment variable, or use the **-filename** or **-dc_setup** option when issuing the **write_design_lib_paths** command.

SEE ALSO

write_design_lib_paths(2)

LBR-19 (error) The entity '%s' does not have an analyzed architecture.

DESCRIPTION

This error message occurs when running the **elaborate** command. The tool encountered an entity that does not have an analyzed associated architecture.

WHAT NEXT

Analyze an architecture for this entity and then rerun the **elaborate** command.

SEE ALSO

elaborate(2)

LBR-20 (error) You cannot specify an architecture when elaborating a configuration.

DESCRIPTION

This error message occurs when the **elaborate** command is run with the **-architecture** option on a configuration.

WHAT NEXT

Reissue the **elaborate** command without the **-architecture** option.

SEE ALSO

elaborate(2)

LBR-21 (warning) The design '%s' has no parameters. The parameters '%s' have been ignored.

DESCRIPTION

This warning message occurs when parameters are specified for a design that does not require parameters. The specified parameters are ignored when building the design.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, use the dc_shell command **report_design_lib** *library_name* to generate a report on the contents of the design library that contains the design. In the report table, an entry with a *p* notation identifies a design that has parameters.

Ignore this warning message if you have a DesignWare library module that requires parameter(s) to select a specific implementation, but the implementation itself does not accept parameters. An example of this is an elaborated and compiled gate-level .db implementation.

SEE ALSO

report_design_lib(2)

LBR-22 (error) The library '%s' cannot be mapped to the same directory as '%s'.

DESCRIPTION

This error message occurs when attempting to map the specified libraries to the same directory. This is illegal.

WHAT NEXT

Remap one of the libraries to a different directory using the **define_design_lib** command with the **-path** option, or specify the mapping in the .synopsys_vss.setup file.

SEE ALSO

define_design_lib(2)

LBR-23 (error) Could not delete the file '%s'.

DESCRIPTION

This error message occurs when the library manager cannot remove the specified file. This should only happen if the permissions on the file are such that you do not have remove permission.

WHAT NEXT

Check the permissions on the specified file. If appropriate, change the permissions to allow you to remove the file in question. Otherwise, contact your System Administrator for assistance.

LBR-24 (error) The file '%s' does not contain the design '%s'.

DESCRIPTION

This error message occurs when the specified .db file does not contain the entity that was expected.

WHAT NEXT

Rewrite the .db file to the library, using the **write** command with the **-library** option. This produces a file in the format that the tool expects.

SEE ALSO

write(2)

LBR-25 (error) The file '%s' contains more than one entity.

DESCRIPTION

This error message occurs when the specified .db file contains multiple entities. The .db files stored in design libraries must contain only one entity per file.

WHAT NEXT

Rewrite the .db file to the library using the **write** command with the **-library** option. This produces a file in the format that the tool expects.

SEE ALSO

write(2)

LBR-26 (error) Could not read in the file '%s'.

DESCRIPTION

This error message occurs when attempting to elaborate an entity out of a design library, and the elaboration failed.

WHAT NEXT

The .db file is probably corrupt. Regenerate the .db file, and overwrite the existing file in the design library.

SEE ALSO

elaborate(2)

LBR-27 (information) Overwriting the '%s' version of architecture '%s' with a '%s' version in the library '%s'.

DESCRIPTION

This information message occurs when you write an architecture into a library. Since each design library is allowed to have only one architecture associated with a particular entity, any existing architectures are overwritten.

WHAT NEXT

This is an information-only message. No action is required.

LBR-28 (error) The %s '%s' depends on the %s '%s' which has been analyzed more recently. Reanalyze the source file for '%s' and try again.

DESCRIPTION

This error message occurs when the specified design unit is out of date with respect to a design unit on which it depends.

WHAT NEXT

Reanalyze the dependent design's source file and run the command again.

LBR-29 (error) Design library '%s' cannot be mapped to the same directory as design library '%s'.

DESCRIPTION

This error message occurs because it is illegal to have two design libraries mapped to the same directory. Doing so can cause library aliasing problems.

WHAT NEXT

One of the two libraries must be mapped to a different directory.

LBR-30 (error) Recursion detected in .syn files. Design unit '%s' was referenced multiple times.

DESCRIPTION

This error should never happen because it is impossible to create recursive dependencies amongst design units. This check is there simply for completeness to eliminate the chance of infinite recursion while checking design units.

WHAT NEXT

Check the dependency hierarchy of the design unit that is in question. If you can find the recursion (which would be illegal VHDL), remove one of the links in the loop to prevent the recursion.

LBR-31 (error) '%s' is being defined as a design library (using the '>'operator), but it was already defined as a logical library (using the ':' operator or the define_design_lib command). To modify the directory that '%s' is mapped to, use ':' or the define_design_lib command.

DESCRIPTION

This error message occurs because a logical library with the specified name has already been defined. The tool does not allow both logical and design libraries to be specified with the same name.

In Example 1 below, DW03 is both a logical library and a design library:

Example 1 .synopsys_vss.setup file:

```
DW03: ./work
DW03 > DEFAULT
```

In Example 2, SOME_LIB is both a logical library and a design library:

Example 2 .synopsys_vss.setup file:

```
SOME_LIB > SOME_LIB
SOME_LIB: ./work
```

WHAT NEXT

This is a limitation in the synthesis support of design libraries. As the error message states, you should be able to get the desired effect by using the colon (:) operator (or the **define_design_lib** command) to redefine the library in question.

In Example 1 above, the logical library DW03 can be renamed to something else, such as DW_03. In Example 2 the line SOME_LIB > SOME_LIB can be eliminated, since it is implied by the line SOME_LIB: ./work.

SEE ALSO

define_design_lib(2)

LBR-32 (error) Cannot find file '%s'. Update failed.

DESCRIPTION

This error message occurs when running the **analyze** command with the **-update** option. The specified .update file could not be found in the directory of your HDL source, so the **analyze** command fails.

WHAT NEXT

Contact your part vendor to obtain the necessary .update file(s).

SEE ALSO

analyze(2)

LBR-33 (error) File '%s' was not generated from '%s'. Update failed.

DESCRIPTION

This error message occurs when running the **elaborate** command with the **-update** option, and a .update file cannot be found in the directory of your HDL source. The .update file must have been generated using **analyze -create_update** on exactly the same HDL source file as you are using now.

The HDL source file you are using has been modified, so the analysis failed.

WHAT NEXT

Use the original HDL source file, or do not specify the **-update** option. Contact your part vendor if you think you have been given the wrong .update or HDL source file.

SEE ALSO

elaborate(2)

LBR-50 (error) An order-based parameter %s was specified

after a name-based parameter.

DESCRIPTION

This error message occurs when the **-parameters** option of the **elaborate** command includes a combination of order-based and name-based parameter values, and all of the order-based parameters are not specified before name-based parameters. It is possible that a syntax error has caused a named-base parameter to be treated as an order-based parameter.

WHAT NEXT

Modify the **-parameters** option of the **elaborate** command so that all order-based parameters occur before name-based parameters, or correct the syntax error.

SEE ALSO

elaborate(2)

LBR-51 (error) Parameter '%s' is multiply defined.

DESCRIPTION

This error message occurs when the same parameter appears more than once in the parameter list specified when running the **elaborate** command. Each parameter can be specified only once.

Parameters are not case-sensitive. You might have specified two names that differed only in case (uppercase and lowercase).

WHAT NEXT

Specify the parameter only once. To ensure that each parameter name is unique, see the parameter syntax explanation in the **elaborate** command man page.

SEE ALSO

elaborate(2)

LBSYN-1 (error) The parameter '%s' has been defined multiple times in module '%s'.

DESCRIPTION

You receive this message during reading of a library, if the **read_lib** command finds that the same parameter has been defined more than once in the synthetic module. Each parameter must have a unique definition.

WHAT NEXT

Edit the .sl file to remove the duplicate parameter definition from the synthetic module. Then reexecute **read_lib**.

LBSYN-2 (error) Pin association '%s' must specify exactly one of "oper_pin" or "value".

DESCRIPTION

You receive this message if the library being read contains a pin association with multiple specifications. The pin association must have either one oper_pin or a value.

WHAT NEXT

Locate the specified pin association in the synthetic library file, and edit the file so that the pin association specifies either one oper_pin or a value. Then reexecute **read_lib**.

LBSYN-3 (error) Binding '%s' must specify "bound_operator".

DESCRIPTION

You receive this message during reading of a library, if the **read_lib** command finds a binding that does not have a bound_operator specification in the binding group in the current processed module. Each binding must have a bound_operator specification.

WHAT NEXT

Edit the file to add the missing bound_operator specification. Then reexecute **read_lib**.

LBSYN-4 (error) The module or component '%s' requires a design_library attribute.

DESCRIPTION

Each module and component in a synthetic library must have a design_library attribute that identifies the design library where its implementation source is stored. The library should correspond to a library identified in the design_design_lib command.

WHAT NEXT

Supply a design_library attribute.

LBSYN-5 (error) Operator pin '%s' must either be "input" or "output".

DESCRIPTION

Synthetic library operators can only represent combinational functions.As such, it does not make sense to have inout pins on operators. Functions with inout pins must be instantiated directly as synthetic library modules.

WHAT NEXT

Do not use operators with inout pins. Use modules if inout pins are really required.

LBSYN-6 (error) Operator '%s' data_class must either be "unsigned" or "signed".

DESCRIPTION

Synthetic library operators can only have a data_class value of "signed" or "unsigned". Other values are illegal.

WHAT NEXT

LBSYN-7 (error) Module pin ’%s’ must have a ’bit_width’ attribute.

DESCRIPTION

’Bit_width’ is a required attribute on all synthetic library module pins.

WHAT NEXT

LBSYN-8 (error) The value "%s" in group %s(%s) is not legal.

DESCRIPTION

Only a string of 1’s and 0’s is allowed in the attribute. The only exception is that "unbound" can occur in constraint groups.

WHAT NEXT

To fix the syntax error, use a legal value.

LBSYN-9 (error) The value attribute is missing in group %s(%s).

DESCRIPTION

A value attribute is required in this group.

WHAT NEXT

Please supply a value attribute.

LBSYN-10 (error) Parameter ’%s’ cannot have both a constant attribute

and a formula attribute.

DESCRIPTION

The constant attribute is used to assigned the parameter a typed constant value. The formula attribute is used to assigned the parameter a computed expression. Only one of these can be used to assign the parameter a value.

WHAT NEXT

Eliminate either the constant or the formula attribute.

LBSYN-11 (error) Parameter '%s' has a constant attribute without a type attribute.

DESCRIPTION

A parameter that sets its value using the constant attribute must have a type attribute to declare the constant's type.

WHAT NEXT

Add a type attribute.

LBSYN-12 (warning) In parameter '%s', the type attribute is ignored.

DESCRIPTION

The formula attribute ignores the type declaration in the type attribute. The formula's type is determined from the equation.

WHAT NEXT

Use the constant attribute to declare typed parameters.

LBSYN-13 (error) The string %s can not be evaluated,

therefore it can’t be used for the bit_width value on pin %s.

DESCRIPTION

This message indicates that the given string contained parameter(s) that were not previously defined in the current module’s scope. Therefore, the string can not be used as the value for the bit_width attribute on the given pin.

WHAT NEXT

Modify the .sl file, by creating the desired parameter group in the module that contains the given pin group. The parameter group should be defined prior to the definition of the pin group.

LBSYN-15 (error) The binding group %s in the module %s does not
contain any pin_association groups.

DESCRIPTION

This message indicates that the given binding group in the stated module does not contain any pin_association groups. At least one pin_association group is required for a binding group. If this is a sequential binding group, at a minimum the clock pin must be connected to the clock input of the operator in each state.

WHAT NEXT

Modify the .sl file, by creating the necessary pin_association group(s) for the binding. The pin_association group statement defines how the module pins are associated with synthetic operator pins and constant values. See the DesignWare Developer Guide for further information on this topic.

LBSYN-16 (warning) The parameter %s does not have the hdl_parameter attribute set true, nor does it have a formula.

DESCRIPTION

This message indicates that the given parameter group does not have its hdl_parameter attribute set to "true", nor does it have a formula defined for it. A parameter must have either a formula or the hdl_parameter attribute set to "true" in order for this parameter to be referenced successfully.

WHAT NEXT

Modify the .sl file to include a formula and/or set the hdl_parameter attribute to "true". See the DesignWare Developer Guide for further information on this topic.

LBSYN-17 (warning) the parameter %s formula may not evaluate correctly during a compile operation because of: %s.

DESCRIPTION

This message indicates that the given formula potentially has an error in it which might prevent this parameter from being evaluated during run time. The reason given may provide helpful information for correcting the problem.

Certain static checks, such as syntax, are performed on formulas within parameters when a library is read in. During this process, a formula is evaluated with values that are available statically. Variables within the formula which are not known until a compile is executed can not be checked.

WHAT NEXT

Check the formula attribute within the given parameter for the problem indicated by the message. Edit the .sl file as necessary to correct the problems.

LBSYN-18 (error) Substitute Licenses are for internal use only.

DESCRIPTION

The "Substitute License" feature is for internal Synopsys use only. This feature is not available to Synopsys customers.

WHAT NEXT

Remove the "substitute_license" group from your implementation description or acquire a "Synopsys" license.

LBSYN-19 (error) The "substitute_license" group requires an

"original_license" attribute.

DESCRIPTION

The "substitute_license" group for synthetic module implementations requires at least an "original_license" and a "substitute_license" attribute. An example "substitute_license" group is:

```
    substitute_license () {
original_license : lic_a;
substitute_license : lic_b;
valid_modules : "DW01_mult DW01_add DW01_addsub";
    }
```

WHAT NEXT

Either add the "original_license" attribute or delete the "substitute_license" group.

LBSYN-20 (error) The "substitute_license" group requires a "substitute_license" attribute.

DESCRIPTION

The "substitute_license" group for synthetic module implementations requires at least an "original_license" and a "substitute_license" attribute. An example "substitute_license" group is:

```
    substitute_license () {
        original_license : lic_a;
        substitute_license : lic_b;
        valid_modules : "DW01_mult DW01_add DW01_addsub";
    }
```

WHAT NEXT

Either add the "substitute_license attribute or delete the "substitute_license" group.

LBSYN-21 (warning) The "substitute_license" group contains

no "valid_modules" attribute.

DESCRIPTION

No "valid_modules" attribute has been specified for this "substitute_license" group. This will allow any modules licensed with the "original_license" to be instantiated in this implementation without consuming the license. An example "substitute_license" group is:

```
    substitute_license () {
        original_license : lic_a;
        substitute_license : lic_b;
        valid_modules : "DW01_mult DW01_add DW01_addsub";
    }
```

WHAT NEXT

If improved protection is desired use the "valid_modules" attribute to restrict the modules to which this license substitution will be applied.

LBSYN-22 (error) Original license must be DesignWare-Foundation.

DESCRIPTION

The "Original License" feature must be DesignWare or DesignWare-Foundation license. We only support Foundation license substitution.

WHAT NEXT

Correct your Original license name. Or delete "susbstitute_license" group from your implementation declaration.

LBSYN-23 (error) Only one generator group can exist in a library.

DESCRIPTION

A synthetic library can have at most one generator group specifying information used during creation of library implementations.

WHAT NEXT

Remove generator groups from the synthetic library. Separate implementations requiring different generators from a single synthetic library into multiple synthetic libraries. In each new synthetic library only one generator should exist with information used to generate all implementations in the new synthetic library.

LBSYN-24 (error) The "generator" group requires the '%s' attribute.

DESCRIPTION

The "generator" group for synthetic libraries requires a minimum set of attributes. This set consists of the following attributes: "executable_os_variable", "generator_interface", and "contact_upon_failure".

WHAT NEXT

Either add the required attributes to the "generator" group or delete the "generator" group.

LBSYN-25 (error) The "generator" group requires a "generator_interface" attribute.

DESCRIPTION

The "generator" group for synthetic libraries requires at least an "executable_os_variable" attribute, a "generator_interface" attribute, and a "contact_upon_failure" attribute. An example "generator" group is:

```
    generator (mult_gen) {
        generator_interface : file;
        executable_os_variable : "/usr/local/bin/mgen";
        contact_upon_failure : "MGEN Customer Support Hotline";
    }
```

WHAT NEXT

Either add the "generator_interface" attribute or delete the "generator" group.

LBSYN-26 (error) The "generator" group requires a

"contact_upon_failure" attribute.

DESCRIPTION

The "generator" group for synthetic libraries requires at least an "executable_os_variable" attribute, a "generator_interface" attribute, and a "contact_upon_failure" attribute. An example "generator" group is:

```
    generator (mult_gen) {
        generator_interface : file;
        executable_os_variable : "/usr/local/bin/mgen";
        contact_upon_failure : "MGEN Customer Support Hotline";
    }
```

WHAT NEXT

Either add the "contact_upon_failure" attribute or delete the "generator" group.

LBSYN-27 (error) Only one "verilog" subgroup may exist in a "generator" group.

DESCRIPTION

A "generator" group may have at most one "verilog" subgroup specifying information used during processing of generator produced Verilog netlists.

WHAT NEXT

Remove "verilog" groups from the generator group leaving at most one "verilog" group.

LBSYN-28 (error) Only one "vhdl" subgroup can exist in a "generator" group.

DESCRIPTION

A "generator" group can have at most one "vhdl" subgroup specifying information used during processing of generator produced VHDL netlists.

WHAT NEXT

Remove "vhdl" groups from the generator group leaving at most one "vhdl" group.

LBSYN-29 (error) The attribute "output_format" requires either a "vhdl" or a "verilog" subgroup.

DESCRIPTION

When the "output_format" attribute specifies "soft_macro", a "vhdl" subgroup or a "verilog" subgroup is required in the "generator" group.

WHAT NEXT

Add a "verilog" or "vhdl" subgroup to the generator group. Change the value of the "output_format" to something other than "soft_macro". Removing the output_format attribute from a generator group will not solve the error because soft_macro is the default output format.

LBSYN-30 (error) Specify either a "vhdl" or "verilog" group, but not both.

DESCRIPTION

When the "output_format" attribute specifies "soft_macro", a "vhdl" subgroup or a "verilog" subgroup is required in the "generator" group.

WHAT NEXT

Add a "verilog" or "vhdl" subgroup to the generator group. Change the value of the "output_format" to something other than "soft_macro". Removing the output_format attribute from a generator group will not remove the error because soft_macro is the default output format.

LBSYN-31 (information) Generator ’%s’ assumed to create DB output.

DESCRIPTION

Neither a "vhdl" group nor a "verilog" group were found within the "generator" group. Thus, the netlist created by the generator is assumed to be a .db file.

WHAT NEXT

If the generator does not produce DB files, then please add either a "verilog" or

"vhdl" subgroup to the generator group. Alternatively, add the "output_format" attribute with the value "hard_macro" to the generator group to specify a hard macro. The default output format expected from the generator is a soft macro.

LBSYN-32 (error) The formula for parameter ’%s’ requires a string expression.

DESCRIPTION

The expression used in the formula should be a double-quoted string.

WHAT NEXT

Modify the formula attribute to the form ’formula : "expression"’.

LBSYN-33 (error) Only one "sdf" subgroup may exist in a "generator" group.

DESCRIPTION

A "generator" group may have at most one "sdf" subgroup specifying information used during processing of generator produced netlists.

WHAT NEXT

Remove "sdf" groups from the generator group leaving at most one "sdf" group.

LBSYN-34 (warning) The module group ’%s’ has no output pins defined.

DESCRIPTION

Synthetic library module declarations must contain at least one output pin group. Additionally, a warning is generated if no input pin groups are declared within the synthetic module.

WHAT NEXT

Add an output pin group to the synthetic module.

LBSYN-35 (warning) The module group '%s' has no input pins defined.

DESCRIPTION

Synthetic library module declarations should generally contain at least one input pin group. This message can also indicate that a synthetic module has been declared with only one port which has the direction attribute value of "inout." Additionally, a warning is generated if no output pin groups are declared within the synthetic module.

WHAT NEXT

Add an input pin group to the synthetic module.

LBSYN-36 (error) The pin '%s' in module group '%s' has an improper
direction specified.

DESCRIPTION

Pin groups within synthetic library modules must specify a direction. This direction attribute can specify one of three choices: "input", "output", or "inout". For example a valid direction attribute within a pin specification might appear as:

```
pin (A) { direction : input; bit_width : "width"; }
```

WHAT NEXT

Change the value of the direction attribute to "input", "output", or "inout".

LBSYN-37 (warning) The pin associations for the module %s do not

bind to any output pins.

DESCRIPTION

One of the pin associations for a module should be bound to an output pin of the module. Note that only one pin association in all of the binding groups needs to be bound to an output pin. Furthermore, module ports of types output and inout are considered valid for pin associations.

WHAT NEXT

Specify a pin association group for the module that names a module pin with the direction of output or inout.

LBSYN-38 (warning) The pin associations for the module %s do not
bind to any input pins.

DESCRIPTION

One of the pin associations for a module should be bound to an input pin of the module. Note that only one pin association in all of the binding groups needs to be bound to an input pin.

WHAT NEXT

Specify a pin association group for the module that names a module pin with the direction of input or inout.

LBSYN-39 (warning) The sequential bindings allow states '%s' and '%s'
to simultaneously use pin '%s' on module '%s'.

DESCRIPTION

This warning indicates that non-clock pins bound to one or more nonexclusive states have been found in the synthetic library description.

WHAT NEXT

Add resources to the module and use these resources within the binding to exclude the possibility of pins being simultaneously used.

LBSYN-40 (Error) The '%s' group named '%s' is multiply defined.

DESCRIPTION

Two or more groups exist within the parent of the same type and the same name.

For example in the fragment of synthetic library code:

```
: : module (ram_wrapper) { resource(address_lines) {} resource(data_in_lines) {}
resource(address_lines) {} resource(address_lines) {} : :
```

The resource group address_lines has been defined three times.

WHAT NEXT

Give each group of the same type a unique name or remove redundant groups.

LBSYN-41 (Warning) The resource named '%s' is used but not defined
in the synthetic module '%s'.

DESCRIPTION

A use_resource group refers to a resource which has not been defined with a resource group.

In the following fragment of synthetic library code a single resource token, r_only, is defined. However, a resource token is used, undefined_resource_token, which has not been defined.

```
: : module (ram_wrapper) { resource(r_only) {} /* This is the only resource defined.
*/ binding (b0) { : : state () { : : use_resource(undefined_resource_token) {} } } }
```

WHAT NEXT

Add a new resource group to the module, or remove the use_resource group that refers to the nonexistent resource.

LBSYN-42 (Warning) Operator '%s' has an excessive number (%d total) of bindings.

DESCRIPTION

The synthetic operator has a large number of either sequential or combinational bindings. A large number of bindings decreases performance, but does not otherwise affect functionality. A large set of bindings usually results from representing each combination of permutable pin with a binding.

Sequential bindings are considered separately from combinational bindings, and in both cases this warning is issued when more than 32 bindings exist.

WHAT NEXT

Verify the set of permutable inputs as specifed through the 'permutable_inputs' attribute. Eliminate unnecessary synthetic bindings.

LBSYN-43 (Error) Unable to find the operator pin '%s' named by an unbound_oper_pin group in binding '%s' in module '%s'.

DESCRIPTION

The unbound_oper_pin group found within a binding group (or a state group within a binding group for sequential bindings) names a pin on the operator that does not exist. Note that the pin names are case-sensitive, so this error can occur if an operator has a pin named "CLK" while the unbound_oper_pin group refers to a pin named "clk". The following synthetic library fragment suffers from this error:

```
: : operator(oper_0) { data_class : "signed"; pin(CLK) { direction : input; } pin(A)
{ direction : input; } pin(Z) { direction : output; } }

module (module_0) { : : binding(binding_0) { bound_operator : "oper_0";
unbound_oper_pin(clk) { value : "1"; } /* Error: There is no pin named clk (lower
case) in oper_0. */ : : } } : :
```

WHAT NEXT

Assuming that the name of the pin in the operator group is correct, change the name of the pin in the unbound_oper_pin group. Another possibility is to remove the unbound_oper_pin group from the synthetic library if it is unnecessary.

LBSYN-44 (Error) Multiple implementation groups named '%s' found in synthetic module '%s'.

DESCRIPTION

One or more implementation groups were found to have the same name. Each implementation group used in a set of synthetic libraries must have a unique group name within the context of the implementation's associated module.

WHAT NEXT

Rename the implementation groups in the synthetic library source file (.sl) with unique names.

LBSYN-45 (Error) Input pin '%s' cannot have both the 'sreset' and the 'areset' attribute in the synthetic module '%s'.

DESCRIPTION

A synthetic library module pin can only have either the sreset attribute or the areset attribute; not both.

In the following synthetic library source fragment, the pin 'a' is an error, while all other module pins properly specify the sreset and areset attributes.

```
            :
            :
      module (module_with_sequential_bindings) {
 pin(a) {
    direction : input;
    bit_width : "width_a";
    sreset    : TRUE;
    areset    : TRUE;
 }
 pin(b) {
    direction : input;
    bit_width : "width_b";
    sreset    : TRUE;
    areset    : FALSE;
 }
 pin(c) {
    direction : input;
    bit_width : "width_c";
 }
            :
            :
```

```
    }
        :
        :
```

WHAT NEXT

Remove either or both of the 'sreset' or 'areset' groups from the pin group. Another solution is to set one of the attributes' values to FALSE.

LBSYN-46 (Error) The binding '%s' in module '%s' contains a constraint specifying a nonexistent pin '%s' of the operator '%s'.

DESCRIPTION

Each synthetic library binding group is bound to an operator, and each binding group might contain a constraint group which refers to pins on the synthetic library operator. This error occurs when a constraint refers to a pin on an operator pin that does not exist.

In the following synthetic library source fragment, the binding binding_0 is bound to the synthetic operator oper_0. Furthermore, the binding group binding_0 specifies a constraint group that does not refer to any pin found in the operator oper_0.

```
: : operator(oper_0) { data_class : "signed"; pin(a) { direction : input; } pin(z) { direction : output; } }

module (module_0) { : : binding(binding_0) { bound_operator : "oper_0"; constraint(BogusPin) { value : "01"; } /* Error: There is no pin named BogusPin in oper_0. */ : : } } : :
```

WHAT NEXT

Modify the constraint to specify a valid operator pin or remove the constraint group altogether.

LBSYN-47 (Warning) The number of permutable inputs (%d) and the number of bindings (%d) do not agree for operator '%s'

in the module '%s'.

DESCRIPTION

Each possible ordering of of permutable input pins requires a unique binding. If the total number of bindings found does not equal or exceed the number of permutable inputs factorial (such as, n!), one or more bindings specifying various permutations have not been specified in the synthetic library.

Note that only bindings referring to the same operator within single modules are counted.

WHAT NEXT

Add binding groups to the synthetic library. One binding group is necessary to representing one pin permutation, and all possible pin permutations require a representative binding group.

Alternately, remove the permutable_inputs attribute from the operator group.

LBSYN-49 (Warning) The binding '%s' in module '%s' refers to an operator, '%s', which is not found in the synthetic library list.

DESCRIPTION

The binding group found within the module attempts bind to an operator which does not exist. This is only a warning as binding groups facilitate the creation of an implementation for the operator. A binding which specifies an operator that does not exist provides no useful information to the synthesis tool and is ignored.

WHAT NEXT

Check the operator spelling within the binding group for correctness. Also check the synthetic library or libraries to ensure that the operator has been declared with an operator group.

If the binding refers to an operator which has been removed from the synthetic library, then perhaps the binding group should also be removed from the synthetic library.

LBSYN-57 (Error) Multiple clock pins exist on module '%s'.

DESCRIPTION

Only one pin group within a module may specify the 'clock_pin' attribute.

WHAT NEXT

If the module only has combinational bindings, then remove all clock pin attributes from the module as they are unnecessary. If the module contains sequentail bindings or a mixture of sequential and combinational bindings, then remove all but one clock pin attributes from the module's pin groups.

LBSYN-58 (Error) Unbound operator pin value must evaluate to '1' for operator pin '%s' in binding '%s' in module '%s'.

DESCRIPTION

You receive this message because the **check_synlib** or **compile** command has found that the specified pin's unbound operator pin value does not evaluate to 1. It must have a value of 1.

WHAT NEXT

Locate the specified binding and pin in the appropriate file, and edit the file so that the unbound operator pin value evaluates to 1. Then reexecute **check_synlib** or **compile**.

LBSYN-59 (Warning) The width function is only supported in module group parameter formulas.

DESCRIPTION

Support for the width function only exists for parameters within module groups.

WHAT NEXT

Remove width functions from formulae which are not found in module groups.

Please refer to the DesignWare Developer Guide.

LBSYN-60 (Warning) Module pin '%s' in state '%s' of binding '%s' for module '%s' is not bound to any operator pin and the module pin does not specify a stall value.

DESCRIPTION

This message only occurs for modules containing sequential bindings. One or more states in these bindings does not have all module input pins either mapped to an operator pin or defined with a stall value.

WHAT NEXT

All control pins such as write enable must be fully specified at all times. Either add a stall value to the pin's definition in the module or add a pin_association in the state group.

For data pins it is optional to force a default value. If this is the intended usage this message can be ignored.

Please refer to the DesignWare Developer Guide.

LBSYN-61 (Error) Module '%s' is of type '%s', which is not a valid type.

DESCRIPTION

The value of the module_type attribute for this module specifies an incorrect type. Incorrect types are those types which are reserved for internal use. This error message may report a module has a type other than that found in the synthetic library source file (.sl). This indicates that the type specified in the synthetic library source file was not a recognized type.

WHAT NEXT

Note that the module_type attribute is optional.

Please refer to the DesignWare Developer Guide.

LBSYN-62 (Error) Operator '%s' is of type '%s', which is not a valid type.

DESCRIPTION

The value of the operator_type attribute for this operator specifies an incorrect type. Incorrect types are those types which are reserved for internal use. This error message may report an error for an operator which has a type other than that found in the synthetic library source file (.sl). This indicates that the type specified in the synthetic library source file was not a recognized type.

WHAT NEXT

Note that the operator_type attribute is optional.

Please refer to the DesignWare Developer Guide.

LBSYN-63 (error) Invalid formula '%s' for parameter '%s'.

DESCRIPTION

You receive this error message because the formula of the specified parameter contains the parameter itself. This will cause an infinite loop during evaluation of the formula.

WHAT NEXT

Verify that you have specified the correct parameter name and that the formula is accurate.

See the *DesignWare Developer Guide* for more information.

SEE ALSO

read_lib (2).

LDB-1 (error) Cannot delete views from the non-view-based library .db '%s'.

DESCRIPTION

This error message occurs because views can only be deleted in a view-based library .db file.

WHAT NEXT

Convert the original .db file into a view-based .db file, and read in the file again.

LDB-2 (error) Cannot delete view '%s'.

DESCRIPTION

This error message occurs when the specified view cannot be deleted because it is one of the following:

- A library-level view
- A cell_content or pin_content view
- Not defined in the ldb.schema

WHAT NEXT

If the object is a library-level view, a cell_content view, or a pin_content view, delete the object directly.

If the object is not defined in the ldb.schema, check the view name and correct as needed.

LDB-3 (error) Failed to load the skeleton view to get all cell

names.

DESCRIPTION

This error message occurs because when reading a view for unspecified cells, the tool reads the skeleton view node to get all cell names. If the skeleton view node cannot be read, this step fails and nothing is loaded.

WHAT NEXT

Make sure the skeleton view node can be read successfully by ldbatt.

LDB-4 (error) Failed to load view node '%s'.

DESCRIPTION

This error message occurs when there is incorrect data in the input view-based .db file.

The pattern of the view node name is as follows:

```
<path_name>/<view_based_db_file_name>/<lib_name>/<view_name>
```

WHAT NEXT

Make sure the content in the specified view node is correct (by ldbatt).

LEFIN-1 (error) There is no layer definition.

DESCRIPTION

You receive this message because the .plib format requires that all layer information be defined before all cell definitions.

WHAT NEXT

Put layer-related information in input Library Exchange Format (LEF) files.

EXAMPLE MESSAGE

Error: There is no layer definition. (LEFIN-1)

LEFIN-2 (error) There is no site information.

DESCRIPTION

You receive this message because the .plib format requires that all site information be defined before all cell definitions.

WHAT NEXT

Put site-related information in input Library Exchange Format (LEF) files.

EXAMPLE MESSAGE

Error: There is no site definition. (LEFIN-2)

LEFIN-3 (warning) There is no cell information.

DESCRIPTION

You receive this message because the .plib format prefers that at least one cell be specified in the file.

WHAT NEXT

Put the cell specification in input Library Exchange Format (LEF) files.

EXAMPLE MESSAGE

Warning: There is no cell information. (LEFIN-3)

LEFIN-4 (error) There is no via information.

DESCRIPTION

You receive this message because the .plib format requires that at least one cell be specified in the file.

WHAT NEXT

Put the via specification in input Library Exchange Format (LEF) files.

EXAMPLE MESSAGE

error: There is no via information. (LEFIN-4)

LEFIN-5 (warning) The technology information is inconsistent with the command line option specified.

DESCRIPTION

You receive this message because the **lef2plib** command line option **-std_cell** or **-array** is specified, but the Library Exchange Format (LEF) file content suggests a technology inconsistent with the given option.

When the **-std_cell** option is specified, the LEF technology information should not contain an ARRAY group. When the **-array** option is specified, the LEF LAYER group should not contain a PITCH attribute.

WHAT NEXT

Examine the command line option and LEF technology information: Ensure that they are consistent.

EXAMPLE MESSAGE

```
Warning: The technology information is inconsistent with the command line option
specified. (LEFIN-5)
```

SEE ALSO

lef2plib (1).

LGDS-1 (error) Macro %s is not specified in pseudo physical library. Cannot create full macro description in physical library.

DESCRIPTION

You receive this error message because the macro you specified for the **-gdsii** option of the **read_lib** command is not in the pseudo physical library (.pplib). Creation of cells failed.

WHAT NEXT

Add the missing macro to the pseudo physical library. The technology GDSII file might be different from the pseudo physical library. Check the input GDSII files.

SEE ALSO

read_lib (2).

LGDS-2 (error) Site information not found for macro %s.

DESCRIPTION

You receive this error message because the site attributes for the macro are not in the pseudo physical library. The library is therefore incomplete and cannot extract information from GDSII source files.

WHAT NEXT

Add the site attributes to the pseudo physical library. Then run the **read_lib** command again.

SEE ALSO

read_lib (2).

LGDS-3 (warning) The input gdsii filename %s does not exist.

DESCRIPTION

You see this warning because the GDSII filename you specified does not exist in the directory you gave as its location.

WHAT NEXT

Check to make sure that the file exists and is readable.

SEE ALSO

read_lib (2).

LGDS-4 (error) Pseudo physical library not loaded in memory.

DESCRIPTION

You receive this error message because Library Compiler cannot read the pseudo physical library (.pplib). The design cannot be created.

WHAT NEXT

Make sure to correct all errors reported during the loading of the pseudo physical library and then rerun Library Compiler.

SEE ALSO

read_lib (2).

LGDS-5 (error) Cannot access physical library resource information.

DESCRIPTION

You receive this error message because the pseudo physical library does not contain any resource information, which is required in case of GDSII extraction.

WHAT NEXT

Add the resource information into the pseudo library and read the library again using the **read_lib** command with the **-gdsii** option. Check to make sure that the pseudo physical library is the same library used for GDSII extraction.

SEE ALSO

read_lib (2).

LGDS-6 (error) Internal error in updating layer information.

DESCRIPTION

You receive this error message because the layer information obtained from the GDSII source file and the layer information in the pseudo physical library do not match.

WHAT NEXT

Make sure the pseudo physical library contains all of the layer information.

SEE ALSO

read_lib (2).

LGDS-7 (error) No layer map table found in library '%s'.

DESCRIPTION

You receive this error message because the pseudo physical library does not contain the layer objects you specified.

WHAT NEXT

Make sure to add all layer information to the pseudo physical library.

SEE ALSO

read_lib (2).

LGDS-8 (error) Internal error in updating

text_to_pin_layer_map.

DESCRIPTION

You receive this error message because the the text_to_pin_layer_map information you specified in the GDSII file is missing in the input pseudo physical library, or it is not correct in that library.

WHAT NEXT

Make sure that the text_to_pin_layer_map information in the input pseudo library and the input GDSII are the same.

SEE ALSO

read_lib (2).

LGDS-9 (error) Internal error in updating via information.

DESCRIPTION

You receive this error message because the via information you specified in the GDSII file is missing in the input pseudo physical library, or it is not correct in that library.

WHAT NEXT

Make sure that the Via information in the input pseudo physical library and the input GDSII file are the same.

SEE ALSO

read_lib (2).

LGDS-10 (error) Internal error in updating via_rule information.

DESCRIPTION

The via_rule information as obtained from the input pseudo physical library does not match the via_rule information in the input GDSII stream.

WHAT NEXT

Make sure the input pseudo physical library contains all via_rule names that match those in the input GDSII stream.

SEE ALSO

read_lib (2).

LGDS-11 (error) Internal error in updating via_rule_generate information.

DESCRIPTION

You receive this error message because the via_rule_generate information as obtained from the input pseudo physical library does not match the via_rule_generate information in the input GDSII file.

WHAT NEXT

Make sure that the via_rule_generate information in the input pseudo library and the input GDSII are the same.

SEE ALSO

read_lib (2).

LGDS-12 (error) Internal error in updating same_net_spacing.

DESCRIPTION

You receive this error message because the same_net_spacing layer names in the GDSII file do not match the the same_net_spacing layer names in the input pseudo physical library.

WHAT NEXT

Make sure the input pseudo physical library has same_net_spacing defined and that the layer names match the layer names defined in the resource group.

SEE ALSO

read_lib (2).

LGDS-13 (error) Internal error in updating in_site information.

DESCRIPTION

You receive this error message because the **in_site** attribute obtained from the input pseudo physical library does not match the **site definition in the input pseudo physical library.**

WHAT NEXT

Make sure that, before it is used in the macro, the input pseudo physical library contains all of the defined sites and that the site names match exactly the site names in the **in_site** attribute.

SEE ALSO

read_lib (2).

LGDS-14 (error) Internal error in updating array information.

DESCRIPTION

You receive this error message because the site array group as obtained from the input pseudo physical library does not match the site array group in the input GDSII stream, or the information is missing.

WHAT NEXT

Make sure the input pseudo physical library contains the defined site array group.

SEE ALSO

read_lib (2).

LGDS-15 (warning) Pseudo macro cell_type not supported for design :%s

DESCRIPTION

You see this warning because the cell_type specified in the pseudo physical library is not supported.

WHAT NEXT

Check to make sure that you specified a valid cell_type.

SEE ALSO

read_lib (2).

LGDS-16 (warning) Duplicate cell name %s found.

DESCRIPTION

You see this warning to let you know that the **read_lib** command encountered more than one macro with the same name and that the command recognizes the first instance and ignores the rest.

WHAT NEXT

Check and remove duplicate macro names in the input pseudo physical library.

SEE ALSO

read_lib (2).

LGDS-17 (warning) Foreign attributes are not set correctly in design %s.

DESCRIPTION

You see this warning because the foreign attributes as obtained from the input pseudo physical library are not correct or are missing.

WHAT NEXT

Make sure the foreign attributes are defined for the macro and are not null.

SEE ALSO

read_lib (2).

LGDS-18 (error) Internal error during creation of pins.

DESCRIPTION

You receive this error message because the pins in the specified macro group are present but are null.

WHAT NEXT

Check to make sure the pins are correct and that all of the required attributes are attached to them.

SEE ALSO

read_lib (2).

LGDS-19 (error) Internal error in finding routing_grid.

DESCRIPTION

You receive this error message because the routing_grid group you specified is not present in the input pseudo physical library.

WHAT NEXT

Make sure the input pseudo physical library contains the routing_grid group you specified.

SEE ALSO

read_lib (2).

LGDS-20 (error) Internal error in finding floorplan.

DESCRIPTION

You receive this error message because the floorplan is absent from the site array group you specified.

WHAT NEXT

Check the input pseudo physical library to make sure the floorplan group is not null

in the site array group.

SEE ALSO

read_lib (2).

LGDS-21 (error) Internal error in creation of tracks.

DESCRIPTION

You receive this error message because the track group is absent from the site array group you specified.

WHAT NEXT

Check the input pseudo library to make sure it contains the tracks and that the attributes are not null.

SEE ALSO

read_lib (2).

LGDS-22 (warning) The layer %s attributes are null.

DESCRIPTION

You see this warning because the layer you specified in the input pseudo physical library does not have any layer attributes defined on it.

WHAT NEXT

Check the input GDSII stream to make sure that the layer you specified is there and that the layer’s attributes are not null.

SEE ALSO

read_lib (2).

LGDS-23 (error) Shape type not supported in pseudo library.

DESCRIPTION

You see this error message because the input pseudo physical library does not support the geometry shape type you specified. The rectangle is the only geometry type supported.

WHAT NEXT

Update the input pseudo physical library so that the rectangle is the type of all of the geometries. A future release will support the other geometry types.

SEE ALSO

read_lib (2).

LGDS-24 (error) The layer name %s does not exist in the macro.

DESCRIPTION

You receive this error message because the layer name you specified in the via geometry is not defined in the input pseudo physical library.

WHAT NEXT

Check to make sure the layer information in the GDSII stream matches the layer information in the input pseudo physical library. Then verify that both sources contain the layer name you specified.

SEE ALSO

read_lib (2).

LGDS-25 (error) Internal error in extraction of macro '%s' geometries.

DESCRIPTION

You receive this error message because during execution of the **read_lib** command the extraction of rectangle geometries for macros failed.

WHAT NEXT

Make sure the **gds2_layer_map** is mapped correctly.

SEE ALSO

read_lib (2).

LGDS-26 (error) Internal error in creation of pins.

DESCRIPTION

You receive this error message because during the execution of the **read_lib** command the extraction of pin geometries from the input GDSII structure failed.

WHAT NEXT

Make sure the **pin_to_text_layer_map** is mapped correctly.

SEE ALSO

read_lib (2).

LGDS-27 (warning) You have objects outside the boundary for cell %s.

DESCRIPTION

You see this warning because the bounding box specified in the input GDSII stream is smaller than the cell.

WHAT NEXT

Check to see if it is possible to remove this warning by correcting the keepout clip box or the obstruction clip box.

SEE ALSO

read_lib (2).

LGDS-29 (information) The file name read is %s.

DESCRIPTION

You see this message to let you know that the file named is the input GDSII file name that will be converted to the physical library.

WHAT NEXT

This message is informational only and requires no action on your part.

LGDS-30 (warning) Structure '%s' is absent within input GDSII stream.

DESCRIPTION

You see this warning to let you know that the named macro structure is not present the input GDSII stream.

WHAT NEXT

Make sure the macro name is spelled correctly in the input pseudo physical library.

LGDS-31 (warning) There are multiple definitions of the structure '%s' within input GDSII stream.

DESCRIPTION

You receive this warning because the **read_lib** command encountered in the input GDSII file more than one definition of the named structure. Library Compiler will use the first instance for this structure and ignore the others.

WHAT NEXT

Remove the duplicate structure definitions.

. SH SEE ALSO

read_lib (2).

LGDS-40 (warning) You have no outline on layer %d for cell %s

DESCRIPTION

WHAT NEXT

EXAMPLE MESSAGE

LGDS-52 (error) Creating Via for port

DESCRIPTION

WHAT NEXT

EXAMPLE MESSAGE

LGDS-53 (error) Creating Obstruction for Macro

DESCRIPTION

WHAT NEXT

EXAMPLE MESSAGE

LGDS-54 (error) Creating Layer geometry for ports

DESCRIPTION

WHAT NEXT

EXAMPLE MESSAGE

LGDS-55 (warning) Obstruction clip box not specified for pseudo library.

DESCRIPTION

You see this warning because the obstructions you specified are not in the input pseudo physical library. If you do not specify the **obs_clip_box** attribute **gds2_extraction_rules**, the tool retains the complete cell layout and does not generate an obstruction.

WHAT NEXT

Check to make sure the pseudo physical library contains the obstruction clip box attribute values.

SEE ALSO

read_lib (2).

LGDS-60 (error) Error found in %s of input GDSii file.

DESCRIPTION

You see this error because the GDSii file is corrupted. Therefore cannot be accepted by Library Compiler.

WHAT NEXT

Make sure the input GDSii file is correct in format and data.

SEE ALSO

read_lib (2).

LIBAN-1 (error) Invalid switch value for '%s'.

DESCRIPTION

You specified an invalid value with the switch that is reported by the message. **Liban** stopped, because it could not process the command line with an invalid switch value.

WHAT NEXT

Invoke the **liban** command again with the correct switch value. If you don't know the valid values for a **liban** switch, consult the liban manpage. For quick reference, invoke **liban** without switches to print its correct command syntax.

```
> liban
Usage: liban [-arch VITAL] [-msgoff] \

             [-hazard transport | inertial | spike | glitch] [-xgen] [-chkoff]\

             [-nc] [-v] [-logical_name <name>] [-output name] \

             file.db
```

LIBAN-2 (error) Undefined switch '%s'.

DESCRIPTION

You specified an invalid switch that is reported by the message. **Liban** stopped because it could not process the command line with an invalid switch.

WHAT NEXT

Invoke the **liban** command again with the correct switch value. If you don't know the correct **liban** command syntax, consult the liban manpage. For quick reference, invoke **liban** without switches to print its correct command syntax.

```
> liban
Usage: liban [-arch VITAL] [-msgoff] \

             [-hazard transport | inertial | spike | glitch] [-xgen] [-chkoff]\

             [-nc] [-v] [-logical_name <name>] [-output name] \

             file.db
```

LIBAN-3 (error) Command syntax error is detected in '%s'.

DESCRIPTION

The command line **Liban** accepts only switches with or without a switch value and one db filename argument. In the command line, you specified an extra non-switch argument, which is reported by the message. This problem might also be caused by forgetting the leading '-' character of a switch or by trying to invoke **liban** with more than one db file. **liban** stopped because it could not process the command line with the specified command line syntax.

WHAT NEXT

Invoke the **liban** command again with correct switches and one db file. If you don't know the correct syntax for the **liban** command line, consult the liban manpage. For quick reference, invoke **liban** without switches to print its correct command syntax.

```
> liban
Usage: liban [-arch VITAL] [-msgoff] \

             [-hazard transport | inertial | spike | glitch] [-xgen] [-chkoff]\

             [-nc] [-v] [-logical_name <name>] [-output name] \

             file.db
```

LIBAN-5 (error) The '%s' DB file is not a technology library.

DESCRIPTION

The command liban requires a technology library db file. The message reports that the wrong db file has been specified and that the db file does not contain a technology library. The **liban** command aborts if a technology library is not provided. Common causes of this problem are:

- Providing a design db file with the liban command
- Making a mistake in typing the file name.

WHAT NEXT

Invoke the liban command again with a technology library db file. If you have access to Design Compiler (dc_shell) or Library Compiler (lc_shell) at your site, use the following command sequence to verify whether a db file is a technology library:

Assume the target db file is called example.db.

```
    dc_shell> read example.db
```

```
    dc_shell> list -lib
```

If the example.db file contains a library, the list command includes it in the execution result.

Another way to determine if a db file is a library is to issue the following command:

Assumeg the library object is called example.

```
    dc_shell> report_lib example
```

The library report header shows that the example object is a library if the file is a technology library db file.

Otherwise, consult your local Synopsys administrator to obtain the correct Synopsys technology library db file.

LIBAN-6 (error) You do not have authorization to use the '%s' library.

DESCRIPTION

The technology db file that was invoked with this command is not authorized to be used by this site. The particular technology library is protected by a security key, and requires a license from the ASIC vendor. The **liban** command aborts because this site is not authorized to use the library.

WHAT NEXT

Consult the ASIC vendor to obtain a license of the library in question.

LIBAN-7 (error) The '%s' library cannot be used for simulation.

DESCRIPTION

The technology db file that was invoked with this command is prohibited, by the semiconductor vendor, to be used by **liban**. The **liban** command aborts because this library is unauthorized for the **liban** application.

WHAT NEXT

Consult the semiconductor vendor to obtain a version of the db file authorized for **liban**.

LIBAN-11 (error) No technology library was specified.

DESCRIPTION

The **liban** command was invoked without a technology library db file. A technology library db file is mandatory for the command **liban**. The command stops because it cannot proceed without a technology library db file.

WHAT NEXT

Invoke the **liban** command again with a technology library db file.

LIBAN-12 (error) The switch value for '%s' is required.

DESCRIPTION

You specified the switch without a switch value and it requires a value. The command **liban** fails, because it cannot not process the command line without a valid switch value.

WHAT NEXT

Invoke the **liban** command again with a valid switch value. If you don't know the acceptable values for a **liban** switch, consult the liban manpage. For quick reference, invoke **liban** without switches to print ts correct command syntax.

```
> liban
Usage: liban [-arch VITAL] [-msgoff] \

             [-hazard transport | inertial | spike | glitch] [-xgen] [-chkoff]\

             [-nc] [-v] [-logical_name <name>] [-output name] \

             file.db
```

LIBAN-13 (error) Cannot read the '%s' file.

DESCRIPTION

The liban command requires a technology library db file. The message reports that the wrong db file has been specified. The db file does not contain a technology library. The **liban** command fails if it cannot read in the file correctly. Common causes of this problem are

- Providing a design db file with the liban command

- Making a mistake in typing the file name
- Using a corrupted db file

WHAT NEXT

Invoke the liban command with a valid technology library db file. If you have access to Design Compiler (dc_shell) or Library Compiler (lc_shell) at your site, use the following command sequence to verify whether a db file is a technology library:

Assume the target db file is called example.db.

```
dc_shell> read example.db
dc_shell> list -lib
```

If the example.db file contains a library, the list command includes it in the execution result.

Another way to determine if a db file is a library is to issue the following command:

Assume the library object is called example.

```
dc_shell> report_lib example
```

The library report header shows that the example object is a library if the file is a technology library db file.

Otherwise, consult your local Synopsys administrator to obtain the correct Synopsys technology library db file.

LIBAN-14 (error) The '%s' library is created with an older version of Synopsys software.

DESCRIPTION

The technology library db file, reported by the message, was compiled by an older version of the Synopsys Library Complier. The **liban** command requires a technology library db compiled by the Synopsys Library Compiler v2.2a or later.

WHAT NEXT

Consult your ASIC vendor to obtain a version of the db file compiled by a newer version of the Synopsys Library Compiler.

LIBAN-15 (error) The ’%s’ switch cannot be defined twice.

DESCRIPTION

You specified a switch (reported by the message) more than once in the command line. Each switch that requires a switch value can be specified no more than once in the command line. The **iban** command fails because it cannot process the command line with a duplicated switch.

WHAT NEXT

Invoke the **liban** command again with valid switches. Make sure that no duplicated command switch is specified.

LIBAN-16 (error) Bad switch value ’%s’ for ’-arch’ is detected. The valid switch value is VITAL.

DESCRIPTION

You specified an invalid value (reported by the message) with the ’-arch’ switch. **liban** fails because it cannot process the command line with an invalid switch value.

WHAT NEXT

Invoke the **liban** command with one of the valid switch values reported in the message.

LIBAN-17 (error) The ’%s’ switch is obsolete.

DESCRIPTION

This switch (reported by the message) is obsolete and no longer supported by **liban**.

WHAT NEXT

Do not use this switch with the **liban** command.

LIBCHK-100 (warning) %s data found. Please refer to %s.

DESCRIPTION

This message occurs when there are more serious issues that are found in the checking result listed in the table that follows. It redirects you to the message ID on next line that will give you detailed information.

WHAT NEXT

Please refer to the man page of the recommended message ID for details.

EXAMPLES

EXAMPLE MESSAGE

Warning: Mismatched data found. Please refer to LIBCHK-110. (LIBCHK-100)

LIBCHK-101 (error) %s data found. Please refer to %s.

DESCRIPTION

This message occurs when there are more serious issues are found in the checking result listed in the table that follows. It redirects you to the message ID on next line that will give you detailed information.

WHAT NEXT

Please refer to the man page of the recommended message ID for details.

EXAMPLES

EXAMPLE MESSAGE

Error: Mismatches data found. Please refer to LIBCHK-212. (LIBCHK-101)

LIBCHK-110 (information) List of cells with missing views

DESCRIPTION

This message is for reporting cells with missing views in physical library. All the physical cells with CEL/FRAM view missing will be reported in this table. In this report table, there are three columns: Cell name, CEL and FRAM. In the table, the CEL and FRAM columns list the cell name:version number. An X marks the view that is missing.

WHAT NEXT

If FRAM view is missing, it is more critical that missing CEL view. You should use extract BPV command extract_blockage_pin_via to generate FRAM view.

EXAMPLES

List of cells with missing views

Cell name	CEL	FRAM
dffs_1	dffs_1:2	X
tiehi_1	tiehi_1:2	X

EXAMPLE MESSAGE

Information: List of cells with missing views (LIBCHK-110)

LIBCHK-111 (warning) List of cells with mismatched views

DESCRIPTION

This message is for reporting cells with mismatched veiwewss in physical library. All the physical cells with CEL/FRAM view mismatched will be reported in this table. In this report table, there are five columns: Cell name, CEL Version, CEL Modified time, FRAM Version and FRAM Modified time. the CEL version and FRAM version columns list the version numbers, and the CEL and FRAM modified time columns list the time when the view was last modified. If a cell has an earlier FRAM view than its CEL view, it is marked as mismatched. The time checked is the internal view creation or modification time in the Milkyway database, not the UNIX time. No mismatch check is performed on the cell content.

WHAT NEXT

If a cell has an earlier FRAM view than its CEL view, please chec is its FRAM view is not updated. You may need to regenerate FRAM view by extracting BPV. If you read

FRAM views from the LEF and then stream in CEL views, the views are shown as mismatched. You can ignore this report in this case.

EXAMPLES

List of cells with mismatched views

Cell name	CEL Version	CEL Modified time	FRAM Version	FRAM Modified time
FILL8	2	Oct 24 19:17:9 2000	1	Oct 24 19:14:33 2000
FILL4	2	Oct 24 19:17:9 2000	1	Oct 24 19:14:33 2000
ANTENNA	2	Oct 24 19:17:23 2000	1	Oct 24 19:14:43 2000

EXAMPLE MESSAGE

Warning: List of cells with mismatched views (LIBCHK-111)

LIBCHK-112 (information) List of cells with same names

DESCRIPTION

This message is for reporting cells with same names among the specified main or design library and all physical reference libraries linked to the specified library. All the physical cells with same name will be reported in this table. In this report table, there are two columns: Cell name and Library list in precedence order. If there are cells with the same name in multiple reference libraries, the tool uses the first cell in the reference control file and ignores the remaining cells. This option does not check naming among the logic libraries.

WHAT NEXT

This is information only. If there are cells with the same name in multiple reference libraries, the tool uses the first cell in the reference control file and ignores the remaining cells. This option does not check naming among the logic libraries.

EXAMPLES

List of cells with same names

Cell Name	Library list in precedence order
XOR3	mainlib ref ref1 ref3 ref5
DFF	ref ref1 ref3

EXAMPLE MESSAGE

```
Information: List of cells with same names (LIBCHK-112)
```

LIBCHK-113 (information) List of signal EM data

DESCRIPTION

This message is for reporting signal EM data for routing layers in physical library. All EM data will be reported in this table. In this report table, there are three columns: Layer name, Current model and Model type. If no signal EM data at all in the library, it will not print the table but print a message: The library is missing signal EM data.

WHAT NEXT

If the signal EM data is not complete, for example, it exists only in some layers but not all layers, you should check and reload the missing data.

EXAMPLES

```
       List of signal EM data (LIBCHK-113)
-------------------------------------------------------------------
     Layer name      Current model       Model type
-------------------------------------------------------------------
     METAL1              peak                table
     METAL1              rms                 table
     METAL1              average             table
-------------------------------------------------------------------
```

EXAMPLE MESSAGE

```
Information: List of signal EM data (LIBCHK-113)
```

LIBCHK-114 (warning) The library is missing signal EM data.

DESCRIPTION

This message occurs when there is no signal EM data for routing layers at all in the physical library.

WHAT NEXT

For flows for and EM analysis with different temperature corners, signal EM data is required. You should check and reload the data into the physical library.

EXAMPLES

EXAMPLE MESSAGE

Warning: The library is missing signal EM data. (LIBCHK-114)

LIBCHK-115 (information) List of antenna rules

DESCRIPTION

This message is for reporting antenna rules in the layers in the specified main library. In this report table, there are six columns: Layer name, Mode, Diode mode, Default metel ratio, Default cut ratio and Max ratio.

WHAT NEXT

This is information only.

EXAMPLES

List of antenna rules

Layer Name	Mode	Diode mode	Default metal ratio	Default cut ratio	Max ratio
M1	1	3	500.00	20.00	500.00
M2	1	3	500.00	20.00	500.00

EXAMPLE MESSAGE

Information: List of antenna rules (LIBCHK-115)

LIBCHK-116 (warning) The library is missing antenna rules.

DESCRIPTION

This message occurs when no antenna rules exist in the physical library.

WHAT NEXT

Please check and load the antenna rule file after FRAM view is created.

EXAMPLES

EXAMPLE MESSAGE

```
Warning: The library is missing antenna rules. (LIBCHK-116)
```

LIBCHK-117 (warning) List of cells missing antenna property

DESCRIPTION

This message is for reporting missing antenna property for cells in physical library. All the cells that are missing antenna property will be reported in this table. In this table, it lists cell names and pin names missing the antenna property and the missing property type. If an input pin is missing the gate size, it is counted as missing the property. If an output pin is missing diode pro tection, it is counted as missing the property. If a macro is missing the hierarchical antenna property, then it is counted as missing the property. It is considered good practice to specify hierarchical antenna properties for macros.

WHAT NEXT

For antenna fix, please check and load the antenna properties (CLF) after FRAM view is created.

EXAMPLES

List of cells missing antenna property

Cell name	Cell type	Missing property	Pin name(s)
TLATNTSCAX1	StdCell	DiodeProt	ECK
TLATNTSCAX4	StdCell	DiodeProt	ECK
XOR2X4	StdCell	DiodeProt	Y
XOR2XL	StdCell	DiodeProt	Y

EXAMPLE MESSAGE

```
Warning: List of cells missing antenna property (LIBCHK-117)
```

LIBCHK-118 (information) List of cells with rectilinear

boundaries

DESCRIPTION

This message is for reporting cells with rectilinear boundaries in physical library. All cells with rectilinear boundaries will be reported in this table. In this report table, there are four columns: Cell name, Cell type, Number of points and Coordinate.

WHAT NEXT

This is information only. No further action is required.

EXAMPLES

List of cells with rectilinear boundaries

Cell Name	Cell type	Number of points	Coordinate
datapath	Macro	17	(78.750, 0.000) (78.750, 490.760)
			(44.435, 490.760) (44.435, 915.035)
			(27.440, 915.035) (27.440,1143.605)
			(0.000,1143.605) (0.000,1313.200)
			(677.295,1313.200) (677.295,1143.605)
			(649.855,1143.605) (649.855, 915.035)
			(632.860, 915.035) (632.860, 490.760)
			(598.545, 490.760) (598.545, 0.000)
			(0.017, 0.000)

EXAMPLE MESSAGE

Information: List of cells with rectilinear boundaries (LIBCHK-118)

LIBCHK-119 (information) List of physical only cells

DESCRIPTION

This message is for reporting physical-only cells in the physical library. In Milkyway, physical-only cells are defined as FillerCell: Filler cell IOPadCell: Pad filler (IO Pad) cell CornerCell: Corner (pad) cell ChipCell: Chip cell FlipChipPadCell:Flip chip pad (bump) cell CoverCell: Cover cell TapCell: Tap cell PGPinOnlyCell: PG-pin-only cell (containing only PG ports) In this report table, there are three columns: Cell name, Cell type and Physical library.

WHAT NEXT

Please verify that the cell types of the physical only cells are marked correctly in the physical library.

EXAMPLES

List of physical only cells

Cell name	Cell type	Physical library
FILL8	FillerCell	tsmc18_cg_LM
FILL64	FillerCell	tsmc18_cg_LM

EXAMPLE MESSAGE

Information: List of physical only cells (LIBCHK-119)

LIBCHK-120 (information) List of main and reference libraries

DESCRIPTION

This message is for reporting each libraries (main and reference physical libraries) and their full path locations, along with unit tile name and size. In this report table, there are four columns: Library name, Path, Unit tile and Tile size.

WHAT NEXT

This is information only. No further action is required. Note: if tile patterns listed in List of tile patterns are not consistent with tiles in List of main and reference libraries, it is recommended that users redo library prep to use same tile. Please refer to example 2.

EXAMPLES

Example 1:

Information: List of main and reference libraries (LIBCHK-120)

Library name	Path	Unit tile	Tile size
tsmc18_cg_LM	/remote/reg_designs/LIB_CENTER/180nm/san	unit	0.660x5.040

Example 2:

Information: List of main and reference libraries(LIBCHK-120)

Library name	Path	Unit tile	Tile size

```
cb18os120_unit010  /remote/dept5532b/styao/design           unit010    0.560x5.600
--------------------------------------------------------------------------------

                List of tile patterns
--------------------------------------------------------------------------------
 Tile pattern     Unit tile     Location     Orientation          Tile size
 1                   unit         (0,0)    R0|R0_MX             0.560x0.560
 2                   unit         (-0.28,0)R0|R0_MX             0.560x0.560
--------------------------------------------------------------------------------
```

EXAMPLE MESSAGE

```
Information: List of main and reference libraries (LIBCHK-120)
```

LIBCHK-121 (information) List of placement properties

DESCRIPTION

This message is for reporting placement properties for cells in physical library. In this report table, there are seven columns: Cell name, PR boundary, Cell Height, Symmetry, Orientation, Tile pattern and Remarks. PR boundary is represented by its lower left and upper right coordinates. Cell height is relative to the unit tile height, such as 1xH for single height. Cell symmetry includes: rxy - RXYsymmetry xy - XYsymmetry y - Ysymmetry x - Xsymmetry r - Rsymmetry a - Asymmetry Cell orientation includes: R0_MX R0_MY R180 R90_MY R90 R270 R90_MX Number in Tile pattern denotes the serial number in the associated List of tile patterns table. Remarks notes that the PR boundary mismatches the tile pattern. For macros, this table reports cell boundary and height. The unit tile size is reported in the format of width x height.

WHAT NEXT

For standard cells, if mismatches are found between PR boundary and the tile pattern (Mismatch in Remarks column), please use the cmSetMultiHeightProperty command to set tile patterns for multi-height cells.

EXAMPLES

```
                List of tile patterns
--------------------------------------------------------------------------------
 Tile pattern     Unit tile     Location     Orientation          Tile size
 1                   unit         (0,0)      R0|R0_MX             0.660x5.040
--------------------------------------------------------------------------------

         List of placement properties
 --------------------------------------------------------------------------------
---------
 Cell name      PR boundary       Height  Symmetry  Orientation       Tile pattern
 Remarks
 --------------------------------------------------------------------------------
```

```
---------
 TLATNTSCAX1    (0,0)(9.24,5.04)     1xH  xy        R0|R0_MX          1
 NOR2X1         (0,0)(1.98,5.04)     1xH  xy        R90_MY            1Mismatch
-------------------------------------------------------------------------------
--------
```

EXAMPLE MESSAGE

```
Information: List of placement properties (LIBCHK-121)
```

LIBCHK-122 (information) List of routing properties

DESCRIPTION

This message is for reporting routing properties for routing layers in physical library. All routing properties for layers will be reported in this table. In this report table, there are six columns: Layer, Preferred direction, Track direction, Offset, Pitch and Remarks. Remarks column denotes if the routing property on this layer has issues. If no issues are found, you will see OK in this Remarks; otherwise, it will note what issue is found, for example, if the offset is 0.46*pitch, which is neither 0 nor half pitch, offset=0.46pitch will be noted.

WHAT NEXT

If remarks other than OK are noted, such as offset=0.46pitch, please check the issue and correct it. In the case of offset!=0.5*pitch, please reset the offset to be either 0 or half pitch. If blanks are left in Preferred direction, that denotes the preferred routing direction has not been set. Please define the preferred routing direction. If less than three routing layers are listed in this table, it is an error. Please check technology file and if some routing layers are missing, define them in the technology file and reload it.

EXAMPLES

```
         List of routing properties
-------------------------------------------------------------------------
              Preferred      Track
   Layer      direction    direction   Offset    Pitch   Remarks
-------------------------------------------------------------------------
   METAL1         H            H       0.280     0.560   OK
   METAL2         V            V       0.330     0.660   OK
   METAL3                      H       0.280     0.560   OK
   METAL4                      V       0.330     0.660   OK
   METAL5                      H       0.280     0.610   offset=0.46pitch
   METAL6                      V       0.380     0.950   offset=0.40pitch
-------------------------------------------------------------------------
```

EXAMPLE MESSAGE

```
Information:  List of routing properties (LIBCHK-122)
```

LIBCHK-123 (information) List of cell and pin properties

DESCRIPTION

This message is for reporting cell and pin properties for cells in physical library. In this report table, there are six columns: Cell name, Cell type, Pin name, Pin direction, Pin type and Multi PG. If a cell has either multiple power pins or multiple ground pins, multiPG will be noted in the last column. At the end of the table, it also reports the number of cells with multiple P/G pins.

WHAT NEXT

If there is not any power or ground pins for a cell, it is an error. Please check the cell and may need to rerun extract BPV.

EXAMPLES

```
         List of cell and pin properties
-------------------------------------------------------------------------------
-
   Cell name            Cell type     Pin name      Pin direction  Pin type  Multi
PG
-------------------------------------------------------------------------------
-
   XOR2XL               StdCell       Y             Output         signal
                                      VSS                          ground
                                      B             Input          signal
                                      A             Input          signal
                                      VDD                          power
   NAND4BBX1            StdCell       BN            Input          signal
                                      Y             Output         signal
                                      VSS                          ground
                                      C             Input          signal
                                      AN            Input          signal
                                      D             Input          signal
                                      VDD                          power
-------------------------------------------------------------------------------
-
```

EXAMPLE MESSAGE

```
Information:  List of cell and pin properties (LIBCHK-123)
```

LIBCHK-124 (warning) List of pins without optimal routeability

DESCRIPTION

This message is for reporting pins without optimal routeability in physical library. All pins without optimal routeability will be reported in this table. Optimal routeability means pin's on-track accessibility of defined wire tracks. It also reports the total number of pins without optimal on-track routability and lists pin names, directions, layers, and tracks for each cell of this issue. In the track column, an H denotes that the pin is not accessible on a horizontal track, a V denotes the pin is not accessible on a vertical track, and H&V denotes that the pin is not accessible on both horizontal and vertical tracks.

WHAT NEXT

If a pin is reported as not accessible on track, the pin might be routed by off-track wire during detailed routing. If too many pins do not have any on-track routability, adjust the offset values of the wire track (0 or half pitch preferred) and run the the create_lib_track command to reduce the number of pins without optimal accessibility. If routability checking is not successful, the cause may be no unit tile or incorrect technology data, such as illegal fatWire threshold for some layers, illegal vias or cut layers, illegal layer Number, and rules not defined. It is possible that a track intersection is within a via region but there is still no optimal routability. The reason is that in checking the routeability, the tool considers the worst case. That is, a via is already dropped in a neighboring pin's via region, which makes the via spot from the via region of the pin being checked smaller.

EXAMPLES

List of pins without optimal routeability

Cell Name	Pin Name	Layer	Direction	Track
TLATNSRX2	D	METAL1	Input	H&V
SDFFSRHQX2	SE	METAL1	Input	H&V
NOR4BBXL	C	METAL1	Input	H&V
DFFRHQX1	D	METAL1	Input	H&V
AND4X2	C	METAL1	Input	H&V

EXAMPLE MESSAGE

Warning: List of pins without optimal routeability (LIBCHK-124)

LIBCHK-125 (warning) List of cells with DRC violation

DESCRIPTION

This message is for reporting cells with DRC violation in physical libraries. All cells with DRC violation will be reported in this table. It checks design rules such as wire minWidth, minEdgeLength, minEnclosedArea, minSpacing, cutWidth, cutSpacing, and minEnclosure. In this report table, there are three columns: Cell Name, Cell type and Error cell. Error cell contains detailed information for DRC violation of the FRAM view cell.

WHAT NEXT

Check the error cells for details of DRC violations. If a cell has DRC violation, it may not be used in the design without correction.

EXAMPLES

List of cells with DRC violation

Cell name	Cell type	Error cell
ONEPIN	Standard	ONEPIN.err

EXAMPLE MESSAGE

Warning: List of cells with DRC violation (LIBCHK-125)

LIBCHK-126 (warning) List of cells with metal density error

DESCRIPTION

This message is for reporting cells with metal density error in physical library. All cells with metal density error will be reported in this table. It checks macro metal density data for the cells, i.e. it checks if a cell has at least one of the following errors: (1) Metal density data in CEL view and FRAM view are inconsistent (2) Metal density windows do not cover the entire area on the layer In this report table, there are three columns: Cell Name, Inconsistency and the layer on which the density windows do not cover the entire area. Y denotes Yes or Inconsistency exists and N denotes No consistency.

WHAT NEXT

If the density windows do not cover the entire area, you may need to add metal fill or smooth metal wire density. If metal density data in CEL view and FRAM view are inconsistent, please check FRAM vs. CEL view.

EXAMPLES

List of cells with metal density error

Cell name	Inconsistency	Not cover entire area
ADDFX1MTR	Y	M4
OA21X1MTR	N	M1
		M2

EXAMPLE MESSAGE

Warning: List of cells with metal density error (LIBCHK-126)

LIBCHK-210 (information) List of cells missing in logic library

DESCRIPTION

This message is for reporting missing cells in logic library during logic vs. physical library checking. All the physical cells except physical only cells that are missing in logic library will be reported in this table. In this report table, there are three columns: Cell name, Cell type and Physical library. Cell type includes Core, Pad, InputPad, OutputPad, PowerPad, SpacerPad, and Unknown.

WHAT NEXT

If some cells are found missing in specified logic library (.db), please check if you have not specified all the db files since logic cells may exist in different db files while the physical cells exist in one Milkyway library.

EXAMPLES

List of cells missing in logic library

Cell name	Cell type	Physical library
AND2	Core	phys_lib
NOR1	Core	phys_lib

EXAMPLE MESSAGE

Information: List of cells missing in logic library (LIBCHK-210)

LIBCHK-211 (warning) List of cells missing in physical library

DESCRIPTION

This message is for reporting missing cells in physical library during logic vs. physical library checking. All the logic cells that are missing in physical library will be reported in this table. In this report table, there are three columns: Cell name, Cell type and Logic library. The cell type includes pad_cell, non pad_cell and unknown. If no missing cells, no table will be printed out, but Number of cells missing in logic library: 0 (out of total) will be printed out.

WHAT NEXT

If some cells are found missing in specified physical library (Milkyway library), please check if you have complete Milkyway library specified since physical cells may exist in different Milkyway library directories. If the cells are used in the design, the physical cells have to exist in the physical library that you are using. If the cells are not expected to be part of the physical library, then the incoming netlist must not have any of the missing cells. For example, by setting the dont_use attribute during synthesis.

EXAMPLES

```
 Number of cells missing in physical library:2 (out of 498)
   List of cells missing in physical library
-------------------------------------------------------------------------
Cell name                  Cell type             Logic library
-------------------------------------------------------------------------
gaard21                    non pad_cell          memory.lib
gaard22                    non pad_cell          memory.lib
-------------------------------------------------------------------------
```

EXAMPLE MESSAGE

Warning: List of cells missing in physical library (LIBCHK-211)

LIBCHK-212 (warning) List of pins missing in %s library

DESCRIPTION

This message is for reporting missing pins in logic (or physical) cells during logic vs. physical library checking. All the physical(or logic) pins that are missing in logic (or physical) cells will be reported in this table. In this report table, there are four columns: Physical(Logic) library, Cell name, Pin name and Pin direction It also checks pg_pin’s in logic library vs. PG pins in physical library if there are pg_pin’s in the logic library, and reports them in the same table.

WHAT NEXT

If some signal pins are found missing in logic cells, it is a real issue and therefore an Error message LIBCHK-101 will occur to direct you to correct the cells that are missing these pins in the logic library. If pg_pins are missing in the logic library, it indicates that the logic library is not pg_pin based, and for UPF flow you need to use add_pg_pin_to_db utility to convert it into pg_pin based db.

EXAMPLES

```
      List of pins missing in logic library
-------------------------------------------------------------------------
Physical library  Cell name  Pin name    Pin direction
-------------------------------------------------------------------------
NLC13IOplLib_3v  pnl_go     A        Output
-------------------------------------------------------------------------
```

EXAMPLE MESSAGE

Warning: List of pins missing in logic library (LIBCHK-212)

LIBCHK-213 (error) List of pins mismatched in logic and physical libraries

DESCRIPTION

This message is for reporting pins mismatched in either direction or pin type between the logic and physical cells during logic vs. physical library checking. All the mismatched pins will be reported in this table. In this report table, at the header of this table, the logic and physical library full path file names are listed followed by the table contents with four columns: Cell name, Pin name, Pin direction and Pin type. In Pin direction and Pin type columns, it lists values for both logic and physical libraries.

WHAT NEXT

If some pins are found mismatched in either pin direction or pin type between logic and physical cells, it is a real issue and you need to correct the cells with this issue in either the logic or physical library or both.

EXAMPLES

```
List of pins mismatched in logic and physical libraries
Logic library:    NLC13IOplLib_3v_fast132Vm40C
Physical library: /remote/fae99/smoot/TO_XIREN/NLC13IOplLib_3v
-------------------------------------------------------------------------
                                        Pin direction       Pin type
Cell name                  Pin name    Logic   Physical    Logic   Physical
```

```
-------------------------------------------------------------------------
pnl_go                        VSSO        output  Output      signal  ground
                              GND         input   Input       signal  ground
                              VDDP        input   Input       signal  power
-------------------------------------------------------------------------
```

EXAMPLE MESSAGE

```
Error: List of pins mismatched in logic and physical libraries (LIBCHK-213)
```

LIBCHK-213w (warning) List of pins mismatched in logic and physical libraries

DESCRIPTION

This message is for reporting pins mismatched in either direction or pin type between the logic and physical cells during logic vs. physical library checking. All the mismatched pins will be reported in this table. In this report table, at the header of this table, the logic and physical library full path file names are listed followed by the table contents with four columns: Cell name, Pin name, Pin direction and Pin type. In Pin direction and Pin type columns, it lists values for both logic and physical libraries.

WHAT NEXT

If some pins are found mismatched in pin type between logic and physical cells, i.e. pg_pins in physical library modelled as signal pins in logical library, add_pg_pin_to_db/lib utility may correct it. Otherwise, if some pins are found mismatched in either pin direction or pin type between logic and physical cells, it is a real issue and you need to correct the cells with this issue in either the logic or physical library or both.

EXAMPLES

```
List of pins mismatched in logic and physical libraries
Logic library:    NLC13IOplLib_3v_fast132Vm40C
Physical library: /remote/fae99/smoot/TO_XIREN/NLC13IOplLib_3v
-------------------------------------------------------------------------
                                        Pin direction       Pin type
Cell name                     Pin name  Logic   Physical    Logic   Physical
-------------------------------------------------------------------------
pnl_go                        VSSO      output  Output      signal  ground
                              GND       input   Input       signal  ground
                              VDDP      input   Input       signal  power
-------------------------------------------------------------------------
```

EXAMPLE MESSAGE

```
Warning: List of pins mismatched in logic and physical libraries (LIBCHK-213w)
```

LIBCHK-214 (information) List of bus naming styles

DESCRIPTION

This message is for reporting bus delimiters in logic and physical libraries. There are three columns in this report table: Library name, Library type and Bus naming style where Library type is either physical library or logic library. If there is no bus delimiter in the library, the field is blank in the report. To report bus naming styles, please set -bus_delimiter to set_check_library_options command. it is often true that logic libraries do not specify the bus delimiter.

WHAT NEXT

This is information only. No further action is needed.

EXAMPLES

```
    List of bus naming styles
-------------------------------------------------------------------
Library name                 Library type        Bus naming style
-------------------------------------------------------------------
tsmc18_xx                      Physical library    _<%d>
memory.lib                   Logic library
-------------------------------------------------------------------
```

EXAMPLE MESSAGE

```
Information: List of bus naming styles (LIBCHK-214)
```

LIBCHK-215 (warning) List of cells with cell_footprint attribute

DESCRIPTION

This message is to check that the cell PR boundary or Cell boundary for Macro in the physical library is consistent among a class of cells with the same cell_footprint attribute specified in the logic library. This option reports cell names and their PR boundaries grouped by cell_footprint string.

WHAT NEXT

If the cells are used in the design, please check their PR boundaries or cell

boundaries for inconsistency. For example, if the PR boundaries of the cells with the same cell_footprint are different, you can not use them during optimization by swapping these cells.

EXAMPLES

```
  List of cells with cell_footprint attribute
-------------------------------------------------------------------
Footprint  Logic library name  Cell name           PR boundary
-------------------------------------------------------------------
add42      slow                CMPR42X1            (0,0)(22.44,5.04)
           slow                CMPR42X2            (0,0)(26.4,5.04)
addf       slow                ADDFX1              (0,0)(13.86,5.04)
-------------------------------------------------------------------
```

EXAMPLE MESSAGE

```
Warning: List of cells with cell_footprint attribute (LIBCHK-215)
```

LIBCHK-216 (warning) List of cells with inconsistent area

DESCRIPTION

This message is to check the area attribute of cells in the logic library versus the actual area by cell PR boundary in the physical library. For comparison, the ratio of a stdCell PRBoundary in the rectangle (or Macro CellBoundary in the polygon) in the FRAM view to the cell area in the .db is used. If the ratio is the same for all the cells in the library, the cell areas are considered to be consistent. Otherwise, if the ratio for a cell deviates from the normal or average ratio for this library by a margin of 5%, it is counted as an inconsistent area. and will be included in the table. The average area ratio is calculated by first filtering out cells with the max and min area ratios and then dividing the total area ratios by the number of cells. There is no area check for pad cells. A pad cell is a special cell at the chip boundary with the pad_cell attribute in a logic cell. Pad cells are not checked because they are not used as internal gates and always have an area of 0. To check cell area, please set -cell_area to set_check_library_options command.

WHAT NEXT

If the cell areas are inconsistent between logic and physical libraries, it will affect timing and placement accurary. The bigger the area deviation, the worse the accuracy and correlation. If the area value is 0 or no area attribute in logic cells, it is more serious and an Error LIBCHK-101 will occur. In this case, you need to correct logic library by adding valid area values to the cells.

EXAMPLES

```
Average cell area ratio physical/logic in the library:0.9978
Number of cells with inconsistent area:9

     List of cells with inconsistent area
-------------------------------------------------------------------
                                                  Area ratio
Logic library name          Cell name             Phys/logic
-------------------------------------------------------------------
slow                        AFCSHCONX4            0.7966
slow                        AFCSHCONX2            0.8431
slow                        AFHCONX2              0.9167
slow                        AFHCINX4              0
-------------------------------------------------------------------
```

EXAMPLE MESSAGE

```
Warning: List of cells with inconsistent area (LIBCHK-216)
```

LIBCHK-220 (information) Logic library is INCONSISTENT with physical library

DESCRIPTION

This message is a concluding statement after cross checking is done. When any inconsistency, for example, missing cells and mismatched pins, is found during cross checking, this message will occur.

WHAT NEXT

This is for your information. You need to go back to the check report to see inconsistent results and resolve them as directed by related man pages (LIBCHK).

EXAMPLES

EXAMPLE MESSAGE

```
Information: Logic library is INCONSISTENT with physical library (LIBCHK-220)
```

LIBCHK-300 (warning) List of inconsistent library group data

DESCRIPTION

This message is for reporting inconsistent data in logic libraries during logic vs. logic library checking. In the associated report table, it reports inconsistent values of the attributes at the library level. The attributes include. a)library version b)library type (pg_pin based or non-pg_pin based) c)units of timing, power,capacitance, etc. d)trip points e)base curve_x

WHAT NEXT

If some inconsistencies are reported at the library level, please check the libraries and correct them. Some attributes should be consistent cross the libraries. If the libraries are used for timing scaing, trip points should be consistent, and if they are used for UPF or MV flow, the libraries should be pg_pin based.

EXAMPLES

List of inconsistent library group data

Library name	SR60_W_SVT_UHD.db	SR60_S_SVT_UHD.db
Voltage unit	1V	1mV
base_curves/curve_x	"0.2, 0.5, 0.8"	"0.2, 0.5, 0.9"

EXAMPLE MESSAGE

Warning: List of inconsistent library group data (LIBCHK-300)

LIBCHK-301 (information) List of operating conditions

DESCRIPTION

This message is for reporting operating conditions of the logic libraries. In this report table, nom_voltage, nom_temperature, nom_process and default_operating_conditions of each lib are reported. If default_operating_condition is not specified, Library Compiler will add a default name nom_pvt by creating one from nominal PVTs.

WHAT NEXT

For library scaling, the operating conditions in the same scaling library group should be different in nominal voltage, temperature and/or process. For MCMM and MV/UPF, the nominal voltages should be different under different operating conditions.

For all others, this is information only. No further action is required. For voltage scaling, it is recommended that the voltages should be no more than 20% apart for good accuracy

EXAMPLES

List of operating conditions

Library name	SR60_W_SVT_UHD.db	SR60_S_SVT_UHD.db
nom P/V/T	3.0/1.0/105.0	1.0/1.4/105.0
default_opcon	"W_105_0.99"	"S_105_1.21"

EXAMPLE MESSAGE

Information: List of operating conditions (LIBCHK-301)

LIBCHK-302 (information) Voltages for library scaling are more than 20%% apart.

DESCRIPTION

This message is for voltage scaling, the voltages should be no more than 20% apart for good accuracy.

WHAT NEXT

This is information only. However, for better accuracy, it is recommended that the voltages should be no more than 20% apart for voltage scaling.

EXAMPLES

EXAMPLE MESSAGE

Information: Voltages for library scaling are more than 20% apart. (LIBCHK-302)

LIBCHK-310 (information) List of cells missing in logic libraries

DESCRIPTION

This message is for reporting cells missing in one or more logic libraries during logic vs. logic library checking. All the logic cells that are missing will be reported in this table.

WHAT NEXT

If cells are found missing in one or more of the libraries, please check why these are existing in onle library but missing in the other. If such cells are used in design, these cells have to be in all the libraries.

EXAMPLES

```
          List of cells missing in logic libraries
-------------------------------------------------------------------------
Cell name           SR60_W_SVT_UHD.dbSR60_S_SVT_UHD.db
-------------------------------------------------------------------------
nsdffnqs_f4_svt     missing                   existing
-------------------------------------------------------------------------
```

EXAMPLE MESSAGE

Warning: List of cells missing in logic libraries (LIBCHK-310)

LIBCHK-311 (information) List of cells with mismatched or missing attributes in logic libraries

DESCRIPTION

This message is for reporting mismatched cell data in logic libraries during logic vs. logic library checking. Mismatched cells are those that have inconsistent attribute values at the cell level.

WHAT NEXT

Mismatched cells will cause issues if used in design. The same name cells existing in different libraries should have the same values for attributes such as function, dont_use and dont_touch, and same attributes should exist in all the libraries.

EXAMPLES

```
         List of cells with mismatched or missing attributes in logic libraries
-------------------------------------------------------------------------------
                                  Attribute value
Cell name           Attribute       SR60_W_SVT_UHD.dbSR60_S_SVT_UHD.db
-------------------------------------------------------------------------------
tieofflx_svt        function    "A * B"            "A * B + c"
std_cell_inv        pin_order       "A_Y"              "VDD_A_Y"
-------------------------------------------------------------------------------
```

EXAMPLE MESSAGE

Warning: List of cells mismatched in logic libraries (LIBCHK-311)

LIBCHK-312 (information) List of cell classification

DESCRIPTION

This message is for reporting cell classification of logic libraries. In this report table, numbers of total cells, inverters, buffers, level shifters, isolation cells, retention cells, switch cells, and always on cells in each library are reported.

WHAT NEXT

For UPF flow, special cells such as level shifters should exist in the library. in general, the library should have inverters. For all other cases, this is information only. No further action is required.

EXAMPLES

List of cell classification

Library name	SR60_W_SVT_UHD.db	SR60_S_SVT_UHD.db
Total number	3	3
Inverter	2	1
Buffer	0	0
Level shifter	0	0
Isolation cell	0	0
Retention cell	0	0
Switch cell	0	0
Always on cell	0	0

EXAMPLE MESSAGE

Information: List of cell classification (LIBCHK-312)

LIBCHK-320 (warning) List of pins missing in logic libraries

DESCRIPTION

This message is for reporting missing signal pins and pg_pins in logic cells during logic vs. logic library checking. All the logic pins that are missing in logic cells will be reported in this table. In this report table, the following columns are listed: Cell name, Pin name and each logic library names.

WHAT NEXT

If some signal pins are found missing in logic cells, it is a real issue and therefore an Error message LIBCHK-101 will occur to direct you to correct the cells

that are missing these pins in the logic library. If pg_pins are missing in the logic library, it indicates that the logic library is not pg_pin based, and you need to use add_pg_pin_to_db utility to convert it into pg_pin based db.

EXAMPLES

List of pins missing in logic libraries

Cell name	Pin name	SR60_W_SVT_UHD.db	SR60_S_SVT_UHD.db
tieofflx_svt__VSS	missing	existing	
tieofflx_svt__VDD	missing	existing	

EXAMPLE MESSAGE

Warning: List of pins missing in logic libraries (LIBCHK-320)

LIBCHK-321 (information) List of pins with mismatched or missing attributes in logic libraries

DESCRIPTION

This information message occurs when the tool finds mismatched pins in the logic cells during logic versus logic library checking. Mismatched pins are those that have inconsistent pin attributes such as pin direction, function, related_power_pin, and so forth.

The report table has the following columns:

- Cell name
- Pin name
- Attribute/Group name
- Attribute value of each of the logic libraries

WHAT NEXT

This is only an information message. No action is required.

However, mismatched pins will cause issues if the cells are used in the design. The same name pins should exist in the same name cells in different libraries with consistent values for attributes such as function, direction, related_power_pin, and related_ground_pin, and the same attributes should exist for the same pins in the same name cells. Characterization values such as capacitance can be different.

EXAMPLES

The following is an example of a mismatched pins list:

List of pins with mismatched or missing attributes in logic libraries

Cell name	Pin name	Attribute /Group	Attribute value SR60_W_SVT_UHD	SR60_S_SVT_UHD
tieofflx_svt	lo	pin_number	0	1
std_cell_inv	Y	related_ground_pin	missing	VSS

SEE ALSO

check_library(2)
set_check_library_options(2)

LIBCHK-322 (information) List of pg_pins with mismatched or missing attributes in logic libraries

DESCRIPTION

This information message occurs when the tool finds pg_ pins with mismatched or missing attributes in the logic cells during logic versus logic library checking. Mismatched pg_pins are those that have inconsistent pg_pin attributes.

The report table has the following columns:

- Cell name
- pg_pin name
- Attribute/Group name
- Attribute value of each of the logic libraries

WHAT NEXT

Mismatched pg_pins will cause issues if the cells are used in the design. The same name pg_pins should exist in the same name cells in different libraries with consistent values for attributes such as direction, pg_function and switch_function. The same attributes should exist for the same pg_pins in the same name cells.

EXAMPLES

The following is an example of mismatched pg_pins list:

```
      List of pg_pins with mismatched or missing attributes in logic libraries
-------------------------------------------------------------------------------
                            Attribute                Attribute value
Cell name       pg_pin name  /Group               non_pg_lib      pg_lib
-------------------------------------------------------------------------------
LVLLHCD         VDD         std_cell_main_rail     missing         true
FOOTER          VSS         pg_function            missing         "TVSS"
-------------------------------------------------------------------------------
```

SEE ALSO

check_library(2)
set_check_library_options(2)

LIBCHK-323 (warning) List of pg_pins missing in logic libraries

DESCRIPTION

This message is for reporting missing pg_pins in logic cells during logic vs. logic library checking. All the logic pg_pins that are missing in logic cells will be reported in this table. In this report table, the following columns are listed: Cell name, Pin name and each logic library names.

WHAT NEXT

If pg_pins are missing in the logic library, it indicates that the logic library is not pg_pin based, and you need to use add_pg_pin_to_db utility to convert it into pg_pin based db.

EXAMPLES

```
      List of pg_pins missing in logic libraries
-------------------------------------------------------------------------------
Cell name Pin name SR60_W_SVT_UHD.db         SR60_S_SVT_UHD.db
-------------------------------------------------------------------------------
tieofflx_svt__VSS    missing                   existing
tieofflx_svt__VDD    missing                   existing
-------------------------------------------------------------------------------
```

EXAMPLE MESSAGE

Warning: List of pg_pins missing in logic libraries (LIBCHK-323)

LIBCHK-330 (information) List of timing arcs missing in libraries

DESCRIPTION

This message is for reporting timing arcs missing in the logic libraries.

WHAT NEXT

For timing scaling, timing arc information should exist with consistent timing data in each library. For other cases, this is information only. No further action is required.

EXAMPLES

```
            List of timing arcs missing in libraries
-------------------------------------------------------------------------------
Cell name     Arc             SR60_W_SVT_UHD.db     SR60_S_SVT_UHD.db
-------------------------------------------------------------------------------
tbufl_f7_svt  gz_y            existing               missing
-------------------------------------------------------------------------------
```

EXAMPLE MESSAGE

Information: List of timing arcs missing in libraries (LIBCHK-330)

LIBCHK-331 (warning) List of timing arcs mismatched in logic libraries

DESCRIPTION

This message is for reporting mismatched arcs in logic libraries during logic vs. logic library checking. It also includes inconsistent output load indices. This report table has the following columns: Cell name, Arc name, Attribute/Group name and attrbute values of each logic libraries.

WHAT NEXT

For timing scaling and timing/delay calculations, consistent timing data should exist in the libraries for each timing arc.

EXAMPLES

```
      List of timing arcs mismatched in logic libraries
-------------------------------------------------------------------------------
Cell name           Arc      Attribute   Attribute value
                              /Group         SR60_W_SVT_UHD.dbSR60_S_SVT_UHD.db
```

```
--------------------------------------------------------------------------------
tbufl_f7_svt        gz_y     timing_sense    positive_unate     non_unate
AND2                A_Z      output_current_rise/total_output_net_capacitance
     5            4
--------------------------------------------------------------------------------
```

EXAMPLE MESSAGE

```
Warning: List of timing arcs mismatched in logic libraries (LIBCHK-331)
```

LIBCHK-332 (warning) Library '%s' is missing CCS %s models.

DESCRIPTION

This warning message occurs during logic versus logic library checking, when no driver or receiver model exists in the library.

WHAT NEXT

This is only a warning message. No action is required.

However, receiver models and driver models (compressed or original format) must exist in the libraries for timing scaling. For all other cases, this is information only.

SEE ALSO

```
check_library(2)
set_check_library_options(2)
```

LIBCHK-340 (warning) List of inconsistent CCS noise models

DESCRIPTION

This message is for reporting inconsistent CCS noise models in logic libraries. It reports: a)inconsistent input_voltage and output_voltage indices for CCS noise models b)inconsistent conditional (when) pin models (when order). c)inconsistent CCS noise models for all pins and arcs. This report table includes the following columns: Cell name, Pin name, Group name, Attrbute name and attribute value of each library.

WHAT NEXT

For CCS noise scaling, consistent noise models are required. For other cases, it is for information only.

EXAMPLES

```
      List of inconsistent CCS noise models
-------------------------------------------------------------------------------
                                      Attribute           Attribute value
Cell name Pin name  Group name        /variable    SR60_W_SVT_UHD   SR60_S_SVT_UHD
-------------------------------------------------------------------------------
inv0d0    ZN        ccsn_first_stage  input_net_transition
                                            "175.0"          "980.0"
inv0d0    ZN        ccsn_last_stage   total_output_net_capacitance
                                            "0.0"            "0.0"
-------------------------------------------------------------------------------
```

EXAMPLE MESSAGE

```
Warning: List of inconsistent CCS noise models (LIBCHK-340)
```

LIBCHK-341 (warning) List of inconsistent power models.

DESCRIPTION

This warning message occurs when there are inconsistent power models in the logic library. It reports the following inconsistencies:

- Inconsistent dynamic_current groups for each cell
- Inconsistent intrinsic_parasitic tables for each cell
- Inconsistent leakage_current groups for each cell
- Inconsistent power_cell_type attribute for each cell
- Inconsistent internal_power tables for each pin or cell
- Inconsistent leakage_power tables for each cell

The report table includes the following columns:

   Cell name
   Group name
   Attribute name
   Attribute value of all logic libraries

WHAT NEXT

This is only a warning message. No action is required.

However, consistent power models are required for power scaling. For other cases,

the report is for information only.

EXAMPLES

The following is an example of a list of inconsistent power models:

```
        List of inconsistent power models
   ------------------------------------------------------------------------------
                                                          Attribute value
   Cell name  Group             Attribute       SR60_W_SVT_UHD     SR60_S_SVT_UHD
   ------------------------------------------------------------------------------
   ap001_svt  leakage_power     value           0.000000          2.686740
   an02d1     dynamic_current   related_inputs  "A1"              "A0"
   ------------------------------------------------------------------------------
```

SEE ALSO

check_library(2)
set_check_library_options(2)

LIBCHK-350 (warning) List of inconsistent data between different timing models

DESCRIPTION

This message is for validating library data between CCS and NLDM models. It reports: a) inconsistent output load indices between CCS and NLDM models, and inconsistent load indices for CCS drive/receiver b)inconsistent NLDM delay and slew indices and values with a default or user specified tolerance. c)inconsistent delays between NLDM and CCS timing with a user specified tolerance for both compact CCS and expanded CCS d)inconsistent data between two CCS driver model current waveforms including compact CCS with expanded CCS data with a tolerance e)inconsistent between CCS power data and NLPM data (not in 2008.09 releases) In this report table, including following columns: Cell name, Croup name, Attrbute name and attribute value of all liogic libraries.

WHAT NEXT

If the difference is significantly larger between the models, please rerun the simulation to correct the libraries.

EXAMPLES

```
Warning: List of inconsistent data between different models (LIBCHK-350)
Cell name:  dtmuxi3_d10m
index_1:    total_output_net_capacitance
index_2:    input_net_transition
```

```
------------------------------------------------------------------------------------
-----------------------
                                                                                gold_timing_in
dex_lib     Error
pin/related_pin timing_type   when  Group/
Attribute (index_1,index_2) (NLDM)    (CCS)     Absolute Relative
------------------------------------------------------------------------------------
-----------------------
y/s2            combinational       cell_rise/values
                                                    (1.83,0.5)      18.016    18.
2206   0.20456  1.1%
                                                    (1.83,4)        19.5332   19.
8679   0.33468  1.7%
                                                    (1.83,12)       23.9233   28.
2093   4.286    18%
------------------------------------------------------------------------------------
-----------------------
```

EXAMPLE MESSAGE

```
Warning: List of inconsistent data between different models (LIBCHK-350)
```

LIBCHK-351 (information) List of inconsistent constructs and values

DESCRIPTION

```
This message is for reporting inconsistent liberty syntax constructs and/or values
of the two logic libraries
```

WHAT NEXT

```
This is information only. No further action is required.
```

EXAMPLES

EXAMPLE MESSAGE

```
Information: List of inconsistent constructs and values (LIBCHK-351)
```

LIBCHK-352 (information) Table of variation-aware model

analysis

DESCRIPTION

This table lists variation aware analysis results for driver, receiver and constraint models. For a set of va_values, there are normally three values: nominal, -Sigma and +Sigma. From the three values for each pair of indices, a linear model is used to find: a)monotonicity (trend) including -delays increase as slew and load increase. - delays increase/decrease as va_parameters increase. b)significance of each va_parameters

As trial and error procedure, the following statistics will be used in the study on the VA models. iThe linear model is used to roughly measure how significant each va_parameters affects on delay. 1)If slope ~= 0, va_parameter is insignificant (not sensitive) 2)If slope > 0, monotonously increasing 3)If slope < 0, monotonously decreasing 4)Alternating slopes may indicate issues 5)Trend: If Dnom > both D+/-sigma, or If Dnom < both D+/-sigma, not monotonous, where D is Delay. 6)coefficient of correlation to measure how closely the va_parameters are related to delays. Std error is used to measure how much va_parameter and delay points deviate from the linear model.

This report table includes the following columns: pin/related_pin, timing_type, when,¬†Group,¬†va_values,¬†(index_1,2),¬†nomimal, -Sigma, +Sigma,¬†Slope, Std error and Trend In Trend column, /is monotonously increasing, is monotonously decreasing, ^ is non-monotonous up, V is non-monotonous down and - is flat.

WHAT NEXT

If the difference is significantly larger between the models, please rerun the simulation to correct the libraries.

EXAMPLES

```
Information: Table of variation-aware model analysis (LIBCHK-352)
Cell name:¬†¬†   Sdffcqs
va_parameters:   (var1, var2)
nominal_va_values: (10,20)
index_1:       input_net_transition
index_2:       output_net_capacitance
-------------------------------------------------------------------------------
--------------------------
                                                                  values
pin/related_pin timing_type  when ¬†Group¬†¬†¬†va_values ¬†(index_1,2)¬†nomimal -
Sigma +Sigma¬† Slope Std error Trend
-------------------------------------------------------------------------------
--------------------------
sq/clk         rising_edge  scan¬†¬†compact_ccs_rise¬†¬†¬†
                                 var1+/-
0.4 (1.11,0.92)¬†23.02¬†¬†¬†22.42 ¬†23.82 ¬† 0.3¬†¬†¬†0.86%¬†¬†   /¬†¬†¬†
¬†¬†¬†
```

```
--------------------------
```

EXAMPLE MESSAGE

```
Information: Table of variation-aware model analysis (LIBCHK-352)
```

LIBCHK-353 (information) Report of the statistical analysis results of characterization models.

DESCRIPTION

This information message reports the statistical analysis results of characterizations between CCS and NLDM models or between the same types of models in two libraries, using the golden NLDM or first library as the base.

The columns in the table include the following:

- Group type: Delay, Slew, Constraint, Receiver capacitance
- Mean of differences: Absolute, Relative
- Standard deviation: Absolute, Relative
- Max outlier: the maximum value of the deviations
- Number of grid points: Passed, Failed

WHAT NEXT

If the mean is far from 0, the two models or libraries have significant differences. If the standard deviation is significantly large, the differences of these two are dispersed. In any case, small numbers of mean and deviation, close to 0, should be expected if the characterizations are generated under the same operating conditions.

EXAMPLES

The following is an example report of the statistical analysis results of characterization models:

```
Information: List of statistical analysis (LIBCHK-353)
-------------------------------------------------------------------------------
               Mean of differences    Std deviation                Number of grids
```

```
Group type      Absolute Relative   Absolute Relative   Max outlier  Pass    Fail
-------------------------------------------------------------------------------
Delay           0.0001   0.00%      0.0016   0.00%      0.0309       892     4
Slew            -0.0003  -0.00%     0.0044   0.01%      -0.0773      856     40
Constraint      65.6896  -69.56%    463.0871 3034.77%   3905.8228    878     42
Receiver cap    0.0000   0.00%      0.0000   0.00%      0.0000       1072    0
-------------------------------------------------------------------------------
```

SEE ALSO

check_library(2)
set_check_library_options(2)

LIBCHK-354 (information) Table of characterization timing table trend analysis.

DESCRIPTION

This information message presents a table of single characterization timing table trend analysis results for delay, slew, driver, receiver and constraint models. The trends include the following:

```
/      monotonously increasing
\<HardSpace     monotonously decreasing
^      non-monotonous up
V      non-monotonous down
-      flat
M      Multiple peaks
W      Multiple troughs
N      2 peaks with 2nd not turning low
```

WHAT NEXT

This is an information message only. No action is required.

However, if the trend indicates that the values do not increase as slew/load indices, please check that the characterizations have been done correctly.

EXAMPLES

The following is an example table:

```
Table of characterization timing table trend analysis (LIBCHK-354)
index_1:    related_pin_transition
index_2:    output_net_capacitance
-------------------------------------------------------------------------------
-----------------
```

```
Cell name   pin/
related_pin timing_type    when    Group       index_1,index_2   values         Tre
nd
-------------------------------------------------------------------------------
-----------------
sdffcqs     q/clk           min_pulse_width        fall_constraint
                                                              1.11,*            "6
6.528,..."   V
sdffcqs     q/
clrz          clear                  cell_fall   1.11,*            "50.8109,..."  /
-------------------------------------------------------------------------------
-----------------
```

LIBCHK-360 (information) Logic library inconsistencies found for MCMM.

DESCRIPTION

This information message occurs when any inconsistency in MCMM is found during cross checking the libraries.

WHAT NEXT

This is an information only message. No action is required.

However, you are advised to go back to the check report to see inconsistent results and resolve them as directed by the associated LIBCHK man pages.

If you see "inconsistencies found" in the summary report, go to the related tables for details in

- LIBCHK-300
- LIBCHK-301
- LIBCHK-310
- LIBCHK-311
- LIBCHK-312
- LIBCHK-320
- LIBCHK-321
- LIBCHK-330
- LIBCHK-331
- LIBCHK-340

Any of the related LIBCHK man pages will lead to the conclusion of inconsistencies found.

SEE ALSO

check_library(2)

set_check_library_options(2)
LIBCHK-300(n)
LIBCHK-301(n)
LIBCHK-310(n)
LIBCHK-311(n)
LIBCHK-312(n)
LIBCHK-320(n)
LIBCHK-321(n)
LIBCHK-330(n)
LIBCHK-331(n)
LIBCHK-340(n)

LIBCHK-361 (information) Logic library inconsistencies found for UPF.

DESCRIPTION

This information message occurs after the cross checking of the libraries is completed. When any inconsistency in the UPF flow is found during cross checking, this message appears.

WHAT NEXT

This is an information message only. No action is required.

However, you are advised to go back to the above check report to see inconsistent results and resolve them as directed by the associated LIBCHK man pages.

If you see "inconsistencies found" in the summary report, go back to the related tables for details in

LIBCHK-300
LIBCHK-301
LIBCHK-302
LIBCHK-310
LIBCHK-311
LIBCHK-312
LIBCHK-320
LIBCHK-321
LIBCHK-330
LIBCHK-331
LIBCHK-332
LIBCHK-340

Any of the related LIBCHK man pages will lead to the conclusion of inconsistencies found.

SEE ALSO

check_library(2)
set_check_library_options(2)
LIBCHK-300(n)
LIBCHK-301(n)
LIBCHK-310(n)
LIBCHK-311(n)
LIBCHK-312(n)
LIBCHK-320(n)
LIBCHK-321(n)
LIBCHK-330(n)
LIBCHK-331(n)
LIBCHK-332(n)
LIBCHK-340(n)

LIBCHK-362 (information) Logic library inconsistencies found for %s scaling.

DESCRIPTION

This information message occurs after the cross checking of the libraries is completed. When the tool finds any inconsistencies, such as CCS timing scaling, CCS noise scaling, or power scaling during cross checking, this message appears.

WHAT NEXT

This is an information only message. No action is required.

However, you are advised to go back to the above check report to see the inconsistent results and resolve them as directed by the associated LIBCHK man pages.

When you see "inconsistencies found for CCS timing scaling" in the summary report, go back to the related tables for details in

LIBCHK-300
LIBCHK-301
LIBCHK-302
LIBCHK-310
LIBCHK-311
LIBCHK-320
LIBCHK-321
LIBCHK-330
LIBCHK-331
LIBCHK-332
LIBCHK-340
LIBCHK-350

Any of the related LIBCHK man pages will lead to this conclusion.

When you see "inconsistencies found for CCS noise scaling" in the summary report, go back to the related tables in

LIBCHK-300
LIBCHK-301
LIBCHK-302
LIBCHK-310
LIBCHK-311
LIBCHK-320
LIBCHK-321
LIBCHK-330
LIBCHK-331
LIBCHK-340

Any of the related man pages (LIBCHK) will lead to this conclusion.

When you see "inconsistencies found for power scaling" in the summary report, go back to the related tables in

LIBCHK-300
LIBCHK-301
LIBCHK-302
LIBCHK-310
LIBCHK-311
LIBCHK-320
LIBCHK-321
LIBCHK-330
LIBCHK-331
LIBCHK-341

Any of the related LIBCHK man pages will lead to this conclusion.

SEE ALSO

check_library(2)
set_check_library_options(2)
LIBCHK-300(n)
LIBCHK-301(n)
LIBCHK-302(n)
LIBCHK-310(n)
LIBCHK-311(n)
LIBCHK-320(n)
LIBCHK-321(n)
LIBCHK-330(n)
LIBCHK-331(n)
LIBCHK-332(n)
LIBCHK-340(n)
LIBCHK-350(n)

LIBCHK-363 (information) Logic library inconsistencies found for %s comparison.

DESCRIPTION

This information message occurs after cross checking between the two libraries is completed. When any the tool finds inconsistencies in the Liberty syntax construct comparison or value comparison during cross checking, this message will appears. In construct comparison, the missing or existing data is reported. In value comparison, the characterization values are reported.

WHAT NEXT

This is an information only message. No action is required.

However, you are advised to go back to the above check report to see inconsistent results and resolve them as directed by the associated LIBCHK man pages.

When you see "inconsistencies found" for the construct or value comparison in the summary report, go back to the related tables for details in

LIBCHK-300
LIBCHK-301
LIBCHK-310
LIBCHK-311
LIBCHK-312
LIBCHK-320
LIBCHK-321
LIBCHK-330
LIBCHK-331
LIBCHK-340
LIBCHK-341

Any of the related LIBCHK man pages will lead to this conclusion.

SEE ALSO

check_library(2)
set_check_library_options(2)
LIBCHK-300(n)
LIBCHK-301(n)
LIBCHK-310(n)
LIBCHK-311(n)
LIBCHK-312(n)
LIBCHK-320(n)
LIBCHK-321(n)
LIBCHK-330(n)
LIBCHK-331(n)
LIBCHK-340(n)
LIBCHK-341(n)

LIBCHK-364 (information) Logic library inconsistencies found for validation.

DESCRIPTION

This information message occurs after validation checking between the two libraries is completed. When the tool finds any inconsistency in validation during validation checking, this message appears.

WHAT NEXT

This is any information only message. No action is required.

However, you are advised to go back to the check report to see the inconsistent results and resolve them as directed by the related LIBCHK man pages.

When you see "inconsistencies found" in the summary report, go back to the related tables for details in

- LIBCHK-300
- LIBCHK-301
- LIBCHK-310
- LIBCHK-311
- LIBCHK-320
- LIBCHK-321
- LIBCHK-330
- LIBCHK-331
- LIBCHK-350

Any of the related LIBCHK man pages will lead to this conclusion.

SEE ALSO

check_library(2)
set_check_library_options(2)
LIBCHK-300(n)
LIBCHK-301(n)
LIBCHK-310(n)
LIBCHK-311(n)
LIBCHK-320(n)
LIBCHK-321(n)
LIBCHK-330(n)
LIBCHK-331(n)
LIBCHK-350(n)

LIBG

LIBG-1 (error) The Synopsys database is corrupted. The library is not created.

DESCRIPTION

A file is read in but no library is found in the file. It is most likely that the file is empty.

WHAT NEXT

Check you library file to make sure it is a valid library.

EXAMPLE MESSAGE

Error: The Synopsys database is corrupted. The library is not created. (LIBG-1)

LIBG-2 (error) An invalid '%s' function string in the '%s' cell.

DESCRIPTION

The string given is not valid for representing a boolean logic defined in Synopsys format.

WHAT NEXT

Refer to your Library Compiler Reference Manual to find out the valid format of the string. It is described in the "function simple attribute" under the "Cell Group Description and Syntax".

EXAMPLES

```
    cell(libg2) {
  area : 1 ;
  pin (I0) {
direction : input ;
capacitance : 0 ;
  }
  pin ("Y") {
direction : output ;
function : "(I0" ;
timing() {
related_pin: "I0" ;
```

```
intrinsic_rise: 1.0 ;
rise_resistance : 0.0 ;
intrinsic_fall  : 1.0 ;
fall_resistance : 0.0 ;
}
  }
```

In this simple case, the closing parenthesis is missing in the function string.

EXAMPLE MESSAGE

Error: Line 400, An invalid '(IO' function string in the 'libg2' cell. (LIBG-2)

LIBG-3 (error) A bad '%s' pin name in the '%s' cell.

DESCRIPTION

This error gets detected during a **read_lib** and an **update_lib** commands. The pin name does not either exist or a previous error in any of the attributes of the pin group is detected. In this case the pin group is not recognized and the pin name is labeled as bad.

WHAT NEXT

Check your library for a wrong pin name in any related attribute or for an incorrect pin group.

EXAMPLES

```
    cell (libg3) {
  area : 4
  pin(A) {
    direction : input
    capacitance : 1
    fanout_load : 1.0
  }
  pin(EN) {
    direction : input
    capacitance : 1
    fanout_load : 1.0
  }
  pin (Z) {
    direction : output
    function : "A"
    three_state : "E";       /* <-- This is wrong */
    max_fanout : 10
 }
```

EXAMPLE MESSAGE

```
Error: Line 426, A bad 'E' pin name in the 'libg3' cell. (LIBG-3)
```

LIBG-4 (error) In the '%s' cell, the '%s' noninput pin cannot be used in the function.

DESCRIPTION

The string associated with a **function** and **three_state** attributes should include only be of **input** or **inout** directions.

WHAT NEXT

Check your library for a wrong direction of the pin in the function attribute. Another possibility is to check the use of the wrong pin name.

EXAMPLES

```
    cell (libg4) {
  area : 4
  pin(A) {
    direction : input
    capacitance : 1
    fanout_load : 1.0
  }
  pin(EN) {
    direction : input
    capacitance : 1
    fanout_load : 1.0
  }
  pin (Z1) {
    direction : output
    function : "A"
    max_fanout : 10
 }
  pin (Z) {
    direction : output
    function : "Z1"           /* <-- This is wrong */
    three_state : "Z1";       /* <-- This is wrong */
    max_fanout : 10
 }
```

EXAMPLE MESSAGE

```
Error: Line 431, In the 'libg4' cell, the 'Z1' noninput pin
        cannot be used in the function. (LIBG-4)
```

LIBG-5 (error) Cannot find the '%s' pin in the '%s' cell.

DESCRIPTION

This error is issued when a pin name attached to a **related_pin** or a **related_bus_pins** attribute does not exist in the cell.

WHAT NEXT

Check your library for a wrong pin name.

EXAMPLES

```
    cell(libg5) {
  area : 1 ;
  pin (I0) {
direction : input ;
capacitance : 0 ;
  }
  pin ("Y") {
direction : output ;
function : "I0" ;
timing() {
related_pin: "IO" ; /* typo zero replaced by letter O */
intrinsic_rise: 1.0 ;
rise_resistance : 0.0 ;
intrinsic_fall  : 1.0 ;
fall_resistance : 0.0 ;
}
  }
```

EXAMPLE MESSAGE

Error: Line 403, Cannot find the 'IO' pin in the 'libg5' cell. (LIBG-5)

LIBG-6 (error) Missing a related_pin for the '%s' pin timing group in the '%s' cell.

DESCRIPTION

This error is issued when the **related_pin** or the **related_bus_pins** attribute is missing in a timing group.

WHAT NEXT

Check your library for a typo in the attribute or add it if it is missing.

EXAMPLES

```
    cell(libg6) {
  area : 1 ;
  pin (I0) {
direction : input ;
capacitance : 0 ;
  }
  pin ("Y") {
direction : output ;
function : "I0" ;
timing() {
   frelated_pin: "I0" ; /* typo f inserted before attribute */
   intrinsic_rise: 1.0 ;
   rise_resistance : 0.0 ;
   intrinsic_fall  : 1.0 ;
   fall_resistance : 0.0 ;
}
  }
```

EXAMPLE MESSAGE

```
Error: Line 399, Missing a related_pin for the 'Y' pin timing group
        in the 'libg6' cell. (LIBG-6)
```

LIBG-8 (error) In the '%s' cell, the '%s' input drives more than one function.

DESCRIPTION

This error is issued when both **function** and **three_state** attributes share one or more inputs pin names.

WHAT NEXT

Either delete one of the attributes or associate a unique string to each of them.

EXAMPLES

```
    cell (libg8) {
  area : 4
  pin(A) {
    direction : input
    capacitance : 1
    fanout_load : 1.0
  }
  pin(EN) {
    direction : input
    capacitance : 1
```

```
    fanout_load : 1.0
  }
  pin (Z1) {
    direction : output
    function : "A"
    three_state : "EN";
    max_fanout : 10
 }
  pin (Z) {
    direction : output
    function : "Z1"       /* ok */
    three_state : "Z1";   /* wrong, Z1 is shared. */
    max_fanout : 10
 }
   }
```

EXAMPLE MESSAGE

```
Error: Line 411, In the 'libg8' cell, the 'Z1' input drives more than one function.
 (LIBG-8)
```

LIBG-10 (warning) Failed to recognize the functionality of cell '%s'.

DESCRIPTION

The warning message is to notify users that Library Compiler fails to synthesize a netlist structure representing functionality of this cell. In order to other cells to recognize the cell, user can specifiy the "user_function_class" attribute either in the .lib file or in Design Compiler.

Note, although the function id of the cell is unknown, it may not be black-box. That is why we are saying that it may not be recognized by Design Compiler.

This message can be used to identify a cell for which pin-class conflict exists. Pin-class is defined as the set of pins which can be swapped without changing the functionality of the gate and is used for DC mapping. In the following simple example, we have PO = ~(PAD * PI) and Y=PAD, and it will cause pin-class conflict because: After parsing the 1st function, we have pin_class(PAD) = pin(PI) because PAD and PI can be exchangable without changing the functionality of the pin PO. However it will break the functionality of the 2nd function cause Y=PAD and Y=PI are totally different.

When pin-class conflict happens, the function id of the cell is set to unknown.

WHAT NEXT

Check your library.

EXAMPLES

```
cell(libg28) {
  area : 1;
  ...
  pin(PAD) {
    direction : input;
    ...
          }
  pin(PI) {
    direction : input;
    ...
          }

  pin(PO) {
    direction : output;
    capacitance : 0;
    ...
    function: "!(PAD * PI)"
  }
  pin(Y) {
    direction : output;
    capacitance : 0;
    ...
    function: "PAD"
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 34,   Failed to recognize the functionality of cell '%s'. (LIBG-10)
```

LIBG-16 (warning) The '%s' Pin/bus on the '%s' cell has no 'function' attribute.
The cell becomes a black box.

DESCRIPTION

This warning is issued when any output of a given cell does not have a valid function(missing or wrong information associated with the function of the pin). A function can be defined either by a **function** attribute, a **three_state** attribute, a **memory_read** group, or an **internal_node** attribute.

WHAT NEXT

Check your library for missing or wrong attributes.

EXAMPLES

```
    cell(libg16) {
  area : 1 ;
  pin (I0) {
direction : input ;
capacitance : 0 ;
  }
  pin ("Y") {
direction : output ;
/*    function : "I0" ;  */
timing() {
related_pin: "I0" ;
intrinsic_rise: 1.0 ;
rise_resistance : 0.0 ;
intrinsic_fall  : 1.0 ;
fall_resistance : 0.0 ;
}
  }
```

EXAMPLE MESSAGE

```
Warning: Line 39, The 'Y' Pin/bus on the 'libg16' cell has no 'function' attribute.
        The cell becomes a black box. (LIBG-16)
```

LIBG-17 (error) The 'function' of the '%s' pin/bus on the '%s' cell can only be '%s' or '%s'.

DESCRIPTION

This error is issued when either the noninverted output (first variable) or the inverted output (second variable) of a sequential model, defined by a ff, a ff_bank, a latch, or a latch_bank group are not assigned to a primary output.

A function statement of each primary output must include either the first variable or the second variable.

WHAT NEXT

Make the appropriate correction in your library, as indicated in the error message. For more information on sequential models, refer to the **Library Compiler Reference** and **User Guide Manuals**.

EXAMPLES

```
    cell(libg17) {
area : 6.50;
pin(CLK) {
direction : input;
```

```
capacitance : 1.5;
}
pin(SET) {
direction : input;
capacitance : 3.0;
}
ff("IQ","IQN") {
next_state : "IQ'";
clocked_on : "CLK";
preset     : "SET'";
}
pin(Q) {
direction : output;
function : "IQ1";/* wrong, should be IQ */
}
pin(QN) {
direction : output;
function : "IQN";
}
      }
```

EXAMPLE MESSAGE

```
Error: Line 23, The 'function' of the 'Q'  in/bus on the 'libg17' cell
        can only be 'IQ' or 'IQN'. (LIBG-17)
```

LIBG-18 (information) The '%s' equation on the '%s' cell is not recognized.

DESCRIPTION

This information is issued when the function is not recognized. The function can be a complex **state_function**, a corrupted string in a **three_state**, a **clocked_on**, or a **clocked_on_also** attribute.

WHAT NEXT

Check your library to determine under which case the information is given. It it is due to the previous error LIBG-4, fix the library. Otherwise, ignore it.

EXAMPLES

```
    cell(libg18) {
area : 6.50;
pin(CLK) {
direction : input;
capacitance : 1.5;
}
pin(SET) {
```

```
direction : input;
capacitance : 3.0;
}
ff("IQ","IQN") {
next_state : "IQ'";
clocked_on : "CLK";
preset     : "SET'";
}
pin(Q) {
direction : output;
function : "IQ";
}
pin(QN) {
direction : output;
function : "IQN";
three_state : "Q"; /* non-input pin not used in function*/
}
      }
```

EXAMPLE MESSAGE

Information: Line 218, The 'three_state' equation on the 'libg18' cell is not recog nized. (LIBG-18)

LIBG-19 (warning) Failed to recognize the functionality of cell '%s'.

DESCRIPTION

Library Compiler fails to synthesize a netlist structure representing functionality of this cell. If the function of a cell is too complex for LC to recognize, the cell becomes a black box. In order to other cells to recognize the cell, user can specifiy the "user_function_class" attribute either in the .lib file or in Design Compiler.

WHAT NEXT

To specify "user_function_class" attribute as described above.

LIBG-20 (error) The '%s' equation on the '%s' cell evaluates to a '%s' constant.

DESCRIPTION

This message is generated when Library Compiler encounters a three-state cell whose

enable signal string is 1 or always evaluates to 1.

WHAT NEXT

Verify the cell and check the library description of the offending cell for correctness.

EXAMPLES

```
    cell(libg20) {
area : 6.50;
pin(CLK) {
direction : input;
capacitance : 1.5;
}
pin(SET) {
direction : input;
capacitance : 3.0;
}
ff("IQ","IQN") {
next_state : "IQ'";
clocked_on : "CLK";
preset     : "SET'";
}
pin(Q) {
direction : output;
function : "IQ";
}
pin(QN) {
direction : output;
function : "IQN";
three_state : "1";
}
      }
```

EXAMPLE MESSAGE

```
Error: Line 218, The 'three_state' equation on the 'libg20' cell evaluates
        to a '1' constant. (LIBG-20)
```

LIBG-21 (error) The derived equality relationship between '%s' and '%s' pins conflicts with the user-specified 'pin_opposite' for the

’%s’ cell.

DESCRIPTION

This error is generated if a cell is read by the library compiler with a pin_opposite attribute that conflicts with the derived equality of the pins. The function statements associated with the pins are the same.

WHAT NEXT

Check your library for a typo in the function strings of the cell or remove the pin_opposite attribute.

EXAMPLES

```
    cell(libg21) {
area : 6.50;
pin(CLK) {
direction : input;
capacitance : 1.5;
}
pin(SET) {
direction : input;
capacitance : 3.0;
}
ff("IQ","IQN") {
next_state : "IQ’";
clocked_on : "CLK";
preset     : "SET’";
}
pin(Q) {
direction : output;
function : "IQ";
}
pin(QN) {
direction : output;
function : "IQ";/* typo, it should be IQN */
}
  pin_opposite("Q","QN");         /* No, they’re equal. */
      }
```

EXAMPLE MESSAGE

```
Error: Line 215, The derived equality relationship between ’QN’ and
        ’Q’ pins conflicts with the user-
specified ’pin_opposite’ for the ’libg21’ cell. (LIBG-21)
```

LIBG-22 (error) The derived opposite relationship between ’%s’

and
’%s’ pins conflicts with the user-specified ’pin_equal’ for the ’%s’ cell.

DESCRIPTION

This error is generated if a cell is read by the library compiler with a pin_equal attribute that conflicts with the derived opposite relationship of the pins . The function statements associated with the pins are opposite.

WHAT NEXT

Check your library for a typo in the function strings of the cell or remove the pin_equal attribute.

EXAMPLES

```
    cell(libg22) {
area : 6.50;
pin(CLK) {
direction : input;
capacitance : 1.5;
}
pin(SET) {
direction : input;
capacitance : 3.0;
}
ff("IQ","IQN") {
next_state : "IQ’";
clocked_on : "CLK";
preset     : "SET’";
}
pin(Q) {
direction : output;
function : "IQ";
}
pin(QN) {
direction : output;
function : "IQN";
}
  pin_equal("Q QN");         /* No, they’re opposite. */
      }
```

EXAMPLE MESSAGE

```
Error: Line 215, The derived opposite relationship between ’QN’ and
        ’Q’ pins conflicts with the user-
specified ’pin_equal’ for the ’libg22’ cell. (LIBG-22)
```

LIBG-24 (information) Unable to honor the ’prefer_tied’ attribute onthe ’%s’ pin
of the ’%s’ cell.

DESCRIPTION

Library Compiler honors as many prefer_tied attributes as possible while it is still able to implement D flip flop functionality. However, it cannot honor all of them. For example, if the library developer specified **prefer_tied : 0** on all the inputs, Library Compiler honors as many as possible and the rest are ignored. If they are ignored, this message is issued during read_lib.

The prefer_tied attribute also can be used to indicate which pin(s) are tied to fixed logic during three_state degeneration for three-state pad cell.

WHAT NEXT

Check your library for the use of the prefer_tied attribute.

EXAMPLES

```
    cell(libg24)  {
        area : 0.0;
pad_cell : true;
pin(Z)  {
    is_pad : true;
    direction : output;
    drive_current : 2.0;
    function : "A";
    three_state : "en tn";
    timing()  {
timing_type : three_state_disable;
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
      related_pin : "tn";
    }
    timing()  {
timing_type : three_state_disable;
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
      related_pin : "en";
    }
    timing()  {
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
            related_pin : "tn";
    }
    timing()  {
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
```

```
        related_pin : "en ";
    }
    timing()  {
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
related_pin : "A";
    }
        }
pin(A)  {
    direction : input;
    capacitance : 0.0;
}
pin(en)  {
    direction : input;
    capacitance : 0.500;
}
pin(tn)  {
    prefer_tied : "0";/* in this case the value should be 1 */
    direction : input;
    capacitance : 0.500;
}
    }
```

EXAMPLE MESSAGE

```
Information: Line 306, Unable to honor the 'prefer_tied' attribute on the  'tn' pin
        of the 'libg24' cell. (LIBG-24)
```

LIBG-25 (warning) Duplicated test signals of '%s' type is found on the '%s' library cell.

DESCRIPTION

The test_cell has more than one of the following valid signal_types: - test_scan_in - test_scan_in_inverted - test_scan_enable - test_scan_enable_inverted - test_scan_out - test_scan_out_inverted - test_scan_clock - test_scan_clock_a - test_scan_clock_b - test_clock

This warning informs you that the port in the test_cell pointed to has more than one signal_type that are listed previously.

WHAT NEXT

Vendors/Library developers should check the test_cell pointed to and make sure that it is the behavior they meant to have. Otherwise,r delete the duplicate signal_type.

If a designer finds this problem, he should contact the vendor or library developer and explain the problem. This problem can only be fixed by the vendor/library

developer.

EXAMPLES

```
  cell(libg25) {
    area : 12;
    pin(D) {
      direction : input;
      capacitance : 1;
    }
    pin(CK,CK2,IH) {
      direction : input;
      capacitance : 1;
    }
    pin(A,B) {
      direction : input
        capacitance : 2;
    }
    pin(SI) {
      direction : input;
      capacitance : 1;
      timing() {
        timing_type : setup_falling;
        intrinsic_rise : 2.8000;
        intrinsic_fall : 2.8000;
        related_pin : "A";
      }
      timing() {
        timing_type : hold_falling;
        intrinsic_rise : 1.2000;
        intrinsic_fall : 1.2000;
        related_pin : "A";
      }
    }
    pin(Q) {
      direction : output;
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 2.5500;
        intrinsic_fall : 2.4000;
        rise_resistance : 0.0700;
        fall_resistance : 0.0300;
        related_pin : "CK IH CK2";
      }
      timing() {
        timing_type : falling_edge;
        intrinsic_rise : 2.5500;
        intrinsic_fall : 2.4000;
        rise_resistance : 0.0700;
        fall_resistance : 0.0300;
        related_pin : "B";
      }
    }
    pin(XQ) {
      direction : output;
```

```
    }
    test_cell(){
      pin(D CK){
        direction : input;
      }
      pin(IH CK2){/* duplicate test_clock */
        direction : input;
        signal_type : "test_clock";
      }
      pin(SI){
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(A){
        direction : input;
        signal_type : "test_scan_clock_a";
      }
      pin(B){
        direction : input;
        signal_type : "test_scan_clock_b";
      }
      state("IQ","IQN"){
        clocked_on : "CK CK2";
        next_state : "D";
      }
      pin(Q){
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(XQ){
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

In this case, there are two test_clock attributes for both 'IH' and 'CK2' pins.

MESSAGE EXAMPLE

```
Warning: Line 67, Duplicated test signals of test_clock type is found on
the 'libg25' library cell. (LIBG-25)
```

LIBG-26 (error) The '%s' test cell pin on the '%s' cell

has no ’function’ attribute. The test cell is removed.

DESCRIPTION

The specified pin has neither a test **signal_type** nor a **function** attribute. This incomplete functional description results in a black-box test cell, which is removed from the library.

WHAT NEXT

Add a proper **function** attribute or **signal_type** attribute to the faulty pin group.

EXAMPLES

```
cell(libg26) {
  area : 12;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CK IH) {
    direction : input;
    capacitance : 1;
  }
  pin(A,B) {
    direction : input
      capacitance : 2;
  }
  pin(SI) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_falling;
      intrinsic_rise : 2.8000;
      intrinsic_fall : 2.8000;
      related_pin : "A";
    }
    timing() {
      timing_type : hold_falling;
      intrinsic_rise : 1.2000;
      intrinsic_fall : 1.2000;
      related_pin : "A";
    }
  }
  pin(Q) {
    direction : output;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 2.5500;
      intrinsic_fall : 2.4000;
      rise_resistance : 0.0700;
      fall_resistance : 0.0300;
```

```
        related_pin : "CK IH";
      }
      timing() {
        timing_type : falling_edge;
        intrinsic_rise : 2.5500;
        intrinsic_fall : 2.4000;
        rise_resistance : 0.0700;
        fall_resistance : 0.0300;
        related_pin : "B";
      }
    }
    pin(XQ) {
      direction : output;
    }
    test_cell(){
      pin(D CK){
        direction : input;
      }
      pin(IH ){
        direction : input;
        signal_type : "test_clock";
      }
      pin(SI){
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(A){
        direction : input;
        signal_type : "test_scan_clock_a";
      }
      pin(B){
        direction : input;
        signal_type : "test_scan_clock_b";
      }
      state("IQ","IQN"){
        clocked_on : "CK CK2";
        next_state : "D";
      }
      pin(Q){
        direction : output;
      }
      pin(XQ){
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

In this case, the pin ’Q’ needs to have a function : "IQ" or signal_type : "test_scan_out" statement

MESSAGE EXAMPLE

```
Error: Line 385, The ’Q’ test cell pin on the ’libg26’ cell
```

has no ’function’ attribute. The test cell is removed. (LIBG-26)

LIBG-27 (warning) The ’%s’ pin is eliminated from the ’%s’ pin function on the ’%s’ cell. The cell becomes a black box.

DESCRIPTION

This message is issued to warn users about the redundant ports in a function string. Redundant ports are ports which are eliminated from the boolean function due to normal boolean simplification.

WHAT NEXT

Check the library for a possible error in the function string.

EXAMPLES

```
    cell(libg27) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }

  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,
     -   ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
  }
  pin(QB) {
    direction : output;
    state_function : "D * 0";
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 448, The ’D’ pin is eliminated from the ’QB’ pin
        function on the ’libg27’ cell. The cell becomes a black box. (LIBG-27)
```

LIBG-28 (warning) The ’%s’ three state pin has no ’function’ or the function is too complex to be recognized; the ’%s’ cell becomes a black box.

DESCRIPTION

This message identifies a cell for which one of its output pins with a three_state attribute has no valid function defined, or its function is too complex to be mapped onto. In this case the library compiler treats the cell as a black box.

WHAT NEXT

Check your library and add the functional information, in case it is absent, to the tri-statable pin. The functional model can be defined by the ’function’ attribute, or ff, latch, memory, or unigen statements.

EXAMPLES

```
cell(libg28) {
  area : 1;
  pin(A) {
    direction : input;
    capacitance : 0;
  }
  pin(TA) {
    direction : output;
    three_state : "A’"; /* missing a function attribute */
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 34, The ’TA’ three state pin has no ’function’ or
the function is too complex to be recognized;
the ’libg28’ cell becomes a black box.  (LIBG-28)
```

LIBG-29 (warning) The state group needs more statements to be meaningful; cell becomes black-box.

DESCRIPTION

This message is issued when a clocked_on or a next_state statement is missing. This message also appears when a latch does not have a minimum of two force statements (force_00, force_01, force_10, and force_11). Library Compiler treats a cell without

a functional model as a black-box.

WHAT NEXT

Check the library for a wrong model and add the missing statement of the corresponding group.

EXAMPLES

```
  cell(libg29) {
    area : 12;
    pin(D) {
      direction : input;
      capacitance : 1;
    }
    pin(CK) {
      direction : input;
      capacitance : 1;
    }
    pin(Q) {
      direction : output;
    }
      state("IQ","IQN"){
        next_state : "D";/* clocked_on : "CK"; missing */
      }
  }
```

EXAMPLE MESSAGE

```
Warning: Line 460, The state group needs more statements to be
        meaningful; cell becomes black-box. (LIBG-29)
```

LIBG-30 (warning) The ’%s’ equation on the ’%s’ cell evaluates to a constant ’%s’. Since this implies the output will never become %s, this equation is ignored.

DESCRIPTION

The sequential library cell has both a force_00 and a force_11 declared. The translation algorithm cannot handle library cells with both of these declarations. This warning message is specific to structural models.

WHAT NEXT

Declare instead either a pair of force_10 and force_01, force_10 and force_11,

force_00 and force_01, force_00 and force_10, or force_01 and force_11. The Q and QN outputs of the specified sequential cell are not complementary. Possible reasons for this are: 1. The library specifies that the outputs are not complementary; 2. The functions driving the force_00 and force_11 inputs of the degenerated sequential cell are not logical zero. For purposes of verification, every sequential cell is degenerated into a primitive sequential cell. The outputs (sourcepoints) of the primitive are Q and QN. The inputs (endpoints) of the primitive are next_state, force_00, force_01, force_10, force_11, clocked_on, and clocked_on_also (for Master-slave cells only). The functions driving the force endpoints characterize the asynchronous properties of the primitive sequential cell. The library might also contain an attribute asserting that the outputs Q and QN are complementary. The force_01 function represents the conditions under which the Q pin can be driven to zero and the QN driven to 1 simultaneously. The other force inputs have a similar interpretation. When the attribute is not present, verification tries to determine that Q and QN are effectively complementary by establishing that both force_00 and force_11 are logically zero. The exact degeneration process depends on the library characterization of the sequential cell and is not described here.

Sequential cells should be modeled using the flip-flop and latch attributes. If you model sequential cells with state attributes, use a local function to describe the asynchronous behavior of each output pin. These functions are hard-coded as async_IQ and async_IQN. The async_IQ, async_IQN, and active functions are based on the forceXX expressions. An example is this flip-flop with Preset and Clear: state (IQ,IQN) { ... force00 : "!CD & !SD" force01 : "!CD & SD" force10 : "CD & !SD" ... } When CD is low, Q is always 0, so the VHDL library generator ORs these two expressions together; instead of (!CD & SD) | (!CD & !SD), the equation becomes !CD. The ORed expression is simplified by Boolean algorithms, which use only 1 and 0 values. If you specify an X for one of these values, the library generator might modify the results.

EXAMPLES

```
    cell(libg30) {
area : 6.50;
pin(CLK) {
direction : input;
capacitance : 1.5;
}
pin(SET) {
direction : input;
capacitance : 3.0;
}
ff("IQ","IQN") {
next_state : "IQ’";
clocked_on : "CLK";
preset     : "SET’";
}
pin(Q) {
direction : output;
function : "IQ";
}
pin(QN) {
direction : output;
function : "IQN";
three_state : "0";
```

```
}
      }
```

EXAMPLE MESSAGE

```
Warning: Line 218, The 'three_state' equation on the 'libg30' cell evaluates
        to a constant '0'. Since this implies the output will never become
        tri-stated, this equation is ignored. (LIBG-30)
```

LIBG-31 (warning) The test cell on cell '%s' does not have any function.

DESCRIPTION

This message indicates that no output port of the test cell has a function attribute.

WHAT NEXT

An output port in the test cell must have a function attribute, a signal_type attribute, or both. At least one output port must have a function attribute. The function attribute can reflect only the nontest behavior of the cell.

LIBG-32 (error) The '%s' parallel sequential cell must use bus/bundle for outputs.

DESCRIPTION

One of the requirement of parallel sequential cells, described by ff_bank or latch_bank groups, is that all outputs are busses or bundles.

This message identifies a parallel sequential cell whose outputs are not busses or bundles

WHAT NEXT

Check your library for a wrong for single bit output pins and define them as busses or bundles.

EXAMPLES

```
cell (LSFDS) {
area : 31.000000 ;
dont_touch : true ;
```

```
dont_use : true ;
bus (D) {
bus_type : BUS4;
direction : input ;
capacitance : 2.000000 ;
}
pin (CK) {
direction : input ;
capacitance : 1.000000 ;
}
ff_bank (IQ,IQN,4) {
next_state : "D" ;
clocked_on : "CK" ;
}
bus (Q) {
bus_type : BUS4;
direction : output ;
function : "IQ" ;
}
pin (SO) {
direction : output ;
function : "IQN" ;
}
}
```

In this case, the pin ’SO’ must be defined as a bus of type BUS4.

EXAMPLE MESSAGE

```
Error: Line 168, The ’libg32’ parallel sequential cell must use
bus/bundle for outputs. (LIBG-32)
```

LIBG-33 (warning) In the ’%s’ cell, the ’%s’ inout pin cannot have feedback in its function. The cell becomes a black box.

DESCRIPTION

The inout pin is in its own function. Library Compiler does not support combinational functions with feedback.

WHAT NEXT

Either break the feedback or try to use a sequential definition.

LIBG-34 (error) The ’%s’ pin in the ’%s’ cell has the ’%s’

direction
The direction must be ’%s’.

DESCRIPTION

The pin on the programmable cell must have the direction specified.

WHAT NEXT

Replace the pin direction attribute by the correct direction.

LIBG-35 (warning) The ’nextstate_type’ attribute on the ’%s’ pin/bus in
the ’%s’ cell is inconsistent with its function. The attribute is ignored.

DESCRIPTION

In a pin group, nextstate_type defines the type of a next_state attribute to be used in an ff group, a seq group, or a ff_bank group.

Any pin with the **nextstate_type** attribute must be in the **nextstate** function. A consistency check is also made between the pin’s nextstate_type attribute and the nextstate function. This message is generated when the attribute ’nextstate_type’ does not match the functional information specified in the cell’s sequential state description.

WHAT NEXT

Check your library for a pin with a nextstate_type attribute but not used in the next_state statement of a sequential group and correct the inconsistency.

EXAMPLES

```
   cell(libg35) {
area : 6.50;
pin(D) {
   direction : input;
   capacitance : 3.0;
}
pin(CLK) {
   direction : input;
   capacitance : 1.5;
}
```

```
pin(SET) {
   direction : input;
   nextstate_type : scan_in;
   capacitance : 3.0;
}

ff("IQ","IQN") {
   next_state : "D";
   clocked_on : "CLK";
   preset     : "SET'";
}

pin(Q) {
   direction : output;
   function : "IQ";
}
pin(QN) {
   direction : output;
   function : "IQN";
}
   }
```

EXAMPLE MESSAGE

```
Warning: Line 153, The 'nextstate_type' attribute on the 'SET' pin/bus in
        the 'libg35' cell is inconsistent with its function. The attribute is ignor
ed. (LIBG-35)
```

LIBG-36 (warning) In the '%s' cell, the '%s' input drives more than one function. The cell might not be optimally used.

DESCRIPTION

This error is issued when more than one attribute inside ff, ff_bank, latch, latch_bank, or seq group share one or more inputs pin names, or when function and three_state on a port have common input pins.

WHAT NEXT

Check your library for shared input pins and associate a unique string to each of them.

EXAMPLES

```
    cell(libg36) {
 area : 6.50;
 pin(D TE) {
```

```
   direction : input;
   capacitance : 3.0;
 }
pin(CLK) {
direction : input;
capacitance : 1.5;
}
ff("IQ","IQN") {
next_state : "D TE";
clocked_on : "CLK";
preset     : "D'";
}

pin(Q) {
direction : output;
function : "IQ";
}
pin(QN) {
direction : output;
function : "IQN";
}
      }
```

In this case, the input pin 'D' is present in the next_state's string and the preset's string.

EXAMPLE MESSAGE

```
Warning: Line 189, In the 'libg36' cell, the 'D' input drives more than one functio
n.
        The cell might not be optimally used. (LIBG-36)
```

LIBG-37 (warning) The '%s' pin/bus is unused in the '%s' cell.

DESCRIPTION

This message is generated when an input pin is not used in the functionality of the cell.

WHAT NEXT

Either delete the unused input pin or add it the functionality of the cell.

EXAMPLES

```
    cell(libg37) {
area : 6.50;
pin(CLK) {
```

```
direction : input;
capacitance : 1.5;
}
pin(SET) {
direction : input;
capacitance : 3.0;
}
ff("IQ","IQN") {
next_state : "IQ'";
clocked_on : "CLK";
}
pin(Q) {
direction : output;
function : "IQ";
}
pin(QN) {
direction : output;
function : "IQN";
      }
  }
```

EXAMPLE MESSAGE

```
Warning: Line 202, The 'SET' pin/bus is unused in the 'libg37' cell. (LIBG-37)
```

LIBG-38 (warning) The '%s' enable pin with a three_state attribute in the '%s' cell should have non-unate timing arcs.

DESCRIPTION

Tri-state enable pins should have "non-unate" timing arcs because the transition depends on the data input. If incorrect timing sense is detected, a warning is issued.

WHAT NEXT

Change the timing sense to "non-unate."

LIBG-39 (warning) The '%s' asynchronous input of the '%s' cell

is inconsistent in active level.

DESCRIPTION

The asynchronous input is inconsistent in "active" level. If "active low," the clear timing arc is **positive-unate**, the preset timing arc is **negative unate**, and the intrinsic fall in recovery constraint is **zero**.

If "active high," the clear timing arc is **negative-unate**, the preset timing arc is **positive-unate**, and the intrinsic rise in recovery constraint is **zero**.

Since the active level of asynchronous input is not explicitly specified, the warning message simply states that, due to inconsistency, the active level of the asynchronous pin cannot be determined by the set of associated timing groups. An inconsistency is found at the given line number.

WHAT NEXT

Determine the asynchronous pin active level. Check the current timing group, and, if inconsistent, make the modification. Otherwise, check other timing groups associated with this asynchronous pin, and change any inconsistency.

EXAMPLES

```
cell("libg39") {
area : 5 ;
state("IQ","IQN") {
  force_00 : "S*R" ;
  force_01 : "R*!S" ;
  force_10 : "S*!R" ;
}
pin("S") {
  direction : input ;
  capacitance : 0.145 ;
}
pin("R") {
  direction : input ;
  capacitance : 0.145 ;
}
pin("Q") {
  direction : output ;
  function : "IQ" ;
  timing() {
    timing_type       : preset ;
    timing_sense      : negative_unate ;
    rise_resistance   :  1.000 ;
    related_pin       : "S" ;
  }
  timing() {
    timing_type       : clear ;
    timing_sense      : negative_unate ;
    intrinsic_fall    :  1.000 ;
```

```
      fall_resistance   :  1.000 ;
      related_pin       : "R" ;
    }
  }
  pin("QN") {
    direction : output ;
    function : "IQN" ;
    timing() {
      timing_type       : clear ;
      timing_sense      : negative_unate ;
      intrinsic_fall    :  1.000 ;
      fall_resistance   :  1.000 ;
      related_pin       : "S" ;
    }
    timing() {
      timing_type       : preset ;
      timing_sense      : positive_unate ;
      intrinsic_rise    :  1.000 ;
      rise_resistance   :  1.000 ;
      related_pin       : "R" ;
    }
  }
}
```

To fix the warning, the timing arc of S in the pin 'Q' has to be positive_unate.

EXAMPLE MESSAGE

```
Warning: Line 32, The 'S' asynchronous input of the 'libg39' cell is inconsistent i
n active level. (LIBG-39)
```

LIBG-40 (warning) The '%s' clock/gate input of the '%s' cell is inconsistent in active edge/level.

DESCRIPTION

A clock is consistent in triggering edge. If positive edge is triggered, only **rising_edge**, **setup_rising**, **hold_rising**, and **recovery_rising** timing types are allowed. If negative edge is triggered, only **falling_edge**, **setup_falling**, **hold_falling**, and **recovery_falling** timing types are allowed. Since the clock-pin triggering edge is not explicitly specified, the warning message simply indicates that, due to inconsistency, the triggering edge of the clock pin cannot be derived from its related timing-group data. An inconsistency is found at the given line number.

A gate is consistent in active level. If "active low," only **non_unate**, **falling_edge**, **setup_rising**, **hold_rising**, and **recovery_rising** timing types are allowed. If "active high," only **non_unate**, **rising_edge**, **setup_falling**, **hold_falling**, and **recovery_falling** are allowed. Since the gate-pin active level is not explicitly specified, the warning message simply indicates that, due to inconsistency, the

active level of the gate pin cannot be derived from its related timing group data. An inconsistency is found at the given line number.

There is one exception: **rising_edge** and **falling_edge** are not checked if the library cell is a black box.

WHAT NEXT

For a clock pin, determine the triggering edge first. Check the current timing group data, and modify timing-group data if found to be inconsistent with clock-triggering edge. Otherwise, check other timing groups that are related to the clock pin, and, if inconsistency is found, make the change.

For a gate pin, determine the active level first, check the current timing-group data, and modify timing-group data if found to be inconsistent with gate-active level. Otherwise, check other timing groups that are related to the gate pin, and, if inconsistency is found, make the change.

EXAMPLES

```
    cell(RAM1) {
area : 4;
pin(D) {
direction : input;
capacitance : 2;
timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.00;
      intrinsic_fall : 1.00;
      related_pin : "WR";
    }
}
pin(WR) {
    direction : input;
    capacitance : 1;
}
state ("IQ","IQN") {
    force_01 : "D’ WR";
    force_10 : "D WR ";
}
pin(QN) {
    direction : output;
    function : "IQN";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.00;
      intrinsic_fall : 1.00;
      rise_resistance : 0.1000;
      fall_resistance : 0.1000;
      related_pin : "WR";
    }
}
   }
```

EXAMPLE MESSAGE

```
Warning: Line 266, The 'WR' clock/
gate input of the 'RAM1' cell is inconsistent in active edge/level. (LIBG-40)
```

LIBG-41 (warning) The 'when' attribute (%s) uses pins that cannot be found in %s (%s).

DESCRIPTION

In a combinational cell, the following pins are allowed to appear in the **when** attribute of the state-dependent timing arc:

1) Pins in the **function** attribute for a combinational timing arc.

2) Pins in the **three_state** attribute for a three_state_disable timing arc.

This warning informs you that one of the previous restrictions has been violated.

WHAT NEXT

Check the **when** attribute and correct any wrong information in the string or in the timing type.

EXAMPLES

```
cell(libg41) {
 area : 2;
 pin(D1 D0 S0 EN) {
   direction : input;
   capacitance : 1;
 }
 pin(Z) {
   direction : output;
   function : "S0'D0 + S0 D1";
   three_state : "EN";
   timing() {
     timing_sense : non_unate;
     timing_type : three_state_disable;
     intrinsic_rise : 1.00;
     intrinsic_fall : 1.00;
     rise_resistance : 0.1;
     fall_resistance : 0.1;
     related_pin : "EN";
   }
   timing() {
     timing_sense : non_unate;
     intrinsic_rise : 1.00;
     intrinsic_fall : 1.00;
```

```
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "EN D1 D0 S0";
    }
    timing() {
      when : "S0'D0 + S0 D1' + EN";
      sdf_cond : "(D1 == 1'b0 && S0 == 1'b1) || (D0 == 1'b1 && S0 == 1'b0)";
      timing_sense : positive_unate;
      intrinsic_rise : 1.00;
      intrinsic_fall : 1.00;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "S0";
    }
  }
}
```

In this case, the pin 'EN' is not included in the function string of the pin 'Z'.

EXAMPLE MESSAGE

```
Warning: Line 69, The 'when' attribute (S0'D0 + S0 D1' + EN) uses pins
        that cannot be found in function attribute (S0'D0 + S0 D1). (LIBG-41)
```

LIBG-42 (error) The '%s' related pin of the '%s' cell has clear/ preset
timing arcs but is not asynchronous.

DESCRIPTION

The timing group is a clear/preset arc but the related pin is not asynchronous. The related pin must be in a force statement or in a clear/preset statement to be in a clear/preset timing arc.

WHAT NEXT

Define the related pin as asynchronous in the functional description or remove the timing arc.

EXAMPLES

```
    cell (libg42)  {
        area : 8.000;
        pin(D)  {
                direction : input;
                capacitance : 0.100;
        }
        pin(CK)  {
```

```
                direction : input;
                capacitance : 0.100;
        }
        ff(IQ,IQB)  {
                next_state : "D";
                clocked_on : "CK";
        }
        pin(QB)  {
                direction : output;
                function : "IQB" ;
                timing()  {
                        timing_type : rising_edge;
                        intrinsic_rise : 2.000;
                        intrinsic_fall : 3.000;
                        rise_resistance : 8.000;
                        fall_resistance : 6.000;
                        related_pin : "CK";
                }
        }
        pin(Q)  {
                direction : output;
                function : "IQ" ;
                timing()  {
                        timing_type : clear ;
                        timing_sense : negative_unate ;
                        intrinsic_fall : 1.000;
                        fall_resistance : 4.000;
                        related_pin : "QB";
                }
        }
}
```

EXAMPLE MESSAGE

```
Error: Line 270, The 'QB' related pin of the 'libg42' cell has clear/preset
        timing arcs but is not asynchronous. (LIBG-42)
```

LIBG-43 (error) The '%s' related pin of this timing arc is an output pin and the timing_sense is not specified.

DESCRIPTION

If the related pin of a timing arc is an output pin, provide the **timing_sense** attribute.

WHAT NEXT

Check the functionality of the cell, and provide the correct **timing_sense** to this

timing arc.

EXAMPLES

```
    cell(libg43) {
      area : 8.000;
      pin(A E) {
direction : input;
capacitance : 1.00;
      }
      pin(B) {
direction : output;
function : "!A";
timing() {
  related_pin : "A";
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
}
      }
      pin(C) {
direction : inout;
function : "A";
three_state : "E";
timing() {
  related_pin : "E";
  timing_type : three_state_disable;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
}
timing() {
  related_pin : "E";
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
}
timing() {
  related_pin : "B";
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
}
      }
    }
```

In this case, a timing_sense attribute is missing in the timing group between the inout pin 'C' and the output pin 'B'.

EXAMPLE MESSAGE

```
Error: Line 75, The 'B' related pin of this timing arc is an output pin and
        the timing_sense is not specified. (LIBG-43)
```

LIBG-44 (error) The logic represented by the 'when' string (%s)

in this
 timing group is not mutually exclusive with the logic represented by
 the ’when’ string (%s) in the timing group on line %d.

DESCRIPTION

The logic represented by the ’when’ string of all state-dependent timing arcs between a pair of pins should be mutually exclusive. If it isn’t, Library Compiler is not be able to determine which timing arc to use to propagate signal through the path when the condition causes both of them to be evaluated ’TRUE’.

WHAT NEXT

Check the ’when’ strings of both timing groups for wrong information and fix it.

EXAMPLES

```
    cell(libg44) {
      area : 2;
      pin(D1 D0 S0) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "S0’D0 + S0 D1";
timing() {
  timing_sense : non_unate;
  intrinsic_rise : 1.00;
  intrinsic_fall : 1.00;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : " D0 D1";
}
timing() {
  when : "S0’D0 + S0 D1’";
  when : "D1’ S0 + S0’D0 ";
  sdf_cond : "(D1 == 1’b0 && S0 == 1’b1) || (S0 == 1’b0 && D0 == 1’b1)";
  timing_sense : positive_unate;
  intrinsic_rise : 1.00;
  intrinsic_fall : 1.00;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "S0";
}
timing() {
  when : "D1 S0 + S0’D0";
  sdf_cond : "(D1 == 1’b1 && S0 == 1’b1) || (S0 == 1’b0 && D0 == 1’b0)";
  timing_sense : non_unate;
```

```
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "S0";
}
timing() { /* default */
  intrinsic_rise : 1.00;
  intrinsic_fall : 2.00;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "S0";
}
      }
    }
```

In this case, the second when attribute's string has a typo. It should be "D1 S0 + S0'D0'"; where the pin D0 should be ticked according to the sdf_cond attribute's string.

EXAMPLE MESSAGE

```
Error: Line 258, The logic represented by the 'when' string (S0'D0 + S0 D1') in this
        timing group is not mutually exclusive with the logic represented by
        the 'when' string (D1 S0 + S0'D0) in the timing group on line 268. (LIBG-
44)
```

LIBG-45 (error) The 'timing_sense' attribute is missing. It is required
for '%s' timing arc.

DESCRIPTION

For timing arcs of timing_type 'clear' or 'preset', timing_sense is a required attribute. It can be either 'positive_unate' or 'negative_unate' or 'non_unate'.

WHAT NEXT

Check your logic between the input and output pins and put the appropriate timing_sense in the timing group.

EXAMPLES

```
    cell(libg45) {
      area : 9;
      pin(D CP CD) {
direction : input;
capacitance : 1;
```

```
      }
      state("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
force_01   : "CD'";
      }
      pin(Q) {
direction : output;
function : "IQ";
timing() {
  timing_type : clear;/* timing_sense missing */
  intrinsic_fall : 0.77;
  fall_resistance : 0.0523;
  related_pin : "CD";
}
      }
      pin(QN) {
direction : output;
function : "IQN";
timing() {
  timing_type : preset;
  timing_sense : negative_unate;
  intrinsic_rise : 0.87;
  rise_resistance : 0.1523;
  related_pin : "CD";
}
      }
    }
```

In this case, there is a missing timing_sense attribute with positive_unate for the 'clear' timing arc of the pin 'Q'.

EXAMPLE MESSAGE

```
Error: Line 256, The 'timing_sense' attribute is missing. It is required
        for 'clear' timing arc. (LIBG-45)
```

LIBG-46 (error) The '%s' pin of the '%s' cell is not a clock/enable pin and cannot be used in the 'related_pin' of timing arc with the '%s' timing_type.

DESCRIPTION

Pin in the 'related_pin' of the timing group with the timing_type rising_edge or falling_edge should be a clock/enable pin.

WHAT NEXT

Check your library to see if you place the wrong pin in the 'related_pin' attribute or you have specified wrong 'timing_type'.

EXAMPLES

```
cell(libg46) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
    min_period : 99
    timing() {
      timing_type : rising_edge
      intrinsic_rise : 1.640000
      intrinsic_fall : 1.880000
      rise_resistance : 0.182000
      fall_resistance : 0.059000
      related_pin : "D"
    }
  }
  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,
     -   ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    inverted_output : FALSE;
    timing() {
      timing_type : rising_edge
      intrinsic_rise : 1.640000
      intrinsic_fall : 1.880000
      rise_resistance : 0.182000
      fall_resistance : 0.059000
      related_pin : "CP"
    }
  }
  pin(QB) {
    direction : output;
    internal_node : "Q";
    inverted_output : TRUE;
    timing() {
      timing_type : rising_edge
      intrinsic_rise : 1.640000
      intrinsic_fall : 1.880000
      rise_resistance : 0.182000
      fall_resistance : 0.059000
      related_pin : "CP"
```

```
    }
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 120, The 'D' pin of the 'libg46' cell is not a clock/enable pin and
        cannot be used in the 'related_pin' of timing arc with the
        'rising_edge' timing_type. (LIBG-46)
```

LIBG-47 (warning) Cell(%s): The state table entries have been expanded.
The following %d %s of overlapping entries %s been found:
For each occurrence, the first "rule out" entry is used.

DESCRIPTION

This message informs the user that overlapping entries have been found in the state table, and that the first one encountered is being used. Overlapping entries can occur when entries (that is, rules) in the **table** attribute of the **statetable** group are expanded. Overlapping means that for a single input value combination, there are multiple next internal node combinations. During expansion, some entries might overlap with others; the entry highest in the table overrides those below it.

NOTE:

All inputs that are **always** don't care are not mentioned in
the input string of occurrences.

WHAT NEXT

You can avoid receiving this message by once explicitly listing the next internal node for every permutation of L and H for the current inputs, previous inputs, and current states.

EXAMPLES

```
  statetable ( "D WR WRN", "Q QN") {
    table : "L/H H L : - - : L/H H/L,\ /* rule 1 */
             -   - - : - - : N   N";   /* rule 2 */
  }
```

During the expansion of the table into an ordered table with L and H inputs and L, H, X, and N next internal nodes, rule 1 expands into

```
            L H L : - - : L H /* rule 3 */
            H H L : - - : H L /* rule 4 */
```

and rule 2 expands into

```
            L H L : - - : N N /* rule 5 */
            H H L : - - : N N /* rule 6 */
```

In this case, there is an overlap between rules 3 and 5 and rules 4 and 6.

EXAMPLE MESSAGE

```
Warning: Line 214, Cell(libg47): The state table entries have been expanded.
The following 2 occurrences of overlapping entries have been found:
occurrence 1: rule in: "L H L", rule out #1: "L H", rule out #2: "N N"
occurrence 2: rule in: "H H L", rule out #1: "H L", rule out #2: "N N"
For each occurrence, the first "rule out" entry is used. (LIBG-47)
```

LIBG-48 (warning) Cell(%s): The following %d %s, which includes
current and delayed input values in the state table, %s unspecified: %s
Outputs are made unknown.

DESCRIPTION

In the 'table' attribute of the 'statetable' group, some entries (rules) are unspecified. All permutations of the input nodes are not specified by the table. Therefore, the internal node is made unknown for all of the missing entries.

WHAT NEXT

This warning can be eliminated by carefully specifying the state table to avoid unspecified entries.

NOTE:

The input edges symbols, {"R", "~R", "F", "~F"}, represent permutations of L and H for the delayed input and the current input. Every edge-sensitive input(one with at least one input edge symbol) is expanded into two level-sensitive inputs: the current input value and the delayed input value. For example, the input edge symbol "R" expands to "L" for the delayed input value and "H" for the current input value.

EXAMPLES

```
  statetable ( "D CP", "Q QB") {
```

```
    table : "L R : - - : L H,\

     - ~R : - - : N   N";
  }
```

During the table expansion, the output for the input permutation of CP* (delayed), CP, and D: "L H H" is not specified. The output is set to "X X".

EXAMPLE MESSAGE

```
Warning: Line 134, Cell(libg48): The following 1 entry, which includes
        current and delayed input values in the state table, is unspecified:
        inputs: CP*, CP, D
                "011"
        Outputs are made unknown. (LIBG-48)
```

LIBG-49 (error) Cell(%s): ’%s’ token in "%s" field is not recognized.

DESCRIPTION

The token is not a valid state table token for that field in the table. The valid tokens for input nodes are {L, H, -, L/H, H/L, R, F, ~R, and ~F}. The valid tokens for current internal nodes are {L, H, -, L/H, and H/L}. The valid tokens for next internal nodes are {L, H, L/H, H/L, X, and N}. Therefore, the table is deleted.

WHAT NEXT

Replace the invalid token with a valid one.

LIBG-50 (error) Cell(%s): Incorrect "%s" field size in table. Size found: %d, expecting: %d.

DESCRIPTION

In the ’table’ attribute of the ’statetable’ group, either the input nodes, the current internal nodes, or the next internal nodes has an incorrect number of tokens.

WHAT NEXT

Fix the number of entries in the table.

EXAMPLES

```
  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - : L/H H/L,\

     -   ~R : - : N   N";
  }
```

The current field must have 2 tokens instead of 1. Change the state table to

```
  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\

     -   ~R : - - : N   N";
  }
```

EXAMPLE MESSAGE

```
Error: Line 134, Cell(libg50): Incorrect "current" field size in table.
Size Found: 1, expecting: 2. (LIBG-50)
```

LIBG-51 (error) Cell(%s): The ’%s’ port has too many port names in ’input_map’.
Number of ports specified is %d, the maximum number expected is %d.

DESCRIPTION

There are too many port names specified in the ’input_map’ attribute of the port. The maximum number of ports in ’input_map’ is equal to the number of input nodes plus the number of internal nodes plus the number of input nodes that are edge sensitive. Therefore, the table is deleted.

WHAT NEXT

Remove some of the port names.

EXAMPLES

```
  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\

     -   ~R : - - : N   N";
  }
  pin(Q) {
    direction : output;
    function : "IQ";
    internal_node : "Q";
```

```
    input_map : "D CP Q QB CP CP";
    ...
  }
```

The maximum number of port names expected in the input_map attribute is 5: 2 input nodes (D, CP), one delayed input (CP*), and 2 internal nodes(Q, QB).

EXAMPLE MESSAGE

Error: Line 139, Cell(libg51): The 'Q' port has too many port names in 'input_map'. Number of ports specified is 6, the maximum number expected is 5. (LIBG-51)

LIBG-52 (error) Cell(%s): The '%s' port requires either 'internal_node' or 'state_function'.

DESCRIPTION

The output or inout port does not have either an 'internal_node' attribute or a 'state_function' attribute even though a state table is defined. If a state table is defined, every output and inout port must have either an 'internal_node' or a 'state_function'. Therefore, the table is deleted.

WHAT NEXT

Add either an 'internal_node' attribute or a 'state_function' attribute to the port.

EXAMPLES

```
  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\

     -   ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
    function : "IQ";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.34;
      intrinsic_fall : 1.54;
      rise_resistance : 0.0718;
      fall_resistance : 0.0347;
      related_pin : "CP";
    }
  }
```

In this example, the pin Q is missing the **state_function** or the **internal_node** attribute.

EXAMPLE MESSAGE

Error: Line 139, Cell(libg52): The ’Q’ port requires either ’internal_node’ or ’state_function’. (LIBG-52)

LIBG-53 (error) Cell(%s): The ’internal_node’ in the ’%s’ port does not match any internal node name in the state table.

DESCRIPTION

The ’internal_node’ attribute on the port is not equal to the name of any internal node in the state table. Every ’internal_node’ attribute must match one of the internal node names. Therefore, the table is deleted.

WHAT NEXT

Change the ’internal_node’ attribute to equal an internal node name, or change an internal node name to equal the ’internal_node’ attribute.

EXAMPLES

```
statetable ( "D CP", "Q QB") {
  table : "L/H R  : - - : L/H H/L,\

   -   ~R : - - : N   N";
}

pin(Q) {
  direction : output;
  function : "IQ";
  internal_node : "Q1";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.34;
    intrinsic_fall : 1.54;
    rise_resistance : 0.0718;
    fall_resistance : 0.0347;
    related_pin : "CP";
  }
}
```

In this case, Q1 is not an internal node in the state table.

EXAMPLE MESSAGE

```
Error: Line 139, Cell(libg53): The 'internal_node' in the 'Q' port
does not match any internal node name in the state table. (LIBG-53)
```

LIBG-54 (information) Cell(%s): The '%s' internal pin does not drive any output or is unneeded. The pin is ignored.

DESCRIPTION

This message indicates that the specified internal pin does not directly or indirectly drive any output port, or that the pin can be deleted without affecting the functionality of the cell. An internal pin that is never visible is functionally useless. Every internal pin must have a unique functional relationship with an output port. The specified internal pin is ignored.

WHAT NEXT

Either delete the internal pin or give it a unique functional relationship with an output port.

EXAMPLES

```
cell(libg54) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 0.9;
      intrinsic_fall : 0.9;
      related_pin : "CP";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.4;
      intrinsic_fall : 0.4;
      related_pin : "CP";
    }
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }

  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\
```

```
    -   ~R : - - : N   N";
  }

  pin(n1) {
    direction : internal;
    internal_node : "Q";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.34;
      intrinsic_fall : 1.54;
      rise_resistance : 0.0718;
      fall_resistance : 0.0347;
      related_pin : "CP";
    }
  }
  pin(Q) {
    direction : output;
    internal_node : "Q";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.34;
      intrinsic_fall : 1.54;
      rise_resistance : 0.0718;
      fall_resistance : 0.0347;
      related_pin : "CP";
    }
  }
  pin(QB) {
    direction : output;
    internal_node : "QB";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.34;
      intrinsic_fall : 1.54;
      rise_resistance : 0.0718;
      fall_resistance : 0.0347;
      related_pin : "CP";
    }
  }
}
```

In this case, n1 is not functionally used.

EXAMPLE MESSAGE

```
Information: Line 139, Cell(libg54): The 'n1' internal pin does not drive any
        output or is unneeded. The pin is ignored. (LIBG-54)
```

LIBG-55 (error) Cell(%s): The 'input_map' in the '%s' port is not

allowed with the ’state_function’. Deleting the table.

DESCRIPTION

This message indicates that the specified port has both a **state_function** attribute and an **input_map** attribute. A port with a **state_function** attribute cannot have an **input_map** attribute. The **input_map** attribute can occur only with the **internal_node** attribute. Therefore, the table is deleted. However, the following combinations of attributes can be specified on the same port:

* **state_function** and **three_state** attributes
* **internal_node** and **input_map** attributes
* **internal_node** and **three_state** attributes

WHAT NEXT

Either replace the **state_function** attribute with an **internal_node** attribute, or delete the **input_map** attribute.

EXAMPLES

```
pin(Q) {
  direction : output;
  state_function : "Q";
  input_map : "D CP";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.34;
    intrinsic_fall : 1.54;
    rise_resistance : 0.0718;
    fall_resistance : 0.0347;
    related_pin : "CP";
  }
}
```

You cannot have both state_function and input_map attributes in the same pin group.

EXAMPLE MESSAGE

```
Error: Line 139, Cell(libg55): The ’input_map’ in the ’Q’ port is not
allowed with the ’state_function’. Deleting the table. (LIBG-55)
```

LIBG-56 (error) Cell(%s): The ’%s’ node must be specified in

the ’input_map’ of the ’%s’ port. Deleting the table.

DESCRIPTION

This message indicates that a node was specified as a don’t care "-" in the ’input_map’ of the port, but the node is necessary for the port. Every functionally related input node and current internal node must be specified. Therefore, the table is deleted.

WHAT NEXT

Investigate why the assumption that the node is functionally unrelated to the port is incorrect. Possible reasons might be that the wrong internal code is chosen, the state table is incorrectly specified, or the ’input_map’ is incorrect.

EXAMPLES

```
statetable ( "D CP", "Q QB") {
  table : "L/H R  : - - : L/H H/L,\

   -   ~R : - - : N   N";
}

pin(Q) {
  direction : output;
  internal_node : "Q";
  input_map : "D -";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.34;
    intrinsic_fall : 1.54;
    rise_resistance : 0.0718;
    fall_resistance : 0.0347;
    related_pin : "CP";
  }
}
```

The use of a dont’care, "-", in the input_map means that the inputs ’CP’ and ’CP*’ are not used for the outport port ’Q’. However, given the state table, the nodes ’CP’ and ’CP*’ (delayed) are necessary for ’Q’ and must be specified in the input_map string.

EXAMPLE MESSAGE

Error: Line 139, Cell(libg56): The ’CP’ node must be specified in the ’input_map’ of the ’Q’ port. Deleting the table. (LIBG-56)

LIBG-57 (error) Cell(%s): Duplicate ’%s’ names in the

’input_map’ of the ’%s’ port.

DESCRIPTION

Two or more nodes have been mapped to the same name either implicitly or explicitly in the ’input_map’ attribute of the port. Every node used in the table must be mapped to a unique port. Unspecified node names in the ’input_map’ are implicitly mapped to the node names specified in the state table. Therefore, the table is deleted.

WHAT NEXT

Change the ’input_map’ attribute to eliminate duplicate names.

EXAMPLES

```
  statetable ( "D CP", "Q") {
    table : "L/H R  : - - : L/H,\

     -   ~R : - - : N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    input_map : "D D";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
```

In the previous case, the port name ’D’ is explicitly duplicated for nodes D and CP.

```
  statetable ( "D CP", "Q") {
    table : "L/H R  : - - : L/H,\

     -   ~R : - - : N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    input_map : "CP";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
```

```
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
```

In the previous case, the port name 'CP' is implicitly duplicated for nodes 'D' (explicitly specified in the input_map string) and 'CP' (implicitly mapped to the node name specified in the state table).

EXAMPLE MESSAGE

Error: Line 139, Cell(libg57): Duplicate 'D' names in the 'input_map' of the 'Q' port. (LIBG-57)

LIBG-58 (error) Cell(%s): For the '%s' port, the '%s' node is mapped to '%s', which is not a port.

DESCRIPTION

After the state table node names have been explicitly and implicitly mapped to names, one of the mapped node names is not the name of a port. Every mapped node name must be the name of a port. Unspecified node names in the 'input_map' are implicitly mapped to the node names specified in the state table. Therefore, the table is deleted.

The state table is in a completely independent, isolated name space. The term "node" refers to the identifiers. The "input nodes" and the "internal nodes" can have any name made up of any character except white space and comments.

The node names are resolved to the real port names by each port with an internal_node attribute. This mapping occurs by a combination of the 'input_map' attribute and the 'internal_node' attribute. If a node name is not mapped explicitly to a real port name in the 'input_map', it automatically inherits the node name as the real port name. The internal node name specified by the 'internal_node' attribute maps implicitly to the output being defined.

After all node names have been mapped to real port names, the real port names are checked to verify that they exist and are of the right direction. That is why the error message occurs at the output port. This is when elaboration occurs.

WHAT NEXT

Change the **input_map** attribute.

EXAMPLES

```
  statetable ( "D CP", "Q") {
    table : "L/H R  : - - : L/H,\

     -   ~R : - - : N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    input_map : "data CP";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
```

In this case, the port ’data’ does not exist in the cell.

EXAMPLE MESSAGE

```
Error: Line 139, Cell(libg58): For the ’Q’ port, the ’D’ node is mapped to
        ’data’, which is not a port. (LIBG-58)
```

LIBG-59 (error) Cell(%s): The ’input_map’ of the ’%s’ port maps the ’%s’ input port to the ’%s’ internal node.

DESCRIPTION

The mapped internal node name refers to an input port. An internal node must be mapped to either an output, an internal pin, or an inout port but not to an input port. An input port cannot be driven. Therefore, the table is deleted.

WHAT NEXT

Change the ’input_map’ attribute.

EXAMPLES

```
  pin(CP EN) {
    direction : input;
    capacitance : 1;
  }
```

```
statetable ( "D CP", "Q QB") {
  table : "L/H R  : L - : L/H H/L,\

           L/H R  : H - : L H,\

   -   ~R : - - : N   N";
}

pin(Q) {
  direction : output;
  internal_node : "Q";
  input_map : "D CP EN";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.34;
    intrinsic_fall : 1.54;
    rise_resistance : 0.0718;
    fall_resistance : 0.0347;
    related_pin : "CP";
  }
}
```

In this case, The internal node 'Q' is mapped to an input port 'EN'. Remove 'EN' from the input_map, or change its direction.

EXAMPLE MESSAGE

Error: Line 140, Cell(libg59): The 'input_map' of the 'Q' port maps the 'EN' input port to the 'Q' internal node. (LIBG-59)

LIBG-60 (warning) Cell(%s): translates into a combinational cell. The State table information is not created.

DESCRIPTION

This message indicates that the library cell has a sequential description that actually represents a combinational function. The state table information is allowed only for describing sequential functions. This situation occurs only when reading in an old technology library DB file. Issuing this warning is controlled by the **dc_shell** or the **lc_shell** environment variable **read_db_lib_warnings**.

WHAT NEXT

Update the original technology library source file and recompile.

EXAMPLE MESSAGE

Warning: Cell(libg60): translates into a combinational cell.

The state table information is not created. (LIBG-60)

LIBG-61 (error) Cell(%s): Verification failure on the '%s' port. Deleting the table.

DESCRIPTION

When a cell has both a state table and the v3.1 format, the Library Compiler automatically converts the v3.1 format to UNIGEN. The UNIGEN generated from the v3.1 format is formally compared against the UNIGEN generated from the state table. They must match.

This message indicates that the state table description for the port does not match its sequential description. If both a state table description and a sequential description (ff, latch, ff_bank, or latch_bank) are specified for the library cell, they must match each other exactly. A listing of the differences is printed out. The maximum number of differences to be listed is controlled by the **dc_shell** environment variable **libgen_max_difference**.

WHAT NEXT

Fix or delete the state table, or fix or delete the sequential description.

EXAMPLES

```
cell(libg61) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }

  seq( IQ, IQN) {
```

```
    clocked_on : "CP";
    next_state : "D";
  }

  statetable ( "D CP", "Q QB") {
    table : "L/H F  : - - : L/H H/L,\

     -   ~F : - - : N   N";
  }

  pin(Q) {
    direction : output;
    function : "IQ";
    internal_node : "Q";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
  pin(QB) {
    direction : output;
    function : "IQN";
    internal_node : "QB";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 139, Cell(libg61): Verification failure on the 'Q' port. Deleting the t
able.  (LIBG-61)
  Both table inputs are: D*, CP*, CP
  List of differences between statetable vs. v3.1 table:
    001    N <=> L
    010    L <=> N
    101    N <=> H
    110    H <=> N
```

LIBG-62 (warning) Cell(%s): The '%s' input node is not required by any

internal node used. The input node is ignored.

DESCRIPTION

This message indicates that the specified input node is not functionally related to any internal node used. Therefore, the input node is unused. An input node must be related to at least one internal node. This warning is for informational purposes because of the possibility of a user error. This message is suppressed if the input node has always been specified with the don’t care,"-", token.

WHAT NEXT

Determine why the input node is unused, and correct the problem.

EXAMPLES

```
cell(libg62) {
   area : 10;
   pin(D) {
     direction : input;
     capacitance : 1;
     timing() {
       timing_type : setup_rising;
       intrinsic_rise : 0.1;
       intrinsic_fall : 0.1;
       related_pin : "CP";
     }
     timing() {
       timing_type : hold_rising;
       intrinsic_rise : 0.1;
       intrinsic_fall : 0.1;
       related_pin : "CP";
     }
   }
   pin(CP) {
     direction : input;
     capacitance : 1;
   }

   ff( IQ, IQN) {
     clocked_on : "CP";
     next_state : "D";
   }

   statetable ( "D CP X", "Q QB") {
     table :  "L/H R  - : - - : L/H H/L,\

                -   ~R L/H : - - : N   N";
   }

   pin(Q) {
     direction : output;
```

```
    function : "IQ";
    internal_node : "Q";
        timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
  pin(QB) {
    direction : output;
    function : "IQN";
    internal_node : "QB";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 134, Cell(libg62): The 'X' input node is not required by any
        internal node used. The input node is ignored. (LIBG-62)
```

LIBG-63 (error) Cell(%s): The '%s' internal node is combinational.

DESCRIPTION

In the table description of the internal node, there is no hold state "N". Every internal node should have a hold state "N". Otherwise, it is not a sequential node. Every internal node should be a single sequential storage element. Therefore, the table is deleted.

WHAT NEXT

Add a hold state to the internal node or delete the internal node.

EXAMPLES

```
cell(libg63) {
  area : 10;
```

```
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }

  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\

     -   ~R : - - : L   N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
  pin(QB) {
    direction : output;
    internal_node : "QB";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
}
```

In this case, the node ’QB’ has a "N" state in the table but, the node ’Q’ does not have an "N" state. All internal nodes in the table require at least one "N" state

and at least one "non-N", or "non-X" state.

EXAMPLE MESSAGE

Error: Line 134, Cell(libg63): The ’Q’ internal node is combinational. (LIBG-63)

LIBG-64 (error) Cell(%s): The ’%s’ port cannot have both ’internal_node’ and ’state_function’ attributes.

DESCRIPTION

The port has both an ’internal_node’ attribute and a ’state_function’ attribute. Ports can only have either an ’internal_node’ attribute, which is a name of an internal node, or a ’state_function’ attribute, which is the output logic. Therefore, the table is deleted.

A port can have the following combination of attributes:

* **state_function** and **three_state** attributes
* **internal_node** and **input_map** attributes
* **internal_node** and **three_state** attributes

WHAT NEXT

Remove either the ’internal_node’ attribute or the ’state_function’ attribute.

EXAMPLES

```
cell(libg64) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
  }
  pin(CP) {
```

```
    direction : input;
    capacitance : 1;
  }

  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\

     -   ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    state_function : "Q";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
  pin(QB) {
    direction : output;
    internal_node : "QB";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 139, Cell(libg64): The 'Q' port cannot have both 'internal_node'
        and 'state_function' attributes. (LIBG-64)
```

LIBG-65 (error) Cell(%s): The '%s' internal pin cannot have a 'three_state' attribute.

DESCRIPTION

The internal pin has a 'three_state' attribute. Internal pins are not allowed to have a 'three_state' attribute. The attribute 'three_state' can only be specified on output or inout ports.

WHAT NEXT

Either change the internal pin to a port or remove the 'three_state' attribute.

EXAMPLES

```
cell(libg65) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }

  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\

     -   ~R : - - : N   N";
      }

      pin(Q) {
    direction : internal;
    internal_node : "Q";
    three_state : "D";/* not allowed for internal pin */
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }

  pin(QB) {
        direction : output;
    internal_node : "QB";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
```

```
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 139, Cell(libg65): The 'Q' internal pin cannot have a 'three_state' att
ribute. (LIBG-65)
```

LIBG-67 (warning) Cell(%s): The '%s' port has both the internal_node and the input_map specified. However, there is a mismatch in the mapping. The '%s' port is mapped by the input_map instead of the '%s' port, the name of the internal_node. The '%s' port, specified in the input_map, is used.

DESCRIPTION

The port mapped by 'input_map' to the internal node specified in internal_node is not equal to the name of the port being defined. The current state of an output port should be equal to the state of the output port, not another port. This condition should almost never be violated, but the user is given the freedom to do so with a warning.

WHAT NEXT

Change the input_map attribute to map the current state to the port being defined.

EXAMPLES

```
cell(libg67) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 0.1;
```

```
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }

  statetable ( "D CP", "Q QB") {
    table : "L/H R  : L - : L/H H/L,\

                L/H R  : H - : L H,\

     -   ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    input_map : "D CP QB";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
  pin(QB) {
    direction : output;
    internal_node : "QB";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 140, Cell(libg67): The 'Q' port has both the internal_node
and the input_map specified. However, there is a mismatch in the mapping.
The 'QB' port is mapped by the input_map instead of the 'Q' port,
```

the name of internal_node. The 'QB' port, specified in the input_map, is used. (LIB G-67)

LIBG-68 (error) Cell(%s): Mismatch in internal pins between the v3.1 format and the state table. Deleting the table.

DESCRIPTION

UNIGEN generated from the v3.1 format is formally compared against UNIGEN generated from the state table. They must match.

This message indicates that the v3.1 format has an implied internal pin that cannot be mapped to an internal pin in the state table. There must be a one-to-one match between the internal pins of the state table and the v3.1 format.

WHAT NEXT

Determine whether the state table is specified incorrectly or is missing an internal pin. Correct the problem.

EXAMPLES

```
cell(libg68) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
  }
  pin(CP CP_ALSO) {
    direction : input;
    capacitance : 1;
  }

  ff( IQ, IQN) {
    clocked_on : "CP";
    clocked_on_also : "CP_ALSO";
```

```
    next_state : "D";
  }

  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - -  : L/H H/L,\

     -   ~R : - - : N   N";
  }

  pin(QB) {
    direction : output;
    function : "IQN";
    internal_node : "QB";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP_ALSO";
    }
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 140, Cell(libg68): Mismatch in internal pins between
the v3.1 format and the state table. Deleting the table. (LIBG-68)
```

LIBG-69 (warning) Cell(%s): The '%s' input is specified as delayed in the state table. It will be used.

DESCRIPTION

Delayed input nodes are specified in the state table description, and can be specified with the asterisk (*) suffix. Only advanced users should consider specifying delayed inputs because there is a potential for error and confusion.

WHAT NEXT

Try to specify the state table without referring to delayed inputs.

EXAMPLES

```
cell(libg69) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
  }
  pin(CP) {
    direction : input;
        capacitance : 1;
  }

  statetable ( "D CP* CP", "Q QB") {
    table : "L/H L  H  : - - : L/H H/L,\

     -   H  - : - - : N   N,\

     -   L  L : - - : N   N";
  }

  pin(Q) {
    direction : output;
            internal_node : "Q";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
          fall_resistance : 0.1;
      related_pin : "CP";
    }
  }

  pin(QB) {
    direction : output;
    internal_node : "QB";
    timing() {
      timing_type : rising_edge;
```

```
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 134, Cell(libg69): The 'CP' input is specified as
        delayed in the state table. It will be used. (LIBG-69)
```

LIBG-70 (warning) Cell(%s): Delayed inputs are specified in the input_map of the '%s' port. They will be used.

DESCRIPTION

Delayed input ports are specified in the input_map attribute, and are specified after the undelayed inputs and the internal nodes. Only advanced users should consider specifying delayed inputs because there is a potential for error and confusion.

WHAT NEXT

Try to specify the 'input_map' without mapping to delayed inputs.

EXAMPLES

```
cell(libg70) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CP";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
      related_pin : "CP";
    }
  }
  pin(CP) {
```

```
    direction : input;
    capacitance : 1;
  }

  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\

     -   ~R : - - : N   N";
  }

      pin(Q) {
    direction : output;
    inverted_output : FALSE;
    internal_node : "Q";
    input_map : "D CP Q - CP";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }

  pin(QB) {
    direction : output;
    internal_node : "QB";
    inverted_output : TRUE;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 139, Cell(libg70): Delayed inputs are specified in
        the input_map of the 'Q' port. They will be used. (LIBG-70)
```

LIBG-71 (error) Cell(%s): The '%s' port was expected to be %s with

respect to the ’%s’ port.

DESCRIPTION

The two ports are not the function of each other as expected. The expected behavior is derived from the v3.1 format, and the state table is expected to match. Therefore, the table is deleted.

WHAT NEXT

Correct the state table or the v3.1 format.

EXAMPLES

```
cell(libg71) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
  }

  pin(CP) {
    direction : input;
    capacitance : 1;
  }

  ff( IQ, IQN) {
    clocked_on : "CP";
    next_state : "D";
  }

  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - -  : L/H H/L,\

     -   ~R : - -  : N   N";
  }

  pin(Q) {
    direction : output;
    function : "IQ";
```

```
    internal_node : "Q";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }

  pin(QB) {
    direction : output;
    function : "IQ";/* Wrong! function should be IQN */
    internal_node : "QB";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
}
```

In this case, the function descriptions for the two ports are inconsistent. From the v3.1 table, the two ports have the same function (notice the typo in the function of the pin 'QB', instead of 'IQN', the function string is 'IQ'). From the UNIGEN table they are inverted.

EXAMPLE MESSAGE

```
Error: Line 139, Cell(libg71): The 'Q' port was expected to be uninverted with
        respect to the 'QB' port. (LIBG-71)
```

LIBG-72 (error) Cell(%s): Cannot find an implicit internal pin in the v3.1 format to match the '%s' internal pin.

DESCRIPTION

The internal pin does not have a corresponding internal pin in the v3.1 format. The internal pins of both the v3.1 format and the state table format must match. Therefore, the table is deleted.

WHAT NEXT

Correct the state table or the v3.1 format.

EXAMPLES

```
cell(libg72) {
  area : 10;
  pin(force11) {
    direction : input;
    capacitance : 1;
  }
  pin(force10) {
    direction : input;
    capacitance : 1;
  }
  pin(force01) {
    direction : input;
    capacitance : 1;
  }
  pin(force00) {
    direction : input;
    capacitance : 2;
  }
  pin(ck ck_also) {
    direction : input;
    capacitance : 2;
  }
  pin(next) {
    direction : input;
    capacitance : 2;
      }

  state("IQ","IQN") {
    next_state : "next";
    clocked_on : "ck";
    clocked_on_also : "ck_also";
    force_00   : "force00";
    force_01   : "force01";
    force_10   : "force10";
    force_11   : "force11";
  }

  statetable ("next ck force00 force01 force10 force11",\

"int_net") {

     table : "-   -   H   L   L   L   : -   : L,\

             -   -   L   H   L   L   : -   : L,\

             -   -   L   L   H   L   : -   : H,\

             -   -   L   L   L   H   : -   : H,\

             -   ~R  L   L   L   L   : -   : N,\

             L/H R   L   L   L   L   : -   : L/H";
  }
```

```
  pin(int_net) {
    direction : internal;
    internal_node : "int_net";
    input_map : "next ck_also force00 force01 force10 force11 int_net";
      }

  pin(Q) {
    direction : output;
    function : "IQ";
    internal_node : "int_net";
    input_map : "int_net ck_also force00 force01 force10 force11 Q";
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 165, Cell(libg72): Cannot find an implicit internal pin in
        the v3.1 format to match the 'int_net' internal pin. (LIBG-72)
```

LIBG-73 (warning) Cell(%s): Table inputs for the '%s' port exceed 16 inputs.

DESCRIPTION

The state table is stored with over 16 table inputs. There is an exponential cost in performance and memory as the number of table inputs increases. This warning tells the user about the excessive size of table inputs. To list the table, use the report_lib command with the **full_table** option.

WHAT NEXT

If possible, take advantage of the input_map attribute to reduce the size of the table.

EXAMPLES

```
cell(libg73) {
  area : 10;
  pin(i0 i1 i2 i3 i4 i5 i6 i7 i8 j0 j1 j2 j3 j4 j5) {
    direction : input;
    capacitance : 1;
  }
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 0.9;
```

```
      intrinsic_fall : 0.9;
      related_pin : "CP";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.4;
      intrinsic_fall : 0.4;
      related_pin : "CP";
    }
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }

  statetable ( "D i0 i1 i2 i3 i4 i5 i6 i7 i8 j0 j1 j2 j3 j4 j5 CP", "Q ") {
    table : "H H H H H H H H H H H H H H H H R   : - : H,\

             - - - - - - - - - - - - - - - - R   : - : L,\

             - - - - - - - - - - - - - - - - ~R  : - : N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.34;
      intrinsic_fall : 1.54;
      rise_resistance : 0.0718;
      fall_resistance : 0.0347;
      related_pin : "CP";
    }
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 149, Cell(libg73): Table inputs for the 'Q' port exceed 16 inputs.
(LIBG-73)
```

LIBG-74 (error) Cell(%s): No internal_node output pin is found.

DESCRIPTION

A state table is defined for the library cell, but none of the output pins are defined as sequential. There must be at least one output with an internal_node attribute specified.

WHAT NEXT

Remove the state table description or add an internal_node attribute to at least one output.

EXAMPLES

```
cell(libg74) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
          related_pin : "CP";
    }
  }

  pin(CP) {
    direction : input;
    capacitance : 1;
  }

  statetable ( "D CP ", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\

     -   ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
    state_function : "D";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }

  pin(QB) {
    direction : output;
    state_function : "D";
    timing() {
      timing_type : rising_edge;
```

```
      intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
          rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
}
```

In this case, both output pins ’Q’ and ’QB’ have state_function and no internal_node attribute.

EXAMPLE MESSAGE

```
Error: Line 137, Cell(libg74): no internal_node output pin is found. (LIBG-74)
```

LIBG-75 (error) Cell(%s): The state_function on the ’%s’ port has
an invalid port in the expression.

DESCRIPTION

A valid port in a state_function expression is either an input port, an inout port with a three_state attribute, or an output port with the internal_node attribute. This error is issued if a port in the state_function is either an output port without an internal_node attribute or an inout port without a three_state attribute. Neither of these two kinds of ports is allowed in the state_function expression.

WHAT NEXT

Change the state_function expression, or change the invalid port.

EXAMPLES

```
cell(libg75) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.1;
```

```
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
  }

  pin(CP) {
    direction : input;
    capacitance : 1;
  }

  statetable ( "D CP ", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\

     -   ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }

  pin(QB) {
    direction : output;
    state_function : "Q";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }

  pin(QC) {
    direction : output;
    state_function : "QB"; /* 'QB' is an output without internal_node*/
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
        }
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 167, Cell(libg75): The state_function on the 'QC' port has
an invalid port in the expression. (LIBG-75)
```

LIBG-76 (warning) The '%s' test cell pin on the '%s' cell has a timing arc. The timing arc is ignored.

DESCRIPTION

The test cell pin has a timing arc, but timing arcs are only valid on the library cell.

WHAT NEXT

Move all timing arcs in the test cell to the top-level library cell.

EXAMPLES

```
cell(libg76) {
  area : 11;
  pin(D0) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK1";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CK1";
    }
  }
  pin(TI) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK1";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
```

```
    related_pin : "CK1";
  }
}
pin(TE) {
  direction : input;
  capacitance : 1;
  prefer_tied : "0";
  timing() {
    timing_type : setup_rising;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "CK1";
  }
  timing() {
    timing_type : hold_rising;
    intrinsic_rise : 0.1;
    intrinsic_fall : 0.1;
    related_pin : "CK1";
  }
}
pin(CK1) {
  direction : input;
  capacitance : 1;
}
pin(CK2) {
  direction : input;
  capacitance : 1;
}
statetable("D0 TE TI CK1 CK2", "n1 Q") {
  table : "-   -  -  -  L  : L/H - : - L/H,\

   L/H L  -  L  -  : -   - : L/H -,\

   -   H L/H L  -  : - - : L/H -,\

   -   -  -  -  -  : - -  : N N";
}

pin(n1) {
  direction : internal;
  internal_node : "n1";
}

pin(Q) {
  direction : output;
  internal_node : "Q";
  timing() {
    timing_type : falling_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "CK2";
  }
}
```

```
    pin(QN) {
      direction : output;
      state_function : "Q'";
      timing() {
        timing_type : falling_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "CK2";
      }
    }
    test_cell() {
      pin(D0) {
        direction : input;
      }
      pin(TI) {
        direction : input;
        signal_type : "test_scan_in";
        timing() {/* move  it to the cell level*/
          timing_type : setup_rising;
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
          related_pin : "CK1";
        }
      }
      pin(TE) {
        direction : input;
        signal_type : "test_scan_enable";
      }
      pin(CK1) {
        direction : input;
        capacitance : 1;
      }
      pin(CK2) {
        direction : input;
        capacitance : 1;
      }
      statetable("D0 CK1", "Q") {
        table : "-   H : - : N,\

         L/H L  : - : L/H";
      }

      pin(n1) {
        direction : internal;
        internal_node : "Q";
      }
      pin(Q) {
        direction : output;
internal_node : "Q";
input_map : "n1 CK2";
        signal_type : "test_scan_out";
      }
      pin(QN) {
```

```
        direction : output;
state_function : "Q'";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Warning: Line 209, The 'TI' test cell pin on the 'libg76' cell
        has a timing arc. The timing arc is ignored. (LIBG-76)
```

LIBG-77 (error) The '%s' test cell pin on the '%s' cell has a conflicting pin type.

DESCRIPTION

This message indicates that the test cell has one of these invalid combinations:

Two pins, of which one has the **signal_type** attribute "test_scan_in" and the other has "test_scan_in_inverted";

or Two pins, of which one has the **signal_type** attribute "test_scan_enable" and the other has "test_scan_enable_inverted".

A test cell cannot have two pins whose **signal_type** attributes are the inversions of each other.

WHAT NEXT

Change one of the **signal_type** attributes so that the test cell has only one of the pins in the above invalid combinations.

LIBG-78 (warning) The '%s' test cell pin on the '%s' cell has a conflicting pin type. Removing the test cell.

DESCRIPTION

This message indicates that the test cell has one of these invalid combinations:

Two pins, of which one has the **signal_type** attribute "test_scan_in" and the other has "test_scan_in_inverted";

or Two pins, of which one has the **signal_type** attribute

"test_scan_enable" and the other has "test_scan_enable_inverted".

A test cell cannot have two pins whose **signal_type** attributes are the inversions of each other. The test cell has been removed; DFT Compiler will not use it.

WHAT NEXT

Change one of the **signal_type** attributes so that the test cell has only one of the pins in the above invalid combinations. Then re-execute.

LIBG-79 (error) The '%s' test cell pin on the '%s' cell has a conflict between the function and the test type.

DESCRIPTION

The test cell pin either has a signal_type attribute of "test_scan_out" and a function of the inverted output (i.e. second variable) or the pin has a signal_type attribute of "test_scan_out_inverted" and a function of the non-inverted output (i.e. first variable).

If a pin has both a signal_type attribute and a function attribute, the two attributes must be consistent. A "test_scan_out" corresponds to the non-inverted output function and a "test_scan_out_inverted" corresponds to the inverted output.

WHAT NEXT

Change either the signal_type attribute or the function.

LIBG-80 (warning) The '%s' test cell pin on the '%s' cell has a conflict between the function and the test type. The test cell is removed.

DESCRIPTION

The test cell pin either has a signal_type attribute of "test_scan_out" and a function of the inverted output (i.e. second variable) or the pin has a signal_type attribute of "test_scan_out_inverted" and a function of the non-inverted output (i.e. first variable).

If a pin has both a signal_type attribute and a function attribute, the two attributes must be consistent. A "test_scan_out" corresponds to the non-inverted output function and a "test_scan_out_inverted" corresponds to the inverted output.

The test cell is removed and DFT Compiler will not use it.

WHAT NEXT

Change either the signal_type attribute or the function.

LIBG-81 (error) Cell(%s): translates into a combinational cell.

DESCRIPTION

The library cell has a sequential description, which represents a combinational function. The state table information is only allowed on sequential library cells.

WHAT NEXT

Change the sequential description.

EXAMPLES

```
    cell(libg81) {
      area : 4;
      pin(Q) {
max_fanout : 1.0;
direction : output;
function : "IQ";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "CK";
}
timing() {
  timing_type : preset;
  timing_sense : "negative_unate";
  intrinsic_rise : 1.0;
  rise_resistance : 0.1;
  related_pin : "SETZ"
}
      }
      pin(QZ) {
direction : output;
function : "IQZ";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
```

```
  fall_resistance : 0.1;
  related_pin : "CK";
}
timing() {
  timing_type : clear;
  timing_sense : "positive_unate";
  intrinsic_fall : 1.0;
  fall_resistance : 1.0;
  related_pin : "SETZ";
}
      }
      pin(CK) {
direction : input;
clock : true;
min_period : 1.0;
capacitance : 0.1;
      }
      pin(S) {
direction : input;
capacitance : 1.0;
timing() {
  timing_type : setup_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "CK";
}
timing() {
  timing_type : hold_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "CK";
}
      }
      pin_opposite("Q","QZ");
      state("IQ","IQZ") {
next_state : "(S' A) + (S B)";
clocked_on : "CK";
force_01   : "SETZ";
force_10   : "SETZ'";
      }
      pin(A) {
direction : input;
capacitance : 1.0;
timing() {
  timing_type : setup_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "CK";
}
timing() {
  timing_type : hold_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "CK";
}
```

```
      }
      pin(B) {
direction : input;
capacitance : 0.1;
timing() {
  timing_type : setup_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "CK";
}
timing() {
  timing_type : hold_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "CK";
}
      }
      pin(SETZ) {
direction : input;
capacitance : 0.1;
      }
    }
```

EXAMPLE MESSAGE

```
Error: Line 109, Cell(libg81): translates into a combinational cell. (LIBG-81)
```

LIBG-82 (error) The test cell on the '%s' cell is not DFT Compiler supported.

DESCRIPTION

This message indicates that the description of the specified test cell is not supported by DFT Compiler. DFT Compiler has restrictions on the non-test mode and test inputs; the test cell violates one or more of these restrictions. For details on these restrictions, refer to the **DFT Compiler Test Design Rule Checking User Guide**.

WHAT NEXT

Revise the test cell description so that it conforms to DFT Compiler restrictions; or, remove the test cell.

LIBG-83 (warning) The test cell on the '%s' cell is not DFT Compiler supported.

Removing the test cell.

DESCRIPTION

The test cell has a description that is not supported by DFT Compiler. DFT Compiler has restrictions on the non-test mode and test inputs; the test cell violates one or more of these restrictions. For details on these restrictions, refer to the **DFT Compiler Test Design Rule Checking User Guide**.

The test cell has been removed; DFT Compiler will not use this cell during scan insertion.

WHAT NEXT

Obtain the technology library source and revise the test cell description so that it conforms to DFT Compiler restrictions; or, remove the test cell.

LIBG-84 (warning) The '%s' port in the '%s' cell does not have a function in the test cell descriptions. The cell is a black box.

DESCRIPTION

No function for that port can be derived from the test cells. The port function must be either explicitly specified or inferable from the test cell descriptions. The cell is a black box.

This warning is issued when reading a .db library and can be switched off by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-85.

WHAT NEXT

Change the technology library source by explicitly or implicitly providing the function for that port.

LIBG-85 (error) The '%s' port in the '%s' cell does not

have a function in the test cell descriptions.

DESCRIPTION

No function for that port can be derived from the test cells. The port function must be either explicitly specified or inferable from the test cell descriptions. Some functional information is described but not all. Either the cell is completely specified, or it is completely unspecified.

WHAT NEXT

Change the technology library source by either describing the port function explicitly or implicitly in the test cell descriptions or removing all functional descriptions.

EXAMPLES

```
cell(libg85) {
  area : 11;
  pin(D0) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.3;
      intrinsic_fall : 1.3;
      related_pin : "CK1";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.3;
      intrinsic_fall : 0.3;
      related_pin : "CK1";
    }
  }
  pin(TI) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.3;
      intrinsic_fall : 1.3;
      related_pin : "CK1";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.3;
      intrinsic_fall : 0.3;
      related_pin : "CK1";
    }
  }
```

```
pin(TE) {
  direction : input;
  capacitance : 1;
  prefer_tied : "0";
  timing() {
    timing_type : setup_rising;
    intrinsic_rise : 1.3;
    intrinsic_fall : 1.3;
    related_pin : "CK1";
  }
  timing() {
    timing_type : hold_rising;
    intrinsic_rise : 0.3;
    intrinsic_fall : 0.3;
    related_pin : "CK1";
  }
}
pin(CK1) {
  direction : input;
  capacitance : 1;
}

pin(Q) {
  direction : output;
  inverted_output : FALSE;
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.09;
    intrinsic_fall : 1.37;
    rise_resistance : 0.1458;
    fall_resistance : 0.0523;
    related_pin : "CK1";
  }
}

pin(QN) {
  direction : output;
  inverted_output : TRUE;
      timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.59;
    intrinsic_fall : 1.57;
    rise_resistance : 0.1458;
    fall_resistance : 0.0523;
    related_pin : "CK1";
  }
}

test_cell() {
  pin(D0) {
        direction : input;
  }
  pin(TE) {
    direction : input;
    signal_type : "test_scan_enable";
```

```
      }
      pin(TI) {
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(CK1) {
        direction : input;
        capacitance : 1;
      }

      statetable("D0 CK1", "Q") {
table : "L/H F : - : L/H,
 -  ~F : - : N";
      }

      pin(Q) {
        direction : output;
        internal_node : "Q";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 177, The 'QN' port in the 'libg85' cell does not
        have a function in the test cell descriptions. (LIBG-85)
```

LIBG-86 (warning) The '%s' port in the '%s' cell has a timing arc related to '%s' that is inconsistent.

DESCRIPTION

The timing type of the timing arc from the specified port to the related port is inconsistent with respect to other timing in the cell. For example, a port cannot have both a **rising_edge** timing type and a **falling_edge** timing type.

This warning occurs only when reading in a technology library DB file. Issuing this warning is controlled by the **dc_shell** or the **lc_shell** environment variable **read_db_lib_warnings**.

The same problem in a .lib library causes an error. See the .lib example for LIBG-88.

WHAT NEXT

Update the original technology library source. Make timing arcs consistent.

EXAMPLE MESSAGE

```
Warning: The 'Q' in the 'libg86' cell has a timing
arc related to 'D' that is inconsistent. (LIBG-86)
```

LIBG-87 (error) Cell(%s): the internal node has L/H or H/L but no input has L/H or H/L. Deleting the table.

DESCRIPTION

In the **table** attribute of the **statetable** group, an internal node has either L/H or H/L specified but none of the input nodes have either L/H or H/L specified. If an internal node has either the L/H or H/L value, at least one input node must be L/H or H/L. Therefore, the table is deleted.

WHAT NEXT

Change the **table** attribute to replace L/H or H/L for the internal node with either L, H, X, or N, or make one of the input nodes L/H or H/L.

EXAMPLES

```
cell(libg87) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }
```

```
  statetable ( "D CP", "Q QB") {
    table :     "L R  : - - : L/H H/L,\

                        - ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }

  pin(QB) {
    direction : output;
    internal_node : "QB";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
}
```

EXAMPLE MESSAGE

```
Error: Line 132, Cell(libg87): the internal node has L/H or H/L but
no input has L/H or H/L. Deleting the table. (LIBG-87)
```

LIBG-88 (error) The ’%s’ port in the ’%s’ cell has a timing arc related to ’%s’ that is inconsistent.

DESCRIPTION

The timing type of the timing arc from the specified port to the related port is inconsistent with respect to other timing in the cell. For example, a port cannot have both a **rising_edge** timing type and a **falling_edge** timing type.

WHAT NEXT

Update the technology library source to make the timing arcs consistent.

EXAMPLES

```
  cell(libg88) {
    area : 13;
    pin(D) {
      direction : input;
      capacitance : 1;
      timing() {
        timing_type : setup_rising;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        related_pin : "C";
      }
      timing() {
        timing_type : hold_rising;
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
            related_pin : "C";
      }
    }
    pin(C) {
      direction : input;
      capacitance : 2;
    }
    pin(D2) {
      direction : input;
      capacitance : 1;
      timing() {
        timing_type : setup_rising;
            intrinsic_rise : 1.0;
            intrinsic_fall : 1.0;
        related_pin : "C2";
      }
      timing() {
        timing_type : hold_falling;/* error */
        intrinsic_rise : 0.0;
        intrinsic_fall : 0.0;
            related_pin : "C2";
      }
    }
    pin(C2) {
      direction : input;
      capacitance : 2;
    }
    pin(Q) {
      direction : output;
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 0.1;
        rise_resistance : 0.1;
```

```
      fall_resistance : 0.1;
      related_pin : "C";
    }
    timing() {
          timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 0.1;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
      related_pin : "C2";
    }
  }
  pin(QN) {
    direction : output;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 2.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "C";
    }
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 2.0;
      rise_resistance : 0.1;
          fall_resistance : 0.1;
      related_pin : "C2";
    }
  }
  test_cell() {
    pin(D) {
          direction : input;
        }
    pin(C) {
      direction : input;
        }
    pin(D2) {
      direction : input;
          signal_type : "test_scan_in";
        }
        pin(C2) {
          direction : input;
      signal_type : "test_scan_clock";
    }
        state ("IQ","IQN") {
      next_state : "D";
      clocked_on : "C";
        }
    pin(Q) {
      direction : output;
      function : "IQ";
      signal_type : "test_scan_out";
    }
```

```
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 89, The 'D2' port in the 'libg88' cell has a timing
        arc related to 'C2' that is inconsistent. (LIBG-88)
```

LIBG-89 (warning) The '%s' port in the '%s' cell has an inconsistent function in the test cells.

DESCRIPTION

The test_cells define different functions for the port. The port must have one unique function among all of the test cells.

When reading a .db library, Library Compiler uses the first test_cell to create the full functional description. The second test_cell is ignored.

This warning can be switched off by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-90.

WHAT NEXT

The default behavior of selecting the first test_cell as the correct one should be correct in most cases.

Change the technology library source to make the function of the port in all of the test cells consistent.

LIBG-90 (error) The '%s' port in the '%s' cell has an inconsistent

function in the test cells.

DESCRIPTION

This message indicates that the test cells define different functions for the specified port. The port must have one unique function among all test cells.

WHAT NEXT

Update the technology library source so that the function of the port in all test cells is consistent.

EXAMPLES

```
cell(libg90) {
  area : 21;
  pin(D1) {
    direction : input;
    capacitance : 1;
  }
  pin(C1) {
    direction : input;
    capacitance : 2;
  }
  pin(D2) {
    direction : input;
    capacitance : 1;
  }
  pin(C2) {
    direction : input;
    capacitance : 2;
  }
  pin(C3) {
    direction : input;
        capacitance : 1;
  }

  pin(Q1) {
    direction : output;
    timing() {
          timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 0.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "C1";
    }
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 0.0;
      rise_resistance : 0.1;
```

```
    fall_resistance : 0.1;
    related_pin : "C2";
  }
}
pin(Q2) {
  direction : output;
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C3";
  }
}
test_cell() {
  pin(D1) {
    direction : input;
  }
  pin(C1) {
    direction : input;
  }
  pin(D2) {
    direction : input;
    signal_type : "test_scan_in";
  }
  pin(C2) {
    direction : input;
    signal_type : "test_scan_clock_a";
      }
  pin(C3) {
    direction : input;
    signal_type : "test_scan_clock_b";
  }
  state("IQ","IQN") {
    force_10 : "C1 D1";
    force_01 : "C1 D1'";
  }
  pin(Q1) {
    direction : output;
        function : "IQ";
  }
  pin(Q2) {
    direction : output;
    signal_type : "test_scan_out";
  }
}
test_cell() {
  pin(D1) {
    direction : input;
  }
  pin(C1) {
    direction : input;
      }
  pin(D2) {
```

```
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(C2) {
        direction : input;
        signal_type : "test_scan_clock_a";
          }
      pin(C3) {
        direction : input;
      }
      seq("IQ","IQN") {
        data_in  : "D1";
        enable : "C1";
        enable_also : "C3'";
      }
      pin(Q1) {
        direction : output;
          }
      pin(Q2) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(Q2N) {
        direction : output;
            function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

For the pin 'Q2', the 'function' attribute is missing in the first test_cell.

EXAMPLE MESSAGE

```
Error: Line 175, The 'Q2' port in the 'libg90' cell has an inconsistent
        function in the test cells. (LIBG-90)
```

LIBG-91 (error) The '%s' attribute is required when both 'clear' and 'preset' are present in the sequential model and the %s '%s' is used in the function attribute of the output pin(s) of the cell.

DESCRIPTION

When both 'clear' and 'preset' are present in the sequential model, the **clear_preset_var1** and/or **clear_preset_var2** attributes are required, depending on which variable of the sequential model is used in the function attribute of the output pin(s) of the cell. For example, if the first variable is used, **clear_preset_var1** is required.

WHAT NEXT

Make the appropriate correction in your library, as indicated in the error message. For more information on the **clear_preset_var** attributes, refer to the **Library Compiler Reference Manual**, Vol. 1.

LIBG-92 (warning) The '%s' port in the '%s' cell has a circular dependency.

DESCRIPTION

There is an undelayed feedback loop to the output, inout, and internal port. This circular dependency is not allowed.

This warning is issued if the current port appears in the list of expanded inputs of the port.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-93.

WHAT NEXT

Break the feedback loop by delaying one of the inputs in the feedback path.

LIBG-93 (error) The '%s' port in the '%s' cell has a circular dependency.

DESCRIPTION

There is an undelayed feedback loop to the output port. This circular dependency is not allowed.

This error is issued if the current port appears in the list of expanded inputs of the port.

WHAT NEXT

Break the feedback loop by delaying one of the inputs in the feedback path.

EXAMPLES

```
cell(libg93) {
  area : 7;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(R) {
    direction : input;
    capacitance : 1;
  }

  statetable("D R CP", "Q") {
    table : "H/L L  R : - : H/L,\

               -  L ~R : - :  N,\

       -  H -  : - :  H";
  }

  /* internal sequential state_function */
  pin(E) {
    direction : internal;
    state_function : "Q1+R";
  }

  /* slave with sequential reset */
  pin(Q1) {
    direction : internal;
    internal_node : "Q";
    input_map : "D Q2 CP";
  }

  /* master driving Q1 */
  pin(Q2) {
    direction : output;
    internal_node : "Q"
    input_map : "D E CP";
  }

  pin(CP) {
    direction : input;
    capacitance : 1;
  }

}
```

In this case, there is a feedback loop for ’Q1’. To break the dependency, delay one of the inputs in the feedback path. The pins ’E’ and ’Q2’ in the cell group can be changed as follows:

```
  pin(E) {
    direction : internal;
    state_function : "D+Q1";
```

```
}
pin(Q2) {
  direction : output;
  internal_node : "Q"
  input_map : "E R CP";
}
```

EXAMPLE MESSAGE

Error: Line 274, The ’Q1’ port in the ’libg93’ cell has a circular dependency. (LIB G-93)

LIBG-94 (warning) The ’%s’ cell needs a noninverted output.

DESCRIPTION

The test cell does not have any noninverted output. This particular type of test cell requires at least one noninverted output to be defined.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-95.

WHAT NEXT

Specify the full function or define an output to be noninverted.

LIBG-95 (error) The ’%s’ cell needs a noninverted output.

DESCRIPTION

The test cell has no noninverted output. This particular type of test cell requires at least one noninverted output to be defined.

WHAT NEXT

Specify the full function or define an output to be noninverted.

EXAMPLES

```
cell(libg95) {
  area : 15;
  pin(D) {
```

```
      direction : input;
      capacitance : 1;
    }
    pin(C) {
      direction : input;
      capacitance : 2;
    }
    pin(TSI) {
      direction : input;
      capacitance : 1;
    }
    pin(TSE) {
      direction : input;
      capacitance : 2;
    }
    pin(QN) {
      direction : output;
      capacitance : 2;
    }
    pin(TSO TSOI) {
      direction : output;
    }
    test_cell() {
      pin(D) {
        direction : input;
      }
      pin(C) {
        direction : input;
      }
      pin(TSI) {
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(TSE) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_enable";
      }
      statetable("D C", "QN") {
table : "L/H H : - : H/L,\

 -   L : - : N";
      }

      pin(TSOI) {
        direction : output;
        signal_type : "test_scan_out_inverted";
      }
      pin(TSO) {
        direction : output;
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
internal_node : "QN";
```

```
      }
    }
  }
```

In this case, the cell is a latch. To fix the problem, add another noninverted pin. For example, the following change to the cell will fix the problem.

```
  cell(libg95) {
    ...
    pin(Q) {
      direction : output;
      capacitance : 2;
    }
    ...
    test_cell() {
...
      statetable("D C", "Q QN") {
table : "L/H H : - - : L/H H/L,\

 -   L : - - : N N";
      }
...
      pin(Q) {
        direction : output;
internal_node : "Q";
      }
    }
}
```

EXAMPLE MESSAGE

```
Error: Line 142, The 'libg95' cell needs a noninverted output. (LIBG-95)
```

LIBG-96 (warning) The '%s' port in the '%s' cell is used in both test and non test mode.

DESCRIPTION

The input port has a test attribute and is also used in the non test mode. This is not allowed.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-97.

WHAT NEXT

Specify the full function of the test cell.

LIBG-97 (error) The '%s' port in the '%s' cell is used in both test and non test mode.

DESCRIPTION

The input port has a test attribute and is also used in the non test mode. This is not allowed.

WHAT NEXT

Specify the full function of the test cell.

EXAMPLES

```
  cell(libg97) {
    area : 13;
    pin(D TSI) {
      direction : input;
      capacitance : 1;
    }
    pin(C TSE) {
      direction : input;
      capacitance : 2;
    }
    pin(Q TSO) {
      direction : output;
    }
    test_cell() {
      pin(D C) {
        direction : input;
      }
      pin(TSI) {
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(TSE) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_enable";
      }
      statetable("C D TSI", "Q") {
table : "H L/H H/L : - : L/H,\

 L -  -  : - : N";
      }
```

```
      pin(Q) {
        direction : output;
internal_node : "Q";
      }
      pin(TSO) {
        direction : output;
        signal_type : "test_scan_out";
       }
    }
  }
```

In this case, the input port 'TSI' has the "test_scan_in" attribute, and it is used in the state table input entry.

EXAMPLE MESSAGE

```
Error: Line 141, The 'TSI' port in the 'libg97' cell is used in both
test and non test mode. (LIBG-97)
```

LIBG-98 (warning) The '%s' test cell has an incompatible non test mode.

DESCRIPTION

The non test mode of the test cell is incompatible with the test attributes of the test cell.

This warning appears after any of the following warning messages: LIBG-128, LIBG-129, LIBG-130, and LIBG-131. For more information, refer to the man page of the issued warning.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-99.

WHAT NEXT

Specify the full function of the test cell.

LIBG-99 (error) The '%s' test cell has an incompatible non test

mode.

DESCRIPTION

This message indicates that the non test mode of the test cell is incompatible with the test attributes of the test cell.

This error is displayed for a cell in UNIGEN format after any of the following error messages: LIBG-158, LIBG-159, LIBG-160, and LIBG-161. For more information, refer to the man page of the issued error.

WHAT NEXT

Update the non test mode description or the test mode description to make them consistent.

EXAMPLES

```
cell(libg99) {
  area : 11;
  pin(D1 D2 D3) {
    direction : input;
    capacitance : 1;
  }
  pin(CP SCK1 SCK2) {
    direction : input;
    capacitance : 1;
  }
  pin(SI) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_falling;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "SCK2";
    }
  }
  pin(Q) {
    direction : output;
  }
  pin(Q2) {
    direction : output;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP SCK1";
    }
  }
```

```
    test_cell() {
      pin(D1 D2 D3 CP) {
        direction : input;
      }
      pin(SCK1) {
        direction : input;
        signal_type : "test_scan_clock_b";
      }
      pin(SCK2) {
        direction : input;
        signal_type : "test_scan_clock_a";
      }
      pin(SI) {
        direction : input;
        signal_type : "test_scan_in";
      }
      statetable("C D ", "Q") {
        table :  "R  H/L : - : H/L,\

 ~R   -  : - :  N";
      }
      pin(Q) {
        direction : output;
internal_node : "Q";
input_map : "CP D1";
        signal_type : "test_scan_out";
      }
      pin(Q2) {
        direction : output;
internal_node : "Q";
input_map : "CP D2";
        signal_type : "test_scan_out";
      }
    }
  }
```

In this case, the pin ‘Q’ generated error LIBG-161, which generated this error.

MESSAGE EXAMPLE

```
Error: Line 62, The ’libg99’ test cell has an incompatible non test mode. (LIBG-99)
```

LIBG-100 (warning) The ’%s’ port in the ’%s’ cell has both a function and a test attribute. The test_cell will be deleted.

DESCRIPTION

This message indicates that the specified port has both a function statement and a test attribute. For this particular test cell type, a port cannot have both a

function statement and a test attribute.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-101.

WHAT NEXT

Remove either the function statement or the test attribute to correctly specify the test_cell.

LIBG-101 (error) The '%s' port in the '%s' cell has both a function
and a test attribute.

DESCRIPTION

This messages is issued only for single-latch LSSD and muxed-latch scan cells. The port has both a function statement and a test attribute. For the particular test cell type, a port cannot have both a function statement and a test attribute.

A function statement can be a **function**, a **state_function**, or an **internal_node** attribute.

A test attribute can be a **test_scan_in**, a **test_scan_in_inverted**, a **test_scan_enable**, a **test_scan_enable_inverted**, a **test_scan_out**, a **test_scan_out_inverted** , a **test_scan_clock**, a **test_scan_clock_a**, a **test_scan_clock_b**, or a **test_clock**.

WHAT NEXT

If you can access the original technology library source file, remove either the function statement or the test attribute to correctly specify the test_cell.

EXAMPLES

```
cell(libg101) {
  area : 13;
  pin(D SDI) {
    direction : input;
    capacitance : 1;
  }
  pin(C SE) {
    direction : input;
    capacitance : 2;
  }
  pin(QN) {
```

```
      direction : output;
    }
    test_cell() {
      pin(D C) {
        direction : input;
      }
      pin(SDI) {
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(SE) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_enable";
      }
      statetable("D C", "QN") {
table : "L/H H : - : H/L,\

 -   L : - : N";
      }
      pin(QN) {
        direction : output;
inverted_output : TRUE;
internal_node : "QN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

In this case, the pin 'QN' has both an **internal_node** and a **test_scan_out_inverted** attributes.

MESSAGE EXAMPLE

```
Error: Line 152, The 'QN' port in the 'libg101' cell has both a function
        and a test attribute. (LIBG-101)
```

LIBG-102 (warning) The '%s' cell has more than one clock.

DESCRIPTION

The auxiliary clocked LSSD cell has more than one clock. This is not supported by DFT Compiler.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-103.

WHAT NEXT

This type of cell is not supported by DFT Compiler, so no further action is indicated.

LIBG-103 (error) The '%s' cell has more than one clock.

DESCRIPTION

The auxiliary clocked LSSD cell has more than one clock. This is not supported by DFT Compiler.

WHAT NEXT

This type of cell is not supported by DFT Compiler, so no further action is indicated.

EXAMPLES

```
cell(libg103) {
  area : 12;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CK,CK2,IH) {
    direction : input;
    capacitance : 1;
  }
  pin(A,B) {
    direction : input
      capacitance : 2;
  }
  pin(SI) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_falling;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "A";
    }
    timing() {
      timing_type : hold_falling;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "A";
    }
  }
  pin(Q) {
```

```
  direction : output;
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "CK IH";
  }
  timing() {
    timing_type : falling_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "B";
  }
}
pin(XQ) {
  direction : output;
}
test_cell(){
  pin(D,CK,CK2){
    direction : input;
  }
  pin(IH){
    direction : input;
    signal_type : "test_clock";
  }
  pin(SI){
    direction : input;
    signal_type : "test_scan_in";
  }
  pin(A){
    direction : input;
    signal_type : "test_scan_clock_a";
  }
  pin(B){
    direction : input;
    signal_type : "test_scan_clock_b";
  }
  ff("IQ","IQN"){
    clocked_on : "CK CK2";
    next_state : "D";
  }
  pin(Q){
    direction : output;
    function : "IQ";
    signal_type : "test_scan_out";
  }
  pin(XQ){
    direction : output;
    function : "IQN";
    signal_type : "test_scan_out_inverted";
  }
```

```
    }
  }
```

In this case, there are two clocks, ’CK’ and ’CK2’, which is not allowed.

MESSAGE EXAMPLE

Error: Line 162, The ’libg103’ cell has more than one clock. (LIBG-103)

LIBG-104 (warning) The ’%s’ pin of the ’%s’ design is not a clock pin
and should not be used in the ’related_pin’ of ’%s’ timing arc.

DESCRIPTION

By definition, a pin in the **related_pin** attribute of the timing group with the **timing_type setup_rising, setup_falling, hold_rising** or **hold_falling** should be a clock pin. It is treated as a warning only for backward compatibility.

WHAT NEXT

Check your library for a wrong pin in the **related_pin** attribute or for an incorrect **timing_type**.

EXAMPLES

```
cell(libg104) {
  area : 10;
  pin(CK) {
    direction : input;
    clock     : true;
    capacitance : 1.0;
  }
  pin(D) {
    direction : input ;
    capacitance : 1.0 ;
    timing() {
      related_pin : "CK";
      timing_type : setup_rising;
      intrinsic_fall : 1.0;
      intrinsic_rise : 1.0;
    }
    timing() {
      related_pin : "CK";
      timing_type : hold_rising;
      intrinsic_fall : 0.1;
      intrinsic_rise : 0.1;
    }
```

```
  }
  pin(P) {
    direction : input;
    capacitance : 1.0;
    timing() {
      related_pin : "CK";
      timing_type : setup_rising;
      intrinsic_rise : 0.0;
    }
  }
  ff ("IQ", "IQN") {
     next_state : "D";
     clocked_on : "CK";
     preset : "P";
 }
  pin(Q) {
    direction : output;
    function  : "IQ";
    timing() {
      related_pin : "P";
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
    }
  }
}
```

The timing group of the pin 'Q' contains the pin 'P' in the related_pin attribute. This caused the warning because the timing_type is **setup_rising**

MESSAGE EXAMPLE

```
Warning: Line 153, The 'P' pin of the 'libg104' design is not a clock pin
and should not be used in the 'related_pin' of 'setup' timing arc. (LIBG-104)
```

LIBG-105 (error) There is a missing timing arc between the '%s' and '%s' pins in the '%s' cell. A timing arc of the right timing_type is expected between the two specified pins of the cell.

DESCRIPTION

A timing arc of the right timing_type is expected between the two specified pins of the cell. For example, a timing arc with timing_type rising_edge/falling_edge is required from the clock/enable pin to the output pin. This error might be generated by a previous warning or error such as: LIBG-104.

WHAT NEXT

Specify or correct the timing arc to make the cell description complete.

EXAMPLES

```
cell(libg105) {
  area           : 10;
  pin(CK) {
    direction            : input;
    clock                : true;
    capacitance          : 1.0;
  }
  pin(D) {
    direction            : input;
    capacitance          : 1.0;
    timing() {
      related_pin        : "CK";
      timing_type        : setup_rising;
      intrinsic_fall     : 1.0;
      intrinsic_rise     : 1.0 ;
    }
    timing() {
      related_pin        : "CK";
      timing_type        : hold_rising;
      intrinsic_fall     : 0.0;
      intrinsic_rise     : 0.0;
    }
  }

  pin(P) {
    direction            : input;
    capacitance          : 1.0;
    timing() {
      related_pin        : "CK";
      timing_type        : setup_rising;
      intrinsic_rise     : 0.0;
    }
  }
  ff ("IQ", "IQN") {
     next_state : "D";
     clocked_on : "CK";
     preset : "P";
 }
  pin(Q) {
    direction            : output;
    function             : "IQ";
    timing() {
      related_pin        : "CK";
      timing_type        : rising_edge;
      intrinsic_rise     : 1.0;
      intrinsic_fall     : 1.0;
    }
  }
}
```

A timing group is missing in the pin 'Q' for the pin 'P'.

MESSAGE EXAMPLE

```
Error: Line 151, There is a missing timing arc between the 'P' and 'Q'
pins in the 'libg105' cell. A timing arc of the right timing_type
is expected between the two specified pins of the cell. (LIBG-105)
```

LIBG-106 (warning) The '%s' timing type is invalid between the two specified pins.

DESCRIPTION

The specified **timing_type** attribute is invalid between the pin that has the timing group and the pin in the **related_pin** attribute specified. It is most likely that you have specified a "combinational" timing arc from the clock, enable, clear, or preset pin to the output pin, or that the **timing_type** attribute is missing.

WHAT NEXT

Specify the correct timing_type attribute.

EXAMPLES

```
cell(libg106) {
  area           : 10;
  pin(CK) {
    direction            : input;
    clock                : true;
    capacitance          : 1.0;
  }
  pin(D) {
    direction            : input;
    capacitance          : 1.0;
    timing() {
      related_pin        : "CK";
      timing_type        : setup_rising;
      intrinsic_fall     : 1.0;
      intrinsic_rise     : 1.0;
    }
    timing() {
      related_pin        : "CK";
      timing_type        : hold_rising;
      intrinsic_fall     : 0.0;
      intrinsic_rise     : 0.0;
    }
  }
  pin(P) {
    direction            : input;
```

```
    capacitance          : 1.0;
    timing() {
      related_pin        : "CK";
      timing_type        : setup_rising;
      intrinsic_rise     : 0.0;
    }
  }
  ff ("IQ", "IQN") {
     next_state : "D";
     clocked_on : "CK";
     preset : "P";
 }
  pin(Q) {
    direction            : output;
    function             : "IQ";
    timing() {
      related_pin        : "CK";
      timing_type        : setup_rising;
      intrinsic_rise     : 1.0;
      intrinsic_fall     : 1.0
    }
  }
}
```

In this case, there is a ’setup_rising’ attribute between the output port ’Q’ and the clock ’CK’.

MESSAGE EXAMPLE

```
Warning: Line 151, The ’setup_rising’ timing type is invalid between the
two specified pins. (LIBG-106)
```

LIBG-107 (error) The complex state_function is not allowed in the ’%s’ test cell.

DESCRIPTION

The test cell has a port with a complex state_function. A complex state_function is any expression not equivalent to a buffer or an inverter.

Currently, complex state_functions are not supported in test cells.

WHAT NEXT

Either remove the state_function or make it into a buffer or an inverter.

EXAMPLES

```
  cell(libg107) {
```

```
    area : 21;
    pin(D1 D2) {
      direction : input;
      capacitance : 1;
    }
    pin(C1 C2 C3) {
      direction : input;
      capacitance : 2;
    }
    pin(Q1 Q2 Q2N) {
      direction : output;
    }
    pin(Q1N) {
      direction : output;
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "C2";
      }
    }
    test_cell() {
      pin(D1 C1 C3) {
        direction : input;
      }
      pin(D2) {
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(C2) {
        direction : input;
        signal_type : "test_scan_clock_a";
      }
      statetable ("C1 D1 C3", "Q1 Q2") {
        table : "H L/H - : H - : L/H -,\

                H - -   : L - : L -,\

                - -   H : L/H - : - L/H,\

                  - -   - : - - : N   N";
      }

      pin(Q1) {
        direction : output;
internal_node : "Q1";
      }
      pin(Q1N) {
        direction : output;
        state_function : "Q1'";
      }
      pin(Q2) {
        direction : output;
```

```
internal_node : "Q2";
        signal_type : "test_scan_out";
      }
      pin(Q2N) {
        direction : output;
/* This state_function is too complex, change it to a buffer/inverter*/
        state_function : "Q2' + C1";
        signal_type : "test_scan_out_inverted";
      }
    }
  }

}
```

EXAMPLE MESSAGE

```
Error: Line 134, The complex state_function is not allowed in the 'libg107' test ce
ll. (LIBG-107)
```

LIBG-108 (error) The three_state attribute is not allowed in the '%s' test cell.

DESCRIPTION

The test cell has a port with a three_state attribute.

Currently, the three_state attribute is not supported in test cells.

WHAT NEXT

Remove the three_state attribute from the test cell.

EXAMPLES

```
  cell(libg108) {
    area : 21;
    pin(D1 D2) {
      direction : input;
      capacitance : 1;
    }
    pin(C1 C2 C3) {
      direction : input;
      capacitance : 1;
    }
    pin(Q1 Q2 Q2N) {
      direction : output;
    }
    pin(Q1N) {
      direction : output;
```

```
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "C2";
      }
    }
    test_cell() {
      pin(D1 C1 C3) {
        direction : input;
      }
      pin(D2) {
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(C2) {
        direction : input;
        signal_type : "test_scan_clock_a";
      }
      statetable ("C1 D1 C3", "Q1 Q2") {
        table : "H L/H - : H - : L/H -,\

 H - - : L - : L -,\

                - -   H : L/H - : - L/H,\

                - -   - : - - : N   N";
      }

      pin(Q1) {
        direction : output;
internal_node : "Q1";
      }
      pin(Q1N) {
        direction : output;
        state_function : "Q1'";
      }
      pin(Q2) {
        direction : output;
internal_node : "Q2";
        signal_type : "test_scan_out";
      }
      pin(Q2N) {
        direction : output;
        state_function : "Q2'";
/* three_state attribute is not allowed in test_cell */
three_state : "C1";
        signal_type : "test_scan_out_inverted";
      }
    }
  }

}
```

EXAMPLE MESSAGE

```
Error: Line 169, The three_state attribute is not allowed in the 'libg108' test cel
l. (LIBG-108)
```

LIBG-109 (warning) Asynchronous specifications in the '%s' cell are incompletely specified.

DESCRIPTION

There is a set of input values for asynchronous inputs that causes more than one force_* condition to be true. The force_* conditions are not mutually exclusive; the cell is unspecified when more than one force_* condition is valid.

Design Compiler cannot support this cell and might generate invalid logic if the cell is used.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-110.

WHAT NEXT

You can put the attributes **dont_touch** and **dont_use** on the library cell to prevent this cell from being used and potentially generating invalid logic.

Alternatively, you can change the source technology library. Change the force_* expressions so they are mutually exclusive. There should be no input condition for which more than one force_* statement is valid.

LIBG-110 (warning) Asynchronous specifications in the '%s' cell are incomplete or are not mutually exclusive. The cell has been made a black box.

DESCRIPTION

There is a set of input values for asynchronous inputs that causes more than one force_* condition to be true.

The force_* conditions are not mutually exclusive; the cell is unspecified when more than one force_* condition is valid.

Design Compiler cannot support this cell; therefore, the cell has been made a black box.

WHAT NEXT

Change the force_* expressions so they are mutually exclusive. There should be no input condition for which more than one force_* statement is valid.

EXAMPLES

```
cell(libg110) {
  area : 10;
  pin(force11) {
    direction : input;
    capacitance : 1;
  }
  pin(force10) {
    direction : input;
    capacitance : 1;
  }
  pin(force01) {
    direction : input;
    capacitance : 1;
  }
  pin(force00) {
    direction : input;
    capacitance : 2;
  }
  pin(ck) {
    direction : input;
    capacitance : 2;
  }
  pin(next) {
    direction : input;
    capacitance : 2;
  }
  state("IQ","IQN") {
    next_state : "next";
    clocked_on : "ck";
    force_00   : "force00";
    force_01   : "force01";
    force_10   : "force10";
    force_11   : "force11";
  }
  statetable ("next ck ck* force00 force01 force10 force11", "out") {
    table : "- - - H L L L : - : L,\

     - - - L H L L : L/H : L,\

     - - - L L H L : - : H,\

     - - - L L L H : - : H,\

     L/H H L L L L L : - : L/H,\
```

```
    - L L L L L L : - : N,\

    - L H L L L L : - : N,\

    - H H L L L L : - : N";
  }

  pin(Q) {
    function : "IQ";
    internal_node : "out";
    direction : output;
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 111, Asynchronous specifications in the 'libg110' cell
are incomplete or are not mutually exclusive.
The cell has been made a black box. (LIBG-110)
```

LIBG-111 (warning) Design Compiler does not support the values for clear_preset_var? in the '%s' cell. The cell has been made a black box.

DESCRIPTION

The cell has invalid values (N, X or T) for clear_preset_var1 and clear_preset_var2.

Because of these values, Design Compiler cannot support the cell. The cell has been made a black box.

WHAT NEXT

Change the N, X or T value to a L or H value.

EXAMPLES

```
cell(libg111) {
area : 11;
pin(D) {
direction : input;
capacitance : 1;
}
pin(CP) {
direction : input;
```

```
capacitance : 1;
}
pin(CLR) {
direction : input;
capacitance : 1;
}
pin(SET) {
direction : input;
capacitance : 1;
}
ff("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
clear   : "CLR'";
preset   : "SET'";
clear_preset_var1 : X;
clear_preset_var2 : X;
}
pin(Q) {
direction : output;
function : "IQ";
timing() {
timing_type : rising_edge;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "CP";
}
            timing() {
timing_type : clear;
      timing_sense : positive_unate;
      intrinsic_fall : 1.0;
      fall_resistance : 0.1;
      related_pin : "CLR";
      }
            timing() {
      timing_type : preset;
      timing_sense : negative_unate;
      intrinsic_fall : 1.0;
      fall_resistance : 0.1;
      related_pin : "SET";
      }
}
pin(QN) {
direction : output;
function : "IQN";
timing() {
timing_type : rising_edge;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "CP";
}
```

```
            timing() {
      timing_type : preset;
      timing_sense : negative_unate;
      intrinsic_fall : 1.0;
      fall_resistance : 0.1;
      related_pin : "CLR";
      }
            timing() {
      timing_type : clear;
      timing_sense : positive_unate;
      intrinsic_fall : 1.0;
      fall_resistance : 0.1;
      related_pin : "SET";
      }
      }
}
```

EXAMPLES

```
Warning: Line 111, Design Compiler does not support the values for
        clear_preset_var? in the 'libg111' cell. The cell has been made a black box
. (LIBG-111)
```

LIBG-112 (error) The timing check condition represented in this timing group is not mutually exclusive with the timing check condition represented in the timing group on line %d.

DESCRIPTION

The timing check conditions represented by the 'when' string of all conditional period and pulse width timing checks should be mutually exclusive. A nonconditional timing check is assumed to have the implied '1' timing check condition (always **TRUE**). If timing check conditions are not mutually exclusive, Library Compiler cannot determine which timing check to use when the condition causes both timing check conditions to be evaluated **TRUE**.

WHAT NEXT

Check the 'when' strings of both timing groups, and make corrections necessary to eliminate duplicate nonconditional timing checks or other erroneous information. Also, ensure that there is no nonconditional timing check defined when at least one conditional timing check of the same pins and timing type is defined.

EXAMPLES

```
cell(libg112) {
```

```
area : 6.0;
pin(CLK) {
direction : input;
capacitance : 1.0;
minimum_period() {
            constraint : 99;
            when : " Q'";
            sdf_cond : "SIG_5 == 1'b1 ";
}
minimum_period() {
constraint : 99;
when : " Q'"
      sdf_cond : "SIG_5 == 1'b0 ";
}
}
pin(SET) {
direction : input;
capacitance : 1.0;
}
ff("IQ","IQN") {
next_state : "IQ'";
clocked_on : "CLK";
preset     : "SET'";
}
pin(Q) {
direction : output;
function : "IQ";
timing() {
timing_type : rising_edge;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "CLK";
}
timing() {
timing_type : preset;
timing_sense : negative_unate;
intrinsic_rise : 1.0;
rise_resistance : 0.1;
related_pin : "SET";
}
}
pin(QN) {
direction : output;
function : "IQN";
timing() {
timing_type : rising_edge;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "CLK";
}
timing() {
```

```
timing_type : clear;
timing_sense : positive_unate;
intrinsic_fall : 1.0;
fall_resistance : 0.1;
related_pin : "SET";
}
}
```

EXAMPLE MESSAGE

```
Error: Line 115, The timing check condition represented in this timing
        group is not mutually exclusive with the timing check condition
        represented in the timing group on line 120. (LIBG-112)
```

LIBG-113 (error) The timing check starting and ending conditions represented in this timing group are not mutually exclusive with the timing check starting and ending conditions represented in the timing group on line %d.

DESCRIPTION

One of the following two conditions must be satisfied between two conditional timing checks of the same pins:

1. The timing check starting conditions represented by the **when_start** or **when** string of all conditional timing checks (setup, hold, recovery, removal and skew) are mutually exclusive.
2. The timing check ending conditions represented by the **when_end** or **when** string of all conditional timing checks (setup, hold, recovery, removal and skew) are mutually exclusive.

A nonconditional timing check is assumed to have the implied ’1’ timing check starting and ending condition (always **TRUE**). If both starting and ending conditions are not mutually exclusive, Library Compiler cannot determine which timing check to use when the condition enables both conditional timing check conditions.

WHAT NEXT

Check the **when_start**, **when_end** and **when** strings of both timing groups and make any corrections necessary to eliminate duplicate nonconditional timing checks or other erroneous information. Also, ensure that there is no nonconditional timing check defined when at least one conditional timing check of the same pins and timing type

is defined.

```
  cell(libg113) {
    area : 10;
    pin(D) {
      direction : input;
      capacitance : 1;
      /* these two timing groups are not mutually exclusive */
      timing() {
        timing_type : setup_falling;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
      when : " MQ ";
      sdf_cond : " MQ == 1'b1 ";
        related_pin : "MC";
      }
      timing() {
        timing_type : setup_falling;
      when : " MQ ";
      sdf_cond : " MQ == 1'b1 ";
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        related_pin : "MC";
      }
    }
    pin(MC) {
      direction : input;
      capacitance : 2;
    }
    statetable ( "D CP", "Q ") {
table : "H/L  R : - : H/L,\

 -   ~R : - : N ";
    }

    pin (MQ) {
      direction : internal;
      inverted_output : FALSE;
      internal_node : "Q";
      input_map : "D MC MQ";
    }
    pin(Q) {
      direction : output;
      internal_node : "Q";
      input_map : "MQ MC Q";
      inverted_output : FALSE;
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "MC";
      }
    }
```

```
 }
```

EXAMPLE MESSAGE

```
Error: Line 116, The timing check starting and ending conditions
        represented in this timing group are not mutually exclusive with the
        timing check starting and ending conditions represented in the
        timing group on line 124. (LIBG-113)
```

LIBG-115 (warning) The when attribute uses '%s' pins that cannot be found in the %s %s.

DESCRIPTION

In a sequential cell, the following pins are allowed to appear in the **when** attribute of the **state-dependent** timing arc:

1) Pins used in **enable**, **enable_also**, and **data_in** in the **latch** group

2) Pins used in **clocked_on**, **clocked_on_also**, and **next_state** in the **ff** group for **timing_arc** with **timing_type** of **rising_edge/falling_edge**

This warning informs you that one of the previous restrictions has been violated.

WHAT NEXT

Check your **when** attribute, and correct any wrong information in the string or in the **timing_type**.

EXAMPLES

```
cell(libg115) {
  area : 9;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }
  pin(CD) {
    direction : input;
    capacitance : 2;
  }
  ff("IQ","IQN") {
    next_state : "D";
    clocked_on : "CP";
    clear   : "CD'";
```

```
  }
  pin(Q) {
    direction : output;
    function : "IQ";
    timing() {
      when : "CD";
      sdf_cond : "D==1'b1";
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
     timing() {
      timing_type : clear;
      timing_sense : positive_unate;
      intrinsic_fall : 1.0;
      fall_resistance : 0.1;
      related_pin : "CD";
    }
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 134, The when attribute uses 'CD' pins
        that cannot be found in the ff/latch group . (LIBG-115)
```

LIBG-116 (warning) No test_scan_in/test_scan_in_inverted signal types exist on the '%s' test_cell cell. Converting the entire cell to a black box.

DESCRIPTION

To be able to accept scan data, each test_cell must have either a **test_scan_in** or **test_scan_in_inverted** signal type.

This warning informs you that the indicated test_cell does not have the **test_scan_in** or **test_scan_in_inverted** signal types. Thus, the test_cell is not valid, and the entire cell has been converted to a black box.

There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. you can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-147.

WHAT NEXT

Check the library description to ensure that each test_cell has a **test_scan_in** or **test_scan_in_inverted** signal type. These signal types can be added within the test_cell using this syntax:

```
signal_type : test_scan_in (or test_scan_in_inverted)
```

LIBG-117 (warning) No test_scan_out/test_scan_out_inverted signal types exisit on the '%s' test_cell cell. Converting the entire cell to a black box.

DESCRIPTION

To be able to scan out data, each test_cell must have either a **test_scan_out** or a **test_scan_out_inverted** signal type.

This warning informs you that the indicated test_cell has neither the **test_scan_out** nor the **test_scan_out_inverted** signal types. Thus, the test_cell is not valid, and the entire cell is converted to a black box.

There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-148.

WHAT NEXT

Check the library description to ensure that each test_cell either has a **test_scan_out** or a **test_scan_out_inverted** signal type. These signal types can be added within the test_cell using this syntax:

```
signal_type : test_scan_out (or test_scan_out_inverted)
```

LIBG-118 (warning) The clocked_on_also function on the '%s' port for

test_cell on the '%s' cell is not specified on the correct pin. Converting the entire cell to a black box.

DESCRIPTION

The **clocked_on_also** function for this test_cell is not specified on the correct pin. This function needs to be specified on the clock of the slave stage of a master-slave configuration.

This warning informs you that the test_cell pointed to has the **clocked_on_also** function specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. Other tools will not be able to use this cell if it is made into a black box.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-149.

WHAT NEXT

Check the library description to ensure that each test_cell has specified the **clocked_on_also** function. To determine the correct function:

* Create a cell with the non test mode as the functional part of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

LIBG-119 (warning) The test_scan_clock_b signal type on the '%s' port for test_cell on the '%s' cell is not specified on the correct pin. Converting the entire cell to a black box.

DESCRIPTION

The **test_scan_clock_b** signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the clock of the slave stage of an LSSD configuration.

This warning informs you that the test_cell pointed to has the **test_scan_clock_b** signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. Other tools will not be able to use this

cell if it is made into a black box.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-150.

WHAT NEXT

Check the library description to ensure that each test_cell has specified the **test_scan_clock_b** signal type.

LIBG-120 (warning) The test_scan_in signal type on the '%s' port for test_cell on the '%s' cell is not specified on the correct pin. Converting the entire cell to a black box.

DESCRIPTION

The **test_scan_in** signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin that takes in the scan data. All scan types and, thus, all test_cells need to have either the **test_scan_in** or **test_scan_in_inverted** signal type.

This warning informs you that the test_cell pointed to has the **test_scan_in** signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box . There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-151.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the **test_scan_in** signal type.

LIBG-121 (warning) The test_scan_in_inverted signal type on the '%s' port for

test_cell on the '%s' cell is not specified on the correct pin. Converting the entire cell to a black box.

DESCRIPTION

The **test_scan_in_inverted** signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin that takes in the scan data. All scan types and, thus, all test_cells need to have either the **test_scan_in** or **test_scan_in_inverted** signal type.

This warning informs you that the test_cell pointed to has the **test_scan_in_inverted** signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-152.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the **test_scan_in_inverted** signal type.

LIBG-122 (warning) The test_scan_enable signal type on the '%s' port for test_cell on the '%s' cell is not specified on the correct pin. Converting the entire cell to a black box.

DESCRIPTION

The **test_scan_enable** signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin that switches the input mode of the cell between test and mission mode. Only multiplexed flip-flop requires this signal type. This signal type can also be used in clocked scan cells.

This warning informs you that the test_cell pointed to has the **test_scan_enable** signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-153.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the **test_scan_enable** signal type.

LIBG-123 (warning) The test_scan_enable_inverted signal type on the '%s' port for test_cell on the '%s' cell is not specified on the correct pin. Converting the entire cell to a black box.

DESCRIPTION

The **test_scan_enable_inverted** signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin that switches the input mode of the cell between test and mission mode. Only, multiplexed flip-flop requires this signal type. This signal type can also be used in clocked scan cells.

This warning informs you that the test_cell pointed to has the **test_scan_enable_inverted** signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-154.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the **test_scan_enable_inverted** signal type.

LIBG-124 The test_scan_clock signal type on the '%s' port for test_cell on the '%s' cell is not specified on the correct pin.

Converting the entire cell to a black box.

DESCRIPTION

The **test_scan_clock** signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the scan clock for clocked scan cells.

This warning informs you that the test_cell pointed to has the **test_scan_clock** signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-155.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the **test_scan_clock** signal type.

LIBG-125 warning) The test_scan_clock_a signal type on the '%s' port for test_cell on the '%s' cell is not specified on the correct pin. Converting the entire cell to a black box.

DESCRIPTION

The **test_scan_clock_a** signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the clock of the master stage of an LSSD configuration.

This warning informs you that the test_cell pointed to has the **test_scan_clock_a** signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools will not be able to use this this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-156.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the **test_scan_clock_a** signal type.

LIBG-126 (warning) The test_clock signal type on the '%s' port for test_cell on the '%s' cell is not specified on the correct pin. Converting the entire cell to a black box.

DESCRIPTION

The **test_clock** signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the clock used for ATPG capture in auxiliary clock lssd cells.

This warning informs you that the test_cell pointed to has the **test_clock** signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-157.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the **test_clock** signal type.

LIBG-127 (warning) The '%s' clocked test cell is not valid because it has a master-slave cell as its nontest mode. Converting the entire cell to a black box.

DESCRIPTION

A clocked test cell has the following characteristics:

- signal types : test_scan_in/test_scan_in_inverted, test_scan_enable/ test_scan_enable_inverted (optional), test_scan_clock, test_scan_out/test_scan_out_inverted

- nontest modes : flip-flop or latch

This warning informs you that the signal types identify this cell as a clocked scan test cell, but it does not have a flip-flop or latch as its nontest mode. It is currently specified as a master-slave cell. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-174.

WHAT NEXT

Check the library description to ensure that nontest modes and signal types are correctly pointed to by the test_cell. To determine why the nontest function is not one of the previous types,

* Create a cell with the nontest mode as the functional part
  of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

LIBG-128 (warning) Invalid nontest mode for test_cell on the '%s' cell; there are more than 2 sequential elements. Converting the entire cell to a black box.

DESCRIPTION

The nontest mode for test_cells must be one of the following:

- A single flip-flop
- A single latch
- A single master-slave latch configuration using clocked_on and clocked_on_also

This warning informs you that the nontest mode of the test_cell has more than 2

distinct sequential elements, so the test_cell does not fit the previous requirements. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

WHAT NEXT

Check the library description to ensure that each test_cell has properly specified the correct nontest mode. To determine why there are multiple sequential elements in this description,

* Create a cell with the nontest mode as the functional part
  of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

LIBG-129 (warning) Invalid nontest mode for test_cell on the '%s' cell.
This mode describes a ganged cell.

DESCRIPTION

The nontest mode for test_cells must be one of the following:

- A single flip-flop
- A single latch
- A single master-slave latch configuration using clocked_on and clocked_on_also

This warning informs you that the nontest mode of the test cell is a ganged cell, and it does not fit the previous requirements. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

WHAT NEXT

Check the library description to ensure that each test_cell does not specify a

ganged cell as its nontest mode. Ganged cells can be recognized by the keywords ff_bank or latch_bank.

LIBG-130 (warning) The nontest mode for test_cell on the '%s' cell is invalid.
The '%s' slave port does not directly feed the output.

DESCRIPTION

The nontest mode for test_cells must be one of the following:

- A single flip-flop
- A single latch
- A single master-slave latch configuration using clocked_on and clocked_on_also

This warning informs you that in nontest mode of the test cell, the slave does not directly feed the output. This means that it is not a master-slave latch configuration that the DFT Compiler supports. Thus, the test_cell is not valid, and the entire cell is a black box.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-160.

WHAT NEXT

Check the library description to ensure that the nontest mode of the test_cell is correctly specified. If you are using a master-slave configuration as the nontest mode, the only accepted description is the state description using

clocked_on : <master clock>
clocked_on_also : <slave clock>

LIBG-131 (warning) The nontest mode for test_cell on the '%s' cell is invalid.
The '%s' state pin is not a latch for a master-slave configuration.

DESCRIPTION

The nontest mode for test_cells must be one of the following:

```
        - A single flip-flop
        - A single latch
        - A single master-slave latch configuration using clocked_on
  and clocked_on_also
```

This warning informs you that the nontest mode of the test cell is an incorrect master-slave description. This stage of the master-slave configuration is not a latch, and it does not fit the previous requirements. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-161.

WHAT NEXT

Check the library description to ensure that the nontest mode of the test_cell is correctly specified. If you are using a master-slave configuration as the nontest mode, the only accepted description is the state description using clocked_on : <master clock> clocked_on_also : <slave clock>

LIBG-132 (warning) The test cell for auxiliary clocked lssd '%s' cell is not valid because its nontest mode is not a flip-flop.

DESCRIPTION

An auxiliary clocked lssd test_cell has the following characteristics:

```
        - signal types : test_scan_in/test_scan_in_inverted,
 test_scan_out/test_scan_out_inverted,
 test_scan_clock_a, test_scan_clock_b, test_clock
        - nontest mode : flip-flop
```

This warning informs you that the signal types point to this auxiliary clocked lssd test_cell, but it does not have a flip-flop as its nontest mode. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-175.

WHAT NEXT

Check the library description to ensure that nontest modes and signal types are correctly pointed to by the test_cell. To determine why the nontest function is not one of the previous types,

* Create a cell with the nontest mode as the functional part of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

LIBG-133 (warning) The test_cell on the '%s' cell cannot have more than one test_scan_in/test_scan_in_inverted signal type. This happens on the '%s' port.

DESCRIPTION

Each test_cell must have only one test_scan_in or test_scan_in_inverted signal type. This signal type is specified on the pin that is used to take scan data into the cell.

This warning informs you that the test_cell pointed to has multiple test_scan_in(test_scan_in_inverted) signal types. The message points to the second port that has this signal type. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-162.

WHAT NEXT

Check the library description to ensure that each test_cell has only one test_scan_in or test_scan_in_inverted signal type.

LIBG-134 (warning) The '%s' port in test_cell on the '%s' cell has a test_scan_out signal type on an inverted output.

DESCRIPTION

The test_scan_out signal type can only be specified on a noninverted output. If the output is inverted, the proper signal type should be test_scan_out_inverted. This signal type specifies the polarity of the port with respect to the state.

This warning informs you that the test_cell pointed to has the test_scan_out signal type specified on an inverted output. When reading a .db library, Library Compiler ignores the scan_out attribute and creates the functional description of the cell using the function statement. In other words, that output is inverted in the functional description.

The same problem in a .lib library causes an error. See the .lib example for LIBG-163.

WHAT NEXT

The default behavior of selecting the function over the signal_type to determine the inversion of the output is be correct in most cases.

Check the library description to ensure that the test_scan_out signal type is only placed on noninverted outputs. To determine if this is an inverted or noninverted output,

* Create a cell with the nontest mode as the functional part
  of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

In the report_lib command's report, an inverted output is not a state if it does not have N. Instead, the output contains an inversion of the state pin.

LIBG-135 (warning) The '%s' port in test_cell on the '%s' cell has a test_scan_out_inverted signal type on a noninverted output.

DESCRIPTION

The test_scan_out_inverted signal type can only be specified on an inverted output. If the output is noninverted, the proper signal type should be test_scan_out. This

signal type specifies the polarity of the port with respect to the state.

This warning informs you that the test_cell pointed to has the test_scan_out signal type specified on an inverted output. When reading a .db library, the Library Compiler ignores the scan_out_inverted attribute and creates the functional description of the cell using the function statement. In other words, that output is noninverted in the functional description.

The same problem in a .lib library causes an error. See the .lib example for LIBG-164.

WHAT NEXT

The default behavior of selecting the function over the signal_type to determine the inversion of the output is correct in most cases.

Check the library description to ensure that the test_scan_out_inverted signal type is only placed on inverted outputs. To determine if this is an inverted or noninverted output,

* Create a cell with the nontest mode as the functional part
  of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

In the report_lib command’s report, an inverted output is not a state if it does not have N. Instead, the output contains an inversion of the state pin.

LIBG-136 (warning) The test cell on the ’%s’ cell cannot have more than one test_scan_enable or test_scan_enable_inverted signal type. This happens on the ’%s’ port.

DESCRIPTION

Each test_cell must have only one test_scan_enable or test_scan_enable_inverted signal type. This signal type is specified on the pin that is used to select between scan and mission mode operation of the cell.

This warning informs you that the test_cell pointed to has multiple test_scan_enable(test_scan_enable_inverted) signal types. The message points to the second port that has this signal type. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-165.

WHAT NEXT

Check the library description to ensure that each test_cell has only one test_scan_enable or test_scan_enable_inverted signal type.

LIBG-137 (warning) The test_scan_clock '%s' port in test_cell on the '%s' cell does not have an active sense.

DESCRIPTION

The test_scan_clock must have an active sense in the full cell description. The Library Compiler determines the active sense by checking the function of the full cell. The test_scan_clock is the scan clock in the clocked scan type.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell is recognized. Both the test_cell and the entire cell are converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error.

WHAT NEXT

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell,

* Create a cell with the nontest mode as the functional part of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

LIBG-138 (warning) The test_scan_clock_a '%s' port in test_cell

on the '%s' cell
 does not have an active sense.

DESCRIPTION

The test_scan_clock_a must have an active sense in the full cell description. The Library Compiler determines the active sense by checking the function of the full cell. The test_scan_clock_a is the scan clock for the master stage of the LSSD scan style.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell is recognized. Both the test_cell and the entire cell are converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error.

WHAT NEXT

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell,

* Create a cell with the non test mode as the functional part
  of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

LIBG-139 (warning) The test_scan_clock_b '%s' port in test_cell on the '%s' cell
 does not have an active sense.

DESCRIPTION

The test_scan_clock_b must have an active sense in the full cell description. The Library Compiler determines the active sense by checking the function of the full cell. The test_scan_clock_a is the scan clock for the slave stage of the LSSD scan style.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell is recognized. Both the test_cell and the entire cell are converted to a black box. There is functional information missing, and other tools

cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error.

WHAT NEXT

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell,

* Create a cell with the nontest mode as the functional part
  of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

LIBG-140 (warning) The test_clock '%s' port in test_cell on the '%s' cell does
not have an active sense.

DESCRIPTION

The test_clock must have an active sense in the full cell description. The Library Compiler determines the active sense by checking the function of the full cell. The test_clock is the capture clock used by ATPG in the auxiliary clocked lssd scan style.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell is recognized. Both the test_cell and the entire cell are converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error.

WHAT NEXT

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell,

* Create a cell with the nontest mode as the functional part

```
  of the cell.
* Compile this cell.
* Issue the following command:

     report_lib -table <library name> <cell name>
```

LIBG-141 (warning) The '%s' port in test_cell for the '%s' cell has an invalid signal type %s.

DESCRIPTION

The valid signal_types in test_cells are

- test_scan_in
- test_scan_in_inverted
- test_scan_enable
- test_scan_enable_inverted
- test_scan_out
- test_scan_out_inverted
- test_scan_clock
- test_scan_clock_a
- test_scan_clock_b
- test_clock

This warning informs you that the port in the test_cell pointed to has a signal_type other than the ones listed previously. Thus, the test_cell is not valid, and the entire cell is converted to a black box.

WHAT NEXT

Check the test_cell pointed to, and change the invalid signal_type.

LIBG-142 (warning) The LSSD test_cell for the '%s' cell has neither a test_scan_clock_b signal type nor a master-slave configuration as its non test mode.

DESCRIPTION

LSSD scan styles must have the following test_cell characteristics:

```
   clocked lssd
```

```
- signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
test_scan_out_inverted, test_scan_clock_a, test_scan_clock_b
- nontest mode: flip_flop
   auxiliary clock lssd
- signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
test_scan_out_inverted, test_scan_clock_a, test_scan_clock_b,
test_clock
- nontest mode : flip_flop
   single-latch lssd
- signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
test_scan_out_inverted, test_scan_clock_a, test_scan_clock_b
- nontest mode: latch
   single-latch lssd
- signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
test_scan_out_inverted, test_scan_clock_a,
test_scan_clock_b (optional)
- nontest mode: master-slave (clocked_on & clocked_on_also)
```

This warning informs you that the other signal types point to the fact that this is an lssd scan style because it has test_scan_in or test_scan_in_inverted, test_scan_out or test_scan_out_inverted, and test_scan_clock_a signal types. However, it is invalid because it has neither a test_scan_clock_b signal type nor a master-slave configuration as its nontest mode. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-171.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the nontest modes and signal types in the test_cell pointed to. If you do not understand why the nontest function is not one of the previous types,

* Create a cell with the nontest mode as the functional part
  of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

In the report_lib command’s report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

LIBG-144 (warning) The test_cell for the ’%s’ cell is not valid because

it has missing or extra test signals.

DESCRIPTION

The supported scan styles must have the following test_cell characteristics:

```
   multiplexed flip-flop
- signal types : test_scan_in/test_scan_in_inverted, test_scan_enable/
test_scan_enable_inverted, test_scan_out/test_scan_out_inverted
- nontest mode : flip-flop, master slave latch pair, or latch
   clocked scan
- signal types : test_scan_in/test_scan_in_inverted, test_scan_enable/
test_scan_enable_inverted (optional), test_scan_clock,
test_scan_out/test_scan_out_inverted
- nontest modes : flip-flop or latch
   clocked lssd
        - signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
                test_scan_out_inverted, test_scan_clock_a, test_scan_clock_b
        - nontest mode: flip-flop
   auxiliary clock lssd
        - signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
                test_scan_out_inverted, test_scan_clock_a, test_scan_clock_b,
                test_clock
        - nontest mode : flip-flop
   single-latch lssd
        - signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
                test_scan_out_inverted, test_scan_clock_a, test_scan_clock_b
        - nontest mode: latch
   single-latch lssd
        - signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
                test_scan_out_inverted, test_scan_clock_a, test_scan_clock_b
        - nontest mode: latch
   single-latch lssd
        - signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
                test_scan_out_inverted, test_scan_clock_a,
                test_scan_clock_b (optional)
        - nontest mode: master-slave (clocked_on & clocked_on_also)
```

This warning informs you that the other signal types do not correspond to one of the previously supported scan styles. Because there are extra or missing signal types, this test_cell is not valid, and the entire cell is a black box.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-172.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the nontest modes and signal types in the test_cell pointed to. If you do not understand why the nontest function is not one of the previous types,

* Create a cell with the non test mode as the functional part
  of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by checking their functional description.

LIBG-145 (warning) Cannot derive full function based on test_cell on the '%s' cell in a library with DPCM vendor specific delay model.

DESCRIPTION

The Library Compiler generates a functional description of the entire cell based on the information in the test_cell. However, if the library is a DPCM library, no full function description will be generated.

This warning is not issued when reading a .db library.

WHAT NEXT

Fill the full function with state table description.

LIBG-146 (warning) Cannot derive full function based on test_cell on the '%s' cell due to previous warnings or errors.

DESCRIPTION

The Library Compiler generates a functional description of the entire cell based on the information in the test_cell. However, if there are warnings or errors in the test_cell, a functional description of the entire cell cannot be generated.

This warning informs you that the test_cell pointed to has previous errors or warnings. Thus, the test_cell is not valid, and the entire cell is a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable **read_db_lib_warnings** to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-173.

WHAT NEXT

Fix the previous problems in order to recognize both the test_cell and full cell functionality. You might have to add a state table description of the entire cell.

LIBG-147 (error) No test_scan_in/test_scan_in_inverted signal types exist on the '%s' test_cell cell.

DESCRIPTION

Each test_cell must have either a test_scan_in or test_scan_in_inverted signal type to be valid. Otherwise, this cell cannot accept scan data.

This warning informs you that the test_cell pointed to does not have the test_scan_in or test_scan_in_inverted signal types. Thus, the test_cell is not valid, and the entire cell is converted to a black box.

There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell has a **test_scan_in** or **test_scan_in_inverted** signal type. These signal types can be added within the test_cell using the syntax:

```
signal_type : test_scan_in [ or test_scan_in_inverted]
```

EXAMPLES

```
    cell(libg147) {
      area : 10;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(C) {
direction : input;
capacitance : 2;
      }
      pin(D2) {
direction : input;
capacitance : 1;
      }
      pin(C2) {
direction : input;
capacitance : 2;
```

```
      }
      pin(C3) {
direction : input;
capacitance : 1;
      }
      pin(MQ) {
direction : internal;
internal_node : "MQ";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "C C2";
}
      }
      pin(Q) {
direction : output;
internal_node : "SQ";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "C C3";
}
      }
      pin(QN) {
direction : output;
state_function : "(Q)'";
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "C C3";
}
      }
      statetable("C D C2 C3 D2", "MQ SQ") {
table :  "R  H/L L L  -  : -   - : H/L H/L,\

              ~R   -  - H  -  : H/L - :  -  H/L,\

              ~R   -  - L  -  : -   - :  -  N,\

               R   -  H -  -  : -   - :  X  X,\

               R   -  - H  -  : -   - :  X  X,\

              ~R   -  H - H/L : -   - : H/L -,\

              ~R   -  L -  -  : -   - :  N  -";
```

```
      }
      test_cell() {
pin(D) {
  direction : input;
}
pin(C) {
  direction : input;
  capacitance : 2;
  signal_type : "test_scan_clock";
}
pin(D2) {
/* missing test_scan_in signal_type */
  direction : input;
}
pin(C2) {
  direction : input;
  capacitance : 2;
  signal_type : "test_scan_clock_a";
}
pin(C3) {
  direction : input;
  capacitance : 1;
  signal_type : "test_scan_clock_b";
}
ff ("IQ","IQN") {
  next_state : "D";
  clocked_on : "C";
}
pin(Q) {
  direction : output;
  function : "IQ";
  signal_type : "test_scan_out";
}
pin(QN) {
  direction : output;
  function : "IQN";
  signal_type : "test_scan_out_inverted";
}
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 177, No test_scan_in/test_scan_in_inverted signal
        types exist on the 'libg147' test_cell cell. (LIBG-147)
```

LIBG-148 (error) No test_scan_out/test_scan_out_inverted signal

types exist on the '%s' test_cell cell.

DESCRIPTION

Each test_cell must have either a test_scan_out or test_scan_out_inverted signal type in order to be valid. Otherwise, this cell cannot scan out data.

This warning informs you that the test_cell pointed to does not have the test_scan_out or test_scan_out_inverted signal types. Thus, the test_cell is not valid, and the entire cell is converted to a black box.

There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell has a test_scan_out or test_scan_out_inverted signal type. These signal types can be added within the test_cell using the syntax:

```
signal_type : test_scan_out [ or test_scan_out_inverted]
```

EXAMPLES

```
    cell(libg148) {
      area : 9;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(C) {
direction : input;
capacitance : 1;
      }
      pin(SI) {
direction : input;
capacitance : 1;
      }
      pin(SE) {
direction : input;
capacitance : 2;
      }

      pin(Q) {
direction : output;
inverted_output : FALSE;

      }
      pin(QN) {
direction : output;
inverted_output : TRUE;
      }
      test_cell() {
```

```
pin(D) {
  direction : input;
}
pin(C) {
  direction : input;
}
pin(SI) {
  direction : input;
  signal_type : "test_scan_in";
}
pin(SE) {
  direction : input;
  signal_type : "test_scan_enable";
}

ff ("IQ","IQN") {
  next_state : "D";
  clocked_on : "C";
}

pin(Q) {
  direction : output;
  function : "IQ";
  /*      signal_type : "test_scan_out"; */
}
pin(QN) {
  direction : output;
  function : "IQN";
  /*      signal_type : "test_scan_out_inverted";*/
}
      }
    }
```

EXAMPLE MESSAGE

```
Error: Line 139, No test_scan_out/test_scan_out_inverted signal
        types exist on the 'libg148' test_cell cell. (LIBG-148)
```

LIBG-149 (error) The clocked_on_also function on the '%s' port for test_cell on the '%s' cell is not specified on the correct pin.

DESCRIPTION

The **clocked_on_also** function for this test_cell is not specified on the correct pin. This function needs to be specified on the clock of the slave stage of a master-slave configuration.

This warning informs you that the test_cell pointed to has the **clocked_on_also**

function specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly used the **clocked_on_also** function. To determine the correct function,

* Create a cell with the nontest mode as the functional part of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

LIBG-150 (error) The test_scan_clock_b signal type on the '%s' port for test_cell on the '%s' cell is not specified on the correct pin.

DESCRIPTION

The test_scan_clock_b signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the clock of the slave stage of an LSSD configuration.

This warning informs you that the test_cell pointed to has the test_scan_clock_b signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the test_scan_clock_b signal type.

EXAMPLES

```
cell(libg150) {
  area : 13;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(C) {
    direction : input;
    capacitance : 2;
  }
```

```
pin(D2) {
  direction : input;
  capacitance : 1;
}
pin(C2) {
  direction : input;
  capacitance : 2;
}
pin(C3) {
  direction : input;
  capacitance : 1;
}
pin(MQ) {
  direction : internal;
  internal_node : "MQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 0.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C2";
  }
}
pin(Q) {
  direction : output;
  internal_node : "SQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
pin(QN) {
  direction : output;
  state_function : "(Q)'";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
statetable("C D C2 C3 D2", "MQ SQ") {
  table :  "R  H/L L L  -  : -   - : H/L H/L,\

           ~R   -  - H  -  : H/L - :  -  H/L,\

           ~R   -  - L  -  : -   - :  -  N,\
```

```
                R   -  H -  -  : -   - :  X  X,\

                R   -  - H  -  : -   - :  X  X,\

               ~R   -  H - H/L : -   - : H/L -,\

               ~R   -  L -  -  : -   - :  N  -";
    }
    test_cell() {
      pin(D) {
        direction : input;
      }
      pin(C) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_clock_b";
      }
      pin(D2) {
        direction : input;
      }
      pin(C2) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_clock_a";
      }
      pin(C3) {
        direction : input;
        capacitance : 1;
      }
      ff ("IQ","IQN") {
        next_state : "D";
        clocked_on : "C";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 181, The test_scan_clock_b signal type on the 'C' port for
         test_cell on the 'libg150' cell is not specified on the correct pin.(LIBG-
150)
```

LIBG-151 (error) The test_scan_in signal type on the '%s' port for
test_cell on the '%s' cell is not specified on the correct pin.

DESCRIPTION

The **test_scan_in** signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin that takes in the scan data. All scan types, and therefore, all test_cells need to have either the **test_scan_in** or **test_scan_in_inverted** signal type.

This warning informs you that the test_cell pointed to has the **test_scan_in** signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the test_scan_in signal type.

EXAMPLES

```
cell(libg151) {
  area : 13;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(C) {
    direction : input;
    capacitance : 2;
  }
  pin(D2) {
    direction : input;
    capacitance : 1;
  }
  pin(C2) {
    direction : input;
    capacitance : 2;
  }
  pin(C3) {
    direction : input;
    capacitance : 1;
  }
  pin(MQ) {
    direction : internal;
    internal_node : "MQ";
    timing() {
      timing_type : rising_edge;
```

```
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "C C2";
    }
  }
  pin(Q) {
    direction : output;
    internal_node : "SQ";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "C C3";
    }
  }
  pin(QN) {
    direction : output;
    state_function : "(Q)'";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "C C3";
    }
  }
  statetable("C D C2 C3 D2", "MQ SQ") {
    table :  "R  H/L L L  -  : -   - : H/L H/L,\

             ~R   -  - H  -  : H/L - :  -  H/L,\

             ~R   -  - L  -  : -   - :  -  N,\

              R   -  H -  -  : -   - :  X  X,\

              R   -  - H  -  : -   - :  X  X,\

             ~R   -  H - H/L : -   - : H/L -,\

             ~R   -  L -  -  : -   - :  N  -";
  }
  test_cell() {
    pin(D) {
      direction : input;
    }
    pin(C) {
      direction : input;
      capacitance : 2;
      signal_type : "test_scan_in";
    }
```

```
      pin(D2) {
        direction : input;
      }
      pin(C2) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_clock_a";
      }
      pin(C3) {
        direction : input;
        capacitance : 1;
        signal_type : "test_scan_clock_b";
      }
      ff ("IQ","IQN") {
        next_state : "D";
        clocked_on : "C";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

In this case the pin 'C' is a clock and should not have a test_scan_in signal_type attribute. The test_scan_in should be on the pin 'D2'.

EXAMPLE MESSAGE

```
Error: Line 182, The test_scan_in signal type on the 'C' port for
test_cell on the 'libg151' cell is not specified on the correct pin. (LIBG-151)
```

LIBG-152 (error) The test_scan_in_inverted signal type on the '%s' port for test_cell on the '%s' cell is not specified on the correct pin.

DESCRIPTION

The test_scan_in_inverted signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin which takes in the scan data. All scan types, and all test_cells need to have either the test_scan_in or test_scan_in_inverted signal type.

This warning informs you that the test_cell pointed to has the test_scan_in_inverted

signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools will not be able to use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the **test_scan_in_inverted** signal type.

EXAMPLES

```
cell(libg152) {
  area : 13;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(C) {
    direction : input;
    capacitance : 2;
  }
  pin(D2) {
    direction : input;
    capacitance : 1;
  }
  pin(C2) {
    direction : input;
    capacitance : 2;
  }
  pin(C3) {
    direction : input;
    capacitance : 1;
  }
  pin(MQ) {
    direction : internal;
    internal_node : "MQ";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "C C2";
    }
  }
  pin(Q) {
    direction : output;
    internal_node : "SQ";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
```

```
    related_pin : "C C3";
  }
}
pin(QN) {
  direction : output;
  state_function : "(Q)'";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
statetable("C D C2 C3 D2", "MQ SQ") {
  table :  "R  H/L L L  -  : -   - : H/L H/L,\

           ~R   -  - H  -  : H/L - :  -  H/L,\

           ~R   -  - L  -  : -   - :  -  N,\

            R   -  H -  -  : -   - :  X  X,\

            R   -  - H  -  : -   - :  X  X,\

           ~R   -  H - H/L : -   - : H/L -,\

           ~R   -  L -  -  : -   - :  N  -";
}
test_cell() {
  pin(D) {
    direction : input;
  }
  pin(C) {
    direction : input;
    capacitance : 2;
    signal_type : "test_scan_in_inverted";
  }
  pin(D2) {
    direction : input;
  }
  pin(C2) {
    direction : input;
    capacitance : 2;
    signal_type : "test_scan_clock_a";
  }
  pin(C3) {
    direction : input;
    capacitance : 1;
    signal_type : "test_scan_clock_b";
  }
  ff ("IQ","IQN") {
    next_state : "D";
    clocked_on : "C";
```

```
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

In this case the pin ’C’ is a clock and should not have a test_scan_in_inverted signal_type attribute. The test_scan_in_inverted should be on the pin ’D2’.

EXAMPLE MESSAGE

```
Error: Line 181, The test_scan_in_inverted signal type on the ’C’ port for
        test_cell on the ’libg152’ cell is not specified on the correct pin. (LIBG-
152)
```

LIBG-153 (error) The test_scan_enable signal type on the ’%s’ port for test_cell on the ’%s’ cell is not specified on the correct pin.

DESCRIPTION

The test_scan_enable signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin that switches the input mode of the cell between test and mission mode. Only, a multiplexed flip-flop requires this signal type. This signal type can also be used in clocked scan cells.

This warning informs you that the test_cell pointed to has the test_scan_enable signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the **test_scan_enable** signal type.

EXAMPLES

```
  cell(libg153) {
    area : 13;
```

```
pin(D) {
  direction : input;
  capacitance : 1;
}
pin(C) {
  direction : input;
  capacitance : 2;
}
pin(D2) {
  direction : input;
  capacitance : 1;
}
pin(C2) {
  direction : input;
  capacitance : 2;
}
pin(C3) {
  direction : input;
  capacitance : 1;
}
pin(MQ) {
  direction : internal;
  internal_node : "MQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C2";
  }
}
pin(Q) {
  direction : output;
  internal_node : "SQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
pin(QN) {
  direction : output;
  state_function : "(Q)'";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
```

```
  }
  statetable("C D C2 C3 D2", "MQ SQ") {
    table :  "R  H/L L L  -  : -   - : H/L H/L,\

              ~R   -  - H  -  : H/L - :  -  H/L,\

              ~R   -  - L  -  : -   - :  -  N,\

               R   -  H -  -  : -   - :  X  X,\

               R   -  - H  -  : -   - :  X  X,\

              ~R   -  H - H/L : -   - : H/L -,\

              ~R   -  L -  -  : -   - :  N  -";
  }
  test_cell() {
    pin(D) {
      direction : input;
    }
    pin(C) {
      direction : input;
      capacitance : 2;
      signal_type : "test_scan_enable";
    }
    pin(D2) {
      direction : input;
    }
    pin(C2) {
      direction : input;
      capacitance : 2;
      signal_type : "test_scan_clock_a";
    }
    pin(C3) {
      direction : input;
      capacitance : 1;
      signal_type : "test_scan_clock_b";
    }
    ff ("IQ","IQN") {
      next_state : "D";
      clocked_on : "C";
    }
    pin(Q) {
      direction : output;
      function : "IQ";
      signal_type : "test_scan_out";
    }
    pin(QN) {
      direction : output;
      function : "IQN";
      signal_type : "test_scan_out_inverted";
    }
  }
}
```

The pin ’C’ is a clock and should not have a test_scan_enable signal_type attribute. The test_scan_enable should be on the pin ’D2’.

EXAMPLE MESSAGE

Error: Line 181, The test_scan_enable signal type on the ’C’ port for test_cell on the ’libg153’ cell is not specified on the correct pin. (LIBG-153)

LIBG-154 (error) The test_scan_enable_inverted signal type on the ’%s’ port for test_cell on the ’%s’ cell is not specified on the correct pin.

DESCRIPTION

The test_scan_enable_inverted signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin that switches the input mode of the cell between test and mission mode. Only a multiplexed flip-flop requires this signal type. This signal type can also be used in clocked scan cells.

This warning informs you that the test_cell pointed to has the test_scan_enable_inverted signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the **test_scan_enable_inverted** signal type.

EXAMPLES

```
cell(libg154) {
  area : 13;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(C) {
    direction : input;
    capacitance : 2;
  }
  pin(D2) {
    direction : input;
    capacitance : 1;
  }
  pin(C2) {
    direction : input;
    capacitance : 2;
```

```
}
pin(C3) {
  direction : input;
  capacitance : 1;
}
pin(MQ) {
  direction : internal;
  internal_node : "MQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C2";
  }
}
pin(Q) {
  direction : output;
  internal_node : "SQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
pin(QN) {
  direction : output;
  state_function : "(Q)'";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
statetable("C D C2 C3 D2", "MQ SQ") {
  table :  "R  H/L L L  -  : -   - : H/L H/L,\

           ~R   -  - H  -  : H/L - :  -  H/L,\

           ~R   -  - L  -  : -   - :  -  N,\

            R   -  H -  -  : -   - :  X  X,\

            R   -  - H  -  : -   - :  X  X,\

           ~R   -  H - H/L : -   - : H/L -,\

           ~R   -  L -  -  : -   - :  N  -";
```

```
    }
    test_cell() {
      pin(D) {
        direction : input;
      }
      pin(C) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_enable_inverted";
      }
      pin(D2) {
        direction : input;
      }
      pin(C2) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_clock_a";
      }
      pin(C3) {
        direction : input;
        capacitance : 1;
        signal_type : "test_scan_clock_b";
      }
      ff ("IQ","IQN") {
        next_state : "D";
        clocked_on : "C";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

The pin ’C’ is a clock and should not have a test_scan_enable_inverted signal_type attribute. The test_scan_enable_inverted should be on the pin ’D2.’

EXAMPLE MESSAGE

```
Error: Line 181, The test_scan_enable_inverted signal type on the ’C’ port for
        test_cell on the  ’libg154’cell is not specified on the correct pin. (LIBG-
154)
```

LIBG-155 (error) The test_scan_clock signal type on the ’%s’ port for

test_cell on the '%s' cell is not specified on the correct pin.

DESCRIPTION

The test_scan_clock signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the scan clock for clocked scan cells.

This warning informs you that the test_cell pointed to has the test_scan_clock signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the **test_scan_clock** signal type.

EXAMPLES

```
cell(libg155) {
  area : 13;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(C) {
    direction : input;
    capacitance : 2;
  }
  pin(D2) {
    direction : input;
    capacitance : 1;
  }
  pin(C2) {
    direction : input;
    capacitance : 2;
  }
  pin(C3) {
    direction : input;
    capacitance : 1;
  }
  pin(MQ) {
    direction : internal;
    internal_node : "MQ";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "C C2";
```

```
  }
}
pin(Q) {
  direction : output;
  internal_node : "SQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
pin(QN) {
  direction : output;
  state_function : "(Q)'";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
statetable("C D C2 C3 D2", "MQ SQ") {
  table :  "R  H/L L L  -  : -   - : H/L H/L,\

           ~R   -  - H  -  : H/L - :  -  H/L,\

           ~R   -  - L  -  : -   - :  -  N,\

            R   -  H -  -  : -   - :  X  X,\

            R   -  - H  -  : -   - :  X  X,\

           ~R   -  H - H/L : -   - : H/L -,\

           ~R   -  L -  -  : -   - :  N  -";
}
test_cell() {
  pin(D) {
    direction : input;
  }
  pin(C) {
    direction : input;
    capacitance : 2;
  }
  pin(D2) {
    direction : input;
    signal_type : "test_scan_in";

  }
  pin(C2) {
```

```
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_clock_a";
      }
      pin(C3) {
        direction : input;
        capacitance : 1;
        signal_type : "test_scan_clock";
      }
      ff ("IQ","IQN") {
        next_state : "D";
        clocked_on : "C";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
}
```

The pin ’C3’ is not a clock and should not have a test_scan_clock signal_type attribute.

EXAMPLE MESSAGE

```
Error: Line 195, The test_scan_clock signal type on the ’C3’ port for
test_cell on the ’libg155’ cell is not specified on the correct pin. (LIBG-155)
```

LIBG-156 (error) The test_scan_clock_a signal type on the ’%s’ port for test_cell on the ’%s’ cell is not specified on the correct pin.

DESCRIPTION

The test_scan_clock_a signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the clock of the master stage of an LSSD configuration.

This warning informs you that the test_cell pointed to has the test_scan_clock_a signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the **test_scan_clock_a** signal type.

EXAMPLES

```
cell(libg156) {
  area : 13;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(C) {
    direction : input;
    capacitance : 2;
  }
  pin(D2) {
    direction : input;
    capacitance : 1;
  }
  pin(C2) {
    direction : input;
    capacitance : 2;
  }
  pin(C3) {
    direction : input;
    capacitance : 1;
  }
  pin(MQ) {
    direction : internal;
    internal_node : "MQ";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "C C2";
    }
  }
  pin(Q) {
    direction : output;
    internal_node : "SQ";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "C C3";
    }
  }
  pin(QN) {
    direction : output;
```

```
      state_function : "(Q)'";
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "C C3";
      }
    }
    statetable("C D C2 C3 D2", "MQ SQ") {
      table :  "R  H/L L L  -  : -   - : H/L H/L,\

               ~R   -  - H  -  : H/L - :  -  H/L,\

               ~R   -  - L  -  : -   - :  -  N,\

                R   -  H -  -  : -   - :  X  X,\

                R   -  - H  -  : -   - :  X  X,\

               ~R   -  H - H/L : -   - : H/L -,\

               ~R   -  L -  -  : -   - :  N  -";
    }
    test_cell() {
      pin(D) {
        direction : input;
      }
      pin(C) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_clock_a";
      }
      pin(D2) {
        direction : input;
      }
      pin(C2) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_in";
      }
      pin(C3) {
        direction : input;
        capacitance : 1;
        signal_type : "test_scan_clock_b";
      }
      ff ("IQ","IQN") {
        next_state : "D";
        clocked_on : "C";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
```

```
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

The pin ’C’ is a clock and should not have a test_scan_clock_a signal_type attribute.

EXAMPLE MESSAGE

```
Error: Line 214, The test_scan_clock_a signal type on the ’C’ port for
        test_cell on the ’libg156’ cell is not specified on the correct pin. (LIBG-
156)
```

LIBG-157 (error) The test_clock signal type on the ’%s’ port for test_cell on the ’%s’ cell is not specified correctly.

DESCRIPTION

The test_clock signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the clock used for ATPG capture in auxiliary clock lssd cells.

This warning informs you that the test_cell pointed to has the test_clock signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the **test_clock** signal type.

EXAMPLES

```
  cell(libg157) {
    area : 13;
    pin(D) {
      direction : input;
      capacitance : 1;
    }
    pin(C) {
      direction : input;
      capacitance : 2;
    }
```

```
pin(D2) {
  direction : input;
  capacitance : 1;
}
pin(C2) {
  direction : input;
  capacitance : 2;
}
pin(C3) {
  direction : input;
  capacitance : 1;
}
pin(MQ) {
  direction : internal;
  internal_node : "MQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C2";
  }
}
pin(Q) {
  direction : output;
  internal_node : "SQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
pin(QN) {
  direction : output;
  state_function : "(Q)'";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
statetable("C D C2 C3 D2", "MQ SQ") {
  table :  "R  H/L L L  -  : -   - : H/L H/L,\

           ~R   -  - H  -  : H/L - :  -  H/L,\

           ~R   -  - L  -  : -   - :  -  N,\
```

```
                R   -  H -  -  : -   - :  X  X,\

                R   -  - H  -  : -   - :  X  X,\

               ~R   -  H - H/L : -   - : H/L -,\

               ~R   -  L -  -  : -   - :  N  -";
    }
    test_cell() {
      pin(D) {
        direction : input;
      }
      pin(C) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_clock_a";
      }
      pin(D2) {
        direction : input;
      }
      pin(C2) {
        direction : input;
        capacitance : 2;
        signal_type : "test_clock";
      }
      pin(C3) {
        direction : input;
        capacitance : 1;
        signal_type : "test_scan_clock_b";
      }
      ff ("IQ","IQN") {
        next_state : "D";
        clocked_on : "C";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

The pin ’C2’ is not a clock and should not have a test_clock signal_type attribute.

EXAMPLE MESSAGE

```
Error: Line 233, The test_clock signal type on the ’C2’ port for
        test_cell on the ’libg157’ cell is not specified correctly. (LIBG-157)
```

LIBG-158 (error) Invalid nontest mode for test_cell on the '%s' cell.
There are more than 2 sequential elements.

DESCRIPTION

The nontest mode for test_cells must be one of the following:

- A single flip-flop
- A single latch
- A single master-slave latch configuration using clocked_on and clocked_on_also

This warning informs you that the nontest mode of the test cell has more than 2 distinct sequential elements. Thus, it does not fit the previous requirements. The test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell has properly specified the correct nontest mode. To determine the multiple sequential elements in this description,

* Create a cell with the nontest mode as the functional part of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

LIBG-159 (error) Invalid nontest mode for test_cell on the '%s' cell.
This describes a ganged cell.

DESCRIPTION

The nontest mode for test_cells must be one of the following:

- A single flip-flop
- A single latch
- A single master-slave latch configuration using clocked_on and clocked_on_also

This warning informs you that the nontest mode of the test cell is a ganged cell. Thus, it does not fit the previous requirements. The test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell does not specify a ganged cell as its nontest mode. Ganged cells can be recognized by the keywords ff_bank or latch_bank.

LIBG-160 (error) The nontest mode for test_cell on the '%s' cell is invalid.
The '%s' slave port does not directly feed the output.

DESCRIPTION

The nontest mode for test_cells must be one of the following:

- A single flip-flop
- A single latch
- A single master-slave latch configuration using clocked_on, clocked_on_also

This warning informs you that in nontest mode of the test cell, the slave does not directly feed the output. This means that this is not a master-slave latch configuration that DFT Compiler supports. Thus, the test_cell is not valid, and the entire cell is converted to a black box.

WHAT NEXT

Check the library description to ensure that the nontest mode of the test_cell is correctly specified. If you are using a master-slave as the non test mode, the only accepted description is the state description using

clocked_on : <master clock>
clocked_on_also : <slave clock>

EXAMPLES

```
    cell(libg160) {
      area : 10;
      bundle (D) {
members(D1, D2);
direction : input;
capacitance : 1;
      }
      pin(G) {
```

```
direction : input;
capacitance : 1;
      }
      latch_bank ("IQ","IQN", 2) {
data_in : "D";
enable : "G";
      }
      bundle (Q) {
members(Q1, Q2);
direction : output;
function : "IQ";
timing() {
  timing_sense : positive_unate;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "D";
}
timing() {
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "G";
}
      }
      test_cell() {
pin(D1) {
  direction : input;
}
pin(G) {
  direction : input;
}
pin(D2) {
  direction : input;
  signal_type : "test_scan_in";
}
pin(Q1 Q2 ) {
  direction : output;
  function : "G D2 D1";
  signal_type : "test_scan_out";
}
      }
    }
```

EXAMPLE MESSAGE

```
Error: Line 193, The nontest mode for test_cell on the 'libg160' cell is invalid.
        The 'Q1' slave port does not directly feed the output. (LIBG-160)
```

LIBG-161 (error) The nontest mode for test_cell on the '%s' cell

is invalid
The ’%s’ state pin is not a latch for a master-slave configuration.

DESCRIPTION

The nontest mode for test_cells must be one of the following:

- A single flip-flop
- A single latch
- A single master-slave latch configuration using clocked_on and clocked_on_also

This warning informs you that the nontest mode of the test cell is an incorrect master-slave description. This stage of the master-slave configuration is not a latch, thus, it does not fit the previous requirements. The test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that the nontest mode of the test_cell is correctly specified. If you are using a master-slave as the nontest mode, the only accepted description is the state description using

clocked_on : <master clock>
clocked_on_also : <slave clock>

EXAMPLES

```
    cell(libg161) {
      area : 11;
      pin(D1 D2 D3) {
direction : input;
capacitance : 1;
      }
      pin(CP) {
direction : input;
capacitance : 2;
      }
      pin(SCK1 SCK2) {
direction : input;
capacitance : 2;
      }
      pin(SI) {
direction : input;
capacitance : 1;
timing() {
  timing_type : setup_falling;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "SCK2";
```

```
}
timing() {
  timing_type : hold_falling;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "SCK2";
}
      }
      pin(Q) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "CP SCK1";
}
      }
      pin(Q2) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "CP SCK1";
}
      }
      pin(Q3) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "CP SCK1";
}
      }
      test_cell() {
pin(D1) {
  direction : input;
}
pin(D2) {
  direction : input;
}
pin(D3) {
  direction : input;
}
pin(CP) {
  direction : input;
}
pin(SCK1) {
```

```
  direction : input;
  signal_type : "test_scan_clock_b";
}
pin(SCK2) {
  direction : input;
  signal_type : "test_scan_clock_a";
}
pin(SI) {
  direction : input;
  signal_type : "test_scan_in";
}
statetable("C D ", "Q") {
  table :  "R  H/L : - : H/L,\

           ~R   -  : - :  N";
}
pin(Q) {
  direction : output;
  internal_node : "Q";
  input_map : "CP D1";
  signal_type : "test_scan_out";
}
pin(Q2) {
  direction : output;
  internal_node : "Q";
  input_map : "CP D2";
  signal_type : "test_scan_out";
}
pin(Q3) {
  direction : output;
  internal_node : "Q";
  input_map : "CP D3";
  signal_type : "test_scan_out";
}
      }
    }
```

EXAMPLE MESSAGE

```
Error: Line 218, The nontest mode for test_cell on the 'libg161' cell is invalid.
The 'Q2' state pin is not a latch for a master-slave configuration. (LIBG-161)
```

LIBG-162 (error) The test_cell on the '%s' cell cannot have more than one test_scan_in or test_scan_in_inverted signal type. This happens on the

’%s’ port.

DESCRIPTION

Each test_cell must have only one test_scan_in or test_scan_in_inverted signal type. This signal type is specified on the pin that is used to take scan data into the cell.

This warning informs you that the test_cell pointed to has multiple test_scan_in or test_scan_in_inverted signal types. The message points to the second port that has this signal type. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell has only one test_scan_in or test_scan_in_inverted signal type.

EXAMPLES

```
    cell(libg162) {
      area : 2;
      pin_opposite ( "Q", "NQ" );
      latch ( "QX" , "QY" ) {
data_in   : " ((D*!SE) + (SI*SE)) ";
      enable  : " CK  ";
      }
      pin (D)    {
direction : input;
capacitance : 1;
      }
      pin (SI, SIN, SE) {
direction : input;
capacitance : 1;
      }
      pin (CK)    {
direction : input    ;
capacitance :   2 ;
      }
      pin (Q)    {
direction : output   ;
function  : "QX" ;
      }
      pin (NQ)    {
direction : output   ;
function  : "QY" ;
      }
      test_cell() {
latch ( "QX", "QY") {
  data_in : " D ";
  enable : " CK’ ";
```

```
}
pin (D,CK) {
  direction : input;
}
pin (SI) {
  direction : input;
  signal_type : "test_scan_in";
}
pin (SIN) {
  direction : input ;
  signal_type : "test_scan_in_inverted";
}
pin (SE) {
  direction : input ;
  signal_type : "test_scan_enable";
}
pin (Q) {
  direction : output ;
  function : " QX ";
  signal_type : "test_scan_out";
}
pin (NQ) {
  direction : output ;
  function : " QY ";
  signal_type : "test_scan_out_inverted";
}
      }
    }
```

EXAMPLE MESSAGE

```
Error: The test_cell on the 'libg162' cell cannot have more than one
test_scan_in or test_scan_in_inverted signal type. This happens on
        the 'SIN' port. (LIBG-162)
```

LIBG-163 (error) The '%s' port in test_cell on the '%s' cell has a test_scan_out signal type on an inverted output.

DESCRIPTION

The test_scan_out signal type can only be specified on a noninverted output. If the output is inverted, the proper signal type is test_scan_out_inverted. This signal type specifies the polarity of the port with respect to the state.

This warning informs you that the test_cell pointed to has the test_scan_out signal type specified on an inverted output. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

The default behavior of selecting the function over the signal_type to determine the inversion of the output is correct in most cases.

Check the library description to ensure that the test_scan_out signal type is only placed on noninverted outputs. To determine if this is an inverted or noninverted output

* Create a cell with the nontest mode as the functional part of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

EXAMPLES

```
cell(libg163) {
  area : 13;
  pin(D) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_falling;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "C";
    }
    timing() {
      timing_type : hold_falling;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "C";
    }
  }
  pin(C) {
    direction : input;
    capacitance : 2;
  }
  pin(SDI) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "C";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.0;
```

```
        intrinsic_fall : 0.0;
        related_pin : "C";
      }
    }
    pin(SE) {
      direction : input;
      capacitance : 2;
    }
    pin(TQ) {
      direction : output;
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "C";
      }
    }
    pin(SDO) {
      direction : output;
      timing() {
        timing_type : falling_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "C";
      }
    }
    test_cell() {
      pin(D) {
        direction : input;
      }
      pin(C) {
        direction : input;
      }
      pin(SDI) {
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(SE) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_enable";
      }

      statetable("C D SDI", "Q") {
table : "H L/H H/L : - : L/H,\

 L -  -  : - : N";
      }

      pin(TQ) {
        direction : output;
```

```
internal_node : "Q";
      }
      pin(SDO) {
state_function : "TQ";
        direction : output;
        signal_type : "test_scan_out";
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 176, The 'SDO' port in test_cell on the 'libg163' cell has a
test_scan_out signal type on an inverted output. (LIBG-163)
```

LIBG-164 (error) The '%s' port in test_cell on the '%s' cell has a test_scan_out_inverted signal type on a noninverted output.

DESCRIPTION

The test_scan_out_inverted signal type can only be specified on an inverted output. If the output is noninverted, the proper signal type is test_scan_out. This signal type specifies the polarity of the port with respect to the state.

This error informs you that the test_cell pointed to has the test_scan_out_inverted signal type specified on a noninverted output. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that the test_scan_out_inverted signal type is only placed on inverted outputs.

To determine if this is an inverted or noninverted output

* Create a cell with the nontest mode as the functional part of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

In the report_lib command's report, an inverted output is a state only if it has N. Instead the output contains an inversion of the state pin.

EXAMPLES

```
cell(libg164) {
  area : 11;
  pin(D0) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK1";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK1";
    }
  }

  pin(TI) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK1";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK1";
    }
  }

  pin(TE) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK1";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK1";
    }
  }
```

```
    pin(CK1) {
      direction : input;
      capacitance : 1;
    }
    pin(Q) {
      direction : output;
      inverted_output : FALSE;
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "CK1";
      }
    }

    pin(QN) {
      direction : output;
      inverted_output : TRUE;
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "CK1";
      }
    }

    test_cell() {
      pin(D0) {
        direction : input;
      }
      pin(TE) {
        direction : input;
        signal_type : "test_scan_enable";
      }
      pin(TI) {
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(CK1) {
        direction : input;
        capacitance : 1;
      }

      statetable("D0 CK1", "Q") {
table : "L/H F : - : L/H,\

 -  ~F : - : N";
      }

      pin(Q) {
        direction : output;
```

```
inverted_output : FALSE;
        internal_node : "Q";
        signal_type : "test_scan_out";
      }

      pin(QN) {
        direction : output;
        inverted_output : TRUE;
state_function : "Q";
        signal_type : "test_scan_out_inverted";
          }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 220, The 'QN' port in test_cell on the 'libg164' cell has a
        test_scan_out_inverted signal type on a noninverted output. (LIBG-164)
```

LIBG-165 (error) The test cell on the '%s' cell cannot have more than one test_scan_enable or test_scan_enable_inverted signal type. This happens on the '%s' port.

DESCRIPTION

Each test_cell must have only one test_scan_enable or test_scan_enable_inverted signal type. This signal type is specified on the pin that is used to select between scan and mission mode operation of the cell. Using the state table format, Library Compiler expects a single test_scan_enable or test_scan_enable_inverted signal type. Otherwise, Library Compiler generates a black box cell.

This warning informs you that the test_cell pointed to has multiple test_scan_enable or test_scan_enable_inverted signal types. The message points to the second port that has this signal type. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell has only one test_scan_enable or test_scan_enable_inverted signal type. Otherwise, provide a full functional description of the non test_cell cell to bypass the multuple scan enable check.

EXAMPLES

```
    cell(libg165) {
      area : 13;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(G) {
direction : input;
capacitance : 2;
      }
      pin(D2) {
direction : input;
capacitance : 1;
      }
      pin(C2) {
direction : input;
capacitance : 2;
      }
      pin(SE) {
direction : input;
capacitance : 2;
      }
      pin(SEB) {
direction : input;
capacitance : 2;
      }
      pin(Q) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "G C2";
}
      }
      pin(QN) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "G C2";
}
      }
      test_cell() {
pin(D) {
  direction : input;
}
pin(G) {
```

```
  direction : input;
}
pin(D2) {
  direction : input;
  signal_type : "test_scan_in";
}
pin(C2) {
  direction : input;
  signal_type : "test_scan_clock";
}
pin(SE) {
  direction : input;
  capacitance : 2;
  signal_type : "test_scan_enable";
}
pin(SEB) {
  direction : input;
  capacitance : 2;
  signal_type : "test_scan_enable_inverted";
}
state ("IQ","IQN") {
  force_01 : "G D'";
  force_10 : "G D";
}
pin(Q) {
  direction : output;
  function : "IQ";
  signal_type : "test_scan_out";
}
pin(QN) {
  direction : output;
  function : "IQN";
  signal_type : "test_scan_out_inverted";
}
      }
    }
```

EXAMPLE MESSAGE

```
Error: The test cell on the 'libg165' cell cannot have more than one
        test_scan_enable or test_scan_enable_inverted signal type.
        This happens on the 'SEB' port. (LIBG-165)
```

LIBG-166 (error) The '%s' test_scan_clock port in test_cell on the '%s' cell
does not have an active sense.

DESCRIPTION

The test_scan_clock must have an active sense in the full cell description. The

Library Compiler determines the active sense by checking the function of the full cell. The test_scan_clock is the scan clock in the clocked scan type.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell are recognized. Both the test_cell and the entire cell are converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell

* Create a cell with the non test mode as the functional part of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

LIBG-167 (error) The '%s' test_scan_clock_a port in test_cell on the '%s' cell does not have an active sense.

DESCRIPTION

The test_scan_clock_a must have an active sense in the full cell description. The Library Compiler determines the active sense by checking the function of the full cell. The test_scan_clock_a is the scan clock for the master stage of the LSSD scan style.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell are recognized. Both the test_cell and the entire cell are converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell

* Create a cell with the nontest mode as the functional part of the cell.
* Compile this cell.
* Issue the following command:

```
    report_lib -table <library name> <cell name>
```

LIBG-168 (error) The '%s' test_scan_clock_b port in test_cell on the '%s' cell
does not have an active sense.

DESCRIPTION

The test_scan_clock_b must have an active sense in the full cell description. The active sense is determined by Library Compiler by checking the function of the full cell. The test_scan_clock_b is the scan clock for the slave stage of the LSSD scan style.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell are recognized. Both the test_cell and the entire cell are converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell

* Create a cell with the nontest mode as the functional part
  of the cell.
* Compile this cell.
* Issue the following command:

```
    report_lib -table <library name> <cell name>
```

LIBG-169 (error) The '%s' test_clock port in test_cell on the '%s' cell does
not have an active sense.

DESCRIPTION

The test_clock must have an active sense in the full cell description. Library Compiler determines the active sense by checking the function of the full cell. The test_clock is the capture clock used by ATPG in the auxiliary clocked lssd scan style.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell are recognized. Both the test_cell and the entire cell are

converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell

* Create a cell with the nontest mode as the functional part of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

LIBG-170 (error) The '%s' port in test_cell for the '%s' cell has an invalid signal type %s.

DESCRIPTION

The valid signal_types in test_cells are

- test_scan_in
- test_scan_in_inverted
- test_scan_enable
- test_scan_enable_inverted
- test_scan_out
- test_scan_out_inverted
- test_scan_clock
- test_scan_clock_a
- test_scan_clock_b
- test_clock

This warning informs you that the port in the test_cell pointed to has a signal_type other than the ones listed previously. Thus, the test_cell is not valid, and the entire cell is converted to a black box.

WHAT NEXT

Check the test_cell pointed to and change the invalid signal_type.

LIBG-171 (error) The LSSD test_cell for the '%s' cell has neither a test_scan_clock_b signal type nor a master-slave as its

nontest mode.

DESCRIPTION

LSSD scan styles must have the following test_cell characteristics:

```
   clocked lssd
- signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
test_scan_out_inverted, test_scan_clock_a, test_scan_clock_b
- nontest mode: flip_flop
   auxiliary clock lssd
- signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
test_scan_out_inverted, test_scan_clock_a, test_scan_clock_b,
test_clock
- nontest mode : flip_flop
   single-latch lssd
- signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
test_scan_out_inverted, test_scan_clock_a, test_scan_clock_b
- nontest mode: latch
   single-latch lssd
- signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
test_scan_out_inverted, test_scan_clock_a,
test_scan_clock_b (optional)
- nontest mode: master-slave (clocked_on & clocked_on_also)
```

This error informs you that this cell is an lssd scan style because it has test_scan_in/test_scan_in_inverted, test_scan_out/test_scan_out_inverted, and test_scan_clock_a signal types. However, it is invalid because it has neither a test_scan_clock_b signal type nor a master-slave as its nontest mode. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the nontest modes and signal types in the test_cell pointed to. If you do not understand why the nontest function is not one of the previous types,

* Create a cell with the nontest mode as the functional part of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

In the report_lib command’s report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

EXAMPLES

```
cell(libg171) {
  area : 21;
```

```
    pin(D1) {
      direction : input;
      capacitance : 1;
    }
    pin(C1) {
      direction : input;
      capacitance : 2;
    }
    pin(D2) {
      direction : input;
      capacitance : 1;
    }
    pin(C2) {
      direction : input;
      capacitance : 2;
    }
    pin(C3) {
      direction : input;
    capacitance : 1;
    }

    pin(Q1) {
      direction : output;
      timing() {
      timing_type : rising_edge;
intrinsic_rise : 1.0;
intrinsic_fall : 0.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "C1";
      }
      timing() {
timing_type : rising_edge;
intrinsic_rise : 1.0;
intrinsic_fall : 0.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "C2";
      }
    }
    pin(Q2) {
      direction : output;
      timing() {
timing_type : rising_edge;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "C3";
      }
    }
    test_cell() {
      pin(D1) {
direction : input;
      }
```

```
      pin(C1) {
direction : input;
      }
      pin(D2) {
direction : input;
signal_type : "test_scan_in";
      }
      pin(C2) {
direction : input;
signal_type : "test_scan_clock_a";
    }
      pin(C3) {
direction : input;
signal_type : "test_scan_clock_b";
      }
      state("IQ","IQN") {
force_10 : "C1 D1";
force_01 : "C1 D1'";
      }
      pin(Q1) {
direction : output;
      function : "IQ";
      }
      pin(Q2) {
direction : output;
signal_type : "test_scan_out";
      }
    }
    test_cell() {
      pin(D1) {
direction : input;
      }
      pin(C1) {
direction : input;
    }
      pin(D2) {
direction : input;
signal_type : "test_scan_in";
      }
      pin(C2) {
direction : input;
signal_type : "test_scan_clock_a";
    }
      pin(C3) {
direction : input;
      }
      state("IQ","IQN") {
force_10 : "C1 C3' D1";
force_01 : "C1 C3' D1'";
      }
      pin(Q1) {
direction : output;
    }
      pin(Q2) {
direction : output;
```

```
 function : "IQ";
 signal_type : "test_scan_out";
       }
     }
   }
```

EXAMPLE MESSAGE

```
Error: Line 229, The LSSD test_cell for the 'libg171' cell has neither
a test_scan_clock_b signal type nor a master-slave as its nontest mode. (LIBG-171)
```

LIBG-172 (error) The test_cell for the '%s' cell is not valid because
it has missing or extra test signals.

DESCRIPTION

```
The supported scan styles must have the following test_cell characteristics:

   multiplexed flip-flop
- signal types : test_scan_in/test_scan_in_inverted, test_scan_enable/
test_scan_enable_inverted, test_scan_out/test_scan_out_inverted
- nontest mode : flip-flop, master-slave latch pair, or latch
   clocked scan
- signal types : test_scan_in/test_scan_in_inverted, test_scan_enable/
test_scan_enable_inverted (optional), test_scan_clock,
test_scan_out/test_scan_out_inverted
- nontest modes : flip-flop or latch
   clocked lssd
        - signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
                test_scan_out_inverted, test_scan_clock_a, test_scan_clock_b
        - nontest mode: flip-flop
   auxiliary clock lssd
        - signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
                test_scan_out_inverted, test_scan_clock_a, test_scan_clock_b,
                test_clock
        - nontest mode : flip-flop
   single-latch lssd
        - signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
                test_scan_out_inverted, test_scan_clock_a, test_scan_clock_b
        - nontest mode: latch
   single-latch lssd
        - signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
                test_scan_out_inverted, test_scan_clock_a, test_scan_clock_b
        - nontest mode: latch
   single-latch lssd
        - signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
                test_scan_out_inverted, test_scan_clock_a,
                test_scan_clock_b (optional)
```

```
        - nontest mode: master-slave (clocked_on & clocked_on_also)
```

This warning informs you that the other signal types do not correspond to one of the previously supported scan styles. Extra or missing signal types point to the fact that the test_cell is not valid, and the entire cell is a black box.

WHAT NEXT

Check the library description to ensure that each test_cell has correctly specified the nontest modes and signal types in the test_cell pointed to. If you do not understand why the nontest function is not one of the previous types,

* Create a cell with the nontest mode as the functional part of the cell.
* Compile this cell.
* Issue the following command:

```
     report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

EXAMPLES

```
    cell(libg172) {
      area : 13;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(C) {
direction : input;
capacitance : 2;
      }
      pin(SDI) {
direction : input;
capacitance : 1;
      }
      pin(SDOB) {
direction : output;
      }
      test_cell() {
pin(D) {
  direction : input;
}
pin(C) {
  direction : input;
}
pin(SDI) {
  direction : input;
  signal_type : "test_scan_in";
}
statetable("D C", "QN") {
  table : "L/H H : - : H/L,
```

```
 -   L : - : N";
}

pin(SDOB) {
  direction : output;
  inverted_output : TRUE;
  internal_node : "QN";
  signal_type : "test_scan_out_inverted";
}
      }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 160, The test_cell for the 'libg172' cell is not valid because
it has missing or extra test signals. (LIBG-172)
```

LIBG-173 (error) Cannot derive full function based on test_cell on the '%s' cell due to previous warnings or errors.

DESCRIPTION

Library Compiler generates a functional description of the entire cell based on the information in the test_cell. However, if there are warnings or errors in the test_cell, a functional description of the entire cell cannot be generated.

This error informs you that the test_cell pointed to has previous errors or warnings. Thus, the test_cell is not valid, and the entire cell is a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Fix the previous problems in order to recognize both the test_cell and full cell functionality. You might have to add a state table description of the entire cell.

EXAMPLES

```
  cell(libg173) {
    area : 11;
    pin(D0) {
      direction : input;
      capacitance : 1;
      timing() {
        timing_type : setup_rising;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        related_pin : "CK1";
      }
```

```
  timing() {
    timing_type : hold_rising;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "CK1";
  }
}

pin(TI) {
  direction : input;
  capacitance : 1;
  timing() {
    timing_type : setup_rising;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "CK1";
  }
  timing() {
    timing_type : hold_rising;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "CK1";
  }
}

pin(TE) {
  direction : input;
  capacitance : 1;
  timing() {
    timing_type : setup_rising;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "CK1";
  }
  timing() {
    timing_type : hold_rising;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "CK1";
  }
}

pin(CK1) {
  direction : input;
  capacitance : 1;
}
pin(Q) {
  direction : output;
  inverted_output : FALSE;
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
```

```
        related_pin : "CK1";
      }
    }

    pin(QN) {
      direction : output;
      inverted_output : TRUE;
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "CK1";
      }
    }

    test_cell() {
      pin(D0) {
        direction : input;
      }
      pin(TE) {
        direction : input;
        signal_type : "test_scan_enable";
      }
      pin(TI) {
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(CK1) {
        direction : input;
        capacitance : 1;
      }

      statetable("D0 CK1", "Q") {
table : "L/H F : - : L/H,\

 -  ~F : - : N";
      }

      pin(Q) {
        direction : output;
inverted_output : FALSE;
        internal_node : "Q";
        signal_type : "test_scan_out";
      }

      pin(QN) {
        direction : output;
        inverted_output : TRUE;
state_function : "Q";
        signal_type : "test_scan_out_inverted";
          }
    }
  }
```

In this case, the test_cell pointed to has the test_scan_out_inverted signal type specified on a noninverted output 'QN' (LIBG-164). Thus, the test_cell is not valid, and the entire cell is converted to a black box.

EXAMPLE MESSAGE

```
Error: Line 189, Cannot derive full function based on test_cell
        on the 'libg173' cell due to previous warnings or errors. (LIBG-173)
```

LIBG-174 (error) The '%s' clocked test cell is not valid because it has a master-slave configuration as its nontest mode.

DESCRIPTION

A clocked test_cell has the following characteristics:

- signal types : test_scan_in/test_scan_in_inverted, test_scan_enable/ test_scan_enable_inverted (optional), test_scan_clock, test_scan_out/test_scan_out_inverted
- nontest modes : flip-flop or latch

This warning informs you that the signal types point to this cell as being a clocked scan test_cell, but it does not have a flip-flop or latch as its nontest mode; it is currently specified as a master-slave cell. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that nontest modes and signal types are correctly pointed to by the test_cell. To determine why the nontest function is not one of the previous types,

* Create a cell with the nontest mode as the functional part of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

EXAMPLES

```
cell(libg174) {
  area : 10;
```

```
pin(D) {
  direction : input;
  capacitance : 1;
  timing() {
    timing_type : setup_falling;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "G";
  }
  timing() {
    timing_type : hold_falling;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "G";
  }
}
pin(G G2) {
  direction : input;
  capacitance : 1;
}
pin(D2) {
  direction : input;
  capacitance : 1;
  timing() {
    timing_type : setup_rising;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "C2";
  }
  timing() {
    timing_type : hold_rising;
    intrinsic_rise : 0.0;
    intrinsic_fall : 0.0;
    related_pin : "C2";
  }
}
pin(C2) {
  direction : input;
  capacitance : 2;
}
pin(Q) {
  direction : output;
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "G C2";
  }
}
pin(QN) {
  direction : output;
  timing() {
    timing_type : rising_edge;
```

```
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : " G2 G C2";
      }
    }
    test_cell() {
      pin(D) {
        direction : input;
      }
      pin(G G2) {
        direction : input;
      }
      pin(D2) {
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(C2) {
        direction : input;
        signal_type : "test_scan_clock";
      }
      latch ("IQ","IQN") {
data_in : "D";
        enable : "G";
        enable_also : "G2";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

In this case, the cell is a master-slave with an unknown test cell type.

EXAMPLE MESSAGE

```
Error: Line 208, The 'libg174' clocked test cell is not valid
        because it has a master-slave configuration as its nontest mode. (LIBG-174)
fi
```

LIBG-175 (error) The test cell for the '%s' auxiliary clocked lssd cell is not

valid because its nontest mode is not a flip-flop.

DESCRIPTION

An auxiliary clocked lssd test_cell has the following characteristics:

- signal types : test_scan_in/test_scan_in_inverted, test_scan_out/ test_scan_out_inverted, test_scan_clock_a, test_scan_clock_b, test_clock
- nontest mode : flip-flop

This warning informs you that the signal types point to this cell as being a auxiliary clocked lssd test_cell, but it does not have a flip-flop as its nontest mode. This makes the test_cell invalid and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

WHAT NEXT

Check the library description to ensure that nontest modes and signal types are correctly pointed to by the test_cell. To determine why the nontest function is not one of the previous types,

* Create a cell with the nontest mode as the functional part of the cell.
* Compile this cell.
* Issue the following command:

```
report_lib -table <library name> <cell name>
```

In the report_lib command’s report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

EXAMPLES

```
    cell(libg103) {
      area : 12;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(CK,IH, CK1) {
direction : input;
capacitance : 1;
      }
      pin(A,B) {
direction : input;
capacitance : 2;
      }
      pin(SI) {
direction : input;
capacitance : 1;
timing() {
```

```
  timing_type : setup_falling;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "A";
}
timing() {
  timing_type : hold_falling;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  related_pin : "A";
}
      }
      pin(Q) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "CK IH CK1";
}
timing() {
  timing_type : falling_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "B";
}
      }
      pin(XQ) {
direction : output;
      }
      test_cell(){
pin(D,CK,CK1){
  direction : input;
}
pin(IH ){
  direction : input;
  signal_type : "test_clock";
}
pin(SI){
  direction : input;
  signal_type : "test_scan_in";
}
pin(A){
  direction : input;
  signal_type : "test_scan_clock_a";
}
pin(B){
  direction : input;
  signal_type : "test_scan_clock_b";
}
ff("IQ","IQN"){
```

```
  clocked_on : "CK";
  next_state : "D";
  clocked_on_also : "CK1";
}

pin(Q){
  direction : output;
  function : "IQ";
  signal_type : "test_scan_out";
}
pin(XQ){
  direction : output;
  function : "IQN";
  signal_type : "test_scan_out_inverted";
}
      }
    }
```

EXAMPLE MESSAGE

```
Error: Line 196, The test cell for the 'libg175' auxiliary clocked lssd cell is not
        valid because its nontest mode is not a flip-flop. (LIBG-175)
```

LIBG-176 (error) Neither the memory_read nor the memory write group
 is allowed on scalar ports.

DESCRIPTION

Either the memory_read group or the memory_write group is specified on a scalar port. These groups are only allowed on bus groups.

WHAT NEXT

Remove the memory_read and memory_write group from all scalar ports.

LIBG-177 (error) The '%s' cell is a ROM, and ROMs cannot have any

memory_write groups.

DESCRIPTION

The cell is defined as a ROM type in the memory group. ROM cells cannot have any memory_write groups because the memory block cannot be written to.

WHAT NEXT

Either change the memory type to a ram type or remove the memory_write group.

EXAMPLES

```
cell(libg177) {
          ...
            memory() {
              type : rom;
     address_width : 10;
     word_width : 8;
          }
          ...
          bus (data_in) {
              bus_type   : "bus8"
              direction : input;
              capacitance : 1.46;
              fanout_load : 1.46;

              memory_write() {/* Not allowed on ROM cells */
                address : ram_addr;
               enable : WR;
              }
  }
          ...
}
```

EXAMPLE MESSAGE

```
Error: Line 22, The 'libg177' cell is a ROM, and ROMs cannot have any
        memory_write groups. (LIBG-177)
```

LIBG-178 (error) The '%s' cell is a RAM, and RAMs must have at
least one memory_read port and at least one memory_write

port.

DESCRIPTION

The cell is defined as a RAM type in the cell memory group. RAM cells must have at least one memory_read port and at least one memory_write port.

WHAT NEXT

You can implement either of the following suggestions:

(1) Change the memory type to **rom** and ensure only the memory_read group is provided.
(2) If the model is for a RAM, make sure that both the memory_read and memory_write groups are provided.

EXAMPLES

```
cell (libg178) {

      area : 2300.0;
      memory() {
        type : ram;
address_width : 10;
word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8";  /* defined in the library */
           direction : input;
           capacitance : 1.0;
           memory_write() {
             address : ram_addr;
             enable : WR;
           }
     }
     pin (WR) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }

     bus(data_out){
       bus_type  : "bus8";
       direction : output;
```

```
    }
 }
```

In this case, the memory_read group is missing in the cell. Add the following group to the port 'data_out' :

```
       memory_read() {
         address : ram_addr;
       }
```

EXAMPLE MESSAGE

```
Error: Line 22, The 'libg178' cell is a RAM, and RAMs must have at
least one memory_read port and at least one memory_write port. (LIBG-178)
```

LIBG-179 (error) The '%s' cell is a ROM, and ROMs must have at
least one memory_read group.

DESCRIPTION

The cell is defined as a ROM type in the cell memory group. ROM cells require at least one memory_read port.

WHAT NEXT

Add the memory_read group to the data port.

EXAMPLES

```
cell (libg179) {

      area : 2300.0;
      memory() {
        type : rom;
address_width : 10;
word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.0;
```

```
     }
     pin (WR) {
       direction : input;
       capacitance : 1.13;
       clock : true;
     }
     bus(data_out){
       bus_type  : "bus8";
       direction : output;
    }
 }
```

In this case, the memory_read group is missing in the cell. Add the following group to the port 'data_out' :

```
       memory_read() {
         address : ram_addr;
       }
```

EXAMPLE MESSAGE

```
Error: Line 22, The 'libg179' cell is a ROM, and ROMs must have at
        least one memory_read group. (LIBG-179)
```

LIBG-180 (error) The '%s' bus has a %s group, but the '%s' cell has no memory group.

DESCRIPTION

The cell is missing a memory group. The bus has memory specific syntax, which is not allowed.

WHAT NEXT

Either add the memory group to the cell or remove the memory_read/write groups from the ports.

EXAMPLES

```
cell (libg179) {

      area : 2300.0;
      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
```

```
            direction : input;
            capacitance : 1.0;
            memory_write() {
              address : ram_addr;
              enable : WR;
            }
      }
      pin (WR) {
        direction : input;
        capacitance : 1.0;
        clock : true;
      }
      bus(data_out){
        bus_type  : "bus8";
        direction : output;

     }
 }
```

EXAMPLE MESSAGE

```
Error: Line 38, The 'data_in' bus has a memory_write group, but the 'lib180' cell
        has no memory group. (LIBG-180)
```

LIBG-181 (error) In the '%s' cell, the '%s' data bus has a width of %d,
but the memory group has a word width of %d.

DESCRIPTION

The size of the data bus does not match the size of the memory group specified in the cell memory group. They must be consistent.

WHAT NEXT

Change the library to make the data bus width and the memory group word's width consistent.

EXAMPLES

```
cell (libg181) {
      area : 2300.0;
      memory() {
        type : ram;
address_width : 8;
word_width : 6;
      }
```

```
      bus (ram_addr) {
            bus_type  : "bus8"; /* defined in the library */
            direction : input;
            capacitance : 1.0;
      }
      bus (data_in) {
            bus_type   : "bus8"
            direction : input;
            capacitance : 1.0;

            memory_write() {
              address : ram_addr;
              enable : WR;
            }
      }
      pin (WR) {
        direction : input;
        capacitance : 1.0;
        clock : true;
      }

      bus(data_out){
        bus_type  : "bus8";
        direction : output;
        memory_read() {
          address : ram_addr;
        }
     }
  }
```

In this case, the width of the bus data_out is 8 and the word width in the memory group is 6. Change either the bus_data's width to 6 or the memory group's word width to 8 to make them consistent.

EXAMPLE MESSAGE

Error: Line 54, In the 'libg181' cell, the 'data_out' data bus has a width of 8, but the memory group has a word width of 6. (LIBG-181)

LIBG-182 (error) The '%s' memory_write data bus can not be an output.

DESCRIPTION

The bus is an input to the memory block because it has the memory_write group specified. Inputs to the memory block can not be an output type.

WHAT NEXT

The direction of the bus must be changed to either input, inout, or internal.

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LIBG-183 (error) In the ’%s’ cell, the ’%s’ address bus is not defined.

The address bus specified in the group is not defined in the cell.

The address specification must refer to a bus defined in the cell.

```
cell (libg183) {
      area : 2300.0;

      memory() {
        type : ram;
address_width : 8;
word_width : 8;
      }
     bus (data_in) {
           bus_type   : "bus8" /* defined in the library */
           direction : output;
           capacitance : 1.0;
           memory_write() {
             address : ram_addr;
             enable : WR;
           }
     }
     pin (WR) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }
     bus(data_out){
       bus_type  : "bus8";
       direction : output;
       memory_read() {
         address : ram_addr;
       }
    }
 }
```

In this case, define the ram_addr as a port in the cell as follows:

```
bus (ram_addr) { bus_type : "bus8"; /* defined in the library */ direction : input;
capacitance : 1.0; }
```

Error: Line 58, In the ’libg183’ cell, the ’ram_addr’ address bus is not defined. (LIBG-183)

LIBG-184 (error) In the ’%s’ cell, the ’%s’ address bus has a

width of %d,
 but the memory group has an address width of %d.

DESCRIPTION

The size of the address bus does not match the address size of the memory group specified in the cell memory group. They must be consistent.

WHAT NEXT

Change the library to make the address bus width and the memory group address width consistent.

EXAMPLES

```
cell (libg184) {
      area : 2300.0;
      memory() {
        type : ram;
address_width : 10;
word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus8"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.0;

           memory_write() {
             address : ram_addr;
             enable : WR;
           }
     }
     pin (WR) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }

     bus(data_out){
       bus_type  : "bus8";
       direction : output;
       memory_read() {
         address : ram_addr;
       }
    }
```

```
  }
```

In this case, the width of the bus data_out is 8 and the address width in the memory group is 10. Either change the width of the ram_addr to 10 or change the memory group's address width to 8 to make them consistent.

EXAMPLE MESSAGE

```
Error: Line 58, In the 'libg184' cell, the 'ram_addr' address bus has a width of 8,
        but the memory group has an address width of 10. (LIBG-184)
```

LIBG-185 (error) The '%s' memory address can not be an output.

DESCRIPTION

The address bus is an input to the memory block. Inputs to the memory block can not be an output type.

WHAT NEXT

The direction of the bus must be changed to either input, inout, or internal.

LIBG-186 (error) In the '%s' cell, the '%s' memory_read data bus
cannot be an input.

DESCRIPTION

The data bus is an output of the memory block because it has the memory_read group specified.

WHAT NEXT

Change the direction of the bus that has the memory_write group to either output, inout, or internal.

EXAMPLES

```
cell (libg186) {
      area : 2300.0;
      memory() {
        type : ram;
```

```
address_width : 8;
word_width : 8;
      }
      bus (ram_addr) {
           bus_type  : "bus8"; /* defined in the library */
           direction : output;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.0;
           memory_write() {
             address : ram_addr;
             enable : WR;
           }
     }
     pin (WR) {
       direction : input;
       capacitance : 1.13;
       clock : true;
     }
     bus(data_out){
       bus_type  : "bus8";
       direction : input; /* should be output */
       memory_read() {
         address : ram_addr;
       }
    }
  }
```

EXAMPLE MESSAGE

```
Error: Line 54, In the 'libg186' cell, the 'data_out' memory_read data bus
cannot be an input. (LIBG-186)
```

LIBG-187 (error) In the '%s' cell, The %s '%s' attribute is not the name of a port or bus.

DESCRIPTION

The attribute specified in the group is not defined in the cell as either a port or a bus.

You cannot specify an expression here, only a port or a bus is valid. If you need to model an expression(logic), create a pin with a state_function attribute and use that internal pin.

WHAT NEXT

Make sure the specification refers to a port or a bus defined in the cell.

EXAMPLES

```
    cell (libg187) {
      area : 1380.0;
      interface_timing : TRUE;

      memory() {
        type : ram;
address_width : 10;
word_width : 8;
      }

      bus (RA) {
bus_type  : "bus10";
direction : input;
capacitance : 1.0;
      }

      bus (DI) {
bus_type   : "bus8";
direction : input;
capacitance : 1.0;

memory_write() {
  address : RA;
  enable : "WRE";
}
      }

      pin (WE) {
direction : input;
capacitance : 1.0;
clock : true;
      }

      pin (CE) {
direction : input;
capacitance : 1.0;
clock : true;
      }

      bus(DO){
bus_type  : "bus8";
direction : output;
capacitance : 1.0;

memory_read() {
  address : RA;
}
      }
    }
```

In this case, the port 'WRE' can be defined :

1. as an internal pin
2. is state_function defines the writing occurence only when
   WE and CE are active.

```
      pin (WRE) {
direction : internal;
capacitance : 1.0;
state_function : "!(WE' * CE')";
clock : true;
      }
```

EXAMPLE MESSAGE

```
Error: Line 43, In the 'libg187' cell, the enable 'WRE' attribute is not
the name of a port or bus. (LIBG-187)
```

LIBG-188 (error) In the '%s' cell, the %s '%s' bus has a width of %d,
but the memory group has a word width of %d.

DESCRIPTION

The size of the bus does not match the word size of the memory block specified in the cell memory group. They must be consistent.

WHAT NEXT

Change the library to make the bus width and the memory group word width consistent.

EXAMPLES

```
cell (libg188) {
      area : 2300.0;
      memory() {
        type : ram;
address_width : 10;
word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
```

```
            direction : input;
            capacitance : 1.0;

            memory_write() {
              address : ram_addr;
              enable : WR;
            }
      }
      bus (WR) {
        bus_type   : "bus10"
        direction : input;
        capacitance : 1.0;
        fanout_load : 1.0;
        clock : true;
      }
      bus(data_out){
        bus_type  : "bus8";
        direction : output;
        memory_read() {
          address : ram_addr;
        }
     }
 }
```

In this case, the bus type of the enable 'WR' is bus10. Change it to bus8.

EXAMPLE MESSAGE

```
Error: Line 42, In the 'libg188' cell, the enable 'WR' bus has a width of 10,
        but the memory group has a word width of 8. (LIBG-188)
```

LIBG-189 (error) In the '%s' cell, the memory_write group cannot have both the enable attribute and the clocked_on attribute.

DESCRIPTION

The memory_write group has both the enable attribute and the clocked_on attribute specified. The Library Compiler does not allow it.

WHAT NEXT

If the memory write process is edge triggered, use the clocked_on attribute. If the memory write process is level-sensitive triggered, use the enable attribute. You cannot specify both at once.

EXAMPLES

```
cell (libg189) {
      area : 2300.0;
      memory() {
        type : ram;
address_width : 10;
word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8";
           direction : input;
           capacitance : 1.0;

           memory_write() {
             address : ram_addr;
             enable : WR;
     clocked_on : WR;
           }
     }
     pin (WR) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }

     bus(data_out){
       bus_type  : "bus8";
       direction : output;
       memory_read() {
         address : ram_addr;
       }
    }
 }
```

For the bus ’data_in’, you can either have the enable attribute or the clocked_on attribute defined in the memory_write, but not both.

EXAMPLE MESSAGE

```
Error: Line 40, In the ’libg189’ cell, the memory_write group cannot
have both the enable attribute and the clocked_on attribute. (LIBG-189)
```

LIBG-190 (error) In the ’%s’ cell, the v3.1 sequential syntax is not

supported on memory cells.

DESCRIPTION

The cell has both the memory syntax and the v3.1 sequential syntax defined by either the **function** attribute or the **ff** and **latch** groups. The two syntaxes are not compatible and cannot both be specified on the same cell.

WHAT NEXT

Remove the v3.1 sequential syntax, and use the new state table syntax.

EXAMPLES

```
cell (libg190) {
      area : 2300.0;
      memory() {
        type : ram;
address_width : 10;
word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.0;

           memory_write() {
             address : ram_addr;
             enable : WR;
           }
     }
     pin (WR) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }

     bus(data_out){
       bus_type  : "bus8";
       direction : output;
       function : "WR + data_in";
       memory_read() {
         address : ram_addr;
       }
    }
 }
```

The function attribute is defined for the pin 'data_out'. This message is displayed for each element of the bus data_out that has the function attribute. To fix the problem, temove the function attribute from the pin.

EXAMPLE MESSAGE

Error: Line 60, In the 'libg190' cell, the v3.1 sequential syntax is not supported on memory cells. (LIBG-190)

LIBG-191 (error) The '%s' memory output cannot have a function.

DESCRIPTION

The memory output has an internal_node or a state_function attribute. A memory output has its function defined by the memory_read group and cannot also have an internal_node or a state_function attribute.

WHAT NEXT

Remove the internal_node or state_function attribute.

EXAMPLES

```
cell (libg191) {
      area : 2300.0;
      memory() {
        type : ram;
address_width : 10;
word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.46;
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.46;

           memory_write() {
             address : ram_addr;
             enable : WR;
           }
     }
     pin (WR) {
       direction : input;
```

```
       capacitance : 1.13;
       clock : true;
     }

     bus(data_out){
       bus_type  : "bus8";
       direction : output;
       state_function : "WR + data_in";/* not allowed */
       memory_read() {
         address : ram_addr;
       }
    }
 }
```

This message is displayed for each element of the bus data_out that has the state_function attribute.

EXAMPLE MESSAGE

```
Error: Line 60, The 'data_out[0]' memory output cannot have a function. (LIBG-191)
```

LIBG-192 (error) The '%s' port that has both memory_read and memory_write must have the inout direction.

DESCRIPTION

Buses with both memory_read and memory_write groups must have the direction inout.

WHAT NEXT

Either change the direction of this bus to inout, or remove either the memory_read or memory_write group from this bus.

EXAMPLES

```
cell (libg192) {
      area : 2300.0;
      memory() {
        type : ram;
address_width : 10;
word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
```

```
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.0;

     }
     pin (WR) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }

     bus(data_out){
       bus_type  : "bus8";
       direction : output;/* must be inout */
       memory_read() {
         address : ram_addr;
       }
       memory_write() {
          address : ram_addr;
          enable : WR;
       }
    }
 }
```

In this case, the direction of the bus 'data-out' is output. To fix the problem, set the direction to inout. This message is displayed for each element of the bus data_out.

EXAMPLE MESSAGE

Error: Line 62, The 'data_out[0]' port that has both memory_read and memory_write must have the inout direction. (LIBG-192)

LIBG-193 (error) The '%s' port that has both memory_read and memory_write must have a three_state expression.

DESCRIPTION

Buses with both memory_read and memory_write groups must have the **three_state** attribute. During the memory write cycle, when the new data value is driven in from outside the cell, the port associated with the memory_read group must have a three_state attribute.

WHAT NEXT

Add a valid three_state expression to this bus, or remove either the memory_read or

memory_write group from this bus.

EXAMPLES

```
cell (libg193) {
      area : 2300.0;
      memory() {
        type : ram;
        address_width : 10;
        word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.0;

     }
     pin (WR) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }

     bus(data_out){
       bus_type  : "bus8";
       direction : inout;/* must have three_state */
       memory_read() {
         address : ram_addr;
       }
       memory_write() {
          address : ram_addr;
          enable : WR;
       }
    }
 }
```

In this case, the bus ’data_out’ has both memory_read and memory_write groups, but no three_state attribute. This message is displayed for each element of the bus data_out. To fix the problem, add the three_state attribute to the bus as follows:

```
     pin (CE) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }
     bus(data_out){
       bus_type  : "bus8";
       direction : inout;
       three_state : "CE";/* new statement */
```

```
      memory_read() {
        address : ram_addr;
      }
      memory_write() {
         address : ram_addr;
         enable : WR;
      }
   }
```

EXAMPLE MESSAGE

```
Error: Line 62, The 'data_out[0]' port that has both memory_read and memory_write
must have a three_state expression. (LIBG-193)
```

LIBG-194 (warning) The function attribute on the '%s' pin is ignored.

DESCRIPTION

This message indicates that the **function** attribute on the specified pin is ignored. If the pin is an internal pin, use **state_function** attribute. Internal pins are equal to internal nodes, which are single sequential elements. If the cell is a memory cell, it does not need a **function** attribute if the pin already has a **memory_read**, has a state_function attribute, or is an internal node.

WHAT NEXT

Either change the internal pin to a output or inout port or remove the **function** attribute.

EXAMPLES

```
cell(libg202) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }
  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\

     -   ~R : - - : N   N";
  }

  pin(Q) {
```

```
    direction : output;
    inverted_output : FALSE;
    function : "Q";
    internal_node : "Q";
  }
  pin(QB) {
    direction : output;
    inverted_output : TRUE;
    internal_node : "QB";
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 127, the function attribute on the 'Q' pin is ignored. (LIBG-194)
```

LIBG-195 (warning) A bundle is not supported in the memory group.

DESCRIPTION

Currently, Library Compiler does not support memory cells with bundles.

WHAT NEXT

Modify the bundle into a bus.

EXAMPLES

```
cell (libg195) {
      area : 2300.0;
      memory() {
       type : ram;
       address_width : 10;
       word_width : 8;
      }

      bundle (ram_addr) {
       members( D_1 D_2);
       direction : input;
       capacitance : 1.0;
     }
     bus (data_in) {
       bus_type   : "bus8"
       direction : input;
       capacitance : 1.0;
       memory_write() {
          address : ram_addr;
          enable : WR;
```

```
      }
    }
    pin (WR) {
      direction : input;
      capacitance : 1.0;
      clock : true;
    }
    bus(data_out){
      bus_type  : "bus8";
      direction : output;
      memory_read() {
        address : ram_addr;
      }
   }
}
```

EXAMPLE MESSAGE

```
Warning: Line 94, A bundle is not supported in the memory group. (LIBG-195)
```

LIBG-196 (error) The inverted_output attribute is not defined in the ’%s’ output port.

DESCRIPTION

Library Compiler uses the **inverted_output** attribute value to determine whether a sequential output pin is inverting or noninverting.

WHAT NEXT

Make sure each inout and output pin has its "inverted_output" attribute set.

EXAMPLES

```
cell(libg202) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }
  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\

     -   ~R : - - : N   N";
  }
```

```
  pin(Q) {
    direction : output;
/*    inverted_output : FALSE; */
    internal_node : "Q";
  }
  pin(QB) {
    direction : output;
    inverted_output : TRUE;
    internal_node : "QB";
  }
}
```

In this case, set the inverted_output value to FALSE in the port 'Q' to construct the correct logic for the Design Compiler.

EXAMPLE MESSAGE

Error: Line 127, The inverted_output attribute is not defined in the 'Q' output por t. (LIBG-196)

LIBG-197 (warning) In the '%s' cell, the '%s' and '%s' memory read or memory write ports have the same address attribute.

DESCRIPTION

This message indicates that the same address attribute is used for both of the specified memory read or memory write ports. Each port must have a unique address attribute.

WHAT NEXT

Edit the cell description so that the specified ports have unique address attributes.

EXAMPLES

```
cell (libg197) {
      area : 2300.0;
      memory() {
       type : ram;
       address_width : 10;
       word_width : 8;
      }

      bus (ram_addr) {
       bus_type  : "bus10"; /* defined in the library */
```

```
      direction : input;
      capacitance : 1.0;
    }
    bus (data_in) {
      bus_type   : "bus8"
      direction : input;
      capacitance : 1.0;
      memory_write() {
         address : ram_addr;
         enable : WR;
      }
    }
    pin (WR) {
      direction : input;
      capacitance : 1.0;
      clock : true;
    }
    pin (EN) {
      direction : input;
      capacitance : 1.0;
    }

    bus(data_out){
      bus_type  : "bus8";
      direction : inout;
      three_state : "EN";
      memory_read() {
        address : ram_addr;
      }
      memory_write() {
         address : ram_addr;
         enable : WR;
      }
   }
}
```

In this case, the ports 'data_in' and 'data_out' have the same address attribute for the memory_write group. This message is displayed for each element of the bus data_in and the bus data_out.

EXAMPLE MESSAGE

```
Warning: Line 38, In the 'libg197' cell, the 'data_in[0]' and 'data_out[0]'
memory read or memory write ports have the same address attribute. (LIBG-197)
```

LIBG-198 (error) The '%s' pin of the '%s' design must be an

’%s’.

DESCRIPTION

By definition, a pin in the **related_pin** attribute for timing constraints must be a input pin.

WHAT NEXT

Check your library for a wrong pin in the **related_pin** attribute or for an incorrect **timing_type**.

EXAMPLE MESSAGE

Error: Line 153, The ’P’ pin of the ’libg198’ design must be an ’input’. (LIBG-198)

LIBG-199 (error) The ’%s’ input port in the ’%s’ cell cannot have timing arcs.

DESCRIPTION

Input ports cannot have timing arcs. There is a possible problem in the direction of the pin, which should be output or inout.

WHAT NEXT

Check your library for a pin with a wrong direction. Change the direction to output or inout.

EXAMPLE MESSAGE

Error: Line 53, The ’D’ input port in the ’libg199’ cell cannot have timing arcs. (LIBG-198)

LIBG-201 (error) The min_period and min_pulse_width attributes are not allowed on the ’%s’ port in the ’%s’ cell.

DESCRIPTION

This message indicates that the specified port has a **min_period**, **min_pulse_width_high**, or **min_period_width_low** attribute. These attributes are allowed only on clock enable ports.

WHAT NEXT

Update the technology library source to remove the offending attributes.

LIBG-202 (information) In the '%s' cell, the '%s' internal pin is replaced with the inverted '%s' output pin.

DESCRIPTION

This message indicates that the specified internal pin is an inversion of the output pin. The internal pin is replaced by the inverted output pin. This deletion is done without affecting the functionality of the cell. An internal pin that is never visible is functionally useless. Every internal pin must have a unique functional relationship with an output port.

WHAT NEXT

Either delete the internal pin or give it a unique functional relationship with an output port.

EXAMPLES

```
cell(libg202) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }
  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\

     -   ~R : - - : N   N";
  }

  pin(Q2) {
    direction : internal ;
    internal_node : "QB" ;
  }
  pin(Q) {
    direction : output;
    internal_node : "Q";
  }
  pin(QB) {
    direction : output;
    state_function : "Q2'";
```

```
  }
}
```

In this case the internal node ’Q2’ is an inversion of the output ’Q’.

EXAMPLE MESSAGE

```
Information: Line 125, In the ’libg202’ cell, the ’Q2’ internal pin is
replaced with the inverted ’Q’ output pin. (LIBG-202)
```

LIBG-203 (warning) The ’%s’ test cell has no function.

DESCRIPTION

One of the test_cells has no functional description. Each test cell needs a functional description (flip-flop or latch description). This is used to determine the full functionality of the cell and is also used for the command insert_test.

When reading a .db library, Library Compiler creates a full function if there is any test_cell with a functional description. If no test_cells have a functional description and there is no full cell functional description, the cell is converted to a black box.

WHAT NEXT

Modify the library to specify a functional description within the test_cell group. If a full cell has the function description instead, the cell is no longer a black box, but the **insert_test** command will not be able to use the functional description.

LIBG-204 (error) The ’%s’ test cell has no function and the cell is black box.

DESCRIPTION

One of the test_cells has no functional description. Each test cell needs a functional description (ff or latch description). This is used to determine the full function of the cell and is also used for the command insert_test.

This cell becomes a black box and read_lib cannot proceed with reading the library if this error is found.

WHAT NEXT

Specify a functional description within the test_cell. If you specify a full cell description instead, the cell is no longer a black box but insert_test cannot use

the functional description.

LIBG-205 (warning) Cell(%s): The function cannot be recognized during functional optimization by Design Compiler.

DESCRIPTION

This message informs you that Library Compiler fails to map the state table description of the cell to the flip-flop or latch group description due to complexity of the function. Therefore, it cannot be recognized by Design Compiler. This cell becomes a black box cell during synthesis. However, it might not be a black box cell to DFT Compiler or other tools, depending on its test_cell description if there is one, for example.

WHAT NEXT

Ignore this message if the intended function cannot be described in v3.1 flip-flop or latch syntax. Otherwise, correct the state table function.

EXAMPLES

```
cell(libg205) {
  area : 16;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CP) {
    direction : input;
    capacitance : 2;
  }
  pin (Q0) {
    direction : output;
    internal_node : "Q";
    input_map : "D CP";
    ...
  }
  pin (Q1) {
    direction : output;
    internal_node : "Q";
    input_map : "Q0 CP";
    ...
  }
  pin (Q2) {
    direction : output;
    internal_node : "Q";
    input_map : "Q1 CP";
    ...
```

```
  }
  pin (Q3) {
    direction : output;
    internal_node : "Q";
    input_map : "Q2 CP";
    ...
  }
  statetable( "D CP", "Q QN" ) {
    table : "- ~R : - - : N N,\

              H/L R : - - : H/L L/H";
  }
}
```

In this case, the cell cannot be modeled in v3.1 format and the warning message should be ignored.

EXAMPLE MESSAGE

```
Warning: Line 21, Cell(libg205): The function cannot be
recognized by Design Compiler. The cell becomes a black box.  (LIBG-205)
```

LIBG-206 (warning) The logic represented by the ’when’ string (%s) in this %s group is equivalent to logic %s.

DESCRIPTION

The logic represented by the ’when’ string of state-dependent internal_power and leakage_power groups should not be logically equivalent to logic 0 or logic 1.

A power table with its ’when’ condition equivalent to logic 0 is meaningless because it will always be ignored during power calculation.

A power table with its ’when’ condition equivalent to logic 1 is valid all states and is therefore not state dependent. It should be represented by a power table without the ’when’ condition.

WHAT NEXT

Check the ’when’ conditions in the internal power or leakage power group and check that that are not equivalent to logic 0 or 1. Since such condition values are typically meaningless, the power tables may have been characterized incorrecly. ’when’ strings with conditons equivalent to logic 1 should be removed. Power tables with conditions equivalent to logic 0 should be removed. This warning may be promoted to an error in future releases.

LIBG-207 (error) The logic represented by the 'when' string (%s) in this %s group is not mutually exclusive with the logic represented by the 'when' string (%s) in the %s group on line %d.

DESCRIPTION

The logic represented by the 'when' string of all state-dependent or path-dependent internal_power groups between a pair of pins should be mutually exclusive. If it is not, Library Compiler is not be able to determine which internal_power group to use when propagating a signal through the path, if the condition causes both of them to be evaluated 'TRUE'.

The logic represented by the 'when' string of all state-dependent leakage_power groups should be mutually exclusive. If it is not, Library Compiler is not be able to determine which leakage_power group to use if the condition cause more than one condition to be evaluated 'TRUE'.

WHAT NEXT

Check the 'when' strings of both timing groups for wrong information and fix.

EXAMPLES

```
    cell(libg44) {
      area : 2;
      pin(D1 D0 S0) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "S0'D0 + S0 D1";
timing() {
  timing_sense : non_unate;
  intrinsic_rise : 1.00;
  intrinsic_fall : 1.00;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : " D0 D1";
}
timing() {
  when : "S0'D0 + S0 D1'";
  when : "D1' S0 + S0'D0 ";
  sdf_cond : "(D1 == 1'b0 && S0 == 1'b1) || (S0 == 1'b0 && D0 == 1'b1)";
  timing_sense : positive_unate;
  intrinsic_rise : 1.00;
  intrinsic_fall : 1.00;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
```

```
  related_pin : "S0";
}
timing() {
  when : "D1 S0 + S0'D0";
  sdf_cond : "(D1 == 1'b1 && S0 == 1'b1) || (S0 == 1'b0 && D0 == 1'b0)";
  timing_sense : non_unate;
  intrinsic_rise : 0.1;
  intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "S0";
}
timing() { /* default */
  intrinsic_rise : 1.00;
  intrinsic_fall : 2.00;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "S0";
}
      }
    }
```

In this case, the second when attribute's string has a typographical error. It should be "D1 S0 + S0'D0'"; where the pin D0 should be ticked according to the sdf_cond attribute's string.

EXAMPLE MESSAGE

```
Error: Line 258, The logic represented by the 'when' string (S0'D0 + S0 D1') in this
        timing group is not mutually exclusive with the logic represented by
        the 'when' string (D1 S0 + S0'D0) in the timing group on line 268. (LIBG-
44)
```

LIBG-208 (warning) Different number of pins on the '%s' test_cell are found.
The test_cell is removed.

DESCRIPTION

The cell and its associated test_cell must have the same number of pins.

This warning informs you that the test_cell pointed to has a different number of pins than its parent cell.

WHAT NEXT

Check the library description to ensure that each test_cell has the same number of pins as the parent cell.

EXAMPLES

```
    cell(lbdb128) {
      area : 13;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(G) {
direction : input;
capacitance : 2;
      }
      pin(D2) {
direction : input;
capacitance : 1;
      }
      pin(C2) {
direction : input;
capacitance : 2;
      }
      pin(Q) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "G C2";
}
      }
      pin(QN) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "G C2";
}
      }
      test_cell() {
pin(D) {
  direction : input;
}
pin(G) {
  direction : input;
}
pin(D2) {
  direction : input;
  signal_type : "test_scan_in";
}
pin(C2) {
  direction : input;
```

```
  signal_type : "test_scan_clock";
}
pin(SE) {
  direction : input;
  capacitance : 2;
  signal_type : "test_scan_enable";
}
state ("IQ","IQN") {
  force_01 : "G D'";
  force_10 : "G D";
}
pin(Q) {
  direction : output;
  function : "IQ";
  signal_type : "test_scan_out";
}
pin(QN) {
  direction : output;
  function : "IQN";
  signal_type : "test_scan_out_inverted";
}
      }
    }
```

In this case, the 'SE' pin is defined in the test_cell, but it is not defined in the parent cell. To fix the problem, add the definition,

```
      pin(SE) {
direction : input;
capacitance : 2;
      }
```

EXAMPLE MESSAGE

```
Warning: Line 124, Different number of pins on the 'lbdb128' cell are found.
        The test_cell is removed. (LIBG-208)
```

LIBG-209 (warning) Unable to find the '%s' pin on the '%s' test_cell.
The test_cell is removed.

DESCRIPTION

This message indicates that you specified a different pin name in the cell and its associated test_cell. This might be caused by a typo. The Library Compiler ignores the associated test_cell.

WHAT NEXT

Check the library description to ensure that each test_cell has the same number of pins as the parent cell.

EXAMPLES

```
    cell(lbdb129) {
      area : 13;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(G) {
direction : input;
capacitance : 2;
      }
      pin(D2) {
direction : input;
capacitance : 1;
      }
      pin(C2) {
direction : input;
capacitance : 2;
      }
      pin(SE) {
direction : input;
capacitance : 2;
      }
      pin(Q) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "G C2";
}
      }
      pin(QN) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "G C2";
}
      }
      test_cell() {
pin(D) {
  direction : input;
}
```

```
pin(G) {
  direction : input;
}
pin(D2) {
  direction : input;
  signal_type : "test_scan_in";
}
pin(C2) {
  direction : input;
  signal_type : "test_scan_clock";
}
pin(SEB) {
  direction : input;
  capacitance : 2;
  signal_type : "test_scan_enable";
}
latch ("IQ","IQN") {
  data_in : "D";
  enable : "G";
}
pin(Q) {
  direction : output;
  function : "IQ";
  signal_type : "test_scan_out";
}
pin(QN) {
  direction : output;
  function : "IQN";
  signal_type : "test_scan_out_inverted";
}
      }
    }
```

In this case, a pin is named 'SE' at the cell level and 'SEB' at the test_cell level. To fix the problem, give the pin the same name.

EXAMPLE MESSAGE

```
Warning: Line 124, Unable to find the 'SE' pin on the 'lbdb129' test_cell.
        The test_cell is removed. (LIBG-209)
```

LIBG-210 (error) The '%s' pin of the '%s' cell has conflicting signal_types between the cell and the test_cell.

DESCRIPTION

This message indicates that you specified conflicting signal_type attributes for the same pin on different test_cell groups.

WHAT NEXT

Check the library description to ensure that each test_cell has no conflicting signal_type attributes on its pins.

EXAMPLES

```
    cell(lbdb131) {
      area : 13;
      pin(D) {
direction : input;
capacitance : 1;
      }
      pin(G) {
direction : input;
capacitance : 2;
      }
      pin(D2) {
direction : input;
capacitance : 1;
      }
      pin(C2) {
direction : input;
capacitance : 2;
      }
      pin(SE) {
direction : input;
capacitance : 2;
      }
      pin(Q) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "G C2";
}
      }
      pin(QN) {
direction : output;
timing() {
  timing_type : rising_edge;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
  related_pin : "G C2";
}
      }
      test_cell() {
pin(D) {
  direction : input;
}
```

```
pin(G) {
  direction : input;
}
pin(D2) {
  direction : input;
  signal_type : "test_scan_in";
}
pin(C2) {
  direction : input;
  signal_type : "test_scan_clock";
}
pin(SE) {
  direction : input;
  capacitance : 2;
  signal_type : "test_scan_enable";
}
state ("IQ","IQN") {
  force_01 : "G D'";
  force_10 : "G D";
}
pin(Q) {
  direction : output;
  function : "IQ";
  signal_type : "test_scan_out";
}
pin(QN) {
  direction : output;
  function : "IQN";
  signal_type : "test_scan_out_inverted";
}
      }
      test_cell() {
pin(D) {
  direction : input;
}
pin(G) {
  direction : input;
}
pin(D2) {
  direction : input;
  signal_type : "test_scan_in";
}
pin(C2) {
  direction : input;
  signal_type : "test_scan_clock";
}
pin(SE) {
  direction : input;
  capacitance : 2;
  signal_type : "test_scan_enable_inverted";
}
state ("IQ","IQN") {
  force_01 : "G D'";
  force_10 : "G D";
}
```

```
pin(Q) {
  direction : output;
  function : "IQ";
  signal_type : "test_scan_out";
}
pin(QN) {
  direction : output;
  function : "IQN";
  signal_type : "test_scan_out_inverted";
}
      }
    }
```

In this case, The 'SE' pin has a test_scan_enable signal_type in the first test_cell group and a test_scan_enable_inverted signal_type in the second test_cell group. To fix the problem, make the signal_type consistent between the two test_cell groups.

EXAMPLE MESSAGE

```
Error: Line 94, The 'SE' pin of the 'lbdb131' cell has conflicting signal_types
       between the cell and the test_cell. (LIBG-210)
```

LIBG-211 (warning) Cell '%s' contains unused input pin(s). It is labeled dont_use and dont_touch.

DESCRIPTION

An input pin is unused if it does not appear in any functional statement, or state table input or input map, nor does it have any test signal_type description. Such cells may cause synthesis to generate errouneous logic because of incomplete modeling.

WHAT NEXT

Either delete the unused input pin or add it the functionality of the cell.

EXAMPLES

```
    cell(acell) {
area : 6.50;
pin(CLK) {
direction : input;
capacitance : 1.5;
}
pin(SET) {
direction : input;
capacitance : 3.0;
}
ff("IQ","IQN") {
```

```
next_state : "IQ'";
clocked_on : "CLK";
}
pin(Q) {
direction : output;
function : "IQ";
}
pin(QN) {
direction : output;
function : "IQN";
      }
  }
```

EXAMPLE MESSAGE

```
Warning: Line 202, Cell 'acell' contains unused input pin(s).
It is labeled dont_use and dont_touch. (LIBG-211)
```

LIBG-212 (warning) The logic represented by the '%s' when string in this %s group does not sensitize one or all pins in the '%s' related_pin attribute for the %s function attribute.

DESCRIPTION

This message indicates that the when attribute within an internal_power group does not make sense given the function associated with the output pin. Library Compiler warns you that allowing these extra tables in the library, you are unnecessarily increasing the size of the library and may be characterizing unnecessary data.

WHAT NEXT

Check the 'when' string of internal_power group for wrong information and fix.

EXAMPLES

```
    cell(libg212) {
      area : 2;
      pin(A B) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "A & B";
internal_power() {
  related_pin : "B";
```

```
  when : "!A'";
   ...
}
      }
    }
```

In this case, this internal power table will never be accessed. This is because in order for B to cause Z to change, pin A must be high.

EXAMPLE MESSAGE

```
Warning: Line 191, The logic represented by the '!A' when string in this internal_p
ower group
        does not sensitize one or all pins in the 'B ' related_pin attribute for th
e (A & B) function attribute. (LIBG-212)
```

LIBG-213 (warning) The default internal power is not needed for the %s pin.

DESCRIPTION

This message indicates that the set of 'when' attributes is complete for the internal_power and there is no need for the default internal power table.

WHAT NEXT

Check the 'when' string of internal_power groups for wrong information and fix or remove the default internal power group.

EXAMPLES

```
    cell(libg213) {
      area : 2;
      pin(A B) {
direction : input;
capacitance : 1;
      }

       pin ( Z ) {
         direction : output ;
         function : "A & B";
         internal_power () {
   when : "A";
           related_pin : "B";
           power(power_template) {
           values (" 1.000000, 1.000000, 1.000000, 1.000000");
           }
         }
         internal_power () {
```

```
   when : "B";
           related_pin : "A";
           power(power_template) {
           values (" 1.000000, 1.000000, 1.000000, 1.000000");
           }
         }
         internal_power () {
           related_pin : "A B";
           power(power_template) {
           values (" 1.000000, 1.000000, 1.000000, 1.000000");
           }
         }
      }
    }
```

In this case, the default internal power table is not needed. This is because in the when attribute contains all possible paths which will sensitize the related_pin B to the output. Therefore, no default internal power table is needed.

EXAMPLE MESSAGE

Warning: Line 183, The default internal power is not needed for the A pin. (LIBG-213)

LIBG-214 (warning) The default internal power is required for the ’%s’ pin.

DESCRIPTION

This message indicates that the set of ’when’ attributes is not complete for the internal_power and there is a need for the default internal power table.

WHAT NEXT

Check the ’when’ string of internal_power groups for wrong information and fix or add the default internal power group.

EXAMPLES

```
    cell(libg214) {
      area : 2;
      pin(A B) {
direction : input;
capacitance : 1;
      }

       pin ( Z ) {
         direction : output ;
         function : "A & B";
```

```
        internal_power () {
   when : "A";
          related_pin : "B";
          power(power_template) {
          values (" 1.000000, 1.000000, 1.000000, 1.000000");
          }
        }
      }
    }
```

In this case, the default internal power table is needed for the related_pin A. This is because the when attribute does not contain all possible paths which will sensitize the related_pin A to the output. Therefore, you either add the power table associated with the related pin A and a when or add the default internal power table as show below:

either internal_power () { when : "B"; related_pin : "A"; power(power_template) { values (" 1.000000, 1.000000, 1.000000, 1.000000"); } } or internal_power () { related_pin : "B"; power(power_template) { values (" 1.000000, 1.000000, 1.000000, 1.000000"); } }

EXAMPLE MESSAGE

Warning: Line 183, The default internal power is required for the 'A' pin. (LIBG-214)

LIBG-215 (error) The '%s' when condition includes the '%s' related pin.

DESCRIPTION

This message indicates that the 'when' and 'related_pin' attributes contain the same pin. This condition does not make sense because the when attribute is a static state while the related_pin attribute is the transitioning pin.

Note that the 'related_pin' of a pin includes the pin itself.

WHAT NEXT

Check the 'when' and the 'related_pin' strings of the internal_power group for wrong information and fix it.

EXAMPLES

```
    cell(libg215) {
      area : 2;
      pin(A B) {
direction : input;
capacitance : 1;
```

```
      }

       pin ( Z ) {
         direction : output ;
         function : "A & B";
         internal_power () {
   when : "A";
           related_pin : " A B";
           power(power_template) {
           values (" 1.000000, 1.000000, 1.000000, 1.000000");
           }
         }
      }
    }
```

In this case, the internal power table contains the A pin in both the when and the related_pin attributes. Either remove the A pin from the related_pin or change the when statement.

EXAMPLE MESSAGE

Error: Line 183, The ’A’ when condition includes the ’A’ related pin. (LIBG-215)

LIBG-220 (warning) The ’%s’ equation on the ’%s’ cell evaluates to a ’%s’ constant.

DESCRIPTION

This message is generated when Library Compiler encounters a three-stated pin, whose three_state attribute always evaluates to 1.

WHAT NEXT

Verify the cell and check the library description of the offending cell for correctness.

EXAMPLES

```
    cell(libg220) {
area : 6.50;
pin(A) {
direction : input;
capacitance : 1.5;
}
pin(Y) {
direction : output;
function : "A";
three_state : "1";
}
```

```
      }
```

EXAMPLE MESSAGE

```
Warning: Line 218, The 'three_state' equation on the 'libg220' cell evaluates
        to a '1' constant. (LIBG-220)
```

LIBG-221 (warning) Cell %s, referred to by cell %s, does not exist.

DESCRIPTION

The missing cell is referred to by the "single_bit_degenerate" attribute from a multibit cell. This attribute will be removed from the multibit cell.

WHAT NEXT

Correct the attribute value or remove the attribute, or add the required cell in the library.

EXAMPLES

```
  cell(FDBBX4) {
    area : 18;
    single_bit_degenerate : FDBB;
    bus(D) {
      ...
    }
    ...
  }
```

In this case, cell FDBB is not in the library.

EXAMPLE MESSAGE

```
Warning: Line 258, Cell FDBB, referred to by cell FDBBX4, does not exist. (LIBG-221)
```

LIBG-222 (warning) Cell %s, referred to by cell %s, is multibit.

DESCRIPTION

The offending cell is referred to by the "single_bit_degenerate" attribute from a multibit cell. This cell must be a single-bit cell.

WHAT NEXT

Correct the attribute value or remove the attribute, or add the required cell in the library.

EXAMPLES

```
cell(FDBBX4) {
  area : 18;
  single_bit_degenerate : FDBBX2;
  bus(D) {
    ...
  }
  ...
}
```

In this case, cell FDBBX2 is a multibit cell.

EXAMPLE MESSAGE

Warning: Line 58, Cell FDBBX2, referred to by cell FDBBX4, is multibit. (LIBG-221)

LIBG-223 (warning) Cells %s and %s have different interfaces.

DESCRIPTION

The first cell is referred to by the "single_bit_degenerate" attribute from the second cell. These cells must have the same interfaces.

WHAT NEXT

Correct the interfaces.

EXAMPLES

```
cell(FDBBX4) {
  area : 18;
  single_bit_degenerate : FDBB;
  bus(D) {
    ...
  }
  pin(CP) {
  }
  bus(Q) {
  }
}
cell(FDBB) {
  pin(D) {
```

```
    }
    pin(clk) {
    }
    pin(Q) {
    }
  }
```

In this case, bus D and pin D, and bus Q and pin Q are matched. But pin CP and pin clk, are not. To correct, either change clk to CP, or change CP to clk.

EXAMPLE MESSAGE

```
Warning: Line 58, Cells FDBB  and FDBBX4 have different interfaces. (LIBG-223)
```

LIBG-224 (warning) Cell %s has unequal bus or bundle widths.

DESCRIPTION

```
To be eligible for having the "single_bit_degerate" attribute, the cell
      must be a multibit black box, and all buses must have the same width.
```

WHAT NEXT

```
Correct the bus range.
```

EXAMPLES

```
  type (downbus3) {
    base_type : array;
    data_type : bit;
    bit_width : 3;
    bit_from : 2;
    bit_to   : 0;
    downto   : true;
  }
  type (bus4) {
    base_type : array;
    data_type : bit;
    bit_width : 4;
    bit_from : 0;
    bit_to   : 3;
    downto   : true;
  }

  cell(FDBBX4) {
```

```
    area : 18;
    single_bit_degenerate : FDBB;
    bus(D) {
      bus_type : downbus3;
      ...
    }
    pin(CP) {
    }
    bus(Q) {
      bus_type : bus4;
    }
  }
```

In this case, bus D has pin from 3 to 0, bus bus Q has range from 0 to 3.

EXAMPLE MESSAGE

Warning: Line 224, Cell FDBBX4 has unequal bus or bundle widths.(LIBG-224)

LIBG-225 (warning) Errors have been detected. The single_bit_degenerate attribute is removed from cell %s.

DESCRIPTION

The single_bit_degenerate attribute is removed from the cell because there is an error regarding the attribute specification on this cell or related cell.

WHAT NEXT

To specify "single_bit_degenerate" on a cell, the cell must satisfy:

It is a multibit black box with bused pins (NOT bundled pins)
The bus member must range from 0 to N-1, (N is the width)
The single-bit cell referred to must be a single-bit black box.
The two cells must have identical interface naming.

EXAMPLES

```
cell(FDBBX2) {
  area : 18;
  single_bit_degenerate : FDBB;
  bundle(D) {
    members(D0, D1); ...
  }
  pin(CP) { ...  }
```

```
  bundle(Q) {
    members(Q0, Q1); ...
  }
  bundle(QN) {
    members(Q0N, Q1N); ...
  }
}

cell(FDBB) {
  area : 18;
  pin(D)  { ...  }
  pin(CP) { ...  }
  pin(Q)  { ...  }
  pin(QN) { ...  }
}
```

The single_bit_denerate would be ok if the bundle groups are replaced with bus groups with bus member ranging from 0 to 1.

EXAMPLE MESSAGE

Warning: Line 225, Errors have been detected. Attribute single_bit_degenerate is removed from cell %s. (LIBG-225)

LIBG-226 (warning) Only cell %s has geometry_print %s.

DESCRIPTION

It is of no use to put a geometry_print on a single cell.

WHAT NEXT

Remove it or put it on other cells when appropriate.

EXAMPLES

```
cell(FDBBX2) {
  area : 18;
  geometry_print : GP1;
  bundle(D) {
    members(D0, D1); ...
  }
  pin(CP) { ...  }

  bundle(Q) {
    members(Q0, Q1); ...
  }
  bundle(QN) {
    members(Q0N, Q1N); ...
```

```
  }
}
```

GP1 only appears on FDBBX2.

EXAMPLE MESSAGE

```
Warning: Line 226, Onle cell FDBBX2 has geometry_print GP1. (LIBG-226)
```

LIBG-228 (warning) Failed to transform the function of cell '%s' to a netlist. The cell becomes a black box for Formality.

DESCRIPTION

Library Compiler fails to synthesize a netlist structure representing functionality of this cell. Library Compiler does not accept a derived statetable description when performing this netlist transformation. That is, if the full-function description is not specified in the .lib file, this warning message will be issued. Other causes of failure should have been reported by other warning messages. This netlist structure is referenced by Formality. Without this netlist, Formality can only treat this cell as a black box.

WHAT NEXT

Check the statetable description and make sure it is specified correctly.

LIBG-229 (warning) Cell '%s' has non-disjoint input.

DESCRIPTION

One or more input pins used in the statetable are used in more than one sequential function, such as clock and enable. As a result, this function cannot be transformed by Library Compiler to a netlist structure referenced by Formality.

WHAT NEXT

Check the statetable description and correct all mistakes.

LIBG-230 (warning) Internal pin '%s' is dangling. The pin is

removed.

DESCRIPTION

The internal pin is not associated with any statetable, it does not have a function or a state_function, it is not a memory port, nor is it part of any timing-arc specification. It is redundant and therefore being removed.

WHAT NEXT

You can add the required element if it is accidentally missing. Or a dummy timing arc will serve the purpose of keeping the internal pin interface.

LIBG-231 (information) Internal pin '%s' is for dcm timing.

DESCRIPTION

The internal pin is labeled for dcm timing use only.

WHAT NEXT

Make sure the pin is used for dcm timing only, not for any other purpose.

LIBG-232 (error) The 'function' attribute on the '%s' internal Pin/ bus of the
'%s' cell is not allowed.

DESCRIPTION

This error is issued when any internal pin of a combinational cell defines a function attribute. In a combinational cell, a function attribute can only be defined on an output pin.

WHAT NEXT

Check your library for wrong attributes.

EXAMPLES

```
cell(libg232) {
  area : 1 ;
  pin (A) {
```

```
direction : input ;
capacitance : 0 ;
  }
  pin (A_INT) {
direction : internal ;
function : A;
capacitance : 0 ;
timing() {
related_pin: "A" ;
intrinsic_rise: 1.0 ;
rise_resistance : 0.0 ;
intrinsic_fall  : 1.0 ;
fall_resistance : 0.0 ;
}
  }
  pin ("Y") {
direction : output ;
function : "A'" ;
timing() {
related_pin: "A_INT" ;
intrinsic_rise: 1.0 ;
rise_resistance : 0.0 ;
intrinsic_fall  : 1.0 ;
fall_resistance : 0.0 ;
}
  }
```

EXAMPLE MESSAGE

```
Error: Line 10, The 'function' attribute on the 'A_INT' internal pin/bus of the
'libg232' cell is not allowed. (LIBG-232)
```

LIBG-233 (error) The 'clock_gate_enable_pin' attribute is defined on more than one pin in the '%s' cell.

DESCRIPTION

This error is issued when the clock_gate_enable_pin attribute is defined on more than one pin in a cell. In a clock gating cell, there should only be at most one pin with the clock_gate_enable_pin attribute defined.

WHAT NEXT

Check your library and remove extra clock_gate_enable_pin attribute.

EXAMPLES

```
cell(libg233) {
  area : 1 ;
  is_clock_gating_cell : TRUE;
  pin (A) {
direction : input ;
capacitance : 0 ;
clock_gate_enable_pin : TRUE;
  }
  pin (B) {
direction : input ;
capacitance : 0 ;
clock_gate_enable_pin : TRUE;
  }
  pin ("Y") {
direction : output ;
function : "A' B'" ;
timing() {
related_pin: "A B" ;
intrinsic_rise: 1.0 ;
rise_resistance : 0.0 ;
intrinsic_fall  : 1.0 ;
fall_resistance : 0.0 ;
}
  }
```

EXAMPLE MESSAGE

```
Error: Line 10, The 'clock_gate_enable_pin' attribute is defined on more than one
pin in the 'libg233' cell. (LIBG-233)
```

LIBG-234 (error) The '%s' cell cannot be used as a clock gating cell.

DESCRIPTION

This error is issued when the is_clock_gating_cell attribute is defined on a cell with disallowed function.

The is_clock_gating_cell attribute can be set on

- 2-input clock gates Examples of 2-input clock gates are AND, NAND, OR, and NOR library cells that are used to gate clocks.

- 1-input cells Examples of 1-input clock gates are buffer and inverter library cells that are used in the fanin and fanout of the 2-input clock gate.

- 2-input D latches These latches can be active high or low and must have a noninverting output.

WHAT NEXT

Check your library and correct the error.

EXAMPLES

```
cell(libg234) {
  area : 1 ;
  is_clock_gating_cell : TRUE;
  pin (A) {
direction : input ;
capacitance : 0 ;
clock_gate_enable_pin : TRUE;
  }
  pin (B) {
direction : input ;
capacitance : 0 ;
  }
  pin (C) {
direction : input ;
capacitance : 0 ;
  }
  pin ("Y") {
direction : output ;
function : "A B C" ;
timing() {
related_pin: "A B C" ;
intrinsic_rise: 1.0 ;
rise_resistance : 0.0 ;
intrinsic_fall  : 1.0 ;
fall_resistance : 0.0 ;
}
  }
```

EXAMPLE MESSAGE

Error: Line 10, The ’libg234’ cell cannot be used as a clock gating cell. (LIBG-234)

LIBG-235 (error) The ’%s’ attribute is either not defined on any pin in the integrated clock gated ’%s’ cell or it is defined on a wrong pin.

DESCRIPTION

This error is issued when the clock_gate_enable_pin or clock_gate_clock_pin or clock_gate_outp_pin attribute is either not defined on any pin in a cell or it is defined on the wrong pin. In a clock gating cell, there should only be at most one pin with the clock_gate_enable_pin or clock_gate_out_pin or clock_gate_clock_pin attribute defined.

WHAT NEXT

Check your library and add the missing clock gate attribute.

EXAMPLES

```
cell(libg235) {
  area : 1;
  clock_gating_integrated_cell : "latch_posedge";
  dont_use : true;
  dont_touch : true;
  statetable(" CP EN ", "IQ ") {
     table : " L  L  : - : L ,
               L  H  : - : H ,
               H  -  : - : N ";
  }
  pin(IQ) {
    direction : internal;
    internal_node : "IQ";
  }
  pin(EN) {
    direction : input;
    capacitance : 1.0;
  }
  pin(CP) {
    direction : input;
    capacitance : 1.0;
    min_pulse_width_low  : 0.319;
    clock_gate_clock_pin : TRUE;
  }
  pin(Z) {
    direction : output;
    state_function : "CP * IQ";
    max_capacitance : 1.0;
    clock_gate_out_pin : TRUE;
  }
```

EXAMPLE MESSAGE

```
Error: Line 10, The 'clock_gate_enable_pin' attribute is either not
defined on any pin in the integrated clock gated 'libg235' cell
or it is defined on a wrong pin. (LIBG-235)
```

LIBG-236 (error) The '%s' clock gate cell has the wrong number

of pins.

DESCRIPTION

This error is issued when the clock_gating_integrated_cell attribute is defined on a cell with disallowed function.

The clock_gating_integrated_cell attribute must have at most two inputs pins and two output pins.

WHAT NEXT

Check your library and correct the error.

EXAMPLES

```
cell(libg236) {
  area : 1;
  clock_gating_integrated_cell : "latch_posedge";
  dont_use : true;
  dont_touch : true;
  statetable(" CP1 EN ", "IQ ") {
     table : " L  L  : - : L ,
               L  H  : - : H ,
               H  -  : - : N ";
  }
  pin(IQ) {
    direction : internal;
    internal_node : "IQ";
  }
  pin(EN) {
    direction : input;
    clock_gate_enable_pin : true;
    capacitance : 1.0;
  }
  pin(CP1) {
    direction : input;
    capacitance : 1.0;
    min_pulse_width_low  : 0.319;
  }

  pin(CP2) {
    direction : input;
    capacitance : 1.0;
    min_pulse_width_low  : 0.319;
  }
  pin(Z) {
    direction : output;
    state_function : "CP1 * IQ";
    max_capacitance : 1.0;
  }
```

EXAMPLE MESSAGE

```
Error: Line 10, The 'libg236' clock gate cell has the wrong number of pins. (LIBG-236)
```

LIBG-237 (error) The '%s' clock gate cell has the wrong type of pins.

DESCRIPTION

This error is issued when the clock_gating_integrated_cell attribute is defined on a cell with the wrong pin types

The clock_gating_integrated_cell attribute expects the following attributes on its pins: - clock_gate_enable_pin - clock_gate_obs_pin - clock_gate_test_pin

WHAT NEXT

Check your library and correct the error.

EXAMPLES

```
cell(libg237) {
  area : 1;
  clock_gating_integrated_cell : "latch_posedge_precontrol";
  dont_use : true;
  dont_touch : true;
  statetable(" CP EN CTL", "IQ ") {
     table : " L  L  L : - : L ,
       L  L  H : - : H ,
               L  H  L : - : H ,
               L  H  H : - : H ,
               H  -  - : - : N ";
  }
  pin(IQ) {
    direction : internal;
    internal_node : "IQ";
  }
  pin(EN) {
    direction : input;
    capacitance : 0.017997;
    clock_gate_enable_pin : true;
  }
  pin(CTL) {
    direction : input;
    capacitance : 0.017997;
  }
  pin(CP) {
    direction : input;
    capacitance : 0.031419;
```

```
    min_pulse_width_low  : 0.319;
  }
  pin(Z) {
    direction : output;
    state_function : "CP * IQ";
    max_capacitance : 0.500;
  }
}
```

The attribute clock_gate_test_pin is missing. You need to add it to the 'CTL' pin.

```
    clock_gate_test_pin : true;
```

EXAMPLE MESSAGE

Error: Line 10, The 'libg237' clock gate cell has the wrong type of pins. (LIBG-237)

LIBG-238 (error) The '%s' clock gate cell is not of type '%s'.

DESCRIPTION

This error is issued when the clock_gating_integrated_cell attribute is defined on a cell with disallowed function.

Check the Library Compiler User Guide for the list of the clock gating integrated cell types.

WHAT NEXT

Check your library and correct the error.

EXAMPLES

```
cell(libg238) {
  area : 1;
  clock_gating_integrated_cell : "latch_posedge";
  dont_use : true;
  dont_touch : true;
  statetable(" CP EN ", "IQ ") {
     table : " L  L  : - : L ,
               L  H  : - : H ,
               H  -  : - : N ";
  }
  pin(IQ) {
    direction : internal;
    internal_node : "IQ";
  }
  pin(EN) {
    direction : input;
    capacitance : 1.0;
```

```
  }
  pin(CP) {
    direction : input;
    capacitance : 1.0;
    min_pulse_width_low  : 0.319;
  }
  pin(Z) {
    direction : output;
    state_function : "CP * IQ * EN";
    max_capacitance : 1.0;
  }
```

EXAMPLE MESSAGE

```
Error: Line 10, The 'libg238' clock gate cell is not of type 'latch_pos'. (LIBG-238)
```

LIBG-239 (information) The timing arc from '%s' to '%s' is resolved into the three_state_enable type.

DESCRIPTION

The timing arc is entered as combitional/sequential. But the related pin is a fanin to the three_state function only.

WHAT NEXT

Add "timing_type : three_state_enable;" to the timing group. Or check if this arc is intended for three_state_enable.

LIBG-240 (warning) The phase relationship of the outputs of cell '%s' is different from that of its test cell at line %d.

DESCRIPTION

The two outputs of the full cell are equal, but the outputs of the test cell are opposite; or vice versa.

WHAT NEXT

If you intended that the outputs of the full cell differ from the outputs of the test cell, no action is required. Otherwise, change the specification of one of the

cells so that they agree.

EXAMPLE

```
  cell (SCAN) {
    ff(IQ, IQN) {
      ...
    }
    pin (Q1) {
      direction : output;
      function  : IQ;
      ...
    }
    pin (Q2) {
      direction : output;
      function  : IQ;
      ...
    }
    ...
    test_cell() {
      ff(IQ, IQN) {
        ...
      }
      pin (Q1) {
        direction : output;
        function  : IQ;
        ...
      }
      pin (Q2) {
        direction : output;
        function  : IQN;
        ...
      }
      ...
    }
  }
```

EXAMPLE MESSAGES

```
Warning: Line 200, The phase relationship of the outputs of cell 'SCAN'
is different from that of its test cell at line %300. (LIBG-240)
```

LIBG-241 (warning) The '%s' cell has %d pins which exceeds the limit 16.
The state table is not generated.

DESCRIPTION

The cell has over 16 pins. There is an exponential cose in performance and memory as

the number of pins increases. This warning tells the user about the excessive size of the table that is being generated.

WHAT NEXT

If possible, take advantage of the state table group and the input_map attribute to reduce the size of the table.

EXAMPLES

```
cell (libg241) {
latch(iq,iqn) {
    data_in : "((c1 *d1_b') +(c2 *d2_b') +(c3 *d3_b') +(c4 *d4_b') +(c5 *d5_b') +(c
6 *d6_b') +(c7 *d7_b') +(c8 *d8_b') +(c9 *d9_b') +(c10 *d10_b') +(c11 *d11_b') + (c
12 * d12_b'))" ;
    enable : "(c1 +c2 +c3 +c4 +c5 +c6 +c7 +c8 +c9 +c10 +c11 +c12)" ;
    clear : "!rb";
    preset : "s";
    clear_preset_var1 : "L";
    clear_preset_var2 : "H";
}

      pin ( q ) {
         direction : output ;
         function : "iq";
        timing () {
            related_pin : "d1_b d2_b d3_b d4_b d5_b d6_b d7_b d8_b
d9_b d10_b d11_b d11_b " ;
            cell_rise ( prop1 ) {
               values ("0.102565, 0.092949, 0.117635, 0.129560");
            }
            rise_transition ( trans1 ) {
               values ("0.090691, 0.085401, 0.117467, 0.143013");
            }
            cell_fall ( prop1 ) {
               values ("0.099571, 0.101830, 0.122101, 0.129110");
            }
            fall_transition ( trans1 ) {
               values ("0.100989, 0.083367, 0.104448, 0.185206");
            }
         }

         timing () {
            related_pin : "c1 c2 c3 c4 c5 c6 c7 c8 c9 c10 c11 c12" ;
            cell_rise ( prop1 ) {
               values ("0.101839, 0.105114, 0.140100, 0.165207");
            }
            rise_transition ( trans1 ) {
               values ("0.097529, 0.087806, 0.104830, 0.119332");
            }
            cell_fall ( prop1 ) {
               values ("0.117794, 0.121551, 0.145506, 0.159811");
            }
            fall_transition ( trans1 ) {
```

```
            values ("0.099574, 0.088423, 0.085064, 0.108336");
         }
         timing_type : rising_edge ;
      }

      timing () {
        related_pin : "s" ;
         cell_rise ( prop1 ) {
            values ("0.111990, 0.110565, 0.144589, 0.173835");
         }
         rise_transition ( trans1 ) {
            values ("0.102461, 0.097734, 0.129652, 0.175103");
         }
         timing_type : preset ;
         timing_sense : positive_unate ;
      }

      timing () {
         related_pin : "rb" ;
         cell_fall ( prop1 ) {
            values ("0.135732, 0.139003, 0.193663, 0.182614");
         }
         fall_transition ( trans1 ) {
            values ("0.090745, 0.091247, 0.107943, 0.171294");
         }
         timing_type : clear ;
         timing_sense : positive_unate ;
      }
   }

   pin(d1_b d2_b d3_b d4_b d5_b d6_b d7_b d8_b d9_b d10_b d11_b d12_b rb s){
      direction : input ;
      capacitance : 0.1 ;

   }

    pin ( c1 c2 c3 c4 c5 c6 c7 c8 c9 c10 c11 c12) {
      direction : input ;
      capacitance : 0.1 ;
      clock : true ;
   }
}
```

EXAMPLE MESSAGE

```
Warning: The 'libg241' cell has 26 pins which exceeds the limit of 16.

The state table is not generated. (LIBG-241)
```

LIBG-242 (warning) The '%s' cell has pins with 'x_function'

attribute and
it becomes a black box.

DESCRIPTION

For combinational cells with x function, th function id is set to be "unknown".

WHAT NEXT

Make sure the description is correct.

EXAMPLES

```
cell(test) {
  area : 1;
  pin(A) {
    direction : input;
    capacitance : 0;
  }
  pin(B) {
    direction : input;
    capacitance : 0;
  }
  pin(O) {
    direction : output;
    function : "A'";
    x_function : "B";
  }
}
```

EXAMPLE MESSAGE

```
Warning: Line 34, The 'test' cell has pins with 'x_function' attribute and
it becomes a black box. (LIBG-242)
```

LIBG-243 (warning) The '%s' cell is missing the "nextstate_type" attribute
for some input pin(s) specified in 'next_state" of its ff/ff_bank group.

DESCRIPTION

In a pin group, nextstate_type defines the type of a next_state attribute to be used in an ff group, a seq group, or a ff_bank group.

This message is generated when the attribute ’nextstate_type’ is not defined in the input pin inclued in the next_state attribute from the cell’s sequential state description.

WHAT NEXT

Check your library for each input pin used in the next_state statement of a sequential group and add nextstate_type attribute if it does not have it.

EXAMPLES

```
   cell(libg243) {
area : 6.50;
pin(D) {
   direction : input;
   capacitance : 3.0;
}
pin(CLK) {
   direction : input;
   capacitance : 1.5;
}
pin(SET) {
   direction : input;
   nextstate_type : scan_in;
   capacitance : 3.0;
}

ff("IQ","IQN") {
   next_state : "D CLK";
   clocked_on : "CLK";
   preset     : "SET’";
}

pin(Q) {
   direction : output;
   function : "IQ";
}
pin(QN) {
   direction : output;
   function : "IQN";
}
   }
```

EXAMPLE MESSAGE

```
Warning: Line 153, The ’libg243’ cell is missing the "nextstate_type" attribute
for some input pin(s) specified in ’next_state" of its ff/ff_bank group. (LIBG-243)
```

LIBG-244 (warning) The values for clear_preset_var1 and clear_preset_var2 in the ’%s’ cell are opposite.

This may cause incorrect DC optimization.

DESCRIPTION

WHAT NEXT

Change the value of clear_preset_var1 or clear_preset_var2.

EXAMPLES

```
cell(libg111) {
area : 11;
pin(D) {
direction : input;
capacitance : 1;
}
pin(CP) {
direction : input;
capacitance : 1;
}
pin(CLR) {
direction : input;
capacitance : 1;
}
pin(SET) {
direction : input;
capacitance : 1;
}
ff("IQ","IQN") {
next_state : "D";
clocked_on : "CP";
clear   : "CLR'";
preset   : "SET'";
clear_preset_var1 : L;
clear_preset_var2 : H;
}
pin(Q) {
direction : output;
function : "IQ";
timing() {
timing_type : rising_edge;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "CP";
}
            timing() {
timing_type : clear;
      timing_sense : positive_unate;
      intrinsic_fall : 1.0;
      fall_resistance : 0.1;
```

```
      related_pin : "CLR";
      }
            timing() {
      timing_type : preset;
      timing_sense : negative_unate;
      intrinsic_fall : 1.0;
      fall_resistance : 0.1;
      related_pin : "SET";
      }
}
pin(QN) {
direction : output;
function : "IQN";
timing() {
timing_type : rising_edge;
intrinsic_rise : 1.0;
intrinsic_fall : 1.0;
rise_resistance : 0.1;
fall_resistance : 0.1;
related_pin : "CP";
}
            timing() {
      timing_type : preset;
      timing_sense : negative_unate;
      intrinsic_fall : 1.0;
      fall_resistance : 0.1;
      related_pin : "CLR";
      }
            timing() {
      timing_type : clear;
      timing_sense : positive_unate;
      intrinsic_fall : 1.0;
      fall_resistance : 0.1;
      related_pin : "SET";
      }
      }
}
```

Change the value of clear_preset_var1 to H or the value of clear_preset_var1 to L.

EXAMPLES

```
Warning: Line 244, The values for clear_preset_var1 and

      clear_preset_var2 in the 'libg111' cell are opposite.

      This may cause incorrect DC optimization. (LIBG-244)
```

LIBG-245 (information) Cell(%s) test scan type is %s. DFT Compiler
should be able to infer this cell during compile -scan.

It is not a black box for DFT Compiler.

DESCRIPTION

Library Compilier recognizes test scan type for the scan cell according to its test_cell description.

WHAT NEXT

report_lib also reports scan type for test scan cell.

LIBG-246 (warning) Cell(%s) test scan type is not recognized by Library Compiler. It becomes a black box for DFT Compiler.

DESCRIPTION

Library Compiler fails to recognize test scan type of the scan cell according to its test_cell description.

WHAT NEXT

Check the signal type of each pin in test_cell description and correct it if it is wrong.

LIBG-247 (error) In test_cell of Cell(%s) clocked_on pin's polarity is opposite from the cell's definition.

DESCRIPTION

The test_cell's non-test mode behavior has to be consistent with what is defined in the cell section. Library Compiler detects that the clocked_on pin in test_cell has opposite polarity than the cell's defintion.

WHAT NEXT

Correct test_cell's clocked_on pin's polarity to be consistent with the cell.

EXAMPLE

```
cell (TNB) {
          ff ("IQ","IQZ")  {
     next_state : " (D SCAN') + (SD SCAN) ";
```

```
            clocked_on : "CLK'";
        }
  test_cell() {
            ff ("IQ","IQZ")  {
            next_state : "D";
            clocked_on : "CLK";
          }
          ...
}
```

In this case the cell TNB is falling-edge triggered but its test_cell describes a rising-edge triggered flip-flop.

LIBG-248 (warning) The '%s' cell's %s groups for %s '%s' do not cover all the states represented by the 'when' string, and the default leakage_power group is not defined for %s '%s', thus 0 will be used as the leakage_power value for the missing states of %s '%s'.

DESCRIPTION

This message indicates the leakage_power information defined in a cell does not cover all the states for the power_level(power_rail value). For the missing states of the power_level, 0 will be used as the leakage_power value.

It is also used to check for related_pg_pin-based leakage_power information.

WHAT NEXT

Add the missing leakage_power information for the power_level.

EXAMPLES

```
  cell(AN2) {
      leakage_power () {
power_level : "VDD1";
when : "A";
value : 1.0;
      }
      leakage_power () {
power_level : "VDD1";
when : "!A";
value : 1.5;
      }
      leakage_power () {
```

```
power_level : "VDD2";
when : "A";
value : 1.0;
      }
      ...
  }
```

In this case, the leakage_power for the state '!A' of power_level 'VDD2' is missing, . To fix the problem, add the leakage_power for the missing state in the cell group:

```
  cell(AN2) {
      leakage_power () {
        power_level : "VDD1";
        when : "A";
        value : 1.0;
      }
      leakage_power () {
        power_level : "VDD1";
        when : "!A";
        value : 1.5;
      }
      leakage_power () {
        power_level : "VDD2";
        when : "A";
        value : 1.0;
      }
      leakage_power () {
        power_level : "VDD2";
        when : "!A";
        value : 1.2;
      }
      ...
  }
```

EXAMPLE MESSAGE

```
Warning: Line 12, The 'AN2' cell's leakage_power groups for power_level 'VDD2'
do not cover all the states represented by the 'when' string, and the default
leakage_power group is not defined for power_level 'VDD2', thus 0 will be used as
the leakage_power value for the missing states of power_level 'VDD2'. (LIBG-248)
```

LIBG-249 (error) The '%s' cell does not specify the %s group with the 'when' string (%s) for the power_level '%s'.

DESCRIPTION

This message indicates the leakage_power information defined in a cell does not cover the state('when' string) for the power_level(power_rail value). For the power-level specific leakage power modeling, for each 'when' statement which appears in the leakage_power groups of a cell, there must exist a leakage_power group with that

'when' statement for every modeled power_level.

The same rule applies for the internal_power groups.

WHAT NEXT

Add the missing leakage_power information for the power_level.

EXAMPLES

```
  cell(AN2) {
      leakage_power () {
power_level : "VDD1";
when : "AB";
value : 1.0;
      }
      leakage_power () {
power_level : "VDD1";
when : "!AB";
value : 1.5;
      }
      leakage_power () {
power_level : "VDD2";
when : "AB";
value : 1.0;
      }
      ...
  }
```

In this case, the leakage_power for the state '!AB' of power_level 'VDD2' is missing, . To fix the problem, add the leakage_power for the missing state in the cell group:

```
  cell(AN2) {
      leakage_power () {
        power_level : "VDD1";
        when : "AB";
        value : 1.0;
      }
      leakage_power () {
        power_level : "VDD1";
        when : "!AB";
        value : 1.5;
      }
      leakage_power () {
        power_level : "VDD2";
        when : "AB";
        value : 1.0;
      }
      leakage_power () {
        power_level : "VDD2";
        when : "!AB";
        value : 1.2;
      }
```

```
    ...
  }
```

EXAMPLE MESSAGE

```
Error: Line 12, The 'AN2' cell does not specify the leakage_power group
with the 'when' string (!AB) for the power_level 'VDD2'. (LIBG-249)
```

LIBG-250 (error) The logic represented by the 'when' string (%s) in this %s group is not equal to or mutually exclusive with the logic represented by the 'when' string (%s) in the %s group on line %d.

DESCRIPTION

The logic represented by the 'when' string of all state-dependent or path-dependent internal_power groups between a pair of pins should be either equal or mutually exclusive for different power_levels. If it is not, Power Compiler will not be able to determine correctly which internal_power group to use when propagating a signal through the path.

WHAT NEXT

Check the 'when' strings of both internal_power groups for wrong information and fix.

EXAMPLES

```
    cell(libg44) {
      area : 2;
      pin(D1 D0 S0) {
direction : input;
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "S0'D0 + S0 D1";
...
internal_power() {
  power_level : VDD1;
  when : "S0'D0 + S0 D1'";
  when : "D1' S0 + S0'D0 ";
  related_pin : "S0";

  power(scalar) { values ( "1.0" ); }
```

```
}
internal_power() {
  power_level : VDD2;
  when : "D1 S0 + S0'D0";
  related_pin : "S0";
  power(scalar) { values ( "2.0" ); }
}
      }
    }
```

In this case, the second when attribute's string has a typographical error. It should be "D1 S0 + S0'D0'"; where the pin D0 should be ticked according to the sdf_cond attribute's string.

EXAMPLE MESSAGE

```
Error: Line 258, The logic represented by the 'when' string (S0'D0 + S0 D1') in this
        internal_power group is not equal to or mutually exclusive with the logic r
epresented by
        the 'when' string (D1 S0 + S0'D0) in the internal_power group on line 268.
(LIBG-250)
```

LIBG-251 (error) The '%s' group has conflicting 'related_pin' with the '%s' group on line %d.

DESCRIPTION

The "related_pin" in different internal_power groups with the same power_level of the same pin must not share pins. Similarly, the related_pin in different internal_power groups without power_level definition of the same pin must not share pins.

One exception is that, for the above 2 cases, if the pins specifided in the "related_pin" of the first internal_power are all included in the "related_pin" of the second internal_power, then Library Compiler will issue LBDB-107 warning and the second internal_power will overwrite the first one.

WHAT NEXT

Correct the 'related_pin' strings of both internal_power groups.

EXAMPLES

```
    cell(libg44) {
      area : 2;
      pin(D1 D0 S0) {
direction : input;
```

```
capacitance : 1;
      }
      pin(Z) {
direction : output;
function : "S0'D0 + S0 D1";
...
internal_power() {
  power_level : VDD1;
  related_pin : "S0";

  power(scalar) { values ( "1.0" ); }
}
internal_power() {
  power_level : VDD1;
  related_pin : "S0 S1";
  power(scalar) { values ( "2.0" ); }
}
      }
    }
```

In this case, the second internal_power group's 'related_pin' conlficts with that of the first internal_power group. One fix can be that replacing the 'related_pin' of the second internal_power group from "S0 S1" to "S1".

EXAMPLE MESSAGE

Error: Line 251, The 'internal_power' group has conflicting 'related_pin' with the 'internal_power' group on line 268. (LIBG-251)

LIBG-252 (error) The 'function' of the '%s' pin/bus on the '%s' cell
is not correctly defined.

DESCRIPTION

This error is issued when the function is not correctly defined. A valid function statement in the sequential model must satisfy the following 2 conditions:

For a ff/latch, the noninverted is called teh first variable and the inverted output is called the second variable. A function statement of each primary output must include either the first variable or the second variable.

1. It must include and can only include the the first variable or the second variable or a the valid input pins defined for the cell in addition to the boolean operators.

2. All the component insider the function statement should be separated by a space or spaces.

WHAT NEXT

Make the appropriate correction in your library, as indicated in the error message. For more information on sequential models, refer to the **Library Compiler Reference** and **User Guide Manuals**.

EXAMPLES

```
    cell(libg17) {
area : 6.50;
pin(CLK) {
direction : input;
capacitance : 1.5;
}
pin(SET) {
direction : input;
capacitance : 3.0;
}
ff("IQ","IQN") {
next_state : "IQ'";
clocked_on : "CLK";
preset     : "SET'";
}
pin(Q) {
direction : output;
function : "IQ1";/* wrong, should be IQ */
}
pin(QN) {
direction : output;
function : "IQN";
}
      }
```

EXAMPLE MESSAGE

```
Error: Line 23, The 'function' of the 'Q'  in/bus on the 'libg17' cell
        is not correctly defined. (LIBG-252)
```

LIBG-253 (error) Cell(%s): The '%s' pin is a duplicate of '%s' internal pin.

DESCRIPTION

This message indicates that the specified internal pin is a duplicate of the other relative pin. For statetable-based sequential cells, the "IQ" function can only be defined in an internal pin with internal_node : "IQ".

WHAT NEXT

Combine the information of the two pins into the internal pin and remove the other pin.

EXAMPLES

```
cell(libg253) {

...
            statetable(" CEN CLK ", " IQ  "){
                  table : "
                  L L : - : L ,
                  H L : - : H ,
                  - H : - : N " ;
            }
...
            pin(IQ){
                  direction : internal;
                  internal_node : "IQ";
...
            }
            pin(Y){
                  direction : output;
                  state_function : "IQ";
...
}
...
}
```

In this case, internal pin IQ and pin Y are duplicate. The correct model should be:

```
cell(libg253) {

... statetable(" CEN CLK ", " IQ "){ table : " L L : - : L ,  H L : - : H ,  - H : -
: N " ; } ... pin(IQ){ direction : output; internal_node : "IQ"; ... } ... }
```

EXAMPLE MESSAGE

```
Warning: Line 139, Cell(libg253): The pin 'SOSV' is a duplicate of the 'IQ' interna
l pin. (LIBG-253)
```

LIBG-254 (error) An invalid '%s' %s string in the '%s' cell.

DESCRIPTION

The string given is not valid for representing a boolean logic defined in Synopsys format.

WHAT NEXT

Refer to your Library Compiler Reference Manual to find out the valid format of the string. It is described in the "function simple attribute" under the "Cell Group Description and Syntax".

EXAMPLES

```
  cell(sample) {
  switch_cell_type : coarse_grain;
  area : 1 ;
  pg_pin ("VVDD") {
pg_type : internal_power;
pg_function : "(IO" ;
  }
  ...
```

In this simple case, the closing parenthesis is missing in the function string.

EXAMPLE MESSAGE

Error: Line 400, An invalid ’(IO’ pg_function string in the ’sample’ cell. (LIBG-254)

LIBG-255 (error) A bad ’%s’ pg_pin name in the ’%s’ cell.

DESCRIPTION

This error gets detected during a **read_lib** and an **update_lib** commands. The pg_pin name does not either exist or an previous error in any of the attributes of the pin group is detected. In this case the pg_pin group is not recognized and the pin name is labeled as bad.

WHAT NEXT

Check your library for a wrong pin name in any related attribute or for an incorrect pin group.

EXAMPLES

```
    cell (libg3) {
    pg_pin(VSS) {
pg_type : primary_power;
voltage_name : VSS;
    }
    pg_pin(VDD) {
pg_type : primary_power;
voltage_name : VDD;
```

```
    }
    pg_pin(VVDD) {
pg_type : internal_power;
voltage_name : VDD1;
      pg_function : "E";       /* <-- This is wrong */
    }
 }
```

EXAMPLE MESSAGE

```
Error: Line 426, A bad 'E' pg_pin name in the 'libg3' cell. (LIBG-255)
```

LIBG-256 (error) The '%s' group is overlapping with the '%s' group on line %d.

DESCRIPTION

This message indicates that two **dynamic_current** groups in ccs power are overlapping with each other.

If following three conditions is true, then two groups are considered to be overlapped :

1. Two groups have at least one pin specified in **related_inputs** attribtue is identical.

2. Both have same list of pins specified in **related_outputs** or both have no **related_outputs** attribtue.

3. **When** atrributes specified in both groups are not mutually exclusive, or both groups have no **when** attribute.

WHAT NEXT

Check **related_inputs**, **related_outputs**, and **When** attributes for all **dynamic_current** groups to see if any of them breaks above rules, and make the necessary correction.

EXAMPLES

```
cell(libg256) {
  ...
  pin(A1) {
    direction : input;
    ...
  }
  pin(A2) {
    direction : input;
    ...
  }
```

```
  pin(A3) {
    direction : input;
    ...
  }
  pin(A4) {
    direction : input;
    ...
  }
  pin(A5) {
    direction : input;
    ...
  }
  pin(ZN1) {
    direction : output;
    ...
  }
  pin(ZN2) {
    direction : output;
    ...
  }
  ...
  dynamic_current() {
    when : "A2";
    related_inputs : "A5 A4";
    related_outputs : "ZN2 ZN1";
    switching_group() {
      pg_current(V2) {
      ...
      }
      ...
    }
  }
  dynamic_current() {
    when : "!A1";
    related_inputs : "A4 A3";
    related_outputs : "ZN1 ZN2";
    switching_group() {
      pg_current(V2) {
      ...
      }
      ...
    }
  }
  ...
```

In this case, "A2" and "!A1" specified in two when attributes respectively are not mutually exclusive, pin "A4" is specified in both related_inputs groups, and same list of pins ("ZN1" and "ZN2") is specified in both related_outputs groups. Two dynamic_current are overlapping. You can modify any of these attributes to fix the problem. For example : change "A4 A3" to "A2 A3".

EXAMPLE MESSAGE

```
Error: Line 79, The 'dynamic_current' group is overlapping with the 'dynamic_curren
t' group on line 88. (LIBG-256)
```

LIBG-257 (error) The %s must be set to 0.0 or omitted.

DESCRIPTION

There are two attributes, input_high_value and input_low_value, within a gate_leakage group. The input_high_value is to specify gate leakage current on a pin when this pin is set to high. The input_low_value is to specify gate leakage current on a pin when this pin is set to low. If the 'when' statement inside leakage_current or va_leakage_current implies that the pin high never occurs, then input_high_value shall be set to 0.0 or ignored. If the 'when' statement implies that the pin low shall never occur, then input_low_value must be set to 0.0 or ignored.

WHAT NEXT

Check **input_low_value** and **input_high_value**, and make the necessary correction.

EXAMPLES

```
leakage_current() {
   when : "A1 & A2 & !ZN";
   ...
   gate_leakage(A2) {
     input_high_value : 2.1;
     input_low_value : -1.7;
   }
   gate_leakage(A1) {
     input_high_value : 7.1;
     input_low_value : -8.7;
   }
}
```

In this case, we have when condition "A1 & A2 & !ZN", which means pins A1 and A2 shall never set to low because they will never occur within this leakage_current. So, input_low_value is meaningless for both pins. We shall set both to 0.0 or comment them out.

EXAMPLE MESSAGE

Error: Line 210, The input_low_value must be set to 0.0 or omitted. (LIBG-257)

LIBG-258 (error) No %s is allowed within an intrinsic_parasitic if power_cell_type is %s.

DESCRIPTION

If the power_cell_type is macro, then followings groups can't be specified within an intrinsic_parasitic : state-dependent condition, intrinsic_resistance and

intrinsic_capacitance.

If the power_cell_type is standard cell or there is no power_cell_type specified, then total_capacitance can’t be specified within an intrinsic_parasitic.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell (test) {
  intrinsic_parasitic() {
    when : "!A1 & A2 & !ZN";
    total_capacitance(V2) {
       value : 9.0;
    }
  }
 ...
}
```

In this case, there is no power_cell_type specified under cell "test", meaning power_cell_type is defaulted to standard cell. The total_capacitance is not allowed within an intrinsic_parasitic group.

```
cell (test) {
  power_cell_type : macro;
  intrinsic_parasitic() {
    when : "!A1 & A2 & !ZN";
    intrinsic_resistance(G1) {
       related_output : "ZN";
       value : 9.0;
    }
    intrinsic_capacitance(G1) {
       value : 8.2;
    }
  }
 ...
}
```

In this case, ’when’ attribute, ’intrinsic_resistance’ and ’intrinsic_capacitance’ are not allowed in an ’intrinsic_parasitic’ group because the ’power_cell_type’ is ’macro’.

EXAMPLE MESSAGE

Error Line 272, No intrinsic_resistance is allowed within an intrinsic_parasitic if power_cell_type is macro. (LIBG-258)

LIBG-259 (error) The power_cell_type must be macro if

min_input_switching_count and max_input_switching_count are defined.

DESCRIPTION

If min_input_switching_count and max_input_switching_count are defined within switching_group, then power_cell_type defined in cell must be macro.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell (test) {
 ...
 power_cell_type : stdcell;
 dynamic_current() {
   ...
   switching_group() {
      min_input_switching_count : 1;
      max_input_switching_count : 9;
      ...
   }
   ...
 }
 ...
}
```

In this case, min_input_switching_count and max_input_switching_count both are defined under one of switching_group groups within a dynamic_current, and power_cell_type is standard cell, which is wrong. We shall change "stdcell" to "macro" to avoid the error.

EXAMPLE MESSAGE

Error Line 272, The power_cell_type must be macro if min_input_switching_count and max_input_switching_count are defined. (LIBG-259)

LIBG-260 (error) The logic represented by the %s string is not equal
to or mutually exclusive with the logic represented by the %s

string.

DESCRIPTION

The logic represented by one programmable driver type string must be not equal to or mutually exclusive with the logic represented by other programmable driver types under the same pin.

WHAT NEXT

EXAMPLES

```
cell(libg260) {
 pad_cell : true;
 ...
  pin(A1) {
   direction : input;
   is_pad : true;
  ...}
  pin(A2) {
   direction : input;
   ...}
  pin(A3) {
    direction : input;
   ...}
  pin(ZN1) {
   direction : inout;
   max_capacitance : 0.1;
   pull_up_function : "!A1 * !A2 * !A3";
   pull_down_function : "A1 * A2 * !A3";
   bus_hold_function : "A1 * !A2 * !A3";
   open_drain_function : "!A1 * A2 * !A3";
   open_source_function : "!A1 * !A2 * A3";
   resistive_function : "A1 * A2 * A3";
   resistive_0_function : "A1 * A2";
   resistive_1_function : "!A1 * A2 * A3";
  ...}
}
```

In this case, the resistive_0_function is not mutually exclusive with pull_down_functioni and resistive_function. To fix the problem, you might want to change it as following :

```
resistive_0_function : "A1 * !A2 * A3";
```

EXAMPLE MESSAGE

```
Error: Line 102, The logic represented by the resistive_0_function string is not eq
ual
        to or mutually exclusive with the logic represented by the pull_down_functi
on string. (LIBG-260)
Error: Line 102, The logic represented by the resistive_0_function string is not eq
```

ual
to or mutually exclusive with the logic represented by the resistive_functi
on string. (LIBG-260)

LIBG-261 (error) The programmable driver type can only be defined on a pad cell.

DESCRIPTION

The programmable driver type can only be defined a pad cell, which has either pad_cell or auxiliary_pad_cell attribute.

WHAT NEXT

Check the library source file, and make the necessary correction.

EXAMPLES

```
cell (libg261) {
  ...
  pin (A) {
    direction : input;
    pull_up_function : "p1 * p2";
    ...
  }
 ...}
```

In this case, a programmable driver type, pull_up_function, is defined on pin A, which is under a cell, ligb261. The cell is not a pad cell, which is wrong. To fix the problem, please either add pad_cell attribute under cell level or remove pull_up_function attribute from the pin.

EXAMPLE MESSAGE

Error: Line 94, The programmable driver type can only be defined on a pad cell. (LI
BG-261)

LIBG-262 (information) Cell(%s) is recognized as one-hot mux cell.

DESCRIPTION

This message is issued when a cell is recognized as one-hot mux cell.

One-hot mux cells have following characteristic: 1. Two equal sized, disjoint sets

of input pins, one is select pins(e.g. "S0,S1"), another set is data input pins(e.g. "D0,D1"). 2. Have cell attribute "contention_condition", e.g. Fc = S0'*S1 + S0*S1. That is there could be one and ONLY one select pin can be logic 1, others are logic 0. 3. There is only one output pin defined and its function is defined with respect to all of its inputs, e.g. Fo = S0*D0 + S1*D1;

WHAT NEXT

The one-hot mux cell will be used in DC logical synthesis.

EXAMPLES

```
cell(OHMUX2) {

  ...
  contention_condition : "( S0 S1 + S0' S1' )";
  pin(D0) {
    direction : input;
    capacitance : 1;
  }
  pin(D1) {
    direction : input;
    capacitance : 1;
  }
  pin(S0) {
    direction : input;
    capacitance : 1;
  }
  pin(S1) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "(S0 D0 + S1 D1)";
    ...
  }
}
```

EXAMPLE MESSAGE

Warning: Line 139, Cell(OHMUX2) is recognized as one-hot mux cell.(LIBG-262)

SEE ALSO

LIBG-263

LIBG-263 (warning) Cell(%s) is not recognized as one-hot mux

cell.

DESCRIPTION

This message is issued when there is cell level attribute "contention_condition" defined, but it does not match with output pin function as a one-hot mux cell.

One-hot mux cells have following characteristic: 1. Two equal sized, disjoint sets of input pins, one is select pins(e.g. "S0,S1"), another set is data input pins(e.g. "D0,D1"). 2. Have cell attribute "contention_condition", e.g. Fc = S0'*S1 + S0*S1. That is there could be one and ONLY one select pin can be logic 1, others are logic 0. 3. There is only one output pin defined and its function is defined with respect to all of its inputs, e.g. Fo = S0*D0 + S1*D1;

This warning message is reported in step 3, when it find the output function with restiction of contention function does not match with the function of one-hot mux cell.

WHAT NEXT

If users intend to define the cell as one-hot mux cell, and use it later on in logical synthesis, check the cell contention_condition definition and output pin function, modify to make them match the definition of one-hot mux cell.

If users won't use the cell as one-hot mux cell, just ignore this warning.

EXAMPLES

```
cell(OHMUX2) {

  ...
  contention_condition : "( S0 S1 + S0' S1' )";
  pin(D0) {
    direction : input;
    capacitance : 1;
  }
  pin(D1) {
    direction : input;
    capacitance : 1;
  }
  pin(S0) {
    direction : input;
    capacitance : 1;
  }
  pin(S1) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "(S0 D0 + S1 D1 + D0' D1)";
    ...
```

```
  }
}
```

In this case, the contention function matches with one-hut mux cell select pin restriction, but the output pin function is not a function of one-hot mux cell.

EXAMPLE MESSAGE

Warning: Line 139, Cell(OHMUX2) is not recognized as one-hot mux cell.(LIBG-263)

LIBG-264 (warning) ICG cell '%s' function can not be recognized during functional optimization by Power Compiler.

DESCRIPTION

A cell with attribute "clock_gating_integrated_cell" defined as "generic" is called a generic ICG cell.

Library Compiler will try to resolve ICG type of a generic ICG cell. Valid resolved types are,

latch_(posedge | negedge | posedgeactivelow | negedgeactivelow)_ (precontrol | postcontrol| *)_(obs | *)_(invgclk | *) or none | (posedge | negedge | posedgeactivelow | negedgeactivelow)_ (control | *)_(invgclk | *).

Please refer to Library Compiler User Guide for the corresponding schematics of these types.

If a generic ICG cell can't be resolved as any exact type, Library Compiler will resolve them as blackbox. It means this generic ICG will not be auto inferred by Power Compiler and understood by Formality and other client tools that need to understand the function of such cells.

FF-based ICG cell won't be supported by Power Compiler, either.

WHAT NEXT

Change the cell to be one of the valid ICG types.

EXAMPLES

EXAMPLE MESSAGE

Warning: ICG cell 'cell1' function can not be recognized during functional optimiza tion by Power Compiler. (LIBG-264)

LIBG-265 (information) Derived ICG type for cell ’%s’ is ’%s’.

DESCRIPTION

A cell with attribute "clock_gating_integrated_cell" defined as "generic" is called a generic ICG cell.

Library Compiler will try to resolve ICG type of a generic ICG cell. If successful, the value of attribute "clock_gating_integrated_cell" will be updated.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

Information: Derived ICG type for cell ’cell1’ is ’latch_posedge’. (LIBG-265)

LIBG-266 (warning) The ’data_in_type’ attribute on the ’%s’ pin/bus in the ’%s’ cell is inconsistent with its function. The attribute is ignored.

DESCRIPTION

This warning message occurs when the **data_in_type** attribute does not match the functional information specified in the cell’s sequential state description.

In a pin group, **data_in_type** defines the type of **data_in** attribute to be used in an ff group, a seq group, or a ff_bank group. Any pin with the **data_in_type** attribute must be in the **data_in** function. The tool performs a consistency check between the pin’s **data_in_type** attribute and the **data_in** function and generates this warning when inconsistencies are found.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this warning, check your library for a pin that has a **data_in_type** attribute but is not used in the **data_in** statement of a sequential group. After making your changes, run the command again.

EXAMPLE MESSAGE

```
   Warning: Line 153, The 'data_in_type' attribute on the 'SET' pin/bus in
            the 'libg35' cell is inconsistent with its function. The attribute is ig
nored. (LIBG-266)
```

LIBG-267 (error) The power_down_function attribute should not be specified inside the test_cell's ff/latch/statetable group.

DESCRIPTION

This error message occurs because the **power_down_function** attribute must be specified in a cell's ff/latch/statetable group, not specified inside the test_cell.

WHAT NEXT

Check your library to delete the **power_down_function** attribute in test_cell.

EXAMPLES

The following example results in this error message:

```
      test_cell () {
         pin (Q) {
            direction : output;
            function : "IQ";
            signal_type : test_scan_out;
         }
         pin (CK) {
            direction : input;
         }
         pin (D) {
            direction : input;
         }
         pin (SI) {
            direction : input;
            signal_type : test_scan_in;
         }
         pin (SE) {
            direction : input;
            signal_type : test_scan_enable;
         }
         ff (IQ,IQN) {
            clocked_on : "!(CK)";
```

```
          next_state : "D";
    power_down_function : "!VDD + VSS";/* <-- This is wrong */
         }
      }
```

EXAMPLE MESSAGE

```
Error: Line 426, Cell 'test', The power_down_function attribute should not be
specified inside the test_cell's ff/latch/statetable group. (LIBG-267)
```

LIBSETUP-001 (warning) cell %s(%s) was constrained to operate under the operating condition %s, but the library cell %s matching this characterization has not been used. Instead, library cell %s from %s:%s (voltage = %s, process = %f, temperature = %f) has been used.

DESCRIPTION

This warning message occurs when the specified block or cell has been required to operate under a certain supply voltage (using the **set_operating_conditions** command), but this particular cell cannot be linked to a library cell that was characterized under this supply voltage.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, check the operating condition for the specified block or cell. Set the proper operating condition using the **set_operating_conditions** command or check the library.

SEE ALSO

set_operating_conditions(2)
set_voltage(2)

LIBSETUP-001a (information) The cell %s with library cell %s is a %s.

DESCRIPTION

This information message appears after a LIBSETUP-001 message occurs. The message informs you of the type of the specified cell. The cell can be any of the following:

- isolation cell
- level-shifter cell
- switch cell
- retention register cell
- normal cell

The normal cells are not power-design specific cells, which includes standard cells and macro cells.

WHAT NEXT

This is an information-only message. No action is required.

SEE ALSO

MV-001(n)

LIBSETUP-001b (information) Library cell %s from %s:%s (voltage = %s, process = %f, temperature = %f) has been found.

DESCRIPTION

This information message appears after a LIBSETUP-001 message occurs. The message helps to identify the cause of the earlier LIBSETUP-001 message, whether it was due to a library setup issue or a problem with the tool. This message reports, one at a time, the related library cell found in both the target and the link library with its supply voltage information.

WHAT NEXT

This is an information-only message. No action is required.

However, you can check all LIBSETUP-001b messages against the previous LIBSETUP-001 message to make sure the library setup is correct.

SEE ALSO

LIBSETUP-001(n)

LIBSETUP-022 (Error) A total of %d operating condition problems (LIBSETUP-001) have been detected; %d of them have been reported above. Delay calculation will be incorrect if these problems are not fixed. %s

DESCRIPTION

This is a summary message for a number of operating condition problems (LIBSETUP-001) detected in the design linking, check_mv_design, or compile/physopt commands. It tells you how many operating condition problems have been detected by the tools, and what libraries have been searched in a prior attempt to link the design.

WHAT NEXT

Check the operating condition for the particular block or cell. Set the proper operating condition using the **set_operating_conditions** command or check the library.

SEE ALSO

set_operating_conditions(2)

LIBSETUP-751 (information) Apply operating condition %s (voltage = %s, process = %f, temperature = %f) to cell %s.

DESCRIPTION

This information message occurs when an operating condition is automatically applied to a cell. For each type of operating condition a maximum of 10 messages are allowed by default. Use the **libsetup_max_auto_opcond_message** variable to change the total number of allowed messages.

WHAT NEXT

This is an information-only message. No action is required.

However, the automatic application of the operating condition might have eliminated some LIBSETUP-001 errors previously shown. You can use the **check_mv_design** command to display the updated list of LIBSETUP-001 errors.

Also, if you do not want automatically-applied operating conditions, use the **set_operating_conditions** command to prevent the automatic application of operating conditions by the tool.

SEE ALSO

set_operating_conditions(2)
libsetup_max_auto_opcond_message(3)

LIBSETUP-752 (information) A total of %d operating condition inferences (LIBSETUP-751) have occurred, %d of them have been reported above.

DESCRIPTION

This is a summary message for LIBSETUP-751 information messages.

WHAT NEXT

This is an information-only message. No action is required.

However, for each type of operating condition a maximum of 10 messages are allowed by default. You can use the **libsetup_max_auto_opcond_message** variable to change the total number of reported messages.

SEE ALSO

libsetup_max_auto_opcond_message(3)

LIBSETUP-753 (warning) Invalid value of '%s' for variable '%s'. The previous value of '%s' is assumed by the tool.

DESCRIPTION

Invalid value have been set for an opcond inference level. The invalid value has been ignored, and the previous value for the variable assumed to be applicable during opcond inference.

WHAT NEXT

Lookup the supported values for the respective opcond inference level, and reset the variable to one of its supported value so that this message is not shown.

SEE ALSO

libsetup_pad_opcond_inference_level
libsetup_macro_opcond_inference_level

LIBSETUP-754 (information) A total of %d operating conditions have been inferred.

DESCRIPTION

This message prints the total number of inferred operating conditions on cells. If there are multiple scenarios, operating conditions can be inferred on the same cell for different scenarios. This is in addition to the LIBSETUP-751 message that prints detailed information. However, these messages are limited to 10 by default and LIBSETUP-754 provides a quick summary of how many cells have inferred operating conditions.

WHAT NEXT

This is an information-only message. No action is required.

However, the automatic application of operating conditions might have eliminated some LIBSETUP-001 errors previously shown. You can use the **check_mv_design** command to display the updated list of LIBSETUP-001 errors.

Also, if you do not want automatically-applied operating conditions, change the operating condition inference level.

SEE ALSO

libsetup_macro_opcond_inference_level(3)
libsetup_pad_opcond_inference_level(3)
libsetup_switch_opcond_inference_level(3)

LICSVR

LICSVR-1 (error) Variable '%s' has invalid value '%s'. Allowed values are: 'package', 'individual', 'package individual' and 'individual package'.

DESCRIPTION

WHAT NEXT

LICSVR-2 (error) Could not obtain a license.

DESCRIPTION

The license for the feature being run could not be obtained.

WHAT NEXT

Check the key file to see if the feature exists. Check the location of the keyfile, either the default location or at $SYNOPSYS_KEY_FILE. It could also be that all the licenses are in use.

LICSVR-3 (error) SYNOPSYS_DS is not set. You must set this environment variable to the root of the installed Synopsys software.

DESCRIPTION

SYNOPSYS_DS variable should be set inorder for the application to find the default location.

WHAT NEXT

Set the SYNOPSYS_DS environment variable to SYNOPSYS root.

LICSVR-4 (error) DISPLAY is not set. You must set this

environment
variable before running the Synopsys software.

DESCRIPTION

The DISPLAY environment variable displays the application on the terminal on which it was brought up.

WHAT NEXT

Check to see if this environment variable is set to the correct value.

LICSVR-5 (error) Can’t initialize the license server.

DESCRIPTION

The vendor daemon will be brought up by the Flexlm license manager lmgrd on the SERVER mentioned in the keyfile. The machine must be accessible.

WHAT NEXT

Check to see if the machne is up and running. If you are starting the license server from a machine other than the server, then you must be able to ping and rsh to the SERVER.

LICSVR-6 (error) The Synopsys License Server has crashed.

DESCRIPTION

The license server went down due to some reason. This may cause the lmgrd and synopsysd processes to hang.

WHAT NEXT

If the machine is down, the machine needs to be up and running. If the license server is being brought up from the startup script, check to make sure that the lmgrd and synopsysd processes have icome up cleanly. Use lmstat to check. If you have to bring up the license server daemons manually, make sure that you do not have any zombie processes for lmgrd and synopsysd. Start the license manager using lmgrd.

LINK-1 (error) Can’t find %s port ’%s’ on reference to ’%s’ in ’%s’.

DESCRIPTION

This message indicates that the specified port has no corresponding port on the design to which the reference is to be linked. Therefore, the reference cannot be linked to the design.

This situation could arise if extra pin names were specified in the name-based instantiation of the cell in the source file. Alternatively, the name of the design port might be misspelled or incorrectly specified in the cell instantiation.

Another, less likely possibility is that there are design name conflicts that caused the linker to attempt to link the reference to the wrong design.

WHAT NEXT

Check the original source file for one or both of the above problems in the cell instantiation, and edit the file to correct the pin names. Check also for incorrect design names and correct them. Then re-execute **link**.

LINK-2 (error) Too many ports on reference to ’%s’ in ’%s’.

DESCRIPTION

WHAT NEXT

LINK-3 (error) Width mismatch on port ’%s’ of reference to ’%s’ in ’%s’.

DESCRIPTION

The reference above could not be resolved due to a port size mismatch. The linker found a design that matches the requested reference name, but the port sizes do not match.

WHAT NEXT

Check that the ports of the target design or library cell are compatible with the reference.

LINK-4 (error) Too few ports on reference to '%s' in '%s'.

DESCRIPTION

WHAT NEXT

LINK-5 (warning) Unable to resolve reference '%s' in '%s'.

DESCRIPTION

This warning is issued when a suitable design can not be found to link a cell reference to. This will result in any cells using that reference being left as "black boxes". Generally this will happen because of one of two reasons: (1) either a design with the same name as the reference does not exist in the database, link libraries and the directories specified by the search_path, or, (2) the design exists but there are port mismatches between the reference and the design. In the second case an additional error message indicating the exact nature of the mismatch would be given.

If this error occurs while building a synthetic library part, you probably need to use "set_local_link_library" within your implementation description. Please refer to the section "Adding Hierarchy-Control Directives" in the DesignWare Developer Guide.

WHAT NEXT

If there are additional error messages indicating the name and nature of the port mismatches, modify the original souce to make the port specifications match in the instantiation and the design. If there are no such messages, find the library or the directory on which the required design resides. If it is a library, then add that library to the *link_library* variable, and the location of the library to the *search_path* variable. If it is in a design file, add its directory to the *search_path* variable. After doing this, run the **link** command again.

LINK-6 (error) Could not find pin '%s' on design '%s' for cell '%s'.

DESCRIPTION

WHAT NEXT

LINK-7 (error) Recursive hierarchy detected in design '%s'.

DESCRIPTION

WHAT NEXT

LINK-8 (error) Cannot resolve enumeration for cell '%s' on design '%s'.

DESCRIPTION

WHAT NEXT

LINK-9 (warning) Unable to resolve reference to synthetic module '%s' in '%s'.

DESCRIPTION

WHAT NEXT

LINK-10 (error) '%s' was not identified as a synthetic library module
and could not be successfully elaborated from design library

’%s’.

DESCRIPTION

The reference above could not be resolved to a synthetic library module in your current **link_library** variable. The design also could not be elaborated from a design that had been analyzed into the given design library. This causes linking to fail for parameterized instances.

WHAT NEXT

If the reference should resolve to a synthetic library module, you should double check that the appropriate synthetic library is in your **link_library** and that the library contains the given module. If other libraries precede your synthetic library in the **link_library** list, be sure that the two libraries do not contain a cell of the same name. Note that VHDL references are case-insensitive; for example, you could erroneously link to a cell named *ADD* from a technology library when you intended to link to a module *add* from a synthetic library.

If the reference should resolve to a parameterized part, you must analyze that part into an appropriate design library before linking. There may have been an error in the actual elaboration. Check the error messages that preceded this one.

LINK-11 (error) Unconstrained port ’%s’ in design referenced by ’%s’ in ’%s’.
This version does not support unconstrained ports.

DESCRIPTION

WHAT NEXT

LINK-12 (warning) Unable to find library ’%s’. This was probably caused by bad Synopsys installation.

DESCRIPTION

WHAT NEXT

LINK-13 (warning) design library ’%s’ was used in design ’%s’

but it was never defined. Ignoring.

DESCRIPTION

Your VHDL source code contains a library clause for the given design. This library has not been defined in Design Compiler.

WHAT NEXT

Define the library using **define_design_lib**.

LINK-14 (warning) Instance of '%s' is defined in both libraries '%s' and '%s', which are both visible in design '%s'. The first library will be used.

DESCRIPTION

Your VHDL source code for the given design contains a library clause for both libraries listed above. Both libraries define an entity for the instance given. Technically, this is an error in VHDL. We are using the entity from the first library listed.

WHAT NEXT

There is nothing to do for now. In the future, it will be important to choose an entity explicitly in a VHDL configuration.

LINK-15 (error) Cannot continue with auto_link disabled. Set 'auto_link_disable = false'.

DESCRIPTION

The **auto_link_disable** variable is only to be used for speeding up long sequences of **set_load**, **set_resistance**, and **set_annotated_delay** commands. The current command cannot be executed while auto_link is disabled.

WHAT NEXT

Set **auto_link_disable** = false, and re-execute the command.

LINK-16 (warning) Parameter mismatch in linking reference '%s' by name. Linked to '%s', which has the correct parameters.

DESCRIPTION

An attempt was made to link a parameterized reference by name, but the name of the reference pointed to a design with incorrect parameters. The link process resolved the reference to the design above, which had the correct parameters.

WHAT NEXT

To avoid this message, you should attempt to keep your design names unique. This is done by keeping your parameter values below the **hdl_naming_threshold**, and by including special naming parameters in your HDL designs. For details, refer to the *VHDL Compiler Reference Manual*.

LINK-17 (warning) Design '%s' was renamed to '%s' to avoid a conflict with another design that has the same name but different parameters.

DESCRIPTION

A design was automatically elaborated by HDL Compiler, but the name generated for the new design was already in use by another design. The new design was renamed to avoid overwriting the existing design.

WHAT NEXT

To avoid this message, ensure that your design names are unique by keeping your parameter values below the **hdl_naming_threshold**, and by including special naming parameters in your HDL designs. For details, refer to the *VHDL Compiler Reference Manual*.

LINK-18 (warning) Parameter mismatch in linking reference '%s' by name.

Can’t find design.

DESCRIPTION

An attempt was made to link a parameterized reference by name, but the name of the reference pointed to a design with incorrect parameters. The processing that follows this message will attempt to elaborate a new design with the correct parameters. If it fails, this reference will remain unresolved.

WHAT NEXT

To avoid this message, you should attempt to keep your design names unique. This is done by keeping your parameter values below the **hdl_naming_threshold**, and by including special naming parameters in your HDL designs. For details, refer to the *VHDL Compiler Reference Manual*.

LINK-19 (warning) "Port ’%s’ was unresolved on reference to ’%s’ in ’%s’.

DESCRIPTION

This warning is issued when a port can not be resolved on a reference. Ports in the given reference may be duplicate by ignoring cases. If it fails, this reference will remain unresolved.

WHAT NEXT

To avoid this message, you should attempt to keep your ports in a reference unique. Check for attribute value dblink_case_insensitive in the warning reference.

LINK-20 (warning) "Attempting to resolve reference ’%s’ from non-synthetic design library ’%s’.

DESCRIPTION

This warning is issued when a reference suspected to be a DesignWare part fails to link from a DesignWare library such as dw02.sldb. However, the reference may still successfully link from a non-DesignWare library.

WHAT NEXT

Often this warning results from neglecting to specify the required synthetic

libraries using the link_library variable. This can be quickly fixed using the following shell script line:

```
link_library = link_library + synthetic_library
```

This ensures that the link_library variable specifies the necessary DesignWare libraries for your design. Also check that the variable, synlib_library_list, specifies the correct design library names for DesignWare parts. Note that if you are using an external implementation of a DesignWare part, you may receive this warning during normal use.

LINK-21 (warning) Design '%s' has %d extra %s port(s) than reference '%s' in '%s'.

DESCRIPTION

You receive this message if the external netlist used by the preserved function has extra ports that are not defined in the preserved function. These ports are unused.

WHAT NEXT

To avoid this message, use a netlist with I/O ports exactly matching the I/O ports specified in the preserved function.

LINK-22 (error) Reference '%s' in '%s' is a preserved function and cannot have inout ports.

DESCRIPTION

This error is issued when a port can not be resolved on a reference because the direction of the port is inout. Bidirectional ports are not allowed with preserved functions and external netlists.

WHAT NEXT

To avoid this error, change the direction of the port to make it either an input or output port.

LINK-23 (error) Design '%s' used to resolve reference '%s' in

’%s’ is a external netlist and cannot have inout ports.

DESCRIPTION

You receive this message if a port cannot be resolved on a reference. In the external netlist used to resolve the reference, the direction of the corresponding port is inout. Bidirectional ports are not allowed with preserved functions and external netlists.

WHAT NEXT

To avoid this error, use a netlist that has only input or output ports that match the ports of the preserved function.

LINK-24 (error) Port ’%s’ of reference ’%s’ in ’%s’ is connected to port ’%s’ of the external netlist ’%s’. The directions of these two ports are not compatible.

DESCRIPTION

This error is issued when a port can not be resolved on a reference because the direction of the corresponding port of the netlist is different. Note that ’inout’ ports are not allowed in preserved functions and external netlists.

WHAT NEXT

To avoid this error, input ports in the preserved function must be same as the input ports in the external netlist. Similarly, output ports in the preserved function must be same as the output ports in the external netlist.

LINK-25 (error) Unable to match ports of cell %s (’%s’) to ’%s’.

DESCRIPTION

The tool issues this error message because it encountered problems when attempting to match the ports of the cell’s existing reference to the new reference.

WHAT NEXT

Check that the ports of the target design or library cell are compatible with the cell’s current reference. You may need to modify the original source to make the port specifications match in the instantiation and the design.

SEE ALSO

change_link (2), **link** (2).

LINK-26 (warning) Design '%s' was renamed to '%s' to resolve a long name which is not supported by some down stream tools.

DESCRIPTION

Down stream tools have limitation for the length of design name. The design name generated by HDL compiler is shortened, then the design can be accepted by down stream tools.

WHAT NEXT

To avoid this message, ensure that your design names do not exceed the limit.

LINK-27 (warning) Width mismatch on port '%s' of reference to '%s' in '%s'.

DESCRIPTION

The linker found a design that matches the requested reference name, but the port sizes do not match. This is usually a design error, and should be corrected.

Due to a special request, the linker will resolve the mismatch rather than leaving the reference unlinked. The port and connected value will be right-aligned. Any excess bits in the left side of the connected value will be truncated. Any excess bits in the left side of the port will be driven by 0 (for input ports) or left unconnected (for out and inout ports).

Note this amounts to zero-extension rather than sign-extension, regardless of the type of the connected value.

WHAT NEXT

Check that the ports of the target design or library cell are compatible with the reference.

LINT-0 (warning) In design '%s', input pin '%s' of leaf cell '%s' is not connected to any net. %s assumed.

DESCRIPTION

This message appears when a leaf cell has an unconnected input pin. Synopsys tools assume a logical value (for example, logic zero or logic one) for such unconnected signals, based on the type of technology library you are using. This warning message is a notification of the assumption that is being made for the named input pin in the named design.

WHAT_NEXT

Verify that the assumption made by Synopsys regarding the logical value for the given signal is correct. If the assumption is not correct, then connect the floating input pin to the correct logical value in your design.

LINT-1 (warning) In design '%s', cell '%s' does not drive any nets.

DESCRIPTION

This warning alerts you that the output(s) of a component is not connected to any load nets. This usually indicates that a design has not been correctly specified. The Design Compiler may remove such components from your design unless they are protected by a *dont_touch* attribute.

WHAT_NEXT

Make sure that you really want the named component to exist in the given design, even though it has no output pins connected. If so, add a *dont_touch* attribute with the *dont_touch* command to keep the component from being removed.

LINT-2 (warning) In design '%s', net '%s' driven by pin '%s' has

no loads.

DESCRIPTION

This warning message occurs when a net is driven by an output pin (or pins) but has no load pins connected to it. This usually indicates that a design is not correctly specified. The Design Compiler may remove such nets and their driving components from your design unless they are protected by a don’t touch attribute.

WHAT_NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Make sure that you want the named net to exist in the given design, even though it has no load pins connected. If so, add a don’t touch attribute with the **dont_touch** command to keep the net from being removed.

Check the value of the **hdlin_keep_signal_name** variable. For some settings, signals without drivers or loads are preserved in the elaborated design. Check the **hdlin_keep_signal_name** man page for more information.

SEE ALSO

hdlin_keep_signal_name(3)

LINT-3 (warning) In design ’%s’, net ’%s’ has no drivers. %s assumed.

DESCRIPTION

This warning message occurs when there is a net that is not driven by any source pins. Synopsys tools will assume a logical value, such as logic zero or logic one) for these unconnected signals, based on the type of technology library you are using. This warning message is a notification of the assumption that is being made for the named input pin in the named design.

WHAT_NEXT

This is only a warning. You can eliminate this warning message by the following the instructions below.

Verify that the assumption made by Synopsys regarding the logical value for the given signal is correct. If the assumption is not correct, then connect the floating net to the correct logical value in your design.

Check the value of the **hdlin_keep_signal_name** variable. For some settings, signals

without drivers or loads are preserved in the elaborated design. Check the **hdlin_keep_signal_name** man page for more information.

SEE ALSO

hdlin_keep_signal_name(3)

LINT-4 (information) In design '%s', net '%s' has multiple drivers. Wired AND assumed.

DESCRIPTION

This warning indicates that *check_design* has found a net with multiple source pins. Synopsys tools must make an assumption regarding the functionality of such wired-logic nets. This message indicates which wired-logic net (for example, wired-AND, wired-OR) will be used for this particular net. The assumption is made based on a description of wired-logic functionality in the technology library that you are using.

WHAT_NEXT

Make sure that you intended to have multiple drivers on the given net. Errors in specifying a design could lead to this message in a situation where wired logic is not intended.

You could also use *set_attribute* and *remove_attribute* commands to specify or remove the wired logic type for a given net.

For example,

set_attribute [get_nets z] wired_and true -type boolean

would set 'wired_and' attribute on net 'z'. While

remove_attribute [get_nets z] wired_and

would remove the 'wired_and' attribute on net 'z'.

LINT-5 (warning) In design '%s', output port '%s' is not driven.

DESCRIPTION

This error message occurs when the **check_design** command finds the specified output port for the design is not driven by any signal.

WHAT_NEXT

Check your design to be sure that it is connected correctly, and then run the command again.

SEE ALSO

check_design (2).

LINT-6 (warning) In design '%s', input port '%s' drives wired logic;
(the port direction may have been specified incorrectly).

DESCRIPTION

This warning message occurs when the **check_design** command encounters an input port connected to a net that has multiple drivers. The input port (which acts as a driver on the net) is part of a wired-logic gate.

WHAT NEXT

This is only a warning message. No action is required.

However, you can make sure that you want multiple drivers on the net driven by the indicated port. Errors in specifying a design can lead to this message in a situation where wired logic is not intended. For example, if the direction of an output port is accidentally specified as input, then this message could occur.

Otherwise, you have encountered a situation where the optimizer has created wired logic on a design boundary. Check the components created by the optimizer to ensure that this is the functionality that you originally intended. Use the **Formality** command to compare the design you currently have with the original design, in addition to simulating the synthesized design to ensure correctness.

SEE ALSO

check_design(2)

LINT-7 (error) Recursive hierarchy detected in design '%s'.

DESCRIPTION

The *check_design* command traces the hierarchy of your design to ensure that "recursive hierarchy" does not occur. The term "recursive hierarchy" means that a

module in a design instantiated a sub-module that, in turn, instantiated the original module. Hierarchically recursive designs cannot be handled by the Design Compiler. This is an error message, not a warning.

WHAT_NEXT

This error usually occurs when a design has been incorrectly described. Modify your design description to remove the recursive hierarchy.

LINT-8 (warning) In design '%s', input port '%s' is unloaded.

DESCRIPTION

The *check_design* command issues this warning when it finds an unconnected (for example, "unloaded") input port on a design. This means that the given input port does not connect to any logic inside the design.

WHAT_NEXT

Make sure that you intended that the specified port be unused in your design.

LINT-10 (warning) In design '%s', cell '%s' has no output pins.

DESCRIPTION

This warning message indicates that *check_design* has found a cell with no output pins. Unless such cells are protected through the use of the *dont_touch* command, the *compile* command will remove them from the design, since they have no functionality.

WHAT_NEXT

This warning probably appeared because of an error in specifying a component in your design, or a component in your technology library. Check the design/library to find the problem, and correct the description of the given cell/design.

LINT-11 (fatal) In design '%s', db_object '%s' does not have a '%s' attribute.

DESCRIPTION

This is a fatal error in the *check_design* command. An object in the Synopsys

internal database for your design has become corrupt or does not have information regarding signal direction (for example, input, output or bidirectional).

WHAT_NEXT

Recreate or re-read your design. If you specified a component pin without a direction attribute, you can fix the problem by making sure that a direction exists for the given pin. Otherwise this error could indicate that there is an internal problem in the Synopsys software that needs to be reported to the Synopsys Hotline or to your Synopsys application engineer.

LINT-12 (fatal) Unable to db_gen_init '%s' from db_object '%s'.

DESCRIPTION

This is a fatal error in the *check_design* command. An object in the Synopsys internal database for your design has become corrupt, or that an object in your design does not have ports attached to it.

WHAT_NEXT

Recreate or re-read your design. If you specified a component without ports, you can fix the problem by making sure that ports exist for the given pin. Otherwise this error could indicate that there is an internal problem in the Synopsys software that needs to be reported to the Synopsys Hotline or to your Synopsys application engineer.

LINT-20 (error) In design '%s', cell '%s' does not have a reference.

DESCRIPTION

This error describes a problem in the database representation for your design. The error means that a particular instantiation of a component (or "cell" in Synopsys terms) does not indicate which type of component it actually is. In Synopsys terminology "reference" describes the part of a design representation that points to the actual component for a given instantiation or cell. If you have an inverter (INV) in your technology library, and you've instantiated that inverter in your design as cell13 and cell23, then each of the instantiations (cells) should own a pointer (reference) to the actual component (in this case INV). This error indicates that, for some reason, the reference does not exist on the cell.

WHAT_NEXT

Make sure that your design specifies the type of the given cell. If you specified a

cell without a type, fix the problem by changing your design description. Otherwise this error could indicate that there is an internal problem in the Synopsys software that needs to be reported to Synopsys Hotline or to your Synopsys application engineer.

LINT-21 (fatal) Unable to db_new_attribute to db_object '%s'.

DESCRIPTION

This is a fatal error in the *check_design* command. Synopsys tools were unable to allocate memory to create an object in the Synopsys internal database description for your design. The *check_design* command creates small markers on your design as it traverses the design checking for errors. These small markers are removed after *check_design* is finished. This error indicates that an attempt to create a marker failed for some reason. This is probably due to a lack of memory, in which case the fatal error was accompanied by an "out of memory" error message. It is.also possible that this message could occur in a badly mangled design which has recursive hierarchy.

WHAT_NEXT

Check the message for an "out of memory" error to determine if your platform needs more virtual memory. Otherwise, the problem is likely to be a faulty design or an internal Synopsys error.

LINT-22 (warning) In design '%s', ref '%s' was not used.

DESCRIPTION

This warning indicates that there is a dangling "reference" with the given name on your design. In Synopsys terminology "reference" describes the part of a design representation that points to the actual component for a given instantiation or cell. If you have an inverter (INV) in your technology library, and you've instantiated that inverter in your design as cell13 and cell23, then each of the instantiations (cells) should own a pointer (reference) to the actual component (in this case INV). Sometimes, during the process of building or modifying a design, a reference will remain, even though all cells that refer to it have been removed or changed. Although this is a waste of memory, it should not impair the functionality of the design or the operation of Synopsys tools.

WHAT_NEXT

A large number of dangling references in your design can increase the memory size of the design. Sometimes these can be removed by writing the entire design out (in Synopsys database "db" format) and then reading it to Synopsys tools again. Otherwise, make a note of when the message occurs and pass the problem and an

example to the Synopsys support Hotline or to your application engineer. Dangling references indicate that the tool is not managing memory efficiently.

LINT-23 (fatal) Unable to remove attribute '%s' from db_object '%s'.

DESCRIPTION

This is a fatal error in the *check_design* command. Synopsys tools were unable to deallocate memory to free an object in the Synopsys internal database description for your design. The *check_design* command creates small markers on your design as it traverses the design checking for errors. These markers are removed after *check_design* is finished. This error indicates that an attempt to remove a marker failed for some reason. This is probably due to an internal memory error in Synopsys tools.

WHAT_NEXT

The problem is either a faulty design or an internal Synopsys error. The *check_design* command may have destroyed your design. Report the problem to the Synopsys Hotline or to your Synopsys application engineer.

LINT-25 (warning) Design '%s' does not have any output ports.

DESCRIPTION

This warning message indicates that *check_design* has found a design with no output pins. Unless such designs are protected through the use of the *dont_touch* command, the *compile* command will remove instances of such designs, since they have no functionality.

WHAT_NEXT

This warning probably appeared because of an error in specifying a component in your design, or a component in your technology library. Check the design/library to find the problem, and correct the description of the given cell/design.

LINT-26 (fatal) Unable to db_set_attribute to db_object '%s'.

DESCRIPTION

This is a fatal error in the *check_design* command. Synopsys tools were unable to

allocate memory to create an attribute in the Synopsys internal database description for your design. The *check_design* command creates small markers on your design as it traverses the design checking for errors. These markers are removed after *check_design* is finished. This error appears when an attempt to create a marker failed for some reason. This is probably due to a lack of memory, in which case the fatal error was accompanied by an "out of memory" error message. It is also possible that this message could occur in a badly mangled design which has recursive hierarchy.

WHAT_NEXT

Check the message for an "out of memory" error to determine if your platform needs more virtual memory. Otherwise, the problem is likely to be a faulty design or an internal Synopsys error.

LINT-27 (error) Object '%s' is not of class dd_design, and should not be seen by db_lint.

DESCRIPTION

This message indicates that the *check_design* command has been called on a database object that is not a design. It indicates an internal problem in the user-interface for the *check_design* command, or a corrupted design database.

WHAT_NEXT

Recreate or re-read your design, and then runn *check_design*. If this does not work, then there is probably an internal problem in the Synopsys software that should be reported to the Synopsys Hotline or to your Synopsys application engineer.

LINT-28 (warning) In design '%s', port '%s' is not connected to any nets.

DESCRIPTION

This warning alerts you that a port in a design is not connected to any nets. This usually indicates that a design has not been correctly specified. However, there are some situations where, as a designer, you choose to specify a port on a design for compatibility reasons, even though the port is not internal to design use. The Synopsys tools leave unconnected ports alone, with one exception; that is, you specified that a given input port is opposite or equal to another input port in a design.

WHAT_NEXT

Make sure that you want the named port to exist in the given design, even though it has no nets connected. Remove the port from your design if you choose.

LINT-29 (warning) In design '%s', input port '%s' is connected directly to output port '%s'.

DESCRIPTION

This warning alerts you to a situation where an input port in a design is directly connected to an output port. This warning is issued because some technologies do not allow such a connection. Many ASIC vendors stipulate that a buffer must be used to connect an input to an output. This restriction might or might not apply to your technology.

WHAT_NEXT

If directed to do so, *compile* inserts the necessary buffering to prevent a direct connection of an input port and an output port. To do this, set the boolean variable *compile_fix_multiple_port_nets* to TRUE, then compile your design. This variable also instructs *compile* to make sure that multiple output ports are not connected to the same electrical net. See the manual page on *compile_variables* for more information.

LINT-30 (warning) In design '%s', %s.

DESCRIPTION

This is the terse version of a *check_design* warning message. This message is displayed when Synopsys command *check_design -summary* performs a design check and gives a summary of warnings.

WHAT_NEXT

Use *check_design* to obtain more information about the warning.

LINT-31 (warning) In design '%s', output port '%s' is connected

directly to output port '%s'.

DESCRIPTION

This warning alerts you to a situation where an output port in a design is connected directly to another output port. This warning is issued because some technologies do not allow such a connection. This restriction might or might not apply to your technology.

WHAT_NEXT

If directed to do so, *compile* inserts the necessary buffering to make sure that multiple output ports are not connected to the same electrical net. To do this, set the boolean variable *compile_fix_multiple_port_nets* to TRUE, then compile your design.

This variable also instructs *compile* to prevent a direct connection of an input port and an output port. See the manual page on *compile_variables* for more information.

LINT-32 (warning) In design '%s', a pin on submodule '%s' is connected to logic 1 or logic 0.

DESCRIPTION

check_design issues this warning when it finds an instance of a hierarchical design (for example, a sub-module) that has an input connected to a logic constant. This warning is issued to verify that this is a desired connection on the submodule. Be aware that *compile* can remove logic in a design that is redundant. So, *compile* can produce designs that display this warning if it has optimized and eliminated the logic driving a submodule.

WHAT_NEXT

Verify that you want the given submodule input connected to logic one or zero. If you have run *compile*, you might want to use *verify* to verify the optimized design with your original. Or, use the -verify option to *compile*, whenever feasible.

LINT-33 (warning) In design '%s', the same net is connected to more than one pin on submodule '%s'.

DESCRIPTION

check_design issues this warning when it finds an instance of a hierarchical design

(for example, a sub-module) that has more than one input connected to the same net. This warning is issued to verify that these are desired connections on the submodule. Be aware that *compile* can remove logic in a design that is redundant. So, *compile* can produce designs that display this warning if it determines that multiple inputs on a submodule are driven by the same logical signal.

WHAT_NEXT

Verify that you want the given submodule inputs connected to the same logical signal. If you have run *compile*, you might want to use *verify* to verify the optimized design with your original. Or, use the -verify option to *compile* whenever feasible.

LINT-34 (warning) In design '%s', three-state bus '%s' has non three-state driver '%s'.

DESCRIPTION

Synopsys libraries contain descriptions of three-state driving pins on components. Synopsys tools classify a net as a three-state net if it is driven by at least one pin that has this three-state attribute. Normally, if there are multiple drivers on such nets, it is assumed that all driving pins should be three-state drivers, for correct operation of the three-state bus. This warning message indicates a situation where at least one non-three-state driver appears on a three-state net.

WHAT_NEXT

Verify that this is what you have intended for the given net. If the *non-three-state* driver pin specified in the message is really on a three-state driver in your ASIC technology, verify that the technology library description is correct.

LINT-35 (information) In design '%s', net '%s' has multiple drivers. Wired OR assumed.

DESCRIPTION

This warning message indicates that *check_design* has found a net with multiple source pins. Synopsys tools make an assumption regarding the functionality of such *wired logic* nets. This message gives the interpretation (for example, Wired-And, Wired-Or) that will be used for this particular net. This assumption is made based on a description of wired logic functionality in the technology library used.

WHAT_NEXT

Make sure that you intend to have multiple drivers on the given net. Errors in specifying a design could lead to this message in a situation where wired logic is not intended.

You could also use *set_attribute* and *remove_attribute* commands to specify or remove the wired logic type for a given net.

For example,

```
set_attribute [get_nets z] wired_and true -type boolean
```

would set 'wired_and' attribute on net 'z'. While

```
remove_attribute [get_nets z] wired_and
```

would remove the 'wired_and' attribute on net 'z'.

LINT-38 (warning) In design '%s', net '%s' has multiple drivers (unknown wired-logic type).

DESCRIPTION

This warning message indicates that *check_design* has found a net with multiple source pins. Synopsys tools must make an assumption regarding the functionality of such *wired logic* nets. This message indicates that the tool was unable to determine the wired-logic type of the net. The assumption about wired-logic type is made based on a description of wired logic functionality in the technology library that you are using. This message could indicate that wired-logic information was not correctly specified in your technology library, or that the description of the design is incorrect.

WHAT_NEXT

Examine the net(s) in question, the descriptions of the components connected to the net, and their respective technology library descriptions. Make sure that the net is not the result of an error in specifying a design. Design Compiler is capable of creating wired logic during optimization, but only in the situation where the logical *function* of that wired logic is understood (for example, Wired-OR).

You could also use *set_attribute* command to specify the wired logic type for a net with multiple drivers. The possible wired types include 'wired_and', 'wired_or' and 'three_state'.

For example,

```
set_attribute [get_nets z] wired_and true -type boolean
```

would set 'wired_and' attribute on net 'z'.

LINT-39 (warning) In design '%s', net '%s' has %s emitters, exceeding the maximum of %s.

DESCRIPTION

This warning message indicates that *check_design* has found a wired logic net that is illegal. Wired logic nets in ECL have a limit on the number of emitters that can legally be connected together. This limit is given by the *max_wired_emitters* attribute in the technology library.

WHAT_NEXT

Make sure that you intend to have this many emitters on the given net. Errors in specifying a design can lead to this message in a situation where a wired logic net of this size is not intended. The Synopsys ECL Compiler can build wired logic to meet design constraints and will legalize illegal wired logic, unless the wired logic net is protected by a *dont_touch* attribute. Finally, you might want to check your technology library to be sure that the specification for the maximum number of wired emitters is correct.

LINT-40 (warning) In design '%s', net '%s' has drivers with conflicting wired connection classes.

DESCRIPTION

This warning message indicates that *check_design* has found a wired logic net that is illegal. Wired logic nets in ECL have to meet *connection class* requirements that ensure that all drivers on the net may be legally connected together. All drivers on a wired logic net must share the same wired connection class. Each driver's class is defined in the technology library description for the driver by the *wired_connection_class* attribute.

WHAT_NEXT

Make sure that you intend to have these drivers on the given net. Errors in specifying a design can lead to this message in a situation where a wired logic net with these drivers is not intended. The Synopsys ECL Compiler can build wired logic to meet design constraints and will legalize illegal wired logic, unless the wired logic net is protected by a *dont_touch* attribute. Finally, you might want to check your technology library, to be sure that the connection classes for the given components are correct.

LINT-41 (warning) In design '%s', pin '%s' is not allowed to drive

wired logic.

DESCRIPTION

This warning message indicates that *check_design* has found a wired logic net that is illegal. All driving pins on a wired logic net must be capable of driving wired logic. The technology library description for driving pins includes the *multiple_drivers_legal* attribute, which will be TRUE if the driving pin can legally drive wired logic, and FALSE otherwise. This attribute also exists at the library level and gives a default value for components in the library.

WHAT_NEXT

Make sure that you intend to have these drivers on the given net. Errors in specifying a design can lead to this message in a situation where a wired logic net with these drivers is not intended. The Synopsys ECL Compiler can build wired logic to meet design constraints and will legalize illegal wired logic, unless the wired logic net is protected by a *dont_touch* attribute. Finally, you might want to check your technology library to be sure that the *multiple_drivers_legal* attributes for the given component is correct.

LINT-42 (warning) In design '%s', pin '%s' is not allowed to be driven by wired logic.

DESCRIPTION

This warning message indicates that *check_design* has found a wired logic net that is illegal. All load pins on a wired logic net must be capable of being driven by wired logic. The technology library description for pins includes the *multiple_drivers_legal* attribute, which will be TRUE if the driving pin can legally drive wired logic, and FALSE otherwise. This attribute also exists at the library level to give a default value for components in the library.

WHAT_NEXT

Make sure that you intend to have these loads on the given net. Errors in specifying a design can lead to this message in a situation where a wired logic net with these loads is not intended. The Synopsys ECL Compiler can build wired logic to meet design constraints and will legalize illegal wired logic, unless the wired logic net is protected by a *dont_touch* attribute. Finally, you might want to check your technology library to be sure that the *multiple_drivers_legal* attributes for the given component is correct.

LINT-44 (information) In design '%s', %s.

DESCRIPTION

This is the terse version of a *check_design* informational message. This message is displayed when Synopsys command *check_design -summary* performs a design check and gives a summary of some important information.

WHAT_NEXT

Use *check_design* to obtain more information about the informational message.

LINT-45 (information) Design '%s' is instantiated %d times.

DESCRIPTION

This information message indicates that a single design is instantiated more than once in the design hierarchy below the current design. This message is issued when "check_design -multiple_designs" is used in XG mode.

WHAT_NEXT

Right now all DC commands handle designs with multiple instances. Each command may invoke *uniquify* under the hood to uniquify user designs if necessary.

LINT-46 (warning) Design '%s', cell '%s', pin '%s' is illegally connected,
since primary output '%s' is unconnected.

DESCRIPTION

This warning message occurs for ECL designs in ECL technologies that use the *primary output* designator for paired ECL outputs. By designating an output as a *primary output* your ASIC vendor has indicated that the given output must be connected before any other outputs of the same polarity are used. As an example, suppose that a component NOR2 has two positive phase outputs, X1 and X2. Suppose that the technology library description for the gate shows X1 as a primary output. Designating X1 as a primary output means that it is illegal to connect output X2 to a net unless X1 is already connected to a different net. This warning indicates a case where (to use this example) output X2 is connected but output X1 is not connected. This is a violation of the design rule described in the technology library.

WHAT_NEXT

Be sure that your design was created correctly. If the Design Compiler or DFT Compiler have created an illegal design, check the technology library to be sure that the *primary_output* attribute is used properly for the given technology. If everything is alright in the technology library and *compile* has created an illegal design, contact your Synopsys application engineer or the Synopsys Hotline with a test case.

LINT-47 (warning) In design '%s' net '%s' has a connection class violation:

DESCRIPTION

This warning message indicates that *check_design* has found a net that does not meet the connection class requirements described in the technology library. These connection class requirements ensure that all pins on a net can legally be connected. All pins connected together on a net must share at least one connection class in common. Each pin's class is defined in the technology library description for the pin, through the *connection_class* attribute.

WHAT_NEXT

Determine whether the design you are checking was (1) created manually as a netlist, or (2) created by Design Compiler (possibly from a high-level description) or DFT Compiler. If (1) is true, investigate the violation to be sure that you have specified the net correctly in your design. If (2) is true, examine the illegal net(s) created by the tool. It might not always be possible for the given net to be legalized. For example, a net might connect though hierarchy to pins whose connection classes cannot be matched. Or, other design rules, such as fanout restrictions or transition time restrictions might have made legalization for connection rules impossible. Also, check your technology library to determine whether there are level shifting components available to convert between the given connect classes.

LINT-48 (error) Not a valid part and speed grade

DESCRIPTION

This error message indicates that *check_design* has found that the part specified on the design does not exist in the technology library.

WHAT_NEXT

Do a *report_library* on the technology library to get the list of parts supported.

Select the one you want and attribute on the design.

LINT-49 (warning) The part %s has fewer I/O ports %d than that required by the design %d.

DESCRIPTION

This warning message indicates that *check_design* has found that the part specified on the design does not have enough number of input/output ports to hold the design.

WHAT_NEXT

Do a *report_library* on the technology library to get the list of parts supported. Select the bigger part and attribute it on the design.

LINT-50 (warning) The part %s has fewer flip-flops %d than that required by the design %d.

DESCRIPTION

This warning message indicates that *check_design* has found that the part specified on the design is unable to accomodate the number of flip-flops present in your design.

WHAT_NEXT

Do a *report_library* on the technology library to get the list of parts supported. Select the part which has more number of flip-flops than the previous part and attribute it on the design.

LINT-51 (warning) Part related checkings is not supported for the technology library.

DESCRIPTION

This warning message indicates that *check_design* has found that the technology library doesn’t have any parts information specified in it.

WHAT_NEXT

Part specific checking is supported only for FPGA technology library. Make sure that you are using FPGA technology library and they have part information specified in them. If there is no part information, ask your vendor to supply a technology library with part information.

LINT-52 (warning) In design '%s', output port '%s' is connected directly to '%s'.

DESCRIPTION

This warning alerts you to a situation where an output port in a design is connected directly to Logic 1 or Logic 0. This warning is issued because some technologies do not allow such a connection. This restriction might or might not apply to your technology. Most case it is a design error.

WHAT_NEXT

Please check the net list carefully to make sure this case is desired, and discuss with your technology team to make sure it is allowed.

LINT-53 (error) In design '%s', net '%s' is driven by both logic 0 and logic 1.

DESCRIPTION

WHAT_NEXT

LINT-54 (warning) In design '%s', net '%s' is driven by %s.

DESCRIPTION

This message alert you the net is driven by const net.

WHAT_NEXT

Please visit your design and make sure it is desired.

LINT-55 (information) Design '%s' does not contain any cells or nets.

DESCRIPTION

WHAT_NEXT

LINT-56 (error) In design '%s', net '%s' has multiple drivers (unknown wired-logic type).

DESCRIPTION

This error message indicates that *check_design* has found a net with multiple source pins. Synopsys tools must make an assumption regarding the functionality of such *wired logic* nets. This message indicates that the tool was unable to determine the wired-logic type of the net. The assumption about wired-logic type is made based on a description of wired logic functionality in the technology library that you are using. This message could indicate that wired-logic information was not correctly specified in your technology library, or that the description of the design is incorrect.

WHAT_NEXT

Examine the net(s) in question, the descriptions of the components connected to the net, and their respective technology library descriptions. Make sure that the net is not the result of an error in specifying a design. Design Compiler is capable of creating wired logic during optimization, but only in the situation where the logical *function* of that wired logic is understood (for example, Wired-OR).

You could also use *set_attribute* command to specify the wired logic type for a net with multiple drivers. The possible wired types include 'wired_and', 'wired_or' and 'three_state'.

For example,

```
set_attribute [get_nets z] wired_and true -type boolean
```

would set 'wired_and' attribute on net 'z'.

To reduce the severity of this error message to a warning, set the variable *check_design_allow_unknown_wired_logic_type* to *true*.

LINT-57 (error) In design '%s', %s.

DESCRIPTION

This is the terse version of a *check_design* error message. This message is displayed when Synopsys command *check_design -summary* performs a design check and gives a summary of errors.

WHAT_NEXT

Use *check_design* to obtain more information about the error.

LINT-58 (warning) In design '%s', input pin '%s' of leaf cell '%s' is connected to undriven net '%s'.

DESCRIPTION

This message appears when leaf cell input pin has a connected net, but the net has no driver.

WHAT_NEXT

LINT-59 (warning) In design '%s', input pin '%s' of hierarchical cell '%s' has one or more internal loads, but is not connected to any nets. '%s' is assumed.

DESCRIPTION

This message appears when hierachical cell input pin has internal load, but no driver. Synopsys tools assume a logical value (for example, logic zero or logic one) for such unconnected signals, based on the type of technology library you are using. This warning message is a notification of the assumption that is being made for the named input pin in the named design.

WHAT_NEXT

Verify that the assumption made by Synopsys regarding the logical value for the given signal is correct. If the assumption is not correct, then connect the floating input pin to the correct logical value in your design.

LINT-60 (warning) In design '%s', input pin '%s' of hierarchical cell '%s' has no internal loads and is not connected to any nets.

DESCRIPTION

This message appears when hierarchical cell input pin has no internal load and no driver. Synopsys tools assume a logical value (for example, logic zero or logic one) for such unconnected signals, based on the type of technology library you are using. This warning message is a notification of the assumption that is being made for the named input pin in the named design.

WHAT_NEXT

Verify that the assumption made by Synopsys regarding the logical value for the given signal is correct. If the assumption is not correct, then connect the floating input pin to the correct logical value in your design.

LINT-62 (error) In design '%s', three-state bus '%s' has non three-state driver '%s'.

DESCRIPTION

Synopsys libraries contain descriptions of three-state driving pins on components. Synopsys tools classify a net as a three-state net if it is driven by at least one pin that has this three-state attribute. Normally, if there are multiple drivers on such nets, it is assumed that all driving pins should be three-state drivers, for correct operation of the three-state bus. This Error message appears when at least one non-three-state driver appears on a three-state net.

WHAT_NEXT

Verify that this is what you have intended for the given net. If the *non-three-state* driver pin specified in the message is really on a three-state driver in your ASIC technology, verify that the technology library description is correct.

To reduce the severity of this error message to a warning, set the variable *check_design_allow_non_tristate_drivers_on_tristate_bus* to *true*.

LINT-63 (warning) Net '%s' has a single tri-state driver.

DESCRIPTION

You receive this warning message when the **check_design** command detects that a net is

driven by a single tri-state driver.

WHAT NEXT

LINT-64 (warning) In design '%s', output port '%s' is driven from the outside.

DESCRIPTION

This error message occurs when the **check_design** command finds the specified output port for the design is driven from the outside.

WHAT_NEXT

Check your design to be sure that it is connected correctly, and then run the command again.

SEE ALSO

check_design (2).

LINT-65 (error) In design '%s', input port '%s' is connected to a multiple-driven net and the drivers include an output port/pin. (port-direction may have been specified incorrectly.)

DESCRIPTION

This error is issued when the *check_design* command encounters an input port connected to a net which has multiple drivers and one or more of the drivers is an output port or pin.

WHAT_NEXT

Make sure that you intend to have multiple drivers on the net driven by the indicated port. Errors in specifying a design port could lead to this message. For example, if the direction of an output port is accidentally specified as "input," then this message could occur. Check the design to ensure that this is the functionality that you originally intended.

LINT-78 (information) Design '%s' has multiply instantiated

designs. Use the ’-multiple_designs’ switch for more information.

DESCRIPTION

This message indicates that the current_design has one or more multiply instantiated designs. To get a list of all the multiply instantiated designs with the instance names, use *-multiple_designs* switch.

WHAT_NEXT

Use *-multiple_designs* to obtain more information about the multiply instantiated designs.

LINT-98 (information) Use the ’check_design’ command for more information about warnings.

DESCRIPTION

This message indicates that a terse version of informational messages or warnings on a design has just been displayed. To obtain more complete information, use *check_design*. This message is displayed when user used *check_design -summary* to get a summary of the potential design problems.

WHAT_NEXT

Use *check_design* to obtain more information about the design.

LINT-99 (information) There are %d potential problems in your design. Please run ’check_design’ for more information.

DESCRIPTION

This message indicates that there are %d potential design problems in the user design. To obtain detailed information, use *check_design*. This message is displayed when Synopsys commands like *compile* perform a design check as part of their operation. If *compile* issued the message but completed its operation, the design might have to be read again for *check_design* to report what was wrong initially.

WHAT_NEXT

Use *check_design* to obtain more information about the design.

LINT-100 (warning) The design does not have back-annotated delays.

DESCRIPTION

check_design -post_layout issues this warning when it finds that the design does not have back-annotated delays.

WHAT_NEXT

To back-annotate delays onto the design, use the *read_timing* command or a series of *set_annotated_delay* command.

LINT-101 (warning) Missing %s delay annotation between pins '%s' and '%s' on cell '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a timing arc on a cell that does not have back-annotated delay.

WHAT_NEXT

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-102 (warning) The design does not have back-annotated cluster assignments.

DESCRIPTION

check_design -post_layout issues this warning when it finds that the design does not have back-annotated cluster assignments (The clusters corresponds to the physical hierarchy of the design).

WHAT_NEXT

To back-annotate cluster assignments onto the design, use the *read_clusters* command to read in the *PDEF* file.

LINT-103 (warning) Missing cluster annotation on cell '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a cell which is not assigned to a cluster.

WHAT_NEXT

Modify the *PDEF* file before applying *read_clusters* command such that cells with missing cluster assignment are correctly assigned to a cluster.

LINT-104 (warning) The design does not have back-annotated cell locations.

DESCRIPTION

check_design -post_layout issues this warning when it finds that the design does not have cell locations back-annotated.

WHAT_NEXT

To back-annotate cell locations onto the design, use the *read_clusters* command to read in the *PDEF* file with cell location (i.e., *PDEF* version 2.0 or later)..

LINT-105 (warning) Missing cell location for cell '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a cell which does not have cell location back-annotated.

WHAT_NEXT

Modify the *PDEF* file before applying *read_clusters* command such that cells with missing cell locations are correctly assigned a cell location.

LINT-106 (warning) Missing %s delay annotation from pin '%s/%s' to pin '%s/%s' on net '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a net timing arc that does not have back-annotated delay.

WHAT_NEXT

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-107 (warning) The design does not have back-annotated net capacitances.

DESCRIPTION

check_design -post_layout issues this warning when it finds that the design does not have back-annotated net capacitances.

WHAT_NEXT

To back-annotate net capacitances on the design, use a series of *set_load* command.

LINT-108 (warning) Missing capacitance annotation on net '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a net that does not have back-annotated capacitance.

WHAT_NEXT

To back-annotate capacitances on nets with missing capacitance annotation, use a series of *set_load* command.

LINT-109 (warning) Missing orientation annotation on cluster

’%s’.

DESCRIPTION

check_design -post_layout issues this warning when it finds a leaf level cluster that does not have back-annotated row-orientation.

WHAT_NEXT

Modify the *PDEF* file before applying *read_clusters* command such that clusters with missing orientations are correctly assigned an orientation.

LINT-110 (warning) Missing bounding box for cluster ’%s’.

DESCRIPTION

check_design -post_layout issues this warning when it finds a leaf level cluster that does not have back-annotated bounding box.

WHAT_NEXT

Modify the *PDEF* file before applying *read_clusters* command such that clusters with missing bounding box are correctly assigned a bounding box.

LINT-111 (warning) Missing %s delay annotation for *setup* arc from pin ’%s’ to pin ’%s’ on cell ’%s’.

DESCRIPTION

check_design -post_layout issues this warning when it finds a *setup* timing arc on a cell that does not have back-annotated delay.

WHAT_NEXT

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-112 (warning) Missing %s delay annotation for *hold* arc

from pin '%s' to pin '%s' on cell '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a *hold* timing arc on a cell that does not have back-annotated delay.

WHAT_NEXT

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-113 (warning) Missing %s delay annotation for 'preset' or 'clear' timing arc from pin '%s' to pin '%s' on cell '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a *preset* or *hold* timing arc on a cell that does not have back-annotated delay. If the warning message indicates a missing *rise* delay annotation, the timing arc with missing annotation is a *preset* timing arc; otherwise, it is a *clear* timing arc.

WHAT_NEXT

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-114 (warning) Missing %s delay annotation from port '%s%s' to pin '%s/%s' on net '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a net timing arc from a *port* to a pin that does not have back-annotated delay.

WHAT_NEXT

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-115 (warning) Missing %s delay annotation from pin '%s/%s' to port '%s%s' on net '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a net timing arc from a pin to a *port* that does not have back-annotated delay.

WHAT_NEXT

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-116 (warning) Missing %s delay annotation from port '%s%s' to port '%s%s' on net '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a net timing arc from a *port* to a *port* that does not have back-annotated delay.

WHAT_NEXT

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-117 (warning) The design does not have any back-annotation information.

DESCRIPTION

You receive this warning message when the **check_design -post_layout** command is executed and it detects that the design does not have any back-annotation information.

WHAT NEXT

To back-annotate delays onto the design, use the **read_sdf** command or a series of **set_annotated_delay** commands. To back-annotate cluster assignments onto the design, use the **read_clusters** command to read in the PDEF file. To back-annotate net capacitances on the design, use a series of **set_load** commands.

LINT-118 (warning) The design has '%d' cells which do not have cluster annotation on them. The cells with missing annotations represent '%f' of all cells.

DESCRIPTION

You receive this warning message when the **check_design -post_layout -summary** command detects that the design has cells that do not have cluster information back-annotated on them. The message reports the total number of all such cells, and prints the percentage of cells with missing annotations.

The **check_design -only_post_layout -summary** command also issues this warning message when it finds cells with missing cluster annotations.

WHAT NEXT

To back-annotate cluster assignments onto the design, correct the PDEF file and use the **read_clusters** command to read in the PDEF file.

LINT-119 (warning) The design has '%d' cells which do not have locations annotation on them. The cells with missing annotations represent '%f' of all cells.

DESCRIPTION

You receive this warning message when the **check_design -post_layout -summary** command detects that the design has cells that do not have location information back-annotated on them. The message reports the total number of all such cells and gives the percentage of the cells with missing annotations.

The **check_design -only_post_layout -summary** command also issues this warning when it finds cells with missing location annotations.

WHAT NEXT

To back-annotate location assignments onto the design, correct the PDEF file, and use the **read_clusters** command to read in the PDEF file.

LINT-120 (warning) The design has '%d' cells annotated with clusters which have no orientation. The cells with this type of

missing annotations represent ’%f’ of all cells.

DESCRIPTION

You receive this warning message when the **check_design -post_layout -summary** command detects that the design has cells that are annotated with clusters that have no orientation. The warning message reports the total number of all such cells and prints the percentage of the cells with missing annotations.

The **check_design -only_post_layout -summary** command also issues this warning message when it finds cells annotated with clusters that have no orientation.

WHAT NEXT

To back-annotate cluster assignments with orientation onto the design, correct the PDEF file and use the **read_clusters** command to read in the PDEF file.

LINT-121 (warning) The design has ’%d’ cells annotated with clusters which have no bounding box. The cells with this type of missing annotations represent ’%f’ of all cells.

DESCRIPTION

You receive this warning message when the **check_design -post_layout -summary** command detects that the design has cells that are annotated with clusters that have no bounding box. The command reports the total number of all such cells and prints the percentage of cells with missing annotations.

The **check_design -only_post_layout -summary** command also issues this warning when it detects cells annotated with clusters that a have missing bounding box.

WHAT NEXT

To back-annotate cluster assignments with a bounding box onto the design, correct the PDEF file and use the **read_clusters** command to read in the PDEF file.

LINT-122 (warning) The design has ’%d’ cells which have missing delay arc annotations. The cells with missing

annotations represent '%f' of all cells.

DESCRIPTION

You receive this warning message when the **check_design -post_layout -summary** command detects that the design has cells that have missing delay arc annotations. The command reports the total number of all such cells and prints the percentage of cells with the missing annotations.

The **check_design -only_post_layout -summary** command also issues this warning when it finds cells with missing delay arc annotations.

WHAT NEXT

To back-annotate delays onto the design, use the **read_sdf** command, or a series of **set_annotated_delay** commands.

LINT-123 (warning) The design has '%d' nets which have missing delay arc annotations. The nets with missing annotations represent '%f' of all nets.

DESCRIPTION

You receive this warning message when the **check_design -post_layout -summary** command detects that the design has nets that have missing delay arc annotations. The command reports the total number of all such nets and prints the percentage of nets with the missing annotations.

The **check_design -only_post_layout -summary** command also issues this warning when it finds nets with missing delay arc annotations.

WHAT NEXT

To back-annotate delays onto the design, use the **read_sdf** command or a series of **set_annotated_delay** commands.

LINT-124 (warning) The design has '%d' nets which do not have capacitance annotation on them. The nets with missing

annotations represent ’%f’ of all nets.

DESCRIPTION

You receive this warning message when the **check_design -post_layout -summary** command detects that the design has nets that do not have capacitance information back-annotated on them. The command reports the total number of all such nets and prints the percentage of nets with missing annotations.

The **check_design -only_post_layout -summary** command also issues this warning message when it finds nets with missing capacitance annotations.

WHAT NEXT

To back-annotate net capacitances on the design, use a series of **set_load** commands.

LNK

LNK-001 (error) Cannot read link_path file '%s'.

DESCRIPTION

The file, specified in the link_path variable, cannot be read. Either the file does not exist or it is not a DB file.

WHAT NEXT

Check the existence of the file in the search_path using the **which** command.

LNK-002 (information) Design '%s' is already linked.

DESCRIPTION

The specified design has already been linked.

WHAT NEXT

Verify that this is the design that you wanted to link.

LNK-003 (information) Design '%s' was not successfully linked: %d unresolved references.

DESCRIPTION

A summary message indicating that the link process failed for your design.

WHAT NEXT

See previous error messages for more details.

LNK-004 (error) Unsupported LSI reference '%s' to '%s'

cannot be resolved

DESCRIPTION

The linker tried to resolve a reference which was derived from an LSI netlist, and the reference a form that the tool does not support. This tool only supports fully name-based references from LSI netlists. Order-based or mixed order and name based references are not supported.

WHAT NEXT

Use another Synopsys tool to read the DB, link it, and write it out to a new DB file. This will resolve the naming issue.

LNK-005 (warning) Unable to resolve reference to '%s' in '%s'.

DESCRIPTION

During the link process, a reference in the design could not be resolved. This means that no match was found for the reference using the semantics of the link_path variable.

This message is generated only for the first instance of the reference. In order to see all of the instances that are unresolved, use "link_design -verbose".

WHAT NEXT

Examine the link_path variable, log messages, and use the **which** command to find out which files were loaded.

LNK-006 (warning) Cannot resolve instance %s/%s (%s).

DESCRIPTION

During the link process, a reference in the design could not be resolved. This message is for the instance that was trying to link to the reference.

This message is only displayed in verbose mode.

WHAT NEXT

Examine the link_path variable, log messages, and use the **which** command to find out which files were loaded.

LNK-007 (error) Cannot instantiate design '%s' in '%s'.

DESCRIPTION

During the link process, a reference was resolved, but the design to which it resolved cannot be instantiated due to errors in the read process.

This message is generated only for the first instance of the reference. Use "link_design -verbose" in order to see all of the instances of this design which could not be instantiated.

WHAT NEXT

Examine the output of the tool when design files were loaded to see what caused the design to be in a state that cannot instantiate.

LNK-008 (error) Cannot find port '%s' on design '%s', referenced by instance '%s'.

DESCRIPTION

During the link process, an instance in the design could not be resolved because a port on the instance was not found in the design. This indicates a mismatch between the pinout of the instance and the design to which it should have resolved.

For example, if you have only these three instances of an FD1 in a design:

```
  FD1 u1 ( .Q(n1), .CP(clock1), .D(data1));
  FD1 u2 ( .Q(n2), .CP(clock2), .D(data2));
  FD1 u3 ( .Q(n3), .CK(clock3), .D(data3));
```

There is a typo in the third instance, listing "CK" instead of "CP". By default, you will get the LNK-008 message for the first instance only.

```
Error: Cannot find port 'CK' on design 'FD1',
       referenced by instance 'u1'. (LNK-008)
```

This might seem confusing, since that instance does not have a CK port. But for a name-based reference, each instance expects at least the total of all listed ports. To see all instances which cannot be resolved, use the -verbose option to **link_design**:

```
Warning: Cannot resolve instance top/u1 (FD1). (LNK-006)
Warning: Cannot resolve instance top/u2 (FD1). (LNK-006)
Warning: Cannot resolve instance top/u3 (FD1). (LNK-006)
```

The LNK-006 messages are generated in addition to LNK-008.

WHAT NEXT

Examine the link_path variable, log messages, and use the **which** command to find out which files were loaded. This could also be due to a typo in the netlist source.

SEE ALSO

link_design (2). **LNK-006** (n).

LNK-009 (error) Reference '%s' to '%s' is missing the following ports:
%s.

DESCRIPTION

The linker tried to resolve a reference which had the correct number of ports, but was unable to match the ports on the reference to those on the target design or library cell. This is an indication of a mismatch between the library and the netlist.

WHAT NEXT

Verify that the library and netlist are in sync.

LNK-010 (error) Too few ports on instance '%s' of '%s' in '%s'.

DESCRIPTION

The specified reference to a design or library cell does not have enough ports. This indicates a mismatch between the library and the netlist.

WHAT NEXT

Make sure the library is correct. Then, verify that the netlist is referencing the correct cell.

LNK-011 (error) Too many ports on instance '%s' of '%s' in '%s'.

DESCRIPTION

The specified reference to a design or library cell has too many ports. This usually indicates a mismatch between the library and the netlist. It can also indicate that there are multiple conflicting references to the same library cell or black box. One such conflict is two references with different pin counts.

WHAT NEXT

This error will cause the link to fail. Make sure the library is correct. Then, verify that the netlist is referencing the correct cell.
If this occurs during black box creation, you would see additional messages, for example:

Error: Too many ports on instance 'u1' of '*SELECT_OP' in 'd1'. (LNK-011)

The first instance of *SELECT_OP for which a black box was created had fewer pins than this reference. This often happens with generic logic. Other than GTECH, PrimeTime does not support generic logic. In this case, the solution is to remove the design containing the generic logic from the link path, or add a wrapper design which creates a black box at a higher level.

LNK-012 (error) Width mismatch on port '%s' of reference to '%s' in '%s'.

DESCRIPTION

The linker matched a bused port on an instance with a bused port on a library cell, but bus width is different between the two. This could indicate an incorrect library or a netlist which is out of date with the library.

WHAT NEXT

Verify that your source is in sync with the library.

LNK-013 (error) Could not resolve %s port '%s' of reference to '%s' in '%s'.

DESCRIPTION

The linker could not find a port (bused or not) on an instance while resolving a

reference with a target library cell. This could indicate an incorrect library or a netlist which is out of date with the library.

WHAT NEXT

Verify that your source is in sync with the library.

LNK-014 (error) Could not resolve direction of port '%s' of reference to '%s' in '%s'.

DESCRIPTION

The linker matched a port on an instance with a port on a library cell, but the directions do not match. This might indicate an incorrect library or a netlist which is out of date with the library.

WHAT NEXT

Verify that your source is in sync with the library.

LNK-015 (Warning) Could not swap '%s' ('%s') with '%s'%s.

DESCRIPTION

You tried to swap a cell with a new design or lib cell, and this action failed. Additional information might be included with this message and previous messages.

WHAT NEXT

Action based on reasons given in message text.

LNK-016 (Information) %s failed due to previous errors.

DESCRIPTION

This is a summary message indicating that the given action was not accomplished.

WHAT NEXT

Action based on reasons given in text of previous messages.

LNK-018 (Error) Cannot swap cells; design is not linked.

DESCRIPTION

The current design is either unlinked or partially linked. Swapping a cell for a new library cell or design can only be done in the context of a linked design.

WHAT NEXT

Link the current design, then retry your swap operation.

LNK-019 (Error) Can only swap in a single target object.

DESCRIPTION

The specification for the design or library cell to **swap_cell** resulted in more than one object. Either you specified a list or used a collection that matched multiple objects.

WHAT NEXT

Narrow the search parameters so only a single object is selected.

LNK-020 (Error) Cannot swap in '%s': it is the current design.

DESCRIPTION

The design you specified is the current design and you cannot instantiate a design within itself.

WHAT NEXT

Select a different design.

LNK-021 (Information) Previous messages occurred while trying to do:

’%s’.

DESCRIPTION

While linking the design, an attempt was made to transfer some information from the source design files which you read to the final linked design and some diagnostics occurred. This message shows you what was attempted which caused the diagnostics.

WHAT NEXT

Action based on the messages referenced.

LNK-023 (error) Recursive hierarchy detected in design ’%s’: %s.

DESCRIPTION

The linker detected recursive hierarchy in the design that is being linked. This is a design error. The message will list the designs that create the recursion.

For example, if design A has an instance of B and design B has an instance of A, that is a recursive loop.

WHAT NEXT

Remove the recursion, reread the designs, and relink.

LNK-024 (Warning) All timing information (backannotation, exceptions, etc.) is being removed from design ’%s’. User-created annotations must be restored after relinking this design.

DESCRIPTION

When a design is linked and there is another design currently linked, the current design is unlinked before the new design is linked. When this occurs, all annotations on the currently linked design are removed. This includes any timing information loaded from DB or added by user commands.

The next time the design is linked, information originally loaded from DB will be automatically restored. For example, clocks stored in the DB which was read in to

PrimeTime will be recreated on the design. However, any information which was added to the design after the link can only be restored if it was saved with **write_script**. For example, if you used the create_clock command to create a new clock, this clock will not be automatically restored.

WHAT NEXT

To save the state of the design before linking a new design, use the write_script command. Then, after relinking the design, source the script which was written to restore all annotations.

, , ,

LNK-025 (information) Link interrupted. Unlinking design: please wait...

DESCRIPTION

You entered a control-C to interrupt the link before it completed. The design which was being linked will be unlinked.

WHAT NEXT

No action.

LNK-026 (warning) min library '%s' found in link_path.

DESCRIPTION

During the link process, a library has been found in the link path that is in use as a min library. Only the max library is used in the link path for min/max analysis with the **set_min_library** command.

WHAT NEXT

Remove the min library from the value of the **link_path** variable, and ensure that the max library is in the link path.

SEE ALSO

set_min_library (2), **link_path** (3).

LNK-028 (Warning) unable to apply some DB constraints because they were
cached in file '%s'
and that file no longer exists.

DESCRIPTION

While linking the design, an attempt was made to transfer some information from the source design DB files which you read to the final linked design. When that information (constraints, exceptions, and so on) is large, it is cached to disk after an initial link. On a subsequent link, that data will be reloaded and reapplied. If the file has been deleted between the first link and the subsequent link, this message is issued.

WHAT NEXT

Examine why the file may have been deleted. Equally, examine why you are linking a second time. Usually this is a bug in a script, for example, executing a command which does an implicit link, followed by an explicit link. It is usually best to pick one style: implicit or explicit. Synopsys recommends that you build the design explicitly, that is, read the files that you want, then issue a link_design command.

SEE ALSO

link_design(2).

LNK-030 (information) Using '%s' as link path for instance '%s'

DESCRIPTION

This informational message tells you that the **link_path_per_instance** variable has been used, and an a match has been found for an instance. The link path and the instance name are shown in the message. The link path should match your setting in **link_path_per_instance** for the instance.

This message is displayed only if the *-verbose* option is used with **link_design**.

WHAT NEXT

No action required. This is strictly for your information.

SEE ALSO

link_design (2). **link_path_per_instance** (3).

LNK-031 (warning) Replacing link path for '%s' with '%s'

DESCRIPTION

This message warns you that you have the same instance listed multiple times in the setting for the **link_path_per_instance** variable. For example, here the instance *i2* is listed twice.

```
set link_path_per_instance [list
   [list i2 "* lib1.db"]
   [list i2 "* lib2.db"]
   [list i2/u1/u1 "* lib1.db"]]
```

WHAT NEXT

Examine the setting for the **link_path_per_instance** variable, and ensure that only one valid link path exists per instance.

SEE ALSO

link_path_per_instance (3).

LNK-033 (error) Incorrect format for link_path_per_instance: %s

DESCRIPTION

This message tells you that the format for the **link_path_per_instance** variable is incorrect. Various things can be wrong. The variable must be a list. Each element is itself a list of exactly two elements, where the first sub-element is a list of instances, and the second is a valid link path. The content of the message will isolate where the problem exists.

WHAT NEXT

Correct the setting for the **link_path_per_instance** variable.

SEE ALSO

link_path_per_instance (3).

LNK-034 (information) Removing %d unneeded designs.....

DESCRIPTION

This message tells you that a number of designs are being deleted following a successful link. This message is issued when you issue **link_design** command without using the **-keep_sub_designs** option or issued a command that performed an implicit link.

WHAT NEXT

No action is required. This is just information only.

SEE ALSO

link_design (2).

LOGDB

LOGDB-0 (error) Design is currently not represented as a PLA.

DESCRIPTION

WHAT NEXT

LOGDB-1 (error) Cells at the current level of the design are not combinational.

DESCRIPTION

WHAT NEXT

LOGDB-2 (error) Cannot write out design with INOUT ports.

DESCRIPTION

WHAT NEXT

LOGDB-3 (error) Cannot write out design with ports with unknown direction.

DESCRIPTION

WHAT NEXT

LOUT

LOUT-1 (warning) %s '%s' is renamed to '%s' in design '%s' because it isn't a legal name.

DESCRIPTION

WHAT NEXT

LOUT-2 (warning) %s '%s' is renamed to '%s' in design '%s' because of %s of the same name.

DESCRIPTION

WHAT NEXT

LOUT-3 (warning) Pin '%s' on cell '%s' has no direction. Not written.

DESCRIPTION

WHAT NEXT

LOUT-4 (information) Net '%s' is renamed to '%s' in design '%s' because it's connected to the port by that name.

DESCRIPTION

WHAT NEXT

LOUT-5 (warning) The name of net '%s' in design '%s'

can’t be changed to the name of both ports ’%s’ and ’%s’ to which it’s connected.

DESCRIPTION

WHAT NEXT

LOUT-6 (warning) Direction of port ’%s’ in design ’%s’ is unknown.

It will not be declared as a port in the output LSI/NDL netlist.

DESCRIPTION

This message is generated by the LSI/NDL writer whenever it encounters a port with an ’unknown’ direction. The port is not written out into the LSI/NDL netlist, even though references to the port may exist.

This symptom is most commonly caused by writing out LSI/NDL from a database that has been built with missing references. This causes port directions in the database to be unresolved since the lower level cells that contain the port are not available.

WHAT NEXT

Create and link the database so that the system does not return any errors.

LOUT-7 (error) (Internal error) Pin ’%s’ cannot be found in cell ’%s’.

DESCRIPTION

We do not expect this message ever to be issued. But if it is, contact your AE for further assistance because it indicates an internal error.

This error message is issued when the LSI/NDL writer is attempting to write out the output-connection list and input-connection list. It indicates that an incorrect pin, as named in the message, has been associated with the current cell (named in the message) being processed. This symptom can be caused by writing out LSI/NDL from a database that has been built with missing references.

WHAT NEXT

Create and link the database so that the system does not return any errors. Call your AE for further assistance.

LSIN-1 (error) Can’t open the input file.

DESCRIPTION

WHAT NEXT

LSIN-2 (warning) File %s [Line %d]:
’%s’ is not supported as an NC value .This is being reset to ’0’ [logic zero]

DESCRIPTION

WHAT NEXT

LSIN-3 (error) File %s, line %d: Mixed explicit and implicit

connections.

DESCRIPTION

WHAT NEXT

LSIN-4 (error) File %s, line %d: Module '%s' used inconsistently.

DESCRIPTION

WHAT NEXT

LSIN-5 (error) File %s, line %d: Illegal %s specification.

DESCRIPTION

WHAT NEXT

LSIN-6 (warning) File %s, line %d: Unsupported NC connection.

DESCRIPTION

WHAT NEXT

LSIN-7 (error) File %s, line %d: Component '%s' could not be

found.

DESCRIPTION

WHAT NEXT

LSIN-8 (error) File %s, line %d: Cell ’%s’ could not be added.

DESCRIPTION

WHAT NEXT

LSIN-9 (warning) File %s, line %d: %s port ’%s’ specified twice.

DESCRIPTION

WHAT NEXT

LSIN-10 (warning) The value of variable ’lsiin_net_name_prefix’ isn’t valid--using ’NET_’.

DESCRIPTION

WHAT NEXT

LSIN-11 (error) File %s [Line %d]:

%s is not a valid NC value.

DESCRIPTION

WHAT NEXT

LSIN-12 (warning) File %s [Line %d]: ’use_global’ is not supported.

DESCRIPTION

This warning message is caused by the **USE_GLOBAL** keyword. The global signals feature is not supported now.

WHAT NEXT

Delete **USE_GLOBAL**, and define local signals instead.

MCMM-101 (error) Must give one of *-hosts*, *-lsf*, *-grd*, or *-nqs*.

DESCRIPTION

This error message occurs when you have not given any option to specify the distributed computing mode. The currently supported modes are *-hosts*, *-lsf*, *-grd*, or *-nqs*.

WHAT NEXT

Give exactly one of these options.

SEE ALSO

set_mcmm_job_options(2)

MCMM-102 (error) Cannot give more than one distributed computing mode option.

DESCRIPTION

This error message occurs when you specify more than one distributed computing mode. The currently supported modes are *-hosts*, *-lsf*, *-grd*, or *-nqs*.

WHAT NEXT

Give exactly one of the options.

SEE ALSO

set_mcmm_job_options(2)

MCMM-103 (error) Option %s is valid only in host mode.

DESCRIPTION

This error message occurs when you give an option that is valid only in host mode (i.e. the *-hosts* option).

WHAT NEXT

Remove the offending option.

SEE ALSO

set_mcmm_job_options(2)

MCMM-104 (error) Option %s is valid only for compute farm modes.

DESCRIPTION

This error message occurs when you give an option that is valid only in compute farm mode (i.e. the *-lsf*, *-grd*, or *-nqs* options).

WHAT NEXT

Remove the offending option or give one of the compute farm options.

SEE ALSO

set_mcmm_job_options(2)

MCMM-105 (error) Option %s is valid only in GRD mode.

DESCRIPTION

This error message occurs when you give an option that is valid only in GRD mode (i.e. the *-grd* option).

WHAT NEXT

Remove the offending option.

SEE ALSO

set_mcmm_job_options(2)

MCMM-106 (error) Distributed MCMM job options are not

properly set.

DESCRIPTION

This error message occurs when you try to run Distributed MCMM without first having specified a useable set of job options with the *set_mcmm_job_options* command.

WHAT NEXT

Use the *set_mcmm_job_options* command to set up the job options.

SEE ALSO

set_mcmm_job_options(2)
get_dominant_scenarios(2)

MCMM-110 (error) Could not read TCL variables from file %s.

DESCRIPTION

This error message occurs the Distributed MCMM slave flow could not read the TCL variable state from the given file. Either the file does not exist in the correct location, there is a problem accessing the correct directory, or its contents have become damaged.

WHAT NEXT

Review any warning or error messages from the main Distributed MCMM flow to see if the file was properly created.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-111 (error) No scenarios are active.

DESCRIPTION

The command cannot run because there are no active scenarios. Most likely the current design is not a multi-scenario design.

WHAT NEXT

Review the results of the commands that were originally supposed to have created the scenarios.

SEE ALSO

get_dominant_scenarios(2)
report_scenarios(2)

MCMM-112 (error) The distributed MCMM flow did not run correctly.

DESCRIPTION

An error occurred during the Distributed MCMM flow, and it did not finish properly. Quite possibly one of the slave jobs did not run correctly due to network, fileserver, or compute farm problems.

WHAT NEXT

Review any previous warning or error messages from the run, and also review the log files for each slave job. If only one or a few slave jobs did not run correctly, it may be possible to manually re-run them, and then run "get_dominant_scenarios -process_distributed" to post-process all the results.

SEE ALSO

get_dominant_scenarios(2)

MCMM-113 (error) Data from the distributed MCMM flow could not be processed successfully.

DESCRIPTION

An error occurred during the post-processing phase of the Distributed MCMM flow, and it did not finish properly. The slave jobs presumably finished successfully, but the results files (<scenario_name>.gds) could not be read and processed.

WHAT NEXT

Review any previous warning or error messages from the run, and also review the log files for each slave job. Examine the work dir to see if there is a .gds file for every scenarios that was to be analyzed.

SEE ALSO

get_dominant_scenarios(2)

MCMM-114 (error) No valid scenarios were specified.

DESCRIPTION

No valid scenario names were given to *get_dominant_scenarios*, and the command cannot run.

WHAT NEXT

Ensure that each scenario name given to get_dominant_scenarios actually exists.

SEE ALSO

get_dominant_scenarios(2)

MCMM-115 (error) Cannot run in threaded mode without setting max_cores.

DESCRIPTION

get_dominant_scenarios cannot run in threaded mode unless the *max_cores* parameter is set with the **set_host_options** command.

WHAT NEXT

Set the max_cores parameter with **set_host_options -max_cores <n>**.

SEE ALSO

set_host_options(2)

MCMM-120 (error) Could not determine the path to the ICC

executable.

DESCRIPTION

The Distributed MCMM flow could not determine where the ICC executable is located. Possibly the ICC installation is non-standard

WHAT NEXT

Ensure that the $synopsys_root and $arch TCL variables have appropriate values.

SEE ALSO

get_dominant_scenarios(2)

MCMM-121 (error) The ICC executable %s does not exist, or does not have execute permission.

DESCRIPTION

The Distributed MCMM flow could not find a usable ICC executable. Possibly the ICC installation is non-standard, or an incorrect executable path was specified via the *set_mcmm_job_options* command.

WHAT NEXT

Ensure that the $synopsys_root and $arch TCL variables have appropriate values. If *set_mcmm_job_options -exec* was used, ensure that it referred to a valid ICC executable.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-122 (error) Could not create file %s in the Distributed MCMM work directory.

DESCRIPTION

The Distributed MCMM flow could not create the given file in the work directory.

WHAT NEXT

Review any previous warning or error messages from the Distributed MCMM flow. Ensure that the work directory actually exists and is writable. Ensure that the work directory does not contain an existing file of this name that cannot be overwritten.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-123 (error) Problem writing parasitics files to the Distributed MCMM work directory.

DESCRIPTION

The Distributed MCMM flow could not write all the necessary binary parasitics files (*.sbpf) to the work directory.

WHAT NEXT

Review any previous warning or error messages from the Distributed MCMM flow. Ensure that the work directory actually exists and is writable. See if the *extract_rc* and *write_parasitics -format SBPF* commands work correctly.

SEE ALSO

extract_rc(2)
get_dominant_scenarios(2)
set_mcmm_job_options(2)
write_parasitics(2)

MCMM-124 (error) Problem writing the TCL variable file %s to the Distributed MCMM work directory.

DESCRIPTION

The Distributed MCMM flow could not write the TCL variable file to the work directory.

WHAT NEXT

Review any previous warning or error messages from the Distributed MCMM flow. Ensure that the work directory actually exists and is writable.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-125 (error) Problem writing the library attributes script file %s to the Distributed MCMM work directory.

DESCRIPTION

The Distributed MCMM flow could not write the library attributes script file to the work directory.

WHAT NEXT

Review any previous warning or error messages from the Distributed MCMM flow. Ensure that the work directory actually exists and is writable.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-126 (error) Problem writing the netlist file %s to the Distributed MCMM work directory.

DESCRIPTION

The Distributed MCMM flow could not write the design netlist file to the work directory.

WHAT NEXT

Review any previous warning or error messages from the Distributed MCMM flow. Ensure that the work directory actually exists and is writable.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-127 (error) User-specified work directory %s does not

exist or is not a directory.

DESCRIPTION

The user-specified work directory for Distributed MCMM does not exist or is not a directory. Generally, an existing file of the same name will prevent Distributed MCMM from being able to create the work directory. In certain modes of operation, Distributed MCMM expects the work directory to already exist, and will not automatically create it.

WHAT NEXT

Ensure that the work directory actually exists and is a writable directory.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-128 (error) Could not determine absolute path name for file or directory %s.

DESCRIPTION

ICC could not expand the given file or directory name to a full rooted pathname (i.e. starting with "/").

WHAT NEXT

Ensure that the given name is a legal file or directory name. Ensure that the present working directory of the ICC process is known. Ensure that there are no filesystem or network problems.

SEE ALSO

get_dominant_scenarios(2)
pwd(2)
set_mcmm_job_options(2)

MCMM-129 (warning) Script file %s does not exist or is not

readable.

DESCRIPTION

The given script file does not exist or is not readable. This is considered a warning rather than a fatal error, since you may be able to create the file or otherwise resolve the problem before the file is actually read by the Distributed MCMM slave jobs.

WHAT NEXT

Ensure that the given script file exists and is readable. Ensure that there are no filesystem or network problems.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-130 (error) Could not create the work directory %s.

DESCRIPTION

ICC could not create a given work directory with the given name (either auto-generated or user-specified).

WHAT NEXT

Ensure that the given name is a legal directory name. Ensure that there is not already a regular file of the same name. Ensure that the present working directory of the ICC process is writable. Ensure that there are no filesystem or network problems.

SEE ALSO

get_dominant_scenarios(2)
pwd(2)
set_mcmm_job_options(2)

MCMM-131 (error) The work directory %s is not writable.

DESCRIPTION

The user-specified work directory exists, but is not writable.

WHAT NEXT

Check the filesystem permissions for the directory.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-132 (error) There must be a user-defined work directory.

DESCRIPTION

In the current mode of operation, the Distributed MCMM flow needs to have a pre-existing user-specified work directory that already contains the necessary data and script files.

WHAT NEXT

Specify the work directory with the *set_mcmm_job_options* command.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-133 (error) Could not build a temporary directory name under %s.

DESCRIPTION

ICC could not construct a usable directory name (of the form mcmm_xxxx) under the given directory.

WHAT NEXT

Ensure the parent directory exists and is writable. Ensure that there are no filesystem or network problems.

SEE ALSO

get_dominant_scenarios(2)
pwd(2)
set_mcmm_job_options(2)

MCMM-134 (error) Could not create the work directory %s.

DESCRIPTION

ICC could not create the given directory.

WHAT NEXT

Ensure the parent directory exists and is writable. Ensure that there are no filesystem or network problems.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-135 (error) No valid hosts have been specified.

DESCRIPTION

None of the hosts specified by the *set_mcmm_job_options -hosts* command actually exist, or they are all inaccessible.

WHAT NEXT

Check the host list given to the *set_mcmm_job_options* command. Ensure that there are no network problems.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-136 (error) Could not submit job to the %s compute farm.

DESCRIPTION

Job submission to the given compute farm (LSF or GRD) failed.

WHAT NEXT

Ensure that the job submission command (by default /lsf/bin/bsub or /lsf/bin/qsub) actually works. If necessary specify an alternate job submission command with the *set_mcmm_job_options* command.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-137 (error) Could not submit job to host %s.

DESCRIPTION

Job submission to the given compute host failed.

WHAT NEXT

Ensure that the given host is actually accessible, and that it will accept remote commands for the current user via the Unix *rsh* command.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-138 (error) The %s batch submission program %s does not exist, or is not executable.

DESCRIPTION

The default or user-specified LSF/GRD batch submission program does not exist, or does not have execute permission.

WHAT NEXT

Ensure that the job submission command (by default /lsf/bin/bsub or /lsf/bin/qsub) actually exists and works. If necessary specify an alternate job submission command with the *set_mcmm_job_options* command.

SEE ALSO

get_dominant_scenarios(2)

MCMM-139 (error) Could not set up master-slave inter-process communication.

DESCRIPTION

Distributed MCMM's inter-process communication mechanism did not start up properly. This is not caused by a problem with a particular remote host, but by a problem with the master ICC job's networking, threading, or IPC environment.

WHAT NEXT

Check for any networking or Unix system configuration problems.

SEE ALSO

get_dominant_scenarios(2)

MCMM-140 (error) Could not determine the local host name.

DESCRIPTION

ICC cannot determine the local host name. This is the name that would be returned by the Unix *hostname* command.

WHAT NEXT

Check for any networking or Unix system configuration problems.

SEE ALSO

get_dominant_scenarios(2)

MCMM-141 (warning) Could not find remote host %s. Skipping.

DESCRIPTION

ICC cannot find a remote host of the given name. The host name will be ignored, and Distributed MCMM execution will continue without it.

WHAT NEXT

Check the all the host names specified by the *set_mcmm_job_options -hosts* command are valid. Check for any networking or Unix system configuration problems.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-142 (error) Could not write scenario analysis data to file %s.

DESCRIPTION

This error message occurs a Distributed MCMM slave could not create a scenario analysis data file for a particular scenario. Either there is a problem accessing the Distributed MCMM work directory, or there is an existing file that cannot be overwritten.

WHAT NEXT

Review any previous warning or error messages from the Distributed MCMM flow. Ensure that the work directory actually exists and is writable.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-143 (error) Syntax error in violation file %s at line %d.

DESCRIPTION

There is a syntax error in the get_dominant_scenarios violation file at the given line number. Either the file was not generated correctly, or has been damaged.

WHAT NEXT

Review any previous warning or error messages from the Distributed MCMM flow. Ensure that the file has not become corrupted.

SEE ALSO

get_dominant_scenarios(2)

MCMM-144 (error) Could not properly read scenario analysis data file %s.

DESCRIPTION

This error message occurs when get_dominant_scenarios could not access a scenario analysis data file, or the file has syntex errors. Either the file does not exist, does not have read permission, or has become corrupted. This could happen in the Distributed MCMM flow if any of the slave jobs (which create these data files) did not finish properly.

WHAT NEXT

Review any previous warning or error messages from the Distributed MCMM flow. Ensure that the work directory actually exists and is readable.

SEE ALSO

get_dominant_scenarios(2)

MCMM-145 (error) Error while reading violation file.

DESCRIPTION

There has been a syntax error in the get_dominant_scenarios violation file that is being read. A previous message should have described the error in more detail.

WHAT NEXT

Review any previous warning or error messages from the Distributed MCMM flow. Ensure that the file has not become corrupted.

SEE ALSO

get_dominant_scenarios(2)

MCMM-146 (error) Violation data for scenario %s has already

been read.

DESCRIPTION

Get_dominant_scenarios is reading multiple violation files, and data for the same scenario has been found in more than one file.

WHAT NEXT

Review any previous warning or error messages from the Distributed MCMM flow. Ensure that none of the files have become corrupted.

SEE ALSO

get_dominant_scenarios(2)

MCMM-147 (warning) Can’t notify master- we are not a slave.

DESCRIPTION

If this warning occurs during an automatically-run Distributed MCMM slave job, then there has been some problem with the master-slave communication mechanism. This warning will always occur if a Distributed MCMM slave job script is manually run. In this case, it may safely be ignored.

WHAT NEXT

Review any previous warning or error messages from the Distributed MCMM flow.

SEE ALSO

get_dominant_scenarios(2)

MCMM-205 (error) Cannot create signature file under working directory

DESCRIPTION

This error message is generated if the master cannot generate a signature file under the working directory. The signature file is used by slaves to check that the work directory seen by master is also visible by slaves.

WHAT NEXT

Check the permission of the current directory from where the master is launched. The permission must be writeable, readable and executable.

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-206 (info) The following TLUPlus file(s) are changed:

DESCRIPTION

This information message is generated when the TLUPlus files are re-defined for current scenario.

WHAT NEXT

This is an information message to inform you that TLUPlus files are being overwritten. No action is required if you intended to overwrite teh TLUPlus files.

SEE ALSO

MCMM-207 (warning) Clock names, sources, and/or periods are different across scenarios.

DESCRIPTION

This warning message is issued when the clock names do not match the clock sources accross scenarios or there are difference in clock periods for the same clock source, etc.

WHAT NEXT

You can ignore this warning if you intend to have such a clock setup.

SEE ALSO

report_clock(2)

MCMM-208 (warning) Design timing derates might not be set correctly for the following scenario(s).

DESCRIPTION

This error message is generated when the tool found that design timing derate(s) might not be set correctly for listed scenario(s).

WHAT NEXT

Please check the setting on the design timing derate to see if the derates are set as intented.

SEE ALSO

set_timing_derate(2)

-

MCMM-209 (info) The following scenario(s) are set as hold, but timing_remove_clock_reconvergence_pessimism variable is set to false. Set this variable to true for better QoR.

DESCRIPTION

This message is isue when the scenario is set as hold-only, but you have not enabled the optimization that improves hold violations.

WHAT NEXT

Set the timing_remove_clock_reconvergence_pessimism variable to true to improve hold violations.

SEE ALSO

timing_remove_clock_reconvergence_pessimism

MCMM-210 (warning) Scenario (%s) contains ILM (%s) with mis-matched PVT as compare to what is defined in top level

design.

DESCRIPTION

This warning message is issued when the specified scenario has PVT values does not match the PVT of their parents. This condition is required by the tool. The tool requires that the the PVT values specified in the ILM match the PVT values of the parent design.

WHAT NEXT

Modify the PVT values.

SEE ALSO

set_operating_conditions(2)

MCMM-211 (warning) Scenario (%s) does not have TLU+ defined.

DESCRIPTION

This message is generated when the tool found that the listed scenario(s) do not have TLU+ files defined. This condition is required by the tool.

WHAT NEXT

User need to define TLU+ for the listed scenario.

SEE ALSO

check_tlu_plus_files(2)
set_tlu_plus_files(2)

MCMM-212 (warning) The complexity of the %s (%s) might cause long runtime and high memory usage.

DESCRIPTION

This warning message is issued when the tool detects that this design might have many timing exceptions which might cause by timining exceptions which result in long run time and high memory usage.

WHAT NEXT

Timing complexity may be increased by the addition of timing exceptions to the design. Please check your timing constraints to see if exceptions (set_false_path, set_multicycle_path...) have been applied, and if so, whether they have been applied in an efficient manner.

An example of an inefficient application is shown here:

```
set_false_path -from [get_cells I1/RegA[*]] -to [get_cells I2/RegB[*]]
```

This will create a point-to-point exception from I1/RegA[0] to I2/RegB[0] and one to RegB[1] .. all the way through the Register Bus RegB. It may be that you only need to create an exception from RegA[0] to RegB[0], RegA[1] to RegB[1] etc etc In which case, applying the constraints in a loop, point-to-point is more efficient

If you did intend to apply constraints from RegA[*] to RegB[*], consider creating a virtual clock to clock Both RegA[*] and RegB[*] cells and set the false path -from the virtual clock to the virtual clock. This is a single exception that covers the requirement.

Secondly, by setting timing_remove_clock_reconvergence_pessimism variable to true, clock reconvergence pessimism while increasing the correctness of timing will increase the complexity measure of the design. For hold scenearios, it is recommended this variable set to true for better QoR.

SEE ALSO

MCMM-213 (warning) %s (%s) has a library setup issue with regard to the PVT values and the operating condition.

DESCRIPTION

This warning message is issued when the specified scenario has a library setup issue with PVT definitions and the operating conditions of the library cells.

WHAT NEXT

Look at the table generated along with this message which lists the lib cells that do not have matching operating condition, click on the lib cell, this will bring forward anther table which lists the libraries contain the lib cells, along with available PVT and operating condition needed by the lib cell. Please look at the list and choose the appropriate libraries.

SEE ALSO

set_operating_conditions(2)

MCMM-214 (error) Please check your ICC environment on machine <name>.

DESCRIPTION

This error message is generated if the master process cannot invoke the helper script "helper.sh" in the Distributed MCMM work directory.

WHAT NEXT

Run <work_dir>/.helper.sh from the unix shell where master icc_shell was invoked. Check if SYNOPSYS_ROOT variable is a valid path where the icc_shell executable is available.

Try issuing the command "rsh <machine_name> -login <login_name> `$path/helper.sh` where $path is the full path to the Distributed MCMM work directory. If the command fails you may need to check the reason. Sometimes the user may have problems in the environment setting, e.g "rsh is not in the user path".

SEE ALSO

get_dominant_scenarios(2)
set_mcmm_job_options(2)

MCMM-218 (error) ICC shell executable on machine <machine_name> has different label.

DESCRIPTION

The error message is generated if the master and the slave executables are not from same installation.Both master and slave should have same synopsys_root. Check the shell scripts generated n the work directory by the setup stage and ensure that the synopsys root is same as in the master.

The message can also be generated if the user cannot do rsh to the slave machine. Run "rsh <machine_name>" from the master shell and check if there is any problem to acesss the specified machine name.

WHAT NEXT

Fix the rsh problem. Also make sure that master and slave runs using same synopsys root. Open "helper.sh" shell script in the Distributed MCMM work directory and verify that the SYNOPSYS_ROOT variable is the same as the synopsys_root for master icc_shell.

SEE ALSO

```
get_dominant_scenarios(2)
set_mcmm_job_options(2)
```

MCMM-219 (warning) Library (%s) has different or is missing nominal and/or default PVTs (def: %.2f %.2f %.2f - nom: %.2f %.2f %.2f).

DESCRIPTION

```
This message is generated when the tool found that the listed scenario(s) have
library setup issue with respect to pvt and opcond.
```

WHAT NEXT

```
Examine nom and default PVTs for the list libraries.
```

SEE ALSO

```
create_operating_conditions(2)
report_operating_conditions(2)
set_operating_conditions(2)
```

MCMM-220 (warning) Scenario (%s) is defined in the top level but not defined in the block (%s).

DESCRIPTION

```
This warning message is issued when the scenario is defined in the top level but not
in the specified block. The set of scenarios from top level should be a subset of
the scenarios defined in the ILM.
```

WHAT NEXT

```
Create the missing scenarios for the specified block
```

SEE ALSO

```
report_scenarios(2)
create_scenarios(2)
```

MCMM-221 (warning) Scenario (%s) contains ILM (%s) with mis-matched TLUPlus files.

DESCRIPTION

This warning message is issued when TLUPlus files for the scenario in the ILM does not match the TLUPlus files of the parents. This is a requirement of the tool.

WHAT NEXT

Change the TLUPlus setting.

SEE ALSO

set_tlu_plus_files(2)

MCMM-222 (warning) Operation condition for scenario (%s) is not defined.

DESCRIPTION

This warning message is issued when operating condition for listed scenario is not defined. This is a requirement of the tool.

WHAT NEXT

Setup operating condition by using set_operationg_condition command.

SEE ALSO

set_operating_condition(2)

MCMM-223 (warning) Design (%s) has missing library cells.

DESCRIPTION

This warning message is issued when the specified scenario has missing library cells compare to other scenarios.

WHAT NEXT

Look at the table generated along with this message which lists the missing lib cells, these library cells might be needed by the tool for better performance.

SEE ALSO

MCMM-224 (warning) Scenario (%s) has unresolved references.

DESCRIPTION

This warning message is issued when the specified scenario or design has unresolved references.

WHAT NEXT

Look at the table generated along with this message which lists the unresolved references. These references need to be resolved.

SEE ALSO

MCMM-225 (warning) %s (%s) has instances which referenced library cells that are marked as "dont_use".

DESCRIPTION

This warning message is issued when the specified scenario has instances referenced library cells that are marked as dont_use.

WHAT NEXT

Look at the table generated along with this message which lists the instances which reference these dont_use lib cells. If this is your intention, no action is required.

SEE ALSO

MCMM-226 (warning) Scenario (%s) does not have the required

gate(s): %s.

DESCRIPTION

This warning message is issued when the specified design/scenario does not have required gates.

WHAT NEXT

The system detects that the loaded libraries do not have required gates, please fix the issue before continue on.

SEE ALSO

MCMM-227 (warning) Design contains ambiguous library cells, both library cells are of the same voltage (%fV), process (%f), and temperature (%f).

DESCRIPTION

This warning message is issued when your $link_libraries and $target_libraries contain multiple libraries which characterize the same lib_cells for the same voltage, process, and temperature. The tool has no way to distinguish which library should be used.

WHAT NEXT

Remove one of the ambiguous libraries from your $link_library and $target_library. If you wanted to use both libraries, and they represent different characterization points, the libraries would need to have different nominal_voltage, nominal_process, and nominal_temperature values. The tool matches these library values with the operating condtions applied to the design, to decide which libraries are suitable for the design cells.

SEE ALSO

MCMM-228 (warning) The following library cells are

inconsistent:

DESCRIPTION

This warning message is issued when your $link_libraries and $target_libraries contain multiple library cells that are of the same name but inconsistent, a typical example would be different set of pins or the pin ordering are different.

WHAT NEXT

Remove one of the inconsistent libraries from your $link_library and $target_library.

SEE ALSO

MEM-1 (error) Pointer %s is not within the range of allocated memory.

DESCRIPTION

This error indicates a potentially serious problem with the internal memory management of the program you are running. It mght lead to a fatal error or have no noticible effect. In very rare cases you can get incorrect results from the program after one of these messages.

WHAT NEXT

If the program appears to execute properly after this message, it is usually OK to continue. It is safest to save your work and exit the program as soon as possible.

In any event, please report the problem to Synopsys.

MEM-2 (error) A memory pad has been overwritten at 0x%x.

DESCRIPTION

This error indicates a potentially serious problem with the internal memory management of the program you are running. It might lead to a fatal error or have no noticible effect. In very rare cases, you can get incorrect results from the program after one of these messages.

WHAT NEXT

If the program appears to execute properly after this message, it is usually OK to continue. It is safest to save your work and exit the program as soon as possible.

In any event, please report the problem to Synopsys.

MEM-3 (error) Pointer was never allocated, was already freed or was not allocated from an item free group.

DESCRIPTION

This error indicates a potentially serious problem with the internal memory

management of the program you are running. It might lead to a fatal error or have no noticible effect. In very rare cases, you can get incorrect results from the program after one of these messages.

WHAT NEXT

If the program appears to execute properly after this message, it is usually OK to continue. It is safest to save your work and exit the program as soon as possible.

In any event, please report the problem to Synopsys.

MEM-4 (error) Memory group structure is not intact.

DESCRIPTION

This error indicates a potentially serious problem with the internal memory management of the program you are running. It might lead to a fatal error or have no noticible effect. In very rare cases, you can get incorrect results from the program after one of these messages.

WHAT NEXT

If the program appears to execute properly after this message, it is usually OK to continue. It is safest to save your work and exit the program as soon as possible.

In any event, please report the problem to Synopsys.

MEM-5 (fatal) Out of memory.

DESCRIPTION

This error is generated when there is not enough memory to run the Design Compiler.

WHAT NEXT

Check your machine memory and reinvoke the Design Compiler.

MEM-6 (warning) A call to SBRK has been made outside the

memory allocator. This should be avoided.

DESCRIPTION

This error indicates a potentially serious problem with the internal memory management of the program you are running. It might lead to a fatal error or have no noticible effect. In very rare cases, you can get incorrect results from the program after one of these messages.

WHAT NEXT

If the program appears to execute properly after this message, it is usually OK to continue. It is safest to save your work and exit the program as soon as possible.

In any event, please report the problem to Synopsys.

MEM-7 (error) %s

DESCRIPTION

This error indicates a potentially serious problem with the internal memory management of the program you are running. It might lead to a fatal error or have no noticible effect. In very rare cases, you can get incorrect results from the program after one of these messages.

WHAT NEXT

If the program appears to execute properly after this message, it is usually OK to continue. It is safest to save your work and exit the program as soon as possible.

In any event, please report the problem to Synopsys.

MENO

MENO-1 (error) No schematic exists for design ’%s’.

DESCRIPTION

WHAT NEXT

MENO-2 (error) Design ’%s’ has no external_scale defined in its symbol library.

DESCRIPTION

WHAT NEXT

MENO-3 (error) Design ’%s’ has no route_grid defined in its symbol library.

DESCRIPTION

WHAT NEXT

MENO-4 (warning) Design ’%s’ has no landscape defined; assuming landscape.

DESCRIPTION

WHAT NEXT

MENO-5 (error) All pins on symbol ’%s’ in library ’%s’ must have

same Y coordinate.

DESCRIPTION

WHAT NEXT

MENO-6 (error) Net connector symbol ’%s’ in library ’%s’ has %d pins; two are required.

DESCRIPTION

WHAT NEXT

MENO-7 (warning) Sheet ’%s’ of design ’%s’ exceeds Mentor’s maximum size of %0.2f.

DESCRIPTION

WHAT NEXT

MENO-8 (error) Off-sheet connector symbol ’%s’ has no name

text.

DESCRIPTION

WHAT NEXT

MENO-9 (error) Port symbol ’%s’ has no name text.

DESCRIPTION

WHAT NEXT

MENO-10 (error) Symbol ’%s’ has no name text.

DESCRIPTION

WHAT NEXT

MENO-11 (warning) Cannot fix feedthroughs on sheet ’%s’; no NETCON symbol found.

DESCRIPTION

WHAT NEXT

MENO-12 (warning) Symbol ’%s’ exceeds Mentor’s maximum

size of %0.2f.

DESCRIPTION

WHAT NEXT

MENO-13 (error) Pin ’%s’ of symbol has unknown direction.

DESCRIPTION

WHAT NEXT

MENO-14 (warning) Unable to fix all feedthroughs on sheet ’%s’ of design ’%s’.

DESCRIPTION

WHAT NEXT

MENO-15 (information) Instance of connector symbol ’%s’ is

being treated as a port.

DESCRIPTION

WHAT NEXT

MENO-16 (information) Design '%s' had %d name changes.

DESCRIPTION

WHAT NEXT

MENO-17 (warning) Can't write symbol information for connector '%s'.

DESCRIPTION

WHAT NEXT

MENO-18 (error) Can't find the symbol libraries attached to design '%s'.

Check the value of the ’search_path’ variable.

DESCRIPTION

WHAT NEXT

MENO-19 (error) Can’t write out a bussed design ’%s’.

DESCRIPTION

WHAT NEXT

MENO-20 (error) No schematic or symbol exists for design ’%s’.

DESCRIPTION

WHAT NEXT

MENO-21 (information) Schematic ’%s’ might have been modified due to netcon insertion.

DESCRIPTION

This message is issued when the Mentor Do writer is executed. If "netcons" are inserted into the schematic, the schematic database from which the writer extracts data may have been modified with those instances. Note that this message is issued when the Mentor Do writer operates, and not when a "netcon" is actually inserted. To determine whether the "netcon" has been inserted into the schematic, examine the schematic after transferring it to the Mentor/Neted system, or by perusing the generated Do-file.

WHAT NEXT

This is not a problem unless "netcon" insertion actually takes place and the user plans to write other data from the same design database the Mentor Do-file was written from. In such a case, "netcons" will appear in the other target format.

To avoid the above situation, regenerate the schematic with the **create_schematic**

command after the Mentor Do writer has completed execution.

Note that "netcons" are inserted within shorted nets (ports) to satisfy design-check criteria on the Mentor/Neted system. To avoid shorted nets altogether, you might consider setting the I/O variable *compile_fix_multiple_port_nets* to "true" prior to running the **compile** command. This action causes buffers to be inserted within shorted nets (ports), which in turn obviates the need for "netcon" insertion. As noted in the **DESCRIPTION** section, however, the diagnostic will still be issued.

MENO-22 (warning) Symbol for cell '%s' in design '%s' is too large for the sheet.

DESCRIPTION

This message is generated when the writer tries to place an instance of a cell within the schematic for a design, causing the symbol boundary to extend beyond the sheet.

WHAT NEXT

This situation is usually caused by autogenerated symbols that have a large number of ports. Regenerate the schematic within Design Analyzer using the next larger sheet size.

MENU-001 (Error) Menu name is empty.

DESCRIPTION

WHAT NEXT

MENU-002 (Error) The menu name needs to be a full hierarchical menu name.

DESCRIPTION

A full hierarchical menu name needs to be specified for the menu name. An example: "&File->Exit".

WHAT NEXT

Checks the option value of the -menu option.

MENU-003 (Error) The -anchor_offset option value needs to be a positive/negative integer and not zero.

WHAT NEXT

Correct the option value of the -anchor_offset option.

MENU-004 (Error) -anchor_offset option needs to be specified

when -anchor_item option is present.

MENU-005 (Error) %s option value is specified incorrectly.

WHAT NEXT

Checks and correct the option value for the specified option.

MENU-006 (Error) -anchor_item option needs to be specified when -anchor_offset option is present.

MENU-007 (Error) Anchor menu item '%s' not found.

WHAT NEXT

Checks the spelling of the option value of the -anchor_menu option. Make sure that the anchor menu item already existed before this gui_add_menu command is called.

MENU-008 (Error) Menu bar items must be popup menus.

DESCRIPTION

First-level items on the menu bar must be popup menus.

WHAT NEXT

Check and correct the option value of the -menu option.

MENU-012 (Error) Menu root: %s not found.

WHAT NEXT

Check and correct the option value of the -menu_root option.

MENU-013 (Warning) Hotkey string: %s is either not supported or reserved by system for other use.

WHAT NEXT

Please check and correct the option value of the -hot_key option. This hotkey key combination may not be supported or has been reserved by the application for some other use. You can try to use another hotkey.

MENU-014 (Error) Duplicate menu item: %s .

DESCRIPTION

Another existiing menu item already has this menu name.

MENU-015 (Error) %s option is specified with invalid value: %s.

WHAT NEXT

Check and correct the option value of the specified option.

MENU-016 (Error) Cannot specify both -anchor_offset and -position options.

MENU-017 (Error) -position option value must not be a negative integer.

DESCRIPTION

Position option value must be zero or a positive integer. It specifies the position of the menu item within the parent popup menu.

MENU-018 (Warning) Specified hotkey %s for this menu item

%s will be ignored. Had been used for %s menu item.

DESCRIPTION

This hotkey has already been mapped to another existing menu item. So it will be ignored and not set for this menu item.

WHAT NEXT

Change the -hotkey option value to specify another hotkey or remove this option.

MENU-019 (Error) Menu item '%s' not found.

DESCRIPTION

The specified menu item was not found in the currently active window. It could not be executed.

WHAT NEXT

Check the menu name to make sure it matches an existing menu item in the active window.

MENU-020 (Error) There is no active main window.

DESCRIPTION

No active main window was found.

WHAT NEXT

Activate a main window before executing this command.

MENU-021 (Error) Menu %s is not a popup menu item.

WHAT NEXT

Add menu items to a popup menu, not to an item with associated command or action. Popup menus are created implicitly by specifying a full hierarchical menu name.

MENU-022 (Warning) Menu bar items must be popup menus. %s not added.

DESCRIPTION

First-level items on the menu bar must be popup menus.

WHAT NEXT

Do not explicitly create popup menus in hierarchical menus. Pop-up menus are created implicitly by creating command menu items with full hierarhcical names, e.g. "&File->&Open..." creates File pop-up menu in the menu bar.

MEXT-1 (error) Design '%s' does not have any connections between cells. Model extraction is not allowed on such designs.

DESCRIPTION

You received this message because you executed the **extract_model** command but the extractor detects that the netlist to be extracted does not have any effective net connectivities among the cells that are instantiated from the library.

WHAT NEXT

Please inspect the netlist and make sure there are effective connectivities among cell instances. This is to avoid improperly exposing timing related information in the libraries you are using.

MEXT-2 (warning) Variable 'extract_model_use_conservative_current_slew' is set to 'true' while design is in 'worst_arrival' slew propagation mode. The variable is not effective in this mode and therefore ignored in extraction.

DESCRIPTION

You received this message because you executed the **extract_model** command with variable 'extract_model_use_conservative_current_slew' set to 'true' while the design is in 'worst_arrival' slew propagation mode. The 'worst_arrival' slew propagation mode makes this model extraction variable not effective and therefore its value is ignored and it will have no impact on model extraction.

WHAT NEXT

Please decide what model you want. If you want the model to propagate the worst conservative slew calculated from the context slews set on input ports, put the design in 'worst_slew' mode and set the model extraction variable to 'true'. If you want the model to propagate real path specific slew regardless of any context slews propagated from other paths, set the model extraction variable to 'false'. This

makes the model match the netlist better if the timing report of the netlist is performed in 'worst_arrival' slew propagation mode.

MEXT-03 (error) The value '%s' set for the modeling environment variable '%s' is illegal.

DESCRIPTION

You receive this message because the value you set for the specified variable is illegal. If it is for number of table index points, it has to be a positive integer; if it is for the maximum limit of the table index, it has to be a non-negative floating point number.

WHAT NEXT

Adjust the settings of these PrimeTime environment variables before executing model extraction.

MEXT-3 (warning) The %s '%s' timing arc extracted from pin '%s' to pin '%s' has only '%s' tables. They are copied to make the missing '%s' tables.

DESCRIPTION

You received this message because the sequential paths contribute to the specified timing arc only have the specified transition applicable. The resulting timing arc is half-unate. It could be caused by disable timing, false paths or cells with half-unate timing arcs in the path. Because there are tools, such as LibraryCompiler, etc. which do not accept half unate sequential arcs. The extracted model has copied the existing half to create the missing half.

WHAT NEXT

Please verify the path setup and confirm that the arcs are what you expected.

MEXT-4 (warning) Detected max_transition violation in the

circuit to be extracted.

DESCRIPTION

You receive this message if the circuit you are currently extracting has max_transition violations. The resulting model can do max_transition checking only at its boundaries; therefore, the model will be inaccurate because it does not reproduce the errant behavior.

The current problem might be caused by an unrealistically low value of the maximum transition time. Many ASIC libraries supply a **default_max_transition** or a **max_transition** attribute on the gate outputs. If a gate in the design does not have a **max_transition** attribute in its library definition, the **extract_model** command uses the value of the **extract_model_transition_limit** variable; the default is 5.0.

WHAT NEXT

Correct the violations using timing analysis and synthesis on the original circuit, or reset the maximum transition time to a higher value. Then reexecute **extract_model**.

MEXT-5 (warning) Some pins do not have clock defined. One example is pin '%s'. Paths to and from such pins are ignored. Run check_timing for details.

DESCRIPTION

You receive this message because the **extract_model** command did not find a clock for some pins. Transparent latches and flip-flops in a design you want to extract must have a clock defined for them. This message warns you that **extract_model** is ignoring all paths to and from such pins that have no clock.

WHAT NEXT

If it is acceptable to you for **extract_model** to ignore paths to and from such pins, no action is required on your part. Otherwise, use the **create_clock** command to define all design clocks on the pins or clock networks. Then reexecute **extract_model**.

In the future, to prevent receiving this message, first execute the **check_timing** command to detect any clock pins that are missing clocks. Create the missing clocks, then execute **extract_model**.

MEXT-6 (warning) Environment variable '%s' has not been set during this session. Using default value '%s'.

DESCRIPTION

You receive this message if the specified environment variable is not set. This message informs you that the default value is being used.

WHAT NEXT

If it is acceptable to you for the specified default value to be used for this environment variable, no action is required on your part. Otherwise, set this variable to one of its allowed values using the command **set** *variable value*. If you want to set the value only for the current session, you can enter this command at the pt_shell prompt or place it in a script file, which you then execute. If you want the variable value to persist, you can enter it in your .synopsys_pt.setup file.

MEXT-7 (warning) Environment variable 'extract_model_tolerance' has a value that is too low. Using minimum value '%s'.

DESCRIPTION

You receive this message if the **extract_model_tolerance** variable is set with a value less than 0.02. The behavior of the extractor degrades sharply when tolerances are below these values. This message informs you that the specified minimum value is being used instead.

WHAT NEXT

If it is acceptable to you for the **extract_model** command to use the specified minimum value, no action is required on your part. Otherwise, set the **extract_model_tolerance** variable to a value greater than 0.02. Then reexecute **extract_model**.

MEXT-8 (warning) Environment variable 'extract_model_tolerance' has a value that is unreasonably high.

Using maximum value '%s'.

DESCRIPTION

You receive this message if the **extract_model_tolerance** variable is set with a value greater than .50. There is little benefit in extractor speed or output file size beyond 50% tolerance. This message informs you that the specified maximum value is being used instead.

WHAT NEXT

If it is acceptable to you for the **extract_model** command to use the specified maximum value, no action is required on your part. Otherwise, set the **extract_model_tolerance** variable to a value less than 0.50. Then reexecute **extract_model**.

MEXT-10 (error) Unknown format '%s' for the -format option.

DESCRIPTION

You received this message because you executed the **extract_model** command and specified an argument for the **-format** option that was neither *db* or *lib*. These are the only valid arguments for the **-format** option; you can use one or both.

WHAT NEXT

Reexecute **extract_model** and specify one or both of **-format db** or **-format lib**.

MEXT-11 (error) Invalid operating condition '%s' specified.

DESCRIPTION

You receive this message if the operating condition you specified using **extract_model -operating_conditions** cannot be found in any library. The operating condition must exist in some library that is in the **link_path**.

This error could be caused by a spelling error or typo, or by the appropriate library not being in the **link_path**.

WHAT NEXT

First, examine the libraries, design files, and library files listed in the **link_path** variable, to ensure that the intended operating condition appears in one of them. (Use the **report_lib** command to list operating conditions defined in a

single library.) If so, note the correct spelling. If not, add the appropriate library to the **link_path**. Next, reexecute **extract_model -operating_conditions** using the correct operating condition name.

MEXT-12 (warning) Pin '%s' is an internal start or end point. Ignoring paths to and from this pin.

DESCRIPTION

You receive this message if the **extract_model** command finds a pin that is an external start or end point, indicating that the pin is participating in a timing exception or has an input delay specified on it. Because of an extracted model (ETM) limitation, **extract_model** does not support such qualifiers.

WHAT NEXT

Remove all **max_delay**, **min_delay**, and external delays from the pin. Then reexecute **extract_model**.

MEXT-16 (warning) No master clock exists for generated clock '%s'.

DESCRIPTION

You receive this message because the **extract_model** command found a generated clock without a master clock defined.

WHAT NEXT

If it is acceptable to you for **extract_model** to ignore paths to and from the named generated clock, no action is required on your part. Otherwise, use the **report_clock** command to see the source pin that needs a clock defined on it.

MEXT-17 (warning) Zero (or negative) max capacitance on library pin. Assuming %f for library cell %s output %s.

DESCRIPTION

You receive this message if the **extract_model** command finds a 0.0 or negative

maximum capacitance specified on a library cell pin. You cannot have a zero or negative maximum capacitive loading for a library output pin. This message warns you that **extract_model** is assuming the specified value for max capacitance instead.

Many ASIC libraries supply a maximum allowable capacitance on gate outputs. If a gate in the design does not have a **max_capacitance** attribute in its library definition, the **extract_model** command uses the value of the PrimeTime **extract_model_capacitance_limit** variable. The default is 64.

WHAT NEXT

Correct the library to specify a maximum capacitance for all arcs. Or, use the PrimeTime variable **extract_model_capacitance_limit** to set a maximum allowable capacitance for all gate outputs in the design. Then reexecute **extract_model**.

MEXT-19 (information) Clock '%s' has multiple sources.

DESCRIPTION

You receive this message to inform you that the specified clock has multiple sources, potentially causing longer runtime and higher memory use than a clock with a single source. Timing arcs are extracted from all clock sources, so a larger model will result because of an increase in the number of timing arcs.

WHAT NEXT

Consider redeclaring your clocks with a single source pin per clock. For information about the implications of delaring clocks with multiple sources, see the *PrimeTime Modeling User Guide*.

MEXT-20 (warning) Clock '%s' has source on hierachical pin '%s'. Consider moving to: %s

DESCRIPTION

The specified clock has a source on the specified hierarchical pin. This message warns you that PrimeTime might not be able to extract a propagated delay for this clock.

WHAT NEXT

If it is acceptable to you for PrimeTime not to extract a propagated delay for the clock, no action is required on your part. Otherwise, to avoid ambiguity of design

intent, move the clock source back to an output pin of the physical driver circuit, then reexecute **extract_model**. The list of possible driver pins to use are those that drive the net containing the hierarchical pin.

MEXT-21 (error) Cannot compute generated clock propagated delay.
Cannot compute delay from pin '%s'
to hierarchical pin '%s'.

DESCRIPTION

You receive this message if a clock pin has a source specified on a hierarchical pin of a net containing RC data. The model extractor cannot compute the propagated delay to this logical node on the net. This message is related to the MEXT-20 warning message.

WHAT NEXT

Move clock sources back to output pins of the physical clock divider circuit to avoid delays to non-physical pins, then reexecute **extract_model**. Warning MEXT-20 might have been issued previously with a list of driver pins on the net with the hierarchical pin.

MEXT-22 (warning) A path from generated clock '%s' back to its master clock is ignored because its length exceeded %d arcs.

DESCRIPTION

A path from the specified generated clock back to the master clock was found to exceed the specified number of arcs. This message warns you that the path(s) is being ignored. The propagated delay to the generated clock will include only the paths shorter than this length. Thus, the propagated delay might not represent the correct min or max path value.

WHAT NEXT

If it is acceptable to you for the path(s) to be ignored, no action is required on your part. Otherwise, check the design topology for excessively long (false) paths from a master clock to a generated clock, and make changes if necessary. Then reexecute **extract_model**.

MEXT-23 (warning) No net is connected to generated clock '%s' %s pin '%s'.

DESCRIPTION

The specified generated clock has no net connected to either the master clock pin or a clock source pin, as the message indicates. Generated clocks must have net connections even if the clocks are not set to be propagated.

WHAT NEXT

Review the circuit to ensure that all clock specification points are properly connected within the design. Make necessary corrections, then reexecute **extract_model**.

MEXT-24 (error) Internal error found while creating a generated clock.

DESCRIPTION

You receive this message if an internal error is detected during the creation of a generated clock.

WHAT NEXT

Execute the **report_clocks** command on both the original netlist and the extracted model. Verify that the period and edges of the generated clocks in the model match those in the original netlist.

MEXT-28 (warning) More than %d boundary nets have detailed parasitics and multiple drivers or load pins.

DESCRIPTION

This message is issued to limit the number of MEXT-27 messages you receive, and warns you of the total number of boundary nets that have detailed parasitics and multiple drivers or load pins.

Model extraction sometimes combines the RC characteristics of one fanout or fanin with the constraint characteristics of another. This can lead to an inaccurate model.

WHAT NEXT

If possible, buffer the net, then reexecute **extract_model**. Always verify the model if you receive this warning.

MEXT-29 (error) ETM Limitation - Arcs between operating conditions do not match.
No model will be written. The first mismatch is from '%s' to '%s'.

DESCRIPTION

You receive this message if **extract_model** cannot write a model because the arcs between the various operating conditions do not match. For correct DB format, arcs between the different operating conditions of the same model must match exactly.

This error could be caused by a difference in naming of internal nodes, or by the merging of arcs being different between operating conditions.

WHAT NEXT

Write the models for each condition to separate files, or use an interface logic model (ILM) instead of an extracted model (ETM).

MEXT-30 (warning) ETM Limitation - Option '-operating_conditions' is not recommended.
The extracted models may not be able to be combined into one db file.

DESCRIPTION

You receive this message if you issue the **extract_model** command with the **-operating_conditions** option. Using this option is not recommended, because there might be a mismatch between extracted arcs for various operating conditions of the same model. DB format requires that the arcs match exactly between the different operating conditions of the same model. If the arcs do not match, an error message is generated and the model is not written.

Mismatch errors could be caused by a difference in naming of internal nodes, or by the merging of arcs differing between operating conditions.

WHAT NEXT

Write the models for each condition to separate files or use an interface logic model (ILM) instead of an extracted model (ETM).

MEXT-35 (warning) ETM Limitation - -remove_internal_arcs option is not recommended.

DESCRIPTION

You receive this message if you issued the **extract_model** command with the **-remove_internal_arcs** option. This option removes all internal pins from the extracted model without moving the constraints or generated clocks to external pins, and its use is not currently recommended.

WHAT NEXT

Reexecute **extract_model** without the **-remove_internal_arcs** option.

MEXT-36 (warning) A core-cell stamp model will be written. The stamp model must be used with a wrapper design.

DESCRIPTION

The stamp model written without using the **-library_cell** option models only the core of the design being extracted. Boundary nets are modeled in a separate wrapper model. This default behavior was different in previous releases.

WHAT NEXT

If you want a stamp model that includes the boundary nets, rerun the **extract_model** with the **-library_cell** option.

SEE ALSO

extract_model (2).

MEXT-37 (error) extract_model -parasitic_format option has

unknown format '%s'.

DESCRIPTION

The valid formats for the **-parasitic_format** option of the **extract_model** command are **spef**, **dspf**, and **binary**. Any other option is invalid.

WHAT NEXT

Use only the **spef**, **dspf**, and **binary** formats.

SEE ALSO

extract_model (2).

MEXT-38 (error) -parasitic_format cannot be used with the -library_cell option.

DESCRIPTION

The **-parasitic_format** option controls the format for boundary net parasitics. When you use the **-library-cell** option, the boundary nets are included in the model and no parasitics can be written for them.

WHAT NEXT

Remove either the **-parasitic_format** option or the **-library-cell** option, and execute the **extract_model** command again.

SEE ALSO

extract_model (2).

MEXT-40 (warning) ETM Limitation - the -latch_level option is recommended only
when you know the latch-borrowing behavior at the interface. Use -context_borrow

instead.

DESCRIPTION

You receive this message if you execute **extract_model** and use the **-latch_level** option. This option is provided for backward compatibility and is not recommended for general use.

WHAT NEXT

Reexecute the **extract_model** command and use the **-context_borrow** option instead of **-latch_level**.

MEXT-43 (information) When tracing paths from %s '%s', borrowing level-sensitive latches ('%s') were traversed through.

DESCRIPTION

You receive this message to inform you that the tracing for model extraction started from the indicated port/clock has gone through some borrowing level-sensitive latches.

WHAT NEXT

If you observe timing discrepancies, this message might be helpful in debugging.

MEXT-44 (information) Sequential arc '%s' is added only as an '%s' transition. Transition ('%s') is being copied from the existing transition.

DESCRIPTION

You receive this message to inform you that in the process of extracting the named sequential arc, either the rising output or falling output is not a valid path. PrimeTime does not support this type of arc. The invalid transition is being added to the model by giving it the same values as the valid transition.

WHAT NEXT

You can set false paths when using this model to avoid using the invalid transition.

MEXT-45 (warning) ETM Limitation - hold value for -arc_types specified without specifying setup value.
Clock gating hold arcs will not be extracted.

DESCRIPTION

You receive this message because you specified **hold**, but not **setup**, among your values for the **-arc_types** option of the **extract_model** command. Clock gating hold arcs will not be extracted without relevant setup arcs. As a result, your model will not include clock gating hold arcs. All other hold arcs will be extracted.

WHAT NEXT

If you want clock gating hold arcs, reissue the **extract_model** command with the **-arc_types** option specifying both setup and hold values.

SEE ALSO

extract_model (2).

MEXT-46 (error) The requested number of delay table points %d does
not fit into the %3.4f to %3.4f index range that is set on, or derived
for, %s %s.

DESCRIPTION

You receive this message because the requested number of delay table points is so big or the min/max bounds for the table index are so tight that the delay table points cannot be reasonably divided into the requested number of pieces. For SI analysis, the transition set on block input ports is used as the maximum transition table point; if the input transition is zero, then this message will result.

WHAT NEXT

Adjust the settings of the PrimeTime environment variables before executing model extraction. For SI analysis, check the transition value on input ports and increase it to the expected maximum value.

MEXT-47 (error) You must adjust the value of the environment variable '%s' or '%s' before model extraction can proceed. The range is too tight to fit in the requested number of table points.

DESCRIPTION

You receive this message because the requested number of delay table points is so big or the max bound for the table index is so small that it cannot be reasonably divided into the requested number of pieces.

WHAT NEXT

Adjust the settings of these PrimeTime environment variables before executing model extraction.

MEXT-48 (error) You must adjust the value of the environment variable '%s' or '%s' before model extraction can proceed. The product of these two variables %d indicates that the requested size
of delay tables is bigger than 100.

DESCRIPTION

You receive this message because the requested number of delay table points is too big. The size of delay tables in the extracted model is limited to less than 100 (for example, less than a 10 by 10 table).

WHAT NEXT

Adjust the settings of these PrimeTime environment variables before executing model extraction.

MEXT-49 (warning) The model extraction environment variable

%s
is obsolete and has no effect on model extraction.

DESCRIPTION

You received this message because you have set the indicated model extraction environment variable to some value before you execute the model extraction.

If the vairable warned is 'extract_model_transition_limit', start from the PrimeTime 2002.03 release, this variable is obsolete and replaced by two new variables "extract_model_data_transition_limit" and "extract_model_clock_transition_limit".

If the variable warned is 'extract_model_core_cell_stamp', start from PrimeTime 2001.08 release, the behavior has changed and the models will always be the same regardless of output format. The model is totally controlled by the "-library_cell" option of command **extract_model**.

If the variable warned is 'extract_model_min_delay_threshold', start from PrimeTime 2001.08 release, the variable has been obsolete and all minimum delay and hold timing arcs are extracted.

WHAT NEXT

Please remove the settings of the old variable and use the new variables to set up the environment for model extraction if applicable.

MEXT-50 (error) ETM Limitation - The design has multiple clocks on the same source. Clock '%s' defines multiple clocks on source %s.

DESCRIPTION

You receive this message because you defined multiple clocks on the same source, so extraction cannot be performed on that design.

WHAT NEXT

Eliminate the definition of multiple clocks on a single source. Do this by removing all but one clock on the clock source.

SEE ALSO

remove_clock (2).

MEXT-51 (error) ETM Limitation - Path borrowing is not supported for short paths during extraction.

DESCRIPTION

You received this message because you set "timing_allow_short_path_borrowing" variable to TRUE. Path borrowing is not supported for min paths during extraction.

WHAT NEXT

Set the variable "timing_allow_short_path_borrowing" to FALSE.

MEXT-52 (error) ETM Limitation - Timing paths cannot be propagated through unclocked registers during extraction.

DESCRIPTION

You received this message because you set "timing_propagate_through_unclocked_registers" variable to TRUE. Unclocked registers are not supported during extraction.

WHAT NEXT

Set the variable "timing_propagate_through_unclocked_registers" to FALSE.

MEXT-53 (warning) The model generated is a context-dependent w.r.t clock frequency on certain clocks. This is done because certain constraints had to be moved to the closing edge of latch. Example: %s.

DESCRIPTION

You receive this message because the model extraction process found that the design has a specific set of non-borrowing latch arrangements where it was necessary to move the constraint from the opening to the closing edge. Hence, the model arc embodies a half-a-clock-cycle and, so, is not a context-independent w.r.t clock frequency.

WHAT NEXT

If you observe timing discrepancies at a different clock frequency, this message might be helpful in debugging.

MEXT-54 (warning) The model generated is a context-dependent w.r.t clock frequency on certain clocks. This is done because some of the MCP exceptions could not be moved to the boundary. Example: %s.

DESCRIPTION

You receive this message because the model extraction process found that the design has a specific set of multi-cycle path exceptions where it was not possible to move the MCP out to boundary. Hence, the model arc embodies the MCP shift and, so, is not a context-independent w.r.t clock frequency.

This means that the ETM arc has had the current clock period subtracted from the arcs effected by this MCP. When validating the module, use the default slack mode. The option -timing_type arc should not be used for write_interface_timing.

WHAT NEXT

Use write_interface_timing -timing_type slack to validate the model. Do not use write_interface_timing -timing_type arc, or the model arc will differ from the netlist arc, my the MCP adjustment value.

If you observe timing discrepancies at a different clock frequency, create a new ETM for the new clock frequency.

MEXT-55 (warning) The -ignore_ports is obsolete.

DESCRIPTION

You receive this message because you have used the -ignore_ports option. This option will reduce the amount of the design that arcs are extracted for, but may in some cases extract some arcs for the ignored ports.

WHAT NEXT

Use the report_etm_arc command to debug the model.

MEXT-56 (warning) Model cannot create a valid noise table for pin %s.

DESCRIPTION

You received this message because the noise immunity table for one or more noise regions of this pin cannot be created. This can occur either because there’s no noise immunity table defined for the given region or because the effective capacitance loading of the first level cell(s) or the noise width points is far outside the bounds of its library cell characterization. Only one message is output per extract_model command, so other pins may also be missing one or more noise immunity tables in the model.

WHAT NEXT

If there’s no noise immunity table defined for the given noise region, then use set_noise_immunity_curve or set_noise_margin for that region.

If there is a noise immunity table for the given noise region, there are several options: 1. If possible, re-characterize the library to expand the width and capacitance range of the pertinent library cell to include the width/capacitance value used in this design. 2. Use set_load to override the load capacitance of the library cell(s) affecting the pin of interest. 3. Set the variable extract_model_noise_width_points to the same set of widths used for the noise_immunity_table of interest. 4. Use set_noise_immunity_curve or set_noise_margin for the given pin for the problematic region(s).

MEXT-57 (error) The -operating_conditions option can not be used with min_library.

DESCRIPTION

You receive this message because you have used the -operating_conditions option while the -min_library option was used for the set_operating_condition command. The -operating_conditions option to extract_model is obsolete and does not work correctly when the -min_library option to set_operating_condition is used.

WHAT NEXT

Either produce one ETM for bc_wc or on_chip_variation mode, or create one ETM for each desired operating condition by using the set_operating_condition command followed by extract_model.

MEXT-58 (warning) The -operating_conditions option is

obsolete.

DESCRIPTION

You receive this message because you have used the -operating_conditions option. This option is being phased out because it can not support all the functionality of set_operating_condition. Today, it will produce a model for each of the operating conditions listed in single analysis mode. It can not support min_library or multi-voltage options.

WHAT NEXT

Convert your script to call extract_model once for each desired operating condition. Use set_operating_condition and related commands to set the operating conditions between each call to extract_model.

MEXT-59 (warning) The -update option is obsolete.

DESCRIPTION

You receive this message because you have used the -update option. This option is being phased out because support for the scaled cell model it produces is being phased out.

WHAT NEXT

Create separate models for each operating condition.

MEXT-60 (warning) Noise features are not supported for the format '%s'

DESCRIPTION

You received this message because you executed the **extract_model** command and specified an option **-noise** with the **-format** option that included an argument other than *lib*. Noise features are not supported in any format other than *lib*, so only the timing model will be written in those formats.

WHAT NEXT

If the *lib* format was not used, re-execute **extract_model** including the *lib* argument with the **-format** option.

MEXT-61 (warning) Model does not support noise steady state current tables.

DESCRIPTION

You received this message because some cell(s) in the design that reach an output port contain steady state current tables for noise analysis. This feature is not supported yet. Steady-state resistance will be used if it's available either in the cell library or added via user-defined commands.

WHAT NEXT

Either re-characterize the affected cell libraries with steady state resistance or set steady-state resistance via noise commands on the output pins of interest.

MEXT-62 (warning) Model cannot create a valid noise I-V curve for pin %s.

DESCRIPTION

You received this message because the steady-state current table (i.e., I-V curve) for one or more noise regions of this pin cannot be created. This may occur because the voltage bounds or number of points need to be adjusted. Only one message is output per extract_model command, so other pins may also be missing one or more noise steady-state current tables in the model.

WHAT NEXT

Use the extract_model variables for noise I-V tables to adjust the number of points or the range of voltages.

MEXT-63 (warning) No input noise defined on port %s.

DESCRIPTION

You received this message because there was no positive input noise defined on the specified input port. It is assumed that all input ports are set to their worst-case input noise level in order to ensure a conservative noise model. Only one message is output per extract_model command, so other input ports may also have no input noise defined.

WHAT NEXT

Use set_input_noise to define an input noise for the specified port.

MEXT-64 (warning) Conflicting clock sense at model pin: %s

DESCRIPTION

You received this message because a pulse clock sense propagates the model pin in the message, but there is a conflicting clock sense that also propagates to this pin. No pulse_clock attribute was added to the model at this pin.

WHAT NEXT

In using the model add generated clocks to model the different pulse clock generators internal to this model.

MEXT-65 (information) Found logic constant value '%s' at output boundary pin/port '%s' due to propagation of case analysis value.

DESCRIPTION

You receive this message to inform you that model extractor detected the specified logic constant has propagated to the output boundary of the block due to certain case analysis settings for the block.

WHAT NEXT

Some tools treat logic constant values differently depending on the values are caused by user set case analysis or intrinsic functional constant of the circuit. By default, ETM writes out .lib and .db files the resulting logic constants from both cases as 'function' attributes for relevant pins. If this behavior is not desired, you can optionally use variable **extract_model_write_case_values_to_constraint_file** to write the user case analysis caused constant values to the ETM constraint files. Note logic value due to functional constant propagation is always written in the .lib and .db ETM files as "function" attribute for pin.

MGI-1 (information) %s

DESCRIPTION

This is a message that is returned from the generator.

WHAT NEXT

MGI-2 (error) %s

DESCRIPTION

This error represents a generic error condition which occurs during netlist generation.

WHAT NEXT

MGI-3 (warning) %s

DESCRIPTION

This error represents a generic warning which occurs during netlist generation.

WHAT NEXT

MGI-4 (error) Failed to create or open '%s'.

DESCRIPTION

This message indicates a failure to read a file or directory, write a file, execute a file, create a directory, or traverse a directory structure.

WHAT NEXT

MGI-5 (error) Could not execute shell command '%s'.

DESCRIPTION

The generator failed to invoke a shell command.

WHAT NEXT

MGI-6 (error) More than one %s files are found in '%s'.

DESCRIPTION

Only one such file (script, HDL, etc.) should be found in the directory.

WHAT NEXT

MGI-7 (error) No %s file is found in directory '%s'.

DESCRIPTION

At least one of such file (script, HDL, etc.) should be in the directory.

WHAT NEXT

MGI-8 (error) Design '%s' contains %s which is not allowed.

DESCRIPTION

A netlist created by an external generator must not contain any generic logic gates, any sequential cells, any design hierarchy (including both user design hierarchy and synthetic design hierarchy).

WHAT NEXT

MGI-9 (error) Failed to link design '%s' created by '%s'.

DESCRIPTION

The netlist created by the external generator failed to link to the technology libraries in the link path.

WHAT NEXT

MGI-10 (error) File '%s' is not an executable file.

DESCRIPTION

DC expected the file to be executable. This file names a generator that DC attempts to invoke to create netlists.

WHAT NEXT

MGI-11 (error) Unauthorized '%s' file name '%s' is found in directory '%s'.

DESCRIPTION

The generated file containing a netlist in the named directory must match the naming convention.

WHAT NEXT

MGI-12 (error) No dc_shell script is found in directory '%s'.

DESCRIPTION

If the generator sets the "read_script" attribute in its .sl file, there must be a dc_shell script file in the temporary directory.

WHAT NEXT

MGI-13 (warning) Design '%s' contains cells that are not in the target library '%s', these cells will be re-mapped to '%s'.

DESCRIPTION

Generated netlists can be linked using technology libraries specified with the 'set_local_link_library' command in an embedded dc_shell script. Cells linked from a technology library specified in this manner may not have equivalent cells in the target library. These cells will get re-mapped to the target library cells.

WHAT NEXT

MGI-14 (error) Unable to spawn a child process for the generator '%s' specifed within the '%s' synthetic library.

DESCRIPTION

MGI failed to create a process for this generator. The problem can stem from a system-imposed limit on the total number of processes alloted to one user. Alternately, the total amount of system memory available may be insufficient to spawn this process.

WHAT NEXT

MGI-15 (error) Unable to properly subinvoke generator '%s'.

DESCRIPTION

This system error is encountered when spawning a generator. There may be other messages written to the transcript in conjunction with this error message. Please refer to the error messages immediately preceding this message in the transcript for a more detailed diagnostic message.

WHAT NEXT

MGI-16 (error) Incorrect type for argument '%s' is detected in the '%s' command.

DESCRIPTION

This error indicates that a communication error occured during netlist generation.

WHAT NEXT

MGI-17 (warning) Incorrect syntax detected in the '%s' command at '%s'.

DESCRIPTION

This error indicates that a communication error occured during netlist generation.

WHAT NEXT

MGI-18 (error) Unrecognized return status code from generator %s.

DESCRIPTION

Recognized status codes from external generator are either "0" or "1".

WHAT NEXT

MGI-19 (error) %s exited with an error condition. Please see directory

’%s’ for more information.

DESCRIPTION

The child process exited with an error code.

WHAT NEXT

MGI-20 (error) Failed to communicate with generator %s via IPC. See directory ’%s’ for more information.

DESCRIPTION

A datapath generator is still running, but either isn’t responding or is returning undecipherable messages.

Any error messages left by the generator follow this message, preceded with the string "generator:".

WHAT NEXT

Contact the Synopsys Customer Support Center in one of the following ways:

- Open a call to your local support center from the Synopsys Web page at http://www.synopsys.com and click SolvNET (SOLV-IT! user name and password required).

- Send an e-mail message to support_center@synopsys.com.

- Telephone your local support center.

  Call (800) 245-8005 from within the continental United States.
  Call (650) 584-4200 from Canada.
  Find other local support center telephone numbers at http://www.synopsys.com/support/support_ctr.

MGI-21 (error) User interrupted execution of generator %s.

DESCRIPTION

The generator terminated due to a request via a user interrupt.

WHAT NEXT

MGI-22 (error) Generator %s failed to generate %s. Please see directory
'%s' for more information.

DESCRIPTION

The generator returned a failing status after an attempt to generate a netlist. This should be accompanied by other messages giving more information.

WHAT NEXT

Contact the Synopsys Customer Support Center in one of the following ways:

- Open a call to your local support center from the
  Synopsys Web page at http://www.synopsys.com and
  click SolvNET (SOLV-IT! user name and password required).

- Send an e-mail message to support_center@synopsys.com.

- Telephone your local support center.

  Call (800) 245-8005 from within the continental United States.
  Call (650) 584-4200 from Canada.
  Find other local support center telephone numbers at
  http://www.synopsys.com/support/support_ctr.

MGI-23 (error) The '%s' datapath generator has timed out after

%d minutes.

DESCRIPTION

A datapath generator has exceeded the time limit for generating a single netlist and is not responding to messages. The generator process has been terminated.

Any error messages left by the generator follow this message, preceded with the string "generator:".

WHAT NEXT

Contact the Synopsys Customer Support Center in one of the following ways:

- Open a call to your local support center from the Synopsys Web page at http://www.synopsys.com and click SolvNET (SOLV-IT! user name and password required).

- Send an e-mail message to support_center@synopsys.com.

- Telephone your local support center.

  Call (800) 245-8005 from within the continental United States.
  Call (650) 584-4200 from Canada.
  Find other local support center telephone numbers at http://www.synopsys.com/support/support_ctr.

MGI-24 (error) Command string, '%s', exceeds the allowable length ('%d') when communicating with generator from the '%s' synthetic library.

DESCRIPTION

The command string's length exceeds the limit imposed by the interface in server mode.

WHAT NEXT

NAME **MGI-25** (warning) The path '%s' specified by variable

'%s' cannot be found.

DESCRIPTION

The variable **synlib_mc_root** specifies the root directory for an MC installation. When the value of **synlib_mc_root** cannot be matched to a directory on the filesystem Design Compiler assumes Module Compiler to be installed in the default location.

WHAT NEXT

Check the value of the **synlib_mc_root** variable for spelling errors. Check that the directory exists on the filesystem.

NAME **MGI-26** (error) The directory '%s' cannot be created.

DESCRIPTION

A necessary directory could not be created.

WHAT NEXT

Ensure that proper write permissions exist for the directory's parent.

NAME **MGI-27** (warning) The directory '%s' cannot be removed.

DESCRIPTION

DC creates temporary directories during the course of creating generated synthetic parts. This warning indicates an unsuccessful attempt to remove such a temporary directory.

WHAT NEXT

The temporary directory may be manually removed.

NAME **MGI-28** (warning) The library '%s' cannot be written to

'%s'.

DESCRIPTION

The DesignWare generator mechanism was unable to write a temporary copy of a library

to disk. The generator used to create the netlist may fail due to the missing library.

WHAT NEXT

Check that you are able to write to the current directory. Check that free disk space is available in the current directory.

NAME **MGI-29** (error) Invalid Module Compiler installation.

DESCRIPTION

The DesignWare generator mechanism requires Module Compiler for proper operation. DesignWare verifies the Module Compiler environment by checking for the existence of a few Module Compiler files. The missing files are listed after the error message.

WHAT NEXT

Ensure that Module Compiler is properly installed.

MGI-30 (error) %s

DESCRIPTION

This messages reports an error detected by the DesignWare generator environment. It should have been preceeded by other error messages with more specific information.

WHAT NEXT

MGI-31 (error) A datapath generator process has received a fatal (%s) signal %s

DESCRIPTION

A datapath generator process has exited unexpectedly after receiving a fatal signal from the system. The error message identifies the signal, and lists whether or not a "core" file was left in the generator invocation directory.

Any error messages left by the generator follow this message, preceded with the string "generator:".

WHAT NEXT

Contact the Synopsys Customer Support Center in one of the following ways:

- Open a call to your local support center from the Synopsys Web page at http://www.synopsys.com and click SolvNET (SOLV-IT! user name and password required).

- Send an e-mail message to support_center@synopsys.com.

- Telephone your local support center.

  Call (800) 245-8005 from within the continental United States.
  Call (650) 584-4200 from Canada.
  Find other local support center telephone numbers at
  http://www.synopsys.com/support/support_ctr.

MGI-32 (error) A datapath generator process has exited with status code %d %s
This probably means the generator detected an illegal condition and aborted.

DESCRIPTION

This error message occurs when a datapath generator process exits unexpectedly. The exit was probably the result of the datapath generator detecting a fatal error and canceling its run. The error message lists the status code returned from the generator, and whether or not a core file is left in the invocation directory.

Any error messages left by the generator follow this message, preceded with the string *generator:*.

WHAT NEXT

Contact the Synopsys Customer Support Center by sending an email message to support_center@synopsys.com.

MGI-33 (error) A datapath generator process has exited with status code % d %s

This probably means the generator %s and aborted.

DESCRIPTION

This error message occurs when a datapath generator process exits unexpectedly. The exit is probably the result of the datapath generator detecting a fatal error and canceling its run. The error message lists the status code returned from the generator, a description of the fatal error, and whether or not a core file is left in the invocation directory.

Another possible cause of this error message is that the system has run out of resources. If the datapath generator process ran out of disk space or memory, this message occurs.

Any error messages left by the generator follow this message, preceded with the string *generator:*.

WHAT NEXT

Check that you have sufficient disk space and memory.

Contact the Synopsys Customer Support Center by sending an email message to support_center@synopsys.com.

MGI-34 (error) Could not extract parameters of physical wire load mode

DESCRIPTION

This error message occurs when a datapath generator process is about to be started, the wire load mode in use is physically aware but the then necessary parameters could not be extracted.

Without those parameters, the generator would produce sub-optimal results.

WHAT NEXT

Check for warnings and errors a prior set_wire_load_mode physical command reported.

Contact the Synopsys Customer Support Center by sending an email message to support_center@synopsys.com.

MODEL-1 (error) Cannot write the updated model to the db file. The scaled cell model has different ports from the original model saved
in the db file %s.

DESCRIPTION

You receive this message if you execute **extract_model** with the **-update** option, and the ports or timing arcs of the updated model are different from those of the original model. Two models written to the same db file must have exactly the same ports and number and order of arcs; the only difference allowed is in the timing values. This message informs you that **extract_model** did not update the db file with the new information.

Some possible reasons why the two models are different could include these:

• You might have used a slightly different version of the design when performing the update.

• The design might have different false path definitions, which could result in different timing arcs.

• You might have inadvertently used a different design when performing the update.

• You might have used different options (for example, **-library_cell** or **-ignore_ports**) for the original and for the updated model.

WHAT NEXT

Ensure that the original and the updated model have the same timing arcs and ports. Then reexecute **extract_model** with the **-update** option.

SEE ALSO

extract_model (2).

MODEL-2 (error) Port name %s found in %s design is not

found in %s design (operating_condition - %s).

DESCRIPTION

You receive this message if **extract_model** detects a port in the nominal model (that is, at nominal operating condition) that is not in the scaled cell (at a different operating condition). The scaled cell must contain the same ports and arcs as the nominal model.

WHAT NEXT

Ensure that the scaled cell model contains the same ports as the nominal model, then reexecute the command.

SEE ALSO

extract_model (2).

MODEL-3 (warning) A scaled cell for operating condition %s already
exists. Replacing it with the new cell.

DESCRIPTION

You receive this message if **extract_model** finds that a scaled cell is already present for the specified operating condition. This message warns you that the existing scaled cell is being replaced by the new one.

WHAT NEXT

This is a warning message only; no action is required on your part. In the future, before executing this command, save a copy of the *_lib.db file so that you can restore any cells that are unintentionally overwritten.

SEE ALSO

extract_model (2).

MODEL-4 (error) Cannot generate a report; cell %s is not an

interface timing specification (ITS) cell.

DESCRIPTION

You receive this message if **report_model** finds in the design an instantiated cell that is not an interface timing specification (ITS) cell. **report_model** generates reports only for designs that are composed entirely of ITS cells. You create such designs using **extract_model**.

WHAT NEXT

Ensure that your design contains only ITS cells. Then reexecute **report_model**.

SEE ALSO

extract_model (2), **report_model** (2).

MODEL-5 (error) Cannot generate a report; the design %s does not instantiate a PrimeTime model.

DESCRIPTION

You receive this message if **report_model** finds that the design does not instantiate a PrimeTime model. The design might contain more than one cell; a PrimeTime model contains one cell per library. **report_model** generates reports only for PrimeTime designs.

WHAT NEXT

You cannot use **report_model** on this design.

SEE ALSO

report_model (2).

MODEL-6 (Information) Min delay arc from '%s' to '%s' missing for

operating_condition '%s'; substituting with a max_delay arc.

DESCRIPTION

The extractor did not extract the min delay arc between the two points for the operating condition. This min delay arc is present in other operating conditions.

WHAT NEXT

No further action is needed.

MODEL-7 (Error) Cannot open file %s for writing.

DESCRIPTION

You receive this message if the command could not write to the specified file. You might be in a directory where you do not have write permission, or perhaps the file exists and is write-protected.

WHAT NEXT

Either change the permissions on the file or directory so that you can write to it, or use another file and directory for which you have write permission. Then reexecute the command.

SEE ALSO

extract_model (2), **save_qtm_model** (2), **write_interface_timing** (2).

MODEL-8 (information) STAMP %s file %s was successfully compiled.

DESCRIPTION

This is an informational message indicating the STAMP file has been compiled succussfully.

WHAT NEXT

No action is needed.

SEE ALSO

compile_stamp_model (2).

MODEL-9 (Error) You must use the -library_cell option with the -remove_internal_arcs option.

DESCRIPTION

You receive this message if you execute **extract_model** with the **-remove_internal_arcs** option and did not also use the **-library_cell** option. You cannot use **-remove_internal_arcs** without also using **-library_cell**.

WHAT NEXT

Reexecute **extract_model** and use the **-library_cell** option along with the **-remove_internal_arcs** option.

SEE ALSO

extract_model (2).

MODEL-10 (warning) The -test_design option is valid only with the -library_cell option. Ignoring the -test_design option.

DESCRIPTION

You receive this message if you execute **extract_model** and use the **-test_design** option without the **-library_cell** option. The **-test_design** option specifies that a test design instantiating the model lib_cell is to be generated; therefore, **-test_design** is invalid without the **-library_cell** option. This message warns you that the **-test_design** option is being ignored.

WHAT NEXT

If it is acceptable to you that the **-test_design** option is ignored, no action is required on your part. However, if you still want to use the **-test_design** option, reexecute the **extract_model** command and use both the **library_cell** and **-test_design** options.

SEE ALSO

extract_model (2).

MODEL-11 (warning) Cannot update library %s; that library does not exist.

DESCRIPTION

You receive this message if you execute **extract_model** with the **-update** option, but the specified library does not exist. **extract_model** therefore cannot update the library.

WHAT NEXT

If it is acceptable to you that the specified library was not updated, no action is required on your part. Otherwise, do one of the following:

1. Reexecute **extract_model -update** and specify the name of an existing library that is consistent with the current design; or

2. Reexecute **extract_model** without the **-update** option and write a new library.

SEE ALSO

extract_model (2).

MODEL-12 (information) %s.

DESCRIPTION

This is a general purpose modeling related informational message usually issued to indicate the progress or status of the program.

WHAT NEXT

No action is needed.

MODEL-13 (warning) Cannot write generated clock %s to the model because all of the clock's derived sources are on internal pins and the **-remove_internal_arcs** option was

specified.

DESCRIPTION

You receive this message if you execute **extract_model** with the **-remove_internal_arcs** option, but one or more generated clocks have their derived sources on internal pins. This message warns you that if internal arcs are removed, the specified clock cannot be written to the extracted model.

WHAT NEXT

If it is acceptable to you that the specified generated clock is not written to the extracted model, no action is required on your part. However, if you want the generated clock to be written, reexecute **extract_model** and do not use the **-remove_internal_arcs** option.

SEE ALSO

extract_model (2).

MODEL-14 (warning) Cannot write generated clock %s to the model because the clock's master pin is on an internal pin, and the **-remove_internal_arcs** option was specified.

DESCRIPTION

You receive this message if you execute **extract_model** with the **-remove_internal_arcs** option, but the specified generated clock has its master pin on an internal pin. This message warns you that if internal arcs are removed, the specified clock cannot be written to the extracted model.

WHAT NEXT

If it is acceptable to you that the specified generated clock is not written to the extracted model, no action is required on your part. However, if you want the generated clock to be written, reexecute **extract_model** and do not use the **-remove_internal_arcs** option.

SEE ALSO

extract_model (2).

MODEL-16 (warning) The models to be merged have different design names
%s and %s, respectively, use %s."

DESCRIPTION

This is to warn that the design names defined in the models to be merged are not the same.

WHAT NEXT

Please check if the names are actually correct. This is a warning message, the models will still be merged.

MODEL-17 (information) extract_model: %-40s

DESCRIPTION

This message shows the progress of the **extract_model** command. The body of each message reflects a specific aspect of the process.

WHAT NEXT

This is an informational message only; no action is required on your part. However, if you want to suppress the display of these messages, or change the level of messages that are displayed, set the **extract_model_status_level** variable to a different value. Allowed values are none, low, medium, or high.

SEE ALSO

extract_model (2); **extract_model_status_level** (3).

MODEL-18 (error) Found different values defined for attribute '%s', %s and %s in the models, cannot merge them.

DESCRIPTION

This is an error indicating that the named attribute defined for the models to be merged are not the same. Model merging cannot proceed with this difference.

WHAT NEXT

Please make sure that the named attribute is defined to have the same values across all the models to be merged.

MODEL-19 (error) The %s defined in the models are different.

DESCRIPTION

This is a general error indicating that the named object(s) defined in the models to be merged are not the same. Model merging cannot proceed with the difference.

WHAT NEXT

Please make sure that the named object(s) are defined the same across all the models to be merged.

MODEL-20 (error) Found %s '%s' in the models defined with different %s, cannot merge them.

DESCRIPTION

This is a general error indicating that the named object(s) defined in the models are not the same. Model merging cannot proceed with the difference.

WHAT NEXT

Please make sure that the named object(s) are defined the same across all the models to be merged.

MODEL-21 (error) %s '%s' is not defined in all models, cannot merge.

DESCRIPTION

This is a general error indicating that the named object is not defined in all the models. Model merging cannot proceed with the difference.

WHAT NEXT

Please make sure that the named object is defined across all the models to be merged.

MODEL-22 (error) The port/pin number %d is different in the models. They are defined as %s and %s, respectively.

DESCRIPTION

This is an error message indicating that the port/pin defined at the specified position in the models are not the same. Model merging cannot proceed with the difference.

WHAT NEXT

Please make sure that the order of pins of direction INPUT/OUTPUT/INOUT/TRIOUT are are defined the same across all the models to be merged. INTERNAL pin order is not important.

MODEL-23 (error) Cannot merge %s '%s' with different '%s' %s and %s in the models.

DESCRIPTION

This is an error indicating that the named attribute defined for the named object are not the same. Model merging cannot proceed with this difference.

WHAT NEXT

Please make sure that the named attribute is defined to have the same values across all the models for the named object.

MODEL-24 (warning) Found %s '%s' with different '%s'

%s and %s in the models, use %s.

DESCRIPTION

This is a warning indicating that the named attribute defined for the named object are not the same. Model merging will use the value specified.

WHAT NEXT

Please check if the named attribute should have the same values for the named object.

MODEL-25 (error) The bit number %d in bus %s is different in the models.
They are defined as %s and %s, respectively.

DESCRIPTION

This is an error message indicating that the specified bit of the bus in the models are not the same. Model merging cannot proceed with the difference.

WHAT NEXT

Please make sure that the bits and the order of bits are the same in the bus across all models to be merged.

MODEL-26 (information) Found unique internal pin '%' in one of the models,
copied into the merged model.

DESCRIPTION

This is an informational message.

WHAT NEXT

No action required.

MODEL-27 (error) %s.

DESCRIPTION

This is a general purpose modeling related error message usually issued to indicate the reason why model merging cannot proceed.

WHAT NEXT

Please invetigate the models to be merged and fix the identified problems and try merge them again.

MODEL-28 (warning) Found %s '%s' with conflict '%s' '%s' and '%s' set in the models, no constant is set for it in the merged model.

DESCRIPTION

This is a warning indicating that the named attribute defined for the named object are not the same. Model merging will use the value specified.

WHAT NEXT

Please check if the named attribute should have the same values for the named object.

MODEL-29 (warning) The %s command will be discontinued in future releases. Changes to model validation has made this command unecessary

DESCRIPTION

A command has been rendered unnecessary by changes to model validation commands. The old command is being supported temporarily but will cause syntax errors in future releases

WHAT NEXT

Use the new functionality instead of the discontinued command.

SEE ALSO

MODEL-30 (error) Cannot merge models because no model files were specified

DESCRIPTION

You receive this message if you execute **merge_models** without specifying model files through either the -model_files or -lib_files option.

WHAT NEXT

Add model files to the command using either the **-model_files** or **-lib_files** option.

SEE ALSO

merge_models (2).

MODEL-31 (error) Cannot merge models because no data files were specified

DESCRIPTION

You receive this message if you execute **merge_models** without specifying any data files in conjunction with the **-model_files** optoin. The **merge_models** command requires data files when **-model_files** is present.

WHAT NEXT

Add data files to the command using the **-data_files** option.

SEE ALSO

merge_models (2).

MODEL-32 (error) Cannot merge models because no mode

names were specified

DESCRIPTION

You receive this message if you execute **merge_models** without specifying any mode names. The **merge_models** command requires one mode name for each input file.

WHAT NEXT

Add mode names to the command using the **-mode_names** option.

SEE ALSO

merge_models (2).

MODEL-33 (error) Cannot merge models because the number of model files does not match the number of data files.

DESCRIPTION

The **merge_models** command requires the number of model and data files match. One model and data file combine to define a model in STAMP format, so **merge_models** requires a one for one correspondance.

WHAT NEXT

Adjust the **-data_files** or **-model_files** as needed so the list lengths match.

SEE ALSO

merge_models (2).

MODEL-34 (error) Cannot merge models because the number of mode names does not match the number of model files.

DESCRIPTION

The **merge_models** command requires the number of mode names to match the number of model files. The model files are specified with either the **-model_files** or **-lib_files** option. A combination of model file and mode name defines a model to merge, so the number in each list must match.

WHAT NEXT

Adjust the mode names or the number of models so that the list lengths match.

SEE ALSO

merge_models (2).

MODEL-35 (error) Cannot merge models because there are duplicate mode names

DESCRIPTION

The **merge_models** command requires that the mode names be unique. There cannot be any duplicates.

WHAT NEXT

Change the duplicate mode names to be unique.

SEE ALSO

merge_models (2).

MODEL-36 (error) Cannot merge models because of an empty %s list

DESCRIPTION

A list for **merge_models** is empty. All lists must have at least one element in them.

WHAT NEXT

Add elements to the list, or remove the option for the list from the command line.

SEE ALSO

merge_models (2).

MODEL-37 (error) Cannot use %s in conjunction with %s

DESCRIPTION

You cannot specify both of these options for **merge_models** at the same time.

WHAT NEXT

Remove one or both of these options from the command.

SEE ALSO

merge_models (2).

MODEL-38 (error) Cannot merge models because there are data files with no model files.

DESCRIPTION

The **merge_models** command cannot have **-data_files** without corresponding **-model_files**.

WHAT NEXT

Either add **-model_files** to merge STAMP files, or remove the **-data_files** to merge LIB files.

SEE ALSO

merge_models (2).

MODEL-39 (error) Library file was not extracted.

DESCRIPTION

When the **merge_models** command read in one of the files in the **-lib_files** list of library files, it did not see at least one required attribute. Each of the library files must be the result of the **extract_models** command.

WHAT NEXT

Ensure that all of the library files are the output of the **extract_model** command.

SEE ALSO

merge_models (2). **extract_model** (2).

MODEL-40 (error) Library file is invalid for merging.

DESCRIPTION

When the **merge_models** command read in one of the files in the **-lib_files** list of library files, it found that one of the libraries was missing some expected attributes, had inconsistant attributes, or had unexpected attributes. Each of the library files must be the result of the **extract_models** command.

WHAT NEXT

Ensure that all of the library files are the output of the **extract_model** command.

SEE ALSO

merge_models (2). **extract_model** (2).

MODEL-41 (error) The %s and %s arguments are mutually exclusive

DESCRIPTION

The **merge_models** command cannot be invoked with both of the arguments at the same time, only one is allowed.

WHAT NEXT

Remove one of the arguments and invoke the command again.

MOUI

MOUI-1 (error) Could not create menu item: ’%s’.

DESCRIPTION

WHAT NEXT

MOUI-2 (error) Widget name conflict: %s.

DESCRIPTION

WHAT NEXT

MOUI-3 (error) Dialog %s is not posted.

DESCRIPTION

WHAT NEXT

MOUI-4 (error) Could not read bitmap file: ’%s’.

DESCRIPTION

WHAT NEXT

MOUI-5 (fatal) Could not create the designs view.

Your generic symbol library may be old or non-existent.

DESCRIPTION

WHAT NEXT

MOUI-6 (error) Could not create viewer log file: ’%s’.

DESCRIPTION

WHAT NEXT

MOUI-7 (error) Minimum rise time must not be greater that maximum rise time.

DESCRIPTION

WHAT NEXT

MOUI-8 (error) Minimum fall time must not be greater that

maximum fall time.

DESCRIPTION

WHAT NEXT

MOUI-9 (error) Unable to push into design %s

DESCRIPTION

WHAT NEXT

MOUI-10 (error) Unable to open file: %s

DESCRIPTION

WHAT NEXT

MOUI-11 (error) '%s': is a file. Choose a directory name.

DESCRIPTION

WHAT NEXT

MOUI-12 (error) '%s': No write permission. Choose another

directory.

DESCRIPTION

WHAT NEXT

MOUI-13 (error) Please specify an output file name.

DESCRIPTION

WHAT NEXT

MOUI-14 (error) Background '%s' task '%s' has exited abnormally.

DESCRIPTION

WHAT NEXT

MOUI-15 (error) You cannot execute '%s' because it is the

current view_log_file.

DESCRIPTION

WHAT NEXT

MOUI-16 (error) No design has been selected to plot.

DESCRIPTION

WHAT NEXT

MOUI-17 (error) Can’t plot design ’%s’ because the schematic could not be created.

DESCRIPTION

WHAT NEXT

MOUI-18 (error) No plot file specified.

DESCRIPTION

WHAT NEXT

MOUI-19 (error) Specified selecting color ’%s’ is not a valid

color.

DESCRIPTION

WHAT NEXT

MOUI-20 (error) Only schematics can be plotted.

DESCRIPTION

WHAT NEXT

MOUI-21 (error) Additional errors suppressed. See the Command Window for a full error message listing.

DESCRIPTION

WHAT NEXT

MOUI-22 (warning) Unable to execute watcher process: ’%s’.

DESCRIPTION

The watcher process is a child process of the Design Analyzer that watches for user interrupts during drawing and selection. If the DA cannot execute this process, the user will not be able to interrupt drawing and selection, but this is not a FATAL error. The most likely cause of this message is that the software has not been installed properly. The DA expects the watcher process to be in the synopsys bin directory.

WHAT NEXT

If there is some reason why you cannot install the software in the normal manner, you can disable this message by putting the statement *view_watcher = ""* in one of the .synopsys setup files.

MOUI-23 (error) HDL library ’%s’ does not exist. Click on "Create New Library if it Doesn’t Exist" in the "Analyze File" dialog to override this error

DESCRIPTION

You have named a non-existent HDL library in the Analyze File dialog box.

WHAT NEXT

Click on "Create New Library if it Doesn’t Exist" in the "Analyze File" dialog box to override this error.

MOUI-24 (error) Command %s requires at least one selected object.

DESCRIPTION

WHAT NEXT

MOUI-25 (information) Multi-lined command flushed.

DESCRIPTION

While entering a multilined command at the command line in the cmdtool window, you hit Ctrl-C, and the lines in progress were flushed from the buffer.

WHAT NEXT

You probably typed Ctrl-C because you noticed an error on a previously entered line, or you no longer wished to enter this command sequence. Reenter the command (cutting and pasting with the mouse is useful here), or enter another command.

MOUI-26 (error) Command incomplete. Command ignored.

DESCRIPTION

Because the Design Analyzer cannot execute an incomplete command, the command was

ignored. Either you improperly entered a user submenu item (through the *view_script_submenu_items* variable) or you used a user alias that redefined a **dc_shell** command.

WHAT NEXT

If you entered the command from a user submenu (on the Setup->Scripts submenu), check the variable setting to see if it was a complete **dc_shell** command. The variable setting is in one of the *.synopsys_dc.setup* files in either the <Synopsys_Root>/admin/setup directory, your home directory, or the local directory.

If the command was automatically generated from the Design Analyzer, check to see if the command was aliased to an incomplete **dc_shell** command. This information is also in one of the *.synopsys_dc.setup files*.

You can quickly see the result of all *.synopsys_dc.setup* settings in the *command.log* file generated by Design Analyzer.

An incomplete command is usually an **if**, **while**, or **foreach** command that was not terminated with its closing "}".

MOUI-27 (error) Can’t invoke Design Analyzer because the value of
the %s variable contains options
which are ambiguous. Please fix the value of this variable in your initialization file and re-invoke Design Analyzer.
To see the valid options to create_schematic, use

the help command in dc_shell.

DESCRIPTION

WHAT NEXT

MOUI-28 (error) Unable to Highlight Selected object(s).

DESCRIPTION

WHAT NEXT

MOUI-29 (warning) Ignoring the value of the variable default_schematic_options
because it is incorrect. Type ’help create_schematic’ in the Command Window or ’create_schematic’ in the Help->Commands
dialog box for a description of the options to the

create_schematic command.

DESCRIPTION

WHAT NEXT

MOUI-30 (error) String required for the option(s) : %s.

DESCRIPTION

WHAT NEXT

MOUI-31 (error) Invalid instance name: '%s'.

DESCRIPTION

The instance name is invalid because it contains a backslash (\).

WHAT NEXT

Remove the backslash from the instance name and try again.

MOUI-32 (warning) '%s' does not have a schematic object.

DESCRIPTION

This given object does not have a schematic object to be viewed or selected.

WHAT NEXT

MOUI-33 (error) The pattern %s to define the From-%s of the

paths does not match any instance.

DESCRIPTION

The tool issues this error when a pattern is given to define From-instances but no instance matches this pattern.

WHAT NEXT

Check the pattern for spelling errors or remove the entire pattern to allow paths to start at any start point.

MOUI-34 (error) The pattern %s to define the Through-%s of the paths does not match any instance.

DESCRIPTION

The tool issues this error when a pattern is given to define Through-instances but no instance matches this pattern.

WHAT NEXT

Check the pattern for spelling errors or remove the entire pattern to allow paths to start at any start point.

MOUI-35 (error) The pattern %s to define the To-%s of the paths does not match any instance.

DESCRIPTION

The tool issues this error when a pattern is given to define To-instances but no instance matches this pattern.

WHAT NEXT

Check the pattern for spelling errors or remove the entire pattern to allow paths to start at any start point.

MPC-001 (warning) This command will be obsolete in a future release. Please use %s.

DESCRIPTION

You receive this warning message because you are using an obsoleting command. We are changing some older MPC command names. FROM TO set_floorplan_options set_mpc_options set_floorplan_port_options set_mpc_port_options set_floorplan_macro_optionsset_mpc_macro_options set_floorplan_macro_array set_mpc_macro_array set_floorplan_pnet_optionsset_mpc_pnet_options report_floorplan_options report_mpc_options report_floorplan_port_options report_mpc_port_options report_floorplan_macro_optionsreport_mpc_macro_options report_floorplan_macro_arrayreport_mpc_macro_array report_floorplan_pnet_options report_mpc_pnet_options

WHAT NEXT

Please update your script to use new command names.

SEE ALSO

set_mpc_options (2), **report_mpc_options** (2), **set_mpc_port_options** (2), **report_mpc_port_options** (2), **set_mpc_macro_options** (2), **report_mpc_macro_options** (2), **set_mpc_macro_array** (2), **report_mpc_macro_array** (2), **set_mpc_pnet_options** (2), **report_mpc_pnet_options** (2).

MPC-002 (Error) Failed to find valid base core site.

DESCRIPTION

The tool is looking at physical library for the site(s) to be instantiated in site array. A base core site is the site which is core type and is having minimum height and width, and is used by cells in current design. If such a site can not be identified, the tool errors out.

WHAT NEXT

Please check your physical library. Usually this error is caused by error in physical library. The site used by design is not defined in library.

SEE ALSO

set_mpc_options (2), **report_mpc_options** (2)

MPC-003 (Warning) Output file is not defined for derive-mpc. Derived constraints will be directly annotated on design objects.

DESCRIPTION

Commands derive_mpc_options, derive_mpc_port_options and derive_mpc_macro_options, all have -output option for you to specify output file name. The tool will write the derived constraints to the file. These commands also take a -apply options. If -apply is specified, the tool will directly annotate the derived constraints on design objects. Both -output and -apply are optional. You can specify both of them or one of them. If both of them are not specified, the tool will imply -apply and issue this warning message.

WHAT NEXT

You don’t have to do anything if your intention is to apply the derived constraints to the design objects.

SEE ALSO

derive_mpc_options (2), **derive_mpc_port_options** (2), **derive_mpc_macro_options** (2)

MPC-004 (warning) The %s %s is having FIXED location at (%f %f). initialize_mpc can’t move it.

DESCRIPTION

You receive this warning message because the cell or port is marked as fixed. initialize_mpc will not change the location for it. If the core area is changed, the location might be valid any more.

WHAT NEXT

If your intension is to keep it at the fixed location, you can ignore this warning message. If you want the location to be reset by the tool, you have to remove fixed placement by using remove_dont_touch_placement command.

SEE ALSO

set_mpc_options (2), **report_mpc_options** (2), **set_dont_touch_placement** (2), **remove_dont_touch_placement** (2),

MPC-005 (warning) No Track is empty on %s, port %s is set to (%d %d).

DESCRIPTION

You receive this warning message because MPC is unable to find an empty track to place the port on the side in create_placement -mpc and physopt -mpc flows.

WHAT NEXT

This is happening as no tracks are available on this side, constraint the port to a different side. You can also limit the number of ports on this side.

SEE ALSO

set_mpc_options (2), **set_mpc_port_options** (2)

MPC-006 (warning) Port Group '%s' too large to fit in core.

DESCRIPTION

You receive this warning message because the port group is too large to fit in the core area specified by mpc in the physopt -mpc and create_placement -mpc flows.

The tool will honor the side constraints on these ports.

WHAT NEXT

Try to reduce the number of ports in the port group. Pitch specified for this port group might also cause the port group to be too large.

SEE ALSO

set_mpc_options (2), **set_mpc_port_options** (2)

MPC-007 (Warning) Minimum site %s in physical library is

different from the minimum site %s used in design. Choose site %s as base site.

DESCRIPTION

The minimum site defined in physical library is not used in the design. Instead a bigger site is used. By default, the minimum site used in design is chosen as the base site.

MPC-008 (Warning) No site is used in design. Minimum site %s from library is used as base site.

DESCRIPTION

The minimum site in the library is chosen as base site. There is no cell in the design that uses sites defined in the library. This can happen if there is no standard cell in the design. Or the sites for standard cells are not defined in library. In this case, please check whether your library is valid.

MTCMOS

MTCMOS-1 (error) Cannot open library %s.

DESCRIPTION

This error message occurs when the specified library is not found.

WHAT NEXT

Option -lib of commands report_IV_table and get_switch_resistance need to be specified as a library name. Make sure the library has been opened before run these commands. Correct this error as following: 1) Use the get_libs command to verify the libraries has been opened currently. 2) If not opened, to open the library, if you will re-run the whole process before the current command, try to put the expected library's .db file in the tcl variable link_library before execute the link command. Re-run the whole process and run the command again. 3) Make sure the library is opened and run the command again.

SEE ALSO

get_libs(2)

MTCMOS-2 (error) Library %s has no cell named %s.

DESCRIPTION

This error message occurs when the specified cell is not found in library.

WHAT NEXT

Option -cell of commands report_IV_table and get_switch_resistance need to be specified as a cell name. Make sure the cell exist in the library. Use the report_lib command to report the info of the lib. Verify the cell list section of the library to check if the specified cell exist in the list. Run the command again by pass in the correct cell name.

SEE ALSO

report_lib(2)

MTCMOS-3 (error) Check number of output_voltage: at least

%d values is needed, but only %d values in %scell %s of lib %s.

DESCRIPTION

This error message occurs when the number of output_voltage less than required value. See the detail as following: 1) At least 3 values for output_voltage is needed to shape an IV(ISD-VVPG) curve. 2) If voltage level of related_pg_pin not equals anyone value in the list of VVPG(voltage on virtual power or ground), it means this value has been omitted in the list, then the least number is 2.

WHAT NEXT

To fix this error, please contact the library provider to correct this issue in library.

MTCMOS-4 (warning) Check monotonicity of output_voltage: VVPGs should monotonically rise, but drop from %f to %f in %scell %s of lib %s.

DESCRIPTION

This warning message occurs when the output_voltage not monotonically rise. The output_voltage is assumed monotonically rise to assure there is no "dirty data" in the IV curve table.

WHAT NEXT

To fix this error, please contact the library provider to correct this issue in library.

MTCMOS-5 (error) Check number of input_voltage: at least 2 values is needed, but only %d values in %scell %s of lib %s.

DESCRIPTION

This error message occurs when the number of input_voltage less than required value. At least 2 values for input_voltage is needed to determine whether rise or fall turns on the switch.

WHAT NEXT

To fix this error, please contact the library provider to correct this issue in library.

MTCMOS-6 (warning) Check monotonicity of input_voltage: VENs should monotonically rise, but drop from %f to %f in %scell %s of lib %s.

DESCRIPTION

This warning message occurs when the input_voltage not monotonically rise. The input_voltage is assumed monotonically rise to assure there is no "dirty data" in the IV curve table.

WHAT NEXT

This is only a warning message. To eliminate this warning message, please contact the library provider to correct this issue in library.

MTCMOS-7 (error) Check number of ISD: numOfISD %d not equal numOfVVPG %d multiply numOfVEN %d in %scell %s of lib %s.

DESCRIPTION

This error message occurs when the number of numOfISD not equal (numOfVVPG*numOfVEN).

WHAT NEXT

To fix this error, please contact the library provider to correct this issue in library.

MTCMOS-8 (error) Check direction of ISD: ISDs should not all

be zero in %scell %s of lib %s.

DESCRIPTION

This error message occurs when the all value of ISDs are zero.

WHAT NEXT

To fix this error, please contact the library provider to correct this issue in library.

MTCMOS-9 (error) Check direction of ISD: %s%s cell %s of lib %s has too much false direction %s ISDs.

DESCRIPTION

This error message occurs when the specified cell has over 25% of false direction ISDs. For header, negative ISD is invalid. For footer, positive ISD is invalid.

WHAT NEXT

To fix this error, please contact the library provider to correct this issue in library.

MTCMOS-10 (warning) Check direction of ISD: %s%s cell %s of lib %s has false direction %s ISDs.

DESCRIPTION

This error message occurs when the specified cell has false direction ISD. For header, negative ISD is invalid. For footer, positive ISD is invalid.

WHAT NEXT

This is only a warning message. To eliminate this warning message, please contact the library provider to correct this issue in library.

MTCMOS-11 (error) Check ISD-VVPG monotonicity: IV curve table for %scell %s in lib %s should not has wholly rise ISD-

VVPG monotonicity.

DESCRIPTION

This error message occurs when the IV curve table has false wholly drop ISD-VVPG monotonicity. See the detail as following: 1) A drop ISD-VVPG point means for the same VEN, the ISD drop as VVPG rise at the point. A rise ISD-VVPG point means for the same VEN, the ISD rise as VVPG rise at the point. 2) When the number of drop ISD-VVPG point is greater than the number of rise ISD-VVPG points in the IV curve table, the IV table has wholly drop ISD-VVPG monotonicity. Otherwise, it has wholly rise ISD-VVPG monotonicity. 3) The IV curve table should has wholly drop ISD-VVPG monotonicity.

WHAT NEXT

To fix this error, please contact the library provider to correct this issue in library.

MTCMOS-12 (warning) Check ISD-VVPG monotonicity: ISD of the ISD-VVPG curve for %s%s cell %s in lib %s should not rise as VVPG rise.

DESCRIPTION

This warning message occurs when the ISD of the ISD-VVPG curve is not drop as VVPG rise. For the same VEN, ISD should always drop as VVPG rise.

WHAT NEXT

This is only a warning message. To eliminate this warning message, please contact the library provider to correct this issue in library.

MTCMOS-14 (warning) Check ISD-VEN monotonicity: ISD of the ISD-VEN curve for %s%s cell %s in lib %s maybe should not %s as VEN rise.

DESCRIPTION

This warning message occurs when the ISD of the ISD-VEN curve not abide by its commonly correct monotonicity. The commonly monotonicity law for ISD-VEN are as following: 1) If Ven is swept from the pin before the internal inverter, the ISD of

the ISD-VEN curve at the same VVPG should rise as VEN rise. 2) Otherwise, the ISD of the ISD-VEN curve at the same VVPG should drop as VEN rise.

Sometimes this warning message maybe not a problem. For example, to a non-internal-inverter case, when the Ven is much higher than library testing Vdd, the montonicity will be reverse as Ven continue rise.

WHAT NEXT

This is only a warning message. To eliminate this warning message, please contact the library provider to correct this issue in library.

MTCMOS-15 (error) IV curve has questionable zero Isd when VVPG %4.2f not equal vlotage value %4.2f on related_pg_pin of %scell %s in library %s.

DESCRIPTION

This error message occurs when the ISD equal to zero while VVPG not equal to the voltage level of related_pg_pin defined in library. When VVPG not equal to the voltage level of related_pg_pin, the voltage Vds will not equal to zero, then the current flow through the cell will not equal to zero too.

WHAT NEXT

To fix this error, please contact the library provider to correct this issue in library.

MTCMOS-16 (error) Working VDD is %4.2f, its corresponding Ven %4.2f is out of range of IV curve table for %scell %s of library %s.

DESCRIPTION

This error message occurs when the value of working VDD out of range of IV curve table. It may occurs at following circumstance: 1) The value of working VDD out specified by -vdd option of command get_switch_resistance is out of range of IV curve talbe. 2) When do PNA/PNS, the working VDD retrieved from design is out of range of IV curve talbe.

WHAT NEXT

This is only a warning message. To eliminate this warning message, follow the instructions below: 1) The value of the working VDD and the value of corresponding VEN has been report in this error message. 2) Contact the library provider to ask if the value of corresponding VEN of the working VDD is out of range of VENs in IV curve table. 3) If not, maybe the value of working VDD is not correct, change the value and run the command again. 4) It could also because the VENs range in the IV curve table is not wide enough. Please raise the problem to the library provider to ask for an updated .db file or .lib file with wider range of VEN.

MTCMOS-17 (error) No dc_current data for cell %s in library %s.

DESCRIPTION

This error message occurs when there is no IV curve table data for the specified cell of the specified library.

WHAT NEXT

Please contact the library provider to correct this libraray error.

MTCMOS-18 (error) No template is defined for LUT in library %s.

DESCRIPTION

This error message occurs when there is no template is defined for LUT in the specified library.

WHAT NEXT

Please contact the library provider to correct this libraray error.

MTCMOS-19 (error) Failed to read values from dc_current section of library %s.

DESCRIPTION

This error message occurs when there is something wrong in the values of dc_current section of the specified library.

WHAT NEXT

Please contact the library provider to correct this libraray error.

MTCMOS-20 (error) Failed to get voltage value of related_pg_pin for %scell %s in library %s.

DESCRIPTION

This error message occurs when failed to get voltage value of related_pg_pin.

WHAT NEXT

Please contact the library provider to correct this libraray error.

MTCMOS-21 (error) Type of related_pg_pin is not correct for %scell %s in library %s.

DESCRIPTION

This error message occurs when the type of related_pg_pin is not power or ground type.

WHAT NEXT

Please contact the library provider to correct this libraray error.

MTCMOS-22 (error) Failed to get related_switch_pin of dc_current for %scell %s in library %s.

DESCRIPTION

This error message occurs when failed to get related_switch_pin of IV curve talbe in dc_current section in the library.

WHAT NEXT

Please contact the library provider to correct this libraray error.

MTCMOS-23 (error) Failed to get the primary power of related_switch_pin for %scell %s in library %s.

DESCRIPTION

This error message occurs when failed to get the primary power of related_switch_pin.

WHAT NEXT

Please contact the library provider to correct this libraray error.

MTCMOS-24 (error) Specified value %s for option -lib_cell is not a power switch name or a lib cell name.

DESCRIPTION

This warning message occurs when your specified value for -lib_cell is not a correct power switch name or lib cell name.

WHAT NEXT

Please put in correct power switch name as value of option -lib_cell when UPF mode.
Or put in correct lib cell name as value of option -lib_cell when None-UPF mode.

SEE ALSO

create_power_switch_array (2),
create_power_switch_ring (2),
create_power_switch (2),
map_power_switch (2),
derive_pg_connection (2),

MTCMOS-25 (Warning) Command ’%s’ is obsolete. Please use ’%s’ instead.

DESCRIPTION

This warning message occurs when you use a certain command which is obsolete and will be removed in later release.

WHAT NEXT

Please use the new command proponed in the warning message.

MTCMOS-26 (Warning) Option '%s' is obsolete. Please use '%s' instead.

DESCRIPTION

This warning message occurs when you use a certain option which is obsolete and will be removed in later release.

WHAT NEXT

Please use the new option proponed in the warning message.

MTCMOS-27 (Warning) Can not find power switch %s, it might be a lib cell name.

DESCRIPTION

This warning message occurs when you use a lib cell name under UPF mode or it is not a correct power switch name.

WHAT NEXT

Please use correct power switch name under UPF mode. If you are using lib cell name under UPF mode, power switches can also be placed, but PG pin connection can not be correctly derived by derive_pg_connection command. You may need to connect them manually.

SEE ALSO

create_power_switch_array (2),
create_power_switch_ring (2),
create_power_switch (2),
map_power_switch (2),
derive_pg_connection (2),

MTCMOS-28 (Warning) Some grid points are blocked.

DESCRIPTION

This warning message occurs when some grid points are blocked by existing power switch cells, other voltage areas (guardband), placement blockages, hard macros, or fixed cells.

WHAT NEXT

By default, the command create_power_switch_array will only honor existing power switch cells and voltage areas. -respect option can allow user to specify the combination of following choices: hard_blockage, soft_blockage, blockage, macro, fixed_cells, and all. The command will honor these objects specified in -respect option and not insert the power switches if these objects could block them. Please also note, the command also honors other voltage area's guardband. If user wants to allow power switches inserted in the guardband, there is a variable to control it. Please use "set ignore_guardband TRUE" before running create_power_switch_array command.

SEE ALSO

create_power_switch_array (2),
ignore_guardband (5),

MTCMOS-29 (Warning) x_increment is not more than 0. The value is adjusted to the width of bounding box or voltage area.

DESCRIPTION

This warning message occurs when the specified x_increment is not more than 0. The value is adjusted to the width of bounding box or voltage area. But for disjoint voltage area, it may cause problem.

WHAT NEXT

Please specify a value which is larger than 0.

SEE ALSO

create_power_switch_array (2),

MTCMOS-30 (Warning) x_increment is not more than 0. The

value is adjusted to the height of switch cell.

DESCRIPTION

This warning message occurs when the specified x_increment is not more than 0. The value is adjusted to the height of switch cell.

WHAT NEXT

Please specify a value which is larger than 0.

SEE ALSO

create_power_switch_array (2),

MTCMOS-31 (ERROR) Illegal input for -bounding_box option.

DESCRIPTION

This error message occurs when the specified -bounding_box option is illegal. The format should be {left bottom right top} and the right should be larger than left and top should be larger than bottom.

WHAT NEXT

Please specify the -bounding_box option in a correct format.

SEE ALSO

create_power_switch_array (2),

MTCMOS-32 (ERROR) There is no intersection of given bounding box and voltage_area, cells can not be inserted.

DESCRIPTION

This warning message occurs when both -voltage_area and -bounding_box are specified, power switches will be added to the intersecting region of the given bounding box and voltage area. Now there is no intersection of given bounding box and voltage area, so no cells can be inserted.

WHAT NEXT

If power switches are supposed to be inserted inside the voltage area, please specify the bounding box within the voltage area. If power switches are supposed to be inserted outside of the voltage area, please don’t specify the -voltage_area option. The power switches will be inserted at default_va.

SEE ALSO

create_power_switch_array (2),

MTCMOS-33 (Warning) Can not fit the cell into row correctly! Check the cell and cell row!

DESCRIPTION

This warning message occurs when option -snap_to_row_and_tile is specified, but cell can not be put into the cell row. Please also check if the row_core_ratio is not 1. The -snap_to_row_and_tile option is ignored.

WHAT NEXT

Please check the cell size and cell row size.

SEE ALSO

create_power_switch_array (2),

MUTIL-1 (fatal) Could not create menu item '%s'.

DESCRIPTION

WHAT NEXT

MUTIL-2 (fatal) More than one menu item has the name '%s'.

DESCRIPTION

WHAT NEXT

MUTIL-3 (fatal) Could not open menu files.

DESCRIPTION

This error occurs if the menu files don't exist or the protection is not set correctly. The menu files are in the <synopsys_root>/<arch>/motif/syn/uid directory.

For example, design analyzer exits with these messages:

Could not open one or more of the following menu files: /remote/rd40/src/dc/uil/mview.uid /remote/rd40/src/dc/uil/mview1.uid /remote/rd40/src/dc/uil/mview2.uid /remote/rd40/src/dc/uil/mview3.uid Fatal: Could not open menu files. (MUTIL-3)

WHAT NEXT

Check and correct uid_directory variable in your .synopsys_dc.setup file, then reinvoke the design_analyzer.

MV-001 (warning) cell %s(%s) was constrained to operate under the operating condition %s, but the library cell %s matching this characterization cannot be found in the link libraries. Instead, library cell %s from %s:%s (voltage = %s, process = %f, temperature = %f) has been used.

DESCRIPTION

This warning message occurs when your block or the cell has been required to operate under a certain supply voltage (using set_operating_condition command), but this particular cell cannot be linked to a library cell that was characterized under this supply voltage.

WHAT NEXT

Check the operating condition for the particular block or cell. Set the proper operating condition using the **set_operating_conditions** command or check the library.

SEE ALSO

set_operating_conditions(2)

MV-001a (information) The cell %s with library cell %s is a %s.

DESCRIPTION

This information message occurs when there is a MV-001 happened earlier. This message is to tell what kind of cell this cell is. The cell can be one of the following: isolation cell, level shifter, switch cell, retention register or a normal cell. The normal cells are non power-design-specific cells, which includes standard cells and macro cells.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

MV-001(2)

MV-001b (information) Library cell %s from %s:%s (voltage = %s, process = %f, temperature = %f) has been found.

DESCRIPTION

This information message occurs when there is a MV-001 happened earlier. This message intends to help user identify what causes the eariler MV-001, whether it is due to a library setup issue or a tool’s problem. This message reports, one at a time, the related library cell found in both target and link library with its supply voltage information.

WHAT NEXT

Check all MV-001b against the previous MV-001 and make sure the library setup is correct.

SEE ALSO

MV-001(2)

MV-002 (error) command %s is not supported in mv_mode in psyn_shell; please use dc_shell -mv_mode.

DESCRIPTION

This error message occurs because the current release does not support the specified command in mv_mode in psyn_shell.

WHAT NEXT

Do not use the mv_mode option for this command, or try dc_shell -mv_mode.

MV-003 (error) The %s option is not supported.

DESCRIPTION

This error message occurs because the specified option is supported only in mv_mode.

WHAT NEXT

Either use mv_mode, or remove the option that is not supported, and run the command again.

MV-004 (information) The operating condition of the parent cell %s is different from that of the child cell %s in the design %s. The child cell will not be ungrouped.

DESCRIPTION

This information message occurs when a cell will not be ungrouped by default if its operating condition is different from its parent.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

compile(2)

MV-005 (error) The %s command is not supported.

DESCRIPTION

This error message occurs because the specified command is supported only in mv_mode.

WHAT NEXT

Rerun the command using mv_mode, or remove the unsupported command.

MV-006 (error) The target_library does not contain an inverter characterized for operating condition %s.

DESCRIPTION

The target_library does not contain an inverter corresponding to the operating condition. For MV design, it is required that all libraries corresponding to the

operating conditions used in the current design be included in the target_library, and each library contains at least an inverter.

WHAT NEXT

Make sure the library characterized for the operating condition is included in the target_library variable, and add an inverter to the library for that operating condition if none exists.

MV-007 (error) The target library for the opcond %s does not contain all required gates.
Either a NOR, or an AND and an OR gate (two-input) is required for mapping.

DESCRIPTION

The target_library corresponding to the operating condition does not contain the minimum set of gates required by the mapping algorithms. For performing mapping, it is required that each opcond that is used in the current design has a target library with minimum set of gates.

WHAT NEXT

Add all the required gates to the target_library for that opcond and rerun the command.

MV-008 (error) The instance %s has the operating condition %s which is different from top level design.
Compile command is not supported with instance specific operating conditions
Please use ACS or bottom up methodology.

DESCRIPTION

This error message is printed out when compile is used without -top option and there are instance specific opconds. It is OK for the instance to have instance specific operating conditions if it has been dont_touched.

WHAT NEXT

Either use ACS or use bottom up methodology and compile -top.

SEE ALSO

set_operating_conditions(2)

MV-009 (error) Object %s has target_library_subset {%s}. Compile command is not supported with target library subsetting.
Please use ACS or bottom up methodology.

DESCRIPTION

This error message is printed out when compile is used without -top option and there are instance specific target library settings. It is OK for the instance to have instance specific target library subset if it has been dont_touched.

WHAT NEXT

Either use ACS or use bottom up methodology and compile -top.

SEE ALSO

set_target_library_subset(2)

MV-010 (error) The target_library_subset {%s} does not contain an inverter characterized for operating condition %s.

DESCRIPTION

For MV design, it is required that each target library subset that is set on instances has an inverter that is characterized for the operating conditions of the instances.

WHAT NEXT

Make sure the library characterized for the operating condition is included in the target library subset, and add an inverter to the library for that operating condition if none exists.

SEE ALSO

set_target_library_subset(2)

MV-011 (error) The target_library_subset does not contain all required gates for the operating condition %s. Either a NOR, or an AND and an OR gate (two-input) is required for mapping.

DESCRIPTION

For performing mapping, it is required that each target_library_subset that is set on instances has at least the minimum set of gates.

WHAT NEXT

Add all the required gates to the target_library_subset and rerun the command.

SEE ALSO

set_target_library_subset(2)

MV-012 (error) Library '%s' specified in target library subset on cell '%s' is not in global target library list.

DESCRIPTION

All the libraries specified using target_library_subset should be listed in the global target library list.

WHAT NEXT

Either add those libraries to target_library TCL variable, or remove them from the target_library_subset.

SEE ALSO

set_target_library_subset(2)
remove_target_library_subset(2)

MV-013 (error) There is mismatch between the target library subset and operating condition specified on cell '%s'.

DESCRIPTION

There must be at least one library in the defined target_library_subset on a block which has nominal process,voltage and temperature (PVT) same as the PVT parameters of the operating condition defined on that block.

WHAT NEXT

Either modify the target_library_subset that is defined on that particular block or modify the operating condition on that block.

SEE ALSO

set_operating_conditions(2)
set_target_library_subset(2)

MV-014 (warning) The library cell of cell %s is not from the target_library_subset being used on that block.

DESCRIPTION

The target_library_subset defined on a block is used when a new cell is created during optimization. Existing mapped cells are not required to come from this subset. However, check_target_library_subset will issue this message to alert you that such a situation exists.

WHAT NEXT

Based on your requirements, you can ignore the message, modify the target_library_subset on the block, or manually translate that cell to use a library cell from the target_library_subset.

SEE ALSO

set_target_library_subset(2)

MV-015 (error) Cannot read target_library_subset file %s

defined on %s.

DESCRIPTION

The library file defined in the target_library_subset cannot be found, or cannot be read into memory.

WHAT NEXT

Check the spelling of that file name, or check your search_path to make sure that the file can be found through search_path.

SEE ALSO

set_target_library_subset(2)

MV-016 (warning) Different operating conditions are used in scenarios %s and %s.
This multicorner functionality requires running with -mv_mode.

DESCRIPTION

Each scenario has its own operating conditions. If you specify different operating conditions across the scenarios, this activates multicorner behavior, which requires running the shell with the -mv_mode option.

WHAT NEXT

Run the shell with the -mv_mode option.

SEE ALSO

set_operating_conditions(2)
report_design(2)
create_scenario(2)

MV-017 (warning) %s operating condition %s for instance %s has a
different temperature than top level %s operating condition %s.

Delays may be inaccurate as a result.

DESCRIPTION

In multi voltage synthesis, you may define different operating conditions for the top level design and cell instances. However, only one max temperature (and one min temperature) is used for wire delay evaluation in the design, so delays may be inaccurate.

WHAT NEXT

Change the conflicting operating condition, or accept delay inaccuracies.

SEE ALSO

set_operating_conditions(2)

MV-018 (error) command %s in mv_mode is not supported in db_mode; please use xg_mode.

DESCRIPTION

This error message occurs because the current release in mv_mode does not support the specified command in db_mode.

WHAT NEXT

Do not use the mv_mode option for this command, or use xg_mode.

MV-019 (error) Use of SPDM library %s is not supported.

DESCRIPTION

Libraries using Single Polynomial Delay Models (SPDM) format are not supported in MV compile.

WHAT NEXT

Supply library which makes use of formats supported in MV compile.

MV-021 (warning) No operating condition was set in scenario %s

DESCRIPTION

If you are creating scenarios with the create_scenario command, it is also necessary to set an operating condition for each scenario. This is done by giving the command set_operating_conditions somewhere after the create_scenario command.

WHAT NEXT

Use the set_operating_conditions command within each scenario.

SEE ALSO

create_scenario(2) set_operating_conditions(2)

MV-022 (Error) A total of %d operating condition problems (MV-001) have been detected; %d of them have been reported above. Delay calculation will be incorrect if these problems are not fixed. %s

DESCRIPTION

This is a summary message for a number of operating condition problems (MV-001) detected in the design linking, check_mv_design, or compile/physopt commands. It tells you how many operating condition problems have been detected by the tools, and what libraries have been searched in a prior attempt to link the design.

WHAT NEXT

Check the operating condition for the particular block or cell. Set the proper operating condition using the **set_operating_conditions** command or check the library.

SEE ALSO

set_operating_conditions(2)

MV-024 (error) Found '%d' occurrence(s) of target library subset

specification(s) with conflicting operating conditions.

DESCRIPTION

This message provides number of target library subset specifications that have conflict with the operating condition specified on respective blocks. The conflict occurs if none of the libraries in a target library subset has nominal process, voltage and temperature values (PVT values) which agree with the PVT values specified in operating condition.

WHAT NEXT

Please run check_mv_design command to get details on incorrect target library subset specifications. Then make sure each specification has at-least one library that matches the operating condition specified on the block.

SEE ALSO

set_operating_conditions(2)
set_target_library_subset(2)
remove_target_library_subset(2)
check_mv_design (2)

MV-025 (warning) You have used set_target_library_subset, but the design already contains %d cells mapped to libraries outside the subset. The target_library_subset will apply to new cells created or modified during optimization.

DESCRIPTION

This message alerts you to the fact that, prior to optimization, your design already contains some cells which are mapped to libraries outside of the target_library_subset you requested.

Depending on your requirements, this may or may not be a problem.

The target_library_subset only affects cells that are created or modified during optimization. Existing mapped cells are not required to come from this subset.

If you are getting this message, and did not want to allow existing cells to be mapped to libraries outside the subset, you need to manually translate those cells using change_link, or recompile the block on its own using a more restrictive $target_library. This situation should not arise if you set the target_library_subset prior to the initial compile from RTL.

WHAT NEXT

Based on your requirements, you may ignore the message, or may need to manually translate existing cells. Use check_mv_design for details about the cells outside the subset.

SEE ALSO

set_target_library_subset(2)
remove_target_library_subset(2)
check_mv_design(2)

MV-026 (warning) No default operating condition is defined for library %s.

DESCRIPTION

All libraries used for multi-voltage design must have the 'default_operating_conditions' attribute defined.

WHAT NEXT

Make sure the library has its 'default_operating_conditions' defined. Re-generate the DB file for the library using library compiler after correcting the problem.

SEE ALSO

check_mv_design (2)

MV-027 (warning) The nominal operating conditions (process = %.3f, voltage = %.3fV, temperature = %.3f) of library %s do not match the values (process = %.3f, voltage = %.3fV, temperature = %.3f) of its default operating conditions %s.

DESCRIPTION

All libraries used for multi-voltage design must have their nonimal process, voltage and temperature values matching that of their default operating conditions, respectively.

WHAT NEXT

Make sure the library has the correct nominal process, voltage and temperature, and they are matching the values defined in the default operating condition. Re-generate the DB file for the library using library compiler after correcting the problem.

SEE ALSO

check_mv_design (2)

MV-028 (warning) No operating condition has been set explicitly on the current design. A default operating condition will be assumed.

DESCRIPTION

The user must use set_operating_conditions command to explicitly apply an operating condition onto the current design, otherwise, a default operating condition will be assumed, which may not be what the user desires.

WHAT NEXT

Use set_operating_conditions command to explicitly apply an operating condition onto the current design.

SEE ALSO

check_mv_design (2)
set_operating_conditions (2)

MV-029 (error) Either no operating condition has been applied for the current design (warning MV-028), or the libraries have improper operating condition characteristics, as reported in warnings MV-026 or MV-027.

DESCRIPTION

Make sure the libraries have default_operating_conditions defined, and are matching the nominal process, voltage and temperature values of the libraries. Also make sure that set_operating_conditions command has been used to explicitly apply an operating condition onto the current design.

WHAT NEXT

Check and correct the library problems in warning MV-026 or MV-027. Also check that an operating condition has been applied onto the current design.

SEE ALSO

check_mv_design (2)
set_operating_conditions (2)

MV-030 (warning) Improper use of %s %s as a core cell in the design.

DESCRIPTION

This message is printed when isolation cell that connects logic cells fully contained in same sub design is found. This results in isolation cell being used as a core cell in the design. Isolation cells should be used as boundary cells to isolate two different power domains. Improper use of isolation cell may result in unexpected tool behavior during placement and routing phase.

WHAT NEXT

Remove isolation cell.

SEE ALSO

check_mv_design (2)

MV-031 (warning) You have used isolation cells without power domains. Please check %s %s is correctly used in the design.

DESCRIPTION

This message is printed when isolation cells or enable level shifters are found but when power domain definitions are not found. Proper use of isolation cells can’t be checked in the absence of power domains. You can ignore this message if cells are properly instantiated. Otherwise, unexpected results may occur.

WHAT NEXT

Define power domains.

SEE ALSO

check_mv_design (2)
create_power_domains(2)

MV-032 (warning) Found %d isolation cell(s) or enable level shifter cell(s) used in the core of the design.

DESCRIPTION

This message summarizes number of isolation cells or enable level shifters used as core cells in the design.

WHAT NEXT

Run **check_mv_design** for more details.

SEE ALSO

check_mv_design (2)

MV-033 (warning) Found %d isolation cell(s) or enable level shifter cell(s) whose connections could not be checked for correctness. Please ensure correct use of isolation cells or use power domain specification.

DESCRIPTION

This message summarizes number of isolation cells or enable level shifters whose connections could not be checked to ensure their proper use . This message is issued when power domain definitions are not found but when isolation cells or enable level shifters are found.

WHAT NEXT

Specify power domain definitions. When power domain definitions are provided, isolation cell connections can be checked to make sure they connect to boundaries of power domains.

SEE ALSO

check_mv_design (2)

MV-034 (error) When power domain is used, your design can not be written in DB format.

DESCRIPTION

This message is issued when you are trying to write the design in DB Format while there is a power domain in your design. Since power domain informaion can not be saved with design in DB format, please write the netlist using DDC format instead of DB format.

WHAT NEXT

Write the design in DDC format.

SEE ALSO

write(2).

MV-035 (error) Use of merged NLDM library %s is not supported.

DESCRIPTION

Libraries using merged Non-linear Delay Model (NLDM) format are not supported in MV compile.

WHAT NEXT

Supply library which makes use of formats supported in MV compile.

MV-036 (error) Cannot find power on signal '%s' in power domain '%s' defined on '%s'.

DESCRIPTION

Power on signal could not be located inside specified power domain.

WHAT NEXT

Check signal name to make sure it is correct. If signal is optimized away, to

prevent optimization mark it dont touch.

MV-037 (error) Cannot find power acknowledge signal '%s' in power domain '%s' defined on '%s'.

DESCRIPTION

Power acknowledge signal could not be located inside specified power domain.

WHAT NEXT

Check signal name to make sure it is correct. If signal is optimized away, to prevent optimization mark it dont touch.

MV-038 (warning) Disable state logic- %d of %s %s differs from value of constant net %s connected to its input pin.

DESCRIPTION

This message is displayed when the disable state of the isolation cell or enable level shifter differs from the logic constant connected to the input of that cell.

WHAT NEXT

Ensure intended use of the isolation cell.

MV-039 (warning) Found %d isolation cells or enable level shifters with inputs connected to logic constants that differ from disable state of these cells.

DESCRIPTION

This message summarizes total number of isolation cells and enable level shifters whose inputs are connected to constants that differ from disable state of these cells.

WHAT NEXT

Ensure intended use of the isolation cell.

MV-040 (error) Cannot find instances of cells matching name(s) '%s' in power domain '%s' defined on '%s'.

DESCRIPTION

This message is printed when instance names are specified in $power task but when instances could not be found in the net-list.

WHAT NEXT

Make sure instance names are correctly specified.

MV-041 (error) Net '%s' crossing two power domain boundaries could not be constrained.

DESCRIPTION

This message is printed when a net crossing power domain boundaries could not be constrained properly. This can happen in extreme cases such as when net has loop on it.

WHAT NEXT

Please check connection on net to make sure it is properly connected to cells. Otherwise, please contact Synopsys Technical Support.

SEE ALSO

check_mv_design (2).

MV-042 (warning) Isolation cell is required on net %s connecting %s and %s.

DESCRIPTION

This message is printed when a net with missing isolation is found. A net must have isolation cell if it is driven by always on domain and connected to relatively less power down domains. If isolation cell on such nets is not provided, then circuit may draw excessive short circuit current. This may result in unexpected behavior.

WHAT NEXT

Please specify proper always on relationship between two power domains or add isolation cell on the net. The message is issued only on first violation detected on the net. Please analyze isolation cell requirement on all connections between drivers and load pins on the net.

SEE ALSO

check_mv_design (2). **set_relative_always_on** (2).

MV-043 (warning) Found redundant isolation cell on net %s connecting %s and %s.

DESCRIPTION

This message is printed when isolation cell is found when it is not required. This can happen when a net driven by always on domain and connected to relatively power down domain is isolated using isolation cell. Presence of isolation cells triggers design constraining. This may result in QOR loss in the final net-list.

WHAT NEXT

Please check always on relationship between two power domains or remove isolation cell from the net. The message is issued only on first violation detected on the net. Please analyze isolation cells on all connections between drivers and load pins on the net and fix isolation requirement accordingly.

SEE ALSO

check_mv_design (2). **set_relative_always_on** (2).

MV-044 (warning) Found isolation cell %s in the logic core of the power domain.

DESCRIPTION

This warning message occurs when the specified isolation cell does not connect two different power domains. The isolation cell should be used as the boundary cell to isolate two different power domains. Improper use of the isolation cell may result in unexpected tool behavior during the place and route phase.

WHAT NEXT

This is only a warning message. No action is required.

However if the results are not what you intended, remove the isolation cell and run the command again.

SEE ALSO

check_mv_design(2)

MV-045 (error) Found '%d' net(s) which could not be properly constrained.

DESCRIPTION

This message provides number of nets which tool could not constrain properly for various reasons.

WHAT NEXT

Please run command **check_mv_design** for details.

SEE ALSO

check_mv_design (2).

MV-046 (warning) Found %d net(s) without isolation.

DESCRIPTION

This message provides number of nets for which isolation is missing.

WHAT NEXT

Please run command **check_mv_design -verbose** for details.

SEE ALSO

check_mv_design (2).

MV-047 (warning) Found %d net(s) with redundant isolation cells.

DESCRIPTION

This message provides number of nets on which redundant isolation cell is found.

WHAT NEXT

Please run command **check_mv_design -verbose** for details.

SEE ALSO

check_mv_design (2).

MV-048 (warning) Found %d isolation cell(s) on net(s) not crossing power domain boundaries.

DESCRIPTION

This message provides number of isolation cells which are not connected to nets crossing power domain boundaries.

WHAT NEXT

Please run command **check_mv_design -verbose** for details.

SEE ALSO

check_mv_design (2).

MV-049 (warning) Block ’%s’ contain(s) %d instance(s) of library cell(s) defined in libraries that (is)are not part of the target library subset ’%s’ specified on it.

DESCRIPTION

This message summarizes number of technology cells linked to libraries that are not part of target library specification set on that block.

WHAT NEXT

Depending upon your circumstances, you can ignore this message. Alternatively, you can modify target library subset specification on the block.

SEE ALSO

check_mv_design (2).

MV-050 (error) %s is required for %s.

DESCRIPTION

-power_down_ctrl requires -power_down option; -power_down_ack requires -power_down_ctrl option.

WHAT NEXT

Add required option to the command

MV-051 (error) %s %s already exists.

DESCRIPTION

The power domain or power net already exist. This error is issued either because the named power domain or net already exist, or becasue you are creating a design-level domain that exists already.

WHAT NEXT

MV-052 (error) Power net %s does not exist.

DESCRIPTION

Could not find the power net.

WHAT NEXT

MV-053 (error) Cannot attach internal net to unswitched domain %s.

DESCRIPTION

Internal power net can only be attached to power down domain.

WHAT NEXT

MV-054 (error) nominal_voltages_list and voltage_ranges_list must be defined together, and the length of the voltage_ranges_list (currently %d) must be twice the length of the nominal_voltages_list (currently %d).

DESCRIPTION

Whenever -nominal_voltages option is specified for create_power_net_info command, -voltage_ranges must also be specified, and vice versa. Furthermore, since voltage_ranges_list define the left and right ranges around the nominal_voltages, its length must be twice that of the length of the nominal_voltages_list.

WHAT NEXT

MV-055 (error) Nominal voltages, voltage ranges, and "switchable" option cannot be used with ground nets.

DESCRIPTION

Nominal voltages, voltage ranges, or ’switchable’ option can only be specified for power nets.

WHAT NEXT

MV-056 (error) %s need to be all positive, and listed in ascending order.

DESCRIPTION

WHAT NEXT

MV-057 (error) Nominal voltage %f is not within the range [%f,%f].

DESCRIPTION

WHAT NEXT

MV-058 (error) Could not connect power net '%s' with power pin '%s' on cell '%s'.

DESCRIPTION

The power pin is not compatible with the type of power net.

WHAT NEXT

Check the types of power net and power pin.

MV-059 (error) Could not find power pin ’%s’ on cell ’%s’.

DESCRIPTION

WHAT NEXT

MV-060 (info) Power domain %s has already been defined as always_on relative to power domain %s.

DESCRIPTION

The relative always on relationship between two power domains has already defined.

WHAT NEXT

MV-061 (warning) Power domain %s is always on. Power domain %s can’t be explicitly set less always on relative to it.

DESCRIPTION

Relative always on behavior can be set when both power domains are power down domains.

WHAT NEXT

MV-062 (error) Instance domain %s cannot be created until top-level power domain is defined.

DESCRIPTION

WHAT NEXT

MV-063 (error) Domain %s is not a power down domain. Power

down ack signal can be specified only on power down domain.

DESCRIPTION

WHAT NEXT

MV-064 (error) Power domain %s can not be created because cell %s can not be added to the power domain.

DESCRIPTION

Only hierarchical cell or black box cell can be added to power domain. Black box cells are defined as cells without behavior. This could be also caused by library link problem.

WHAT NEXT

MV-065 (error) Cell %s already belongs to power domain %s.

DESCRIPTION

A cell can not belong to more than one power domain.

WHAT NEXT

MV-066 (error) Root cell %s is a child cell of %s. Root cells located at different level of hierarchy must not enclose each other.

DESCRIPTION

This message is issued when cell which is a child cell of another cell is specified in power domain definition.

WHAT NEXT

MV-067 (error) Power down signal must be specified using either port, net or pins.

DESCRIPTION

WHAT NEXT

MV-068 (error) Power down port can be specified only on top-level domain.

DESCRIPTION

WHAT NEXT

MV-069 (error) Only one power down port can be specified on top-level domain.

DESCRIPTION

WHAT NEXT

MV-070 (error) Only input port can be specified as power down

port on top-level domain.

DESCRIPTION

WHAT NEXT

MV-071 (error) Cannot mix power down pin and net definitions.

DESCRIPTION

WHAT NEXT

MV-072 (error) Only one power down net can be specified per domain.

DESCRIPTION

WHAT NEXT

MV-073 (error) Cannot add partial set of instances of the non-uniquified design %s to a power domain.

DESCRIPTION

WHAT NEXT

MV-074 (error) Design-level power domain %s cannot be

removed until all instance power domains are removed.

DESCRIPTION

WHAT NEXT

MV-075 (error) This grouping will split power domain '%s'.

DESCRIPTION

WHAT NEXT

MV-076 (warning) Always on net '%s' is driven by normal cell '%s' of type '%s'.

DESCRIPTION

You receive this message when **check_connection_rules** command detects an always on net that is driven by regular cell. Always on nets must be driven by special cells which always stay powered during operation of the circuit.

WHAT NEXT

Design compiler will automatically fix this error when design is compiled. If you receive this message after design is compiled, please make sure at least one always on buffer and one always on inverter is defined in the target library.

SEE ALSO

check_mv_design (2).

MV-077 (warning) Net '%s' drives pass gate pin '%s' of cell '%s' of type '%s' instantiated in power down region.

DESCRIPTION

You receive this message when **check_mv_design** command detects a pass gate pin of a cell that is driven by always on net or a net driven by always on domain. Such

connections are not recommended for power saving reasons since always on nets stay powered during operation of the circuit. This results in power leakage through the pass gate circuit of the pin.

WHAT NEXT

Design Compiler will automatically fix this violation when design is compiled. If you receive this message after design is compiled, please make sure target library has functionally equivalent cell that does not have pass gate pin.

SEE ALSO

check_mv_design (2).

MV-078 (warning) Always on cell '%s' of type '%s' drives normal net '%s'.

DESCRIPTION

You receive this message when **check_connection_rules** command detects always on cell driving normal net. Such connection is not recommended for power saving reasons since always on cells drain more power compared to regular cells implementing same functionality.

WHAT NEXT

Design Compiler will automatically fix this violation when design is compiled. Please compile design to eliminate this violation.

SEE ALSO

check_mv_design (2).

MV-079 (warning) Output pass gate pin '%s' of cell '%s' drives input pass gate pin '%s' of cell '%s'.

DESCRIPTION

You receive this message when **check_connection_rules** command detects cascaded connection of pass gates. Such connection is not recommended for signal integrity related reasons.

WHAT NEXT

Design Compiler will automatically fix this violation when design is compiled. If you receive this error after design is compiled, please check target libraries and make sure cells without pass gate pins are available.

SEE ALSO

check_mv_design (2).

MV-080 (warning) Found '%d' always on nets that are driven by normal cells.

DESCRIPTION

You receive this message when **check_connection_rules** command detects always on nets that are driven by regular cells. Always on nets must be driven by special cells which always stay powered during operation of the circuit.

WHAT NEXT

Design compiler will automatically fix these errors when design is compiled. If you receive this message after design is compiled, please make sure at least one always on buffer and one always on inverter is defined in the target library.

SEE ALSO

check_mv_design (2).

MV-081 (warning) Found '%d' net(s) that drive pass gate pins of cells instantiated in power down regions.

DESCRIPTION

You receive this message when **check_connection_rules** command detects pass gate pins of cells that are driven by always on nets or nets driven by always on regions. Such connections are not recommended for power saving reasons since always on cells stay powered during operation of the circuit. This results in power leakage through the pass gate circuit of the pin.

WHAT NEXT

Design Compiler will automatically fix these violations when design is compiled. If

you receive this message after design is compiled, please make sure target library has functionally equivalent cell that does not have pass gate pin.

SEE ALSO

check_mv_design (2).

MV-082 (warning) Found '%d' always on cell(s) that drive normal nets.

DESCRIPTION

You receive this message when **check_connection_rules** command detects always on cells driving normal nets. Such connections are not recommended for power saving reasons since always on cells consume more power compared to regular cells implementing same functionality.

WHAT NEXT

Design Compiler will automatically fix these violations when design is compiled. Please compile design to eliminate these violations.

SEE ALSO

check_mv_design (2).

MV-083 (warning) Found '%d' cells whose output pass gate pins drive input pass gate pins of other cells.

DESCRIPTION

You receive this message when **check_connection_rules** command detects cascaded connection of pass gates. Such connections are not recommended for signal integrity related reasons.

WHAT NEXT

Design Compiler will automatically fix these violations when design is compiled. If you receive these errors after design is compiled, please check target libraries and make sure cells without pass gate pins are available.

SEE ALSO

check_mv_design (2).

MV-084 (error) Always on buffer and inverter were not found in target libraries.

DESCRIPTION

You receive this message when design contains always on logic but always on inverter and buffers were not found in the target libraries.

WHAT NEXT

Add always on buffer and inverter for each operating condition and re-run design compiler.

SEE ALSO

MV-085 (error) Always on buffer and inverter cells are found in target libraries.

DESCRIPTION

You receive this message when always on buffers and inverters are found in the target libraries. These special cells are not supported.

WHAT NEXT

Please remove these cells from target libraries or exclude these cells using set_dont_use command.

SEE ALSO

set_dont_use (2)

MV-086 (warning) You have provided ambiguous libraries: %s:%s %s:%s

Both are characterized for voltage %fV, process %f, temperature %f
and contain the same lib_cell names (e.g. %s).
The latter library will be ignored.

DESCRIPTION

This warning message occurs when your $link_library and $target_library contain multiple libraries which characterize the same lib_cells for the same voltage, process, and temperature. The tool has no way to distinguish which library should be used. This warning will be issued and the first library will be used.

WHAT NEXT

Remove one of the ambiguous libraries from your $link_library and $target_library. If you wanted to use both libraries, and they represent different characterization points, the libraries would need to have different nominal_voltage, nominal_process, and nominal_temperature values. The tool matches these library values with the operating condtions applied to the design, to decide which libraries are suitable for the design cells.

SEE ALSO

set_operating_conditions(2)

MV-087 (error) lib_cell %s:%s/%s is inconsistent with lib_cell %s:%s/%s.

%s %s:%s/%s will be ignored.
Please correct your $link_library and/or $target_library.

DESCRIPTION

You have provided two libraries describing the same lib_cell name (characterizing the part for different operating conditions). However, the descriptions of the part are not consistent, apart from variation allowed for the characterization.

The reason for the inconsistency is reported following this error message. A typical example is if the lib_cells have a different set of pins.

WHAT NEXT

Remove one of the inconsistent libraries from your $link_library and $target_library.

SEE ALSO

MV-088 (error) Library inconsistencies have been reported. This command will not execute.

DESCRIPTION

Inconsistent libraries have been found, and reported with MV-087. The current command will not execute. You need to correct your $link_library and $target_library to remove one or both of the inconsistent libraries.

WHAT NEXT

Remove one of the inconsistent libraries from your $link_library and $target_library.

SEE ALSO

MV-089 (error) Unsupported method to create always on exception paths in domain '%s' created inside block '%s'.

DESCRIPTION

This message is printed when tool encounters $power HDL directive that translates into power down domain but has primitive instances in instance list. When tool finds domain with primitive instances, it marks input pins of all these instances with always on attribute. However, this is done only when the domain is designated as always on domain. When domain with a power down signal is found, the tool does not know how to handle domain creation. This message informs users of this condition.

WHAT NEXT

Check $power directives specified in the RTL and rerun infer_power_domains command.

SEE ALSO

infer_power_domain(2)

MV-090 (error) You are using isolation cells without power domains. Use of isolation cells without power domain definitions

is not supported.

DESCRIPTION

This message is printed when isolation cells are found in the design but no power domain specification is found. Starting 2006.06 release of Design Compiler, the tool set is enhanced to support power domain specification. Power domain specification allow users to identify multi voltage / multi supply blocks and specify relative power sequencing behavior between them. This enhancement enables Design Compiler to properly derive constraints on nets connected to isolation cells. Power domains also allow tool to check for incorrect use of isolation cells.

WHAT NEXT

It recommended to use power domain specification for designs containing isolation cells.

SEE ALSO

create_power_domain(2)
check_mv_design(2)

MV-091 (error) You are using isolation cells without power domains, as a result the derived design constraints may not be correct. Supply power domain definitions and re-start synthesis session.

DESCRIPTION

This message is printed when isolation cells are found in the design but no power domain specification is found. Starting 2006.06 release of Design Compiler, the tool set is enhanced to support power domain specification. Power domain specification allows users to identify multi voltage / multi supply blocks and specify relative power sequencing behavior between them. This enhancement enables Synopsys tools to properly derive constraints on nets connected to isolation cells so that nets can be optimized using buffers from correct power domain.

Power domains also allow tool to check for incorrect use of isolation cells. This helps identification of incorrect use of ISO cells in early stages of design development.

WHAT NEXT

It recommended to use power domain specification for designs containing isolation cells. If you still want to continue without aborting synthesis, use TCL variable

allow_iso_cell_without_power_domains and set it to true prior to compile. Support for derived constraints related to isolation cells without power domains specification will be obsoleted in the next major release of software.

SEE ALSO

create_power_domain(2)
check_mv_design(2)

MV-092 (error) The command translate is not supported for MV designs. In order to translate, please write out a Verilog netlist and run the command in a separate shell.

DESCRIPTION

The command translate should only be used for non-MV designs.

WHAT NEXT

Do not use this command for MV designs, or in a shell with -mv_mode option. Instead, follow these steps to translate a design that was originally an MV design:

Step 1: start dc_shell (without -mv_mode option) Step 2: set link_library to the old libraries used by the design Step 3: read the design netlist (Verilog/VHDL etc.) Step 4: set target_library to the new libraries Step 5: invoke 'translate' command Step 6: apply the multi-voltage constraints now (operating conditions, target library subsets, etc.)

If the original netlist has level-shifters, they would have been removed during the translation. You have to invokes 'insert_level_shifters' command again to insert level-shifters for the MV design based on the new libraries.

MV-093 (warning) Power domain %s inferred from HDL source is removed. Simulation and synthesis results may not match.

DESCRIPTION

This messages is printed when power domain inferred from HDL is removed using remove_power_domain command. Its purpose is to warn users that pre synthesis simulation results of design with power domain definitions in HDL may not match post synthesis simulation results.

SEE ALSO

infer_power_domain (2)

MV-094 (warning) Signal %s controlling switching of the domain %s is not connected to cell %s. Power down signal will not be associated with domain being propagated during constrain budgeting.

DESCRIPTION

This message is printed when signal controlling power down behavior was not found during constraint propagation. This can happen when dc_allocate_budget or characterize command is issued on a cell which does not have power down signal connected to it. Tool will mark propagated domain as power down domain, however, power down signal will not be associated with it. For more information on how domain is marked power down without power down signal, please refer to **create_power_domain** man page.

WHAT NEXT

Connect power down signal to the cell.

SEE ALSO

create_power_domain(2)

MV-095 (warning) Power acknowledgement signal %s for domain %s is not connected to cell %s. Power acknowledge signal will not be associated with domain being propagated during constrain budgeting.

DESCRIPTION

This message is printed when power acknowledge signal was not found during constraint propagation. This can happen when dc_allocate_budget or characterize command is issued on a cell which does not have power acknowledge signal connected to it.

WHAT NEXT

Rewire connections to connect power acknowledge signal to the cell.

SEE ALSO

create_power_domain(2)

MV-096 (warning) Retiming will not be performed because one of the blocks (%s) specified for retiming contains heterogeneous operating conditions.

DESCRIPTION

Retiming can only be performed if all the blocks specified for retiming contains homogeneous operating conditions. In other words, every one of them can only have one operating conditions between its hiererachy.

WHAT NEXT

Check that every block specified by set_optimize_registers or set_balance_registers commands contains only homegenenous operating conditions. Specify the sub-blocks separately for retiming if the top block is heterogeneous.

SEE ALSO

set_optimize_registers(2)
set_balance_registers(2)

MV-097 (error) You have specified power domain definitions and also set variable disable_iso_net_constraints to true. Please remove variable from script.

DESCRIPTION

This message is printed when power domain definitions are provided and at the same time disable_iso_net_constraints variable is set to true. Variable disable_iso_net_constraints should be used only when power domain definitions are not provided.

WHAT NEXT

Remove disable_iso_net_constraints from the script.

SEE ALSO

MV-098 (error) No power domain has been created.

DESCRIPTION

This message is printed when a power domain is needed but has not been created.

WHAT NEXT

Create a power domain.

SEE ALSO

create_power_domain(2)

MV-099 (warning) Control signal %s specified on power domain %s will be removed from power domain.

DESCRIPTION

This message is printed when power down control signal or power acknowledge signal is deleted during optimization. This can happen if logic connected to this signal is redundant and optimization algorithms decided to eliminate that logic for saving design area.

This message is also printed when power acknowledge signal is removed from power domain when power down signal is optimized away during optimization. This is because power acknowledge signal can be specified only when power down signal is specified.

When power down signal is removed, domain is marked as power down domain without power down signal.

WHAT NEXT

SEE ALSO

create_power_domain(2)

MV-100 (error) For power net %s, either max-delay operating voltage (%f) or min-delay operating voltage (%f) do not reside within a valid range, or they do not reside in the same range.

DESCRIPTION

Both max-delay and min-delay operating voltages must reside in a valid voltage range, and in the same range.

WHAT NEXT

MV-101 (error) Internal power net %s attached to a power domain cannot have different nominal/ranges properties from the primary power net %s.

DESCRIPTION

Internal and primary power nets connected to a power domain must have the same nominal voltages and voltage ranges.

WHAT NEXT

create_power_net_info

MV-102 (error) Power/ground net %s cannot be connected to the internal port of a coarse-grained MTCMOS switch-box because the power/ground net is already switched by another switch-box in the design.

DESCRIPTION

To prevent multiple sources/sinks of different voltage levels from connecting to the same power/ground net, only one coarse-grained switch is allowed for a power/ground net.

WHAT NEXT

create_power_net_info
connect_power_domain

MV-103 (warning) Power/ground net %s is being replaced by %s as a %s connection for power domain %s.

DESCRIPTION: You received this message because this command does not take incremental defination s.

WHAT NEXT: Combine all the power and ground declarations for one particular power domain in one statement for connect_power_domain. connect_power_domain -primary_power_net [ ] -primary_ground _net [ ]

MV-104 (error) Redefinition of power net %s.

DESCRIPTION

Power net has been redefined.

WHAT NEXT

MV-105 (error) The template of power states is not defined.

DESCRIPTION

The template of power states need to be defined before create or remove nominal power states.

WHAT NEXT

Set power state template by set_nominal_power_state_template.

SEE ALSO

set_nominal_power_state_template(2)

MV-106 (error) The definition of power states is incompatible

with the current template.

DESCRIPTION

The definition of power states must be compatible with the template created using the **create_pst** command in UPF mode, or the **set_nominal_power_state_template** command in non-UPF mode. For example:

```
prompt> create_pst my_pst -supplies {VDD VDDG VDDGS VDDMS VDDX VDDXS VDDY VDDYS}

prompt> add_pst_state overdrive -pst my_pst -state {HV HV HV HV LV LV LV}
```

In this example, the number of supplies listed in the template (8) does not match those listed in **add_pst_state** (7).

WHAT NEXT

Rerun the **add_pst_state** command listing the correct number of supplies.

SEE ALSO

add_pst_state(2)
create_nominal_power_state(2)
create_pst(2)
remove_nominal_power_state(2)
set_nominal_power_state_template(2)

MV-107 (error) Voltage %s is not a nominal voltage of %s.

DESCRIPTION

Voltage used to define power state should be one of the nominal voltages of the power net.

WHAT NEXT

SEE ALSO

set_nominal_power_state_template(2)
create_nominal_power_state(2)
remove_nominal_power_state(2)

MV-108 (error) Power net %s is not switchable.

DESCRIPTION

The power net should be switchable if 'off' is used as a nominal voltage.

WHAT NEXT

SEE ALSO

set_nominal_power_state_template(2)
create_nominal_power_state(2)
remove_nominal_power_state(2)

MV-109 (error) power state %s has been defined.

DESCRIPTION

The power state has already been defined.

WHAT NEXT

MV-110 (Error) Power domain %s cannot be defined as always on relative to itself.

DESCRIPTION

The always on relationship can be specified between two different domains.

WHAT NEXT

MV-111 (error) power state template has been defined. To proceed please reset the template.

DESCRIPTION

The power state template can not be set multiple times.

WHAT NEXT

MV-112 (error) can not find power state %s.

DESCRIPTION

The power state to be deleted must be created first.

WHAT NEXT

MV-113 (error) Multicorner feature is not supported in Design Compiler.

DESCRIPTION

All the scenarios should have the same operating conditions.

WHAT NEXT

Specify the same operating conditions for all the scenarios.

SEE ALSO

MV-114 (error) Multi-scenario and and multi-voltage features can only be used together in UPF mode in Design Compiler.

DESCRIPTION

You must invoke dc_shell with UPF mode in order to take advantage of the combined support of multi-scenario creation and multi-voltage synthesis.

WHAT NEXT

Rerun the DC script with UPF mode turned on.

MV-115 (warning) Correct %s operating condition cannot be

determined for macro cell %s given the supply voltages %s.

DESCRIPTION

Worst-case or best-case operating conditions are normally derived for a supply connected macro cell if a library containing the macro cell can be determined, and the library has been characterized for the given worst-base or best-case voltage settings, respectively. This warning is given when such a library cannot be found. Instead, the instance-specific operating condition on the macro-cell is used, if given. Otherwise, operating condition of the macro-cell's parent is inherited.

WHAT NEXT

Make sure that all power pins of the macro cell are connected to proper supply nets, and operating voltages (worst and best cases) are properly set. Use check_mv_design command to aid debugging.

To be included in the search for the proper operating condition, the worst-case libraries must be specified in link_library variable, and the best-case libraries must be specified through set_min_library command. The best-case libraries should not be included in the link_library variable.

SEE ALSO

set_min_library

MV-116 (warning) Characterization of power supply data (UPF constraints, operating_voltages, etc.) to hierarchical cell '%s' have been skipped.

DESCRIPTION

In order to correct characterize power supply intent into a hierarchical cell, certain requirements on UPF constraints in terms of the topology of the power domains, its scope, and the supply ports must be met. Some basic requirments are: (1) The instance being characterized to must be aligned to the scope of the power domain containing (covering, in terms of extent) this instance. (2) There should not exist any descendent cell that belongs to a power domain whose scope is above the hierarchical instance we are characterizing to. (3) No supply net should cross the hierarchical boundary of instance being characterized to connect to a lower-level supply port. This is to avoid supply port punching that inadvertently modifies the power intent.

WHAT NEXT

Make sure that the basic requirements as stated in the messages are met, then re-

issue characterize command for the problematic cell.

SEE ALSO

characterize

MV-117 (warning) Characterization of %s '%s' has been skipped because it is refering to objects outside the scope of its domain '%s'.

DESCRIPTION

In order to characterize a strategy (set_retention or set_isolation) or create_power_switch command, the command must not refer to any object outside of its scope.

WHAT NEXT

Correct the skipped commands to refer only to objects defined at the same scope as the domain, then re-issue characterize.

SEE ALSO

characterize set_retention set_isolation create_power_switch

MV-118 (warning) The exception supply connections on cell '%s' are getting lost because its libcell '%s' is being relinked/ resized to an incompatible one.

DESCRIPTION

This problem happens when the old and new library cells are incompatible libraries in terms of the followings: (1) have different sets of pg_pin's, (2) have different pg_pin to voltage_name mapping.

The problem is really in the libraries. The libraries in use are either incompatible, or have errors.

WHAT NEXT

Check your libraries using check_lib command.

MV-119 (warning) Characterization of %s '%s' has been skipped because it contains objects not fully representable in the target instance '%s' of characterize.

DESCRIPTION

In order to characterize a strategy that has -elements list, the objects in the -elements list must be fully representable in the target instance of characterize. For example, the following set_retention strategy cannot be characterized to instance U1:

```
set_retention ret1 -domain U1/PD -retention_power_net U1/TVDD -elements {U1 U1/U2/U3}
```

because within U1, U1 cannot be referenced.

On the other hand, the following set_retention strategy can still be characterized to instance U1:

```
set_retention ret1 -domain U1/PD -retention_power_net U1/TVDD -elements {U1}
```

because within U1, this strategy can be represented using an equivalent form:

```
set_retention ret1 -domain PD -retention_power_net TVDD
```

WHAT NEXT

Correct the skipped commands, possibly by splitting the original strategies into two.

MV-150 (error) Cells '%s' and '%s' in power domain '%s' have different %spower supply voltages.

DESCRIPTION

This error message is printed when two cells in the same power domain are detected to have different power supply voltages. Within one power domain, only one power supply voltage is allowed for all the hierarchical cells.

WHAT NEXT

Check the operating condition for the particular block or cell. Set the proper operating condition using the **set_operating_conditions** command. Or create new power domains to separate cells with different power supply voltages in the differnet power domains.

SEE ALSO

set_operating_conditions(2)
create_power_domain(2)
check_mv_design(2)

MV-151 (warning) %d more voltage mismatches (MV-150) found in the power domain.

DESCRIPTION

This warning message is printed when there are more MV-150 errors but the check_mv_design command has not reported their details.

WHAT NEXT

Use a larger value for the -max_messages option of the check_mv_design command to see the detailed MV-150 error reporting.

SEE ALSO

set_operating_conditions(2)
create_power_domain(2)
check_mv_design(2)

MV-152 (error) Using %s net %s as a %s connection of a power domain is not allowed.

DESCRIPTION

You are either trying to: (1) use a power net as a ground connection for a power domain, or, (2) use a ground net as a power connection for a power domain. This is not allowed.

WHAT NEXT

MV-155 (information) Found target library subset specification

on cell %s. The cell will not be ungrouped.

DESCRIPTION

Cells with target library subset specification can’t be ungrouped.

WHAT NEXT

SEE ALSO

compile(2)

MV-156 (warning) Retention strategy "%s" will not be implemented for cell "%s" in power domain "%s". This cell has no mapping constraint defined using the map_retention_cell command.

DESCRIPTION

This warning indicates that the specified cell targeted for retention synthesis has not been mapped using the **map_retention_cell** command. As a result, the strategy will not be implemented for the specified cell.

WHAT NEXT

Use the **map_retention_cell** command to map all the cells specified using the **-elements** option of the **set_retention** command.

SEE ALSO

set_retention(2)
map_retention_cell(2)

MV-157 (warning) Retention strategy "%s" for power domain "%s" has no mapping constraints defined using the map_retention_cell command. No retention cells will be inserted

for this strategy.

DESCRIPTION

This warning indicates that mapping constraints have not been defined on the retention strategy for the specified power domain using the **map_retention_cell** command. As a result, no retention cells will be inserted for the specified strategy.

WHAT NEXT

Define the mapping constraints for the retention strategy using the **map_retention_cell** command.

SEE ALSO

set_retention(2)
map_retention_cell(2)

MV-158 (warning) The library cell "%s" does not exist in the target libraries.

DESCRIPTION

This warning indicates that the library cell specified using the **map_retention_cell** command, does not exist in the target libraries.

WHAT NEXT

Make sure the library cell specified using the **map_retention_cell** command exists in the target libraries.

SEE ALSO

map_retention_cell(2)
target_library(2)

MV-159 (warning) The library cell "%s" is not a retention cell.

DESCRIPTION

This warning indicates that the library cell specified using the **map_retention_cell** command is not a retention cell.

WHAT NEXT

Make sure that the specified library cell is a retention cell. To check if a library cell is a retention cell, use the **report_lib** command.

SEE ALSO

map_retention_cell(2)
report_lib(2)

MV-160 (warning) Retention cells of type "%s" do not exist in the target libraries.

DESCRIPTION

This warning indicates that the retention cell type specified using the **map_retention_cell** command, does not exist in the target libraries.

WHAT NEXT

Use the target libraries that contain retention cells of the specified type.

SEE ALSO

map_retention_cell(2)
target_library(2)

MV-161 (warning) The library cell "%s" is not in the correct power and ground(PG) pin format.

DESCRIPTION

This warning indicates that the target libraries contain retention cells that are not in the correct power and ground(PG) pin format.

WHAT NEXT

Use the target libraries which have all the retention cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-162 (warning) The library cell "%s" does not have a primary power pin.

DESCRIPTION

This warning indicates that the library cell must have a primary power pin for it to be in the correct power and ground(PG) pin format.

WHAT NEXT

Use the target libraries that have all the library cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-163 (warning) The library cell "%s" does not have a primary ground pin.

DESCRIPTION

This warning indicates that the library cell must have a primary ground pin for it to be in the correct power and ground(PG) pin format.

WHAT NEXT

Use the target libraries that have all the library cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-164 (warning) The multi-rail %s library cell "%s" does not have a backup power or backup ground pin.

DESCRIPTION

This warning indicates that the multi-rail library cell must have a backup power or backup ground pin for it to be in the correct power and ground(PG) pin format.

WHAT NEXT

Use the target libraries that have all the library cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-165 (warning) Found %d retention library cell(s) that are not in the correct power and ground(PG) pin format.

DESCRIPTION

This warning is a summary of the violating retention library cells that are not in the correct power and ground(PG) pin format.

WHAT NEXT

Use the **check_mv_design -verbose** command to view the details of these violations. Use the target libraries that have retention cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)
check_mv_design(2)

MV-165a (warning) The multi-rail retention library cell "%s" does not have the save pin related to its backup power pin.

DESCRIPTION

This warning indicates that the multi-rail retention library cell does not have the save pin related to its backup power pin. This relation is required by the tool to synthesize this cell.

WHAT NEXT

Use the target libraries that have all the retention cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-165b (warning) The multi-rail retention library cell "%s" does not have the restore pin related to its backup power pin.

DESCRIPTION

This warning indicates that the multi-rail retention library cell does not have the restore pin related to its backup power pin. This relation is required for the tool to synthesize this cell.

WHAT NEXT

Use the target libraries that have all the retention cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-165c (warning) The retention library cell "%s" does not have all its signal pins related to a primary power or primary ground pin.

DESCRIPTION

This warning indicates that one or more signal pins of the retention library cell are not related to a primary power or primary ground pin. This relation is required for the tool to synthesize this cell.

WHAT NEXT

Use the target libraries that have all the retention cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-166 (warning) The retention cell "%s" does not have any associated UPF retention strategy.

DESCRIPTION

This warning indicates that the retention cell in the design is not associated with any UPF retention strategy. All retention cells need to have an associated strategy.

WHAT NEXT

Use the **set_retention** command to define a new strategy in the power domain to which the cell belongs. After defining the strategy, use the **map_retention_cell** command to map this cell. Mapping the cell associates it with a UPF retention strategy.

SEE ALSO

set_retention(2)
map_retention_cell(2)
set_retention_control(2)
compile(2)

MV-167 (warning) Found %d level shifter library cell(s) that are not in the correct power and ground(PG) pin format.

DESCRIPTION

This warning is a summary of the violating level shifter library cells that are not in the correct power and ground(PG) pin format.

WHAT NEXT

Use the **check_mv_design -verbose** command to view the details of these violations. Use the target libraries that have level shifter cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)
check_mv_design(2)

MV-167a (warning) The pin "%s" of the level shifter library cell

"%s" is not related to any of its power pins.

DESCRIPTION

This warning indicates that the pin is not related to any power pins of the level shifter library cell.

WHAT NEXT

Use the target libraries that have all the level shifter cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-167b (warning) The pin "%s" of the level shifter library cell "%s" is not related to any of its ground pins.

DESCRIPTION

This warning indicates that the pin is not related to any ground pins of the level shifter library cell.

WHAT NEXT

Use the target libraries that have all the level shifter cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-167c (warning) The power pin "%s" of the level shifter library cell "%s" is not related by any of its signal pins.

DESCRIPTION

This warning indicates that the power pin of the level shifter library cell is not the related power pin for any of its signal pins.

WHAT NEXT

Use the target libraries that have all the level shifter cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-167d (warning) The enable and the output pin of the enabled level shifter library cell "%s" are not related to the same primary power pin.

DESCRIPTION

This warning indicates that the enable and the output pin of the enabled level shifter library cell must be related to the same primary power pin.

WHAT NEXT

Use the target libraries that have all the level shifter cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-167e (warning) The "input_signal_level" attribute is required on the input pin of the single-rail level shifter library cell "%s".

DESCRIPTION

This warning indicates that the "input_signal_level" attribute is not defined on the input pin of the single-rail level shifter library cell. The definition of this attribute is expected on the input pin of the single-rail level shifter library cell.

WHAT NEXT

Use the target libraries that have all the level shifter cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-167f (warning) The "input_voltage_range" attribute is required on the input pin of the level shifter library cell "%s".

DESCRIPTION

This warning indicates that the "input_voltage_range" attribute is required on the input pin of the level shifter library cell unless the variable "mv_default_level_shifter_voltage_range_infinity" is set to "TRUE".

WHAT NEXT

Use the target libraries that have all the level shifter cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-167g (warning) The "output_voltage_range" attribute is required on the output pin of the level shifter library cell "%s".

DESCRIPTION

This warning indicates that the "output_voltage_range" attribute is required on the output pin of the level shifter library cell unless the variable "mv_default_level_shifter_voltage_range_infinity" is set to "TRUE".

WHAT NEXT

Use the target libraries that have all the level shifter cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-168 (warning) The isolation cell "%s" does not have any

associated UPF isolation strategy.

DESCRIPTION

This warning indicates that the isolation cell in the design is not associated with any UPF isolation strategy. All isolation cells must have an associated strategy.

WHAT NEXT

Use the **set_isolation** command to define a new isolation strategy in the power domain, on the port that the cell is isolating.

SEE ALSO

set_isolation(2)

MV-169 (warning) Found %d isolation library cell(s) that are not in the correct power and ground(PG) pin format.

DESCRIPTION

This warning is a summary of the violating isolation library cells that are not in the correct power and ground(PG) pin format.

WHAT NEXT

Use the **check_mv_design -verbose** command to view the details of these violations. Use the target libraries that has isolation cells in the correct power and ground(PG) pin format.

SEE ALSO

check_mv_design(2)

MV-169a (warning) The pin "%s" of the isolation library cell "%s" is not related to any of its power pins.

DESCRIPTION

This warning indicates that the pin of the isolation library cell is not related to any of its power pins. All the pins of the isolation library cell must be related to a power pin (must have the related_power_pin attribute defined).

WHAT NEXT

Use the target libraries that have all the isolation cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-169b (warning) The pin "%s" of the isolation library cell "%s" is not related to any of its ground pins.

DESCRIPTION

This warning indicates that the pin of the isolation library cell is not related to any of its ground pins. All the pins of the isolation library cell must be related to a ground pin (must have the related_ground_pin attribute defined).

WHAT NEXT

Use the target libraries that have all the isolation cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-169c (warning) The isolation library cell "%s" does not have its output pin related to its backup power pin.

DESCRIPTION

This warning indicates that the isolation library cell must have its output pin related to its backup power pin (through the related_power_pin attribute), if it exists.

WHAT NEXT

Use the target libraries that have all the isolation cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-169d (warning) The isolation library cell "%s" does not have its output pin related to its backup ground pin.

DESCRIPTION

This warning indicates that the isolation library cell must have its output pin related to its backup ground pin (through the related_ground_pin attribute), if it exists.

WHAT NEXT

Use the target libraries that have all the isolation cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-170 (warning) Found %d always-on library cell(s) that are not in the correct power and ground(PG) pin format.

DESCRIPTION

This warning is a summary of the violating always-on library cells which are not in the correct power and ground(PG) pin format.

WHAT NEXT

Use the **check_mv_design -verbose** command to view the details of these violations. Use target libraries that have always-on cells in the correct power and ground(PG) pin format.

SEE ALSO

check_mv_design(2)

MV-170a (warning) The always-on library cell "%s" does not

have a backup power or backup ground pin. This can lead to undesirable results in synthesis as the cell may lose power.

DESCRIPTION

This warning indicates that the always-on library cell does not have a backup power pin. As there are no backup pins on the cell, it may not remain powered when the power domain containing the cell turns off. Special consideration needs to be given to the cell’s placement, while going to place and route, to ensure the cell stays on.

WHAT NEXT

Use the target libraries that have all the always-on cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-170b (warning) Pin "%s" of the always-on library cell "%s" is not related to its backup power pin.

DESCRIPTION

This warning indicates that the always-on library cell does not have all its signal pins related to the cell’s backup power pin. This relation is required for the tool to synthesize this cell.

WHAT NEXT

Use the target libraries that have all the always-on cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-170c (warning) Pin "%s" of the always-on library cell "%s" is

not related to a backup ground pin.

DESCRIPTION

This warning indicates that the always-on library cell does not have all its signal pins related to the cell’s backup ground pin. This relation is required for the tool to synthesize this cell.

WHAT NEXT

Use the target libraries that have all the always-on cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-171 (warning) Buffer or Inverter library cell "%s" is not in the proper PG pin format. Connecting supply nets to these cells may not be possible.

DESCRIPTION

This is a severe warning which indicates that always on cells that exist in the target libraries violate the PG pin rules. Using such cells in synthesis can cause undesirable results.

WHAT NEXT

Use the target libraries that have all the always-on cells in the correct power and ground(PG) pin format.

SEE ALSO

target_library(2)

MV-172 (information) A total of %d cases found where a retention strategy or a cell targeted for retention synthesis do not have a map_retention_cell constraint defined; %d of them have

been reported.

DESCRIPTION

This is a summary of total number of retention strategies or cells targeted for retention synthesis that do not have a **map_retention_cell** constraint defined.

WHAT NEXT

All of these violations can be viewed using the **check_mv_design -max_messages** command. Use a larger value with **-max_messages** if you are already seeing this message with the **check_mv_design** command.

SEE ALSO

set_retention(2)
map_retention_cell(2)
check_mv_design(2)

MV-173 (information) A total of %d retention cells found that do not have an associated UPF retention strategy; %d of them have been reported.

DESCRIPTION

This is a summary of total number of retention cells that do not have an associated UPF retention strategy.

WHAT NEXT

All of these violations can be viewed using the **check_mv_design -max_messages** command. Use a larger value with **-max_messages** if you are already seeing this message with the **check_mv_design** command.

SEE ALSO

set_retention(2)
check_mv_design(2)

MV-174 (information) A total of %d references to the target library cells or the library cell types have been found that do not

exist in the target libraries; %d of them have been reported.

DESCRIPTION

This is a summary of total number of references to library cells or library cell types that are not present in the target libraries. These references were set as constraints by the **map_retention_cell** command.

WHAT NEXT

All of these violations can be viewed using the **check_mv_design -max_messages** command. Use a larger value with **-max_messages** if you are already seeing this message with the **check_mv_design** command.

SEE ALSO

set_retention(2)
map_retention_cell(2)
check_mv_design(2)

MV-175 (information) A total of %d isolation cells found which do not have an associated UPF isolation strategy; %d of them have been reported.

DESCRIPTION

This is a summary of total number of isolation cells that do not have an associated UPF isolation strategy.

WHAT NEXT

All of these violations can be viewed using the **check_mv_design -max_messages** command. Use a larger value with **-max_messages** if you are already seeing this message with the **check_mv_design** command.

SEE ALSO

set_isolation(2)
check_mv_design(2)

MV-176 (warning) The operating condition of the cell "%s", under retention strategy "%s", in power domain "%s", does not

match with the operating condition of any of the retention library cells, which have been set as a mapping constraint.

DESCRIPTION

This warning indicates that the operating condition of the specified cell does not match with the operating condition of any of the retention library cells, set as a mapping constraint using the **-lib_cells** option of the **map_retention_cell** command.

WHAT NEXT

Check if at least one of the retention library cells, set as a mapping constraint, have been characterized for the required operating voltage in the target libraries/ target library subset. Also check if the correct voltage has been set for the cell which needs to be mapped. The existing operating condition for the cell can be viewed using the **report_cell** command.

SEE ALSO

set_retention(2)
set_voltage(2)
set_target_library_subset(2)
map_retention_cell(2)
report_cell(2)

MV-177 (warning) The operating condition of the cell "%s", under retention strategy "%s", in power domain "%s", does not match with the operating condition of retention library cells of type "%s".

DESCRIPTION

This warning indicates that the operating condition of the specified cell does not match with the operating condition of any of the retention library cells of the specified type, set as a mapping constraint using the **-lib_cell_type** option of the **map_retention_cell** command.

WHAT NEXT

Check if at least one of the retention library cells of the specified type, set as a mapping constraint, have been characterized for the required operating voltage in the target libraries/target library subset. Also check if the correct voltage has been set for the cell which needs to be mapped. The existing operating condition for the cell can be viewed using the **report_cell** command.

SEE ALSO

set_retention(2)
set_voltage(2)
set_target_library_subset(2)
map_retention_cell(2)
report_cell(2)

MV-178 (information) A total number of %d retention library cells and/or cell types found, whose operating conditions do not match with that of cells, on which they have been set as mapping constraints; %d of them have been reported.

DESCRIPTION

This is a summary of a total number of cases where the specified retention library cells or library cells of a specified type, have their operating conditions mismatched with the operating conditions of the cells, on which they have been set as mapping constraints, using **-lib_cells** and/or **-lib_cell_type** of the **map_retention_cell** command.

WHAT NEXT

As a result of the mismatch of the operating conditions, the cells which bear the retention library cells or library cell type constraints will not be mapped. Clear the existing mapping constraints, set the correct mapping constraints on the cell and run **compile** again to map these cells.

SEE ALSO

map_retention_cell(2)
compile(2)

MV-179 (warning) Non-technology cell pin %s will not be applied related supply nets.

DESCRIPTION

set_related_supply_net command is supported only on design ports and leaf cell pins.

WHAT NEXT

If hierarchical pins were included unintentionally in the objects, no action is

needed. The design ports and leaf cell pins specified in the object list have been applied related_supply_net attributes.

SEE ALSO

set_related_supply_net(2)

MV-180 (information) Applying related_supply_nets (power = '%s', ground = '%s') to port/pin '%s'.

DESCRIPTION

This is just an information to inform you are the set_related_supply_net setting has been applied.

WHAT NEXT

None.

SEE ALSO

set_related_supply_net(2)

MV-200 (error) No power domain definitions found in the design.

DESCRIPTION

This message is printed when power domain definitions are not found in the design. Power domains allow precise definition of operating environment and switching behavior of the design. Without power domains, certain operations, such as insertion of isolation cells, cannot be performed.

WHAT NEXT

Provide power domain definitions.

SEE ALSO

create_power_domains(2)

MV-201 (error) Usable ISO/ELS cells matching name %s could

not be found in link libraries.

DESCRIPTION

This message is displayed when ISO/ELS cells for a given name do not exist in link libraries or when cells are marked dont_use or dont_touch.

WHAT NEXT

Check link library setting. Check library cell name or remove dont_use or dont_touch attribute from library cells.

MV-202 (warning) Changes to electrical isolation between power domains modified design functionality.

DESCRIPTION

Insertion or deletion of of ISO/ELS cells modify design functionality. Formal verification may fail to compare post and pre synthesis designs.

WHAT NEXT

MV-203 (error) ISO/ELS cell %s is marked dont touch. It will not be removed.

DESCRIPTION

remove_isolation_cell command does not remove isolation cells with dont touch attribute.

WHAT NEXT

Use -force option and re-run remove_isolation_cell command.

SEE ALSO

remove_isolation_cell(2)

MV-204 (error) Cell %s is not isolation cell or enabled level

shifter. It will not be removed.

DESCRIPTION

WHAT NEXT

SEE ALSO

`remove_isolation_cell(2)`

MV-205 (error) Pin or port %s controlling enable pins of isolation cell must have output direction.

DESCRIPTION

WHAT NEXT

SEE ALSO

`insert_isolation_cell(2)`

MV-206 (warning) ISO cell was added on always on net %s.

DESCRIPTION

`This message informs that ISO cell was added on always on net.`

WHAT NEXT

SEE ALSO

`remove_isolation_cell(2)`

MV-210 (warning) Found %d incorrect instantiation(s) of level

shifters.

DESCRIPTION

This message summarizes total number of level shifters in design which do not implement correct voltage shifts. Information on individual violation can be obtained by running check_mv_design command using -verbose switch.

WHAT NEXT

Make sure reference library cell in each violation reported by check_mv_design implements voltage shift correctly.

SEE ALSO

check_mv_design(2)

MV-211 (warning) Found %d level shifter(s) with input pin fan-in logic operating at different voltages.

DESCRIPTION

This message summarizes total number of level shifters in design whose input pins are driven by cells which operate at different voltages. Information on individual violation can be obtained by running check_mv_design command using -verbose switch.

WHAT NEXT

Make sure each level shifter is driven by cells which operate at same voltage.

SEE ALSO

check_mv_design(2)

MV-212 (warning) Found %d level shifter(s) with output pin fan-out logic operating at different voltages.

DESCRIPTION

This message summarizes total number of level shifters in design which drive cells operating at different voltages. Information on individual violation can be obtained by running check_mv_design command using -verbose switch.

WHAT NEXT

Check connections and make sure level shifters drive cells which operate at same voltage.

SEE ALSO

check_mv_design(2)

MV-213 (warning) Found %d level shifter(s) not conforming to level shifter insertion strategy.

DESCRIPTION

This message summarizes total number of level shifters which do not conform to level shifter insertion strategy set by set_level_shifter_strategy command. Information on individual violation can be obtained by running check_mv_design command using -verbose switch.

WHAT NEXT

Change level shifter insertion strategy or remove appropriate level shifters from net-list.

SEE ALSO

check_mv_design(2)
set_level_shifter_strategy(2)

MV-214 (warning) Found %d pin to pin connection(s) without level shifter(s).

DESCRIPTION

This message summarizes total number pin to pin connections which require level shifters but on which no level shifters were found. Information on individual violation can be obtained by running check_mv_design command using -verbose switch.

WHAT NEXT

If you receive this warning after compile, make sure nets are not dont touched. If they are dont touched, remove dont touch attribute and recompile design. Also, make sure technology libraries have level shifters which implement appropriate level shifts. You can ignore this warning issued at the beginning of the compile. Compile

will automatically insert level shifters. Alternatively, you can insert level shifters manually by issuing insert_level_shifter command.

SEE ALSO

check_mv_design(2)
insert_level_shifter(2)

MV-215 (warning) Found %d net(s) with net drivers operating at different voltages.

DESCRIPTION

This message summarizes total number of nets in design which are driven by cells operating at different voltages. Information on individual violation can be obtained by running check_mv_design command using -verbose switch.

WHAT NEXT

Make sure each net is driven by cells which operate at same voltage.

SEE ALSO

check_mv_design(2)

MV-216 (warning) Cell %s is used to shift voltage levels %.3f->%.3f. However, its reference cell %s is designed to shift %.3f->%.3f.

DESCRIPTION

This message is printed when incorrect level shifter is instantiated to shift voltage difference between driver and load pins.

WHAT NEXT

If this level shifter is manually instantiated in the design and if it is deliberately marked as dont touch, then this message can be ignored. If this level shifter is not dont touch, then compile or insert_level_shifter command will replace it with the correct level shifter available in the library.

SEE ALSO

compile(2)
insert_level_shifter(2)

MV-217 (warning) Input pin %s of level shifter %s is driven by pins %s(%.3fV) and %s(%.3fV) which operate at different voltages.

DESCRIPTION

This message is printed when a level shifter input pin is driven by two drivers which operate at different voltages. The tool prints the first two pins that it finds. It is possible that additional pins operating at different voltages are connected to level shifter.

WHAT NEXT

Check level shifter connections.

SEE ALSO

insert_level_shifter(2)

MV-218 (warning) Output pin %s of level shifter %s drives pins %s(%.3fV) and %s(%.3fV) which operates at different voltages.

DESCRIPTION

This message is printed when a level shifter ouput pin drivs two load pins which operate at different voltages. The tool prints the first two pins that it finds. It is possible that additional pins operating at different voltages are connected to level shifter.

WHAT NEXT

Check level shifter connections.

SEE ALSO

insert_level_shifter(2)

MV-219 (warning) Level shifter %s(%.3f->%.3f) does not conform to strategy "%s".

DESCRIPTION

This message is printed when level shifter is found when it is not required based on strategy specified by set_level_shifter_strategy command was found.

WHAT NEXT

Check level shifter strategy setting. If the level shifter cell is dont touch, remove dont touch. Rerun insert_level_shifter or compile.

SEE ALSO

set_level_shifter_strategy(2)
insert_level_shifter(2)
compile(2)

MV-220 (warning) Found multi voltage net %s without level shifter. The net connects pins %s(%.3fV) and %s(%.3fV) which operate at different voltages.

DESCRIPTION

This message is printed when a multi voltage net crossing voltage boundary without level shifter is found.

WHAT NEXT

Insert level shifters using insert_level_shifter command or compile the design.

SEE ALSO

insert_level_shifter(2)
compile(2)

MV-221 (warning) Net %s is driven by pins %s(%.3fV) and

%s(%.3fV) which operate at different voltages.

DESCRIPTION

This message is printed when a net is driven by two drivers which operate at different voltages. The tool prints the first two driver pins that it finds. It is possible that additional pins operating at different voltages are connected to the net.

WHAT NEXT

Check net connections.

SEE ALSO

insert_level_shifter(2)

MV-222 (warning) Found %d pin to pin connections requiring level shifter(s) on dont touch nets.

DESCRIPTION

This message summarizes total number of pin to pin connections on dont touch nets with missing level shifters. More information on each net connection can be obtained by running check_mv_design in verbose mode.

WHAT NEXT

Use check_mv_design in verbose mode to report the details of level shifter violations. Use insert_level_shifter and/or compile to insert level shifters to remove the violations.

SEE ALSO

check_mv_design(2)
insert_level_shifter(2)
compile(2)

MV-223 (warning) Found %d violating level shifter(s) that are

marked dont touch.

DESCRIPTION

This message summarizes total number of level shifters that are marked dont touch. Tool will not be able to perform optimization of these cells. More information on each violation can be obtained by running check_mv_design in verbose mode.

WHAT NEXT

Run check_mv_design to report the details of the violations on those level shifters. In order to remove the level shifters with violations, please remove the dont_touch on the level shifters.

SEE ALSO

check_mv_design(2)

MV-224 (warning) Net %s is dont touch. Level shifter will not be added on this net.

DESCRIPTION

This message informs that level shifter cannot be added on the net because it is marked dont touch.

WHAT NEXT

SEE ALSO

MV-225 (warning) Level shifter %s is marked dont touch. It will not be optimized.

DESCRIPTION

This message informs that level shifter will not be optimized because it is marked dont touch.

WHAT NEXT

In order to enable optimization on the level shifters, remove the dont touch on

them.

SEE ALSO

MV-226 (information) Net %s is clock net which requires level shifter.

DESCRIPTION

This message informs that level shifter is required on a clock net.

WHAT NEXT

SEE ALSO

MV-227 (warning) Found clock net %s without level shifter. The net connects pins %s(%.3fV) and %s(%.3fV) which operate at different voltages.

DESCRIPTION

This message is printed when a clock net crossing voltage boundary without level shifter is found.

WHAT NEXT

Insert level shifters using insert_level_shifter command or compile the design. Check man pages of these commands on further instructions on how level shifters on clock nets can be inserted.

SEE ALSO

insert_level_shifter(2)
compile(2)

MV-228 (warning) Found %d pin to pin connections on clock

nets requiring level shifter(s).

DESCRIPTION

This message summarizes total number of pin to pin connections with missing level shifters on clock nets. More information on each connection can be obtained by running check_mv_design in verbose mode.

WHAT NEXT

Insert level shifters using insert_level_shifter command or compile the design. Check man pages of these commands on further instructions on how level shifters on clock nets can be inserted.

SEE ALSO

check_mv_design(2)
insert_level_shifter(2)
compile(2)

MV-229 (warning) Found %d pin to pin connections requiring level shifter(s).

DESCRIPTION

This message summarizes total number of pin to pin connections with missing level shifters. More information on each net connection can be obtained by running check_mv_design in verbose mode.

WHAT NEXT

Run check_mv_design in verbose mode to report more details. Run insert_level_shifter or compile the design to insert level shifters.

SEE ALSO

check_mv_design(2)
insert_level_shifter(2)
compile(2)

MV-230 (warning) Found dont touch net %s without level shifter. The net connects pins %s(%.3fV) and %s(%.3fV) which operate

at different voltages.

DESCRIPTION

This message is printed when a dont touch net crossing voltage boundary without level shifter is found.

WHAT NEXT

Remove dont touch attribute. Insert level shifters using insert_level_shifter command or compile the design.

SEE ALSO

insert_level_shifter(2)
compile(2)

MV-231 (warning) Pin '%s'(%s) cannot drive '%s'(%s) due to %s.

DESCRIPTION

This message is printed when the driver pin can not drive the load pin. The reasons are: 1) Driver pin and load pin is operating at different voltages (**set_voltage** defines the operating voltage of a supply net). 2) PST indicates that the driver pin and load pin could operate at different voltages. 3) The port states definition are incomplete. For example, port states have been defined on the supply of the driver pin but not the load pin.

WHAT NEXT

Completely define port states on supply nets if it is not done yet. Insert level shifters using **insert_level_shifter** command or **compile** the design.

SEE ALSO

insert_level_shifter(2)
compile(2)
set_level_shift_strategy(2)
set_voltage(2)

MV-232 (warning) Level shifter '%s' has violations(s): %s.

DESCRIPTION

This message is printed when a level shifter has any of the following violations. 'Floating': the input/output pin of the level shifter is not connected. 'Voltage range mismatch': the level shifter library cell cannot satisfy the voltage shifting range. 'Level shifter type mismatch': the type of the level shift library cell is incompatible with the level shifting rule defined by set_level_shift_strategy. 'Location mismatch': the location of the level shifter cannot satisfy the location requirement defined on the level shifter library cell.

WHAT NEXT

Re-insert level shifters using remove_level_shifter and insert_level_shifter commands or re-compile the design.

SEE ALSO

insert_level_shifter(2)
compile(2)
set_level_shift_strategy(2)

MV-232a (warning) Level shifter '%s' has violations(s): %s.

DESCRIPTION

This message is printed when a level shifter has 'voltage range mismatch' violation: the level shifter library cell cannot satisfy the voltage shifting range. More detail information are shown by the **report_level_shifter** command.

WHAT NEXT

Check if the voltage range defined for the level shifter library cell has covered the voltage range specified by the power state table in the design.

Re-insert level shifters using remove_level_shifter and insert_level_shifter commands or re-compile the design.

SEE ALSO

insert_level_shifter(2)
compile(2)
set_level_shift_strategy(2)
report_level_shifter(2)

MV-232b (warning) Level shifter '%s' has violations(s): %s.

DESCRIPTION

This message is printed when a level shifter has 'type mismatch' violation: the type of the level shift library cell is incompatible with the level shifting rule defined by set_level_shift_strategy. More detail information are shown by the **report_level_shifter** command.

WHAT NEXT

Check if the level shifter type defined for the level shifter library cell has covered the all possible conversion type specified by the power state table in the design.

Re-insert level shifters using remove_level_shifter and insert_level_shifter commands or re-compile the design.

SEE ALSO

report_level_shifter(2)
insert_level_shifter(2)
compile(2)
set_level_shift_strategy(2)

MV-232c (warning) Level shifter '%s' has %s violation due to location constraint.

DESCRIPTION

This message is printed when a level shifter has 'main power mismatch' violation: the location of the level shifter cannot satisfy the location requirement defined by the level shifter library cell. More detail information are shown by the **report_level_shifter** command.

WHAT NEXT

Check if the power pin with attribute of **std_cell_main_rail** is connected to the default supply of the domain where the level shifter is located at.

Re-insert level shifters using remove_level_shifter and insert_level_shifter commands or re-compile the design.

SEE ALSO

insert_level_shifter(2)

compile(2)
set_level_shift_strategy(2)

MV-232d (warning) Level shifter '%s' has violations(s): %s.

DESCRIPTION

This message is printed when a level shifter has 'Floating' violation: the level shifter is floating. More detail information are shown by the **report_level_shifter** command.

WHAT NEXT

Check the input/output connectivity of the level shifter.

Re-insert level shifters using remove_level_shifter and insert_level_shifter commands or re-compile the design.

SEE ALSO

report_level_shifter(2)
insert_level_shifter(2)
compile(2)
set_level_shift_strategy(2)

MV-232e (warning) Level shifter '%s' has violations(s): %s.

DESCRIPTION

This message is printed when a level shifter has 'Unmapped' violation: the level shifter is unmapped. More detail information are shown by the **report_level_shifter** command.

WHAT NEXT

Check if there exist level shifter libraries for mapping the level shfiter cell.

Re-insert level shifters using remove_level_shifter and insert_level_shifter commands or re-compile the design.

SEE ALSO

report_level_shifter(2)
insert_level_shifter(2)
compile(2)

MV-232f (warning) Level shifter '%s' has violations(s): %s.

DESCRIPTION

This message is printed when a level shifter has 'operating condition mismatch' violation. This violation could be caused by an mismatch between the input/output signal levels of the level shifter and operating voltages of its driver and load, or by an mismatch between the process and temperature of the level shifter and its operating environment. More detail information are shown by the **report_level_shifter** command.

WHAT NEXT

Check if the operating condition of the level shifter library cell matches the voltage specified on the supplies connected to the level shifters.

Re-insert level shifters using remove_level_shifter and insert_level_shifter commands or re-compile the design.

SEE ALSO

report_level_shifter(2)
insert_level_shifter(2)
compile(2)
set_level_shift_strategy(2)
set_voltage(2)

MV-232g (warning) Level shifter '%s' has violations(s): %s.

DESCRIPTION

This message is printed when a level shifter has 'target library subset mismatch' violation. This violation shows that the level shifter library cell doesn't belong to the target library subset defined on its parent block. More detail information are shown by the **report_level_shifter** command.

WHAT NEXT

Check if the level shifter belongs to a library that is included in the target library subset defined for the parent hiearchy for the level shifter.

Re-insert level shifters using remove_level_shifter and insert_level_shifter commands or re-compile the design.

SEE ALSO

report_level_shifter(2)
insert_level_shifter(2)
compile(2)
set_level_shift_strategy(2)
set_target_library_subset(2)

MV-232h (warning) Level shifter '%s' has violations(s): %s.

DESCRIPTION

This message is printed when a level shifter has 'no state on supply' violation. This violation shows that no valid port states have been defined on any port connected to one of the supply net of the level shifter. More detail information are shown by the **report_level_shifter** command.

WHAT NEXT

Check if the supplies of the level shifter are connected to a supply port with port states defined.

Re-insert level shifters using remove_level_shifter and insert_level_shifter commands or re-compile the design.

SEE ALSO

report_level_shifter(2)
insert_level_shifter(2)
compile(2)
set_level_shift_strategy(2)
add_port_state(2)

MV-232i (warning) Level shifter '%s' has violations(s): %s.

DESCRIPTION

This message is printed when a level shifter has 'isolation violation' This violation occurs when PST has defined a power state that the input supply of the buffer-type level shifter is off while the output supply of the buffer-type level shifter is on. More detail information are shown by the **report_level_shifter** command.

WHAT NEXT

Check if PST has defined a state where the input supply of the level shifter is off

and the output is not.

Re-insert level shifters using remove_level_shifter and insert_level_shifter commands or re-compile the design.

SEE ALSO

insert_level_shifter(2)
compile(2)
set_level_shift_strategy(2)

MV-232j (warning) Level shifter '%s' has violations(s): %s.

DESCRIPTION

This message is printed when a level shifter has 'supply not available' violation. This violation occurs when the supply of the level shifter has not been defined inside the domains of the level shifter. More detail information are shown by the **report_level_shifter** command.

WHAT NEXT

Define the supplies of the level shifter in the domain where the level shifter is located.

SEE ALSO

insert_level_shifter(2)
compile(2)
set_level_shift_strategy(2)

MV-232k (warning) Level shifter '%s' has violations(s): %s.

DESCRIPTION

This message is printed when a level shifter has 'supply undetermined' violation. This violation occurs when the supply of a level shifter is not determined. More detail information are shown by the **report_level_shifter** command.

WHAT NEXT

This warning occurs when the tool can not automatically determine the supply of the level shifter. Connecting the power pins of the level shifter to appropriate supplies would help to resolve the problem.

Re-insert level shifters using remove_level_shifter and insert_level_shifter commands or re-compile the design.

SEE ALSO

report_level_shifter(2)
insert_level_shifter(2)
compile(2)
set_level_shift_strategy(2)
connect_supply_net(2)

MV-232I (warning) Level shifter '%s' has violations(s): %s.

DESCRIPTION

This message is printed when a level shifter has 'redundant' violation. This violation occurs when the level shifter is not needed in the design. More detail information are shown by the **report_level_shifter** command.

WHAT NEXT

Check if the input and output supply of the level shifter is the same or connected.

Re-insert level shifters using remove_level_shifter and insert_level_shifter commands or re-compile the design.

SEE ALSO

report_level_shifter(2)
insert_level_shifter(2)
compile(2)
set_level_shift_strategy(2)

MV-233 (error) An off state (supply port state) has been defined on supply port %s, which is part of a ground supply network.

DESCRIPTION

You have added an off supply port state to a supply port which is part of a ground supply network. This is not allowed, because 2007.12 release does not support power switching at ground supply network.

WHAT NEXT

Re-design your supply network. Specifically, remove any off state from supply ports

that are part of any ground supply networks.

MV-234 (error) remove_upf command cannot be used once a UPF design has been compiled.

DESCRIPTION

You were trying to remove UPF constraints after the UPF design has gone through compile. This is not supported, and design compiler does not support reverting netlist changes effected by UPF constraints.

The command 'remove_upf' can only be used on a UPF design if it has not been compiled at all.

WHAT NEXT

Please fix your UPF files as needed, and reload into the original RTL netlist.

MV-235 (error) UPF/MV data '%s' cannot be retrieved because of a previous error.

DESCRIPTION

This error message indicates that other errors have occurred that prevent further progress in retrieving UPF data.

This can happen in the following cases (not exhaustive):

• You are reading a .ddc file with an incorrect library setup; for example, missing some macro cell libraries. Watch for a LINK-5 error occurring prior to this message.

• You are reading a .ddc file from IC Compiler into Design Compiler, and the .ddc file contains a PG netlist. This is currently not supported as of the C-2009.06 release.

WHAT NEXT

Fix previous errors and run the command again.

MV-236 (info) Found %d level shifter(s) inserted on power

switch sleep net.

DESCRIPTION

This message summarizes total number of level shifters which are inserted on power switch sleep net. Information on individual level shifter can be obtained by running check_mv_design command using -verbose switch.

WHAT NEXT

SEE ALSO

check_mv_design(2)

MV-240 (error) UPF power switch '%s' cannot be maintained because its %s has been deleted.

DESCRIPTION

This error message occurs because internal errors caused the removal of the UPF power switch.

WHAT NEXT

Contact your ACs if no control nets or acknowledge nets have been intentionally removed.

MV-250 (warning) Voltage Area %s has no placeable area, voltage area utilization will not be computed.

DESCRIPTION

This warning message is issued when the placeable area is 0 in the VA (voltage area), it happens because there are no free space for placement, the VA is fully ocuppied by : (1) blockages; (2) hard macros;

WHAT NEXT

Please check what fully ocuppies the VA.

SEE ALSO

create_voltage_area (2) **report_voltage_area** (2)

MV-301 (warning) Skipping power switch cell %s, no matching library pin found.

DESCRIPTION

This is related to -mode daisy in connect_power_switch command. If the given cell has multiple switch or acknowledge pins, but none matches the library pins specified by -lib_pin option, the cell is skipped for connection.

WHAT NEXT

Check the -lib_pin options and specify all the related library pins. Sometimes the object list for power switches might have more than one type of library cells. In that case all the library pins should be specified using -lib_pin option.

SEE ALSO

connect_power_switch

MV-499 (warning) A dual power always-on cell '%s' of type '%s' is used in power domain with always-on strategy of single_power.

DESCRIPTION

You receive this message when **check_connection_rules** command detects that a dual power always on cell is instantiated in shutdown power domain that requires single power cells as always-on. This is violation of always-on strategy specified on the power domains.

WHAT NEXT

Design Compiler will automatically fix this violation when design is compiled. Please compile design to eliminate this violation.

SEE ALSO

check_mv_design (2).

MV-500 (error) The support of power_domain and power_net_info is not available in current shell.

DESCRIPTION

The support of power_domain and power_net_info is limited to some tools such as IC Compliler and Design Compiler. This message is printed when power_domain or power_net_info objects are to be created in a shell not supporting them.

WHAT NEXT

Use a product/shell supporting power_domain/power_net_info. For example, IC Compiler or Design Complier.

SEE ALSO

create_power_domain(2)
create_power_net_info(2)

MV-501 (error) Failed to load voltage area %s because no cell is associated with it.

DESCRIPTION

This error occurs when there is a voltage area in Milkyway database, but no cell is associated with it.

WHAT NEXT

Check the tool/script that generated the Milkyway database. Or re-create the voltage area using create_voltage_area command.

SEE ALSO

create_voltage_area(2)

MV-502 (error) Consistency check between power domains and

voltage areas failed.

DESCRIPTION

This error message occurs when the matching between power domains and voltage areas failed. For a design with both voltage areas and power domains, there should be one voltage area with the same name for each power domain (except the top power domain) and vice versa. And the matching voltage area and power domain should also include the same set of hierarchical cells.

WHAT NEXT

Check voltage areas and power domains in the design and make them consistent.

SEE ALSO

report_voltage_area(2) report_power_domain(2)

MV-503 (error) Power net hookup for power domains is not specified properly.

DESCRIPTION

This error occurs when the tool cannot get the required power net hookup information for power domains. It may due to the following issues:
• A power domain does not have primary power/ground net.
• A power net info object does not have a power/ground net with same name in the netlist.

WHAT NEXT

Hookup primary power/ground connections for all power domains. Make sure each power net info object have a matching power/ground net with same name in the design. If the auto-hookup for tie-off cells is not needed, this requirement can be waived by using variable **mv_enable_power_domain_power_net_check**.

SEE ALSO

connect_power_domain(2) connect_pg_net(2) connect_logic_zero(2) connect_logic_one(2) mv_enable_power_domain_power_net_check(3)

MV-504 (warning) Tie high/low pin %s of always-on cell %s is

connected to power/ground net %s.

DESCRIPTION

This messages is printed when an always-on cell has an input pin tied to logic constant and a power/ground net is connected to the pin.

SEE ALSO

create_power_domain (2) **create_power_net_info** (2) **connect_power_domain** (2) **connect_logic_one(2) connect_logic_zero(2)**

MV-505 (warning) Tie high/low pin %s of cell %s is connected to power/ground net %s other than the primary power/ground net %s of its power domain.

DESCRIPTION

This messages is printed when a power/ground net is used for a tie-high/low connection, and the power/ground net is not the primary power/ground net of the cell’s power domain. This happens often on cells with special and/or mutliple power connections, such as always-on cells, retention registers, macros, etc.

SEE ALSO

create_power_domain (2) **create_power_net_info** (2) **connect_power_domain** (2) **connect_logic_one(2) connect_logic_zero(2)**

MV-506 (warning) Power/ground net %s connected to logic constant pin %s of cell %s does not match the cell’s power connection.

DESCRIPTION

This messages is printed when the power/ground net connected to a tie off pin is not the same net derived based power connections of the cell’s power domain.

WHAT NEXT

Check whether the tie high/low connection is correct. If not, fix it automatically

using commands **connect_logic_one -reconnect_all**, **connect_logic_zero -reconnect_all**; or perform manual connection through command **connect_pg_net**.

SEE ALSO

connect_logic_one(2) connect_logic_zero(2) connect_pg_net(2) create_power_domain (2) **create_power_net_info** (2) **connect_power_domain** (2)

MV-507 (warning) The power domain %s has an associated voltage area. This association will be lost after removal of the power domain.

DESCRIPTION

This message is printed when a power domain being removed using **remove_power_domain** command has an associated voltage area. It is recommended to also remove the associated voltage areas and have a consistent design information.

WHAT NEXT

Remove the associated voltage area using **remove_voltage_area** command.

SEE ALSO

create_power_domain (2) **remove_power_domain** (2) **create_voltage_area** (2) **remove_voltage_area** (2)

MV-508 (error) Power pins in logical lib_cell %s (linked to cell %s) do not match with power pins in the corresponding FRAM lib_cell.

DESCRIPTION

This messages is printed when the power pin information in logical lib_cell does not match with that in the corresponding FRAM lib_cell.

WHAT NEXT

Check whether the logical lib_cell and the corresponding FRAM lib_cell have same number of power pins, the power pins have same names, and a power pin with the same name have the same power/ground type.

SEE ALSO

check_mv_design(2)

MV-509 (error) Total %d logical lib_cell(s) used in the design have power pins not matching with the corresponding FRAM lib_cell(s).

DESCRIPTION

This messages is printed when the power pin information in one or more logical lib_cells do not match with that in the corresponding FRAM lib_cells.

WHAT NEXT

Use **check_mv_design -power_net -verbose** to print out the lib_cells having inconsistent power pin information.

SEE ALSO

check_mv_design(2)

MV-510 (warning) Power connection/checking is skipped for %d power pins because the required power pin information cannot be found in logical libraries.

DESCRIPTION

This messages is printed when one or more logical lib_cells do not have power pin information.

WHAT NEXT

Get detail information on lib_cells without power pins using **check_mv_design -power_net -verbose**, and switch to logical libraries with power pins.

SEE ALSO

check_mv_design(2)

MV-511 (warning) Total %d power pin(s) are found having connections inconsistent with their power domain(s).

DESCRIPTION

This messages is printed when there are one or more power pins whose existing connection is inconsistent to power domain connection.

WHAT NEXT

Get detail information on these power pins using **check_mv_design -power_net -verbose**.

SEE ALSO

check_mv_design(2) connect_power_net_info(2) create_power_domain(2) connect_power_domain(2) auto_connect_pg_nets(2)

MV-512 (warning) Logical lib_cell %s (linked to cell %s) does not have power/ground pin definition.

DESCRIPTION

This messages is printed when the logical lib_cell do not have power pin information. The automatic power connection and checking may not work for cells using the lib_cell.

WHAT NEXT

Switch to logical libraries with power pins.

SEE ALSO

check_mv_design(2)

MV-513 (warning) Isolation cell %s connecting pin %s (related supply net %s) and %s (related supply net %s) may be redundant. Supply net %s is more always on or equal always on

to supply net %s.

DESCRIPTION

This is message is printed when isolation cell is found on a signal path that does not require isolation cell. Isolation cell is required to isolate signal path only if domain of the driver pin is less always on than domain of the load pin. When the tool determines that domain of the driver pin is equal to or more always on than the domain of the load pin, then it considers isolation cell as redundant and issues the message.

EXAMPLES

Let us consider design with following power state table. PORT1, PORT2 and PORT3 are supply ports connected to 0.7V supply. These ports also have off state informing the tool that domain connected to ports can switch off. Lets assume, VDD_1, VDD_2 and VDD_3 are connected to PORT1, PORT2 and PORT3, respectively.

```
add_port_state -state {s_off off} -state {s0.7 0.7} PORT1
add_port_state -state {s_off off} -state {s0.7 0.7} PORT2
add_port_state -state {s_off off} -state {s0.7 0.7} POST3
create_pst pst_table -supplies {PORT1 PORT2 PORT3}

add_pst_state -pst pst_table -state  {s0.7 s0.7 s_off} state1
add_pst_state -pst pst_table -state  {s0.7 s0.7 s0.7} state2
add_pst_state -pst pst_table -state  {s_off s_off s_off} state3
```

Now let us consider ISO cell ISO_CELL1 connected between driver and load pins two gates, G1 and G2. Also consider that power pin of G1 is connected to PORT1 supply port and power pin of G2 is connected to supply port PORT2. From state1 and state2 of the power state table, it is evident that PORT1 is equal always on to PORT2. That means G1 and G2 are in operation or switched off simultaneously. The tool will detect this and inform that ISO_CELL1 may not be required.

Warning: Isolation cell ISO_CELL1 connecting pin G1/Q (related supply net VDD_1) and G2/A (related supply net VDD_2) may be redundant. Supply net VDD_1 is more always on or equal always on to supply net VDD_2. (MV-513)

Now let us consider ISO cell ISO_CELL2 connected between driver and load pins two gates, G3 and G4. Also consider that power pin of G3 is connected to PORT1 supply port and power pin of G4 is connected to supply port PORT3. From state1 and state3 of the power state table, it is evident that PORT1 is more always on to PORT3. That means G3 is always in operation when G4 is in operation (but not the other way). The tool will detect this and inform that ISO_CELL2 may not be required.

Warning: Isolation cell ISO_CELL2 connecting pin G3/Q (related supply net VDD_1) and G4/A (related supply net VDD_3) may be redundant. Supply net VDD_1 is more always on or equal always on to supply net VDD_3. (MV-513)

WHAT NEXT

Check power state table table and ensure always on relationship between supply nets

is correctly specified.

SEE ALSO

create_pst(2)
add_port_state(2)
report_pst(2)

MV-514 (warning) Power state of driver pin %s (related supply net %s) is less always on or unrelated to power state of load pin %s (related supply net %s). Isolation cell is required on net %s connecting these pins.

DESCRIPTION

This message occurs when a net without an isolation cell is found. The isolation cell is required to isolate the signal path if the domain of the signal's driver pin is *less always on* or *unrelated* to the domain of the signal's load pin. When the tool determines that the domain of the driver pin is *less always on*, or *unrelated* compared to the domain of the load pin, then it considers a need for the isolation cell and issues the warning message.

EXAMPLES

Let us consider design with following power state table. PORT1, PORT2 and PORT3 are supply ports connected to 0.7V supply. These ports also have off state informing the tool that domain connected to ports can switch off. Lets assume, VDD_1, VDD_2 and VDD_3 are connected to PORT1, PORT2 and PORT3, respectively.

```
add_port_state -state {s_off off} -state {s0.7 0.7} PORT1
add_port_state -state {s_off off} -state {s0.7 0.7} PORT2
add_port_state -state {s_off off} -state {s0.7 0.7} POST3
create_pst pst_table -supplies {PORT1 PORT2 PORT3}

add_pst_state -pst pst_table -state  {s0.7 s_off s0.7} state1
add_pst_state -pst pst_table -state  {s0.7 s_off s_off} state2
add_pst_state -pst pst_table -state  {s_off s0.7 s_off} state3
```

Now let us consider a net N1, between two gates, G1 and G2. Also consider that power pin of G1 is connected to PORT1 supply port and power pin of G2 is connected to supply port PORT2. From state3 of the power state table, it is evident that PORT1 is less always on than PORT2. That means G1 can switch off when G2 is in operation. The tool will detect this and indicate the need of isolation cell on net N.

Warning: Power state of driver pin G1/Q (related supply net VDD_1) is less always on or unrelated to power state of load pin G2/A (related supply net VDD_2). Isolation cell is required on net N1 connecting these pins. (MV-514)

Now let us consider a net N2, between two gates, G3 and G4. Also consider that power pin of G3 is connected to PORT2 supply port and power pin of G4 is connected to supply port PORT3. From state1 and state3 of the power state table, it is evident that PORT2 and PORT3 do not have specific always on relationship. That is, their switching behavior is unrelated. That means G3 can switch off when G4 is in operation and vice a versa. The tool will detect this and indicate the need of isolation cell on net N2.

Warning: Power state of driver pin G3/Q (related supply net VDD_2) is less always on or unrelated to power state of load pin G4/A (related supply net VDD_3). Isolation cell is required on net N2 connecting these pins. (MV-514)

WHAT NEXT

This is only a warning message. No action is required.

However, if the results are not what you intended, check the power state table and ensure the *always on* relationship between supply nets are correctly specified. Correct errors if needed, or insert the isolation cell and run the command again.

SEE ALSO

create_pst(2)
add_port_state(2)
report_pst(2)

MV-515 (error) Following %d regular cell(s) on always-on path(s) is(are) having no corresponding always-on power guide(s). It will cause always-on legality violation.

DESCRIPTION

This messages is printed when the always-on paths contains one or more regular single-powered cells but there exists no corresponding always-on power_guide.

WHAT NEXT

Set always-on power guides inside the relevant voltage area.

SEE ALSO

set_power_guide(2)

MV-516 (warning) Found two back to back connected isolation

cells %s and %s with same enable signals and connected to equivalent power supply network. One of the isolation cells may be redundant.

DESCRIPTION

This message is printed when tool detects two isolation cells with same enable signal and connected to equivalent power supply.

WHAT NEXT

Remove one of the isolation cells.

SEE ALSO

MV-517 (warning) Found %d isolation cell(s) whose power on state is less always on or unrelated to the power on state of domain connected to its output pin.

DESCRIPTION

This message summarizes number of isolation cells with improper power supply connection.

WHAT NEXT

Please run command **check_mv_design** in verbose mode for details.

SEE ALSO

check_mv_design (2).

MV-518 (error) Supply nets connected together cannot have different operating voltages.

DESCRIPTION

This error message occurs when you attempt either of the following actions:

• Connect two groups of supply nets that are currently operating at different voltages.

• Specify different operating voltages on supply nets that are connected together as a group.

WHAT NEXT

Respecify the operating voltages on the supply nets so that all supply nets connected together as a group operate at the same voltage.

MV-519 (error) Cannot insert an isolation cell on net %s connected to pin %s.

DESCRIPTION

This error message occurs when the **insert_isolation_cell** command cannot insert an isolation cell on the specified net.

The tool cannot insert an isolation cell when it encounters any of the following conditions:

• The isolation cell reference is not characterized to the operating condition specified on the net’s subdesign.

• The isolation cell does not exist in the target library subset specified on the net’s subdesign.

• The net has multiple drivers or it is connected to an I/O driver.

• The net is set as dont_touch or always on.

• The net has load pins operating at multiple voltages.

WHAT NEXT

Run the **insert_isolation_cell -verbose** command on the error nets for more information. After making any necessary changes, run the command again.

SEE ALSO

insert_isolation_cell(2)

MV-520 (warning) On state of isolation cell output pin %s (related supply net %s) is less always on or unrelated to the on state of pin %s (related supply net %s). Signal path through net %s from pin %s to pin %s may be broken when isolation cell gets turned off.

DESCRIPTION

This message is printed when tool detects the on state of isolation cell output pin is less always on compared to on state of load pin driven by isolation cell. The message is also printed when these two pins have undefined always on relationship. If isolation cell looses power when the domain that it is isolating is in operation, the it is possible for isolation cell's floating output pin to drive logic that is powered on. This may cause unexpected consequences.

EXAMPLES

Let us consider design with following power state table. PORT1, PORT2 and ISO_PORT are supply ports connected to 0.7V supply. These ports also have off state informing the tool that domain connected to ports can switch off. Lets assume, VDD_1, VDD_2 and VDD_ISO are connected to PORT1, PORT2 and PORT_ISO, respectively.

```
add_port_state -state {s_off off} -state {s0.7 0.7} PORT1
add_port_state -state {s_off off} -state {s0.7 0.7} PORT2
add_port_state -state {s_off off} -state {s0.7 0.7} ISO_PORT
create_pst pst_table -supplies {PORT1 PORT2 ISO_PORT}

add_pst_state -pst pst_table -state  {s0.7 s0.7 s_off} state1
add_pst_state -pst pst_table -state  {s0.7 s0.7 s0.7} state2
add_pst_state -pst pst_table -state  {s_off s0.7 s0.7} state3
```

Let us consider that ISO cell "iso" connects driver and load pins of two gates G1 and G2. Let us also consider that power pins of G1 and G2 are connected to supply ports PORT1 and PORT2 respectively. Cell iso is required since PORT1 is less always on than PORT2 which is evident from state1 and state2 of the power state table. Let us consider that ISO_PORT is connected to isolation power supply of "iso". Looking at state1 of the power state table, it is evident that ISO_PORT is less always on than PORT2. This can result in output of "iso" to switch off when gate G2 is in operation. Tool detects this condition and issues message.

On state of isolation cell output pin iso/DO (related supply net ISO_VDD) is less always on or unrelated to the on state of pin G1/A (related supply net VDD2). Signal path through net N from pin iso/DO to pin G/A may be broken when isolation cell gets turned off. (MV-520)

WHAT NEXT

Check power state table table and ensure always on relationship between supply nets

is correctly specified.

SEE ALSO

create_pst(2)
add_port_state(2)
add_pst_state(2)
report_pst(2)

MV-521 (warning) Found %d always on cell(s) without supply connections.

DESCRIPTION

This warning message advises you of the number of always on cells for which the tool cannot determine the power connections.

WHAT NEXT

This is only a warning message. No action is required.

However, to obtain more information, run the **check_mv_design** command with the **-verbose** option.

SEE ALSO

check_mv_design(2)

MV-522 (warning) Found cell %s with missing supply connection. The cell is on always on path ending at %s pin(s).

DESCRIPTION

This message is printed when tool could not derive power connection for cells on always-on path. To connect power for always on cells, the tool first determines the supply net of the always on anchor pin such as enable pin of isolation cell or control pins of retention register. It then uses the supply net to connect power pins of always on cells. Such power hookup ensures that always on path is in operation as long as control pin is operation.

WHAT NEXT

You can take one or more of the following steps to debug the power connections.

1. Use net-list traversal commands to determine the always on anchor pins driven by the output of the cell with missing connection. Few always on anchor pin are printed in the message.

2. By inspecting UPF file, identify related supply net of the always on anchor pin.

3. Make sure the supply net is available in the cell’s parent domain. If the supply net is not available, then use -reuse switch of create_supply_net command to declare the availability of the net.

4. Check if cell drives multiple always on anchor pins with different supply nets.

5. Check if the cell will missing connection is linked to a library that is characterized for voltage other than always on anchor pin’s related supply. This can happen if cell is inserted on always on path to fix functionality violations and when domain’s primary supply voltage is different than always on anchor pin’s supply voltage. The functionality violations are fixed when identical power management cell is not available and sense specification on control pin requires insertion of inverter on AO net.

SEE ALSO

all_fanout(2)
all_fanin(2)
create_supply_net(2)
set_isolation_control(2)
set_retention_control(2)

MV-523 (error) Operating voltages (max=%.2f, min=%.2f) mismatch the power states of supply net %s.

DESCRIPTION

The operating voltages of a supply net must be within the voltage range of a power state of the supply net

WHAT NEXT

set an appropriate voltage on the supply net by set_voltage.

SEE ALSO

set_voltage

MV-524 (warning) %d more volatge mismatches in power

domain but detail not reported as (MV-523).

DESCRIPTION

This warning message is printed when there are more MV-523 errors but the check_mv_design command does not report their details.

WHAT NEXT

Increase the maximum number of error messages in command check_mv_design to see the detailed MV-523 error reporting.

SEE ALSO

MV-525 (warning) Some level shifters without voltage ranges defined are not used in automatic insertion.

DESCRIPTION

This warning message is printed when some level shifter library cells are not qualified for automatic level shifter insertion because no voltage ranges are defined on these cells.

WHAT NEXT

Define voltage ranges to all level shifter library cells, or set variable mv_default_level_shifter_voltage_range_infinity to be true.

SEE ALSO

MV-526 (error) %s specification is not allowed on %s.

DESCRIPTION

This warning message is printed when multi voltage constraint is specified on synthetic cell or pin of the synthetic cell.

WHAT NEXT

Group cell into a separate hierarchy and specify multi voltage cell on newly created cell or pin of the newly created cell.

SEE ALSO

group(2)

MV-527 (warning) Non UPF isolation cell found UPF net-list. Cell %s will be treated as standard cell.

DESCRIPTION

This message is printed when tool detects user instantiated ISO cells in the UPF design. When user instantiated ISO cells are found, tool does not understand how to connect these cells to power supply. Therefore, tool implicitly connects power pins of such cell to primary supply nets of the domain.

WHAT NEXT

If technology ISO cell is instantiated, provide exception connections. Otherwise, use UPF commands to insert ISO cells in design.

SEE ALSO

set_isolation (2)
set_isolation_control (2)

MV-528 (warning) %d non UPF isolation cell found UPF net-list, they will be teated as standard cells.

DESCRIPTION

This message summarizes total number of non UPF isolation cells found in the UPF net-list.

WHAT NEXT

SEE ALSO

MV-529 (warning) Found unused power management cell %s.

DESCRIPTION

This message is printed when unused power management cell is found in the design.

WHAT NEXT

Remove cell from the design.

SEE ALSO

MV-530 (warning) Found %d unused power management cells in the design.

DESCRIPTION

This message summarizes total number of unused power management cells in the design.

WHAT NEXT

SEE ALSO

MV-531 (warning) Cannot complete tie-off re-connection for pin '%s' due to failure of getting the proper power/ground net.

DESCRIPTION

The warning message is issued in re-connection of tie-high/low pins to proper power/ground net. The power/ground net can either derived from UPF or non-UPF power intention or from power connection in the Milkway database depending on the mode specified in connect_logic_one/connect_logic_zero commands. The tie-off reconnection of a tie-off pin will be skipped if the tool failed to derive the power/ground net.

WHAT NEXT

SEE ALSO

connect_logic_one(2)
connect_logic_zero(2)

MV-532 (error) Load pins of hierarchical tie-off pin %s requires conflicting P/G nets; for example, load pin %s requires P/G net %s, while load pin %s requires P/G net %s.

DESCRIPTION

This error happens when the multiple load pins of a hierarchical tie-off pin have conflicting P/G net requirement. When a hierarchical signal pin is connected to logic constant or P/G nets, the hierarchical pin together with its load nets and load pins become a hierarchical tie-off net. All load pins of a hierarchical tie-off net need to be connected to the same power or ground net finally because they are all driven by one hierarchical pin and the pin can be driven by only one P/G net. In multi-voltage designs, different tie-off pins may require different P/G nets, depending on their voltage areas, power domains, or P/G pins' power connections. Therefore, a hierarchical tie-off net will get this error when not all its load pins require the same P/G net. This typically happens for hierarchical tie-off nets crossing multiple voltage areas and/or power domains. The error needs to be fixed by users through manual netlist editing to break such a hierarchical tie-off net, such that all load pins of each hierarchical tie-off net need the same P/G net. Reporting commands **all_fanin** and **all_fanout** can be used to trace the connections of a hierarchical tie-off net.

WHAT NEXT

SEE ALSO

connect_logic_one(2)
connect_logic_zero(2)
all_fanin(2)
all_fanout(2)

MV-533 (warning) The P/G nets '%s/%s' of cell %s is not the same as '%s/%s' of driver cell %s on tie net %s.

DESCRIPTION

This messages is printed when there are cells using different power/ground nets

found on the tieoff net.

WHAT NEXT

SEE ALSO

MV-506

MV-534 (information) Isolation cell %s is NOT redundant (required by some of its connection(s)), but it’s not required for the connection(s): %s.

DESCRIPTION

This is message is printed when part of isolation cell’s connections require to be isolated but some are not. Isolation cell is required to isolate signal path only if domain of the driver pin is less always on than domain of the load pin.

EXAMPLES

Let us consider design with following power state table. PORT1 and PORT2 are supply ports connected to 0.7V supply. These ports also have off state informing the tool that domain connected to ports can switch off. Lets assume, VDD_1, VDD_2 are connected to PORT1 and PORT2 respectively.

```
add_port_state -state {s_off off} -state {s0.7 0.7} PORT1
add_port_state -state {s_off off} -state {s0.7 0.7} PORT2
create_pst pst_table -supplies {PORT1 PORT2}

add_pst_state -pst pst_table -state  {s0.7 s_off} state1
add_pst_state -pst pst_table -state  {s0.7 s0.7} state2
```

Now let us consider ISO cell ISO_CELL1 connected between one driver pin DRV/Q and two load pins LOAD_1/A and LOAD_2/B. Also consider that power pin of DRV is connected to PORT1 supply port, power pin of LOAD_1 is connected to supply port PORT2 and power pin of LOAD_2 is connected to supply port PORT1 (same as DRV). From state1 and state2 of the power state table, it is evident that PORT1 is less always on to PORT2. That means the connection between DRV and LOAD_1 needs to be isolated, so ISO_CELL1 is NOT redundant. But since DRV and LOAD_2 are connected to the same supply port, this connection is NOT required to be isolated.

```
Information: Isolation cell ISO_CELL1 is NOT redundant (required by some of its
connection(s)), but it’s not required for the connection(s): DRV/Q (related supply
net (VDD_1,VSS)) and LOAD_2/B (related supply net (VDD_1,VSS)). (MV-534)
```

WHAT NEXT

Check how the isolation cells were inserted.

SEE ALSO

MV-513(n)
create_pst(2)
add_port_state(2)
report_pst(2)

MV-535 (error) Cannot connect net %s to tie-off pin %s due to name conflicts.

DESCRIPTION

This messages is printed when derive_pg_connection -tie cannot connect the tie off pin to the power and ground net because the net already exists in the logical hierarchy but it is not power/ground type or not connected to the pg network.

WHAT NEXT

Check and verify the net connections

SEE ALSO

all_fanin(2) all_fanout(2)

MV-566 (error) set_related_supply_net cannot apply onto this hierarchical pin%s because it is not on a power domain boundary.

DESCRIPTION

This error happens when set_related_supply_net is applied onto a hierarchical pin. And this hierarchical pin is not on a power domain boundary. set_related_supply_net on hierarchical pins are only supported when they are on power domain boundary.

WHAT NEXT

SEE ALSO

MV-596 (error) The primary %s net of power domain %s is not defined.

DESCRIPTION

The message is printed when a power domain's primary power net or primary ground net is not defined. In UPF mode, use set_domain_supply_net to set the primary nets. In non-UPF mode, use connect_power_domain command.

SEE ALSO

report_power_domain (2)
set_domain_supply_net (2)
connect_power_domain (2)

MV-597 (warning) Total %d logical library cell(s) used in the design do not have power/ground pins.

DESCRIPTION

The message is printed when some logical library cells do not have power pins.

WHAT NEXT

The detail list of these library cells can be shown using **check_mv_design -power_net -verbose**.

SEE ALSO

check_mv_design(2)

MV-598 (warning) Auto derivation of P/G nets for %d P/G pins

failed.

DESCRIPTION

The tool failed to derived proper P/G nets for some power pins. To check the detail information of the power pins and the failure reasons, use **check_mv_design -power_net -verbose**.

SEE ALSO

derive_pg_connection(2)
check_mv_design(2)

MV-599 (warning) Auto derivation of P/G nets skipped for %d P/G pins on physical only cells.

DESCRIPTION

Auto P/G derivation does not work on physical only cells. So the related functions such as **derive_pg_connection** will sikp these P/G pins.

WHAT NEXT

Please run command **check_mv_design -verbose** for details.

SEE ALSO

derive_pg_connection(2)
check_mv_design(2)

MV-600 (error) Failed to transfer %s to MW database.

DESCRIPTION

This error occurs when the tool failed to tranfer the specific object/constraint into to MW database.

WHAT NEXT

If the design is loaded through DDC format, check the tool/script that generated the DDC file. Or re-create the object(s)/contraint(s).

MV-601 (error) Supply net %s and its connected supply net(s) are used as both power net and ground net.

DESCRIPTION

This error occurs when a supply net and its connected supply_nets through supply ports or power switches are used as power net for some power domain(s) or domain element(s), but also as ground net for some other power domain(s) or domain element(s).

WHAT NEXT

Check all UPF connections and constraints using this supply net and its connected supply nets, and make sure they are all used only as power net or only as ground net.

SEE ALSO

set_domain_supply_net(2) connect_supply_net(2) set_isolation(2) set_retention(2) create_power_switch(2)

MV-602 (error) %s is supported only in UPF shell mode.

DESCRIPTION

This error message occurs because the specified command/option is supported only in upf_mode.

WHAT NEXT

Rerun the command using UPF shell mode, or remove the unsupported command/option.

MV-603 (warning) No matching lib cell between voltage %f - %f.

DESCRIPTION

The command insert_level_shifter could not find any library cell that is characterized for the specified voltage range.

WHAT NEXT

You can try -verbose options to check which cells are being identified by the

command as a proper candidates.

SEE ALSO

check_mv_design(2)

MV-604 (error) The coordinate [%g %g] of voltage area '%s' is outside the die area.

DESCRIPTION

The voltage area is defined outside of the die area which is not supported.

WHAT NEXT

Redefine the voltage area coordinates.

SEE ALSO

create_voltage_area(2)

MV-605 (error) Could not derive boundary for default voltage area.

DESCRIPTION

The tool failed to find adequate space in the floorplan for the default voltage area needed by the tool.

WHAT NEXT

Modify the floorplan to allow creation of default voltage area.

SEE ALSO

create_voltage_area(2)

MV-606 (error) The specified voltage area is overlapping with

voltage area ’%s’.

DESCRIPTION

The tool has detected overlapping voltage area partitions which is not supported.

WHAT NEXT

Modify the voltage area boundaries to remove the overlap.

SEE ALSO

create_voltage_area(2)

MV-607 (error) Found mismatch between voltage area %s and its corresponding power domain %s .

DESCRIPTION

This error occurs a voltage area and its corresponding power domain are not defined on the same set of cells.

WHAT NEXT

Check the voltage area and power domain definition, and make sure they are defined on the same set of cells

SEE ALSO

create_power_domain(2) create_voltage_area(2) report_power_domain(2) report_voltage_area(2)

MV-608 (error) Failed to get the matching power domain for voltage area %s.

DESCRIPTION

For a non-default voltage area, the error happens when the power domain with the same name as the voltage area is not defined. For the DEFAULT_VOLTAGE_AREA, the error happens when the top level power domain is not defined.

WHAT NEXT

Check the voltage area and power domain definition, and make sure each voltage area has a corresponding power domain.

SEE ALSO

create_power_domain(2) create_voltage_area(2) report_power_domain(2) report_voltage_area(2)

MV-609 (error) Failed to get the matching voltage area for power domain %s.

DESCRIPTION

The error happens when the voltage area with the same name as a non-top-level power domain is not defined.

WHAT NEXT

Check the power domain and voltage area definition, and make sure each non-top-level power domain has a corresponding voltage area.

SEE ALSO

create_power_domain(2) create_voltage_area(2) report_power_domain(2) report_voltage_area(2)

MV-610 (info) Needs level shifters %s from %s to %s. No suitable library cells are found.

DESCRIPTION

This messages shows that certain level shifters are needed to be inserted on a particular net or replace an isolation (or enabled level shifter) cell. Adding suggested level shifters to the library is one way (but not the only way) to help the tool to eliminate voltage violations on the global net to which the target net/cell belongs. This message is followed by the reasons why level shifters in current libraries can not be used.

The following factors are considered for level shifter insertion: functionality, target library (subset), input/output signal level, level shifter type, input/output voltage range, and standard cell main power setting.

WHAT NEXT

Add qualified level shifter cells to the library and/or making more power nets (in power domain or UPF designs) available for level shifters.

SEE ALSO

MV-611 (warning) %d nets required level shifters but matching level shifters were not found.

DESCRIPTION

This warning message shows the total number of global nets which requires level shifters but no suitable level shifters can be found in the library. In general, to successfully insert level shifter, all conditionals including level shifter type, operating conditions, target library subset, standard cell main power setting, input/output_voltage_range, and availablility of supply nets should be satsified. If it is possible, information message **MV-753** would be shown to identify the root cause. Otherwise, setting variable **mv_insert_level_shifter_verbose** to be **true** could also help to find the exact reason(**MV-610**) why level shifters could not be inserted.

WHAT NEXT

Use **check_mv_design -level_shifters -verbose** to display the required level shifters on each net. In particular, MV-231 would be found to describe the pin-to-pin voltage shifting violations if no level shifters could be found to fix the violations.

Follow MV-753 and MV-610 to ensure that appropriate level shifters could be inserted to fix existing level shifter violations in the design.

SEE ALSO

report_level_shifter(2)
insert_level_shifter(2)
compile(2)
set_level_shift_strategy(2)
MV-753(n)
MV-610(n)

MV-612 (warning) %d nets required level shifters but was

ignored.

DESCRIPTION

This warning message shows the total number of global nets which require level shifters, but are considered ineligible for level shifter insertion and ignored.

WHAT NEXT

Use 'check_mv_design -level_shifters -verbose' to show why the nets are not eligible for level shifter insertion.

SEE ALSO

MV-613 (warning) The global net driven by pin %s is ineligible for level shifter insertion %s.

DESCRIPTION

This warning message shows why a global net is not eligible for level shifter insertion.

WHAT NEXT

SEE ALSO

MV-614 (warning) %d nets has level shifter constraints but no level shifters are inserted.

DESCRIPTION

This warning message shows the total number of global nets which have level shifter strategy (constraints) defined but no violations are found. No level shifters are inserted to these nets.

WHAT NEXT

SEE ALSO

MV-616 (warning) Some nets (ports) in the global net driven by pin %s is not allowed for level shifter insertion.

DESCRIPTION

The message states that some ports of a global net are not allowed for level shifter insertion, which could be caused by dont_touch, special handling of clock net, and no_shift level shifter strategy. This could make it more difficult to find a solution for level shifter insertion on the global net.

WHAT NEXT

SEE ALSO

MV-617 (warning) large distance (%d) between components %d and %d may stop the proper buffering on paths between them.

DESCRIPTION

The message is printed when large distances are found in disjoint VA design.

In disjoint VA design, if a distance between two disjoint components is too large, QoR issues might be caused in place and route phase. In pre-place phase, ICC will try to find and report such components so that user can adjust the design floorplan in early phase.

By default, the tool will use value defined by set_max_net_length as threshold to analyze the large distances. If the value is not defined, a threshold based on the buffer features used by current design will be derived.

The disjoint voltage area analysis can be triggerd by **check_physical_design -phase pre_place_opt** .

WHAT NEXT

User should try to adjust the large voltage areas by put them closer to avoid this warning.

SEE ALSO

check_physical_design(2)

MV-618 (info) found %d disjoint voltage areas.

DESCRIPTION

This message is triggered by check_physical_constraint when disjoint voltage areas are found. All disjoint voltage areas will be shown.

The distance of any two disjoint components in a disjont va will be checked. If the distance is potentially large to impact buffering, warning message **MV-617** will be given.

WHAT NEXT

SEE ALSO

MV-617

MV-619 (information) %d nets are partially resolved.

DESCRIPTION

This messages gives the total number of nets partially resolved for level shifter violations. This is the number of nets that could not be completed fixed for level shifter violations, but some level shifters are inserted to resolve subtrees rooted at isolation cells. These subtrees can only be rooted at isolation cells as isolation cell output power is fixed as specified in **set_isolation** command.

WHAT NEXT

This is an information only message. Please use check_mv_design to investigate why global net could not be completely resolved

SEE ALSO

check_mv_design(n)

MV-627 (error) Supply net %s and %s are connected to the same power switch %s, but they have been used as different

power/ground types.

DESCRIPTION

This error message occurs when there are supply nets of different power or ground types, as used in other commands, being connected to the same power switch. A power switch is used to switch either the power, or the ground network, but not a mixture of both.

WHAT NEXT

Check all UPF connections and constraints using the specified supply net and its connected supply nets, and make sure they are all used only as a power net or only as a ground net.

SEE ALSO

connect_supply_net(2)
create_power_switch(2)
set_domain_supply_net(2)
set_isolation(2)
set_retention(2)

MV-750 (error) The point with coordinate %s is not in voltage area %s.

DESCRIPTION

This error occurs when a point which is supposed to be inside the given voltage area, is not inside.

WHAT NEXT

Check the point’s coordinate and voltage area boundary

MV-751 (information) Apply operating condition %s (voltage = %s, process = %f, temperature = %f) to cell %s.

DESCRIPTION

This information message happens when an operating condition is automatically applied to a cell. For each type of operating condition at most 10 messages are

allowed by default. Variable **mv_max_auto_opcond_message** can be used to change the total number of allowed messages.

WHAT NEXT

The automatic application of opcond could have eliminated some MV-001 errors shown previously. Please use check_mv_design to display the updated list of MV-001 errors.

If the automatically applied operating condition is not desired, use **set_operating_conditions** to prevent the automatical application of operating conditions by the tool.

SEE ALSO

set_operating_conditions(2)

MV-752 (information) No port state has been defined. Level shifter insertion is based on operating voltages.

DESCRIPTION

This information message happens when no port state has been defined on any port of the design. Under this circumstances, level shifters are inserted with only consideration of operating voltages defined by **set_voltage** or operating conditions defined by **set_operating_conditions**.

WHAT NEXT

Define port states on supply ports and power state table if necessary.

SEE ALSO

set_operating_conditions(2)
set_voltage(2)
create_pst(2)
add_port_state(2)

MV-753 (info) Level shifter %s from library %s cannot be %s because %s.

DESCRIPTION

This message shows that certain (enabled) level shifters cannot be instantiated in the design due to tight constraints.

WHAT NEXT

Relax the constraints would help the insertion of level shifters.

SEE ALSO

set_level_shifter(2)

MV-754 (error) Cannot insert an isolation cell on net %s because it is undriven.

DESCRIPTION

This error message occurs when the **insert_isolation_cell** command cannot insert an isolation cell on an undriven net.

The tool cannot insert an isolation cell when it encounters any of the following conditions:

- The isolation cell reference is not characterized to the operating condition specified on the net’s subdesign.
- The isolation cell does not exist in the target library subset specified on the net’s subdesign.
- The net has multiple drivers or it is connected to an I/O driver.
- The net is set as dont_touch or always on.
- The net has load pins operating at multiple voltages.
- The net is not driven by any pin.
- The port is floating.

WHAT NEXT

Run the **insert_isolation_cell -verbose** command on the error nets for more information. After making any necessary changes, run the command again.

SEE ALSO

insert_isolation_cell(2)

MV-755 (error) Cannot insert an isolation cell on port %s because it is floating.

DESCRIPTION

This error message occurs when the **insert_isolation_cell** command cannot insert an isolation cell on floating port.

The tool cannot insert an isolation cell when it encounters any of the following conditions:

• The isolation cell reference is not characterized to the operating condition specified on the net’s subdesign.

• The isolation cell does not exist in the target library subset specified on the net’s subdesign.

• The net has multiple drivers or it is connected to an I/O driver.

• The net is set as dont_touch or always on.

• The net has load pins operating at multiple voltages.

• The net is not driven by any pin.

• The port is floating.

WHAT NEXT

Run the **insert_isolation_cell -verbose** command on the error nets for more information. After making any necessary changes, run the command again.

SEE ALSO

insert_isolation_cell(2)

MV-756 (warning) Total %d port has/inherited a dont_touch which may prevent the insertion of isolations.

DESCRIPTION

This error message occurs when it is found that the isolation insertion for some port could be prevented by dont_touch. For example, isolation cells are not allowed to be inserted if the parent hierarchy, where the isolation is to be located, is dont_touch.

WHAT NEXT

Use **check_mv_design -verbose** to see the details of the ports.

Check the dont_touch setting around the port to ensure the successful insertion of isolation cells.

SEE ALSO

set_isolation(2)
insert_isolation_cell(2)
set_dont_touch(2)

MV-756a (warning) Port %s has/inherited a dont_touch which has prevented the insertion of isolation for strategy %s.

DESCRIPTION

This error message occurs when the isolation insertion for a port is prevented by dont_touch. For example, isolation cells are not allowed to be inserted if the parent hierarchy, where the isolation is to be located, is dont_touch.

WHAT NEXT

Check the dont_touch setting around the port.

SEE ALSO

set_isolation(2)
insert_isolation_cell(2)
set_dont_touch(2)

MV-756b (warning) Port %s has/inherited a dont_touch which may prevent the insertion of isolation for strategy %s.

DESCRIPTION

This error message occurs when it is found that the isolation insertion for a port could be prevented by dont_touch. For example, isolation cells are not allowed to be inserted if the parent hierarchy, where the isolation is to be located, is dont_touch.

WHAT NEXT

Check the dont_touch setting around the port to ensure the successful insertion of isolation cells.

SEE ALSO

set_isolation(2)
insert_isolation_cell(2)
set_dont_touch(2)

MV-757 (error) Failed to get matching power or ground net for power_net_info object %s.

DESCRIPTION

This error message occurs when the specified power_net_info does not have a matching power or ground net.

WHAT NEXT

Use the **derive_pg_connection -create_net** command to create power or ground nets if they are missing. Ensure that all supply nets and ports are properly defined and connected.

SEE ALSO

check_mv_design(2)
derive_pg_connection(2)

MV-758 (error) No nominal Process, Voltage, and Temperature is defined for library %s. And an assertion FATAL is expected with this error message, because the tool does not know how to continue when this error occurs.

DESCRIPTION

All libraries used for multi-voltage design must have the 'nom_process','nom_voltage', and 'nom_temperature' attribute defined.

WHAT NEXT

Make sure the library has its 'nom_process','nom_voltage', and 'nom_temperature' defined. Re-generate the DB file for the library using library compiler after correcting the problem.

SEE ALSO

check_mv_design (2)

MV-759 (warning) Total %d logic constant pin(s) are connected to power/ground net(s) that are inconsistent with the cell's power connection.

DESCRIPTION

This messages is printed when one or more tie off pin(s) are connected to power/ ground net(s) that are different from the connections derived from the power connections of the cell's power domain.

WHAT NEXT

Check whether the tie high/low connection is correct. If not, fix it automatically using commands **connect_logic_one -reconnect_all**, **connect_logic_zero -reconnect_all**; or perform manual connection through command **connect_pg_net**.

SEE ALSO

connect_logic_one(2) connect_logic_zero(2) connect_pg_net(2) create_power_domain (2) **create_power_net_info** (2) **connect_power_domain** (2)

MV-760 (Error) Source '%s' is already connected to '%d' Switch Cell Pins. It cannot be connected to other power switch pins.

DESCRIPTION

This messages is printed when connect_power_switch command finds that the source port or pin is already connected to some load pins.

WHAT NEXT

Check if the net connected to the given source pin/port is connected to some load

pins. You should disconnect the previouse connection before using connect_power_switch. You can also start with saved design before the power switch connections were made.

SEE ALSO

connect_power_swtich(2)

MWCN-001 (error) When build and check full name for "%s", error "%s

DESCRIPTION

Please find cooresponding explanation for each error:

mwcnMsgEscStyleMismatch: The base name’s escaping style (NO_ESCAPE) is not compatible with the database (APF). Please add ’’ in front of every hierarchical delimiter.

mwcnMsgNameTooLong: The full name’s length exceeds 1024 characters that database can support. You can try to use a shorter name instead.

MWCN-002 (information) The database is not modified.

DESCRIPTION

This message occurs when the tool attempted to change object names in the database into an supported escaping style, but did not change any name or database property.

MWCN-003 (warning) Changing name from %s to %s is NOT the default behavior!

DESCRIPTION

This warning message occurs when the tool is trying to do a non-default change to the escaping style of the object names in the database. The default change of each escaping style is listed below:

```
NO_ESCAPE --> NO_ESCAPE (no change)
 APF --> APF (no change)
 VERILOG --> NO_ESCAPE
 APF_VERILOG(mixed) --> APF
 DEF --> APF
 UNKNOWN --> NO_ESCAPE
```

MWCN-004 (error) Changing name from %s to %s is not

allowed!

DESCRIPTION

This warning message occurs when the tool is ordered to do an unsupported change of the escaping style of the object names in the database. The supported change for each escaping style is listed below:

```
NO_ESCAPE --> NO_ESCAPE (no change)
 APF --> APF (no change), NO_ESCAPE
 VERILOG --> NO_ESCAPE
 APF_VERILOG(mixed) --> APF, NO_ESCAPE
 DEF --> APF, NO_ESCAPE
 UNKNOWN --> NO_ESCAPE
```

MWCN-005 (information) Changing names from %s to %s...

DESCRIPTION

This message indicates that the tool is changing the object names in the database into a different escaping style and the user need to wait for the change to complete. The supported target escaping styles are APF and NO_ESCAPE style.

MWCN-006 (warning) Cannot open name-change log file %s for write.

DESCRIPTION

This warning message occurs when the tool is changing the escaping style of object names in the database. It attempts to record the object name changes in a log file with a given name, but the file cannot be opened.

MWCN-007 (information) Log file %s generated for changed object name.

DESCRIPTION

This message occurs after the tool has changed the object names in the database into a different escaping style. It indicates that a log file with a given name is generated for the user’s referece. All name changes are recorded in the log file.

MWCN-008 (information) The database is changed into %s style.

DESCRIPTION

This message indicates that the tool has changed the escaping style of object names in the database into a different style.

MWCN-009 (error) The target style %s is not supported!

DESCRIPTION

This warning message occurs when the tool is trying to change the object names in the database into an unsupported escaping style. The supported target escaping styles are APF and NO_ESCAPE style.

MWCN-010 (warning) The hierarchy information of net 0x%08x %s cannot be decided, skipped changing the name of 0x%08x.

DESCRIPTION

This warning message occurs when the tool is trying to change the name of a flat net from an unsupported escaping style to a supported one. Because the flat net or one of its hierarchical net is not contained in any hierarchical cell instance, its full name cannot be decided. Therefore the name changing does not happen.

MWCN-011 (warning) %s 0x%08x and %s 0x%08x both have name %s. Skipped changing the name of 0x%08x due to undecidable hierarchy information.

DESCRIPTION

This warning message occurs when a scalar name is colliding with a bus name due to name escaping style changing. When this happens, the tool always trys to change the scalar name instead of the bus name. This message indicates that at least one of the two objects is not contained in any hierarchical cell instance. The full name of the uncontained object cannot be decided. So the attempted changing of the scalar name does not happen.

MWCN-012 (warning) UNKNOWN escaping style is returned because the input argument is not supported.

DESCRIPTION

This warning message occurs when the function is getting an input argument which is not supported. In this case, UNKNOWN escaping style is returned.

MWCN-020 (information) Changed name of %s 0x%08x from %s to %s.

DESCRIPTION

This information message shows up when the name of an object is being changed from an unsupported escaping style into a supported style. It lists the object id, old name and new name. The name changing information can also be found in the name-change log file.

WHAT NEXT

See name-change log file for record of name changes.

MWDB-1 (error) Cell does not have a cell boundary.

DESCRIPTION

You received this error message because cell boundary is missing.

WHAT NEXT

Run initialize_floorplan

MWDC

MWDC-001 (error) Can not create instance master '%s' in FRAM view.

DESCRIPTION

You receive the error message because for some reasons, the instance master can't be create in FRAM view. For instance, please check the read and write permission for FRAM directory, please check if the instance master name is longer than 1024 chars, the instance master should not existed.

WHAT NEXT

Pleae check the read and write permisson for the FRAM directory

MWDC-002 (error) Can not create cell instance '%s' because can't find the reference cell in FRAM view.

DESCRIPTION

For create operation, user should has full permission of the library. The cell instance's name should valid, that means the name is unique, the name's length should not longer than 1024 chars. Another thing is the master of the cell instance should available in FRAM view.

WHAT NEXT

MWDC-003 (error) Can not create cell instance '%s'.

DESCRIPTION

You receive this error message because by some reasons the cell instance can't be create, for instance, the cell instance name is not unique, master of the cell instance can't be find in FRAM view, the cell instance's name is too long, more than 1024 chars, permission is not allow you create it in the library.

WHAT NEXT

MWDC-004 (error) Cannot create Port %s(0x%x) in design %s(0x%x).

DESCRIPTION

For create operation, user should has full permission for the milkyway library, and the name should unique, the name length should not longer than 1024 chars.

WHAT NEXT

MWDC-005 (error) Cannot find instance in CEL view '%s'.

DESCRIPTION

User should have read permission for CEL view, and check that the instance name being input is correct or not.

WHAT NEXT

MWDC-006 (error) Cannot create net '%s'.

DESCRIPTION

For create action, user should have full permission for the Milkyway library, and the name should be unique; also the name length should not longer than 1024 chars.

WHAT NEXT

MWDC-007 (warning) Scaling factor less than 1, will result in

loss of accuracy.

DESCRIPTION

WHAT NEXT

MWDC-008 (error) Unable to get direction for pin '%s' of cell '%s', assuming INPUT.

DESCRIPTION

During loading Milkyway library, a no direction pin was found: by default, the pin will be set to INPUT pin.

WHAT NEXT

MWDC-009 (error) Unable to find port %s(0x%x) in design %s(0x%x).

DESCRIPTION

To find a port in CEL, you should provide a valid port name, and the owner cell should exist and be valid too.

WHAT NEXT

MWDC-010 (error) Failed to open %s %s.

DESCRIPTION

This error message indicates that the specified MW design library cannot be open. The reasons for this could be either of the following.

- Library/CEL name not specified.

- Library/CEL named not found in the search_path.
- Library/CEL named not found in the search_path.
- Library/CEL is locked.
- No read/write permissions for the Library/CEL.

WHAT NEXT

Please check that the MW design library/CEL names are specified, and that they exist in one of the directories specified in the search_path. They should also be unlocked and the user should have read/write permissions for them.

MWDC-011 (error) Hierarchy preservation does not exist; this command cannot proceed.

DESCRIPTION

This error message occurs when the input CEL view does not contain hierarchy preservation data. Various commands eg **link, current_design** require hierarchy preservation data to be present in the CEL view, in order to properly create the data structures required to execute those commands. Since the hierarchy preservation data cannot be found, the command cannot continue.

WHAT NEXT

Regenerate the input CEL view with hierarchy preservation data and run the command again. For example, if the CEL was created using some other tool, eg Astro, use Astro to save the CEL properly.

SEE ALSO

link(2)
current_design(2)

MWDC-012 (error) Cannot open library '%s'.

DESCRIPTION

This error message occurs when the FRAM view and technology file cannot be found. Or, the design lib directory name may be an invalid Milkyway design lib, for example, an existing normal unix dir.

WHAT NEXT

Verify that the Milkyway library directory is a valid mw design lib directory and the files are available and that you have write permission for the Milkyway library directory and then run the command again.

MWDC-013 (error) Cannot initialize route storage for design '%s'.

DESCRIPTION

This error message occurs when route info will not be loaded for this design.

WHAT NEXT

Check that you have write permission for the directory which the test case is running. Also check that there is disk space available in the directory. Some disk space is necessary for storing route information used in the current session.

MWDC-014 (error) Cannot write Milkyway for %s design.

DESCRIPTION

For a design to be written out in Milkyway database format, it has to be uniquified and mapped, since the Milkyway database does not support un-uniquified or un-mapped design. This error occurs when the design in memory is un-uniquified/un-mapped, and a command was executed that would trigger writing of design to Milkyway database. Besides save_mw_cel, commands that internally link the design could trigger creation of auto-CEL, which could lead to this error if the design is un-uniquified or un-mapped.

WHAT NEXT

Please make sure the design is mapped and uniquified.

MWDC-015 (error) Invalid hierarchy preservation: %s %s(0x%x) of %s %s(0x%x) is connected to %s %s(0x%x), which is not in

the same level of hierarchy.

DESCRIPTION

This error message occurs when the hierarchy preservation data in the Milkyway CEL is inconsistent. A hierarchical port(or a leaf pin) can only be connected to a hierarchical net that is within the same level of hierarchy. In this case, the hierarchical port(or the leaf pin) and the hierarchical net above are not in the same level of hierarchy. This Milkyway CEL cannot be read in.

Note that the hexadecimal value (0x%x) specifies the object id. For hier cell, you can use UI command "get_cells -object_id $object_id" to retrieve the full hierarchical name of the hier cell.

WHAT NEXT

If this CEL was generated by Astro/JXT, try running 'astRepairHierPreservation' command in Astro/JXT. If the CEL was generated by PC/ICC, or if 'astRepairHierPreservation' in Astro/JXT did not resolve the issue, please contact Synopsys Support.

MWDC-016 (error) Invalid hierarchy preservation: hier net %s(0x%x) is connected to port %s(0x%x) of hier cell %s(0x%x), but the port is not connected to the hier net.

DESCRIPTION

This error message occurs when the the hierarchy preservation data in the Milkyway CEL is inconsistent. The hierarchical net appears to be connected to the hierarchical port, but the hierarchical port does not appear to be connected to this hierarchical net. Note that the hexadecimal value (0x%x) specifies the object id. For hier cell, you can use UI command "get_cells -object_id $object_id" to retrieve the full hierarchical name of the hier cell.

WHAT NEXT

If this CEL was generated by Astro/JXT, try running 'astRepairHierPreservation' command in Astro/JXT. If the CEL was generated by PC/ICC, or if 'astRepairHierPreservation' in Astro/JXT did not resolve the issue, please contact Synopsys Support.

MWDC-017 (warning) Pin %s(0x%x) of cell instance %s(0x%x) connected to hier net %s(0x%x), but not connected to any flat

net.

DESCRIPTION

You receive the error message because the flat and hierarchical netlist in the CEL have been found to be inconsistent. A leaf pin connected to hier net should be connected to a corresponding flat net.

WHAT NEXT

If this CEL was generated by Astro/JXT, try running 'astRepairHierPreservation' command in Astro/JXT. If the CEL was generated by PC/ICC, or if 'astRepairHierPreservation' in Astro/JXT did not resolve the issue, please contact Synopsys Support.

MWDC-020 (Warning) Design is from MW. This command does not incrementally update the CEL. This will result loosing route data.

DESCRIPTION

This design is read from MW database. Command you are currently running does not incrementally update the in-memory CEL. This means the changes done by this command will not be there in CEL and you will loose some data.

WHAT NEXT

set the variable mw_create_cel_force to TRUE, to avoid incremental update of CEL. However this might results in loosing the route data.

MWDC-021 (Error) Design is from MW. This command does not incrementally update the CEL. Can not proceed.

DESCRIPTION

This design is read from MW database. Command you are currently running does not incrementally update the in-memory CEL. As the variable mwdc_update_bypass_error is set to FALSE, this error can not be by passed.

WHAT NEXT

Set the variable mw_create_cel_force to TRUE, to avoid incremental update of CEL. Set the variable mwdc_update_bypass_error to TRUE to by-pass this error. However this will results in loosing the route data.

MWDC-022 (warning) Some MWDC messages have been suppressed. The following list gives the number and format of the messages.

DESCRIPTION

Some MWDC message formats are issued no more than 20 times (by default) to avoid extremely long log files.

WHAT NEXT

Use the **mwdc_message_limit** variable to allow more instances of each format to be issued. Example: set **mwdc_message_limit** 10000 allows ten thousand instances of each format to be issued before suppressing the rest.

MWDC-023 (information) CellInst '%s' (%s) is not part of hierarchy or did not link and will be treated as physical only.

DESCRIPTION

This message may be followed by MWDC-024 which is a serious error related to linking or a corrupt Milkyway CEL. If there is no later MWDC-024 error, then this message just indicates that certain cellInsts in the design are physical only.

WHAT NEXT

MWDC-024 (error) Either 1) link error or 2) corrupted Milkyway database: The net %s(0x%x) connects to pin %s(0x%x) of cell instance %s(0x%x) with physical masterCell %s(0x%x).

DESCRIPTION

1) If there are earlier MWDC-023 messages stating that the masterCell did not link,

then the logical library must be updated to have the logical cell description. 2) If there are no link warnings, then the Milkyway database may be corrupted and should be rebuilt.

Issue 1) occurs when there was a previous linking error, MWDC-023, because a logical cell in the design had no physical cell description in the physical library. The physical library needs to be updated to provide a physical cell for each logical cell used in the design.

Issue 2) occurs when there is some corruption in the input Milkyway CEL and some cellInsts are not included in the Milkyway hierarchy information. When that happens, a DC netlist cannot be properly constructed. Possibly, the hierarchy information can be repaired, using the Milkyway or Astro executables. If not, then the Milkyway CEL should should be re-built.

WHAT NEXT

MWDC-025 (error) FPGA libraries are not supported in Incremental/Hybrid mode.

DESCRIPTION

WHAT NEXT

MWDC-026 (error) Failed to link physical library with link library.

DESCRIPTION

Make sure that 1) the logical library is defined, 2) the physical library is defined, 3) any earlier library errors are addressed (PSYN-141, PSYN-125, PSYN-027, PSYN-028).

WHAT NEXT

MWDC-027 (error) Failed to load design from MW CEL named '%s'.

DESCRIPTION

Earlier MWDC-* errors and warnings should explain what went wrong when trying to

build a DC design from a MW CEL.

If there were messages about inconsistencies between hier_nets and flat_nets in the MW CEL, then it may be necessary to run astRepairHierarchy in Astro or Jupiter before loading the MW CEL in IC Compiler.

WHAT NEXT

MWDC-028 (Warning) The non-constant Milkyway net '%s' has %s load pin '%s' on cell instance '%s' but no driver. It will now be driven by logic zero.

DESCRIPTION

The named net connects to a load pin (input or inout) of a cell instance in the target_library, but the net has no driver.

Such nets are given a logic zero driver by default. The net is considered non-constant because the name is not equal to either variable **mw_logic0_net** or **mw_logic1_net**.

WHAT NEXT

The net name pertains to a power/ground net. The words POWER or GROUND appear in the message to help the user identify the type of net involved.

The user must independently make sure that the variables **mw_logic0_net** and **mw_logic1_net** are properly set to indicate which nets are power/ground. Without proper settings, there is a potential for bad logic.

This message is important and indicates a problem with your design that must be addressed by the user.

MWDC-029 (error) %s

DESCRIPTION

This is a internal error. Please report to Synopsys

WHAT NEXT

Please alert the Synopsys Support Center.

MWDC-030 (Warning) No uniquify allowed on design with Milkyway already written in IC Compiler.

DESCRIPTION

This warning message is issued by the **uniquify** command. No uniquify is allowed by IC Compiler after a Milkyway database has been written (by **link** or other commands that link the design).

WHAT NEXT

Uniquify the design before loading it in IC Compiler.

Check the man page for the **uniquify** command.

MWDC-032 (Warning) No Route constrains on dangling net, or net with constant driver '%s'.

DESCRIPTION

This warning message can be issued by the **read_mw_cel** command and physopt command. Route onstrains will not be set on dangling net, or net with constant driver.

MWDC-033 (Error) Cannot use a pin on a physical-only cell, %s, for logical operations.

DESCRIPTION

This error occurs when the user of IC Compiler is trying to connect a signal net to a pin on a physical-only cell. The cell is physical-only because there is no logical library cell for the cell. Also, some types of cells are always treated as physical-only, such as filler and tap cells.

WHAT NEXT

Use the fconnect_pg_nets command to connect pins on physical-only cells.

MWDC-034 (Error) The cell instance '%s' with reference type '%s' was not linked to the logical library and cannot be written to

the database.

DESCRIPTION

This error can occur when a dseign is read in from Verilog and there is a linking error because a cell instance has an unknown reference type. IC Compiler does not write black-boxes automatically from Verilog when there are missing library references.

WHAT NEXT

Either fix the Verilog type reference or augment the link library and re-run.

MWDC-035 (warning) The cell instance '%s' has reference type '%s' which is not in the Physical Library.

DESCRIPTION

This warning occurs because a Milkyway design has a cell instance with a reference type that is not in the Physical Library. The tool does not allow the creation of black boxes from unknown references.

WHAT NEXT

Either fix the Verilog type reference or augment the link and physical libraries and rerun the command.

MWDC-036 (Warning) The cell instance '%s' with reference type '%s' has non-power/ground pins but is not part of the hierarchy.

DESCRIPTION

This warning occurs when a cell instance has non-power/ground pins but is not part of the Milkway hierarchy. The database may be corrupt and the user should look for later messages about failed attempts to connect to this cell instance.

WHAT NEXT

If there are later errors about connections to the cell instance, then report the problem to Synopsys. If the cell instance is not connected to the logical netlist, then IC Compiler can proceed.

MWDC-037 (Warning) The cell instance '%s' (%s) has non-power/ground pins (or no pins), but is not in the link library. It will be treated as an unlinked black-box. The physical library cell %s.

DESCRIPTION

This warning occurs when a Milkyway design has a cell instance with a reference type that is not in the link library.

IC Compiler will create a black-box for this instance and can proceed. Some advantages of having a link libray cell are listed below.

The message also tells whether the physical library cell exists or not.

WHAT NEXT

The user may want to provide a link library cell for the cell instance so that optimizations can work on it. Timing will also be more accurate if the link library cell is provided.

MWDC-038 (Error) Cannot delete the physical_only net '%s'.

DESCRIPTION

This error occurs when a Milkyway net cannot be deleted.

WHAT NEXT

Look for earlier messages for possible explanations. If there are none, then there is some database inconsistency problem: call Synopsys.

MWDC-039 (Error) A Milkyway cell instance has an inconsistency between its hierarchical name '%s' and flat name '%s'.

DESCRIPTION

This error occurs when a Milkyway cell instance has different names stored for the same Milkyway object. The database is inconsistent.

WHAT NEXT

Report the problem to Synopsys.

MWDC-040 (Information) Net %s has no connections.

DESCRIPTION

This information message can be issued when trying to iterate over the ports/pins connected to a net in Milkyway.

MWDC-041 (information) CellInst '%s' (%s) is part of the hierarchy but has only power/ground pins. It will be treated as physical only.

DESCRIPTION

This message may be followed by MWDC-024 which is a serious error related to linking or a corrupt Milkyway CEL. If there is no later MWDC-024 error, then this message just indicates that certain cellInsts in the design are physical only.

WHAT NEXT

MWDC-042 (warning) The net connection on input pin %s(0x%x) of cell instance %s(0x%x) is not complete. It should be connected to %s(0x%x).

DESCRIPTION

This message may be preceded by MWDC-125, which describes a mismatch between the mw_logic0/1 variable and the value stored in the Milkyway design library. Example:

Warning: Name of mw_logic0/1 net 'vdd' specified by TCL variable does not match the name of mw_logic0/1 'VDD' in milkyway design library. (MWDC-125)

WHAT NEXT

You might be able to fix this problem if the net is a power/ground net reported by MWDC-125:

set mw_logic0_net VSS set mw_logic1_net VDD

where VDD and VSS are the names for power and ground stored in the Milkyway design library.

Otherwise, report this problem to Synopsys.

MWDC-043 (error) Multiply-instantiated Hierarchical Cell Master '%s' (one instance is '%s').

DESCRIPTION

This error occurs because designs should be uniquified before loading them in the tool.

WHAT NEXT

Use the **uniquify** command after reading verilog and before using the **link** command. Designs that are already in MW CEL format must be uniqufied in Astro or written to verilog and read again.

MWDC-044 (Warning) Net %s has multiple drivers.

DESCRIPTION

This warning message can be issued if net has multiple drivers.

MWDC-052 (warning) Some MWDC messages have been suppressed. The following list gives the number and format of the messages.

DESCRIPTION

Some MWDC message formats are issued no more than 20 times (by default) to avoid extremely long log files.

WHAT NEXT

Use the **mwdc_message_limit** variable to allow more instances of each format to be issued. Example: set **mwdc_message_limit** 10000 allows ten thousand instances of each

format to be issued before suppressing the rest.

MWDC-053 (Error) The -only_physical option may not be used on remove_nets in IC Compiler.

DESCRIPTION

Do not use the -only_physical option on **remove_nets** in IC Compiler. No option is needed to remove physical only nets, but remember that power/ground nets cannot be removed.

WHAT NEXT

Try **remove_nets** with no options.

MWDC-054 (Error) Hier net %s (0x%x) has no type.

DESCRIPTION

The Milkyway database does not contain type information for the named net.

WHAT NEXT

Contact Synopsys.

MWDC-055 (Error) PG pin (0x%x) is connected with multiple %s nets: net1 = (0x%x) and net2 = (0x%x)

DESCRIPTION

In the Milkyway database, the named PG pin has connections to more than one net. This is an inconsistency.

WHAT NEXT

Contact Synopsys.

MWDC-056 (Error) Hierarchical Tie Net %s (0x%x) connected to

output pin (0x%x).

DESCRIPTION

The named net is a tie high or low net and is connected to an output port. Tie nets should only be connected to input pins of leaf cells or hierarchical cells.

WHAT NEXT

Contact Synopsys.

MWDC-057 (Error) Flat PG net %s contains %s pin %s

DESCRIPTION

The flat Milkyway PG net contains either a VDD or GND pin.

WHAT NEXT

MWDC-060 (Error) Unable to create cell inst master '%s'.

DESCRIPTION

Unable to create cell inst master for the given reference.

WHAT NEXT

Make sure the reference cel exists and library is writable.

MWDC-061 (Error) Cannot add new cellInst '%s'.

DESCRIPTION

Unable to add new instance in the MW design.

WHAT NEXT

Make sure the reference cel exists and library is writable.

MWDC-066 (error) Internal error - %s.

DESCRIPTION

Internal error.

WHAT NEXT

Report the problem to Synopsys

MWDC-070 (Error) Could not get milkyway id from "%s".

DESCRIPTION

This error message occurs when the milkyway id for the given object is not found in the database.

WHAT NEXT

Please check the DC object specified in the command.

MWDC-100 (error) CEL consistency check failed.

DESCRIPTION

This error occurs because the netlist data in the CEL view is inconsistent. The inconsistencies should have been reported before this error message appeared.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

MWDC-101 (error) The design is not uniquified.

DESCRIPTION

You receive the error message because the input design has non-uniquified netlist,

i.e. there are more than one hierarchical cell instances with the same reference.

WHAT NEXT

If the design comes from JupiterXT or Astro, please go back and uniquify the Milkyway design in JupiterXT or Astro.

If you are running a design with multi instantiated modules (MIM) inside IC Compiler, please identify which MIM flow (Top-Down MIM Flow; Black Box MIM Flow; or Virtual Flat MIM Flow) you are working on and follow the suggestions as stated in IC Compiler Design Planning's User Guide or Application Note.

Otherwise, uniquify the design with uniquify_fp_mw_cel before saving it.

MWDC-102 (error) The flat net %s(0x%x) is connected to pin %s(0x%x) of cell instance %s(0x%x) in a flat netlist, but not in a hierarchical netlist.

DESCRIPTION

This error occurs because the flat and hierarhcial netlist in the CEL are inconsistent. In this case, a PortInst is connected to a flat net in the flat netlist, but is not connected to the corresponding hierarhical net in the hierarchical netlist.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-103 (error) The flat net %s(0x%x) is connected to port %s(0x%x) of design %s(0x%x) in a flat netlist, but not in a hierarchical netlist.

DESCRIPTION

This error occurs because the flat and hierarhcial netlist in the CEL are

inconsistent. In this case, a port is connected to a flat net in the flat netlist, but is not connected to the corresponding hierarhical net in the hierarchical netlist.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-104 (error) The following hier nets should correspond to one flat net, but they do not.

DESCRIPTION

This error occurs because the flat and hierarchical netlist in the CEL are inconsistent. Hierarchical nets connected together through hierarchical ports should belong to one single flat net; but, in this case, they belong to multiple flat nets.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

MWDC-105 (error) The cell inst %s (0x%x) has no parent hierarchy, but is connected to a logical netlist.

DESCRIPTION

This error occurs because a leaf cell instance that does not belong to any hierarchy is connected to a hierarchical netlist.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact

Synopsys Support.

MWDC-106 (error) The cells (0x%x) and (0x%x) have the same name, '%s', in the same level of hierarchy.

DESCRIPTION

This error occurs because multiple cell instances have the same name in the same level of hierarchy, which is not allowed.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

MWDC-107 (error) A cross-hierarchy connection exists for HierNet %s (0x%x).

DESCRIPTION

This error occurs because a HierNet is connected to ports/portInsts not within the same level of hierarchy, without crossing via a hierarchical port.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

MWDC-108 (error) The hierCells (0x%x) and (0x%x) have the same name, '%s', in the same level of hierarchy.

DESCRIPTION

This error occurs because more than one hierCellInst with the same name exists in the same level of hierarchy, which is not allowed.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

MWDC-109 (error) More than one port exists with the name %s in design %s(0x%x).

DESCRIPTION

This error occurs because more than one port with same name exists in the same level of hierarchy, which is not allowed.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-110 (error) Orphaned hierarchical cells exist.

DESCRIPTION

This error occurs because certain hierarchical cells exist in the database that cannot be reached by traversing the hierarchy.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

MWDC-111 (error) The hier net %s(0x%x) is connected to the port %s(0x%x) of hier cell %s(0x%x) in a hierarchical netlist, but

is not connected to the corresponding flat net %s(0x%x) in the flat netlist.

DESCRIPTION

This error occurs because the flat and hierarchical netlist connections are inconsistent. In this case, a port/pin is connected to a hierNet, but is not connected to the corresponding flat net.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-112 (error) Port %s(0x%x) of hier cell %s(0x%x) is reachable from the hier net %s(0x%x), but the hier net is not reachable from port.

DESCRIPTION

This error occurs because a HierPortInst is connected to a HierNet, but the same HierNet is not connected to the HierPortInst.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-113 (error) Internal database error.

DESCRIPTION

You receive the error message because an internal database access has failed.

WHAT NEXT

Please contact Synopsys support.

MWDC-114 (error) %s %s of %s %s(0x%x) does not exist in the hierarchy.

DESCRIPTION

This error occurs because a port exists in the flat netlist, but does not exist in the hierarchical netlist.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-115 (error) Unable to find the TOP instance in the hierarchy.

DESCRIPTION

This error occurs because the database does not identify any instance as the TOP instance in the netlist hierarchy.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact

Synopsys Support.

MWDC-116 (error) Unable to get the parent of the cell %s (0x%x).

DESCRIPTION

This error occurs because a leaf cellInst has no parent in the hierarchy preservation data.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

MWDC-117 (error) Unable to get the parent of the hier cell %s (0x%x).

DESCRIPTION

This error occurs because a hier cellInst has no parent in the hierarchy preservation data.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

MWDC-118 (info) Performing CEL netlist consistency check.

DESCRIPTION

This message indicates that consistency check for netlist data in CEL is being performed.

WHAT NEXT

MWDC-119 (info) CEL consistency check PASSED.

DESCRIPTION

This message indicates that consistency check of CEL netlist data was performed and no issues were found.

WHAT NEXT

MWDC-120 (warning) Net %s (0x%x) has no type.

DESCRIPTION

This message indicates that a net with no valid type was found.

WHAT NEXT

Please contact Synopsys Support.

MWDC-121 (error) Net %s(0x%x) is connected to port %s(0x%x) of design %s(0x%x), but the port is connected to a different net, %s(0x%x).

DESCRIPTION

This error occurs because netlist data in a CEL is inconsistent. A net is connected to a port, but the port is connected to a different net.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-122 (error) Net %s(0x%x) is connected to port %s(0x%x) of cell instance %s(0x%x), but port is connected to a different net %s(0x%x).

DESCRIPTION

This error occurs because netlist data in a CEL is inconsistent. A net is connected to a PortInst, but the port is connected to a different net.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-123 (error) Nets (0x%x) and (0x%x) have the same name, '%s'.

DESCRIPTION

This error occurs because two flat nets have the same name, which is not allowed.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

MWDC-124 (error) The tool cannot find hierarchy preservation data. A CEL cannot be read in.

DESCRIPTION

This error occurs because the input CEL does not contain any hierarchy preservation data. The tool cannot open such a CEL.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

MWDC-125 (warning) Name of mw_logic0/1 net '%s' specified by TCL variable does not match the name of mw_logic0/1 '%s' in milkyway design library.

DESCRIPTION

Logic0/1 nets are identified by their names. When the name specified by the TCL variables (mw_logic0_net, mw_logic1_net) does not match the setting in the database, TCL variables are given preference.

WHAT NEXT

Please make sure that the values of TCL variables mw_logic1_net and mw_logic0_net match the names of logic0/1 nets in the Milkyway design library.

MWDC-126 (warning) Found mw_logic0/1 net '%s' in the database with non PG net type.

DESCRIPTION

You receive this warning message when a net with mw_logic0/1_net name was found in the database but was not of type PG. Logic0/1 nets should be of type PG in the database.

WHAT NEXT

Please make sure mw_logic0/1 nets are defined as PG in the database.

MWDC-127 (warning) Mw_logic0/1 net '%s' not found in the

database.

DESCRIPTION

You receive this warning message when a net with mw_logic0/1_net name is not found in the database. The logic0/1 net name is determined by TCL variables mw_logic0_net (defalut VSS) and mw_logic1_net (default VDD). Note that a net not being found indicates that either the TCL variables are not set correctly, or there are no logic0/1 connections in the netlist. In the latter case, this warning should be ignored.

WHAT NEXT

Please make sure the settings for TCL variables mw_logic0_net/mw_logic1_net match the names of logic0/1 nets in the database. If there are no logic0/1 connections in the netlist, then this warning should be ignored.

MWDC-128 (warning) TCL variable mw_logic0/1 not set, using the logic0/1 net names setting from the database %s.

DESCRIPTION

You receive this warning message when you have not define the TCL variables (mw_logic0_net, mw_logic1_net) to specify the names of tiehi/lo nets in the netlist, and a setting for these names exists in the database. The tool will pick up the name specified in the database.

WHAT NEXT

Please make sure that the tool is picking up correct logic0/1 net names as specified in the message. If not, please restart after setting correct values for TCL variables mw_logic0_net and mw_logic1_net.

MWDC-129 (Error) Unable to infer names for logic0/1 net.

DESCRIPTION

You receive this error message when the tool was unable to find the names for logic0/1 nets in TCL variables as well as in the milkyway design library. In order for the tool to proceed, logic0/1 net names need to be defined.

WHAT NEXT

Please specify logic0/1 net names using TCL variables mw_logic0_net and mw_logic1_net. For example, 'set mw_logic1_net VDD'.

MWDC-130 (error) Cell %s (0x%x) belongs to multiple hierarchies

DESCRIPTION

This error occurs because a particular cell in the design has multiple immediate parents. A cell can have one, and only one, immediate hierarchical parent.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

MWDC-131 (error) Cell %s (0x%x) is reachable from parent hierarchy

DESCRIPTION

This error occurs because a particular cell in the design is reachable from its parent multiple times when traversing the netlist.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

MWDC-132 (Error) Un-supported name-escaping style.

DESCRIPTION

You receive this error message when the CEL being opened contains names that have an escape style that is not supported by ICC. This could happen for CELs that are

generated by Astro/JXT. ICC only supports names that are either not escaped, or are DEF style escaped. Names containing verilog-style escaping are not supported by ICC.

WHAT NEXT

Generate ASCII from the CEL using the tool that was used to generate the CEL, and read in ASCII (netlist, physical data and constraints) into ICC.

MWDC-133 (warning) CEL does not have hierarchy preservation.

DESCRIPTION

You receive this warning message when you are trying to open a CEL with no hierarchy preservation data. A design CEL is expected to have hierarchy preservation data. If this is a reference lib CEL, please ignore the message.

WHAT NEXT

If this is a design CEL, and the CEL was generated by Astro/JXT, try running astRepairHierPreserve command in Astro/JXT. If this is a library CEL, please ignore this message. Else, please contact Synopsys Support.

MWDC-134 (Error) Missing PG net information on voltage area %s.

DESCRIPTION

You receive this error message when you are trying to open a CEL which contains voltage areas with no power and ground net information on them.

WHAT NEXT

If this is a design CEL, and the CEL was generated by Astro/JXT, try running axgLinkPowerNetToVoltageArea command in Astro/JXT and specify at least one set of power and ground net names. Alternatively, try running set_power_net_to_voltage_area command in ICC and specify at least one set of power and ground net names. Else, please contact Synopsys

MWDC-135 (Warning) The PG net %s specified on voltage area

%s do not exist in CEL.

DESCRIPTION

You receive this warning message when you are trying to open a CEL where the power/ ground nets on voltage area do not exist in CEL yet.

WHAT NEXT

MWDC-136 (Warning) The pin on cell %s (%s) in the scanDEF is lost, delete scanDEF definition of the scan chain.

DESCRIPTION

A pin in the scanDEF is missing. So the scanDEF information is wrong and has to be deleted from the design. This can happen on the combinational logic cells after optimization. In order to prevent this from happening, the user should either 1) set_dont_touch or size_only (with same pin names) on those combinational logic cells defined on the scanDEF, or 2) remove them from the scanDEF definition (not from the netlist).

WHAT NEXT

Check the scanDEF and find the combinational logic cells. Either remove them from the scanDEF or set_dont_touch or size_only on them.

MWDC-137 (Error) Remove the scanDEF definition because some scan chain contains combinational logic gates without dont_touch or size_only attribute.

DESCRIPTION

A combinational logic gate on a scan chain must be set_dont_touch or size_only. Please review the scanDEF and find the scan chain containing the combinational logics, then either set_dont_touch or size_only on them, or remove the combinational logic cells from the scanDEF (not from the netlist).

WHAT NEXT

Review the scanDEF and find the combinational logic cells, then either set_dont_touch or size_only on them, or remove them from the scanDEF. User can use

report_scan_chain to find the scanDEF information as well.

MWDC-138 (Error) The net %s specified on voltage area %s is not PG type.

DESCRIPTION

You receive this error message because the nets you specified on voltage area property "VoltageAreaNetInfo" are not power/ground type.

WHAT NEXT

If this is a design CEL, and the CEL was generated by Astro/JXT, try running axgLinkPowerNetToVoltageArea command in Astro/JXT and specify at least one set of power and ground net names. Else, please contact Synopsys Support.

MWDC-139 (error) Losing connection on the PG pin %s of cell instance %s(0x%x). This pin was previously connected to regular signal net %s(0x%x).

DESCRIPTION

Users are getting this message because the PG pin that used to connect to a regular signal net will now be disconnected. This might lead to this pin being grounded later. The reason why this is happening is because there is a discrepancy in terms of pin type between FRAM and the logic db of the design.

WHAT NEXT

Please make sure that the FRAM and logic db are consistent across the Galaxy flow. Otherwise, users might need to establish the connection themselves by using netlist editing commands.

MWDC-140 (Warning) Scanning database for unsupported name escape style. This may take a few minutes depending on

the size of your design.

DESCRIPTION

You receive this warning message when you are trying to open a CEL with a possible unknown or even unsupported name escape style. Under this circumstance, the tool is now performing a name scanning on CEL to clarify whether its name escape style can indeed be supported by the tool.

WHAT NEXT

If you do not want the name scanning to happen, you should try to regenerate the CEL with a supported name escape style. Else, please contact Synopsys Support.

MWDC-141 (Error) Command can not proceed when the Milkyway CEL is opened in read only mode.

DESCRIPTION

Users are getting this message because an optimization command is issued when the Milkyway CEL is opened in read only mode. Only pure analyze commands can proceed when the Milkyway CEL is opened in read only mode.

WHAT NEXT

Please make sure that the Milkyway CEL is opened in both read and write mode if trying to execute optimization commands. Otherwise, please contact Synopsys Support for further assistance.

MWDC-142 (Error) Un-supported name-escaping style.

DESCRIPTION

You receive this error message when the CEL being opened contains names that have an escape style that is not supported by ICC. This could happen for CELs that are generated by Astro/JXT and ICC failed to change names in CEL with ICC supported naming style. ICC only supports names that are either not escaped, or MW APF style escaped. Other naming style are not supported by ICC.

WHAT NEXT

Generate ASCII from the CEL using the tool that was used to generate the CEL, and read in ASCII (netlist, physical data and constraints) into ICC.

MWDC-143 (error) Losing connection on the PG pin %s of cell instance %s(0x%x). This pin was previously connected to a power net %s(0x%x). This pin might now be tied to logic zero.

DESCRIPTION

Users are getting this message because the PG pin that used to connect to a power net will now be disconnected. This might lead to this pin being grounded later. The reason why this is happening is because there is a discrepancy in terms of pin type between FRAM and the logic db of the design.

WHAT NEXT

Please make sure that the FRAM and logic db are consistent across the Galaxy flow. Otherwise, users might need to establish the connection themselves by using netlist editing commands.

MWDC-150 (Error) Missing %s net information on voltage area %s.

DESCRIPTION

You receive this error message when you are trying to open a CEL which contains voltage areas with no power or ground net information on them.

WHAT NEXT

If this is a design CEL, and the CEL was generated by Astro/JXT, try running axgLinkPowerNetToVoltageArea command in Astro/JXT and specify at least one set of power and ground net names. Alternatively, try running set_power_net_to_voltage_area command in ICC and specify at least one set of power and ground net names. Else, please contact Synopsys

MWDC-155 (error) The hierarchy crossing flat net %s (0x%x) does not have a corresponding hier net.

DESCRIPTION

This error occurs because the flat and hierarhcial netlist in the CEL is inconsistent. The flat net that crosses a hierarchy should have a corresponding hierarchical net; otherwise, it is causes an error.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

MWDC-160 (warning) Found hierarchical net 0x%x without hierarchical port.

DESCRIPTION

You receive this warning message because there exists hierarchical net which has no hierarchical port attached to it. Every hierarchical net should always have a hierarchical port attached to it.

WHAT NEXT

Please contact Synopsys Support.

MWDC-161 (warning) Name of the flat net %s (0x%x) is not derived correctly from its hierarchical nets.

DESCRIPTION

You receive this warning message because the name of flat net is not properly derived from one of its hierarchical net. Usually, every flat net should be assigned the name of one of its hierarchical net. The consequence of having inconsistent names for the net is that the user might get inconsistent collection results

WHAT NEXT

Please contact Synopsys Support.

MWDC-165 (warning) logic0/1 net names setting not found in milkyway design library, using the TCL variable mw_logic0/

1_net setting.

DESCRIPTION

You receive this warning message because the logic0/1 net names setting does not exist in the Milkyway design library and you have defined the TCL variables (mw_logic0_net, mw_logic1_net) to specify the names of logic0/1 nets. The tool will pick up the names specified in the TCL variables as the logic1/0 net names.

WHAT NEXT

Please make sure that the tool is picking up correct logic0/1 net names as specified in the message. If not, please restart after setting correct values for TCL variables mw_logic0_net and mw_logic1_net.

MWDC-166 (warning) Using %s setting from the TCL variable %s

DESCRIPTION

You receive this warning message when tiehi/lo nets are not found in mw design library and tool uses the values defined by the TCl variables (mw_logic0_net, mw_logic1_net).

WHAT NEXT

Please make sure that the tool is picking up correct logic0/1 net names as specified in the message. If not, please restart after setting correct values for TCL variables mw_logic0_net and mw_logic1_net.

MWDC-169 (Information) Floating net %s is preserved.

DESCRIPTION

This information message is issued because user specify floating nets in "preserve_floating_nets" TCL variable. From the nets specified in "preserved_floating_nets", only floating nets will be honored, and a dont-touch is derived for these nets.

MWDC-170 (Warning) Power and Ground nets are never

deleted by netlist editing.

DESCRIPTION

You receive this warning message when you are connecting a net to a hierarchical port that has a Power or Ground net attached on the other side. This warning informs the user that the Power or Ground net will be the surviving net when the two Milkyway nets are merged in the database.

WHAT NEXT

MWDC-171 (error) Exclusive movebound/plangroup '%s' partially overlaps with movebound/planggroup '%s'.

DESCRIPTION

You receive this error message when some of the movebounds or plangroups overlap.

WHAT NEXT

Please make sure all the movebounds and plangroups are not overlap to each other. And re-check the overlap/nesting of movebounds.

MWDC-172 (warning) Should load physical library before reading this design, which has physical information.

DESCRIPTION

You receive this warning message when you open the design, meanwhile the corresponding physical library is not opened.

WHAT NEXT

Please check the design library and find if the FRAM veiw is correctly created. You can also try the command "open_mw_lib" to open the library. If failed, you can try to re-create the design library.

MWDC-173 (warning) design via %s has too many rectangles

(%d). Skip it.

DESCRIPTION

You receive this warning message when the design via has too many rectangles and out of limitation (e.g.10000). The tool perhaps can not match this kind of via.

WHAT NEXT

Please make sure the via description is right.

MWDC-174 (error) Failed to save CEL "%s".

DESCRIPTION

This error message indicates that the design CEL could not be saved into the Milkyway library. The reasons for this could be one of the following. No write permission for the Library/CEL. No disk space is available.

WHAT NEXT

Please check that the Milkyway design library and CEL are writeable and that there is sufficient disk space available.

MWDC-175 (warning) Found rectilinear region, only support rectangles.

DESCRIPTION

You receive this warning message when the rectilinears are used. This version only supports rectangles region.

WHAT NEXT

Please make sure all region are in rectangle shape.

MWDC-176 (warning) Found disjoint bound, skip writing to

database.

DESCRIPTION

You receive this warning message when the union of rectangles has disjoint bound. The tool will skip writing to database which may impact the voltage area creation.

WHAT NEXT

Please make sure the rectangle union areas are combined together.

MWDC-177 (error) The width and height values for cell %s differ between the reference library (width=%d, height=%d) and the design library (width=%d, height=%d).

DESCRIPTION

This error indicates that the bounding box defined for the cell differs between the design library and the reference library. This error can result in errors further in the design flow. For example, the design might contain cell overlaps, even after placement legalization.

WHAT NEXT

This error can occur if you change the reference library associated with the Milkyway design library after you saved the design. Use the report_mw_lib command to see the reference library associated with the current design library. If necessary, use the set_mw_lib_reference command to reset the reference library.

MWDC-178 (error) A physical-only cell instance %s (0x%x) has no parent hierarchy.

DESCRIPTION

This error occurs because a physical-only leaf cell instance exists that does not belong to any hierarchy.

WHAT NEXT

If this CEL was generated by Astro/JupiterXT or by an IC Compiler version before b2008.09, convert it into version b2008.09 by using the **convert_mw_lib** command in IC

Compiler version b2008.09. Contact Synopsys Support if the issue remains unresolved after converting.

MWDC-179 (error) A physical-only cell instance %s (0x%x) has logical connections.

DESCRIPTION

This error occurs because a physical-only leaf cell instance has logical connections. A physical-only cell instance is not allowed to connect to logical nets.

WHAT NEXT

If this CEL was generated by Astro/JupiterXT or by an IC Compiler version before b2008.09, convert it into version b2008.09 by using the **convert_mw_lib** command in IC Compiler version b2008.09. Contact Synopsys Support if the issue remains unresolved after converting.

MWDC-180 (error) A non-physical-only cell instance %s (0x%x) has no parent hierarchy.

DESCRIPTION

This error occurs because a non-physical-only leaf cell instance does not belong to any hierarchy.

WHAT NEXT

If this CEL is generated by Astro/JupiterXT, run the **astRepairHierPreservation** command. If the CEL is generated by IC Compiler or if running **astRepairHierPreservation** in Astro/JupiterXT does not resolve the issue, contact Synopsys Support.

MWDC-181 (warning) Unable to support the type %srotate counter-clockwise %d degree, cell %s.

DESCRIPTION

The orientation of the following types currently can’t been fully supported, it will

been treated as orientation unknow: rotate counter-clockwise 45 degree rotate counter-clockwise 135 degree rotate counter-clockwise 225 degree rotate counter-clockwise 315 degree mirror, then rotate 45 degree mirror, then rotate 135 degree mirror, then rotate 225 degree mirror, then rotate 315 degree

WHAT NEXT

Please contact Synopsys Support.

MWDC-182 (Error) PG %s %s(0x%x) of %s %s(0x%x) is connected with multiple %s nets: net1 is %s(0x%x) and net2 is %s(0x%x).

DESCRIPTION

PG pin should only connected with one flat net, you receive this message because in the MW CEL, the indicated PG pin is connected to more than one flat nets.

WHAT NEXT

Check the MW CEL and correct the connection.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-183 (Error) Hierarchical Tie Net %s(0x%x) connected as output %s %s(0x%x) of hier cell %s(0x%x)(hiConn net for port).

DESCRIPTION

You receive this message due to a Hier Tie Net is connected to output pin or as output port hiConn net. which is not supported.

WHAT NEXT

Check the MW CEL and correct the connection.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-184 (Error) Hierarchical net %s (0x%x) has no type.

DESCRIPTION

You receive this message due to a Hier Tie Net in MW CEL has no/Unknown net type.

WHAT NEXT

Check the MW CEL and correct the connection.

MWDC-185 (Error) Flat PG net %s(0x%x) contains %s pin %s(0x%x) of cell instance %s(0x%x).

DESCRIPTION

You receive this message due to the Flat PG net in the MW CEL contains VDD/GND pins. The leaf level VDD/GND pins should not be stored in the Flat PG net.

WHAT NEXT

Check the MW CEL and correct the connection.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-186 (Error) Flat %s net %s (0x%x) associated with Hier %s Net %s (0x%x).

DESCRIPTION

You receive this message due to the Flat net is associated with wrong type of Hier net.

WHAT NEXT

Check the MW CEL and correct the connection.

MWDC-187 (Error) Flat %s net %s (0x%x) associated with

multiple Direct Hier %s Nets.

DESCRIPTION

You receive this message due to the Flat Tie net is associated with multiple Direct Hier Tie nets. only one is allowed in the MW CEL.

WHAT NEXT

Check the MW CEL and correct the connection.

MWDC-188 (Error) Flat %s net %s (0x%x) not associated with any coresponding type Hier Net.

DESCRIPTION

You receive this message due to the Flat net is not associated with any coresponding type of Hier Net.

WHAT NEXT

Check the MW CEL and correct the connection.

MWDC-189 (Error) PG pin %s(0x%x) of cell instance %s(%x0x) has broken flat/hier net connection, the pin is connected with Hier Net %s(0x%x) and Flat Net %s(0x%x), but the Hier Net %s(0x%x) is connected with Flat Net %s(0x%x).

DESCRIPTION

You receive this message because the hier/flat net cross hierarchy connection is broken. The pin connected to the Hier net and the Flat net, but the Hier and Flat nets are not associated with each other.

WHAT NEXT

Check the MW CEL and correct the connection.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to

retrieve the name of the object.

MWDC-190 (warning) Nets %d(NAME: %s)connected to ports %d(TYPE: %s) and %d(TYPE: %s) are not of same type even though they are connected to same physical net.

DESCRIPTION

The ports connected to one net have different type.

WHAT NEXT

Please contact Synopsys Support.

MWDC-191 (Error) Hierarchical Tie Net %s(0x%x) connected as input port %s(0x%x) of hier cell %s(0x%x) (loConn net of port).

DESCRIPTION

You receive this message due to a Hier Tie Net is connected to input pin or as input port loConn net which is not supported.

WHAT NEXT

Check the MW CEL and correct the connection.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-192 (Information) CEL Checker is disabled.

DESCRIPTION

CEL Checker is disabled by mw_enable_cel_check control.

MWDC-193 (Error) P/G pin %s(0x%x) of cell instance %s(0x%x)

connected to non-P/G net %s(0x%x).

DESCRIPTION

You get this message because in the MW CEL, the pin is PG pin type, but it’s connected to a net which is not PG net type.

WHAT NEXT

Check the MW CEL and correct the connection.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-194 (Error) Port %s(0x%x) of hier cell %s(0x%x) %s net %s(0x%x) is invalid.

DESCRIPTION

The particular connected net of the Hierarchical port is not a valid net in MW CEL.

WHAT NEXT

Check the MW CEL and correct the connection.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-195 (Error) Port %s(0x%x) of hier cell %s(0x%x) on hier net %s (0x%x) is invalid.

DESCRIPTION

The particular hierarchical port attached with the hierarchical net is not a valid net in MW CEL.

WHAT NEXT

Check the MW CEL and correct the connection.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-196 (Error) Master port %x of port %s(0x%x) of hier cell %s(0x%x) is invalid.

DESCRIPTION

The particular port’s Master is not a valid object in MW CEL.

WHAT NEXT

Check the MW CEL and correct the connection.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-197 (Warning) Hier Net %s (0x%x) with multiple driver 0x%x and 0x%x.

DESCRIPTION

You get this message because ther hierachical net has multiple drivers as listed.

WHAT NEXT

Check the MW CEL and correct the connection.

MWDC-198 (Error) Flat net 0x%x is connected with pin 0x%x but the pin is not listed in the flat net.

DESCRIPTION

You get this message because the pin has the flat net connection but from the flat net pin connection, the pin is not listed. PG pin will not be listed in flat PG net, this Error won’t be reported for such case.

WHAT NEXT

Check the MW CEL and correct the connection.

MWDC-199 (Error) %s %s %s(0x%x) of %s %s(0x%x) connected net %s(0x%x) not with %s type.

DESCRIPTION

You get this message because the PG pin or port connected net does not have same PG polarity type or is not a PG net.

WHAT NEXT

Check the MW CEL and correct the connection.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-200 (Error) Non-PG %s %s (0x%x) is driving PG net %s (0x%x).

DESCRIPTION

You get this message because the PG net is driven by a non-PG type of pin or port.

WHAT NEXT

Check the MW CEL and correct the connection.

MWDC-201 (Error) Flat net %s(0x%x) is connected with %s %s(0x%x) of %s %s(0x%x) but the pin is not listed in the flat net.

DESCRIPTION

You receive this message because the flat net connection is attached in the pin, but the pin is not listed in the flat net pin connection attachment.

WHAT NEXT

Check the MW CEL and correct the connection.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-202 (Error) Flat net %s(0x%x) is connected with %s %s(0x%x) of %s %s(0x%x) but the pin is listed in the flat net %s(0x%x).

DESCRIPTION

You receive this message because the flat net connection is attached in the pin, but the pin is listed in another flat net.

WHAT NEXT

Check the MW CEL and correct the connection.

MWDC-203 (Error) SCANDEF stored in DB is not updated to design.

DESCRIPTION

You receive this message because SCANDEF and design stored in DB are asynchronous.

WHAT NEXT

Try remove_scan_def before reloading design.

MWDC-204 (Error) There is an inconsistency with regards to cover/bump cover cell type between cell instance %s and its master. The cover/bump cover cell info on master will be used

as golden.

DESCRIPTION

You get this message because there is an inconsistency between cell instance and its master ragarding the cover/bump cover cell type. In ICC, the cover/bump cover cell type is always taken from cell masters.

WHAT NEXT

Regenerate the MW CEL

MWDC-205 (Warning) Cover/bump cover cells are not marked fixed, a fixed placement status is now derived.

DESCRIPTION

You get this message because there is a cover/bump cover cell which does not have a fixed placement status. Since ICC does not intend to place and legalize these cells, a fixed placement status is now derived on such cover/bump cover cells.

WHAT NEXT

Please mark the non-fixed cover/bump cover cells explicitly, or make sure if they are not a part of the logical netlist.

MWDC-206 (Error) Cover/bump cover cell %s is not placed.

DESCRIPTION

You get this message because there is an unplaced cover/bump cover cell in the logical netlist. Since ICC does not perform placement or legalization on these cells, a fixed placement status with valid placement location is required for such cover/bump cover cells.

WHAT NEXT

Please place these unplaced cover/bump cover cells explicitly, and mark them with fixed placement status. Or else, remove them from the logical netlist.

MWDC-207 (Warning) Pad driver cells which are directly connected to universal bond pads are not marked fixed, a fixed placement status is now derived.

DESCRIPTION

You get this message because there are pad driver cells (they are directly connected to bond pads) which do not have a fixed placement status. Since ICC does not intend to place and legalize these cells, a fixed placement status is now derived on such pad driver cells.

WHAT NEXT

Please mark these non-fixed pad driver cells explicitly, or make sure if they are not directly connected to bond pads.

MWDC-208 (Error) Tie Net %s(0x%x) connected to an output pin %s(0x%x) of cell instance %s(0x%x).

DESCRIPTION

You receive this message due to a Tie Net is connected to output pin, which is not supported.

WHAT NEXT

Check the MW CEL and correct the connection.

Note that the hexadecimal value (0x%x) specifies the object id. For cell/net/port, you can use UI command "get_cells/get_nets/get_ports -object_id $object_id" to retrieve the name of the object.

MWDC-209 (Warning) Failed to dump cell attach file %s to unix filename %s.

DESCRIPTION

Attempt was made to dump a cell attached file with pseudo-access name to a file with a unix filename, but the attempt failed.

WHAT NEXT

Contact your Synopsys technical support representative.

MWDC-210 (Error) %s failed in %s

DESCRIPTION

An internal error occured.

WHAT NEXT

Contact your Synopsys technical support representative.

MWDC-211 (warning) cell %s is already attached to %s %s; skip attaching to %s %s.

DESCRIPTION

You receive this warning message when a cell is attached to multiple plangroups or movebounds in the database. While being loaded, the cell will just be considered to be attached to the first plangroup or movebound it hits, and the relationships to other plangroups or movebounds will be ignored.

WHAT NEXT

You need check the design by UI command "get_cells of [get_plan_group/get_bounds $name]" or using "write_def -regions_groups -o $DEF". And you can fix it by reading in a DEF with correct group and cell mapping, or using plangroup/bound editing commands.

MWDC-212 (error) hier port 0x%x and 0x%x of hier cell %s(0x%x) have the same name %s.

DESCRIPTION

You receive this error message when a hierarchical cell has two port of the same name. This is not allowed.

WHAT NEXT

You need to remove the duplicate port and correct the net connections with netlist editing commands. If it does not work, please contact Synopsys Support.

MWDC-228 (Warning) The non-constant Milkyway net '%s' (0x%x) has a leaf load pin '%s' but no driver. It will now be driven by logic zero.

DESCRIPTION

The named net connects to a load pin (input or inout) of a cell instance in the target_library, but the net has no driver.

Such nets are given a logic zero driver by default. The net is considered non-constant because the name is not equal to either variable **mw_logic0_net** or **mw_logic1_net**.

WHAT NEXT

It is most likely it is a signal net that simply has no driver. The user may want to make an explicit assignment in the original HDL or ignore this message.

MWDC-229 (Warning) The non-constant Milkyway net '%s' (0x%x) has a hierarchical load pin '%s' but no driver. It will now be driven by logic zero.

DESCRIPTION

The named net connects to a load pin (input or inout) of a cell instance in the target_library, but the net has no driver.

Such nets are given a logic zero driver by default. The net is considered non-constant because the name is not equal to either variable **mw_logic0_net** or **mw_logic1_net**.

WHAT NEXT

It is most likely it is a signal net that simply has no driver. The user may want to make an explicit assignment in the original HDL or ignore this message.

NG-1 (error) Generation error: %s (%s).

DESCRIPTION

WHAT NEXT

NLE-001 (Error) Specified pin '%s' is not connected to net '%s'.

DESCRIPTION

This error message occurs when all the pins specified in the **<pin object>** option is not connected to same net which is being buffered.

WHAT NEXT

May be the given pins are all connected electrically but are on different hierarchy. Check the pins connected to net being buffered using **all_connected** command.

SEE ALSO

insert_buffer(2)
all_connected(2)

NLE-002 (Warning) buffer cell '%s' has both inverted and non-inverted outputs connected.

DESCRIPTION

This warning message occurs when the buffer cell being removed has both its inverter and non-inverter output pin being used up.

WHAT NEXT

Such cells will not be removed by the **remove_buffer** command

However, if you want to remove such cells, disconnect one of the pins

SEE ALSO

remove_buffer(2)
disconnect_net(2)

NLE-003 (Warning) Could not derive location for the new buffer

cells; placing them at location {0 0}.

DESCRIPTION

This warning message occurs when the tool is not able to derive the location for new buffer cells.

WHAT NEXT

This is only a warning message.

However, if you want to the new cells placed near to the driver pin of the net being buffered, check the location of the driver cell or assign the location for the new cells directly using **-location** option.

SEE ALSO

insert_buffer(2)
set_cell_location(2)

NLE-004 (Error) library cell '%s' has dont_use attribute set on it.

DESCRIPTION

This error message occurs when the specified reference lib_cell has the dont_use attribute set to true.

WHAT NEXT

use other similar equivalent lib_cells from the target library or remove the dont_use attribute and then use the lib_cell.

SEE ALSO

insert_buffer(2)
size_cell(2)
remove_attribute(2)
set_dont_use(2)

NLE-005 (Error) net '%s' is driving multiple cells.

DESCRIPTION

This error message occurs when the net driven by a inverter cell is driving more

than one cell.

WHAT NEXT

remove_buffer can only remove inverter-pair(s) or buffer(s) introduced by the **insert_buffer** command. To remove all the buffers in the path use **remove_buffer_tree** command.

SEE ALSO

remove_buffer(2)
insert_buffer(2)
remove_buffer_tree(2)

NLE-006 (Error) net '%s' should have one driver pin

DESCRIPTION

This error message occurs when the operating net has more than one driver pin or the net has no valid driver pin.

WHAT NEXT

remove_buffer and **insert_buffer** cannot operate on nets having multiple driver pins.

SEE ALSO

remove_buffer(2)
insert_buffer(2)

NLE-007 (Error) pin '%s' is not associated with the buffer tree path of the net '%s'.

DESCRIPTION

This error message occurs when the specified **-to** pin/port is not connected to the buffer tree path starting from the given net.

WHAT NEXT

check if the specified pin/port is on the buffer tree path using **report_buffer_tree** command.

SEE ALSO

remove_buffer(2)
report_buffer_tree(2)

NLE-008 (Error) No buffer(s) or inverter-pair(s) connected to net '%s'.

DESCRIPTION

This error message occurs when the **remove_buffer** command is not able to find any buffer or inverter-pair for the given net.

WHAT NEXT

Report the buffer tree for the net using **report_buffer_tree** command and see if there are any buffer or inverter-pairs associated with it.

SEE ALSO

remove_buffer(2)
report_buffer_tree(2)

NLE-009 (Error) Could not size '%s' ('%s') with '%s'.

DESCRIPTION

This error message occurs when the specified **lib_cell** is not logically matching with the library cell of the cell being sized.

WHAT NEXT

Check for the equivalence of library cells using **get_alternative_lib_cells** command.

• Check if their is a dont_touch or dont_use attribute for the specified library cell in the used scenarios. Remove the dont_touch and dont_use attributes settings ("remove_attribute") for the used library cell.

• Check the target library settings and the operating conditions. Make sure that the libraries which contain the specified library cell are included in target_library settings (variable "target_library" or command "set_target_library_subset") for each of the scenarios accordingly.

SEE ALSO

size_cell(2)
get_alternative_lib_cells(2)

NLE-010 (Error) library cell '%s' is not a buffer or an inverter.

DESCRIPTION

You recieve this error message, if the library cell matching the specified name is not a buffer or inverter library cell from the target library.

WHAT NEXT

Check to make sure that the target_libray is set correctly and use the **get_buffers** command to get the buffers and inverters that are available in the target library.

SEE ALSO

insert_buffer(2)
get_buffers(2)
report_lib(2)

NLE-011 (Error) Could not assign location (%d, %d) to the cell '%s'.

DESCRIPTION

You recieved this error message because the named cell could not be assigned the specified location.

WHAT NEXT

Perform a coarse placement on the cell to assign a new location for the cell.

SEE ALSO

insert_buffer(2)

NLE-012 (Warning) Net '%s' is not routed.

DESCRIPTION

This warning message occurs when the named net is not routed.

WHAT NEXT

This is only a warning message.

However, if the result is not what you intended. route the design or ECO route the net.

SEE ALSO

insert_buffer(2)
route_eco(2)
route_group(2)

NLE-013 (Error) Error in argument '%s'. '%s'.

DESCRIPTION

You recieved this error message because an option in the command has an incorrect value. Either the tool could not find the expected value for the argument or the number of arguments is invalid.

WHAT NEXT

Clarify the proper use of the option, see the man page of the command.

NLE-014 (Error) Cell '%s' has the dont_touch attribute set on it.

DESCRIPTION

You receive this error message if **remove_buffer** or **size_cell** encounters a cell that has dont_touch attribute set to **true** on it. The **dont_touch** attribute is designed to protect cells from being modified or optimized, so these commands exit without making any changes.

WHAT NEXT

If you want to remove the cell or size the cell, remove the **dont_touch** attribute, either with **remove_attribute** or by executing **set_dont_touch false**.

SEE ALSO

remove_buffer(2)
size_cell(2)
remove_attribute(2)
set_dont_touch(2)

NLE-015 (Error) Net '%s' has the dont_touch attribute set on it.

DESCRIPTION

You receive this error message if **remove_buffer** or **insert_buffer** encounters a net that has dont_touch attribute set to **true** on it. The **dont_touch** attribute is designed to protect nets from being modified or optimized, so these commands exit without making any changes.

WHAT NEXT

If you want to remove the net or buffer the net, remove the **dont_touch** attribute, either with **remove_attribute** or by executing **set_dont_touch false**.

SEE ALSO

remove_buffer(2)
insert_buffer(2)
remove_attribute(2)
set_dont_touch(2)

NLE-016 (Warning) buffer cell '%s' is not connected to any net.

DESCRIPTION

This warning message occurs when the buffer cell being removed is not connected is not driving any other cells in the netlist.

WHAT NEXT

Such cells will not be removed by the **remove_buffer** command

However, if you want to remove such cells, consider using **remove_cell** command

SEE ALSO

remove_buffer(2)
remove_cell(2)
disconnect_net(2)

NLE-017 (Error) Could not derive number of buffers.

DESCRIPTION

This error message occurs when **-max_route_lenght** option is used on a net that is not routed or trying to buffer a net that does not have RC-tree information annotated.

WHAT NEXT

see if you have **NLE-012** or **NLE-018** messages, remove those warnings.

SEE ALSO

insert_buffer(2)
NLE-012(n)
NLE-018(n)

NLE-018 (Warning) Could not traverse the RC tree of the net '%s'.

DESCRIPTION

This warning message occurs when the named net is not extracted.

WHAT NEXT

This is only a warning message.

However, if the result is not what you intended. Extract the design by runing **extract_rc** before executing insert_buffer command.

SEE ALSO

insert_buffer(2)
extract_rc(2)
NLE-012(n)

NLE-019 (Warning) Not relinking cell '%s'.

DESCRIPTION

This warning message occurs when the above cell is already linked with the specified target library cell.

WHAT NEXT

This is only a warning message.

However, the result is not what is expected, specify the reference library cell different from the current one. Query the possible alternative library cells for the above cells by using **get_alternative_lib_cells** and use one of the library cells from its output.

SEE ALSO

size_cell(2)
get_alternative_lib_cells(2)

NLE-020 (Error) net '%s' does not have any loads.

DESCRIPTION

This error message occurs when the operating net has no load pin connected to it.

WHAT NEXT

insert_buffer will not buffer unconnected nets.

SEE ALSO

insert_buffer(2)

NLE-021 (Error) Could not find library cell '%s' matching the operating condition.

DESCRIPTION

This error message occurs when the given library cell does not have an equivalent library cell matching the operation condition of the net being buffered.

WHAT NEXT

• Check the target library settings and the operating conditions. Make sure that the libraries which contain the specified library cell are included in target_library settings (variable "target_library" or command "set_target_library_subset") for each of the scenarios accordingly.

• Check if their is a dont_touch or dont_use attribute for the specified library cell in the used scenarios. Remove the dont_touch and dont_use attributes settings ("remove_attribute") for the used library cell.

SEE ALSO

insert_buffer(2)
set_target_library_subset(2)
remove_attribute(2)

NLE-022 (Error) Could not find library cell '%s' matching the operating condition of cell '%s'.

DESCRIPTION

This error message occurs when the given library cell does not have an equivalent library cell matching the operation condition of the cell being sized.

WHAT NEXT

• Check the target library settings and the operating conditions. Make sure that the libraries which contain the specified library cell are included in target_library settings (variable "target_library" or command "set_target_library_subset") for each of the scenarios accordingly.

• Check if their is a dont_touch or dont_use attribute for the specified library cell in the used scenarios. Remove the dont_touch and dont_use attributes settings ("remove_attribute") for the used library cell.

SEE ALSO

size_cell(2)

set_target_library_subset(2)
remove_attribute(2)

NLE-023 (Info) Buffering entire segments of hierarchical nets driven by pin '%s'.

DESCRIPTION

This is an info message only. This occurs when *-repeater_distance* or *-divide_load_by* options is used and a hierarchical net or hierarchical pin is specified for **insert_buffer** command.

The *-on_route* option that is used along with *-repeater_distance* or *-divide_load_by* option works on the physical nets and hence the buffer can be introduced on any hierarchical net segment.

SEE ALSO

insert_buffer(2)

NLE-024 (Error) Could not find leaf driver pin associated with net '%s'.

DESCRIPTION

This error message occurs when their is no leaf driver pin for the hierarchical net segments starting from the given net.

WHAT NEXT

check if the hierarchical nets has at-least one pin with direction *out*.

SEE ALSO

insert_buffer(2)
get_nets(2)

NLE-025 (Warning) Need extraction information of net;

extracting RC values for the design.

DESCRIPTION

This warning message occurs when **insert_buffer** is issued with *-on_route* option without extracting RC values for the design.

WHAT NEXT

This is only a warning message.

If you don't want this message to appear do **extract_rc** prior to issuing **insert_buffer** command.

SEE ALSO

insert_buffer(2)
extract_rc(2)

NLE-026 (Error) Extraction information is not initialized.

DESCRIPTION

This error message occurs when the RC values for the design is not initialized correctly.

WHAT NEXT

See if any problem in the extraction; running of **extract_rc** command. Check if the net being buffered is ignored for extraction of RC values or if the extraction was interrupted prematurely.

SEE ALSO

insert_buffer(2)
extract_rc(2)
get_nets(2)

NLE-027 (Warning) Specified location (%d, %d) for buffer/

inverter is outside the core area.

DESCRIPTION

This warning message occurs when the coordinates provided for *-location* option of **insert_buffer** command is not inside the core area of the design.

WHAT NEXT

This is only a warning message.

If you don’t want this message to appear provide locations for the buffers which are inside the core area.

SEE ALSO

insert_buffer(2)
set_cell_location(2)

NLE-028 (Warning) No buffer (inverters) were inserted.

DESCRIPTION

This warning message occurs when the **insert_buffer** command could not insert any buffers. For example, the **repeater_distance** may be too big to insert any buffers.

WHAT NEXT

Please correct the arguments and rerun the command.

SEE ALSO

insert_buffer(2)

NLE-030 (Error) Load capacitance of buffer ’%s’ is greater than total capacitance of the net ’%s’.

DESCRIPTION

This error message occurs when **insert_buffer** *-divide_load_by* option is used and the capacitance of the specified buffer is greater than the total capacitance of the net being buffered.

Total net capacitance = Net capacitance + Pin capacitance(s) of all connected load pin(s)

This message means, specified buffer’s capacitance is too large to be used for reducing(dividing) the load capacitance of the net.

WHAT NEXT

a) Use different library buffer cell which has less capacitance.

b) Make **insert_buffer** to ignore pin capacitance matching (use *-ignore_pin_cap* option)

SEE ALSO

insert_buffer(2)
extract_rc(2)
get_attribute(2)
get_buffers(2)

NLE-031 (Warning) Load capacitance of buffer ’%s’ is greater than required capacitance of the net ’%s’.

DESCRIPTION

This warning message occurs when the capacitance of the specified buffer is greater than the required net capacitance.

Required net capacitance = Total net capacitance / *-divide_load_by* value

Total net capacitance = Net capacitance + Pin capacitance(s) of all connected load pin(s)

The **insert_buffer** command would continue with load based buffer insertion on the specified net. But this message would signify that more number of buffers may be introduced due to high load capacitance of buffer(s) being introduced.

WHAT NEXT

This is only a warning message, if the result is not what you expected.

a) Use different library buffer cell which has less capacitance.

b) Make **insert_buffer** to ignore pin capacitance matching (use *-ignore_pin_cap* option)

SEE ALSO

insert_buffer(2)
extract_rc(2)
get_attribute(2)
get_buffers(2)

NLE-033 (Warning) Library cell '%s' has dont_use attribute.

DESCRIPTION

This warning message occurs when the specified library cell for **insert_buffer** or **size_cell** command has a 'dont_use' attribute set to true.

WHAT NEXT

This is only a warning message, if the result is not what you expected.

a) Use other equivalent library cell which does not have dont_use set.

b) remove the dont_use setting on the library cell using **remove_attribute** command.

SEE ALSO

insert_buffer(2)
size_cell(2)
report_lib(2)
remove_attribute(2)
get_alternative_lib_cells(2)
get_buffers(2)

NLE-034 (Warning) Library cell '%s' is an inverter; assuming -inverter_pair option.

DESCRIPTION

You recieve this message, if you have specified an inverter library cell for *buffer_lib_cell* option without specifying the *-inverter_pair* option.

WHAT NEXT

This is just a warning message, if result is not what you expected.

a) specify a library buffer cell.

b) specify -inverter_pair option along with inverter library cell.

SEE ALSO

insert_buffer(2)
get_buffers(2)
report_lib(2)

NLE-035 (Error) Could not find any common segment of the route driving the pins {%s}.

DESCRIPTION

This error message occurs when **insert_buffer** *-on_route* option is used on a multi load nets and the tool could not find any route segment where buffer can be inserted honoring the above load pins.

Sometimes the route topology of a net can be such that no buffers can be introduced preserving the logical hierarchy.

WHAT NEXT

a) Check the physical distribution of the above load pins and select only those pins/nets that can be buffered based on the route topology.

b) Manually specify the location where the buffer needs to be inserted by using *-location* option.

SEE ALSO

insert_buffer(2)
set_cell_location(2)

NLE-036 (Error) no net connected to pin/port '%s'.

DESCRIPTION

This error message occurs when trying to place buffer connected to a pin which is not connected by a valid net.

WHAT NEXT

insert_buffer can only insert buffer on a net which is driven by a leaf pin or port. please check if the netlist is correct and the pin or net being buffered is connected correctly.

SEE ALSO

all_connected(2)
insert_buffer(2)

NLUTDB-1 (error) Invalid I/P name at position '%d' of lut_function.

DESCRIPTION

LUT has invalid input port name.

WHAT NEXT

Check the target_library.

NLUTDB-2 (error) Unknown symbol encountered at position '%d' in lut_function.

DESCRIPTION

LUT has an unknown symbol in it's lut_function.

WHAT NEXT

Fix the lut_function in the input(edif/lib/db..).

NLUTDB-3 (warning) Right parenthesis is missing at position '%d' of lut_function.

DESCRIPTION

Right parenthes is missing in the lut function.

WHAT NEXT

Add missing parenthesis to the lut_function.

NLUTDB-4 (error) Unexpected error at position '%d' of

lut_function.

DESCRIPTION

Unexpected error.

WHAT NEXT

Contact Support.

NLUTDB-5 (error) Missing lut_bag in library design %s.

DESCRIPTION

The tool issues this error when the lut_bag is missing in the library design. The error can be caused by Library compiler or from the library.

WHAT NEXT

Contact vendor to get the correct library.

NLUTDB-7 (error) lut_function to EQN conversion failure, empty EQN.

DESCRIPTION

The tool issues this error message when the lut_function to EQN conversion has failed. Make sure the lut_function is supported by the tool.

WHAT NEXT

See the set_lut_function command for the valid symbols supported by the lut_function format.

NLUTDB-8 (error) EQN to lut_function convertion failure, leads

to empty lut_function.

DESCRIPTION

EQN to lut_function convertion failure, leads to empty lut_function. EQN string may have following symbols :- *, (,), ~, +

EXAMPLE

Following represents the same LUT functionality :-

```
EQN -> ((I0 * I1) + (I2 * ~I3) + (I0 * I1 * I2 * I3))
lut_function -> ((I0 I1) + (I2 I3') + (I0 I1 I2 I3))
INIT -> 88F8
```

WHAT NEXT

NLUTDB-9 (error) Invalid pin name '%s' while describing LUT functionality.

DESCRIPTION

Invalid pin name used while describing LUT's functionality. LUT's lut_function/EQN can only be described in terms of LUT pin names.

WHAT NEXT

Check the library for valid LUT pin names.

NLUTDB-10 (error) The cell %s is not a LUT (Look Up Table), or the cell is not linked.

DESCRIPTION

The tool issues this error message when the cell is not a LUT, or the cell it not linked. Make sure the target cell is a LUT primitive, or use the link command to link cells to its library.

WHAT NEXT

NLUTDB-11 (error) Invalid INIT value provided for LUT cell %s.

DESCRIPTION

INIT is a format to describe LUT’s functionality. It is a string of hex digits, derived from the truth table of a given function.

EXAMPLE

If a 2-input AND functionality is built using a 2-input LUT, then the corresponding lut_function representation would be (I0 I1) and the EQN representation would be (I0 * I1). Table 1 shows the truth table representation of this function. The INIT value of this function would be computed by traversing the truth table output column in bottom-up fashion, that is, 1000 binary, which is equivalent to hexadecimal 8.

Table 1

I1	I1	O
0	0	0
0	1	0
1	0	0
1	1	1

WHAT NEXT

NLUTDB-12 (error) %s-%s at column number ’%d’ of ’%s’ ’%s’

DESCRIPTION

This indicates an Error in any of the below procedures :-

1. lut_function to EQN convertion
2. EQN to lut_function convertion
3.Mixed format to lut_function

Valid symbols supported in these formats are listed below.

lut_function format
AND space

```
      OR    +
      INV   ’
      Misc. (,),0,1

EQN format
 AND *
 OR +
 INV ~
 Misc. (,),0,1




Mixed format
 AND *, &, space
 OR +, |
 INV ~, !, ’
 XOR  ^,@
 Misc. (,),0,1



INIT format
      Hex Number to indicate the functionality 0-9 & A-F
```

SEE ALSO

set_lut_function (2)

NMA-2 (error) Negative max_length rule '%d' is invalid.

DESCRIPTION

You receive this message because the **change_names** command has found a negative **max_length** rule, so the names remain unchanged.

WHAT NEXT

Examine the **define_name_rules max_length** argument and provide a valid rule value.

SEE ALSO

change_names (2), **define_name_rules** (2).

NMA-3 (error) The max_length rule '%d' is invalid: It must be greater than 8.

NMA-4 (error) Special rules '%s' is invalid.

NMA-5 (error) Range specified in string '%s' is invalid.

NMA-6 (error) Replacement character '%c' is invalid. It is not an allowed character according to existing rules.

NMA-7 (error) String '%s' is invalid: At least 10 chars must be

allowed.

NMA-8 (information) %d names changed in design '%s'.

WHAT NEXT

This is an informational message only. No action is required on your part.

NMA-9 (information) No names changed in design '%s'.

WHAT NEXT

This is an informational message only. No action is required on your part.

NMA-10 (error) A %s named '%s' already exists in design '%s'.

DESCRIPTION

You receive this message because the **change_names** command has found conflicting names between the proposed new name and existing old names (for example: bus bag name), so the name remains unchanged.

WHAT NEXT

To correct the error, edit your names file to ensure that it contains new names that do not exist in the design.

SEE ALSO

change_names (2).

NMA-11 (error) name mapping string '%s' is illegal.

DESCRIPTION

You receive this message because the **change_names** command found an illegal name mapping string. The name remains unchanged.

WHAT NEXT

Replace the illegal name mapping string with a valid value.

SEE ALSO

change_names (2),

NMA-12 (error) Name mapping pattern string '%s' is illegal.

DESCRIPTION

You receive this message because the **change_names** command found an illegal name mapping pattern string. The names remained unchanged.

WHAT NEXT

Provide a valid value for the name mapping pattern string.

SEE ALSO

change_names (2).

NMA-13 (warning) The bus_naming_style variable is not defined. Use '%s' in the change_names command.

DESCRIPTION

You receive this message because the **bus_naming_style** variable is not defined. The **change_names** command uses this variable to handle bus type names. If it is not defined, **change_names** uses the "%s[%d]" default value during a name change. However, if the **define_name_rules** command **-special** option contains the predefined **sge_vhdl** *output_format*, **change_names** uses the the "%s(%d)" default value.

WHAT NEXT

No action is necessary.

SEE ALSO

change_names (2), **define_name_rules** (2), **bus_naming_style** (3).

NMA-14 (warning) The bus_naming_style variable contains characters that are not defined within the "-allowed" character set in the current name rule. They are found in the following type(s) of objects: ’%s’.

DESCRIPTION

You receive this message because the **define_name_rules** command has changed the bus naming style, so you must change the **bus_naming_style** variable to conform to the new one.

WHAT NEXT

Execute the **help define_name_rules** command for more detail.

SEE ALSO

define_name_rules (2), **bus_naming_style** (3).

NMA-15 (warning) Design ’%s’ has a duplicate reference ’%s’ that it ignores.

DESCRIPTION

You receive this message because the **change_names** command has been given a duplicate reference. It ignores the second reference.

WHAT NEXT

No action is necessary.

SEE ALSO

change_names (2).

NMA-16 (warning) In design %s, %s bus member ’%s’ has been

changed to ’%s’.

DESCRIPTION

You receive this message because the specified bus member name has been changed. By default, the **change_names** command gives a bus member the base name from its owning bus. Thus, a possible reason for this change is that the member name did not previously use the base name from its owning bus.

WHAT NEXT

To recover the original name(s) of the bus member(s), reload your original **db** file and start again. In the future, to see the name changes without actually implementing them, first execute the **report_names** command; then, to prevent **change_names** from making unwanted name changes to bus members, set the **change_names_dont_change_bus_members** environment variable to *true*. For more information, see the **change_names_dont_change_bus_members** man page.

SEE ALSO

change_names (2), **change_names_dont_change_bus_members** (3).

NMA-17 (warning) File %s, line %d: Can’t find %s ’%s’ in %s ’%s’.

NMA-18 (warning) The variable "%s" was set to "%s" from "".

NMA-19 (error) File %s, Line %d: The names file is missing an expected delimiter ’%s’. Reading of the file has been terminated.

DESCRIPTION

You receive this message because your names file apparently contains **use delimiter:true** as the first line, so the command expects the fifth (delimiter) field. However, it has not found a delimiter where it expected one and, consequently, has stopped reading the file.

The normal names file format has four fields, each separated by a space:

<design_name> <object_type_string> <object_name> <new_name>

You have the option of adding a fifth field for a delimiter, currently a semicolon <;>. To specify the delimiter field, add **use delimiter:true** as the first line of the names file, as in the following example:

```
use delimiter:true
Design      Type        Object      New Name
-------------------------------------------------------------------------
TOP         busport     DATAIN      NEW_DATAIN ;
```

WHAT NEXT

You can correct the error in either of the two following ways:

- Edit your names file to add the missing delimiter (;), and re-execute the command.

- Edit your names file to delete the first line **use delimiter:true**, remove any other delimiters, and reexecute the command.

For more information about the names file format, see the **change_names** man page.

SEE ALSO

change_names (2).

NMA-20 (error) File %s, Line %d: The names file contains an unexpected delimiter '%s'. Reading of the file has been terminated.

DESCRIPTION

You receive this message because your names file apparently contains **use delimiter:true** as the first line, so the command expects the fifth (delimiter) field. However, the command has found a delimiter in the wrong field and, consequently, has stopped reading the file.

The normal names file format has four fields, separated by a space:

<design_name> <object_type_string> <object_name> <new_name>

You have the option of adding a fifth field for a delimiter, currently a semicolon <;>. To specify the delimiter field, add **use delimiter:true** as the first line of the names file, as in the following example:

```
use delimiter:true
```

```
Design          Type            Object          New Name
_____________________________________________________________
TOP             busport         DATAIN          NEW_DATAIN ;
```

WHAT NEXT

To correct the error, edit your names file to ensure that all delimiters are in the fifth field, and reexecute the command. For more information about the names file format, see the **change_names** man page.

SEE ALSO

change_names (2).

NMA-21 (warning) No valid name changes found in names file '%s'.

DESCRIPTION

You receive this message because the specified names file contains invalid name changes. The **change_names** command has found invalid name changes and has stopped reading the names file.

WHAT NEXT

To correct the error, edit your names file to ensure that the name changes in the file are valid. For more information about the names file format, see the **change_names** man page.

SEE ALSO

change_names (2).

NMA-22 (error) Too many errors in names file '%s'.

DESCRIPTION

You receive this message because the specified names file contains too many errors, so the names remain unchanged.

WHAT NEXT

To correct the error, edit your names file to ensure that it contains the correct

information required by the **change_names** command. For more information about the names file format, see the **change_names** man page.

SEE ALSO

change_names (2).

NMA-23 (information) %d names changed using names file '%s'.

WHAT NEXT

This is an informational message only. No action is required on your part.

NMA-24 (warning) File %s,
line %d; and
File %s,
line %d: Unsupported multiple names files.
%s '%s' is the new name of %s '%s' in %s '%s'.

NMA-25 (error) Cannot open '%s' names file.

DESCRIPTION

You receive this message because the **change_names** command cannot open the names file to read. Consequently, it has stopped performing changing names.

WHAT NEXT

Check the read permission for the names file.

SEE ALSO

change_names (2).

NMA-26 (warning) File %s,

Line %d, ObjectType %s,
BusMemberName '%s', BusPortName '%s':
The change_names command cannot be applied to individual bus members.
Specify the BusPortName instead.

DESCRIPTION

You receive this message because the **change_names** command does not allow individual bus members to be changed. In versions earlier than v3.1a, users could change bus members, and then the bus port was automatically changed. However, in the current version you cannot change individual bus members. You must change the entire bus, and then the names of bus members are simultaneously changed. Error message UIMG-32 warns users that they cannot change only a bus member.

WHAT NEXT

Instead of changing an individual bus member, specify the BusPortName.

SEE ALSO

change_names (2),

NMA-27 (warning) File %s,
line %d: Cannot find %s name '%s'.

NMA-28 (warning) File %s, line %d; and
File %s, line %d:
Duplicate change for %s '%s'.
The previous change is overwritten by the latest one.

NMA-29 (warning) File %s,

line %d: Unsupported class string ’%s’ in ’%s’.

NMA-30 (error) Invalid class string ’%s’.

NMA-31 (error) ’%s’ does not specify a unique %s.
Use the complete "full_file_name:%s_name" specification.

NMA-32 (error) Design ’%s’ is not in the system.

NMA-33 (warning) File %s, Line %d:
The %s named ’%s’ already exists in design ’%s’.

NMA-34 (error) File %s, Line %d:
The names file contains an incomplete line.
Reading of the file has been terminated.

DESCRIPTION

You receive this message because the command has not found an entry in one or more of the expected nondelimiter fields in the names file and has stopped reading the file. The names file can have one of the following two formats:

```
<design_name> <object_type_string> <object_name> <new_name>
<design_name> <object_type_string> <object_name> <new_name> <";">
```

WHAT NEXT

Edit the names file to add the missing field(s), and reexecute the command. For more information about the names file format, see the **change_names** man page.

SEE ALSO

change_names (2).

NMA-35 (error) File %s, Line %d:
This line has no effect on changing names in the %s command.

DESCRIPTION

You receive this message because the specified line does not have any effect on changing any name. This is an informational message.

WHAT NEXT

If this behavior is intended, no action is necessary.

NMA-36 (error) Cannot open the '%s' names file for writing.

DESCRIPTION

You receive this message because the change_names cannot open the names file to write and has stopped performing changing names.

WHAT NEXT

Check the write permission for the names file.

SEE ALSO

change_names (2).

NMA-37 (warning) Multiple changes to '%s'.

NMA-38 (error) Option target_bus_naming_style '%s' is invalid.

DESCRIPTION

You receive this message because only %s[%d], %s(%d), %s_%d, and %s_%d_ are supported **target_bus_naming_style** options.

WHAT NEXT

Use the valid options.

NMA-39 (warning) In design %s, the %s bus member '%s' contains a member '%s' with a different base name.

DESCRIPTION

You receive this message because the specified bus name contains a member with a different base name, so the **change_names** command uses this member instead of the base name from the owning bus.

SEE ALSO

change_names (2).

NMA-40 (warning) New net %s is added for design %s.

DESCRIPTION

You receive this message because either the design has an unconnected port or the port cannot be mapped due to a VHDL semantic error. An intermediate signal is created. This error message applies only to a port name that is designed to comply with the VHDL syntax rule.

NMA-41 (warning) Port or net name changed from %s to %s.

DESCRIPTION

You receive this message because a port or net has had a name change to comply with the VHDL syntax or semantic rule.

NMA-42 (warning) In design %s, net %s contains '%d' different bus bags.

DESCRIPTION

This warning message indicates that the specified net name contains more than one bus bag. The net is ignored.

WHAT NEXT

Check your design and make the appropriate changes to avoid this warning.

SEE ALSO

change_names (2).

ONH-001 (error) Flow error - (%s).

DESCRIPTION

This is a general error message that occurs when the command encountered errors in executing its sub-tasks and hence is unable to complete the flow.

WHAT NEXT

If there are other error messages generated by this command prior to this error, resolve those errors first and then try to re-run the command. If this is the only error message generated by the command, then it is likely an internal error. Please contact your technical support for further assistance.

SEE ALSO

none

ONH-002 (warning) Missing module type %s.

DESCRIPTION

This warning message indicates that command encountered a module while processing the input net-list and could not determine the type (such as soft macro, hard macro, IO, Standard cell, Black-Box etc). In this case, the command will proceed by assuming the type to be Black-box.

WHAT NEXT

If module type is expected to be defined, please check the object attributes in the Milkyway library. Black-boxes may need some values to be estimated for flow to work.

SEE ALSO

estimate_fp_black_boxes (2)

ONH-003 (error) File I/O error - (%s).

DESCRIPTION

This error message indicates that command was unable to perform file operation for the specified file.

WHAT NEXT

Check the file name and its path and verify that the directory allows file operations to be performed. To rectify, try changing the path/file name and then re-run the command.

SEE ALSO

none

ONH-004 (warning) Net hierarchy error - (%s).

DESCRIPTION

This warning indicates that the command encountered a hierarchical net with more than one parent net. This typically occurs when the command encountered an unexpected statement in the input net-list and performed an invalid action or encountered some other internal error.

WHAT NEXT

The command will try to auto-fix the problem by picking one of the parent nets and removing others. In order to avoid this message from recurring in future runs, first verify the input net-list consists of only supported syntax. If the input net-list is compatible, then this might indicate some internal error. Please consult with your technical support for further assistance.

SEE ALSO

none

ONH-005 (information) Net %s/%s is connected to instance %s

by floating ports only.

DESCRIPTION

This information message is given out when the command encounters net that is connected to an instance but the net does not have any corresponding lower hierarchy net inside the instance. For example if Cell A has net A1 which connects to instance B_1 (of Master B) via port B_1/A1. If master B has no internal net connected to its port A1 then the net A1 of Cell A is connected to a instance B_1 vis a floating port. This connection will not exist in flat netlist view.

WHAT NEXT

When debugging an incorrect output netlist, frequently the issue can be narrowed by inspecting these messages to see if non-floating ports have been incorrectly treated by the command as floating ports. This can help narrow the problem.

SEE ALSO

none

ONH-006 (error) Invalid value %s for option %s.

DESCRIPTION

This error message occurs when command options are specified invalid values.

WHAT NEXT

Please rectify the option value and re-run the command.

SEE ALSO

none

ONH-007 (warning) Conflicting options given. Will use option specified for %s. Ignoring following additional options given: %s"

DESCRIPTION

This warning message is triggered when command is invoked with a conflicting combination of options. The message clearly identifies which options are accepted and which are ignored as part of conflict resolution.

WHAT NEXT

This message does not need any action from user as command should automatically resolve the conflict and continue.

SEE ALSO

none

OPT-100 (error) %s has abnormally terminated.

DESCRIPTION

This message indicates that the synthesis command has terminated and has not written the intermediate design back to the database. Because the design has not been written back to the database, the current design is unchanged. The explanation for abnormal termination should have appeared in an error message previous to this one.

WHAT NEXT

Resolve errors and rerun optimization.

OPT-101 (error) The target library does not contain an inverter. An inverter is required for mapping.

DESCRIPTION

The target_library does not contain an inverter.

WHAT NEXT

Add an inverter to the target_library.

OPT-102 (error) The target library does not contain all required gates.
Either a NOR, or an AND and an OR gate (two-input) is required for mapping.

DESCRIPTION

The target_library does not contain the minimum set of gates required by the mapping algorithms.

WHAT NEXT

Add the required gates to the target_library.

OPT-103 (information) Verification Failed.

DESCRIPTION

This error indicates that the **compare_design** command (or the '-verify' option of **compile**) has determined that the combinational logic portions of the two designs being compared are not functionally equivalent.

Another cause for verification failure is if the primary inputs and outputs of the combinational logic partitions do not have the same names. For example, if the names of flip-flops, black boxes, or ports of the designs are not identical, then verification will fail because combinational logic partitions will appear as being fed by different signals.

WHAT NEXT

If you are using -verify and this error occurs, contact the Synopsys Hotline.

OPT-104 (information) Verification is too expensive...unable to complete.

DESCRIPTION

The default value for Verify_effort is "low" which means if the design cannot be verified in a relatively short amount of time, the process is terminated.

WHAT NEXT

When "effort" is set to "high", verification will continue indefinitely, so be cautioned that some designs may take an extremely long time to verify. Set "effort" to "medium" or "high" using the -effort option of **compare_design** or the -verifiy_effort option of **compile**.

OPT-105 (information) Flattening is too expensive...unable to complete.

Total Endpoints: %d Endpoints unable to be flattened: %d

DESCRIPTION

The flattening of one or more endpoints was determined to be too expensive relative to the specified 'flatten_effort'. An endpoint is considered too expensive to flatten if the flattened (sum of products) representation grows too large during the flattening process.

WHAT NEXT

The default value for 'flatten_effort' is "low". Use the **set_flatten** command to change the effort to "medium" or "high". Be aware that if an endpoint is considered difficult to flatten (i.e. the flattened representation is large) then this may be an indication that flattening is not a viable optimization strategy for this design. Also be aware that with flatten_effort set to "high" the flattening will continue indefinitely. Certain logic functions (large parity trees, for example) have an extremely large flattened representation, and it is possible that flattening with "high" effort will never terminate because of memory limitations of the machine you are running on.

OPT-106 (warning) Cell %s conflicts with the %s in the target library.

DESCRIPTION

The named cell in the design being compiled is linked to a design or library cell with the same name as a cell in your target_library. Due to this the initial technology translation step of **compile** was unable to resolve the conflict. Translation will not be able to resolve the conflict if the dont_touch attribute is assigned, if the cell is a black box (unresolved reference), or if the cell is hierarchical.

WHAT NEXT

If the conflicting cell is already in the target_library, add the target_library to the front of your link_library then do an explicit **link** before the compile.

If you do not want the conflicting cell to be mapped to the target_library, apply the **dont_use** attribute to the conflicting cell in the target_library.

If the conflicting cell is hierarchical, rename the referenced design using **rename_design** and **change_link**.

OPT-107 (warning) Cell %s conflicts with another %s in the

same design.

DESCRIPTION

The design being compiled has two or more cells linked to different library cells (or designs) which have the same name. This can happen if you have two different versions of the same library loaded in Design Compiler, or different libraries with the same cell names, and some cells in the design have been linked to one library and some to another. One possible way that cells will end up linked inconsistently is if you have changed current_design to a lower level module and did a **link** (or any command that causes an auto-link), and then changed current_design back to the top level module and changed your search_path or link_path.

WHAT NEXT

The design needs to be explicitly re-linked using the **link** command.

OPT-108 (information) Design '%s' has no optimization constraints set.

DESCRIPTION

The specified design will not be optimized for speed, area, or power consumption because no optimization constraint has been set. For additional information on how to set up optimization constraints, see Chapter 6 of the *Design Compiler Family Reference Manual*.

WHAT NEXT

Set optimization constraints, unless it is not important for your design to be optimized for area, delay, or power.

OPT-109 (warning) In design %s, there are sequential cells not driving any load.

DESCRIPTION

The design being compiled has sequential cells that are not driving any load. Therefore, there exists at least one sequential cell that has an explicit no-load or an inferred no-load due to optimized logic. The default in **compile** is to delete such cells. To make **compile** retain such cells, set variable "compile_delete_unloaded_sequential_cells" to "false" (default "true"). The command "check_design" lists all the unloaded sequential cells.

NOTE: In cases where there exists a feedback loop, with no path from any section of the loop to a primary output, a warning will not be issued as theoretically the output of the sequential cell is connected.

WHAT NEXT

Use *check_design* to obtain more information about the design.

OPT-110 (warning) %s libraries have conflicting technology types.
%s '%s' has technology '%s',
and %s '%s' has technology '%s'.

DESCRIPTION

The libraries in the **link_library** and **target_library** variables must have the same technology specified. It is invalid to have both ECL and CMOS libraries in the link_library or the target_library.

WHAT NEXT

Reset the link_library or target_library variable to a valid set of libraries. The libraries the link_library and target_library must all have the same technology attribute.

EXAMPLE MESSAGE

Warning: Target libraries have conflicting technology types. (OPT-110) Library 'xyz' has technology 'ecl', and library 'qrs' has technology 'cmos'.

OPT-111 (error) The compile_new_optimization variable is obsolete.

DESCRIPTION

This error message occurs because the **compile_new_optimization** variable enabled a set of optimizations in **compile_ultra** that caused excessive runtimes that are no longer used.

WHAT NEXT

Remove **compile_new_optimization** from your script in order to use the default **compile_ultra** flow, which is tuned up to produce the best quality of results.

SEE ALSO

compile_ultra(2)

OPT-113 (warning) %s libraries have conflicting delay models. Library '%s' has delay model '%s', and library '%s' has delay model '%s'.

DESCRIPTION

This error occurs when the libraries of link_library or target_library contain multiple delay models. A target_library or link_library that has more than one specified library must contain the same delay model.

WHAT NEXT

Set the link_library or target_library variable to a valid set of libraries. If you have the library source files, you can examine them to determine the delay model for each one. You might have omitted a "delay_model" attribute for one library, which results in the use of a default setting. If you do not have library source files, you might need to ask your library vendor whether the libraries you are using are compatible.

EXAMPLE MESSAGE

Warning: Target libraries have conflicting delay models. (OPT-113) Library 'xyz' has delay model 'generic_ecl', and library 'qrs' has delay model 'generic_cmos'.

OPT-114 (error) Delay model '%s' in library '%s' is not supported.

DESCRIPTION

This error occurs when the delay model of a library is not a supported model.Valid delay models are "generic_cmos" and "generic_ecl". A number of custom delay models are supported. Design Compiler is unable to time the design if the delay model is not valid.

WHAT NEXT

If you have library source files, edit the library source to set the delay_model to a valid value. Then use Library Compiler to save the library as a .db file.

If you do not have library source files, contact your library vendor to obtain a valid library file.

OPT-115 (warning) The target library '%s' was compiled with a version 1.1 Library Compiler; this version has a known bug when compiling multiple-output combinational gates. To avoid this problem, either obtain a version of this library which was compiled with version 1.2 or greater, or use the 'dont_use' command to disable all of its multiple-output combinational gates.

DESCRIPTION

The target library specified was compiled with version 1.1 of Library Compiler; this version has a known bug when compiling multiple-output combinational gates.

WHAT NEXT

To avoid this problem, either obtain a version of this library which was compiled with version 1.2 or greater of Library Compiler from your ASIC vendor, or re-compile your library source file (.lib) with a version of Library Compiler greater than version 1.1, using the **read_lib**, **write_lib** command sequence (if you have access to the library source, and Library Compiler). Another solution is to keep the current library and use the **dont_use** command to disable in the target library the insertion of all multiple-output combinational cells during **compileFP. Note that this may result in creating a less optimum design than if those cells were available during compile**.

OPT-116 (warning) The target library '%s' was also compiled

using version 1.1.

DESCRIPTION

The target library specified was compiled with version 1.1 of Library Compiler; this version has a known bug when compiling multiple-output combinational gates.

WHAT NEXT

To avoid this problem, either obtain a version of this library which was compiled with version 1.2 or greater of Library Compiler from your ASIC vendor, or re-compile your library source file (.lib) with a version of Library Compiler greater than version 1.1, using the **read_lib**, **write_lib** command sequence (if you have access to the library source, and Library Compiler). Another solution is to keep the current library and use the **dont_use** command to disable in the target library the insertion of all multiple-output combinational cells during **compileFP. Note that this may result in creating a less optimum design than if those cells were available during compile**.

OPT-119 (information) Compatibility version is less than '%s'.

DESCRIPTION

This message indicates that the value of the **compatibility_version** variable is set to a release version that is less than the version that is being used.

This message will be followed by another message which will indicate some corresponding behavior of Design Compiler that is modified because of the compatibility version setting.

WHAT NEXT

Reset **compatibility_version**.

OPT-120 (information) Compile will ungroup all hierarchy that is not 'dont_touch'.

DESCRIPTION

This message indicates that the **compatibility_version** variable has been set to a release less than 'v2.0', so the default behavior of **compile** will be to ungroup all hierarchy that does not include the dont_touch attribute. For releases v2.0 and higher the normal default behavior of **compile** is to not ungroup hierarchy.

WHAT NEXT

Reset the **compatibility_version**.

OPT-121 (information) Replacing three-state busses with multiplexed busses.

DESCRIPTION

The **compile** or **translate** command is unable to find any three_state components in the target_library, so it replaces three_state busses with multiplexed busses.This process is completed by first mapping the three_state components into generic three_state cells, and then replacing each generic three_state by logic which AND's the Enable and Input pins and then replacing the bus with logic that OR's all of the signals together.This replacement algorithm assumes the original bus was fully decoded. This procedure is only performed if the variable **compile_assume_fully_decoded_three_state_busses** is set to "true".

WHAT NEXT

Recompile with a target library that contains three_state components if you want to keep three_state busses.

OPT-122 (information) Unable to remove three-state bus '%s' from design '%s'.

DESCRIPTION

The **compile** or **translate** attempted to replace the three-state bus with multiplexed bus, but was unable to do so. This can happen if the three-state cells on the bus could not be mapped into generic three_state cells because they included the dont_touch attribute. This can also happen if the hierarchy of the design is such that the transformation cannot legally be done. One case where this happens is when the bus leaves a lower level block but is also used inside that block. In this case you cannot replace the bus by a multiplexed bus, since that would require adding another port to the block to feed the bussed signal back into the block for the internal usage.

WHAT NEXT

Remove the **dont_touch** attribute or ungroup the hierarchy to allow replacement of the three_state bus.

OPT-123 (error) Unable to verify the two designs because at least
one of the designs contains a state table.

DESCRIPTION

The **compare_design** command cannot verify state tables.

WHAT NEXT

Use **compile** to convert both designs into netlists, then use **compare_design** to verify them. Be aware that compare_design only verifies that the combinational logic of the two designs are functionally equivalent. If the state encoding or number of registers in the designs is different, then combinational verification is meaningless and will most likely report that the designs are not the same even though they might have the same sequential behavior.

You can also use the **comare_fsm** command to compare two state machines.

OPT-124 (error) Use the 'uniquify' command to fix multiply instantiated designs.

DESCRIPTION

The **compile** and **reoptimize_design** commands will not accept designs that have multiply-instantiated subdesigns because the commands need to be able to optimize each design specifically for the environment in which it is instantiated.

WHAT NEXT

To keep multiple instances of the same design, you must assign the **dont_touch** attribute to all instances. Otherwise, the multiply instantiated design will not be optimized. You must pick one instance to **characterize** from, and then optimize the multiply-instantiated design separately.

If you do not want to retain the multiple instances, use the **uniquify** command to eliminate multiple instances. This command creates a unique copy of the design for each instance and names the new designs according to the **uniquify_naming_style** variable. You can also manually uniquify by using the **copy_design** and **change_link** commands.

Another option is to apply **set_ungroup** to the multiply-instantiated design, which will cause all the instances to be ungrouped during optimization.

OPT-125 (information) Unable to map three-state cells.

DESCRIPTION

The **compile** or **translate** command was unable to map three_state cells because the target_library does not contain any three_state components.

WHAT NEXT

Rerun **compile** using a library that contains three_state components.

OPT-126 (information) Leaving generic three-state cells in design.

DESCRIPTION

The **compile** or **translate** command was unable to map into three_state components from the target_library so the three_state elements in the design are left as generic components.

WHAT NEXT

Rerun **compile** using three_state components.

OPT-127 (error) Designs which contain synthetic library parts cannot be %s when ’synthetic_library’ is not specified or synthetic libraries are disabled.

DESCRIPTION

The design contains synthetic library parts, but synthetic libraries have been disabled.

WHAT NEXT

Enable synthetic libraries by setting the **synthetic_library** variable to "standard.sldb".

OPT-128 (error) There are conflicts between cells in libraries %s:%s (%s) and %s:%s (%s).

DESCRIPTION

This error message follows error messages OPT-106 or OPT-107 and gives the full path name of the libraries involved in cell conflicts. This information is useful when the cell conflicts are actually caused by having two versions of the same library (with different full path names) loaded into Design Compiler at one time.

WHAT NEXT

If you have two versions of the same library loaded you can remove the one you do not need with the **remove_design** command. Check your search_path to make sure the library you want to use can be found on the search_path.

OPT-129 (warning) The three_state bus '%s' drives more than one port and cannot be split apart because at least one of the ports is an inout mode port.

DESCRIPTION

This error message identifies a net that drives more than one port. The net cannot be split apart because it is a three-state bus with an inout mode port. The **set_fix_multiple_port_nets** command directs compile to insert enough extra logic in a design to ensure that there are no feedthroughs and/or that no two output ports are connected to the same net. In the case of three-state bus nets, however, it is impossible to alter the network without knowing the enabling conditions on the three states that drive the inout mode port from the outside.

WHAT NEXT

The designer needs to manually rearrange the logic hierarchy so that no multiple-port nets exist. The tool cannot automatically help in this case.

OPT-130 (warning) The cell '%s' has no drive (drive == 0.0)

and therefore no net driven by that cell will be buffered.

DESCRIPTION

This error message identifies a cell (or port) that has a drive of 0. That means the cell will not introduce any delay when driving loads of any size. If the net driven by that cell or port really needs buffering, then some drive should be set on it before command balance_buffer is invoked.

WHAT NEXT

Use command set_drive on the cell or port that drives the net being buffered, and then reinvoke command balnace_buffer.

OPT-140 (warning) Could not buffer the multiple port net %s because
doing so would increase the connection class violation of the design.

DESCRIPTION

Design Compiler could not buffer the multiple port net without increasing the connection class cost. Connection class cost is the highest priority cost used by Design Compiler. No transform is allowed to create a connection class violation or worsen an existing connection class violation.

WHAT NEXT

Find out and resolve why you are having connection class violations. You can use the 'check_design' command to know more about the connection class violations.

OPT-141 (warning) Port '%s' cannot be isolated with '%s' because the corresponding cell is not a buffer or an inverter.

DESCRIPTION

You received this warning message because you executed the **set_isolate_ports** command and specified a port with a cell that is not a buffer or an inverter. Design Compiler cannot isolate ports with cells that are not buffers or inverters.

WHAT NEXT

Reexecute the **set_isolate_ports** command and specify a cell that is a buffer or an inverter.

SEE ALSO

set_isolate_ports (2).

OPT-142 (warning) Port '%s' cannot be isolated with '%s' because the corresponding cell is not found in the library.

DESCRIPTION

You receive this warning message because you executed the **set_isolate_ports** command and specified a cell that is not in the target library. Therefore, Design Compiler could not isolate the port with the specified cell.

WHAT NEXT

Verify that the cell specified for isolating the port is in the target library.

SEE ALSO

set_isolate_ports (2).

OPT-143 (warning) Port '%s' cannot be isolated because the connected net '%s' is dont_touch.

DESCRIPTION

You receive this warning message because Design Compiler could not isolate the specified port because the net connected to the port has the **dont_touch** attribute set on it.

WHAT NEXT

Remove the **dont_touch** attribute from the net, then reexecute the **set_isolate_ports** command.

SEE ALSO

remove_attribute (2), **set_isolate_ports** (2).

OPT-144 (warning) Port '%s' cannot be isolated because it is driven by the tristate cell '%s'.

DESCRIPTION

You receive this warning message because Design Compiler could not isolate the specified port because the cell driving the port is a tristate cell. Port isolation cannot be performed on inout ports or ports driven by tristate cells.

WHAT NEXT

Remove the port from the list of ports given to **set_isolate_ports**, then reexecute the command.

SEE ALSO

set_isolate_ports (2).

OPT-145 (warning) The port named %s cannot be isolated because it is a clock port.

DESCRIPTION

This warning message occurs if Design Compiler cannot isolate the specified port because it is a clock source.

WHAT NEXT

This is a warning message only. No action is required.

However, you can eliminate the message by removing the port from the list of ports given to the **set_isolate_ports** command. After making your changes, reexecute the command.

SEE ALSO

set_isolate_ports(2)

OPT-150 (information) Timing loop detected.

DESCRIPTION

The design contains at least one timing loop. This message is followed by a list of pins on one loop and then messages indicating which timing arcs are being automatically disabled to break the loop.

WHAT NEXT

Use **report_timing -loops** to view all timing loops in your design. Use **disable_timing** to manualy break the loops.

OPT-151 (information) %s interrupted. Saving intermediate design.

DESCRIPTION

A Control-C interrupt was received by the **compile** command or the **reoptimize_design** command. The current state of the design is being written back to the database. The design will reflect all of the optimization steps that have been performed. During a compile command, if the optimization has not progressed to the mapping step, the design will be unmapped (generic logic).

WHAT NEXT

You can start again from the original design by rereading it or by saving the current design.

OPT-153 (warning) Unable to maintain nets '%s' and '%s' as separate entities.

DESCRIPTION

Two named nets have **probe_point** assigned to them but during optimization they were merged into one net. The resulting net will retain the name of the second net indicated in the error message.

WHAT NEXT

If you need the two nets to remain separate entities throughout optimization, assign the **dont_touch** attribute to them.

OPT-155 (error) ECL technology libraries are not supported.

DESCRIPTION

Starting in release v3.4b, ECL technology libraries and (the ECL delay model) are no longer supported.

WHAT NEXT

Target a different (non-ECL) technology library when synthesizing a new design.

If your design was already compiled against an ECL library, revert back to an older version of the Design Compiler product (v3.4a and before) which supports ECL technology libraries and the ECL delay model. Use the older version of the Design Compiler product to translate the design to a new (non-ECL) library; then read that design into the latest version of the Design Compiler product.

OPT-156 (warning) max_power attribute is ignored on non-ECL designs.

DESCRIPTION

This message appears prior to optimization if the **max_power** attribute has been set on a non-ECL design. Design Compiler will ignore the attribute.

WHAT NEXT

If you are using a **dc_shell** script, edit it to remove the **max_power** command. You can remove the **max_power** attribute on a design with the command:
dc_shell> **remove_attribute find(design,design_name) max_power**.

OPT-157 (error) Cannot perform optimization with generic cell '%s' (reference %s) which is not dont_touched. Use the report_cell command to list all unmapped cells in the design.

DESCRIPTION

You receive this message because Compiler is unable to optimize the design due to generic logic that is not assigned the **dont_touch** attribute. To perform optimization, the design must either be free of any generic logic or all generic logic must be assigned the **dont_touch** attribute. Use the **report_cell** command to view all cells that are generic and do not have the **dont_touch** attribute assigned to

them.

WHAT NEXT

If you are doing technology translation, before you optimize the design, first do a normal compile or translate to fully map the design into the new technology.

SEE ALSO

report_cell (2).

OPT-160 (error) Unable to model design '%s'.

DESCRIPTION

The modeling of the specified design failed. This can be because the library could not be found or could not be modified. The modeling library can be manually created or read with **read_lib command.**

WHAT NEXT

Check if the modeling library is in memory with **list -libraries**. If the modeling library is not in memory, create it and then read it in with **read_lib**, or read the existing library in explicitly, with the **read** command. Also, check if the given library is found within the search path with **list search_path**. Verify you have write privileges to modify the modeling library. Re-initiate the **model** command.

OPT-161 (warning) Text file for model '%s' contains illegal or incomplete library compiler code.

DESCRIPTION

The **model** command did not succeed. The text file describing the model specified in this message could not be written properly. The text file generated cannot be used as a modeling library. This could be because the user ran out of disk space, or because the user has no write privileges for the modeling library.

WHAT NEXT

If the modeling library could not be written successfully, do not use the modeling library created. Check if there is enough disk space left on your device. Check for write permission on the library file and its directory. Once the problem is fixed, create another model for the specified design.

OPT-162 (error) Model can only currently handle busses which are arrays of bits.

DESCRIPTION

The **model** command did not complete successfully because the current design contains busses of a type different than an arrays of bits.

WHAT NEXT

Do not use the model created in the modeling library. Modify the HDL code that is being used as a source to the **model** command to use arrays of bits to represent busses, and use **model** to create a new model for the current design.

OPT-163 (error) Library '%s' must use the same technology as design '%s' to add a model.

DESCRIPTION

The model created must be added in a library with the same technology as the design to be modelled. The library used has a different technology as the design to model.

WHAT NEXT

Use another library to model the design. To check the technology library of a library, use **report_lib**, and look under "Library Type". One way to check the technology on the design is to use **write_timing -f sdf** and look at the PROGRAM field in the sdf file.

OPT-170 (information) Changed wire load model for '%s' from '%s' to '%s'.

DESCRIPTION

Your technology library contains a description of which wire load model to use based on the area of the design. During optimization, **compile** modifies the area of the design and automatically choose the new wire load model necessary to estimate net delays.

WHAT NEXT

Once **compile** completed, verify the constraints are still met, because changing a wire load model means changing net delay estimations. You verify the constraints with **report_constraints**.

OPT-171 (information) Changed minimum wire load model for '%s' from '%s' to '%s'.

DESCRIPTION

Your technology library contains a description of which wire load model to use for minimum delay analysis based on the area of the design. During optimization, **compile** modifies the area of the design and automatically chooses the new wire load model necessary to estimate net delays.

WHAT NEXT

Once **compile** completed verify the constraints are still met, because changing a wire load model means changing net delay estimations. Verify the constraints with **report_constraints**.

OPT-180 (Warning) File '%s' already exists; appending to the end of it.

DESCRIPTION

A command tried to open a file for writing/appending, but the file already existed. This warning message is to inform you that the new text will be appended to the end of the existing file. The old text will remain in the file.

WHAT NEXT

To avoid getting this message, make sure to delete the file before executing this command.

OPT-181 (Error) Could not open file '%s' for writing.

DESCRIPTION

A command tried to open a file for writing, but failed.

WHAT NEXT

Make sure that you have write permission in this directory. If the file already exists in the directory, make sure that you have write permission for that file.

If the permissions are OK, try NOT using the '~' (tilde) character. Some file manipulation functions do not accept path names that start with the tilde character. Try using absolute paths or relative paths instead.

OPT-187 (warning) There are conflicts between cells in libraries %s:%s (%s) and %s:%s (%s).

DESCRIPTION

This warning message follows the OPT-106 or OPT-107 warning message and provides the full path name of the libraries involved in cell conflicts. This information is useful when the cell conflicts are caused by having two versions of the same library (with different full path names) loaded into Design Compiler at one time.

WHAT NEXT

This is a warning message only. No action is required.

However, if you have two versions of the same library loaded, remove the unneeded library with the **remove_design** command. Check the search_path to ensure that the library you want to use can be found on the search_path.

SEE ALSO

remove_design(2)
OPT-106(n)
OPT-107(n)

OPT-190 (Error) Must have an expert license to use 'compile -in_place'.

DESCRIPTION

The -in_place option of compile requires an expert license.

WHAT NEXT

See command get_license to obtain the expert license.

OPT-191 (Error) Must have an expert license to use ’balance_registers’.

DESCRIPTION

The balance_registers command requires an expert license.

WHAT NEXT

OPT-192 (Error) Must have a Design Compiler Expert license to use complex clocking.

DESCRIPTION

A Design Compiler Expert license is required to use complex clocking. Complex clocking means multiple clocks with different periods or any clocks with multiple pulses in the waveform.

WHAT NEXT

Redefine clocks using common period and single pulse per waveform, or obtain a Design Compiler Expert license.

OPT-193 (Warning) Must have a Design Compiler Expert license
to use ’balance_registers’.

DESCRIPTION

The **balance_registers** feature requires a Design Compiler Expert license. Register balancing will not be performed during compile if no Design Compiler Expert license is available.

WHAT NEXT

Check whether your site has a Design Compiler Expert key. If this is not the case, purchase one from Synopsys. Otherwise all your Design Compiler Expert Keys are currently in use. Wait until one becomes free at your site.

OPT-194 (Information) Expert license required for latch time-borrowing.

DESCRIPTION

Latch time-borrowing requires an expert license. Max_time_borrow will be set to zero for all latches if no expert license is available.

WHAT NEXT

OPT-195 (Error) Must have %s license(s) to use %s.

DESCRIPTION

A command was invoked which requires the specified license(s). However, this license either does not exist at this site or it is already in use by other users.

WHAT NEXT

To proceed with this command you must ensure that this license is available at this site. Then reinvoke the command.

OPT-196 (error) The target technology is '%s'. The design '%s' can only be optimized or mapped to an FPGA technology because either '%s' or at least one of its sub-designs was read or elaborated using the FPGA specific HDL-Compiler. The following design(s) in '%s' were read or elaborated by the FPGA specific HDL-Compiler: %s .

DESCRIPTION

An optimization command (**compile**) was issued. As the design was loaded, one or more designs were found to have been read or elaborated using an FPGA-specific HDL Compiler license. But the technology of the target library was not FPGA. To optimize these designs, the target technology must be FPGA.

WHAT NEXT

Reread or re-elaborate the designs, making sure that a nontechnology-specific HDL license is checked out by the **read** or **elaborate** command.

To do the above, remove all FPGA-specific HDL licenses, and get a nontechnology-specific HDL license, such as HDL Compiler or VHDL Compiler (see manual pages for **remove_license** and **get_license**).

OPT-197 (Error) You must have a BOA-BRT license to run the pipeline_design or optimize_registers commands.

DESCRIPTION

You receive this error message if you do not have a BOA-BRT license. The **pipeline_design** and **optimize_registers** commands run only with a BOA-BRT license. This license is either not available at your site, or all licenses for this feature are currently in use.

WHAT NEXT

Wait for one of the existing licenses to become available, or purchase an additional BOA-BRT license from Synopsys.

OPT-200 (Warning) Library cell '%s' has a valid function-id, but it has also been annotated with the user_function_class attribute. Resolving this conflict by ignoring the user_function_class attribute for this library cell.

DESCRIPTION

The specified cell has been annotated with the **user_function_classr** attribute even though it has a valid function-id. Library Compiler can generate a function-id for most cells in a technology library. However, there may be a few complex sequential or combinational cells that Library Compiler cannot successfully generate a function-id for. In addition, some black-box cells in the library do not have any function information. The **user_function_class** attribute is intended for such cells that otherwise would not have a function-id. The **user_function_class** attribute is not intended for library cells that already have a valid function-id.

WHAT NEXT

This warning message indicates that the **user_function_class** attribute for this

library cell will be ignored. No further action is required. To turn off this warning message in the future, make sure that a **user_function_class attribute** is not set on this library cell.

OPT-201 (Warning) Library cells '%s' and '%s' have different pin information, but they have been assigned the same user_function_class. Resolving this conflict by ignoring the user_function_class attribute on the latter library cell.

DESCRIPTION

Two library cells that are assigned the same **user_function_class** attribute should have the exact same pin information. That is, they must have the same number of pins and the same pin names. This requirement is necessary so that Design Compiler can establish pin-to-pin correspondence between two cells in the same **user_function_class** when it replaces a reference to one library cell by a reference to the other library cell.

This warning message indicates that an inconsistency was found between the pin information of two library cells in the same **user_function_class**. To resolve this conflict, the **user_function_class** attribute for the second library cell will be ignored.

WHAT NEXT

This warning message indicates that the **user_function_class** attribute for the second library cell will be ignored. No further action is required. To turn off this warning message in the future, make sure that all library cells in a given **user_function_class** attribute have the same pin information.

OPT-202 (warning) Variable '%s' is obsolete.

DESCRIPTION

Setting this variable has no effect on compile. Please see the the man page for the variable for alternatives.

WHAT NEXT

Please see the man page for the variable for alternatives.

OPT-203 (Warning) Library cells '%s' and '%s' have different function_id, but they have been assigned the same clock_gating_integrated_cell attribute. Resolving this conflict by removing the latter library cell from the clock_gating class.

DESCRIPTION

You receive this warning message when two library cells that have the same **clock_gating_integrated_cell** attribute have a different function_id. Library cells with the same **clock_gating_integrated_cell** attribute must have the same function_id.

WHAT NEXT

Verify that all library cells with the same **clock_gating_integrated_cell** attribute have the same function_id.

OPT-205 (error) Inconsistent references found for cell '%s'.

DESCRIPTION

This is an internal Design Compiler error which indicates that two references by the same name have different port interfaces.

WHAT NEXT

Ensure that no library cells addresses conflict. An example is a design named AND2 with ports I1, I2, 01 and a library cell of the same name with ports A, B, and Z. In this case changing the name of the design will solve the problem.

OPT-206 (warning) The sequential library cell '%s' does not have any setup or hold timing arcs.

DESCRIPTION

The sequential cell '%s' is inherently hazardous. Using such cells in synchronous designs may result in metastable behaviour.

WHAT NEXT

The user can infer this cell directly from HDL by using the asynch_set_reset pragma in the HDL description. See the Application Note "HDL Coding Style: Sequential Devices" for more detail.

OPT-210 (error) Variable '%s' is malformed near '%s' and will be ignored.

DESCRIPTION

The cost vector used by compile can be modified or overridden by environment variables to change the priority of the costs.

This warning message indicates that the user-defined cost vector could not be parsed successfully, and that the problem occured near the reported word (only the first detected error is reported). Because of the error, the user-defined cost vector is ignored and the optimization will proceed with the standard cost vector.

WHAT NEXT

Check the variable definition for a misspelled word. Make sure that each cost is contained in a separate word, e.g.,

```
         {"delay", "area"},
```

instead of

```
         {"delay area"},
```

Also make sure that each modifier is a single word, e.g.,

```
         { ..., "max_cap before max_fo"},
```

instead of

```
         { ..., "max_cap", "before", "max_fo"}
```

OPT-220 (information) Switching to base optimization engine for the current compile run.

DESCRIPTION

The new optimization engine is known to give good results for rich libraries having several consistently sizes cells. Before invoking the new optimization engine

library analysis is run to determine if the target library meets the above criterion.

The current target library has failed to meet the above criterion. For such a library the quality of results produced by the new optimization engine can be unpredictable. Hence the base optimization engine will be used for all compiles with the current library.

WHAT NEXT

Please contact your silicon vendor for the latest version of their library.

OPT-221 (warning) The new optimization engine might not produce the best results for the specified target library.

DESCRIPTION

The new optimization engine is known to give good results for rich libraries having several consistently sizes cells. Before invoking the new optimization engine library analysis is run to determine if the target library meets the above criterion.

The current target library has just met the above criterion. As the library analysis criterion is not very tight, the above does not imply good quality of results.

WHAT NEXT

Please contact your silicon vendor for the latest version of their library.

OPT-301 (warning) The design named %s has %d out of %d cells marked size-only, which may limit optimization.

DESCRIPTION

This warning message occurs when a large number of cells in the design are marked size-only. A cell is marked size-only by the **set_size_only** command or indirectly by any reference to the cell in a timing constraint, such as the **set_multicycle_path** command, or indirectly by **compile** in the early stage of **compile** to preserve the constraints being applied on the cell during **compile**. The size-only which is indirectly applied by **compile** to preserve the constraints is removed later when the constraint inheritance is done. So, you will not see the size-only attribute through report_cell command after **compile** if the size-only is indirectly applied by **compile**. Marking cells size-only significantly constrains logic optimization for the corresponding logic.

The following is an example of the warning message:

```
Warning: The design named top has 19034 out of 19641 cells
marked size-only, which may limit optimization (OPT-301).
```

WHAT NEXT

This is only a warning message. No action is required.

However, if the large number of size-only cells is unexpected, review your constraints, particularly constraints using wildcards and filters that may accidentally be including more cells than you intended.

SEE ALSO

set_multicycle_path(2)
set_size_only(2)

OPT-306 (warning) Could not find %s '%s' in design '%s'.

DESCRIPTION

This error indicates that a pin or port cannot be found in the design.This can happen if an attribute was placed on an object that no longer exists. A pin name may be invalid because a new design has been linked to it.

WHAT NEXT

If the design hierarchy has changed, you should remove attributes and other information which refers to nonexistent pins or ports.

EXAMPLE MESSAGE

Warning: Could not find pin 'u1/u4/u3/u7/Z' in design 'top'. (OPT-306)

OPT-309 (warning) Design '%s' contains unmapped cells. Use report_cell to list unmapped cells in the design.

DESCRIPTION

This warning is displayed by the **check_timing** command if the design contains unmapped cells (generic logic). Timing paths that pass through generic logic will be inaccurate because zero delay is assumed for generic cells. Use **report_cell** to see

which cells in the design are unmapped.

WHAT NEXT

Use **compile** to map the generic logic in the design. Make sure that no generic cells have the **dont_touch** attribute set, because **dont_touch** attributes cause **compile** to display warning message before mapping the cell.

OPT-314 (warning) Disabling timing arc between pins '%s' and '%s' on cell '%s'%s

DESCRIPTION

This message is displayed when timing arcs are disabled by Design Compiler to break combinational feedback loops. It is not displayed for arcs that are manually disabled with the **disable_timing** command.

WHAT NEXT

If you want to manually break a timing loop, examine the design to see why there is combinational feedback and then choose a different point at which to break the loop. To do this, use the **disable_timing** command instead of letting Design Compiler automatically break the loop.

EXAMPLE MESSAGE

Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'u10'to break a timing loop (OPT-314)

OPT-317 (warning) Could not fix %s violation of %.2f at %s '%s'.

DESCRIPTION

This warning may appear in the "Fixing Design Rules" phase of compile. This message indicates that there was a min_delay or hold violation which could not be corrected by adding delay in the form of inverters or buffers. It also indicates the pin or port at which the violation occurred.

WHAT NEXT

The violation could not be fixed either because adding a buffer violates higher priority costs. You can prioritize min-path over Design Rule/Max Path by using set_cost_priority command. You can examine the resulting netlist to see why there was a min_delay or hold violation. It may be possible to modify the original design

to avoid the violation. If the error was a hold violation, you can disable "fixing" by removing the **fix_hold** attribute from clocks in the design. If the error was a min_delay violation, you can disable "fixing" by removing any **min_delay** attributes in the design. Another possibility is to stop compile before the "Fixing Design Rules" phase using **compile-no_design_rule**. Use the **report_constraint** command to examine the design rule violations which **compile** would have attempted to fix. If you have a preferred method for correcting certain design rule violations, you can make the change in the design and then mark the changes with the **dont_touch** command before proceeding. Complete the procedure using **compile-only_design_rule** to correct any remaining design rule violations.

EXAMPLE MESSAGE

Warning: Could not fix hold violation of 2.40 at pin 'ff1/D'. (OPT-317).

OPT-318 (warning) Inserting delay to fix %s violation of %.2f at %s '%s'.

DESCRIPTION

This warning may appear in the "Fixing Design Rules" phase of compile. This message indicates that there was a min_delay or hold violation which was corrected by adding delay in the form of inverters or buffers. It also indicates the pin or port at which the violation occurred.

WHAT NEXT

You can examine the resulting netlist to see why there was a min_delay or hold violation. It may be possible to modify the original design to avoid the violation. If the error was a hold violation, you can disable "fixing" by removing the **fix_hold** attribute from clocks in the design. If the error was a min_delay violation, you can disable "fixing" by removing any **min_delay** attributes in the design. Another possibility is to stop compile before the "Fixing Design Rules" phase using **compile-no_design_rule**. Use the **report_constraint** command to examine the design rule violations which **compile** would have attempted to fix. If you have a preferred method for correcting certain design rule violations, you can make the change in the design and then mark the changes with the **dont_touch** command before proceeding. Complete the procedure using **compile-only_design_rule** to correct any remaining design rule violations.

EXAMPLE MESSAGE

Warning: Inserting delay to fix hold violation of 2.40 at pin 'ff1/D'. (OPT-318).

OPT-319 (information) Complementing port '%s' in design '%s'.

The new name of the port is '%s'.

DESCRIPTION

During **compile**, a hierarchical port in the design has undergone a phase change. This can occur only if that port was part of a hierarchical block that was enabled for boundary_optimization, or if the **compile** command was run with the boundary_optimization switch enabled.

WHAT NEXT

To completely disable boundary_optimization, remove the boundary_optimization attribute from all of the hierarchical blocks in the design.You can also selectively enable it on certain blocks.

To turn off only hierarchical phase optimization, set the environment variable compile_disable_hierarchical_inverter_opt to TRUE. This will prevent the **compile** command from changing the phase of hierarchical port signals. Other boundary_optimizations will still be attempted.

OPT-320 (warning) Illegal value for variable port_complement_naming_style. Inverter optimization disabled for design '%s'.

DESCRIPTION

The **dc_shell** variable **port_complement_naming_style** has an illegal value. For more information, consult the man page for this variable.

WHAT NEXT

OPT-403 (warning) Could not find cell '%s' in design '%s'.

DESCRIPTION

This message indicates that a cell that exists in the .db database for the design could not be found in the optimization data structure representation for the same design.

WHAT NEXT

If this condition occurs, it means that the optimization datastructure is somehow

inconsistent with the .db database. Any attributes or directives that exist on this cell in the database will be ignored.

OPT-407 (warning) There are no unconnected '%s' pins with signal type '%s' in block '%s.'

DESCRIPTION

The **compile** or **translate** command attempted to connect the 'clocked_on_also' net in the designated block, but was unable to do so because there were no unconnected pins (load or driver) to connect the net to.

WHAT NEXT

Make sure that signal type attributes have been properly specified in the design.

OPT-408 (warning) No associated_clock found for clocked_on_also %s '%s' in block '%s'.

DESCRIPTION

The **compile** or **translate** command attempted to connect the **clocked_on_also** pin or port in the designated block, but was unable to do so because the **associated_clock** was not found.

Whenever a design has more than one clock port, all **clocked_on_also** ports must specify an **associated_clock**.

WHAT NEXT

Make sure that the **associated_clock** is correctly specified for the given **clocked_on_also** pin or port. The associated clock object must be only one port.

OPT-450 (warning) Could not find net '%s' in design '%s'.

DESCRIPTION

This message indicates that a net that exists in the .db database for the design could not be found in the optimization data structure representation for the same design.

WHAT NEXT

When this condition occurs, it means that the optimization data structure is somehow inconsistent with the .db database. Any attributes or directives that exist on this net in the database will be ignored.

OPT-455 (error) This design has no %ss for distribute_capacitance.

DESCRIPTION

The **distribute_capacitance** command requires that the current design has a wireload, a maximum delay constraint, and at least one appropriate net for distributing capacitance. An appropriate net is one that has no back-annotation, is not dont_touch'ed, and is constrained by the maximum delay constraint.

WHAT NEXT

Correct the design deficiency. Reissue the **distribute_capacitance** command.

OPT-460 (warning) Ignoring dont_touch on net '%s' because it is connected only to generic logic which must be mapped. Use all_connected to see net connections.

DESCRIPTION

A **dont_touch** attribute has been placed on a net that is connected only to unmapped (generic) logic. This **dont_touch** attribute is ignored by **compile** because it must map the logic. A **dont_touch** attribute on a net will only have an effect if there is mapped logic on that net. Use the **all_connected** command to list all objects connected to the net in question.

WHAT NEXT

If you are using a script to mark the net as **dont_touch**, you should remove that **dont_touch** command from the script.

OPT-461 (warning) Dont_touch on net '%s' may be overridden by compile because it

is connected to generic logic. Use all_connected to see net connections.

DESCRIPTION

A **dont_touch** attribute has been placed on a net that connects some unmapped (generic) logic. This **dont_touch** attribute may be ignored by **compile** because the structure of the design may change, eliminating the need for that net. The net might disappear if its logical value can be obtained from another point in the design, or if that value is not used.

If the net is not eliminated, the dont_touch attribute will allow the logic on the net to be mapped. An example of when the dont_touch will be useful is when you have a mapped multiple-output buffer driving a number of roughly balanced loads of generic logic. You can preserve balancing by marking the output nets of the buffer as dont_touch.

Use the **all_connected** command to list all objects connected to the net in question.

WHAT NEXT

After compile is finished, examine the design to see what changes were made to the net. If the net is lost and you want to preserve it, you can instantiate mapped logic connected to the net.

OPT-462 (error) The following net has multiple drivers which are logically
opposite in function: '%s'
This is an illegal design. Type 'help OPT-462' for more details.

DESCRIPTION

As the design was being read into **compile**, it was found that a net in the design has more than one driver, and that the functions computed by a pair of drivers on the net are the inverse of each other. For example, if a net is connected to both logic one and logic zero or is connected to the Q and QBAR outputs of flip-flop, the drivers are inverse of each other. This type of connect is not allowed in **compile** and thus compile terminates.

WHAT NEXT

Fix the multiple driver net, such that there are no drivers on it which are opposite in functionality. Or make the net a wired-net of some known type.

OPT-463 (warning) Deleting scan chain information from design '%s'.

DESCRIPTION

This message tells you that **compile** has deleted scan chain information from a design. **report_test -scan_path** will no longer show that the design has scan chains. Hierarchical scan insertion will no longer infer that there are scan segments in the design.

compile needs to delete the scan chain information because the information includes references to design database objects that may get obsoleted by **compile**.

You can use **check_dft** to restore the scan chain information. It is important that you do this before using **insert_dft** to attempt hierarchical scan operations.

This message will appear regardless of whether test models are used. If you are using a Test Model flow (by setting the variable **test_use_test_models** to true), scan chain information is stored in a Test Model and so is not actually lost. The scan chain information stored in the Test Model will be used at the top level hierarchical scan.

WHAT NEXT

If you are not using a test model flow, run **check_dft** on the design to restore scan chain information.

If you are using a test model flow, you can safely disregard this message.

OPT-464 (warning) Library has non-scan cells like '%s'.

DESCRIPTION

This message tells you that you have set **compile_seqmap_is_scan_only** to true and the libray has non-scan cells. This can result in incorrect results with **compile -scan**.

WHAT NEXT

Set compile_seqmap_is_scan_only to false(default) and execute compile -scan With new-scan flow this variable need to be set.

OPT-465 (warning) There are '%d' scan cells in the design

without scanned_by_test_compiler attribute

DESCRIPTION

This message tells you that **compile -scan** found the given no of scan cells that does not have scanned_by_test_compiler attribute on them. If this attribute is not set. **compile -scan** will try to scan-replace it, thinking that it is used functionally. This can result in redundant logic.

WHAT NEXT

Set scanned_by_test_compiler attribute on all scan cells that are not used functionally. The following example sets the attribute on all scan cells in the design

Eg., prompt>set scells [get_cells -hier * -filter @is_a_test_cell==true]
prompt>set_attribute $scells scanned_by_test_compiler true

SEE ALSO

set_attribute

OPT-466 (warning) Optimization for shift-registers can be done only by compile_ultra -scan.

DESCRIPTION

This message is shown when **compile -scan** is invoked and you have set **set_scan_configuration -identify_shift_registers true**. for **compile -scan**. Only **compile_ultra -scan** can do shift-register optimizations for scan. Medium effort compile will do this optimization.

WHAT NEXT

Run **compile_ultra -scan** for optimizing back-to-back shift-registers for scan, if you want to see the best results in your first compilation.

SEE ALSO

compile_ultra preview_dft insert_dft

NAE

OPT-467 (information) Automatic shift-register identification is enabled for scan. Not all registers will be scan-replaced

DESCRIPTION

This message is shown when **compile -scan** is invoked and shift-register identification is enabled. Shift-register identification and optimization for scan will identify back-to-back shift-registers and scan only the first one. So the design after compile_ultra -scan will have non-scan cells with the attribute shift_register-flop.

WHAT NEXT

To disable this feature set **set_scan_configuration -identify_shift_registers false before**. **compile_ultra -scan**.

SEE ALSO

set_scan_configuration compile_ultra preview_dft insert_dft

NAE

OPT-468 (information) Scan related optimization for shift-registers will be undone in this flow.

DESCRIPTION

This message is shown when **compile -scan** is invoked and shift-register identification is disabled for a test-ready design. Shift-register identification and optimization for scan will identify back-to-back shift-registers and scan only the first one. If this message was shown the design after compile_ultra -scan will not have non-scan cells with the attribute shift_register-flop.

WHAT NEXT

To enable this feature set **set_scan_configuration -identify_shift_registers true before**. **compile_ultra -scan**.

SEE ALSO

set_scan_configuration compile_ultra preview_dft insert_dft

OPT-470 (information) Using ’high’ timing effort.

DESCRIPTION

The target library being used indicates that the transition time (slew) at a gate’s input pin may affect the output transition delay of the gate. Which means that local changes to the netlist may affect gate delays in the entire transitive fanout of the changed cells, requiring significant delay calculation and path tracing overhead. During optimization, all gate delays are being calculated exactly at the expense of greater run time.

By default all delays are calculated exactly; timing effort is high.

WHAT NEXT

Early in the design cycle, this additional timing accuracy may not be worth the increased run time incurred by modeling the input transition effect on output pin transition.

To optimize using approximate timing and reduce run time, set **compile_use_low_timing_effort = true**.

OPT-471 (information) Using ’low’ timing effort.

DESCRIPTION

The target library being used indicates that the transition time (slew) at a gate’s input pin may affect the output transition delay of the gate. Which means that local changes to the netlist may affect gate delays in the entire transitive fanout of the changed cells, requiring significant delay calculation and path tracing overhead. Optimization is using approximate output pin transitions to reduce runtime because the variable **compile_use_low_timing_effort** has been set to "true."

Since optimization is using approximate pin transitions, Design Compiler may meet the design’s constraints using the approximate timing, but not meet them using exact timing. The compile log will show delay costs calculated using approximate timing. Timing and constraint reports are always produced using exact timing.

WHAT NEXT

Low timing effort should only be used early in the design cycle, when the additional timing accuracy of high timing effort may not be worth the increased run time incurred by modeling the input transition effect on output pin transition.

To optimize using exact timing, set **compile_use_low_timing_effort = false**.

OPT-472 (information) Using fast delay calculation mode.

DESCRIPTION

The variable **compile_use_fast_delay_mode** is set to *true* and optimization is using either the cmos2 delay model or the nonlinear delay model.

SEE ALSO

compile_use_fast_delay_mode(3).

OPT-473 (warning) Cannot perform multibit optimization on '%s' '%s'.

DESCRIPTION

This message indicates that multibit optimization cannot be performed on a cell or a multibit component. The reasons include having a don't touch attribute, having local optimization disabled, the multibit component not being sufficiently wide, or the multibit component having cells with differing functionalities.

WHAT NEXT

If this condition occurs, it means that the multibit optimization could not be performed on the design object indicated. Check the multibit component or cell indicated and ensure that the above conditions are avoided. Use the **create_multibit** or **remove_multibit** commands to manipulate multibit components. Then re-run the **compile** command.

SEE ALSO

create_multibit(2). remove_multibit(2). report_multibit(2).

OPT-474 (warning) Internal Scan State detection disabled.

DESCRIPTION

Internal scan-state detection is disabled when ungrouping or boundary optimizations are turned on.

WHAT NEXT

Turn off ungrouping and/or boundary optimizations in compile -scan.

SEE ALSO

compile_ultra preview_dft insert_dft

OPT-475 (information) Internal Scan State detection enabled.

DESCRIPTION

Internal scan-state detection is enabled to identify cells already stitched in the design.

WHAT NEXT

To turn off scan-state detection, set variable compile_scan_enable_state_detection to false

SEE ALSO

compile_ultra preview_dft insert_dft

OPT-500 (Error) LUT library design '%s' has more than one output port.

DESCRIPTION

LUT library design can not have more than one output port.

WHAT NEXT

OPT-501 (Error) LUT library design '%s' has pin count mismatch.

DESCRIPTION

LUT library design input pin count should match with lut_bag pin count.

WHAT NEXT

OPT-502 (Error) LUT library design '%s' has ports other than in and out direction types.

DESCRIPTION

LUT library design can not have ports other than in and out direction.

WHAT NEXT

OPT-503 (Warning) Constant sequential cell '%s'.

DESCRIPTION

The inputs to this sequential cell are tied to logic constants in such a way that the register will never change state.

WHAT NEXT

You can set the variable 'fpga_seq_const_prop = 1' and compile will push the constant through and remove the sequential cell. However, changing your hdl may be a cleaner option.

OPT-504 (Warning) Constant-push through sequential cell '%s'.

DESCRIPTION

The inputs to this sequential cell were tied to logic constants in such a way that the register would never change state. The constant has been pushed through and the cell has been removed.

WHAT NEXT

You can set the variable 'fpga_seq_const_prop = 0' and compile will just issue a warning but not push the constant through.

OPT-505 (Error) Clock gating cell '%s' was inserted by Power

Compiler.
This cannot be automatically removed. Please use Power Compiler to remove this clock-gating cell.

DESCRIPTION

DCFPGA cannot remove clock-gating logic that was inserted by the Power Compiler product. This logic must be removed using Power Compiler.

WHAT NEXT

Use Power Compiler to remove clock-gating logic.

OPT-506 (Information) Reimplemented clock-gating for cell '%s'.

DESCRIPTION

DCFPGA has reimplemented the clock-gating logic for this cell according to the 'cg_clk' and 'cg_en' attributes on the cell. This means that all registers that were gated by this cell have been rewired to use the ungated clock signal (the cg_clk function) at clock pins and the gating condition (the cg_en function) at clock-enable pins. Registers were replaced with clock-enabled versions if necessary.

If the clock-gating cell only drives registers then it will be removed after this rewiring. If the clock-gating cell has other non-register loads then the clock-gating cell will be retained to drive these other loads, even though the registers have been rewired.

WHAT NEXT

This is an informational message, no action is required. However, note that the design may fail formal verification (compile -verify) as a result of this clock-gate rewiring because the gate logic is different (even though sequential functionally is the same).

OPT-507 (Error) Bad clock-gating '%s' function (%s).

DESCRIPTION

DCFPGA was unable to reimplement clock-gating logic because the logic function given by this attribute was not parseable into a valid boolean equation. The function must

be a logic equation in terms of the clock-gate cell input pins using standard + and * operators. The tick ’ is used for inversion, and parenthesis may be used in the equation as needed to specify operator precedence.

For example:

```
set_attribute find(cell,"CG1") cg_clk -type string "CP’" set_attribute
find(cell,"CG1") cg_en -type string "E + TE"
```

WHAT NEXT

Fix the function attribute so equation is paresable.

OPT-508 (Error) Could not find cg_relink design ’%s’.

DESCRIPTION

DCFPGA was unable to find a replacement design in the cg_relink attribute. The cg_relink attribute should be of the form:

```
"LIBCELL:REPLACEMENT_DESIGN [LIBCELL2:REPLACEMENT_DESIGN2 etc]"
```

For example:

```
set_attribute CG1 cg_relink -type string "CG:mycgx LD_1:myld1"
```

In this example the design ’myld1’ will be substituted for instances of the LD_1 library cell found in this gated clock domain. The design ’myld1’ can have ports named the same as the pins of LD_1, and these ports will be connected by name match when the substitution is performed. In addition, the replacement design may have additional input ports which match pin names on the original clock-gate cell (CG1 in this example), or on the replacement clock-gate design (mycgx in this example).

It may be possible to fully specify the latch replacement designs in terms of the original cg_cell inputs, in which case it would not be necessary to specify a replacement design for the cg_cell itself (the CG:mycgx in the above example).

WHAT NEXT

Make sure all referenced replacement designs are loaded into dcfpga before the compile command is executed.

OPT-509 (Error) Could not parse cg_relink attribute '%s'.

DESCRIPTION

DCFPGA was unable to parse the cg_relink attribute. The cg_relink attribute should be of the form:

"LIBCELL:REPLACEMENT_DESIGN [LIBCELL2:REPLACEMENT_DESIGN2 etc]"

For example:

set_attribute CG1 cg_relink -type string "LD_1:myld1"

In this example the design 'myld1' will be substituted for instances of the LD_1 library cell found in this gated clock domain.

WHAT NEXT

Fix the cg_relink attribute to conform to above syntax.

OPT-510 (Error) Unmatched cg_relink port '%s' for '%s:%s'.

DESCRIPTION

No match could be found for this replacement-design port. The replacement design ports must match by name to pins of the lib_cell type being replaced, or to input-pins of the cg_cell, or to any port of the cg_cell replacement design if there is one.

WHAT NEXT

Fix the replacement design ports to match by name as described above.

OPT-511 (Warning) Constant propagation through registers has been enabled by fpga_seq_const_prop = true, but these registers will NOT be deleted after constant propagation because the variable

compile_delete_unloaded_sequential_cells = false.

DESCRIPTION

This behavior can be desirable to aid formal verification, as the formal verification tool will be able to match and verify the constant register endpoints.

WHAT NEXT

You can set 'compile_delete_unloaded_sequential_cells = true' and compile will automatically delete unloaded registers. This is also the default behavior if the variable is not explicitly set in your script.

OPT-512 (Information) Reimplemented clock-gating at net '%s'.

DESCRIPTION

DCFPGA has reimplemented the clock-gating logic at this net according to the VIRTUAL_CLKBUF specification in a 'cg_relink' attribute.

WHAT NEXT

This is an informational message, no action is required. However, note that the design may fail formal verification (compile -verify) as a result of this clock-gate rewiring because the gate logic is different (even though sequential functionally is the same).

OPT-513 (Information) Automatic clock-gate removal at net '%s'.

DESCRIPTION

DCFPGA has automatically reimplemented the clock-gating at this net by using clock-enabled sequential devices rather than a clock-gating element.

WHAT NEXT

This is an informational message, no action is required. However, note that the design may fail formal verification (compile -verify) as a result of this clock-gate rewiring because the gate logic is different (even though sequential functionally is the same).

OPT-600 (information) Translate interrupted. Saving intermediate design.

DESCRIPTION

A CONTROL-C interrupt was induced by the **translate** command. The design, in its current state, is being written back to the database. The design will reflect all translation steps that have been completed so far.

WHAT NEXT

You can start again from the original design by re-reading it or you can start again by saving the current design.

OPT-601 (warning) No sequential cell of target library has synchronous set/reset inputs as required by cell '%s'

DESCRIPTION

You receive this message if your HDL description indicates that the specified sequential element needs synchronous set and/or reset inputs, and there is no library cell with such functionality. Instead, a simple flip-flop is instantiated. However, instantiating a simple flip-flop could cause the synchronous set/reset signal(s) to be moved away from the sequential element, possibly causing simulation problems.

WHAT NEXT

Add the directive 'sync_set_reset' (// synopsys sync_set_reset) to the HDL source code, and reexecute the **compile** command.

SEE ALSO

compile (2).

OPT-700 (warning) Dual-site technology attributes are inconsistent across libraries.

These attributes will be ignored.

DESCRIPTION

Attributes specific to dual site technologies, needed for optimization geared towards such technologies, are required to have values consistent across all libraries used in the compile process. If the values are inconsistent, the normal optimization mode will be in use. Note that the absence of any of these attributes in a library forces default values to be used.

WHAT NEXT

Make attributes consistent across all libraries used in the compile process.

OPT-774 (information) '%s' will not be ungrouped because of the verification_priority attribute set on it.

DESCRIPTION

This information message occurs when the specified design or instance has the **verification_priority attribute set on it, even though automatic ungrouping is enabled during compile.**

WHAT NEXT

This is an information-only message. No action is required.

SEE ALSO

compile(2)
set_verification_priority(2)

OPT-775 (information) Ungrouping %d of %d hierarchies before Pass 1

DESCRIPTION

You receive this message because the specified number of hierarchies were automatically ungrouped before Pass 1 due to the enabling of automatic ungrouping during compile.

WHAT NEXT

This is an informational message only.

SEE ALSO

compile (2), **compile_ultra_ungroup_small_hierarchies** (3),

OPT-776 (information) Ungrouping hierarchy %s before Pass 1

DESCRIPTION

You receive this message because the specified hierarchy is automatically ungrouped before Pass 1 due to the enabling of automatic ungrouping during compile.

WHAT NEXT

This is an informational message only.

SEE ALSO

compile (2), **compile_ultra_ungroup_small_hierarchies** (3),

OPT-777 (information) Ungrouping hierarchy %s '%s' #insts = %d.

DESCRIPTION

You receive this message because the specified hierarchy is automatically ungrouped due to the enabling of automatic ungrouping during compile. Automatic ungrouping is enabled by using the **compile** command with the **-auto_ungroup [area|delay]** option. The hierarchy is specified by *Instance Name Cell Type Number of Instances*.

WHAT NEXT

This is an informational message only.

SEE ALSO

compile (2), **compile_auto_ungroup_override_wlm** (3),
compile_auto_ungroup_area_num_cells (3),

OPT-778 (information) Preview of ungrouping hierarchy.

DESCRIPTION

You receive this message to inform you that the hierarchy you specified is a possible candidate for ungrouping. You can selectively ungroup the listed hierarchy (or hierarchies) with subsequent **compile** commands: either use the **compile** command with the **-auto_ungroup** option or set the **compile_auto_ungroup_hierarchy** variable to *1*.

WHAT NEXT

This is an informational message only. No action is required on your part.

If you choose to ungroup the specified hierarchy, use one of the methods described.

SEE ALSO

compile (2), **compile_auto_ungroup_hierarchy** (3).

OPT-779 (information) The wire load model of the parent cell %s is different from that of the child cell %s in the design %s. The child cell will not be ungrouped.

DESCRIPTION

This information message occurs when a cell will not be auto_ungrouped by default if its wire load model is different from its parent.

WHAT NEXT

This is an informational message only. No action is required.

However, you can override the default by setting the **compile_auto_ungroup_override_wlm** to true.

SEE ALSO

compile(2)
compile_auto_ungroup_override_wlm(3)

OPT-780 (information) There is no timing violation in design %s.

Delay-based auto_ungroup will not be performed.

DESCRIPTION

This information message occurs when delay-based auto_ungroup will not take place if there is no timing violation for the current_design.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

compile(2)

OPT-781 (information) Using dc_star strategy for automatic ungrouping.

DESCRIPTION

You receive this information message when you use the **set_dc_star_optimization** command to enable enhanced features for automatic ungrouping during the execution of the **compile_ultra** command. You can revert to the standard **compile_ultra** command ungrouping strategy within dc_star by setting the **compile_dc_star_area_ungroup** variable to false.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

compile_ultra(2)
set_dc_star_optimization(2)
compile_dc_star_area_ungroup(3)

OPT-800 (warning) Removing some annotated net capacitances from design '%s'.

DESCRIPTION

One or more net capacitance values which were annotated with the **set_load** command

have been removed from the design. The capacitance values for these nets will now be estimated using wire load models.

All annotated net capacitance values are removed by the **compile** command (except with the **in_place** option) or the **translate** command.

Annotated net capacitance values are preserved wherever possible when running **compile -in_place**, **reoptimize_design -in_place**, or **reoptimize_design -post_layout_opto**.

The **reoptimize_design** command without the **in_place** or **-post_layout_opto** flags preserves annotated net capacitance on inter-cluster nets. Annotated capacitances are removed from nets enclosed within leaf-level clusters.

WHAT NEXT

The **set_dont_touch** command can be used to maintain annotation on nets during optimization, although it also limits optimization from certain transforms on those nets. The **dont_touch** attribute can be placed on nets directly and may also be placed on hierarchical cells to keep the capacitances annotated on nets within the hierarchical cell during optimization.

The **create_wire_load** command allows optimization to make use of annotated capacitance values which have been removed from the design by incorporating them into the wire load estimates.

OPT-801 (warning) Removing some annotated net resistances from design '%s'.

DESCRIPTION

One or more net resistance values which were annotated with the **set_resistance** command have been removed from the design. The resistance values for these nets will now be estimated using wire load models.

All annotated net resistance values are removed by the **compile** command (except with the **in_place** option) or the **translate** command.

Annotated net resistance values are preserved wherever possible when running **compile -in_place**, **reoptimize_design -in_place**, or **reoptimize_design -post_layout_opto**.

The **reoptimize_design** command without the **in_place** or **-post_layout_opto** flags preserves annotated net resistance on inter-cluster nets. Annotated resistances are removed from nets enclosed within leaf-level clusters.

WHAT NEXT

The **set_dont_touch** command can be used to maintain annotation on nets during optimization, although it also limits optimization from certain transforms on those

nets. The **dont_touch** attribute can be placed on nets directly and may also be placed on hierarchical cells to keep the capacitances annotated on nets within the hierarchical cell during optimization.

OPT-802 (warning) Removing some annotated pin to pin connect delays.

DESCRIPTION

One or more net delay values which were annotated with the **set_annotated_delay** or **read_timing** commands have been removed from the design. The delay values for these nets will now be estimated using wire load models and the interconnect model defined by the current operating conditions.

The following optimization modes remove all annotated net delay values from the design: **translate** (all modes), **compile** (except **-in_place**), and **reoptimize_design** (except **-post_layout_opto** and **-in_place**).

Annotated net delays are preserved wherever possible when running **compile -in_place**, or **reoptimize_design -in_place**. See the variable **compile_update_annotated_delays_during_inplace_opt** for more information on how these delays are treated during in-place optimization.

The **reoptimize_design** command with the **-post_layout_opto** option preserves annotated net delays on inter-cluster nets. Annotated delays are removed from nets enclosed within leaf-level clusters.

WHAT NEXT

The **set_dont_touch** command can be used to maintain annotation on nets during optimization, although it also limits optimization from certain transforms on those nets. The **dont_touch** attribute can be placed on nets directly and may also be placed on hierarchical cells to keep the capacitances annotated on nets within the hierarchical cell during optimization.

OPT-803 (warning) Removing annotated pin to pin cell delays.

DESCRIPTION

One or more cell-delay or timing-check values that were annotated with the **set_annotated_delay**, **set_annotated_check**, or **read_timing** commands have been removed from the design. The *delay* and *check* values for these cells will be calculated using the library’s delay parameters.

All annotated cell-delay and check values are removed by the **compile** and **reoptimize_design** commands (except where the **-in_place** option is defined) or the

translate command.

Annotated cell-delay and check values are preserved wherever possible when running **compile -in_place** or **reoptimize_design**. See the variable *compile_update_annotated_delays_during_inplace_opt* for more information about how these delays are treated during in-place optimization.

WHAT NEXT

You can use the **set_dont_touch** command to maintain annotation on cells during optimization, although it limits optimization from certain transforms on those cells. During optimization, to keep the capacitances annotated on cells within the hierarchical block, you can place the **dont_touch** attribute directly on leaf cells and on hierarchical blocks.

OPT-804 (information) Removing all annotated delays from design '%s'.

DESCRIPTION

The cell and net delays annotated with the **set_annotated_delay** and **read_timing** commands are removed from the design. Annotated cell and net delays are removed from the design with the **remove_annotated_delay** command.

WHAT NEXT

The cell and net delays are now calculated from the the library timing and from estimations of net length from the wire load models. To re-annotate net and cell delays, use the **set_annotated_delay** or **read_timing** commands.

OPT-805 (warning) Net '%s' already has '%s' for annotated resistance. '%s' is discarded.

DESCRIPTION

A net has already been annotated with a resistance value and has been annotated a second time with a new value. Net resistances are annotated with **set_resistance**.

This warning condition can happen when a net crossing hierarchical boundaries, has different names on either side of the boundary and thus would have been annotated twice. In this case, the maximum net resistance is kept.

WHAT NEXT

Update the script annotating resistances to avoid annotating the net twice. If the resistance value annotated on the net is unacceptable, use the **set_resistance** command to override the value annotated on the net.

OPT-806 (warning) Net '%s' already has '%s' for annotated capacitance. '%s' is discarded.

DESCRIPTION

A net has already been annotated with a capacitance value and is annotated a second time with a new value. Net capacitances are annotated with **set_load**.

This condition can happen when a net crossing hierarchical boundaries, and has different names on either side of the boundary. Thus the net would have been annotated twice. In this case, the maximum net capacitance is kept.

WHAT NEXT

Update the script annotating capacitances to avoid annotating the net twice. If the capacitance value annotated on the net is unacceptable, use the **set_load** command to override the value annotated on the net.

The current design has been modified. To save the changes, use the **write** command.

OPT-807 (warning) Annotation on pin '%s' is invalid because its cell, '%s', is not a leaf cell.

DESCRIPTION

This warning message occurs because pin-to-pin delay and timing-check back-annotation can be done only between pins of leaf cells. Leaf cells are cells that do not contain any other cells. Timing cannot be annotated to or from ports of nonleaf cells because pins of nonleaf cells have no physical location in layout. The tool does not use the timing value to and from the invalid pin.

WHAT NEXT

This is a warning message only. No action is required on your part.

However, to avoid this warning, do not use pins of hierarchical cells with the **set_annotated_delay**, the **set_annotated_check**, and the **set_annotated_transition** commands, or in the timing files read with the **read_timing** command.

SEE ALSO

read_timing (2), **set_annotated_check** (2), **set_annotated_delay** (2), **set_annotated_transition** (2).

OPT-808 (warning) Connect delays annotated to and from this pin are removed.

DESCRIPTION

A connect delay has been annotated to or from an invalid pin. Connect delay can only be annotated between pins of leaf cells. Leaf cells are cells with no hierarchy, cells which do not contain any cells. Timing cannot be annotated to or from ports of non-leaf cells. This is because pins of non leaf-cells have no physical location in layout.

WHAT NEXT

The current design has been modified. To save the changes, use the **write** command. The connect delays annotated to and from this pin are removed from the design database automatically, so that next time the database is loaded, this warning will not appear.

OPT-809 (warning) Cell delays annotated from this pin are removed.

DESCRIPTION

A cell delay has been annotated to or from an invalid pin. Cell delays can only be annotated between pins of leaf cells. Leaf cells are cells which do not contain any cells.

Timing cannot be annotated to or from ports of non-leaf cells. This is because pins of non leaf-cells have no physical location in layout. This error message is generated after **OPT-807** error message. Refer to **OPT-807** error man page for more information on the context of this error message.

WHAT NEXT

The current design has been modified. To save the changes, use the **write** command. The cell delays annotated to and from this pin are removed from the design database automatically, so that next time the database is loaded, this warning will not appear.

OPT-810 (error) Direction of pin '%s' cannot be of type '%s'.

DESCRIPTION

Cell delays can only be annotated from pins of direction input or inout and to pins of direction output or inout. Net delays can only be annotated from pins of direction output or inout and to pins of direction input or inout. The **-net** or **-cell** options of **set_annotated_delay** might be used incorrectly.

Cell and net delays are annotated with **set_annotated_delay**. Cell and net delays can also be annotated with **read_timing**.

WHAT NEXT

Modify the **set_annotated_delay** command for the given pin. Verify the occurences of the given pin in the timing file if **read_timing** was used.

OPT-811 (error) Direction of port '%s' cannot be of type '%s'.

DESCRIPTION

Net delays can also be annotated with **read_timing**. Net delays can only be annotated from pins with direction output or inout. Net delays can only be annotated to pins with direction input or inout. Net delays can be annotated between leaf cell pins and between the top level ports of the current design and leaf cell pins. If the driver pin of the annotated net is a port, the port direction must be input or inout. If the load pin of the annotated net is a port, the port direction must be output or inout.

Net delays are annotated with **set_annotated_delay -net**.

WHAT NEXT

Verify the use of **set_annotated_delay** command for the given port. Verify the use of the given port in the timing file if **read_timing** was used. Annotate the delay to or from the given port with **set_annotated_delay**.

OPT-812 (warning) Object '%s' is invalid. It must be a pin of a leaf cell or a port.

DESCRIPTION

Cell delays are annotated between input and output pins of leaf cells. Net delays can be annotated between leaf cells pins and between the ports of the current design

and leaf cell pins. A leaf cell is a cell which do not contain other cells. The given object is invalid if it is a pin of a non-leaf cell.

To annotate the given object, it should be a pin on a leaf cell or a port at the top level of the current design. All other object types are invalid for annotation. Net and cell delays are annotated with **set_annotated_delay**. Net and cell delays can also be annotated with **read_timing**.

WHAT NEXT

Verify the use of **set_annotated_delay** command with the given object. Verify the use of the given object in the timing file if **read_timing** was used.

OPT-813 (warning) Timing check annotated to and from this pin is removed.

DESCRIPTION

A timing check has been annotated to or from an invalid pin. Timing checks can be annotated only between pins of leaf cells. Leaf cells are cells with no hierarchy; they are cells that do not contain any cells. Timing cannot be annotated to or from ports of nonleaf cells because pins of nonleaf cells have no physical location in the layout.

WHAT NEXT

The current design has been modified. To save the changes, use the **write** command. The timing checks annotated to and from this pin are removed from the design database automatically so that the next time the database is loaded, this warning will not appear.

OPT-814 (error) Pins '%s' and '%s' are not on the same cell.

DESCRIPTION

For back-annotation of timing checks, the from and to pins must be on the same cell.

WHAT NEXT

Enter the command again with pins that are on the same cell.

OPT-815 (warning) There is no '%s' timing arc between pins

’%s’ and ’%s’.

DESCRIPTION

Back-annotated delays or timing checks on cells require that there be a corresponding timing arc on the referenced library cell. When no clock edge is specified in the SDF file, **read_timing** attempts to annotate the timing check on the timing arc with both clock rising and clock falling, thus possibly generating this warning message if the library has only either a clock rising or a clock falling timing check. This warning is not generated for HOLD if the library contains a removal timing check between the pins specified with the SDF HOLD construct, because the SDF HOLD construct is recommended for specifying removal timing checks.

WHAT NEXT

Check the library for a possible missing timing arc. Also, ensure that the direction of the arc is correct; for example, setup arcs must go from the clock pin to the data pin. For further information, refer to the appropriate command manual page.

OPT-822 (warning) Pins (or ports) ’%s’ and ’%s’ are not on the same net.

The back-annotated data between these two objects is removed.

DESCRIPTION

A net delay is back-annotated, but the two pins specified with **set_annotated_delay** , or in the timing file read with **read_timing**, are not on the same net. The net delays annotated from the given pin have been removed from the design.

WHAT NEXT

Verify the **set_annotated_delay** commands are used for pins on the same net, or verify the timing file specifies pin-to-pin timing for pins on the same net. Since the design database has been modified, to save the changes, write the design with the command **write**.

OPT-830 (information) Removing annotated delays from pin

’%s’ to pin ’%s’.

DESCRIPTION

The command **remove_annotated_delay** removes annotated delay between pins on the same net or cell. Use **remove_annotated_delay -to** to remove annotated delays set with **set_annotated_delay -to** . Use **remove_annotated_delay -from** to remove annotated delays set with **set_annotated_delay -from** . Use **remove_annotated_delay -from -to** to remove annotated delays set with **set_annotated_delay -from -to**.

WHAT NEXT

The design database has been modified. To save the changes, use the **write** command.

OPT-831 (information) Removing delays annotated to pin ’%s’.

DESCRIPTION

The command **remove_annotated_delay -to** removes annotated delay up to the given pin. Use **remove_annotated_delay -to** to remove annotated delays set with **set_annotated_delay -to** . Use **remove_annotated_delay -from** to remove annotated delays set with **set_annotated_delay -from** . Use **remove_annotated_delay -from -to** to remove annotated delays set with **set_annotated_delay -from -to**.

WHAT NEXT

The design database has been modified. To save the changes, use the **write** command.

OPT-832 (information) Removing delays annotated from pin ’%s’.

DESCRIPTION

The command **remove_annotated_delay -from** removes annotated delay from the given pin. Use **remove_annotated_delay -to** to remove annotated delays set with **set_annotated_delay -to** . Use **remove_annotated_delay -from** to remove annotated delays set with **set_annotated_delay -from** . Use **remove_annotated_delay -from -to** to remove annotated delays set with **set_annotated_delay -from -to**.

WHAT NEXT

The design database has been modified. To save the changes, use the **write** command.

OPT-833 (info) Deleted pin to pin delay values will be approximated via automatically annotated resistance.

DESCRIPTION

There are certain conditions under which annotated pin-to-pin net delays must be deleted; for details, refer to the OPT-802 man page. If delay is deleted during the use of **reoptimize_design -post_layout**, then the deleted delay annotation is approximated by automatically annotating resistance values. These values are calculated using the annotated pin-to-pin delays, annotated capacitance, and the delay equation appropriate for the current tree delay model. Note that if the tree type is 'best_case_tree', then no resistance annotation will be done, because wire delay is assumed to be 0 for this tree type.

WHAT NEXT

OPT-834 (warning) There is no timing annotated between pin '%s' and pin '%s'.

DESCRIPTION

You have tried to remove annotated delay set between two pins, where there is no delay annotated between the specified pins. This problem will occur when there is no timing arc between the specified pins. Either the two given pins are not on the same net or are not on the same cell or are on the same cell but there is no timing arc defined in the library between them. This can also happen if there was no delay annotated between the two pins.

WHAT NEXT

If you have specified valid pins, then no annotation is present. If you have not specified valid pins, then make this correction to your design.

OPT-835 (warning) Overwriting the %s delay between pin '%s' and pin '%s' with (%f).

DESCRIPTION

The rise/fall delay between the specified pins was already annotated. This is because *set_net_delay* was used multiple times and in different ways to specify the delay between the two pins. This created an ambiguity. For example, an ambiguity can appear when using *set_net_delay <value1> -from <pin_A>* and *set_net_delay <value2> -*

to <pin_B> where *pin_A* and *pin_B* are on the same net.

WHAT NEXT

No action is required. To eliminate the warning, check the back-annotation on each pin and remove the ambiguity. To remove annotated delays, use the *remove_delay* command. To check the delay annotated between two pins, use the command *report_annotated* or *report_timing -from <pin> -to <pin> -input_pin*.

OPT-836 (Information) Annotated delays on net/cells have been modified/deleted.

DESCRIPTION

When cells are swapped, the connect delays on nets connected to the swapped cells are updated to reflect the change of pin capacitance due to the new cells. The annotated connect delays on nets connected to the swapped cells have been incrementally modified. If the net resistance is zero, net delays will not be modified. If the net resistance is different than zero (worst case or balanced case) the annotated net delay is modified relative to the difference in pin capacitance.

Annotated delays are removed from cells in both the immediate fanout and the immediate fanin of a swapped cell. The delays through cells in the immediate fanout may have changed due to the different drive capability of the new cell. Delays through cells in the immediate fanin may have changed due to the change in load capacitance.

Back-annotated delays are updated in order to maintain delay accuracy while the design is being modified. More information is available in the **compile_update_annotated_delays_during_inplace_opt** man page. To avoid updating annotated delays, set **compile_update_annotated_delays_during_inplace_opt** to **false**.

WHAT NEXT

OPT-837 (Warning) Design '%s' already has annotated delays, read_timing and set_annotated_delay only annotate worse delays.

DESCRIPTION

The design already has annotated delays. **read_timing** and **set_annotated_delay** only annotated delays that were greater than the initially annotated delays. If you wish to overwrite previously annotated delays, independently of their values, use **remove_annotated_delay -all** before using **read_timing** or **set_annotated_delay**. The

worst option is useful when reading a timing file which might contain conditional timing. Refer to the **read_timing** and **set_annotated_delay** man pages for more information on the **worst** option.

WHAT NEXT

Use **remove_annotated_delay -all** and back-annotate the timing again if you wish to overwrite all old annotated delays with delays in the timing file. Use **set_annotated_delay** without the **worst** option, if you wish to overwrite old annotated delays with new delays.

OPT-850 (error) %s '%s' has annotated delays already including load delay.

Annotate delays including load delay or remove old annotated delays.

DESCRIPTION

The commands **set_annotated_delay** and **read_timing** annotate delays on cells and nets. You tried to annotate delays without load delay on a cell or a net that already has annotated delays including load delay. Delays must be consistently annotated on each cell and net. You either need to annotate delay values that include the load delay or remove the previously annotated delays before annotating new delays.

Load delay (also known as extra source gate delay) is the portion of cell delay which is due to the capacitive load of the net being driven. Some delay calculators consider load delay part of the net delay and others consider it part of the cell delay.

You specify that the load delay is included in the net delay values by using the **-load_delay net** option of **set_annotated_delay** or **read_timing**. You specify that the load delay is included in the cell delay values by using the **-load_delay cell** option of **set_annotated_delay** or **read_timing**.

WHAT NEXT

If the net delay values you wish to annotate include the load delay, use **-load_delay net** option of **set_annotated_delay** or **read_timing**. If the cell delay values you wish to annotate include the load delay, use the **-load_delay cell** option of **set_annotated_delay** or **read_timing**.

If the delay values you wish to annotate do not include the load delay, remove the existing annotated delays on the cell or net before proceeding in the back-annotation. To do so, run **report_annotated_delay** with **-net** or **-cell** option to report the annotated delays. Then, use **remove_annotated_delay** or **reset_design** to remove the annotated delays. Then use **read_timing** or **set_annotated_delay** to proceed in the delay back-annotation.

SEE ALSO

read_timing(2), set_annotated_delay(2).

OPT-851 (error) %s '%s' already has annotated delays, and these annotated delays do not include load delay. You must either annotate delays without including load delay; or remove old annotated delays.

DESCRIPTION

The commands **set_annotated_delay** and **read_timing** annotate delays on cells and nets. You have tried to annotate a delay value that includes load delay on a cell or a net that already has annotated delays that do not include load delay. You need to annotate delay values without including the load delay or remove the previously annotated delays before annotating new delays.

Load delay is also known as extra source gate delay, and is the portion of cell delay caused by the capacitive load of the net being driven. Some delay calculators consider load delay part of the net delay and others consider it part of the cell delay.

You specify that the load delay is not included in the net delay values by using the **-load_delay cell** option of **set_annotated_delay** or **read_timing**. You specify that the load delay is not included in the cell delay values by using the **-load_delay net** option of **set_annotated_delay** or **read_timing**.

WHAT NEXT

If the cell or net delay values you wish to annotate do not include the load delay, use the **-load_delay net** or **-load_delay cell** options of **read_timing** or **set_annotated_delay**.

If the cell or net delay values you wish to annotate include the load delay, remove the annotated delays on the cell or net before proceeding with back-annotation. To remove annotated delays, first report them by running **report_annotated_delay** with the **-net** or **-cell** option. Next, use **remove_annotated_delay** or **reset_design** to remove the annotated delays. Finally, use **read_timing** or **set_annotated_delay** to proceed in the delay back-annotation.

SEE ALSO

read_timing(2), set_annotated_delay(2).

OPT-852 (warning) Use of the best_case_tree delay model

during reoptimize_design -post_layout is discouraged.

DESCRIPTION

This message indicates that you have used the best_case_tree model during **reoptimize_design**. During **reoptimize_design -post_layout**, all pin-to-pin net delays are deleted for nets that do not cross cluster boundaries. If the best_case_tree delay model is used, nets that do not have back-annotation will have 0 delay.

WHAT NEXT

Change the operating conditions so that the best_case_tree delay model is not used.

OPT-853 (warning) Target library does not contain any 2-1 multiplexor.

DESCRIPTION

The design contains generic multiplexor cells (MUX_OP). They were created by HDL Compiler (TM) because either the variable hdlin_infer_mux = all or the HDL code contains comments with infer_mux process_label. MUX_OP cells in the design were implemented without trees of multiplexors. This may severely effect quality of results.

WHAT NEXT

Add a library with a 2-1 multiplexor in the search path to make multiplexor mapping possible. Or turn off the multiplexor mapping feature by overriding the infer_mux directives in the HDL with hdlin_infer_mux = none. Or remove the infer_mux directives from the HDL code.

OPT-854 (warning) Ignoring dont_touch attribute on cell(s) in multiplexor implementation ’%s’

DESCRIPTION

The multiplexor mapping functionality supports specification of the "dont_touch" attribute only on the entire multiplexor implementation. If a "dont_touch" is specified on a cell(or collection of cells) within the implementation, the "dont_touch" attribute is ignored.

WHAT NEXT

In order to apply a "dont_touch" attribute to a multiplexor implementation use the set_dont_touch command and specify the instance-name of the multiplexor implementation (e.g. U7/U4).

OPT-855 (error) Cannot estimate resistance or capacitance per unit length

DESCRIPTION

Cannot find enough back-annotated data for estimating the resistance or capacitance per unit length in the current design.

WHAT NEXT

Try to back annotate enough physical information for the current design, or change the option criteria. Possible commands are: set_load, read_sdf, read_pdef.

OPT-860 (Information) Back-annotated pin delays for Net: %s is ignored because net belongs to a clock mesh.

DESCRIPTION

The tool is ignoring the back-annotated pin-to-pin delays values for the specified net because the specified net is part of a clock mesh.

WHAT NEXT

To turn off the above filtering, please set variable ba_pin_annotation_filter_clock_mesh to FALSE.

OPT-900 (error) replace_fpga terminated abnormally.

DESCRIPTION

This message indicates that an error occurred during the execution of the command *replace_fpga* which caused the command to abort. The intermediate design was not written back to the database. The *current_design* is not changed. The reason for the abnormal termination should have appeared in an error message previous to this one.

WHAT NEXT

Resolve errors and rerun *replace_fpga*.

OPT-901 (error) replace_fpga interrupted. Saving intermediate design.

DESCRIPTION

A CONTROL-C interrupt was recieved by the *replace_fpga* command. The design in its current state is being written back to the database. Note that some fpga cells may not be converted to their gate level equivalents and further generic logic may be present.

WHAT NEXT

OPT-902 (warning) This site does not have an FPGA License. Trying to obtain a CMOS license and enable CMOS optimizations. NO FPGA SPECIFIC OPTIMIZATIONS WILL BE ENABLED !

DESCRIPTION

The command executed required an FPGA license. Your site does not have an FPGA license (if such a license existed at your site the command would have aborted and this error message would not have appeared). The command will continue and attempt to obtain a CMOS license. If a CMOS license is obtained, the command will continue assuming the technology is CMOS. For example, if the command is *compile* then only CMOS related optimization will be performed.

WHAT NEXT

OPT-903 (error) The technology of the target library is the Xilinx %s series FPGA. Optimization requires that the library contain the Xilinx programmable cell core cell(CLB). Either the CLB cell does not exist in the library or a dont_use attribute has been

placed on the cell.

DESCRIPTION

Optimization, translation, and mapping that target a Xilinx FPGA technology requires that the library contain a Xilinx programmable core cell (CLB).

WHAT NEXT

Use the the **report_lib** command to check the library for the existence of Xilinx programmable core cell (CLB). If it does not exist, contact Xilinx. If it does exist, there may be a **dont_use** attribute on the CLB cell. Remove the **dont_use** attribute on the CLB cell.

OPT-904 (warning) The replace_fpga command has already been run on this design, or sub-designs below this design. The proper methodology is to run replace_fpga AFTER this command.

DESCRIPTION

It is important to understand that **replace_fpga** removes CLBs and IOBs, and replaces them with primitive components in the Xilinx library. At the same time, **replace_fpga** places important mapping information on your design; this mapping information is used by the XNF writer to create Xilinx FMAP and HMAP directives for your design. These directives control how logic is divided among the CLBs and IOBs that are actually built for your design.

Remember also that **replace_fpga** is a necessary step that must be run before writing out XNF for your design. This is because Xilinx does not accept CLB or IOB symbols in their XC4000 family XNF. Instead, you must make sure that your XNF is in terms of primitive components. That's where **replace_fpga comes in. By running replace_fpga** before writing out a design, you can be sure that the design is implemented only in primitive gates.

This warning message tells you that **replace_fpga** has previously been run on this design, or subsections of this design, and that it is a methodology error to run the command from which this error was issued after running **replace_fpga**.

WHAT NEXT

Make sure that you, or your script, only invokes **replace_fpga** just before writing out the design to XNF. Only run the current command (the one that generated this error) BEFORE running **replace_fpga**, not after running **replace_fpga**.

OPT-905 (warning) The replace_fpga command has already been run on this design, or sub-designs below this design. Partitioning information created by replace_fpga may become invalid as a result. The proper methodology is to run replace_fpga AFTER this command.

DESCRIPTION

It is important to understand that **replace_fpga** removes CLBs and IOBs, and replaces them with primitive components in the Xilinx library. At the same time, **replace_fpga** places important mapping information on your design; this mapping information is used by the XNF writer to create Xilinx FMAP and HMAP directives for your design. These directives control how logic is divided among the CLBs and IOBs that are actually built for your design.

Remember also that **replace_fpga** is a necessary step that must be run before writing out XNF for your design. This is because Xilinx does not accept CLB or IOB symbols in their XC4000 family XNF. Instead, you must make sure that your XNF is in terms of primitive components. That's where **replace_fpga comes in. By running replace_fpga** before writing out a design, you can be sure that the design is implemented only in primitive gates.

This warning message tells you that **replace_fpga** has previously been run on this design, or subsections of this design. Since each invocation of **replace_fpga** (1) removes any pre-existing mapping information and then (2) replaces existing CLBs and IOBs by primitive gates, you can see that repeatedly calling **replace_fpga** can destroy mapping information on your design. This can possibly result in a lower quality circuit.

WHAT NEXT

Make sure that you, or your script, only invokes **replace_fpga** once on a design.

OPT-906 (error) The FPGA cell '%s' does not contain the proper instance specific configuration information.

DESCRIPTION

This error message, which indicates an illegal design, occurs when the identified FPGA cell does not contain the proper instance-specific configuration information. An example is when a design is saved using a format (such as Edif, Verilog, VHDL, and so forth) that is not the Synopsys DB format, and is then read back into Synopsys. If this is not the case, the DB file must be corrupt. Currently, FPGA designs created by compile that contain programmable cells can be saved only in DB format.

WHAT NEXT

You must recreate the original compiled design. If the original compiled design was saved in DB format, it can be read back into Synopsys.

OPT-907 (warning) Inverter Removal Optimization is being disabled because an FPGA license is not available.

DESCRIPTION

The specialized optimization for removing inverters is being turned off for this design, because a valid FPGA license was not available. FPGA Compiler or FPGA Option must be enabled before this extra optimization will be done.

WHAT NEXT

OPT-908 (warning) FPGA-specific Library Component Optimization is being disabled because an FPGA license is not available.

DESCRIPTION

This warning message occurs when your library contains components whose use requires an FPGA license. When such a library is encountered, the optimizer first tries to acquire an FPGA license. If this is not possible, **compile** continues, with the FPGA-specific optimization disabled.

WHAT NEXT

OPT-909 (error) The target technology is '%s'. Using fpga_shell or fpga_analyzer requires that the target technology be FPGA.

DESCRIPTION

Either **fpga_shell** or **fpga_anlyzer** is being used, and an attempt has been made to optimize a design with the *target_library* set to a non-FPGA technology library. The **fpga_shell** or **fpga_analyzer** tools can be used only to optimize and map to FPGA technologies.

WHAT NEXT

Use **dc_shell** or **design_analyzer** instead of **fpga_shell** or **fpga_analyzer**.

OPT-910 (error) Target library must contain a usable N-input lut cell.

DESCRIPTION

This message indicates that one of the target libraries (as specified by the **dc_shell target_library** library variable) is a lut technology library, and no usable lut library cells can be found in any of the target libraries. The lut library must contain at least one lut library cell.

WHAT NEXT

Use **remove_attribute** to remove the **dont_use** attribute from one of the lut library cells.

OPT-911 (warning) Target library contains multiple lut output marker cells.

DESCRIPTION

This warning message occurs when the target libraries, as specified by the **dc_shell target_library** variable, contain more than one lookup table (lut) output marker cell. In this case, the **replace_fpga** command will use the first output marker cell that it finds. This warning indicates that it is possible for your library to be incorrect, because it has more than one lut output marker cell; or that in using multiple target libraries you have created a situation where more than one marker cell is available for **replace_fpga** to use.

WHAT NEXT

The lut library should contain only one lut output marker library cell. Make sure that **replace_fpga** is building your design with the marker cell that you expect it to use. If the desired marker cell is not being used, consider placing a **dont_use** attribute on the extra marker cell(s).

OPT-912 (warning) replace_fpga is not valid for designs implemented

with this target library. Use the ’-force’ option to override this message.

DESCRIPTION

This message indicates that you do not need to use **replace_fpga** for designs implemented in your current technology. If you are using an Altera library, your target library (as specified by the **dc_shell target_library** library variable) does not contain a usable lut output marker library cell. If you are using a Xilinx technology library, **replace_fpga** is not needed as part of your design flow.

Replacing lut cells is an irreversible process, so **replace_fpga** performs methodology checks to prevent its own execution if it determines that running **replace_fpga** on your design would be a methodology error.

WHAT NEXT

First, determine whether you really need to run **replace_fpga** in your design methodology. Some technology libraries (for example, Altera) require this command; but others (for example, Xilinx 3k family) do not. Use **replace_fpga -force** to disable the methodology checks, if 1) your FPGA vendor does require replacement of lut cells by gate equivalents but does not have an output marker cell in the library; or 2) you simply want to do a trial replacement without the risk of aborting.

For more information about using the **-force** option, refer to the **replace_fpga** manual page.

OPT-913 (error) Aborting replace_fpga due to lack of a usable output marker cell.

DESCRIPTION

This message indicates that the target libraries (as specified by the **dc_shell target_library** library variable) are lut technology but do not contain a usable lut output marker library cell. replace_fpga must abort. This message typically indicates a methodology error; that is, you might not need or want to run **replace_fpga**.

Replacing lut cells is an irreversible process, so **replace_fpga** performs methodology checks to prevent its own execution if it determines that running **replace_fpga** on your design would be a methodology error.

WHAT NEXT

First, determine whether you really need to run **replace_fpga** in your design

methodology. Some technology libraries (for example, Altera) require this command; but others (for example, Xilinx 3k family) do not. Use **replace_fpga -force** to disable the methodology checks, if 1) your FPGA vendor does require replacement of lut cells by gate equivalents but does not have an output marker cell in the library; or 2) you simply want to do a trial replacement without the risk of aborting.

For more information about using the **-force** option, refer to the **replace_fpga** manual page.

OPT-914 (warning) No single bit degenerate for multibit library cell '%s'.

DESCRIPTION

This message indicates that the target library/libraries (as specified by the **dc_shell target_library** library variable) have no single bit version of the multibit component named above. This means that the multibit element will not be constructed as part of the multibit component optimization process inside compile. Multibit optimization requires that a "single bit" version of each multibit component must exist in the target library.

WHAT NEXT

If you do not want this component to be built by **compile**, then you can ignore the warning. If, however, you do want **compile** to construct such gates then you'll need to modify your target library to contain a component which is a single bit version of the named multibit component.

OPT-915 (warning) Cannot perform multibit optimization on '%s' '%s'.

DESCRIPTION

This message indicates that multibit optimization cannot be performed on a cell or a multibit component. The reasons include having a don't touch attribute, having local optimization disabled, the multibit component not being sufficiently wide, or the multibit component having cells with differing functionalities.

WHAT NEXT

If this condition occurs, it means that the multibit optimization could not be performed on the design object indicated. If this is the desired effect, you can ignore this warning. Otherwise, check the multibit component or cell indicated and ensure that the aforemetioned conditions are avoided. Use the **create_multibit** or

remove_multibit commands to manipulate multibit components then rerun the **compile** command.

SEE ALSO

create_multibit (2), **remove_multibit** (2), **report_multibit** (2).

OPT-916 (warning) Incorrect setting for bus naming style variables.

DESCRIPTION

The variables **bus_naming_style**, **bus_range_separator_style**, and **bus_multiple_separator_style** are used to generate names for multibit components. Set these variables to values so that a name can be unabiguously parsed to extract the base name and component bits of the name. The conditions checked are

a. range and multiple separators cannot be empty.
b. range separator, multiple separator, and bus_naming_style need to be distinct.
c. range separator, multiple_separator, and bus_naming_style cannot contain digits.

WHAT NEXT

If this condition occurs, check the settings of **bus_naming_style**, **bus_range_separator_style**, and **bus_multiple_separator_style**. Set them to values that meet the aforementioned conditions and rerun the **compile** command. You need to reread HDL files if you change settings of these variables.

SEE ALSO

bus_naming_style (3), **bus_range_separator_style** (3), **bus_multiple_separator_style** (3).

OPT-917 (warning) Losing member of multibit component '%s'.

DESCRIPTION

This message indicates that some optimization, which is being performed on a member of a multibit component, cannot reliably assign a new cell to the component. As a result the multibit component might have missing bits.

WHAT NEXT

If this condition occurs, please report this testcase to Synopsys. The design will

still be logically correct, but the multibit components might not have the desired structure.

SEE ALSO

create_multibit (2), **remove_multibit** (2), **report_multibit** (2).

OPT-918 (warning) Multibit library cell '%s' will not be used in multibit optimization.

DESCRIPTION

This message indicates that the target library (as specified by the **dc_shell target_library** library variable), containing the multibit library cell named previous, was not compiled using the latest version of Library Compiler, or that the multibit cell was too complex to be recognized. As a result, some attributes needed to use this multibit library cell in optimization are missing. This means that this multibit library cell will not be constructed as part of the multibit component optimization process inside **compile**.

WHAT NEXT

If you do not want this component to be built by **compile**, you can ignore the warning. However, if you want **compile** to construct such gates, you need to use the latest version of Library Compiler on your target library, so that all the relevant attributes are available to **compile**. If the cell is too complex to be recognized by Library Compiler, it must be instantiated and cannot be inferred.

OPT-919 (warning) Invalid value '%d' for environment variable '%s'; resetting it to '%d'.

DESCRIPTION

This warning indicates that the specified environment variable contains an invalid value. Valid values for the variable are from -1 to 5.

WHAT NEXT

If the default value assigned to the environment variable is not acceptable, set the variable to one of the valid values specified above.

EXAMPLE MESSAGE

```
Warning: Invalid value '10' for environment variable 'compile_dash_top_drc_levels';
resetting it to '-1'. (OPT-919)
```

OPT-920 (Error) Found an unmapped cell '%s' in the design.

DESCRIPTION

The design contains unmapped logic. You cannot use the **-top** option of the **compile** command on designs that contain unmapped logic.

WHAT NEXT

Check the design to ensure that all cells are mapped before running **compile -top**.

EXAMPLE MESSAGE

```
Error: Found an unmapped cell 'adder' in the design. (OPT-920)
```

OPT-931 (information) High fanout net '%s' is not %s.

DESCRIPTION

You receive this message because this Net has more than 1000 pins. The recommended methodology is to set this net as **ideal_net**, as well as to set all timing paths through it as **false_path** so that it does not impact optimization. The high fanout net should be optimized at a separate stage with, for example, the **create_buffer_tree** command.

WHAT NEXT

Use the **set_ideal_net** command to mark this net as **ideal_net**. Use the **set_false_path** command to mark timing paths through this net as **false_path**.

EXAMPLE MESSAGE

```
Warning: High fanout net NET_B is not on false_path. (OPT-931)
```

SEE ALSO

create_buffer_tree (2), **set_false_path** (2), **set_ideal_net** (2).

OPT-932 (Warning) High fanout net '%s' is skipped by global route.

DESCRIPTION

You receive this warning message when you execute the **reoptimize_design** command, and a net with more than 10000 pins exists in the design. Global routing will not occur on this net because the allowed pin limit for an individual net has been exceeded.

EXAMPLE MESSAGE

Warning: High fanout net NET_A is skipped by global route. (OPT-932)

WHAT NEXT

This is a warning message. No action is required on your part.

OPT-933 (information) Dont_touch on cell '%s' of design '%s' will be ignored by compile because it contains unmapped synthetic cells.

DESCRIPTION

A **dont_touch** attribute has been placed on a cell that contains some unmapped synthetic logic. This **dont_touch** attribute will be ignored by **compile** to allow the unmapped logic to be mapped.

WHAT NEXT

This is an informational message. Unless your design requires the **dont_touch** functionality on the specified cell, no further action is required. If the **dont_touch** functionality is needed, the design must be restructured.

OPT-934 (information) High fanout net '%s' is not %s.

DESCRIPTION

You receive this message because this net has more than 1000 pins. The recommended methodology is to set this net as **ideal_net**, as well as to set all timing paths

through it as **false_path** so that it does not impact optimization. The high fanout net should be optimized at a separate stage with, for example, the **create_buffer_tree** command.

WHAT NEXT

Use the **set_ideal_net** command to mark this net as **ideal_net**. Use the **set_false_path** command to mark timing paths through this net as **false_path**.

EXAMPLE MESSAGE

Warning: High fanout net NET_B is not ideal_net. (OPT-934)

SEE ALSO

create_buffer_tree (2), **set_false_path** (2), **set_ideal_net** (2).

OPT-935 (Warning) Top-level nets do not have enough back-annotations to calculate RC value. Design Compiler will use all back-annotated nets for RC calculation.

DESCRIPTION

The **reoptimize_design** command using the **-top** option tries to come up with an estimated RC value using only back-annotated nets in the top-level only. If enough top-level nets are not back-annotated, Design Compiler uses all back-annotated nets in the design. This method takes more time to calculate RC value, but produces more accurate RC values.

WHAT NEXT

Make sure there are enough top-level nets to derive RC value.

SEE ALSO

compile (2), **reoptimize_design** (2).

OPT-936 (Information) Top level nets have enough back-annotations, so Design Compiler (DC) used back-annotated,

top-level nets for R and C calculation.

DESCRIPTION

You receive this message to inform you that enough top-level nets are back-annotated. As a result, the **reoptimize_design** command **-top** option can calculate the R/C value with back-annotated nets only in the top level. If enough top-level nets were not back-annotated, Design Compiler (DC) would use all back-annotated nets in the entire design.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

reoptimize_design (2).

OPT-937 (Information) Design Compiler (DC) is always forced to use back-annotated, top-level nets for R and C calculation if at least one top-level net is back-annotated.

DESCRIPTION

You receive this message to inform you of the following useful instruction. The **reoptimize_design** command **-top** option attempts to calculate an R/C value with back-annotated nets only in the top level, if enough top-level nets are back-annotated. Otherwise, Design Compiler (DC) uses all back-annotated nets for R/C calculation. If you use the **reopt_design_top_estimates_RC_with** variable with the **always_top_level_nets** option, DC always uses back-annotated top-level nets to the extent that at least one exists.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

reoptimize_design (2), **reopt_design_top_estimates_RC_with** (3).

OPT-938 (Information) Design Compiler (DC) is always forced

to use all back-annotated nets in the entire design for R and C calculation.

DESCRIPTION

You receive this message to inform you of the following useful instruction. The **reoptimize_design** command **-top** option attempts to calculate an R/C value with back-annotated nets only in the top level if enough top-level nets are back-annotated. Otherwise, Design Compiler (DC) uses all back-annotated nets for R/C calculation. If you use the **reopt_design_top_estimates_RC_with** variable with the **always_top_level_nets** option, DC always uses all back-annotated nets in the entire design even if top-level nets have enough back-annotations.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

reoptimize_design (2). **reopt_design_top_estimates_RC_with** (3).

OPT-939 (Warning) No top-level nets have back-annotation that can be used to calculate the R and C value. Design Compiler (DC) uses all back-annotated nets for R and C calculation.

DESCRIPTION

You receive this message because no annotated top-level nets are found that Design Compiler (DC) can use to calculate the R/C value. By default, the **reoptimize_design** command **-top** option attempts to calculate an R/C value with back-annotated nets only in the top level. If there are not enough back-annotated top-level nets, DC uses all back-annotated nets in the entire design. If you use the **reopt_design_top_estimates_RC_with** variable with the **always_top_level_nets** option, DC always uses back-annotated top-level nets to the extent that at least one exists.

WHAT NEXT

Ensure that at least one top-level net is back-annotated to use for deriving an R/C value.

SEE ALSO

reoptimize_design (2). **reopt_design_top_estimates_RC_with** (3).

OPT-940 (error) Virtex target library is missing the following required gate%s:

DESCRIPTION

The specified fpga_technology of the target_library is from the Xilinx Virtex family (Virtex, Virtex II, Virtex E) but the library is missing required gates. Assuming the vendor library originally had all of the required gates, this error should only happen if the user has explicitly done 'set_dont_use' on one or more of these gates.

WHAT NEXT

Remove the 'dont_use' from listed gates.

SEE ALSO

set_dont_use (2).

OPT-941 (error) Cannot find buffer '%s' in target library.

DESCRIPTION

The cell name specified could not be found in the target library.

WHAT NEXT

Check to make sure that the target_library is set correctly and that this cell is contained in the library. The 'report_lib' command can be used to list library cells.

SEE ALSO

report_lib (2). **set_fpga_global_buffer** (2). **set_fpga_global_buffer_min_fanout** (2).

OPT-942 (error) Cell '%s' is not a buffer.

DESCRIPTION

The cell specified must be a non-inverting buffer.

WHAT NEXT

Specify a valid buffer cell.

SEE ALSO

set_fpga_global_buffer (2). **set_fpga_global_buffer_min_fanout** (2).

OPT-943 (information) Minimum fanout for internal clock buffering is %d.

DESCRIPTION

Internal clock nets (those not driven by a top-level pad) will not be considered for a global-buffer if they have fanout less than the value specified by the 'set_fpga_global_buffer_min_fanout -clock' command.

WHAT NEXT

SEE ALSO

set_fpga_global_buffer (2). **set_fpga_global_buffer_min_fanout** (2).

OPT-944 (information) Minimum fanout for internal non-clock buffering is %d.

DESCRIPTION

Internal non-clock nets (nets which are not a clock source) will not be considered for a global-buffer if they have fanout less than the value specified by the 'set_fpga_global_buffer_min_fanout -non_clock' command.

WHAT NEXT

SEE ALSO

set_fpga_global_buffer (2). **set_fpga_global_buffer_min_fanout** (2).

OPT-945 (information) Buffering of internal non-clock nets is

disabled.

DESCRIPTION

Internal non-clock nets (nets which are not a clock source) will not be considered for a global-buffering.

WHAT NEXT

SEE ALSO

set_fpga_global_buffer (2). **set_fpga_global_buffer_min_fanout** (2).

OPT-946 (information) Buffering of internal clock nets is disabled.

DESCRIPTION

Internal clock nets (those not driven by a top-level pad) will not be considered for a global-buffering.

WHAT NEXT

SEE ALSO

set_fpga_global_buffer (2). **set_fpga_global_buffer_min_fanout** (2).

OPT-947 (error) Could not find resource ’%s’ in target library.

DESCRIPTION

The specified resource name was not found in the target library. Note that resource names are not necessarily the same as library cell names because a cell may use multiple resources.

WHAT NEXT

Use ’set_fpga_resource_limit -show_all’ to see list of all valid resource names for the current target library.

SEE ALSO

set_fpga_resource_limit (2). **set_fpga_target_device** (2).

OPT-948 (information) No resource limits specified.

DESCRIPTION

No user-specified resource limits have been placed on the current_design. By default resource limits come from the specified target device and no user-interaction is required to specify them. However, if the user wishes to override a part value then the 'set_fpga_resource_limit' command can be used to do so. For example, in a bottom-up compile methodology it may be desireable to limit the resources allocated to the current block being compiled to a value less than the part maximum.

WHAT NEXT

SEE ALSO

set_fpga_resource_limit (2). **set_fpga_target_device** (2).

OPT-949 (error) Speed grade '%s' is not valid for part '%s'.

DESCRIPTION

The specified speed-grade is not valid for this target device.

WHAT NEXT

Use 'set_fpga_target_device -show_all' to see valid speed grades.

SEE ALSO

set_fpga_target_device (2). **set_fpga_resource_limit** (2).

OPT-950 (error) Could not find part '%s' in target library.

DESCRIPTION

The specified part name could not be found in the target library.

WHAT NEXT

Use ’set_fpga_target_device -show_all’ to see valid device names.

SEE ALSO

set_fpga_target_device (2). **set_fpga_resource_limit** (2).

OPT-951 (information) Target device for current design is ’%s’.

DESCRIPTION

This is the specified target device for this design.

WHAT NEXT

Use ’set_fpga_target_device -show_all’ to see all valid device names.

SEE ALSO

set_fpga_target_device (2). **set_fpga_resource_limit** (2).

OPT-952 (Error:) No target device specified for current design.

DESCRIPTION

No target device has been specified for the current design.

WHAT NEXT

Use ’set_fpga_target_device -show_all’ to see all valid device names.

SEE ALSO

set_fpga_target_device (2). **set_fpga_resource_limit** (2).

OPT-953 (warning) Multiple pads are connected to port '%s'.

DESCRIPTION

The instantiated pads at port '%s' are not correct for this technology. This may be caused by illegal connection of pads at the port's net (i.e. a non-pad cell or an extra pad cell is on the net in addition to the pad cells).

WHAT NEXT

Check the pad cells instantiated at this port and modify the cells or attributes which define the pad configuration at this port.

OPT-954 (warning) Cell '%s' count in design has violated the max_count value in the library. The design has '%d' instances but PART contains only '%d'.

DESCRIPTION

Design contains excess '%s' instantiated components. It has '%d' instances but PART contains only '%d'.

WHAT NEXT

Use a part that contains more resources than used or limit the no. of instances in the design.

OPT-955 (warning) LPM_TYPE parameter on cell '%s' does not match with the name of the cell reference

DESCRIPTION

There is a mismatch between the value of parameter LPM_TYPE set on cell '%s' and the name of the cell reference. This may lead to error during Place and Route.

WHAT NEXT

Check the HDL code where the parameter LPM_TYPE is set on the cell. Make sure that the parameter value is same as the name of module which is being instantiated.

OPT-996 (warning) Always-on inverter characterized for '%s' operating condition was marked dont_use or it is not defined in target library.

DESCRIPTION

This warning message occurs when the target library does not contain an always-on inverter, or always-on inverter library cells are marked as dont_use, or dont_touch. When always-on strategy is dual rail, optimization needs to use an always-on inverter and always-on buffers on the always-on path. If those cells are missing or being marked as dont_touch or dont_use, and the always-on strategy is dual rail, the always-on path will be marked as dont_touch.

In addition, if the target library does not have always-on inverters or if they are marked as dont_touch or dont_use, and if the always-on strategy is dual rail, when retention hookup or isolation cell mapping needs to put the inverter on the retention or isolation control line to work with the control signal's sense value, those inverters will remain as normal inverters after optimization is done. The **check_mv_design** command will issue a warning on those cells. In this case, you should either use single rail strategy or add always-on inverters into the target_library.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this warning, add an always-on inverter to the target library. If an always-on inverter exists, then make sure it is not marked with a **dont_use** attribute.

SEE ALSO

check_mv_design(2)

OPT-997 (warning) Always-on buffer characterized for '%s' operating condition was marked dont_use or it is not defined in the target library.

DESCRIPTION

This warning message occurs when the target library does not contain an always-on inverter, or always-on inverter library cells are marked as dont_use, or dont_touch. When always-on strategy is dual rail, optimization needs to use an always-on inverter and always-on buffers on the always-on path. If those cells are missing or being marked as dont_touch or dont_use, and the always-on strategy is dual rail, the

always-on path will be marked as dont_touch.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this warning, add an always-on inverter to the target library. If an always-on inverter exists, then make sure it is not marked with a **dont_use** attribute.

OPT-998 (warning) Operating condition %s set on design %s has different process, voltage and temperatures parameters than the parameters at which target library

DESCRIPTION

When process, voltage and temperature parameters specified in design operating condition do not match parameters at which target library is characterized, the tool uses scaling to compute delays. Therefore delays may be inaccurate. This warning message informs about the resulting inaccuracies.

WHAT NEXT

Change either target libraries or operating condition.

SEE ALSO

set_operating_conditions(2)

OPT-1000 (error) Need to insert a pad on port '%s' before compiling.

DESCRIPTION

Pad optimization is done only on existing pads. The *insert_pad* command has to be used before *compile*, in order to add the IO pads to the design.

WHAT NEXT

Please use the *insert_pad* command and then *compile* again.

OPT-1001 (error) Multiple tristate buffers are driving pad net '%s'.

DESCRIPTION

Output pads can be added only to tristated lines driven by single tristate buffers. In this case, the pad will incorporate a single tristate buffer. When multiple tristate cells drive a single output port, it is not possible to use a single tristate in the output pad and still have an equivalent circuit. It is the responsibility of the user to resolve the problem by making sure a single tristate buffer drives the output port.

WHAT NEXT

Two customary transformations obtain a single tristate driver out of many: tristate merging, and tristate-ORing. Tristate merging replaces all tristates with inputs (data, enable) = (Di,Ei) by a single tristate buffer with inputs (data = D0*E0 + D1*E1 + ...) and (enable = E0 + E1 + ...).

Note that this transformation is valid only if the enable signals are disjoint (E0*E1*... = 0).

Tristate-ORing adds one more tristate whose data input is connected to the OR of all pre-existing tristates, and whose enable signal is E0 + E1 +...

Note that both transformations modify the logic behavior of the original circuit. They will not pass verification.

OPT-1002 (warning) Example pad '%s' is not in the library.

DESCRIPTION

The pad used as an example to specify the required attributes on the port is not available in the library. As a result, no constraints will be derived from the user-specified example pad.

WHAT NEXT

Please verify that the pad can be found in the library.

OPT-1003 (warning) Exact pad '%s' is not in the library.

DESCRIPTION

The exact pad specified as the cell to use on the port is not available. Therefore, pad selection will proceed with default cells selected from the library.

WHAT NEXT

Please verify that the pad can be found in the library.

OPT-1004 (warning) No matching pad found for port '%s';

DESCRIPTION

No IO pad having the right characteristics has been found to connect to the port. Therefore, no pad will be instantiated and connected to that port.

WHAT NEXT

The problem is probably due to over-constraining; that is, specifying too many IO pad constraints on the port.

OPT-1005 (warning) Relaxing user-specified IO pad constraints on port '%s'

DESCRIPTION

No matching pad was found for the port. Pad selection will now be done using only pads of the right direction (input/output/inout). All other constraints will be dropped.

WHAT NEXT

OPT-1006 (warning) Pad '%s' connected to port '%s' is dont-

touch. No optimization done.

DESCRIPTION

Pad connected to port is marked as *dont_touch*. No pad optimization will take place for that port. In order to either remove or optimize the IO pad connected to the port, the dont-touch attribute has to be removed.

WHAT NEXT

See command remove_attribute

OPT-1007 (information) Insert_pads interrupted. Saving intermediate design.

DESCRIPTION

A CONTROL-C interrupt was recieved by the *insert_pads* command. The design in its current state is being written back to the database. The design will reflect all of the pad insertion steps that have been performed so far.

WHAT NEXT

No action is required on your part.

OPT-1008 (error) Insert pads terminated abnormally.

DESCRIPTION

This error indicates that the *insert_pads* command terminated and did not write the intermediate design back to the database. Since the design was not written back to the database, the *current_design* is unchanged from before the insertion. The reason for the abnormal termination should have appeared in an error message prior to this one.

WHAT NEXT

Resolve errors and rerun *insert_pads*.

OPT-1009 (warning) Port '%s' has no net attached to it: no pad

inserted.

DESCRIPTION

The port is not connected to any net. It does not drive, or is not driven, by any core-logic gates. As a result, no pad is needed on that port.

WHAT NEXT

Verify that the port is supposed to be unconnected. If not, then connect the port to the correct core-logic gates in your design.

OPT-1010 (warning) Output port '%s' is not driven: no pad will be inserted.

DESCRIPTION

The output port is not driven by any core-logic cell. An output pad is not required and none will be connected to the particular port.

WHAT NEXT

Verify that the port is supposed to be unconnected. If not, then connect the port to the correct core-logic gates in your design.

OPT-1011 (warning) Target library has no pads in it. No pads inserted.

DESCRIPTION

There are no pad cells in the target library. The library needs to be updated with cells that have the *is_pad* attribute. Note that the pads should NOT have the *dont_use, dont_touch* attributes set. Otherwise, pad insertion and optimization will fail.

WHAT NEXT

Add a library with pads to the target_library.

OPT-1012 (warning) Design '%s' has no pad constraints. No

pad inserted.

DESCRIPTION

The current design on which command insert_pads is operating does not need any pads. Use the commands *set_port_is_pad* to indicate the ports that require pads. Optionally, use command *set_pad_type* to indicate the properties of the pads that are to be connected to the port (for example, voltage levels, current levels, presence of pull ups, etc).

WHAT NEXT

Use the command *set_port_is_pad*.

OPT-1013 (warning) Net '%s' is dont_touch (connected to port '%s'). No pad inserted.

DESCRIPTION

The port which the user marked as requiring an I/O pad is connected to a *dont_touch* net. This implies opposite requirements, since *dont_touch* nets cannot have new cells connected to them. In this case, the *dont_touch* attribute on the net is honored and no pad is inserted. If a pad is really needed, the dont_touch attribute should be removed from the net.

WHAT NEXT

See command remove_attribute

OPT-1014 (warning) I/O pad attribute mismatch on port '%s'

DESCRIPTION

The I/O pad(s) attached to the port does not have the same attributes as those set by the user on the corresponding port. This message appears during optimization, which will try to instantiate pads having characteristics closer to those requested on the port.

WHAT NEXT

OPT-1015 (warning) Connection class of port '%s' does not match that of any I/O pads.

DESCRIPTION

The connection class on the port is not compatible with any I/O pad classes. For that reason, no I/O pad will be instantiated, and the port will be left untouched.

WHAT NEXT

Check the connection classes of the I/O pad cells in the library. The port's class should match them. Use command *set_connection_class* to specify the connection classes of ports.

OPT-1016 (information) Remove_pads interrupted. Saving intermediate design.

DESCRIPTION

A CONTROL-C interrupt was received by the **remove_pads** command. The design in its current state is being written back to the database. The design will reflect all of the pad removal steps that had been performed so far.

WHAT NEXT

No action is required on your part.

OPT-1017 (error) Remove pads terminated abnormally.

DESCRIPTION

This error indicates that the **remove_pads** command terminated and did not write the intermediate design back to the database. Since the design was not written back to the database, the current_design is unchanged from before the removal. The reason for the abnormal termination should have appeared in an error message previous to this one.

WHAT NEXT

Resolve errors and rerun **remove_pads**.

OPT-1018 (warning) Pad already present on port '%s'. No new pad inserted.

DESCRIPTION

This warning indicates that the **insert_pads** command was used on a design where pads were already present. IO pads will only be added to ports which are not yet connected to pads. A warning will be issued to tell the user about ports which didn't require pads.

WHAT NEXT

No action is required on your part.

OPT-1019 (warning) Input port '%s' is not loaded: no pad will be inserted.

DESCRIPTION

The input port is not loaded by any core-logic cell. An input pad is not required and none will be connected to the particular port.

WHAT NEXT

Verify that the port is supposed to be unconnected. If not, then connect the port to the correct core-logic gates in your design.

OPT-1020 (warning) Inout port '%s' not driven by a tristate element. Assumed to be an output port.

DESCRIPTION

This warning indicates that the inout port is not recognized as a bidirectional port because no tristate gate is driving it. It is therefore considered an output port.

WHAT NEXT

Verify that the assumption made by Synopsys regarding the direction for the given port is correct. If the assumption is not correct, then modify the design so that the inout port is driven by a tristate element.

OPT-1021 (warning) Inout port '%s' assumed to be an input port.

DESCRIPTION

This warning indicates that the inout port is not recognized as a bidirectional port because no tristate gate is driving it. In addition, there is no gate that drives this port. It is therefore considered to be an input port.

WHAT NEXT

Verify that the assumption made by Synopsys regarding the direction for the given port is correct. If the assumption is not correct, then modify the design so that the inout port is driven by a tristate element.

OPT-1022 (warning) IO pad '%s' is unusable: unknown logic function.

DESCRIPTION

This warning indicates that the logic function associated with that IO pad is not known. As a result, it will not be considered during IO pad insertion and/or optimization.

WHAT NEXT

OPT-1023 (warning) IO Pad '%s' ('%s') has unknown logic function

DESCRIPTION

This pad has an unknown logic function, which will be ignored for pad optimization.

WHAT NEXT

OPT-1024 (error) Cannot insert a pad to drive bidirectional port '%s'

DESCRIPTION

The bidirectional port is driven by a tristate which is in a different level of hierarchy than the level of the load going back into the core logic. In that case, it is not possible to correctly instantiate a bidirectional IO pad in the circuit.

WHAT NEXT

There are two solutions to this problem. The first solution is to pull the tristate element and the load into the same level of hierarchy (typically, pulling the tristate element at the highest level will solve the problem). The second solution is to make the port an output port instead of an inout port. In that case, a simple buffer IO pad will be inserted at the highest level of hierarchy, driving the port directly. The second solution is valid only in cases where the port is not a true inout port (the port can never be driven from outside).

OPT-1025 (warning) Multiple drivers for net '%s'

DESCRIPTION

The net is driven by more than one gate. If this net is going to an output port, then a simple buffer IO pad will be instantiated. If the net is going to a bidirectional port which feeds back into the core logic, then no IO pad will be instantiated.

WHAT NEXT

For true bidircetional ports, the driving logic needs to be modified such that a single driver (a tristate) will appear on the net.

OPT-1026 (warning) Fixing %s introduces worse %s from %f to %f

DESCRIPTION

Design rules have different priorities. For example, by default, max_transition has

a higher priority than max_capacitance. To fix max_transition violations, max_capacitance could be sacrificed in some cases. The user could see more max_capacitance violations after max_transition fixing.

WHAT NEXT

One or a few more incremental runs of DRC fixing could probably resolve the newly generated low priority design rule violations. The user can also change the priority of design rules using command "set_cost_prioriry".

SEE ALSO

set_cost_prioriry (2)

OPT-1027 (warning) Has_builtin_pad attribute present on pin '%s' connected to to port '%s'. No pad inserted.

DESCRIPTION

This warning indicates that the port is connected to the pin with has_builtin_pad attributed on it. IO pads will only be added to ports which are not connected to pins attributed with has_builtin_pad. A warning will be issued to tell the user about ports which didn't require pads.

WHAT NEXT

No action required on your part.

OPT-1028 (error) Cannot insert pad at three-state port '%s' because
driver cell '%s' is dont_touch.

DESCRIPTION

The port is driven by an existing three-state cell that is marked as dont_touch. The dont_touch prevents inserting a three-state pad here because doing so would require replacing the dont_touch cell.

WHAT NEXT

Remove dont_touch from the three-state cell.

OPT-1030 (error) No appropriate operating condition found for level-shifter cell %s.

DESCRIPTION

When you characterize or the design is written out, for each level-shifter cell there must be a correct operating condition defined in its library. Most importantly is to have the rails defined with the correct voltage levels, master power supply and input pins voltage.

WHAT NEXT

Make sure you are using the correct library in the link list. Create additional operating conditions if necessary. Make sure the rail names and the corresponding input/output supply voltages match the level-shifter cell instance.

SEE ALSO

create_operating_condition(2),

OPT-1050 (warning) The wire logic is found on %s

DESCRIPTION

This message shows that mutiply drive net or wire logic net is found in netlist. It might be ignored for optimization.

WHAT_NEXT

If the wire logic is not desired, modify your netlist to remove WIRE logic.

OPT-1051 (Error) Cannot optimize wire logic net.

DESCRIPTION

You receive this error message when you issue the **reoptimize_design** command and the tool encounters wire logic net in the netlist. Wire logic is not available in this release of the software.

WHAT NEXT

Modify your netlist to remove wire logic, or run the **compile** command with the **-**

incremental option to remove it.

SEE ALSO

compile (2), **reoptimize_design** (2).

OPT-1052 (warning) Cannot set global buffer on output port '%s'.

DESCRIPTION

This warning is displayed when user tries to set global buffer on output port. Global buffer can not be set on the output port.

WHAT NEXT

OPT-1053 (information) Simplify constants interrupted. Saving intermediate design.

DESCRIPTION

A CONTROL-C interrupt was recieved by the *simplify_constants* command. The design in its current state is being written back to the database.

WHAT NEXT

No action is required on your part.

OPT-1054 (error) Simplify constants terminated abnormally.

DESCRIPTION

This error indicates that the *simplify_constants* command terminated and did not write the intermediate design back to the database. Since the design was not written back to the database, the *current_design* is unchanged from before the insertion. The reason for the abnormal termination should have appeared in an error message prior to this one.

WHAT NEXT

Resolve errors and rerun *simplify_constants*.

OPT-1055 (information) Removing unused design '%s'.

DESCRIPTION

The design is removed because it is no longer referred in the netlist. This usually happens in **ungroup** or **compile**.

WHAT NEXT

If you want to keep the design, set **ungroup_keep_original_design** to true in your script.

OPT-1100 (information) Balance_buffer interrupted. Saving intermediate design.

DESCRIPTION

A CONTROL-C interrupt was received by the **balance_buffer** command. The design in its current state is being written back to the database. The design will reflect all of the buffering steps that had been performed so far.

WHAT NEXT

No action is required on your part.

OPT-1101 (error) Balance_buffer terminated abnormally.

DESCRIPTION

This error indicates that the **balance_buffer** command terminated and did not write the intermediate design back to the database. Because the design was not written back to the database, **current_design** is unchanged. The explanation for the abnormal termination should have appeared in an error message previous to this one.

WHAT NEXT

Resolve errors and rerun **balance_buffer**.

OPT-1102 (warning) Cannot find %s '%s'

DESCRIPTION

This error indicates that the object passed as a parameter does not have the expected type. That situation can happen when two objects with different types have the same name. A typical example is a port and a net connected to it, which often have the same name.

WHAT NEXT

Use the find() command to specify the right object.

OPT-1103 (warning) Pin (or port) '%s' has no net attached to it.

DESCRIPTION

This warning indicates that the pin (or port) passed as a parameter is not connected to any net. Therefore, that pin will not be considered by the **balance_buffer** command.

WHAT NEXT

Include only pins (or ports) that are connected to nets, or use the **-net** option to specify the desired nets.

OPT-1104 (information) A memory leak has been detected (%s).

DESCRIPTION

This message indicates that Design Compiler has detected a memory leak. It is an internal message which is important for Synopsys, but which has little importance for the customer.

The accompanying (OPT-103) message which immediately follows this is used internally to signal to us when this situation occurs in any of our regression tests (so we can check it out). It can be ignored.

WHAT NEXT

Supply a testcase to Synopsys illustrating this problem so it can be fixed.

OPT-1155 (information) Unbinding all unconnected pin(s) in the design, which was set to ignore binding by the 'ignore_binding_open_pins' variable.

DESCRIPTION

This information message advises you that you have set all open pins to be ignored by binding to a constant pin.

WHAT NEXT

This is an information message only. No action is required.

OPT-1156 (information) Unbinding the '%s' unconnected pin, which was set to ignore binding by the 'ignore_binding_open_pins' variable.

DESCRIPTION

This information message advises you that you have set the specified open pin to be ignored by binding to a constant pin.

WHAT NEXT

This is an information message only. No action is required.

OPT-1157 (Information) Not binding the unconnected PG pin '%s'.

DESCRIPTION

This information message advises you that the tool is not binding the specified PG pin to any constant pin and the PG pin will be left unconnected.

WHAT NEXT

This is an information message only. To remove this message, connect the specified PG pin correctly in the netlist.

OPT-1200 (warning) Library cell '%s' has INOUT port(s). Not considered for sequential mapping.

DESCRIPTION

The library cell has an inout port, which will be ignored by the sequential mapping step.

WHAT NEXT

OPT-1201 (warning) Library cell '%s' could not be modeled for sequential mapping.

DESCRIPTION

The library cell has a complex functionality that could not be modeled for sequential mapping. So this cell will be ignored for sequential mapping.

WHAT NEXT

OPT-1202 (warning) Library cell '%s' has unknown behavior

DESCRIPTION

The library cell has a complex functionality that could not be modeled for sequential mapping. So this cell will be ignored for sequential mapping.

WHAT NEXT

OPT-1203 (warning) Combinational loop detected at '%s' during sequential mapping

DESCRIPTION

A combinational feedback loop was detected during sequential mapping. None of the cells in this loop will be considered during the sequential mapping operation.

WHAT NEXT

OPT-1204 (warning) The cell '%s' will not be considered for sequential optimization.

DESCRIPTION

The cell '%s' has an output pin that feeds back (through some levels of logic) into its clock pin. This is an illegal configuration. Using such configurations may result in inaccurate timing information.

WHAT NEXT

Modify the specification such that the forementioned feedback is absent.

OPT-1205 (warning) The register '%s' may not be optimally implemented because of a lack of compatible components with correct clock/enable phase.

DESCRIPTION

The initial sequential mapping step tries to match the desired register clock phase exactly. When this matching fails due to a difference in clock phase, the mapper will attempt to avoid building a register with an incorrect clock/enable phase. When that happens, this warning is issued.

WHAT NEXT

If you want compile to initially build a register with the opposite clock/enable phase, then you can use the variable **compile_automatic_clock_phase_inference** to alter the way that mapping operates. Setting this variable to "none" will instruct the initial sequential mapping to ignore clock phase entirely during this process, thus allowing the mapper to consider registers with both positive and negative clock/enable phase as needed. Setting this variable to "relaxed" will instruct sequential mapping to only try the opposite phase device if there is no other way to implement the register with the automatically inferred phase. And, setting the variable to "strict" (the default setting) will instruct the initial sequential mapping to reject all candidate components whose clock/enable phase does not match the automatically inferred phase.

OPT-1206 (information) The register '%s' is a constant and will

be removed.

DESCRIPTION

When constant propagation is enabled, the sequential mapping step will remove any detected constant register. When that happens, this information is issued.

Removal of constant regsiters is controlled by two variables: compile_seqmap_propagate_constants and compile_seqmap_propagate_high_effort, both of which are "true" by default.

WHAT NEXT

SEE ALSO

compile_seqmap_propagate_constants (3), **compile_seqmap_propagate_high_effort** (3).

OPT-1207 (information) The register '%s' will be removed.

DESCRIPTION

The register has been identified during optimization to be redundant. This could be due to optimizations like constant propagation, or the register being found to be unloaded.

WHAT NEXT

OPT-1208 (information) Sequential output inversion is enabled. SVF file must be used for formal verification.

DESCRIPTION

This message indicates that sequential output inversion is enabled for this invocation of the compile or compile_ultra command. When sequential elements are inverted, Formality will not be able to verify the design unless the SVF file is used. To disable sequential output inversion for the **compile** command, set the variable **compile_seqmap_enable_output_inversion** to "false". To disable sequential output inversion for the **compile_ultra** command, use the **-no_seq_output_inversion** option to that command.

SEE ALSO

compile_seqmap_enable_output_inversion (3)

OPT-1209 (warning) The nextstate or clock_on object of the test_cell definition of the library cell '%s' has scan pins.

DESCRIPTION

The nextstate or clock_on object of the test_cell definition of the library cell '%s' has scan pins.

WHAT NEXT

OPT-1210 (information) Retiming is enabled. SVF file must be used for formal verification.

DESCRIPTION

This message indicates that retiming is enabled for this invocation of the compile_ultra command. If sequential cells are move across combinational cells, Formality will not be able to verify the design unless the SVF file is used. To disable retiming for the **compile_ultra** command, do not use the **-retime** option to that command and do not use the optimize_registers or balance_registers attributes.

WHAT NEXT

SEE ALSO

compile_ultra (2) **set_optimize_registers** (2) **set_balance_registers** (2)

OPT-1211 (warning) The DW sequential cell '%s' can not be mapped to the preferred library cells.

DESCRIPTION

You set 'synlib_preferred_ffs' variable. But this DW sequential cell in a DW FF chain can not be mapped to the preferred library cell. This might be due to the fact that the functionality of the preferred library cell does not match that of the DW

sequential cell; or you may have set 'dont_use' attribute on the preferred library cell.

SEE ALSO

OPT-1212 (warning) The DW synchronizer FF chain starting from '%s' can not be mapped to the preferred FF chain library cells.

DESCRIPTION

You set 'synlib_preferred_ff_chains' variable. But this DW sequential cells in a DW FF chain can not be mapped to the preferred FF chain library cell. This might be due to the fact that the functionality of the preferred FF chain library cell does not match that of the DW FF chain; or you may have set 'dont_use' attribute on the preferred FF chain ibrary cell.

SEE ALSO

OPT-1213 (information) Register '%s' stores a value equal or opposite to register '%s', and will be removed.

DESCRIPTION

When sequential constant propagation is enabled, the sequential mapping step may remove registers that can be shown to be always equal or opposite to another register in the design. The OPT-1213 message reports registers that are removed from the design for this reason.

Removal of constant regsiters is controlled by two variables: compile_seqmap_propagate_constants and compile_seqmap_propagate_high_effort, both of which are "true" by default.

WHAT NEXT

SEE ALSO

compile_seqmap_propagate_constants (3), **compile_seqmap_propagate_high_effort** (3).

OPT-1215 (information) In design '%s', the register '%s' is

removed because it is merged to ’%s’.

DESCRIPTION

When register merging is enabled, compile state reachability will detect the set of equivalent registers and merge them. When that happens, this information is issued.

WHAT NEXT

SEE ALSO

set_register_merging (2).

OPT-1216 (Warning) Sequential mapping has discovered reconvergent clock/data inputs on register ’%s’ in design ’%s’. Simulation/synthesis mismatches could occur.

DESCRIPTION

Sequential mapping has discovered that the clock pin of a register appears in the "next-state" function of that register. When this happens, sequential mapping assumes that the clock signal will be logic 0 for a rising edge clock, or logic 1 for a falling edge clock.

For example, this error will occur in situations like the following:

```
assign next_q = clk | data;

always @(posedge clk)
  q <= next_q;
```

In this case, Design Compiler will assume that clk is logic 0 (because it is a rising edge clock). Accordingly, Design Compiler will produce the folllowing mapping for q_reg:

```
FD1 q_reg (.D(data), .CP(clk), .Q(q));
```

Note that Design Compiler is not guaranteed to detect this situation. It will only be detected if the reconvergence occurs entirely within the logic considered by sequential mapping (a few logic levels from the register being mapped).

WHAT NEXT

OPT-1240 (error) Failed to uniquify the design. Use the uniquify -dont_skip_empty_designs command to fix designs instantiated multiple times.

DESCRIPTION

You receive this error message because you executed the **remove_unconnected_ports** command and specified a design that has subdesigns instantiated multiple times. The command will not accept designs that have subdesigns instantiated multiple times, even if the subdesigns are empty, because this might cause some designs to be inconsistent.

WHAT NEXT

First, force all the subdesigns, including empty subdesigns, to be uniquified using the **uniquify -dont_skip_empty_designs** command. Then, reexecute the **remove_unconnected_ports** command.

SEE ALSO

remove_unconnected_ports (2), **uniquify** (2).

OPT-1241 (warning) The remove_unconnected_ports command skipped the following cells: %s.

DESCRIPTION

This warning message occurs when you execute the **remove_unconnected_ports** command and specify a cell that instantiates a subdesign that is multiply instantiated.

The command does not remove any unconnected port from the multiply instantiated subdesign because it may cause some designs to be inconsistent.

WHAT NEXT

This is a warning message only. No action is required.

However, if you do not want the cells to be skipped, use the **uniquify -dont_skip_empty_designs** command to force all of the subdesigns (including empty subdesigns) to be uniquified. Reexecute the **remove_unconnected_ports** command.

SEE ALSO

remove_unconnected_ports(2)
uniquify(2)

OPT-1242 (Warning) IOB register inference step is skipped because %s is not a valid value for fpga_iob_mapping.

DESCRIPTION

Allowed values for the **fpga_iob_mapping** variable are *all*, *none*, and *default*. When *all* is the value, compile tries to infer IOB registers for all ports with *port_is_pad* attribute. It ignores those ports for which IOB register inference is disabled using the command *set_fpga_iob_register*.

When *none* (the default value) is the value, then no IOB register inference is done.

When *default* is the value, compile tries to infer IOB registers for only those ports for which IOB register inference is enabled using the command *set_fpga_iob_register*.

To determine the current value of this variable, type **list fpga_iob_mapping**.

WHAT NEXT

Set **fpga_iob_mapping** to one of the values *all*, *default*, or *none*.

SEE ALSO

compile (2), **set_port_is_pad** (2), **set_fpga_iob_register** (2), **fpga_iob_mapping** (3).

OPT-1300 (warning) Location based buffer insertion disabled.

DESCRIPTION

The PDEF file read for the current design contained locations for the leaf cells. This typically enables location based optimization (buffer insertion and removal) to take place. In this case however, location based buffer insertion was not activated because it was explicitly disabled either by setting "compile_ok_to_buffer_during_inplace_opt" or "lbo_buffer_insertion_enabled" to FALSE.

WHAT NEXT

To enable location based buffer insertion, make sure that the above variables are set to true in the setup file.

OPT-1301 (warning) Location based buffer removal disabled.

DESCRIPTION

The PDEF file read for the current design contained locations for the leaf cells. This typically enables location based optimization (buffer insertion and removal) to take place. In this case however, location based buffer removal was not activated because it was explicitly disabled by setting "lbo_buffer_removal_enabled" to FALSE.

WHAT NEXT

To enable location based buffer removal, make sure that the previously stated variables are set to true in the setup file.

OPT-1302 (warning) The simple_compile_mode variable is obsolete. Setting this variable now defaults to compile -map_effort medium. Please update your script accordingly.

DESCRIPTION

Setting this variable now defaults to compile -map_effort medium.

WHAT NEXT

Please update your script accordingly.

OPT-1303 (warning) The compile -map_effort low is obsolete. Setting this variable now defaults to compile -map_effort medium. Please update your script accordingly.

DESCRIPTION

Setting this variable now defaults to compile -map_effort medium.

WHAT NEXT

Please update your script accordingly.

OPT-1304 (error) Using compile -top with unmapped logic

DESCRIPTION

This message indicates that some part of the design is not mapped.

WHAT NEXT

Resolve errors and rerun optimization.

OPT-1305 (error) The %s%s is obsolete in 2005.09 release. Please use Formality instead and update your script accordingly.

DESCRIPTION

Old verification code inside Design Compiler will no longer be supported, starting with the major release in 2005.09. Instead please use stand-alone Formality to verify your design.

WHAT NEXT

Please update your script accordingly.

OPT-1306 (warning) The %s%s will be obsolete in the next major release.

DESCRIPTION

Pad mapping code inside DesignCompiler will no longer be supported, starting with the next major release.

WHAT NEXT

Please update your script accordingly.

OPT-1307 (warning) Setting dont_use on dont_touched lib_cell

’%s’/’%s’.

DESCRIPTION

Design Compiler will mark all dont_touched libcells in the given libraries as also being dont_use.

WHAT NEXT

OPT-1308 (error) The %s%s is now obsolete.

DESCRIPTION

Pad mapping code inside DesignCompiler will no longer be supported, starting with the next major release.

WHAT NEXT

Please update your script accordingly.

OPT-1309 (warning) The -no_auto_ungroup switch with compile_ultra will be obsolete in the next major release. Please use -no_autoungroup instead.

DESCRIPTION

compile_ultra -no_auto_ungroup is being phased out. Please use compile_ultra -no_autoungroup instead.

WHAT NEXT

Please update your script accordingly.

OPT-1310 (Information) No valid alib found for target library.

Proceeding with library analysis.

DESCRIPTION

The tool could not find a usable alib for one of the target libraries. Therefore the target libraries were analyzed. Given a target library file named 'x.db', the tool searches for an alib file named 'x.db.alib'. Two directories are searched: (1) the directory specified by the environment variable **alib_library_analysis_path**, and (2) the directory specified by the environment variable **alib_library_analysis_cache**. If the alib exists but is unusable, either the file-system modification date of the target library has changed since the alib was created, or the alib was created with a different version of the tool.

WHAT NEXT

To avoid library analysis at compile time, use the command **alib_analyze_libs** to generate alibs for your target libraries. For example:

```
set target_library "x.db y.db"
set alib_library_analysis_path "./"
alib_analyze_libs
```

OPT-1311 (Warning) Only placeholder alibs were found. Proceeding with library analysis.

DESCRIPTION

A placeholder alib represents a target library that is not complete or a target library that has not yet been fully analyzed.

A target library is complete if and only if both (1) it contains all of the following: logic zero, logic one, a buffer, an inverter; and (2) it contains one of the following: and2, or2, nand2, nor2.

One or more of the target libraries must have a corresponding non-placeholder alib. Otherwise, library analysis occurs.

WHAT NEXT

Use the **alib_analyze_libs** command to create alibs for your target libraries. Refer to the **OPT-1310** manpage for more information.

OPT-1312 (error) No target library found.

DESCRIPTION

The target_library is empty or the libraries contained in it are not found.

WHAT NEXT

Add valid libraries to target_library.

OPT-1313 (error) The alib file '%s' is not writable.

DESCRIPTION

The alib file in this message could not be written to disk. This could be because the user ran out of disk space, or because the user has no write privileges for the alib file directory.

WHAT NEXT

Check if there is enough disk space left on your device. Check for write permission on the alib file directory specified in *alib_library_analysis_path*.

SEE ALSO

alib_library_analysis_path.

OPT-1314 (Warning) The target_library cells '%s' will be ignored for mapping as the timing arcs mismatch with the logically equivalent cell '%s'.

DESCRIPTION

You receive this message because the timing arcs in the cells listed are not matching even though all the cells implement the same logic.

WHAT NEXT

Make sure that the cells in the library have acurate timing arcs.

OPT-1350 (warning) Using user selected most dominant scenario '%s', although '%s' might be a better choice.

DESCRIPTION

This message is issued because user has selected a dominant scenario that may not be the best one, although user's selection is still used.

WHAT NEXT

Check if variable dominant_scenario needs to be set to a better scenario.

OPT-1351 (warning) Ignoring preferred scenario '%s' because it %s.

DESCRIPTION

This message is issued because user has selected a preferred scenario that either does not exist or is not activated.

WHAT NEXT

Check the name of the scenario or make sure it exists and is active.

OPT-1401 (error) This design was created using DC Topographical technology. Command '%s' can not be used on this design.

DESCRIPTION

This message indicates that the current design was created using DC Topographical technology. The command indicated in the error message is not supported in the DC Topographical flow.

WHAT NEXT

OPT-1402 (error) This design was created using DC

Topographical technology. Please use the -incremental switch.

DESCRIPTION

This message indicates that the current design was created using DC Topographical technology. The DC Topographical flow requires that compile_ultra will be run with the -incremental switch.

WHAT NEXT

OPT-1403 (warning) Removing previous data generated by DC Topographical technology.

DESCRIPTION

This message indicates that all topographical data created previously using DC Topographical technology is being removed since **compile_ultra** non-incremental mode or incremental mode with clock-gating has been called. This may result in design qor convergence issues.

WHAT NEXT

If you want to use previous generated data use 'compile_ultra -incremental'. Also, use '-gate_clock' option in the non-incremental compile_ultra rather than the incremental one.

OPT-1404 (warning) Found %d percent of cells (%d) without DC Topographical data. Generating data for those cells...

DESCRIPTION

This message indicates that the current design contain cells that were not created using DC Topographical technology. DC Topographical will try to generate data for those cells.

WHAT NEXT

OPT-1405 (error) DC Topographical Failed to place the design.

DESCRIPTION

This message indicates that DC Topographical technology could not place the design. No physically aware optimizations will be performed.

WHAT NEXT

OPT-1406 (error) Command %s is not supported in DC Topographical mode.

DESCRIPTION

This message indicates that the command you are trying to run is not supported in DC Topographical mode.

WHAT NEXT

Revise your script to avoid running the indicated command.

OPT-1407 (warning) Variable %s is not supported in DC Topographical mode and will be ignored.

DESCRIPTION

This message indicates that the variable you are trying to set is disabled in DC Topographical mode. The value of the variable will be ignored while running in Topographical mode.

WHAT NEXT

Revise your script to avoid using the indicated variable.

OPT-1408 (error) Failed to generate DC Topographical data.

DESCRIPTION

This message indicates that DC Topographical technology encountered errors while trying to generate the physical data it requires. The command that is being executed will be aborted.

WHAT NEXT

Check the run log for clues regarding the reasons for this error.

OPT-1409 (error) DC Topographical failed to find physical data for design %s.

DESCRIPTION

This message indicates that DC Topographical technology failed to locate the physical data it requires for the specified design. The command that is being executed will be aborted.

WHAT NEXT

Check the run log for clues regarding the reasons for this error.

OPT-1410 (error) DC Topographical design already exists.

DESCRIPTION

This message indicates that DC Topographical design already exists for a different top level design. DC Topographical technology supports only one top level design in memory.

WHAT NEXT

Modify your scripts to save and remove any previous designs.

OPT-1411 (Warning) Design %s contains the following

unmapped cells: %s.

DESCRIPTION

The design contains unmapped logic after compile_ultra mapping stage. DC Topographical technology requires that all cells will be mapped in the Topographical stage. This problem may have been caused by setting **dont_touch** attribute on a generic (unmapped) cell. This error may also be caused by running **compile_ultra -incremental** on a design which contain unmapped cells.

WHAT NEXT

Check the design to ensure that no unmapped cells have a dont_touch attribute.

OPT-1412 (Info) Ignoring the %s switch. It is no longer required for '%s' in topographical mode.

DESCRIPTION

The indicated switch is no longer required for the command in DC Topographical mode. Since the switch no longer has any functionality it is being ignored. This switch may be removed in future releases.

WHAT NEXT

Remove the switch to avoid problems in future releases.

OPT-1413 (Warning) Created physical library cell for logical library cell %s.

DESCRIPTION

DC Topographical technology requires that all logical library cells have corresponding physical library cells. If a physical library cell for a logical library cell is missing, DC Topographical technology creates one by default.

WHAT NEXT

Check the logical and physical libraries to make sure they match.

OPT-1414 (Warning) DC Topographical detected significant design changes.
DC Topographical data will be reset.

DESCRIPTION

DC Topographical technology detected significant design change since the last compile was run. DC Topographical data will be regenerated for all the design. This may cause qor convergence issues. This problem is usually caused by a significant increase in design area that makes previous data invalid.

WHAT NEXT

Check the run log to understand the reasons for the design area increase.

OPT-1415 (Information) Voltage area %s will be created during compile.

DESCRIPTION

DC Topographical technology delays the creation of voltage area after netlist is mapped during compile. The delay is necessary to ensure the voltage area has correct cells and utilization.

OPT-1416 (Error) Failed to create voltage area %s.

DESCRIPTION

DC Topographical technology fails to create voltage area due of various reasons. The reasons should already be listed. Please check respective error messages for more informaiton.

WHAT NEXT

Modify command according to more specific error messages issued during voltage area creation.

OPT-1417 (Error) Failed to create voltage area %s on MW

design.

DESCRIPTION

DC Topographical technology fails to create voltage area on the MW design.

OPT-1418 (Information) Removed voltage area with name %s.

DESCRIPTION

The voltage area with the name is removed from the design.

OPT-1419 (Error) Specified voltage area does not exist in the design.

DESCRIPTION

The voltage area specified does not exist in the design. Please check voltage area name or object name in your command.

OPT-1420 (Error) There is no voltage area in the design

DESCRIPTION

When there is no voltage area specified in the design, report and remove voltage area command fails.

OPT-1421 (Error) Cell object %s doesn’t have voltage area defined

DESCRIPTION

There is no voltage area defined on this object. Please check your report_voltage_area or remove_voltage_area command to see whether the cell name is specified correctly. Please use report_voltage_area -all to see voltage area name and cell object for each voltage area.

SEE ALSO

report_voltage_area(2)
remove_voltage_area(2)

OPT-1422 (Warning) Sub-block '%s' was not created using DC Topographical technology.

DESCRIPTION

DC Topographical detected a Hierarchy in the top-level design that does not contain DC Topographical data. For best results when using 'compile_ultra -top' in Topographical mode all sub-modules of the design should be compiled using DC Topographical technology.

WHAT NEXT

If possible, compile the sub-module using DC topographical technology.

OPT-1423 (Warning) User physical constraints set in DC-Topograpical will be lost in non-topographical DC_SHELL.

DESCRIPTION

The DDC reader prints this message if the file being read into non-topo DC_SHELL contains any DCT user physical constraints. The physical constraints saved in DDC will not be restored in the current non-topo DC_SHELL.

WHAT NEXT

This is a warning. Please make sure your want to read a DCT DDC with physical constraints into non-topo DC_SHELL and lose all the user physical constraints.

OPT-1424 (Error) Design %s has no placeable technology leaf cells.

DESCRIPTION

DC failed to generate the Topographical data because the design does not have any placeable technology leaf cells.

OPT-1425 (warning) Cannot run compile_ultra in DC Topographical mode when variable '%s' is set.

DESCRIPTION

The indicated variable is not supported in DC Topographical mode. **compile_ultra** in DC Topographical mode cannot run correctly when this variable is set. The variable will automatically be reset.

EXAMPLE MESSAGE

```
Warning: Cannot run compile_ultra in DC Topographical mode when variable
'physopt_optimize_placement' is set. (OPT-1425)
```

OPT-1426 (Warning) Ignoring the %s option. Option is no longer supported for compile_ultra.

DESCRIPTION

The indicated command line option is no longer supported for compile_ultra in DC Topographical mode. The option is being ignored. This option may be removed in future releases.

WHAT NEXT

Remove the option to avoid problems in future releases.

OPT-1427 (warning) Not all metal layers have preferred routing direction.

DESCRIPTION

This error message occurs when not all metal layers have preferred routing direction set for them. The preferred routing direction of a metal layer is the library defined preferred routing direction unless a user defined library direction is explicitly set in the design.

WHAT NEXT

This is only a warning message. Use set_preferred_routing_direction command to set a user defined direction for a layer in the design. To remove a user defined direction and revert back to using the library defined direction, use remove_preferred_routing_direction command. To identify which layer does not have preferred routing direction, use report_preferred_routing_direction command.

SEE ALSO

set_preferred_routing_direction(2)
remove_preferred_routing_direction
report_preferred_routing_direction

OPT-1428 (error) DC-Topographical Failed to link physical library.

DESCRIPTION

You receive this error message because you have not read in a physical library before you ran one of these commands: **compile_ultra**, **extract_physical_constraints**, **set_ignored_layers**, or **report_ignored_layers**.

WHAT_NEXT

Check your setup to make sure the physical library is correct and is set properly. Also check that the search path is correctly stated in the **search_path** variable. Then invoke the command again.

SEE ALSO

compile_ultra (2), **extract_physical_constraints** (2), **report_ignored_layers** (2), **set_ignored_layers** (2), **search_path** (3).

OPT-1429 (error) TLU+ sanity check failed.

DESCRIPTION

You receive this error message because TLU+ sanity check have failed during the **compile_ultra** command.

WHAT_NEXT

Check your setup to make sure the TLU+ setting is correct and is set properly. Then

invoke the command again.

SEE ALSO

compile_ultra (2).

OPT-1430 (error) Routing layers sanity check failed.

DESCRIPTION

You receive this error message because the routing layers data is incomplete. The **compile_ultra** command cannot run properly in DC-Topographical mode without the missing data. The following data is required for every routing layer: width, direction, pitch, resistance and capacitance. Look for preceding errors to indicate which of the above is missing.

WHAT_NEXT

Check your setup to make sure the routing layers data is correct and is set properly. Then invoke the command again.

SEE ALSO

compile_ultra (2), **set_tlu_plus_files** (2), **set_preferred_routing_direction** (2).

OPT-1431 (warning) Instantiated cell '%s' (Reference: '%s/%s') does not have a corresponding physical library cell.

DESCRIPTION

This warning message occurs because Design Compiler topographical technology requires that all instantiated cells have corresponding physical library cells. If a physical library cell for an instantiated cell is missing, Design Compiler topographical creates one by default.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, make sure every instantiated cell has a corresponding physical library cell, and run the command again.

OPT-1432 (warning) Total of %d instantiated cells without corresponding physical library cells are found. Run '-check_only' with 'compile_ultra' to see more details.

DESCRIPTION

This warning message occurs because Design Compiler topographical technology requires that all instantiated cells have corresponding physical library cells. If a physical library cell for an instantiated cell is missing, Design Compiler topographical creates one by default.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, make sure every instantiated cell has corresponding physical library cells, and run the command again.

SEE ALSO

compile_ultra(2)

OPT-1433 (warning) Multiple technology library cells with the same name '%s' are found in the following libraries: %s

DESCRIPTION

This warning message occurs when there are multiple technology library cells with same name in the target and/or link libraries. It is considered best practice to for Design Compiler topography to use technology library cells with unique names.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, make sure every technology library cell's name is unique, and run the command again.

OPT-1434 (warning) Total of %d technology library cells with the

same names are found. Run '-check_only' with 'compile_ultra' to see more details.

DESCRIPTION

This warning message occurs when there are multiple technology library cells with same names in the target and/or link libraries. It is considered best practice for Design Compiler topography to use technology library cells with unique names.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, make sure every technology library cell's name is unique, and run the command again.

SEE ALSO

compile_ultra(2)

OPT-1435 (error) Design %s has invalid ILM or physical hierarchy and cannot proceed with compile.

DESCRIPTION

This error message occurs when the design has Design Compiler ILM or non-Design Compiler topographical physical hierarchy. For the Design Compiler topographical hierarchical flow to run, all ILMs must be created on a placed IC Compiler netlist in IC Compiler, or on a Design Compiler topographical placed netlist in Design Compiler topographical. All Design Compiler topographical physical hierarchies must be Design Compiler topographical pre-placed.

WHAT NEXT

Make sure that the input hierarchies are valid, and run the command again.

OPT-1436 (Error) Design was not created using DC Topographical technology.
Command 'report_congestion' can not be run without DC

Topographical data.

DESCRIPTION

DC Topographical detected the design does not contain DC Topographical data. 1report_congestion’ requires the design to be compiled using DC Topographical in order to run correctly.

WHAT NEXT

To use ’report_congestion’, compile the design using DC topographical technology.

OPT-1437 (Error) Compile with multiple scenarios can only be used in DC Topographical mode.

DESCRIPTION

Compile detected that there are multiple scenarios in your design and this feature can only be used in DC Topographical mode.

WHAT NEXT

Compile the design in DC Topographical mode.

OPT-1438 (Error) Command ’%s’ does not work with active scenarios.

DESCRIPTION

The tool detected active scenarios in your design and this command in not compatible with active scenarios.

WHAT NEXT

OPT-1439 (error) TLU+ file not set for scenarios ’%s’.

DESCRIPTION

You receive this error message because there is no TLU+ file set for the scenario.

compile_ultra command requires TLU+ file to be set for all the active scenarios.

WHAT_NEXT

Please specifiy the TLU+ file for every scenario using **set_tlu_plus_files** command before running **compile_ultra**.

SEE ALSO

compile_ultra (2). **set_tlu_plus_files**

OPT-1441 (warning) The ILM/physical block %s(%s) has dont_touch attribute set to FALSE. It will be affected by optimization.

DESCRIPTION

This warning message occurs when there are ILMs or physical blocks with the **dont_touch** attribute set to FALSE on their reference designs. This will cause optimization to modify the instances.

WHAT NEXT

Make sure that the reference designs have the **dont_touch** attribute set to TRUE. Remove any **dont_touch** attributes on the instances.

SEE ALSO

compile_ultra(2)

OPT-1442 (error) Total of %d cells do not have locations in the ILM or physical block (%s). Run '-check_only' with 'compile_ultra' to see more details.

DESCRIPTION

This error message occurs when there are cells in the ILM or physical block that do not have locations. Compile cannot propagate locations if the locations are not specified.

WHAT NEXT

Ensure that the ILM or physical block has valid cell locations, and run the command again.

SEE ALSO

compile_ultra(2)

OPT-1443 (error) Total of %d ports do not have locations in the ILM or physical block (%s). Run '-check_only' with 'compile_ultra' to see more details.

DESCRIPTION

This warning message occurs when there are ports in the ILM or physical block that do not have locations.

WHAT NEXT

Ensure that the ILM or physical block has valid port locations and run the command again.

SEE ALSO

compile_ultra(2)

OPT-1500 (information) Running optimization using a maximum of %d cores.

DESCRIPTION

This information messages advises you that the tool is running in multicore mode. You can specify the maximum number of CPU cores to be used with the **set_max_cores** command.

WHAT NEXT

This is an information message only. No action is required.

SEE ALSO

compile_ultra(2)
set_max_cores(2)

OPT-1501 (error) Unable to start messaging for parallel execution on host %s.

DESCRIPTION

This error message occurs when tool is unable to set up the messaging infrastructure for the interprocess communication required to start parallel execution. This failure occurs when there is a system problem.

WHAT NEXT

If the problem is repeatable, it is likely that there is a problem with the current system. Try running the tool on a different host.

SEE ALSO

compile_ultra(2)
set_max_cores(2)

OPT-1502 (warning) The -num_cpus option is obsolete and will be removed in the next release. Please use 'set_host_options -max_cores' instead.

DESCRIPTION

This message indicates that you have used the *-num_cpus* option to the **compile_ultra** command. This option is obsolete. Please use the **set_host_options** -fI-max_cores command instead.

WHAT NEXT

Run **set_host_options** *-max_cores* before running **compile_ultra**, and remove the *-num_cpus* option from the **compile_ultra** command.

SEE ALSO

set_host_options(2)
compile_ultra(2)

OPT-1503 (error) The -num_cpus option (%d) conflicts with the value set with 'set_host_options -max_cores' (%d). The -num_cpus option will be removed in a future release. Please use 'set_host_options -max_cores' only.

DESCRIPTION

This error message occurs when you use the **-num_cpus** option is to the **compile_ultra** command, and the value provided is different than the value that was set with the **set_host_options -max_cores** command. The command cannot proceed. The **-num_cpus** option is obsolete. Use only the **set_host_options -max_cores** command to set the number of processor cores to use for parallel execution.

WHAT NEXT

Run **set_host_options -max_cores** before running **compile_ultra**, and remove the **-num_cpus** option from the **compile_ultra** command.

SEE ALSO

compile_ultra(2)
set_host_options(2)

OPT-1600 (information) Checkpoint design written: %s. Checkpoint designs are for analysis purposes only. Optimization commands cannot be run on a checkpoint design.

DESCRIPTION

This information tells the user that the checkpoint design written out by optimization is to be used for analysis purposes only (eg. timing analysis). The user will not be able to run optimization commands on the checkpoint design.

SEE ALSO

set_checkpoint_strategy(2) report_checkpoint_strategy(2)
remove_checkpoint_designs(2)

OPT-1601 (error) The options are not compatible.

DESCRIPTION

This error indicates to the user that the options used by the user are not compatible and the command did not succeed. Please provide compatible options.

WHAT NEXT

Refer to man page of the command and provide compatible options.

SEE ALSO

set_checkpoint_strategy(2) report_checkpoint_strategy(2) remove_checkpoint_designs(2)

OPT-1602 (error) Failed to save checkpoint design

DESCRIPTION

This error indicates to the user that an error occurred while optimization was trying to save a checkpoint design. Possible causes include insufficient disk space, error in filesystem access, etc.

WHAT NEXT

Check to see that there is enough disk space for saving checkpoint design or that filesystem access is working.

SEE ALSO

set_checkpoint_strategy(2) report_checkpoint_strategy(2) remove_checkpoint_designs(2)

OPT-1603 (error) Insufficient virtual memory. Please increase swap space, or reduce other processes on this host.

DESCRIPTION

This error message occurs when the host machine has insufficient virtual memory (swap space) to start another process. Possible causes are that the host does not have enough swap space configured, or there are too many other processes sharing the

host and not leaving sufficient swap space available.

WHAT NEXT

Check what else is running on the host, and perhaps schedule large jobs to run at different times. Also, consider increasing swap space on the host.

OPT-1604 (information) Verification priority attribute is set for '%s'.

DESCRIPTION

This information message occurs when **verification_priority** attribute is set on the specified design or instance.

WHAT NEXT

This is an information-only message. No action is required.

SEE ALSO

compile(2)
set_verification_priority(2)

OPT-1650 (warning) Area recovery is stopped due to unexpected long run time, and the final optimization QoR may be affected.

DESCRIPTION

This error indicates that the area recovery optimization takes too much time and it is stopped prematurely. This is likely due to potential run time issues in the tool. As the area recovery optimization does finish properly as in normal flow, the resulted design may have sub-optimal QoR.

WHAT NEXT

It is recommended to discard this result and re-run the optimization command in one of the two ways: (1) remove the **-area_recovery** option; (2) set **psynopt_disable_auto_cpulimit_for_area_recovery**. Please also contact Synopsys for additional support.

SEE ALSO

psynopt_disable_auto_cpulimit_for_area_recovery(3) place_opt(2) psynopt(2) remove_checkpoint_designs(2)

OPT-1701 (information) Keep the hierarchy %s that contains CRC logic.

DESCRIPTION

This information message occurs when the specified hierarchy contains CRC logic. Isolating such hierarchies helps Formality to successfully verify the design. The hierarchy is retained until the **ungroup** command is run with the **-force** option.

WHAT NEXT

This is an information-only message. No action is required.

SEE ALSO

compile(2)

OPT-1702 (information) Create design %s with CRC logic in %s.

DESCRIPTION

This information message occurs when the specified hierarchy contains CRC logic in function calls. The new design is created for the CRC logic and the new design hierarchy will be kept at the end of the compile. The new design cannot be ungrouped until the **ungroup** command is run with the **-force** option. Isolating such hierarchies helps Formality to successfully verify the design.

WHAT NEXT

This is an information-only message. No action is required.

SEE ALSO

compile(2)

OPT-9990 (warning) more hier VA overwrite DB VA message

suppressed.

DESCRIPTION

When checking voltage area consistency, if there are more than 20 cell instances met with voltage area mismatch, the detail messages will be suppressed.

WHAT NEXT

Check voltage area setting of the whole hier scope.

SEE ALSO

OPT-999

OPT-9991 (warning) cannot find tech info about mask layer <%s>.

DESCRIPTION

Cannot find tech info about mask layer <%s> when loading layer info from technology file.

WHAT NEXT

Check technology file to make sure the setting about layer <%s>.

OPT-9992 (warning) hier %s does not exist.

DESCRIPTION

Cannot find hier in design when handle DontTouch setting.

WHAT NEXT

Check design and related DontTouch setting.

OPT-9993 (warning) level shifter '%s' could not be sized

because it is marked as dont_touch.

DESCRIPTION

Shows level shifters could not be sized which are marked as dont_touch.

OPT-9994 (warning) Use ’astWriteDC’ to dump all dont_touch cells.

DESCRIPTION

If necessary please use "astWriteDC" to dump all dont_touch cells and check them.

WHAT NEXT

Check DontTouch settings dumpped by "astWriteDC" if necessary.

OPT-9995 (warning) cell instance ’%s’ hier VA ’%s’ overwrite DB VA ’%s.

DESCRIPTION

When checking voltage area consistency, there may be mismatch between voltage area of hier scope of cell instance and voltage area of cell instance. This warning shows the mismatch occurs and the voltage area of cell instance is overwritten by the voltage area of hier scope of the cell instance.

WHAT NEXT

Check voltage area setting of the whole hier scope.

OPT-9996 (error) set_max_dynamic_power should be specified for all the scenarios.

DESCRIPTION

For dynamic power optimization, set_max_dynamic_power should be specified for all the scenarios. If you do not want to optimize dynamic power, set_max_dynamic_power should not be specified for any scenario.

WHAT NEXT

Either specify set_max_dynamic_power for all the scenarios or do not specify it for any scenario.

OPT-9997 (error) %s cannot be used for multicorner designs.

DESCRIPTION

This error message occurs because the specified feature is not supported for multicorner designs.

WHAT NEXT

Remove the command or unset the environment variable that needs this feature during compile.

OPT-9998 (error) %s cannot be used for multi-scenario designs.

DESCRIPTION

This error message occurs because the specified feature is not supported for multi-scenario designs.

WHAT NEXT

Remove the command or unset the environment variable that needs this feature during compile.

SEE ALSO

compile(2)

OPT-9999 (error) Scenario ’%s’ does not have a scaling library group setting.

DESCRIPTION

This error message occurs when the scaling library group is set for the reported scenario(s).

WHAT NEXT

Use the **set_scaling_lib_group** command to set the scaling library group for the reported scenario(s).

SEE ALSO

set_scaling_lib_group(2)

OPT-10000 (Information) Scenario '%s': Scenario option '%s' conflicts with '%s' constraint.

DESCRIPTION

This error message occurs when **set_max_leakage_power** constraint is set but scenario_option '**leakage_power**' is set to false. OR **set_max_dynamic_power** constraint is set but scenario option **dynamic_power** is set to false.

Both the scenario_option and constraint need to be set for the constraint to be honored. The conflicting constraint will be ignored.

WHAT NEXT

Remove the conflcting constraint **set_max_leakage_power** or **set_max_dynamic_power** OR set to true the scenario option 'leakage_power' or 'dynamic_power'.

SEE ALSO

report_scenarios(2)
report_scenario_options(2)
set_scenario_options(2)
set_max_leakage_power(2)
set_max_dynamic_power(2)

PARA-001 (error) Cannot open file '%s'.

DESCRIPTION

The file name provided to **read_parasitics** cannot be opened.

WHAT NEXT

Validate that the file name is correct.

PARA-003 (information) The net '%s' has many (%d) nodes, which might result in long runtime.

DESCRIPTION

You receive this message if the number of nodes in an annotated parasitic network exceeds the value of the **parasitics_warning_net_size** variable (default 10000). This message warns you that extended runtime could occur.

If the number of nodes exceeds the value of **parasitics_rejection_net_size** (default 20000), the network is rejected and automatically replaced by a lumped capacitance to avoid extended runtime. You receive a message (PARA-004) warning you of that action.

The value of **parasitics_warning_net_size** is ignored if it is greater than or equal to the value of **parasitics_rejection_net_size**.

The values of these variables are checked every time **read_parasitics** is issued.

WHAT NEXT

This is an informational message only. No action is required on your part. To avoid receiving this message, you can increase the value of the **parasitics_warning_net_size** variable, or modify your parasitic network so that it contains fewer nodes.

SEE ALSO

PARA-004 (n).

PARA-004 (warning) The net '%s' has too many (%d) nodes, so a lumped capacitance will be used instead.

DESCRIPTION

You receive this message if the number of nodes in an annotated parasitic network exceeds the value of the **parasitics_rejection_net_size** variable. This message warns you that the detailed network is being replaced by a lumped total capacitance to avoid extended runtime.

If the number of nodes exceeds the value of the **parasitics_warning_net_size** variable (default 10000), you receive a message (PARA-003) warning you that extended runtime could occur.

The value of **parasitics_warning_net_size** is ignored if it is greater than or equal to the value of **parasitics_rejection_net_size**.

The values of these variables are checked every time **read_parasitics** is issued.

WHAT NEXT

If it is acceptable to you for your detailed network to be replaced by a lumped total capacitance, no action is required on your part. Otherwise, you can increase the value of the **parasitics_rejection_net_size** variable, or modify the annotated parasitic network so that it contains fewer nodes.

SEE ALSO

PARA-003 (n).

PARA-005 (error) Cannot use -keep_capacitive_coupling with %s format.

DESCRIPTION

You specified the **read_parasitics** command with the **-keep_capacitive_coupling** option, and the file format does not support it. Detailed Standard Parasitic Format (DSPF) and Reduced Standard Parasitic Format (RSPF) do not support **-keep_capacitive_coupling**.

WHAT NEXT

To read this file, reenter the **read_parasitics** command without using the **-keep_capacitive_coupling** option.

PARA-006 (error) %s pin '%s' is missing in the RC annotation for net '%s'. Ignoring the incomplete RC annotation.

DESCRIPTION

You receive this message if **report_annotated_parasitics** detects an incompletely back-annotated RC network in the current design. The message informs you that the RC network annotation on the specified net is being ignored because it is incomplete; the specified pin is not physically connected to the RC network annotation.

An incomplete RC network might be caused by errors in the parasitics file, or by missing information from the tool that generated the parasitics file. For example, a parasitics file generated by a place and route tool that has parasitics only for the top level (between the blocks) would generate this error, because PrimeTime requires the RC network to connect all leaf drivers to all leaf nodes.

This message is not issued for unconnected hierarchy pins; when these are missing in RC annotations, warning message PARA-007 is issued and the annotation is not ignored during delay calculation.

WHAT NEXT

Examine the SPF or SPEF file to determine why the specified RC network is incomplete. If the error is caused by a valid incomplete network, you can complete it using the parasitics completion feature **read_parasitics -complete_with** or **complete_net_parasitics**. For other errors, you must correct the parasitics file manually. You might need to estimate the missing segments and manually add them. After you have corrected the SPF or SPEF file, reexecute **read_parasitics**.

To determine whether the parasitics file contains a valid incomplete RC network, start from a driver and try to reach all loads through resistances. If all missing segments of a net are between two pins, you can complete them using the parasitics completion feature; otherwise, you must correct the SPF or SPEF file manually.

SEE ALSO

PARA-007 (n), **read_parasitics** (2), **report_annotated_parasitics** (2), **complete_net_parasitics** (2).

PARA-007 (warning) Unconnected hierarchy pin '%s' is missing

in the RC annotation for net '%s'.

DESCRIPTION

You receive this message if **read_parasitics** or **report_annotated_parasitics -check** detects an incompletely back-annotated RC network in the current design. PrimeTime can tolerate missing unconnected hierarchy pins in RC annotations, so the annotation is not ignored during delay calculation. This message is only a warning; it can be suppressed with the **suppress_message** command.

If a missing pin is not an unconnected hierarchy pin, error message PARA-006 is issued instead and the RC annotation is ignored during delay calculation.

WHAT NEXT

If you have not intentionally disconnected hierarchy pins from networks with exisiting RC annotations, investigate the source of the disconnection. Some tools temporarily add routing ports and fail to remove those unused after routing, and others disconnect test ports during scan-chain reordering.

SEE ALSO

PARA-006 (n), **read_parasitics** (2), **report_annotated_parasitics** (2), **complete_net_parasitics** (2).

PARA-008 (error) The RC annotation for net '%s' has too many near-zero elements.

DESCRIPTION

This message is shown if **report_annotated_parasitics** detects that the RC annotation has too many near-zero elements. Too many near-zero elements can lead to numeric instability in calculations.

A resistor with value less than or equal to 0.01 ohm is considered near-zero.

A capacitor with value less than or equal to 0.001 femtofarad is considered near-zero.

PrimeTime allows up to ten-thousand near-zero resistors and up to ten-thousand near-zero capacitors before rejecting the annotation.

Please note that near-zero capacitor elements can occur in an annotation due to specifying resistors without specifying the capacitors at resistors' nodes. In such cases PrimeTime will automatically create such capacitors with values of 0.001 femtofarad.

WHAT NEXT

The only known instance of this problem is trying to annotate a gigantic clock-tree as a single net (i.e. with tens of thousands of fanouts) with near-zero placeholder data. The annotation must make physical sense in order to be used in RC delay calculations. Either the near-zero data must be changed or the net must be broken-up into smaller segments.

SEE ALSO

read_parasitics (2), **report_annotated_parasitics** (2), **complete_net_parasitics** (2).

PARA-010 (error) multiple occurrences of net '%s' in this file. Removed parasitics from this net.

DESCRIPTION

You read a binary parasitics (SBPF) file and there were multiple occurrences of some nets in that file, which is illegal. This is a very serious error. Either the netlist does not match the parasitics file, or there is a problem with the writer of the file. Each of these nets with corrupt parasitics has had its parasitics removed, generating this message. Further, all coupling for the entire file is ignored.

The binary parasitics file is expected to be an image of parasitics. That is, it is meant to be restored to the same netlist from which it was generated. Attempting to restore a binary parasitics file to a different netlist is an unsupported flow.

WHAT NEXT

This condition has put the parasitics annotated on the design into an incomplete state. This may lead to inaccurate or incorrect results. You should discontinue the current session and determine if this is a mismatch between the file and the netlist, or if there is a problem with the provider of the binary parasitics file.

SEE ALSO

read_parasitics (2). **PARA-011** (n).

PARA-011 (error) Due to previous errors, all effects of coupling have been ignored

from '%s'

DESCRIPTION

You receive this message in conjunction with PARA-010. You read a binary parasitics (SBPF) file and there were multiple occurrences of some nets in that file, which is illegal. Because of this problem, any effects of coupling were ignored for the file being read. If you were using *-keep_capacitive_coupling*, no new coupling capacitors would be added. If you were not using *-keep_capacitive_coupling*, no coupling capacitors would be reduced. They are simply ignored.

WHAT NEXT

It is not recommended that you continue at this point. See the documentation for PARA-010 for mode details.

SEE ALSO

read_parasitics (2). **PARA-010** (n).

PARA-020 (warning) -keep_capacitive_coupling not specified for a design which already has coupling.

DESCRIPTION

You receive this message from the **read_parasitics** command if you did not specify the **-keep_capacitive_coupling** option, but you previously issued a **read_parasitics** command to read an SPEF file (for the same design) and did use the **-keep_capacitive_coupling** option. This message warns you about a possible inconsistency between multiple **read_parasitics** commands.

WHAT NEXT

If you intended not to use the **-keep_capacitive_coupling** option, no action is required on your part. Otherwise, reissue **read_parasitics** and use the **-keep_capacitive_coupling** option.

PARA-027 (error) Cannot specify both the -coupling_reduction_factor and

the -keep_capacitive_coupling options.

DESCRIPTION

The **read_parasitics** command found that both the **-coupling_reduction_factor** and the **-keep_capacitive_coupling** options are set.

WHAT NEXT

Choose either the **-coupling_reduction_factor** or the **-keep_capacitive_coupling** option, but not both. If you specify the **-coupling_reduction_factor** option, the coupling capacitors are reduced to ground with the factor specified by the *factor* value, which conflicts with the use of the **-keep_capacitive_coupling** option. If you intend to keep the coupling capacitors, you do not need to specify the **-keep_capacitive_coupling** option.

SEE ALSO

read_parasitics (2).

PARA-040 (warning) Coupling capacitor (%s %s %g) on net %s is discarded because %s

DESCRIPTION

The **read_parasitics** command found a problem with a coupling capacitor and the capacitor was discarded. The reason is given in the message. Typical reasons include missing objects (nets, pins), both nodes being in the same net (self-coupling of nets is not supported), or a capacitance value less than or equal to zero.

Note that in the case of self-coupling, this message will be issued whether or not the **-keep_capacitive_coupling** option is specified.

WHAT NEXT

Examine the Standard Parasitic Exchange Format (SPEF) file for correctness.

SEE ALSO

read_parasitics (2).

PARA-041 (warning) Coupling capacitor (%s %s %g) on net %s

is reduced because %s

DESCRIPTION

You receive this message if the **read_parasitics** command found a coupling capacitor in a SPEF file which specifies a nonexistent aggressor sub-node. This error could be caused by a large RC network that was discarded by PrimeTime. This message warns you that the coupling capacitor connected being reduced (grounded).

WHAT NEXT

This is a warning message only. If it is acceptable to you that the specified coupling capacitor is grounded, no action is required on your part. Otherwise, check the consistency between the netlist and SPEF file, and check for the presence of a large RC network. Make any changes necessary, then reexecute **read_parasitics**.

PARA-043 (warning) Invalid coupling capacitor (%s %s %g) on net %s:
%s

DESCRIPTION

While reading a SPEF file, the **read_parasitics** command found an invalid coupling capacitor. This is usually due to a semantic error in the specification of the capacitor.

WHAT NEXT

The reason is given in the body of the message.

SEE ALSO

read_parasitics (2).

PARA-044 (error) Invalid %s (%s %g) on net %s:
%s

DESCRIPTION

The **read_parasitics** command found a capacitor or resistor which is invalid. This is usually due to a mismatch between the netlist and the parasitics file. The reason is

given in the body of the message.

WHAT NEXT

Examine the parasitics file for correctness.

SEE ALSO

read_parasitics (2).

PARA-045 (information) Merging parallel capacitor on net %s from %s %s with value %g: new total value %g.

DESCRIPTION

The **read_parasitics** command found a capacitor in parallel with another capacitor. This could be due to duplicate entries in a parasitics file, or a reduced coupling capacitor in a SPEF file.

WHAT NEXT

No action necessary.

SEE ALSO

read_parasitics (2).

PARA-046 (warning) No matching coupling capacitor found with value %g for victim net %s and aggressor net %s: Ground this coupling capacitor.

DESCRIPTION

The **read_parasitics** command found a coupling capacitor in the SPEF file in a victim D_NET which does not have a complimentary entry in the referenced aggressor D_NET. In this case, the coupling capacitor is grounded.

WHAT NEXT

Correct SPEF calls for symmetric entries. Validate that this is an expected behavior of your extraction application.

SEE ALSO

read_parasitics (2).

PARA-047 (warning) Net %s has been annotated with %s %s using the %s command. This takes precedence over values from parasitics.

DESCRIPTION

The **read_parasitics** command found a network which already has annotated lumped capacitance or resistance set using the **set_load** or **set_resistance** commands, respectively. Lumped values from these commands take precedence over the values from parasitics files.

WHAT NEXT

To use the total capacitance or resistance read in from a parasitics file, you must remove the existing values by using the **remove_capacitance** or **remove_resistance** command.s PrimeTime then reverts to the detailed (or other) RC network.

SEE ALSO

read_parasitics (2), **remove_capacitance** (2), **remove_resistance** (2), **set_load** (2), **set_resistance** (2).

PARA-050 (information) Merged %d parallel coupling capacitors to total %g pf between file nodes '%s' and '%s'

.

DESCRIPTION

While reading a SPEF file, the **read_parasitics** command found parallel coupling capacitors between two nets which needed to be merged. These parallel coupling capacitors are replaced by a single coupling capacitor with the capacitance equal to

the sum of the capacitance of the parallel coupling capacitors. The number of capacitors, and the resulting total capacitance, are shown in the message.

WHAT NEXT

No action necessary.

SEE ALSO

read_parasitics (2).

PARA-051 (warning) Self-coupling for net '%s' is discarded

DESCRIPTION

The **read_parasitics** command found coupling from a net to itself in a Synopsys Binary Parasitics Format (SBPF) file. PrimeTime does not support self-coupling, so this coupling is discarded. Note that this message will be issued whether or not the **-keep_capacitive_coupling** option is specified.

WHAT NEXT

No action is necessary. However, the user should determine if the application which wrote the binary parasitics file has a mode which will suppress self-coupling.

SEE ALSO

read_parasitics (2).

PARA-052 (warning) Cannot use -increment with reduced parasitics.
Net '%s' will be overwritten with %s parasitics from '%s'

DESCRIPTION

The **read_parasitics** command was used with the **-increment** option, and the net in question already has parasitics. This message is issued if the current file has reduced parasitics for the net, or if the net has reduced parasitics and the current file has detailed parasitics for the net. In any of these cases, the parasitics for the net are removed, and the parasitics from the file overwrite what was there. The **-increment** option only works for detailed parasitics.

WHAT NEXT

No action is necessary. However, the user should determine if the usage of the **-increment** option is correct.

SEE ALSO

read_parasitics (2).

PARA-053 (error) %s '%s' exists but is not connected to net '%s'

DESCRIPTION

The **read_parasitics** command was used to read binary parasitics. There is a mismatch between the binary parasitics file and the netlist. The data in the file indicates that the named pin or port is connected to the specified net, but it is not. This error will prevent the parasitics from being annotated on this net.

WHAT NEXT

Ensure that you are applying the correct binary parasitics file to the correct netlist.

SEE ALSO

read_parasitics (2).

PARA-060 (warning) failed to re-anchor parasitics on net '%s'

DESCRIPTION

An **insert_buffer** command was issued to buffer either the load or driver side pin of a net with parasitics. The parasitics are re-anchored on either the driver or load side of the buffer being inserted. If the re-anchoring failed all the parasitics of the orignial net will be removed. When this happens both the driver and load side nets of the inserted buffer will have no parasitics.

WHAT NEXT

Parasitics will only be preserved if a single load or driver pin is being buffered. Although multiple pins can be buffered parasitics will not be preserved if more than one pin is buffered.

Use set_load to try and compensate for the removed parasitics.

SEE ALSO

insert_buffer

PARA-061 (warning) failed to re-anchor parasitics on net '%s'

DESCRIPTION

A **remove_buffer** command was issued and parasitics were present on the driver and/or load side nets connected to the buffer. The parasitics with the worst ground capacitance are moved to the net resulting after the buffer removal. If the re-anchoring failed all the parasitics of the driver and/or load side nets originally connected to the buffer will be removed. When this happens the resulting net after the buffer removal will have no parasitics.

WHAT NEXT

Use report_net to examine the pins of load and driver side nets of the buffer being removed.

Use set_load to try and compensate for the removed_parasitics

SEE ALSO

remove_buffer

PARA-062 (error) -original_file_name used without -eco.

DESCRIPTION

The **original_file_name** can only be used along with the **eco** option to specify which original parasitic file that the given eco file corresponds to.

WHAT NEXT

Use -eco switch also if you are reading ECO parasitics. If not, do not use -original_file_name option.

SEE ALSO

read_parasitics

PARA-063 (error) An ECO file cannot be read without reading original parasitics in SPEF or in version 3 (or later) of SBPF.

DESCRIPTION

The **-eco** option is used to load parasitics incrementally for an ECO change after original analysis is performed. The original parasitics should be present before one can read the ECO parasitics. Also, even if the original parasitics were read using version 2 or version 1 of SBPF, ECO operation cannot be applied. Only the version 3 or later versions of SBPF can be used for ECO operations.

WHAT NEXT

Read the original parasitics before reading the ECO parasitics.

SEE ALSO

read_parasitics

PARA-064 (error) Cannot auto-determine original file name for the ECO.

DESCRIPTION

The **-eco** option is used to load ECO parasitics corresponding to a particular extraction database. In the current session, parasitics were read in using multiple files. The attempt to auto-determine the original file name failed. Use **-original_file_name** option to distinguish which parasitic file that this ECO file corresponds to.

WHAT NEXT

Give the **-original_file_name** option.

SEE ALSO

read_parasitics

PARA-065 (error) The specified original file cannot be found.

DESCRIPTION

The specified original file can not be found. If you used **-path** option while reading the original file, please issue the same **-path** for reading the ECO file also.

WHAT NEXT

Check the file name given to **-original_file_name** option.

SEE ALSO

read_parasitics

PARA-066 (information) Attempting to read the ECO file to determine original file name.

DESCRIPTION

The **-eco** option is specified without specifying the **-original_file_name** option. Since parasitics are annotated into the current session using multiple parasitic files, it is necessary to determine which file does the ECO file correspond to. An attempt is being made to determine this information by looking at the ECO file.

WHAT NEXT

If you do not want PTSI to auto determine this information, please provide **-original_file_name** option.

SEE ALSO

read_parasitics

PARA-067 (information) Attempting to read the parasitic file to auto-determine location transformation factors.

DESCRIPTION

The **-path** and **-increment** options are specified to read a parasitic file with locations without specifying the locations transformation factors. An attempt is

being made to determine this information by looking at the parasitic file.

WHAT NEXT

This is just information message, no action required.

SEE ALSO

read_parasitics

PARA-068 (information) Locations of block %s are being transformed for '%s' rotation, '%s' flip, '%i' X offset and '%i' Y offset.

DESCRIPTION

This message gets issued only when you are reading parasitics with locations turned on via the variable 'read_parasitics_load_locations'. It was determined that the given block is rotated, flipped and/or offset before being placed at the chip-level. Hence, the locations will be automatically transformed to global co-ordinates. Global co-ordinates are determined by looking at the file that was read in without the -path option.

WHAT NEXT

This is just an information message.

SEE ALSO

read_parasitics (2)

PARA-069 (error) Invalid '%s' scale factor '%f'.

DESCRIPTION

A parasitic scale factor is defined as a floating point number greater than ZERO. You get this message when you specified a parasitic scale factor that is less than or equal to ZERO.

WHAT NEXT

Make sure you specify correct scale factors and re-run the command.

SEE ALSO

scale_parasitics (2)

PARA-070 (error) There are no parasitics loaded.

DESCRIPTION

You have attempted to perform an operation like scale_parasitics that requires parasitics to have been loaded but no parasitics are set on this current design.

WHAT NEXT

Read the parasitics first and re-run the command.

SEE ALSO

read_parasitics (2) **scale_parasitics** (2)

PARA-071 (error) No net-specific scaling has been done.

DESCRIPTION

You have attempted to reset scaling for few nets. But, reset_scale_parasitics on certain number of nets works only if there has been some previous net-specific scaling done. This message indicates that no such scaling has been done previously.

WHAT NEXT

You may not want to issue reset_scale_parasitics, you may want to use scale_parasitics instead with factors equal to 1.0.

SEE ALSO

scale_parasitics (2) **reset_scale_parasitics** (2)

PARA-072 (warning) No net-specific scaling has been done for

net ’%s’.

DESCRIPTION

You have attempted to reset/report scaling for few nets. But, reset_scale_parasitics or report_scale_parasitics on certain number of nets works only if there has been some previous net-specific scaling done. This message indicates that no such scaling has been done previously.

WHAT NEXT

You may not want to issue reset_scale_parasitics, you may want to use scale_parasitics instead with factors equal to 1.0.

SEE ALSO

scale_parasitics (2) **reset_scale_parasitics** (2) **report_scale_parasitics** (2)

PARA-073 (error) No scaling has been done.

DESCRIPTION

You have attempted to reset scaling of parasitics. But, reset_scale_parasitics works only if there has been some previous parasitic scaling done. This message indicates that no such scaling has been done previously.

WHAT NEXT

You may not want to issue reset_scale_parasitics.

SEE ALSO

scale_parasitics (2) **reset_scale_parasitics** (2)

PARA-074 (error) Invalid ECO SBPF found.

DESCRIPTION

You have attempted to read an ECO SBPF file. PTSI determined that the ECO file does not correspond to the original parasitic file. No coupling will be read from this current file.

WHAT NEXT

You may not want to make sure you are using correct ECO SBPF file.

SEE ALSO

read_parasitics (2)

PARA-075 (error) Could not resolve net '%s'.

DESCRIPTION

This message gets issued when you are reading parasitics and a net name is found in the parasitic file that could not be resolved to any real net in the design. This happens when your physical design does not match the logical design. Net is searched by the net name and may also be searched by pin names associated on the net. This message tells you that all the searching did not the net name to any net or it resolved it to more than one net in the design.

WHAT NEXT

Make sure your parasitic file matches the design.

SEE ALSO

read_parasitics (2)

PARA-076 (error) Failed to create on-disk-caching files.

DESCRIPTION

The program failed to create temporary files for on disk caching. This can be due a number of reasons like the lack of write permissions on the specified cache directory, lack of disk space and so on.

WHAT NEXT

Verify the permissions, disk space and reissue the command

PARA-077 (information) Coupling separations are set on the

design that might overwrite the annotated cross-couplings.

DESCRIPTION

This message gets issued to inform you that you have set coupling separations for cross-talk or noise analysis and are reading parasitics. The coupling separation constraints take precedence and will overwrite the annotated cross-couplings for the specific nets.

WHAT NEXT

This is just an information. No action is required.

SEE ALSO

read_parasitics (2) **set_coupling_separation** (2) **report_si_delay_analysis** (2) **report_si_noise_analysis** (2)

PARA-078 (error) Could not find pin/port '%s' in design.

DESCRIPTION

You get this message when you are trying to read parasitics and a specified pin/port cannot be found in the design.

WHAT NEXT

Check the parasitic file/parasitic extractor for errors.

SEE ALSO

read_parasitics (2)

PARA-079 (error) Could not find net connected to pin/port '%s' in design.

DESCRIPTION

You get this message when you are trying to read binary parasitics and an unconnected pin/port is being annotated in the design.

WHAT NEXT

Check the parasitic file/parasitic extractor for errors.

SEE ALSO

read_parasitics (2)

PARA-080 (error) Cannot read variation-aware parasitics when parasitics are already present.

DESCRIPTION

You get this message when you are trying to read variation-aware parasitics and the design is already annotated with parasitics. This is a limitation for now, and will be supported in future.

WHAT NEXT

Remove the annotated parasitics and re-issue the read_parasitics command.

SEE ALSO

read_parasitics (2) **remove_annotated_parasitics** (2)

PARA-081 (error) Cannot read regular parasitics as variation-aware parasitics are already annotated on the design.

DESCRIPTION

You get this message when you are trying to read non-variation aware parasitics and variation-aware parasitics are already annotated on the design.

WHAT NEXT

Remove the annotated parasitics and re-issue read_parasitics command.

SEE ALSO

read_parasitics (2) **remove_annotated_parasitics** (2)

PARA-082 (error) Cannot open parasitic corner file '%s'.

DESCRIPTION

You get this message when you issue set_parasitic_corner command and the corner file cannot be opened for reading.

WHAT NEXT

Check the file permissions and re-issue the command.

SEE ALSO

set_parasitic_corner (2) **report_annotated_parasitics** (2)

PARA-083 (error) Unexpected data at line number '%d'.

DESCRIPTION

You get this message when you issue set_parasitic_corner and the parasitic corner file has unexpected contents.

WHAT NEXT

Check the file contents and re-issue the command.

SEE ALSO

set_parasitic_corner (2) **report_annotated_parasitics** (2)

PARA-084 (error) Variation-aware parasitics are not loaded.

DESCRIPTION

You get this message when you perform an operation that requires variation-aware parasitics to be set and there are no such parasitics currently annotated.

WHAT NEXT

Read the variation-aware parasitics and re-issue the command.

SEE ALSO

set_parasitic_corner (2) **remove_parasitic_corner** (2) **read_parasitics** (2) **report_annotated_parasitics** (2)

PARA-085 (error) Parasitic corner is not set previously.

DESCRIPTION

You get this message when you issue 'remove_parasitic_corner' to remove the parasitic corner set for analysis in the presence of variation-aware parasitics and the tool determines that no parasitic corner was set previously.

WHAT NEXT

No action is required.

SEE ALSO

remove_parasitic_corner (2) **set_parasitic_corner** (2) **read_parasitics** (2) **report_annotated_parasitics** (2)

PARA-086 (error) Parasitic corner cannot be found.

DESCRIPTION

You get this message when you issue 'set_parasitic_corner' to set the parasitic corner but the specified corner name cannot be found in the specified corner file.

WHAT NEXT

Check the corner file and re-issue the command.

SEE ALSO

set_parasitic_corner (2) **remove_parasitic_corner** (2) **read_parasitics** (2) **report_annotated_parasitics** (2)

PARA-087 (warning) Variation multiplier value for '%s' is outside

the bounds at line '%d'.

DESCRIPTION

You get this message when you issue 'set_parasitic_corner' to set the parasitic corner but the specified corner in the corner file contains invalid variation multiplier values. These values are supposed to be within -3.0 to +3.0.

WHAT NEXT

Check the corner file.

SEE ALSO

set_parasitic_corner (2) **remove_parasitic_corner** (2) **read_parasitics** (2) **report_annotated_parasitics** (2)

PARA-088 (error) Corner file does not match the base corner - aborting the reading. This is occuring while reading ground capacitances/resistances of net '%s'.

DESCRIPTION

You get this message when you are trying to read multiple corner parasitics but it is found that the current corner topology does not match the base corner.

WHAT NEXT

Check the corner parasitic file and re-issue the command.

SEE ALSO

read_parasitics (2)

PARA-089 (warning) Ignoring the temperature parameter or unknown process variation parameter '%s'.

DESCRIPTION

You get this message when you are trying to read a corner file for variation-aware

parasitics but the variation parameters given in the file do not match with the defined parasitic parameters. This can also happen for temperature corner setting because PrimeTime VX does not currently support temperature as a variation.

WHAT NEXT

You may want to check the corner parasitic file.

SEE ALSO

set_parasitic_corner (2) **report_annotated_parasitics** (2)

PARA-090 (error) The "-create_default_variations" option can be used only along with "-keep_variations" option.

DESCRIPTION

You get this message when you are trying to read parasitics without keeping variation sensitivities but trying to generate default variation parameters.

WHAT NEXT

Re-issue the command without the "-create_default_variations" option.

SEE ALSO

read_parasitics (2)

PARA-091 (warning) Failed to create node map information for the parasitic file.

DESCRIPTION

You get this message when you are trying to read parasitics with keeping coupling but PT was unable to create node map information between the parasitic file and PT. This node map information is usually not needed for the operation of PT, unless when you try to read in an ECO parasitic file via "read_parasitics -eco" in future.

WHAT NEXT

You do not need to do anything.

SEE ALSO

read_parasitics (2)

PARA-092 (error) Cannot read variation-aware parasitics as regular parasitics are already annotated on the design.

DESCRIPTION

You get this message when you are trying to read variation-aware parasitics and non-variation-aware parasitics are already annotated on the design.

WHAT NEXT

Remove the annotated parasitics and re-issue read_parasitics command.

SEE ALSO

read_parasitics (2) **remove_annotated_parasitics** (2)

PARA-093 (error) Number of variation parameters do not match. Aborting the reading.

DESCRIPTION

You get this message when you are trying to read variation-aware parasitics and the number of variation parasitics do not match the previous annotation. It is assumed that all parasitic extractions are done with the same variation-ITF file, hence the number of variation parameters, their names and order is supposed to match across all parasitic files.

WHAT NEXT

Check the parasitic files, the writer and figure out the reason for the mismatch and re-issue the command.

SEE ALSO

read_parasitics (2) **remove_annotated_parasitics** (2)

PARA-094 (error) Number of variation parameters do not match. Aborting the reading.

DESCRIPTION

You get this message when you are trying to read variation-aware parasitics and the number of variation parasitics do not match the previous annotation. It is assumed that all parasitic extractions are done with the same variation-ITF file, hence the number of variation parameters, their names and order is supposed to match across all parasitic files.

WHAT NEXT

Check the parasitic files, the writer and figure out the reason for the mismatch and re-issue the command.

SEE ALSO

read_parasitics (2) **remove_annotated_parasitics** (2)

PARA-095 (error) Number of corners do not match for multi-corner read.

DESCRIPTION

You get this message when you are trying to read multi-corner binary parasitic file but the number of corners from the file do not match what is set previously. Aborting the read.

WHAT NEXT

Check the parasitic files, the writer and figure out the reason for the mismatch and re-issue the command.

SEE ALSO

read_parasitics (2)

PARA-096 (information) Scaling parasitics to operating

temperature of '%f'.

DESCRIPTION

You get this message when you are trying to read variation-aware parasitic files that have temperature sensitivities. If the operating condition temperature is different than the (global) extraction temperature, then this message is issued to inform you that the parasitics will be scaled to the given operating temperature.

WHAT NEXT

No need of any action.

SEE ALSO

read_parasitics (2)

PARA-097 (error) All instance paths in the -path option should correspond to valid and same sub-design.

DESCRIPTION

You get this message when you are trying to read parasitic files with a list of paths specified in the -path option and not all the paths correspond to the same sub design or some of the paths do not correspond to a valid hierarchical instances.

WHAT NEXT

Reissue the command with proper paths in the -path option.

SEE ALSO

read_parasitics (2)

PARA-098 (warning) Detected semantically incorrect SPEF in coupling section.

DESCRIPTION

You get this message when you are trying to read parasitic files where the coupling capacitances are written in semantically incorrect manner. According to IEEE Std

SPEF, coupling should be written so that current net comes first followed by coupled net. The application will read the file but runtime may be slower. Also, the support is not guaranteed in future versions.

WHAT NEXT

No action needed for now, but please check with the SPEF writer tool to see why it is not following the standard.

SEE ALSO

read_parasitics (2)

PARA-099 (error) Loading locations with simultaneous hierarchy reading is currently not supported.

DESCRIPTION

You get this message when you are trying to read parasitic files by loading the files simulataneously using multiple instances in the -path option but have also enabled loading locations. For loading locations, you have to issue each instance separately in -path option.

WHAT NEXT

Please re-issue read_parasitics command with one -path at a time.

SEE ALSO

read_parasitics (2)

PARA-100 (warning) No matching coupling capacitor found with value %g for victim net %s and aggressor net %s: Forcing symmetry for this coupling capacitor.

DESCRIPTION

The **read_parasitics** command found a coupling capacitor in the SPEF file in a victim

D_NET which does not have a complimentary entry in the referenced aggressor D_NET. In this case, the coupling capacitor is forced to be symmetric, that is, a coupling capacitor of that value is created between the two nets at the given nodes. If there are similar records in the two D_NETs, but the values are dissimilar, then the result will be a single coupling capacitor with a value that is the sum of the two dissimilar values.

WHAT NEXT

Correct SPEF calls for symmetric entries. Validate that this is an expected behavior of your extraction application.

SEE ALSO

read_parasitics (2).

PARA-101 (error) read_parasitics -eco can only be used when the program is in ECO mode.

DESCRIPTION

The **read_parasitics** command with -eco option can only be used in ECO mode.

WHAT NEXT

Use set_program_options -enable_eco to enable the ECO mode.

SEE ALSO

set_program_options (2), **sh_eco_enabled** (3).

PARA-102 (information) Reading parasitics file '%s' because parasitic information is required by the multicore master.

DESCRIPTION

During a multicore analysis using PrimeTime, the master process attempts to save runtime and memory by skipping the reading of parasitics, letting the remote processes perform this task instead. This saving is possible only when a single parasitics file, of any format other than PARA, DSPF or RSPF, is used within a session and the '-keep_capacitive_coupling', '-verbose', '-syntax_only', '-

keep_variations', or '-path' options are not used with **read_parasitics**.

However, several subsequent ECO or reporting commands will force the master to read the parasitics file: **complete_net_parasitics**, **connect/disconnect_net**, **insert/remove_buffer**, **report_annotated_parasitics**, **scale_parasitics**, **set_parasitic_corner** and **write_parasitics**.

WHAT NEXT

No action is needed but, for optimal performance, check your script to see whether the command that forces the parasitics to be read is necessary.

SEE ALSO

read_parasitics (2),

PARA-103 (information) Parasitics file '%s' will be read by the remote processes.

DESCRIPTION

During a multicore analysis using PrimeTime, this message is outputted to indicate that the remote processes will read the parasitics file directly if it has not already been done so by the master process.

WHAT NEXT

No action necessary.

SEE ALSO

read_parasitics (2), **PARA-102** (n).

PARA-104 (error) Corner file does not match the base corner - aborting the reading. This occurs while reading coupling between nets '%s' and '%s'.

DESCRIPTION

You get this message when you are trying to read multiple corner parasitics but it is found that the current corner topology does not match the base corner in coupling section.

WHAT NEXT

Check the corner parasitic file and re-issue the command.

SEE ALSO

read_parasitics (2)

PARA-105 (warning) Parasitics file ’%s’ was not read by the multicore master because the multi_core_read_parasitics variable is set to ’disabled’.

DESCRIPTION

During a multicore analysis using PrimeTime, this warning is outputted to indicate that the master did not read the parasitics file because the **multi_core_read_parasitics** variable is set to ’disabled’.

WHAT NEXT

To allow the master to read the parasitics file, set **multi_core_read_parasitics** to ’auto’.

SEE ALSO

read_parasitics (2),

PARSE

PARSE-1 (error) %s: %s on line %d at or near ’%s’.

DESCRIPTION

WHAT NEXT

PARSE-2 (error) %s on line %d at or near ’%s’.

DESCRIPTION

WHAT NEXT

PDC-001 (Warning) Cell %s does not have a port named %s

DESCRIPTION

The message is issued because a physical pin constraint has been read in that is to be applied to a non-existing port. This may not be a problem, especially if the pin constraint is for a feedthrough port not yet created. Nevertheless, the user is advised to double-check that the constraint being read in is really meant for the named cell.

WHAT NEXT

No action needed if user is positive that the constraints being read in are meant for the named cell

SEE ALSO

See man pages for read_io_constraints and set_pin_physical_constraints for proper u sages of these commands for loading physical pin constraints.

PDC-1 (error) Internal error.

DESCRIPTION

This error message indicates an unexpected internal error.

WHAT NEXT

Contact technical support.

SEE ALSO

NONE

PDC-2 (warning) Requested object(s) not found in Milkyway

database.

DESCRIPTION

This error message occurs when user requested data/action that depends on non-existing Milkyway objects. For example, user may have asked to report constraints on a pin but no constraints were previously set in the Milkyway database. In this case, user can either ignore the message or add the missing objects to the Milkyway database first and then re-try this command.

WHAT NEXT

If it is not obvious why the objects are missing in the database, verify the sequence of flow steps. If no flow error is identifiable, it is possible the database is corrupted. In that case either the database can be regenerated from scratch. If none of these steps remedy the situation consult your technical support

SEE ALSO

NONE

PDC-3 (error) File I/O error.

DESCRIPTION

There was an error in trying to create, access or update the specified file.

WHAT NEXT

Check the filename and path for correctness and verify if appropriate permissions exist.

SEE ALSO

NONE

PDC-4 (warning) Atleast one option should be specified

DESCRIPTION

The command requires atleast one of the listed options be specified.

WHAT NEXT

In some cases, the commands applies a default option. In that case nothing needs to be done. When a default is not obvious, command cannot continue. Try supplying the required option.

SEE ALSO

NONE

PDC-5 (error) Illegal value specified.

DESCRIPTION

The value supplied is not an acceptable value. Use the man page or command help or user’s guide to find out how to determine allowed values.

WHAT NEXT

Re-try the command by supplying a valid value.

SEE ALSO

NONE

PDEFP-1 (error) The PDEF file contains cluster data for the design '%s'; this cluster data cannot be annotated on the design '%s'.

DESCRIPTION

This message indicates that the design for which the cluster data was written, as indicated by the DESIGN construct of the PDEF file, is not the **current_design**. The name in the DESIGN construct of the PDEF file must be the name of the **current_design**.

WHAT NEXT

Verify that the PDEF file was created for the **current_design**, and if so, edit the PDEF file so that the DESIGN construct contains the name of the **current_design**.

PDEFP-2 (warning) The PDEFVERSION values we accept are '%s'.

DESCRIPTION

This message indicates that the current PDEF file was written using an unrecognized revision of the PDEF language. Revisions recognized by the current version of the **read_clusters** command are listed in the message.

This message is a warning only; **read_clusters** will attempt to read the file. However, if syntactic or semantic errors occur, you should suspect version incompatibility.

WHAT NEXT

If the file is read successfully, you need do nothing. However, if the file is not read successfully, verify that the PDEF file created is compatible with one of the versions indicated by this warning message.

PDEFP-3 (warning) The cluster '%s' has been duplicated; the most recently

read description of the cluster will be kept, while all previous versions will be overwritten.

DESCRIPTION

This message indicates that the cluster identified in the message has been defined more than once in the PDEF file. The last instance of the cluster in the file is considered valid; all other instances are ignored.

WHAT NEXT

Search the PDEF file for more than one cluster whose hierarchical name is the same as the one identified in the message. Determine the intent behind the duplication, and make appropriate corrections to the file.

PDEFP-4 (warning) The cell instance '%s' does not exist.

DESCRIPTION

The identified cell instance cannot be found in the logical hierarchy beneath **current_design**. The instance will be ignored unless the -allow_physical_cells option of read_pdef is used.

WHAT NEXT

Check to see why the instance identified in the message was included in the PDEF file. If the instance is meant to be in the floorplan as a physical-only cell, such as a filler cell or endcap cell, re-run read_pdef with the -allow_physical_cells option.

PDEFP-5 (warning) The cell instance '%s' has already been listed under cluster '%s'; this previous classification will be overwritten.

DESCRIPTION

This message indicates that the identified cell instance was previously listed as part of another cluster. The previous association is ignored. Only the most recent cluster association (that is, the cluster association furthest down in the file) will be preserved.

WHAT NEXT

Investigate the reason why the cell instance was listed in more than one cluster, and correct any errors.

PDEFP-6 (error) %s at or near token '%s'.

DESCRIPTION

A lexical or syntactic error has occurred in processing this PDEF file.

WHAT NEXT

Look at the line and token indicated in the message, and fix the problem.

PDEFP-7 (warning) The name of the cluster '%s' contains the character '/', which cannot be processed by dc_shell commands.

DESCRIPTION

This message warns you that you will not be able to refer to the specified cluster, or its sub-clusters, by name within **dc_shell**. The name contains the slash character ("/"), commonly used as a separator to identify the names of hierarchical clusters; the **dc_shell** cluster-processing commands cannot properly parse a cluster name that contains an embedded slash character.

WHAT NEXT

If you will not be referring to the specified cluster within **dc_shell**, you can leave the name as it is; it is possible to optimize a design that contains clusters of this type.

However, if you do intend to refer to the cluster within **dc_shell**, edit the cluster file and replace the slash character with another character in each cluster name.

PDEFP-8 (warning) The cell instance '%s' is not a leaf cell. Its presence

within this cluster will be ignored.

DESCRIPTION

This message indicates that the identified cell instance does not refer to a leaf cell. Each cell instance defined within a cluster must refer to a leaf cell; you cannot completely enclose a hierarchical cell in a cluster.

WHAT NEXT

Enumerate all leaf cells contained in this cell, and put each of them individually into the cluster.

PDEFP-9 (error) The subdesign '%s' of the current design '%s' contains unmapped cells. The entire design must be fully mapped.

DESCRIPTION

This message indicates that an unmapped cell was found in a subdesign during the checking phase of the **read_clusters** command. **read_clusters** requires that a design be completely mapped.

WHAT NEXT

Ensure that all cells are mapped by executing **compile** on the **current_design**.

PDEFP-10 (warning) A percentage utilization less than 0.0 was specified.

DESCRIPTION

The negative utilization percentage specified here will be ignored.

WHAT NEXT

If the negative utilization percentage was not intended, re-create the PDEF file.

PDEFP-11 (warning) A percentage utilization greater than 100.0

was specified.

DESCRIPTION

A percentage utilization greater than 100% was defined, which means that there is more cell area than the cluster can contain.

WHAT NEXT

The situation was probably caused by an error in the application that produced the PDEF file. The **read_clusters** command accepts the erroneous value and interprets it as an over-utilized block.

The **reoptimize_design** command seeks a secondary objective to reduce the utilization of all clusters below their MAX_UTILIZATION constraint. This cluster receives special attention to reduce the cell-area.

PDEFP-12 (warning) No UTILIZATION has been specified; the MAX_UTILIZATION value cannot be correctly interpreted in its absence, so it will be ignored.

DESCRIPTION

You have assigned a MAX_UTILIZATION attribute to a cluster, but no corresponding UTILIZATION attribute. To enforce the MAX_UTILIZATION restriction and determine how large the cluster can become, we must know the current utilization of the cluster.

WHAT NEXT

Modify the PDEF file to define the UTILIZATION attribute for the indicated cluster. Then, reread the file using the **read_clusters** command.

PDEFP-13 (warning) The attribute '%s' has been specified more than once for the object '%s'; the new value will override the old.

DESCRIPTION

This message indicates that an attribute is defined more than once for the specified

cluster or cell. The last value defined will be used.

WHAT NEXT

Remove the extra attributes.

PDEFP-14 (warning) The attribute '%s' has been specified with a value whose type is not %s; this value will be ignored.

DESCRIPTION

This message indicates that an attribute has been found that has an invalid type. Each of the possible cluster attributes can be only of a specific type. For example, the UTILIZATION attribute can be only an integer or a floating-point number. If an invalid value type is defined, it will be ignored, and the attribute's value will remain unchanged.

WHAT NEXT

Set the value of the attribute to the correct type.

PDEFP-15 (warning) The wire_load '%s' for cluster '%s' could not be found.

DESCRIPTION

A wire-load defined for a cluster could not be found in the libraries linked to the design being annotated. Either the link libraries don't include the library with the wire-load, or the name of the wire-load is incorrect.

WHAT NEXT

Set the **link_library** variable to include the library that contains this wire-load, or change the name of the wire-load in the .PDEF file.

PDEFP-16 (warning) The cell instance '%s' is not linked. Its presence

within this cluster will be ignored.

DESCRIPTION

This message indicates that the specified cell instance is not linked. Each cell instance defined within a cluster must refer to a fully linked leaf cell. You cannot define a cell in a cluster that is not fully linked.

WHAT NEXT

Find the design or library cell to which this cell instance should be linked, and include it in the **search_path** or **link_library**.

PDEFP-17 (warning) The attribute '%s' of %s '%s' is not recognized and will be ignored.

DESCRIPTION

This message indicates that the specified attribute is not recognized by the **read_clusters** command. **read_clusters** recognizes only a certain number of attributes and ignores the rest. This attribute is not recognized and is being ignored.

WHAT NEXT

Make sure the unrecognized attribute is not the result of some typing or translation error. If you intended for the attribute to be in the PDEF file, it does no harm to leave it in the PDEF file, but it has no effect on the processing of the cluster or cell.

PDEFP-18 (warning) The attribute '%s' has been specified with an invalid value. The value must be %s.

DESCRIPTION

This message indicates that an attribute has been defined with an illegal value.

WHAT NEXT

Change the attribute value to a legal value, as stated in the message.

PDEFP-19 (warning) The attribute '%s' has been specified more than once for
the cluster file %s; the new value will override the old.

DESCRIPTION

This message indicates that an attribute has been defined more than once for the specified cluster file. The last value defined will be used.

WHAT NEXT

Remove the extra attributes.

PDEFP-20 (warning) Attributes ignored for hierarchical cell %s.

DESCRIPTION

A cluster file has had an attribute defined for a hierarchical cell. Attributes are not currently supported on hierarchical cells.

WHAT NEXT

Remove the attributes from the hierarchical cell or else put leaf cells in the PDEF file instead, and set the attributes on the leaf cells.

PDEFP-21 (warning) Invalid NAMEPREFIX index (%d) for cell %s.

DESCRIPTION

The specified cell has a NAMEPREFIX index which was never defined via a NAMEPREFIX attribute in the current PDEF file. No prefix will be prepended to the cell name. This will most likely prevent the cell from being found in the design.

WHAT NEXT

Fix the PDEF file such that there is a NAMEPREFIX attribute with the proper index, or else remove the NAMEPREFIX index from the cell name definition.

PDEFP-22 (warning) Reading LOC attribute in a PDEF 1.x file.

DESCRIPTION

LOC attribute is defined only for version 2.0 and later. Though this application will read and utilize and write out the LOC attribute without any problem, we will also write out the same version number as read in. This may either cause problems for other application or if the other application ignores the LOC attributes in the PDEF file without warning the user, it may result in an unpredictable/inaccurate flow.

WHAT NEXT

Make sure that the PDEF writer that generated the file writes out correct PDEFVERSION.

PDEFP-23 (warning) There is no cluster information to write out.

DESCRIPTION

This happens when you tried to write out a pdef file and there is no cluster information for it to write out.

WHAT NEXT

Make sure to use read_pdef command or read a db file which contains cluster information.

PDEFP-24 (warning) The attribute %s %s will be not written out.

DESCRIPTION

This happens when you tried to write out a v2.0 pdef file after reading ieee pdef files.

WHAT NEXT

Try to write out a ieee pdef or change the attribute to be compatible with ieee pdef.

PDEFP-25 (warning) Obstruction size will be ignored in this

version. use CLUSTER RECT attribute to represent the obstruction size.

DESCRIPTION

In this version obstruction support is the same as the PDEF 2.0

WHAT NEXT

To represent the obstruction size, please use the cluster rect attribute. (RECT <llx> <lly> <urx> <ury>)

PDEFP-26 (warning) The pin '%s' does not exist.

DESCRIPTION

The identified pin/port cannot be found in the **current_design**. The pin/port will be ignored.

WHAT NEXT

Check to see why the pin identified in the message was listed in the PDEF file.

PDEFP-27 (warning) All the warnings will not print out when using -quiet.

DESCRIPTION

When -quiet option is used, then all the warning messages will not be printing out.

WHAT NEXT

remove -quiet to get all the warnings.

PDEFP-28 (error) The PDEF file does not contain core area data

for the design '%s'.

DESCRIPTION

It is required to have the core area description for physical synthesis. This message indicates either the core area description in the PDEF file is not in the right format or it is missing. The core area is expected in the following format: (CORE_AREA <number number number number>) The first two numbers are lower left coordinates and the last two numbers are upper right coordinates.

The core area must be either in CLUSTERFILE or in the first CLUSTER. For example A: (CLUSTERFILE (PDEFVERSION "3.0") (DESIGN ctl_v) (DATE "Wed Nov 18 18:56:48 PST 1998") (VENDOR "SYNOPSYS") (PROGRAM "CONVERTER") (VERSION "1998.02") (DIVIDER /) (PIN_DELIMITER /) (BUS_DELIMITER [ ]) (NETLIST_TYPE VERILOG) (DISTANCE_UNIT 0.01) (CORE_AREA 0 0 1728 15000)

For example B: (CLUSTERFILE (PDEFVERSION "3.0") (DESIGN ctl_v) (DATE "Wed Nov 18 18:56:48 PST 1998") (VENDOR "SYNOPSYS") (PROGRAM "CONVERTER") (VERSION "1998.02") (DIVIDER /) (PIN_DELIMITER /) (BUS_DELIMITER [ ]) (NETLIST_TYPE VERILOG) (DISTANCE_UNIT 0.01) (CLUSTER TOP (CORE_AREA 0 0 1728 15000))

WHAT NEXT

Make sure the core area is in proper format in the PDEF file.

PDEFP-29 (warning) Ignore unknown orientation '%s'.

DESCRIPTION

This message indicates the orientation value is not according to the PDEF orientation. They are one of those following: "0","0-mirror", "90","90-mirror", "180","180-mirror", "270","270-mirror"

WHAT NEXT

Use the PDEF orientation enumeration.

PDEFP-30 (warning) Cells could be moved out of boundary.

DESCRIPTION

You receive this warning because the floorplan description contains move bounds descriptions. These specify that the placement of some cells should be constrained to be within the area specified by the move bounds. The move bounds constraint is read and stored in the design, however the coarse placer might place the cells

included in the move bound outside the move bounds area. This would occur if the placement engine was trying to resolve timing or congestion costs which would force the cells to be placed outside the desired area. This warning does not suggest that this will happen, it is merely reminding you that this might happen.

WHAT NEXT

Run write_pdef or run report_cell -physical on cells in the cluster to examine their placement after coarse placement or legalization. Check to see that your cells have been placed where you desire.

PDEFP-31 (warning) The net instance '%s' does not exist.

DESCRIPTION

The identified net instance cannot be found in the hierarchy beneath **current_design**. The instance will be ignored.

WHAT NEXT

Check to see why the net instance identified in the message was listed in the PDEF file.

PDEFP-32 (warning) The net instance '%s' has already been listed under cluster '%s'; this previous classification will be overwritten.

DESCRIPTION

This message indicates that the identified net instance was previously listed as part of another cluster. The previous association is ignored. Only the most recent cluster association (that is, the cluster association furthest down in the file) will be preserved.

WHAT NEXT

Investigate the reason why the net instance was listed in more than one cluster, and correct any errors.

PDEFP-33 (warning) This obstruction becomes placement obstruction. Obstruction size will be ignored for placement

obstruction. use CLUSTER RECT and CLUSTER X_BOUNDS/ Y_BOUNDS attribute to represent the obstruction size.

DESCRIPTION

Though the OBSTRUCTION construct is syntactically correct, the size from this construct is ignored. Instead, the size from the parent cluster in which this construct is found, will be used to assign the size to this obstruction. RECT and X_BOUNDS/Y_BOUNDS from the parent cluster are used to arrive at the size of this obstruction.

WHAT NEXT

To represent the obstruction size, please use the cluster rect attribute. (RECT <llx> <lly> <urx> <ury>) (X_BOUNDS <llx> <urx>) (Y_BOUNDS <lly> <ury>)

PDEFP-34 (information) Cell '%s' of a '%s' is converted into a physical cell.

DESCRIPTION

This happens when the cell does not exist in the netlist but exist in the physical library. This conversion only happens using -allow_physical_cells in the read_pdef command.

WHAT NEXT

Make sure if the cell is a real physical cell by checking the gate existing in the physical library but not in the logical library.

PDEFP-35 (Error) The physicall cell '%s' can not be generated because it is missing either FIXED_PLACEMENT attribute, GATE_NAME attribute , or location.

DESCRIPTION

The identified physical cell instance cannot be created because it requires to have fixed_placement and location. Also it requires GATE_NAME attribute. This gate name should be the one used in the physical library.

WHAT NEXT

Check to see why the cell instance identified in the message was listed in the PDEF file.

PDEFP-36 (Error) This layer '%s' is not defined in the LAYER_DEF section.

DESCRIPTION

The message indicates that this layer is not defined in the LAYER_DEF. This VIA_RECT will be ignored because of that.

WHAT NEXT

Add this missing layer_name into LAYER_DEF section. Forexample (LAYER_DEF (LAYER <missing_layer_name> <positive_number>) ...)

PDEFP-37 (warning) The PNET instance '%s' exists in the netlist.

DESCRIPTION

This warning means that the specified PNET instance exists in the netlist below the current design in the hierarchy. The instance will be transferred to NET construction from PNET construction in the PDEF file. In the PDEF file, NET construction is for logical nets and PNET construction is for physical nets.

WHAT NEXT

Run the **get_nets** command to see if there is already a net with the specified name. If you want to define the PNET, use a unique name. PNET can be defined in the PDEF file or created using the **create_net** command.

SEE ALSO

create_net (2), **get_nets** (2).

PDEFP-38 (warning) The site array has been defined more than

once.

DESCRIPTION

You receive this warning message because the site array read into the PDEF file has been defined more than once. You can define a site array only once, either in the cluster or in the design.

WHAT NEXT

Remove one of the site array definitions and reexecute the **read_pdef** command.

SEE ALSO

create_site_row (2), **get_site_row** (2), **ignore_site_row** (2), **remove_site_row** (2).

PDEFP-39 (Error) Cell information not present

DESCRIPTION

You get this error because you are trying to access the cell information that is either not loaded or removed from memory.

WHAT NEXT

Use -load_pdef option of report_cell_displacement command to load the cell information again.

SEE ALSO

report_cell_displacement (2)

PDEFP-40 (Error) The pdef data is not read properly

DESCRIPTION

You get this error when the data that is loaded using report_cell_displacement is not proper.

WHAT NEXT

Please check the input pdef file that is given as input to report_cell_displacement

command.

SEE ALSO

report_cell_displacement(2)

PDEFP-41 (Warning) No change in placement information.

DESCRIPTION

You get this warning when you try to compare the two placement information which are identical.

WHAT NEXT

Some placement changes should be there to see the report on report_cell_displacement command.

SEE ALSO

report_cell_displacement(2).

PDEFP-42 (Error) The physical cell '%s'cannot be generated as its reference '%s' does not exist in the physical library

DESCRIPTION

You get this error if your PDEF file uses a physical_only cell that does not have a corresponding model in the physical library.

WHAT NEXT

Check that the reference (GATE_NAME attribute) of the physical_only cell in your PDEF is present in the physical library.

PDEFP-43 (warning) No orientation found for the cell '%s'.

Assigning the default orientation '%s'.

DESCRIPTION

You get this warning when the cell mentioned in the warning message has location specified in the pdef file, but not orientation. The default orientation, mentioned in the warning message, is assigned to the cell.

WHAT NEXT

If the default orientation is not acceptable, you must specify the ORIENT statement in CELL definition in the pdef file and read the pdef again. If the default orientation is acceptable, then you can continue with no changes made.

PDEFP-44 (information) Found program version '%s' from the PDEF file. Port shapes are considered to be relative to the corresponding port locations and are converted to be internally relative to the origin of the containing object.

DESCRIPTION

This message advises you that during execution of the **read_pdef** command. It occurs when reading a Physical Design Exchange Format (PDEF) file that contains the VERSION construct with one of the following sets of strings:

2001.08 (plus all variants)

2002.05

2002.05-1, 2002.05-2, 2002.05-2-RH7, 2002.05-3,

2002.05-3-RH7, 2002.05-4, 2002.05-4-RH7

For example, your PDEF file might contain the following statements:

```
(VENDOR "Synopsys, Inc" )
(PROGRAM "Design Compiler" )
(VERSION "2002.05-4" )
```

This allows the tool to identify PDEFs written by older releases of the tool. In these versions, the PDEF described the top level ports as PIN constructs with RECT statements using relative XY coordinates. The values of the coordinates are specified relative to the origin of the PIN. In later releases of the tool, the PDEF uses absolute coordinates to specify the PIN RECT statements. The values of the

coordinates are specified relative to the chip origin at (0,0).

EXAMPLE

Old style (incorrect)

```
(PIN data_1
(LOC 300 400)
(RECT -10 -20 30 40)
(LAYER 23)
  )

(PIN data_1
(LOC 300 400)
(RECT 290 380 330 440)
(LAYER 23)
  )
```

If you inadvertently read in an old version PDEF, you would be annotating incorrect coordinates for your top level ports. By identifying the older versions, the **read_pdef** command then automatically converts the PIN RECT coordinates from a relative to an absolute coordinate system before storing it onto your design .db database.

WHAT NEXT

This is only an informational message. No action is required. However, if your input PDEF contains relative coordinates to describe the PIN RECT statements, ensure that the VERSION construct uses one of the string values described above.

If your input PDEF contains absolute coordinates to describe the PIN RECT statements, ensure that the VERSION construct does not use one of the string values described above. For example (VERSION "2002.05-SP1") will not invoke the translation step.

You can use a text editor to change the PDEF VERSION value if necessary.

PDEFP-45 (warning) %s at or near token '%s'.

DESCRIPTION

A lexical or syntactic warning message.

WHAT NEXT

This is a warning message only. No action is required on your part. Check the line and the token indicated in the message, and be aware of the problem.

PDEFP-46 (Warning) The design name '%s' in input PDEF file dose not match the current design name '%s'.

DESCRIPTION

You receive this warning message because the design name in input PDEF file does not match the current design name.

WHAT NEXT

Make sure that the PDEF is loaded to the correct design.

PDEFP-47 (warning) A negative VIA number was specified in via_ref.

DESCRIPTION

A negative VIA number was specified. The via_ref section will be ignored.

WHAT NEXT

Modify the PDEF file to define VIA number positive.

PDEFP-48 (Error) This layer '%d' is not defined in the LAYER_DEF section.

DESCRIPTION

The message indicates that this layer is not defined in the LAYER_DEF. This VIA_RECT will be ignored because of that.

WHAT NEXT

Add this missing layer_name into LAYER_DEF section. Forexample (LAYER_DEF (LAYER <missing_layer_name> <positive_number>) ...)

PDIN-1 (warning) Ignore '%s'.

DESCRIPTION

This PDEF syntax is ignored.

WHAT NEXT

PDIN-2 (warning) Ignore '%s'.

DESCRIPTION

Probably it does not have the right parameters. The parser will not process its value. This happens specially reading SYNOPSYS defined attributes: 1. (DEF_CONVERSION_FACTOR <number>) example: (DEF_CONVERSION_FACTOR 1000) It describes 1000 as DEF CONVERSION FACTOR.

2. (SITE <site_name> "<origin_x origin_y>" "<H|V>" "<orientation>" "<space>" "<site width>" "<number of sites>") example: (SITE core "0 0" "H" "0-mirror" "0.8" "0.8" "100") It defined a horizontal row using 100 of site "core" starting (0,0). The width of the site is 0.8. There is no space between site. NOTE: <space> means distance from the lower left corner of a site to the next lower left corner of a site.

3. (SITE <row name> <site name> "<origin_x origin_y>" "<H|V>" "<orientation>" "<space>" "<site width>" "<number of sites>") This is the same as 2 except has additional row name.

4. (CORE_AREA <number number number number>) example: (CORE_AREA 100 100 200 200) The first two numbers are lower left coordinates of the core area. The last two numbers are upper right coordinates of the core area.

5. (LAYER_WIDTH <layer_id> <wire_width>) example: (LAYER_WIDTH 2 10.0) The layer_id is defined in the LAYER_DEF section. The wire width specified the wire width on that layer.

6. (LAYER_SPACING <layer_id> <space>) example: (LAYER_SPACE 2 10.0) The layer_id is defined in the LAYER_DEF section. The space specified the edge-to-edge separation on that layer.

7. (LAYER_SPACING_RANGE <layer_id> <minspace> <maxspace>) example: (LAYER_SPACE 2 10.0 100.0) It is like LAYER_SPACING except here specifying a range.

8. (VIA_PATTERN "<pattern_name>") example: (VIA_PATTERN "cut_layer111_$$_cut_layer222") This attribute is to describe the VIA pattern name.

9. (VIA_RECT <layer_name> "llx lly urx ury") example: (VIA_RECT METAL1 "-20 -20 20 20") This attribute is to describe a via rectangle on a specific layer.

WHAT NEXT

Edit your input PDEF file.

PDIN-3 (warning) Ignore '%s'.

DESCRIPTION

This message indicates that the attribute is not in the right context. This happens specially reading SYNOPSYS defined attributes: 1. (DEF_CONVERSION_FACTOR <number>) should be in the CLUSTERFILE context. example: (CLUSTERFILE (PDEFVERSION "IEEE 1481-1998") (DESIGN "the_design") (DATE "April 6, 1999") (VENDOR "Synopsys, Inc.") (PROGRAM "Design Compiler") (VERSION "1998.02") (DIVIDER /) (PIN_DELIMITER /) (BUS_DELIMITER [ ]) (NETLIST_TYPE VERILOG) (DESIGN_FLOW " ") (DISTANCE_UNIT 0.00100000) (DEF_CONVERSION_FACTOR 1000)

2. (SITE <site_name> "<origin_x origin_y>" "<H|V>" "<orientation>" "<space>" "<site width>" "<number of sites>") It should be in either the clusterfile or in the first cluster which can represent the top. Example 1: (CLUSTERFILE (PDEFVERSION "IEEE 1481-1998") (DESIGN "the_design") (DATE "April 6, 1999") (VENDOR "Synopsys, Inc.") (PROGRAM "Design Compiler") (VERSION "1998.02") (DIVIDER /) (PIN_DELIMITER /) (BUS_DELIMITER [ ]) (NETLIST_TYPE VERILOG) (DESIGN_FLOW " ") (DISTANCE_UNIT 0.00100000) (DEF_CONVERSION_FACTOR 1000) (SITE ROW_22 tsm1site "-92000.00 85000.00" "H" "0" "800.00" "231")

example 2: (CLUSTERFILE (PDEFVERSION "IEEE 1481-1998") (DESIGN "the_design") (DATE "April 6, 1999") (VENDOR "Synopsys, Inc.") (PROGRAM "Design Compiler") (VERSION "1998.02") (DIVIDER /) (PIN_DELIMITER /) (BUS_DELIMITER [ ]) (NETLIST_TYPE VERILOG) (DESIGN_FLOW " ") (DISTANCE_UNIT 0.00100000) (DEF_CONVERSION_FACTOR 1000) (CLUSTER TOP (SITE ROW_22 tsm1site "-92000.00 85000.00" "H" "0" "800.00" "231"))

3. (SITE <row name> <site name> "<origin_x origin_y>" "<H|V>" "<orientation>" "<space>" "<site width>" "<number of sites>") This is the same as 2 except has additional row name.

4. (CORE_AREA <number number number number>) It has the same context as the SITE attribute.

NOTES: You can only describe one CORE AREA or SITE ARRAY in the PDEF file. One PDEF file represents one design. Therefore only one CORE AREA/SITE ARRAY for one PDEF file.

5. (LAYER_WIDTH <layer_id> <wire_width>) example: (LAYER_WIDTH 2 10.0) The layer_id is defined in the LAYER_DEF section. The wire width specified the wire width on that layer. This attribute can be in PNET or ROUTE. (PNET power_net (LAYER_WIDTH 2 10.0) (ROUTE (LAYER_WIDTH 2 3.4) (2 (100 299) (299 *))))

6. (LAYER_SPACING <layer_id> <space>) example: (LAYER_SPACE 2 10.0) The layer_id is

defined in the LAYER_DEF section. The space specified the edge-to-edge separation on that layer. This attribute is in PNET. (PNET power_net (LAYER_SPACING 2 100))

7. (LAYER_SPACING_RANGE <layer_id> <minspace> <maxspace>) example: (LAYER_SPACE 2 10.0 100.0) It is like LAYER_SPACING except here specifying a range. This attribute is in PNET. (PNET power_net (LAYER_SPACING_RANGE 2 10 100))

8. (VIA_PATTERN "<pattern_name>") example: (VIA_PATTERN "$cut222$cut111") This attribute is to decribe a via pattern name. This attribute is in VIA. (VIA VIA0 1 (VIA_PATTERN "$cut222$cut111"))

9. (VIA_RECT <layer_name> "llx lly urx ury") example: (VIA_RECT METAL1 "-20 -20 20 20") This attribute is to decribe a via rectangle on a specific layer. This attribute is in VIA. (VIA VIA0 1 (VIA_RECT METAL1 "-20 -20 20 20") (VIA_RECT CUT "-10 -10 10 10") (VIA_RECT METAL2 "-30 -30 30 30"))

WHAT NEXT

Edit your input PDEF file.

PDIN-4 (warning) The attribute '%s' is in relative coordinates.

DESCRIPTION

This message indicates that the attribute is under CONTENT_LOCATIONS relative effect. That means the numbers in the attribute represents relative coordinates. It is relative to the cluster origin. If there is no cluster origin then it is relative to cluster RECT/BOUNDS.

This happens specially reading SYNOPSYS defined attributes:

2. (SITE <site_name> "<origin_x origin_y>" "<H|V>" "<orientation>" "<space>" "<site width>" "<number of sites>") For Example : defining a row that is relative to cluster origin (10 10).

example 1: (CLUSTER TOP (CONTENT_LOCATIONS relative) (ORIGIN 10 10) (SITE ROW_22 tsm1site "100.00 100.00" "H" "0" "800.00" "231")) This is the same as the following description: (CLUSTER TOP (SITE ROW_22 tsm1site "110 110" "H" "0" "800.00" "231"))

4. (CORE_AREA <number number number number>) For example: defining a core area that is relative to cluster origin (10 10)

example 1: (CLUSTER TOP (CONTENT_LOCATIONS relative) (ORIGIN 10 10) (CORE_AREA 100 100 200 200)) This is the same as the following description: (CLUSTER TOP (CORE_AREA 110 110 210 210)

WHAT NEXT

They can be in CLUSTERFILE context. Then there is no relative coordinates.

PDIN-5 (warning) The attribute '%s' is in absolute coordinates.

DESCRIPTION

This message indicates that the attribute is using chip origin (0,0). That means the numbers in the attribute represents absolute coordinates.

These attributes are the following:

2. (SITE <site_name> "<origin_x origin_y>" "<H|V>" "<orientation>" "<space>" "<site width>" "<number of sites>") For example, "110 110" are absolate coordinates. This is the same as the following description: (CLUSTER TOP (SITE ROW_22 tsm1site "110 110" "H" "0" "800.00" "231"))

4. (CORE_AREA <number number number number>) For example: (110 110) (210 210) are absolate coordinates. This is the same as the following description: (CLUSTER TOP (CORE_AREA 110 110 210 210)

WHAT NEXT

Edit your input PDEF file.

PDIN-6 (warning) The attribute '%s' is treated as a user attribute.

DESCRIPTION

This message indicates that this attribute will be ignored. The user attributes are simply read in and get written out.

WHAT NEXT

PDIN-7 (warning) Inherited cluster attributes are not supported.

DESCRIPTION

This message indicates that cluster will not inherit its parent cluster attributes. The location attributes(RECT,X_BOUNDS and YBOUNDS), size attributes (MAX_HALF_PERIMETER, MAX_X_PERIMETER, and MAX_Y_PERIMETER will not be inherited from the parent cluster. The obstruction attribute will not be inherited from its child clusters.

WHAT NEXT

Add the cluster attributes to the cluster itself.

PDIN-8 (error) Duplicate EEQ_MACRO_REF '%s'.

DESCRIPTION

You receive this error message because more than one EEQ_MACRO_REF statement is defined for a cell in the PDEF file. The flow allows only one EEQ_MACRO_REF statement for a cell definition. This error message is the result of commands that read the PDEF file such as **read_pdef**.

WHAT NEXT

Delete the duplicate EEQ_MACRO_REF statement from the cell definition in the PDEF file.

PDIN-9 (error) EEQ_MACRO_REF '%s' has no definition in physical libraries.

DESCRIPTION

You receive this error message because the EEQ_MACRO_REF has no definition in the physical libraries provided. The cell should have a reference in the physical library. This error message is the result of commands that read the PDEF file such as **read_pdef**.

WHAT NEXT

Include the physical library which has the definition for the cell.

PGRT-001 (error) Invalid pin access edge range.

DESCRIPTION

You have specified negative value in the option "-protect_pin_access_edge_within_range". The command failed.

WHAT NEXT

Check the command syntax.

SEE ALSO

set_preroute_drc_strategy(2)

PGRT-002 (error) Options '%s' and '%s' are mutually exclusive.

DESCRIPTION

These two options are mutually exclusive. The command failed.

WHAT NEXT

Check the command syntax, select one of the options.

SEE ALSO

create_rectilinear_rings(2)
set_preroute_drc_strategy(2)

PGRT-003 (error) Layer specified by the option '%s' not found.

DESCRIPTION

Layer specified by the option not found in DB. The command failed.

WHAT NEXT

Check the command syntax.

SEE ALSO

create_pad_rings(2)
create_power_straps(2)
create_preroute_vias(2)
create_rectangular_rings(2)
create_rectilinear_rings(2)
preroute_instances(2)
preroute_standard_cells(2)
set_preroute_drc_strategy(2)
set_preroute_special_rules(2)

PGRT-004 (warning) Layer specified by the option '%s' is not routing metal layer.

DESCRIPTION

Layer specified by the option is not routing metal layer. It is automatically replaced by default value.

WHAT NEXT

Check the option, and, if you need other than default layer, change the value.

SEE ALSO

set_preroute_drc_strategy(2)

PGRT-005 (error) No nets specified in the option '%s'.

DESCRIPTION

At least one net should be specified if you use this option. The command failed.

WHAT NEXT

Check the command syntax.

SEE ALSO

set_preroute_drc_strategy(2)

PGRT-006 (error) No nets match to the pattern specified by the option '%s'.

DESCRIPTION

At least one net should match to the pattern specified by this option. The command failed.

WHAT NEXT

Check the option; use the command '**get_nets** -all ...' to validate the pattern.

SEE ALSO

create_pad_rings(2)
create_rectangular_rings(2)
create_rectilinear_rings(2)
create_straps(2)
get_nets(2)
preroute_instances(2)
preroute_standard_cells(2)
set_preroute_drc_strategy(2)
slot_wire(2)

PGRT-007 (error) Memory allocation error in function '%s'.

DESCRIPTION

The function could not allocate memory for internal data.

WHAT NEXT

Check if the host has enough memory to process your design. If you think the design should work with this amount of memory, please contact the Synopsys Support Center for assistance.

PGRT-008 (error) Internal error (return code of function '%s' = %d).

DESCRIPTION

The function returned the code, which is not expected. The command failed.

WHAT NEXT

This is an internal error. Please, check if there are no other errors which might obviously cause this situation. If you find something, try to fix it to get a workaround. Anyway, that should not happened. Please contact the Synopsys Support Center for assistance.

PGRT-009 (error) Command '%s' failed.

DESCRIPTION

The command failed.

WHAT NEXT

There should be other error message(s) preceding to this, which describe a reason of the failure. Please fix them and re-run.

PGRT-010 (error) '%s' requires the option '%s'.

DESCRIPTION

In this case the option is mandatory.

WHAT NEXT

Check the command syntax.

SEE ALSO

create_pad_rings(2)
create_rectangular_rings(2)
create_rectilinear_rings(2)
preroute_instances(2)
set_preroute_special_rules(2)

PGRT-011 (error) Length of the pattern specified by the option

'%s'/n is longer than %d bytes. .

DESCRIPTION

The pattern is too long. The command failed.

WHAT NEXT

Check the command syntax. Try to optimize the pattern using regular expressions.

SEE ALSO

preroute_standard_cells(2)

PGRT-012 (warning) Invalid syntax of rectangle specified in the option '%s'.

DESCRIPTION

A rectangle must be specified in the form {{*llx lly*} {*urx ury*}}. The ignored, default area will be used instead.

WHAT NEXT

Check the command syntax.

SEE ALSO

create_preroute_vias(2)
preroute_standard_cells(2)

PGRT-013 (error) Invalid syntax of the option '%s'.

DESCRIPTION

Invalid syntax of the value specified by the option. The command failed.

WHAT NEXT

Check the command syntax.

SEE ALSO

create_rectangular_rings(2)
create_rectilinear_rings(2)
set_preroute_advanced_via_rule(2)
set_preroute_special_rules(2)
slot_wire(2)

PGRT-014 (error) Contact code specified by the option '%s' not found.

DESCRIPTION

Contact code specified by the option not found in DB. The command failed.

WHAT NEXT

Check the command syntax; check list of contacts in the technology file.

SEE ALSO

set_preroute_advanced_via_rule(2)

PGRT-015 (error) Cut layer specified by the option '%s' not found.

DESCRIPTION

Layer specified by the option either not found in DB or is not cut layer. The command failed.

WHAT NEXT

Check the command syntax; check list of layers in the technology file.

SEE ALSO

set_preroute_advanced_via_rule(2)

PGRT-016 (error) Invalid layer '%s' specified in the option '%s'.

DESCRIPTION

Wrong layer is specified in the option. The command failed.

WHAT NEXT

Check the command syntax; check list of layers in the technology file.

SEE ALSO

create_power_straps(2)
create_preroute_vias(2)
create_rectangular_rings(2)
preroute_instances(2)
set_preroute_special_rules(2)
slot_wire(2)

PGRT-017 (error) No cells match to the pattern specified by the option '%s'.

DESCRIPTION

At least one cell should match to the pattern specified by this option. The command failed.

WHAT NEXT

Check the option; use the command '**get_cells**' to validate the pattern.

SEE ALSO

create_rectangular_rings(2)
create_rectilinear_rings(2)
get_cells(2)
preroute_instances(2)

PGRT-018 (warning) Option '-undo' overrides all other options.

DESCRIPTION

The option '-undo' specified along with others. All other options ignored.

WHAT NEXT

Check the command syntax.

SEE ALSO

create_power_straps(2)
create_preroute_vias(2)
create_rectangular_rings(2)
create_rectilinear_rings(2)
preroute_instances(2)

PGRT-019 (error) Option '%s' is not specified.

DESCRIPTION

The option is mandatory for this command. The command failed.

WHAT NEXT

Check the command syntax.

SEE ALSO

create_power_straps(2)
create_rectilinear_rings(2)
set_preroute_special_rules(2)

PGRT-020 (error) Set of special rules '%s' specified by the option '%s' not found.

DESCRIPTION

The option refers to a set of special rules which is not found. The command failed.

WHAT NEXT

Check the command syntax. Rules has to be pre-set by the command / fBset_preroute_special_rules.

SEE ALSO

create_power_straps(2)
preroute_instances(2)

set_preroute_special_rules(2)

PGRT-021 (error) Distributed routing failed: %d CPUs requested, but %s

DESCRIPTION

The command cannot run in distributed routing mode using current settings. The command failed.

WHAT NEXT

Check the current settings.

SEE ALSO

create_power_straps(2)
preroute_standard_cells(2)

PGRT-022 (error) The layer %s specified by the option %s is out the range specified by the command **set_preroute_drc_strategy**

DESCRIPTION

The layer should be within the range. The command failed.

WHAT NEXT

Check the options and change either the layer or the range specified by the command **set_preroute_drc_strategy**.

SEE ALSO

create_power_straps(2)
create_preroute_vias(2)
create_rectangular_rings(2)
preroute_instances(2)
set_preroute_drc_strategy(2)
set_preroute_special_rules(2)

PGRT-023 (error) The option %s is omitted but no %s layers found in the range specified by the command **set_preroute_drc_strategy**

DESCRIPTION

The command cannot set default layer within the range. The command failed.

WHAT NEXT

Check the options and change either the layer or the range specified by the command **set_preroute_drc_strategy**.

SEE ALSO

create_power_straps(2)
create_preroute_vias(2)
create_rectangular_rings(2)
preroute_instances(2)
set_preroute_drc_strategy(2)
set_preroute_special_rules(2)

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PGRT-024 (error) The target layer is the same as the source layer.

The layers should differ. The command failed.

Check the options -from_layer and -to_layer.

create_preroute_vias(2)
set_preroute_drc_strategy(2)

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PGRT-025 (error) The %s route type is not specified.

Neither option specifying the objects by their route type are set. The command failed.

Check the options syntax.

create_preroute_vias(2)

PGRT-026 (warning) failed to create ring %s %s.

DESCRIPTION

Command create_rectilinear_rings failed to create ring around the reported area.

WHAT NEXT

Check the command options. If there is enough space, changing offset(s) and/or increasing the value of "-max_deviation" might help.

SEE ALSO

create_rectilinear_rings(2)

PGRT-027 (error) No shapes match to the pattern specified by the option '%s'.

DESCRIPTION

At least one shape should match to the pattern specified by this option. The command failed.

WHAT NEXT

Check the option; use the command '**get_net_shapes**' to validate the pattern.

SEE ALSO

create_preroute_vias(2)
get_net_shapes(2)

PGRT-028 (warning) The shape(object_id: %d) is not in specified nets.

DESCRIPTION

The shapes should be in specified nets. The command failed.

WHAT NEXT

Check if shape belong to the nets specified in -nets option.

SEE ALSO

create_preroute_vias(2)
get_net_shapes(2)

PGRT-029 (error) Macro pin layer is not specified through special rules.

DESCRIPTION

The command **create_power_straps** is required to create straps over pins of macro cells, but the layer of those pins is not specified. The command failed.

WHAT NEXT

Specify the layer using the command **set_preroute_special_rules** and refer to the rules set by its name using the option "-special_rules" of the command **create_power_straps**.

SEE ALSO

create_power_straps(2)
set_preroute_special_rules(2)

PH

PH-001 (warning) Cell %s doesn’t have ph cell, wont be in a cluster.

DESCRIPTION

WHAT NEXT

PH-002 (warning) Hier cell %s doesn’t have ph cell and will not be placed as a hierarchy.

DESCRIPTION

WHAT NEXT

PH-003 (warning) Hier cell %s doesn’t have core area and will not be placeds as a hierarchy.

DESCRIPTION

WHAT NEXT

PH-004 (warning) Hier cell %s doesn’t have cluster created and will not be placed as a hierarchy.

DESCRIPTION

WHAT NEXT

PLAI-1 (error) Can’t read file "%s

DESCRIPTION

WHAT NEXT

PLAI-2 (error) Illegal command at line %d.

DESCRIPTION

WHAT NEXT

PLAI-3 (error) Port %s declared twice at line %d.

DESCRIPTION

WHAT NEXT

PLAI-4 (warning) Unknown value ’%s’ for .phase keyword.

Positive phase will be used for all outputs.

DESCRIPTION

WHAT NEXT

PLAI-5 (warning) Unknown PLA type "%s

DESCRIPTION

WHAT NEXT

PLAI-6 (warning) Unknown command "%s

DESCRIPTION

WHAT NEXT

PLAI-7 (error) Design name must be specified at line %d.

DESCRIPTION

WHAT NEXT

PLAI-8 (error) Ports incompletely specified at line %d.

DESCRIPTION

WHAT NEXT

PLAI-9 (error) Mismatched number of inputs.

DESCRIPTION

WHAT NEXT

PLAI-10 (error) Mismatched number of outputs.

DESCRIPTION

WHAT NEXT

PLAI-11 (error) No product terms for PLA found in file.

DESCRIPTION

WHAT NEXT

PLAI-12 (error) ON-set and OFF-set overlap.

DESCRIPTION

WHAT NEXT

PLAI-13 (error) Mismatched number of outputs and phase values.

Positive phase will be used for all outputs.

DESCRIPTION

WHAT NEXT

PLAI-14 (error) Invalid character on or near line %d.

DESCRIPTION

WHAT NEXT

PLAI-15 (error) Unknown port '%s' in .field statement at line %d.

DESCRIPTION

WHAT NEXT

PLAI-16 (error) Invalid order of input and output ports at '%s' at line %d.

DESCRIPTION

WHAT NEXT

PLAI-17 (error) The use of the percent operator has resulted in

an ambiguous specification.

DESCRIPTION

WHAT NEXT

PLAI-18 (warning) Ignoring row at line %d since previous row(s) containing the percent operator cover all input conditions implied by this row.

DESCRIPTION

WHAT NEXT

PLAI-19 (error) Ambiguous output values specified at lines %d and %d.

DESCRIPTION

WHAT NEXT

PLAI-20 (error) Port %s declared twice.

DESCRIPTION

WHAT NEXT

PLAO

PLAO-0 (error) Design is currently not represented as a PLA.

DESCRIPTION

WHAT NEXT

PLAO-1 (error) Cells at the current level of the design are not combinational.

DESCRIPTION

WHAT NEXT

PLMGR-01 (Error) The tluplus files are not set in this scenario '%s'. The RC values will be zero.

DESCRIPTION

In MCMM, you need to use set_tlu_plus_files in every scenrio. It could be from the set_tlu_plus_files command or from previously setting stroed in the design. If missing the setting, then your RC will be all zeros.

WHAT NEXT

Use set_tlu_plus_files command to set the files.

EXAMPLE MESSAGE

Warning: The tluplus files are not set in this scenario A. THe RC values will be ze ro. (PLMGR-01)

SEE ALSO

set_tlu_plus_files (2), **report_tlu_plus_files** (2),

PLMGR-02 (Info) RCs will be annoated for scenario '%s', %s corner.

DESCRIPTION

The message is to tell you which corner(max/min) in which scenario, the RCs will be annoated on.

WHAT NEXT

Use read_parasitics command to read the file.

EXAMPLE MESSAGE

SEE ALSO

read_parasitics (2), **report_scenario(2),**

PLMGR-03 (Info) Scenario '%s', %s corner has not been udpated yet.

DESCRIPTION

The message is to tell you which corner(max/min) in which scenario still need to be annoated.

WHAT NEXT

Use read_parasitics command to read the file.

EXAMPLE MESSAGE

SEE ALSO

read_parasitics (2), **report_scenario(2),**

PLMGR-04 (Error) Can not support some scenario has emulation tluplus but other not.

DESCRIPTION

The message is to tell you set emulation tluplus files in some scenario but not all scenarios. Currently we can not support partial setting.

WHAT NEXT

Use report_tlu_plus_files command to check the setting.

EXAMPLE MESSAGE

SEE ALSO

set_tlu_plus_files (2), **report_tlu_plus_files(2),**

PNA-001 (error) Design is not open.

DESCRIPTION

No Milkyway cell is open. The command is supposed to operate on the currently opened cell.

WHAT NEXT

Open the design you want the command to act on.

PNA-002 (error) Cannot specify this option together with '-layer', '-ring_nets', or '-global' option.

DESCRIPTION

The current option and '-layer', '-ring_nets', or '-global' option. cannot be specified together. They may be multually exclusive or have dependency between each other.

WHAT NEXT

Specify the current option in a seperate command.

PNA-003 (error) In order to use this option, %s option must be specified.

DESCRIPTION

The entered option has a dependency on the option %s.

WHAT NEXT

Please also specify option %s.

PNA-004 (error) Design name is not found.

DESCRIPTION

WHAT NEXT

PNA-005 (error) No top-level pins are connected to net %s logically.

DESCRIPTION

When the option *-use_pin_as_pads* is specified in PNA/PNS, the tool will first check the logic connectivity of the top-level P/G pins. If no P/G pins, or the P/G pins are not connected to the synthesized net(s), PNA/PNS will not be able to proceed using them as pads.

Another possible reason for this error is that the port type of the top-level pins is not "POWER" or "GROUND".

WHAT NEXT

Please set the port type of P/G pins to "POWER" or "GROUND". Then, use *derive_pg_connection* command to connect the top-level pin to the synthesized nets.

SEE ALSO

derive_pg_connection (2)

PNA-006 (error) All the P/G pads do not have power ports, or all the power ports are not connected to power or ground net logically.

DESCRIPTION

This error could be due to the following reasons:

(1) the specified power/ground pad master/instance cannot be found in the design.
(2) there is no power/
ground port in the specified pads or the ports are not logically connected to the a
nalyzed power/ground nets.

WHAT NEXT

Please use **derive_pg_connection** to make the logical connection, or use **create_fp_virtual_pad** command to specify virtual pads.

SEE ALSO

derive_pg_connection (2)
create_fp_virtual_pad (2)

PNA-007 (error) No existing core rings for net %s. Power network synthesis fails to extend straps to existing core ring.

DESCRIPTION

By default if -skip_ring option in the command set_fp_rail_constraints was set, PNS extends synthesized straps to existing core ring. However, if there is no core ring in the design, PNS is unable to extend the straps.

WHAT NEXT

Please apply any of the followings. (1) Synthesize also the core ring by using set_fp_rail_constraints -set_ring (2) Extends synthesized straps to boundary or pad ring by using set_fp_rail_constraints -extend_strap boundary or set_fp_rail_constraints -extend_strap pad_ring (3) Create core ring by using the Preroute command create_rectangular_rings

SEE ALSO

set_fp_rail_constraints (2)
synthesize_fp_rail (2)
create_rectangular_rings (2)

PNA-008 (error) Cannot find net %s in the design.

DESCRIPTION

There is no specified net in the design. You can also use the following command and option to check if the net is in the design.

get_net -all *net_name*

WHAT NEXT

Please apply any of the followings.

(1) Add the specified net in the database

(2) Specify the correct PG net name.

SEE ALSO

get_net (2)

PNA-009 (error) Cannot obtain technology information.

DESCRIPTION

PNA/PNS is unable to get technology information in the MilkyWay database.

WHAT NEXT

Please check if the technology file was set by using

write_mw_lib_files -technology -output *tech_file_name library_name*

Please set technology file by using

set_mw_technology_file

SEE ALSO

set_mw_technology_file (2)
write_mw_lib_files (2)

PNA-010 (error) All synthesized straps are removed due to blockage.

DESCRIPTION

During DRC checking stage, all the synthesized straps are removed. Please check the following:

(1) Any big routing blockages in the design?
(2) Any existing power/
ground straps in the design that use different routing direction than the synthesized ones?

(3) The die size is too small for the given strap layer constraints?

WHAT NEXT

Reduce the strap number, or change strap width/direction/layer, use the global constraints '-ignore_blockages', resize the region for PNS.

SEE ALSO

set_fp_rail_constraints (2)

PNA-011 (error) Power network synthesis cannot synthesize more than two nets.

DESCRIPTION

PNS synthesizes only one power and one ground nets.

WHAT NEXT

Please specify one power and/or one ground nets for power network synthesis.

SEE ALSO

synthesize_fp_rail (2)

PNA-012 (error) Cannot find any power/ground nets in the design.

DESCRIPTION

The net names are missing for setting MVDD PNS constraints.

WHAT NEXT

Please set the net names by using

set_fp_rail_voltage_area_constraints -voltage_area *VA_name -voltage_supply supply_voltage -nets net_names*

SEE ALSO

set_fp_rail_voltage_area_constraints (2)

PNA-013 (error) Layer %s has zero resistance.

DESCRIPTION

There is zero unit resistance defined in the technology file, causing PNA/PNS is unable to perform PG extraction.

WHAT NEXT

PNA-014 (error) Cannot find layer %s from the technology file.

DESCRIPTION

The specified layer is not defined in MilkyWay database.

WHAT NEXT

Plese use the command "get_layer" to list all the layers and check if the specified layer in in the list.

SEE ALSO

get_layer (2)

PNA-015 (error) Cannot find layer %d from the technology file.

DESCRIPTION

The specified layer ID is not defined in MilkyWay database.

WHAT NEXT

Plese use the command "get_layer" to list all the layers and check if the layer with the specified layer Id is in the list.

SEE ALSO

get_layer (2)

PNA-016 (error) No power/ground port of %s is connected to net %s logically.

DESCRIPTION

Before running PNA/PNS, instances in the design should be connected to the synthesized P/G nets logically. In this error, no P/G port of standard cell instance or hard macro is connected to the synthesized net(s).

WHAT NEXT

Please use *derive_pg_connection* command to connect instances to the synthesized P/G net(s).

SEE ALSO

derive_pg_connection (2)

PNA-017 (error) Cannot load power network analysis results for net %s.

DESCRIPTION

After PNA or PNS is done, highlight files named <design_name>.<net_name>.pw_hl.pna will be created in the ./pna_output dierctory. These file are used for displaying IR/EM map. This error message shows that PNA or PNS failed such that the highlight files was not created.

WHAT NEXT

Please check the error message in the ICC log file, and then correct them accordingly.

SEE ALSO

synthesize_fp_rail (2)
analyze_fp_rail (2)
analyze_fp_rail (2)
set_fp_rail_constraints (2)
set_fp_rail_region_constraints (2)

set_fp_rail_strategy (2)
set_fp_rail_voltage_area_constraints (2)

PNA-018 (error) Not enough disk space for file %.

DESCRIPTION

By default PNA or PNS creates several files in the ./pna_output directory. The message means not enough disk space for storing these files.

WHAT NEXT

The directory used by PNA/PNS can be reset using the option -output_directory in the analyze_fp_rail (PNA) or synthesize_fp_rail (PNS) command. Please make sure the specified dierctory exists or can be created before running PNA or PNS.

SEE ALSO

analyze_fp_rail (2)
synthesize_fp_rail (2)

PNA-019 (error) Cannot open file %s.

DESCRIPTION

The specified file does not exist or is not readable.

WHAT NEXT

Please check if the correct file name was specified, or make the file readable.

PNA-020 (error) %s is not writable.

DESCRIPTION

The file cannot be written.

WHAT NEXT

Please make sure files can be created under ./pna_output directory. If not, users can change the output directory by usig the option -output_directory in the

analyze_fp_rail (PNA) or synthesize_fp_rail (PNS) command. Please make sure the specified dierctory exists or can be created before running PNA or PNS.

SEE ALSO

analyze_fp_rail (2)
synthesize_fp_rail (2)

PNA-021 (error) Cannot create directory %s.

DESCRIPTION

If the ./pna_output directory does not exist, PNA/PNS will create one. This message shows that the directory cannot be created.

WHAT NEXT

Please make sure that ./pna_output directory can be created. Users can also change the directory to be created by using the option -output_directory in the analyze_fp_rail (PNA) or synthesize_fp_rail (PNS) command.

SEE ALSO

analyze_fp_rail (2)
synthesize_fp_rail (2)

PNA-022 (error) Out of memory.

DESCRIPTION

There is not enough memory for PNA to solve matrix during IR drop simulation.

WHAT NEXT

Please switch the default matrix solver to ultra matrix solver by using set_fp_rail_strategy -pna_ultra_solver true. Note that ultra matrix solver uses less memory but longer CPU time.

SEE ALSO

set_fp_rail_strategy (2)
analyze_fp_rail (2)

PNA-023 (error) PNS region is not correctly defined.

DESCRIPTION

The PNS synthesis region defined in the region file or through mouse-click is not correct. The region can be rectangle or rectlinear region, but not self-slicing or disjoint region.

WHAT NEXT

Please redefine the region with GUI or Tcl command set_fp_rail_region_constraints.

SEE ALSO

set_fp_rail_region_constraints (2)
synthesize_fp_rail (2)

PNA-024 (error) Cannot fine voltage area %s in the design.

DESCRIPTION

The specified voltage area does not exist in the design.

WHAT NEXT

Please use the command *get_voltage_areas to list all the voltage areas and check if the specified voltage area is in the list. If not, please either specify the correct voltage area name or create voltage area by the command create_voltage_area.*

SEE ALSO

get_voltage_areas (2)
create_voltage_area (2)

PNA-025 (error) %s is not specified.

DESCRIPTION

The information %s is required for PNS/PNA to proceed.

WHAT NEXT

Please specify %s.

PNA-026 (error) The specified offset from pad to ring %.3f microns is larger than half of the design width.

DESCRIPTION

The specified ring offset is unreasonable large.

WHAT NEXT

Please use a smaller ring offset by the command and option set_fp_rail_constraints -set_ring -ring_offset *value*

SEE ALSO

set_fp_rail_constraints (2)

PNA-027 (error) The specified offset from pad to ring %.3f microns is less than the minimum %s spacing %.3f.

DESCRIPTION

The specified ring offset is smaller than the minimum spacing, which may cause DRC error between pin shapes of pads and ring segments.

WHAT NEXT

Please use a larger ring offset by the command and option set_fp_rail_constraints -set_ring -ring_offset *value*

SEE ALSO

set_fp_rail_constraints (2)

PNA-028 (error) The %s edge (%.3f %.3f) (%.3f %.3f) in PNS region is overlapped with the IO cells %s with the boundary (%.3f %.3f) (%.3f %.3f)

DESCRIPTION

PNS does not synthesize straps of the region overlapping with IO area in order to

avoid DRC erorrs.

WHAT NEXT

Please redefine the region with GUI or Tcl command set_fp_rail_region_constraints.

SEE ALSO

set_fp_rail_region_constraints (2)
synthesize_fp_rail (2)

PNA-029 (error) Cannot find %s %s in the design.

DESCRIPTION

These is no the specified objects in the design.

WHAT NEXT

Please use the following commands to check if the object is in the design.

get_mw_cels -> instance get_cells -> master get_plan_groups -> plan group

SEE ALSO

get_mw_cels (2)
get_cells (2)
get_plan_groups (2)

PNA-030 (error) The %s constraints %7.3f for layer %s is larger than the maximum allowable width %7.3f.

DESCRIPTION

PNS derives the maximum allowable width based on straps constraints and the size of the core area. The error message means that the minimum width constarints of the layer is larger than the derived maximum width, causing PNS unable to synthesize straps.

WHAT NEXT

Please set a smaller minimum width constraint by using

set_fp_rail_constraints -add_layer -layer *layer_name -direction direction -min_width*

width

SEE ALSO

set_fp_rail_constraints (2)
synthesize_fp_rail (2)

PNA-031 (error) The specified PG spacing for layer %s is larger than the maximum allowable spacing %.3f.

DESCRIPTION

The specified PG spacing is so large that PNS is unable to even synthesize straps with specified minimum strap number.

WHAT NEXT

Please specify a smaller PG spacing by using

set_fp_rail_constraints -add_layer -layer *layer_name -direction direction -min_width width -spacing value*

SEE ALSO

set_fp_rail_constraints (2)
synthesize_fp_rail (2)

PNA-032 (error) The %s constraints %7.3f for layer %s is smaller than the minimum allowable width %7.3f.

DESCRIPTION

PNS computes the minimum allowable width based on the minimum width in the technology file plus 2*via_cut_to_biundary to avoid DRC errors when power and ground straps next to each other.

WHAT NEXT

Please set a larger maximum width by using

set_fp_rail_constraints -add_layer -layer *layer_name -direction direction -max_width width*

SEE ALSO

set_fp_rail_constraints (2)
synthesize_fp_rail (2)

PNA-033 (error) No voltage area constraint is set for %s.

DESCRIPTION

PNS cannot find any power network constraint set for voltage area/design %s. User need to specify power network constraint for each voltage area in which power/ground mesh will be created.

WHAT NEXT

Please specify PNS constraints for a voltage area using the command *set_fp_rail_voltage_area_constraints.*

SEE ALSO

set_fp_rail_voltage_area_constraints (2)
report_fp_rail_voltage_area_constraints (2)

PNA-034 (error) Net name is not specified for voltage area %s.

DESCRIPTION

The name of the net to be synthesized in the voltage area %s is requried for PNS to proceed. There are two ways to specify the nets. One way is using the PNS voltage area constraits command. The other way is to use UPF. PNS can automatically obtain the primary power and ground net for a particular power domain from UPF.

WHAT NEXT

Please use the following command to specify net name in PNS voltage area constraints:

set_fp_rail_voltage_area_constraints -voltage_area *voltage_area -nets nets*

SEE ALSO

set_fp_rail_voltage_area_constraints (2)
report_fp_rail_voltage_area_constraints (2)

PNA-035 (error) Voltage supply is not specified for voltage area %s.

DESCRIPTION

The voltage supply is missing for setting MVDD PNS constraints.

WHAT NEXT

Please set the supply voltage by using

set_fp_rail_voltage_area_constraints -voltage_area *VA_name -voltage_supply supply_voltage -nets net_names*

SEE ALSO

set_fp_rail_voltage_area_constraints (2)

PNA-036 (error) Net %s is not power/ground net.

DESCRIPTION

PNA/PNS analyzes/synthesizes only for power and ground nets. The specified net is not power or ground net.

WHAT NEXT

Please specify the correct PG net names.

SEE ALSO

analyze_fp_rail (2)
synthesize_fp_rail (2)

PNA-037 (error) Cell %s.CONN has no port %s.

DESCRIPTION

There is no PG ports in the CONN view, causing PNA unable to read PG geometries stored in the CONN view.

WHAT NEXT

Please regenerate CONN view using ICC command create_connview or PrimRail.

SEE ALSO

create_connview (2)

PNA-038 (error) Cannot find net %s in %s.CONN.

DESCRIPTION

There is no analyzed net defined in the CONN view, causing PNA unable to read PG geometries stored in the CONN view.

WHAT NEXT

Please regenerate CONN view using ICC command create_connview or PrimRail.

SEE ALSO

create_connview (2)

PNA-039 (error) Fail to open cell %s.CONN.

DESCRIPTION

PNA is uanble to open the CONN view.

WHAT NEXT

Please regenerate CONN view using ICC command create_connview or PrimRail.

SEE ALSO

create_connview (2)

PNA-040 (error) Fail to read net geometry from %s.CONN.

DESCRIPTION

PNA is unable to read net geometry in the CONN view.

WHAT NEXT

Please regenerate CONN view using ICC command create_connview or PrimRail.

SEE ALSO

create_connview (2)

PNA-041 (error) No cell instances connected to net %s in the specified region.

DESCRIPTION

WHAT NEXT

PNA-042 (error) cannot write file %s.

DESCRIPTION

The file cannot be written.

WHAT NEXT

Please make sure files can be created under ./pna_output directory. If not, users can change the output directory by usig the option -output_directory in the analyze_fp_rail (PNA) or synthesize_fp_rail (PNS) command. Please make sure the specified dierctory exists or can be created before running PNA or PNS.

SEE ALSO

analyze_fp_rail (2)
synthesize_fp_rail (2)

PNA-043 (error) Power network synthesis cannot synthesize more than one power net.

DESCRIPTION

PNS can synthesize only one power and one ground nets.

WHAT NEXT

Please specify only one power net.

SEE ALSO

synthesize_fp_rail (2)

PNA-044 (error) Power network synthesis cannot synthesize more than one ground net.

DESCRIPTION

PNS can synthesize only one power and one ground nets.

WHAT NEXT

Please specify only one ground net.

SEE ALSO

synthesize_fp_rail (2)

PNA-045 (error) Cannot get preferred routing direction on layer %d.

DESCRIPTION

The preferred routing direction for the layer is not defined.

WHAT NEXT

PNA-046 (error) Ring width must be larger than %.3f microns..

DESCRIPTION

PNS calculates the minimum width based on the minimum wire width of the layer and the minimum via size from the technology file.

WHAT NEXT

Increase the ring width so it is no smaller than the minimum width.

PNA-047 (error) Ring width must be smaller than %.3f microns..

DESCRIPTION

PNS calculates the maximum ring width based on the ring width and spacing constraints, and the size of the core area.

WHAT NEXT

Reduce the ring width so it is no larger than the maximum width.

PNA-048 (error) Power is not enabled for design %s.

DESCRIPTION

PNS or PNA with "-analyze_power" option requires design with power analysis capability.

WHAT NEXT

Try to use "Link" command first or make sure power analysis related licences are included.

PNA-049 (error) The maximum strap width considering standard cell rail alignment is %g microns, and is smaller than the

specified minimum strap width %g microns at layer %s.

DESCRIPTION

PNS with -align_strap_with_m1_rail strategy will re-caculate the maximum width to avoid standard cell power (or ground) rails blocked by ground (or power) straps. The specified minimum width constraint cannot be satisfied.

WHAT NEXT

Adjust the layer width constraint as suggested.

PNA-050 (error) The straps at layer %s cannot be put inside standard cell rows to avoid standard cell rail blockage.

DESCRIPTION

PNS with -align_strap_with_m1_rail strategy will re-caculate the maximum width to avoid standard cell power (or ground) rails blocked by ground (or power) straps. The specified minimum width constraint cannot be satisfied. The maximum allowed width becomes a non-positive value considering the location of standard cell rows and power pins height, and spacing constraint.

WHAT NEXT

To flip every other cell row or increase the distance between two adjacent cell rows.

PNA-051 (error) Cannot find pin %s at layer %s.

DESCRIPTION

PNA is unable to find the switching cell pin at the specified layer.

WHAT NEXT

Please specify the correct switching cell pin and layer by using

set_attribute [get_physical_lib_cel master_name] "mtcmos_pin_layers" "pin1_name pin1_layername pin2_name pin2_layername"

PNA-052 (error) Cannot get %s net from UPF in power domain %s.

DESCRIPTION

PNS/PNA is unable to find the %s net information from UPF defined for power domain %s.

WHAT NEXT

Please check the UPF information defined for power domain %s. Or specify supply nets explicitly using **-nets** option.

SEE ALSO

set_fp_rail_voltage_area_constraints (2)

PNA-053 (error) %s must be a positive value.

DESCRIPTION

The value of %s is either negative or zero or unspecified. PNS/PNA requires this value to be positive to proceed correctly.

WHAT NEXT

Please specify a positive value for %s.

PNA-054 (error) Cannot specify both strap and pitch constraints.

DESCRIPTION

PNS cannot synthesize the P/G network based on both the number of straps and strap pitch constraints.

WHAT NEXT

Please specify either number of straps constraints or strap pitch constraints, but not both of them.

SEE ALSO

set_fp_rail_constraints (2)
set_fp_rail_voltage_area_constraints (2)

PNA-055 (error) The core area is too small for the minimum number of horizontal straps %d for layer %s

DESCRIPTION

The design is too small to fulfill the specified minimum number of horizontal straps for the specified layer constraints. Note that the default minimum number of straps is 16.

WHAT NEXT

Please decrease the minimum number of straps for the synthesized horizontal layer.

SEE ALSO

set_fp_rail_constraints (2)

PNA-056 (error) The core area is too small for the minimum number of vertical straps %d for layer %s

DESCRIPTION

The design is too small to fulfill the specified minimum number of vertical straps for the specified layer constraints. Note that the default minimum number of straps is 16.

WHAT NEXT

Please decrease the minimum number of straps for the synthesized vertical layer.

SEE ALSO

set_fp_rail_constraints (2)

PNA-057 (error) There is not enough space to synthesize core

ring.

DESCRIPTION

The design is too small such that core ring cannot be synthesized.

WHAT NEXT

Please disable core ring generation by using the following command and options: set_fp_rail_constraints -skip_ring -extend_strap boundary Or change the floorplan by increasing the die size.

SEE ALSO

set_fp_rail_constraints (2)
initialize_floorplan (2)

PNA-058 (error) Cannot specify multiple voltage area names.

DESCRIPTION

This option cannot take multiple voltage area names.

WHAT NEXT

Please use seperate command to specify for each voltage area.

SEE ALSO

set_fp_rail_voltage_area_constraints (2)
report_fp_rail_voltage_area_constraints (2)
remove_fp_rail_voltage_area_constraints (2)

PNA-059 (error) Cannot find P/G pad of net %s in the design.

DESCRIPTION

PNS fail to read in the P/G pad of net %s from the design. This could be due to the following reasons:

(1) There is no pad in the design.
(2) No pad is logically connected to net %s.

WHAT NEXT

Please check if there exists P/G pad for net %s in the design. If the P/G pads are not connected to net %s, please use the command *derive_pg_connection* to connect them. If there is no pad, please use the command *create_fp_virtual_pad* to define virtual pad for PNS.

SEE ALSO

create_fp_virtual_pad (2)
derive_pg_connection (2)

PNA-060 (error) All the pads of net %s cannot reach any power port of the leaf cells or blocks.

DESCRIPTION

PNS can find pads for net %s in the design; however, these pads are not able to connected to the cell instances through P/G network. This means the pads have been defined, but there is no direct connection between the pads and the power network. The following reasons could cause this problem:

(1) There is blockages between pads and the closest power straps.
(2) There are no cell instances in the design.
(3) Pads are connected to the nearest power strap, however that power strap cannot be connected to the cell instances in the design.
(4) The power mesh is not created successfully due to blockage or DRC violation.
(5) In MV design, other voltage areas block the connection path between pads and th e logically connected power network.
(6) In MV design, if the voltage area is a power-
down voltage area, there is no direction connection from the pads to the existing p ermanent power strap or synthesized permanent power straps. Please check the log me ssage to see if the MTCMOS alignment straps are synthesized successfully.

WHAT NEXT

Please remove the blockage between pads and power networks, or use the option -*ignore_blockage* in the *synthesize_fp_rail* command to debug. If the pads are virtual pads, please define virtual pads at a different location. In the MVDD design, please check if the pads are able to reach the voltage area. In the power-down voltage area, please check if the power switch cells are inserted and connected properly and set the alignment strategy using the command set_fp_rail_strategy -align_strap_with_mtcmos_cells.

SEE ALSO

create_fp_virtual_pad (2)
synthesize_fp_rail (2)
set_fp_rail_strategy (2)

PNA-061 (error) Voltage area name is not specified in Power Switch Array Synthesis.

DESCRIPTION

In the Power Switch Array Synthesis flow, user must specify the voltage area that is to be powerd-down.

WHAT NEXT

Please specify the voltage area name using the **-voltage_area** option.

SEE ALSO

synthesize_fp_rail (2)
set_fp_rail_voltage_area_constraints (2)

PNA-062 (error) Cannot specify more than one voltage area in Power Switch Array Synthesis.

DESCRIPTION

In the Power Switch Array Synthesis flow, user cannot specify more than one power-down voltage area.

WHAT NEXT

Please specify only one voltage area name using the **-voltage_area** option.

SEE ALSO

synthesize_fp_rail (2)
set_fp_rail_voltage_area_constraints (2)

PNA-063 (error) Cannot get the reference library cell name of

power switch for voltage area %s.

DESCRIPTION

PNS cannot find the reference library cell name (master name) of the power switch. This could be either user did not define power switch cell in UPF mode; or user did not specify the **-power_switch** option in non-UPF mode.

WHAT NEXT

Please first check if power switch cell is specified. If not, please specify it using option **-power_switch**. If power switch is already specified using the power switch name defined in UPF, it could be that PNS cannot find such power switch in the voltage area %s. Please double check UPF definition for voltage area %s.

SEE ALSO

create_power_switch (2)
set_fp_rail_voltage_area_constraints (2)

PNA-064 (error) Cannot find power switch cell %s in the library.

DESCRIPTION

PNS cannot find power switch cell %s in the library.

WHAT NEXT

Please use **get_cells** command to check if the power switch cell is in the library.

SEE ALSO

get_cells (2)
get_physical_lib_cel (2)
set_fp_rail_voltage_area_constraints (2)

PNA-065 (error) Cannot get the on-resistance of power switch cell %s.

DESCRIPTION

PNS cannot get the on-resistance of power switch cell %s. Therefore, power switch cell will not able to be synthesized in the flow and IR drop result can be very

inaccurate.

WHAT NEXT

Please specify the on-resistance for power switch cell %s using the following command:

```
set_attribute [get_physical_lib_cells <master_name>] "mtcmos_resistance"
<resistance_value>
```

SEE ALSO

synthesize_fp_rail (2)
set_fp_rail_voltage_area_constraints (2)

PNA-066 (error) The power net type of layer %s has not been defined.

DESCRIPTION

Power switch array synthesis will synthesize the permanent and virtual power nets on different metal layers in the power-down voltage area. Therefore, user should define the net type for each layer using command **set_fp_rail_voltage_area_constraints**.

WHAT NEXT

Please specify the net type for layer %s as the example below:

```
set_fp_rail_voltage_area_constraints \
-layer %s \
-mtcmos_net_type <permanent | virtual>
```

SEE ALSO

set_fp_rail_voltage_area_constraints (2)

PNA-067 (error) No synthesized power network.

DESCRIPTION

In order to commit a power plan, user need to synthesize the power network first.

WHAT NEXT

Please use command **synthesize_fp_rail** to synthesize the power network.

SEE ALSO

commit_fp_rail (2)
synthesize_fp_rail (2)

PNA-068 (error) Cannot get power domain of voltage area %s

DESCRIPTION

Cannot find the corresponding power domain of voltage area %s. Please use report_power_domain and check for the Votlage Area Information in the log. If the Voltage Area Information shows 'N/A', then please run create_voltage_area with correct power domain information.

WHAT NEXT

Please run create_voltage_area with -power_domain

SEE ALSO

report_power_domain (2)
create_voltage_area (2)

PNA-099 (error) %s

DESCRIPTION

See the error message.

WHAT NEXT

See the error message.

PNA-101 (warning) Layer constraint is not set in %s.

DESCRIPTION

PNS synthesizes P/G network based on user-specified layer constraints. By default,

PNS uses the highest two metal layers.

WHAT NEXT

Set layer constraints using *set_fp_rail_constraints* command for single-voltage PNS or *set_fp_rail_voltage_area_constraints* command for multi-voltage PNS.

PNA-102 (warning) Ring constraint is not set in %s.

DESCRIPTION

PNS synthesizes core ring based on user-specified ring layer constraints. By default, PNS uses the highest two metal layers and twice the strap width to synthesize core ring.

WHAT NEXT

Set core ring constraint using *set_fp_rail_constraints* command for single-voltage PNS and *set_fp_rail_voltage_area_constraints* command for multi-voltage PNS.

PNA-103 (warning) Power/Ground pad constraint is not set in %s.

DESCRIPTION

Power pad synthesis (PPS) needs pad constraints to synthesize P/G pads.

WHAT NEXT

Set power/ground pad constraints using *set_fp_power_pad_constraints* command.

PNA-104 (warning) Block ring width is not set.

DESCRIPTION

PNS needs block ring width to synthesize block ring.

WHAT NEXT

Use the minimum width from technology file.

PNA-105 (warning) Cannot find any blocks with the given block type.

DESCRIPTION

The block name and block type do not match

WHAT NEXT

No blocks will be selected.

PNA-106 (warning) %d pad instances cannot connect to power net wires due to %s.

DESCRIPTION

If PG pad instances do not physically connect to power network, PNA/PNS will create virtual wires for connection. However, if there is blockage between the connected path, PNA is unable to make this connection such that the pad cannot be used during IR drop analysis.

WHAT NEXT

Please change the locations of pads or the blocking hard macros if users would like to use ths pads to supply current to core area.

PNA-107 (warning) There are %d pad instances which do not have any pin shape.

DESCRIPTION

For such pads, PNA will not use them during IR drop analysis.

WHAT NEXT

Please check if they are reasonable pad instances.

PNA-108 (warning) Target IR drop for net %s cannot be

satisfied.

DESCRIPTION

PNS is unable to synthesize power plan reaching the specified target IR drop. However, the power plan is still synthesized with the lowest possible IR drop values.

WHAT NEXT

PNA-109 (warning) Total %d pad(s) for net %s have currents over target pad current constraint %f.

DESCRIPTION

PPS is unable to synthesize power pads satisfying maximum pad current constraints.

WHAT NEXT

Please add more pads or change power plan to satisfy the maximum pad current constraints.

SEE ALSO

set_fp_power_pad_constraints (2)

PNA-110 (warning) The specified ring spacing is less than the minimum spacing of %.3f microns.

DESCRIPTION

For such a case, PNS uses the required minimum ring spacing.

WHAT NEXT

PNA-111 (warning) There are no wires in net %s.

DESCRIPTION

There is no PG wires in the specified net. PNA will skip the net for IR drop analysis.

WHAT NEXT

PNA-112 (warning) Power budget in %s is not specified. Power will be assigned automatically by PNS.

DESCRIPTION

If the power budget of a voltage area is not specified, PNS assigns power budget to this voltage area automatically in one of the following three ways:

(1) If -
analyze_power is used in the *synthesize_fp_rail* command, PNS will obtain power consumption of each cell instance from Power Compiler and use them as power budget.
(2) If power consumption file from Power Compiler, PrimeTime PX or default power consumption file is used in the *synthesize_fp_rail* command, PNS will obtain power consumption of each cell instance from the power consumption file and use them as power budget.
(3) If none of the above options are used, by default, PNS will use the total power budget specified in the *synthesize_fp_rail* command and assign it to each voltage area based on the total instance area and the supply voltage in the voltage area. Note that, if power budget in some voltage areas have already been specified, PNS will honor the specified power budget and assign the rest of power budget to the remaining voltage areas.

WHAT NEXT

SEE ALSO

synthesize_fp_rail (2)

PNA-113 (warning) Cannot find layer constraint for layer %s.

DESCRIPTION

PNS cannot find layer constraints for the specified layer. It could be due to unspecified layer constraints or internal error.

WHAT NEXT

Please check if user has set layer constraints for the specified layer.

PNA-114 (warning) Cannot find layer constraint for layer %d.

DESCRIPTION

PNS cannot find layer constraints for the specified layer. It could be due to unspecified layer constraints or internal error.

WHAT NEXT

Please check if user has set layer constraints for the specified layer.

PNA-115 (warning) Number of % straps aligned with top-level pin is 0.

DESCRIPTION

When user specifies strategy *align_strap_with_top_pin* and also set the variable *pns_pin_alignment_strap_only* to *true*, PNS will only generate power mesh with the pin alignment straps. In this case the number of % alignment straps is 0 and PNS may not generate a proper power/ground mesh.

WHAT NEXT

Set the variable *pns_pin_alignment_strap_only* to *false*.

SEE ALSO

set_fp_rail_strategy (2)

PNA-116 (warning) Virtual pad at (%s %s) for net %s cannot be used.

DESCRIPTION

The defined virtual pad cannot be used. This could be due to the following reasons:

(1) The virtual pad is inside hard macros.

(2) The area from virtual pad to the closest power net wires/vias is blocked by hard macros.

(3) The virtual pad cannot find a straight route to connect to any power net wires.

WHAT NEXT

PNA-117 (warning) The power value %.3f mW for master %s from PWR view, power consumption file, or LM view is higher than the power budget of the design %.3f mW.

DESCRIPTION

The engine uses area ratio rather than this power value to assign power to the instances.

WHAT NEXT

PNA-118 (warning) Cannot find port %s in %s.

DESCRIPTION

PNA/PNS will skip the instances whose PG ports are missing.

WHAT NEXT

PNA-119 (warning) The % block ring width of %s is too large..

DESCRIPTION

The block ring width constraint is larger than 1/6 of the chip width. PNS will ignore such block ring constraint.

WHAT NEXT

Choose a smaller block ring width.

PNA-120 (warning) cannot find standard cell pin for generating virtual straps for net %s.

DESCRIPTION

PNA is unable to find any standard cells connecting to the specified net. The information is needed when generating virtual rail.

WHAT NEXT

PNA-121 (warning) Cannot find %s %s in the design.

DESCRIPTION

WHAT NEXT

PNA-122 (warning) The power value of %s %s is negative and is ignored.

DESCRIPTION

The specified power file contains isntances with negative power values. PNA will ignore them.

WHAT NEXT

PNA-123 (warning) The IR drop of the synthesized net is higher than the target IR drop %.2f (mV).

DESCRIPTION

The maximum IR drop in the power network synthesized by PNS is greater than the user-specified target. This could be due to the target IR drop is too small, or the constraints for the power network is too tight.

WHAT NEXT

Increase the target IR drop or relax the power network constraints, or add more power/ground pads.

SEE ALSO

synthesize_fp_rail (2)
set_fp_rail_constraints (2)

PNA-124 (warning) Warning: %s has more than %d equivalent layers

DESCRIPTION

The layer has more than 16 equivalent layers. PNA can take at most 16 equivalent layers.

WHAT NEXT

PNA-125 (warning) Warning: minimum number of straps of layer %s needs to be less than %d, the current setting is %d, PNS will ignore this constraint

DESCRIPTION

The minimum straps should be less than maximum straps.

WHAT NEXT

PNA-126 (warning) Warning: Minimum strap constraints needs to be less than %d, PNS will ignore this constraints

DESCRIPTION

The minimum straps should be less than maximum straps.

WHAT NEXT

PNA-127 (warning) layer_name %s cannot be found, ignored

DESCRIPTION

It is unable to find the specified layer name.

WHAT NEXT

PNA-128 (warning) Warning: Virtual Segment setting error, support only vertial or horizontal wire, (x1, y1) = (%d, %d), (x2, y2) = (%d, %d)

DESCRIPTION

PNA supports only vertical or horizontal virtual segments.

WHAT NEXT

PNA-129 (warning) Cannot get supply voltage of net %s from UPF.

DESCRIPTION

PNS/PNA cannot find supply voltage of net %s from UPF definition.

WHAT NEXT

Please check the UPF information defined for supply net %s, or specify the supply voltage explicitly using **-voltage_supply** option.

SEE ALSO

set_fp_rail_voltage_area_constraints (2)

PNA-130 (warning) Supply voltage of net %s specified by user is inconsistent with the supply voltage defined in UPF.

DESCRIPTION

Supply voltage of net %s specified by user is inconsistent with the supply voltage defined in UPF.

WHAT NEXT

User-specified supply voltage will be honored. Please check the UPF definition.

SEE ALSO

set_fp_rail_voltage_area_constraints (2)

PNA-131 (warning) Cannot find net %s from UPF definition in

power domain %s.

DESCRIPTION

Supply net %s specified by user is not defined in UPF in power domain %s.

WHAT NEXT

PNS will honor the supply net specified by the users. However, user should also explicitly specify the supply voltage of this net, since it is not available in UPF.

SEE ALSO

set_fp_rail_voltage_area_constraints (2)

PNA-132 (warning) Fail to align net %s with MTCMOS power switch cells. PNS may not deliver power to instances in voltage area %s.

DESCRIPTION

PNS cannot align net %s with MTCMOS power switch cells that are used to shutdown voltage area %s. It could be due to the following reasons:

(1) There are no MTCMOS cells inserted in the design.
(2) User did not specify the MTCMOS cell name and on-resistance.
(3) MTCMOS cells are not logically connected to the net %s.
(4) There are blockages in the design that disallow alignment straps to be generate d.

WHAT NEXT

If the reason is:

(1) Insert MTCMOS cells first.
(2) Specify the MTCMOS cell name and on-resistance using the following Tcl command:
set_attribute [get_physical_lib_cells <*master_name*>] "mtcmos_resistance" <*resistanc e_value*>
set_attribute [get_physical_lib_cells <*master_name*>] "mtcmos_pin_layers" <*pin1_name* > <*pin1_layer*> <*pin2_name*> <*pin2_layer*>
(3) Connect MTCMOS cells to the primary and internal net.
(4) Check if there are blockages that block the alignment straps. If it is blocked by other voltage area, you may set the global constraints **-allow_routing_over_voltage_area**, otherwise, you may change the layer and/or direction of the alignment straps by setting the PNS strategy **-align_strap_with_mtcmos_cells**.

SEE ALSO

set_fp_rail_voltage_area_constraints (2)
set_fp_rail_strategy (2)
derive_pg_connection (2)

PNA-133 (warning) No power switch cell found in voltage area %s. PNS may not generate P/G network for the power-down voltage area correctly.

DESCRIPTION

PNS cannot find any MTCMOS power switch cells placed in the power-down voltage area %s, or the internal P/G pin of the power switch cell does connect to the shutdown net of the voltage area. This could be due to the following reasons:

(1) Power switch cells have not been physically inserted.
(2) User did not define the power switch cell name and on-resistance in the library.
(3) Logical connection is not made correctly between the power switch and the suppl y P/G net.

WHAT NEXT

If the reason is:

(1) Please insert power switch cells using the command **add_header_footer** command.
(2) Specify the power switch cell master name and on-resistance using the following command:
set_attribute [get_physical_lib_cells *<master_name>*] "mtcmos_resistance" *<resistanc e_value>*
set_attribute [get_physical_lib_cells *<master_name>*] "mtcmos_pin_layers" *<pin1_name > <pin1_layer> <pin2_name> <pin2_layer>*
(3) Connect power switch to the corresponding P/G net by **derive_pg_connection** command.

SEE ALSO

add_header_footer (2)
map_power_switch (2)
derive_pg_connection (2)

PNA-134 (warning) The primary power net %s is different from

the primary power net defined in UPF.

DESCRIPTION

The primary power net specified by user for the voltage area is different from the primary power net defined in UPF. This may cause cells in the voltage area not connect to the correct power supply net. Especially in power-down voltage area, the permanent and virtual power network may be generated incorrectly.

WHAT NEXT

Check your power net specification. Update the primary power net with the correct net name.

SEE ALSO

set_fp_rail_voltage_area_constraints (2)
report_power_domain (2)
derive_pg_connection (2)

PNA-135 (warning) Found broken %s ring wire at (%s %s)

DESCRIPTION

The ring of %s net is not connected to any other ring net at the location.

WHAT NEXT

Check the ring wire at (%s %s).

SEE ALSO

check_fp_rail (2)

PNA-136 (warning) Found floating %s wire segment at (%s %s).

DESCRIPTION

The wire at (%s %s) is not connected to any other wires or vias of the same net.

WHAT NEXT

Check the wire segment at (%s %s).

SEE ALSO

check_fp_rail (2)

PNA-137 (warning) Found power switch instance %s at (%s %s) unconnected to net %s

DESCRIPTION

There is no wire or via to connect the input power pin of the power swich to the permanent power net. Power switch cannot deliver power to the power down voltage area.

WHAT NEXT

Check the power switch connection of instance %s.

SEE ALSO

check_fp_rail (2)

PNA-138 (warning) No power/ground pads are specified and no virtual pads are defined.

DESCRIPTION

Power/ground pad master/instance is not defined by user; and no virtual pad is created in the design.

WHAT NEXT

PNS/PNA will regard all the IO pads that are logically connected to the analyzed power/ground net as power pads.

SEE ALSO

create_fp_virtual_pads (2)

PNA-139 (warning) The %s option will be ignored in the MVDD

power network synthesis.

DESCRIPTION

When **-synthesize_voltage_areas** or **-synthesize_power_switch_array** option is specified, PNS is performed per voltage area base (MVDD PNS). Therefore, this %s option will be ignored in this command. User should specify this %s option for each voltage area individually using **-set_fp_rail_voltage_area_constraints**.

WHAT NEXT

Specify the %s option using **-set_fp_rail_voltage_area_constraints**.

SEE ALSO

set_fp_rail_voltage_area_constraints (2)
synthesize_fp_rail (2)

PNA-140 (warning) All the %d pad instances are not connected to the power network or no direct pseudo wire can be made to the nearest power straps.

DESCRIPTION

WHAT NEXT

Please check the blockage between power pad pins and the designated power network area. In PNS, this could also be due to the power straps closer to the power pad pins are being cut because of blockage or DRC violation. Please use '-ignore_blockage' option to debug.

SEE ALSO

set_fp_rail_constraints (2)
set_fp_rail_voltage_area_constraints (2)
synthesize_fp_rail (2)

PNA-141 (warning) All the %d virtual pads cannot make direct

pseudo wire to the nearest power straps.

DESCRIPTION

WHAT NEXT

Please check the blockage between virtual pads and the designated power network area. In PNS, this could also be due to the power straps closer to the power pad pins are being cut because of blockage or DRC violation. Please use '-ignore_blockage' option to debug.

SEE ALSO

set_fp_rail_constraints (2)
set_fp_rail_voltage_area_constraints (2)
synthesize_fp_rail (2)
analyze_fp_rail (2)

PNA-142 (warning) One %s strap at (%.3f %.3f %.3f %.3f) is not created successfully due to DRC violation with nearby %s wires.

DESCRIPTION

A %s strap can not be synthesized by PNS because it has DRC violation with the nearby ring wires or existing wires.

WHAT NEXT

Please enlarge the distance between the synthesized strap and the nearby existing wire or ring wire. If the nearby wire is ring wire, please increase the offset of rings. If the synthesized strap is to align the power switch cells, please replace the power switch cells or increase the offset of rings.

SEE ALSO

synthesize_fp_rail (2)

PNA-143 (warning) Synthesized P/G straps may overlap with plangroup edges. Please use *-cut_plangroup_edge_layers*

strategy to remove them.

DESCRIPTION

In top-level PNS, synthesized straps may overlap with plangroup edges. After the top-level straps are pushed down to soft macros, these overlapping straps may create pins overlapping with soft macro boundaries and result in undesirable results when running PNS at block level. Therefore, if user uses the the hierachical PNS flow by specifying *-create_hierachical_pns_script* strategy, it is suggested that user also specifies the *-cut_plangroup_edge_layers* strategy during top-level PNS, in order to achieve a DRC clean power mesh at block level.

WHAT NEXT

Please specify the following stragegy:

set_fp_rail_strategy -cut_plangroup_edge_layers **<layer_name>**

SEE ALSO

set_fp_rail_strategy (2)

PNA-144 (warning) Supply net name %s is different from supply net %s defined in UPF for power domain %s.

DESCRIPTION

The supply net %s specified is different from the supply net defined in UPF for the power domain. PNS will honor user's specified supply net and synthesize power network inside the voltage area. However, if there is no cell instance that is logically connected to the supply net, PNS will issue error and exit.

WHAT NEXT

Please double check the supple net information with the UPF definition.

SEE ALSO

set_domain_supply_net (2)
create_supply_net (2)

PNA-145 (warning) The %s pin in MTCMOS cell %s is not

connected to the power network.

DESCRIPTION

The permanent/virtual pin in MTCMOS cells need to be physically connected to the power network or the virtual rail in order for PNA/PNS to simulate them by making pseudo resistance. If either pin is not connected to the power network, the power may not be able to deliver to the cells in the shutdown region.

WHAT NEXT

Please first check if both permanent and virtual pins in the MTCMOS cell have been logically and physically connected to the supply power network. If there is no standard cell rail in the design, please check if the -create_virtual_rail option is set when running PNA.

SEE ALSO

synthesize_fp_rail (2)
analyze_fp_rail (2)

PNA-199 (warning) %s

DESCRIPTION

See warning message.

WHAT NEXT

See warning message.

PNR-001 (error) check_physical_design failed: %s"

DESCRIPTION

An error was found by check_physical_design. The design is not ready for IC Compiler.

WHAT_NEXT

Use the "-verbose" option of check_physical_design for more details.

SEE ALSO

check_design (2)
check_physical_constraints (2)

PNR-002 (warning) check_physical_design found this: %s"

DESCRIPTION

The design may not be ready for IC Compiler.

WHAT_NEXT

Use the "-verbose" option of check_physical_design for more details.

SEE ALSO

check_design (2)
check_physical_constraints (2)

PNR-101 (error) No Milkyway CEL view is open.

DESCRIPTION

No Milkyway CEL view is open.

WHAT NEXT

Make sure that a Milkyway CEL view is open before proceeding.

SEE_ALSO

current_mw_cel(2)
open_mw_cel(2)

PNR-129 (Warning) Found ideal net that is not a clock net (%s). This net will not be optimized.

DESCRIPTION

You receive this warning message during check_physical_design, because a net has ideal_net attribute while it is not a clock.

This situation disables timing update and optimization of cells and nets in the transitive fanout of the specified objects during place_opt or psynopt.

WHAT NEXT

Check if the net should be defined as Clock, it is a High Fanout Net, or just regular net. Use create_clock if it sould have been a clock. Use remove_ideal_network to remove this restriction from ports or pins in the current design as sources of an ideal network.

SEE ALSO

create_clock(2) remove_ideal_network(2) report_ideal_network(2) set_ideal_netwok(2)

PNR-130 (Warning) dont_touch_network for non-clock high-fanout-net (%s) is found.

DESCRIPTION

This warning message tells you that the design has non-clock nets with 100+ fanout that are set as don’t touch.

WHAT_NEXT

Make sure that is exactly what you want. Or use **remove_attribute** to remove the don’t touch attribute for the net.

SEE ALSO

remove_attribute(2)
set_dont_touch_network(2)
set_dont_touch(2)
all_dont_touch(2)

PNR-131 (Warning) Non-clock net (%s) has fanout of over 500.

DESCRIPTION

This error message tells you that the design has non-clock nets which have high fanout of over 500.

WHAT_NEXT

SEE ALSO

PNR-133 (Warning) Net (%s) has fanout of over 1000 and not marked as ideal net.

DESCRIPTION

This warning message tells you that the design has nets with fanout of over 1000. These kind of nets are calculated pesimistically.

WHAT_NEXT

Mark these nets as ideal before extra optimization. You should optimze these nets later using command create_buffer_tree - or using command compile_clock_tree -high_fanout_net.

SEE ALSO

create_buffer_tree(2) compile_clock_tree(2)

PNR-137 (error) Area for %s %s is not defined.

DESCRIPTION

This error message tells you that the design contains move bound or group bound with undefined area or area of 0.

WHAT_NEXT

Use **update_bounds** to update the area attribute of the bound.

SEE ALSO

update_bounds(2)
create_bounds(2)
remove_bounds(2)
report_bounds(2)
get_bounds(2)

PNR-138 (error) Utilization of the design is at (%d%).

DESCRIPTION

This error message tells you that the design currently at 100% or above for utilization.

WHAT_NEXT

SEE ALSO

PNR-139 (error) Initial location is not set for cell (%s).

DESCRIPTION

This error message tells you that the design has cells without proper location, this design is not ready for routing.

WHAT_NEXT

Please run place_opt.

SEE ALSO

PNR-140 (error) No corresponding physical cell for logical cell %s.

DESCRIPTION

This error message tells you that this design contains logical cell which does not have a corresponding physcial cell, this cell will not be placed.

WHAT_NEXT

Check to make sure that the DEF input file matches with the verilog input file.

SEE ALSO

PNR-141 (error) Cannot get height and width for cell %s.

DESCRIPTION

This error message tells you that the design contains cell whose dimension was not specified.

WHAT_NEXT

SEE ALSO

PNR-142 (warning) The %s utilization of (%d) exceeds specified threshold (%d).

DESCRIPTION

This error message tells you that the design contains a move bound or group bound where the total cell area within the bound exceeds the specified threshold.

WHAT_NEXT

If exceeding the threshold is unacceptable, remove cells from the bound (move bounds

only) or remove and re-create the bound with a larger area.

SEE ALSO

update_bounds(2)
create_bounds(2)
remove_bounds(2)
report_bounds(2)
get_bounds(2)

PNR-143 (warning) Utilization of the design is at (%d%).

DESCRIPTION

This error message tells you that the design currently at 90% or above for utilization.

WHAT_NEXT

SEE ALSO

PNR-146 (warning) The design contains only (%d) routing layers, this might lead into congestion issue.

DESCRIPTION

This warning message tells you that the design might not have enough routing layers(<3), which might cause congestion issues or QOR degradation later in the flow.

WHAT_NEXT

Check for Congestion. If you find congestion problems should define more routing layers for the design

SEE ALSO

set_net_routing_layer_constraints(2)
report_net_routing_layer_constraints(2)
remove_net_routing_layer_constraints(2)

PNR-148 (warning) Placement area is less than specified site width of %d.

DESCRIPTION

This warning message tells you that the design has Narrow Placement Areas that are less than the given threshold. The threshold is defined in terms of base site widths. The default is the maximum width of the cells in the library. The narrow placement area threshold width is same for both the vertical and the horizontal direction.

This message followed by list of Narrow Placement Area coordinates.

Narrow Placement Area might be misused by cells bigger than the area. This harms the design utilization and effects displacement during legalization. Cells located inside narrow placement areas, might have optimization problems. This can cause QOR degradation, or extra burden over routing resources. Cells located inside narrow placement areas, might have routing access problems. In this can cause QOR degradation or extra burden over routing resources, the narrow placement becomes placement traps.

Be aware that In some cases Narrow Placement Areas might have no impact. This might be in cases that most of the design is using relatively small cells, or the number if these areas are neglectable, or no routing access problems to these cells.

WHAT_NEXT

It is not recommended to ignore this message. It is up to User to verify for each Narrow Placement Area coordinates - what type is it.

If the narrow placement is between macros or there is routing access problems (very high congestion in the edges) it is recommended to use command create_placement_blockage to avoid cells placement in that area.

If user finds that this area not causes any issue - there are no congestion or utilization problems - user can continue the flow while carefully inspect these areas.

SEE ALSO

check_physical_constraints(2) create_placement_blockage(2)

PNR-149 (error) Core area is bigger than die size.

DESCRIPTION

This error message tells you that the core area of the design is bigger than the

specified die size.

WHAT_NEXT

Reset the die area use **set_die_area**

SEE ALSO

get_die_area(2)
set_die_area(2)
get_core_area(2)

PNR-151 (error) Found macro cell without fixed placement: '%s'

DESCRIPTION

The tool has found a macro cell without fixed placement.

WHAT NEXT

Macro cells must have fixed placement before the placer can be run.

SEE_ALSO

all_fixed_placement(2)
all_macro_cells(2)
set_dont_touch_placement(2)

PNR-152 (error) Clock '%s' has hierarchical pin '%s' as source.

DESCRIPTION

A clock was found to have a hierarchical pin as source. A hierarchical pin cannot be the root for a clock-tree. CTS will fail for this clock.

WHAT NEXT

Redefine the clock source.

SEE_ALSO

create_clock(2)
set_driving_cell(2)

PNR-153 (error) verify_pg_nets failed.

DESCRIPTION

Some power/ground pins in the design are not properly connected to the power/ground nets.

WHAT NEXT

SEE_ALSO

connect_pg_nets(2)

PNR-155 (error) %s is not define for this %s %s.

DESCRIPTION

This error message tells you that the design does not either have the unit or track defined.

WHAT_NEXT

SEE ALSO

PNR-156 (warning) Macro (%s) has no keepout margins.

DESCRIPTION

This warning message tells you that the specified marco does not have keepout margins.

The set_keepout_margin command creates keepout margins for the specified cells and library cells. The tool will derive the keepout margins for the cells in the following order.

1. keepout margin specified on the cell itself
2. keepout margin specified on the lib cells of the cell
3. Pin count based derived keepout margin values in case of macro cells.

WHAT_NEXT

Use **set_keepout_margin** to define the keepout region for the macro, or create

placement blockages arounnd the macro.

SEE ALSO

get_attribute(2)
report_keepout_margin(2)
set_keepout_margin(2)
remove_keepout_margin(2)
create_placement_blockage(2)

PNR-158 (warning) Fixed placement cell (%s) has no keepout margins.

DESCRIPTION

This error message tells you that the specified fixed placement cell does not have keepout margins. Placing cells close to this cell might generate routability problems later in the flow.

WHAT_NEXT

Check if this was done by purpose. If not, set_keepout_margine to create one.

SEE ALSO

get_attribute(2) set_keepout_margine(2) remove_keepout_margin(2)
report_keepout_margin(2)

PNR-159 (warning) %s for design %s.

DESCRIPTION

This error message tells you that either the die area or ports are not fixed for the current design. These are the basic floorplan elements which need to define prior to running place_opt.

WHAT_NEXT

SEE ALSO

PNR-160 (warning) Cell (%s) is a standard cell which has fixed

placement.

DESCRIPTION

This warning message tells you the specified standard cell has fixed placement. Usually this is not expected. a standard cell that has fixed placement restriction cannot be optimized.

WHAT_NEXT

Check if this restriction was done by purpose. If not, use command remove_dont_touch_placement to remove this restriction.

SEE ALSO

remove_dont_touch_placement(2) set_dont_touch_placement(2)

PNR-161 (warning) Macro cell (%s) is not fixed.

DESCRIPTION

This error message tells you the specified macro cell is not fixed, and to run create_placement and place_opt need macro cell fixed.

WHAT_NEXT

Please fix the macro cell location use *set_cell_location*.

SEE ALSO

get_attribute(2)
set_attribute(2)
set_cell_location(2)

PNR-162 (warning) %s under congested area are: (%s)

DESCRIPTION

This error message tells you that the listed nets or cells are in the congested area of over 95%.

WHAT_NEXT

SEE ALSO

PNR-163 (Info) The design has existing routes.

DESCRIPTION

This error message tells you that the design has existing routes.

WHAT_NEXT

SEE ALSO

PNR-164 (Info) Report design vs library layers and preferred routing directions.

DESCRIPTION

WHAT_NEXT

SEE ALSO

PNR-165 (Info) Report track info.

DESCRIPTION

WHAT_NEXT

SEE ALSO

PNR-166 (Warning) Net (%s) has DRC violation but is set as

don’t touch.

DESCRIPTION

This warning message tells you that the design has nets with DRC violations but are set as dont touch. This causes optimization to skip on this net, and may impact the whole path that this net is member at.

WHAT_NEXT

Check to see where don’t touch attributes are coming from. Use **set_dont_touch** to remove the don’t touch attribute or/and fix the DRC violation.

SEE ALSO

set_attribute(2)
set_dont_touch(2)

PNR-167 (Warning) The design has %d congested areas with over %.2f utilization. Only display %d congested areas.

DESCRIPTION

This error message tells you the design has more congested areas than specified by the variable snps_cpd_congestion_area_limit (default 100). Criteria for congestion is specified by the variable snps_cpd_congestion_threshold (default 95%).

WHAT_NEXT

SEE ALSO

PNR-168 (Error) Port (%s) has geometry on layer (%s), which is set as ignored layer.

DESCRIPTION

This error message tells you that the design has port which has geometry set on unaccessible layers.

WHAT_NEXT

SEE ALSO

PNR-169 (Warning) Port (%s) is long port.

DESCRIPTION

This error message tells you that the design has long ports without the flag physopt_long_port_support set to TRUE.

WHAT_NEXT

SEE ALSO

PNR-171 (Info) port (%s) is a physical only port.

DESCRIPTION

This error message tells you that the design has physical only ports and it is listing the port names.

WHAT_NEXT

SEE ALSO

PNR-172 (error) Track is not define for layer %s.

DESCRIPTION

This error message tells you that the layer does not have the track defined, and the layer is a preferred routing layer.

WHAT_NEXT

Use **create_track** to define the tracks. If the floorplan generated by DEF reading, you can use the DEF file to get the track data.

SEE ALSO

```
create_track(2)
report_track(2)
report_ignored_layers(2)
reportt_preferred_routing_layer_direction(2)
```

PNR-173 (error) Length unit is not define for design %s.

DESCRIPTION

This error message tells you that the design does not have the length unit defined.

WHAT_NEXT

Please update the tech file for missing design units. Please define unitLengthName and lengthPrecision inside tech file.

```
For example:
icc_shell> write_mw_lib_files -technology -output dumped.tf myLib;
Look for Technology section,  add unitLengthName and lengthPrecision if not avialab
le. The format looks like:
Technology  {
        unitLengthName          = "micron"
        lengthPrecision         = 1000
}
cc_shell> close_mw_lib;
icc_shell> set_mw_technology_file -technology changed_from_dump.tf myLib;
icc_shell> open_mw_lib myLib;
```

SEE ALSO

```
report_mw_lib(2)
```

PNR-175 (error) Move Bound %s is over-utilized (%s used).

DESCRIPTION

This error message tells you that the indicated move bound has more cells inside it than can fit.

WHAT_NEXT

Use **update_bounds** to update the dimensions of the bound, or remove cells from the bound.

SEE ALSO

update_bounds(2)
create_bounds(2)
remove_bounds(2)
report_bounds(2)
get_bounds(2)

PNR-176 (error) Fixed cell %s is outside %s move bound %s.

DESCRIPTION

This error message tells you that the indicated cell has been fixed to a location that is outside of the hard/exclusive move bound it is associated with. This represents an unachievable goal, and will impact the runtime or quality of the placement.

WHAT_NEXT

Use **update_bounds** to update the dimensions of the move bound or remove the cell from the bound. Alternatively, removed the fixed attribute from the cell.

SEE ALSO

update_bounds(2)
create_bounds(2)
remove_bounds(2)
report_bounds(2)
get_bounds(2)

PNR-177 (Warning) %s %s cannot fit into group bound %s.

DESCRIPTION

This warning message tells you that the indicated object (either a fixed cell or a hard/exclusive move bound) has an area greater than the dimensions of the group bound. This may impact runtime or quality of the placement.

WHAT_NEXT

Use **update_bounds** to update the group bound to increase its dimension attribute or remove the object from the group bound.

SEE ALSO

update_bounds(2)

create_bounds(2)
remove_bounds(2)
report_bounds(2)
get_bounds(2)

PNR-178 (Warning) %s %s and %s %s cannot both fit into group bound %s.

DESCRIPTION

This warning message tells you that the two indicated objects (either fixed cells or hard/exclusive move bounds) have both been placed inside the named group bound. However, the dimension of the group bound is too small to contain both objects at the same time. This may impact runtime or quality of the placement.

WHAT_NEXT

Use **update_bounds** to update the group bound to increase its dimension attribute or remove one or the other object from the group bound.

SEE ALSO

update_bounds(2)
create_bounds(2)
remove_bounds(2)
report_bounds(2)
get_bounds(2)

PNR-179 (Warning) Net (%s) is high fanout net but set as don’t touch.

DESCRIPTION

This message tells you that the design has high fanout nets but are set as dont touch before place_opt.

WHAT_NEXT

Check to see where don’t touch attributes are coming from. Use **set_dont_touch** to remove the don’t touch attribute .

SEE ALSO

set_attribute(2)

PNR-254 (error) No clocks were found.

DESCRIPTION

No clocks were found in the design.

WHAT NEXT

Define the clocks before proceeding.

SEE_ALSO

create_clock(2)
get_clocks(2)

PPLI-1 "Cannot register RTL Net %s[%d:%d], because its individuals bits are not available"

DESCRIPTION

The DesignPower PLI interface to Verilog-XL is not able to register individual bits of a bused net when the bused net is at the RTL level. An RTL level net does not have any of its individual pins connected to cells in the verilog design hierarchy. If all connections of the bus are connected in a bused fashion, Verilog PLI v1.0 does not provide a mechanism to monitor the individual nets within the bus. This is a Verilog PLI v1.0 limitation.

WHAT NEXT

The Verilog language provides compiler directives that provide a workaround to this problem. The expand_vectornets directive forces the verilog simulator to expand all vector nets independent of their connections. This directive must appear before module definitions that contain unexpanded bus signals. Note that this directive has a negative impact on Verilog simulation performance and memory. The corresponding directive noexpand_vectornets must be used after module definition in order to limit the impact on cpu performance.

You can make changes to the verilog description to work around this problem. If you ignore this message, no activity is reported for this bus or any of the component nets in the bus. Alternately, you can modify the verilog source description and connect cells or ports to a component net of the bus.

Verilog does not expand bused connections below the library cell frontier, so check to see if you are using the (-y or -v) options for designs which are not library cells.

PPLI-2 Please specify the path for the testbench module models in the $read_rtl_saif() command.

DESCRIPTION

You did not specify the path for the testbench modules. This is likely to cause the PLI routines fail to register the RTL objects. To specify the path, use $read_rtl_saif("file", "test_modules.design_instance").

WHAT NEXT

This is a warning.

PPLI-3 "Output Port %s Ignored."

DESCRIPTION

The power Verilog PLI does not register output port nets when operating in one of the two port registration modes (dp_ports_only, dp_top_ports_only). These ports are not registered because the port only modes are typically used for seeding probabalistic analysis within the DesignPower product. Not monitoring output ports can save memory and cpu runtime during the verilog simulation. This is an information message.

WHAT NEXT

No action is required.

PPLI-4 "Out of memory. Cannot create more VCL links"

DESCRIPTION

The power Verilog PLI was not able to allocate memory for its data structure. The process exceeded available memory limit.

WHAT NEXT

Increase memory limit and rerun.

PPLI-5 " $set_toggle_region must always be done before toggle_stop"

DESCRIPTION

The power Verilog PLI requires a specific order of routine calls. In this case, a $toggle_stop() command appears before the $set_toggle_region command in the testbench.

WHAT NEXT

Check the test bench and fix order of $toggle_stop command.

PPLI-6 "$toggle_start must always be done before calling on $toggle_stop."

DESCRIPTION

The power Verilog PLI requires a specific order of routine calls. In this case, a $toggle_stop() command appears before the $toggle_start() command in the testbench. The correct order is to perform $toggle_start() before $toggle_stop.

WHAT NEXT

Check the test bench and fix order of the $toggle_stop command.

PPLI-7 "Out of memory. Cannot create DP Hash table/list."

DESCRIPTION

The power Verilog-PLI hash table routine can not allocate memory for its data structure. This error indicates that Verilog application exceeded memory limit for the process.

WHAT NEXT

Run with a larger memory configuration.

PPLI-8 "There are 0 nets registered. This typically happens when the only input parameter provided has no ports and you requested the dp_top_ports_only option for non-recursive-port registration."

DESCRIPTION

The power Verilog PLI did not register any design objects for monitoring during simulation. This usually indicates that there is a problem in the $toggle_set function parameters set within the testbench.

WHAT NEXT

Check the verilog testbench and $toggle_set parameters to determine why the error occured.

PPLI-9 "$toggle_report must always be done before calling on $toggle_reset."

DESCRIPTION

The power Verilog PLI requires a specific order of routine calls. In this case, a $toggle_reset() command appears before the $toggle_report call in the estbench.

WHAT NEXT

Check the test bench and fix order of $toggle_reset command.

PPLI-10 "Net %s with less than 2 connections ignored."

DESCRIPTION

The power Verilog PLI attempted to monitor a net, but found the net had less than 2 connections. In this case the Verilog PLI does not monitor toggle activity on this net in an effort to save memory and CPU runtime. Single pin nets typically are not relevant to the process of power analysis.

WHAT NEXT

No action is required. You might want to review the net and ensure that this situation is correct.

PPLI-11 "The module instance %s does not match the cell specification in the SAIF file. No sdpd info is registered for this instance."

.SH DESCRIPTION The port information of this module instance does not match the cell specification in the SAIF file. For example, a port specified in the SAIF file could not be found in the module instance. In this case, Verilog PLI ignore the state-path dependencies of this intsnace.

WHAT NEXT

No action is required. You might want to review the net and ensure that this situation is correct.

PPLI-12 " $toggle_stop must always be done before toggle_report"

DESCRIPTION

The power Verilog PLI requires a specific order of routine calls. In this case, a $toggle_report() command appears before the $toggle_stop command in the testbench.

WHAT NEXT

Check the test bench and fix order of $toggle_report command.

PPLI-13 "read_lib_saif() must be called before the $set_toggle_region()

DESCRIPTION

The power Verilog PLI requires a specific order of routine calls. In this case, a $read_lib_saif() command appears after the $set_toggle_region() command in the testbench. Please change your testbench file so that it appears before the $toggle_start() command.

WHAT NEXT

Check the test bench and fix order of $read_lib_saif() command.

PPLI-14 "read_rtl_saif() must be called before the $set_toggle_region()

DESCRIPTION

The power Verilog PLI requires a specific order of routine calls. In this case, a $read_rtl_saif() command appears after the $set_toggle_region() command in the testbench. Please change your testbench file so that it appears before the $set_toggle_region() command.

WHAT NEXT

Check the test bench and fix order of $read_rtl_saif() command.

PPLI-15 "set_toggle_reion() must be called before $toggle_start().

DESCRIPTION

The power Verilog PLI requires a specific order of routine calls. In this case, a $set_toggle_region() command appears after the $toggle_start() command in the testbench. Please change your testbench file so that it appears before the $toggle_start() command.

WHAT NEXT

Check the test bench and fix order of $set_toggle_region() command.

PPLI-16 "You have to also include a RTL forward SAIF file using $read_rtl_saif() command because you included an MPM forward SAIF file.

DESCRIPTION

An MPM forward SAIF file only describes cell-specific MPM information. Since a cell could be instantiated in different places in the design, you need include a RTL forward SAIF file to identify which instance is an MPM cell. A RTL forward SAIF file is generated by using rtl2saif command from dc_shell.

WHAT NEXT

Check the test bench and add read_rtl_saif() command

PPLI-17 "set_gate_level_monitoring() must be called before $toggle_start().

DESCRIPTION

The power Verilog PLI requires a specific order of routine calls. In this case, a

$set_gate_level_monitoring() command appears after the $toggle_start() command in the testbench. Please change your testbench file so that it appears before the $toggle_start() command.

WHAT NEXT

Check the test bench and fix order of $set_gate_level_monitoring() command.

PPLI-18 "set_toggle_reion() must be called before $toggle_report().

DESCRIPTION

The power Verilog PLI requires a specific order of routine calls. In this case, a $set_toggle_region() command appears after the $toggle_report() command in the testbench. Please change your testbench file so that it appears before the $toggle_report() command.

WHAT NEXT

Check the test bench and fix order of $set_toggle_region() command.

PPLI-19 "set_toggle_reion() must be called before $toggle_start().

DESCRIPTION

The power Verilog PLI requires a specific order of routine calls. In this case, a $set_toggle_region() command appears after the $toggle_start() command in the testbench. Please change your testbench file so that it appears before the $toggle_start() command.

WHAT NEXT

Check the test bench and fix order of $set_toggle_region() command.

PPLI-20 Two consecutive $toggle_start() calls are not allowed.

DESCRIPTION

You can not have consecutive $toggle_start() calls without $toggle_stop() in between. Please go to your testbench and make sure a $toggle_stop() is placed prio to the second $toggle_start().

WHAT NEXT

This is an error.

PROC-1 (fatal) PROC(%s): Could not start child.

DESCRIPTION

WHAT NEXT

PROC-2 (error) Could not fork child process.

DESCRIPTION

WHAT NEXT

PROC-3 (error) Could not connect to child process.

DESCRIPTION

WHAT NEXT

PROC-4 (error) Could not establish child connection.

DESCRIPTION

WHAT NEXT

PROC-5 (information) Child process returned unexpectedly.

DESCRIPTION

The tool has tried to create a child process to help it perform some function, and that child process could not properly start up and connect to its parent. This could be for any one of a number of reasons: The system is out of memory, TCP/IP is not installed properly on the system, ...

WHAT NEXT

Check to see if your system has run out of virtual memory (swap space). Different systems do this differently, on SUNs use the /etc/pstat -s command.

Check to see if TCP/IP is installed properly on your system:

Try to rlogin localhost

Try to rlogin ‘hostname‘ (Use backquotes around hostname)

If either of these commands fail, see you local system administrator for further help.

PROC-6 (error) Unknown host ’%s’.

DESCRIPTION

WHAT NEXT

PS-1 (error) Bad plot command '%s'.

DESCRIPTION

This error occurs because this command is not supported and has been obsoleted.

WHAT NEXT

Use the GUI to produce schematic and placement printouts for your design.

PS-2 (error) Bad plot command.

DESCRIPTION

This error occurs because this command is not supported and has been obsoleted.

WHAT NEXT

Use the GUI to produce schematic and placement printouts for your design.

PS-3 (error) Cannot open plot file '%s'.

DESCRIPTION

This error occurs because this command is not supported and is obsolete.

WHAT NEXT

Use the GUI to produce schematic and placement printouts for your design.

PSCH

PSCH-1 (warning) Cannot plot design '%s' because it does not have a schematic.
You can create a schematic by using the create_schematic command.

DESCRIPTION

This warning occurs because this command is not supported and is obsolete.

WHAT NEXT

Use the GUI to produce schematic and placement printouts for your design.

PSCH-2 (warning) Cannot plot design '%s' because it does not have a symbol view.
You can create a symbol by using the create_schematic -symbol_view command.

DESCRIPTION

This warning occurs because this command is not supported and is obsolete.

WHAT NEXT

Use the GUI to produce schematic and placement printouts for your design.

PSYN-001 (error) Design has synthetic parts.

DESCRIPTION

You receive this error message because your design contains synthetic parts. You must map all synthetic parts before running the **physopt** command, **create_placement** command, or **legalize_placement** command.

WHAT NEXT

To map synthetic parts, run the **compile** command.

SEE ALSO

compile (2), **create_placement** (2), **legalize_placement** (2), **physopt** (2).

PSYN-002 (error) Design contains unmapped cells.

DESCRIPTION

You receive this error message because your design contains generic, unmapped cells. You must map all such cells before running the **physopt** command, the **create_placement** command, or the **legalize_placement** command.

WHAT NEXT

To map generic cells, run the **compile** command.

SEE ALSO

compile (2), **create_placement** (2), **legalize_placement** (2), **physopt** (2).

PSYN-003 (error) Command '%s' had an error while executing. Discontinuing.

DESCRIPTION

You receive this error message because the command you specified cannot execute and

has been discontinued. This happens when input data is insufficient or when input is not in a format the command requires.

WHAT NEXT

Correct the input using the errors and warning issued and reissue the command.

SEE ALSO

read_lib (2).

PSYN-004 (error) Technology data not supplied.

DESCRIPTION

You receive this error message because you did not specify the per-unit length values of resistance and capacitance in this instance.

WHAT NEXT

To set the values, use the **set_delay_estimation_options** command

SEE ALSO

read_lib (2), **set_delay_estimation_options(2).**

PSYN-005 (error) Design %s has no associated physical design.

DESCRIPTION

You receive this error message because you specified no physical data for your design.

WHAT_NEXT

Specify the physical data for the design in the PDEF format, and read it in using the **read_pdef** command.

SEE ALSO

read_pdef (2).

PSYN-006 (warning) The core area for block is not defined.

DESCRIPTION

You receive this warning because the core area for the block you specified for optimization is not defined.

WHAT NEXT

Specify the core area in using the initialize_floorplan command or input DEF using the read_def command.

SEE ALSO

read_def (2) **initialize_floorplan** (2)

PSYN-007 (error) Following Ports have no location.

DESCRIPTION

You receive this error message because a port in your design does not have a specified location. To run the **create_placement** command and the **physopt** command, all ports must have their location defined.

WHAT NEXT

In the input PDEF file, add locations to all of the ports, and read in the PDEF file using the **read_pdef** command.

If you do not have a port locations you can instruct the tool to generate port locations for unfixed ports by using the **-mpc** switch with the **create_placement**, **physopt** or **compile_physical** commands.

SEE ALSO

create_placement (2), **physopt** (2), **read_pdef** (2).

PSYN-008 (error) The following cells have no location.

DESCRIPTION

You receive this error message because one or more cells in your design do not have their locations specified.

All cells must have locations specified in the following instances:

To run the **legalize_placement** command.

To run the **physopt** command with the **-incremental** option.

WHAT NEXT

In the input PDEF file,add locations to the cells. Then read in the input PDEF file using the **read_pdef** command

or

use a floorplanner, use set_cell_location command, or run placement or use legalize_placement -eco

SEE ALSO

create_placement (2), **legalize_placement** (2), **physopt** (2), **read_pdef** (2).

PSYN-009 (error) Blockage %s has no dimensions specified.

DESCRIPTION

You receive this error message because a blockage you specified does not have a corresponding rectangle defined in the input PDEF file. It is necessary to define a corresponding rectangle for every blockage in your design.

WHAT NEXT

Add a rectangle to the blockage in the input PDEF file, and read in the PDEF file using the **read_pdef** command. Or use the **create_obstruction** command to create the blockage rectangle.

SEE ALSO

create_obstruction (2), **read_pdef** (2).

PSYN-010 (error) No site array is specified.

DESCRIPTION

You receive this error message because your macro does not contain a specified site array. To run the **legalize_placement** command and the **physopt** command, a specified site array is necessary.

WHAT_NEXT

Add a site array definition to the input PDEF file, and read in the PDEF file using the **read_pdef** command.

SEE ALSO

legalize_placement (2), **physopt** (2), **read_pdef** (2).

PSYN-011 (error) Site array has no rows specified.

DESCRIPTION

You receive this error message because the site array you specified has no rows defined. The completed site array is necessary to run the **legalize_placement** command and the **physopt** command.

WHAT_NEXT

Correct the site array definition to the input PDEF file, and read in the input PDEF file using the **read_pdef** command.

SEE ALSO

legalize_placement (2), **physopt** (2), **read_pdef** (2).

PSYN-012 (error) Row has no sites specified.

DESCRIPTION

You receive this error message because a row in your specified site array has no sites defined on it. Every row needs to have a nonzero number of sites.

WHAT NEXT

Correct the site array definition to the input PDEF file, and read in the input PDEF file using the **read_pdef** command.

SEE ALSO

read_pdef (2).

PSYN-013 (error) PhysOpt license is not enabled.

DESCRIPTION

You receive this error message because the command you used requires a PhysOpt license, and a license is not available. Your site might not have acquired a PhysOpt license, or other processes might be using all the available licenses.

WHAT NEXT

To get the PhysOpt license, invoke the **get_license PhysOpt** command or call your Synopsys representative.

SEE ALSO

get_license (2).

PSYN-014 (error) No physical library cells for following library cells

DESCRIPTION

You received this error message because one or more logical library cells do not have a corresponding physical library cell. Every library cell referenced in the input design must have a physical library cell defined for it in a physical library.

WHAT NEXT

All logical library cells in the design should have corresponding physical library cells.

Check the physical libraries specified using the command report_mw_lib -mw_reference_library. If this list does not contain all the expected physical libraries, update the list using the command set_mw_lib_reference.

If all expected physical libraries are loaded, use the check_library command to detect inconsistencies between the logical and physical libraries in the design.

The command get_physical_lib_cells */* will list all physical cells currently loaded (use appropriate patterns or filters to restrict the results).

SEE ALSO

report_mw_lib(2) set_mw_lib_reference(2) check_library(2) get_physical_lib_cells(2)

PSYN-015 (error) Dimensions of following library cells is not specified.

DESCRIPTION

You receive this error message because a library cell in your library does not have specified height or width. Every library cell must have both height and width defined.

WHAT NEXT

In the input physical library, correct the specification of the library cell. Then recompile the library using the **read_lib** command.

SEE ALSO

read_lib (2).

PSYN-016 (error) There is no physical pins for following library pins

DESCRIPTION

You receive this error message because a pin on a logical library cell has no corresponding pin in the physical library. The physical library cell should contain pins corresponding to every pin in the logical library cell.

WHAT NEXT

In the input physical library, correct the specification of the library cell. Then recompile the library using **read_lib**.

SEE ALSO

read_lib (2).

PSYN-017 (error) There is no location specified for library pin

%s/%s.

DESCRIPTION

You receive this error message because a library pin you specified has no location defined in the physical library. Every pin must have a specified location in the physical library.

WHAT NEXT

In the input physical library, correct the definition of the pin. Then recompile the library using the **read_lib** command.

SEE ALSO

read_lib (2).

PSYN-018 (error) Site %s is not defined in physical library.

DESCRIPTION

You receive this error message because the site name instantiated to create a row in the site array is not defined in the physical library.

For the **physopt** command and the **legalize_placement** command to work, the site has to be linked to a site in the physical library.

WHAT NEXT

In the physical library, add the site definition. Then recompile the library using the **read_lib** command.

SEE ALSO

legalize_placement (2), **physopt** (2), **read_lib** (2).

PSYN-019 (error) Dimensions of site %s are not specified.

DESCRIPTION

You receive this error message because the site name instantiated to create a row in the site array does not have its height and width defined in the physical library. For the **physopt** command and the **legalize_placement** command to work, the site has to

have an associated height and width defined in the physical library.

WHAT NEXT

Add the height and width attributes to the site in the physical library and recompile the library using **read_lib**.

SEE ALSO

legalize_placement (2), **physopt** (2), **read_lib** (2).

PSYN-020 (error) Site width on a row is not an integer multiple of the spacing between sites on the row.

DESCRIPTION

You receive this error message because the site array you specified does not meet certain requirements.

For horizontal rows, the width of a site on a row should be an integer multiple of the spacing between sites on the row. Also, the spacing between sites should not exceed the width of the site. For vertical rows, the height of the site on the row should meet the above requirements.

WHAT NEXT

In the input PDEF file, adjust the site array to meet the above requirements. Then read in the PDEF file using the **read_pdef** command.

SEE ALSO

read_pdef (2).

PSYN-021 (error) Could not read the following physical library.

DESCRIPTION

You specified a physical library in the **physical_library** variable, but it is not in the directories listed in the **search_path** variable. For the **link_physical_library** command to perform, a full set of physical libraries must be present.

WHAT NEXT

Add the path name of the library to the **search_path** variable or, at the command line, specify the full path to the library (as in /usr/joe/my_lib.pdb), or remove the library from the **physical_library** variable.

SEE ALSO

link_physical_library (2); **physical_library** (3), **search_path** (3).

PSYN-022 (error) The library cell %s has no legal orientation, or cannot fit to any row site. Check LEF/DEF.

DESCRIPTION

A library cell is legal on a row if the site type of the row matches that of the library cell and if the library cell has an orientation defined that is allowed on that row. The detailed placer will try and legalize the placement so that the cell meets the above legality condition.

WHAT NEXT

An alternative to relying on the detailed placer to legalize the placement is to change the orientation of the sites on the rows so that all library cells are legal on the rows, in some orientation.

SEE ALSO

legalize_placement (2), **physopt** (2).

PSYN-023 (error) Site array has rows and columns specified at the same time.

DESCRIPTION

You receive this error message because the site array you defined in the input PDEF contains both horizontal and vertical arrays. Only one orientation of arrays can be specified in the site array, horizontal rows or vertical columns, but not both.

WHAT_NEXT

Change the input PDEF, and read it back in using the **read_pdef** command.

SEE ALSO

read_pdef (2).

PSYN-024 (warning) The '%s' cell in the '%s' technology library does not have corresponding physical cell description.

DESCRIPTION

You see this warning because you specified a logical cell in the technology library that does not have a matching cell in the physical library. Every logical cell must have corresponding matching cell in the physical library. If there is no matching cell in the physical library then that particular logical cell is marked as don't use and won't be considered any more.

Physical synthesis requires both logical and physical library information. A matching physical cell is defined as a physical cell with the same name as the logical cell. It must contain, at least, all of the same-name pins defined in the logical cell.

WHAT NEXT

Make sure each cell in the technology library has a matching physical cell.

EXAMPLE MESSAGE

Warning: The 'AND2A' cell in the 'demo' technology library does not
have corresponding physical cell description. (PSYN-24)

SEE ALSO

physopt (2), **list_libs** (2), **report_lib** (2).

PSYN-025 (warning) The '%s' cell in the '%s' physical library does not have corresponding logical cell description.

DESCRIPTION

You receive this warning because you have specified a cell in the physical library for which a matching logical cell description in the technology library does not

exist. Every cell in the technology library must have a matching cell in the physical library. If there is no matching logical cell, then that particular physical cell cannot be used. Physical synthesis requires both logical and physical library information. A matching logical cell is defined as a logical cell with the same name as the physical cell. The matching logical cell contains, at least, all of the same-name pins defined in the physical cell.

This warning is also issued if the pin direction of the same-name pins in the corresponding logical library cell and physical library cell do not match.

WHAT NEXT

No action is required on your part.

However, you can avoid receiving this warning by ensuring that each cell in the technology library has a matching physical library cell and that their pin directions match.

EXAMPLE MESSAGE

Warning: The 'AND2A' cell in the 'demo' physical library does not have corresponding logical cell description. (PSYN-25)

SEE ALSO

physopt(2)
list_libs(2)
report_lib(2)

PSYN-026 (warning) This physical library is missing '%s' technology information.

DESCRIPTION

A physical library, at the least, needs to contain the following technology information:

- distance unit
- capacitance unit
- resistance unit
- site definition

- layer definition

Be sure that the library source for the creation of the physical library contains this information.

WHAT NEXT

Add the information and regenerate the physical library with Library Compiler, using the **read_lib** command.

SEE ALSO

read_lib (2).

PSYN-027 (error) Cannot link logical library '%s' with physical library '%s'.

DESCRIPTION

You specified a physical library in the **physical_library** variable, but it is not in the directories listed in the **search_path** variable. For the **link_physical_library** command to perform, a full set of physical libraries must be present.

WHAT NEXT

Be sure the name of the physical library is correct and is set properly. Also check that the search path is correctly stated in the **search_path** variable.

SEE ALSO

link_physical_library (2); **physical_library** (3), **search_path** (2).

PSYN-028 (error) Cannot link logical library '%s' with physical library '%s'.

DESCRIPTION

You specified a physical library in the **physical_library** variable, but the compiler cannot link the logical library and the physical library. This failure probably occurred because the name of one of the cells (and the pins therein) in the logical library do not match the names of their counterparts in the physical library.

WHAT NEXT

Be sure that the names of the cells and pins in the logical library match those in the physical library. Remember that these names are case-sensitive.

If a cell name in the logical library matches that in the physical library, but the pin name or names of the cell do not, linking will fail.

SEE ALSO

link_physical_library (2); **physical_library** (3), **search_path** (3).

PSYN-029 (warning) The compiler cannot locate the physical library.

DESCRIPTION

The compiler is not able to locate a physical library to link with the logical library. This failure occurred because either the **physical_library** variable is not set or the named library does not exist.

WHAT NEXT

Be sure the name of the physical library is correct and is set properly in the **physical_library** variable. Also check that the search path is correctly stated in the **search_path** variable.

SEE ALSO

link_physical_library (2); **physical_library** (3), **search_path** (3).

PSYN-030 (error) Failed to find physical cell '%s'.

DESCRIPTION

This error occurs because the tool cannot find the named physical cell. The cell might be missing from the physical library, or the tool failed to link the two libraries because the cell in the logical library did not match any cell in the physical library.

WHAT NEXT

Ensure that the cell name in the logical library exactly matches the cell name in the physical library. Note that the tool is case sensitive. Ensure that the pin

names also match. If a pin in the logical cell does not exist in the corresponding physical cell, there is no match and the error occurs.

SEE ALSO

physopt(2)

PSYN-031 (error) Failed to find physical cell pin '%s'.

DESCRIPTION

This error occurs because the tool cannot find the named physical cell pin. The cell might be missing from the physical library or the cell pin in the logical library does not match any cell pin in the physical library. Another possibility is that the tool failed to link the logical library with the physical library.

WHAT NEXT

Ensure that the cell pin name in the logical library matches the cell pin name in the physical library. Note that the tool is case sensitive. If a pin in the logical cell does not exist in the corresponding physical cell, there is no match and the error occurs.

SEE ALSO

.nf physopt(2)

PSYN-032 (error) Site array has irregular rows specified.

DESCRIPTION

You receive this error message because the site array is not regular, which means that all sites in the rows do not have the required equal width and equal spacing between them. Both the **physopt** command and the **legalize_placement** command require that you specify the site array as regular in the input PDEF.

WHAT NEXT

Correct the site array definition in the PDEF so that it is regular. Then read it in using **read_pdef**.

SEE ALSO

read_pdef (2).

PSYN-033 (error) Site array has negative site count specified.

DESCRIPTION

You receive this error message because the input site array you defined has rows with a negative count of sites.

WHAT NEXT

Correct the input site array specification in the site array, and read it in using the **read_pdef** command.

SEE ALSO

read_pdef (2).

PSYN-034 (error) Library has no associated physical library.

DESCRIPTION

You receive this error message because you have not read in a physical library before you ran one of these commands: **create_placement**, **legalize_placement**, or **physopt**.

WHAT_NEXT

Be sure the name of the physical library is correct and is set properly in the **physical_library** variable. Also check that the search path is correctly stated in the **search_path** variable. Then invoke the command again.

SEE ALSO

create_placement (2), **legalize_placement** (2), **physopt** (2); **physical_library** (3), **search_path** (3).

PSYN-035 (warning) There is no physical library specified.

DESCRIPTION

You receive this error message because you did not specify a physical library before you issued a physopt command.

WHAT NEXT

Use the **physical_library** variable ("physical_library = ...") to indicate which library the design should be linking to. Also check that the search path is correctly stated in the **search_path** variable. Then invoke the command again.

SEE ALSO

link_physical_library (2); **physical_library** (3), **search_path** (3).

PSYN-036 (information) Linking logical library %s with physical library %s.

DESCRIPTION

This information message is to let you know that the compiler is loading the physical library into the system. This message is informational only and requires no action on your part.

WHAT NEXT

Every physical library you specify in the **physical_library** variable is to be loaded.

SEE ALSO

physical_library (3).

PSYN-037 (error) You must specify two PrimeTime images with two timing corners and SI enabled.

DESCRIPTION

You receive this error because **signoff_opt** is not able to automatically run **PrimeTime** with two timing corners and SI enabled. Thus, you must provide two PrimeTime saved sessions for Min and Max corner using **set_primetime_options**.

Optionally, you can also run your own Star RCXT runs, and provide directories defined by STAR_DIRECTORY command in the Star RCXT command file using **set_starrcxt_options**.

signoff_opt invokes **PrimeTime** timing engine to perform static timing analysis. With signal integrity effects enabled, such as delta delay or static noise, **PrimeTime SI** is used. **PrimeTime SI** always uses on_chip_variation (OCV) mode, therefore, if you have two timing corners with **set_min_library**, timing will be computed using both

timing corners as library OCV. This leads to pessimistic timing results which are not desired.

WHAT NEXT

There are several actions you can take to avoid this error message.

If you think you indeed WANT **signoff_opt** to perform on_chip_variation analysis based on the two timing corners that you have provided, you can use **set_operating_condition** command in **IC Compiler** to specify on_chip_variation mode. Moreover, if you have provided a signoff SDC file through **set_primetime_options** command, you must modify the **set_operating_condition** in that SDC file to specify on_chip_variation mode.

Alternatively, you can choose to run your own **PrimeTime SI** for both timing corners, individually. You can then save a session for each run using **save_session** command in **PrimeTime**, and give both sessions to **signoff_opt** using **set_primetime_options** commands as -max_image and -min_image.

Note when you run your own **PrimeTime**, you need to ensure:

- Both sessions contain same netlist comparing to IC Compiler
- Both sessions contain same timing exceptions and clock definitions
- Both sessions contain libraries that are also used in IC Compiler

If, for example, the timing exception needs to be different between your min and max **PrimeTime** runs (you have a false path in min corner, but not in max corner), this is not supported in regular **signoff_opt**. You must use MCMM capability of **signoff_opt** to define two scenarios, one for min and one for max.

EXAMPLES

In **IC Compiler**, you have both fast and slow libraries, with **set_min_library**, bc_wc operating condition, and delta delay turned ON:

- set link_libary "* slow.db fast.db"
- set_min_library -min fast.db slow.db
- set_operating_conditions -analysis_type bc_wc
- set_si_options -delta_delay true

In this case, **signoff_opt** will error out with this message.

If you choose to run **PrimeTime SI** on your own, you will need to run the following two **PrimeTime SI** runs:

- PrimeTime SI max corner
- PrimeTime SI min corner

In PrimeTime SI max corner, you will need:

- set si_enable_analysis true
- set link_path "* slow.db"
- read netlist
- read max corner sdc
- read max corner parasitics
- save_session -include noise pt_run.max

In PrimeTime SI min corner, you will need:

- set si_enable_analysis true
- set link_path "* fast.db"
- read netlist
- read min corner sdc
- read min corner parasitics
- save_session -include noise pt_run.min

Note the max corner sdc should contain the same exceptions and clock definitions comparing to the min corner sdc.

You can then give pt_run.max and pt_run.min to **set_primetime_options** as **-max_image** and **-min_image**, respectively, and proceed with **signoff_opt**. **signoff_opt** will use the setup information in max image and hold information in the min image to perform signoff based optimization. Hold information in max image and setup information in min image are ignored.

SEE_ALSO

signoff_opt(2),
set_primetime_options(2),
set_min_library(2),
set_opearting_conditions(2),
set_si_options(2)

PSYN-038 (error) Site array extends beyond core area.

DESCRIPTION

You receive this error message because the input site array you specified is larger than the core area defined in PDEF.

WHAT NEXT

Change the information in the input PDEF to match the site array and the core area definitions. Then read the input PDEF back in using the **read_pdef** command.

SEE ALSO

read_pdef (2).

PSYN-039 (warning) The '%s' cell in the '%s' technology library is being
marked as "dont_use".

DESCRIPTION

This warning occurs because the tool encountered a cell in the logical library but cannot find the cell's counterpart in the physical library. The tool marks this as a "dont_use" cell.

WHAT NEXT

To use this library cell, first create a physical library cell for it; and, then, use the **read_lib** command to read the physical library.

SEE ALSO

read_lib(2)

PSYN-040 (warning) Cell '%s' is being marked as "dont_touch" because it has

a fixed_placement attribute.

DESCRIPTION

You see this warning because a cell in your design bears a *fixed_placement* attribute in the input PDEF. The tool marks such a cell as "dont_touch".

WHAT NEXT

To modify the cell, remove the *fixed_placement* attribute in PDEF. Then read in the PDEF again, using the **read_pdef** command.

SEE ALSO

read_pdef (2).

PSYN-041 (error): The tool cannot place the block because it is over capacity (density is %5.1f%%).

DESCRIPTION

This error occurs because Std cells core area over utilized (more than 100%) so No area left for std cell placement. As a result the tool cannot produce a legal placement for your block.

WHAT NEXT

Increase the core site area in your Design Exchange Format (DEF) file by increasing the number of sites per row or increasing the total number of rows in the floorplan. Alternatively, use the initialize_floorplan command to make the same change(s).

SEE ALSO

initialize_floorplan(2)

PSYN-042 (error) There are blockages that lie partially or completely outside the bounds of the block.

DESCRIPTION

You receive this error message because the dimensions or locations of the specified blockages cause them to lie outside the block. Therefore, these blockages in your

design are located off the chip.

WHAT NEXT

Correct the core area to include all the blockages within the block. Or correct the locations or dimensions to fit within the block.

SEE ALSO

physopt (2).

PSYN-043 (warning) Some cells are located at invalid locations. The cells will be snapped to the nearest legal location.

DESCRIPTION

You see this warning because some cells were fed into the placement legalizer with an invalid seed location. This situation should not occur under normal circumstances.

One possibility for it happening here might be because the cells were placed on top of a blockage. Another possibility is that the cells were placed outside the boundary of the block.

The legalizer will snap these cells to their nearest valid location. But if the distance is considerably off, it is possible that long wire lengths will result and QOR might be degraded.

WHAT NEXT

If problems in timing arise because of the situations that produce these warnings, please file a STAR and notify Synopsys.

SEE ALSO

physopt (2), **legalize_placement** (2).

PSYN-044 (error) A legal placement could not be found.

DESCRIPTION

This error occurs because the tool cannot find a legal placement for your block. You probably have a site array that is smaller than the core area.

WHAT NEXT

Check the site array definition, increase the size of the site array, and rerun the command.

SEE ALSO

create_placement(2)
legalize_placement(2)
physopt(2)
read_pdef(2)

PSYN-045 (error) The following library pins does not have consistent directions
in the physical and logical library. This mismatch in pin direction will result in
ignore of that cell.

DESCRIPTION

You receive this error message because the directions you specified on the named pin are not the same in the logical and physical library descriptions.

WHAT NEXT

Examine the libraries and correct inconsistences in the pin directions. Then recompile the libraries using the **read_lib** command.

SEE ALSO

read_lib (2).

PSYN-046 (warning) The cell %s is multirow high. This can degrade the quality of the placement result.

DESCRIPTION

You see this warning because the height of the named cell spans multiple rows. The quality of the overall placement result might be degraded.

WHAT_NEXT

This message is a warning only. The detailed placer will still produce valid results. But if the results are not satisfactory, discontinue the use of multirow-high cells in your design.

SEE ALSO

physopt (2), **legalize_placement** (2).

PSYN-047 (error) Cannot find site definitions in physical library.

DESCRIPTION

This error message indicates one of two things:

- There is no site definition in any physical library.
- There is no accessible physical library.

The site definition contains the description of the sites that can be used in the design, including, for each site, the site type, site width, and site height. This information is necessary to check whether the core area from the site array is consistent with the given core area.

WHAT NEXT

Add site definition information and regenerate the physical library using Library Compiler and the **read_lib** command.

SEE ALSO

read_lib (2).

PSYN-048 (warning) Unrecognized distance unit in the physical library. 1um assumed.

DESCRIPTION

You receive this warning because you have specified a distance unit that the compiler does not recognize. The only distance units the physical library supports are 1um or 1mm.

WHAT_NEXT

Be sure the physical distance unit in your design is either 1um or 1mm. Then regenerate the physical library using Library Compiler and the **read_lib** command.

SEE ALSO

read_lib (2); **physical_library** (3).

PSYN-049 (warning) Overwriting the given core area (%f %f) (%f %f) with the new core area (%f %f) (%f %f).

DESCRIPTION

This warning indicates the presence of an inconsistency between the given core area and the core area defined in the site array. The meaning of the message in this case is that the compiler will adjust the core area, using the site array, and ignore the given core area.

WHAT NEXT

Check the PDEF file to be sure the given core area correctly matches the core area defined in the site array.

PSYN-050 (warning) The given core area (%f %f) (%f %f) is different from the core area (%f %f) (%f %f) in the site array definition in the PDEF file.

DESCRIPTION

This warning indicates the presence of an inconsistency between the given core area and the core area defined in the site array.

WHAT NEXT

Check the PDEF file to be sure the given core area correctly matches the core area defined in the site array.

PSYN-051 (warning) Cannot find site %s in physical library.

DESCRIPTION

This warning message occurs when site definition is not defined in the physical library. Because the compiler cannot find the site in the physical library, it cannot determine whether this site belongs to CORE or IO. This warning indicates that in this case the compiler will ignore the site.

WHAT NEXT

Add the site definition to the physical library. Then recompile the physical library using the **read_lib** command.

SEE ALSO

read_lib(2)

PSYN-052 (error) Error in argument '%s'. '%s'.

DESCRIPTION

This error message occurs when an argument in your library has an incorrect value. Either the compiler could not find the expected object, or the number of arguments is invalid.

WHAT NEXT

Refer to the command man page for complete information about using the command.

PSYN-053 (information) '%s'.

DESCRIPTION

This information message advises you of the progression of a particular physical optimization command.

WHAT NEXT

This is only an information message. No action is required.

However, you can refer to the command man page for complete information about the physical optimization command.

PSYN-054 (information) Use the -verbose option to get details about the legality violations.

DESCRIPTION

This information message occurs when legality violations exist after detailed placement. Use the **-verbose** option to display more detailed information about each violation.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

legalize_placement(2)

PSYN-055 (warning) Cell %s overlaps with cell %s.

DESCRIPTION

You see this warning to inform you that one cell overlaps one of the other cells in the design. The placement is not valid.

WHAT NEXT

To make the placement valid, use the **legalize_placement** command.

SEE ALSO

legalize_placement (2).

PSYN-056 (warning) Cell %s overlaps with a blockage.

DESCRIPTION

This warning informs you that the named cell overlaps one of the blockages in the design. The placement of the cell is not valid.

WHAT NEXT

To make the placement valid, use the **legalize_placement** command.

SEE ALSO

legalize_placement (2).

PSYN-057 (warning) Cell %s is not on a row.

DESCRIPTION

You see this warning because the named cell does not lie on one of the site rows specified in the design. The placement is not valid.

WHAT NEXT

To make the placement valid, use the **legalize_placement** command.

SEE ALSO

legalize_placement (2).

PSYN-058 (warning) The pin direction of '%s' pin on '%s' cell in the '%s' technology library is inconsistent with the same-name pin in the '%s' physical library. No physical link for the logical lib cell.

DESCRIPTION

You see this warning because the specified direction of a cell pin in the technology library is different from that of the cell pin of the same name in the physical library. The logical cell will not be linked with the cell of the same name in the physical library.

WHAT NEXT

The pin direction attributes should be the same in both libraries. Make the correction and run Library Compiler again. Or make sure the technology library and physical library matches.

SEE ALSO

read_lib (2).

PSYN-059 (warning) Initial location does not exist for cell %s.

DESCRIPTION

You see this warning because you have not specified the initial location for the named cell. For detailed placement, the initial location is required.

WHAT NEXT

To place the cell, use the **create_placement** command or the **legalize_placement** command with the *-eco* mode.

SEE ALSO

create_placement (2), **legalize_placement** (2).

PSYN-060 (error) An error has occurred in the execution of the detailed placer.

DESCRIPTION

This error occurs because the tool has encountered an error while trying to legalize the placement.

WHAT NEXT

Examine the output of the detailed placer for error information.

SEE ALSO

legalize_placement(2)

PSYN-061 (error) lib cell '%s' of cell %s is illegal for all sites in

the block.

DESCRIPTION

You receive this message because cells exist that are illegal for all sites inside the block. Under normal circumstances, this should occur only when there are problems with the library or the row definition or when cell pins and power straps overlap.

WHAT NEXT

Use the GUI to manually check the illegal lib cell against the floorplan. Set the **psyn_debug_dpi_lib_cell*** variable in psyn_shell (.tcl) to print a detailed explanation of why the cell is illegal for all sites. Use the following format, where you replace *cellname* with the actual name of the lib cell in the message:

set psyn_debug_dpi_lib_cell *cellname*

Once you set this variable, the **legalize_placement** command can print a detailed message containing information pertaining to the pins that overlap with power straps.

SEE ALSO

legalize_placement(2) psyn_debug_dpi_lib_cell(3)

PSYN-062 (error) Unable to find legal locations for all multi-row cells.

DESCRIPTION

You receive this message because, although there are legal locations for all cells, as the multi-row cells are placed, their placements obstruct other multi-row cells from being placed. This error should be extremely rare.

WHAT NEXT

Ensure that the multi-row cells do not have overly-severe restrictions. If the error still occurs, increase the size of the block.

PSYN-063 (warning) Some areas of the block have densities much greater than 100%%.

For example: rows %d to %d have a density of %.1f%%.

DESCRIPTION

You receive this message because some consecutive rows have densities of much greater than 100%, so it is unlikely that a good placement can result when the cells in these rows are legalized.

WHAT NEXT

If there are no timing issues with the resulting placement, no action is required. However, if there are timing problems, examine the coarse placer to determine why it created a netlist with consecutive rows over capacity. This could occur due to an unusual characteristic of the block being placed, or it could be due to a bug in the placement that is generated. In the latter case, please contact Synopsys.

PSYN-064 (warning) The average displacement of a cell after legalization is %.1f rows.

DESCRIPTION

You receive this message because when the output of the coarse placer was legalized, the average displacement of a cell was greater than the amount that is considered to be normal. This large displacement might mean that a poor placement results after it has been legalized. Examine the timing of the circuit to see if there are any unusual problems.

WHAT NEXT

This warning should never happen under a usual run. However, it might be caused by combinations of high densities, blockages, and/or over-restrictive preroutes or power straps that restrict where cells can be placed.

Determine if any of these conditions apply, and do whatever you can to make the placement less restrictive. If the block does not seem unusual in terms of density, blockages, and/or preroutes, please report this problem to Synopsys.

PSYN-065 (error) The site array contains more than two types of rows based on their heights.

DESCRIPTION

You receive this message because the site array cannot contain more than two types

of rows based on their heights.

WHAT NEXT

Update the site array information so that the number of distinct heights for all rows is no more than two.

PSYN-066 (warning) This obstruction with (%f %f) (%f %f) is exceeding its parent cluster boundary (%f %f) (%f %f).

DESCRIPTION

You receive this message because the **create_obstruction** command creates an obstruction that might be partially or completely outside its parent boundary.

WHAT_NEXT

Issue another **create_obstruction** command to overwrite the previous obstruction.

SEE ALSO

create_obstruction (2).

PSYN-067 (warning) The obstruction layer %d for %s is ignored. Obstruction %s is treated as a placement obstruction.

DESCRIPTION

You receive this message because the layer id is not defined in the PDEF, and is ignored. This obstruction is treated only as a placement obstruction.

WHAT_NEXT

Examine the PDEF to determine if the layer ID has been defined.

PSYN-068 (warning) The row (%f %f) (%f %f) exceeds the core

area (%f %f) (%f %f).

DESCRIPTION

You receive this message because the **create_site_row** command has created a row that exceeds the core area.

WHAT_NEXT

Determine the proper parameters setting for the **create_site_row** command to ensure that it does not exceed the core area.

SEE ALSO

create_site_row (2).

PSYN-069 (warning) The lib cell (%s) height (%d) is different from its site height(%d).

DESCRIPTION

You receive this message because the **lib cell height is different from its site height.**

WHAT_NEXT

Double check the library cell height and its associated site master height to ensure that this library cell has no problem.

SEE ALSO

PSYN-070 (error) The 'read_phys_info_db' command has not read in the specified phys_info_db '%s'.

DESCRIPTION

You receive this message because the value of the **read_phys_info_db** command **-phys_info_db** option must be a database the command has read in. It must be a placed net list.

WHAT NEXT

Use the **list** command with the **-design** option to determine the name of a placed database file that was read in. Read in this file with **read_phys_info_db** command by specifing that name as the **-phys_info_db** argument.

SEE ALSO

list (2), **read_phys_info_db** (2).

PSYN-071 (error) Specified phys_info_db '%s' is not unique in memory.

DESCRIPTION

You receive this message because the **-phys_info_db** argument must be a database read in by the **read_phys_info_db** command. This database must be a placed netlist.

WHAT NEXT

Choose a placed database file and use the **read_phys_info_db** command to read it. Use the **list** command with the **-design** option to determine the name for the read-in database. Specify the unique name (for example, one of the form <file>:<name>) as the **-phys_info_db** argument.

SEE ALSO

read_phys_info_db (2).

PSYN-072 (error) phys_info_db '%s' has no physical information and is not a placed netlist.

DESCRIPTION

You receive this message because the argument for the **read_phys_info_db** command must be a placed netlist.

SEE ALSO

read_phys_info_db (2).

PSYN-073 (error) Cannot find hierarchy '%s' in phys_info_db '%s'.

DESCRIPTION

You receive this message because the specified **-phys_info_db** argument must be a database read in by the **read_phys_info_db** command. This database must be a placed netlist. The *current design* must either have the same specified hierarchy as this database or be a subhierarchy of it.

WHAT NEXT

If the *current design* is a subhierarchy of this database, use the **-path_for_phys_info** argument to specify the instance of *current design* in the database.

SEE ALSO

current_design (2), **read_phys_info_db** (2).

PSYN-074 (error) Cannot find hierarchy '%s' (under instance path '%s') in phys_info_db '%s'."

DESCRIPTION

You receive this message because the **-phys_info_db** argument must be a database read in by the **read_phys_info_db** command. This database must be a placed netlist.

The *current design* must either have the same specified hierarchy as this database or be a subhierarchy of it.

WHAT NEXT

If the *current design* is a subhierarchy of this database, use the **-path_for_phys_info** argument to specify the instance of *current design* in the database.

SEE ALSO

current_design (2), **read_phys_info_db** (2).

PSYN-075 (information) Deriving physical timing model for

design ’%s’.

The compile_physical command bases its timing calculation for wires on the information on floorplan, placement and routing.

This message is for informational purpose.

PSYN-076 (Error) Back-annotation canceled.

DESCRIPTION

You receive this message because the back-annotation structure has not been initialized.

WHAT NEXT

The **load_estimate** command builds such a structure in the database.

SEE ALSO

load_estimate (2).

PSYN-077 (error) Invalid value %f for %s.

DESCRIPTION

You receive this message because an invalid value has been supplied to the parameter.

WHAT_NEXT

See the appropriate man page to determine the proper usage.

PSYN-078 (Error) Cell %s has no location.

DESCRIPTION

You receive this message because the specified cell in the design does not have a specified location. Each cell must have a location in order to derive physical information for the design.

WHAT_NEXT

Ensure that the physical information database file is a placed netlist.

PSYN-079 (Error) Cell %s has location.

DESCRIPTION

You receive this message because the specified cell in the design has a specified location. Each cell must not have a location for a design to be synthesized.

WHAT_NEXT

Ensure that the *current design* is not a placed netlist.

SEE ALSO

current_design (2).

PSYN-080 (Error) No floorplan is defined for the current design for incremental physical synthesis.

DESCRIPTION

You receive this message because a design without floorplan information is run with place_opt or physopt.

WHAT_NEXT

Use the initialize_floorplan or read_def to create/read floorplan information for the current design.

SEE ALSO

current_design (2), **compile_physical** (2), **initialize_floorplan** (2), **read_def** (2).

PSYN-081 (Error) Lower-left corner coordinates are not smaller

than upper-right corner coordinates.

DESCRIPTION

You receive this message because the coordinates of a rectangle are not given in order from the lower-left corner to the upper-right corner or the coordinates form a line instead of a rectangle.

WHAT_NEXT

Place the lower-left corner coordinates before the upper-right corner coordinates, and ensure that it forms a valid rectangle.

PSYN-082 (error) The ungroup option has been disabled. Use "ungroup -all -flatten" before using "physopt".

DESCRIPTION

You receive this message because the **physopt** command with the **-ungroup** option does not retain the original attributes. If you want to retain original attributes, use the **ungroup** command with the **-all -flatten** options.

WHAT_NEXT

Use **ungroup -all -flatten**, and then use **physopt**.

SEE ALSO

physopt (2), **ungroup** (2).

PSYN-083 (information) User-specified wire load models or library wire load models are ignored in physical synthesis.

DESCRIPTION

You receive this message because timing models are derived for physical synthesis based on design physical characteristics in physical synthesis, and any customer wire load model specified for the design is ignored.

WHAT_NEXT

No action is necessary.

PSYN-084 (Error) Command %s should be issued before issuing command %s.

DESCRIPTION

This message indicates that you haven’t run set_wire_capacitance_multiplier or set_wire_capacitance_multiplier before running set_wire_min_resistance_multiplier or set_wire_min_capacitance_multiplier.

WHAT NEXT

First run set_wire_capacitance_multiplier/set_wire_capacitance_multiplier before running this command. Use man page to find out the proper usage.

PSYN-085 (Error) The value of attribute %s is smaller than the value of attribute %s.

DESCRIPTION

You receive this message because you have not specified the correct value for the attribute.

WHAT NEXT

Specify the correct value for the attribute. See the appropriate man page to determine the proper usage.

PSYN-086 (warning) Net ’%s’ is connected to a pad cell and other cells.

DESCRIPTION

You receive this message because the specified port net is connected to a pad cell and to other cells, some of which might be pad cells.

WHAT NEXT

No action is required.

PSYN-087 (information) Port '%s' inherits its location from %s pin '%s/%s'.

DESCRIPTION

You receive this message to inform you that the port without a specified location will inherit its location from a pin that the port connects with. And the pin should belong to a fixed-placement pad-cell or macro-cell. If it is the macro-cell-pin, it must be the unique pin that connects with port.

The cell will be regarded as pad-cell, (1) If the corresponding logical db library cell bears **is_pad** attribute; (2) Or the pin itself bears **is_pad** attribute; (3) Or the design cell instance is IOPadCell/FlipChipPadCell/CornerPadCell; (4) Or the corresponding reference library cell is IOPadCell/FlipChipPadCell/CornerPadCell.

WHAT NEXT

This is an informational message only. No action is required on your part.

PSYN-088 (information) Setting a dont_touch attribute on net '%s' because it is connected to a pad cell.

DESCRIPTION

You receive this message to inform you that a dont_touch attribute is placed on a net that is connecting a port to a pad cell. This prevents transformations such as buffering from being performed on the net.

WHAT NEXT

This is an informational message only. No action is required on your part.

PSYN-089 (error) Cannot find path '%s' or its hierarchy in placed

database.

DESCRIPTION

You receive this message because the **-inst_name_in_physical_db** argument must start with the design and end with the cell instance, and its hierarchy must exist in the instance tree of the design.

WHAT NEXT

Examine the instance path hierarchy for consistency with the design and compliance with the Synopsys format. For example, a leading slash (/) is not allowed; and, the instance path hierarchy should be something similar to *test_design/BLK/o*.

PSYN-090 (error) Specified -physical_db '%s' is not found or has not been read into memory.

DESCRIPTION

You receive this message because the **-physical_db** argument must be in the format of file:design, where file is a database file and has a placed netlist. The file must already be read into memory.

WHAT NEXT

Ensure that the file has been read in by the **read_db** command, and the design exists in the placed database.

SEE ALSO

read_db (2).

PSYN-091 (error) Specified '%s' '%s' is not found or cannot be read into memory.

DESCRIPTION

You receive this message because the file you specified for **-physical_db_file** or **-subdesign_mapped_db_file** argument cannot be found or is not a database file.

WHAT NEXT

Ensure that the file exists and is reachable by a search path.

PSYN-092 (error) Specified -physical_db '%s' is missing the -inst_name_in_physical_db argument.

DESCRIPTION

You receive this message because the **-inst_name_in_physical_db** argument must exist if the **-physical_db** argument is specified.

WHAT NEXT

Choose the instance path in the placed database file and specify that path as the **-inst_name_in_physical_db** argument.

SEE ALSO

read_db (2).

PSYN-093 (error) Specified -physical_db_file '%s' is missing the -inst_name_in_physical_db argument.

DESCRIPTION

You receive this message because the **-inst_name_in_physical_db** argument must exist if the **-physical_db_file** argument is specified.

WHAT NEXT

Choose the instance path in the placed database file, and specify that path as the **-inst_name_in_physical_db** argument.

PSYN-094 (error) Specified inst_name_in_physical_db '%s'

does not have reference design in placed database.

DESCRIPTION

You receive this message because the reference design of the **-inst_name_in_physical_db** argument must exist and be linked in the placed database that the **-physical_db_file** argument specifies.

WHAT NEXT

Choose the correct instance path and ensure that the link is correct.

PSYN-095 (error) The reference design name of the specified instance '%s' does not match the current_design name.

DESCRIPTION

You receive this message because the *current design* must either have the same hierarchy as this database or be a subhierarchy of the placed database that the **-physical_db_file** argument specifies. The *current design* name must be the same as the reference design of the instance cell.

WHAT NEXT

Set the correct *current design* and specify the correct path.

SEE ALSO

current_design (2).

PSYN-096 (information) Deriving initial location for cell %s.

DESCRIPTION

You receive this message because

Initial Location does not exist for the cell. Physical compiler will derive the initial location as -eco option is specified.

WHAT NEXT

Nothing. This is for information only.

PSYN-097 (error) The height (%f) of the structure block %s is more than the height (%f) of the core area.

DESCRIPTION

This error occurs because the tool has found that the structure block does not fit in the current core area. This might be due to overestimating the size of the structure block for the current core area.

WHAT NEXT

Redo the floorplan to increase the core area or use Module Compiler to shrink the structure block.

SEE ALSO

compile(2)

PSYN-098 (warning) The width (%f) of structure block %s is more than the width (%f) of the core area.

DESCRIPTION

You receive this message because the structure block might be overlapped with other cells in the current core area. This is might be due to over-estimating the structure block for the current core area.

WHAT NEXT

If placement fails, redo the floorplan to increase the core area, or use Module Compiler to shrink the structure block.

PSYN-099 (warning) The width (%f) of expanded structure block %s is more than the width (%f) of the core area and will not be expanded.

DESCRIPTION

You receive this message because the structure block is expanded by using the utilization (current total cell area / core area) and its width exceeds the core area, so it might be overlapped with other cells in the current core area. When this

occurs, the width is not expanded by using the utilization.

WHAT NEXT

If placement fails, redo the floorplan to increase the core area, or use Module Compiler to shrink the structure block.

PSYN-100 (error) Layer '%s' is missing the '%s' attribute.

DESCRIPTION

You receive this message because some of the required information described below is missing. Every metal layer in the physical library must specify information about pitch, default width, preferred routing direction, and resistance and capacitance per square.

WHAT_NEXT

Generate the physical library file from the source, and use the **read_lib** command to read it in. Ensure that the required layer information is present.

SEE ALSO

read_lib (2).

PSYN-101 (warning) Layer '%s' is missing the optional '%s' attribute.

DESCRIPTION

This warning occurs because the required information described below is missing. Every metal layer in the physical library must specify information about edge capacitance. This is useful to improve the correlation between preroute and postroute timing and timing after routing.

WHAT_NEXT

Generate the physical library file from the source, and use the **read_lib** command to read it in. Ensure that the required layer information is present.

SEE ALSO

read_lib(2)

PSYN-102 (warning) Layer name '%s' is invalid.

DESCRIPTION

You receive this message because the layer name specified in user TCL variables cannot be found in the library. This layer is ignored.

WHAT_NEXT

Ensure that the layer name is present in the physical library.

PSYN-103 (error) Keep-out Area for cell '%s' is larger than the core Area.

DESCRIPTION

You receive this message because the hard keep-out distance is causing the keepout area corresponding to the specified cell to be greater than the core area. When this condition occurs, no placement can be found.

WHAT_NEXT

Ensure that the hard keepout value is more reasonable or increase the core area to accommodate the keepout area.

PSYN-104 (warning) Soft keepout channel width is significantly large considering core area width or height. Ignoring soft keepout channel width for placement.

DESCRIPTION

You receive this message because the soft keepout channel width threshold specified by the **placer_soft_keepout_channel_width** variable is very large: It is greater than 33% of either the core area width or height. This condition can potentially lead to poor quality results. Hence, it is ignored for the purpose of obtaining placement.

WHAT_NEXT

Ensure that the soft keepout channel width value is smaller or increase the core area to accommodate the soft keepout channel width value.

SEE ALSO

placer_soft_keepout_channel_width (3).

PSYN-105 (information) The design has %d physical cells.

DESCRIPTION

You receive this message to inform you that the specified number of physical cells exist in the design. These physical cells must have the FIXED_PLACEMENT attribute with location.

WHAT NEXT

This is an informational message only. No action is required on your part.

PSYN-106 (error) Cannot find a valid site for %s.

DESCRIPTION

You receive this message because a valid site for this movable cell is not available. The site might not exist in the floorplan, or it might have been internally filtered out because this site is used by a black box cell and is not used by any other functional cell.

This filtering process is needed to support mixed horizontal and vertical rows in the site array. A site that is used only by unknown function cells is filtered out. Usually such a cell must be fixed, and sometimes this occurs in the opposite direction of rows.

WHAT_NEXT

Change the input PDEF to set this cell to be fixed placement, and use the **read_pdef** command to read it back in.

SEE ALSO

read_pdef (2).

PSYN-107 (warning) Overwriting the existing core area (%f %f)

(%f %f) with the new core area (%f %f) (%f %f).

DESCRIPTION

You receive this message because there is an inconsistency between the specified new core area and the existing core area. The existing core area is overwritten.

WHAT_NEXT

Examine the coordinates to ensure that the new core area is correct and is intended to overwrite the existing one.

PSYN-108 (error) Cannot find this layer %s in the LAYER_DEF section.

DESCRIPTION

You receive this message because the layer_name used in the VIA_RECT clause is not defined in the LAYER_DEF section. This VIA_RECT information is not read in.

WHAT_NEXT

Add this layer to the LAYER_DEF section. For example:

```
(LAYER_DEF
 (LAYER this_layer_was_missing 1 )
 ...
)
```

PSYN-109 (warning) No valid site for cell %s. Placement is not legalized for this cell.

DESCRIPTION

You receive this message because

This message indicates the tool cannot find a valid site to place this cell. since you set psyn_disable_site_check to true, the tool will continue to run. But you have to manually legalize the placement for this cell in the end.

WHAT_NEXT

Change the input PDEF to set this cell to be fixed placementand read it back in using **read_pdef**.

PSYN-110 (warning) Current floorplan is highly utilized. Switching back to normal legalization mode.

DESCRIPTION

This warning occurs because the current floorplan is highly utilized and the congestion cost cannot be met during cell legalization. To achieve a legal placement, the tool defaults back to using normal legalization where congestion is not a cost factor. This typically occurs when a design is highly utilized and also has high routing congestion, so local congestion fixes do not address the global congestion issue with this design.

WHAT_NEXT

Your design is probably highly congested. You must run the **physopt** command with the **-congestion** option to resolve the congestion problems. Additionally, consider using the **physopt** command with the **-congestion -area_recovery** options to try to minimize utilization and congestion problems.

SEE ALSO

physopt(2)

PSYN-111 (warning) Given coordinates are out of the core area.

DESCRIPTION

You receive this message because the given coordinates specify an area that falls partially or totally outside of the core area. This message does not stop the command from running.

WHAT_NEXT

Examine the given coordinates to ensure that they are valid for your purpose.

PSYN-112 (error) Cannot find PDEF layer ID for the given %s

layer name in the current design database.

DESCRIPTION

You receive this message because the PDEF layer ID was not found for the specified layer name. It might be because the layer name is defined, or the pdef was not read, or the pdef was missing the LAYER_DEF part.

WHAT_NEXT

Determine if the specified layer name is correct, if the PDEF was read, if the PDEF has the LAYER_DEF part.

PSYN-113 (warning) Obstruction %s is treated as a placement obstruction.

DESCRIPTION

You receive this message because the layer is not specified. The specified obstruction is considered to be only a placement obstruction.

WHAT_NEXT

Determine if you actually want to create a placement obstruction. If you want to create a routing obstruction on a specific layer, you should define the layer name by using the **-layer** option.

PSYN-114 (warning) No location specified for library pin %s of pad cell %s. Its location is assigned to the center of the cell.

DESCRIPTION

This error occurs because the library pin of a pad cell has no location specified in the physical library. The tool assigns the pin’s location to the center of the cell for placement. This might affect the accuracy of timing calculation. You can ignore this warning if this is a PAD pin for an IOPAD cell and is not intended to be routed in the core area.

WHAT NEXT

Ensure that this is not a problem for your library. If necessary, correct the definition of the pin in the physical library and recompile it by using the **read_lib**

command.

SEE ALSO

read_lib (2)

PSYN-115 (error) There is no capacitance unit or time unit specified in the logical library.

DESCRIPTION

This error occurs because the tool cannot find a capacitance unit or time unit specified in the logical library. The compiler needs a capacitance unit and time unit to convert physical library units to logical library units.

WHAT_NEXT

Ensure that there is a capacitance unit and a time unit in the logical library. Then use Library Compiler to recompile it.

SEE ALSO

compile(2)

PSYN-116 (warning) Cell %s violates one or more power straps.

DESCRIPTION

This warning occurs because the tool has found that the named cell violates one or more of the power straps in the design. The violation occurs because the placement is not legal.

WHAT_NEXT

Use the **legalize_placement** command to make the placement legal.

compile(2)
legalize_placement(2)

PSYN-117 (error) Port ’%s’ cannot inherit its location from %s

pin '%s/%s', %s

DESCRIPTION

This error occurs because the port does not have a specific location. The tool will try to inherit the port location from the a pin that connects with port. And the pin should belong to a fixed-placement pad-cell or macro-cell. If port connects with multiple pad-cell-pins, port will inherit from first pad-cell-pin. If port connects with macro-cell-pin, the pin should be the unique pin connects with port.

But currently the cell of the pin is neither a pad-cell nor a macro-cell. Or the port connects with multiple cell-pins. Or the port direction and the macro-cell pin direction are opposite. Or the pad-cell/macro-cell does not define fixed-placement. Or the tool cannot find the pad-cell/macro-cell location. Or the tool cannot find the pin location of the pad-cell/macro-cell.

The cell will be regarded as pad-cell, (1) If the corresponding logical db library cell bears **is_pad** attribute; (2) Or the pin itself bears **is_pad** attribute; (3) Or the design cell instance is IOPadCell/FlipChipPadCell/CornerPadCell; (4) Or the corresponding reference library cell is IOPadCell/FlipChipPadCell/CornerPadCell.

WHAT NEXT

Check the logical library to see if the cell bears the **is_pad** attribute using command "get_attribute". Also check the DEF file to see if fixed placement is defined for the cell.

SEE ALSO

read_def(2)
get_attribute(2)

PSYN-118 (error) Cannot determine a keepout type.

DESCRIPTION

You receive this error message because the **create_keepout_area** command expects the keepout type to be defined as soft or hard.

WHAT NEXT

Specify the proper keepout type as soft or hard, and rerun the testcase.

SEE ALSO

create_keepout_area (2), **remove_keepout_area** (2).

PSYN-119 (error) Cannot determine cell names.

DESCRIPTION

This error occurs because the tool cannot find a list of cell names that identify target cells. When you invoke the **create_keepout_area** command, you must identify the target cells that the command is to process.

WHAT NEXT

Specify the cell names or reference name for the library cell, and rerun the test case.

SEE ALSO

create_keepout_area(2)
remove_keepout_area(2)

PSYN-120 (error) Cannot determine margin parameters.

DESCRIPTION

You receive this error message because when you run the **create_keepout_area** command, you must provide a list of margin parameters. Margin parameters are of the form {left_x bottom_y right_x top_y}. All of these parameters must be nonnegative quantities. Microns are the units for specification.

WHAT NEXT

Specify proper margin parameters for the **create_keepout_area** command.

SEE ALSO

create_keepout_area (2).

PSYN-121 (Error) Error in argument '%s': '%s'.

DESCRIPTION

You receive this message because the argument has the wrong value. Either the expected object has not been not found or the number of arguments is not right.

WHAT_NEXT

See the appropriate man page for the proper usage.

PSYN-122 (warning) Instance %s does not have a FIXED_PLACEMENT attribute.

DESCRIPTION

This warning occurs because only cells bearing the FIXED_PLACEMENT attribute can have a keepout area. The tool ignores cells that do not have the attribute. The cell or reference you specified for the **create_keepout_area** command does not have this attribute.

WHAT NEXT

Set the FIXED_PLACEMENT attribute on the relevant cell in the Physical Design Exchange FormAT (PDEF) file.

SEE ALSO

create_keepout_area(2)
read_pdef(2)
report_keepout_area(2)

PSYN-123 (warning) Instance %s already has a keepout of type %s with margin parameters %f %f %f %f. It will be overwritten.

DESCRIPTION

For a fixed cell, only one soft or one hard keepout is used. If more than one keepout is defined using **create_keepout_area**, the most recent one overwrites the previous one.

The instance named in this message already has a keepout associated with it. That keepout will be overwritten by the current one.

WHAT_NEXT

This is a warning only. If the placement is not satisfactory, check the keepout area using **report_keepout_area**.

SEE ALSO

create_keepout_area (2), **report_keepout_area** (2).

PSYN-124 (warning) Instance %s does not have a keepout of type %s associated with it. This command will be ignored.

DESCRIPTION

This warning occurs because the tool has found that the named instance does not have a keepout of the specified type associated with it. Keepout removal for such a cell is not possible. The tool ignores the **remove_keepout_area** command.

WHAT_NEXT

Use the **report_keepout_area** command to check cells with existing keepouts associated with them.

SEE ALSO

create_keepout_area(2)
remove_keepout_area(2)
report_keepout_area(2)

PSYN-125 (error) Physical libraries %s and %s have conflicting technology data.

DESCRIPTION

You receive this message because conflicts exist in technology data between the specified multiple physical libraries. The comparison is made between the first specified library and all other libraries. Any conflicting data found between any two libraries results in this error.

WHAT_NEXT

Reorder the libraries so that the first library contains data that is a superset of the libraries that follow it. This technique works unless there are true differences in the technology data values between the compared physical libraries.

PSYN-126 (warning) Net %s has no back-annotated

capacitance. The report ignores this net.

DESCRIPTION

You receive this message because the reported net does not have a back-annotated capacitance value. It should have back-annotated capacitance for comparison purposes. If it does not have back-annotated capacitance, the net is not considered in the report.

WHAT_NEXT

Before executing this command, either read a database with back-annotated capacitance on the net, or execute the **set_load** command on the net to explicitly set the capacitance value.

SEE ALSO

set_load (2).

PSYN-127 (error) Design has no back-annotated capacitance.

DESCRIPTION

You receive this message because the design does not have back-annotated capacitance with which to compare estimated capacitance.

WHAT_NEXT

Before executing this command, either read a post-route database, or execute the **set_load** command on the nets of the design to explicitly set the capacitance value.

SEE ALSO

set_load (2).

PSYN-128 (Warning) Object '%s' belongs to another bound '%d' and is ignored.

DESCRIPTION

You receive this message because the specified object in the object list of the **set_bounds** command is ignored because it belongs to another bound.

WHAT_NEXT

Use the **report_bounds** command to determine the bound to which this object belongs, and use the **remove_bounds** command to reorganize the bounds in the design.

SEE ALSO

remove_bounds (2), **report_bounds** (2), **set_bounds** (2).

PSYN-129 (information) The bound %s is created succesfully.

DESCRIPTION

You receive this message to inform you that the **create_bounds** command has just created a bound with the specified name. You can use this name in the **remove_bounds** command to remove the bound. You can use the **report_bounds** command to review all bounds in the design. You can use the **attach_bounds** command to attach cells to the bound. You can use the **detach_bounds** command to detach cells from the bound.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

remove_bounds (2), **report_bounds** (2), **create_bounds** (2), **attach_bounds** (2), **detach_bounds** (2).

PSYN-130 (Warning) Bound ID '%d' is invalid and is ignored.

DESCRIPTION

You receive this message because the specified bound ID in the object list of the command is invalid and, so, it is ignored.

WHAT_NEXT

Use the **report_bounds** command to check the bound ID.

SEE ALSO

report_bounds (2).

PSYN-131 (error) Design is not test ready to order the scan chains.

DESCRIPTION

This error occurs because the design is not test ready. The tool cannot order the scan chains on this design. The design might not be scan replaced or the design might have test rule violations.

WHAT NEXT

Ensure that the design is scan replaced. Run the **check_test** command to ensure that the design does not have any test rule violations.

SEE_ALSO

check_test(2)
physopt(2)
report_test(2)

PSYN-132 (warning) MC-Pro license could not be checked out.

DESCRIPTION

MC-Pro license could not be checked out. Structured placement constraints will be ignored.

WHAT_NEXT

Make sure that MC-Pro license is available to you at your site.

PSYN-133 (warning) %d thin pnets were found along the site array direction. These are filtered out for legalization.

DESCRIPTION

This warning occurs because pnets exist in the floorplan that run along the site row direction. This might interfere with the legalization of cells, because of redundant definition of power and ground rails. The tool automatically removes these for legalization purposes.

PSYN-134 (information) Current design has no violation.

DESCRIPTION

This informational message tells you that the current design has no violations when you run the **create_buffer_tree** or **remove_buffer_tree** command. This is an informational message only. No action is required on your part.

WHAT_NEXT

To avoid receiving this message, you can set tighter constraints on the current design, then rerun the command.

SEE ALSO

create_buffer_tree (2), **remove_buffer_tree** (2).

PSYN-135 (warning) %s '%s' cannot be found in design '%s'.

DESCRIPTION

This warning messages tells you that the named object you searched for in the specified design cannot be found. This failure might have occurred because the object name is misspelled.

WHAT_NEXT

Check the spelling of the object, then rerun the command.

PSYN-136 (error) Design '%s' is not a placed netlist.

DESCRIPTION

This error message tells you that you used the **create_buffer_tree** or **remove_buffer_tree** command, but there is no placement information on the design.

WHAT_NEXT

Use the **create_placement** or **physopt** command to set placement information on the design. Then, rerun the command.

SEE ALSO

create_buffer_tree (2), **create_placement** (2), **physopt** (2), **remove_buffer_tree** (2).

PSYN-137 (warning) Skipping driver %s for HFS ('%s' %s).

DESCRIPTION

You receive this warning message because the **create_buffer_tree** and **remove_buffer_tree** commands cannot run if any of the following are true:

- The specified driver is not an output pin.
- The driver is a tristate driver.
- The driver is a pad.
- The driver does not drive a load.

In addition, the specified driver must drive a Steiner routable net with either the **ideal_net** or **dont_touch** attribute set.

The **create_buffer_tree** command cannot run on hierarchical pins. Therefore, the drivers specified with **create_buffer_tree -from** cannot be hierarchical pins, and the nets specified with the **-net** option cannot have a hierarchical pin as a driver.

WHAT NEXT

Examine the arguments and remove the offending driver or net from the argument list and rerun the command.

This warning also occurs if you are running **create_buffer_tree** on a net with more fanout than the amount specified by the **high_fanout_net_threshold** variable. Change the **high_fanout_net_threshold** variable to a higher value to resolve the warning.

SEE ALSO

create_buffer_tree (2), **remove_buffer_tree** (2); **high_fanout_net_threshold** (3).

PSYN-138 (error) No legitimate driver is found.

DESCRIPTION

You receive this error message because you used the **create_buffer_tree** or **remove_buffer_tree** command and specified a pin on which either no driver at all was found or no legitimate driver was found.

WHAT NEXT

Check the command and make sure you specified the options that you intended.

This problem can occur when you run **create_buffer_tree** on a net with more fanout than the amount specified by the **high_fanout_net_threshold** variable. Change the **high_fanout_net_threshold** variable to a higher value and run the command again.

SEE ALSO

create_buffer_tree (2), **remove_buffer_tree** (2); **high_fanout_net_threshold** (3).

PSYN-139 (information) This region is assigned with ID %d.

DESCRIPTION

This informational message means that the ID for the regional congestion parameters has been created by the **set_congestion_options** command. You can use this ID to remove the regional congestion parameters by using the **remove_congestion_options** command and specifying the ID. You can also review congestion parameters in the design by using the **report_congestion_options** command and specifying the ID.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

remove_congestion_options (2), **report_congestion_options** (2), **set_congestion_options** (2).

PSYN-140 (information) Extractor-based RC computation is enabled.

DESCRIPTION

This informational message occurs because the tool performs automatic computation for capacitance that is based on extraction parameters. This feature does not support min/max RC computation.

Use the following command to disable extractor-based computation:

set physopt_enable_extractor_rc FALSE

The tool disables extractor based RC computation only if all of the following are true:

- User RC is not used.
- TLU+ RC model is not used.
- Optional extraction parameters are present in the physical library.

The tool requires the following extraction parameters to perform automatic computation:

- Field oxide thickness
- Field oxide permitivity
- Layer thickness for all routable layers
- Layer oxide thickness for all routable layers
- Layer oxide permitivity for all routable layers
- Layer lateral oxide thickness for all routable layers
- Layer lateral oxide permitivity for all routable layers

See *Physical Library User Guide* for the syntax of extraction parameters.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

physopt_enable_extractor_rc(3)
PSYN-144(n)

PSYN-141 (error) Physical library %s does not contain technology data.

DESCRIPTION

This error occurs because you used the **link_physical_library** command and specified a physical library that is missing the required technology data.

WHAT_NEXT

Check that the first physical library in the physical library list contains technology information, then rerun the command.

SEE ALSO

link_physical_library (2).

PSYN-142 (warning) Physical library specifies a single lateral oxide and a multiple lateral oxide. Using data from multiple lateral oxide.

DESCRIPTION

You receive this warning message because the physical library specifies both a single lateral oxide and a multiple lateral oxide. The single lateral oxide syntax is obsolete. Only the multiple lateral oxide is used.

WHAT NEXT

No action is required on your part. However, to avoid this warning message, remove the single lateral oxide from the physical library.

PSYN-143 (information) Extractor-based RC computation is disabled.

DESCRIPTION

This informational message occurs because the tool will not perform automatic computation for capacitance that is based on the given extraction parameters although you have specified them in the physical library.

The tool uses the following extraction parameters:

field oxide thickness

field oxide permitivity

layer thickness for all routable layers

layer oxide thickness for all routable layers

layer oxide permitivity for all routable layers

layer lateral oxide thickness for all routable layers

layer lateral oxide permitivity for all routable layers

See *Physical Library User Guide* for the syntax of extraction parameters. See the **PSYN-140** error message for conditions that determine whether this feature is enabled.

If your physical library does not contain extraction parameters, you will not see this message

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

PSYN-140(n)

PSYN-144 (information) TLU+-based RC computation is enabled.

DESCRIPTION

This informational message occurs because the tool performs automatic computation for capacitance that is based on the TLU+ model.

You can set the **physopt_enable_tlu_plus** variable to *False* to turn off this feature. However, the tool performs this automatic computation only if both of the following conditions are true:

- User RC is not used.
- TLU+ technology file is available.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

physopt_enable_tlu_plus(3)

PSYN-145 (information) TLU+-based RC computation is

disabled.

DESCRIPTION

This informational message occurs because the tool does not perform automatic computation for capacitance that is based on the TLU+ model.

WHAT NEXT

This is an informational message only. No action is required on your part.

See *Physical Library User Guide* for the syntax of extraction parameters. See the **PSYN-144** error message for conditions that determine whether this feature is enabled.

SEE ALSO

PSYN-144(n)

PSYN-146 (error) No TLU+ files were found.

DESCRIPTION

This error indicates that no TLU+ files could be found.

WHAT NEXT

TLU+ files can be set using "set_tlu_plus_files".

SEE ALSO

set_tlu_plus_files(2), report_tlu_plus_files(2)

PSYN-147 (warning) TLU+ files are already attached to the Milkyway library.

DESCRIPTION

This message indicates that TLU+ files are already attached to the Milkyway library.

WHAT NEXT

No action is needed from the user.

SEE ALSO

report_tlu_plus_files(2)

PSYN-148 (error) TLU+ file checking failed.

DESCRIPTION

This error indicates that TLU+ file checking failed.

WHAT NEXT

Verify the data in the TLU+ files before proceeding.

SEE ALSO

set_tlu_plus_files(2), report_tlu_plus_files(2)

PSYN-149 (information) Running signoff_opt with ILMs.

DESCRIPTION

You receive this information message because you're running **signoff_opt** with ILMs.

WHAT NEXT

This is an informational message only.

SEE ALSO

signoff_opt(2)
set_si_options(2)

PSYN-150 (error) No physical design for current logical design.

DESCRIPTION

You receive this error because there is no physical design for the current logical design in create_placement -mpc and physopt -mpc flows.

You may have physical information for the top module, and are doing current design to a sub module. In this case create_placement -mpc and physopt -mpc flows will not generate physical information for the sub module.

WHAT NEXT

Fix your input data to include the necessary physical information for this module.

SEE_ALSO

current_design(2)
create_placment(2)
physopt(2)
set_mpc_options(2)

PSYN-151 (error) Design is not ready to run signoff_opt because it has %s.

DESCRIPTION

You receive this error because you are trying to run **signoff_opt** command on a design that is not ready. A design is considered as not ready if any of the following condtions are true:

- it has shorted routes in the routing database
- it has too many routing design rule violations
- it has too many unrouted signal nets
- it has too many violating timing paths
- it has too many logic design rule violations (max_transition, max_capacitance, max_fanout ...)

WHAT NEXT

Run **report_design -physical** and **report_constraint -all_violators** to see the details of violations.

Use **IC Compiler** to fix the violations first, and then come back to run **signoff_opt**.

SEE_ALSO

signoff_opt(2)
report_design(2)
report_constraint(2)

PSYN-152 (warning) Your design contains unsupported port names.

DESCRIPTION

You receive this warning because you are trying to run **signoff_opt** command on a design which has the following conditions:

- A port is driving a net with different name, AND,
- A port has more than one pin (shape)

WHAT NEXT

Use **change_names** command to rename the offending ports.

SEE_ALSO

signoff_opt(2)
change_names(2)

PSYN-153 (error) No arguments are specified for switch '%s'.

DESCRIPTION

You receive this message because the specified switch of the **set_power_rail_connection** command has empty arguments.

WHAT_NEXT

Specify the arguments for the switch, and invoke the **set_power_rail_connection** command again.

SEE ALSO

set_power_rail_connection (2).

PSYN-154 (error) A mismatch has occurred between the number of '%s' and '%s'.

DESCRIPTION

You receive this message because the specified lists must map one-to-one. Both lists must have the same number of entries.

WHAT_NEXT

Specify the **set_power_rail_connection** command with the **-lib_rail_name** *rail_name_list*, **-pnet_name** *pnet_name_list*, and **-port_type** *(input | output)list* options. The values assigned to these options must be lists and must have one-to-one mapping among the three lists. Then, execute **set_power_rail_connection** again.

SEE ALSO

set_power_rail_connection (2).

PSYN-155 (error) Switch -force must be specified with -hierarchy.

DESCRIPTION

You receive this message because the you have activated the switch specified by the **-force** option of the **set_power_rail_connection** command without also specifying the **-hierarchy** option.

WHAT_NEXT

Specify the **-hierarchy** option, and invoke the **set_power_rail_connection** command again.

SEE ALSO

set_power_rail_connection (2).

PSYN-156 (error) No power rail connection annotations exist in '%s'.

DESCRIPTION

You receive this message because the specified design object does not have any power rail connection annotations.

WHAT_NEXT

See the man page for the **set_power_rail_connection** command to determine what options to use for power rail connection annotations. Specify the command with the appropriate options, and invoke it again.

SEE ALSO

set_power_rail_connection (2).

PSYN-157 (warning) Power rail '%s' does not exist.

DESCRIPTION

You receive this warning because the specified power rail does not exist in the library.

WHAT_NEXT

No action is required on your part. However, you can use the **report_lib** command to determine the valid power rails.

SEE ALSO

report_lib (2).

PSYN-158 (warning) The tool is overriding the previous power

annotations on ’%s’.

DESCRIPTION

You receive this warning because the **set_power_rail_connection** command is overriding the previous annotations on the specified subdesign.

WHAT_NEXT

No action is required on your part. However, you can use the **set_power_rail_connection** command without specifying the **-force** option to preserve the previous annotations.

SEE ALSO

set_power_rail_connection (2).

PSYN-159 (warning) The tool is ignoring the current annotations on design ’%s’.

DESCRIPTION

You receive this warning because the tool is ignoring annotations applied to the specified design by using the **set_power_rail_connection** command. Thus, the previous annotations are preserved.

WHAT_NEXT

No action is required on your part. However, you can specify the **-force** option to set a switch to override the previous annotations with the current ones.

SEE ALSO

set_power_rail_connection (2).

PSYN-160 (error) set_row_type command simultaneously specifies -site and row_name_list.

DESCRIPTION

You receive this message because you have specified the **-site** and *row_name_list*

options of the **set_row_type** command at the same time, and they are mutually exclusive. These options specify switches that used to set row_types.

WHAT_NEXT

Use the **set_row_type** command with either the **-site** option, to set the row type based on all rows in the specified site array, or the *row_name_list* option, to set the row_type on individual rows in the list; but you cannot use both options at once.

SEE ALSO

set_row_type (2).

PSYN-161 (error) Specify either the -site or row_name_list option for the set_row_type command.

DESCRIPTION

You receive this message because you have not specified any switches for the **set_row_type** command. These switches are used to set row_types. You can specify a switch by using the **set_row_type** command with the **-site** or *row_name_list* option. The **-site** option specifies a site array. The *row_name_list* option specifies rows in a list form. These options are mutually exclusive.

WHAT_NEXT

Use the **set_row_type** command with either the **-site** option or the *row_name_list* option; but do not use both options at once.

SEE ALSO

set_row_type (2).

PSYN-162 (warning) The previous row type '%d' of row '%s' is changed to '%d'.

DESCRIPTION

You receive this warning because you have changed the row type of the specified row.

WHAT_NEXT

No action is required on your part. However, if you did not intend to change the row type of the specified row, use the **set_row_type** command with the **-type** option to set the row type to its previous value.

SEE ALSO

set_row_type (2).

PSYN-163 (error) Specify either the -all or net_list option for the '%s' command.

DESCRIPTION

You receive this message because you have not specified any switches for the **set_preroute_check** command or **remove_preroute_check** command. The tool uses these switches to select the net or nets for which the preroute checks should be enabled or disabled. The **-all** option tells the tool to select all nets with preroutes. The **net_list** option specifies the list of net or nets. These options are mutually exclusive and cannot be used together.

WHAT NEXT

Use the **set_preroute_check** command or **remove_preroute_check** command with either the **-all** option or the **net_list** option defined. But do not use both options at once in the same command.

SEE ALSO

remove_preroute_check (2), **set_preroute_check** (2).

PSYN-164 (error) '%s' command simultaneously specifies -all and net_list.

DESCRIPTION

You receive this message because you have specified at the same time the **-all** option and the **net_list** option of either the **set_preroute_check** command or the **remove_preroute_check** command. These options are mutually exclusive and cannot be used together. The tool uses these options to specify switches it uses to enable or disable preroute checks during placement.

WHAT NEXT

Use the **set_preroute_check** command or the **remove_preroute_check** command with either the **-all** option or the **net_list** option. But do not use both options at once in the same command.

SEE ALSO

remove_preroute_check (2), **set_preroute_check** (2).

PSYN-165 (error) Cannot find any pre-routes for the specified net(s).

DESCRIPTION

You receive this message because the **set_preroute_check** command, the **remove_preroute_check** command, or the **report_preroute_check** command cannot find any preroute geometries for the net or nets you specified in your design.

WHAT NEXT

Check the DEF file and the PDEF file; make sure that preroutes exist for the specified net or nets.

SEE ALSO

remove_preroute_check (2), **report_preroute_check** (2), **set_preroute_check** (2).

PSYN-166 (error) %s: Wrong physopt_hfs_remove_effort specified.

DESCRIPTION

You receive this message because a wrong effort is set.

WHAT_NEXT

To set the correct effort, use the **physopt_hfs_remove_effort** variable with the appropriate option. The available options are **-none**, **-med**, and **-high**.

SEE ALSO

physopt_hfs_remove_effort (3).

PSYN-167 (warning) Your design has %d unrouted signal nets.

DESCRIPTION

You receive this warning because you are trying to run **signoff_opt** command on a design that has some unrouted signal nets.

WHAT NEXT

It is recommended that you use **IC Compiler** to route all signal nets before running **signoff_opt**.

SEE_ALSO

signoff_opt(2)
route(2)

PSYN-168 (warning) The row '%s' already has row type '%d'.

DESCRIPTION

You receive this warning because you are trying to specify a row type for a row that already has that type set on it.

WHAT NEXT

No action is required.

SEE ALSO

set_row_type(2)

PSYN-169 (warning) PrimeTime image does not contain detail

parasitics.

DESCRIPTION

This warning message occurs because at least one of the specified **PrimeTimage** image from **save_session** does not contain detail parasitics from **read_parasitics** command. As a result, **signoff_opt** will not be able to perform additional signoff analysis after optimization and incremental place and route.

WHAT NEXT

Provide a **PrimeTime** image with detail parasitics.

SEE ALSO

signoff_opt(2)
set_primetime_options(2)

PSYN-170 (error) You are using an invalid StarRCXT image for '%s'.

DESCRIPTION

This error message occurs because you specified an invalid **StarRCXT** image for **signoff_opt**. **IC Compiler** requires the image was created with exactly the same StarRCXT binary that you run **signoff_opt**.

WHAT NEXT

Recreate the image with the same StarRCXT binary.

SEE ALSO

signoff_opt(2)
set_starrcxt_options(2)

PSYN-171 (error) You are using a StarRCXT command file that consists of unsupported options.

DESCRIPTION

This error message occurs because you are using a **StarRCXT** command file that

consists of unspported options. In order to run **signoff_opt**, **IC Compiler** requires certain options to be reserved and does not support them in the user command file.

Here is the list of reserved options:

- MILKYWAY_DATABASE, always uses the same as **IC Compiler**
- MILKYWAY_EXPAND_HIERARCHICAL_CELLS, used by ILM flow
- TCAD_GRD_FILE, specified through **set_starrcxt_options**
- MAPPING_FILE, specified through **set_starrcxt_options**
- COUPLE_TO_GROUND, derived from **set_si_options**
- STAR_DIRECTORY, internally decided
- TARGET_ANALYSIS, internally decided
- INCREMENTAL, internally decided
- NETLIST_INCREMENTAL, internally decided
- NETLIST_FORMAT, internally decided
- NETLIST_COMPRESS_COMMAND, not supported
- NETLIST_NODE_SECTION, always set to **YES**
- NETLIST_TAIL_COMMENTS, internally decided
- NETLIST_FILE, internally decided
- EXTRA_GEOMETRY_INFO, always set to **NODE**
- BLOCK, internally decided
- NETLIST_UNSCALED_COORDINATES, always set to **NO**
- HIERARCHICAL_SEPARATOR, same as **IC Compiler**
- MULTI_CPU_ON_LICENSE_ONLY, always set to **YES** with distributed processing

WHAT NEXT

Remove the unsupported options from your command file.

SEE ALSO

signoff_opt(2)
set_starrcxt_options(2)

PSYN-172 (error) Duplicate keepout name : '%s'. '%s'.

DESCRIPTION

You receive this error message because you tried to perform one of the following actions:

• You tried to create a wiring keepout and give it the same name as that of an already existing wiring keepout.

• You tried to create a placement keepout and give it the same name as that of an already existing placement keepout.

You can have a wiring keepout and a placement keepout of the same name. But you cannot have two wiring keepouts with the same name nor two placement keepouts with the same name.

WHAT NEXT

Using the **report_wiring_keepout** command and the **report_placement_keepout** command, check the names of existing wiring keepouts and placement keepouts, respectively. Make appropriate correction.

SEE ALSO

create_placement_keepout(2)
create_wiring_keepout(2)
report_placement_keepout(2)
report_wiring_keepout(2)

PSYN-173 (error) The specified StarRCXT platform '%s' is incompatible with IC Compiler platform '%s'.

DESCRIPTION

This error message occurs because you are using a **StarRCXT** binary that is different with the current platform of **IC Compiler**. In order to run **signoff_opt**, you must use the same platform for all tools.

WHAT NEXT

It is recommended that you use the same platform of **StarRCXT** with **IC Compiler**.

SEE ALSO

signoff_opt(2)
set_starrcxt_options(2)

PSYN-174 (error) The specified PrimeTime platform '%s' is incompatible with IC Compiler platform '%s'.

DESCRIPTION

This error message occurs because you are using a **PrimeTime** binary that is different with the current platform of **IC Compiler**. In order to run **signoff_opt**, you must use the same platform for all tools.

WHAT NEXT

It is recommended that you use the same platform of **PrimeTime** with **IC Compiler**.

SEE ALSO

signoff_opt(2)
set_primetime_options(2)

PSYN-175 (warning) Physical information will not be written to '.ddc' format from the tool.

DESCRIPTION

This warning occurs because the Synopsys logical database (.ddc) format cannot store the physical information. Writing the design in .ddc format from a session of the tool can result in a loss of physical information associated with the design. This is a current limitation of the ddc format. Use .ddc format only if your design contains no physical information.

WHAT NEXT

If the design contains physical information, the recommended storage format is Milkyway. You can use the **write_milkyway** command to write the design into the Milkyway database.

SEE ALSO

write(2)

PSYN-176 (error) The tool cannot write ’COMPACT’ parasitic from a non-Milkyway design.

DESCRIPTION

This error occurs because the COMPACT format can be written only with the design that is read from Milkway by using the **read_milkyway** command. If you use other read commands to read the design, such as the **read_db** or **read_verilog** command, the tool cannot write COMPACT parasitics.

WHAT NEXT

Use the **read_milkyway** command to read the design from the Milkyway database, or use another parasitic format such as Standard Parasitic Exchange Format (SPEF) or Synopsys Binary Parasitic Format (SBPF).

PSYN-177 (error) The tool cannot read ’COMPACT’ parasitic from non-Milkyway design.

DESCRIPTION

This error occurs because the **COMPACT** format can be read only with a design that is read from Milkway by using the **read_milkyway**command. If you read the design using other read commands, such as the **read_db** or **read_verilog** command, the tool cannot read in COMPACT parasitics.

WHAT NEXT

Use the **read_milkyway** command to read a design from Milkyway database. Or, use other parasitic format such as Standard Parasitic Exchange Format (SPEF) or Synopsys Binary Parasitic Format (SBPF).

PSYN-178 (Information) setting %s as ignored_layer due to min_max lay er setting.

DESCRIPTION

You receive this error message because you have set the **Min/Max** using this command. In order to be consistent, ICC will set all the metal layers below/above this layer as "ignored layer" automatically.

WHAT NEXT

Using report_ignored_layers command to see current min/max/ignored layer status.

SEE ALSO

report_ignored_layers (2) remove_ignored_layers (2)

PSYN-179 (Information) setting %s as %s routing layer.

DESCRIPTION

You receive this error message because you have set the **Min/Max** using this command. Setting Min/Max routing layers will affect the following routing.

WHAT NEXT

Using report_ignored_layers command to see current Min/Max layer status.

SEE ALSO

report_ignored_layers (2) remove_ignored_layers (2)

PSYN-180 (error) Invalid value %s for switch %s. Valid values are %s.

DESCRIPTION

You receive this error because the value you specify for the given switch is not valid. Check **signoff_opt** man page for more information.

WHAT NEXT

Correct your input by using one of the valid values.

SEE_ALSO

signoff_opt(2)

PSYN-181 (error) Command can only be run with a Milkyway

design.

DESCRIPTION

You receive this error because you are trying to run **signoff_opt** command on a non-Milkyway design. In order to run **signoff_opt**, the design must be read from Milkyway, such as **open_mw_cel**.

WHAT NEXT

Use **open_mw_cel** to open your design.

SEE_ALSO

signoff_opt(2)

PSYN-182 (warning) You are using a newer version of PrimeTime that might not be compatible.

DESCRIPTION

This warning message occurs because you are using a newer version of **PrimeTime** that might not be compatible with the current version of **IC Compiler**.

WHAT NEXT

This is only a warning message. However, it is recommended that you use a compatible version of **PrimeTime** with **IC Compiler** to avoid potential problems.

SEE ALSO

signoff_opt(2)

PSYN-183 (warning) You are using an older version of StarRCXT that might not be compatible.

DESCRIPTION

This warning message occurs because you are using an older version of **StarRCXT** that might not be compatible with the current version of **IC Compiler**.

WHAT NEXT

This is only a warning message. However, it is recommended that you use a compatible version of **StarRCXT** with **IC Compiler** to avoid potential problems.

SEE ALSO

signoff_opt(2)

PSYN-184 (information) SI analysis and fixing is enabled for signoff_opt.

DESCRIPTION

You receive this information message because the analysis and fixing for signal integrity problems are enabled.

WHAT NEXT

This is an informational message only. However, if you do not intend to enable SI analysis and fixing, you can use **set_si_options** command to modify your SI options, and then re-run **signoff_opt**.

SEE ALSO

signoff_opt(2)
set_si_options(2)

PSYN-185 (error) Cannot find an appropriate shell.

DESCRIPTION

You receive this error because **IC Compiler** is not able to find an appropriate shell to run **signoff_opt**.

WHAT NEXT

Correct this problem by contacting your UNIX system administrator.

SEE_ALSO

signoff_opt(2)

PSYN-186 (error) Path to PrimeTime is not specified.

DESCRIPTION

You receive this error because you didn't specify the path to **PrimeTime** before running **signoff_opt**. The path is required for **IC Compiler** to locate the **PrimeTime** executable to run **signoff_opt**.

WHAT NEXT

You can use **-exec_dir** switch with **set_primetime_options** to specify the path to **PrimeTime**.

SEE_ALSO

set_primetime_options(2)
report_primetime_options(2)
signoff_opt(2)

PSYN-187 (information) Use PrimeTime path %s.

DESCRIPTION

IC Compiler uses this information message to tell you what is that path that we used to search for **PrimeTime** executable during **signoff_opt**.

WHAT NEXT

This is an informational message only. You can change the path by using **-exec_dir** switch of **set_primetime_options**.

SEE ALSO

set_primetime_options(2)
report_primetime_options(2)
signoff_opt(2)

PSYN-188 (information) Use StarRCXT path %s.

DESCRIPTION

IC Compiler uses this information message to tell you what is that path that we used to search for **StarRCXT** executable during **signoff_opt**.

WHAT NEXT

This is an informational message only. You can change the path by using **-exec_dir** switch of **set_starrcxt_options**.

SEE ALSO

set_starrcxt_options(2)
report_starrcxt_options(2)
signoff_opt(2)

PSYN-189 (error) Path to StarRCXT is not specified.

DESCRIPTION

You receive this error because you didn't specify the path to **StarRCXT** before running **signoff_opt**. The path is required for **IC Compiler** to locate the **StarRCXT** executable to run **signoff_opt**.

WHAT NEXT

You can use **-exec_dir** switch with **set_starrcxt_options** to specify the path to **StarRCXT**. Please also specify **-max_nxtgrd_file** and **-map_file** as they are also required to run StarRCXT. **-min_nxtgrd_file** is optional.

SEE_ALSO

set_starrcxt_options(2)
report_starrcxt_options(2)
signoff_opt(2)

PSYN-190 (warning) Your design has %d shorted routes in the routing database.

DESCRIPTION

You receive this warning because you are trying to run **signoff_opt** command on a design that has several shorts in the routing database.

WHAT NEXT

Run **report_design -physical** to see the details of routing violations.

It is recommended that you use **IC Compiler** to fix the routing violations first, and

then come back to run **signoff_opt**.

SEE_ALSO

signoff_opt(2)
report_design(2)

PSYN-191 (warning) Your design has %d routing violations.

DESCRIPTION

You receive this warning because you are trying to run **signoff_opt** command on a design that has some routing violations.

WHAT NEXT

Run **report_design -physical** to see the details of routing violations.

It is recommended that you use **IC Compiler** to fix the routing violations first, and then come back to run **signoff_opt**.

SEE_ALSO

signoff_opt(2)
report_design(2)

PSYN-192 (error) Command cannot be run with a readonly Milkyway design.

DESCRIPTION

You receive this error because you are trying to run **signoff_opt** command on a readonly Milkyway design. In order to run **signoff_opt**, the Milkyway design must be writeable.

WHAT NEXT

Do not use any **-readonly** switch when opening your Milkyway design.

SEE_ALSO

signoff_opt(2)

PSYN-193 (error) You are using an incompatible version of StarRCXT.

DESCRIPTION

This error message occurs because you are using an incompatible version of **StarRCXT** comparing with the current version of **IC Compiler**. Your **StarRCXT** is either too new or too old. **IC Compiler** is not forward-compatible with newer **StarRCXT**, and a too old **StarRCXT** does not have all the features that are required to run **signoff_opt**.

WHAT NEXT

It is recommended that you use a compatible version of **StarRCXT** with **IC Compiler** to avoid potential problems.

SEE ALSO

signoff_opt(2)

PSYN-194 (error) You are using an incompatible version of PrimeTime.

DESCRIPTION

This error message occurs because you are using an older version of **PrimeTime** comparing with the current version of **IC Compiler**. **PrimeTime** is not forward-compatible with **IC Compiler**.

WHAT NEXT

It is recommended that you use a compatible version of **PrimeTime** with **IC Compiler** to avoid potential problems.

SEE ALSO

signoff_opt(2)

PSYN-195 (error) Command can only be run with a routed

design.

DESCRIPTION

You receive this error because you are trying to run **signoff_opt** command on an unrouted design. In order to run **signoff_opt**, the design must be fully routed. It is also highly recommended to run optimization before running **signoff_opt**.

WHAT NEXT

Use **route** command to route your design.

SEE_ALSO

signoff_opt(2)

PSYN-196 (warning) Switch '%s' is not scenario specific. The last value will be used for all scenarios.

DESCRIPTION

You receive this warning because you are using a switch that is not scenario specific in a multi scenario setting. For example, the path to PrimeTime exec is not scenario specific. That is, you cannot use different PrimtTime executables for different scenarios. The last value will be used for all scenarios, overwriting previous setting specified by this switch.

WHAT NEXT

Modify your script to only use scenario specific switches in a multi scenario setting. Set the switch that is not scenario specific before creating the first scenario.

SEE_ALSO

set_primetime_options(2)
set_starrcxt_options(2)

PSYN-197 (warning) Switch '%s' has no effect in multi scenario.

DESCRIPTION

You receive this warning because you are using a switch that is not supported in

multi scenario. The switch will be ignored.

You will also receive this warning if you have applied this switch in non multi scenario mode, then start your signoff_opt run in multi scenario mode.

WHAT NEXT

Modify your script to remove the switch.

SEE_ALSO

set_primetime_options(2)
set_starrcxt_options(2)
signoff_opt(2)

PSYN-198 (information) Running signoff_opt with multi scenarios.

DESCRIPTION

You receive this information message because you're running signoff_opt with multi scenario capability.

WHAT NEXT

This is an informational message only.

SEE ALSO

signoff_opt(2)
create_scenario(2)

PSYN-199 (warning) '%s' is not supported in multi scenario.

DESCRIPTION

You receive this warning because you are using a feature that is not supported in multi scenario signoff optimization. This request to use this feature will be ignored.

For example, traditional min/max timing analysis is not supported in multi scenario signoff optimization. Each scenario will be analyzed with either single or on_chip_variation mode (where on_chip_variation is the recommended analysis type). Therefore, if you specify min tech file for StarRCXT, or use set_min_library to sepcify a min library, these settings will be ignored during multi scenario signoff

optimization. Note this does not affect the non-signoff multi scenario optimization, nor single or bcwc (best case - worst case) signoff optimization.

WHAT NEXT

Modify your script so that it does not use the feature.

SEE_ALSO

signoff_opt(2)
set_primetime_options(2)
set_starrcxt_options(2)

PSYN-200 (warning) '%s' pin on '%s' cell in the '%s' technology library is missing in the '%s' physical library.

DESCRIPTION

You receive this message because a cell pin in the technology library is missing from the same-name cell pin in the physical library. Consequently, the logical cell cannot be linked with the same-name cell in the physical library.

WHAT NEXT

Examine this cell pin in both libraries. Add the missing cell pin to your physical library.

PSYN-201 (error) Cannot determine net names.

DESCRIPTION

This error occurs because you used the **set_net_width_options** command but did not specify a list of net names. A list of net names must be specified as target nets.

WHAT NEXT

Rerun the command and specify a list of net names.

SEE ALSO

set_net_width_options (2).

PSYN-202 (warning) Cell %s has illegal orientation on the row.

DESCRIPTION

This warning message tells you that the specified cell is illegally placed on the row. The cell orientation does not match the row site orientation definition in the floorplan.

WHAT_NEXT

Rerun the **legalize_placement** command to make the cell placement legal.

SEE ALSO

legalize_placement (2).

PSYN-203 (warning) Cell %s located on the wrong row site.

DESCRIPTION

This warning message tells you that the specified cell is located on the wrong row site. The cell must be located on the site that is defined in the physical library. For example, if the cell is defined as the "CORE" site cell in the LEF, then the placement tool must place the cell on the "CORE" site array. If the placement tool places the cell on the "CORE1" site array, it is an illegal cell.

Another case is the cell be placed outside the row bbox, for example, the cell is placed outside the right end of the row site, or left end of the row side. Please check the cell bbox against its row site bbox.

WHAT_NEXT

Maker sure the site is defined in the physical library, or, check the GUI or PDEF to see the cell is placed inside the site row. Use **legalize_placement** to make the cell placement legal.

SEE ALSO

check_legality (2), **legalize_placement** (2).

PSYN-204 (error) Cannot find PDEF layer ID for given layer

name ’%s’.

DESCRIPTION

This error message tells you that the PDEF layer ID for the given layer name was not found. This might be because you specified the wrong layer name, the layer name is not defined, or the PDEF file was not read.

WHAT_NEXT

Check for one of the factors above. Make the appropriate change, then rerun the command.

PSYN-205 (warning) Value ’%g’ specified to switch ’%s’ is out of range.

DESCRIPTION

This warning message tells you that the specified value is out of the normal range. Though the command still runs, the results might not be accurate.

WHAT_NEXT

Rerun the command and specify a valid value to the switch.

PSYN-206 (error) Invalid value ’%d’ specified to switch ’%s’.

DESCRIPTION

This error message tells you that the value specified to the switch is invalid.

WHAT_NEXT

Rerun the **set_net_width_options** command and specify a valid value to the switch.

SEE ALSO

set_net_width_options (2).

PSYN-207 (error) Number of layer names, width multipliers and

space multipliers do not match.

DESCRIPTION

This error occurs because the number of layer names, width multipliers and space multipliers do not match.

WHAT_NEXT

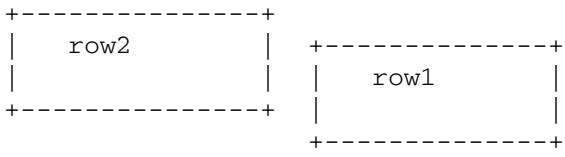
Rerun the command and specify an equal number of layer names, width multipliers and space multipliers.

PSYN-208 (error) Row %s (y=%d) and row %s (y=%d) are not aligned in Y coordinates. Check DEF data.

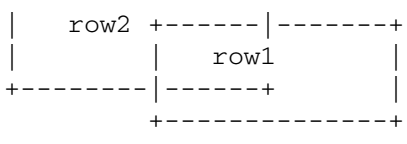
DESCRIPTION

This error message tells you that the specified rows are not aligned in the Y coordinates. The detailed placement requires that rows with the same site type, such as row1 and row2 in site CORE, are aligned in Y (X may not fully overlap). See the following examples. Note that both rows are of the same site type.

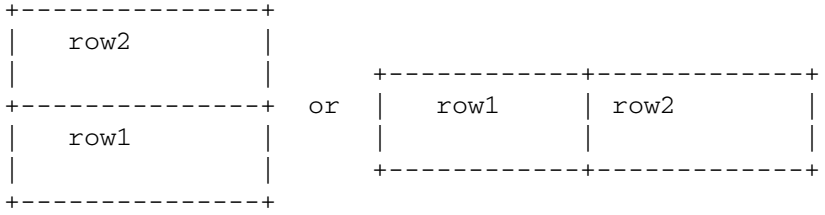
The following example shows an unsupported floorplan:



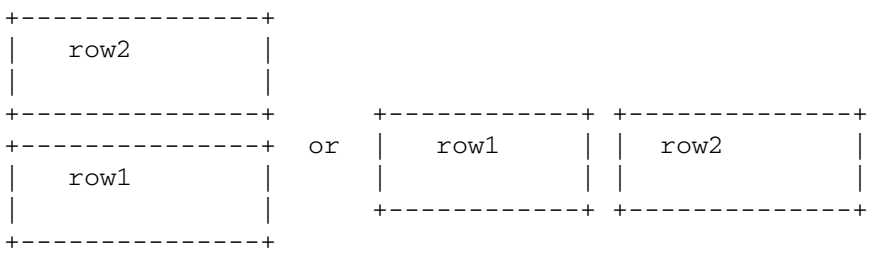
or



The following example shows a supported floorplan:



or



WHAT_NEXT

Modify rows use command cut_row and add_row, or check the DEF data and change the rows so that they align in the Y coordinates.

SEE ALSO

read_def(2)
cut_row(2)
add_row(2)

PSYN-209 (warning) physopt_row_overlap_threshold setting as %.3f is too big.

DESCRIPTION

This warning message tells you that the value specified with **physopt_row_overlap_threshold** exceeds the recommended threshold for detailed placement. This can negatively effect the quality of the results.

WHAT_NEXT

Check the floorplan and make sure that the site arrays are overlapping within the recommended threshold.

SEE ALSO

physopt_row_overlap_threshold (3).

PSYN-210 (error) Site array type %s overlapping is beyond

overlapping threshold of site array type %s (normal core site).

DESCRIPTION

This error message occurs because site arrays are not overlapping within the threshold that has been set using physopt_row_overlap_threshold. If multiple types of site_arrays are defined in the floorplan the detail placer requires that the site_arrays overlap with in a threshold.Abnormal core site arrays should overlap with normal core site arrays within the threshold setting range. Row differences should not be larger than the threshold. The threshold is set using the **physopt_row_overlap_threshold** variable. For example, if the threshold is set to 0.1, 10 percent difference of normal core area is allowed.

WHAT_NEXT

Check the floorplan and make sure that multitype site arrays are overlapping within a small threshold.

You can turn off overlap checking by setting **physopt_check_site_array_overlap** to FALSE, or by increasing the threshold setting using the **physopt_row_overlap_threshold** variable. Note that this will negatively effect the quality of results.

SEE ALSO

physopt_check_site_array_overlap (3), **physopt_row_overlap_threshold** (3).

PSYN-211 (error) Site type %s height %d is not an integer multiple of site type %s height %d.

DESCRIPTION

This error occurs because the abnormal site height is not an integer multiple of the normal site height. Detail placement requires that the abnormal site height is an integer multiple of the normal site height.

WHAT_NEXT

Check the physical library make sure that the multiheight site is an integer multiple of the normal site height.

PSYN-212 (warning) '%s' pin on '%s' macro in the '%s' physical

library is missing in the '%s' technology library.

DESCRIPTION

You receive this message because a macro pin in the physical library is missing from the same-name cell pin in the technology library.

WHAT NEXT

Examine this cell pin in both libraries. Add the missing cell pin to your technology library. Ignore this message if this is a physical-only pin.

PSYN-213 (information) Your design has no logic design rule violation left.

DESCRIPTION

You receive this message because there is no logic design rule violation left in your design. **signoff_opt** might stop.

WHAT NEXT

It is just an information message.

SEE_ALSO

signoff_opt(2)

PSYN-214 (information) Your design has at least %d %s logic design rule violations.

DESCRIPTION

You receive this message because you are trying to run **signoff_opt** command on a design that has some logic design rule violations, such as max_transition, max_capacitance and max_fanout violations.

WHAT NEXT

Run **report_constraint -all_violators** to see the details of violations.

It is recommended that you use **IC Compiler** to fix the violations first, and then

come back to run **signoff_opt**.

SEE_ALSO

signoff_opt(2)
report_constraint(2)

PSYN-215 (error) There are some cells with an illegal placement.

DESCRIPTION

This error message tells you that the detail placement is illegal for one or more of the following reasons:

- Cell is not placed on a row
- Cells overlap each other
- Cell overlaps a blockage
- Cell has illegal orientation on the row
- Cell is placed on a wrong site type
- Cell pin overlaps power strap or violates physical spacing rule
- Cell is placed outside core area.

WHAT_NEXT

Use the **check_legality -verbose** command to see more detailed messages about the placement issues. Run legalize_placement if it has not already been run.

SEE ALSO

check_legality (2), **legalize_placement** (2).

PSYN-216 (information) Your design has no timing violation left.

DESCRIPTION

You receive this message because there is no timing violation left in your design. **signoff_opt** might stop.

WHAT NEXT

It is just an information message.

SEE_ALSO

signoff_opt(2)

PSYN-217 (error) Cannot run incremental signoff analysis without running full analysis first.

DESCRIPTION

You receive this error because you are trying to run **run_signoff** command with incremental signoff analysis, before running it first with full signoff analysis. A full signoff analysis is required before any incremental signoff analysis.

In addition, when you change PrimeTime or StarRCXT options using **set_primetime_options** or **set_starrcxt_options** after a full signoff analysis, the full signoff analysis becomes invalid, and you cannot run incremental signoff analysis without without another full signoff analysis.

WHAT NEXT

Use **run_signoff** command to perform a full signoff analysis first.

SEE_ALSO

run_signoff(2)
set_primetime_options(2)
set_starrcxt_options(2)

PSYN-218 (warning) QoR report might not include all violating paths.

DESCRIPTION

You receive this warning because you are trying to run **signoff_opt** or **run_signoff** command on a design that has excessive number of violating paths as reported by **PrimeTime**. **report_qor** command after **signoff_opt** or **run_signoff** only reports TNS and number of violating paths based on a limited number of violations. Thus, the TNS and number of violating paths in the QoR report might not include all violating paths in your design.

WHAT NEXT

Run **report_constraint -all_violators** to see the details of violations.

SEE_ALSO

signoff_opt(2)
run_signoff(2)
report_constraint(2)

PSYN-219 (information) Static noise analysis and fixing is enabled for signoff_opt.

DESCRIPTION

You receive this information message because the static noise analysis and fixing is enabled in **signoff_opt**.

WHAT NEXT

This is an informational message only. However, if you do not intend to enable static noise analysis and fixing, you can use **set_si_options** command to modify your SI options, and then re-run **signoff_opt**.

SEE ALSO

signoff_opt(2)
set_si_options(2)

PSYN-220 (information) lib cell: %-16s: %.2f%% (%d/%d) legality check pass rate.

DESCRIPTION

You receive this information message showing the rate at which the physical library cells can be legalized, when you run the **check_physical_constraints** command.

A high rate of legalization means that it is easy for the cell to find a legal site. All physical library cells should have a high legalization rate.

A low rate of legalization means that it is difficult for the cell to find a legal site, causing a large amount of displacement, and the timing might be negatively effected. This might also cause legalization failure. For example, if only 50 percent of the sites of a cell can be legalized, then only 50 percent placement area

can fit the cell. However, in the design, this library cell might need more than 50 percent placement area. In this case, legalization fails because there is not enough space to place the cell legally.

Another example is when 50 percent of the sites of a library cell are legal sites, and 30 percent of the sites of another library cell are legal sites. The combinational legal rate for the two library cells might be lower than the individual rate because they might share the same legal sites. To prevent legalization failure, make sure the legal rate is high for all of the physical library cells the design is using.

The following command can be used to analyze the legalization rate for the library cells against the floorplan.

psyn_shell> **check_physical_constraints -analyze_legality -lib_cell <> -verbose**

WHAT NEXT

Check the library cell and floorplan to ensure the legal rate is high for every library cell. You might have to modify the floorplan (such as power straps) to make the cell easy to be legalized, or set **dont_use** on some library cells to prevent the design from linking to these cells.

SEE ALSO

check_physical_constraints (2).

PSYN-221 (error) %d cells could not be placed during ECO placement.

DESCRIPTION

This error occurs because the tool expects that new ECO cells must be connected to the existing placed netlist. The exception occurs when individual unplaced, unconnected cells are introduced in the ECO flow (such as spare cells). These are placed evenly within the core area.

It is possible that the ECO changes in this design have a set of connected, unplaced cells which, as a collection, have no connection to the existing placed design. This type of netlist change is not currently supported through the ECO flow.

WHAT_NEXT

Continue by restructuring the ECO changes to satisfy the above requirements. Alternatively, perform coarse placement on the entire design using either the **create_placement** or **physopt** command.

PSYN-222 (error) The x-scale and y-scale for the physical timing model must
be nonnegative.

DESCRIPTION

This error message tells you that you used the **compile_physical** command and specified negative physical timing model scale values. The **compile_physical** command expects nonnegative values. Negative values result in negative delays.

WHAT_NEXT

Check the values of the scales and make sure that they are nonnegative.

SEE ALSO

compile_physical (2).

PSYN-223 (error) Failed to derive physical timing model scales.

DESCRIPTION

The design might not have sufficient physical information. As a result, the command was not successful in deriving the physical timing models for the design.

WHAT_NEXT

Make sure the design has sufficient physical information.

PSYN-224 (warning) %d cells have no location.

DESCRIPTION

This warning message tells you that some of the cells specified with the **check_legality** command do not have placement information. As a result, no legality information was gathered for those cells.

WHAT_NEXT

Perform coarse placement, or make ECO changes to place all the cells. Then, rerun the **check_legality** command.

SEE_ALSO

check_legality (2), **create_placement** (2), **legalize_placement** (2), **physopt** (2).

PSYN-225 (error) Cannot assign location for cell %s added for wired logic.

DESCRIPTION

This error occurs because you used the **compile_physical -incremental** or **physopt -incremental** command before the design was placed. Once the wired logic is replaced by mapped gates, the newly-added gates must have locations assigned to them. This message tells you that the location assignment was not successful.

WHAT NEXT

Make sure the design is placed before using **compile_physical -incremental** or **physopt -incremental**.

SEE ALSO

compile_physical (2), **physopt** (2).

PSYN-226 (information) Assigned location for cell %s added for wired logic.

DESCRIPTION

This message tells you that the location assignment for the specified cell was successful. For incremental physical compile, once the wired logic is replaced by mapped gates, the newly-added gates must be assigned locations.

WHAT NEXT

Make sure the wired logic in the design is functioning as expected.

SEE ALSO

compile_physical (2), **physopt** (2).

PSYN-227 (error) Site array (%s) has irregular rows specified for location (%d %d), spacing (%d) > width (%d).

DESCRIPTION

You receive this error message because the tool has found a discrepancy between the PDEF file definition of spacing in the named row and the spacing defined for the same row in the physical library. The spacing defined in the PDEF file is larger than the spacing defined for the row in the physical library. The tool requires that you define the site array as "regular," so that the width and the spacing between the sites are equal.

The **physopt** command and the **legalize_placement** command require that you specify the site array as regular in the PDEF input.

WHAT NEXT

Correct the site array definition in the PDEF file so that it is regular, and read in the PDEF file using the **read_pdef** command.

SEE ALSO

legalize_placement(2)
physopt(2)
read_pdef(2)

PSYN-228 (error) The via ID cannot be -1. Examine the PDEF file to ensure that the via is defined.

DESCRIPTION

This error occurs because an error occurred when the tool was using the **read_pdef** command to read the Physical Design Exchange Format (PDEF) file. That error was caused by an invalid via ID of -1. A valid via ID is one which has a correct reference to the VIA_DEF section inthe PDEF.

WHAT NEXT

Specify a valid via ID from the VIA_DEF section of the PDEF and execute the **read_pdef** command.

SEE ALSO

read_pdef(2)

PSYN-229 (warning) Inconsistent library data found. Layer %s is ignored for resistance and capacitance computation.

DESCRIPTION

You receive this warning because the library data for the specified layer is inconsistent. For example, you receive this message if the pitch is less than the width plus the spacing. As a result, the layer is excluded from resistance and capacitance computation. However, this does not impact congestion computation.

WHAT NEXT

No action is required on your part. However, you can examine the library data for possible problems, fix the library resistance and capacitance inconsistency problem, and regenerate the physical library.

SEE ALSO

GR-15 (n), **GR-16** (n).

PSYN-230 (error) Unable to complete detailed placement.

DESCRIPTION

You receive this error message because a problem with the initial placement of cells or the relocation of cells is preventing the completion of the detailed placement.

WHAT NEXT

Place all of the cells in the design, and then rerun the **optimize_placement** command.

SEE ALSO

create_placement (2), **legalize_placement** (2), **optimize_placement** (2), **physopt** (2).

PSYN-231 (error) Cannot receive paths array.

DESCRIPTION

You receive this error message because the compiler is unable to generate an array of worst paths of the design using the **optimize_placement** command.

WHAT NEXT

Run the **report_timing** command before running **optimize_placement**.

SEE ALSO

optimize_placement (2), **report_timing** (2).

PSYN-232 (error) Unable to perform placement optimization.

DESCRIPTION

You receive this error message because errors when executing the **optimize_placement** command. Possible causes are as follows:

• An incorrect netlist is specified.

• Inconsistent units are used.

• The structure of the critical paths is invalid.

• Unable to estimate the changes in timing parameters after replacement.

• The initial placement was illegal; for example, some cells were placed outside the core area.

WHAT NEXT

Perform placement and use the **run_router** command before using the **optimize_placement** command. If the **-no_legalize** switch is not set, run **legalize_placement** before running **optimize_placement**.

SEE ALSO

create_placement (2), **legalize_placement** (2), **optimize_placement** (2), **physopt** (2), **run_router** (2).

PSYN-233 (error) Cannot remove old location of cell %s from the map.

DESCRIPTION

You receive this error message because the placement map created during initialization of the detailed placer is invalid. Possible causes are the following:

• Incorrect initial placement. Some cells are outside of the core area.

• If the **-no_legalize** switch for the **optimize_placement** command is not set, the initial placement has legality violations.

WHAT NEXT

Perform coarse placement or make ECO changes to place all of the cells before using the **optimize_placement** command. If the **-no_legalize** switch for **optimize_placement** is not set, run **legalize_placement** before running **optimize_placement**.

SEE ALSO

create_placement (2), **legalize_placement** (2), **optimize_placement** (2), **physopt** (2).

PSYN-234 (error) Cannot place the cell %s in the new location (%d, %d).

DESCRIPTION

You receive this error message because the named cell cannot be placed in the specified location during placement optimization.

WHAT NEXT

Perform coarse placement or make ECO changes to place all of the cells before running the **optimize_placement** command.

SEE ALSO

create_placement (2), **legalize_placement** (2), **optimize_placement** (2), **physopt** (2).

PSYN-235 (error) Unable to perform placement optimization for path group %s.

DESCRIPTION

You receive this error message because an error occurred during placement optimization. The possible causes are as follows:

• An incorrect netlist is specified.

- Inconsistent units are used.
- The structure of the critical paths is invalid.

WHAT NEXT

Perform placement to place all of the cells, and then use the **run_router** command before executing the **optimize_placement** command.

SEE ALSO

create_placement (2), **legalize_placement** (2), **optimize_placement** (2), **physopt** (2), **run_router** (2).

PSYN-236 (error) Invalid or absent layer information.

DESCRIPTION

You receive this error message because the compiler is unable to receive the library parameters (capacitance and resistance per unit length in both directions) of the layer.

WHAT NEXT

Make sure that the capacitance and resistance parameters exist in the library, and then rerun the **optimize_placement** command.

SEE ALSO

optimize_placement (2).

PSYN-237 (error) Illegal data found for net %s.

DESCRIPTION

You receive this message because the specified net has an irregular structure; the tool detects no pins or bounds.

WHAT_NEXT

Examine the initial net list. Perform coarse placement or make engineering change order (ECO) changes to place all the cells before using the **optimize_placement** command.

SEE ALSO

optimize_placement (2).

PSYN-238 (error) Illegal timing data for cell %s.

DESCRIPTION

You receive this error message because the specified cell has no available arcs corresponding to input and output pins found in some critical paths.

WHAT NEXT

Check the libraries for corresponding library cells that exist in loaded libraries. If a corresponding library cell exists in a loaded library, remove it from the library and rerun the **optimize_placement** command.

SEE ALSO

optimize_placement (2).

PSYN-239 (warning) Unable to find the location of cell %s near (%d,%d).

DESCRIPTION

You receive this warning because detailed placement cannot find the legal location for the given cell near the specified point.

WHAT NEXT

No action is required on your part unless you want to examine the specified location and cell to ensure that they are as you intended.

PSYN-240 (error) %s: No current design.

DESCRIPTION

You receive this error message because you did not set a current design before using the **optimize_placement** command.

WHAT NEXT

Set the current design and then run the **optimize_placement** command.

SEE ALSO

optimize_placement (2).

PSYN-241 (information) %s: Number of optimized paths set is more than the number of generated paths. The number of optimized paths must equal the number of generated paths.

DESCRIPTION

This message informs you that you set the number of paths to be optimized to more than the the number of paths to be generated. As a result, the number of paths to be optimized is automatically reset to equal the number of paths to be generated.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

optimize_placement (2).

PSYN-242 (error) Unable to initialize detailed placement.

DESCRIPTION

You receive this error message because the compiler is unable to initialize detailed placement for incremental relocations.

WHAT NEXT

Perform placement to place all of the cells and then rerun the **optimize_placement** command.

SEE ALSO

create_placement (2), **legalize_placement** (2), **optimize_placement** (2), **physopt** (2).

PSYN-243 (error) Conflicting parameter %s for the core. Cannot set more than two of -utilization, -core_width, -core_height, -aspect_ratio options.

DESCRIPTION

You receive this message because there is a conflict in the parameters passed for the core area. These parameters are set by using the **set_floorplan_options** command. See the man page for **set_floorplan_options** or the user guide to determine the allowable combinations for the following options:

-utilization
-core_width
-core_height
-aspect_ratio

WHAT_NEXT

Try to use only two of the options listed above. You can use the **report_floorplan_options** command to view the parameters that have been set for core area.

SEE_ALSO

report_floorplan_options (2), **set_floorplan_options** (2).

PSYN-244 (warning) Corner keepout %2f is too big to fit the core area. Resetting it to 0.

DESCRIPTION

You receive this warning because the corner keepout you specified for port placement is too big. A keepout this size would completely block every side of the core area, so that ports could not be placed. The tool resets the corner keepout to 0 (zero) and continues as if there is no corner keepout constraint.

WHAT NEXT

No action is required on your part unless you want to examine the value of the corner keepout compared with the generated core area. You can see the core area by using the **write_pdef** command to write the Physical Design Exchange Format (PDEF) file from the flow or by using the **report_design** command with the **-physical** option on the resulting .db design. You can specify the target placement utilization for the core area by using the **set_floorplan_options** command with the **-corner_keepout** option. Note that the **-corner_keepout** option is specified in microns.

SEE_ALSO

report_design (2), **set_floorplan_options** (2), **write_pdef** (2).

PSYN-245 (warning) Cell '%s' is too big to fit the core area. Fixing it to the lower-left corner.

DESCRIPTION

You receive this warning because the width or height of the cell is bigger than the core area's width or height; This is not allowed for placement. The tool fixes this cell to the lower-left corner of the core area so that the flow can continue.

WHAT NEXT

No action is required on your part unless you want to examine the placement result and adjust the core area constraints, utilization, aspect_ratio, and so on, to ensure that the core area is feasible for the design. Then you can rerun the flow. You can also define the legal orientation for this cell to place it in the desired orientation and match its shape with the core area.

SEE_ALSO

set_floorplan_macro_options (2), **set_floorplan_options** (2).

PSYN-246 (error) No layer name(s) specified.

DESCRIPTION

You receive this error message because the **create_track**, **remove_track**, or **shift_track** command cannot execute without a specified layer name.

WHAT NEXT

Specify the layer name and run the command again. Refer to the command man page for information about the optional and required parameters.

SEE ALSO

create_track (2), **remove_track** (2), **shift_track** (2).

PSYN-247 (warning) Direction is not specified. Using the library-specified direction.

DESCRIPTION

You receive this warning because the direction is not specified in the command invoked, so the tool uses the library-specified direction.

WHAT NEXT

No action is required on your part unless you want to specify a direction. You can examine the library to see the direction being used and the man page for the command that caused the warning for detailed information on specifying a direction value.

SEE_ALSO

create_track (2), **remove_track** (2), **report_track** (2), **shift_track** (2).

PSYN-248 (error) No offset is specified for shifting tracks.

DESCRIPTION

You receive this message because no offset is specified for shifting tracks.

WHAT_NEXT

See the man page for the command that caused the error for detailed information on optional and required parameters, then specify the offset.

SEE_ALSO

create_track (2), **remove_track** (2), **report_track** (2), **shift_track** (2).

PSYN-249 (warning) Count value is not specified. Covering placement area, depending on pitch.

DESCRIPTION

You receive this warning because the number of tracks to be created is not specified. When the count value is not specified, the tool attempts to cover the entire placement area with tracks. The distance between the tracks is equal to the

pitch.

WHAT_NEXT

No action is required on your part. You can see the man page for the command that caused the warning for detailed information on specifying optional and required parameters.

SEE_ALSO

create_track (2), **remove_track** (2), **report_track** (2), **shift_track** (2).

PSYN-250 (warning) Coordinate value is not specified. Defaulting to half pitch.

DESCRIPTION

You receive this warning because the value of the start of the first track is not specified. First the tool attempts to get it from the library; but if this is not successful, it uses half of the pitch value.

WHAT NEXT

No action is required on your part. You can see the man page for the command that caused the warning for detailed information on specifying optional and required parameters.

SEE_ALSO

create_track (2), **remove_track** (2), **report_track** (2), **shift_track** (2).

PSYN-251 (warning) Space is not specified. Considering using pitch.

DESCRIPTION

You receive this warning because the space between the tracks is not provided. The tool uses the default value, which is the pitch value provided by the library.

WHAT NEXT

No action is required on your part. You can see the man page for the command that

caused the warning for detailed information on specifying optional and required parameters.

SEE_ALSO

create_track (2), **remove_track** (2), **report_track** (2), **shift_track** (2).

PSYN-252 (warning) Ignoring bound for port '%s'. Compare bound (%d %d %d %d) against core area (%d %d %d %d).

DESCRIPTION

You receive this warning because you have used the **set_floorplan_port_options** command with the **-x_bounds** and/or **-y_bounds** options to set bound for this port. However, the coordinates of the specified bound conflict with the core area or are not meaningful. For example, you might have specified a bounding box not within the core area or not overlapping with it. The placement tool cannot honor this bound.

WHAT NEXT

No action is required on your part. Check the value you specified for the **-x_bounds** or **-y_bounds** options. Ensure that the bound is reasonable for the intended floorplan.

SEE_ALSO

set_floorplan_options (2), **set_floorplan_port_options** (2).

PSYN-253 (warning) Cell %s is outside of its hard bound.

DESCRIPTION

You receive this warning because the tool has found that the named cell is not placed within its specified hard bound. The violation occurs because its placement is not legal.

WHAT NEXT

No action is required on your part unless you want to use the **legalize_placement** command to make the placement legal.

legalize_placement (2).

PSYN-254 (warning) lib cell '%s' height(%d) is different from its site height(%d).

DESCRIPTION

You receive this warning because the specified cell height is different from its lib site height. In the physical library, you might have defined a cell linked to the lib site with a different height.

WHAT NEXT

No action is required on your part unless you want to examine the physical library to see if the cell is linked to the correct lib site.

SEE ALSO

report_cell (2), **report_lib** (2).

PSYN-255 (warning) Cannot derive the location for port '%s' from placement.

DESCRIPTION

You receive this warning because the tool cannot determine the port location from placement. Usually this is because this port is not connected to a cell in the netlist. In this case, the tool sets its location to an available routing track. Side constraint will be honored for such a port.

WHAT NEXT

No action is required on your part unless you want to check the netlist and, if necessary, set the location for this port by using the **set_port_location** command.

SEE ALSO

set_port_location (2).

PSYN-256 (warning) The orientation of the fixed cell '%s' does

not match legal orientations. Ignoring the legal orientations.

DESCRIPTION

You received this warning because the named cell is fixed but its orientation does not match any of the legal orientations defined for the cell. Because it is a fixed cell, the tool uses its orientation and ignores the legal orientations.

WHAT NEXT

No action is required on your part if the cell is in the orientation you want. Otherwise, you can set the legal orientations for the fixed cell by using the **set_fp_macro_options** command with the **-legal_orientations** option.

SEE ALSO

set_fp_macro_options(2)

PSYN-257 (warning) Cell '%s' has a relative constraint with cell '%s'. Its legal orientations have to be with same footprint of initial orientation '%s'.

DESCRIPTION

You receive this warning to let you know that the tool has detected a relative constraint (an alignment) for the named cell with another cell. The placement tool rotates the cell only within legal orientations. For cells with relative constraint: If the defined legal orientations do not have the same footprint, to start orientation the tool chooses those orientations that do. (The default is north, or first legal orientation.)

WHAT NEXT

If the orientation the tool set is the one you want, you do not have to do anything. If the orientation is not what you want, define legal orientations for the named cell, using the **set_mpc_macro_options** command and its **-legal_orientation** option with a value of **list**. Then start the orientation by invoking the **rotate_objects -to** command with the legal orientations defined, as follows: **rotate_objects -to** *legal_orientation*.

SEE ALSO

rotate_objects(2)
set_mpc_macro_options(2)

PSYN-258 (warning) '%s' is invalid with '%s'. Ignore it ...

DESCRIPTION

You receive this warning message from the **set_floorplan_macro_options** command or the **set_floorplan_macro_array** command because you did not correctly specify the **-x_offset** or -**y_offset arguments** for the macro bound or macro array, respectively, when you ran these commands.

Specify the anchor offset for a macro cell or macro array involving the edges of the core area by defining **-x_offset** or **-y_offset** as follows:

• For anchor bound top (**t**) and bottom (**b**), only the **-y_offset** is allowed. The value specifies the distance to the top or bottom edge, and the value must be positive (>0).

• For anchor bound left (**l**) and right (**r**), only the **-x_offset** is allowed. The value specifies the distance to the left edge or the right edge, and the value must be positive (>0).

• For anchor bound at corners (**bl**, **tl**, **br**, **tr**), both the **-x_offset** and the **-y_offset** are allowed; you can specify either or both offsets. The values specify the distance to the edges of each corner, and the values must be positive (>0).

• For anchor bound bottom-middle (**bm**), top-middle (**tm**), right-middle (**rm**), left-middle (**lm**), and center (**c**), both the **-x_offset** and the **-y_offset** are allowed. The value can be positive or negative.
For **tm** or **bm**:

• The **-y_offset** specifies the distance to the top edge or the bottom edge.

• The **-x_offset** specifies the offset of the center of the macro or the macro array to the middle line. A negative value defines the center as left of the middle line. A positive value defines the center as right of the middle line.
Apply this interpretation also to the values for **lm**, **rm**, and **center**.

WHAT NEXT

This message is only a warning and requires no action on your part. However, you might want to confirm that you intended to specify offset values. Also confirm that the tool can ignore the offset you specified, without causing unwanted alteration of your design.

SEE ALSO

set_floorplan_macro_array (2), **set_floorplan_macro_options** (2).

PSYN-259 (error) Unable to fix static noise without enabling

delta delay in signoff_opt.

DESCRIPTION

You receive this error because you are trying to run **signoff_opt** command on a design that has enabled static noise fixing but not delta delay.

In signoff_opt, it is required to have enabled delta delay in order to fix static noise.

It is not required to enable static noise fixing if you just want to fix delta delay.

WHAT NEXT

Run **set_si_options** to enable delta delay together with static noise.

SEE_ALSO

signoff_opt(2)
set_si_options(2)

PSYN-260 (warning) Resistance of layer %s varies more than the specified factor (%.2f) from layer %s.

DESCRIPTION

You receive this warning because the resistance for the given routing layer varies more than the specified factor from another routing layer. This determination is made to check for the possibility of specifying the wrong resistance or "Poly" values as the routing layer. "Poly" should not be specified as a routing layer. You might receive this warning only because of differences in metal width for different routing layers:

WHAT NEXT

No action is required on your part.

SEE ALSO

check_physical_constraints (2).

PSYN-261 (warning) Capacitance of layer %s varies more than

the specified factor (%.2f) from layer %s.

DESCRIPTION

You receive this warning because the capacitance for the given routing layer varies more than the specified factor from another routing layer. This determination is made to check for the possibility of specifiing the wrong capacitance or "Poly" values being as the routing layer. "Poly" should not be specified as a routing layer. You might receive this warning only because of differences in metal width for different routing layers:

WHAT NEXT

No action is required on your part.

SEE ALSO

check_physical_constraints (2).

PSYN-262 (error) RC values for Layer : %s, Resistance : %g, Capacitance : %g.

DESCRIPTION

You receive this message because the resistance or capacitance for the routing layer %s is set to zero. The resistance or capacitance for the routing layer should not be zero.

WHAT NEXT

Examine the physical library, and correct the RC values for the given layer.

SEE ALSO

check_physical_constraints (2).

PSYN-263 (error) Library %s has no metal layer information.

DESCRIPTION

You receive this error message because the physical library does not contain the metal layers information.

WHAT NEXT

Check the physical library and provide the missing routing layer information, and then rerun the command.

SEE ALSO

check_physical_constraints (2).

PSYN-264 (error) %s is set to 0 (illegal) for metal layers.

DESCRIPTION

You receive this message because the width, spacing, or pitch is set to zero for metal layers.

WHAT NEXT

Examine the physical library, and provide the missing metal layer information.

SEE ALSO

check_physical_constraints (2).

PSYN-265 (error) The pitch and width difference is less than min space for metal layer %s.

DESCRIPTION

You receive this message because the width, spacing, and pitch do not follow the rule:

```
space > pitch - width
```

If the minimum spacing is not followed, design rules are violated and the design might not be fabricated.

WHAT NEXT

Correct the values for the specified metal layer.

SEE ALSO

check_physical_constraints (2).

PSYN-266 (warning) Missing %s nets in the floorplan.

DESCRIPTION

You receive this warning because there are no power or ground nets in the floorplan.

WHAT NEXT

No action is required on your part. However, you can determine whether ground and power nets are defined in the floorplan. Absence of power nets might lead to illegal placements later.

SEE ALSO

check_physical_constraints (2).

PSYN-267 (error) Cell '%s' (lib_cell: %s, lib_site: %s) has no associated site row defined in the floorplan.

DESCRIPTION

You receive this error because this std cell's site does not match the site row - site definition in the design . This will cause that this std cell could not be placed by the placer.

The site rows in the floorplan generated either by reading Design Exchange Format (.def) file, or pre defined in the MW database (by: **initialize_floorplan** or by: **copy_floorplan** or by: **create_site_row** commands).

The std cells in the design should have same site definitions as the rows in the floorplan.

For example: in Netlist and Def flow, suppose a standard cell in the design is defined in the physical library as the "CORE" site cell. However, site rows in the floorplan as discribed in the floorplan Design Exchange Format (.def) file has "CORE2" site type . In this case, the **legalize_placement** command cannot place this cell anywhere in the placement area because there is no site row defined for the site type.

WHAT NEXT

1. Examine the physical library to see if the cell is linked to a correct lib site.

2. Examine the library linking to see there is any missing physical library.

3. Examine the floorplan to see if there is unmatched site or unitTile.

4. Fix the mismatches

SEE ALSO

read_def (2) **initialize_floorplan** (2) **create_site_row** (2) **legalize_placement** (2)

PSYN-268 (error) The design is not legalized.

DESCRIPTION

You receive this error message because the **insert_spare_cells** command requires the design to be legalized before any spare cells can be inserted.

WHAT NEXT

Legalize the design using the **legalize_placement** command, and then rerun the **insert_spare_cells** command.

SEE ALSO

insert_spare_cells (2), **legalize_placement** (2).

PSYN-269 (error) Cannot find lib cell (%s) or it is not a technology cell.

DESCRIPTION

You receive this message because the **insert_spare_cells** command cannot insert spare cells for the given library cell. This is because it either does not exist in the linked libraries or is not a technology cell.

WHAT NEXT

Examine the cell name and determine that it exists and is of the correct type.

SEE ALSO

insert_spare_cells (2).

PSYN-270 (warning) Layer %s is missing definition in the physical library.

DESCRIPTION

You receive this warning message when the floorplan has information for the given layer but it is not defined in the physical library.

WHAT NEXT

Check the floorplan and the physical library. The layers defined in the floorplan should have a corresponding definition in the physical library. Check for the correct version of the physical library.

SEE ALSO

check_physical_constraints(2).

PSYN-271 (warning) Via %s is using a layer that is not defined in the physical library.

DESCRIPTION

You receive this warning because the floorplan has information for the given via, but it is not defined in the physical library.

WHAT NEXT

No action is required on your part, unless you want to examine the floorplan and the physical library. A via defined in the floorplan should have a corresponding definition in the physical library. You can also ensure that the version of the physical library is correct.

SEE ALSO

check_physical_constraints (2).

PSYN-272 (warning) The movebound '%s' has also been removed.

DESCRIPTION

This warning message occurs when the **remove_voltage_area** command removes the named movebound, because the movebound was created in and resided within the voltage area that was removed. When the **remove_voltage_area** command removes a specified voltage area, it deletes all movebounds within the voltage area.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Use the **remove_bounds** command to remove movebounds within a voltage area before you remove the voltage area with **remove_voltage_area**.

SEE ALSO

create_bounds(2)
remove_bounds(2)
remove_voltage_area(2)
report_bounds(2)

PSYN-273 (error) Object %s belongs to voltage area %s.

DESCRIPTION

This error message occurs when the object you specified to the **update_voltage_area** command already resides in the voltage area named in this error message. An object cannot reside in two different voltage areas.

WHAT NEXT

Decide which voltage area you want the object to reside in. Then verify the top-level objects associated with that voltage area, using the **report_voltage_area** command. Remove the object from the inappropriate voltage area, using the **update_voltage_area** command with the **-delete** option. Then rerun **update_voltage_area** with the **-add** option.

SEE ALSO

create_voltage_area(2)
remove_voltage_area(2)
update_voltage_area(2)

PSYN-274 (error) Design contains bounds. No voltage areas allowed.

DESCRIPTION

This error message occurs when running the **create_voltage_area** command, because the design you specified contains bounds you created earlier with the **create_bounds** command. Create voltage areas first, then create bounds.

WHAT NEXT

Remove the bounds in your design using the **remove_bounds** command. Then rerun the **create_voltage_area** command to create the voltage area. You can now create bounds, but only after you create the voltage area.

SEE ALSO

create_voltage_area(2)
remove_bounds(2)
remove_voltage_area(2)
report_voltage_area(2)

PSYN-275 (error) Voltage area %s already exists in the design.

DESCRIPTION

This error message occurs when running the **create_voltage_area** command, because the name of the voltage area you defined already exists in the design. The voltage areas have unique names for identification purposes.

WHAT NEXT

To create a new voltage area with a name that does not already exist in the design, use the **report_voltage_area** command to verify the names of all voltage areas already present in the design. Then use the **create_voltage_area** command to create the voltage area with a new name.

SEE ALSO

create_bounds(2)
create_voltage_area(2)
remove_bounds(2)
remove_voltage_area(2)
report_bounds(2)

PSYN-276 (error) Cell %s must be top-level hierarchical cell of the current design.

DESCRIPTION

This error message occurs when running the **create_voltage_area** command, because the named cell is not a top-level hierarchical cell in your design. The command can only create a voltage area when the specified cell is a top-level hierarchical cell.

WHAT NEXT

Verify the top-level cells associated with your design using the **report_voltage_area** command. Select the top-level hierarchical cell for which you want to create a voltage area. Rerun **create_voltage_area**, specifying the name of the top-level cell you selected.

SEE ALSO

create_bounds(2)
create_voltage_area(2)
remove_bounds(2)
remove_voltage_area(2)
report_bounds(2)

PSYN-277 (error) Voltage area %s has utilization greater than 1.

DESCRIPTION

This error message occurs when running the **create_voltage_area** command, because the tool finds that the area of the voltage area you defined is smaller than the total area of the fixed and standard cells. When you create a voltage area with the **-coordinate** option of the **create_voltage_area** command, and it is too small, you need to change the coordinates, to make the voltage area larger.

WHAT NEXT

Determine the total area of the cells associated with the voltage area you defined, using the **report_cell** command. Using the **-coordinate** option of **create_voltage_area**, adjust the coordinates to enlarge the voltage area. Or use the **-anchor** option of **create_voltage_area** to specify that the anchor point is to automatically derive the shape of the voltage area. Run the **create_voltage_area** command again.

SEE ALSO

attach_voltage_area(2)
create_voltage_area(2)

detach_voltage_area(2)
remove_voltage_area(2)
report_cell(2)

PSYN-278 (error) Cannot find a legal location for '%d' spare cells.

DESCRIPTION

You receive this message because the **insert_spare_cells** command cannot insert the specified number of spare cells. This is because there are no legal locations for those cells in the placed design.

WHAT NEXT

Examine the floorplan for chip density and site types.

SEE ALSO

insert_spare_cells (2).

PSYN-279 (error) The specified subdesign '%s' does not exist.

DESCRIPTION

You receive this message because the **insert_spare_cells** command cannot find the specified design hierarchy object.

WHAT NEXT

Examine the specified object name and reissue the command.

SEE ALSO

insert_spare_cells (2), **report_cell** (2), **report_hierarchy** (2).

PSYN-280 (error) Unable to load PrimeTime image due to %s.

DESCRIPTION

You receive this error because **signoff_opt** is not able to load a PrimeTime image that is specified in **set_primetime_options**. **signoff_opt** could fail to load the image due to one or more of the following reasons:

- The specified image contains inconsistent library
- The specified image contains inconsistent netlist
- The specified image contains inconsistent power domain

WHAT NEXT

If the specified image contains inconsistent library, please ensure that all target libraries in **IC Compiler** (or its corresponding min version if the image is intended for min corner) are visible in the image. You can re-generate the PrimeTime image using the correct link path. You can also use **-ignore_library_mismatch** to overwrite.

If the specified image contains inconsistent netlist, you can either re-generate the PrimeTime image using the same MW CEL as **IC Compiler**, or re-generate a MW CEL for **IC Compiler** using the same netlist your **PrimeTime** uses.

If the specified image contains inconsistent power domains, you can correct the mismatch in your standalone **PrimeTime** run, and re-generate the PrimeTime image by saving a new session using **save_session** in PrimeTime.

EXAMPLE

You’re running **signoff_opt** in BCWC mode, and you have the following settings in your **IC Compiler** run:

```
set target_library "slow.db" set link_library "* slow.db" set_min_library -min
fast.db slow.db ... open_mw_cel -lib mymw mycel
```

Your standalone max corner **PrimeTime** script should look like:

```
set link_path "* slow.db" read_milkyway -library mymw mycel
```

And your standalone min corner **PrimeTime** script should look like:

```
set link_path "* fast.db" read_milkyway -library mymw mycel
```

SEE_ALSO

run_signoff(2)
signoff_opt(2)
set_primetime_options(2)

PSYN-281 (error) Voltage area %s does not exist in the design.

DESCRIPTION

This error message occurs when running the **update_voltage_area** command, because the tool finds that the specified voltage area does not exist in your design, so the tool is unable to continue.

WHAT NEXT

Run the **report_voltage_area** command to verify the names of all voltage areas that exist in the design. Rerun the **update_voltage_area** command, using the correct voltage_area name.

SEE ALSO

create_bounds(2)
create_voltage_area(2)
remove_voltage_area(2)
report_voltage_area(2)
update_voltage_area(2)

PSYN-282 (error) Default voltage area '%s' already specified.

DESCRIPTION

This error message occurs when running the **create_voltage_area** command, because a default voltage area, which is already present in the design and covers all of the cells that are not within any specified voltage areas, is in conflict with the voltage area you want to create now.

WHAT NEXT

Remove the default voltage area using the **remove_voltage_area** command. Rerun the **create_voltage_area** command.

SEE ALSO

create_voltage_area(2)
remove_voltage_area(2)
report_voltage_area(2)

PSYN-283 (warning) Given coordinates are greater than

MAX_INT.

DESCRIPTION

You receive this warning message because one or more of the given coordinates are greater than MAX_INT (0x7FFFFFFE).

WHAT NEXT

No action is required on your part. However, you can check the value of the coordinates to ensure that they are valid for your purpose.

PSYN-284 (warning) Ignoring variable %s, use set_pnet_options command.

DESCRIPTION

You receive this warning to inform you that the variable named in the message is obsolete, and the tool ignores it. To set the pnet layer options, use the **set_pnet_options** command. The obsolete variables that evoke this warning are: **physopt_minimum_pnet_height**, **physopt_minimum_pnet_width**, **physopt_pnet_complete_blockage_layer_names**, **physopt_pnet_partial_blockage_layer_names**, and **physopt_pnet_via_additive**.

For example: the variable: set physopt_pnet_complete_blockage_layer_names "M1 M2" should be replaced by command: set_pnet_options -complete {M1 M2}

the variable: set physopt_pnet_partial_blockage_layer_names "M1 M2" should be replaced by command: set_pnet_options -partial {M1 M2}

WHAT NEXT

Verify the pnet settings using the **report_pnet_options** command. Then set or change the pnet option settings using **set_pnet_options**. To remove pnet options, use the **remove_pnet_options** command.

SEE ALSO

remove_pnet_options (2), **report_pnet_options** (2), **set_pnet_options** (2).

PSYN-285 (warning) Not enough space (too thin).

DESCRIPTION

You receive this warning to let you know that, within the region you specified, gaps exist in the row of sites.

You receive this message for one of two reasons:

• The filler cells you specified are not small (or thin) enough to fill in all the spaces between all cells in your design.

• The placement boundary is not on the site grid, which leaves a space between a placement boundary and a valid site grid location.

WHAT NEXT

Define a list of narrower filler cells for the same region of your floorplan. Then rerun the **insert_filler** command on that region. Or snap your placement obstruction to a site grid *before* you run **insert_filler**.

SEE ALSO

insert_filler (2), **remove_filler** (2), **report_filler** (2).

PSYN-286 (warning) Not enough space (too short).

DESCRIPTION

You receive this warning message because some sites are not filled by filler cells within the region you specified with the **insert_filler** command. This is because the filler cells you specified are too tall to fit into the available space in the sites.

WHAT NEXT

Define a list of shorter filler cells for the same region of your floorplan. Rerun the **insert_filler** command on that region.

SEE ALSO

insert_filler (2), **remove_filler** (2), **report_filler** (2).

PSYN-287 (information) This region is assigned with ID %d.

DESCRIPTION

You receive this message to let you know that the **set_routing_wire_model** command has created an ID for the regional routing wire model in your design. Use this ID with the **remove_routing_wire_models** command if you want to remove the regional routing wire model. Use it also with the **report_routing_wire_models** command to review regional routing wire models in the design.

The tool always assigns an ID of 0 to a routing wire model for a design, and IDs beginning from 1 to regional routing wire models.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

remove_routing_wire_models (2), **report_routing_wire_models** (2), **set_routing_wire_model** (2).

PSYN-288 (Warning) Routing wire model ID ’%d’ is invalid and is ignored.

DESCRIPTION

You receive this message from the **report_routing_wire_models** command or the **remove_routing_wire_models** command because the routing wire model ID you specified in the command is not a valid ID; and the tool ignores it.

WHAT NEXT

Use the **report_routing_wire_models** command to check the routing wire model ID. Then run the command again.

SEE ALSO

remove_routing_wire_models (2). **report_routing_wire_models** (2).

PSYN-289 (Error) Via '%s' is already defined in design db.

DESCRIPTION

You receive this message from the **define_via** command, because the via you specified in your design is already defined in the design .db file.

WHAT NEXT

Use the previously defined via in your design, or define the new via using a different name. Then run the command again.

SEE ALSO

define_via (2).

PSYN-290 (Error) No '%s' defined for define_via command.

DESCRIPTION

You receive this message from the **define_via** command, because you did not specify for the command the option named in the error.

WHAT NEXT

Make sure you are using the correct command syntax. Then run the command again.

SEE ALSO

define_via (2).

PSYN-291 (Error) Layer '%s' is not defined in current design db (rect list '%s').

DESCRIPTION

You receive this message from the **define_via** command, because the layer you specified is not defined in the design .db file.

WHAT NEXT

Make the necessary correction to the layer name. Then run the command again.

SEE ALSO

define_via (2).

PSYN-292 (Error) Cannot recognize the pattern of given list '%s' for -rect option.

DESCRIPTION

You receive this message from the **define_via** command, because the geometry pattern you specified for the **-rect** option of the command is not correct.

WHAT NEXT

Make sure you are using the correct syntax. Then run the command again.

SEE ALSO

define_via (2).

PSYN-293 (Error) No via def is found in current design db. You have to read in PDEF file before defining a special via.

DESCRIPTION

You receive this message from the **define_via** command, because the tool cannot generate a special via (and therefore fails). This occurs because no via definition exists in the current design.

WHAT NEXT

Read in the PDEF file that contains the via definition. Then run the command again.

SEE ALSO

define_via (2).

PSYN-294 (warning) Setting default orientation '%s' on the object '%s'.

DESCRIPTION

This warning occurs because you tried to set the location on an object for which you have not defined an orientation by using the **set_cell_location** command. The tool sets a default orientation on such objects.

WHAT NEXT

This message is only a warning and requires no action on your part if you accept the default orientation the tool sets on the object.

To set a desired orientation for the object named in the message, first excute the **rotate_object** command, then run the **set_cell_location** command again.

SEE ALSO

rotate_object(2)
rotate_objects(2)
set_cell_location(2)

PSYN-295 (warning) legalize -timing option can only be used with -incr option, -timing is disabled.

DESCRIPTION

You receive this warning because you tried to run the **legalize_placement** command, with its **-timing** option specified, without also specifying the command's **-incremental** timing mode. The message is to inform you that the tool therefore disables the **-timing** option.

WHAT NEXT

This message is a warning only and requires no action on your part. However, you most likely want to rerun the command, with both the **-timing** option and the **-incremental** option defined.

SEE ALSO

legalize_placement (2).

PSYN-296 (warning) legalize -clip option can only be used with -coord option, -clip is disabled.

DESCRIPTION

You receive this warning because you tried to run the **legalize_placement** command, with its **-clip** option specified, without also specifying the command's **-coordinate** option, which is the regional legalize mode. The message is to inform you that the tool therefore disables the **-clip** option.

WHAT NEXT

This message is a warning only and requires no action on your part. However, you most likely want to rerun the command, with both the **-clip** option and the **-coordinate** option defined, as shown in this example:

```
legalize_placement -coord {llx lly urx ury} -clip ...
```

SEE ALSO

legalize_placement (2).

PSYN-297 (warning) Setting the value of option %s removes the value of the conflicting option %s automatically.

DESCRIPTION

You receive this warning message because the above two options cannot be valid at the same time.

WHAT NEXT

To prevent this warning message, remove the first option before setting the second option.

SEE ALSO

remove_xtalk_router_options (2), **set_xtalk_router_options** (2).

PSYN-298 (warning) Removing routing for non dont touch nets.

DESCRIPTION

You get this warning because you are modifying netlist on a post-route design. The routing information may not be valid, hence need to be deleted. You may need to re-route your design after completing this command.

WHAT NEXT

Run "route" command if you need a routed design.

PSYN-299 (warning) Physical net %s has %s type. Potential special net should have either GND,PWR or CLOCK type.

DESCRIPTION

You receive this warning message because the named physical net has an incorrect type and cannot be treated as a special net.

WHAT NEXT

Check the initial floorplan and the PDEF (Physical Design Exchange Format) file for the correct type of the net, and then run the command again.

SEE ALSO

compile_clock_tree (2), **physopt** (2).

PSYN-300 (warning) Non-rectilinear edge was found in port/obstruction geometry.

DESCRIPTION

This warning occurs because there is a polygon-shaped port or obstruction geometry that contains at least one non-rectilinear edge. The tool ignores this type of non-rectilinear geometry.

WHAT NEXT

This is a warning message only. No action is required on your part.

However, you can check the original Synopsys Physical Library (.plib) file or Library Exchange Format (LEF) file to ensure that all polygons are rectilinear and make changes as necessary. Then, run the command again.

PSYN-301 (warning) cannot find location in physical lib cell for the pin %s

DESCRIPTION

You receive this warning message because the tool cannot set the bounds for a specific pin in the macro cell, since there is no location information in the physical library view for the specified pin.

The cause might be that the pin is logical only, the cell is logical only, or there is no port geometry definition in the physical library definition.

WHAT NEXT

You can either check the **link_physical_library** command information to ensure that the physical cell is linked, or you can use the following command to bound a specific location of the macro cell directly.
set_macro_cell_bound_spot -coordinate {x y} [get_cells "<macro_cell_name>"]

This command works around the pin problem by allowing you to specify the spot of the macro cell that needs to be bounded.

SEE ALSO

create_bounds (2), **link_physical_library** (2), **set_macro_cell_bound_spot** (2), **update_bounds** (2).

PSYN-302 (Information) bound pin %s in cell %s at (%d %d) only.

DESCRIPTION

You receive this information message because the **create_bounds** or **update_bounds** command set the bounds for a specific pin location in the macro cell.

The pin might have multiple port geometries in various locations. Only the first selected location is used and the tool only bounds that spot of the macro cell. All other port locations of the same pin are not bounded.

For example, the macro cell might have multiple CLK port geometries in different locations. In the following example, the **create_bounds** command finds the first port

location of the CLK pin in the macro cell and applies the move bound on this port location.
create_bounds -coord {0 0 100 100} [get_pins "macro_cell/CLK"]

WHAT NEXT

This is an informational message only. No action is required on your part.

However, if you want to force the **create_bounds** command to apply to a different port location, use the following command to directly bound a specific location of the macro cell, substituting the coordinates *0 0 100 100* and *x y*, and the *macro_cell_name* as necessary.
create_bounds -coord {0 0 100 100} [get_cells "<macro_cell_name>"]
set_macro_cell_bound_spot -coord {x y} [get_cells "<macro_cell_name>"]

SEE ALSO

create_bounds (2), **set_macro_cell_bound_spot** (2), **update_bounds** (2).

PSYN-303 (warning) object %s is not a cell object

DESCRIPTION

You receive this warning message because the object specified in the command line is not a cell object in the design db. A cell object must be specified in the command line.

The command **[get_cells "cell_name"]** requires that the cell name be a full path name, such as **top/blk1/blk1_1/.../cell_name**, where *top* is the top cell name in the current design.

WHAT NEXT

Check the object specified in the command line. Use the **get_cells** command to determine if the object is a cell.

SEE ALSO

get_cells (2).

PSYN-304 (information) Backward compatibility mode is

enabled for signoff_opt.

DESCRIPTION

You receive this information message because the backward compatibility mode is enabled in **signoff_opt**.

Backward compatibility mode will be automatically enabled if **signoff_opt** detects that you have passed a version of signoff tool, such as **StarRCXT** or **PrimeTime** that is not fully compatible with **IC Compiler** to run **signoff_opt**. You will notice some impacts on both runtime and quality of results.

WHAT NEXT

This is an informational message only. However, it is recommended that you always use a version of signoff tool, such as **StarRCXT** or **PrimeTime** which at least has the same major version of **IC Compiler**. For example, **IC Compiler Z-2007.03** should be used with **StarRCXT Z-2006.12** and **PrimeTime Z-2006.12**, not **StarRCXT Y-2006.06** or **PrimeTime Y-2006.06**.

SEE ALSO

signoff_opt(2)
set_primetime_options(2)
set_starrcxt_options(2)

PSYN-305 (warning) Macro pdbs %s have more layers than the layers
in tech pdb %s. The additional layers are ignored.

DESCRIPTION

This warning occurs because you are linking in technology physical library database (.pdb) files and macro .pdb files. Technology .pdb files describe the process layers, and macro .pdb files describe the standard cells and RAMs that you want to use.

This warning occurs if all of the conditions in the following example are met. Given a technology .pdb file that has *n* layers and macro .pdb files that have *m1,m2*... layers, and the macro .pdb file layers (*m1,m2*...) are greater than the technology .pdb file layers (*n*).

The extra layers in the macro .pdb files are used to describe routing obstructions. These layers do not form any functional part of the cells, but the tool uses them for RC calculations. The library vendor creates cells with extra layers so that a single cell definition can be used by multiple process libraries without duplicating the same cell description.

Example Message

```
Warning: Macro pdbs SIARC_WIDE1 SIARC_WIDE2 have more layers than the layers
         in tech pdb SIARC25. The additional layers are ignored. (PSYN-305)

         Tech pdb  SIARC25        :  5 layers
         Macro pdb SIARC_WIDE1    :  6 layers
         Macro pdb SIARC_WIDE2    :  7 layers
```

WHAT NEXT

Ensure that you have specified the correct physical libraries. If the specified libraries are correct, ignore the warning message.

SEE ALSO

physopt(2)
report_timing(2)

PSYN-306 (warning) All cells with more than %d rows are set back to original location.

DESCRIPTION

You receive this warning message because the legalizing process does not move cells that would be displaced more than the number of specified rows. This warning message occurs when you set following variable:
set physopt_max_displace_rows <number>

The *<number>* indicates the maximum number of rows a cell can be moved from its original location. This occurs during the intermediate step in some flows. For example, if you set the number to 10 (as shown below), the legalizing process does not move the cell more than 10 rows away from its original location.
set physopt_max_displace_rows 10

WHAT NEXT

Some cells may not be legalized at the end of the legalizing process, because of the row displacement constraint. Ensure that you unset this variable before the final legalization step in the flow.

SEE ALSO

physopt_max_displace_rows (2).

PSYN-307 (warning) you are using %s, please use set_pnet_options command.

DESCRIPTION

You receive this warning message because you used variables that may now be obsolete to set the pnet options. Use the **set_pnet_options** command, as described in the **set_pnet_options** man pages.

The obsolete variables that produce this warning message are as follows:

physopt_minimum_pnet_height
physopt_minimum_pnet_width
physopt_pnet_complete_blockage_layer_names
physopt_pnet_partial_blockage_layer_names
physopt_pnet_via_additive

Replace prior usages of the command with the **set_pnet_options** command, as shown below.

- Example of the prior usage: **set physopt_pnet_partial_blockage_layer_names "M1 M2"**
- Example of the new usage: **set_pnet_options -partial {M1 M2}**

The **set_pnet_options** command can only be applied after the design is read. This is different from prior usage, which allowed the variable to be set anywhere before placement.

WHAT NEXT

Verify the pnet settings using the **report_pnet_options** command. Set or change the pnet option settings using **set_pnet_options**. To remove pnet options, use the **remove_pnet_options** command.

SEE ALSO

remove_pnet_options (2), **report_pnet_options** (2), **set_pnet_options** (2).

PSYN-308 (information) Critical range constraint is used for TNS optimization.

DESCRIPTION

You receive this information message when the **physopt** command takes the critical range constraint set by the **set_critical_range** command into consideration during timing optimization.

WHAT NEXT

This message is informational only and requires no action on your part.

All of the paths from the critical range specified in the **set_critical_range** command are optimized.

SEE ALSO

physopt (2), **set_critical_range** (2).

PSYN-309 (information) Your design has at least %d %s violating end points.

DESCRIPTION

You receive this message because you are trying to run **signoff_opt** command on a design that has some timing violations. The number of timing violations reported is the lower bound of all timing violations existing in your design.

WHAT NEXT

Run **report_constraint -all_violators** to see the details of violations.

SEE_ALSO

signoff_opt(2)
report_constraint(2)

PSYN-310 (warning) '%s' %s keepout does not extend upto block boundary.

DESCRIPTION

You receive this warning message because the keepout being inverted does not extend up to the die area boundary (or the core area boundary, if the die area is not specified).

Problems at the top level might arise if the coordinates are not adjusted. When propagating keepouts to the top level using the **propagate_ilm** command, the inverted keepout area is made available as a placement or wiring resource, and the rest of the ILM block area is marked as a keepout at the top level. The result is a placement or wiring resource surrounded by keepouts.

WHAT NEXT

Check and adjust the keepout coordinates as needed.

• Use the **report_placement_keepout** or the **report_wiring_keepout** command to obtain the keepout coordinates.

• Use the **get_die_area** or the **get_placement_area** command to obtain the block coordinates.

SEE ALSO

get_die_area (2), **get_placement_area** (2), **propagate_ilm** (2), **report_placement_keepout** (2), **report_wiring_keepout** (2), **set_die_area** (2), **set_inverted_placement_keepout** (2), **set_inverted_wiring_keepout** (2).

PSYN-311 (error) '%s' option for this command is only available in psyn_shell.

DESCRIPTION

You receive this error message because you are either running a command or passing an argument that requires you to be running in the psyn_shell.

WHAT NEXT

Invoke the psyn_shell and run the command again.

PSYN-312 (error) '%s' No ILM sub-designs in current design.

DESCRIPTION

You receive this error message because the command requires ILM subdesigns in the current design in order to run.

WHAT NEXT

Read in the ILM models for the ILM subdesigns and run the command again.

PSYN-313 (error) Could not create %s keepout named

’%s’.

DESCRIPTION

You receive this error message because the **propagate_ilm -keepout** command tried to subtract the inverted keepouts from the area of the block and then create keepouts, but an error occurred in the creation of the keepout.

WHAT NEXT

Delete all of the propagated keepouts and run the command again.

SEE ALSO

remove_placement_keepout (2), **remove_wiring_keepout** (2).

PSYN-314 (error) Cell ’%s’ not an ILM cell.

DESCRIPTION

You receive this error message when the **propagate_ilm** command cannot run on the specified cell because it is not an ILM cell.

WHAT NEXT

Delete the cell from the cell list and run the command again.

SEE ALSO

extract_ilm (2), **identify_interface_logic** (2), **propagate_ilm** (2).

PSYN-315 (error) To run xtalk_reduction, please enable SI.

DESCRIPTION

You receive this error message because xtalk_reduction is enabled but SI flow is not enabled. The xtalk_reduction is effective on delta delay, switching noise and static noise. To run xtalk_reduction, at least one of SI effects such as delta delay, switching noise and static noise has to be used. To enable SI effect, please use **set_si_options**.

WHAT NEXT

Please set any one of SI effects through **set_si_options**.

SEE ALSO

signoff_opt (2) **set_si_options** (2)

PSYN-316 (Warning) The %s is not big enough to accommodate all the IO pads, some IO pads may be placed outside of IO sites!

DESCRIPTION

You receive this message because the core size is not big enough to accommodate the IO pads. Some IO pads may be placed outside of IO sites.

WHAT_NEXT

You can enlarge the core size to avoid this problem.

SEE ALSO

PSYN-317 (Warning) The %s IO Margin is not big enough to accommodate the IO Pads! Expand the IO Margin(Die Area) automatically !

DESCRIPTION

You receive this message because the IO Margin is not big enough to accommodate the IO pads. MPC will expand the IO Margin (Die boundary) in order to place the IO cells.

WHAT_NEXT

If you would like, you can set the IO Margin again. Otherwise MPC will expand the IO Margin automatically.

SEE ALSO

PSYN-318 (Warning) The destination core size can not accommodate all of the children cells, expanding core size automatically. The user-specified utilization/aspect_ratio value(s) may not be respected !

DESCRIPTION

You receive this message because there are some conflictions among user specified values of core_width, core_height, utilization and aspect_ratio. Also MPC will make sure that both generated core_height and core_width should be no less than the maximum child_height and maximum child_width of all the children cells.

WHAT_NEXT

Set the options (core_width, core_height, utilization, aspect_ratio) again and make sure that there will be no confliction among your setting. Also your setting need to make sure that the destination core_height and core_width should not be less than the maximum child_height and maximum child_width of all the children cells.

SEE ALSO

PSYN-319 (Error) The core height setting of %s is less than the height of its children !

DESCRIPTION

You receive this message because you have set the core_height less than the height of its children.

WHAT_NEXT

Set the core_height again using command set_floorplan_options, and make sure that the core_height is not less than the maximum height of its children.

SEE ALSO

PSYN-320 (error) Width of trunk -width ’%f’ less than minimum

in the physical library '%f'.

DESCRIPTION

You receive this error message when you specify the **-width** value of the pnet to be less than the width specified for the metal layer (**-metal**) in the physical library.

This is a violation because the width must be equal to or greater than the width specified for the layer in the physical library.

The tool does not assume a default for the width, since it might default to a very narrow power trunk, and that might be an optimistic assumption.

WHAT NEXT

Specify the **-width** value to be greater than or equal to the minimum metal width specified for the library shown in the error message.

SEE ALSO

set_floorplan_pnet_options (2).

PSYN-321 (error) Pitch between trunks -pitch '%f' less than minimum in the physical library '%f'.

DESCRIPTION

You receive this error message when you specify the **-pitch** value of the pnet trunks to be less than the width specified for the metal layer (**-metal**) in the physical library.

This is a violation because the pitch must be equal to or greater than the pitch specified for the layer in the physical library.

The tool does not assume a default for the pitch, since it might default to a highly congested power structure, and that might be a pessimistic assumption.

WHAT NEXT

Specify the **-pitch** value to be greater than or equal to the minimum pitch specified for the library shown in the error message.

SEE ALSO

set_floorplan_pnet_options (2).

PSYN-322 (Error) The core width setting of %s is less than the width of its children !

DESCRIPTION

You receive this error message because the **core_width** is set to less than the width of its children.

WHAT NEXT

Reset the **core_width** using the **set_floorplan_options** command. Ensure that the **core_width** is not less than the maximum width of its children.

SEE ALSO

set_floorplan_options (2).

PSYN-323 (Error) There are no meaningful cells in the netlist of design %s!

DESCRIPTION

You receive this error message because the design does not contain any meaningful cells in the netlist. For example, the tool filtered all dangling cells that do not have any connection in the netlist.

WHAT NEXT

Check the input data, make the necessary corrections, and then run the command again.

PSYN-324 (Warning) ignore user set_via_region on pin %s of lib cell %s because via is not defined.

DESCRIPTION

This message shows the uset set_via_region on the particular pin is ignored because the via on the pin layer and its upper layer has no VIA defined (or loaded) from physical lib. Please check your physical lib and make sure the via is defined and report the physical lib to make sure the via is loaded. If via is not defined, the via_region is meaningless. For example, if the pin layer is metal1, you set via

region of via12 on the pin. However if the via12 is not defined in the lib, then the via_region is meaningless.

WHAT NEXT

check physical lib and report physical lib to see if the via is defined.

PSYN-325 (warning) Corrupted SI options found in database.

DESCRIPTION

You receive this warning message because **IC Compiler** found your SI options in the database are corrupted.

WHAT NEXT

Please use **report_si_options** to check your SI options, and re-run **set_si_options** to set your SI options if necessary.

SEE ALSO

signoff_opt (2) **set_si_options** (2) **report_si_options** (2)

PSYN-326 (error) The distance between the left edge of the core area and the left edge of row %s is not of multiple site width.

DESCRIPTION

This error occurs because the distance between the left edge of the core area and the left edge of the row is not of multiple site width. The tool does not support this irregular site array. This might create a routing track alignment problem.

WHAT_NEXT

Check your floorplan (site array) and the core area setting to ensure that the distance of the row X location and the core area left X is of multiple site width. For example, given a row location at (10, 0) with a core site width of 5, and a core area of llx = 0, then the equation (10-0)/5=2 is an integer (that is, it is a multiple site width), so this is a correct site row. If, for example, the row is located at (8, 0), then (8-0)/5 does not equal an integer (that is, it is not a multiple site width), so this is not a correct row.

PSYN-327 (information) Using auto-derived max SDC %s and min SDC %s.

DESCRIPTION

You receive this message because **signoff_opt** automatically runs two **PrimeTime** with two timing corners, using two SDC files that are derived from your original SDC file.

signoff_opt invokes **PrimeTime** timing engine to perform static timing analysis. With signal integrity effects enabled, such as delta delay or static noise, **PrimeTime SI** is used. **PrimeTime SI** always uses on_chip_variation (OCV) mode, therefore, if you have two timing corners with **set_min_library**, timing will be computed using both timing corners as library OCV. This leads to pessimistic timing results which are not desired.

In this case, **signoff_opt** will pass only max library to the max corner **PrimeTime** run, and only min library to the min corner **PrimeTime** run. **signoff_opt** will also pass the max corner SDC file and min corner SDC file to the corresponding **PrimeTime** runs. These SDC files are automatically derived from your original SDC file.

WHAT NEXT

If needed, please examine the auto-derived SDC files specified.

SEE ALSO

signoff_opt (2),
set_min_library(2),
set_si_options

PSYN-328 (error) legalize -coordinate option must be used with -cells option.

DESCRIPTION

You receive this warning because you tried to run the **legalize_placement** command, with its **-coordinate** option specified, without also specifying the command's **-cells** option, which indicates which cells are going to be legalized inside the region specified with -coordinate. The message is to ask you to re-enter the legalize_placement command with the correct options.

WHAT NEXT

This message is an error and ask user to re-enter the correct usage. For example, **legalize_placement -coordinate {llx lly urx ury} -cells [get_cells BLK_A/*]**

SEE ALSO

legalize_placement (2).

PSYN-329 (error) Please specify ’X’ or ’Y’ for direction.

DESCRIPTION

You receive this error because the tool does not recognize the direction you specified for the routing tracks. Valid values for direction are X or Y.

WHAT NEXT

Specify X or Y as the routing track direction, as shown:

```
create_track -dir X
report_track -dir Y
```

SEE_ALSO

create_track(2)
remove_track(2)
report_track(2)
shift_track(2)

PSYN-330 (error) Placeable area (%.2f) of the voltage area is less than total cell area (%.2f).

DESCRIPTION

This error message occurs when the placeable area is too small to place cells inside the voltage area. Areas occupied by macro cells and hard placement keepouts inside the voltage area are excluded from the placeable area. Macro cells are also not considered in the total cell area.

WHAT NEXT

Adjust the coordinates to fit all cells inside voltage area and run the command again.

SEE_ALSO

create_voltage_area(2)

PSYN-331 (information) Saved a snapshot for %s as %s.

DESCRIPTION

You receive this message because a snapshot for **StarRCXT** or **PrimeTime** is saved by **signoff_opt**. A **StarRCXT** snapshot is the run directory of the **StarRCXT** run, and a **PrimeTime** snapshot is the directory created by the **save_session** command in **PrimeTime**. The snapshot contains all the setup that **signoff_opt** uses to run these tools.

You can re-use the corresonding snapshots from **StarRCXT** and/or **PrimeTime** by specifying them in **set_starrcxt_options** or **set_primetime_options**, using **-max_image** or **-min_image**. Running **signoff_opt** with images saves runtime because **signoff_opt** can skip the initial runs of **StarRCXT** and/or **PrimeTime**. Subsequent runs of incremental **StarRCXT** and/or **PrimeTime** will not be affected.

WHAT NEXT

This is just an information message.

SEE ALSO

signoff_opt (2),
run_signoff (2),
set_primetime_options (2),
set_starrcxt_options (2),
report_primetime_options (2),
report_starrcxt_options (2)

PSYN-332 (error) The %s option can only be used in conjunction with the %s command.

DESCRIPTION

The specified option is not valid without specifying the command.

WHAT NEXT

To see the correct use of options, refer to the appropriate documentation.

PSYN-333 (information) Revert back to snapshot %d.

DESCRIPTION

You receive this message to inform you that **signoff_opt** decides to revert back to a snapshot that was saved earlier, which has better quality of results (QoR).

WHAT NEXT

This is an informational message only. No action is required on your part.

PSYN-334 (error) Command is disabled in signoff mode.

DESCRIPTION

You receive this error message because you try to run a command that is disabled in signoff mode. **IC Compiler** enters signoff mode after you call **run_signoff**. In order to use the command, you must exit the signoff mode by calling **run_signoff -signoff_analysis false**.

WHAT NEXT

Call **run_signoff -signoff_analysis false** to exit the signoff mode, and then re-issue this command. Note after you call **run_signoff -signoff_analysis false**, you will lose all signoff data. To see signoff data again, you must call **run_signoff** again.

SEE_ALSO

signoff_opt(2),
run_signoff(2)

PSYN-335 (error) Cannot %s signoff mode without running run_signoff or signoff_opt.

DESCRIPTION

You receive this error because you are trying to run **run_signoff -signoff_analysis false|sleep|wakeup** command on a design that has not been run with **run_signoff** or **signoff_opt** yet. You must run **run_signoff** or **signoff_opt** first before you can run this command.

WHAT NEXT

Use **run_signoff** or **signoff_opt** command to perform signoff analysis or signoff optimization first.

SEE_ALSO

signoff_opt(2),
run_signoff(2)

PSYN-336 (Warning) Dropping %s '%s' because its lower-left corner coordinates are bigger than upper-right corner coordinates.

DESCRIPTION

You receive this message because the coordinates of a rectangle are not given in order from the lower-left corner to the upper-right corner.

WHAT_NEXT

Fix the input so the object mentioned has lower-left corner coordinates before the upper-right corner coordinates, otherwise this object will be ignored.

PSYN-337 (warning) Design readiness check is disabled in signoff_opt.

DESCRIPTION

You receive this warning message because you are running **signoff_opt** command with **-ignore_design_readiness** switch.

signoff_opt has a built-in readiness checker which checks the following conditions: - design shall have no more than 100 violating end points in either best case or worst case analysis - design shall have no routing shorts - number of routing design rule violations shall be no more than 0.1% of number of nets or 100 (whichever is bigger) - number of logic design rule violations shall be no more than 0.1% of number of nets or 100 (whichever is bigger)

If your design fails the design readiness check, and you still force **signoff_opt** to run signoff driven optimization with **-ignore_design_readiness**, the design might not converge to a solution with better quality of results (QoR).

WHAT NEXT

It is recommended that the designs still need to go through regular timing/SI closure flows within **IC Compiler** to reduce the number of violations seen by signoff tools as much as possible.

SEE_ALSO

signoff_opt(2)

PSYN-338 (information) Any existing PrimeTime or StarRCXT image is removed.

DESCRIPTION

IC Compiler uses this information message to tell you that all previously specified PrimeTime and StarRCXT images using **set_primetime_options** and **set_starrcxt_options** are now removed.

You receive this message typically after running **signoff_opt**. After signoff driven optimization, the images are no longer valid due to changes in the database. Thus, **IC Compiler** removes all specified images that are stored in the database to avoid them being used in the subsequent signoff driven analysis or optimization.

WHAT NEXT

This is an informational message only. You can verify the change by calling **report_primetime_options** or **report_starrcxt_options**. You can also specify new images by calling **set_primetime_options** or set_starrcxt_options.

SEE ALSO

set_primetime_options(2)
report_primetime_options(2)
set_starrcxt_options(2)
report_starrcxt_options(2)
signoff_opt(2)

PSYN-339 (information) Hold time fixing is enabled in signoff_opt.

DESCRIPTION

You receive this information message because the hold time fixing is enabled in

signoff_opt. **signoff_opt** enables hold time fixing if any of your clock object has fix_hold attribute set.

WHAT NEXT

This is an informational message only. However, if you do not intend to enable hold time fixing, you can remove the fix_hold attribute from all your clock objects.

SEE ALSO

signoff_opt(2)
set_fix_hold(2)

PSYN-340 (Error) No snapshot exists.

DESCRIPTION

You receive this message because No any snapshot created yet.

WHAT_NEXT

PSYN-341 (Information) No congestion report in current snapshot.

DESCRIPTION

WHAT_NEXT

PSYN-342 (Information) No constraint report in current

snapshot.

DESCRIPTION

WHAT_NEXT

PSYN-343 (Information) No power report in current snapshot..

DESCRIPTION

WHAT_NEXT

PSYN-344 (Information) No qor report in current snapshot..

DESCRIPTION

WHAT_NEXT

PSYN-345 (Information) No route report in current snapshot..

DESCRIPTION

WHAT_NEXT

PSYN-346 (Warning) Can not find snapshot '%s'.

DESCRIPTION

You receive this message because Can not find the specified snapshot.

WHAT_NEXT

PSYN-347 (Information) No clock tree report in current snapshot.

DESCRIPTION

WHAT_NEXT

PSYN-348 (error) Macro cell %s is not fixed.

DESCRIPTION

You receive this error because one or more macros in your design are not fixed. The coarse placer and the detail placer will error out if any macros are not fixed.

By default, ICC detail placement will treat "very tall" standard cells as "hard macros". If a standard cell has a height of more than 6x site heights, then it will be treated as a "hard macros". Please check whether the problematic hard macro is the one that has been described above. If yes, then users will also see "PSYN-442" error message. User can either change their design, or adjust the "default hard macro height threshold" to overcome this issue. To adjust the "default hard macro height threshold" to a "bigger" number, users can use the below command setting:

```
set physopt_macro_cell_height_threshold X
```

Here "X" is an integer number which is bigger than 6.

For example, if the user wants to place some 10x site height cells as "standard cells", then the user can use below command setting:

```
set physopt_macro_cell_height_threshold 11
```

With the above setting, these 10x site height cells will be placed as "standard cells". However, such a practice is not recommended, because the detail placement enginre is not designed for such a design style. Please use it with caution.

For more information for how to adjust the "default hard macro height threshold"or the usage model of variable "physopt_macro_cell_height_threshold", user can refer to the man pages of "PSYN-442" and "physopt_macro_cell_height_threshold".

WHAT NEXT

If your macros are not placed, you should run **create_fp_placement** to place them.

If your macros are placed, you should mark them fixed and try again.

SEE_ALSO

set_dont_touch_placement(2)
create_fp_placement(2)
legalize_fp_placement(2)
create_placement(2)
refine_placement(2)
place_opt(2)
legalize_placement(2)

PSYN-349 (error) You must specify PrimeTime image(s)/tcl(s) to run %s.

DESCRIPTION

You receive this error because **signoff_opt** is not able to automatically run **PrimeTime** with one of the following reasons:

- Running with advanced on-chip-variation mode (AOCVM)
- Running with variation based analysis (VX)

Thus, you must provide **PrimeTime** saved session for each corner/scenario, or provide PT TCL file, using **set_primetime_options**.

Optionally, you can also run your own Star RCXT run(s), and provide directories defined by STAR_DIRECTORY command in the Star RCXT command file using **set_starrcxt_options**.

WHAT NEXT

signoff_opt invokes **PrimeTime** timing engine to perform static timing analysis. The default setting used by **signoff_opt** to run **PrimeTime** does not support running AOCVM or VX. Therefore, if you would like to see AOCVM or VX effects in **signoff_opt**, you must run your own **PrimeTime** runs with proper setup, and provide the saved session(s) to **IC Compiler** using **set_primetime_options**. Alternatively, you can provide a TCL script which defines the environment to **set_primetime_options**, using either **-common_file** or **-specific_file** switch.

Note when you run your own **PrimeTime**, you need to ensure:

- Saved session(s) contain same netlist comparing to IC Compiler
- Saved session(s) contain same timing exceptions and clock definitions

• Saved session(s) contain libraries that are also used in IC Compiler

SEE_ALSO

signoff_opt(2),
set_primetime_options(2),
set_starrcxt_options(2)

PSYN-350 (information) '%s'.

DESCRIPTION

You receive this information message because the spacing specified to well-tie placement is invalid. The spacing must be greater than both the site spacing and the cell height. The tool changes the spacing internally to greater of the two values.

WHAT NEXT

This an informational message only. No action is required on your part.

However, consider the new spacing indicated in the message when invoking well-tie placement in the future.

PSYN-351 (information) '%s'.

DESCRIPTION

You receive this information message when a full row is skipped during well-tie cell placement, because the height of the cell is more than the available space in the row.

This occurs when the area specified in the **insert_filler** command does not align fully with the rows. If the specified area causes the top and the bottom rows to be partially covered, then this message is shown.

WHAT NEXT

This is an informational message only. No action is required on your part.

However, you can avoid the message by adjusting the area specified in the **insert_filler** command.

SEE ALSO

insert_filler (2).

PSYN-352 (information) %s.

DESCRIPTION

You receive this information message when a well-tie cell cannot be placed at the specified location due to a blockage. The message indicates the type of blockage preventing the placement of the well-tie cell.

WHAT NEXT

This is an informational message only. No action is required on your part.

However, if you want to place a well-tie cell at that location, you can remove the blockage. If you want to place a well-tie cell over the blockage, specify the **-ignore_keepouts** option with the **insert_filler** command.

SEE ALSO

insert_filler (2).

PSYN-353 (information) Wiring obstruction (%f %f %f %f) at bottom layer is being treated as placement obstruction

DESCRIPTION

You receive this information message when the wiring obstruction or keepout in the lowest metal layer is treated as a placement obstruction. This is a default feature of the tool. You can disable this feature using the following variable:
psyn_enable_auto_keepout_generation

WHAT NEXT

This is an informational message only. No action is required on your part.

Refer to the **create_wiring_keepout** man page for a description of how lowest layer wiring keepouts are automatically converted to placement keepouts.

If there are too many wiring keepouts in the lowest metal layer and the legalizer process is having problems, you can turn off this feature by setting the following variable to FALSE:
physopt_enable_auto_keepout_generation

You can also control the threshold for automatic conversion of lowest layer wiring keepouts into placement keepouts by using the following variable.
physopt_auto_placement_keepout_threshold_value

SEE ALSO

create_wiring_keepout (2); **physopt_auto_placement_keepout_threshold_value** (3), **physopt_enable_auto_keepout_generation** (3).

PSYN-354 (information) '%s'.

DESCRIPTION

You receive this information message because the wiring obstruction or keepout in the lowest metal layer is being treated as a placement obstruction. This is a default feature of the tool. You can disable this feature using the following variable:
psyn_enable_auto_keepout_generation

WHAT NEXT

This is an informational message only. No action is required on your part.

PSYN-355 (information) '%s'.

DESCRIPTION

You receive this information message because the wiring obstruction or keepout in the lowest metal layer is being treated as a placement obstruction. This is a default feature of the tool. You can disable this feature using the following variable:
psyn_enable_auto_keepout_generation

WHAT NEXT

This is an informational message only. No action is required on your part.

PSYN-356 (error) '%s'.

DESCRIPTION

You receive this error message because the coordinates specified lie outside the core area and the command cannot proceed to execute.

WHAT NEXT

For the commands related to well-tie or filler cells placement, check that the coordinates lie inside the core area.

For all other commands, check the core area coordinates and the coordinates specified to the command.

After making your corrections, run the command again.

PSYN-357 (information) %s.

DESCRIPTION

The tool issues this information message to advise you of the total number of well-tie or filler cells added, or removed, or reported by the previous command.

WHAT NEXT

This is an informational message only. No action is required on your part.

PSYN-358 (error) '%s'.

DESCRIPTION

You receive this error message because negative spacing information has no meaning during well-tie placement.

WHAT NEXT

Provide valid positive spacing and run the command again.

PSYN-359 (error) %s.

DESCRIPTION

You receive this error message because you cannot specify the **-density** option along with the **-complete** or **-none** option in the **set_pnet_options** command.

WHAT NEXT

Use the **-density** and the **-partial** options for density control of cells under power

nets.

Refer to the **set_pnet_options** man page for detailed information about the options to use.

SEE ALSO

set_pnet_options (2).

PSYN-360 (warning) Macro placement timed out. Some macros may be illegally placed.

DESCRIPTION

You receive this warning because macro placement timed out. By default, macro placement fails early if runtime is too long when compared to the rest of coarse placement. This occurs to prevent excessively long runtimes. Although you receive this warning, coarse placement runs to completion; however, some macros, (particularly smaller ones) may be illegally placed.

WHAT NEXT

No action is required on your part.

However, you can avoid receiving this warning by setting the **placer_disable_macro_placement_timeout** variable to **true**. Alternatively, you can try reducing the number of floating macros in the design.

SEE_ALSO

set_mpc_macro_options(2)
set_mpc_options(2)
placer_disable_macro_placement_timeout(3)

PSYN-361 (information) %s

DESCRIPTION

You receive this information because a movebound is completely covered by a blockage. When this occurs, the placer ignores the bound.

WHAT NEXT

This is an informational message only. No action is required on your part.

Although it is not required, it is good practice to avoid this situation by reviewing the movebounds to ensure that they do not conflict with the blockages.

SEE_ALSO

create_bounds(2)

PSYN-362 (warning) Placer unable to satisfy constraints on macro cell %s.

DESCRIPTION

You receive this warning because the placer was unable to satisfy one or more constraints on the specified macro cell. The macro may be overlapping another macro, or it may be violating a user-specified constraint such as a movebound, macro array, or spatial constraint. This is usually due to a high density of macros or constraints that are difficult or impossible to satisfy.

WHAT NEXT

No action is required on your part if your floorplan is usable despite the violated constraint.

However, you can avoid receiving this warning by following the guidelines described below:

•If the problem is minor, then you can either modify your constraints and rerun placement or edit the floorplan by hand.

•If the problem is more severe, then increase the size of your core area or reduce the number of constraints.

SEE_ALSO

set_mpc_macro_options(2)
set_mpc_options(2)

PSYN-363 (error) The placer detected conflicting constraints on the following cells:

%s

DESCRIPTION

You receive this message because, by default, the placer errors out if it detects conflicting constraints on one or more cells. These constraints can be movebounds, array constraints, or simple (non-disjunctive) spatial constraints that are impossible to meet. This can occur due to cells being fixed, the requirement for cells to fit on the chip, or constraints directly conflicting with each other.

WHAT NEXT

If you want the placer to run to completion despite conflicting constraints, set the **physopt_error_out_on_conflicting_macro_constraints** variable to **false**. Otherwise, remove or change the conflicting constraints and rerun the placer.

SEE_ALSO

set_mpc_macro_options(2)
set_mpc_options(2)
physopt_error_out_on_conflicting_macro_constraints(3)

PSYN-364 (warning) The placer detected conflicting constraints on the following cells:
%s

DESCRIPTION

You receive this warning because the placer detected conflicting constraints on one or more cells. These constraints can be movebounds, array constraints, simple (non-disjunctive) spatial constraints that are impossible to meet. This can occur due to cells being fixed, the requirement for cells to fit on the chip, or constraints directly conflicting with each other.

WHAT NEXT

No action is required on your part.

However, you can avoid receiving this warning, if you are satisfied with your macro placement, by removing or changing the conflicting constraints and rerunning the placer. If you want the placer to error out when it detects conflicting constraints, set the **physopt_error_out_on_conflicting_macro_constraints** variable to **true**.

SEE_ALSO

set_mpc_macro_options(2)
set_mpc_options(2)
physopt_error_out_on_conflicting_macro_constraints(3)

PSYN-365 (warning) The following bounds conflict:%s Treating groupbounds as soft constraints.

DESCRIPTION

You receive this message because the placer detected conflicting movebounds and groupbounds on two or more cells. The placer will still honor the movebounds but it will treat all conflicting groupbounds as soft constraints. This means that the placer will attempt to honor the groupbounds, but they will be given the same priority as wirelength.

A conflict is defined as a physical impossibility. For example, suppose cell A is in a movebound with coordinates ((0 0)(10 10)), cell B is in a movebound with coordinates ((1000 1000)(1010 1010)) and cells A and B are both in a groupbound with dimension (20 20). There is no way for all three of those bounds to be satisfied. Alternatively, if cell B were fixed at location (1000 1000) we would have a similar problem. This kind of situation causes the placer to perform poorly, so the tool will weaken the groupbounds.

WHAT NEXT

No action is required on your part.

However, you can avoid receiving this warning by reviewing your movebounds and groupbounds and removing all conflicts. If you want the placer to error out when it detects conflicting bounds, set **placer_dont_error_out_on_conflicting_bounds** to **false**.

SEE_ALSO

create_bounds(2)
create_placement(2)
place_opt(2)
placer_dont_error_out_on_conflicting_bounds(3)

PSYN-366 (error) The following bounds conflict:%s

DESCRIPTION

You receive this message because, by default, the placer errors out if it detects

conflicting movebounds and groupbounds on two or more cells. These bounds can be user-specified bounds or bounds generated by the tool (designated as "auto_bound").

A conflict is defined as a physical impossibility. For example, suppose cell A is in a movebound with coordinates ((0 0)(10 10)), cell B is in a movebound with coordinates ((1000 1000)(1010 1010)) and cells A and B are both in a groupbound with dimension (20 20). There is no way for all three of those bounds to be satisfied. Alternatively, if cell B were fixed at location (1000 1000) we would have a similar problem. This kind of situation causes the placer to perform poorly, so the tool will error out.

WHAT NEXT

You should review your movebounds and groupbounds and remove all conflicts. Alternatively, you can set the variable **placer_dont_error_out_on_conflicting_bounds** to **true**. This will cause the tool to automatically weaken the conflicting groupbounds and continue. If one or more of the conflicting bounds were generated by the tool ("auto_bound") then you can either remove the bounds that you have set or use the variable described above.

SEE_ALSO

create_bounds(2)
create_placement(2)
place_opt(2)
placer_dont_error_out_on_conflicting_bounds(3)

PSYN-367 (warning) Placer detected excessive or conflicting groupbounds. All groupbounds will be treated as extra-soft bounds for this placement.

DESCRIPTION

You receive this warning because you have too many groupbounds in your design, or you have conflicting bounds. These may be bounds you have set yourself with create_bounds or bounds that have been generated by the tool.

The placer will still attempt to honor your groupbounds, but it will give them the same priority as wirelength.

The placer does not allow the number of groupbounds to exceed 5% of the number of nets in the design. This is because the placer performs poorly when it is overconstrained.

Additionally, if the placer detects any conflicts then it will convert all groupbounds containing less than two cells to extra-soft bounds. A conflict is defined as a physical impossibility, such as two cells confined to opposite corners by movebounds but being pulled close together by a groupbound. This is because the placer performs poorly when it is given conflicting constraints.

WHAT NEXT

No action is required on your part.

However, you can avoid receiving this warning by reducing the number of groupbounds you generate with create_bounds.

SEE_ALSO

create_bounds(2)
create_placement(2)
physopt(2)

PSYN-368 (warning) -quick option not supported in current flow. Running low effort placer instead.

DESCRIPTION

You receive this warning because you have specified the -quick option to create_placement or physopt and you are running a flow (such as region placement) that interacts poorly with the -quick option.

Because quick mode is not compatible with your flow, the placer will automatically run in low effort mode instead of quick mode. This is equivalent to using the -effort low option instead of -quick.

WHAT NEXT

No action is required on your part.

SEE_ALSO

physopt(2)
create_placement(2)

PSYN-369 (error) The following fixed cells have no location:

DESCRIPTION

You receive this error message because one or more fixed cells in your design do not have their locations specified.

All fixed cells must have locations specified before running placement.

WHAT NEXT

Either remove the fixed_placement attribute or specify a location for the listed cells.

SEE ALSO

create_placement (2), **place_opt** (2),

PSYN-370 (warning) Site %s has different height(width) in the pdbs
%s and %s . Site defined in %s will be used.

DESCRIPTION

You receive this warning message because there is conflicting site information in the .pdb files you specified in the **set physical_library** command. This warning occurs if two .pdb files have a site with the same name, but different heights or widths. The tools uses the site definition from the first .pdb file in which the site is defined.

Example Message

```
Warning: Site core1 has different height (width) in the pdbs SIARC_WIDE1
         and SIARC_WIDE2. Site defined in SIARC_WIDE2 will be used.
         (PSYN-370)
```

WHAT NEXT

This is a warning message only. No action is required on your part.

However, you can check that the physical libraries have the correct site definitions. To avoid future problems, ensure that no two .pdb files have conflicting site information (the same name, but different heights or widths).

SEE ALSO

physical_library (3).

PSYN-371 (warning) %s.

DESCRIPTION

This warning message indicates that density value is specified wrongly.

WHAT NEXT

Specify a density value ranging between 0 and 1.

PSYN-372 (warning) Net '%s' is connecting to a spare cell '%s'.

DESCRIPTION

You receive this warning because a cell identified as a spare cell is connected to a net. The tool considers all cells which are not on a path from an input port to an output port as spare cells.

WHAT NEXT

No action is required on your part.

However, it is recommended that you review your netlist for accuracy.

SEE_ALSO

insert_spare_cells(2)
all_spare_cells(2)

PSYN-373 (warning) Possible syntax error found in SDC file.

DESCRIPTION

You receive this warning message because **IC Compiler** found your SDC file contains possible syntax errors. The errors found are displayed after this message.

WHAT NEXT

In **signoff_opt** or **run_signoff**, only **PrimeTime** will read this SDC file. Thus, if you believe **PrimeTime** is able to read this SDC file successfully, you can ignore this message.

SEE ALSO

signoff_opt (2) **run_signoff** (2) **set_primetime_options** (2) **report_primetime_options** (2)

PSYN-374 (information) Using auto-derived max script %s and

min script %s.

DESCRIPTION

You receive this message because **signoff_opt** automatically runs two **PrimeTime** with two timing corners that might need different timing derate settings.

signoff_opt invokes **PrimeTime** timing engine to perform static timing analysis. However, **IC Compiler** supports timing derating with both min/max and early/late, for best-case-worst-case analysis, but SDC syntax only allows early/late. Therefore, if you have both min/max and early/late derate settings in your database, and you didn't provide a signoff SDC file, ICC's sdc output will not be sufficient to run **PrimeTime**. Thus, two auto-derived script files are used in addition to the SDC file, which contain proper derate setting for min and max corner of **PrimeTime**.

WHAT NEXT

If needed, please examine the auto-derived script files specified.

SEE ALSO

signoff_opt (2),
run_signoff (2),
set_timing_derate(2)

PSYN-375 (severe) Fatal error: Placer did not complete.

DESCRIPTION

You receive this warning because the coarse placer did not complete successfully. You should also receive a more specific error message telling you why the placement failed.

WHAT NEXT

You should fix the problem with your setup and rerun the command.

SEE_ALSO

create_placement(2)
refine_placement(2)
place_opt(2)

PSYN-376 (information) %d inactive secnario(s) will not be

analyzed/optimized.

DESCRIPTION

You receive this message because **signoff_opt** finds that you have some inactive scenarios in your database. Only active scenarios will be analyzed and optimized by **signoff_opt**.

WHAT NEXT

Use **set_active_scenarios** to change the set of active scenarios.

SEE ALSO

signoff_opt (2),
run_signoff (2),
all_scenarios(2),
all_active_scenarios(2),
set_active_scenarios(2)

PSYN-377 (error) Cannot use -skip_initial_analysis without previous signoff analysis.

DESCRIPTION

You receive this error because you are trying to run **signoff_opt** with **-skip_initial_analysis** on a design that has not been run with signoff analysis first.

You can run **run_signoff** first before you run **signoff_opt** with **-skip_initial_analysis**.

WHAT NEXT

Use **run_signoff** command to perform initial signoff analysis first.

SEE_ALSO

signoff_opt(2),
run_signoff(2)

PSYN-378 (information) %d %s process(es) will be run on local

host.

DESCRIPTION

This message tells you how many processes will be run on your local host, where you invoke **icc_shell**.

WHAT NEXT

Use **add_distributed_hosts** to change the number of remote hosts.

SEE ALSO

signoff_opt (2),
run_signoff (2),
add_distributed_hosts(2)

PSYN-379 (Information) Updated utilization of voltage area %s is %f.

DESCRIPTION

WHAT_NEXT

PSYN-380 (error) Leakage constraint is not set, but -power_recovery or -only_power_recovery flag has been used.

DESCRIPTION

You receive this message because you tried to perform power optimization without setting a required leakage constraint.

WHAT NEXT

Change the script to include a leakage constraint, using the **set_max_leakage_power** command.

You must set as true the value of the **physopt_enable_power_optimization** variable before the tool can perform power recovery.

SEE ALSO

physopt(2)
report_power(2)
set_max_leakage_power(2)
physopt_enable_power_optimization(3)

PSYN-381 (warning) There are design rule checking (DRC) violations in constant nets due to hierarchy.

DESCRIPTION

This warning occurs because in your design you defined a hierarchy pin that is driven by a constant net. This situation limits the corrections the tool can make to DRC violations on the net connected to the hierarchical pin. The tool always preserves the design hierarchy and does not add buffers or inverters to correct DRC violations on constant nets.

WHAT NEXT

Change the interface of the module, and push constants to the lower hierarchy. You can make these changes by using the **set_boundary_optimization** command or by changing the netlist so that no hierarchical pins are driven by constant nets.

SEE ALSO

set_auto_disable_drc_nets(2)
set_boundary_optimization(2)

PSYN-382 (warning) The pin %s is driven by constant %d cell from the voltage_area %s to the voltage area %s.

DESCRIPTION

This warning message occurs when the design has a constant net that crosses the voltage area boundary. When the voltage areas are bound to the power supply, crossing the voltage area may cause some issues. It is considered best practice to ensure that constant nets are within the voltage area boundary.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Change the interface of the module and push the constants to the lower hierarchy.

SEE ALSO

create_voltage_area(2)
set_auto_disable_drc_nets(2)

PSYN-383 (Warning) Target library does not have any constant lib_cells. Therefore tool cannot replace virtual constants.

DESCRIPTION

This warning message occurs when target library does not have any constant lib_cells.

WHAT NEXT

Add a library with constant lib_cells to Target_library.

PSYN-384 (error) Incremental StarRCXT directory cannot be used as image.

DESCRIPTION

You receive this error because you are trying to specify a StarRCXT image, using a StarRCXT run directory which has been run with incremental extraction.

When you specify a StarRCXT image using **set_starrcxt_options** command, you must use a StarRCXT run directory that does not run with incremental extraction.

WHAT NEXT

Re-run non-incremental StarRCXT extraction, and use the new run directory as the image.

SEE_ALSO

signoff_opt(2),
set_starrcxt_options(2)

PSYN-385 (warning) Incremental signoff analysis is disabled.

DESCRIPTION

You receive this warning message because incremental signoff analysis is disabled in **signoff_opt**, which could significantly increase your runtime.

By default, **signoff_opt** invokes **StarRCXT** and **PrimeTime** in incremental mode whenever is possible. However, user can overwrite this hehavior by using **-full_extract** and/or **-full_analysis**. Always using full StarRCXT extraction and full PrimeTime analysis could lead to significant increase in runtime.

WHAT NEXT

You can ignore this warning message if you indeed want to turn off incremental signoff analysis.

SEE ALSO

signoff_opt (2)

PSYN-386 (warning) The variable %s is obsolete. The correct name is %s.

DESCRIPTION

You receive this warning because you are using an obsolete variable. Your setting is still valid in this release, but it will be ignored in future releases.

WHAT NEXT

You should update your scripts to use the correct variable name.

PSYN-387 (error) Found unsupported syntax in common file %s.

DESCRIPTION

You receive this error because you are trying to specify a TCL file to **set_primetime_options -common_file**, which contains unsupported syntax.

In this TCL file, you can only change TCL variables.

In addition, only a subset of PrimeTime TCL variables are allowed.

- all rc variables
- all case analysis variables
- all ccs variables
- all pba variables
- all report variables
- all sdc variables
- all timing variables except timing_save_pin_arrival_and_slack
- all si variables except si_enable_analysis
- all parasitics variables except read_parasitics_load_locations
- all variation variables except variation_enable_analysis and variation_derived_scalar_attribute_mode

Variables starting with "myvar_" are also allowed.

Exceptions:

- **timing_save_pin_arrival_and_slack** is always set to **true** by **IC Compiler**
- **si_enable_analysis** is derived from **set_si_options** command in **IC Compiler**
- **read_parasitics_load_locations** is always set to **true** by **IC Compiler**
- **variation_enable_analysis** is drived from **-variation** switch
- **variation_derived_scalar_attribute_mode** is always set to **quantile** when **-variation** is used

Example:

```
set timing_remove_clock_reconvergence_pessimism true
```

WHAT NEXT

Remove contents in the file other than setting tcl variables.

SEE_ALSO

set_primetime_options(2)

PSYN-388 (error) Found unsupported syntax in specific file %s.

DESCRIPTION

You receive this error because you are trying to specify a TCL file to **set_primetime_options -specific_file**, which contains unsupported syntax.

In this TCL file, you can change TCL variables using the same rule defined in the man page for PSYN-387.

In addition, you can also use the following TCL commands:

- all report commands
- all check commands
- all update commands
- all set commands except set_program_options, set_units and set_unix_variable
- all reset commands except reset_design
- group_path
- scale_parasitics and complete_net_parasitics
- read_aocvm and remove_aocvm
- create_correlation, create_operating_conditions and create_variation
- define_design_mode_group and define_scaling_lib_group

Note TCL procedures and flow control (if, while, etc.) are not supported.

WHAT NEXT

Remove contents in the file other than the allowed commands.

SEE_ALSO

set_primetime_options(2)
PSYN-387(n)

PSYN-389 (error) %s %s is not allowed at line %d in PT TCL file.

DESCRIPTION

You receive this error because you are trying to specify a TCL file to

set_primetime_options -specific_file or, to **set_primetime_options -common_file**, which contains unsupported syntax.

Check PSYN-387 and/or PSYN-388 for allowed syntax.

WHAT NEXT

Remove contents in the file other than the allowed commands.

SEE_ALSO

set_primetime_options(2)
PSYN-387(n)
PSYN-388(n)

PSYN-390 (warning) Switch '%s' only has effect in multi scenario.

DESCRIPTION

You receive this warning because you are using a switch that is only supported in multi scenario. The switch will be ignored in non-multi scenario.

WHAT NEXT

You can ignore this message if you will define scenarios later.

SEE_ALSO

set_primetime_options(2)
set_starrcxt_options(2)
signoff_opt(2)

PSYN-391 (information) The recommended %s version is %c-%g.

DESCRIPTION

IC Compiler uses this information message to tell you what is the recommended **StarRCXT** or **PrimeTime** version to use with **signoff_opt** or **run_signoff**.

WHAT NEXT

This is an informational message only.

SEE ALSO

set_primetime_options(2)
report_primetime_options(2)
set_starrcxt_options(2)
report_starrcxt_options(2)
signoff_opt(2)
run_signoff(2)

PSYN-392 (information) %s version is %s.

DESCRIPTION

IC Compiler uses this information message to tell you what is the **StarRCXT** or **PrimeTime** version you specified.

WHAT NEXT

This is an informational message only.

SEE ALSO

set_primetime_options(2)
report_primetime_options(2)
set_starrcxt_options(2)
report_starrcxt_options(2)
signoff_opt(2)
run_signoff(2)

PSYN-393 (information) Ignore cover macro %s in the logical netlist.

DESCRIPTION

The cover macro cell’s name exists as a name of logical cell in a netlist. The logical cell is deleted to avoid conflict, since cover cell cannot be a logical cell.

WHAT_NEXT

Check if it is alright that the logical cell with the name mentioned is removed from logical netlist. If it is not alright, please change the name of the logical cell or the cover cell.

PSYN-394 (warning) Layer %s used in the physical library %s is not defined %s %s.

DESCRIPTION

This warning occurs because you are linking in technology physical library database (.pdb) files and macro .pdb files. Technology .pdb files describe the process layers and macro .pdb files describe the standard cells and RAMs that you want to use.

This warning occurs if all of the conditions in the following example are met. Given a technology .pdb file that has *n* layers and macro .pdb files that have *m1,m2*... layers, and the macro .pdb file layers (*m1,m2*...) are greater than the technology .pdb file layers (*n*).

The extra layers in the macro .pdb files are used to describe routing obstructions. These layers do not form any functional part of the cells, so all the geometry specifications on them are ignored, but the tool uses them for RC calculations. The library vendor creates cells with extra layers so that a single cell definition can be used by multiple process libraries without duplicating the same cell description.

WHAT NEXT

Ensure that you have specified the correct physical libraries. If the specified libraries are correct, ignore the warning message.

SEE ALSO

physopt (2)
report_timing (2)

PSYN-395 (warning) Enabling path based analysis with too many violating paths will slow down your runtime.

DESCRIPTION

You receive this warning because you are enabling path based analysis in **signoff_opt** or **run_signoff**, while your design still has a lot of violating paths.

Path based analysis will recalculate violating paths to reduce pessimism. Additional runtime is required for this recalculation. If you have too many violating paths, you could experience a significant increase in runtime.

WHAT NEXT

Disable path based analysis to save runtime.

SEE_ALSO

signoff_opt(2)
run_signoff(2)

PSYN-396 (warning) '%s' variable is obsolete. Please use set_physopt_cpulimit_options command instead.

DESCRIPTION

You receive this warning message because you used a variable that is obsolete. Use the **set_physopt_cpulimit_options** command, as described in the **set_physopt_cpulimit_options** man pages.

WHAT NEXT

Remove the obsolete variable, and replace it with the new command.

SEE ALSO

set_physopt_cpulimit_options (2).

PSYN-397 (information) Released license %s.

DESCRIPTION

IC Compiler uses this information message to tell you a license is released. When running **signoff_opt** or **run_signoff**, we release the license while signoff tools begin running. It will be re-acquired from the license server after signoff tools finish running.

WHAT NEXT

This is an informational message only.

SEE ALSO

PSYN-398(n)
PSYN-399(n)

PSYN-398 (information) Re-acquired license %s.

DESCRIPTION

IC Compiler uses this information message to tell you a license is re-acquired from the license server. When running **signoff_opt** or **run_signoff**, we release the license while signoff tools begin running. After signoff tools finish running, we re-acquire it from the license server.

WHAT NEXT

This is an informational message only.

SEE ALSO

PSYN-397(n)
PSYN-399(n)

PSYN-399 (information) Waiting for license %s.

DESCRIPTION

IC Compiler uses this information message to tell you that we're waiting for a license to become available. When running **signoff_opt** or **run_signoff**, we release the license while signoff tools begin running. After signoff tools finish running, we need to re-acquire it from the license server. If the key is not available at this time, **IC Compiler** will wait until the license becomes available again. We will try to acquire the license every 60 seconds.

WHAT NEXT

This is an informational message only.

SEE ALSO

PSYN-397(n)
PSYN-398(n)

PSYN-400 (error) No core area defined for design.

DESCRIPTION

You receive this error because you have not specified the core area for the design before attempting placement.

WHAT NEXT

Specify the core area as part of the design information, or use the -mpc flag to automatically generate a floorplan.

SEE_ALSO

create_placment(2)
physopt(2)

PSYN-401 (error) No location defined for pin %s of library cell %s.

DESCRIPTION

You receive this error because the specified pin does not have a location.

WHAT NEXT

Fix your library data so that all pins have locations.

SEE_ALSO

create_placment(2)
physopt(2)

PSYN-402 (error) No physical cell for logical cell %s.

DESCRIPTION

You receive this error because the there is no physical cell for the specified logical cell.

WHAT NEXT

Fix your library data to include the necessary physical information.

SEE_ALSO

create_placment(2)
physopt(2)

PSYN-403 (error) No height or width defined for physical cell %s.

DESCRIPTION

You receive this error because the there is no height or width information for the specified physical cell.

WHAT NEXT

Fix your library data to include the necessary physical information.

SEE_ALSO

create_placment(2)
physopt(2)

PSYN-404 (error) No height or width defined for placement keepout %s.

DESCRIPTION

You receive this error because there is no height or width information for the specified placement keepout.

WHAT NEXT

Fix your input data to include the necessary physical information.

SEE_ALSO

create_placment(2)
physopt(2)

PSYN-405 (error) No location specified for fixed cell %s.

DESCRIPTION

You receive this error because there is no location information for the specified fixed cell.

WHAT NEXT

Fix your input data to include the necessary physical information.

SEE_ALSO

create_placment(2)
physopt(2)

PSYN-406 (error) No R or C per unit length defined.

DESCRIPTION

You receive this error because there is no resistance or capacitance per unit length defined for this design.

WHAT NEXT

Fix your input data to include the necessary physical information.

SEE_ALSO

create_placment(2)
physopt(2)

PSYN-407 (error) No physical design for logical design.

DESCRIPTION

You receive this error because there is no physical design for the logical design.

WHAT NEXT

Fix your input data to include the necessary physical information.

SEE_ALSO

create_placment(2)
physopt(2)

PSYN-408 (error) Some cells are unplaced before incremental congestion removal.

DESCRIPTION

You receive this error because some cells are unplaced before incremental congestion removal. All cells must have locations before running incremental congestion removal.

WHAT NEXT

Run create_placement or physopt to place all cells.

SEE_ALSO

create_placment(2)
physopt(2)

PSYN-409 (Error) Cannot perform on_route SI on a global routed design.

DESCRIPTION

At global route stage, the coupling capacitance accuracy is not good. So, we don’t do any SI fixing.

WHAT NEXT

PSYN-410 (error) No physical cell pin %s for logical cell %s.

DESCRIPTION

You receive this error because the there is no physical pin defintion for the specified logical cell.

WHAT NEXT

Fix your library data to include the necessary physical information.

SEE_ALSO

create_placment(2)
physopt(2)

PSYN-411 (information) Following commands are now PrimeTime based.

DESCRIPTION

This message gives you a list of commands that are now PrimeTime based. This happens after you run **signoff_opt** or **run_signoff**.

WHAT NEXT

Use **run_signoff -signoff_analysis false** to revert these commands back to IC Compiler based.

SEE ALSO

signoff_opt (2) **run_signoff** (2)

PSYN-412 (information) Following PrimeTime commands are now available.

DESCRIPTION

This message gives you a list of PrimeTime commands that now become available in **IC Compiler**. This happens after you run **signoff_opt** or **run_signoff**.

WHAT NEXT

Running **run_signoff -signoff_analysis false** will disable these commands.

SEE ALSO

signoff_opt (2) **run_signoff** (2)

PSYN-413 (information) Following commands are now IC Compiler based.

DESCRIPTION

This message gives you a list of commands that were PrimeTime based after **signoff_opt** or **run_signoff**, which are now IC Compiler based. This happens after you run **run_signoff -signoff_analysis false**.

WHAT NEXT

Use **signoff_opt** or **run_signoff** to switch them to be PrimeTime based.

SEE ALSO

signoff_opt (2) **run_signoff** (2) **PSYN-411** (n)

PSYN-414 (information) Following PrimeTime commands are now disabled.

DESCRIPTION

This message gives you a list of PrimeTime commands that were available after **signoff_opt** or **run_signoff**, which are now disabled. This happens after you run **run_signoff -signoff_analysis false**.

WHAT NEXT

Use **signoff_opt** or **run_signoff** to make them available again.

SEE ALSO

signoff_opt (2) **run_signoff** (2) **PSYN-412** (n)

PSYN-415 (warning) Circuit has no valid timing end points.

DESCRIPTION

This warning message occurs when you are running timing driven placement without defining the timing constraints.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Check your design timing constraints, make the necessary corrections, and then run the command again.

PSYN-416 (warning) Missing signoff SDC, using ICC SDC instead.

DESCRIPTION

You receive this warning message because you did not specify a signoff SDC file with **set_primetime_options -sdc_file**.

WHAT NEXT

You can ignore this warning message if you indeed want to use the ICC SDC file.

SEE ALSO

signoff_opt (2) **run_signoff** (2) **set_primetime_options** (2)

PSYN-417 (information) Following commands are now disabled.

DESCRIPTION

This message gives you a list of commands that are disabled. This happens after you run **run_signoff**.

WHAT NEXT

Use **run_signoff -signoff_analysis false** to re-enable these commands.

SEE ALSO

signoff_opt (2) **run_signoff** (2)

PSYN-418 (information) Following commands are now re-

enabled.

DESCRIPTION

This message gives you a list of commands that were disabled after **run_signoff**, which are now re-enabled. This happens after you run **run_signoff -signoff_analysis false**.

WHAT NEXT

SEE ALSO

signoff_opt (2) **run_signoff** (2) **PSYN-417** (n)

PSYN-419 (information) No changes were made during optimization.

DESCRIPTION

IC Compiler uses this information message to tell you that there were no changed made during optimization. There were no netlist changes, such as added/deleted/ modified instances, nor routing changes.

Since there were no changes made, **signoff_opt** will stop.

WHAT NEXT

This is an informational message only.

SEE ALSO

signoff_opt (2)

PSYN-420 (Information) Generating dummy physical description for cell %s. Generated physical library cell is having height %f and width %f.

DESCRIPTION

You receive this Information message because one of the physical cells doesn’t have a physical library cell in any of the physical libraries specified. Tool is

generating dummy physical description of this missing physical library cell.

Physical compiler needs physical description of all the logical cells to proceed further and gives PSYN-024 warning for this.

These created ummy physical cells are not persistent in the design DB and are recreated everytime a new physical compiler session is started.

These dummy physical cells are required mainly for the exploration flow and finnally should be replaced by the correct physical description using correct physical libraries.

To turn off this feature, please set "physopt_create_missing_physical_libcells" variable to FALSE.

WHAT NEXT

Check the physical libraries specified. All physical cells in the design should have physical library cells.

SEE ALSO

physopt_create_missing_physical_libcells(3)

PSYN-421 (Error) No sequential or combinational cells in the lib - %s

DESCRIPTION

You receive this error message because tool is not able find any sequential or combinational cells in the specified library. Tool will continue to find a base cell in other target libraries, until it finds a one. Tool is finding these cells, so that it can be used to create dummy physical description of other missing physical libraries cells.

WHAT NEXT

Check the physical libraries specified. All physical cells in the design should have physical library cells. Dummy physical description of missing phlib cell is generated only when physopt_create_missing_physical_libcells variable is set to TRUE. If you do not want to generate dummy physical description, set this variable to FALSE.

PSYN-422 (information) PrimeTime path based analysis is

enabled.

DESCRIPTION

IC Compiler uses this information message to tell you that PrimeTime path based analysis is enabled in **signoff_opt** or **run_signoff**.

Path based analysis is a **PrimeTime** technology which reduces pessimism during static time analysis.

WHAT NEXT

This is an informational message only.

SEE ALSO

signoff_opt (2)
run_signoff (2)

PSYN-423 (information) PrimeTime advanced OCV mode is enabled.

DESCRIPTION

IC Compiler uses this information message to tell you that PrimeTime advanced OCV mode is enabled in **signoff_opt** or **run_signoff**.

Advanced OCV mode (AOCVM) is a **PrimeTime** technology which reduces pessimism during static time analysis.

WHAT NEXT

This is an informational message only.

SEE ALSO

signoff_opt (2)
run_signoff (2)

PSYN-424 (information) Variation aware signoff analysis is

enabled.

DESCRIPTION

IC Compiler uses this information message to tell you that variation aware analysis is enabled in **signoff_opt** or **run_signoff**. **signoff_opt** or **run_signoff** will invoke **PrimeTime-VX** and **StarRC-XT-VX**.

WHAT NEXT

This is an informational message only.

SEE ALSO

signoff_opt (2)
run_signoff (2)

PSYN-425 (information) PrimeTime rail analysis is enabled.

DESCRIPTION

IC Compiler uses this information message to tell you that rail analysis is enabled in **signoff_opt** or **run_signoff**.

Rail based analysis is a **PrimeTime** technology which analyzes the IR drop effects on rail voltages.

WHAT NEXT

This is an informational message only.

SEE ALSO

signoff_opt (2)
run_signoff (2)

PSYN-426 (warning) Cell %s and cell %s violate a spacing rule.

DESCRIPTION

You get this warning because the specified cells violate a user-defined spacing rule.

WHAT_NEXT

Use **legalize_placement** to make the cell placement legal.

SEE ALSO

check_legality (2), **legalize_placement** (2).

PSYN-427 (warning) Placement utilization is %s.

DESCRIPTION

You get this warning because the placement utilization is extremely high. Placement will continue, but you may get poor results or errors later in the flow due to the high utilization.

WHAT_NEXT

No action is required.

SEE ALSO

create_placement (2), **place_opt** (2).

PSYN-428 (error) Must exit signoff mode before running correlation analysis.

DESCRIPTION

You receive this error because you are trying to run **run_signoff -correlation** command on a design that has been run with **run_signoff** or **signoff_opt**. You must run **run_signoff -signoff_analysis false** first before you can run **run_signoff -correlation**.

WHAT NEXT

Run **run_signoff -signoff_analysis false**.

SEE_ALSO

run_signoff(2)

PSYN-429 (error) Image directory %s must be writeable.

DESCRIPTION

You receive this error because you are trying to specify a PrimeTime image whose directory is not writeable.

WHAT NEXT

Change the permission of the directory.

SEE_ALSO

set_primetime_options(2)

PSYN-430 (Warning) The snapshot file is corrupted, can’t be loaded.

DESCRIPTION

This warning message occurs when the snapshot file is corrupted.

SEE ALSO

report_qor_snapshot (2)

PSYN-431 (information) Using high effort path based analysis.

DESCRIPTION

IC Compiler uses this information message to tell you that PrimeTime path based analysis is enabled with high effort in **signoff_opt** or **run_signoff**.

Path based analysis is a **PrimeTime** technology which reduces pessimism during static time analysis.

There are two ways of invoking path based analysis in **PrimeTime**:

- get_recalculated_timing_paths [get_timing_paths ...]
- get_timing_paths -recalculate ...

The first method runs faster because it has less number of paths to re-analyze, but

it might also miss the real critical path.

The second method runs slower (and if you have a lot of near critical timing paths, this method can run much slower), but it will eventually give you the real critical path.

By default, **IC Compiler** uses the first method during **run_signoff** or **signoff_opt**.

If you enable advanced OCV mode (AOCVM) with path based analysis (PBA), we will switch to high effort.

WHAT NEXT

This is an informational message only.

SEE ALSO

signoff_opt (2)
run_signoff (2)
PSYN-422 (n)
PSYN-423 (n)

PSYN-432 (warning) Only the following scenarios will be set active: %s.

DESCRIPTION

You receive this warning message because you try to run **set_active_scenarios** on a design with only a subset of scenarios that were analyzed/optimized by **run_signoff** or **signoff_opt**.

EXAMPLE

If your design contains three scenarios, SC1, SC2, and SC3, and you run **set_active_scenarios {S1 S2}** before you run **run_signoff** or **signoff_opt**, **IC Compiler** will only perform signoff analysis/optimization on S1 and S2. S3 will not be analyzed/optimized by **run_signoff** or **signoff_opt**. You should notice a **PSYN-376** to tell you how many inactive scenarios that will not be analyzed/optimized by **run_signoff** or **signoff_opt**.

If you run **set_active_scenarios -all** on this design, you will receive this warning message to tell you that **IC Compiler** will not activate scenario S3 because it was not analyzed by signoff tools.

You will only receive this warning message after **run_signoff** or **signoff_opt**.

WHAT NEXT

You can ignore this warning message if you are satisfied with the given set of active scenarios.

You can also re-run signoff analysis for all scenarios by:

- run_signoff -signoff_analysis false
- set_active_scenarios -all
- run_signoff

SEE ALSO

signoff_opt (2) **run_signoff** (2) **set_active_scenario** (2) **PSYN-376** (n)

PSYN-433 (Error) None of given scenarios can be set active.

DESCRIPTION

You receive this error message because **IC Compiler** is not able to set active the given scenarios.

EXAMPLE

If your design contains three scenarios, SC1, SC2, and SC3, and you run **set_active_scenarios {S1 S2}** before you run **run_signoff** or **signoff_opt**, **IC Compiler** will only perform signoff analysis/optimization on S1 and S2. S3 will not be analyzed/optimized by **run_signoff** or **signoff_opt**. You should notice a **PSYN-376** to tell you how many inactive scenarios that will not be analyzed/optimized by **run_signoff** or **signoff_opt**.

If you run **set_active_scenarios S3** on this design, you will receive this error message to tell you that **IC Compiler** will not activate scenario S3 because it was not analyzed by signoff tools.

You will only receive this error message after **run_signoff** or **signoff_opt**.

WHAT NEXT

You can also re-run signoff analysis for all scenarios by:

- run_signoff -signoff_analysis false
- set_active_scenarios -all
- run_signoff

SEE ALSO

signoff_opt (2) **run_signoff** (2) **set_active_scenario** (2) **PSYN-376** (n) **PSYN-432** (n)

PSYN-434 (information) Timing constraint changes will not be saved in signoff mode.

DESCRIPTION

IC Compiler uses this information message to tell you that you will not be able to save timing constraint changes after **run_signoff**.

If you change your timing constraints after **run_signoff**, such as **set_timing_derate**, these changes will not be saved in your database, and will be lost after you exit signoff mode.

WHAT NEXT

Use **run_signoff -signoff_analysis false** to exit signoff mode, and then re-apply the timing constraint changes.

SEE ALSO

run_signoff (2)

PSYN-435 (information) Signoff timing constraints will not be updated in signoff mode.

DESCRIPTION

IC Compiler uses this information message to tell you that you will not be able to update signoff timing constraints after **run_signoff** or **signoff_opt**.

If you change your signoff timing constraints after **run_signoff** or **signoff_opt**, such as calling **set_timing_derate**, you will not see the effort in timing reports.

WHAT NEXT

Use **run_signoff -signoff_analysis false** to exit signoff mode.

SEE ALSO

run_signoff (2)
signoff_opt (2)

PSYN-436 (warning) Scenario '%s' will be analyzed with On-Chip-Variation.

DESCRIPTION

IC Compiler uses this warning message to tell you that the given scenario will be analyzed with On-Chip-Variation in PrimeTime.

Each active scenario in IC Compiler will be analyzed by PrimeTime DMSA. PrimeTime uses On-Chip-Variation as its default analysis mode. Therefore, if you specify an operating condition other than On-Chip-Variation (such as BC_WC) for a scenario, you will receive this warning message. You could notice additional pessimism during static timing analysis for this scenario.

WHAT NEXT

You can ignore this warning if you're satisfied with On-Chip-Variation analysis.

For BC_WC analysis, you could split the original scenario into two scenarios, one for BC corner (with OCV), and another for WC corner (with OCV).

SEE ALSO

signoff_opt (2) **run_signoff** (2) **set_operating_conditions** (2)

PSYN-437 (Error) Inconsistent NUM_PARTS found in StarRCXT command file.

DESCRIPTION

You receive this error message because **IC Compiler** found that your **StarRCXT** NUM_PARTS settings are not consistent across differet corners.

NUM_PARTS is a reserved keyword in **StarRCXT** command file to enable distributed processing capability. It is an integer number that defines how many partitions

StarRCXT will create and run in parallel.

When **IC Compiler** invokes **StarRCXT**, we require that this setting is consistent among all extraction corners. If you have defined different NUM_PARTS for different extraction corners, you will receive this error message.

There are three places you can define NUM_PARTS:

- set_starrcxt_options -num_parts
- set_starrcxt_options -option_file
- set_starrcxt_options -max_image or -min_image

The first method directly use the command line switch **-num_parts** of **set_starrcxt_options** to define the number of partitions.

The second method specify an option file for **StarRCXT** which could also include a line that defines NUM_PARTS.

The third method specify a **StarRCXT** run directory, which contains a copy of the original command file that could also include a line that defines NUM_PARTS.

All the values specified using above methods need to be consistent.

WHAT NEXT

Examine your settings of NUM_PARTS, and make them consistent.

SEE ALSO

set_starrcxt_options (2) **signoff_opt** (2) **run_signoff** (2)

PSYN-438 (information) Min delta delay is enabled with delta delay.

DESCRIPTION

IC Compiler uses this information message to tell you that min delta delay is enabled in signoff mode because you have enabled delta delay.

WHAT NEXT

You can avoid this message by using **set_si_options -min_delta_delay true**.

SEE ALSO

set_si_options (2)

PSYN-439 (information) UPF is enabled for signoff analysis.

DESCRIPTION

IC Compiler uses this information message to tell you that UPF is enabled in signoff mode.

WHAT NEXT

This is only an information message.

SEE ALSO

load_upf (2)
save_upf (2)

PSYN-440 (Error) Incrorrect cell type.

DESCRIPTION

You receive this error message because you have specified a wrong cell_type attribute to the given library reference cell. set_cell_type command only accepts following cell_types, "BLOCK", "COVER", "RING", "PAD" and "CORE". First three cell_types are used to mark any cell as macro cell. If you want to put any cell as a normal cell, you can mark this cell as "CORE" type.

WHAT NEXT

Please check -cell_type argument to set_cell_type command and give correct type as per your requirement. To mark any cell as Macro cell, please use "BLOCK", "COVER" or "RING" type. To remove macro cell attribute from any cell, please use "CORE" or "PAD" type.

SEE ALSO

all_macro_cells (2), **set_cell_type** (2).

PSYN-441 (warning) PrimeTime image for '%s' does not enable

eco.

DESCRIPTION

This warning message occurs because at least one of the specified **PrimeTimage** image from **save_session** does not enable eco. You must enable eco in PrimeTime to allow **signoff_opt** to perform additional signoff analysis after optimization and incremental place and route.

WHAT NEXT

Provide a new **PrimeTime** image with eco enabled. You need to call **set_program_options -enable_eco** in PrimeTime first, and source the rest of your regular PrimeTime script, before generating the saved session for **signoff_opt**.

SEE ALSO

signoff_opt(2)
set_primetime_options(2)

PSYN-442 (Warning) lib cell "%s" of size (%d sites x %d rows) will be treated as macro cell because it is larger than 6 site heights (default threshold).

DESCRIPTION

You receive this warning message because the lib cell is defined as core cell type in the physical library but its size is large enough (cell height is more than "physopt_macro_cell_height_threshold" row height) so that it is treated as macro cell in placement legalization. There are two cases the cell can be treated as macro cell in legalization and check legality:

CASE 1. the "cell type" is set as BLOCK or RING or COVER in the phsyical lib, or
CASE 2. the cell height is larger then "physopt_macro_cell_height_threshold".

The default value of "physopt_macro_cell_height_threshold" is 6, i.e. a cell can be treated as macro cell if its height is larger then 6 core site rows (even its "cell type" is CORE in the physical library).

WHAT NEXT

Please check the physical lib and modify the cell type in the cell definition.

User can adjust the "physopt_macro_cell_height_threshold" to prevent a std cell be treated as macro cell. For example, if user has a design which contains some 10x site height standard cells. By default, ICC detail placement will treat these 10x

site height cells as "hard macros". If the user still wants these 10x site height cells be placed as "standard cells", then the user can set hidden variable "physopt_macro_cell_height_threshold" to a value which is more than 10, for example, 18:

```
set physopt_macro_cell_height_threshold 18
```

Then, these 10x site height cells will be placed as "standard cells". However, such a practice is not recommended, because the detail placement enginre is not designed for such a design style. Please use it with caution.

SEE ALSO

set_cell_type (2). **all_macro_cells** (2),

PSYN-443 (information) signoff_opt stopped due to %s in PrimeTime image.

DESCRIPTION

IC Compiler uses this information message to tell you that **signoff_opt** is not able to perform additional signoff analysis after optimization and incremental place and route, due to the fact that some of the given PrimeTime images are either missing parasitics, or having eco disabled.

WHAT NEXT

You can save the CEL, and proceed to run your own signoff analysis manually. Or, if you would like to see **signoff_opt** to perform additional signoff analysis after optimization and incremental place and route, please provide corrected PrimeTime images.

SEE ALSO

signoff_opt(2)
set_primetime_options(2)
PSYN-169(n)
PSYN-441(n)

PSYN-444 (warning) Fill metals exist in CEL view.

DESCRIPTION

This warning message occurs because your database contains fill metals in your CEL view. This could interfere with eco router.

WHAT NEXT

Remove the fill metals before running signoff_opt. Or use FILL view instead of CEL view for fill metals.

SEE ALSO

signoff_opt(2)
insert_metal_filler(2)

PSYN-445 (warning) Option '%s' is ignored in signoff mode.

DESCRIPTION

This warning message occurs because you specified an option that is not supported in signoff mode. The specified option is ignored.

WHAT NEXT

You can ignore this warning message if the specified option can be safely ignored.

SEE ALSO

signoff_opt(2)
run_signoff(2)

PSYN-446 (error) Cannot change signoff mode to %s because %s.

DESCRIPTION

You receive this error because you are trying to change signoff mode by running **run_signoff -signoff_analysis true|false|sleep|wakeup** command on a design that has not been run with proper command before.

For example, you cannot change signoff mode to wakeup if it is not in sleep mode. You cannot change signoff mode to sleep if it is already in sleep mode too.

WHAT NEXT

Check the user manual of **run_signoff** or **signoff_opt** to determine what is the command you need to run.

SEE_ALSO

signoff_opt(2),
run_signoff(2)

PSYN-447 (error) Option %s is not allowed at line %d in StarRCXT option file.

DESCRIPTION

You receive this error because you are trying to specify a StarRCXT option file to **set_starrcxt_options -option_file**, which contains unsupported syntax.

Check PSYN-171 for allowed syntax.

WHAT NEXT

Remove contents in the file other than the allowed options.

SEE_ALSO

set_starrcxt_options(2)
PSYN-171(n)

PSYN-448 (warning) Skipping ’%s" because it requires ’%s’.

DESCRIPTION

This warning message occurs because a requested PrimeTime feature is skipped for the given reason.

WHAT NEXT

Please fix reported problem to re-enable this feature.

SEE ALSO

signoff_opt(2)
run_signoff(2)

PSYN-449 (warning) Soft macro '%s' is not expanded.

DESCRIPTION

This warning message occurs because PrimeTime is not able to expand the named soft macro.

WHAT NEXT

Please check path and permission of CEL view of the named soft macro.

SEE ALSO

signoff_opt(2)
run_signoff(2)

PSYN-450 (error) %s.

DESCRIPTION

You get this error because the placement utilization is extremely high. The utilization reported here may be different than the utilization reported in other parts of the tool due to placer constraints such as soft placement blockages.

WHAT_NEXT

You should modify your placement constraints to bring the utilization down to less than 100%.

SEE ALSO

create_placement (2), **place_opt** (2). **create_placement_blockage** (2).

PSYN-451 (information) A process scaling factor '%g' is used for all extraction corners.

DESCRIPTION

IC Compiler uses this information message to tell you that a processing scaling factor is used for all extraction corners.

WHAT NEXT

This is only an information message.

SEE ALSO

run_signoff (2)
signoff_opt (2)

PSYN-452 (information) Optimizing leakage power with %d voltage thresholds.

DESCRIPTION

IC Compiler uses this information message to tell you that **signoff_opt** is currently optimizing leakage power with multiple voltage thresholds library cells.

WHAT NEXT

This is only an information message.

SEE ALSO

signoff_opt (2)

PSYN-453 (warning) Leakage power optimization is skipped since only %d voltage threshold is found.

DESCRIPTION

You receive this warning message because you are trying to perform leakage power optimization without enough voltage threshold.

WHAT NEXT

You need to provide libraries which contain multiple voltage thresholds in order to perform leakage power optimization in **signoff_opt**.

SEE_ALSO

signoff_opt (2)

PSYN-454 (Error) Inconsistent MAGNIFICATION_FACTOR found in StarRCXT command file.

DESCRIPTION

You receive this error message because **IC Compiler** found that your **StarRCXT** MAGNIFICATION_FACTOR settings are not consistent across differet corners.

MAGNIFICATION_FACTOR is a reserved keyword in **StarRCXT** command file to enable processing scaling. It is an float number that defines the processing scaling factor.

When **IC Compiler** invokes **StarRCXT**, we require that this setting is consistent among all extraction corners. If you have defined different MAGNIFICATION_FACTOR for different extraction corners, you will receive this error message.

There are three places you can define MAGNIFICATION_FACTOR:

- set_extraction_options -max_process_scale
- set_starrcxt_options -option_file
- set_starrcxt_options -max_image or -min_image

The first method derives MAGNIFICATION_FACTOR from ICC extraction options.

The second method specify an option file for **StarRCXT** which could also include a line that defines MAGNIFICATION_FACTOR.

The third method specify a **StarRCXT** run directory, which contains a copy of the original command file that could also include a line that defines MAGNIFICATION_FACTOR.

All the values specified using above methods shall be consistent.

WHAT NEXT

Examine your settings of MAGNIFICATION_FACTOR, and make them consistent.

SEE ALSO

set_extraction_options (2) **set_starrcxt_options** (2) **signoff_opt** (2) **run_signoff** (2)

PSYN-455 (information) Cell attach file '%s' will be deleted.

DESCRIPTION

This message informs the user that the given cell attach file will be deleted.

WHAT NEXT

This is only an information message. No action is required.

PSYN-456 (warning) Running StarRCXT on a pre-routed design.

DESCRIPTION

This warning message occurs because you are running StarRCXT on a pre-routed design.

WHAT NEXT

StarRCXT should be run with a post-routed design. You are recommended to use **-pt_only** for pre-routed design.

SEE ALSO

signoff_opt(2)
run_signoff(2)

PSYN-457 (information) All '%s' timing paths will be disabled in scenario '%s'.

DESCRIPTION

This message informs the user that the given timing paths will be disabled in the given scenario.

This happens when set_scenario_options is used to specify the scenario as leakage only scenario or hold only scenario.

All setup and hold timing paths will be disabled in leakage only scenarios. All setup timing paths will be disabled in hold only scenarios.

WHAT NEXT

This is only an information message. No action is required.

PSYN-458 (error) Command is only available with PrimeTime.

DESCRIPTION

You receive this error message because you try to run a command that requires PrimeTime. **IC Compiler** invokes PrimeTime after you call **run_signoff**.

WHAT NEXT

Call **run_signoff** before invoking this command.

SEE_ALSO

run_signoff(2)

PSYN-459 (error) Only Milkyway database extraction flow is supported.

DESCRIPTION

You receive this error message because you provided a StarRCXT run directory image that does not use Milkyway database extraction flow. Instead, StarRCXT was run with LEF/DEF database extraction flow, or Calibre connectivity interface, or Hercules database extraction flow.

IC Compiler only supports Milkyway database extraction flow.

WHAT NEXT

Please re-run your standalone StarRCXT extraction with Milkyway database extraction flow.

SEE_ALSO

run_signoff(2)
signoff_signoff(2)
set_starrcxt_options(2)

PSYN-467 (Warning) This design -- %s does NOT have max transition time constraint.

DESCRIPTION

You receive this warning because this design does not have the max_transition time constraint set. If the max_transition time is not set on the design, it will be ascertained from the library and may not always be correct. Setting a proper max_transition time reduces the possibility of cross-talk/SI issues later in the flow.

WHAT NEXT

No action is required on your part.

However, you can avoid receiving this warning by setting the max_transition time. You can do this by using the **set_max_transition** command. The recommended values are:

```
0.25 Micron technology - 1.2 nS
0.18 Micron technology - 0.9 nS
0.13 Micron technology - 0.5 nS
0.09 Micron technology - 0.3 nS
```

SEE ALSO

set_max_transition(2)

PSYN-468 (Warning) This clock -- %s does NOT have transition attribute set.

DESCRIPTION

You receive this warning because this clock is an ideal clock and does not have the transition attribute set. If the correct transition time is not set on an ideal clock, it may result in an under-optimized design and may have problems later in the flow during Clock Tree Synthesis (CTS).

WHAT NEXT

No action is required on your part.

However, you can avoid receiving this warning by setting the correct transition time. You can do this by using the **set_clock_transition** command with the correct **-rise** or **-fall** option and the appropriate combination of the **-min** and **-max** options to properly set the transition time for this clock.

SEE ALSO

set_clock_transition(2)
remove_clock_transition(2)

PSYN-469 (Warning) This design has low (%.2f) utilization and placer_max_cell_density_threshold is NOT set.

DESCRIPTION

You receive this warning because this design has low utilization.

WHAT NEXT

No action is required on your part.

However, you can avoid receiving this warning by setting the **placer_max_cell_density_threshold** variable to the proper value for this design to get a better Quality of Results (QOR). For example, the value could be set to 0.7; however, the proper value for this design depends on the utilization figure.

SEE ALSO

placer_max_cell_density_threshold(3)

PSYN-470 (Warning) This cell '%s' is appeared in '%d' Failing paths and is having '%s' attribute.

DESCRIPTION

You receive this warning because this particular cell is on multiple critical paths of the design and has the dont_touch or size_only attribute set. These attributes restrict the tool's capability during optimization.

WHAT NEXT

No action is required on your part.

However, you can avoid receiving this warning by examining this particular cell and determining whether the dont_touch or size_only attribute is intended to be set. If the attribute is not required to be there, you can remove it.

SEE ALSO

check_constraints(2)
check_physical_constraints(2)
check_design(2)

PSYN-471 (Warning) This Net '%s' is appeared in '%d' Failing paths and is having '%s' attribute.

DESCRIPTION

You receive this warning because this particular net is on a critical path of the design and has the dont_touch attribute set. This attribute restricts the tool's capability during optimization.

WHAT NEXT

No action is required on your part.

However, you can avoid receiving this warning by examining this particular net and determining whether this attribute is intended to be set. If the attribute is not required to be there, you can remove it.

SEE ALSO

check_constraints(2)
check_physical_constraints(2)
check_design(2)

PSYN-475 (warning) Mismatch in the main library and the Milkyway library timing units. In the main library it is %.3f ns and in the Milkyway technology file it is %.3f ns. Check and correct the timing units in the .tf and .db files.

DESCRIPTION

This warning message occurs when there is a mismatch in the timing units in the main library and the Milkyway design library. The main library is the first library specified in the link library. In Milkyway, timing units are taken from the .tf technology file.

Ensure that the timing units are consistent between the two tools to avoid errors in the flow.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.
Make the timing units consistent in the main library database and the Milkyway .tf technology file.

SEE ALSO

check_constraints(2)
check_design(2)
check_physical_constraints(2)

PSYN-476 (warning) Mismatch in the main library and the Milkyway library resistance units. In the main library it is %.3f kohm and in the Milkyway design library it is %.3f kohm. Check and correct the resistance units in the .tf and .db files.

DESCRIPTION

This error message occurs when there is a mismatch in the resistance units in the main library and the Milkyway design library. The main library is the first library specified in the link library.
Ensure that the resistance units are consistent between the two libraries to avoid errors in the flow.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Make the resistance units consistent in the main library database and the Milkyway .tf technology file.

SEE ALSO

check_constraints(2)
check_design(2)
check_physical_constraints(2)

PSYN-477 (warning) Mismatch in the main and the Milkyway library capacitance units. In the main library it is %.3f pf and in the Milkyway design library it is %.3f pf. Check and correct the

capacitance units in the .tf and .db files.

DESCRIPTION

This warning message occurs when there is a mismatch in the capacitance units in the main library and the Milkyway design library. The main library is the first library specified in link library.
Ensure that the capacitance units are consistent between the two libraries to avoid errors in the flow.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Make the capacitance units consistent in the main library database and the Milkyway .tf technology file.

SEE ALSO

check_constraints(2)
check_design(2)
check_physical_constraints(2)

PSYN-481 (Error) Change site name failed because can not mapping site name between DB and Milkway.

DESCRIPTION

This error message occurs in xg mode, because Physical Compiler can not find site name mapping between DB and Milkyway, please check the value of the variable **mw_site_name_mapping** The value should be a string list. For example:

```
dc_shell-xg-t> set mw_site_name_mapping [list old_name1 new_name1
     old_name2 new_name2 ...]

psyn_shell-xg-t> set mw_site_name_mapping "old_name1 new_name1
     old_name2 new_name2 ..."
```

The variable must be set before loading the database and each *old_name* must pair off with a *new_name*.

WHAT NEXT

Refer to the **mw_site_name_mapping** man page for complete information.

SEE ALSO

mw_site_name_mapping(3)

PSYN-482 (Error) Routing Layer %s direction not defined, please check library unitTile.

DESCRIPTION

You receive this message because routing layer preferred direction is not set in design library unitTile. Please set all routing layers direction in design library before starting any physical commands.

WHAT NEXT

Set all routing layer direction in design library. Or set derive_default_routing_layer_direction TRUE to let the tool derive default directions

SEE ALSO

PSYN-483(2)

PSYN-483 (Information) To enable the tool to derive default directions, set derive_default_routing_layer_direction TRUE.

DESCRIPTION

You receive this message because there is routing layer missing preferred direction definition in design library unitTile. When this variable is set to true, the tool will derive default routing direction for layers missing direction definition. e.g if Metal1 has been defined as H in unitTile, Metal2 has been defined as V, but Metal3 is missing direction, the tool will derive Metal3’s direction as H. If none layer direction is defined, the tool will derive all layer directions as HVHV for Metal1/Metal2/Metal3/Metal4, etc. If this deriving is not the desired behavior, please don’t set this variable but define the directions in design library unitTile.

WHAT NEXT

SEE ALSO

PSYN-482(2)

PSYN-485 (warning) Layer %s preferred routing direction is defined as %s in design(CEL), but in library it’s defined as %s.

DESCRIPTION

This error message occurs when there is a mismatch in the design(CEL) defined routing direction and library defined one for same layer. The design(CEL) defined one will be used as layer routing direction.

Make sure the design(CEL) defined routing direction is the correct one, if need to use library defined one, don’t define the preferred routing direction for the layer in design(CEL)

WHAT NEXT

Doublecheck to make sure the direction is set as expected, If not, change the routing layer direction using set_preferred_routing_layer_direction.

SEE ALSO

set_preferred_routing_layer_direction(2)
reportt_preferred_routing_layer_direction(2)
report_ignored_layers(2)

PSYN-486 (error) Layer %s does not have preferred routing direction defined, neither in the design(CEL) nor in the library.

DESCRIPTION

This error message occurs when the layer routing direction not defined. The layer preferred routing direction can be defined in the design(CEL) or in the library. The preferred routing direction defined in the design(CEL) is used if the direction is defined in both the design(CEL) and the library.

WHAT NEXT

Make sure the layer preferred routing direction is defined in at least one of the two locations. Either define it in the design(CEL) or define it in the library and run the command again.

SEE ALSO

set_preferred_routing_direction(2)

PSYN-487 (information) Net ’%s’ is being marked as "dont_touch" because it has (nearly) abutted pins.

DESCRIPTION

You see this information because a net in your design has nearly abutted pins. To avoid any change to that net the tool mark such net as "dont_touch".

WHAT NEXT

SEE ALSO

PSYN-500 (error) This db has inconsistency multiple port shape storage.

DESCRIPTION

You receive this error message because the database does not correctly store the port shape in cdb.

WHAT NEXT

Set the **psyn_get_port_shape_from_user_attrs** variable to TRUE before writing out the .pdef file. Read the same .pdef file back in to regenerate the database. Rerun the command reading the new database.

SEE ALSO

read_pdef (2), **write_pdef** (2).

PSYN-501 (Warning) Net '%s' is not routed.

DESCRIPTION

You receive this warning message because the net is not routed. physopt -on_route can not perform optimization on the net.

WHAT NEXT

PSYN-502 (Warning) Pin '%s' is not connected by routing.

DESCRIPTION

You receive this warning message because the pin is not connected to its net by routing. physopt -on_route can not perform optimization on the net.

WHAT NEXT

PSYN-503 (Infomation) RC extraction has been freed.

DESCRIPTION

WHAT NEXT

PSYN-504 (error) Cannot find lib cell (%s) characterized for P=%f, V=%f, T=%f and library subset = %s. Also it might have dont-use attribute.

DESCRIPTION

You receive this message because the **insert_spare_cells** command cannot insert spare cells for the given library cell. This is because it either does not exist in the linked libraries or has no timing information for specified process, voltage or temperature.

WHAT NEXT

Examine the cell name and determine that it exists and is of the correct type.

SEE ALSO

insert_spare_cells (2).

PSYN-508 (information) %-5s CPU: %6d s (%5.2f hr) ELAPSE: %6d s (%5.2f hr) MEM-PEAK: %5lu Mb %s

DESCRIPTION

When **monitor_cpu_memory** is true, the cpu time, elapse time and memory peak usage will be printed out at the major steps in ICC commands, such as place_opt, clock_opt etc.

CPU/Elapse time is the total time spent on main process and all the child processes or multiple threads, e.g. when you use -num_cpus option, the reported CPU time contains the sum of the main process and all child process or threads CPU usage. Just like the output of command of "cputime -self -child" or "cputime -all".

Following is a special note for **Multiple threads**: when use -num_cpus ICC will run in multpile trheads. Currently OS system meansures the cputime by adding all the threads usage. It does not take into account of parallelization of the threads. This means user may see the CPU usage reported larger than elapse time when -num_cpus option is used and ICC is running in multi-threading mode.

Following are the special notes for **Elapse time**: the elapse time (e.g. wall-clock time) is depended on many external factors and can vary from every run. It depends on the IO traffic, network traffic, RAM/Swap usage, other processes running on the same machine, etc. When user sees elapse time is much longer than the CPU time, it may point out the inefficiency of the computing environment, such as insufficient memory, too many processes running on the same machine, slow network, etc. The only way to make the elapse time close to CPU time is to run only one icc_shell on the machine with enough RAM and using local disk.

Memory peak is defined as the memory high-water-mark of the main process. When ICC report memory peak, it means the maximum memory ICC allocated from the system. When child process exits, ICC will report the maximum number of main and child memory usage. User can also use following command to get the ICC memory information interactively: **mem -all -verbose**

EXAMPLE

If you set monitor_cpu_memory true in the TCL, you will see following message in the log file.

Information: CPU: 23 s (0.01 hr) ELAPSE: 89 s (0.02 hr) MEM-PEAK: 155 Mb Mon Oct 27 17:22:16 2008. (PSYN-508)

SEE ALSO

monitor_cpu_memory (3)
cputime (2)
mem (2)

PSYN-509 (Information) MEM-PEAK in main process: %5lu Mb, MEM-PEAK in child processes: %5lu Mb.

DESCRIPTION

You receive this information message becaus variable **physopt_monitor_cpu_memory** is set to *true*, and there are child processes invoken under the main process.

It display the memory peak usage of the main process, and the maximum memory peak usage of all the child processes.

SEE ALSO

physopt_monitor_cpu_memory (3)
PSYN-508 (n)

PSYN-511 (information) Set variable mw_site_name_mapping to change site name.

DESCRIPTION

This information message occurs in xg mode, because you need to use the **mw_site_name_mapping** variable to change to a new site name.

The format is as follows:

```
dc_shell-xg-t> set mw_site_name_mapping [list old_name1 new_name1
     old_name2 new_name2 ...]

psyn_shell-xg-t> set mw_site_name_mapping "old_name1 new_name1
```

```
      old_name2 new_name2 ..."
```

The variable must be set before loading the database and each *old_name* must pair off with a *new_name*.

The **change_site_name** command cannot be used in xg mode because the site name mapping must be performed before you load the design. The **change_site_name** command is only valid after the design is loaded, so it does not work in xg mode.

You can use the **change_site_name** command in normal mode.

WHAT NEXT

Refer to the **mw_site_name_mapping** man page for complete information.

SEE ALSO

mw_site_name_mapping(3)

PSYN-512 (warning) Different TLU+/NXTGRD between IC Compiler and StarRCXT

DESCRIPTION

You receive this warning because you are trying to run **run_signoff -correlation** command with different TLU+ or NXTGRD version. Please check the version name, version number, or technology name in both files.

WHAT NEXT

Have consistent TLU+/NXTGRD files for correlation.

SEE_ALSO

run_signoff

PSYN-513 (warning) SDC commands for IC Compiler and PrimeTime correlation

DESCRIPTION

You receive this warning because you are trying to run **run_signoff -correlation** command, some SDC commands may cause correlation issues.

set_input_transition: For correlation purpose, user has to use "set_driving_cell" for input pin in SDC file.

set_input_delay: For correlation purpose, user has to use "set_clock_latency -source" for clock port in SDC file.

set_clock_latency: For correlation purpose, the latency value should be larger than 0 in SDC file.

set_propagated_clock: For correlation purpose, user has to set it on all clocks to make sure all clocks will be propagated.

set_load: For correlation purpose, any net specified should not be used in set_load command

set_resistance: For correlation purpose, any net specified should not be used in set_resistance command

WHAT NEXT

Check and modify SDC file for correlation.

SEE_ALSO

run_signoff

PSYN-514 (warning) Tcl commands for IC Compiler and PrimeTime correlation

DESCRIPTION

You receive this warning because you are trying to run **run_signoff -correlation** command with some correlation related Tcl commands between IC Compiler and PrimeTime.

set_delay_calculation: Use arnoldi in both IC Compiler and PrimeTime.

set_operating_condition: Use on_chip_variation in both IC Compiler and PrimeTime when this design is MCMM.

set_clock_gating_check: Turn on set_clock_gating_check in both IC Compiler and PrimeTime.

WHAT NEXT

Have a correct setting for correlation.

SEE_ALSO

run_signoff

PSYN-515 (warning) Inconsistent SI settings between IC Compiler and PrimeTime

DESCRIPTION

You receive this warning because you are trying to run **run_signoff -correlation** command with different SI settings. To use SI for correlation purpose, user has to set delta delay. To use static noise, the delta delay should be set first.

WHAT NEXT

Have a consistent setting for correlation.

SEE_ALSO

run_signoff

PSYN-516 (warning) Different setting or value between IC Compiler and PrimeTime

DESCRIPTION

You receive this warning because you are trying to run **run_signoff -correlation** command with different setting or value between IC Compiler and PrimeTime.

WHAT NEXT

Always have a consistent setting and value for correlation.

SEE_ALSO

run_signoff

PSYN-517 (warning) Different setting or value between IC

Compiler and PrimeTime

DESCRIPTION

You receive this warning because you are trying to run **run_signoff -correlation** command with different setting or value between IC Compiler and PrimeTime.

WHAT NEXT

Always have a consistent setting and value for correlation.

SEE_ALSO

run_signoff

PSYN-518 (warning) Different setting or value between IC Compiler and StarRCXT

DESCRIPTION

You receive this warning because you are trying to run **run_signoff -correlation** command with different setting or value between IC Compiler and StarRCXT.

WHAT NEXT

Always have a consistent setting and value for correlation.

SEE_ALSO

run_signoff

PSYN-519 (error) Correlation script problem

DESCRIPTION

You receive this warning because you are trying to run **run_signoff -correlation** command, but there is a problem for a script generated automatically. By default, there is a script called "signoff_correlation_setup.user_name.process_id.tcl" created after **run_signoff -correlation**. This problem may happen when tool can not detect user name, find a valid process id, or have permission problem to write. Check the permission issue first. Latest result will be appened to end of file in multiple run.

WHAT NEXT

Solve permission problem first.

SEE_ALSO

run_signoff

PSYN-520 (Warning) %s (%s) is placed at (%d,%d) which is outside die area.

DESCRIPTION

This error message tells you that the placement for the specified pad or I/O is illegal.

WHAT_NEXT

Use the **check_legality -verbose** command to see more detailed messages about the placement issues. Run legalize_placement if it has not already been run.

SEE ALSO

check_legality (2), **legalize_placement** (2).

PSYN-541 (warning) All cells and nets in cluster ’%s’ is being marked
as "dont_touch" because the cluster has a fixed_logic attribute.

DESCRIPTION

You see this warning because a cluster in your design bears a *fixed_logic* attribute in the input PDEF. The tool marks all cells and nets in such cluster as "dont_touch".

WHAT NEXT

To modify the cluster, remove the *fixed_logic* attribute in PDEF. Then read in the PDEF again, using the **read_pdef** command.

SEE ALSO

read_pdef (2).

PSYN-543 (error) cell instance '%s' does not have a reference design.

DESCRIPTION

You see this error because there is cell instance in your design which does not have a design reference.

WHAT NEXT

Fixed the reference to the cell instance mentioned in the error message. You may have a corrupted db, and it might be necessary to regenerate the db file.

SEE ALSO

PSYN-544 (warning) design cluster '%s' is an obstruction without design objects.

DESCRIPTION

This warning occurs because the specified cluster is designated as a design cluster. However, it is an obstruction cluster and does not have any design objects in it. The tool considers sub-clusters, cells, and nets to be design objects. In this case, the tool ignores this design cluster and treats it as an obstruction.

WHAT NEXT

You might want to remove the design cluster designation from the obstruction cluster.

PSYN-555 (error) Checking any commands accessing wrongly

DC/NID attribute (id: %d)for already ported attributes

DESCRIPTION

You see this error because there is a commands accessing wrongly DC/NID attribute for already ported attributes

WHAT NEXT

Contact the Synopsys Customer Support Center by sending an email message to support_center@synopsys.com.

SEE ALSO

PSYN-562 (error) %s value is invalid: %g

DESCRIPTION

You receive this message because the resistance or capacitance in the specified direct is less than or equal to zero. The resistance and capacitance for each direction should be greater than 0.

WHAT NEXT

Examine the physical library and correct the RC values.

SEE ALSO

check_physical_constraints (2).

PSYN-590 (Warning) No physical library cell for physical instance %s.

DESCRIPTION

You received this warning message because a physical instance doesn’t have a physical library cell in any of the physical libraries specified.

WHAT NEXT

All instances in the design must have an associated physical library cell.

Check the physical libraries specified using the command report_mw_lib -mw_reference_library. If this list does not contain all the expected physical libraries, update the list using the command set_mw_lib_reference.

The command get_physical_lib_cells */* will list all physical cells currently loaded (use appropriate patterns or filters to restrict the results).

SEE ALSO

report_mw_lib(2) set_mw_lib_reference(2) get_physical_lib_cells(2)

PSYN-600 (error) Number specified is invalid

DESCRIPTION

You receive this error message because the input numbers are invalid. The last command aborted due to this error.

WHAT NEXT

Examine the input numbers to the last command, correct the invalid numbers, and run the command again.

PSYN-601 (error) Current directory is not writable!

DESCRIPTION

You receive this error message because the current directory is not writable. In stand-alone mode detail placement, the current directory must be writable. The last command aborted due to this error.

WHAT NEXT

Examine current directory, make sure it is writable, and run the command again.

PSYN-602 (error) Failed in reading back data.

DESCRIPTION

This error occurs because the stand-alone process cannot read back the data from the disk. The reason for this failure might be due to some problem with the swapping directory .sdp or might be because you have changed some of the content of the

swapping directory. The tool prohibits any change to the files inside swapping directory because they are internal data and might be constantly changing. The last command aborted due to this error.

WHAT NEXT

Check current directory, ensure that it is writable, and do not alter it. Then, rerun the command.

PSYN-603 (error) Can not get the site master of cell '%s'.

DESCRIPTION

You receive this error because the tool can not get the site master of the specified cell. The option -measurement num_sites need to get site master for each specified cell to computer the keepout margin.

WHAT_NEXT

You need to check and make sure the cells you set keepout margin have correct information of site master.

SEE ALSO

set_keepout_margin (2)

PSYN-604 (Error) Can not define option 'num_sites' together with 'soft|all_macros|macro_masters|macro_instances'.

DESCRIPTION

You receive this message because you specify 'num_sites' and 'soft|all_macros|macro_masters|macro_instances' together at the same time.

These options are mutually exclusive and cannot be used together at the same time in command **set_keepout_margin**.

WHAT NEXT

Use either '-measurement num_sites' or 'soft|all_macros|macro_masters|macro_instances'.

SEE ALSO

set_keepout_margin (2)

PSYN-605 (information) Running stand-alone coarse placer in a separate process using temp directory '%s'.

DESCRIPTION

This message indicates that the coarse placer will run in a separate process. Placer separate process can be disabled by using the variable placer_run_in_separate_process. The temp directory can be changed using the UNIX environment variable TMPDIR.

WHAT_NEXT

SEE ALSO

placer_run_in_separate_process

PSYN-606 (information) Preparing to run stand-alone detail placer (SDP) in remote ...

DESCRIPTION

This message indicates that the detail placer will be run in a separate process.

WHAT_NEXT

PSYN-607 (information) The stand-alone detail placer (SDP) is running in remote ...

DESCRIPTION

This message indicates that the detail placer is running in a separate process.

WHAT_NEXT

PSYN-608 (information) The stand-alone detail placer (SDP) %s!

DESCRIPTION

This message indicates whether the stand-alone detail placer is successful or not.

WHAT_NEXT

PSYN-609 (information) %d filler cells have been removed!

DESCRIPTION

This message indicates that filler cells are present during detail placement. IC Compiler will first remove all of the movable filler cells, then perform the legalization. Users will need to insert filler cells again later.

WHAT_NEXT

PSYN-610 (warning) '%s' command is obsoleted. Although it will still function normally now, please use '%s' command to replace this command in the future.

DESCRIPTION

This warning occurs because the tool is obsoleting this command. However, it is still functional in this version. In the future, please use the replacement command.

WHAT NEXT

Remove the obsolete command, and replace it with the new command.

PSYN-611 (warning) '%d' cells placed outside their hard bounds

DESCRIPTION

This message indicates that there are some cells which are not in their assigned hard-bounds after floorplan region based legalization. Following are some of the reasons:-

- The region or bound is over the capacity.
- There is no site in the bound which is legal for some cells.

WHAT NEXT

Verify the feasibility of the region constraints for cells and the floorplan.

PSYN-612 (error) The cell '%s' does not fall in any region.

DESCRIPTION

This message indicates that the mentioned cell does not belong to any floorplanning region in the design. The physopt requires that if regions exists in the design, then all cells must belong to some region. Following are some of the reasons:-

- The cell was meant to be in default region which is not yet created.
- The floorplan is not correctly partitioned into physical regions.

WHAT NEXT

Verify the feasibility of the region constraints for cell and the floorplan.

PSYN-613 (Error) The value of '-measurement percentage' can not be negative or all zero.

DESCRIPTION

You receive this message because the value (lx by rx ty) you are inputting with 'set_keepout_margin -measurement percentage' is negative or all zero.

WHAT_NEXT

Provide a percentage value larger than zero. For example, 0.1 (10 percent).

SEE ALSO

set_keepout_margin (2)

PSYN-614 (Error) The inputting (lx by rx ty) are equal or greater than 1.

DESCRIPTION

You are inputting (lx by rx ty), ICC considers them as (lx*100% by*100% rx*100% ty*100%) since you have defined the '-measurement' as percentage, ICC believes the normal scope should be 0.01-0.99 (1%-99%).

WHAT_NEXT

Provide positive and proper value (lx by rx ty).

SEE ALSO

set_keepout_margin (2)

PSYN-615 (Error) The '-measurement' option takes only microns|percentage|num_sites as argument.

DESCRIPTION

You receive this error message because you are inputting wrong argument for -measurement option.

WHAT_NEXT

You should input microns|percentage|num_sites for -measurement.

SEE ALSO

set_keepout_margin (2)

PSYN-616 (Warning) Converge problem found, The

max_net_length constraint of net %s might not be met!

DESCRIPTION

This message indicates that the detail placer is trying to fix the max_net_length constraint of a certain net, but it failed. The possible reasons may be: 1) Too many nets have this max_net_length constraint; 2) Too many cells/nets with this constraint are overlapping each other; 3) The constraint threshold is too tight; 4) There are some fixed cells with this net, and the bbox net length of the fixed cells is larger than the user defined threshold; 5) There may exist some constraint loop among the existing max_net_length nets, which makes such a fixing an impossible task.

WHAT_NEXT

Once this error message shows up, the users need to check their design data, and try to relax some constraint setting.

PSYN-617 (Warning) Violating Net: %s orig_length/ current_length/threshold = %d/%d/%d

DESCRIPTIO

This message indicates that some nets may have "max_net_length" violation. This message is to report the "original net_length", "current net_length", and the "threshold" which has been set by the users.

WHAT_NEXT

Once this error message shows up, the users need to check their design data, and try to relax some constraint setting such as make the threshold value bigger.

PSYN-618 (Error) At lease one of the "left padding" or "right padding" should be specified!

DESCRIPTIO

This message indicates that neither "left padding" nor "right padding" has been defined with command "set_cell_padding". Users should define at least one of the "-left" or "-right" option.

WHAT_NEXT

Correct the mistake and run command "set_cell_padding" again.

PSYN-619 (Error) One and only one of [-reference_name] or [object_list] should be specified!

DESCRIPTIO

This message indicates that users have specified either both of [-reference_name] and [object_list] or none of them. Users should define only one of them.

WHAT_NEXT

Correct the mistake and run command "set_cell_padding" again.

PSYN-620 (Error) The bounding box or rectangle of '%s' is illegal,
it's lower-left corner coordinates are not smaller than upper-right corner coordinates.

DESCRIPTION

You receive this message because the coordinates of a bounding box or rectangle are not given in order from the lower-left corner to the upper-right corner or the coordinates form a line instead of a bounding box or rectangle.

WHAT_NEXT

Place the lower-left corner coordinates before the upper-right corner coordinates, and ensure that it forms a valid bounding box or rectangle.

PSYN-621 (error) %s: Invalid buffer cell(s) specified for the -default_reference option.

DESCRIPTION

You receive this message because an invalid buffer cell is set.

WHAT_NEXT

To set the correct buffer reference, make sure the cell name specified in **physopt_hfs_default_reference** variable is a valid and active buffer cell for current design.

SEE ALSO

set_ahfs_options (2).

PSYN-625 (warning) Removed the physical data of design '%s' in order to load physical data for the current design or another design.

DESCRIPTION

This warning occurs because the command you have run is trying to read physical design data, and a design already exists that has physical design data. Currently, the tool can have only one design with physical data in memory. You must remove existing physical design data before you read physical design data for another design.

If you remove the physical data of a design, you can still apply current_design to that design, but you will not be able to see, modify, or create any physical information of that design.

WHAT_NEXT

Follow the recommended flow of reading designs and physical data into memory.

PSYN-626 (error) No additional PSYN-XG licenses are available.

DESCRIPTION

You receive this error message because no PSYN-XG or no more PSYN-XG licenses are available.

WHAT NEXT

SEE ALSO

PSYN-650 (warning) Cell %s has no orientation; check %s library %s cell symmetry.

DESCRIPTION

This warning message occurs when the cell symmetry is not found in the physical library or in the FRAM library. The tool sets the symmetry to one (the default value), which impacts the detail placement result.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Add the symmetry to the physical library or the FRAM library for the cell.

SEE ALSO

PSYN-651(n)

PSYN-651 (warning) Cell %s orientation is set to the default.

DESCRIPTION

This warning message occurs when cell symmetry is not found in the physical library or the FRAM library. The symmetry is set to 1 (the default value), which impacts the detail placement result.

This warning message is always issued after the **PSYN-650** message.

The default orientation is set during the data preparation flow of Milkyway while running the **auSetPRBoundary** command. In Milkyway, you can set the orientations by using the **dbBdbSetStdCellOrient** command. The syntax for this command is:

dbSetStdCellOrient *libName cellName*
orientation

where *orientation* is either one of the following keywords: Any, Reflect, or **Noreflect**, or any combination of the following keywords: R0, R0_MX, R0_MY, R180, R90, R90_MX, R90_MY, and R270, such as "R0 R0_MY R180 R90_MX".

WHAT NEXT

This is only a warning message. You can eliminate this warning message by adding symmetry to the physical library or the FRAM library for the cell.

SEE ALSO

PSYN-650(n)

PSYN-652 (warning) Cell %s (%d %d) overlaps with exclusive_region (%d %d) (%d %d).

DESCRIPTION

This warning message occurs when one cell overlaps an exclusive_region that you have defined. The placement is not valid.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Use the **legalize_placement** command to make the placement valid.

SEE ALSO

legalize_placement(2)

PSYN-653 (warning) Library Cell %s has invalid boundBox, size is set to 0, please check the library.

DESCRIPTION

This warning message occurs when the Cell’s boundBox is invalidated. Set the size as 0.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Please check the libray.

SEE ALSO

PSYN-654(n)

PSYN-654 (warning) Cell size will be set as 0.

DESCRIPTION

This warning message occurs when the Cell’s width or height is invalidated. Set the size as 0.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Please check the libray.

SEE ALSO

PSYN-655(n)

PSYN-655 (warning) Library Cell %s has invalid width:%d or height:%d, please check library cell PRbbox (%d %d)(%d %d).

DESCRIPTION

This warning message occurs when the Cell’s width or height is invalidated. Set the size as 0.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Please check the libray.

SEE ALSO

PSYN-654(n)

PSYN-656 (error) Multiple pin with same name %s defined in

physlib design %s.

DESCRIPTION

This message indicates that there are more than one pin named as same.

WHAT NEXT

Verify the physlib design.

PSYN-657 (warning) MW mode rc layer plate_cap loading not working, no support.

DESCRIPTION

This warning message occurs when run this command under MW mode.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Please check the mode.

PSYN-658 (warning) nondrule layer shield_width and shield_spacing not working for MW mode.

DESCRIPTION

This warning message occurs when run this command under MW mode.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

R&D must do before release.

PSYN-659 (warning) FRAM loading %s has problem getting

layer number.

DESCRIPTION

This warning message occurs when load layer has problem getting layer number.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Please check the layer.

PSYN-660 (warning) No routing direction for layer : %s, set to %s.

DESCRIPTION

This warning message occurs when no routing direction for this layer.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Please check the direction.

PSYN-661 (error) MW TF layer loading number mismatch, multiple layers defined with same maskname.

DESCRIPTION

This message indicates that there are more than one layers defined with same maskname.

WHAT NEXT

Please correct the TF for the design library.

PSYN-665 (warning) Setting fixed placement attribute on

hierarchical cell not allowed.

DESCRIPTION

This warning message occurs when you are trying to set fixed placement attribute by set_dont_touch_placement command or by set_attribute command on a object and the object is hierarchical cell.

WHAT NEXT

Hierarchical cells does not have location and no physical properties. Please check your script first and find out why you setting fixed placement attribute on hierarchical cell.

PSYN-666 (warning) Object %s does not have location. Can not set fixed placement attribute.

DESCRIPTION

This warning message occurs when you are trying to set the fixed placement attribute (by using the set_dont_touch_placement or set_attribute command) on an object and the object is not yet placed. This warning message is issued only for leaf cells and not for hierarchical cells that also do not have a location.

WHAT NEXT

Assign a location to the object and reissue the set_dont_touch_placement or set_attribute (with restrictions attribute) command.

PSYN-670 (warning) No '%s' keepout margin found on '%s' '%s' to remove.

DESCRIPTION

You receive this message because remove_keepout_margin command is not able to remove the soft/hard keepout margin on the specified cells or lib cells or all macro cells or all macro instances etc.. because soft/hard keepout margin is not present.

WHAT_NEXT

Please make sure that the cell or lib cell has keepout margin before calling remove_keepout_margin

PSYN-671 (Info) Over writing the existing keepout margin values on ’%s’ ’%s’.

DESCRIPTION

You receive this message when you are over writing the keeout margin values of cells or lib cells using set_keepout_margin command

WHAT_NEXT

PSYN-672 (warning) Unable to set keepout margin on object ’%s’.

DESCRIPTION

You receive this message because set_keepout_margin command is unable to set the keepout margin on cells or lib cells. This may be because you are trying to set keepout margin on hierarchical cell or any other object other than cell or lib cell.

WHAT_NEXT

Please make sure that you are setting keepout margin on leaf cells or lib cells

PSYN-673 (warning) Invalid value specified for ’%s’.

DESCRIPTION

You receive this message because you have specified out of range value for one of -tracks_per_macro_pin or -max_padding_per_macro or -min_padding_per_macro.

WHAT_NEXT

Please make sure that you follow the following range 0.0 <=tracks_per_macro_pin <= 10.0 -1.0 <= max_padding_per_macro <= 1.0 0.0 <=min_padding_per_macro <= 0.5

PSYN-674 (warning) Unable to set pin count based keepout

margin.

DESCRIPTION

You receive this message because set_keepout_margin is not able to set the pin count based keepout margin.

WHAT_NEXT

Please make sure that the CEL is opened in write mode.

PSYN-675 (warning) Ignoring object '%s' not a macro.

DESCRIPTION

You receive this message because you are trying to set keepout margin on non macro cell or non macro lib cell with -macro_masters/-macro_instances options

WHAT_NEXT

Please make sure that the cell or lib cell are macros when ever using one of the options -macro_masters/-macro_instances

PSYN-676 (warning) Invalid value specified for -type.

DESCRIPTION

You receive this message because you have specified invalid value for -type option. Only hard or soft can be specified for -type

WHAT_NEXT

Please make sure that you hard/soft for -type

PSYN-677 (Error) Unable to remove pin count based keepout

margin.

DESCRIPTION

You receive this message because there is no pin count based keepout margin exist or CEL is opened in read-only mode.

WHAT_NEXT

Please make sure that pin count based keepout margin exist before removing it and make sure the CEL is opened in write mode

PSYN-678 (Error) Require argument 'object list' | '-paramter' not found.

DESCRIPTION

You receive this message because you have not specified 'object list' or '-parameter' option for report_keepout_margin

WHAT_NEXT

Please make sure you specify one of 'object list' or '-parameter' for report_keepout_margin

PSYN-679 (warning) Unable to get keepout margin on '%s' '%s'.

DESCRIPTION

You receive this message because you are not able to get the keepout margin specified on cell or lib cell.

WHAT_NEXT

Please make sure that the cell or lib cell has keepout margin

PSYN-680 (warning) Either user defined or pin count based

keepout margin should be specified.

DESCRIPTION

You receive this message because you have specified both user defined keepout margin (usign -outer) and global pin count based derived keepout margin together.

WHAT_NEXT

Please make sure that you specify only one for set_keepout_margin command

PSYN-681 (warning) Pin count based keepout margin is always hard.

DESCRIPTION

You receive this message because you have specified pin count based keepout margin along with soft for -type option. Pin count based keepout margin is always hard and '-type soft' will be ignored.

WHAT_NEXT

PSYN-700 (error) The mw_design_library variable is not specified. Checkpointing cannot be enabled without mw_design_library.

DESCRIPTION

This error message occurs in xg mode when you have enabled checkpointing by setting the **physopt_checkpoint_stage** variable, but the **mw_design_library** variable is not defined. In xg mode, checkpointing is done in the CEL view for which the **mw_design_library** variable is necessary. The last command aborted due to this error.

WHAT NEXT

Set the **mw_design_library** variable to a string and run the command again.

SEE_ALSO

physopt(2)
mw_design_library(3)

PSYN-725 (error) Voltage area %s has utilization of %f which is greater than 1.

DESCRIPTION

This error message occurs when the tool tries to operate on voltage areas. It finds that the specified voltage area is over utilizied and thus it cannot proceed further. The utilization is infered as ratio of moveable cells area and placement area of a voltage area.

WHAT NEXT

To fix this error, you can either remove the specified voltage area and re-create it with adjusted coordinates and hierarchies or just remove some hierarchies from voltage area.

SEE ALSO

create_voltage_area(2)
remove_voltage_area(2)
update_voltage_area(2)
report_cell(2)

PSYN-750 (Warning) For net %s, %s is less than %s.

DESCRIPTION

You receive this message because either threshold or bound specified with all_drc_violated_nets command is less than the required value (constraint). If it is threshold then the command will report the violated nets only and ignore all the non-violated nets even if they cross threshold. If it is bound then command may not report any net at all.

WHAT_NEXT

Provide a more appropriate value of threshold/bound with all_drc_violated_nets command.

PSYN-840 (warning) Object '%s' not found in design. Attribute

'%s' will not be set.

DESCRIPTION

This warning is issued in PC-XG if an object exists in the instance tree but not in the actual design. The most likely cause of this problem is that the instance tree is not upto date and needs to be cleaned up.

WHAT NEXT

Setting the hidden variable update_instance_data_in_db to TRUE in PC-XG will clean up the instance tree during read_db. Alternately in PC-DB mode, the hidden command update_instance_data can be used to clean up the instance tree and then save the db file. Use this cleaned up db file in PC-XG mode in a new shell.

PSYN-850 (warning) New port '%s' is generated to sub_module '%s' as an additional of original port '%s'.

DESCRIPTION

This warning is issued in AHFS when a new port is added into a sub_module. It happens only when AHFS port punching is enabled.

WHAT NEXT

physopt_enable_placement_hfs (3), physopt_hfs_hf_new_port (3), physopt_hfs_hf_new_port_map (3).

PSYN-860 (warning) The automatic high-fanout synthesis variable %s is being replaced. The recommended flow is to use the set_ahfs_options command.

DESCRIPTION

This warning message occurs because the specified user variable to control the automatic high-fanout synthesis behavior is being replaced by the **set_ahfs_options** command

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following

the instructions below.

Use the **set_ahfs_options** command to set the specified variable and then run the command again.

SEE ALSO

set_ahfs_options(2)

PSYN-861 (warning) Automatic high-fanout synthesis is disabled in the region based design.

DESCRIPTION

This warning message occurs when automatic high-fanout synthesis is disabled because the design has physical regions.

WHAT NEXT

This is only a warning message. No action is required.

SEE ALSO

create_buffer_tree(2)

PSYN-862 (warning) Automatic high-fanout synthesis has been done. It will not be executed now.

DESCRIPTION

This warning message occurs when automatic high-fanout synthesis has already been executed and will not be performed again.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Use the **set_ahfs_options** command to set the preferred settings for automatic high-fanout synthesis to run again.

SEE ALSO

set_ahfs_options(2)

PSYN-863 (error) No current library defined!

DESCRIPTION

This message is to inform users that no current logical library has been defined during Automatic High-Fanout Synthesis.

WHAT_NEXT

User should make sure that all the library settings are correct before running physopt or Automatic High-Fanout Synthesis.

PSYN-864 (information) Automatic high-fanout synthesis adds %d new cells.

DESCRIPTION

This information message advises you of the number of new cells that automatic high-fanout synthesis has added to the design.

WHAT NEXT

This is an informational message only. No action is required.

PSYN-865 (information) Total number of drivers is %d.

DESCRIPTION

This information message advises you of the the number of drivers that are selected by automatic high-fanout synthesis.

WHAT NEXT

This is an informational message only. No action is required.

PSYN-866 (error) Automatic high-fanout synthesis failed.

DESCRIPTION

This error message occurs when automatic high-fanout synthesis fails on the selected drivers.

WHAT NEXT

Contact the Synopsys Customer Support Center by sending an email message to support_center@synopsys.com.

PSYN-867 (information) Automatic high-fanout synthesis removes all buffer trees.

DESCRIPTION

This information message advises you that automatic high-fanout synthesis is removing all buffer trees.

WHAT NEXT

This is an informational message only. No action is required.

PSYN-868 (information) Automatic high-fanout synthesis removes critical buffer trees.

DESCRIPTION

This information message advises you that automatic high-fanout synthesis is removing only buffer trees that are timing critical.

WHAT NEXT

This is an informational message only. No action is required.

PSYN-869 (information) Automatic high-fanout synthesis in

progress for high fanout nets.

DESCRIPTION

This information message advises you that automatic high-fanout synthesis is optimizing the nets that have fanouts higher than the **hf_threshold** that is specified with the **set_ahfs_options** command.

WHAT NEXT

This is an informational message only. No action is required.

PSYN-870 (information) Automatic high-fanout synthesis in progress for medium fanout nets.

DESCRIPTION

This information message advises you that automatic high-fanout synthesis is now optimizing nets that have fanouts higher than the **mf_threshold** and lower than the **hf_threshold** that is specified with the **set_ahfs_options** command.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

set_ahfs_options(2)

PSYN-871 (information) No driver found.

DESCRIPTION

This information message advises you that no driver has been selected by automatic high-fanout synthesis for optimization.

WHAT NEXT

This is an informational message only. No action is required.

PSYN-872 (error) The %s net has no netgroup.

DESCRIPTION

This error message occurs when the specified net does not have an associated netgroup.

WHAT NEXT

Contact the Synopsys Customer Support Center by sending an email message to support_center@synopsys.com.

PSYN-873 (error) Automatic high-fanout synthesis could not open the port mapping file %s for writing.

DESCRIPTION

This error message occurs when the specified file cannot be opened by automatic high-fanout synthesis for write permission.

WHAT NEXT

Ensure that the specified file has the correct file permissions before starting the run.

PSYN-874 (warning) Keepout margin on '%s' falls outside core/die area.

DESCRIPTION

This warning message occurs when the keepout margin parameters are not within the core/die area.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the directions below.

Check the PDEF file to be sure that the given keepout margin values are well within the core/die area.

PSYN-875 (information) Time units from Milkyway: '%s'.

DESCRIPTION

This information message advises you about the time units Milkyway is using. There may be a difference between the timing units followed in tool and Milkyway database.

WHAT NEXT

This is an informational message only. No action is required.

PSYN-876 (information) Timing units are matched - '%.3f' ns.

DESCRIPTION

This information message advises you that both tool and Milkyway database use the same timing units and shows the exact match of units.

WHAT NEXT

This is an informational message only. No action is required.

PSYN-877 (information) Executable name is '%s'.

DESCRIPTION

This information message advises you of the executable name used during placement.

WHAT NEXT

This is an informational message only. No action is required.

PSYN-878 (Information) linking reference library : %s.

DESCRIPTION

You receive this information message because the **link_physical** command is linking logical libraries with reference libraries.

WHAT NEXT

PSYN-879 (warning) ’%s’ pin on ’%s’ cell in the ’%s’ physical library is missing in the ’%s’ technology library.

DESCRIPTION

You receive this message because a cell pin in the physical library is missing from the same-name cell pin in the technology library. Consequently, the logical cell cannot be linked with the same-name cell in the physical library.

WHAT NEXT

Examine this cell pin in both libraries. Add the missing cell pin to your technology library.

PSYN-880 (error) Need buffers and inverters to proceed.

DESCRIPTION

You receive this message because there is no buffer or inverter available for optimization in the target library.

WHAT NEXT

Examine if your library has both buffers and inverters. Add the missing cell to your library.

PSYN-882 (warning) Consecutive metal layers have the same preferred routing direction.

DESCRIPTION

This error message occurs when two or more consecutive metal layers have the same prefferred routing direction. The preferred routing direction of a metal layer is the library defined preferred routing direction unless a user defined library direction is explicitly set in the design(CEL).

WHAT NEXT

This is only a warning message. Use set_preferred_routing_direction command to set a user defined direction for a layer in the design(CEL). To remove a user defined direction & defult to using the library defined direction, use remove_preferred_routing_direction command.

SEE ALSO

set_preferred_routing_layer_direction(2)
remove_preferred_routing_direction

PSYN-883 (error) Can’t use non-metal layer ’%s’.

DESCRIPTION

You get this error because you are trying to set direction on a non-metal layer in layer list.

WHAT NEXT

Run set_layer_preferred_direction on existing routable metal layers from the physical library.

PSYN-884 (warning) All metal layers have the same preferred routing direction.

DESCRIPTION

This error message occurs when all metal layers have the same preferred routing direction set for them. The preferred routing direction of a metal layer is the library defined preferred routing direction unless a user defined library direction is explicitly set in the design(CEL).

WHAT NEXT

This is only a warning message. Use set_preferred_routing_direction command to set a user defined direction for a layer in the design(CEL). To remove a user defined direction & defult to using the library defined direction, use

remove_preferred_routing_direction command.

SEE ALSO

set_preferred_routing_layer_direction(2)
remove_preferred_routing_direction

PSYN-885 (error) ’%s’ is invalid layer in option -%s list.

DESCRIPTION

You get this error because you specified an invalid layer. User-defined layer name, or mask name "poly", "metal1", "metal2", ..., "metal12" are acceptable.

PSYN-886 (error) ’%s’ is invalid value in option -%s list.

DESCRIPTION

In -dir list, ’V’, ’H’, ’v’, ’h’ are acceptable as direction. In -offset list, double value is acceptable as offset.

PSYN-887 (Error) cell %s is not on a row! this cell will be ignored!

DESCRIPTION

This message indicates that the input data has an issue: "same_row_eco" mode legalization requests that all input cells should reside in a row. If a cell does not reside in any row, ICC legalization will ignore it as if it does not exist at all. Users may end up with some overlapping between this cell and other cells.

WHAT_NEXT

Once this error message shows up, the users need to check their design data. If this is a user error, users need to run a "normal-mode" legalization before they run this "same_row_eco".

PSYN-888 (Error) row %s{%.3f %.3f %.3f %.3f} is over-capacity! The demand is: %d

sites(%d+%d+%d)(cell+padding+blockage), but the supply is: %d sites.

DESCRIPTION

This message indicates that the input data has an issue: "same_row_eco" mode legalization requests that a row should have enough room to accommodate all the cells on this row. If the row does not have enough room to place the cells, users may end up with some overlapping among cells.

WHAT_NEXT

Once this error message shows up, the users need to check their design data. In this situation, users need to relax their design constraints.

PSYN-889 (Information): Porosity Control is ON (%s). Now the utilization with Porosity Control is: %s

DESCRIPTION

This message indicates that the users have set the variable "legalize_porosity_control" to a non_zero value. Doing so may over-constrain the detail placement. As a result, it is easier for detail placement to fail in such a situation. So please use this constraint cautiously.

WHAT_NEXT

If the legalization fails with this constraint, users need to relax the constraint and try again.

PSYN-890 (Information) cell %s is not on a legal location at the beginning of Same_Row_ECO!

DESCRIPTION

This message indicates that one cell is illegal at the original location when ICC "Same_Row_ECO" is reading in the data. Idealy, ICC "Same_Row_ECO" legalization is expecting all cells are located at legal locations at the beginning. However, ICC "Same_Row_ECO" will try its best to legalize it during "Same_Row_ECO".

WHAT_NEXT

Once this error message shows up, the users need to check their design data. If this is a user error, users need to run a "normal-mode" legalization before they run this "same_row_eco".

PSYN-891 (Warning) cell %s (%.3f %.3f) inside row %s (%.3f %.3f %.3f %.3f)(sub_row: %d %d) is not on a legal location after Same_Row_ECO!

DESCRIPTION

This message indicates that one cell can not be legalized by ICC "Same_Row_ECO".

WHAT_NEXT

Once this error message shows up, the users need to check their design data. One potential reason is: this row may be overcapacity, so there may be no way for "Same_Row_ECO" to finish its work. Also, this violation may be due to other reasons. If this is a user error, users need to run a "normal-mode" legalization before they run this "same_row_eco". Also, users need to make sure that there is enough space to accommodate all the cells within this row before they run ICC "Same_ROW_CEO".

PSYN-892 (Information) User "porosity_control" has been disabled in Same_Row_ECO!

DESCRIPTION

This message indicates that ICC Same_Row_ECO has detected that user "porosity_control" is ON. In "Same_Row_ECO" legalization, user "porosity_control" is not recommended. As a result, ICC "Same_Row_ECO" will disable the user "porosity_control" automatically.

WHAT_NEXT

Once this error message shows up, the users need to check whether the user "porosity_control" is really needed in "Same_Row_ECO". In ICC "Same_Row_ECO", there should not be any user "porosity_control".

PSYN-893 (Error) cell %s {%.3f %.3f} has "single-site-gap"

violation!

DESCRIPTION

This message indicates that the cell has a "single-site-gap" violation: this cell is neighboring with a "single-site-gap".

WHAT_NEXT

Once this error message shows up, if users want to fix such kind of "single-site-gap" violations, they can run detail placement to fix them, with the below variable being set to a non_zero value: set legalize_skip_site_gap n

n is an integer which is greater than 0.

PSYN-895 (warning) With preferred routing direction on poly layer doesn’t make poly layer routable.

DESCRIPTION

This warning message occurs when set prefferred routing direction on poly layer. This doesn’t mean poly layer is a routing layer.

WHAT NEXT

This is only a warning message. Use set_preferred_routing_direction command to set a user defined direction for a layer in the design(CEL). To remove a user defined direction & defult to using the library defined direction, use remove_preferred_routing_direction command.

SEE ALSO

remove_preferred_routing_direction
report_preferred_routing_direction

PSYN-896 (Error) Cell %s does not have a location!

DESCRIPTION

This warning message occurs when command connect_dft_eco finds that a new scan cell

does not have a location. If a new scan cell does not have a location, then this cell will not be added into the existing scan chain.

WHAT NEXT

The cell must have been assigned a location before it is being added into a scan chain using command connect_dft_eco.

SEE ALSO

connect_dft_eco

PSYN-897 (Error) Can’t find SCAN-IN/SCAN-OUT pins for cell %s!

DESCRIPTION

This error message occurs when command connect_dft_eco can not find the corresponding "SCAN-IN" and/or "SCAN-OUT" pins for this specific cell. Basically, this will happen if users try to add this cell into a scan chain, but command connect_dft_eco can not find the corresponding "SCAN-IN" and/or "SCAN-OUT" pins.

WHAT NEXT

When a cell is being added into a scan chain, it is required that connect_dft_eco command find its "SCAN-IN" and "SCAN-OUT" pins. Such information is either located inside the logical library, or can be set by using command "set_dft_eco_options".

SEE ALSO

connect_dft_eco
set_dft_eco_options

PSYN-898 (Error) cell %s can not be added into chain %s

because it is already inside this scan chain!

DESCRIPTION

This error message occurs when command connect_dft_eco can not add a cell into a scan chain because this cell is already inside this chain, a cell can not be added into a chain twice. This belongs to user error.

WHAT NEXT

No need to add this cell because it is already inside the current scan chain.

SEE ALSO

connect_dft_eco
set_dft_eco_options

PSYN-900 (Warning) Cell %s is of type padFiller, CornerPad, flipChip or Tap cellbut do not have location.

SH DESCRIPTION This error occurs there are some specific types of physical only cells are there in design but they are not having location. Tool can not derive is_fixed attribute on these cells because they do not have location.

WHAT NEXT

Use set_cell_location OR move_object to put proper location on these cells.

SEE ALSO

PSYN-909 (Warning) Obsolete Command. It will be removed in future version of the tool.

SH DESCRIPTION This error occurs when user is using a command which is not officially supported command for the current release. There are following possibilites Command is going to be EoL’ed in later versions and currently hidden. Command is not production ready yet and hidden. Internal hidden command and not meant for customer usage.

WHAT NEXT

Contact your Synopsys representative and get clarity on alternatives.

SEE ALSO

PSYN-941 (Error) Cannot add new cellInst %s.

SH DESCRIPTION This error occurs while writing a new cell into milkway cell view if the cell instance in dc can not be created in milky way.

WHAT NEXT

SEE ALSO

PSYN-942 (Error) No objects specified to the command get_bounding_box.

DESCRIPTION

This error occurs when no object(s) specified in the command get_bounding_box. The command will not be executed.

WHAT_NEXT

At least one object has to be specified to execute the command.

PSYN-943 (warning) Deprecated command.

DESCRIPTION

You are getting this error because it is deprecated command.Use only the officially supported command.

WHAT NEXT

Instead of the above command which you used, use the other officially supported command and rerun.

PSYN-945 (Error) threshold/bound need(s) exactly one of following -max_transition, -max_capacitance, -max_fanout.

SH DESCRIPTION If threshold and bound options are specified, then exactly one among "max_trans","max_cap", and "max_fanout" must be specified. Otherwise this error will show.

WHAT NEXT

SEE ALSO

PSYN-946 (Error) Only the lowest metal layer is allowed to this command.

SH DESCRIPTION This error occurs when there are more than one layer to the set wiring keepout options command.

WHAT NEXT

SEE ALSO

ui_set_wiring_keepout_options_cmd_incr(2)

PSYN-947 (Error) Cannot find the layer in the library.

SH DESCRIPTION This error occurs if the layer can not be found in the library.

WHAT NEXT

Specify the correct layer.

SEE ALSO

PSYN-948 (Error) The name of the lowest metal layer doesn‘t match with the given name.

SH DESCRIPTION This error occurs when the lowest metal layer doesnot match with the given name.

WHAT NEXT

Give the correct metal layer name.

SEE ALSO

ui_set_wiring_keepout_options_cmd_incr(2)

PSYN-949 (Error) Design doesn’t have even two horizontal or vertical rows.

SH DESCRIPTION This error occurs if the design does not have even two horizontal or vertical rows.

WHAT NEXT

SEE ALSO

PSYN-950 (warning) Unmapped cell %s is ignored to set location.

DESCRIPTION

You receive this warning message because it is illegal to set location for unmapped cells.

WHAT NEXT

SEE ALSO

set_cell_location (2), **extract_physical_constraints** (2),

PSYN-951 (Error) Hierarchical cell %s is not an ICC or DCT ILM or a DCT physical hierarchy. No location will be set on it.

DESCRIPTION

You receive this error message because for a hierarchical cell to have a fixed

location from set_cell_location, it must be an ICC or DCT ILM or a DCT physical hierarchy.

WHAT NEXT

To have the location set on the hier cell, please provide a DCT physical hierarchy, or an ICC or DCT ILM netlist for it.

SEE ALSO

set_cell_location (2), **extract_physical_constraints** (2), **set_physical_hierarchy** (2), **create_ilm** (2)

PSYN-952 (error) Hierarchical cell %s is not an ILM or Design Compiler topographical placed physical hierarchy; keepout and placement propagation failed.

DESCRIPTION

This error message occurs because in order to propagate a hierarchical cell's keepout and placement, the cell must be an ILM or Design Compiler topographical placed physical hierarchy.

WHAT NEXT

Use the **set_physical_hierarchy** command to set the cell as a physical hierarchy, or provide an ILM netlist.

SEE ALSO

set_physical_hierarchy(2)

PSYN-953 (Information) Hierarchical cell %s is not set as physical hierarchy prior to set_cell_location. The cell will be set as physical hierarchy as part of set_cell_location command.

DESCRIPTION

You receive this information message because setting location on a hierarchical cell that is not an ICC or DCT ILM makes the cell a physical hierarchy automatically. A physical hierarchy is dont_touch by default.

SEE ALSO

set_cell_location (2), **extract_physical_constraints** (2), **set_physical_hierarchy** (2)

PSYN-954 (information) The bound %s will be created during compile.

DESCRIPTION

This information message advises you that the **create_bounds** command has just recorded a bound with the specified name, and the real bound will be created during compile. Design Compiler topographical technology delays the creation of a bound after a netlist is mapped during compile. The delay is necessary to ensure the bound has correct cells.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

create_bounds(2)
remove_bounds(2)
report_bounds(2)
update_bounds(2)

PSYN-955 (Warning) Option root_coord ignored in command get_bounding_box.

DESCRIPTION

Command get_bounding_box ignores the root_coord option. If you specify this option in this command, this messages warns you that this option will be ignored and boudning box returned by this command will have absolute value in its llx lly urx ury.

WHAT_NEXT

If you are using the output of this command to some other command, and if you need relative value of this boudning box, you need to add root coordinate of your core area to this boudning box.

PSYN-956 (warning) Report all physical cells include non filler physical cells.

DESCRIPTION

If library cell type OR filler cells instances regexp not specified in this command, this command will report all the physical only cells of the design, which include non-filler cells also.

WHAT NEXT

Specify the proper library cell for filler cells OR filler cell regexp to report filler cells.

SEE ALSO

all_physical_only_cells

PSYN-957 (Error) %s is not a valid magnet object.

DESCRIPTION

This error occurs when the port information of the magnet object is not valid for place all magnets commands.

WHAT NEXT

Specify the correct information.

SEE ALSO

PSYN-958 (error) No valid link library specified, please check library setup.

DESCRIPTION

This error comes when there is no valid link library specified to link reference libraries and logical libraries.

WHAT NEXT

Please check the library setup.

SEE ALSO

PSYN-959 (Error) Invalid name type for illegality checkings.

DESCRIPTION

This warning shows that a valid -name option is not specified to this command get_illegal_cell_collection. User has to enter one of the following, cells_not_on_row,cells_overlap,blocks_overlap,orientation_violations,site_violations, power_strap_violation etc.

WHAT NEXT

Specify the correct option and rerun this command.

PSYN-960 (error) Create_keepout_area command is renamed to set_keepout_margin. Please use set_keepout_margin instead.

DESCRIPTION

This error comes when the command create_keepout_area is used create keepout. This command renamed to to set_keepout_margin.So,instead of the previous command use set_keepout_margin.

WHAT NEXT

Specify set_keepout_margin command in place of create_keepout_area.

PSYN-961 (Error) All four horizontal and vertical resistance and capacitance units are not specified.

DESCRIPTION

This error occurs when all the four horizontal and vertical resistance and

capacitance units are not specified. Thenames of these units are horizontal minimum capacitance, vertical minimum capacitance, horizontal minimum resistance and vertical minimum resistance.

WHAT NEXT

Specify all these four units correctly and run the command again.

PSYN-962 (error) All four horizontal and vertical resistance and capacitance units are not specified.

DESCRIPTION

This error occurs when all the four horizontal and vertical resistance and capacitance units are not specified. The names of these units are horizontal maximum capacitance, vertical maximum capacitance, horizontal maximum resistance and vertical maximum resistance.

WHAT NEXT

Specify all these four units correctly and rerun the command.

SEE ALSO

PSYN-963 (error) No objects specified to get_location.

DESCRIPTION

Error occurs if no objects are specified for get_location_cmd.

WHAT NEXT

SEE ALSO

PSYN-964 (error) Routing rule "%s" not found.

DESCRIPTION

This error occurs when valid routing rule is not found.

WHAT NEXT

Specify the correct routing rule and rerun this command.

PSYN-965 (Error) Could not create region %s .Failed in region boundary continuity check.

DESCRIPTION

This error occurs when user is specified non-continuous boundary in the command create_region.

WHAT NEXT

Specify the continuous boudnary for the command and rerun this command.

SEE ALSO

create_voltage_area(2)

PSYN-966 (Warning). Obsolete options used in the command create_region.

DESCRIPTION

This error comes when obsolete options like -anchor, -utilization, -cut, -aspect_ratio, -edge_anchor and -end_points are specified to the command create_region. These options are not supported by this command anymore and results will be unpredictable.

WHAT NEXT

Do not use these options.

SEE ALSO

create_voltage_area(2)

PSYN-967 (Error) %s is not a valid magnet object.

DESCRIPTION

This error occurs when the magnet object is not a valid magnet object under conditions like when the cell is not in ILM mode.

WHAT NEXT

SEE ALSO

PSYN-968 (Warning) Voltage area %s with guard band margins x=%g and y=%g is overlapping with the neighbouring voltage areas.

DESCRIPTION

This error occurs when user specifies a guard band margin to a voltage area such that it starts overlapping with neighbouring voltage areas.

WHAT NEXT

Either reduce the guard band margin OR re-create the voltage area with proper size so that overlapping can be avoided.

PSYN-969 (Error) Unable to update guard-band value of the VA in in-memory Milkyway database.

DESCRIPTION

This error occurs when tool is unable to update the value of the guard band in the in-memory milkyway CEL.

WHAT NEXT

Ensure all the parameters are correctly specified during VA creation. MW CEL is correctly opened and no errors are there while opening the MW CEL.

PSYN-970 (warning) More than one operating conditions are defined for one hier cell instance.

DESCRIPTION

This error occurs when more than one min or max or normal operating conditions associated with a hier cell instance.

WHAT NEXT

Ensure only one operating condition is defined for one hier cell instance for each min/max/normal type.

PSYN-971 (Warning) Voltage area %s with guard band margins is overlapping with the neighbouring voltage areas.

DESCRIPTION

This error occurs when user specifies a guard band margin to a voltage area such that it starts overlapping with neighbouring voltage areas.

WHAT NEXT

Either reduce the guard band margin OR re-create the voltage area with proper size so that overlapping can be avoided.

PSYN-972 (error) report_congestion failed because some cells are placement illegalized.

DESCRIPTION

This error message occurs when some cells are placement illegalized in the design before call of report_congestion.

WHAT_NEXT

Use the **legalize_placement** command to make the placement legal, and then use **check_legality** command to check the placement legality.

legalize_placement (2), **check_legality** (2).

PSYN-973 (Error) %s is not set.

DESCRIPTION

This error occurs when the varaible from the user environment does not exist.

WHAT NEXT

SEE ALSO

PSYN-974 (Warning) An attribute with this name is already exposed.

DESCRIPTION

This error occurs when you try to expose an attribute which is already exposed.

WHAT NEXT

SEE ALSO

PSYN-975 (Error) Failed to create region %s.

DESCRIPTION

This error occurs when create region command could not create region for a logical block due to geometry check failures like when the region is not continuous or it is with disjoint rectangles or overlapping with existing regions.

WHAT NEXT

Please check the library setup.

SEE ALSO

PSYN-976 (Error) could not add cell %s to dpi.

DESCRIPTION

This error occurs when the cell could not be placed in a clean area.It may not be placed if the cell already exists or if it is not a standard cell.

WHAT NEXT

Check whether if it is not a standard cell or if it already exists.

SEE ALSO

PSYN-977 (Error) -critical_cells_only option is being used but there are no critical cells in the design.

DESCRIPTION

This error occurs when critical cells only option is used and also there are no critical cells.

WHAT NEXT

When there are no critical cells, do not use the critical cells only option.

SEE ALSO

PSYN-978 (Warning) There is no path between the specified magent and endpoints.

DESCRIPTION

This error occurs when set of eligible cells that lie on a path from startpoint to endpoint can not be generated.So,normal magnet placement will be done.

WHAT NEXT

SEE ALSO

PSYN-979 (Warning) Moving a fixed cell because -move_fixed specified.

DESCRIPTION

This warning occurs when a fixed cell is moved because move_fixed is specified.

WHAT NEXT

SEE ALSO

PSYN-980 (Warning) Moving a soft fixed cell because -move_soft_fixed specified.

DESCRIPTION

This warning occurs when a soft fixed cell is moved because move_soft_fixed is specified.

WHAT NEXT

SEE ALSO

PSYN-981 (Error) Unrecognized object class %s.

DESCRIPTION

This error occurs when the object class used is not an existing one.

WHAT NEXT

Specify the correct object name and rerun the command.

SEE ALSO

PSYN-982 (Error) Unrecognized object class %s.

DESCRIPTION

This error occurs when the object class used is not an existing one.

WHAT NEXT

Specify the correct object name and rerun the command.

SEE ALSO

PSYN-983 (Error) -class is required for -source option.

DESCRIPTION

The -class is required for -source option when trying to find an attributei using find attribute command.

WHAT NEXT

SEE ALSO

PSYN-984 (Error) attribute %s is not found.

DESCRIPTION

This error occurs when the attribute is not found in the attribute table.

WHAT NEXT

Specify the correct attribute name.

SEE ALSO

PSYN-985 (Error)attribute name %s is already in use.

DESCRIPTION

This error occurs when you are trying touse an attribute which is aleady in use.

WHAT NEXT

Use new attribute.

SEE ALSO

PSYN-986 (Error) Attempt to alias non-existent attribute %s.

DESCRIPTION

This error occurs when the attribute does not exist in the attribute table and the alias for the attribute can not be created.

WHAT NEXT

Use existing attributes.

SEE ALSO

PSYN-987 (Error) no voltage_area specified for report.

DESCRIPTION

While trying to execute report voltage area command if the voltage area is not specified, this error occurs.

WHAT NEXT

Specify voltage area and rerun the command.

SEE ALSO

PSYN-988 (Error) not able to get extra port instance master data.

DESCRIPTION

This error occurs when extra port instance master data is unable to get when object is deleted or object id is in invalid format.

WHAT NEXT

SEE ALSO

PSYN-989 (Error) could not get cell of this internal pin %s.

DESCRIPTION

This error occurs when the internla pin of a cell can not be obtained while translateing an object for DC to XCLS.

WHAT NEXT

SEE ALSO

PSYN-990 (Error) could not map hier MW port to flat port %d.

DESCRIPTION

This error occurs when hier MW port can not be mapped to flatport.

WHAT NEXT

Use existing attributes.

SEE ALSO

PSYN-991 (Error) Expected AX_HierPortinst_tld ori AX_Port_tld for MW id %d.

SH DESCRIPTION

WHAT NEXT

SEE ALSO

PSYN-992 (Error) Could not get type of MW id %d.

SH DESCRIPTION This error occurs when type of MW id can not be get.

WHAT NEXT

SEE ALSO

PSYN-993 (Error) could not get cel_inst from pin.

SH DESCRIPTION While translating an object from DC to XCLS, this error occurs when unable to get cell instance from pin.

WHAT NEXT

SEE ALSO

PSYN-994 (Warning) DC to MW translation failed - no CEL view open.

SH DESCRIPTION This warning occurs when either current status of design is not from MW or CEL view id is not open.

WHAT NEXT

SEE ALSO

PSYN-995 (Warning) ignored object with id %d.

```
SH DESCRIPTION This warning occurs when it fails to get the MW name of XCLS object.
```

WHAT NEXT

SEE ALSO

PSYN-996 (Error) Could not call dbGetObjType in xcls_a_port_box.

```
SH DESCRIPTION This error occurs when oject id is not found or deleted it could not
call get object type.
```

WHAT NEXT

SEE ALSO

PSYN-997 (Error) Could not axGetTypedObjData for port bbox.

```
SH DESCRIPTION
```

WHAT NEXT

SEE ALSO

```
ui_galileo_get_hier_cell_inst_of_hier_port_inst(2)
```

PSYN-998 (Error) cannot find the top cell instance.

```
SH DESCRIPTION This error occurs the topmost hier cell instance is unable to get.
```

WHAT NEXT

SEE ALSO

PSYN-999 (Error) can’t get bounding box of %s:%s.

SH DESCRIPTION This error occurs when bounding box can not be obtained for object or pin or design or wiring keepout.The error occurs if sufficeint core area is not found for design or the design is not found.

WHAT NEXT

SEE ALSO

PSYN-1000 (error) report_congestion fails to report GR congestion data.

DESCRIPTION

This error message occurs when report_congestion fails to read GR congestion data from MW.

WHAT_NEXT

SEE ALSO

PSYN-1001 (error) report_congestion fails due to no CEL associated with current design.

DESCRIPTION

This error message occurs when no CEL is associated with current design.

WHAT_NEXT

SEE ALSO

PSYN-1002 (warning) Skipping high-fanout net '%s' because %s.

DESCRIPTION

This warning message occurs when a net is being skipped as a high-fanout net. The possible reasons may be 1) The net is marked as don't touch; 2) The net is tristate net; 3) DRC checking is disabled on the net; 4) The net is constant net; 5) The net is ideal; 6) The net has multiple drivers; 7) Driver pin has no timing arcs; 8) The net is part of the clock network.

WHAT_NEXT

For multi-voltage designs, some net segments may be inferred as don't touch implicitly. You can set the variable "physopt_pccts_dont_touch_support" to true to allow AHFS to work on those nets.

SEE ALSO

PSYN-1003 (warning) '%s'.

DESCRIPTION

This message indicates user uses incorrect hfs mode or variable.

WHAT NEXT

To clarify the proper use of the physopt command you used, see the man page for the command.

PSYN-1004 (error) Invalid value %s for switch '%s'. Valid values

are %s.

DESCRIPTION

You receive this error because the value you specify for the given switch is not valid. Check **set_ahfs_options** man page for more information.

WHAT NEXT

Correct your input by using one of the valid values.

SEE_ALSO

set_ahfs_options(2)

PSYN-1005 (information) Pin %s is not bufferable for ILM preprocessing as net %s is %s

DESCRIPTION

This message is generated while preprocessing ILMs for high fanout synthesis. You will see this information messge a buffer can not be inserted in net.

The current preprocessing of ILMs does not insert buffers if the net is . an ideal . dont touch . three state bus . tristate . drc disabled . multiple driver . constant

WHAT NEXT

This is an informative message. No action requierd.

SEE ALSO

PSYN-1006 PSYN-1007

PSYN-1006 (information) Inserted buffer on net %s for isolating ILM pin %s.

DESCRIPTION

This message is generated while preprocessing ILMs for high fanout synthesis. You will see this information messge when the preprocessing step inserts a buffer to isolate the ILM pin.

WHAT NEXT

This is an informative message. No action requierd.

SEE ALSO

PSYN-1005 PSYN-1007

PSYN-1007 (error) No suitable buffer found for isolating %s pin.

DESCRIPTION

This message is generated while preprocessing ILMs for high fanout synthesis. You are seeing this message because preprocessing step was not able to find a suitable buffer in the library to isolate the ILM pin.

WHAT NEXT

Make sure that you have buffer definitions in the library and rerun the high fanout synthesis command.

SEE ALSO

PSYN-1005 PSYN-1006

PSYN-1008 (error) "get_congested_regions" fails to fetch Congested Map

DESCRIPTION

This error message occurs when required Congested Map is not available

WHAT_NEXT

Please run route_global or report_congetion to build global route congested map.Or run report_congestion -routing_stage detail / track to build detail / track stage congestion map.

SEE ALSO

PSYN-1009 (information) A %d row (%.2f micron) radius region centered at %.2f,%.2f
has a local density of %.1f%%

DESCRIPTION

This condition happens when a region of the block being placed has a local density of over 100%. It is only an informational message, and if the results of the placement run are acceptable, then nothing needs to be done.

However, if the legalization step seems to be causing timing degradations, it could be because of these local "hotspots".

WHAT NEXT

Results may improve if these local hot spots can be reduced. You can check the floorplan to see if the hotspots are floorplan related. You could also try turning on area recovery (or running error recovery on a higher effort) or even increasing the size of the core area.

PSYN-1010 (warning) Density is %.1f%%

DESCRIPTION

This message is printed when the density is high going into legalization. If the QOR is acceptable, nothing needs to be done about this. The legalizer can often handle high densities without serious problems.

However, if you are seeing timing degradations during legalization, you might get better QOR if you could reduce the density somewhat.

WHAT NEXT

If necessary, reduce density by either running area recovery at a higher effort, or increase the size of the core area.

PSYN-1011 (warning) Estimated density including spacing rules

is %.1f%%

DESCRIPTION

This message is printed when the density is high going into legalization. If the QOR is acceptable, nothing needs to be done about this. The legalizer can often handle high densities without serious problems.

The density number here is somewhat higher than the normal calculation for density because this calculation tries to estimate the amount of "forced" empty sites due to spacing rules.

If you are seeing timing degradations during legalization, you might get better QOR if you could reduce the density somewhat.

WHAT NEXT

If necessary, reduce density by either running area recovery at a higher effort, or increase the size of the core area.

PSYN-1012 (warning) There is high fragmentation caused by many blockages or fixed cells.
The median subrow width (space between blockages) is %d sites
and the median cell width is %d sites. This makes it difficult for the legalizer to pack in the cells and can result in high displacements and long runtimes.

DESCRIPTION

Typically, this message will be printed when there are a large number of fixed cells which fragment the rows and make it difficult for the legalizer to place the remaining cells.

WHAT NEXT

If the QOR is acceptable, then nothing needs to be done. However, if you are seeing poor QOR and if the timing degrades after legalization, then you can probably achieve better QOR by ensuring that fewer cells are fixed.

PSYN-1013 (warning) %.1f%% sites did not pass cell specific

legality checks.
If too many callbacks fail, legalization QOR may suffer.

DESCRIPTION

Various rules or conditions can make it illegal for cells to be placed in certain areas of the chip. For example, if there are preroutes (such as power straps), the location of the pins in a cell may make it illegal for a cell to be placed on some sites. If this happens too often, the legalizer may have difficulty legalizing the design.

WHAT NEXT

If you are not seeing QOR issues, or timing degradations after legalization, then there is nothing that you need to do. In general, the legalizer can handle these illegal sites without a significant degradation. However, if you suspect that legalization is causing timing problems, then you might achieve better if there were less "tricky areas" for the legalizer to deal with. For example, you could try making the power straps complete blockages.

PSYN-1014 (error) Legalizer timed out.

Generally this happens due to bad input that is likely to yield poor QOR anyway. However, if you would like to over-ride this limit,
please set the variable:
set legalizer_enable_timeout false

DESCRIPTION

When given a poor starting point, the legalizer can sometimes run for a very long time. In general, when this happens, legalization (as well as the following optimizations) can often run for a very long time, and will likely yield poor QOR. This error is an attempt to abort the command before a lot of CPU is wasted to achieve unacceptable results.

WHAT NEXT

If you think that this error can be ignored, you can bypass it by setting the variable legalizer_enable_timeout to true.

However, it is more likely that the source of the bad input needs to be fixed. Usually, this error is associated with large "hot spots" that contain over capacity regions, and the legalizer has a hard time spreading out all of the cells. If this

happens, you might consider increasing the core area of the block, or turning on higher effort area recovery.

PSYN-1015 (error) Fixed cell '%s' overlaps fixed cell '%s'.

DESCRIPTION

Fixed cells are not supposed to overlap each other.

WHAT NEXT

Modify the floorplan so the fixed cells are not overlapping each other.

PSYN-1016 (error) Aborting due to high local densities. Continuing is possible, but will likely result in long runtimes and poor QOR. Add the following command to over-ride this check and continue anyway: set legalizer_skip_overcapacity_check true

DESCRIPTION

In general, when this happens, legalization (as well as the following optimizations) can often run for a very long time, and will likely yield poor QOR. This error is an attempt to abort the command before a lot of CPU is wasted to achieve unacceptable results.

WHAT NEXT

If you think that this error can be ignored, you can bypass it by setting the variable legalizer_skip_overcapacity_check to true.

However, it is more likely that the source of the bad input needs to be fixed. Usually, this error is associated with large "hot spots" that contain over capacity regions, and the legalizer has a hard time spreading out all of the cells. If this happens, you might consider increasing the core area of the block, or turning on higher effort area recovery.

PSYN-1017 (warning) A %d row (%.2f micron) radius region centered at %.2f,%.2f
has a local density of %.1f%%

DESCRIPTION

This condition happens when a region of the block being placed has high local densities. This is a warning because the local densities are high enough that it is likely that QOR will not be acceptable.

However, if the legalization step seems to be causing timing degradations, it could be because of these local "hotspots".

WHAT NEXT

Results may improve if these local hot spots can be reduced. You can check the floorplan to see if the hotspots are floorplan related. You could also try turning on area recovery (or running error recovery on a higher effort) or even increasing the size of the core area.

There is also a chance that the overcapacity region is being caused by a flaw in the tool. If you think this might be the case, please contact Synopsys support.

PSYN-1018 (error) A %d row (%.2f micron) radius region centered at %.2f,%.2f
has a local density of %.1f%%

DESCRIPTION

This condition happens when a region of the block being placed has a high local density. An error is generated because the local densities are high enough that poor QOR will almost certainly result.

WHAT NEXT

You can check the floorplan to see if the hotspots are floorplan related. You could also try turning on area recovery (or running error recovery with a higher effort) or even increasing the size of the core area.

Another option would be to try running refine_placement on the over-capacity region to re-place the cells (make sure that you specify a region that is large enough to fit all of the cells).

If you believe that the results will be acceptable despite the local density issues, you can bypass the error by setting the variable legalizer_skip_overcapacity_check

to true.

There is also a chance that the overcapacity region is being caused by a flaw in the tool. If you think this might be the case, please contact Synopsys support.

PSYN-1019 (warning) There are %d scan chains with no PARTITION label which can result in lower QoR.

DESCRIPTION

This condition happens when there are scan chains with no PARTITION label. A warning is generated because scan cells in those chains cannot be re-parti- tioned across the chains, which may result in lower QoR.

WHAT NEXT

You can continue without the PARTITION labels and check the scan chain structure if QoR is low. If you need repartitioning, consider using your DFT-insertion tool to update the SCANDEF to include PARTITION labels.

PSYN-1020 (error) NO SCANCHAIN defined in SCANDEF.

DESCRIPTION

This message appears when there is no SCANDEF data loaded into the Milkyway Database. No physical DFT optimizations can be done without SCANDEF data.

WHAT NEXT

If you want to perform physical scan chain optimizations, you need to load SCANDEF by either read_def or by reading a .ddc with embedded SCANDEF. The SCANDEF data should be consistent with the netlist data to be loaded properly.

PSYN-1021 (error) there are %d components in the SCANDEF of the scan chain

DESCRIPTION

This error lists all components of specific scan chain exist in the SCANDEF, but do not exist in scan netlist.

WHAT NEXT

You need check your scan design flow and load correct SCANDEF file consistent with scan netlist.

PSYN-1022 (error) The pin %s is not connected.

DESCRIPTION

The error reports a specific floating scan in pin in the netlist, which is not connected to any other pin. The scan chain appears broken.

WHAT NEXT

Update the design without any floating pins along the scan path.

PSYN-1023 (error) the pin %s is connected to logic zero.

DESCRIPTION

The error reports a specific problematic scan in pin, which connect to logic zero. The scan chain appears broken.

WHAT NEXT

Update the design without any pins along the scan path tied off.You need check your scan design flow and scan netlist.

PSYN-1024 (error) the pin %s is connected to logic one.

DESCRIPTION

The error reports a specific problematic scan in pin, which connect to logic one. The scan chain appears broken.

WHAT NEXT

Update the design without any pins along the scan path tied off.

PSYN-1025 (error) could not find correspondence in the SCANDEF for netlist output pin %s.

DESCRIPTION

When tracing back on a scan chain, the tool reached a netlist pin for which there is no correspondence found in the SCANDEF. This indicates the SCANDEF data does not correspond to the netlist.

WHAT NEXT

Examine the design netlist to find the pin and its scan path load. Update the SCANDEF to ensure both pins exist and are specified to be in the same chain.

PSYN-1026 (warning) Ordered list checking failed in chain - %s. The connection before %s is inconsistent between the SCANDEF and the netlist.

DESCRIPTION

When the tool is doing backward tracing from CELL’s input pin, it cannot reach any of output pins in the SCANDEF. This could be caused by: 1) Inconsistent input pin of CELL specified in warning message. 2) Inconsistent output pin of the previous cell. 3) the previous cell is not specified in the SCANDEF. This inconsistency will not affect the DFT optimization, but the source of the inconsistency should be investigated.

WHAT NEXT

You need to check if there is any of the three violations and make a fix to ensure the SCANDEF is consistent with the netlist.

PSYN-1027 (warning) Ordered list checking failed in chain - %s. There are

DESCRIPTION

When an ordered list is checked, some scan cells specified in the SCANDEF are not found in the netlist accordingly.

This inconsistency will not affect the DFT optimization, but the source of the

inconsistency should be investigated.

WHAT NEXT

You need to check both the SCANDEF and netlist to make them consistent.

PSYN-1028 (warning) there are '%d' failed scan chains, and these scan chains will not be reordered.

DESCRIPTION

You receive this warning because there are some failed scan chains in the design. This scan chain data corruption prevents the chain order to be optimized.

WHAT NEXT

Use check_scan_chain to see which scan chains are not valid. Check your input SCANDEF file to correct the scan data corruption.

SEE ALSO

check_scan_chain (2).

PSYN-1029 (warning) Pin '%s' appears multiple times in the SCANDEF, in chain(s): %s

DESCRIPTION

The specified pin appears in several scan chains as shown. This is not allowed and all the releated chains are marked as FAILED.

WHAT NEXT

You need to update the SCANDEF with the true scan chains.

PSYN-1030 (warning) The scan chain %s has no scan element.

DESCRIPTION

There are not any scan elements in the specified chain. So the chain should be an invalid one.

WHAT NEXT

You need to update the SCANDEF with the true scan chains.

PSYN-1032 (Warning) Command %s option %s will soon become obsolete.

DESCRIPTION

You receive this warning because this command option is to be obsoleted in the next ICC release.

WHAT NEXT

Contact Synopsys representative regarding replacement command and options.

PSYN-1033 (Warning) Command %s will soon become obsolete.

DESCRIPTION

You receive this warning because this command is to be obsoleted in the next ICC release..

WHAT NEXT

Contact Synopsys representative regarding replacement command.

PSYN-1034 (warning) The pin '%s' of '%s' cell in technology library '%s' is signal pin, but it's Power/ground pin in the

reference library ’%s’.

DESCRIPTION

You see this warning due to the pin type mis-matchin in the technology library standard cell and reference library cell.

WHAT NEXT

There should be no PG pins in logical technology library standard cells, unless it’s the analog pin which the tool supports for analog macros.

check_library will report such issues for all standard and macro cells.

Double check your library for standard cells and clean them up.

SEE ALSO

check_library

read_lib (2).

PSYN-1035 (Error) Could not find congestion data for %s routing_stage.

DESCRIPTION

This error message occurs when report_congestion fails to read track / detail stage congestion data.

WHAT_NEXT

Rebuild congestion data using report_congestion -routing_stage track / detail

SEE ALSO

PSYN-1001 (error) get_congested_region fails due to no CEL

associated with current design.

DESCRIPTION

This error message occurs when no CEL is associated with current design.

WHAT_NEXT

SEE ALSO

PSYN-1038 (warning) A hard placement blockage may be needed to block thin channel {{%9.3f %9.3f} {%9.3f %9.3f}}.

DESCRIPTION

This warning message occurs when a thin channel is detected in this floorplan by the derive_placement_blockages command.

WHAT_NEXT

You are recommended to add a hard placement blockage at the suggested coordinates.

SEE ALSO

PSYN-1038 (warning) A soft placement blockage may be needed to block thin channel {{%9.3f %9.3f} {%9.3f %9.3f}}.

DESCRIPTION

This warning message occurs when a thin channel is detected in this floorplan by the derive_placement_blockages command.

WHAT_NEXT

You are recommended to add a soft placement blockage at the suggested coordinates.

SEE ALSO

PSYN-1040 (warning) The scan chain %s has no PARTITION label, in which the scan elements will not be repartitioned.

DESCRIPTION

This condition happens when the specified scan chain has no PARTITION label. A warning is generated because scan elements in the chain cannot be re-parti- tioned across the chains, which may result in lower QoR.

WHAT NEXT

You can continue without the PARTITION labels and check the scan chain structure if QoR is low. If you need repartitioning, consider using your DFT-insertion tool to update the SCANDEF to include PARTITION labels.

PSYN-1041 (warning) Warning: No plan groups are found in the design. Ignore the option ’-plan_group’

DESCRIPTION

This condition happens when the ’-plan_group’ is speccified for optimize_dft but the design does not contain plan groups. The ’-plan_group’ option is ignored.

WHAT NEXT

You need do nothing or just remove the ’-plan_group’ option.

PT-001 (fatal) %s is not enabled.

DESCRIPTION

The application tried to reserve the specified license, but it was not available.

WHAT NEXT

Verify that the key file is up to date and that sufficient licenses are available.

PT-002 (error) Unrecognized feature name '%s'.

DESCRIPTION

You tried to get or remove a license that does not exist in the key file.

WHAT NEXT

Verify that the key file is up to date and that the feature name is spelled correctly.

PT-003 (information) You already have a '%s' license.

DESCRIPTION

You tried to get a license that is already checked out.

WHAT NEXT

Verify that the feature name is spelled correctly in case it was a different feature that you wanted to get.

PT-004 (error) You don’t have a ’%s’ license to remove.

DESCRIPTION

You tried to remove a license that is not checked out.

WHAT NEXT

Verify that the feature name is spelled correctly in case it was a different feature that you wanted to remove.

PT-005 (error) Can’t remove your ’%s’ license: %s.

DESCRIPTION

You tried to remove a license that is locked by the application. For example, this might be the license that is required to launch the application, or the license might be required by a design that is in memory. The message will indicate the condition that triggered it.

WHAT NEXT

Action based on the message text.

PT-006 (error) %s is not supported on ’%s’ platform.

DESCRIPTION

This is an error message indicating the command or option is not supported on the specified platform.

WHAT NEXT

Please check the command manpage or product manuals for supported platforms. Make sure you run this command on the platforms that are supported.

PT-007 (warning) %s will be obsoleted and removed from future releases

of %s starting %s on %s platforms.

DESCRIPTION

This is a warning message indicating the specified command, option or variable is in the process of being obsoleted and will not be supported in future releases on the specified platform.

WHAT NEXT

Please check the command/variable manpages, product manuals or release notes for more details about the obsolescence, and whether there are alternative approaches or replacements for this feature being obsoleted.

PT-008 (error) %s has been obsoleted since %s release and is no longer supported on %s platforms.

DESCRIPTION

This is an error message indicating that the specified command, option or variable has been obsoleted and no longer supported on the specified platform.

WHAT NEXT

Please check the command/variable manpages, product manuals or release notes for more details about the obsolescence, and whether there are alternative approaches or replacements for this feature being obsleted.

PT-009 (warning) The BC_WC analysis mode will be phased out in future releases.

DESCRIPTION

The analysis mode you are setting, best case - worst case, is potentially inaccurate and should be avoided for sign-off. It will be obsoleted in a future release of PrimeTime.

For a thorough analysis, both setup and hold times should be checked at each corner of interest using the on_chip_variation analysis mode. In the BC_WC analysis mode, two corners are analyzed simultaneously. Hold times are checked at the fast (min) corner, and setup times are checked at the slow (max) corner. In the fast corner, fast slews are propagated along both the launch and capture sides of hold timing paths. As a result, worst-case slow timing cannot be guaranteed on the hold capture

paths. In the slow corner, slow slews are propagated along both the launch and capture sides of setup timing paths. Again, worst-case fast timing cannot be guaranteed on the setup capture paths. In addition, the BC_WC analysis is incomplete because setup times are not cross-checked in the fast corner, and hold times are not cross-checked in the slow corner.

WHAT NEXT

Migrate flows and scripts to avoid setting BC_WC analysis mode.

PT-010 (error) %s is not enabled.

DESCRIPTION

The application tried to reserve the specified license, but it was not available.

WHAT NEXT

Verify that the key file is up to date and that sufficient licenses are available.

PT-014 (information) Successfully checked out feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

PT-018 (n).

PT-015 (information) Started queuing for feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

PT-018 (n).

PT-016 (information) Still waiting for feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

PT-018 (n).

PT-017 (information) Timeout while waiting for feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE in pt_shell.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

PT-018 (n).

PT-018 (information) License queuing is enabled.

DESCRIPTION

You receive this message because you have enabled licensing queuing.

The license queuing is enabled by setenv SNPSLMD_QUEUE TRUE

When enabled the following timeouts can be adjusted:

Timeout for the initial license: setenv SNPS_MAX_WAITTIME <number of seconds>

Timeout for all subsequent licenses: setenv SNPS_MAX_QUEUETIME <number of seconds>

Defaults are equivalent to setenv SNPS_MAX_WAITTIME 259200 setenv SNPS_MAX_QUEUETIME 28800

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

PTE-001 (Error) There are no arcs from pin '%s' to pin '%s' on cell '%s'.

DESCRIPTION

This error occurs when any arc does not exist between the two pins specified by the -from option and the -to option of set_disable_timing or remove_disable_timing commands.

WHAT NEXT

Make sure the pins really exist on the cell or the libcell.

PTE-003 (warning) Some timing arcs have been disabled for breaking timing loops
 or because of constant propagation. Use the 'report_disable_timing'
 command to get the list of these disabled timing arcs.

DESCRIPTION

This message is displayed when timing arcs are disabled by tool to break combinational feedback loops or when propagating constant value due to case analysis. It is not displayed for arcs that are manually disabled with the **set_disable_timing** command.

WHAT NEXT

If you want to manually break a timing loop, examine the design to see why there is combinational feedback, then choose a different point at which to break the loop. To do this, use the **set_disable_timing** command instead of letting the tool automatically break the loop. To see details on the timing loops in the design, use **check_timing -inlcude loops -verbose**.

EXAMPLE MESSAGE

Warning: Some timing arcs have been disabled for breaking timing loops or because of constant propagation. Use the 'report_disable_timing' command to get the list of these disabled timing arcs. (PTE-003)

PTE-004 (error) The pin '%s', which is a generated clock pin, is either in a loop or is in the fanout of two clock sources.

DESCRIPTION

The generated clock pin is in a loop or is in the fanout of two clock sources. You cannot have loops in the clock network, nor can you have a generated clock in the fanout of two clock sources.

WHAT NEXT

If it is a loop, break the loop. If the generated clock is in the fanout of two clock sources, try to isolate it or use internal clocks instead.

PTE-005 (information) Invalidating all auto-disabled timing arcs.

DESCRIPTION

Some arcs have been enabled, forcing the tool to do loop detection from scratch. The tool therefore enables all auto-disabled arcs.

WHAT NEXT

To view all timing loops in your design, use **check_timing -loops**. To manually break the loops, use **disable_timing**.

PTE-006 (error) Cannot specify '%s' as the group name.

DESCRIPTION

Some path groups are internal and cannot be modified by you.

WHAT NEXT

Use **group_path** with a valid group name.

PTE-007 (warning) Attempting to remove a clock gating check

that was not previously set.

DESCRIPTION

Removal of clock gating check on an object is valid only if a clock gating check was set before on that object.

WHAT NEXT

This command will be ignored. Please check the spelling of the object for the **remove_clock_gating_check** command.

PTE-008 (error) No%s timing arc in cell '%s(%s)' from pin %s'%s' to pin '%s'.

DESCRIPTION

Some cell timing arcs specified in the SDF file cannot be found in the current design.

WHAT NEXT

Check if your SDF file is up-to-date with your design.

PTE-009 (warning) No %s arcs from pin '%s'.

DESCRIPTION

Delay annotation does not match netlist. The message is issued because some timing arcs specified in the SDF file, or by set_annotated_delay command cannot be found in the current design.

This can happen for example when SDF file was written for one design and applied with read_sdf to a different design.

The message is also issued if set_annotated_delay command is used to annotate timing arcs that do not exit. For example due to incorrect directions of ports, such as bidirectional pin u1/PAD being connected to a net with single input port IN. Then command set_annotated_delay -net -from u1/PAD 10.2 results in PTE-009 because arc u1/PAD to IN does not exits.

The message is automatically suppressed when annotating only delta delay.

WHAT NEXT

If the message occurs during read_sdf then check that your SDF file is up-to-date with your design. If the missing arc is due to false path (e.g., in the example above the path from u1/PAD to IN would never be functionally sensitized) then suppress the message.

SEE ALSO

read_sdf (2), **set_annotated_delay** (2), **suppress_message** (2), **si_enable_analysis** (3).

PTE-010 (error) No %s arcs to pin '%s'.

DESCRIPTION

Some timing arcs specified in the SDF file cannot be found in the current design.

WHAT NEXT

Check if your SDF file is up-to-date with your design.

PTE-011 (warning) No%s timing arc in cell '%s(%s)' with condition '%s' from pin %s'%s' to pin '%s'.

DESCRIPTION

Some timing arcs specified in the SDF file cannot be found in the current design.

WHAT NEXT

Check if your SDF file is up-to-date with your design.

PTE-012 (warning) A non-unate path in clock network detected. Propagating noninverting sense for clock '%s' to endpoints through pin '%s'.

DESCRIPTION

The clock tree for the specified clock contains non-unate paths. Clock networks

normally do not contain cells such as exclusive-OR gates which have non-unate behavior. This implies that both inverting and noninverting clock waveforms reach the specified pin. Since it is ambiguous PrimeTime always uses the noninverting sense of clock at clock pins down stream from these pins.

WHAT NEXT

If you want to analysis both the inverted and non_inverted clock from this point set the variable timing_non_unate_clock_compatibility to false. If you want to control the sense of the clock used through this pin, use the command 'set_clock_sense'.

PTE-013 (warning) Some clock relationships result in a common base period which require clock waveforms to be expanded more than 1000 times. PrimeTime limits clock waveforms expansion to be no more than 1000. Please check your clocks and apply set_false_path between unrelated clock domains.

DESCRIPTION

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime computes a base period (over all the clocks in the set).

If the large base period is due to the fact that clock periods do not divide evenly then PrimeTime tries to tweak the periods so that they divide evenly. Use **report_clock** to find out the exact clock period used. In any case, the PrimeTime restricts clock waveform expansion to no more than 1000.

Sometimes unexpected clock relationships due to automatically inferred clock-gating checks may cause a very large base period. You can disable clock-gating checks by setting the environment variable timing_disable_clock_gating_checks to "true".

WHAT NEXT

Use **set_false_path** to declare that timing paths between unrelated clocks are false.

PTE-014 (error) No net timing arc from pin '%s' to pin '%s'.

DESCRIPTION

There were no timing arcs between the specified pins. You received this error because the net timing arcs specified in the SDF cannot be found in the current design, or the entered command requires the existance of a timing net arc between the two pins.

WHAT NEXT

Check if both nets are connected to the same net. If the error is issued during reading of a SDF file, make sure that the SDF file is up-to-date with your design.

PTE-015 (error) Net delay from pin '%s' to pin '%s' cannot be annotated because of a timing assertion on hierarchical pin '%s'.

DESCRIPTION

When a timing assertion such as create_clock or a max_delay is specified on a hierachical pin, SDF annotation cannot be performed between the 'from_pin' and 'to_pin' of the net. This is because of the net segmentation performed on the hierarchical pin which is inbetween the 'from_pin' and 'to_pin'.

WHAT NEXT

It is recommened that you do not specify timing assertion on hierarchical pins.

PTE-016 (information) Expanding clock '%s' to base period of %.2f (old period was %.2f, added %d edges).

DESCRIPTION

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using

the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime computes a base period (over all the clocks in the set) and expands the clock waveforms to the base period.

WHAT NEXT

It is recommened that you mark paths between unrelated clocks as false.

PTE-017 (information) Inferring %d clock-gating checks.

DESCRIPTION

PrimeTime automatically checks setup and hold violations on gating inputs. This ensures that the clock signal is not interrupted or clipped by the gate. Disable clock gating checks by setting the variable timing_disable_clock_gating_checks to true.

WHAT NEXT

To disable automatic inferring of clock-gating checks, set the environment variable timing_disable_clock_gating_checks to true.

PTE-018 (information) Abandoning fast timing updates.

DESCRIPTION

PrimeTime has a built-in efficient algorithm to update the timing of a design, after it has been timed at least once, to accommodate a change that requires this update.

When the user makes a change that invalidates the timing of the design such as new assertions, exceptions, etc, PrimeTime automatically tries to do an incremental update_timing whenever a query is made that requires a timing update. When the number and severity of changes made since the last update is small, the incremental update provides over 10X runtime improvement over the initial timing update.

However, when those changes are large, the incremental update becomes inefficient. To ensure that the incremental update does not result in any slowdown, PrimeTime automatically switches to update from scratch a larger portion of the design than the portion immediately affected by the changes. This message informs the user of this switching. The incremental update remains faster than the update executed after an update_timing -full command.

PrimeTime provides the variable ’timing_update_effort’, which can be set to "low", "medium", and "high" to control the switch to full timing updates. It is unlikely that the user would need to change the default setting of the variable. See the

manual page for this variable for more information.

WHAT NEXT

Use 'set timing_update_effort low' if timing_update_effort is medium. Use 'set timing_update_effort medium' if timing_update_effort is high.

PTE-019 (error) report_delay_calculation is not enabled for library '%s'.

DESCRIPTION

The delay calculation report shows detailed performance information about library cells. By default, cell delay reporting is disabled. The technology library vendor can enable delay calculation for a library by specifying the following in the **.lib** source:

```
library_features(report_delay_calculation);
```

WHAT NEXT

Contact your library vendor to request a library with this feature enabled.

PTE-020 (error) The master clock %s has %d edges in a period. Cannot do frequency multiplication.

DESCRIPTION

If the master clock of a generated clock has more than 3 edges in a period, you cannot generate a frequency multiplied clock from that master clock.

WHAT NEXT

You can use -edges option to generate the clock.

PTE-021 (error) The generated clock '%s' is in the fanout of

clock
source %s.

DESCRIPTION

A generated clock can only be in the fanout of a clock source from which it is generated. Here the generated clock is found to be in the fanout of some other clock source.

WHAT NEXT

Generate this clock from a clock in whose fanout it is in.

PTE-022 (error) Generated clock '%s' is not in the fanout of its master clock.

DESCRIPTION

The generated clock is not in the fanout of the master clock with respect to which it has been defined. A generated clock must be in the fanout of its master clock.

WHAT NEXT

Please check the design and redefine the generated clock to be in the fanout of its master clock.

PTE-023 (warning) The generated clock '%s' has not been expanded,
please create or activate its master clock.

DESCRIPTION

A generated clock will not expand if the master clock from which it is generated has not been created or activated. Also if the master clock was given with a -master_clock but does not reach the pin given with -source, this message will be given.

WHAT NEXT

Please create or activate the master of the generated clock or change the -source

pin given. Use the **report_clock** command to see if the master clock is created or inactive.

SEE ALSO

create_clock(2), set_active_clocks(2), report_clock(2).

PTE-024 (error) The following generated clocks '%s' form a loop.

DESCRIPTION

The generated clock listed are defined in a loop. A loop of generated clocks is formed in that there is a circular dependency of generated clock to master clock.

For example, if A and B are generated clocks, and A is generated from B, and B is generated from A, there is a circular dependency.

WHAT NEXT

Remove cirular dependency in the generated clock sources.

PTE-025 (error) The master of the generated clock '%s' is not connected to any clock source.

DESCRIPTION

The master clock of a generated clock must be either a clock source, or must be connected to a clock source. If it is neither, it is an error.

WHAT NEXT

Make sure that the master source from which the clock is generated is a clock source or is connected to a clock source.

PTE-026 (information) Found %d generated clock master pins

that are not connected to clock sources.

DESCRIPTION

It gives a summary of the number of generated clock master pins that are not connected to clock sources.

WHAT NEXT

For a more detailed description of which generated clock master pins are not connected to any source, do check_timing -with -verbose option.

PTE-027 (information) Found %d loops in the generated clock network.

DESCRIPTION

This message gives a summary of the number of loops in the generated clock network. If there is a circular dependency of generated clock sources and its master, there will be a loop in the generated clock network.

WHAT NEXT

To get a more detailed description of where the generated clock loops are, use check_timing -verbose.

PTE-028 (warning) The variables timing_disable_bus_contention_check and timing_disable_floating_bus_check are both set to true. Reverting the setting of these variables to the default (false) value.

DESCRIPTION

It is a contradiction to set the variables timing_disable_bus_contention_check and timing_disable_floating_bus_check both to true. This is because setting the variable timing_disable_bus_contention_check implies that the user guarantees that on all multi-driven tri-state busses, disabling of the old drivers in the previous clock cycle is done before the enabling of the new drivers in the current clock cycle. This contradicts what is implied by setting the variable

timing_disable_floating_bus_check that enabling of the new drivers occurs before disabling of the old drivers. PrimeTime detects this contradiction and resets the value of the two variables to the default (false) value. In most cases, the user need not adjust these default values.

WHAT NEXT

Change your script to set both variables timing_disable_bus_contention_check and timing_disable_floating_bus_check to false, or to set only one of them to true.

PTE-030 (warning) No annotated %ss from '%s' to '%s'

DESCRIPTION

You attempted to remove an annotated delay or check between two pins and there was no annotation to remove.

WHAT NEXT

Verify that the -from and/or -to arguments in the command are correct.

PTE-031 (Warning) No annotated timing checks were removed

DESCRIPTION

The remove_annotated_check command did not find any checks to remove. If you did not limit the scope of the objects searched, then there are no checks in the design. If you did limit the search to a set of pins, cells, etc., then there are no checks on the objects which you specified.

WHAT NEXT

PTE-032 (Error) Cannot %s annotated check from '%s' to '%s':%s

DESCRIPTION

An attempt to set or remove an annotated check failed because the from and to pins specified are on different cells.

WHAT NEXT

Specify pins which are on the same cell.

PTE-033 (warning) Some related clocks cannot be expanded to a common clock period
within the expansion limit of 100 times per pair of related clock. The subject clocks are: %s, %s, ...

DESCRIPTION

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime computes a base period (over all the clocks in the set) and expands the clock waveforms to the base period.

The timing analysis when this warning is present can potentially miss some paths from being analyzed since some clock pulse relations would not be known.

If the large base period is due to the fact that clock periods do not divide evenly then PrimeTime tries to tweak the periods so that they divide evenly. Use **report_clock** to find out the exact clock period used. In any case, the PrimeTime restricts clock waveform expansion to no more than 100 times per pair clocks.

Sometimes unexpected clock relationships due to automatically inferred clock-gating checks may cause a very large base period. You can disable clock-gating checks by setting the environment variable timing_disable_clock_gating_checks to "true".

WHAT NEXT

Use **set_false_path** to declare that timing paths between unrelated clocks are false.

PTE-035 (warning) Dynamic loop breaking causes report_timing to
track a large number of paths; PrimeTime may run out of memory. Please consider manually breaking some loop paths before

issuing report_timing.

DESCRIPTION

You receive this message if the **timing_dynamic_loop_breaking** variable is set to *true* and your design contains a large number of loops, long paths in the loops, and many non-unate arcs in the path. In this case, the **report_timing** command could consume a large amount of memory, eventually causing PrimeTime to run out of memory.

WHAT NEXT

There are two potential solutions, as follows:

1. Manually break some long loops, then reexecute **report_timing**.

2. Reset the **timing_dynamic_loop_breaking** variable to *false* to return to static loop breaking mode, then reexecute **report_timing**. While in dynamic loop breaking mode, use **report_constraint -all_violators** to verify if there are more constraining paths than static loop breaking mode reports. **report_constraint -all_violators** consumes less memory and always works in dynamic loop breaking mode.

PTE-036 (warning) User specified '%s' in set_clock_gating_check command overwrites what the logic function of the cell or pin implies that clock gating check at pin '%s' should be against the '%s' of the clock.

DESCRIPTION

You receive this message if you execute **set_clock_gating_check** with the **-high** or **-low** option, and this specification is different from the PrimeTime inference based on the logic function of the cell. This message warns you that your current specification takes precedence over the PrimeTime inference.

WHAT NEXT

Verify that your specification of **-high** or **-low** is correct; the PrimeTime inference is usually accurate. If you are satisfied that your specification is correct, no action is required on your part. Otherwise, reexecute the **set_clock_gating_check** command and do not specify **-high** or **-low** so that the PrimeTime inference remains.

PTE-037 (information) Issuing set_operating_conditions for

setting analysis mode on_chip_variation.

DESCRIPTION

You receive this message when PrimeTime puts the design in on_chip_variation analysis mode during linking a design. PrimeTime issues a **set_operating_conditions** command with **-analysis_type on_chip_variation**, using best-case and worst-case operating conditions that are the same as the default operating condition in the main library.

WHAT NEXT

This is an informational message only; no action is required on your part.

PTE-038 (warning) Net "%s" has many driver/load combinations (%d); expect performance degradation.

DESCRIPTION

You receive this message if the **update_timing** command finds a net with a large number of driver/load combinations. This message warns you that PrimeTime could run out of memory, because creating net arcs for each driver/load pair is very memory-intensive. You should expect a performance degradation.

WHAT NEXT

PrimeTime can, under certain conditions, reduce the timing arcs in the net’s fanin to alleviate the problem. This can be achieved by setting timing_reduce_multi_drive_net_arcs to true. Please refer to the man page for timing_reduce_multi_drive_net_arcs(3) for more details.

PTE-039 (information) Issuing set_operating_conditions corresponding to timing_slew_propagation_mode setting.

DESCRIPTION

You receive this message when you set the **timing_slew_propagation_mode** variable to *worst_arrival* and have specified a single operating condition using **set_operating_conditions -analysis_type single**. PrimeTime cannot compute accurate transition time for hold timing paths if the analysis type is *single*. In this case, PrimeTime issues this message and executes a **set_operating_conditions** command with **-analysis_type on_chip_variation**, using best-case and worst-case operating conditions that are the same as the single operating condition under which you set the

variable.

Conversely, if you set the **timing_slew_propagation_mode** variable back to its default value of *worst_slew*, PrimeTime again issues this message and executes a **set_operating_conditions** command with **-analysis_type single**.

In both cases, PrimeTime echoes the exact command that was issued.

WHAT NEXT

This is an informational message only; no action is required on your part. However, you can avoid receiving this message by changing your script to use a **set_operating_conditions -analysis_type on_chip_variation** command with an appropriate operating condition.

PTE-040 (Warning) Source Latency defined on pin/port '%s' will overwrite the clock source latency for clock '%s' .

DESCRIPTION

You receive this message if clock source latency is defined for both a clock and its port (source pin). In this case, the source latency for the port takes precedence, because it is more specific.

WHAT NEXT

If it is acceptable to you for the source latency on the specified pin/port to overwrite the clock source latency, no action is required on your part. Otherwise, reexecute the **set_clock_latency** command with the required specifications.

PTE-041 (warning) Unable to find specified driving cell for port '%s':
expected %s/%s %s -> %s.

DESCRIPTION

The driving cell information for the specified port indicates that the port should inherit its drive capability from a certain library cell. This error indicates that the application was unable to locate a matching library cell, a pin on that library cell, or an arc between the pins. This might happen if the **link_path** variable does not contain the library for that cell, or if the cell name or pin name is incorrect. The driving cell information, set by the **set_driving_cell** command, is specified in the text of the message, and you can see it by using the **report_port** command with the **-drive** option.

WHAT NEXT

If the driving cell requires a library that has not been identified in the link path, the **link_path** variable should be changed to include that library. Otherwise, check the information for errors in the library name, library cell name, or library cell pin name.

SEE ALSO

report_port (2), **set_driving_cell** (2), **link_path** (3).

PTE-042 (warning) Conflicted logic driving pin %s, setting resolved logic value %s on pin %s.

DESCRIPTION

You receive this message because, during the propagation of case analysis or logic constants, update_timing detects two conflicting logic values propagated to a pin. (The update_timing may occur as a result of executing the **update_timing** command or other commands, such as **report_timing**.)

For example, if two strong drivers drive a net with one carrying case analysis **0** and the other carrying case analysis **1**, then a logic conflict would arise.

In these situations, **update_timing** resolves the logic conflict to **0** and continues propagating this forward in the design. The message warns you that a logic conflict has occurred at the specified pin and that it has been resolved to the specified logic value.

WHAT NEXT

The case analysis values that propagated to the pin in question should be changed to prevent the logic conflict from arising, if the resolved value propagated forward is unsuitable. To identify the case values causing the problem, perform the following steps:

1. Enable the generation of a case analysis propagation log file by setting the **case_analysis_log_file** variable to a filename of your choice.

2. Reexecute update_timing, and review the log file to determine the reason for the conflicting values.

3. Correct the problem and reexecute **update_timing**.

SEE ALSO

set_case_analysis (2), **report_timing** (2), **update_timing** (2), **case_analysis_log_file** (3).

PTE-044 (warning) In the data check from reference pin '%s' to constraint
pin '%s', multiple clocked signals arrive at the reference pin.
The signal driven by clock '%s' is selected by default. You can use
set_data_check -clock to select the clock.
timing_enable

DESCRIPTION

You receive this message during data checks performed by **update_timing**, if your design contains multiple clocks per register, the **timing_enable_multiple_clocks_per_reg** variable is set to false, and you did not specify a clock using **set_data_check -clock**. For these conditions, PrimeTime selects a random clock among all clocks that arrive at the reference pin, and issues this message.

PrimeTime supports multiple clocks when the **timing_enable_multiple_clocks_per_reg** variable is at its default setting of true. Normally, if your circuit contains more than one clocked signal that arrives at a reference pin, you should leave this variable at its default setting of true to analyze all clocks, or specify which clock you want to use with **set_data_check -clock**. You can use the **-clock** option even if you are using a library cell for the data check.

If only one clock arrives at the reference pin, you do not need to specify the clock.

WHAT NEXT

If it is acceptable to you for the specified clock to be used by default, no action is required on your part. Otherwise, verify that you intended for multiple clocked signals to arrive at the reference pin of the specified data check. If not, adjust your design accordingly.

If so, do one of the following:

• If you want all clocks to be analyzed simultaneously, set the **timing_enable_multiple_clocks_per_reg** variable to true.

• If you want to select one clock to be analyzed, use **set_data_check -clock** to select the clock to be used.

Finally, reexecute **update_timing**.

SEE ALSO

set_data_check (2), **update_timing** (2); **timing_enable_multiple_clocks_per_reg** (3).

PTE-045 (warning) The generated clock '%s' does not have a valid master clock because its master clock has been removed.

DESCRIPTION

When a generated clock is created using -add option , it's master clock must be specified using -master_clock option. But if at a later time, the master clock is deleted then the dependent generated clocks would not have a valid master.

WHAT NEXT

Please make sure if the deletion of master clock is really intended. If it was intended, define a master clock for the generated clock, otherwise the generated clock would not be expanded.

SEE ALSO

create_generated_clock (2)

PTE-046 (information) Reducing %d parallel drivers:
Reduction at net: '%s'
Reduced to timing arcs from cell: '%s'

DESCRIPTION

The parallel timing arcs through the specified net will be reduced to a single driver cell for timing analysis purposes. This optimization is triggered when the variable timing_reduce_multi_drive_net_arcs is set to true.

WHAT NEXT

Refer to the man pages of timing_reduce_multi_drive_net_arcs(3) and timing_reduce_multi_drive_net_arcs_threshold(3) for more details.

PTE-047 (information) Cannot reduce parallel timing arcs at net '%s'

which has %d drivers x loads
Reason: Driving cell %s%s%s

DESCRIPTION

Even though the net drivers-loads product exceeds the threshold value set in timing_reduce_multi_drive_net_arcs_threshold(3), the cells driving this net will not be reduced for the reason specified.

WHAT NEXT

For more details regarding the restrictions on clock network parallel buffers collapse, check the man pages for timing_reduce_multi_drive_net_arcs.

PTE-048 (information) No net arcs %s pin '%s' due to multi-drive timing arcs reduction

DESCRIPTION

The necessary timing arc to annotate does not exist because it was subject to parallel drivers reduction instigated by setting *timing_reduce_multi_drive_net_arcs* to true. Annotations specified as such will be ignored.

WHAT NEXT

For more details regarding reducing multi-drivers in the clock network, check the man pages for *timing_reduce_multi_drive_net_arcs*. These messages may be suppressed using the following command: "suppress_message PTE-048".

PTE-049 (warning) power rails of operating condition on port '%s' are incompatible with power rails of driving cell '%s'. Driving cell ignored.

DESCRIPTION

The power rails specified in the library of a driving cell must be a subset of those specified in the operating condition. Rails are matched by name, and the order of rails much also be identical.

WHAT NEXT

Consider another operating condition or driving cell.

SEE ALSO

report_port (2), **set_operating_condition** (2), **create_operating_condition** (2), **set_driving_cell** (2),

PTE-051 (warning) Using minimum CRP value due to mismatch in the launching and %s clock edges at the common point.

DESCRIPTION

You receive this message when you execute the **report_crpr** command. This message will occur for one of two reasons. One, the transition sense of the launching and capturing clocks at the common point differ. For example, a rising clock edge through the common point triggers the launching register and a falling clock edge through the common point triggers the capturing register. Two, the capturing register is a level-sensitive latch. In this case two CRP values will be calculated, one corresponding to the opening edge and one corresponding to the closing edge. This means that there will be a mismatch in one of these CRP values and the minimum CRP value will be used.

WHAT NEXT

For the case when the capturing device is a level-sensitive device the report should clearly indicate what edge is using the minimum CRP.

SEE ALSO

timing_remove_clock_reconvergence_pessimism (3), **report_crpr** (2).

PTE-052 (warning) For computing a common base period for a number of clocks

PrimeTime limits the waveform expansion of the smallest period to be no more than %d times and the waveform expansion of the largest period to be no more than %d times. Since the largest period is too large compared to the smallest period,

no common base period is possible satisfying these limits, and PrimeTime has taken the largest period as the common base period
but still has not expanded the smallest period beyond its limit.

DESCRIPTION

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime computes a base period (over all the clocks in the set).

PrimeTime must ensure that the common base period of a set of related clocks is evenly divisible by every clock in the set. Since clock periods can be arbitrary floating-point numbers, this may require some adjustments to the clock periods. Moreover, to prevent the common base period from becoming too large, PrimeTime must restrict clock waveform expansions by the limits mentioned in the warning message.

Therefore, three cases can occur while computing the common base period: (1) The largest clock period is so large compared to the smallest clock period that no common base period can be computed satisfying the limits. In this case, PrimeTime takes the largest clock period as the common base period but still does not expand the smallest period beyond its limit; (2) A common base period is computed but it has to be decreased to satisfy the limits; and (3) A common base period is computed and it already satisfies the limits. This warning message handles the first case.

Sometimes unexpected clock relationships due to automatically inferred clock-gating checks may cause a very large common base period. You can disable clock-gating checks by setting the environment variable timing_disable_clock_gating_checks to "true".

WHAT NEXT

Use **set_false_path** to declare that timing paths between unrelated clocks are false.

PTE-053 (warning) For computing a common base period for a number of clocks

PrimeTime limits the waveform expansion of the smallest period to be no more than %d times and the waveform expansion of the largest period to be no more than %d times.

PrimeTime has computed a common base period bounded by these limits.

DESCRIPTION

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime computes a base period (over all the clocks in the set).

PrimeTime must ensure that the common base period of a set of related clocks is evenly divisible by every clock in the set. Since clock periods can be arbitrary floating-point numbers, this may require some adjustments to the clock periods. Moreover, to prevent the common base period from becoming too large, PrimeTime must restrict clock waveform expansions by the limits mentioned in the warning message.

Therefore, three cases can occur while computing the common base period: (1) The largest clock period is so large compared to the smallest clock period that no common base period can be computed satisfying the limits. In this case, PrimeTime takes the largest clock period as the common base period but still does not expand the smallest period beyond its limit; (2) A common base period is computed but it has to be decreased to satisfy the limits; and (3) A common base period is computed and it already satisfies the limits. This warning message handles the second case.

Sometimes unexpected clock relationships due to automatically inferred clock-gating checks may cause a very large common base period. You can disable clock-gating checks by setting the environment variable timing_disable_clock_gating_checks to "true".

WHAT NEXT

Use **set_false_path** to declare that timing paths between unrelated clocks are false.

PTE-054 (Information) Zero transition time used at to pin of annotated arcs. Delays on not annotated delay arcs will be estimated using best available slew.

DESCRIPTION

This message is issued when more than 95 percent of delay arcs on a design have annotated values and **timing_use_zero_slew_for_annotated_arcs** is set to *auto*, or when **timing_use_zero_slew_for_annotated_arcs** has been set to **always. This functionality is intended for use only on a design that is completely (or almost completely) SDF annotated, and in a flow which does not require transition times.**

WHAT NEXT

See man page of **timing_use_zero_slew_for_annotated_arcs** for more details on this functionality.

PTE-055 (warning) Variable "%s" must be set before link

DESCRIPTION

The PrimeTime variable indicated can only be consumed before the design is linked. That is, the current change in value will only be honored the next time the link_design command is invoked.

WHAT NEXT

Please verify that the current setting is correct. If so, either invoke the link_design command or move the variable setting to a position prior to invoking the link_design command and rerun your script.

SEE ALSO

timing_propagate_through_unclocked_registers (3)

PTE-056 (Warning) Due to the value set by timing_crpr_threshold_ps, the CRP displayed in the timing_report will lie in the range: %g < CRP < %g.

DESCRIPTION

You receive this message when you execute the **report_crpr** command. In order to reduce the computational complexity of deriving a CRP value during update_timing, different compute mechanisme are utilized in the production of the CRP values for **report_timing** and **report_crpr**. This may result in a difference between the CRP values produced by report_timing and report_crpr. The difference will not be greater than the value of the variable, **timing_crpr_threshold** and will lie in the range: CRP(report_crpr)-threshold < CRP < CRP(report_crpr). Hence, the value of CRP used in report_timing, if different to report_crpr, will always be more pessimistic.

WHAT NEXT

If more accuracy is required in the CRP value issued by **report_timing** set the variable **timing_crpr_threshold_ps** to a lower value and execute a full **update_timing**. Setting the variable ftiming_crpr_threshold_ps to a low value will result in significantly increased runtime and memory usage.

SEE ALSO

report_crpr (2), **timing_remove_clock_reconvergence_pessimism** (3), **timing_crpr_threshold_ps** (3).

PTE-057 (Warning) Transition times on not annotated delay arcs have been set to zero. Cannot perform max_transition checking.

DESCRIPTION

This message issues if a zero value is used for transition time on the load pins of fully delay annotated arcs. For this reason, **report_constraint -max_transition** is disabled.

Fully annotated arcs are those with values for both rise and fall either read from an SDF file, or set with the command **set_annotated_delay**.

Zero transition times are used when more than 95 percent of delay arcs on a design have annotated values and the varibale **timing_use_zero_slew_for_annotated_arcs** is set to **auto**, or when **timing_use_zero_slew_for_annotated_arcs** is set to **always** (irrespective of the percentage of annotated delay arcs).

WHAT NEXT

See man page of **timing_use_zero_slew_for_annotated_arcs** for more details on this functionality. Setting this this variable to **never will re-enable calculation of slews, and max_transition constraint checking.**

PTE-058 (Warning) timing_use_zero_slew_for_annotated_arcs will be disabled when slew propagation mode is not *worst_slew*.

DESCRIPTION

The functionality enabled by **timing_use_zero_slew_for_annotated_arcs** is compatible only with *worst_slew* slew propagation and will not be invoked when **timing_slew_propagation_mode** is set to anything other than *worst_slew***.**

WHAT NEXT

See man page of **timing_use_zero_slew_for_annotated_arcs** for more details on this functionality.

PTE-059 (Error) timing_use_zero_slew_for_annotated_arcs cannot be enabled unless timing_slew_propagation_mode is worst_slew.

DESCRIPTION

The functionality enabled by **timing_use_zero_slew_for_annotated_arcs** is compatible only with **worst_slew B slew propagation mode.**

WHAT NEXT

Setting **timing_slew_propagation_mode to worst_slew** will allow **timing_use_zero_slew_for_anntoated_arcs** to be enabled. See man page of **timing_use_zero_slew_for_annotated_arcs** for more details on this functionality.

PTE-060 (warning) No clock-gating check is inferred for clock %s
at pins %s and %s of cell %s.

DESCRIPTION

Unless the variable **timing_disable_clock_gating_checks** is set to true, PrimeTime automatically infers clock-gating checks. For this cell, PrimeTime cannot infer a clock-gating check. This happens because the logic of this cell does not provide enough information to determine whether to perform a gating check on the high level or low level of the input clock signal.

WHAT NEXT

Use **set_clock_gating_check** with either the **-high** or **-low** option to specify the level of the clock.

PTE-061 (Warning) Since the launching device is a level-sensitive latch and the variable timing_early_launch_at_borrowing_latches is set to TRUE, the

CRP for any paths launched from the latch data pin will be zero.

DESCRIPTION

You receive this message when you execute the **report_crpr** command. Since the same (early) clock arrival time is used to both launch and capture data at a level-sensitive latch with borrow, normal application of CRPR may be optimistic. For this reason the CRP is set to zero for such paths. For more details see the man page for the variable **timing_early_launch_at_borrowing_latches**.

WHAT NEXT

In order to apply CRPR to paths launched from a borrowing data pin set the variable **timing_early_launch_at_borrowing_latches** to FALSE. This is recommended for PrimeTime to minimize the overall pessimism throughout a latch-based design.

SEE ALSO

report_crpr (2), **timing_remove_clock_reconvergence_pessimism** (3), **timing_early_launch_at_borrowing_latches** (3).

PTE-062 (information) Accepted db inherited disable timing arcs to break loops.

DESCRIPTION

Accepted db inherited disable timing arcs to break loops due to a true value of the variable **timing_keep_loop_breaking_disabled_arcs**. Variable **timing_keep_loop_breaking_disabled_arcs** is false by default.

There may still be loops in the design that the db inherited disabled timing arcs did not break, they are broken using the default loop breaking technique.

There is a difference between DC and PT where additional set_case_analysis and set_disable_timing commands will not remove db inheritied disabled timing arcs.

A boolean attribute **is_db_inherited_disabled** has been added to the class timing_arcs, where true indicates an arc is a db inherited disabled arc.

The command **remove_disable_timing** may be used to remove db inherited disabled timing arcs, since these arcs are considered to be under user control.

To remove all db inherited disable timing arcs for loop breaking, issue command **remove_disable_timing** [get_timing_arcs -of [get_cell *] -filter "is_db_inherited_disabled == true"]

SEE ALSO

report_disable_timing (2), **timing_keep_loop_breaking_disabled_arcs** (3).

PTE-063 (warning) Resetting value of variable timing_keep_loop_breaking_disabled_arcs will have no effect.

DESCRIPTION

Resetting value of variable **timing_keep_loop_breaking_disabled_arcs** will have no effect after accepting db inherited disable timing arcs to break loops. This value of this variable is only checked during linking.

If the user wishes to remove the db inherited disable timing arcs, issue command **remove_disable_timing** [get_timing_arcs -of [get_cell *] -filter "is_db_inherited_disabled == true"]

SEE ALSO

report_disable_timing (2), **timing_keep_loop_breaking_disabled_arcs** (3).

PTE-064 (information) Related clock set %d includes clock '%s' with period %.2f.

DESCRIPTION

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime assigns an integer identification number and computes a base period (over all the clocks in the set). This message says that this clock is a member of this clock set.

WHAT NEXT

It is recommened that you mark paths between unrelated clocks as false.

SEE ALSO

set_clock_groups (2), **set_false_path** (2).

PTE-065 (information) Related clock set %d has base period %.2f.

DESCRIPTION

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime assigns an integer identification number and computes a base period (over all the clocks in the set). This message shows the base period of this clock set.

WHAT NEXT

It is recommened that you mark paths between unrelated clocks as false.

SEE ALSO

set_clock_groups (2), **set_false_path** (2).

PTE-066 (Warning) Zero transition time will be used at to pins of annotated arcs since more than 95 percent of delay arcs are annotated. Delays on not annotated delay arcs will be estimated using best available slew.

DESCRIPTION

If more than 95 percent of delay arcs on a design have annotated values, the SDF flow is automatically switched on during the timing update or during the execution of **report_annotated_delay**. Note that issuing **read_sdf** with the **-verbose** option will implicitly call **report_annotated_delay**. Switching on of the SDF flow will result in faster performance of update_timing, at the expense of no longer calculating the slews on the load pins of annotated arcs.

This functionality is intended for use on a design that is completely (or almost completely) SDF annotated, and in a flow which does not require transition times.

WHAT NEXT

See man page of **timing_use_zero_slew_for_annotated_arcs** for more details on this functionality.

To avoid the SDF flow being automatically switched on, set **timing_use_zero_slew_for_annotated_arcs** to *never*.

PTE-067 (warning) Setting this variable to a lower value can cause a significant performance degradation during a timing update.

DESCRIPTION

You receive this message when setting the variable **timing_crpr_threshold_ps**. Turning CRPR on can cause a noticable performance degradation both in terms of CPU and capacity. Further to this, setting the variable to values lower than the default (20ps) can further degrade performance with little corresponding increase in the accuracy of the CRP calculation. See the man page for **timing_crpr_threshold_ps** for more details.

WHAT NEXT

The recommended setting for the variable **timing_crpr_threshold_ps** is about one half of the stage (gate plus net) delay of a typical stage in the clock network.

PTE-068 (information) Using CRPR on a pre-layout clock network can cause performance degradation during a timing update.

DESCRIPTION

You receive this message during a timing update. The CRPR algorithm is optimized for post layout clock networks. Because of this fact it is not recommended to use this algorithm on a pre-layout (pre-clock tree synthesis) clock network as it can lead to degradation in both CPU performance and in capacity.

WHAT NEXT

In order to alleviate performance concerns turn CRPR off by setting the variable **timing_remove_clock_reconvergence_pessimism** to false.

SEE ALSO

timing_remove_clock_reconvergence_pessimism (3).

PTE-069 (error) The requested clock sense at pin '%s' for clock '%s' does not exist. Propagating the '%s' sense of the clock through this pin.

DESCRIPTION

There is a 'set_clock_sense' directive at the pin given and the requested clock sense does not exist at the pin for the given clock. This may be due to a conflicting 'set_clock_sense' directive on a previous pin or it may be because the only clock paths to that pin are not of the sense requested.

WHAT NEXT

Remove the conflicting 'set_clock_sense' directives.

PTE-070 (information) A non-unate path in clock network detected. Propagating both inverting and noninverting senses of clock '%s' from pin '%s'.

DESCRIPTION

The clock tree for the specified clock contains non-unate paths. Clock networks normally do not contain cells such as exclusive-OR gates which have non-unate behavior. This implies that both inverting and noninverting clock waveforms reach the specified pin. This is an informational message that such a pin has been detected and that PrimeTime is propagating both senses of clock.

WHAT NEXT

If you want to control the sense of the clock used through this pin, use the command 'set_clock_sense'.

PTE-071 (warning) The '%s' edge of clock '%s' through pin '%s' causes the clock to both rise and fall.

A generated clock is needed at this pin.

DESCRIPTION

The clock tree for the specified clock contains two half unate paths such that the clock edge given causes both a rising and falling clock edges and the other edge of clock causes no change. This type of edge relationship requires that a generated clock be added. In the 'create_generated_clock' command, use of non-monitomic edges such as (1 1 3) or (2 2 4).

WHAT NEXT

Place a generated clock at the given pin.

PTE-072 (Warning) SI analysis is not enabled, therefore the adaptive CRPR engine will not be used.

DESCRIPTION

You receive this message during a timing update if the variable **timing_crpr_enable_adaptive_engine** is set to TRUE and SI analysis is turned off (**si_enable_analysis**). The adaptive CRPR engine applicable only when SI is turned on therefore will have no effect on the non-SI timing update.

See the man page for **timing_crpr_enable_adaptive_engine** for more details.

WHAT NEXT

If the users intention is to perform an SI analysis then set the variable **si_enable_analysis** to TRUE. Otherwise turn off the adaptive CRPR engine by setting **timing_crpr_enable_adaptive_engine** to FALSE.

SEE ALSO

timing_crpr_enable_adaptive_engine (3), **timing_remove_clock_reconvergence_pessimism** (3).

PTE-073 (Warning) Turning off Adaptive CRPR.

DESCRIPTION

You receive this message during a timing update if the variable **timing_crpr_enable_adaptive_engine** is set to TRUE and either the max SI iteration

count (set by **si_xtalk_exit_on_max_iteration_count**) or the max SI incremental iteration count (set by **si_xtalk_exit_on_max_iteration_count_incr**) is set to 1.

The adaptive CRPR engine requires at least two SI iterations to perform its analysis. Because of this the adaptive engine is turned off and standard CRPR analysis is performed.

See the man page for **timing_crpr_enable_adaptive_engine** for more details.

WHAT NEXT

Set the variable **si_xtalk_exit_on_max_iteration_count** to at least 2 and repeat the timing update.

SEE ALSO

si_xtalk_exit_on_max_iteration_count (3) **timing_crpr_enable_adaptive_engine** (3), **timing_remove_clock_reconvergence_pessimism** (3).

PTE-074 (warning) At pin '%s' clock '%s' does not have the needed %s edge.

DESCRIPTION

The clock tree contains half unate timing arcs or disable timing commands that have disabled the needed rise or fall edge. The register clock pin given will not have the clock assigned to it and will not be timed.

WHAT NEXT

Alter clock network to propagate the needed clock edge to this register.

PTE-075 (warning) Generated clock '%s' has no path to its master clock.

DESCRIPTION

The generated clock has no path to the master clock on which it has been defined. This may be because there is no physical path, or because the generated clock has been defined as a -combinational and the generated clock is not in the direct fanout of the master clock. A propagated source latency of zero will be use from the master clock to the generated clock.

WHAT NEXT

Please check the design and redefine the generated clock to be in the fanout of its master clock.

DESCRIPTION

To conserve memory, PrimeTime retains arrival, required and slack information only where necessary to service the timing update and standard reporting requirements. This warning was issued to indicate that the command the user issued does not work under the current analysis settings.

WHAT NEXT

No explicit action is required on your part - under these circumstances PrimeTime adjusts the analysis settings as needed, updates timing and proceeds with the execution of the command.

SEE ALSO

timing_save_pin_arrival_and_slack (3) **timing_save_pin_arrival_and_required** (3)

DESCRIPTION

This command requires that additional slack-related info be available throughout the design for execution. To produce this information, an additional timing update will be incurred. In order to avoid the extra CPU cost of this additional update the variable should be set to TRUE before the initial timing update in this flow.

WHAT NEXT

The optimal flow for any commands requiring pin arrivals and slacks is to set the associated variable to TRUE before the initial timing update. This prevents the need for additional work before and command requiring arrivals and slacks is executed.

PTE-079 (Warning) The %s attribute does not exist on the given pin because %s is set to FALSE.

DESCRIPTION

To conserve memory, PrimeTime retains arrival, required and slack information only where necessary to service the timing update and standard reporting requirements. This warning was issued to indicate that the attribute the user queried does not

exist for the given pin under the current analysis settings.

WHAT NEXT

Set the variable appearing in the warning message to TRUE.

SEE ALSO

timing_save_pin_arrival_and_slack (3) **timing_save_pin_arrival_and_required** (3)

PTE-080 (Error) pulse clock sense merging at pin: '%s' for clock: '%s' The clock will not propagate forward from this pin.

DESCRIPTION

A pulse clock is combinationally combining with another sense of the same clock. PrimeTime does not resolve this conflict. Any registers down stream from this point will be have this clock assigned to them.

WHAT NEXT

Resolve the conflict by specifying the sense of the clock used through this pin by using the command 'set_clock_sense'.

PTE-081 (error) Can not honor set_clock_sense -pulse option at pin '%s'. Clock '%s' is missing needed rise and/or fall, or has conflicting high or low pulse types at this pin

DESCRIPTION

The user has specified a set_clock_sense -pulse option at the given pin. The needed clock senses were not available at this pin. For example, a 'rise_triggered_high_pulse' expects to find a clock source rise to this pin rise path and a clock source rise to this pin fall path. If both paths can not be found this message will be issued. There can be conflict between the pulse type propagating and that set by set_clock_sense -pulse. For example, if the propagating pulse is high and user sets a low pulse type at a pin, then this message will be issued. The pulse clock assignment for registers down stream from this pin will not be correct.

WHAT NEXT

Change the options to the command 'set_clock_sense'.

PTE-082 (warning) Connected pin groups were detected that may generate a very large number of loops. Please check the validity of this feedback logic by inspecting the connected pin groups above. Dynamic loop breaking is being disabled.

DESCRIPTION

The design contains one or more regions of logic which have combinational feedback. PrimeTime has identified these regions of connected pin groups which have the potential to generate a large number of combinational loops. Because the number of loops increases exponentially with the number of pins, these regions have the potential to exceed the limits of the machine during dynamic loop breaking. Dynamic loop breaking is being disabled.

WHAT NEXT

Check the listed pin groups to ensure that the combinational feedback loops are expected and correct in the design. If they are unavoidable, manually disable dynamic loop breaking by setting the variable timing_dynamic_loop_breaking to false.

PTE-083 (warning) Connected pin groups were detected that generate a large number of loops. Here is the connected pin group that has generated the largest number of loops so far. Dynamic loop breaking will continue, which may exceed the machine's capabilities.

DESCRIPTION

The design contains one or more regions of logic which have combinational feedback. PrimeTime has identified a region of logic which has a very large number of

combinational loops. The pins in this group will be reported, and PrimeTime will continue to attempt dynamic loop breaking. This may result in exceeding the limits of the machine. The system may become unstable and an "out of memory" error may occur.

WHAT NEXT

Check the listed pin groups to ensure that the combinational feedback loops are expected and correct in the design. If they are unavoidable and dynamic loop breaking proves to be too costly, manually disable dynamic loop breaking by setting the variable timing_dynamic_loop_breaking to false.

PTE-084 (warning) Parasitics on the net "%s" have been overridden, because the net is part of an ideal network.

DESCRIPTION

This message is displayed during a timing update for ideal nets that have parasitics annotated. The effect of leaving ideal networks in the design is that the parasitics are ignored and the net delay is ideal. This may obscure timing violations.

WHAT NEXT

To display the ideal networks is the design use the **report_ideal_network** command. To remove ideal networks that are not intended use the **remove_ideal_network** command.

SEE ALSO

remove_ideal_network (2), **report_ideal_network** (2).

PTE-085 (Warning) the calculated SHPR curve is not monotonic.

DESCRIPTION

The calculated interdependent setup/hold curve is not monotonic. The results of setup_hold_pessimisim_reduction (SHPR) may be inaccurate.

WHAT NEXT

Check SHPR library data of setup/hold value and make sure they are characterized properly.

PTE-086 (Warning) Target constraint value is beyond the boundary of characterized SHPR library. Using nearest boundary value instead.

DESCRIPTION

The target constraint value, wich is required by SHPR optimization parameter, is beyond the boundary of characterized SHPR library. To avoid optimism, PrimeTime use the nearest boundary value as the updated target constraint value.

WHAT NEXT

Check SHPR library data of setup/hold value and make sure they are characterized properly and the characterization scale covers the target constraint value.

PTE-087 (Warning) %s constraint set on %s '%s' will be ignored.

DESCRIPTION

Pulse clock constraint set on the design, lib cell, instance or clock will be ignored. This can due to the fact that the design may not have any pulse generator cells, the constrained lib cell may not be a pulse generator or is not instantiated in the design, the constrained instance is not a pulse generator or the clock may not driving any pulse generators.

WHAT NEXT

PTE-088 (Information) report_analysis_coverage was reported with timing_enable_pulse_clock_constraints variable set to FALSE.

DESCRIPTION

timing_enable_pulse_clock_constraints was set to FALSE during report_analysis_coverage for -check_type min_pulse_width and then set to its preset value i.e. TRUE after reporting.

WHAT NEXT

PTE-089 (Warning) Abandoning distributed timing update.

DESCRIPTION

PrimeTime was unable to successfully perform a distributed timing update and has set the **multi_core_enable_analysis** variable to FALSE.

WHAT NEXT

PTE-090 (Error) No output clock defined on the output '%s' of the PLL.

DESCRIPTION

You receive this message if the design has a PLL and there is no clock defined on the output that is connected to the feedback pin of the PLL.

WHAT NEXT

You should define a generated clock at the output of every PLL using the **create_generated_clock** command with the required specifications.

PTE-091 (Error) The feedback pin '%s' has no path to its PLL output clock.

DESCRIPTION

You receive this message if the design has a PLL and the feedback path is not connected correctly. Ideally, the feedback pin of a PLL should be connected to an output pin of the PLL. In addition, a generated clock should be defined on the output that is connected to the feedback pin.

WHAT NEXT

You should check that there is a path from the output of the PLL to the feedback pin. In addition, define a generated clock at the output of every PLL using the **create_generated_clock** command with the required specifications.

PTE-092 (Warning) The timing arcs from the reference pin to the output pin of the PLL '%s' are not unate. Not performing the PLL adjustment.

DESCRIPTION

You receive this message if the library model of the PLL does not have unate arcs from the reference clock pin to the output clock pin.

WHAT NEXT

PTE-093 (Warning) the -delay_calculation_only_mode flag is ignored because of the current variable settings.

DESCRIPTION

You may receive this message in the following case(s):

timing_use_zero_slew_for_annotated_arcs == always

timing_use_zero_slew_for_annotated_arcs == auto and more
than 95 percent of delay arcs on a design have annotated values"

WHAT NEXT

See man page of **timing_use_zero_slew_for_annotated_arcs** for more details.

PTE-094 (Warning) the si_xtalk_exit_on_max_iteration_count variable is ignored; only one iteration is performed

DESCRIPTION

You receive this warning because the **-delay_calculation_only_mode** option of the **write_sdf** command is exclusive with:

si_enable_analysis==true and **si_xtalk_exit_on_max_iteration_count**>1

Since only one iteration is performed, the results may be less accurate (but always

pessimistic.)

WHAT NEXT

Do nothing if this behavior is acceptable to you or remove the **-delay_calculation_only_mode** option if you insist in running multiple SI iterations. Note the general issue that using SDF generated after several SI iterations can lead to optimistic results if not done properly.

PTE-095 (Error) Generated clock is not defined on the output pin of the PLL connected to the feedback pin; not performing the PLL correction.

DESCRIPTION

You receive this error because PLL cell output defined using **-pll_output** connected to the feedback pin defined using **-pll_feedback** does not have a generated clock defined on it.

Since the generated clock is not defined, no PLL correction would be performed.

WHAT NEXT

If you want to perform PLL correction, define a generated clock at the PLL output connected to the feedback pin of the PLL.

PTE-096 (Warning) The variable multi_core_enable_analysis has been automatically set to FALSE as the following flow is not supported - '%s'. The update will now complete in scalar mode and no remote processes will be launched.

DESCRIPTION

You have attempted to perform a distributed update_timing but PrimeTime has detected a flow which is not supported in distributed mode. All remote_processes will be killed and your update will now complete as a scalar update.

WHAT NEXT

You can continue with your timing analysis. All commands will execute in scalar mode.

PTE-097 (fatal) An exceptionally long combinational path with greater than 25,000 pins is encountered. PrimeTime will exit its current session.

DESCRIPTION

PrimeTime does not time paths that have exceptionally large combinational depth for reasons of memory efficiency.

WHAT NEXT

Consider breaking combinational paths that span across more than 25,000 pins. Note that there can be multiple paths which have such exceptionally large combinational depths and all such paths need to be broken to correctly time the design.

PWR-1 (error) Clock '%s' has not been created.

DESCRIPTION

The clock '%s' has not been created in the design.

WHAT NEXT

Use the create_clock command to create a clock and define its period.

PWR-2 (error) The static probability must have a value between 0 and 1.

DESCRIPTION

The static probability argument cannot be greater than 1 or less than 0.

WHAT NEXT

Use a legal value for the **static_probability** field of the **set_switching_activity** command.

PWR-3 (error) The toggle rate value must be non-negative.

DESCRIPTION

A signal's toggle rate represents the number of transitions the signal makes during a specific amount of time. This must be a non-negative number.

WHAT NEXT

Use a legal value for the **toggle_rate** field of the **set_switching_activity** command.

PWR-4 (error) The period value must be greater than 0.

DESCRIPTION

The period argument represents the time over which the transitions in the toggle_rate argument occur. This must be a positive number.

WHAT NEXT

Use a legal value (that is, a value greater than 0) for the period field of the **set_switching_activity** command.

PWR-5 (warning) -period and -clock option both specified. Using the value from -period.

DESCRIPTION

The -period and -clock option are mutually exclusive. Both are used to specify a time period to scale the toggle rate value. Only one option is necessary.

WHAT NEXT

This is a warning.

PWR-6 (information) Propagating switching activity (%s effort %s).

DESCRIPTION

Power Compiler is estimating the power switching activity of all the design nets. The switching activity estimation mechanism uses the switching activity that has been annotated by the user to derive the switching activity of the unannotated design nets. The user can annotate switching activity using the read_saif, set_switching_activity and merge_saif commands.

WHAT NEXT

This is an information message. No user action is required.

PWR-7 (error) Unknown value ’%s’ for option ’-power_mode’ of

psynopt command.

DESCRIPTION

The '-power_mode' of psynopt command only accepts the value none, all, leakage, dynamic, only_power, only_leakage and only_dynamic. The specified value is not one of them.

WHAT NEXT

Please correct the option value and run the command again.

PWR-8 (warning) Gate level '%s' power optimization is not turned on in the place_opt/psynopt command, and '%s' power constraints is ignored.

DESCRIPTION

Gate level power optimization will only be run when proper value is specified for '-power_mode' option of the place_opt/psynopt command and there are corresponding power constraints.

WHAT NEXT

Please check the option of place_opt/psynopt and make sure power is turned on.

PWR-9 (error) Unknown value '%s' for option '-power_mode' of place_opt command.

DESCRIPTION

The '-power_mode' of place_opt command only accepts the value none, all, and leakage. The specified value is not one of them.

WHAT NEXT

Please correct the option value and run the command again.

PWR-10 (warning) Black-box output '%s/%s' has not

been annotated with switching information. Using default values of (%f, %f) for static probability and toggle rate, respectively.

DESCRIPTION

The specified black-box output pin does not have any functional description. Therefore, the tool cannot estimate the switching activity of that output as a function of the cell's input switching activities. In addition, the pin's net has not been annotated with switching activity information.

In this case, the tool assumes some default switching activity for the output pin. Usually, DesignPower will try to generate a reasonable default based on the switching activity of the clock(s) in the design. Therefore, you should make sure that you have defined valid clocks for the design so that the tool will use reasonable defaults. You can use the **report_clocks** command to check the design's clocks.

WHAT NEXT

Use the **set_switching_activity** command to explicitly specify switching activity information for this pin.

PWR-11 (warning) Breaking combinational loop at cell '%s'. This cell
will be treated as a primary input for purposes of power estimation.

DESCRIPTION

There are combinational loops in the design. During probabilistic mode, all combinational loops are broken and the "loop-breakers" are treated as primary inputs. The tool assumes a default switching activity for the output pin of the cell. The static probability is set to 0.5, and the toggle rate is set to 0.5. In order to get around the default behaviour, you can use commands such as **disable_timing** to break loops and annotate the correct switching information for such cells. To find the combinational loops in the design, use the **report_timing** command with the **-loops** option.

WHAT NEXT

Use the **set_switching_activity** command to explicitly specify correct switching activity information for the output of this cell.

PWR-12 (warning) The derived %s value (%f) for the clock net '%s' conflicts with the annotated value (%f). Using the %s value.

DESCRIPTION

One or more of the toggle rate and static probability switching activity values annotates on the clock net using the read_saif or set_switching_activity commands does not match the value derived from the clock net. The switching activity value annotated by the user is used for power calculation.

This warning indicates that the switching activity values annotated by the user may be invalid.

WHAT NEXT

The warning message contains both the derived and annotated switching activity values. Compare the two values, the difference might be very small, in which case the calculated power values will use a slightly inaccurate clock rate.

If the user annotated switching activity values are obtained by simulation then the clocks used during simulation is different from the one used for synthesis, or that the target library time units are different from the time units used by simulation. In either case, the annotated switching activities may give invalid dynamic power calculations. Check the annotated switching activity values. If you used the read_saif command, make sure that you specified the target library time unit using the -scale and -unit options.

PWR-13 (error) Target library(s) are not characterized for internal power. Compile with power constraints is NOT recommended.

DESCRIPTION

This error is issued when the **compile** command is invoked with a dynamic (or total) power constraint (see **set_dynamic_power**) and the target libraries has not been characterized for cell internal power. Without internal power information, power optimization proceeds but reduces power due only to net and pin capacitance. Without internal power characterized libraries, using compile with power constraints can lead to increased power.

WHAT NEXT

This is a error. It is highly recommended that a version of the target libraries characterized for internal power be obtained from the library vendor.

PWR-14 (warning) Clock %s no longer exists. set_switching_activity will be discarded for net %s.

DESCRIPTION

This warning occurs when toggle information for the net is specified with the -clock option of the **set_switching_activity** command and the given clock no longer exists in the design.

WHAT NEXT

This is a warning. The switching activity previously annotated on the net is discarded. **report_power** calculates switching_activity values for the net.

PWR-15 (information) Net '%s' has a static probability value but no toggle rate. Estimating the toggle rate from the static probability.

DESCRIPTION

The specified net was explicitly annotated with a static probability value, but it was not given a toggle rate. Toggle rates indicate the number of transitions that a net makes during a specified period of time.

Using the static probability value for the net, the tool will estimate the net's toggle rate (as 2*sp*[1-sp]).

WHAT NEXT

If the estimate is acceptable, nothing needs to be done. However, if the estimate is inaccurate, use the **set_switching_activity** command to explicitly specify a toggle rate for the net.

Alternatively, the **set_switching_activity** command can be used to remove the static_probability value for the specified net and allow the probabilistic analysis feature to estimate the toggle rate for that net given toggle rates for the design's primary inputs.

PWR-16 (information) Design '%s' does not have any dynamic power information. Use the report_power command to perform a

dynamic power analysis of the design.

DESCRIPTION

The design must undergo power analysis to compute the dynamic power values for the entire design. This message indicates that the design has not undergone power analysis; therefore, dynamic power information is not available for the design.

WHAT NEXT

Use the **report_power** command to force a dynamic power analysis of the design. Then proceed normally; the design should then have dynamic power information.

PWR-17 (warning) There is set_max_%s_power constraint unit but the library is unitless.

DESCRIPTION

set_max_dynamic/leakage/total_power has been specified but the library parameters are without units (eg. nW, mV). During power analysis, the units specified with set_max_dynamic/leakage/total_power will be ignored and all comparisons will be unitless. During optimization, total power will still be defined as a weighted sum of dynamic and leakage power, although no unit conversions will be performed. This may result in undesireable results, since typically libraries have different units for dynamic and leakage power.

WHAT NEXT

This is a warning. Ask your vendor to provide units in the library.

PWR-18 (warning) There is conflicting switching activity information on %s %s.

DESCRIPTION

This error occurs when there are two or more nets, pins, or ports on the same hierarchical net with different switching activity information. In such cases the switching activity information having the highest toggle rate is used for power calculations.

WHAT NEXT

This is a warning message.

PWR-19 (warning) There are %d switching activity information conflicts.

DESCRIPTION

This error occurs when there are two or more nets, pins, or ports on the same hierarchical net with different switching activity information. In such cases the switching activity information having the highest toggle rate is used for power calculations.

WHAT NEXT

For more detailed warning messages, unsuppress the PWR-18 warning message.

PWR-20 (error) Object '%s' is not a %s.

DESCRIPTION

The -only argument of the report_power command should contain a list of cells of the -cell flag is specified; a list of nets of the -net flag is specified; and a list of cells and nets if both -net and -cell are specified.

WHAT NEXT

Re-invoke the command with a valid object list with the -only argument.

PWR-21 (warning) The %s option must be positive.

DESCRIPTION

A positive number was expected for the specified option. Instead a negative number or zero was specified as the value for the option. The value will be overwritten with the default of infinity (max_int), and the command will proceed normally.

WHAT NEXT

This is a warning; the command will resume normally with the default value for the

option. In the future, a positive value should be specified for this option.

PWR-22 (warning) The %s can only be used in conjunction with the %s.

DESCRIPTION

An invalid combination of options has been specified. The first option(s) will be ignored (default value will be used), and the command will continue normally.

WHAT NEXT

This is a warning; the command will resume normally with the default value for the specified option(s). Refer to the appropriate documentation for correct usage of the option(s).

PWR-23 (error) '%s' is not a valid value for the '%s' option.

DESCRIPTION

The command was issued with an invalid option argument.

WHAT NEXT

Refer to the usage statement (or the command's documentation) for this command for a list of the valid values for the option. To see the usage statement, use the -help option of the command. Rerun the command with a valid value for the option.

PWR-24 (information) The target library(s) contains cell(s), other than black boxes, that are not characterized for internal power.

DESCRIPTION

This informational message is issued when the **compile** command is invoked with a dynamic (or total) power constraint (see **set_max_dynamic_power** or **set_max_total_power**) and the target library(s) contains cells which have not been characterized for cell internal power. Power optimization will proceed but will reduce power due only to net and pin capacitance for those cells that have not been characterized for internal power.

WHAT NEXT

This is an informational message. Check with your library vendor to make sure that all non black box, non IO pad cells are characterized for internal power.

PWR-25 (information) The design contains cell(s), other than black boxes, that are not characterized for internal power.

DESCRIPTION

This informational message is issued when the **report_power** command is invoked and the design contains some cells which are charaterized for power and others that are not. Report_power will proceed but will report power due only to net and pin capacitance for those cells that have not been characterized for internal power.

WHAT NEXT

This is an informational message. Check with your library vendor to make sure that all non black box, non IO pad cells are characterized for internal power.

PWR-26 (warning) The library cells used by your design are not characterized for internal power.

DESCRIPTION

This warning is issued when the **report_power** command is invoked and all of the the library cells which are used by your design have not been characterized for cell internal power. Without internal power information, report_power proceeds but reports power due only to net and pin capacitance. Without internal power characterized libraries, using compile with power constraints can lead to increased power.

WHAT NEXT

This is a warning. It is highly recommended that a version of the library(s) characterized for internal power be obtained from the library vendor.

PWR-27 (warning) The design %s has been mapped to the gate.

rtl2saif only works on the pre-mapped GTECH level netlist.

DESCRIPTION

This warning is issued because part of the circuit has been mapped into the gate. The **rtl2saif** command only works on the pre-mapped GETCH level netlist. If your design has been mapped to the gate, none of the sequential elements inside the design will be reported by rtl2saif.

WHAT NEXT

This is a warning. It is highly recommended that you use rtl2saif only on pre-mapped GTECH level netlist.

PWR-28 (error) Can’t set both -dynamic_weight and -leakage_weight to 0.0 in set_max_total_power command.

DESCRIPTION

This error message is issued because both the values of *-dynamic_weight* and *-leakage_weight* are 0.0.

WHAT NEXT

Check and correct the options of **set_max_total_power** command.

PWR-29 (warning) Unknown ’%s’ power effort in ’set_max_total/dynamic/leakage_power commands’.

DESCRIPTION

This error message is issued because the value of *-effort* is not as expected in **set_max_total/dynamic/leakage_power** commands. The option will be ignored.

WHAT NEXT

Check and correct the options for **set_max_total/dynamic/leakage_power** command.

PWR-30 (warning) The %s option cannot be used in conjunction

with the %s option(s). The %s option is ignored.

DESCRIPTION

An invalid combination of options has been specified. One of the options will be ignored, and the default value will be used; then, the command will continue normally.

WHAT NEXT

This is a warning; the command will resume normally with the default value of the specified option. Refer to the appropriate documentation for correct usage of the options.

PWR-31 (error) No valid %s specified.

DESCRIPTION

The -only argument needs a list of cells if -cell is specified; a list of nets of -net is specified; and a list of nets and cells if both -cell and -net are specified. Note that if both -cell and -net are specified the -only argument should contain at least one cell and at least one net.

WHAT NEXT

Re-invoke the command with a valid list of objects in the -only argument and with a valid combination of the -cell and -net flags.

PWR-32 (error) Sort mode '%s' applies only to the %s option.

DESCRIPTION

An invalid sort_mode value was specified. The sort_mode should be applicable to cells if the -cell option is specified; to nets if the -net option is specified; and to both nets and cells if both -net and -cell are specified.

WHAT NEXT

Refer to the usage statement of this command for a list of the valid sort modes. To see the usage statement, use the -help option of the command.

PWR-33 (error) Transition_type must be either rising or falling.

DESCRIPTION

An invalid transition_type option was set. The transition_type option takes only "rising" or "falling". It is case sensitive.

WHAT NEXT

Respecify set_switching_activity command with a valid transition_type option.

PWR-34 (warning) %d incomplete rise or fall specifications for pin %s of cell %s.

DESCRIPTION

There were a certain number of user specified rise (fall) toggle rates without the corresponding fall (rise) toggle rates. Design power assumes that the rise and fall toggle rates are the same and annotate the corresponding toggle rates which were left unspecified. However, for completeness, you should specify both rising and falling toggle rates.

WHAT NEXT

If you want the rise and fall toggle rates to be equal, proceed with **report_power**. However, if the rise and fall toggle rates should be different, specify the missing toggle rate specifications with **set_switching_activity**.

PWR-35 (warning) Incorrect state-dependent static probability for cell %s. This state-dependent static probability is being ignored.

DESCRIPTION

The user-specified state-dependent static probability does not match the state-dependent leakage power tables on the library cell. Therefore, this user-specified state-dependent static probability is ignored. The user-specified conditions for static probability must be logically equivalent to those on the leakage power groups of the library cell.

WHAT NEXT

Do **report_lib -power** to see the leakage power state dependencies. You can then redo **set_switching_activity** to respecify the state-dependent static probabilities. If user-specified state-dependent static probabilities are not provided, report_power computes them.

PWR-36 (warning) The static probabilities specified on cell %s add up to more than 1. These probabilities are being scaled.

DESCRIPTION

The static probability information you provided for this cell is not accurate. The static probability for each state condition in the state-dependent leakage power model adds up to more than 1. The sum of the leakage power states must add up to 1. Therefore, the static probability for each leakage state is scaled to add up to 1.

WHAT NEXT

If the scaled values are OK, go ahead with **report_power**. Otherwise, reset the switching activity using **set_switching_activity**. To see the leakage power state dependencies, use **report_lib -power**.

PWR-37 (warning) The static probabilities specified on cell %s add up to less than 1. These probabilities are being scaled.

DESCRIPTION

The static probability information you provided for this cell is not accurate. The static probability for each state condition in the state-dependent leakage power model adds up to less than 1. The sum of the leakage power states must add up to 1. Therefore, the static probability for each leakage state is scaled to add up to 1.

WHAT NEXT

If the scaled values are OK, go ahead with **report_power**. Otherwise, reset the switching activity using **set_switching_activity**. To see the leakage power state dependencies, use **report_lib -power**.

PWR-38 (warning) Overriding existing static probability for same

condition on cell %s.

DESCRIPTION

There was already a previous user-specified static probability for the same condition for this cell. Therefore, the old specification is ignored.

WHAT NEXT

If you want the old static probability for this condition for this cell, respecify it using **set_switching_activity**. Otherwise, proceed with **report_power**.

PWR-39 (warning) Low effort leakage power optimization is suggested not to use with -use_sd_info option.

DESCRIPTION

Using state dependent information to calculate leakage power can slow down the performance. In the case of low effort, the state dependent leakage power information does not help a lot on the quality of the results, but will make the tool run slower. It’s suggested that low effort leakage power optimization should not be used together with *-use_sd_info* option.

WHAT NEXT

To consider state dependent leakage power in optimization, please use high effort mode, otherwise please remove the *-use_sd_info* option.

PWR-40 (error) Unable to obtain a Power-Analysis license.

DESCRIPTION

Power commands such as **report_power** or **report_constraints** require that a Power-Analysis key be checked out.

WHAT NEXT

To determine who is using the Power-Analysis license, use the **license_users** command. Should problems occur with the license server, contact your system administrator.

PWR-41 (error) The '%s' command is not supported in dp_shell.

DESCRIPTION

This error occurs when a valid Design Compiler command is used, but the command is not supported in **dp_shell**, the power-analysis user interface. Commands such as **compile** are supported only in **dc_shell**, and are ignored in **dp_shell**.

WHAT NEXT

If you need to use the command, use the **dc_shell** program instead.

PWR-42 (warning) Unable to obtain a HighLevel-Power-Analysis license.

DESCRIPTION

The command **report_power** for unmapped parts requires that a HighLevel-Power-Analysis key be checked out. The **report_power** command will proceed but will only analyze gate-level mapped parts.

WHAT NEXT

To determine who is using the HighLevel-Power-Analysis license, use the **license_users** command. If problems occur with the license server, contact your system administrator.

PWR-43 (information) Processing library '%s' for lib2saif information.

DESCRIPTION

Power Compiler is processing the specified library in order to obtain the power characterization information needed for generating a forward SDPD library SAIF file.

WHAT NEXT

This is an information message. Very large libraries with detailed power characterization may take a few minutes to load and process the required information.

PWR-44 (information) Library SAIF file generated %s RISE/ FALL dependent path dependent directives.

DESCRIPTION

The forward SAIF file generated by the lib2saif command can include directives to generate separate rise and fall values for path-dependent toggle rates that are not state-dependent. The variable **power_lib2saif_rise_fall_pd** controls the generation of such directives. Generating separate rise and fall values results in better accuracy, but older simulators and SAIF generation applications may not be able to understand such directives. The SAIF generation PLI provided with X-2005.09 supports such directives but older versions do not.

WHAT NEXT

Check whether the client reading the generated forward SAIF file supports path-dependent toggle rate directives for separate rise and fall values, and set the value of the **power_lib2saif_rise_fall_pd** variable accordingly.

PWR-50 (warning) Switching activity has been annotated on nets connected to combinational logic. This information may be lost during a full compile.

DESCRIPTION

This warning is issued when the **compile** command is invoked with a dynamic (or total) power constraint (see **set_max_dynamic_power**, **set_max_total_power**) and switching activity has been annotated on nets connected to combinational logic (see **set_switching_activity**). The switching activity values might be discarded because a full **compile** might map the logic to a new structure with different switching activity. However, switching activtity annotated to primary input ports and sequential outputs are preserved.

WHAT NEXT

This is a warning. Use the **-incremental** option of **compile** if the design is fully mapped and you want to preserve as much switching activity as possible.

PWR-51 (error) Cannot read library %s.

DESCRIPTION

The library or one of the libraries in the **lib2saif** specification could not be found. The libries must be in .db form (not .lib form) and must be accessable from the search_path variables.

WHAT NEXT

Update the search_path to include the path to this library or respecify **lib2saif** with the whole path of this library.

PWR-52 (error) Cannot find file name to write state and path dependent SAIF forward-anotation file.

DESCRIPTION

There is no file specified to write the state-dependent and path-dependent SAIF forward annotation file. Specify the -output option for the **lib2saif** command or set the variable power_sdpd_saif_file to something other than "".

WHAT NEXT

Either modify the power_sdpd_saif_file variable or specify the -output option for the **lib2saif** command.

PWR-53 (error) Cannot open file %s to be written.

DESCRIPTION

The file where the forward-annotation SAIF file created by the *lib2saif* command is to be written is not able to be written. This file is specified with the -output option on the **lib2saif** command or by the variable power_sdpd_saif_file. This file needs to be specified.

WHAT NEXT

Change the permissions for this file or respecify another file name using the -output option of **lib2saif** or changing the power_sdpd_saif_file variable. To see the current value of the power_sdpd_saif_file variable, use **list -variables power**.

PWR-54 (error) The number of library files and library paths must be the same.

DESCRIPTION

If the -lib_pathname option is specified with the **lib2saif** command, the number of libraries and number of library path names must be the same. The library path name is used to tell the simulator where the library is. The number of library path names need to be the same as the number of libraries to associate the correct path name with the correct library.

WHAT NEXT

Respecify the **lib2saif** command without any -lib_pathname options or with the same number of libraries and library path names. If a particular library does not have a path name just specify " " for its path name.

PWR-55 (warning) The library does not contain SDPD power information, or SDPD information is not needed in the SAIF file.

DESCRIPTION

The **lib2saif** command only works with a library that contains cells with state and/or path dependent internal power and/or state dependent leakage power characterization. If the library does not contain such SDPD power characterization, or if the SDPD power information in the library is not needed, then no forward SAIF information is generated.

The SAIF file generated by the **lib2saif** command excludes certain SDPD information that is not needed to generate backward SAIF files with complete switching activity information. For example, if the internal power of a cell pin is fully characterized by only one SDPD table, then the SDPD characterization for this pin is not needed in the library forward SAIF file, since SDPD toggle rate information can be accurately derived from the non-SDPD toggle rate on the cell pin. (Basically, the SDPD toggle rate for the power table is exactly equal to the SDPD toggle rate on the pin.) Note, that the internal power characterization on the output pins of single input buffers and inverters are usually characterized this way.

WHAT NEXT

Check your library and make sure it has cells with SDPD power characterization.

PWR-56 (warning) The bus naming style specified, %s, is

invalid.

DESCRIPTION

The bus naming style specified is invalid. This bus_naming_style will be ignored and the default bus_naming_style If this is not your intent please specify a valid bus_naming_style.

WHAT NEXT

If you are happy with the default, you need to do nothing. Otherwise, you need to change the bus_naming_style to a valid one.

PWR-57 (error) Target libraries must be specified when running power analysis.

DESCRIPTION

You must either set the target_libraries variable or set the -target_libs option on the command line. In order to do rtl level power analysis, we need to know the target library to correlate power numbers.

WHAT NEXT

Specify the **target_libraries** variable or use the -target_lib option.

PWR-58 (error) The value of -dynamic_weight or -leakage_weight is negative.

DESCRIPTION

This error message is issued because the value of *-dynamic_weight* or *-leakage_weight* is negative which is not an acceptable value.

WHAT NEXT

Check and correct the options of **set_max_total_power** command.

PWR-59 (warning) Ignoring ’power_effort’ option since there is

no power constraint.

DESCRIPTION

You receive this message if you specify **compile -power_effort**, but there is no power constraint for the current design. In this case, power optimization will not be enabled, and **-power_effort** is ignored.

WHAT NEXT

Set power constraints.

PWR-60 (error) The time unit in the -unit option must be one of these: s, ms, us, ns, ps, fs.

DESCRIPTION

The -unit option specifies the synthesis base time unit. It can be either s, ms, us, ns, ps, or fs. If not specified, the default is ns.

WHAT NEXT

Re-invoke the command with a valid time unit.

PWR-61 (error) Invalid -scale value, the valid -scale values are 1, 10, and 100.

DESCRIPTION

The -scale option specifies the scale factor of the synthesis time unit. It can be 1, 10 or 100. If not specified, the default is 1.

WHAT NEXT

Re-invoke the command with a valid value for the -scale argument.

PWR-62 (warning) The -unit_base option is not specified, the

default is ns.

DESCRIPTION

The **-unit_base** option specifies the base unit of the intended synthesis time unit. It can be either **us**, or **ns**, or **ps**. The synthesis time unit is usually obtained from the target library. However, if the target library is not avialable when the user applies the **read_saif** command, the **-scale** and **-unit_base** arguments can be used to specify the intended synthesis time unit.

WHAT NEXT

Specify the -scale and -unit and options if the intended synthesis time unit is not 1 ns.

PWR-63 (warning) The -scale option is not specified, the default is 1.

DESCRIPTION

The **-scale** option specifies the scaling factor of the intended synthesis time unit. It can be either **1**, **10**, or **100**. The synthesis time unit is usually obtained from the target library. However, if the target library is not avialable when the user applies the **read_saif** command, the **-scale** and **-unit_base** arguments can be used to specify the intended synthesis time unit.

WHAT NEXT

Specify the -scale and -unit and options if the intended synthesis time unit is not 1 ns.

PWR-64 (warning) The -strip option is obsolete in this release. PowerCompiler will use it as if the -instance option is specified. In the future, please use the -instance option.

DESCRIPTION

The -strip option is no longer supported. Instead, the user should use -instance option to indicate which instance in the SAIF file will be annotated on the current design.

WHAT NEXT

Please see the man page for read_saif on the usage of -instance option.

PWR-65 (error) Conflicting -instance and -strip options specified.

DESCRIPTION

The -strip option is obsolete, and is not required if the -instance option is specified. This error occurs when the -strip and -instance options are specified and their arguments are different. If the command is invoked with the same -strip and -instance arguments, then the -strip argument is ignored.

WHAT NEXT

Re-invoke the command with a valid -instance option, and without the -strip option.

PWR-66 (information) Please use '%s' variable for the related feature.

DESCRIPTION

The message indicates that this variable may be used to turn on and off a feature. The old way to turn on and off this feature has been obsolete.

WHAT NEXT

Use this variable to turn on and off the feature.

PWR-68 (warning) Variable '%s' is obsolete.

DESCRIPTION

The message indicates that the variable used to control power optimization is no long supported.

WHAT NEXT

No action.

PWR-70 (warning) The cell %s does not comply with the bus naming style

DESCRIPTION

The current bus_naming_style does not match the name of the cell. Please check the style and correct it appropriately.

WHAT NEXT

This is a warning.

PWR-71 (warning) The bus naming style %s is not supported.

DESCRIPTION

The bus naming styles supported now must match the pattern of "*%s?%d*". zero or more separators, and ? means one or more separators. Only two bus naming styles are supported at this moment: %s[%d] and %s_%d.

WHAT NEXT

This is a warning.

PWR-72 (error) The path_dep option must be a pin or set of pins on cell %s

DESCRIPTION

The path dependent option must contain pins that are on the same cell as the pin for which you are specifying the **set_switching_activity**. This pin or set of pins should be the name of the pins, such as Z, A, or B, not an instance specific pin such as U1/Z.

WHAT NEXT

If you want to specify a path-dependent toggle rate, respecify **set_switching_activity** with a pin name or set of pin names which are on the same cell that the toggle rate is being specified for.

PWR-73 (error) The path source '%s' is not a valid pin name for the cell instance '%s'.

DESCRIPTION

The given path source does not specify a pin name. The path source needs to be a valid library cell pin name for the cell that is being annotated with switching activity. Also note that it needs to be just the simple name instead of the hierarchical pin name; for example "U1/A" is not valid, but "A" is.

WHAT NEXT

Use a valid path source.

PWR-74 (error) Specification of state-dependent toggle rate must be for a pin.

DESCRIPTION

When specifying a state-dependent toggle rate, it must be for a pin. In other words, the <object_list> portion of the **set_switching_activity** command must have exactly 1 pin. State-dependent toggle rates for cells or ports are not allowed.

WHAT NEXT

Respecify **set_switching_activity** with a pin.

PWR-75 (error) The conditions in the state-dependent toggle rate must be in terms of pins on that cell.

DESCRIPTION

The state_dep option must be a boolean equation of pins that are on the same cell as the pin for which you specify the **set_switching_activity**. The pins in the condition should be the name of the pins, such as A and B, not an instance specific pin such as U1/A.

WHAT NEXT

If you want to specify a state-dependent toggle rate, respecify wfIset_switching_activity with a boolean equation of pins that are on the same cell

that the toggle rate is specified for.

PWR-76 (warning) The current static probability on %s is different from the existing one. Using new static probability.

DESCRIPTION

There was a previously set user-specified static probability for this object. The new user-specified static probability takes precedence over the previously specified one.

WHAT NEXT

If the new static probability is what you want, continue. Otherwise, respecify the old value using **set_switching_activity**.

PWR-77 (error) Specification of a path-dependent toggle rate can only be for an output or inout pin.

DESCRIPTION

When specifying a path-dependent toggle rate, the <object_list> portion of the **set_switching_activity** command must be an output or an inout pin. This is because path dependency does not work for input pins.

WHAT NEXT

To specify toggle rates on input pins, respecify **set_switching_activity** without the -path_dep option. To specify a path-dependent switching activity, you must use -path-dep and an output pin like the <object_list>.

PWR-78 (error) The path_dep option must contain either input or inout pins.

DESCRIPTION

The path dependent option must contain input or inout pins that are on the same cell as the pin for which you are specifying the **set_switching_activity**. This pin or set of pins should be the name of the pins, such as Z, A, or B, not an instance specific pin such as U1/Z. It does not make sense to have path dependency from output pins,

so only input or inout pins are allowed in the -path_dep option.

WHAT NEXT

To specify a path-dependent toggle rate, respecify **set_switching_activity** with an input/inout pin name or set of input/inout pin names that are on the same cell that the toggle rate is specified for.

PWR-79 (error) The start and end point of a path must be different pins.

DESCRIPTION

Any pin in the -path_dep option and the <object_list> of the *set_switching_activity* command cannot be the same pin. This is because you cannot have path dependency from one pin to itself.

WHAT NEXT

If you want to specify a path-dependent toggle rate, respecify *set_switching_activity* with pins in the -path_dep option that are different from the one in the <object_list>.

PWR-80 (warning) There is no defined clock in %s.

DESCRIPTION

This warning message occurs when there is no clock in the entire design (or in a scenario for multi-scenario designs). For the purposes of power analysis, the cycle-based simulation requires a reference timing unit, which is obtained from the design clock. The design clock can be virtual. In case no clock has been created, the library timing unit is used as a reference unit for the simulation.

WHAT NEXT

This is a only a warning message. No action is required.

However, if the result is not what you intended, use the **create_clock** command to define the clocks of the design.

SEE ALSO

create_clock(2)

PWR-81 (warning) Sequential cell %s with no output activity annotation.

DESCRIPTION

This warning occurs when there is a sequential cell with no switching activity annotated on either of its outputs. In this case, DesignPower will propagate the switching activity from the cell's inputs, however, to increase the accuracy of the power estimation, annotate the outputs with valid switching activity.

WHAT NEXT

This is a warning. Annotate the outputs with valid switching activity.

PWR-82 (error) Incorrect toggle rate specification for %s. Specification of state-dependent, path-dependent, or separate specification of rise/fall toggle rates must be for a pin.

DESCRIPTION

When specifying state-dependent, path-dependent, or separate rise/fall toggle rates, the <object_list> of the *set_switching_activity* command must be a pin. Cells and ports are not allowed.

WHAT NEXT

Only specify state-dependent, path-dependent, or separate rise/fall toggle rates on pins.

PWR-83 (error) Specification of state-dependent static probability must be for a cell.

DESCRIPTION

When using the -static_prob and -state_dep options of the **set_switching_activity** command, you can only have cells in the <object_list>.

WHAT NEXT

To specify state-depenedent static probabilities, use a cell in the <object_list> of

the *Bet_switching_activity* command.

PWR-84 (error) Specification of a path-dependent toggle rate must be for only one pin.

DESCRIPTION

When specifying a path-dependent toggle rate, the <object_list> portion of the **set_switching_activity** command must be for only one output or inout pin.

WHAT NEXT

To specify toggle rates on input pins, respecify *set_switching_activity* without the -path_dep option. To specify a path-dependent switching activity, use -path-dep and only one output/inout pin as the <object_list>.

PWR-85 (error) Specification of a path-dependent toggle rate must be for a pin.

DESCRIPTION

When specifying a path-dependent toggle rate, the <object_list> portion of the **set_switching_activity** command must be an output or an inout pin. Cells and ports are not allowed for path-dependent toggle rates.

WHAT NEXT

To specify toggle rates on input pins, respecify *set_switching_activity* without the -path_dep option. To specify a path-dependent switching activity, use -path-dep and an output/inout pin as the <object_list>.

PWR-86 (warning) The option '%s' of '%s' command is obsolete.

DESCRIPTION

The message indicates that the option of the command is obsolete. Although it may still work, users are recommanded to use the proposed new interface if the feature still exists.

WHAT NEXT

Change to the new interface.

PWR-87 (warning) The state dependent toggle rate specification for pin %s of cell %s does not match the state dependent specification for the library cell. Ignoring this toggle.

DESCRIPTION

The state dependencies specified for toggle rates must be the same state dependencies specified on the library cell. If the state dependencies do not match, your specified toggle rate is ignored.

WHAT NEXT

To see the state dependencies on the library cell, use *report_lib -power*. To respecify state-dependent toggle rates use *set_switching_activity* with the -state_dep options.

PWR-88 (warning) The path-dependent toggle rate specification for pin %s of cell %s is not complete, all of the related pins are not specified.

DESCRIPTION

This pin of this cell has a path-dependent internal power model in its library cell. The path-dependent toggle rate you specified did not take into account all of the paths specified in the library. Therefore, the path-dependent toggle rates you specified will be ignored for this pin.

WHAT NEXT

To see the path dependencies in the library cells use *report_lib -power*. Then use *set_switching_activity* with the -path_dep option to specify all of the path dependencies. If you want *report_power* to proceed with calculated toggle rates, just continue.

PWR-89 (warning) Multiple equivalent path-dependent toggle rate specifications for pin %s of cell %s. Ignoring all your toggle

rate specifications for this pin.

DESCRIPTION

You specified two or more equivalent path-dependent toggle rates. Therefore, all your specified toggle rates for this pin will be ignored.

WHAT NEXT

To override path-dependent toggle rates, first delete the old toggle rates using *set_switching_activity* <pin>. Then you can respecify the path-dependent toggle rate using the -path_dep option of *set_switching_activity*. If it is alright to use calculated path-dependent toggle rates, proceed with **report_power**.

PWR-90 (warning) There was an extra rise/fall toggle rate specification for pin %s of cell %s. Because all of the state and path dependencies for this pin were already specified, this specification is ignored.

DESCRIPTION

The user specified a rise/fall toggle rate without any state or path dependencies. Because this cell had state and path dependent switching activity already specified, these rise/fall toggle rates are ignored.

WHAT NEXT

Remove the other toggle rates using /fIset_switching_activity/fP <pin> and respecify only the rise/fall toggle rates. Otherwise, if it is acceptable that the rise/fall toggle rates are ignored, proceed with /fIreport_power/fP.

PWR-91 (warning) The state dependent toggle rate specification for pin %s of cell %s is not complete. All states must be specified.

DESCRIPTION

This pin of this cell has a state-dependent internal power model in its library cell. You specified state-depedent toggle rates that did not cover all of the state dependencies specified for this library cell.

WHAT NEXT

To see the state dependencies in the library cells use *report_lib -power*, then use /fIset_switching_activity/fP with the -state_dep options to specify all of the state dependencies. If you want *report_power* to proceed with calculated toggle rates, just continue.

PWR-92 (warning) Too many state or path dependent toggle rate specifications for pins %s of cell %s. Ignoring all user-specified toggle rates for this pin.

DESCRIPTION

You specified two or more equivalent path-dependent or state-dependent toggle rates. Therefore, all user specified toggle rates for this pin will be ignored. To override path-dependent or state-dependent toggle rates, first delete the old toggle rates using *set_switching_activity* <pin>.

WHAT NEXT

To override state-dependent or path-dependent toggle rates, first delete the old toggle rates using *set_switching_activity* <pin>. Then you can respecify the state-dependent or path-dependent toggle rate using the -state_dep or -path_dep options of *set_switching_activity*. If it is alright to use calculated state-dependent or path-dependent toggle rates, proceed with **report_power**.

PWR-93 (warning) There is both a separate rise/fall and an average toggle rate specification for pin %s of cell %s. Because this library cell has a separate rise/fall internal power model, the average specification is ignored.

DESCRIPTION

You specified rise or fall toggle rates and the average toggle rate for a pin. The library cell has a separate rise/fall internal power specification, so the average toggle rate specification is ignored.

WHAT NEXT

If it is acceptable to assume to ignore the user specified toggle rate, proceed with *report_power*. Otherwise, delete the existing specifications for this pin using *set_switching_activity* <pin_name> and respecify the average toggle rate for this

pin.

PWR-94 (error) Cannot find file name to write RTL forward-annotation SAIF.

DESCRIPTION

There is no file specified to write the RTL forward annotation SAIF file. Specify the -output option for the **rtl2saif** command or set the variable power_rtl_saif_file to something other than "".

WHAT NEXT

Modify the power_rtl_saif_file variable or specify the -output option for the **rtl2saif** command.

PWR-95 (error) Cannot open file %s to be written.

DESCRIPTION

The file where the forward-annotation SAIF file created by the **rtl2saif** command is to be written is not able to bewritten. Verify you have the write permission in the current directory.

WHAT NEXT

Change the permissions for this file or respecify another file name using the -output option of **rtl2saif** or changing the power_rtl_saif_file variable. To see the current value of the power_rtl_saif_file variable, use **list -variables power**.

PWR-96 (warning) There are sequential cells with no output activity annotation.

DESCRIPTION

This warning occurs when there is a sequential cell with no switching activity annotated on either of its outputs. Unsuppress warning PWR-81 for more information.

WHAT NEXT

This is a warning.

PWR-97 (error) You have not set the environment variable 'power_preserve_rtl_hier_names' to TRUE. The rtl2saif command cannot proceed.

DESCRIPTION

The environment variable 'power_preserve_rtl_hier_names' must be set to TRUE when you analyze and elaborate a design and issue the rtl2saif command. This variable enables important information to be saved in DB, which is necessary for generating the forward-annotated SAIF file.

WHAT NEXT

Set the variable and reanalyze and elaborate the design.

PWR-98 (error) There must be a toggle rate or static probability specified when you specify the -toggle option.

DESCRIPTION

When you specify the -toggle option for **set_switching_activity** command, you must also specify either the tr or sp options or both. Therefore this specification is being ignored.

WHAT NEXT

Respecify the **set_switching_activity** command with either a -tr or -sp option. Otherwise, if you want to specify a clock period only, do a **create_clock** with a specified period.

PWR-99 (error) The -instance option is not specified.

DESCRIPTION

While annotating switching activity with the read_saif command, you must specify which instance in the SAIF file is to be annotated onto the current design. For example, read_saif -input my.saif -instance top/U1 to specify that the instance top/U1 in the SAIF file contains switching activity for the current design insdie dc_shell.

WHAT NEXT

Specify the -instance option for the read_saif command and rerun the command again.

PWR-100 (error) The state dependent condition cannot contain the pin that has the switching activity specified.

DESCRIPTION

Any pin in the -state_dep option and the <object_list> of the **set_switching_activity** command cannot be the same pin. This is because you cannot have state dependency from a pin to itself.

WHAT NEXT

If you want to specify a state-dependent toggle rate, respecify **set_switching_activity** with pins in the -state_dep option that are different from the one in the <object_list>.

PWR-101 (error) Clock gating element missing in design %s.

DESCRIPTION

User probably has manually removed clock gating elements.

WHAT NEXT

Use remove_clock_gating command to remove gating elements. period.

PWR-102 (warning) replace_clock_gating_cells

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-103 (error) The %s command expects at least one option.

DESCRIPTION

The command was issued without valid options. The command expects at least one option.

WHAT NEXT

Re-issue the command with one or more valid options. Use the -help option to list all possible options. More information can be found in the man page for this command.

PWR-104 (error) The '%s' option cannot be used in combination with other options.

DESCRIPTION

The command was issued with an invalid combination of options.

WHAT NEXT

Re-issue the command with a valid combination of options. Use the -help option to list all possible options. More information can be found in the man page for this command.

PWR-105 (warning) Not clock-gating register %s since -

minimum_bitwidth constraint is violated after splitting.

DESCRIPTION

You receive this warning message when certain registers are not clock-gated due to the **-minimum_bitwidth** constraint. During **elaborate** large register banks are split between multiple clock-gating elements when the **-max_fanout** constraint is specified. This may result in some clock-gating elements gating a fewer number of registers than the constraint specified by the **-minimum_bitwidth** option.

WHAT NEXT

The **-minimum_bitwidth** variable can be modified by using the **set_clock_gating_style** command to control the minimum width of the register banks that can be clock gated.

PWR-106 (error) The -max_fanout option cannot be honored unless the variable hdlin_no_group_register is set to TRUE.

DESCRIPTION

You receive this warning message when you execute the **set_clock_gating_style** command with the -max_fanout option and the **hdlin_no_group_register** environment variable is not set to TRUE. For HDL Compiler to limit the fanout load of the clock-gating cells, the environment variable **hdlin_no_group_register** should be set to TRUE. Otherwise, the **-max_fanout** option cannot be honored.

WHAT NEXT

If you want the **elaborate** command to limit the fanout of each clock-gating cell, set the environent variable **hdlin_no_group_register** to TRUE. If you do not want the **elaborate** command to limit the fanout, do not use the -max_fanout option to the **set_clock_gating_style** command. Setting the variable **hdlin_no_group_register** to TRUE disables multi-bit registers optimizations during **compile**.

PWR-107 (error) The value of -max_fanout (%d) cannot be less than the value of -minimum_bitwidth (%d).

DESCRIPTION

You receive this error message when an invalid argument to the **-max_fanout** option for the **set_clock_gating_style** command has been specified. The entire command will be ignored, and the clock gating style, if defined, is not changed. The **set_clock_gating_style** command terminates without changing the clock gating style.

WHAT NEXT

The argument to the **-max_fanout** option (default value is 2048) should be a positive whole number which is greater than or equal to the argument to the **-minimum_bitwidth** option (default value is 3).

SEE ALSO

set_clock_gating_style(2).

PWR-108 (warning) The register %s could not be considered for splitting since the variable %s is not set to TRUE.

DESCRIPTION

When you execute the **elaborate** command, register banks may be grouped (internally) to enable multi-bit optimizations during compile. However, these regsiter banks cannot be split to satisfy the max_fanout constraint on the clock-gating cells. In order to allow the splitting of register banks to limit the max_fanout of individual clock-gating cells, the registers must be ungrouped internally during **elaborate**.

WHAT NEXT

Set the required variable **hdlin_no_group_registers** to TRUE. Setting the variable to TRUE will not allow Design Compiler to select multi-bit cells for this register.

SEE ALSO

elaborate(2), set_clock_gating_style(2).

PWR-109 (error) The max_fanout value cannot be non-positive: %d.

DESCRIPTION

You receive this error message when an invalid argument has been specified for the **-max_fanout** option of the **set_clock_gating_style** command. The command will be ignored, and the clock gating style, if defined, is not changed.

WHAT NEXT

Specify a valid value for the **-max_fanout** option. The argument to the **-max_fanout** option should be a positive whole number.

SEE ALSO

set_clock_gating_style(2).

PWR-110 (warning) The setup/hold time for the clock gate is negative: %s.

DESCRIPTION

The setup or hold time specified by the set_clock_gating_style command is negative. This may corrupt the clock waveform.

WHAT NEXT

Check if the setup/hold time should really be negative.

PWR-111 (error) The minimum register bank size cannot be negative: %d.

DESCRIPTION

An invalid option value has been specified. The complete command will be ignored, and the clock gating style, if defined, is not changed.

WHAT NEXT

The command terminates without changing the clock gating style. Refer to the appropriate documentation for correct usage of the option.

PWR-112 (error) The circuitry specified for gating the clocks of %s-edge triggered registers does not match the specified latch style.

DESCRIPTION

An invalid option value has been specified. The complete command will be ignored, and the clock gating style, if defined, is not changed.

WHAT NEXT

The command terminates without changing the clock gating style. Refer to the appropriate documentation for correct usage of the option.

PWR-113 (error) The gate %s specified for clock gating has multiple outputs. This is not allowed.

DESCRIPTION

An invalid option value has been specified. The complete command will be ignored, and the clock gating style, if defined, is not changed.

WHAT NEXT

The command terminates without changing the clock gating style. Refer to the appropriate documentation for correct usage of the option.

PWR-114 (error) The gate %s specified for clock gating is not a %s.

DESCRIPTION

An invalid option value has been specified. The complete command will be ignored, and the clock gating style, if defined, is not changed.

WHAT NEXT

The command terminates without changing the clock gating style. Refer to the appropriate documentation for correct usage of the option.

PWR-115 (error) The cell list specified for clock gating is too short: %s.

DESCRIPTION

An invalid option value has been specified. The complete command will be ignored, and the clock gating style, if defined, is not changed.

WHAT NEXT

The command terminates without changing the clock gating style. Refer to the appropriate documentation for correct usage of the option.

PWR-116 (error) The cell list specified for clock gating is too long: %s.

DESCRIPTION

An invalid option value has been specified. The complete command will be ignored, and the clock gating style, if defined, is not changed.

WHAT NEXT

The command teminates without changing the clock gating style. Refer to the appropriate documentation for correct usage of the option.

PWR-117 (error) The pre gate specified for the clock gating circuitry has an invalid function %s.

DESCRIPTION

An invalid option value has been specified. The complete command will be ignored, and the clock gating style, if defined, is not changed.

WHAT NEXT

The command terminates without changing the clock gating style. Refer to the appropriate documentation for correct usage of the option.

PWR-118 (error) The main gate specified for the clock gating circuitry has invalid function %s.

DESCRIPTION

An invalid option value has been specified. The complete command will be ignored, and the clock gating style, if defined, is not changed.

WHAT NEXT

The command terminates without changing the clock gating style. Refer to the appropriate documentation for correct usage of the option.

PWR-119 (error) The post gate specified for the clock gating circuitry has invalid function %s.

DESCRIPTION

An invalid option value has been specified. The complete command will be ignored, and the clock gating style, if defined, is not changed.

WHAT NEXT

The command terminates without changing the clock gating style. Refer to the appropriate documentation for correct usage of the option.

PWR-120 (error) Clock gating cannot be performed if no clock gating style has been set.

DESCRIPTION

You need to set the clock gating style using the command set_clock_gating_style before clock gating can be performed. The command is terminated.

WHAT NEXT

Specify the clock gating style.

PWR-121 (error) The gate %s specified for clock gating does not have the correct number of %d input pins.

DESCRIPTION

An invalid option value has been specified. The complete command will be ignored, and the clock gating style, if defined, is not changed.

WHAT NEXT

The command terminates without changing the clock gating style. Refer to the appropriate documentation for correct usage of the option.

PWR-122 (error) The gate %s specified for clock gating does not exist in the target library.

DESCRIPTION

The clock gating style specifies a cell from a certain target library to be used in the clock gating circuitry, but the cell cannot be found in the target library. There are two possible reasons: first, a target library with the specified name does not exist. Note that you need to give the library name as used, for example, with the report_lib command, and not the library file name. This error can also occur if the target library with the specified name exists, but a cell with the specified name does not exist in the library. The complete command will be ignored, and the clock gating style, if defined, is not changed.

WHAT NEXT

The command terminates without changing the clock gating style. Refer to the appropriate documentation for correct usage of the option.

PWR-123 (warning) The enable signal of cell %s is computed by circuitry which is fed by flip-flops triggered by different edges. Clock gating will not be applied to the current cell.

DESCRIPTION

Latch-free clock gating requires that the enable signal arrives at the 2-input clock gate before the inactive clock edge (clock of the flip-flop which is to be gated). This cannot be guaranteed if the logic driving the enable signal depends on the other clock edge or on other clocks. Therefore, the clock of a flip-flop is not gated if its enable logic is fed by any flip-flop that is not triggered by the same clock edge. Similarly, for module level clock gating, a manually inserted clock gate is not replaced if its enable logic is fed by any flip-flop that is not triggered by the same clock edge.

WHAT NEXT

This restriction only applies to latch-free clock gating. Use latch-based clock gating to achieve larger power reduction.

PWR-124 (warning) The enable signal of cell %s is computed by circuitry which is fed by a design input port. Clock gating will not be applied to the current cell.

DESCRIPTION

Latch-free clock gating requires that the enable signal arrives at the 2-input clock gate before the inactive clock edge (clock of the flip-flop which is to be gated). This cannot be guaranteed if the logic driving the enable signal depends on an input port of the design. Therefore, the clock of a flip-flop is not gated if its enable logic is fed by any design input port. Similarly, for module level clock gating, a manually inserted clock gate is not replaced if its enable logic is fed by any design input port.

WHAT NEXT

This restriction only applies to latch-free clock gating. Use latch-based clock gating to achieve larger power reductions.

PWR-125 (warning) The enable signal of flip-flop %s is computed by circuitry which is fed by flip-flops triggered by unknown edges. Clock gating will not be applied to the current flip-flop.

DESCRIPTION

Latch-free clock gating requires that the enable signal arrives at the 2-input clock gate before the inactive clock edge (clock of the flip-flop which is to be gated). This cannot be guaranteed if the logic driving the enable signal depends on the other clock edge or on other clocks. Therefore, the clock of a flip-flop is not gated if its enable logic is fed by any flip-flop that is not triggered by the same clock edge. For the current flip-flop, it was not possible to determine the clocks of the flip-flops feeding the enable logic.

WHAT NEXT

This restriction only applies to latch-free clock gating. Use latch-based clock gating to achive larger power reduction.

PWR-126 (error) The clock gating style is incorrect.

DESCRIPTION

The clock gating style has been corrupted since its last setting.

WHAT NEXT

Set the clock gating style using the command set_clock_gating_style.

PWR-127 (error) Incorrect specification of the control point in the clock gating style.

DESCRIPTION

The command set_clock_gating_style has been used with invalid control point specification.

WHAT NEXT

For the control point option, use set_clock_gating_style with one of the following arguments: none, before_latch, or after_latch.

PWR-128 (error) Incorrect specification of the control signal in the clock gating style.

DESCRIPTION

The command set_clock_gating_style has been used with an invalid control signal specification.

WHAT NEXT

For the control signal option, use set_clock_gating_style with one of the following arguments: scan_enable or test mode.

PWR-129 (error) The observability logic’s xor tree depth did not

have a non-negetive value.

DESCRIPTION

An invalid option value has been specified. The complete command will be ignored and the clock gating style, if defined, is not changed.

WHAT NEXT

The command terminates without changing the clock gating style. Refer to the appropriate documentation for correct usage of the option.

PWR-130 (error) The sequential cell is neither none nor latch: %s.

DESCRIPTION

This error message occurs because the sequential cell specified using the **set_clock_gating_style** command with the **-sequential_cell** option has an invalid value. The accepted values for **-sequential_cell** are **none** or **latch**.

WHAT NEXT

Check the clock-gating style and run the command again specifying the **-sequential_cell** as either **none** or **latch**.

SEE ALSO

set_clock_gating_style(2)

PWR-131 (warning) With the specified clock gating style, an inverter will be created to connect the ENCLK pin of the clock gating circuitry with the clock pin of gated cell.

DESCRIPTION

Due to the clock gating circuitry chosen by the set_clock_gating_style command, and possibly due to an inverter in the register block, another inverter needs to be inserted on the clock net to produce the correct clock waveform. The input of the new inverter is connected to the ENCLK pin of the clock gating circuitry; the output of the new inverter is connected to the clock pin of the gated subdesign. This design can be a register, a clock gate or a module. It depends on your compile

methodology (ungrouping, boundary optimization) if this inverter will be mapped with the generic sequential cell to a flip-flop of the target library or will be integrated with the gated module. Note that you may end up with the additional inverter on the clock network after compilation. This may impact clock tree synthesis.

WHAT NEXT

Choose a different clock gating style such that the additional inverter on the clock network is not needed.

PWR-132 (warning) The clock gating style was not changed.

DESCRIPTION

Setting a new clock gating style failed. The old clock gating style (if it exists) is still in use.

WHAT NEXT

Be aware that you correctly set the new clock gating style before performing clock gating.

PWR-133 (error) Incorrect specification of the observation point in the clock gating style.

DESCRIPTION

The command set_clock_gating_style has been used with invalid observation point specification.

WHAT NEXT

Use set_clock_gating_style with one of the following arguments to the observation point option: true, false.

PWR-134 (warning) No warnings will be given about testability

implications of clock gating style.

DESCRIPTION

The specified scan style is none or combinational. Therefore, you will not get any warnings alerting you about testability implications of your clock gating style.

WHAT NEXT

Specify a noncombinational scan style if you want to perform clock gating of registers.

PWR-135 (warning) Clock pins of flip-flops are not controllable after clock gating.

DESCRIPTION

Clock pins of flip-flops with gated clocks will not be controllable during scan shift. Therefore, such flip-flops cannot be included in the scan chain. This can result in a loss of fault coverage.

WHAT NEXT

If you cannot accept the loss in fault coverage, use the **-control_point** option of the **set_clock_gating_style** command to specify control point insertion.

PWR-136 (warning) Clock gating signals will not be observable.

DESCRIPTION

The signals used to gate register clocks will not be observable because the test mode signal is constant during testing. Therefore, this configuration will result in a loss of fault coverage.

WHAT NEXT

If you cannot accept the loss of fault coverage, either specify a scan enable signal instead of a test mode signal using the **-control_signal** option, or introduce observability circuitry using the **-observation_point** option of the **set_clock_gating_style** command.

PWR-137 (warning) The test clock waveform must be compatible with the clock gating cell.

DESCRIPTION

Because the control point is after the latch, the scan enable signal can corrupt the clock signal at gated clock registers during testing, if the test clock waveform is not chosen properly.

WHAT NEXT

Define the test clock waveform at the scan enable port such that the resting value of the clock at the port reaches the clock pins of gated clock registers. That is, the resting value of the clock at the port implies the controlling value of the clock gating cell.

PWR-138 (warning) For this scan style, the clock gating style need not specify a control point.

DESCRIPTION

Due to the specified scan style, the clock pins of the registers with gated clocks are controllable. Therefore, no control point need be inserted during clock gating.

WHAT NEXT

Use -control_point none with the **set_clock_gating_style** command to designate no control point.

PWR-139 (error) The library cell %s specified for clock gating has the dont_use attribute set, but not the is_clock_gating_cell attribute.

DESCRIPTION

The specified library cell has the dont_use attribute set. Since the is_clock_gating_cell attribute is not set on the library cell, the cell cannot be used in the clock gating circuitry.

WHAT NEXT

If you want to use this library cell, you need to have the is_clock_gating_cell attribute on the cell.

PWR-140 (warning) Command was called without an option and has no effect.

DESCRIPTION

The **propagate_constraints** command was called without option **-gate_clock**. The command does not have an effect.

WHAT NEXT

Call **propagate_constraints -gate_clock**.

PWR-141 (error) The pin specification for the clock gate is incorrect.

DESCRIPTION

The names of the clock gate pins must match the names of the specified library cell.

WHAT NEXT

Check pin specification %s.

PWR-142 (error) The operand isolation style is not set.

DESCRIPTION

The operand isolation style is not set.

WHAT NEXT

Set the operand isolation style using the **set_operand_isolation_style** command.

PWR-143 (error) Operand isolation style is incorrect.

DESCRIPTION

The operand isolation style has been corrupted since its last setting.

WHAT NEXT

Set the operand isolation style using the set_operand_isolation_style command.

PWR-144 (warning) The operand isolation style was not changed due to errors.

DESCRIPTION

Setting a new operand isolation style has failed. The old operand isolation style (if it exists) is still in use.

WHAT NEXT

Make sure that you are satisfied with the operand isolation style that is set before proceeding.

PWR-145 (error) The percentage area penalty allowed cannot be negative.

DESCRIPTION

The percentage area penalty allowed cannot be negative.

WHAT NEXT

Set the percentage area penalty allowed to a positive number using the "-area <number>" option in the set_operand_isolation_style command.

PWR-146 (error) The logic specified for operand isolation is not

valid.

DESCRIPTION

The logic specified for operand isolation is not valid. The isolation logic can be AND, OR, or adaptive only.

WHAT NEXT

Set the isolation logic to AND, OR or adaptive using the -logic option in the set_operand_isolation_style command.

PWR-147 (error) The specified values are out of range.

DESCRIPTION

The maximum negative slack value specified with the **set_operand_isolation_slack** command should be non-negative. The value for the weight should be between 0.0 and 1.0.

WHAT NEXT

Correct the values specified as arguments to the **set_operand_isolation_slack** command.

PWR-148 (Warning) Isolation operations list is empty.

DESCRIPTION

The list of operations to be included/excluded for isolation is empty.

WHAT NEXT

If you do not want to manually isolate(or not) any operations, do not use the set_isolation_operations command. This command is used to specify operations that the user wants to include/exclude irrespective of the results of the automated technique.

PWR-149 (warning) Conflict between included and excluded

isolation operations.

DESCRIPTION

There is a conflict between included and excluded operations from operand isolation.

WHAT NEXT

Check the options to the set_isolation_operations command for any conflicts.

PWR-150 (error) Syntax error in MPML file.

DESCRIPTION

This error is a result of syntax errors in the MPML file, which is being compiled using the **load_mpm** command.

WHAT NEXT

Fix errors in the source MPML file and reload it using the **load_mpm** command.

PWR-151 (error) Error in executing the code in an MPM.

DESCRIPTION

This error occurs during the execution of the code in an MPM during the power estimation process. It is due to a logical error in the MPML file source file describing the MPM.

WHAT NEXT

Debug the MPM using the **test_mpm** command and make changes in the source MPML file. Reload the corrected MPM using the **load_mpm** command and use the updated library to estimate power.

PWR-152 (error) Error while linking MPM with design object.

DESCRIPTION

This error is due to a failure to link a power model with a design object. The most

likely cause is a mismatch in pin definitions between the MPM and the design object it is being used for. The mismatch can result from different pin names, different pin sizes, or missing pins.

WHAT NEXT

Change the pin definitions in the MPML file to be consistent with the pin definition of the design object.

PWR-153 (error) Error while calculating library information.

DESCRIPTION

This error is due to an error in initialization of library related information for use with an MPM.

WHAT NEXT

Check if the target_library environment variable is set to the desired library.

PWR-154 (error) No library name specified in the parameter for -mpm_name option.

DESCRIPTION

The -mpm_name option requires a string of the form "mpm_lib/mpm_name", where the mpm_lib is the name of the library and the mpm_name is the name of the MPM in the library.

WHAT NEXT

Use the command with the name of the library specified.

PWR-155 (error) One and only one option (-prop_sa|-sim|-dynamic_power| -static_power) can be used with the **test_mpm**

command.

DESCRIPTION

The **test_mpm** command tests individual functions inside the MPM. Every invocation of the command can test only one function at a time.

WHAT NEXT

Use only one option (-prop_sa|-sim|-dynamic_power|-static_power).

PWR-156 (error) Wrong combination of options while defining association. The -remove cannot be used with the %s option.

DESCRIPTION

Commands that define the associations between MPMs and design components (set_mpm_on_instance, set_mpm_on_lib_cell and set_reference_on_mpm) are also used to remove existing associations. The -remove option is used to remove existing associations. This option cannot be used with the -mpm_name (for the set_mpm_on_instance and set_mpm_on_lib_cell commands), or the -reference option (for the set_reference_on_mpm command), which are used to set the associations.

WHAT NEXT

Use the command with only one option (-remove or -mpm_name/-reference).

PWR-157 (error) Wrong combinations of options for the load_mpm command. One, and only one of the two options -compile_only and -mpm_name can be used. The -newlib option can be used only with the -mpm_name option.

DESCRIPTION

The **load_mpm** command is used to compile MPML code and load it into a library. If the -compile_only option is used, the code is checked for syntax errors, but it is not loaded into a library. The -compile_only option cannot be used with the -mpm_name or the -newlib option.

WHAT NEXT

In case you are interested in detecting syntax errors, only use the -compile_only option. If you want to compile the MPML and load it into a library as an MPM, use the -mpm_name option.

PWR-158 (error) MPM %s not found in library %s.

DESCRIPTION

The specified library does not contain the desired MPM.

WHAT NEXT

Check if the MPM name is misspelt.

PWR-159 (error) %s file %s not found.

DESCRIPTION

The specified file was not found in search path. The filename might be misspelt or the file might not exist in the search_path.

WHAT NEXT

Check to see if the file exists and the search_path variable is set properly.

PWR-160 (error) The design contains cells other than combinational ones.

DESCRIPTION

The command is intended for combinational designs only.

WHAT NEXT

For other types of designs, look at your characterization methods manual.

PWR-161 (error) Unable to write to file %s.

DESCRIPTION

The file is either protected of an invalid file name has been specified.

WHAT NEXT

Change the permissions for this file or respecify another file name using the -output option .

PWR-162 (warning) The switching activity propagation model is too large.

DESCRIPTION

This warning occurs when a arithmetic block suitable for mpm_propagate_logic is modelled with its switching activity propagation. Typical examples are huge multipliers and dividers, where those can be nicely described with a brief arithmetic mpm_propagate_logic model.

WHAT NEXT

You can still use the automatically generated model at your discretion. Reexamine the designs and if it is an arithmetic block, model it with mpm_propagate_logic.

PWR-163 (error) Internal error in the MPM module.

DESCRIPTION

This error is due to an internal error in the MPM module.

WHAT NEXT

Check if the MPML file used to create the MPM has the correct syntax.

PWR-164 (error) MPM %s already exists in the library %s.

DESCRIPTION

This error occurs, when the load_mpm or the copy_mpm or the rename_mpm command is used to add/rename an MPM to a library which already has one with the same name. These commands do not overwrite an existing MPM in a library.

WHAT NEXT

If you want to replace the existing MPM, use the delete_mpm command followed by the load_mpm/copy_mpm/rename_mpm command.

PWR-165 (error) Cannot use -remove option with -mpm_name option.

DESCRIPTION

This error occurs when either the set_mpm_on_instance or the set_mpm_on_lib_cell command is used with both the -remove and the -mpm_name options. You can either set an attribute on the instance/lib_cell by specifying the MPM using the -mpm_name option, or remove the attribute using the -remove option, but cannot do both simultanously.

WHAT NEXT

If you want to remove the attribute, use the -remove option. If you want to add an attribute, use the -mpm_name option.

PWR-166 (error) Cannot use -remove option with -reference option.

DESCRIPTION

This error occurs when the set_reference_on_mpm command is used with both the -remove and the -reference options. You can either set an attribute on the MPM using the -reference option, or remove the attribute using the -remove option, but cannot do both simultaneously.

WHAT NEXT

If you want to remove the attribute on the MPM, use the -remove option. If you want

to add an attribute on the MPM, use the -reference option.

PWR-167 (error) Neither -referene nor -remove option specified.

DESCRIPTION

This error occurs when the set_reference_on_mpm command is used without either the -remove or the -reference option. At least one option has to be specified.

WHAT NEXT

If you want to remove the attribute, use the -remove option. If you want to add an attribute, use the -reference option.

PWR-168 (error) Neither -mpm_name nor -remove option specified.

DESCRIPTION

This error occurs when either the set_mpm_on_instance or the set_mpm_on_lib_cell command is used without either the -remove or the -mpm_name option. At least one option has to be specified.

WHAT NEXT

If you want to remove the attribute, use the -remove option. If you want to add an attribute, use the -mpm_name option.

PWR-169 (error) Wrong combinations of options for the load_mpm command. The -newlib option has to be used with the -mpm_name option.

DESCRIPTION

The **load_mpm** command is used to compile an MPML file and load it into a library. The -newlib option is used to create a new library object to store the MPM. This option can be used only with the -mpm_name option.

WHAT NEXT

In case you are interested in detecting syntax errors only, use the -compile_only option. If you want to compile the MPML file and create a new library to store the MPM, use the -newlib along with the -mpm_name options.

PWR-170 (error) The %s with name %s that was specified for clock gating only has inverted outputs.

DESCRIPTION

An invalid option value has been specified. The complete command will be ignored, and the clock gating style, if defined, is not changed.

WHAT NEXT

The set_clock_gating_style command terminates without changing the clock gating style. Refer to the appropriate documentation for correct usage of the option.

PWR-171 (information) The library cell %s specified for clock gating has the dont_use and the is_clock_gating_cell attribute set.

DESCRIPTION

The specified library cell has the dont_use attribute set. This is ok since the library cell has the is_clock_gating_cell attribute set to true as well.

WHAT NEXT

Continue.

PWR-173 (error) Creating a reference for the library cell %s is not possible since another reference with the same name exists already.

DESCRIPTION

The **set_clock_gating_style** command has specified a certain library cell to be used

in the clock gating circuitry. A reference for this library cell cannot be built because the current design already has a reference that has the same name and refers to a different design.

WHAT NEXT

Check the other reference with the same name. If it refers to a subdesign, give the subdesign a different name. If the reference refers to another library cell, chose a different library cell.

PWR-174 (error) Library %s already exists in memory.

DESCRIPTION

The -newlib option is used to create a new library object to store the MPM. However, if the library specified with the -mpm_name option already exists in memory, a new library is not created.

WHAT NEXT

If you wish to create a new library, check that a library with the same name does exist already. In case you wish to create another library with the same name, remove the old library from dc_shell using the **free** command. The new library created with the -newlib option will replace the old library in memory.

PWR-175 (error) Cannot use -newlib option for a library which already exists in memory.

DESCRIPTION

The -newlib option is used to create a new library object to store the MPM. However, if the library specified with the -mpm_name option already exists in memory, a new library is not created.

WHAT NEXT

If you wish to create a new library, check that a library with the same name does exist already. In case you wish to create another library with the same name, remove the old library from dc_shell using the **free** command. The new library created with the -newlib option will replace the old library in memory.

PWR-180 (warning) There is no %s cell in the target library,

assuming 0 power for these cells

DESCRIPTION

If your design contains cells of this type, you need to have the associated cells in the target library. Otherwise, we cannot correctly estimate the power of these cells. We will assume 0 for these types of cells.

WHAT NEXT

Need to respecify target_library to include library which contains these types of cells.

PWR-181 (warning) 'hookup_power_gating_ports' command failed to connect any ports of the design.

DESCRIPTION

The command 'hookup_power_gating_ports' failed because either there is no port to be stitched or all the power gating pins were already stitched.

WHAT NEXT

Check whether there is power_gating_pin attributes on the retention registers. Verify that those pins were not driven by non constant logics.

PWR-182 (warning) Pin '%s' of cell '%s' was already driven by pin or port '%s' with incompatible power_gating_pin/power_gating_style attributes.

DESCRIPTION

This happens in 'hookup_power_gating_ports' command when a pin with

power_gating_pin/power_gating_style attribute was driven by a port/cell without the attribute or with different values of the attribute. The pin will be skiped in 'hookup_power_gating_ports' command.

WHAT NEXT

Check the power_gating_pin/power_gating_style attributes on the pin and port and make sure the attributes are the same.

PWR-183 (warning) Pin '%s' of hierarchical cell '%s' was driving %d pin(s) with incompatible power_gating_pin attribute.

DESCRIPTION

This happens in 'hookup_power_gating_ports' command when a hierarchical pin with power_gating_pin attribute driving pins without the attribute or with different values of the attribute. The 'hookup_power_gating_ports' command will still hookup the hierachical pin to the higher level of hierarchy.

WHAT NEXT

Check the power_gating_pin attributes on the pins and make sure these are the intended behavior;

PWR-184 (warning) There are multiple ports with the same 'power_gating_pin/power_gating_style' attribute in design '%s'. Port '%s' will be used to hook up the power gating pins in the design.

DESCRIPTION

This happens in 'hookup_power_gating_ports' command when a design/sub-design has multiple ports with the same power_gating_pin/power_gating_style attributes. In this situation, only one port is used to hook up all the power gating pins inside the design.

WHAT NEXT

Check the design to make sure only one port has one type of power gating pin.

PWR-185 (warning) Port/pin '%s' of design/cell '%s' was driving %s pins

with incompatible ’power_gating_pin’ attribute.

DESCRIPTION

This happens in ’hookup_power_gating_ports’ command when a a port/pin of the design/cell with power_gating_pin attribute was driving pins without the attribute or with different values of the attribute. The ’hookup_power_gating_ports’ command will still use this port to hook up the power gating pins in the design.

WHAT NEXT

Check the power_gating_pin attributes on the port/pins and make sure these are what you want.

PWR-186 (error) Port/pin ’%s’ of design/cell ’%s’ was driving pin ’%s’ of retention register or hierarchical cell ’%s’ with incompatible ’power_gating_pin/power_gating_style’ attributes.

DESCRIPTION

This happens in ’hookup_power_gating_ports’ command when a a port/pin of the design/cell with power_gating_pin/power_gating_style attribute driving a pin of the retention register or the hierarchical cell without the attributes or with different values of the attributes. The ’hookup_power_gating_ports’ command will not use this port to hook up the power gating pins in the design.

WHAT NEXT

Check the power_gating_pin/power_gating_style attributes on the port/pins and correct the attributes.

PWR-187 (error) Design ’%s’ was not uniquified. Command failed.

DESCRIPTION

Command **hookup_power_gating_ports** requires the design to be uniquified.

WHAT NEXT

Uniquify the design before using **hookup_power_gating_ports** command.

PWR-188 (error) Can’t find any object for ’set_power_gating_signal’ command.

DESCRIPTION

Can not find objects (pins or ports) in the design from the object specified in ’set_power_gating_signal’ command.

WHAT NEXT

Check the argument of ’set_power_gating_signal’ command and try again.

PWR-189 (warning) Can not set power gating signal on pin/port ’%s’ because
the object has already had a different types of power gating signal.

DESCRIPTION

This happens when ’set_power_gating_signal’ command tries to set the signal on the pin/port which has already had a different type of signal.

WHAT NEXT

Check the arguments of ’set_power_gating_signal’ command and try again.

PWR-190 (error) The library cell %s specified for use as an integrated clock gating does not exist in the libraries specified.

DESCRIPTION

The library cell specified for use as an integrated clock gating cell does not exist in the libraries specified. This may be because either (a) you specified a wrong library or (b) you specified a wrong cell in the set_clock_gating_style command.

WHAT NEXT

Check your target libraries and the set_clock_gating_style command.

PWR-191 (error) The library cell required for use as an integrated clock gating does not exist in the libraries specified. The required attribute is %s.

DESCRIPTION

The library cell with the appropriate attribute required for use as an integrated clock gating cell does not exist in the libraries specified. This may be because either (a) you specified a wrong library , or (b) you specified a wrong cell in the set_clock_gating_style command.

WHAT NEXT

Check your target libraries and the set_clock_gating_style command.

PWR-192 (error) The library cell %s specified for use as an integrated clock gating does not have the correct value for the clock_gating_integrated_cell attribute. The attribute required is %s.

DESCRIPTION

The library cell specified for use as an integrated clock gating cell does not have the correct value for the clock_gating_integrated_cell attribute. This may be because either (a) you specified a wrong library, or (b) you specified a wrong cell in the set_clock_gating_style command or (c) the functionality of the specified cell does not match the functionality required by the set_clock_gating_style command.

WHAT NEXT

Check your target libraries and the set_clock_gating_style command.

PWR-193 (error) The library cell %s specified for use as an integrated clock gating does not have the clock_gating_integrated_cell attribute. The value required for

this attribute is %s.

DESCRIPTION

The library cell specified for use as an integrated clock gating cell does not have the clock_gating_integrated_cell attribute. This may be because either (a) you specified a wrong library, or (b) you specified a wrong cell in the set_clock_gating_style command or (c) you did not specify the clock_gating_integrated_cell on the specified cell.

WHAT NEXT

Check your target libraries and the set_clock_gating_style command.

PWR-194 (error) Invalid option for the set_clock_gating_style command. If you specify the "integrated" option for the -positive_edge_logic or -negative_edge_logic options, you cannot specify any inverters/buffers before or after it.

DESCRIPTION

If you specify the "integrated" option for the -positive_edge_logic or -negative_edge_logic options, you cannot specify any inverters/buffers before or after it.

WHAT NEXT

Re-enter the set_clock_gating_style command.

PWR-195 (warning) The setup and hold values are ignored for the integrated cell. For these cells the setup and hold must be specified on the library.

DESCRIPTION

If you specify the "integrated" option for the -positive_edge_logic or -negative_edge_logic options, an integrated clock gating cell from the library will be used. In this case, any values specified for the -setup and -hold options will be ignored for the integrated styles and used only for the non-integrated cells. If you have specified "integrated" for only one of the -positive_edge_logic or -

negative_edge_logic options, the setup and hold values will be used for the non-integrated clock gating style only. If you have specified "integrated" for both the -positive_edge_logic and -negative_edge_logic options, then the setup and hold values will be ignored completely.

WHAT NEXT

This is only a warning, you should be aware of what will happen.

PWR-196 (Error) The value of the "clock_gating_integrated_cell" attribute (%s) is not a valid value. Please correct this.

DESCRIPTION

The value of the "clock_gating_integrated_cell" attribute (%s) is not valid. Check the value of this attribute on both the library cell and the clock gating design cell.

WHAT NEXT

You need to check the value of this attribute on both the library cell and the clock gating design cell and make sure you have a correct attribute.

PWR-197 (error) Could not find the exact pin matches with the integrated clock gating cell %s.

DESCRIPTION

Could not get the exact pin matches to connect the integrated cell in place of the current clock gating circuit.

WHAT NEXT

Check the pin connections on the library cell and make sure that they are correct.

PWR-198 (error) Could not find design port %s on the clock

gating design %s.

DESCRIPTION

The ports of a clock gating design added by Power Compiler have specific names. One of the ports required on the design could not be found.

WHAT NEXT

Make sure the this port exists on the clock gating design.

PWR-199 (error) Could not find the %s pin with the correct attribute on the specified integrated clock gating cell %s.

DESCRIPTION

Could not find the pin with the required attribute in the integrated clock gating cell specified.

WHAT NEXT

Check the attributes on the pins on the integrated clock gating library cell and make sure that they are correct.

PWR-200 (warning) The design has existing user-annotated switching activity data; not all such data is overwritten by the SAIF file.

DESCRIPTION

The design has user-annotated switching activity data on some nets, ports and/or pins. It is detected that the SAIF file does not overwrite all such data.

WHAT NEXT

This is a warning. If it is expected that the current design is not annotated with any switching activity information before this command, then use the **reset_switching_activity** command to clean up all user-annotated switching activity, and read the SAIF file again.

SEE ALSO

reset_switching_activity (2)

PWR-201 (error) Can’t find the %s file (%s).

DESCRIPTION

The specified file was not found in the search path. The filename might be misspelt or the file might not exist in the search_path.

WHAT NEXT

Check to see if the file exists and the search_path variable is set properly.

PWR-202 (error) Currently, BC does not support the integrated clock gating cell.

DESCRIPTION

User set clock gating style to use integrated cell. However, BC does not support the integrated clock gating cell.

WHAT NEXT

Reset the clock gating style using the command set_clock_gating_style to non integrated clock gating cell.

PWR-203 (warning) Clock %s related to max_toggle_rate object %s no longer exists.

DESCRIPTION

This warning occurs when max_toggle_rate information for the net/pin is specified with the -clock option of the **max_toggle_rate** command and the given clock no longer exists in the design.

WHAT NEXT

This is a warning. The related clock is ignored.

PWR-204 (warning) There are conflicting set_max_toggle_rate commands on object %s.

DESCRIPTION

This error occurs when there are two (or more) **set_max_toggle_rate** commands on different nets or pins within the same physical connection specifying different values for toggle rates and static probability.

WHAT NEXT

Remove the unnecessary **set_max_toggle_rate** commands for the reported net or pin.

PWR-205 (information) The derived max_toggle_rate value (%f) for the clock net '%s' conflicts with the value annotated with the set_switching_activity command (%f). Using the %f value.

DESCRIPTION

During electromigration analysis, **max_toggle_rate** information is derived for clock nets from clock waveforms that were set by **create_clock**. This informational message indicates that the derived value conflicts with the value that was explicitly annotated on the net by **set_max_toggle_rate**.

The tool will usually override the derived value with your annotated switching information.

WHAT NEXT

If this behavior is acceptable, you need not do anything. However, if you want the derived clock information used, reset the annotated **max_toggle_rate** information by executing **set_max_toggle_rate** with no options.

PWR-210 (warning) The clock gating design has more than one cell with clock-gating setup or hold attributes. Only of the setup and one of the hold attributes will be transfered to the integrated

cell.

DESCRIPTION

The clock gating design has more than one cell with clock-gating setup or hold attributes. Only of the setup and one of the hold attributes will be transfered to the integrated cell.

WHAT NEXT

This is a warning. Its best to make sure that only one of the cells in the clock gating design had the setup and hold attributes, to make sure that the correct one is being copied. Please remove one of them using the "remove_clock_gating_check" command.

PWR-211 (error) Object '%s' is not a net or cell.

DESCRIPTION

You receive this message if you have specified an object other than *net* or *cell* for **report_saif -only**. You must specify either *net* or *cell*; no other objects are accepted.

WHAT NEXT

Re-execute the **report_saif** command and specify either *net* or *cell* with the **-only** option.

SEE ALSO

report_saif(2).

PWR-212 (error) -type option accepts only rtl or gate name.

DESCRIPTION

You receive this message if you specify something other than *rtl* or *gate* as the argument of the **-type** option of the **report_saif** command. You must use either *rtl* or *gate*.

WHAT NEXT

Identify the level of the current_design (that is, rtl or gate-level) and re-execute

report_saif using the appropriate argument (*rtl* or *gate*) for the **-type** option.

SEE ALSO

report_saif(2).

PWR-213 (warning) The report_saif command was called without specifying either -type gate or -type rtl. Using the default (gate).

DESCRIPTION

You receive this message if you issue the **report_saif** command without specifying the **-type** option with the argument *rtl* or *gate*. This message informs you that the default, *gate*, will be used.

WHAT NEXT

If *gate* is the correct level type for your design, no action on your part is required, but for clarity you might want to re-execute **report_saif** using **-type gate**. However, if *rtl*, and not *gate*, is the correct level type for your design, re-execute **report_saif** using **-type rtl**.

SEE ALSO

report_saif(2).

PWR-214 (error) -input_list option expects -input .

DESCRIPTION

The -input_list option of the merge_saif command expects -input .

WHAT NEXT

Correct the *-input_list* option and run the command again.

PWR-215 (error) -input_list option expects -weight .

DESCRIPTION

The -input_list option of the merge_saif command expects -weight .

WHAT NEXT

Correct the *-input_list* option and run the command again.

PWR-216 (error) Error in read_saif process.

DESCRIPTION

The merge_saif command cannot read saif file.

WHAT NEXT

Check the saif file, correct the errors and run the command again.

PWR-217 (Error) Empty list in input_list option.

DESCRIPTION

Empty list in input_list option for merge_saif command.

WHAT NEXT

Correct the *-input_list* option and run the command again.

PWR-218 (Error) Weight value must be between 0 and 100.

DESCRIPTION

In merge_saif command, input_list option accepts only weight value between 0 and 100.

WHAT NEXT

Correct the *-input_list* option and run the command again.

PWR-219 (Error) The number of saif files is different of the number of weights in input_list.

DESCRIPTION

In merge_saif command, The number of saif files must be equal to the number of weights in input_list option.

WHAT NEXT

Correct the *-input_list* option and run the command again.

PWR-220 (Error) The sum of weights must be 100.

DESCRIPTION

In input_list option, the sum of weights must be 100.

WHAT NEXT

Correct the *-input_list* option and run the command again.

PWR-221 (error) The -only option cannot be used with -gated -ungated or the -gating_element options.

DESCRIPTION

The report_clock_gating command can either produce a design specific report using the -gated, -ungated and -gating_element options; or it can produce a report about specific cells via the -only option.

WHAT NEXT

Use either the instance-specific -only option or the design specific -gated, -ungated or the -gating elements options.

PWR-222 (information) Producing default clock-gating report.

DESCRIPTION

You receive this message if you issue the **report_clock_gating** command without options. In that case, **report_clock_gating** displays a default report, as the message states.

WHAT NEXT

This is an informational message only; if you are satisfied with the default report, no action is required on your part. Otherwise, reissue the **report_clock_gating** command with any of the available options.

SEE ALSO

report_clock_gating (2).

PWR-224 (Information) -simple_merge option is not set, default is -cps_propagation.

DESCRIPTION

You receive this informational message when you do not specify an option for the **merge_saif** command. By default, the option is set to **-cps_propagation**.

WHAT NEXT

If you are satisfied with the default option set for the **merge_saif** command, no action is required on your part. If yo are not satisfied with the default setting, set the desired option for the command.

PWR-225 (Error) SDPD is not supported in this release.

DESCRIPTION

In merge_saif command, SDPD is not supported in this release.

WHAT NEXT

Please use non-SDPD switching activity and try this command again.

PWR-226 (Error) SAIF files must have the same time unit.

DESCRIPTION

In merge_saif command, SAIF files must have the same time unit.

WHAT NEXT

Please regenerate your saif files with the same time unit and try this command again.

PWR-227 (information) The library cell '%s' in the library '%s' is not characterized for %s power.

DESCRIPTION

The given library cell is not characterized for leakage power, internal power or both. A leakage and/or internal power value of 0 is assumed for this cell; Since this power value may not be accurate, power optimizations may not use this cell effectively and power analysis of designs containing instances of this cell may not be accurate.

WHAT NEXT

This is an information message. Please contact your library vendor if you believe that this library cell needs the missing leakage and/or internal power characterization.

PWR-228 (information) The design contains cells, other than constants and black boxes, that are not characterized for %s power.

DESCRIPTION

This information message is issued when power calculations are performed on the current design and it contains instances of library cells that are not characterized for leakage power, internal power or both. The missing leakage and/or internal power values in the characterization are assumed to be 0.

WHAT NEXT

This is an information message. Please contact your library vendor if you believe that power characterization is needed for your design.

PWR-229 (information) The cells in your design are not characterized for %s power.

DESCRIPTION

This information message is issued when power calculations are performed on the current design and none of the cells are characterized for leakage power, internal power or both. In such cases, the missing leakage and/or internal power is assumed to be 0.

WHAT NEXT

This is an information message. Please contact your library vendor if you believe that power characterization is needed for your design.

PWR-230 (Information) %s power model preference is frozen to %s, it cannot be changed later in the flow.

DESCRIPTION

This message is to inform user that the power model preference is set with the above value, and is frozen for the rest of the flow. This is to prevent the user from changing power model preference from NLPM to CCS later in the flow, while CCS power data are pruned away.

WHAT NEXT

Do not modify the power model preference after the first library load.

PWR-231 (error) No clock-gated register specified as an argument to the group_clock_gated_registers command

DESCRIPTION

The argument to the -registers option of the group_clock_gated_registers command

should contain a list of clock-gated registers.

WHAT NEXT

Check that all the members of the argument to the -registers option are valid clock-gated registers. Use the report_clock_gating command to find a list of clock-gated registers.

PWR-232 (error) %s is not a clock-gated register.

DESCRIPTION

The argument to the -registers option of the group_clock_gated_registers command should contain a list of clock-gated registers. All registers should be clock-gated.

WHAT NEXT

Check that all the members of the argument to the -registers option are valid clock-gated registers. Use the report_clock_gating command to find a list of clock-gated registers.

PWR-233 (error) Clock-gated registers do not belong to the same design instance.

DESCRIPTION

The argument to the -registers option of the group_clock_gated_registers command should contain a list of clock-gated registers which are in the same level of hierarchy. Clock-gated registers under different hierarchies cannot be grouped together.

WHAT NEXT

Check that all the members of the argument to the -registers option are clock-gated registers under the same level of hierarchy. Use the report_clock_gating command to find a list of clock-gated registers.

PWR-234 (error) Cannot use both -default and -exclusive

options together.

DESCRIPTION

The -default and -exclusive options are mutually exclusive. Use -default to remove the cells from a user-defined group. Use -exclusive to create a new group which will have its own separate clock-gating cell. The clock-gating cell used to gate these registers will not gate any other registers

WHAT NEXT

Either use the -default option or the -exclusive option for the group_clock_gated_registers command. Use the report_clock_gating command to find a list of clock-gated registers.

PWR-235 (warning) Cannot annotate the cell '%s' with the switching activity for the SAIF condition '%s'.

DESCRIPTION

The given state condition is not valid for annotating state-dependent static probabilities on the given cell. This usually occurs when the gate-level SAIF file is read on a different design than the one used to generated the SAIF file. For example, the design has been modified using an implementation step (like compile -inc). Alternatively the design is linked with a different library than the one used when generating the backward SAIF file. If the SAIF file is generated using a simulation flow, the link library may be different from the one used to generate the library forward SAIF.

WHAT NEXT

Check that the backward SAIF file being read is intended for the current design.

PWR-236 (warning) Cannot annotate the pin '%s' with the switching activity for the SAIF condition '%s'.

DESCRIPTION

The given state condition is not valid for annotating state-dependent toggle rates on the given pin. This usually occurs when the gate-level SAIF file is read on a different design than the one used to generated the SAIF file. For example, the design has been modified using an implementation step (like compile -inc). Alternatively the design is linked with a different library than the one used when

generating the backward SAIF file. If the SAIF file is generated using a simulation flow, the link library may be different from the one used to generate the library forward SAIF.

WHAT NEXT

Check that the backward SAIF file being read is intended for the current design.

PWR-237 (warning) Cannot annotate the pin '%s' with the switching activity for the SAIF path source '%s'.

DESCRIPTION

The given path source is not valid for annotating path-dependent toggle rates on the given pin. This usually occurs when the gate-level SAIF file is read on a different design than the one used to generated the SAIF file. For example, the design has been modified using an implementation step (like compile -inc). Alternatively the design is linked with a different library than the one used when generating the backward SAIF file. If the SAIF file is generated using a simulation flow, the link library may be different from the one used to generate the library forward SAIF.

WHAT NEXT

Check that the backward SAIF file being read is intended for the current design.

PWR-238 (warning) Cannot annotate the pin '%s' with the switching activity for the SAIF condition '%s' and path source '%s'.

DESCRIPTION

The given state condition and path source are not valid for annotating state-dependent and path-dependent toggle rates on the given pin. This usually occurs when the gate-level SAIF file is read on a different design than the one used to generated the SAIF file. For example, the design has been modified using an implementation step (like compile -inc). Alternatively the design is linked with a different library than the one used when generating the backward SAIF file. If the SAIF file is generated using a simulation flow, the link library may be different from the one used to generate the library forward SAIF.

WHAT NEXT

Check that the backward SAIF file being read is intended for the current design.

PWR-239 (warning) Removing invalid SDPD switching activity from cell '%s'.

DESCRIPTION

The state-dependent static probabilities annotated on the given cell and/or the state-dependent and/or path-dependent toggle rates annotated on the pins of the given cell are invalid and are being removed so that power can be calculated. For this particular cell, Power Compiler will estimate the required SDPD switching activities instead of using the annotated ones. The reason that the SDPD switching activity is invalid is likely to be that the design is linked with a technology library that has different states/paths in its power characterization than the one used when the SDPD activity was annotated.

WHAT NEXT

This is a warning message; check that the intended link library is specified.

PWR-240 (error) Neither static_probability nor toggle_rate specified.

DESCRIPTION

Either the static_probability or the toggle rate must be spcified, if either the period or the clock is specified. If none of these four options are specified, the command will reset switching activity on the objects specified.

WHAT NEXT

If you want to annotate activity, you must enter a valid value for at least one of these: -static_probability or -toggle_rate. If you want to reset activity, make sure that you have none of the following options specified: -static_probability, -toggle_rate, -clock, -period.

PWR-241 (error) Invalid value %s for the -select option.

DESCRIPTION

The valid values for the -select option are "regs" "ports" or "all". Please check the man pages to find out the meaning of each of these. The value specified is not valid.

WHAT NEXT

Please specify a valid value for the -select option.

PWR-242 (error) Invalid value %s for the -type option.

DESCRIPTION

The valid values for the -type option are "datapath" or "control". Please check the man pages to find out the meaning of each of these. The value specified is not valid.

WHAT NEXT

Please specify a valid value for the -type option.

PWR-243 (information) Resetting switching activity for the specified objects.

DESCRIPTION

Since none of the following options: -static_probability, -toggle_rate, -clock, and -period, were specified switching activity will be reset to the default values on the objects specified.

WHAT NEXT

If you want to annotate activity, you must enter a valid value for at least one of these: -static_probability or -toggle_rate; and should also specify a value for -period or -clock.

PWR-250 (error) Specification of cell internal power must be for a pin.

DESCRIPTION

You receive this message if you issue the **set_cell_internal_power** command without specifying at least one pin name as an argument, or if a name you specified is not the name of a pin in your design. The *pin_names* argument is required for **set_cell_internal_power**, and names supplied for this argument must represent pins in your design.

WHAT NEXT

Verify the correct spelling of names of pins in your design for which you want to set the cell internal power, and re-issue **set_cell_internal_power** with correct pin names.

SEE ALSO

set_cell_internal_power(2).

PWR-251 (error) Command %s not supported in pe_shell.

DESCRIPTION

This command is not supported in pe_shell. In order to use it you must use the more powerful dc_shell.

WHAT NEXT

Use *dc_shell*.

PWR-252 (warning) RTL-Power-Analysis license must already by checked out for this command to run, and you should be in pe_shell.

DESCRIPTION

RTL-Power-Analysis license must already by checked out for this command to run.

WHAT NEXT

Please use pe_shell, not dc_shell. Also, make sure you have the RTL-Power-Analysis license.

PWR-253 (warning) RTL-Power-Analysis license not available.

DESCRIPTION

RTL-Power-Analysis license not available.

WHAT NEXT

Please set up RTL-Power-Analysis license and *run pe_shell* again.

PWR-254 (Error) Error detected while reading design.

DESCRIPTION

You receive this message from **create_power_model** to inform you that it has stopped executing because an error was detected while reading the design. This message is issued in addition to a similar message issued earlier.

WHAT NEXT

You would have received at least one other error message prior to this one. Examine the messages, identify the message that relates to reading the design, and use the information in that message to help you correct the error. Then reexecute **create_power_model**.

SEE ALSO

create_power_model (2).

PWR-255 (Error) Error detected while reading constraints.

DESCRIPTION

You receive this message from **create_power_model** to inform you that it has stopped executing because an error was detected while reading constraints. This message is issued in addition to a similar message issued earlier.

WHAT NEXT

You would have received at least one other error message prior to this one. Examine the messages, identify the message that relates to reading constraints, and use the information in that message to help you identify and correct the error. Then reexecute **create_power_model**.

SEE ALSO

create_power_model (2).

PWR-256 (Error) Error detected while creating models.

DESCRIPTION

You receive this message from **create_power_model** to inform you that it has stopped executing because an error was detected while creating models. This message is issued in addition to a similar message issued earlier. The error could possibly be caused by an incorrect setting of the **link_library** or **target_library** variables.

WHAT NEXT

You would have received at least one other error message prior to this one. Examine the messages, identify the message that relates to reading the design, and use the information in that message to help you identify and correct the error. Also, verify that the **link_library** and **target_library** variables are set correctly. Then reexecute **create_power_model**.

SEE ALSO

create_power_model (2); **link_library** (3), **target_library** (3).

PWR-257 (Error) Error detected while reading switching activity.

DESCRIPTION

You receive this message from **estimate_power** to inform you that it has stopped executing because an error was detected while reading the switching activity file. This message is usually issued in addition to a similar message issued earlier; if no earlier message is issued, the problem might be with an incorrect SAIF instance name.

WHAT NEXT

You might have received at least one other error message prior to this one. Examine the messages, identify the message that relates to reading the switching activity file, and use the information in that message to help you identify and correct the error. If you did not receive any other error messages and you used the **-saif** option, verify that the **-saif** *instance_name* argument is correct.

SEE ALSO

estimate_power (2).

PWR-258 (Error) Error detected while reporting RTL power

estimation.

DESCRIPTION

You receive this message from **estimate_power** to inform you that it has stopped executing because an error was detected while reporting the RTL power estimation. This message is issued in addition to a similar message issued earlier.

WHAT NEXT

You would have received at least one other error message prior to this one. Examine the messages, identify the message that relates to reporting RTL pwer estimation, and and use the information in that message to help you identify and correct the error.

SEE ALSO

estimate_power (2).

PWR-259 (Error) link_library not set or empty.

DESCRIPTION

You receive this message from **create_power_model** or **estimate_power** if the **link_library** variable is not set, or if a library it points to is empty. Before executing these commands, you must set the **link_library**, **synthetic_library**, and **target_library** variables.

WHAT NEXT

Set the **link_library** variable to a valid list of designs and libraries to be used during linking. Then reissue the **create_power_model** or **estimate_power** command.

SEE ALSO

create_power_model (2), **estimate_power** (2); **link_library** (3), **synthetic_library** (3), **target_library** (3).

PWR-260 (Error) target_library not set or empty.

DESCRIPTION

You receive this message from the **create_power_model** or **estimate_power** command if

the **target_library** variable is not set, or if a library it points to is empty. Before executing these commands, you must set the **link_library**, **synthetic_library**, and **target_library** variables.

WHAT NEXT

Set the **target_library** variable to a valid list of technology libraries of components to be used when compiling your design. Then reissue the **create_power_model** or **estimate_power** command.

SEE ALSO

create_power_model (2), **estimate_power** (2); **link_library** (3), **synthetic_library** (3), **target_library** (3).

PWR-261 (Error) The option "-format" is required.

DESCRIPTION

You receive this message if you issue the **create_power_model** or **estimate_power** command without the **-format** option. The **-format** option is required.

WHAT NEXT

Reissue the command and specify either **-format vhdl** or **-format verilog**.

create_power_model (2), **estimate_power** (2).

PWR-262 (Error) HDL designs required to read in.

DESCRIPTION

You receive this message if you issue the **create_power_model** or **estimate_power** command without the **-hdl_files** option; or if the list contains a file that is not a Verilog or VHDL file. The **-hdl_files** option is required, and only Verilog and VHDL are valid formats.

WHAT NEXT

Reissue the command and specify **-hdl_files** with a list of files that are either all Verilog or all VHDL.

SEE ALSO

create_power_model (2), **estimate_power** (2).

PWR-263 (Error) The option "-top_design" is required.

DESCRIPTION

You receive this message if you issue the **create_power_model** or **estimate_power** command without the **-top_design** option. The **-top_design** option is required.

WHAT NEXT

Reissue the command and specify **-top_design** with the name of your top-level design.

SEE ALSO

create_power_model (2), **estimate_power** (2).

PWR-264 (Error) Too many arguments for the -saif option.

DESCRIPTION

You receive this message if you issue the **estimate_power** command with the **-saif** option and enter more than two arguments for **-saif**. This option requires two arguments, as follows:

-saif {*saif_file_name instance_name*}

where *instance_name* is the name of the instance in the SAIF file.

WHAT NEXT

Reissue the **estimate_power** command and use only the *saif_file_name* and *instance_name* arguments for the **-saif** option.

SEE ALSO

estimate_power (2).

PWR-266 (Error) Cannot find saif file (%s).

DESCRIPTION

You receive this message if you issue the **estimate_power** command with the **-saif** option and the named SAIF file cannot be found. The file might not be in your search path; or, the error could be caused by a spelling error or typo.

WHAT NEXT

Check the SAIF filename and verify that the file exists, that its name is spelled correctly, and that it is in your search path. Then reissue the **estimate_power** command with the correct SAIF filename.

estimate_power (2).

PWR-267 (Error) Activity file not found.

DESCRIPTION

You receive this message if you issue the **estimate_power** command with the **-activity_file** option and the named activity file could not be found. The file might not be in your search path; or, the error could be caused by a spelling error or typo.

WHAT NEXT

Check the activity filename and verify that the file exists, that its name is spelled correctly, and that it is in your search path. Then reissue the **estimate_power** command with the correct activity filename.

estimate_power (2).

PWR-268 (Error) -saif and -activity_file options are mutually exclusive.

DESCRIPTION

You receive this message if you issue the **estimate_power** command with both the **-saif** and **-activity_file** options. You must use one of these options, but you cannot use both.

WHAT NEXT

Reissue the **estimate_power** command with either the **-saif** or **-activity_file** option, but not both.

SEE ALSO

estimate_power (2).

PWR-269 (Error) The -saif option requires two arguments (saif_file_name and instance_name).

DESCRIPTION

You receive this message if you issue the **estimate_power** command with the **-saif** option and do not enter two arguments for **-saif**. This option requires two arguments, as follows:

-saif {*saif_file_name instance_name*}

where *instance_name* is the name of the instance in the SAIF file.

WHAT NEXT

Reissue the **estimate_power** command and use both the *saif_file_name* and *instance_name* arguments for the **-saif** option.

SEE ALSO

estimate_power (2).

PWR-270 (Error) You must use either the -saif or -activity_file option.

DESCRIPTION

You receive this message if you issue the **estimate_power** command without either the **-saif** and **-activity_file** options. You must use one of these options, and you cannot use both.

WHAT NEXT

Reissue the **estimate_power** command with either the **-saif** or **-activity_file** option, but not both.

SEE ALSO

estimate_power (2).

PWR-271 (Error) Invalid argument for the -transform option. Currently, the only allowed argument is gate_clock.

DESCRIPTION

You receive this message if you issue the **create_power_model** or **estimate_power** command with the **-transform** option, and have used an argument for **-transform** other than *gate_clock*. Currently, *gate_clock* is the only allowed argument for **-transform**.

WHAT NEXT

Reissue the command and use the *gate_clock* argument with the **-transform** option.

SEE ALSO

create_power_model (2), **estimate_power** (2).

PWR-272 (Error) synthetic_library not set or empty.

DESCRIPTION

You receive this message from **create_power_model** or **estimate_power** if the **synthetic_library** variable is not set, or if a library it points to is empty. Before executing these commands, you must set the **link_library**, **synthetic_library**, and **target_library** variables.

WHAT NEXT

Set the **synthetic_library** variable to a valid list of designs and synthetic libraries to be used during linking. Then reissue the **create_power_model** or **estimate_power** command.

SEE ALSO

create_power_model (2), **estimate_power** (2); **link_library** (3), **synthetic_library** (3), **target_library** (3).

PWR-273 (information) Fixing SDPD switching activity annotation.

DESCRIPTION

This message is issued when user-annotated state-dependent and/or path-dependent (SDPD) switching activity is being modified by the SDPD fixing step. The SDPD fixing step is enabled by the **power_fix_sdpd_annotation** variable; please check the man page of **power_fix_sdpd_annotation** for more information on this step.

WHAT NEXT

This is an information message; no user action is required.

SEE ALSO

power_fix_sdpd_annotation (3), **power_fix_sdpd_annotation_verbose** (3), **power_sdpd_message_tolerance** (3).

PWR-274 (warning) Negative annotated static probability on state '%s' of cell '%s' is set to 0.

DESCRIPTION

Negative state-dependent static probability values have been annotated on the specified cell. Such static probability annotations are invalid and are being removed before the swicthing activity can be used.

WHAT NEXT

Power Compiler will not use the negative static probability values; the script used to annotate the static probability values should be modified to avoid annotating negative static probabilities.

PWR-275 (information) Unannotated static probability for false

state '%s' of cell '%s' is automatically set to 0.

DESCRIPTION

The specified cell is partially annotated with state-dependent static probability values. Power Compiler is setting the static probability value of unannotated false states to 0.0. False states are states that always evaluate to 0 and include the default state in cells where the other states cover all possible states of the cell.

This message is issued by the SDPD fixing step which can be controlled by the variables **power_fix_sdpd_annotation**, **power_fix_sdpd_annotation_verbose** and **power_sdpd_message_tolerance**.

WHAT NEXT

This is an information message; no user action is required.

SEE ALSO

power_fix_sdpd_annotation (3), **power_fix_sdpd_annotation_verbose** (3), **power_sdpd_message_tolerance** (3).

PWR-276 (information) Non-zero static probability annotation for false state '%s' of cell '%s' is automatically set to 0.

DESCRIPTION

The specified cell has false states annotated with a non-zero state-dependent static probability values. Power Compiler is setting the static probability of false states to 0.0. False states are states that always evaluate to 0 and include the default state in cells where the other states cover all possible states of the cell.

This message is issued by the SDPD fixing step which can be controlled by the variables **power_fix_sdpd_annotation**, **power_fix_sdpd_annotation_verbose** and **power_sdpd_message_tolerance**.

WHAT NEXT

This is an information message; no user action is required.

SEE ALSO

power_fix_sdpd_annotation (3), **power_fix_sdpd_annotation_verbose** (3), **power_sdpd_message_tolerance** (3).

PWR-277 (information) The user annotated state dependent static probabilities on cell '%s' are being scaled so they add up to 1.

DESCRIPTION

The user annotated state-dependent static probability values on the specified cell do not add to 1.0. Power Compiler is scaling the static probability values so that they add up to 1.0.

This message is issued by the SDPD fixing step which can be controlled by the variables **power_fix_sdpd_annotation**, **power_fix_sdpd_annotation_verbose** and **power_sdpd_message_tolerance**.

WHAT NEXT

This is an information message; no user action is required.

SEE ALSO

power_fix_sdpd_annotation (3), **power_fix_sdpd_annotation_verbose** (3), **power_sdpd_message_tolerance** (3).

PWR-278 (information) The annotated state dependent static probabilities on cell '%s' add up to more than 1.0; Annotated static probabilities are being scaled down and the unannotated states are automatically annotated with 0.

DESCRIPTION

The specified cell is partially annotated with state-dependent static probability values. The sum of the annotated state-dependent static probabilities adds up to 1.0 or more. The annotated static probability values are being scaled down so that they add up to 1.0. The unannotated states are automatocally annotated with a static probability value of 0.0.

This message is issued by the SDPD fixing step which can be controlled by the variables **power_fix_sdpd_annotation**, **power_fix_sdpd_annotation_verbose** and **power_sdpd_message_tolerance**.

WHAT NEXT

This is an information message; no user action is required.

SEE ALSO

power_fix_sdpd_annotation (3), **power_fix_sdpd_annotation_verbose** (3), **power_sdpd_message_tolerance** (3).

PWR-279 (warning) Negative annotated %s toggle rate on the %s of pin '%s' is set to 0.

DESCRIPTION

Negative state-dependent and/or path-dependent toggle rate values have been annotated on the specified pin. Such toggle rate annotations are invalid and are being removed before the swicthing activity can be used.

WHAT NEXT

Power Compiler will not use the negative toggle rate values; the script used to annotate the switching activiy should be modified to avoid annotating negative toggle rates.

PWR-280 (warning) %s is not a buffer cell and will be ignored.

DESCRIPTION

The specified cell is not a buffer cell and for the purpose of clock tree power estimation it will be ignored.

WHAT NEXT

This is a warning; the command will resume normally with the default behaviour of finding an appropriate buffer in the link library.

PWR-281 (warning) %s buffer cell does not exist.

DESCRIPTION

The specified cell name has not been found in any link library and it will be ignored.

WHAT NEXT

This is a warning; the command will resume normally with the default behaviour of finding an appropriate buffer in the link library.

PWR-282 (warning) The link library does not contain a buffer.

DESCRIPTION

There is no buffer in the link library and clock tree power estimation will be aborted.

WHAT NEXT

Provide a link library in the link path with a buffer in it.

PWR-283 (warning) The specified clock-tree buffer fanout (%d) is invalid.

DESCRIPTION

You receive this warning because, during execution of the **report_power** command, Power Compiler found that the clock-tree buffer fanout you specified in the environment variable **clocktree_buffer_fanout** is invalid. Power Compiler will ignore the clock-tree buffer and will use the default value instead.

WHAT NEXT

If you do not want the compiler to select a fanout value (the selection is buffer-dependent), assign to the variable **clocktree_buffer_fanout** a value that is 2 or more. Then rerun the **report_power** command.

SEE ALSO

report_power (2); **clocktree_buffer_fanout** (3).

PWR-290 (error) Object '%s' is not an operator.

DESCRIPTION

You receive this message if you issue the **set_operand_isolation_cell** command and

specify as part of the *object_list* an object that is not an operator. You can specify only operator cells for this command. This error could possibly be caused by a spelling error or typo.

WHAT NEXT

Check the items in the *object_list* and verify that all are operator cells and that the spelling is correct. Then reissue the **set_operand_isolation_cell** command with the correct *object_list*.

SEE ALSO

set_operand_isolation_cell (2).

PWR-291 (warning) Invalid isolation style specified. Using the default AND-based isolation style.

DESCRIPTION

You receive this message if you issue the **set_operand_isolation_style** command with an invalid value for the **-logic** *logic_style* option. Allowed values are *AND* (the default) and *OR*. This message informs you that the default (*AND*) is being used.

WHAT NEXT

If it is acceptable to you that the *logic_style* of *AND* is used, no action is required on your part. Otherwise, reissue the **set_operand_isolation_style** command with the option **-logic_style OR**.

SEE ALSO

set_operand_isolation_style (2).

PWR-292 (warning) Removing isolation logic for operator %s.

DESCRIPTION

You receive this message if, after delay optimization, PowerCompiler finds that the isolation logic for the specified operator causes a timing violation that exceeds the current timing threshold value. In that case, PowerCompiler removes the isolation logic from the operator, as stated in the message.

The default timing threshold value is 0; you use the **set_operand_isolation_slack** command to set a different timing threshold that overrides the default. If the delay

optimization takes place after initial mapping, you can also adjust the **-weight** option to relax the slack constraint for removal of isolation logic.

WHAT NEXT

This is an informational message only; no action is required on your part.

If you did not want this isolation logic to be removed, you can go back to the version of the design before the first compile, reset the timing threshold to a much higher value, and recompile.

SEE ALSO

compile (2), **set_operand_isolation_slack** (2).

PWR-301 (Warning) The isolation cells required for operand isolation are not available in the target library; no operand isolation can be performed.

DESCRIPTION

This warning is issued when the target library does no contain the required cells to perform operand isolation. Depending on the isolation style, a two-input AND or OR gate must be available. When the isolation style is set to adaptive (the default), both a two-input AND and a two-input OR gate must be available.

WHAT NEXT

Check that the target library contains the required combinational cells. Make sure the usage of the cell was not disable with the **set_dont_use** command. If no two-input AND and/or OR gates are available, operand isolation cannot be applied.

SEE ALSO

set_dont_use (2), **set_operand_isolation_style** (2), **do_operand_isolation** (3).

PWR-302 (error) At least one, and only one, of the options -all, -min_bitwidth, -gated_registers or -gating_cells must be used

with the remove_clock_gating command.

DESCRIPTION

The **remove_clock_gating** command requires that you use one (but only one) of the four options **-all**, **-min_bitwidth**, **-gated_registers**, or **-gating_cells**.

WHAT NEXT

To remove all the clock-gating cells in the current level of hierarchy, use the **-all option**. To remove only register that belong to banks smaller than a certain minimum size, use the **-min_bitwidth** option. Along with the **-all** and **-min_bitwidth** options, you can also use the **-no_hier** option to limit removal of clock-gating cells to the current level. To remove selected individual clock gating cells or registers in lower levels of the design hierarchy, give their complete path names from the current level of hierarchy as arguments to the **-gated_registers** option or the **-gating_cells** option of the **remove_clock_gating** command.

SEE ALSO

remove_clock_gating (2).

PWR-303 (error) Clock-gating cannot be removed from cell %s because the cell has the size_only attribute assigned to it.

DESCRIPTION

You receive this error message because the **remove_clock_gating** command is trying to mark for ungating a register that has the **size_only** attribute assigned to it. Removal of clock-gating requires remapping of the register, and the **size_only** attribute cannot be honored. Hence, this cell is not being marked for removal of clock-gating.

WHAT NEXT

If you want to remove clock-gating from the cell, use the **reset_attribute** command to remove the **size_only** attribute. Then reissue the **remove_clock_gating** command. This ensures that **compile -incremental** (and **physopt** and **physopt -incremental**) will remove clock-gating from this cell.

SEE ALSO

remove_clock_gating (2), **reset_attribute** (2).

PWR-304 (error) Clock-gating cannot be removed from cell %s because the dont_touch attribute is assigned to the cell.

DESCRIPTION

You receive this error message because the **remove_clock_gating** command is trying to mark for ungating a register that has the **dont_touch** attribute assigned to it. Removal of clock-gating requires remapping of the register, and the **dont_touch** attribute cannot be honored. Hence, this cell is not being marked for removal of clock-gating.

WHAT NEXT

If you want to remove clock-gating from the cell, use the **remove_attribute** command to remove the **dont_touch** attribute. Then reissue the **remove_clock_gating** command. This ensures that **compile -incremental** (and **physopt** and **physopt -incremental**) will remove clock-gating from this cell.

SEE ALSO

remove_clock_gating (2), **remove_attribute** (2).

PWR-305 (warning) Cell %s has a timing exception that might be lost.

DESCRIPTION

You receive this warning to inform you that the **remove_clock_gating** command provides a directive to **compile -incremental** (and **physopt** and **physopt -incremental**) to remove clock-gating from a cell that has a timing exception. One of these commands set the exception: **set_max_delay**, **set_min_delay**, **set_multicycle_path** or **set_false_path**. This exception might be lost during the remapping of the cell during **compile -incremental**.

WHAT NEXT

After the **compile -incremental** command removes clock-gating from the cell, run the **report_timing** command to verify that the exception is being honored. If the exception is lost, reapply the timing exception by reissuing **set_max_delay**, **set_min_delay**, **set_multicycle_path**, or **set_false_path**. Reissue **compile -incremental** to ensure that the exception the command specifies is being honored.

SEE ALSO

remove_clock_gating (2), **report_timing** (2), **set_false_path** (2), **set_max_delay** (2),

set_min_delay (2), **set_multicycle_path** (2).

PWR-306 (error) Cell %s has a timing exception and cannot be ungated.

DESCRIPTION

You receive this error message to inform you that the **remove_clock_gating** command does not provide a directive to **compile -incremental** (and **physopt** and **physopt -incremental**) to remove clock-gating from a cell that has a timing exception. One of the following commands set the exception: **set_max_delay**, **set_min_delay**, **set_multicycle_path**, or **set_false_path**.

WHAT NEXT

To remove clock-gating from the cell, use the **reset_path** command to remove the timing exception.

SEE ALSO

remove_clock_gating (2), **report_timing** (2), **reset_path** (2), **set_false_path** (2), **set_max_delay** (2), **set_min_delay** (2), **set_multicycle_path** (2).

PWR-307 (warning) The current design is a hierarchical design; consider using the -hier option.

DESCRIPTION

You see this warning because you issued the **remove_clock_gating** command with the **-all** option on a hierarchical design but did not use the **-heir** option. The **-all** option did not find clock-gating logic at the current level of hierarchy and will not mark any clock-gating logic for removal. If you intended to invoke both the **-all** and the **-hier** options, specify the **-hier** option at this time, in addition to the specifying the **-all** option.

WHAT NEXT

To remove clock-gating logic from all the hierarchies in the design, use the **remove_clock_gating** command with both the **-hier** option and the **-all** option.

SEE ALSO

remove_clock_gating (2), **report_clock_gating** (2).

PWR-308 (Information) No clock-gating cell found; no clock-gating logic will be removed.

DESCRIPTION

You receive this message if you issue the **remove_clock_gating** command with only the **-all** option. The result is that **remove_clock_gating** did not find clock-gating logic at the current level of hierarchy and did not mark any clock-gating logic for removal.

WHAT NEXT

To remove clock-gating logic from all the hierarchies in the design, use the **remove_clock_gating** command with both the **-hier** option and the **-all** option.

SEE ALSO

remove_clock_gating (2), **report_clock_gating** (2).

PWR-309 (error) Clock Gating cell %s will be removed and cannot be used for rewiring.

DESCRIPTION

You receive this message because you used an invalid cell as an argument to the **-gating_cell** option of the **rewire_clock_gating** command. The cell is invalid because it is already marked for removal by the **remove_clock_gating** command. A cell that is marked for removal cannot be used to rewire other gated registers.

WHAT NEXT

If you do not want **compile -incremental** (or **physopt** and **physopt -incremental**) to remove the cell, use the **-undo** option with the **remove_clock_gating** command.

SEE ALSO

compile (2), **remove_clock_gating** (2), **rewire_clock_gating** (2).

PWR-310 (error) Clock-gated cell %s will be ungated and cannot

be rewired.

DESCRIPTION

You receive this message because you used an invalid cell as the value of the **-gating_cell** option of the **rewire_clock_gating** command. The cell is invalid because it is already marked for ungating by the **remove_clock_gating** command. A gated cell that is marked for removal of clock-gating cannot be rewired.

WHAT NEXT

If you do not want **compile -incremental** (or **physopt** and **physopt -incremental**) to remove clock-gating from the gated cell, use the **-undo** option with the **remove_clock_gating** command. Then reissue the **rewire_clock_gating** command.

SEE ALSO

compile (2), **physopt** (2), **remove_clock_gating** (2), **rewire_clock_gating** (2).

PWR-311 (error) Clock-gated cell %s is not gated by a gating cell that is logically equivalent to %s.

DESCRIPTION

You receive this error message because you specified a clock-gating cell to gate the named cell (which could be a register, clock gating cell or module) that is not logically equivalent to the current clock-gating cell gating the cell.

WHAT NEXT

Find a clock-gating cell that is logically equivalent to the one currently gating the cell, and use it as an argument to the **-gating_cell** option of the **rewire_clock_gating** command. To find logically equivalent cells, use the **report_clock_gating** command with the **-verbose** option. To create more than one logically equivalent clock-gating cell during **insert_clock_gating** use the **-max_fanout** option of the **set_clock_gating_style** command.

SEE ALSO

insert_clock_gating (2), **report_clock_gating** (2), **rewire_clock_gating** (2), **set_clock_gating_style** (2).

PWR-312 (error) Clock-gating cell %s does not have clock-

gating information and cannot be used for rewiring.

DESCRIPTION

You receive this message because you specified an invalid clock-gating cell to gate the named register, clock gate or module. The cell is invalid because it does not have enough information.

WHAT NEXT

Power Compiler saves information related to clock-gating in the Synopsys database (.db) format file created for the design. If this information is lost, Power Compiler is unable to recognize the clock-gating cell. Ensure that the design remains in the .db format throughout your design flow.

SEE ALSO

elaborate (2), **report_clock_gating** (2), **rewire_clock_gating** (2), **set_clock_gating_style** (2).

PWR-313 (warning) Cell %s is already gated by clock-gating cell %s.

DESCRIPTION

You see this warning to let you know that the option arguments of the **rewire_clock_gating** command specified for this cell are partially incorrect. For instance, the clock-gating cell you specified already gates the named cell (register, clock-gate or module). Other correct arguments to the **rewire_clock_gating** command might be honored anyway. But if not, the **rewire_clock_gating** command will not save any directive for **compile -incremental** to change the structure of the design. If the **-gated_registers** option of the **remove_clock_gating** command has more than one argument, one of the arguments might trigger the warning although the other arguments are valid.

WHAT NEXT

Use a different logically equivalent clock-gating cell to rewire the clock-gating cell. To find other logically equivalent clock-gating cells, use the **report_clock_gating** command with the **-verbose** option. To ensure that **insert_clock_gating** limits the fanout of a single clock-gating cell and creates more than one logically equivalent clock-gating cell, use the **-max_fanout** option of the **set_clock_gating_style** command.

SEE ALSO

elaborate (2), **report_clock_gating** (2), **rewire_clock_gating** (2), **set_clock_gating_style** (2).

PWR-314 (warning) Clock-gating cannot be removed from design %s because it has a dont_touch attribute.

DESCRIPTION

You see this warning message because the design from which you are trying to remove clock-gating with the **remove_clock_gating command** is marked with the **dont_touch** attribute.

WHAT NEXT

To remove clock-gating from the design, remove the **dont_touch** attribute using the **reset_attribute** command. Then reissue the **remove_clock_gating** command. This ensures that **compile -incremental** (or **physopt** and **physopt -incremental**) will remove clock-gating from this cell.

SEE ALSO

remove_clock_gating (2), **reset_attribute** (2).

PWR-315 (error) The cell %s is not a hierarchical clock-gating cell and cannot be removed.

DESCRIPTION

You receive this error message because you specified a nonhierarchical clock-gating cell as an argument of the **-gating_cell** option of the **remove_clock_gating** command. Nonhierarchical cells cannot be removed.

WHAT NEXT

Make sure the specified cell is a hierarchical clock-gating cell. To find clock-gating cells in the design, use the **report_clock_gating** command. Do not ungroup the hierarchical clock-gating cells during the compile flow.

SEE ALSO

remove_clock_gating (2), **report_clock_gating** (2), **ungroup** (2).

PWR-316 (warning) The library cell %s is not up-to-date and, hence, the register cannot be ungated.

DESCRIPTION

You see this warning message because the cell in your library that corresponds to the specified clock-gated register is not up-to-date, and the register mapped to this library cell cannot be ungated.

The library vendor might be using an older version of Library Compiler to read the library. The library may also be using the obsolete state group instead of the ff group or latch group to describe the sequential functionality of the cell.

WHAT NEXT

If you have the .lib source file for your technology library, check to make sure that the sequential cells are using the ff group or latch group and not the obsolete state group.

If you do not have access to the .lib source file, contact the library vendor to verify that the vendor is using the latest version of Library Compiler to read the .lib file and that the .lib file uses the ff group or latch group (and not the obsolete state group) to describe the sequential functionality of the cell.

For more information about Library Compiler and the ff group and latch group, see the Library Compiler documentation suite.

SEE ALSO

read_lib (2), **write_lib** (2).

PWR-317 (warning) Clock-gated cell %s does not have a rewiring directive to undo.

DESCRIPTION

You see this warning message because you gave an invalid cell as the **-undo** option of the **rewire_clock_gating** command. The cell you specified does not have a rewiring directive on it.

WHAT NEXT

Check to make sure you are using the name of the correct cell in this instance. To check on information and names of cells related to clock-gating in your design, use the **report_clock_gating** command.

SEE ALSO

report_clock_gating (2), **rewire_clock_gating** (2).

PWR-318 (error) At least one cell or pin must be in the -gated_objects list.

DESCRIPTION

You see this error message because the list you specified as the **-gated_objects** option of the **rewire_clock_gating** command did not include a clock-gated cell (register, clock-gate or module). The **rewire_clock_gating** command requires that you specify at least one clock-gated cell or pin in the list you use as the argument to the **-gated_objects** option.

WHAT NEXT

Check to make sure you are using the name of the correct cell or pin in this instance. To check on information and names of cells related to clock-gating in your design, use the **report_clock_gating** command.

SEE ALSO

report_clock_gating (2), **rewire_clock_gating** (2).

PWR-319 (error) Only one of the options -gating_cell or -undo can be used.

DESCRIPTION

You receive this error message because you have specified a cell as an argument to the **rewire_clock_gating** command that has more than one of the allowed options defined. The **rewire_clock_gating** command requires that you define only one option, either **-gating_cell** or **-undo**.

WHAT NEXT

Check to make sure you are using the name of the correct cell in this instance. To check information and names of the cells related to clock-gating in your design, use the **report_clock_gating** command. To undo the effect of an earlier **rewire_clock_gating** command, use the **-undo** option. To rewire clock-gated registers in your design, use the **-gating_cell** option.

SEE ALSO

report_clock_gating (2), **rewire_clock_gating** (2).

PWR-320 (error) Only one clock-gating cell can be specified for the -gating_cell option

DESCRIPTION

You receive this error message because you have specified more than one cell as the argument of the **-gating_cell** option of the **rewire_clock_gating** command. The **-gating_cell** option takes only one cell as its value.

WHAT NEXT

Check to make sure you are using the name of the correct cell in this instance. To check information and names of cells related to clock-gating in your design, use the **report_clock_gating** command. Then make sure to use only one clock-gating cell as an argument of the **-gating_cell** option.

SEE ALSO

report_clock_gating (2), **rewire_clock_gating** (2).

PWR-321 (warning) The rewire_clock_gating cell command did not find a valid clock-gated cell to rewire.

DESCRIPTION

You see this warning message because the **rewire_clock_gating** command did not find any cell to rewire. This might be because the clock-gating cell you specified in the **-gating_cell** option already gates all the cells or pins you named in the **-gated_objects** option.

WHAT NEXT

Check to make sure you are using the name of the correct cell in this instance. To check information and names of cells related to clock-gating in your design, use the **report_clock_gating** command.

SEE ALSO

report_clock_gating (2), **rewire_clock_gating** (2).

PWR-322 (error) Clock-gating cell %s is a target cell for the rewire_clock_gating command.

DESCRIPTION

The named cell is not a valid option of the **remove_clock_gating** command because it is a target clock-gating cell for the **rewire_clock_gating** command.

WHAT NEXT

If a cell is a target clock-gating cell for the **rewire_clock_gating** command, it cannot be marked for removal. If you want to use the **compile** command with the **-incremental** option (or **physopt** and **physopt -incremental**) to remove the cell, use the **-undo** option of the **rewire_clock_gating** command with the **-gated_registers** option. Include as the argument to the **-gated_objects** option all the cells and pins that are marked to be moved to the new clock-gating cell. Then reissue the **remove_clock_gating** command.

SEE ALSO

compile (2), **remove_clock_gating** (2), **rewire_clock_gating** (2).

PWR-323 (error) The cell %s is marked for rewiring and cannot be ungated.

DESCRIPTION

You receive this error message because you specified as an option to the **remove_clock_gating** command a cell that is marked for rewiring by the **rewire_clock_gating** command.

WHAT NEXT

A cell that is marked for rewiring cannot be marked for removal. If you want to use the **compile** command with the **-incremental** option (or **physopt** and **physopt -incremental**) to remove the cell, use the **-undo** option of the **rewire_clock_gating** command. Use the cells and pins you specified as an argument for the **-gated_objects** option. Then reissue the **remove_clock_gating** command.

SEE ALSO

compile (2), **remove_clock_gating** (2), **rewire_clock_gating** (2).

PWR-324 (error) The cell %s is not a clock-gated flip-flop.

DESCRIPTION

You receive this message because you issued the **remove_clock_gating** command, but specified a non-clock-gated register as an argument. The **remove_clock_gating** command will not mark a non-clock-gated register for removal. Nor can you undo the effect of a previous **remove_clock_gating** command if you used the **-undo option.**

WHAT NEXT

Reissue the **remove_clock_gating** command with the appropriate arguments. If you want to remove a clock-gating cell, use the **-gating_cells** option. Check that the cells you specify are hierarchical clock-gating cells. If you want to remove clock-gating on specific registers, use the **-gated_registers** option of the **remove_clock_gating** command. Check that the cells you specify are clock-gated registers and have not been ungated already. Use the **report_clock_gating** command to get information about the clock-gated logic in the design. If you want to undo the effect of a previous **remove_clock_gating** command, use the **-undo** option.

SEE ALSO

remove_clock_gating (2), **report_clock_gating** (2).

PWR-325 (error) Clock-gating cell %s cannot be removed because it has a dont_touch attribute.

DESCRIPTION

You receive this error message because you specified for removal by the **remove_clock_gating** command a cell that has the **dont_touch** attribute defined on it. This cell is not being marked for removal of clock-gating.

WHAT NEXT

To remove clock-gating from the cell, remove the **dont_touch** attribute from the cell using the **reset_attribute** command. Then reissue the **remove_clock_gating** command. This ensures that **compile -incremental** (and **physopt** and **physopt -incremental**) will remove the clock-gating cell.

SEE ALSO

remove_clock_gating (2), **reset_attribute** (2).

PWR-326 (warning) Pin %s has a timing exception that might be lost.

DESCRIPTION

The **remove_clock_gating** command provides a directive to **compile -incremental** (and **physopt** and **physopt -incremental**) to remove clock-gating from a cell whose pin has a timing exception. One of the following commands set this timing exception: **set_max_delay**, **set_min_delay**, **set_multicycle_path**, or **set_false_path**. This exception might be lost during the remapping of the cell during **compile -incremental**.

WHAT NEXT

After **compile -incremental** removes clock-gating from the cell, run the **report_timing** command to check that the original timing exception is being honored. If the constraint is lost, reapply the timing exception by reissuing **set_max_delay**, **set_min_delay**, **set_multicycle_path**, or **set_false_path**. To ensure that the constraint specified by the command is being honored, reissue **compile -incremental**

SEE ALSO

remove_clock_gating (2), **report_timing** (2), **set_false_path** (2), **set_max_delay** (2), **set_min_delay** (2), **set_multicycle_path** (2).

PWR-327 (error) Pin %s has a timing exception and the cell cannot be removed.

DESCRIPTION

You receive this error message because you have specified to the **remove_clock_gating** command a clock-gating cell whose pin has a timing exception on it. The **remove_clock_gating** command does not provide a directive for **compile -incremental** (and **physopt** and **physopt -incremental**) to remove such a clock-gating cell. This timing exception was set by one of the following commands: **set_max_delay**, **set_min_delay**, **set_multicycle_path**, or **set_false_path**.

WHAT NEXT

To remove clock-gating from the cell, use the **reset_path** command to remove the timing exception from the pin.

SEE ALSO

remove_clock_gating (2), **report_timing** (2), **reset_path** (2), **set_false_path** (2), **set_max_delay** (2), **set_min_delay** (2), **set_multicycle_path** (2).

PWR-328 (warning) A pin of cell %s has a timing exception that might be lost.

DESCRIPTION

The **remove_clock_gating** command provides a directive to **compile -incremental** (and **physopt** and **physopt -incremental**) to remove clock-gating from a cell whose pin has a timing exception. One of the following commands set this timing exception: **set_max_delay**, **set_min_delay**, **set_multicycle_path**, or **set_false_path**. This exception might be lost when remapping of the cell occurs during **compile -incremental**.

WHAT NEXT

After **compile -incremental** removes clock-gating from the cell, run the **report_timing** command to check that the original timing exception is being honored. If the constraint is lost, reapply the timing exception by reissuing **set_max_delay**, **set_min_delay**, **set_multicycle_path**, or **set_false_path**. Then reissue **compile -incremental** to ensure that the constraint specified by the command is being honored.

SEE ALSO

remove_clock_gating (2), **report_timing** (2), **set_false_path** (2), **set_max_delay** (2), **set_min_delay** (2), **set_multicycle_path** (2).

PWR-329 (error) A pin of cell %s has a timing exception and the cell cannot be removed.

DESCRIPTION

You receive this error message because you have specified to the **remove_clock_gating** command a clock-gating cell whose pin has a timing exception on it. The **remove_clock_gating** command does not provide a directive for **compile -incremental** (and **physopt** and **physopt -incremental**) to remove such a clock-gating cell. This timing exception was set by one of the following commands: **set_max_delay**, **set_min_delay**, **set_multicycle_path**, or **set_false_path**.

WHAT NEXT

To remove clock-gating from the cell, use the **reset_path** command to remove the timing exception from the pin. Then reissue **compile -incremental**.

SEE ALSO

remove_clock_gating (2), **report_timing** (2), **reset_path** (2), **set_false_path** (2), **set_max_delay** (2), **set_min_delay** (2), **set_multicycle_path** (2).

PWR-330 (error) Clock-gated cell %s does not have clock-gating information and cannot be used for rewiring.

DESCRIPTION

You receive this error message because you specified a clock-gating cell to gate the named cell (which could be a register, clock-gate or module) and the cell does not have enough information.

WHAT NEXT

Power Compiler saves information related to clock-gating in the Synopsys database format (.db) file created for the design. If this information is lost, Power Compiler is unable to recognize the clock-gating cell. Ensure that the design remains in the .db format throughout your design flow.

SEE ALSO

elaborate (2), **report_clock_gating** (2), **rewire_clock_gating** (2), **set_clock_gating_style** (2).

PWR-331 (error) You must use the -control_point option with the -control_signal option.

DESCRIPTION

You receive this error message because you have used the **set_clock_gating_style** command with incomplete specification for the test control circuitry. If you specify the **-control_signal** option to the **set_clock_gating_style** command, you must also use the **-control_point** option to specify where in the circuitry to insert the control point. If you use the default value **none**, no test control logic is inserted.

WHAT NEXT

Use the **-control_point** option of the **set_clock_gating_style** command if the **-control_signal** option is specified. Use the **before_latch** or **after_latch** argument of the **-control_point** option if you want to insert a test control point.

SEE ALSO

set_clock_gating_style (2).

PWR-332 (Warning) Unable to rewire cell %s; clock-gating cells might not be equivalent.

DESCRIPTION

The **rewire_clock_gating** command could not be honored during **compile** because the target clock-gating cell is not equivalent to the original clock-gating cell.

WHAT NEXT

Verify that the target clock-gating cell is logically equivalent to the original clock-gating cell. Make sure that you have have not changed the name of the clock-gating cells or ungrouped the design after using the **rewire_clock_gating** command. To find logically equivalent cells, use the **report_clock_gating** command.

SEE ALSO

report_clock_gating (2), **rewire_clock_gating** (2).

PWR-333 (warning) Unable to find target clock-gating cell for rewiring cell %s.

DESCRIPTION

You receive this warning to let you know that the **rewire_clock_gating** command could not be honored during **compile** because Power Compiler could not find the target clock-gating cell.

WHAT NEXT

Make sure you have not changed the name of the clock-gating cells or ungrouped the design after using the **rewire_clock_gating** command. To find logically equivalent cells, use the **report_clock_gating** command.

SEE ALSO

report_clock_gating (2), **rewire_clock_gating** (2).

PWR-334 (error) Use at least one of the options, -include_instances, -exclude_instances, or -undo with the set_clock_gating_registers command.

DESCRIPTION

You receive this error message because the **set_clock_gating_registers** did not mark the registers to be included or excluded from clock-gating. Use at least one of these three options: **-include_instances**, **-exclude_instances**, or **-undo**. The arguments to the options should be registers in the current design.

WHAT NEXT

Use the appropriate set of options for the command. Make sure you are using the correct name of the registers you want to include or exclude for clock-gating. To find cells in the design, use the **find** command.

SEE ALSO

find (2), **insert_clock_gating** (2), **set_clock_gating_registers** (2).

PWR-335 (error) The cell %s is used in more than one of these options: -include_instances, -exclude_instances, or -undo.

DESCRIPTION

You receive this error message because you used the same cell as an argument to more than one option of the **set_clock_gating_registers** or **set_replace_clock_gates** command. Each option must have a different cell as its argument. The command therefore did not mark the signals that are to be included or excluded from clock-gating.

WHAT NEXT

Use an individual cell as an argument to only one of these options: **-include_instance**, **-exclude_instances**, or **-undo**.

SEE ALSO

report_clock_gating (2), **set_clock_gating_registers** (2). **set_replace_clock_gates** (2).

PWR-336 (error) An argument, %s, to the %s command is not a register that can be clock-gated by the insert_clock_gating command.

DESCRIPTION

You receive this error message to let you know that the **set_clock_gating_registers** command did not mark the registers that need to be included or excluded from clock-gating. One of the arguments was not a SEQGEN object that can be clock-gated.

WHAT NEXT

Make sure you are using the correct name for the registers you want to include or exclude for clock-gating. Use the **find** command to find cells in the design. Use the **report_cell** command to find information about individual cells.

SEE ALSO

set_clock_gating_style (2), **insert_clock_gating** (2), **report_cell(2), find** (2).

PWR-337 (error) Cannot use -undo option on register %s because the register's clock-gating cell is marked for removal.

DESCRIPTION

You receive this message if you issue the **remove_clock_gating** command with the **-undo** option for a register whose clock-gating cell is already marked for removal. An earlier invocation of the **remove_clock_gating** command, with either the **-gating_cell** option or the **-all** option, marked the cell for removal.

WHAT NEXT

Reissue the **remove_clock_gating** command with the appropriate arguments. If you do not want **compile -incremental** to remove clock-gating from the register, make sure that the clock-gating cell gating the register is not marked for removal. Use the **-undo** option of the **remove_clock_gating** command on the clock-gating.

If you want to selectively ungate a few registers, first unmark the clock-gating cell using the **remove_clock_gating** command with the **-undo** option. Then use the **remove_clock_gating** command with the **-gated_registers option to mark the registers you want ungated.**

SEE ALSO

remove_clock_gating (2), **report_clock_gating** (2).

PWR-338 (warning) Skipping cell %s because its clock-gating cell will be removed.

DESCRIPTION

You receive this message if you issue the **remove_clock_gating** command, with the **-gated_registers** option, but the cell's clock-gating cell is already marked for removal. The **compile** command with the **-incremental** option will remove the clock-gating on this cell because the gating cell itself is being removed.

WHAT NEXT

Check the spelling and confirm that you specified the correct cell. If you want to remove a clock-gating cell, use the **remove_clock_gating** command with the **-gating_cells** option. Verify that the cells you specify are hierarchical clock-gating cells.

If you want to remove clock-gating on a specific register, use the **-gated_registers** option. Verify that the cell you specify is a clock-gated register and has not been ungated already.

Use the **report_clock_gating** command to get information about the clock-gated logic in the design. To undo the effect of a previous **remove_clock_gating** command, use **remove_clock_gating -undo**.

SEE ALSO

compile (2), **remove_clock_gating** (2), **report_clock_gating** (2).

PWR-339 (error) Cell %s is causing a split in the clock-gating circuitry; group not possible.

DESCRIPTION

You receive this message if you issue the **group** command, and the selected cells to be grouped leads to the partition of clock-gating circuitry and the gated registers. All clock-gated registers being gated by a particular clock-gating cell should remain in the same or lower levels of hierarchy as the gating cell. This means that it is allowed to group clock-gated registers without its clock-gating cell, but it is not allowed to group the clock-gating cell without its gated objects (registers, modules and clock-gating cells).

WHAT NEXT

Check the spelling and confirm that you specified the correct cell. To find the cells that are gated by a particular gating cell, use the **report_clock_gating** command. Do not supply options that lead to a partition of clock-gating cells and the gated register. To explicitly exclude cells from the design being created, use the **-except** option of the **group** command

SEE ALSO

group (2), **report_clock_gating** (2).

PWR-340 (warning) Cell %s will not be rewired.

DESCRIPTION

You receive this message if you issue the **group** command, and the selected cells contain a clock-gated cell (a register or clock-gating cell) marked for rewiring. The rewiring directive is lost if you use the **group** command on the design.

WHAT NEXT

Check the spelling and confirm that you specified the correct cell. To find the cells that are gated by a particular gating cell, use the **report_clock_gating** command. Then use the **rewire_clock_gating** command again to mark cells for rewiring. Make sure that the target clock-gating cell and the gated cell are in the same design.

SEE ALSO

group (2), **report_clock_gating** (2), **rewire_clock_gating** (2).

PWR-341 (warning) The cell %s is an ungated flip-flop.

DESCRIPTION

You receive this message if you issue the **remove_clock_gating** command, and one of the flip-flops to be ungated is already not gated.

WHAT NEXT

Reissue the **remove_clock_gating** command with the appropriate arguments. To remove a clock-gating cell, use the **-gating_cells** option of the **remove_clock_gating** command. Check that the cells you specify are hierarchical clock-gating cells.

To remove clock-gating on a specific register, use the **-gated_registers** option of the **remove_clock_gating** command. Check that the cell you specify is a clock-gated register and has not been ungated already.

To get information about the clock-gated logic in the design, use the **report_clock_gating** command.

To undo the effect of a previous **remove_clock_gating** command, use the **-undo** option.

SEE ALSO

remove_clock_gating (2), **report_clock_gating** (2).

PWR-350 (error) Power Optimization license needed by command %s is not available.

DESCRIPTION

This error message occurs when the specified command requires the Power Optimization license. Either your site does not have the license or all of the available licenses are in use.

WHAT NEXT

You can use the **power_keep_license_after_power_commands** environment variable to keep holding the Power Optimization license after using a Power Compiler command. This ensures that other users do not take the license from your session. Contact your Synopsys representative to obtain more licenses if your site does not have enough.

SEE ALSO

dc_shell(1)
dp_shell(1)
synopsys_users(1)
get_license(2)
license_users(2)
power_keep_license_after_power_commands(3)

PWR-351 (warning) Clock-gating related optimizations require the Power Optimization license, which is not available.

Optimizations related to clock gating will be skipped.

DESCRIPTION

This warning message occurs when you use a command that requires a Power Optimization license. The **compile** command and related optimization commands require the Power Optimization license to perform clock-gating related optimizations. Either your site does not have the license or all of the available licenses are in use.

WHAT NEXT

You can use the **power_keep_license_after_power_commands** environment variable to keep holding the Power Optimization license after using a Power Compiler command. This ensures that other users do not take the license from your session. Contact your Synopsys representative to obtain more licenses if your site does not have enough.

SEE ALSO

dc_shell(1)
dp_shell(1)
synopsys_users(1)
get_license(2)
license_users(2)
power_keep_license_after_power_commands(3)

PWR-352 (error) Module Compiler license is not available; insert_clock_gating not possible.

DESCRIPTION

You receive this error message because your site is not licensed for Module Compiler or all the licenses are in use. The **insert_clock_gating** command requires the Module Compiler license if you are inserting clock-gating in a Module Compiler generated netlist with the **-mc** option.

WHAT NEXT

To ensure that other users do not snatch the license from your session, use the **get_license** command to check out the Module Compiler license. If your site does not have enough licenses, contact your Synopsys representative to obtain more.

SEE ALSO

dc_shell (1), **synopsys_users** (1). **get_license** (2), **license_users** (2).

PWR-353 (error) Cannot continue because the Power Compiler license is not available and the design has clock gating.

DESCRIPTION

This error message occurs when you use a command that requires a Power Compiler license. The **compile** command and related optimization commands require the Power Optimization license to perform clock-gating related optimizations. Either your site does not have the license or all of the available licenses are in use.

WHAT NEXT

You can use the **power_keep_license_after_power_commands** environment variable to keep holding the Power Optimization license after using a Power Compiler command. This ensures that other users do not take the license from your session. Contact your Synopsys representative to obtain more licenses if your site does not have enough.

SEE ALSO

dc_shell(1)
dp_shell(1)
synopsys_users(1)
get_license(2)
license_users(2)
power_keep_license_after_power_commands(3)

PWR-354 (error) Clock-gated register %s is not linked to a technology library cell and cannot be ungated.

DESCRIPTION

remove_clock_gating will not put a directive for the compile -incremental (and the physopt and physopt -incremental) command to remove a clock-gating cell which is not linked to a technology library cell or is a generic cell.

WHAT NEXT

If you want the clock-gating to be removed from the cell, make sure that the design is linked and all cells have an associated technology library cell. Also make sure that the design is mapped to a technology. Use the report_cell command to find the details of the cell. Use the link command if the design is already mapped.

SEE ALSO

remove_clock_gating (2), **report_cell(2), link** (2).

PWR-355 (error) The clock-gating cell %s and gated object %s are not in the same level of hierarchy.

DESCRIPTION

rewire_clock_gating will not put a directive to rewire the gated cell for the compile -incremental command because the target clock-gating cell is not in the same level of hierarchy as the gated cell.

WHAT NEXT

If you want the clock-gating cell to be changed, pick a logically equivalent clock-gating cell in the same level of hierarchy as the gated cell.

SEE ALSO

rewire_clock_gating (2), **report_clock_gating(2).**

PWR-356 (warning) '-transform gate_clock' is not supported in Flexible Analysis Flow, option ignored.

DESCRIPTION

If the design is read in through 'analyze' and 'elaborate' steps or through a 'read' step, 'create_power_model' can not do clock gating.

WHAT NEXT

In Flexible Analysis flow, use 'insert_clock_gating' and then create_power_model command to create the power model incorporating clock gating. If in the interactive mode, use 'create_power_model -hdl_files <> -top_design <> -transform gate_clock' to do clock gating in the power model.

SEE ALSO

elaborate(2)

PWR-357 (error) pe_shell does not support tcl_mode

DESCRIPTION

pe_shell currently does not support tcl_mode

WHAT NEXT

Invoke pe_shell with out the -tcl_mode argument.

PWR-358 (error) Bad option combination between ‘hier_level’ and ‘this_level_only’.

DESCRIPTION

‘hier_level’ and ‘this_level_only’ are mutually exclusive options. Only one of them can be used.

WHAT NEXT

Invoke ’report_activity’ with either ’hier_level’ OR ’this_level_only’ option.

PWR-359 (error) Bad option combination between ‘all’ and ‘only’.

DESCRIPTION

‘all’ and ‘only’ are mutually exclusive options. Only one of them can be used.

WHAT NEXT

Invoke ’report_activity’ with either ’all’ OR ’only’ option.

PWR-360 (error) The number assigned to hier_level option must

be positive.

DESCRIPTION

hier_level option takes only positive integer arguments.

WHAT NEXT

Invoke 'report_activity' with '-hier_level <positive number>' option.

PWR-361 (error) Only 'ports' and 'registers' are accepted with -all option.

DESCRIPTION

'-all' options takes only a list of 'ports', 'registers' or both.

WHAT NEXT

Invoke 'report_activity' with '-all ports' OR '-all registers' OR '-all {ports registers}'.

PWR-362 (error) No switching activity has been annotated.

DESCRIPTION

The read_saif command could not annotate any switching activity. This is usually due to an invalid instance name specified with the -instance argument.

WHAT NEXT

Check that the -instance argument is valid; the instance specified by the -instance argument must be present in the backward SAIF file storing the switching activity.

PWR-363 (error) Only low or high is accepted for -effort.

DESCRIPTION

The valid choices for -effort option is either 'low' or 'high'.

WHAT NEXT

Reinvoke the command with either ’-effort low’ or ’-effort high’.

PWR-364 (error) The <em drc switch> argument of set_electromigration_drc must be either ’on’ or ’off’.

DESCRIPTION

The valid choices for the <em drc switch> argument of the set_electromigration_drc command are either ’on’ or ’off’.

WHAT NEXT

Reinvoke the command with either ’on’ or ’off’ as its <em drc switch> argument.

PWR-365 (error) The clock gating cell ’%s’ has an unknown pin.

DESCRIPTION

The clock gating cell has an unknown pin which can not be processed.

WHAT NEXT

Look for any steps which might have changed the clock gating cell since elaborate or last compile. Avoid any steps that would change the attributes or manipulate the clock gating cells and re-compile.

PWR-366 (error) Cannot specify ’-path_dep’, ’-rise_ratio’, or ’-period’ argument without ’-toggle_rate’.

DESCRIPTION

The ’-path_dep’, ’-rise_ratio’ and ’-period’ arguments require a toggle rate value given with the ’-toggle_rate’ argument.

WHAT NEXT

Reinvoke the command with a valid ’-toggle_rate’ argument.

PWR-367 (error) Cannot specify '-state_dep' without either '-toggle_rate' or '-static_probability'.

DESCRIPTION

The '-state_dep' argument requires a toggle rate value given with the '-toggle_rate' argument or a static probability value given with the '-static_probability' argument.

WHAT NEXT

Reinvoke the command with a valid '-toggle_rate' or '-static_probability' argument.

PWR-368 (error) The '-toggle_rate' argument has to be numeric.

DESCRIPTION

The argument specified with '-toggle_rate' must be a decimal number.

WHAT NEXT

Reinvoke the command with a valid numeric '-toggle_rate' argument.

PWR-369 (error) The '-period' argument has to be numeric.

DESCRIPTION

The argument specified with '-period' must be a decimal number.

WHAT NEXT

Reinvoke the command with a valid numeric '-period' argument.

PWR-370 (error) The '-rise_ratio' value must be between 0 and 1.

DESCRIPTION

The value of the rise_ratio argument represent the ratio of rise toggles with

respect to the total toggles and must be a decimal number greater or equal to 0.0 and less or equal to 1.0.

WHAT NEXT

Reinvoke the command with a value value for the '-rise_ratio' argument.

PWR-371 (error) Invalid type of switching activity for an object of type %s.

DESCRIPTION

This error occurs when the arguments of the set_switching_activity command are not applicable to the object being annotated. Examples of such invalid switching activities are: any state and path dependent switching activity on design ports and nets; path dependent toggle counts on input pins, state dependent static probability on pins, any toggle count on cells, and non-state dependent static probability on cells.

WHAT NEXT

Check the type of the switching activity given in the arguments and the type of objects being annotated, and then re-apply the set_switching_activity command.

PWR-372 (error) The -khrate value must be non-negative.

DESCRIPTION

The value of the -khrate argument represents the de-rating factor of glitches and must be a non-negative real number.

WHAT NEXT

Re-invoke the command with a non-negative value of the -khrate argument.

PWR-373 (error) Empty/bad object list.

DESCRIPTION

The command was invoked with an empty list of objects, or with objects of the wrong type.

WHAT NEXT

Check the object types that are valid for this command, and re-invoke it with a valid object list.

PWR-374 (error) The %s argument cannot be used with %s.

DESCRIPTION

The command was invoked with a number of arguments that are mutually exclusive.

WHAT NEXT

Re-invoke the command with a valid list of arguments.

PWR-375 (error) The %s argument cannot be used without %s.

DESCRIPTION

The command was invoked with an argument that is meaningless or illegal unless used in conjunction with some other particular arguments.

WHAT NEXT

Re-invoke the command with a valid list of arguments.

PWR-376 (error) Bad arguments.

DESCRIPTION

The command was invoked with an illegal list of arguments.

WHAT NEXT

Re-invoke the command with a valid list of arguments.

PWR-377 (error) The %s value must be non-negative.

DESCRIPTION

The command argument needs a numeric value that is greater or equal to 0.

WHAT NEXT

Re-invoke the command with a non-negative value for this argument.

PWR-378 (warning) Unknown pins on clock gating cell '%s'. The clock gate will not be removed or rewired.

DESCRIPTION

There are unknown pins on the clock gating hierarchy. Only clock, enable, test control, test observation and gated clock output pins are allowed. Since the cell might contain additional functionality it will not be removed or rewired.

WHAT NEXT

Detect the step that inserted additional pins on the clock gating hierarchy and fix it. Run the rewire or remove clock gating command after that.

PWR-379 (warning) Using scan_enable with latch free clock gating may cause DRC violations during test insertion

DESCRIPTION

When using latch free clock gating with scan_enable, the glitches or edges in scan_enable can propagate to the clock pin of the register. Since scan_enable is not constrained during parrallel input vector setup, there is a potential risk of scan_enable switching and hence causing an unwanted clock edge at the register clock pin. The test insertion or test DRC tool might issue violations like, clock pin not controllable or capture violations in this case.

WHAT NEXT

If you can ensure that there will be no unwanted glitching at scan_enable, you can safely ignore this warning. Otherwise reconsider using test_mode control signal or using a latch based clock gating style

PWR-380 (warning) Required pins missing on clock gating cell '%s'. The clock gate will not be removed or rewired.

DESCRIPTION

Any of the mandatory pins (EN, CLK, ENCLK) of the clock gating hierarchy is missing. This could happen because of two reasons. The pins got removed by some other tools. OR the pins as such exist, but some of their attributes got removed.

WHAT NEXT

Detect the step that edited the clock gating hierarchy and fix it. Run the rewire or remove clock gating command after that.

PWR-381 (error) Use the 'uniquify' command to fix multiply instantiated designs.

DESCRIPTION

Hookup_testports command needs the design to be uniquified in XG mode.

If you don't want some instances to be modified please set_dont_touch those instances.

WHAT NEXT

You can resolve the multiply instantiated designs into separate designs using uniquify. If this is not acceptable, you can set_dont_touch on instances which should not be modified. Run hookup_testports after this.

PWR-382 (error) No objects are specified; a list of objects or -select is required.

DESCRIPTION

This command needs acts on a number of objects which can be specified explicity as a list of objects, or implicity using the -select argument.

WHAT NEXT

Re-invoke the command with a list of object in its argument, or use the -select

option.

PWR-383 (error) Both an object list and -select are given as arguments.

DESCRIPTION

The command is invoked with a list of objects in its arguments together with the -select option. This command works on a number of objects that can be specified explicitly as a list of objects in its arguments, or implicitly using the -select option. The two options are mutually exclusively.

WHAT NEXT

Check the command arguments and reinvoke the command excluding the -select option or the list of objects in its arguments.

PWR-384 (error) -hier and/or -instance options given without -select.

DESCRIPTION

The -hier and -instance options can only be used with the -select option.

WHAT NEXT

Check the command line arguments and reinvoke the command with the -select option, or without the -hier/-instance options.

PWR-385 (error) %s is %s; it is not a valid instance.

DESCRIPTION

An invalid instance is given as an argument to this command. Only non-leaf cells are valid instances.

WHAT NEXT

Reinvoke the command with valid instances.

PWR-386 (error) State/Path dependent switching activity given with -select.

DESCRIPTION

State Dependent (-state_dep option) and Path Dependent (-path option) switching activity can only be used when the design objects being annotated are specified explicity as a list of objects. State/Path dependent switching activity cannot be used with the -select option.

WHAT NEXT

Reinvoke the command without the -select option.

PWR-387 (error) Unrecognized select type: %s.

DESCRIPTION

An invalid argument is given to the -select option. The following selection types can be used with the -select option: regs, tris, inputs, outputs, inouts, ports, nets.

WHAT NEXT

Reinvoke the command with a valid list of selection types given to the -select argument.

PWR-388 (error) Empty type list given to -select.

DESCRIPTION

The -select option needs a non-empty list of selection types.

WHAT NEXT

Reinvoke the command with a non-empty list of selection types.

PWR-390 (warning) -max_fanout

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-391 (warning) Clock gating style has non-default -max_fanout.

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-392 (warning) Clock gate replacement requires at least one designated clock port; no replacement is performed on design %s.

DESCRIPTION

Before clock gate replacement can be performed, the clock ports must be identified with the **create_clock** command.

WHAT NEXT

Define the clock ports with the **create_clock** command.

SEE ALSO

replace_clock_gates (2), **create_clock** (2).

PWR-393 (warning) Cell %s is not replaced by a clock gate since it is not on a clock tree.

DESCRIPTION

Clock gate replacement only considers cells that are on the clock tree. The cell that was included with the **set_replace_clock_gates** command does not appear on the clock tree, hence it was not considered for clock gate replacement. Perhaps the wrong port was defined as the clock port, or there are multiple clock ports, and some of them where not properly defined with the **create_clock** command.

WHAT NEXT

Do not include this cell for clock gate replacement, or define the missing clock port with the **create_clock** command.

SEE ALSO

insert_clock_gating (2), **set_replace_clock_gates** (2), **create_clock** (2).

PWR-394 (warning) Cell %s is not replaced by a clock gate since it depends on multiple clock signals.

DESCRIPTION

Clock gate replacement will only replace the combinational cell when it can find a matching clock-gating cell. The specified combinational cell has multiple clock inputs. Since the Power Compiler clock gates only have one clock input, there is no opportunity for clock gate replacement. Perhaps the other path is not really a clock input -- in that case the driving port should not be defined as a clock port.

WHAT NEXT

Remove the clock for the port that is not a clock port with the **remove_clock command**, or exclude the combinational cell with the **set_replace_clock_gates** command.

PWR-395 (warning) The arc from %s to %s of cell %s is not unate; no clock gate replacement is performed upstream of the

cell output.

DESCRIPTION

Clock gate replacement will only replace the combinational cell with a clock gate when it can find a matching clock-gating cell. Only cells with AND/NOR or OR/NAND functionality can be replaced. The specified cell has a non-unate arc from the clock input to it’s output, hence it cannot be replaced by a Power Compiler clock gate.

WHAT NEXT

Reconsider the RTL implementation. If the functionality of this manually inserted clock gate is intended, exclude the cell with the **set_replace_clock_gates** command.

PWR-396 (warning) No compatible clock gating structure available to replace manually inserted clock gate %s; no clock gate replacement is performed for this cell.

DESCRIPTION

Clock gate replacement will only replace the combinational cell with a clock gate when it can find a matching clock-gating cell. Only cells with AND/NOR or OR/NAND functionality can be replaced

WHAT NEXT

Exclude the cell with the **set_replace_clock_gates** command.

PWR-397 (warning) Cell %s is a module which cannot be ungated; clock gate %s will not be removed.

DESCRIPTION

Module-level clock gates, i.e., clock gates which are driving modules cannot be removed, because the module cannot be ungated at the top level of hierarchy in the design. If the module contains registers, it can be ungrouped to bring the registers to the top level. If the module is a black-box cell, it cannot be further ungrouped; in that case removal of the clock gating cell is not possible.

WHAT NEXT

Ungroup the module with the **ungroup** command.

PWR-398 (error) Cell %s is a module which cannot be ungated; clock gate %s will not be removed.

DESCRIPTION

Module-level clock gates, i.e., clock gates which are driving modules cannot be removed, because the module cannot be ungated at the top level of hierarchy in the design. If the module contains registers, it can be ungrouped to bring the registers to the top level. If the module is a black-box cell, it cannot be further ungrouped; in that case removal of the clock gating cell is not possible.

WHAT NEXT

Ungroup the module with the **ungroup** command.

PWR-399 (warning) Cell %s drives both rising and falling edge registers; no clock gate replacement is performed upstream of the cell output.

DESCRIPTION

Clock gate replacement can only be performed if the fanout of the cell consists strictly of registers with the same edge sensitivity.

WHAT NEXT

Split the positive and negative edge registers in two groups, and use two different gated clock signals driven by two different clock-gating cells.

PWR-400 (warning) Cell %s drives a module output; no clock gate replacement is performed upstream of the cell output.

DESCRIPTION

Clock gate replacement can only be performed if the fanout of the cell consists

strictly of registers with the same edge sensitivity. Because the clock signal is also fed to an output port, it is not possible to determine what the edge type will be in the fanout of this output port. Hence, no replacement is performed.

WHAT NEXT

Split the output port from the internal signals by using two different gated clock signals driven by two different clock-gating cells.

PWR-401 (warning) Cannot determine active edge of register %s; no clock gate replacement is performed upstream of this cell.

DESCRIPTION

Clock gate replacement can only be performed if the fanout of the cell consists strictly of registers with the same edge sensitivity. For this sequential cell the edge type cannot be determined. Hence, no replacement is performed.

WHAT NEXT

If the edge type is known, specify it with the **set_replace_clock_gates** command.

PWR-402 (warning) Cell %s cannot be replaced by a clock gate.

DESCRIPTION

Clock gate replacement will only replace the combinational cell with a clock gate when it can find a matching clock-gating cell. Only combinational cells with a single output and at least two inputs are considered. Buffers and inverters are never considered for clock gate replacement, unless they are explicitly included with the **set_replace_clock_gates command.**

WHAT NEXT

Do not include this cell with the **set_replace_clock_gates** command.

PWR-403 (warning) Cannot determine active edge at output of

cell %s; no clock gate replacement is performed for this cell.

DESCRIPTION

Clock gate replacement can only be performed if the fanout of the cell consists strictly of registers or modules with the same edge sensitivity. For this manually inserted clock gate the edge type of the cells in the fanout cannot be determined. Hence, no replacement is performed.

WHAT NEXT

In case there are black box modules in the fanout, specify the edge type for those modules with the **set_replace_clock_gates** command. In case of mixed edge type, exclude the cell with the **set_replace_clock_gates -exclude** command. If there is an output in the fanout for which the edge type can be ignored, force clock gate replacement by including the cell with the **set_replace_clock_gates -include** command.

PWR-404 (warning) Pin %s of clock gate %s is not a clock input; no clock gate replacement is performed upstream of this pin.

DESCRIPTION

Clock gate replacement allows Power Compiler clock gating cells on the clock path, but the clock net should drive the clock input of these cells. When this is not the case, the edge type of the fanout of this cell cannot be determined, hence no replacement can be performed. Most likely, this warning occured because the wrong port was assigned as the clock port.

WHAT NEXT

Remove the clock for the port that is not a clock port with the **remove_clock command**, or exclude the combinational cell with the **set_replace_clock_gates** command.

PWR-405 (warning) Cell %s is too complex to be replaced by a clock gate; no clock gate replacement is performed for this cell.

DESCRIPTION

Clock gate replacement will only replace the combinational cell with a clock gate when it can find a matching clock-gating cell. Only cells with AND/NOR or OR/NAND functionality can be replaced. The specified cell has a mix of AND and OR behavior, hence it cannot be replaced by a Power Compiler clock gate.

WHAT NEXT

Reconsider the RTL implementation. If the functionality of the manually inserted clock gate is intended, exclude the cell with the **set_replace_clock_gates** command.

SEE ALSO

insert_clock_gating (2), **set_replace_clock_gates** (2).

PWR-406 (warning) Clock gate replacement for cell %s demands a latch-%s clock gating style; no replacement is performed for this cell.

DESCRIPTION

Clock gate replacement will only replace the combinational cell with a clock gate when it can find a matching clock-gating cell. Only cells with AND/NOR or OR/NAND functionality can be replaced. The combination of the clock-gating style and the edge type does not match the functionality of the manually inserted clock gate, hence it cannot be replaced by a Power Compiler clock gate.

WHAT NEXT

Change the clock gating style from latch-based to latch-free or visa-versa to match the functionality of the cell.

SEE ALSO

replace_clock_gates (2), **set_clock_gating_style** (2).

PWR-407 (warning) Combinational loop detected at cell %s; no clock gate replacement is performed upstream of this cell.

DESCRIPTION

If a combinational loop exists on the clock path, the edge type of the registers in the fanout is undefined, hence no clock gate replacement can be performed. This warning usually indicates that something is wrong with the RTL description, since combinational loops on the clock path are almost never intentional.

WHAT NEXT

Revise the RTL description.

PWR-408 (error) The port %s is used in more than one of these options: -rising_edge_clock, -falling_edge_clock, or -undo.

DESCRIPTION

The same port of a design cannot have different edge types. If an instance pin is specified, the corresponding design port is used instead, since the edge type property is design specific. It is not allowed to specify the same port in more than one list in the options of the **set_replace_clock_gates** command.

WHAT NEXT

Remove the pin from one of the lists, as it cannot have 2 edge types

PWR-409 (warning) Instance '%s' of design '%s' is not clock gated because other instances of the same design are excluded from clock gating.

DESCRIPTION

If a design is not uniquified, and some instances of a subdesign are excluded from clock gating with the **set_dont_touch command**, all other instances are automatically excluded as well.

WHAT NEXT

Uniquify the conflicting instances before executing **insert_clock_gating -global**, or remove the set_dont_touch directive for the multiply-instantiated subdesigns.

PWR-410 (warning) Given -clock argument '%s' does not exist.

DESCRIPTION

The string argument of the -clock option of set_switching_activity needs to be an existing clock. The -clock option of set_switching_activity associates a clock with the annotated object. When specified, toggle rates annotated to design objects will

be divided by the period of the associated clock (also called the related clock) when power values are calculated.

WHAT NEXT

Check that the specified -clock option is correct, re-issue the set_switching_activity with the correct clock name if it is not. Otherwise, create a clock with the name of the -clock argument before calculating power numbers.

PWR-411 (warning) Both -clock and -period arguments are specified.

DESCRIPTION

A set_switching_activity command has been specified with both the -clock and -period arguments, which is probably a user error. The -period argument specifies the time period relative to which the given -toggle_rate is applied. Basically, the value of the -toggle_rate argument is divided by the value of the -period argument at the time of the annotation. For instance, the following two commands:

```
set_switching_activity [get_net n1] -toggle_rate 2.0  -period 100.0
set_switching_activity [get_net n1] -toggle_rate 0.02
```

are equivalent since both annotate a toggle rate of 0.02 to the net n1.

The -clock argument specifies a related clock for the annotated object. When an object has a related clock, the annotated toggle rate is divided by the clock period during power calculations. For example,

```
create_clock clk -period 100.0 set_switching_activity [get_net n1] -toggle_rate 2.0
-clock clk
```

annotates the toggle rate of 2.0 to the net n1. When power values are calculated (assuming that the period of clk remains changed) a toggle rate of 0.02 is used for the net n1. The user can change the clock period of clk and get different effective toggle rates for the net n1, without re-annotating the switching activity of the net n1.

When both the -period and -clock options are specified, the toggle rate value is first divided by the value of the -period argument during the time of annotation, and then divided again by the period of the clock given by the -clock option during power calculation. This is often not the intended behaviour.

WHAT NEXT

Check the arguments of the set_switching_activity command, and make sure that giving both the -period and -clock arguments to the set_switching_activity command is intended. You can avoid getting this warning by specifying two set_switching_activity commands:

set_switching_activity -toggle_rate <tr> -period <p> ... set_switching_activity -clock <clk>

which has the same effect as the single command:

set_switching_activity -toggle_rate <tr> -period <p> -clock <clk> ...

PWR-412 (warning) The clock '%s' associated with the %s '%s' does not exist or has no period.

DESCRIPTION

The design object (net, pin, or port) given in the warning message has a clock associated with it that does not exist or has no period. A clock can be associated to a design object by using the -clock option of the set_switching_activity command. The associated, or related, clock period is used to calculate the effective toggle rate of the object used in power calculations. The effective toggle rate is the annotated toggle rate divided by the period of the related clock. When a related clock is not specified, the annotated toggle rate relative to the library time unit is used. In this case, the related clock does not exists in the current design or has no period; for power calculations, the related clock period is assumed to be 1.0.

WHAT NEXT

Create the required clock and re-issue the command giving the warning message.

PWR-413 (warning) The variable '%s' is obsolete; use '%s' instead.

DESCRIPTION

The variables for specifying the default switching activity values for unannotated primary inputs and black-box outputs are: **power_default_toggle_rate** and **power_default_static_probability**.

The variable you are using is obsolete and its value is ignored.

WHAT NEXT

Modify your scripts to use the **power_default_toggle_rate** and **power_default_static_probability** variables.

PWR-414 (warning) Design has unannotated primary inputs.

DESCRIPTION

A number of primary input ports of your design are not user annotated with switching activity. Default switching activity values are used for these ports. This may result in inaccurate power numbers.

WHAT NEXT

Check the switching activity annotation of your primary inputs. You can use the command:

```
report_saif -missing
```

to check which ports are not user annotated. Annotate the switching activities of these ports using the set_switching_activity or read_saif commands. You can set the value of the variable **power_sa_propagation_verbose** to *true* before propagating the switching activity to get a warning message for each unannotated black-box output. You can also force a verbose re-propagation of the switching activity information by calling **propagate_switching_activity -verbose**.

PWR-415 (warning) Design has unannotated sequential cell outputs.

DESCRIPTION

Some sequential cell outputs are not user annotated with switching activity. The switching activity propagation mechanism of Power Compiler will be used to derive these values. Propagated switching activity of sequential cells may be less accurate than the propagted activity of combination cells.

WHAT NEXT

Although the unannotated switching activity values of the sequential cell outputs will be derived by Power Compiler, more accurate power numbers can be achieved if these are user annotated with accurate switching activities. You can use:

```
report_saif -type rtl -flat -missing
```

to check how many sequential cells are not user annotated.

PWR-416 (warning) The unannotated %s ’%s’ %s a black-box

output.

DESCRIPTION

The given net or pin is not user annotated with switching activity values. Default switching activity values based on the variables:

power_default_toggle_rate power_default_static_probability

will be used since the functionality of the driving cell cannot be determined. The cell driving the net is either a black-box or has unknown functionality.

This may have an impact on the accuracy of the calculated power values.

Note that this warning message is only issued when the switching activity propagation mechanism is called in verbose mode. The boolean variable **power_sa_propagation_verbose** specifies the default propagation verbose level.

WHAT NEXT

You can use the **report_cell** command on the driving cell to check the type of cell. Use the **set_switching_activity** or **read_saif** command to annotate the switching activity of the specified net.

PWR-417 (warning) The net '%s' is only annotated with a static probability value. A default toggle rate value of %f is used.

DESCRIPTION

This warning message occurs when the net has static probability annotation but no toggle rate annotation, no related clock is associated with the net, and a default toggle rate value has to be annotated. Default switching activity values have to be annotated when they are not user annotated and Power Compiler cannot estimate the missing switching activity. This occurs on nets connected to primary inputs and black-box outputs.

The default toggle rate value is derived from the two variables: **power_default_toggle_rate** and **power_default_toggle_rate_type**.

If the value of the **power_default_toggle_rate_type** is **fastest_clock** then the default toggle rate value is derived by multiplying the value of the **power_default_toggle_rate** with the frequency of the fastest clock in the design. If no clock is defined in the current design, then a frequency value of 1.0 is used.

If the value of the **power_default_toggle_rate_type** is **absolute** then the value of the **power_default_toggle_rate** variable is used as the default toggle rate value.

WHAT NEXT

If possible annotate both the toggle rate and static probability values for this net.

PWR-418 (warning) The net '%s' is only annotated with a static probability value and the related clock '%s'. A default toggle rate value of %f is used.

DESCRIPTION

This warning message occurs when the net has static probability annotation but no toggle rate annotation, a related clock is associated with the net, and a default toggle rate value has to be annotated. Default switching activity values have to be annotated when they are not user annotated and Power Compiler cannot estimate the missing switching activity. This occurs on nets connected to primary inputs and black-box outputs.

The default toggle rate value is derived from the two variables: **power_default_toggle_rate** and **power_default_toggle_rate_type**.

If the value of the **power_default_toggle_rate_type** is **fastest_clock** then the default toggle rate value is derived by multiplying the value of the **power_default_toggle_rate** with the frequency of the related clock.

If the value of the **power_default_toggle_rate_type** is **absolute** then the value of the **power_default_toggle_rate** variable is used as the default toggle rate value.

WHAT NEXT

If possible annotate both the toggle rate and static probability values for this net.

PWR-419 (warning) The net '%s' is annotated with a toggle rate but no static probability. A default static probability value of %f is used.

DESCRIPTION

This warning message occurs when the net has toggle rate annotation but no static probability annotation. Power Compiler needs both toggle rate and static probability values on a net in order to use its switching activity during propagation. If a static probability value is missing, a default value is assumed and the annotated toggle rate and the default static probability value are used during propagation. In

such cases, the default static probability value is assumed to be 0.0 if the annotated toggle rate is 0.0, otherwise the value given by the **power_default_static_probability** variable is used.

WHAT NEXT

If possible annotate both the static probability and toggle rate values for this net.

PWR-420 (warning) The partially annotated net '%s' has an estimated %s value of %f.

DESCRIPTION

Only the static probability value of the given net is user annotated. The unannotated toggle rate value is derived using the switching activity propagation mechanism of Power Compiler. The user annotated static probability value is not overwritten with the propagated value, but it is not used to derive the missing user annotation.

Both the static probability and toggle rate values are required in order for the switching activity of a particular net is used during propagation. If the static probability is missing a default value is assumed, but a default value cannot be assumed for such missing toggle rates, so the annotated static probability value cannot be used during propagation.

It is desirable that both the toggle rate and static probability values of design objects are user annotated. Partial annotation may result in inaccurate power calculations.

WHAT NEXT

If possible, annotate both the toggle rate and static probability of the given object.

PWR-421 (warning) Invalid switching activity annotation on constant net(s) is being ignored.

DESCRIPTION

The design contains logic 0 or 1 nets, or cell pins driven by such nets, that have been annotated with invalid switching activity. Basically, for constants the annotated toggle rate value must be 0. The static probability for logic 1 objects must 1.0 and that of logic 0 must be 0.0.

Since the user annotation is clearly invalid, it is ignored and the correct switching activity values will be used for power calculation purposes.

WHAT NEXT

This is a warning message. The invalid user annotation is being ignored during power calculation.

PWR-422 (warning) The partially annotated net '%s' has a derived %s value of %f.

DESCRIPTION

Only one of the toggle rate and static probability values of the given net is user annotated. The unannotated value has been derived by Power Compiler and may be used by the switching activity propagation mechanism to estimate the switching activity of other unannotated design objects.

WHAT NEXT

If possible, annotate both the toggle rate and static probability of the given object.

PWR-423 (warning) The value of the variable '%s' is invalid; the default value of %s will be used instead.

DESCRIPTION

The following variables:

float power_default_static_probability float power_default_toggle_rate

are used to derive default switching activity values of primary inputs and black box outputs that have not been annotated by the user. Valid values for these are:

The value of power_default_static_probability should be a floating number between 0.0 and 1.0 both inclusive. The value of power_default_static_probability should be a floating number greater or equal to 0.0.

When an invalid value for these variables is specified, then the default value of 0.5 will be used for deriving default switching activity values.

Also, if the value of power_default_static_probability is 1.0 or 0.0, then the value of power_default_toggle_rate should be 0.0. If the value of power_default_toggle_rate is not 0.0, then Power Compiler will issue this warning

message and use the value 0.0 for default toggle rates. If the value of power_default_toggle_rate is 0.0, then the value of power_default_static_probability should be 0.0 and 1.0. If the value of power_default_toggle_rate is neither 1.0 nor 0.0, then this warning message will be issued, and a default value of 0.0 will be used.

WHAT NEXT

Set the values of power_default_static_probability and power_default_toggle_rate to valid value.

SEE ALSO

power_default_static_probability (3), **power_default_toggle_rate** (3).

PWR-424 (warning) Main library '%s' does not specify the following unit%s required for power: '%s'.

DESCRIPTION

The following units are required for power calculations: Voltage, Capacitance, Time, and Leakage Power units. If some of these units are not defined in your technology library then the power reports may be unitless.

The main library is determined as follows: During reporting the main library is the first library in the link path that contains a cell that is used in the design. During optimization the main library is the first target library specified.

WHAT NEXT

Use a library that defines the units required for power. Specify this as the main library by making it the first library in your link and/or target library path list. You will need to remove the **local_link_library** attribute from the current design if this specifies a main library that does not contain power units. You can also use the **set_local_link_library** command to change the local link libraries after reading a compiled .db design file.

PWR-425 (error) The cell '%s' is a leaf cell.

DESCRIPTION

A leaf cell is specified where a hierachical cell is expected.

WHAT NEXT

Please specify a hierarchical cell. You can use the report_cell command to check whether a cell is hierarchical.

PWR-426 (error) The command '%s' is only available in XG mode.

DESCRIPTION

The specified command is only available in XG mode.

WHAT NEXT

Please use XG mode to run this command.

PWR-427 (warning) Cannot determine the time units, using 1 ns.

DESCRIPTION

This warning message is displayed during write_saif when the time units cannot be obtained from the main synthesis library. This usually happens when the technology library is not yet loaded, or when the first element in your link/target library list does not have a defined time unit. For instance, if the first element of your link library is a synthetic library, then it probably does not specify a time unit. In such cases, Power Compiler will assume that the intended synthesis time units are 1 ns.

WHAT NEXT

You can use a technology library that defines a time unit as the first element of your link and target libraries.

PWR-428 (warning) Design has unannotated black-box outputs.

DESCRIPTION

The design contains a number of black-box cells whose outputs are not user annotated with switching activity information. Since switching activity cannot be propagated for design nets connected to black-box outputs, default values are used for these nets. This may result in inaccurate power numbers.

WHAT NEXT

Check the switching activity annotation of the nets connected to black-box outputs. You can set the value of the variable **power_sa_propagation_verbose** to *true* before propagating the switching activity to get a warning message for each unannotated black-box output. You can also force a verbose re-propagation of the switching activity information by calling **propagate_switching_activity -verbose**.

PWR-429 (warning) The unannotated net '%s' is driven by a primary input port.

DESCRIPTION

The given net is driven by a primary input port and is not user annotated with switching activity values. Default switching activity values based on the variables:

power_default_toggle_rate power_default_static_probability

will be used since the unannotated switching activity cannot be estimated using the propagation mechanism.

This may have an impact on the accuracy of the calculated power values.

Note that this warning message is only issued when the switching activity propagation mechanism is called in verbose mode. The boolean variable **power_sa_propagation_verbose** specifies the default propagation verbose level.

WHAT NEXT

Use the **set_switching_activity** or **read_saif** command to annotate the switching activity of the specified net.

PWR-430 (warning) The cell %s is not a hierarchical clock-gating cell and cannot be removed.

DESCRIPTION

You receive this error message because you issued the **remove_clock_gating** command with the **-all** option on a design that has a nonhierarchical clock-gating cell. Such cells cannot be removed.

WHAT NEXT

The other (hierarchical) clock gates will still be marked for removal with the **remove_clock_gating** command. Do not ungroup the hierarchical clock-gating cells

during the compile flow.

SEE ALSO

remove_clock_gating (2), **report_clock_gating** (2), **ungroup** (2).

PWR-431 (error) Use at least one of the options -rising_edge_clock, -falling_edge_clock, or -undo with the set_module_clock_edges command.

DESCRIPTION

The **set_module_clock_edges** requires at least one of the options above.

WHAT NEXT

Specify at least on of the options.

PWR-432 (error) Use at least one of the options -include_instances, -exclude_instances, or -undo with the set_module_clock_gates command.

DESCRIPTION

You receive this error message because the **set_module_clock_gates** did not mark the cells to be included or excluded from clock-gate replacement. Use at least one of these three options: **-include_instances**, **-exclude_instances**, or **-undo**. The arguments to the options should be cells in the current design intended as manually inserted clock gates.

WHAT NEXT

Use the appropriate set of options for the command. Make sure you are using the correct name of the cells you want to include or exclude for clock-gate replacement. To find cells in the design, use the **find** command.

SEE ALSO

find (2), **insert_clock_gating** (2), **set_module_clock_gates** (2).

PWR-433 (error) Clock gate %s is marked for rewiring and cannot be ungated; its driving clock gate %s will not be removed.

DESCRIPTION

You receive this error message because you specified as an option to the **remove_clock_gating** command a cell that is marked for rewiring by the **rewire_clock_gating** command.

WHAT NEXT

A cell that is marked for rewiring cannot be marked for removal. If you want to use the **compile** command with the **-incremental** option (or **physopt** and **physopt -incremental**) to remove the cell, use the **-undo** option of the **rewire_clock_gating** command. Use the cell you specified as an argument for the **-gated_objects** option. Then reissue the **remove_clock_gating** command.

SEE ALSO

compile (2), **remove_clock_gating** (2), **rewire_clock_gating** (2).

PWR-434 (error) Clock gate %s is marked for rewiring and cannot be removed.

DESCRIPTION

You receive this error message because you specified as an option to the **remove_clock_gating** command a clock-gating cell that is marked for rewiring by the **rewire_clock_gating** command.

WHAT NEXT

A clock gating cell that is marked for rewiring cannot be removed. If you want to use the **compile** command with the **-incremental** option (or **physopt** and **physopt -incremental**) to remove the cell, use the **-undo** option of the **rewire_clock_gating** command. Use the cell you specified as an argument for the **-gated_objects** option. Then reissue the **remove_clock_gating** command.

SEE ALSO

compile (2), **remove_clock_gating** (2), **rewire_clock_gating** (2).

PWR-435 (error) Use at least one of the options -gating_cell or -undo with the rewire_clock_gating command.

DESCRIPTION

The **rewire_clock_gating** command requires at least one of the options above.

WHAT NEXT

Specify at least one of the options.

PWR-436 (warning) max_fanout ignored when power_cts_driven_placement set to true.

DESCRIPTION

In the CTS driven clock gate placement flow, there is no need to specify max_fanout constraint. Power Compiler resets the max_fanout to the default number of 2048 in this case to maximize power savings.

WHAT NEXT

No action required. To avoid the warning, remove **-max_fanout** option of **set_clock_gating_style** command.

PWR-437 (error) Port %s is an output; edge specification with the set_replace_clock_gates command can only be applied to input ports.

DESCRIPTION

The pins or ports in the object lists of the **-rising_edge_clock** or **-falling_edge_clock** options for the **set_replace_clock_gates** command have to be input ports.

WHAT NEXT

Do not attempt to specify the clock edge type for output ports.

PWR-438 (error) -proximity can not be used with any other options except -verbose

DESCRIPTION

-proximity option can not be combined with any other option except -verbose.

WHAT NEXT

Reissue rewire_clock_gating command with correct options.

PWR-439 (error) Enable path to clock gating cell '%s' is unconstrained.

DESCRIPTION

Enable path to the above clock gate does not have any timing constraints. Since **merge_clock_gates** can not honor the **-min_slack** option in this case, no merging will be done.

WHAT NEXT

Most probable cause for this is, the design does not have any clocks. Run **create_clock** with a valid **-period** option and then reissue **merge_clock_gates -min_slack <value>** command. Also explore other reasons why enable path is not constratined. For unconditional merging of clock gates, use **merge_clock_gates** with out **-min_slack** option.

PWR-440 (warning) Not clock-gating register %s due to structural limitations.

DESCRIPTION

You receive this warning message when certain registers are not clock-gated due to structural limitations. This situation can occur during hierarchical clock-gating (issued with **insert_clock_gating -global**) on multiple-instantiated designs. Because of differences instantiations of the design, not all instances of the design can be treated the same. Because of this limitation, it can occur that registers are excluded from clock-gating.

WHAT NEXT

Uniquify the conflicting instances before executing **insert_clock_gating -global**.

SEE ALSO

insert_clock_gating (2), **set_clock_gating_style** (2).

PWR-441 (Error) The latch specified (%s) for %s edge logic does not have the required functionality

DESCRIPTION

The specified latch can not be used in the clock gating circuitry since it does not have the required functionality.

Power Compiler uses a transparent low latch for positive edge triggered registers and transparent high latch for negative edge triggered logic.

WHAT NEXT

Specify another latch which sticks to the above requirement

PWR-442 (warning) Cannot determine active edge for module input pin %s; no clock gate replacement is performed upstream of this module.

DESCRIPTION

Clock gate replacement can only be performed if the edge type of the cells in the fanout can be determined. For registers the edge type can be determined automatically, but for black box modules the edge type must be specified explicitly with the **set_replace_clock_gates** command.

WHAT NEXT

Set the edge type with the **set_replace_clock_gates** command.

PWR-443 (information) Unannotated %s toggle rate for false %s

of pin '%s' is automatically set to 0.

DESCRIPTION

The specified pin is partially annotated with state-dependent and/or path-dependent (SDPD) toggle rate values. Power Compiler is automatically setting the SDPD toggle rate value of unannotated false states/arcs to 0.0. False states are states that always evaluate to 0 and include the default state in pins where the other states cover all possible states of the cell. False arcs are invalid paths from an input to an output.

This message is issued by the SDPD fixing step which can be controlled by the variable **power_fix_sdpd_annotation**.

WHAT NEXT

This is an information message; no user action is required.

SEE ALSO

power_fix_sdpd_annotation (3).

PWR-444 (information) Non-zero %s toggle rate annotation on false %s of pin '%s' is automatically set to 0.

DESCRIPTION

The specified pin is annotated with non-zero state-dependent and/or path-dependent (SDPD) toggle rate values on false states/arcs. Power Compiler is automatically setting the SDPD toggle rate value of false states/arcs to 0.0. False states are states that always evaluate to 0 and include the default state in pins where the other states cover all possible states of the cell. False arcs are invalid paths from an input to an output.

This message is issued by the SDPD fixing step which can be controlled by the variables **power_fix_sdpd_annotation**, **power_fix_sdpd_annotation_verbose** and **power_sdpd_message_tolerance**.

WHAT NEXT

This is an information message; no user action is required.

SEE ALSO

power_fix_sdpd_annotation (3), **power_fix_sdpd_annotation_verbose** (3),

power_sdpd_message_tolerance (3).

PWR-445 (information) The user annotated SDPD %s toggle rates on pin '%s' are being scaled so they add up to half of the pin toggle rate.

DESCRIPTION

The user annotated rise/fall state-dependent and/or path-dependent (SDPD) toggle rate values on the specified pin do not add to half of the non-SDPD toggle rate on the pin (i.e. the toggle rate of the net connected to the pin). Power Compiler is scaling the SDPD toggle rate values so that they add up to half of the pin toggle rate.

This message is issued by the SDPD fixing step which can be controlled by the variables **power_fix_sdpd_annotation**, **power_fix_sdpd_annotation_verbose** and **power_sdpd_message_tolerance**.

WHAT NEXT

This is an information message; no user action is required.

SEE ALSO

power_fix_sdpd_annotation (3), **power_fix_sdpd_annotation_verbose** (3), **power_sdpd_message_tolerance** (3).

PWR-446 (information) The annotated SDPD %s toggle rates on pin '%s' add up to more than half the pin toggle rate; Annotated toggle rates are being scaled down and the unannotated toggle rates are automatically annotated with 0.

DESCRIPTION

The specified pin is partially annotated with state-dependent and/or path-dependent (SDPD) toggle rates. The user annotated rise/fall (SDPD) toggle rate values add to more than half of the non-SDPD toggle rate on the pin (i.e. the toggle rate of the net connected to the pin). Power Compiler is scaling the user annotated SDPD toggle rate values so that they add up to half of the pin toggle rate. Also, the non-annotated SDPD toggle rate values for this pin are set to 0.

This message is issued by the SDPD fixing step which can be controlled by the

variables **power_fix_sdpd_annotation**, **power_fix_sdpd_annotation_verbose** and **power_sdpd_message_tolerance**.

WHAT NEXT

This is an information message; no user action is required.

SEE ALSO

power_fix_sdpd_annotation (3), **power_fix_sdpd_annotation_verbose** (3), **power_sdpd_message_tolerance** (3).

PWR-447 (information) Scaling the unannotated SDPD toggle rates for pin '%s' since the totals of the rise and fall SDPD toggle rates are different.

DESCRIPTION

The sums of the rise and fall state-dependent and/or path-dependent (SDPD) toggle rates on this pin differ. Power Compiler is scaling the user annotated SDPD toggle rate values so that the rise and fall sums become the same.

This message is issued by the SDPD fixing step which can be controlled by the variables **power_fix_sdpd_annotation**, **power_fix_sdpd_annotation_verbose** and **power_sdpd_message_tolerance**.

WHAT NEXT

This is an information message; no user action is required.

SEE ALSO

power_fix_sdpd_annotation (3), **power_fix_sdpd_annotation_verbose** (3), **power_sdpd_message_tolerance** (3).

PWR-448 (information) The toggle rate on pin '%s' is automatically set to the total of the annotated SDPD pin toggle

rates.

DESCRIPTION

The specified pin is annotated with state-dependent and/or path-dependent (SDPD) toggle rates, but not with a non-SDPD toggle rate value (i.e. a toggle rate on the net connected to the pin). Power Compiler is setting the non-SDPD toggle rate for this pin to be equal to the sum of the SDPD toggle rates.

This message is issued by the SDPD fixing step which can be controlled by the variable **power_fix_sdpd_annotation**.

WHAT NEXT

This is an information message; no user action is required.

SEE ALSO

power_fix_sdpd_annotation (3).

PWR-449 (information) The toggle rate on pin '%s' is automatically set to twice the total of the annotated SDPD %s pin toggle rates.

DESCRIPTION

The specified pin is annotated with state-dependent and/or path-dependent (SDPD) toggle rates, but not with a non-SDPD toggle rate value (i.e. a toggle rate on the net connected to the pin). Power Compiler is setting the non-SDPD toggle rate for this pin to be equal to twice of the sum of the rise/fall SDPD toggle rates.

This message is issued by the SDPD fixing step which can be controlled by the variable **power_fix_sdpd_annotation**.

WHAT NEXT

This is an information message; no user action is required.

SEE ALSO

power_fix_sdpd_annotation (3).

PWR-450 (warning) The value of the variable '%s' is invalid; the default value of %s will be used instead.

DESCRIPTION

The value of the following variable:

string power_sa_propagation_effort

specifies the default propagation effort used when propagating switching activity. This value is used when a command option specifying the propagation effort is not used. For instance, the **-analysis_effort** option of the **report_power** command, and the **-effort** option of the **propagate_switching_activity** command, specify the propagation effort. The valid values for this variable are: *low*, *medium* and *high*. If an invalid value is set to this variable, a default value is assumed.

WHAT NEXT

Set the value of the power_sa_propagation_effort **variable to a valid one.**

SEE ALSO

power_sa_propagation_effort (3).

PWR-451 (warning) The -exclude_boundary_nets flag is obsolete.

DESCRIPTION

The **-exclude_boundary_nets** flag of the **report_power** command is obsolete, and it is being ignored by the command. The **report_power** command now excludes the net switching power of primary input nets by default, since this switching power is not consumed by the current design, but rather by the external designs driving the input ports.

The switching power of nets driven by an input or inout port is included only if the net is also driven by a cell in the current design. You can include the switching power of all input and inout ports by using the **-include_input_nets** flag of the **report_power** command

WHAT NEXT

The **-exclude_boundary_nets** is being ignored. You can call **report_power** without this flag.

PWR-452 (warning) There are %d objects not found during annotation.

DESCRIPTION

A number of objects in the SAIF file cannot be found in the current design; the switching activity information for this object is not annotated.

WHAT NEXT

Check the arguments of the (**read_saif** or **merge_saif**) command used to read the SAIF file. You can use the **-verbose** flag of the command to get warning messages for each unannotated object.

PWR-453 (warning) There are %d state/path dependent mismatches during annotation.

DESCRIPTION

A number of objects in the SAIF file have state/path dependent information that does not match with the state/path dependent information in the technology library characterization. This can occur when the backward SAIF file was generated using a forward library/gate-level SAIF file for a different library than the one used for linking the current design. It is also possible that the netlist used during simulation is different from the current design.

WHAT NEXT

Check that the designs and technology library used during simulation match the current design and link library.

PWR-454 (information) Inferring related clocks.

DESCRIPTION

This message specifies that Power Compiler will infer the related clocks on design object that need related clock inference. These objects have a **related_clock** attribute with value **"*"**. Power Compiler will infer a valid related clock on these objects and sets the **related_clock** attribute to the name of the inferred related clock.

WHAT NEXT

This is an information message. You can use the **report_attribute** and **check_attribute** commands to check that the **related_clock** attribute on the objects needing related clock inference has changed to a valid clock name.

PWR-455 (warning) Cannot infer related clocks: Unable to check out a Power Compiler license.

DESCRIPTION

Power Compiler is trying to infer related clocks, but a Power Compiler license is not available for check-out and the related clock inference process is aborted. The mechanism to infer related clock is requested when a command needs power switching activity information and the design has objects (ports, nets or pins) with the **related_clock** attribute set to the value **"*"**.

WHAT NEXT

Make sure that a Power Compiler license is available. In general, only Power Compiler commands need power switching activity information. If you get this warning message from a non-Power Compiler command, note that you can disable the related clock inference mechanism by removing the **related_clock** attributes from the design ports, nets and pins using the **remove_attribute** command.

PWR-456 (information) The clock '%s' is inferred as a related clock for the %s '%s'.

DESCRIPTION

Power Compiler has inferred a related clock on the specified object. The name of the inferred related clock is given in the information message. This message is displayed if the variable **power_sa_propagation_verbose** is set to **true**, or if the related clocks are inferred during a call to a verbose execution of the **propagate_switching_activity** command.

WHAT NEXT

This is an information message, no user action is required.

PWR-457 (information) The %s '%s' does not have an inferred

related clock.

DESCRIPTION

The user requested an inferred related clock on the specified object and Power Compiler inferred that the object does not have a related clock. This can happen for a number of cases, depending on the switches used to control the mechanism used to infer related clocks (the variables **power_rclock_inputs_use_clocks_fanout**, **power_rclock_use_asynch_inputs**, **power_rclock_unrelated_use_fastest**). For instance, if the user requests that the inferred related clock on input nets does not depend on the inferred related clocks in the nets trasitive fanout (the variable ffBpower_rclock_inputs_use_clocks_fanout) then non-clock input nets will not have an inferred related clock.

This information message is only issued when the mechanism to infer related clocks is used with the verbose option, for example, when the **power_sa_propagation_verbose** variable is set to **true**, or when the issues the **propagate_switching_activity** command with the **-verbose** flag.

When the mechanism inferring related clocks determines that an object with the / fBrelated_clock/fP attribute set to **"*"** does not have a related clock, then the / fBrelated_clock/fP attribute is removed.

WHAT NEXT

This is an information message, no user action is required.

SEE ALSO

propagate_switching_activity (2), **power_rclock_inputs_use_clocks_fanout** (3), **power_rclock_use_asynch_inputs** (3), **power_rclock_unrelated_use_fastest** (3). **power_sa_propagation_verbose** (3).

PWR-458 (information) Writing %s SAIF information to file '%s'.

DESCRIPTION

Power Compiler is generating a Switching Activity Interchange Format (SAIF) file. The following commands can generate SAIF files: **rtl2saif**, **lib2saif**, **merge_saif**, **write_saif**.

WHAT NEXT

This is an information message.

PWR-459 (error) The regs_on_clocks select type of the -select option of the set_switching_activity command has to be followed by a list of valid clock names.

DESCRIPTION

The **regs_on_clocks** select type of the **-select** option of the **set_switching_activity** command is used to select design registers that are clocked by a given list of clocks. The list of clocks is given as an argument of the **fBregs_on_clocks** inside the select list of the **-select** option. The following are examples of valid uses of the **regs_on_clocks** select type:

```
dc_shell-xg-t> set_switching_activity -select {regs_on_clock clk} ...
```

applies the **set_switching_activity** command on the outputs of the registers clocked by the clock clk.

```
dc_shell-xg-t> set_switching_activity -select {regs_on_clock {clk1 clk2} inputs} ...
```

applies the **set_switching_activity** command on the outputs of the registers clocked by the clock clk1 or clk2, and all the design inputs.

Note that the select type **regs** can be used to select all the register outputs.

WHAT NEXT

Specify a list of clock names after the **regs_on_clock** select type.

PWR-460 (error) Not all objects are of the same type.

DESCRIPTION

The objects specified for the **report_power_calculation** command must all be of the same type. Only pins, cells or nets are allowed, and you cannot mix objects of multiple types.

WHAT NEXT

Issue the **report_power_calculation** command multiple times, each time with objects of one specific time.

SEE ALSO

report_power_calculation (2).

PWR-461 (error) Options -rise and -fall are specified together.

DESCRIPTION

The **-rise** and **-fall** options cannot be used together for the **report_power_calculation** command.

WHAT NEXT

Use either **-rise** or **-fall**, or omit the edge specification altogether.

SEE ALSO

report_power_calculation (2).

PWR-462 (error) The -verbose option can only be used with objects of type cell or pin.

DESCRIPTION

This error occurs when the **report_power_calculation** command is used with the **-verbose** option for objects of type net. The **-verbose** option can only be used with objects of type cell or pin.

WHAT NEXT

Do not specify the **-verbose** option when applying **report_power_calculation** to nets.

SEE ALSO

report_power_calculation (2).

PWR-463 (error) Object '%s' is not a pin; options -rise or -fall cannot be specified.

DESCRIPTION

The **-rise** and **-fall** options cannot be used for objects of type cell or net. The **report_power_calculation** command only allows an edge specification for objects of type pin.

WHAT NEXT

Omit the edge specification for objects of type cell or net. Or, if you want to report the internal power calculation, specify a pin instead of a cell or net.

SEE ALSO

report_power_calculation (2).

PWR-464 (error) Cell '%s' is not a leaf cell.

DESCRIPTION

The **report_power_calculation** command can only be issued for objects that are associated with leaf cells. This excludes reporting for hierarchical cells or pins of such cells.

WHAT NEXT

Issue the **report_power_calculation** command for a leaf cell or a pin that belongs to a leaf cell.

SEE ALSO

report_power_calculation (2).

PWR-465 (error) Object '%s' is not a pin; a path condition cannot be specified.

DESCRIPTION

The **-path_source** option of the **report_power_calculation** command can only be used to narrow down the report of internal power calculation specific to a single pin. Therefore, this option can only be specified with objects of type pin.

WHAT NEXT

Omit the path source. Or, if you want to report the internal power calculation, specify a pin instead of a cell or net.

SEE ALSO

report_power_calculation (2).

PWR-466 (error) Object '%s' is not a pin or cell; a state condition cannot be specified.

DESCRIPTION

The **-state_condition** option of the **report_power_calculation** command can only be used to narrow down the report of state dependent power calculation. This applies to both internal power calculation (pin specific) and leakage power calculation (cell specific). Therefore, this option can only be used with objects of type cell or pin.

WHAT NEXT

Omit the state condition if you want to report the calculation of switching power. If you want to report internal or leakage power calculation, specify a pin or a cell instead of a net.

SEE ALSO

report_power_calculation (2).

PWR-467 (error) No internal power modeling available for library cell '%s'.

DESCRIPTION

The **report_power_calculation** command was applied to a pin that belongs to a leaf cell without internal power modeling. There is no internal power calculation for such a cell, and as a result the report cannot be generated.

WHAT NEXT

Use **report_power -cell -verbose -only to find out more details about the power calculation specific to this cell.**

SEE ALSO

report_power_calculation (2), **report_power** (2).

PWR-468 (error) Library cell '%s' does not have power

information for state condition "%s

DESCRIPTION

The **report_power_calculation** command was issued with the **-state_condition** option to narrow down the report. However, there is no power information available in the library characterization for the specified cell or pin.

WHAT NEXT

The possible state conditions are printed together with this error. Select one of the possible states. Alternatively, the option **-state_condition all** can be specified, in which case the power will be reported for all possible states.

SEE ALSO

report_power_calculation (2).

PWR-469 (error) Library cell ’%s’ does not have a pin named ’%s’.

DESCRIPTION

The **report_power_calculation** command was issued with the **-path_source** option to narrow down the report to a specific path source. However, the object for which the internal power calculation is to be reported belongs to a cell that does not have a pin by that name.

WHAT NEXT

The possible path sources are printed together with this error. Select one of the possible path sources. Alternatively, the option **-path_source all** can be specified, in which case the internal power will be reported for all possible path sources.

SEE ALSO

report_power_calculation (2).

PWR-470 (error) There are no matching internal power tables or

polynomials.

DESCRIPTION

The **report_power_calculation** command was issued with a state condition and/or a path source to narrow down the internal power calculation report. However, there are no matching internal power tables or polynomials that match these constraints.

WHAT NEXT

The possible state and path combinations are printed together with this error. Select one of the possible combinations, or relax the constraint by omitting the path source and/or the state condition. When the option **-verbose** is specified the internal power will be reported for all matching states and path sources.

SEE ALSO

report_power_calculation (2).

PWR-471 (error) There is more than one matching internal power table or polynomial.

DESCRIPTION

The **report_power_calculation** command was issued with state and path constraints that are too relaxed. There is more than one matching internal power table or polynomial. By default, the **report_power_calculation** command will only report the power calculation for a single matching state / path combination.

WHAT NEXT

Specify the **-verbose** option, which is equivalent to **-state_condition all -path_source all** to allow reporting of internal power calculation for all matching state / path combinations.

SEE ALSO

report_power_calculation (2).

PWR-472 (error) There are no matching leakage power values

or polynomials.

DESCRIPTION

The **report_power_calculation** command was issues with a state condition to narrow down the leakage power calculation report. However, there are no matching leakage power values or polynomials that match these constraints.

WHAT NEXT

The possible state conditions are printed together with this error. Select one of the possible states, or relax the constraint by omitting the state condition.

SEE ALSO

report_power_calculation (2).

PWR-473 (error) There is more than one matching leakage power value or polynomial.

DESCRIPTION

The **report_power_calculation** command was issued without a state condition. Because there are multiple matching leakage power values or polynomials, no report is generated. By default the **report_power_calculation** command will only report the power calculation for a single matching state.

WHAT NEXT

Use the **-state_condition all** option to report leakage power for all matching states. Alternatively, the **-verbose** option can be used, but this will result in the reporting of internal power calculation for all corresponding pins in addition to the leakage power calculation report.

SEE ALSO

report_power_calculation (2).

PWR-474 (error) Library cell power information is protected.

DESCRIPTION

This error is seen during **report_power_calculation** if the technology library associated with a cell leakage power table or pin internal power table has not been loaded with the read_lib command or if the technology library does not have the library feature report_power_calculation enabled.

WHAT NEXT

Load the ASCII version of the library with the read_lib command or modify the library source to add the library feature report_power_calculation.

PWR-475 (error) Design contains no clocks or clock sources

DESCRIPTION

identify_clock_gating could not find any clocks or clock sources in the design

WHAT NEXT

Run *create_clock <port_name>* for all clocks of the design and reissue identify_clock_gating command.

PWR-476 (error) Pin '%s' of library cell '%s' has average rise/fall internal power modeling; options -rise or -fall cannot be specified.

DESCRIPTION

This error occurs because the **report_power_calculation** command was applied to a pin for which the internal power is not characterized with separate rise and fall power modeling, but nevertheless a specific edge was specified with the **-rise** or **-fall** options.

WHAT NEXT

Omit the edge specification.

PWR-477 (information) Removing redundant clock gate '%s'.

DESCRIPTION

You receive this message when a redundant clock gate is removed during **compile -incremental** or **physopt -incremental**. A clock gate is considered redundant when it is always enabled. This is the case when the enable net is tied to logic one.

The automatic removal of redundant clock gates can be disabled by setting the variable **power_remove_redundant_clock_gates** to *false* (the variable is set to *true* by default).

WHAT NEXT

This is an informational message only; if you want to prevent the redundant clock gates to be removed, set the variable **power_remove_redundant_clock_gates** to *false*.

SEE ALSO

power_remove_redundant_clock_gates (3).

PWR-478 (error) The options -global and -no_hier are mutually exclusive for the insert_clock_gating command.

DESCRIPTION

When the **-no_hier** option is specified for the **insert_clock_gating** command, clock gating is restricted to the top level of the hierarchy. This conflicts with the **-global option, which enables hierarchical clock gating.**

WHAT NEXT

Leave out one of the two options when issuing the **insert_clock_gating command.**

PWR-479 (Error) Clock gate module naming style has multiple occurrences of '%%d' identifier.

DESCRIPTION

The clock gate module naming style specified using **power_cg_module_naming_style** has multiple occurences of '%d'. **power_cg_module_naming_style** can only contain utmost one occurrance of '%d'.

WHAT NEXT

Change **power_cg_module_naming_style** variable to contain only one or no occurrence of '%d' identifiers and re-invoke **insert_clock_gating** command.

PWR-480 (Error) Clock gate module naming style contains an unknown format identifier '%s'.

DESCRIPTION

The clock gate module naming style specified using **power_cg_module_naming_style** variable contains an unknown format identifier. The supported format identifiers are,

target_library names (when using discrete clock gating)

WHAT NEXT

Change **power_cg_module_naming_style** variable to contain only legal format identifiers and re-invoke **insert_clock_gating**.

PWR-481 (Error) Clock gate cell naming style has multiple occurrences of '%%d' identifier.

DESCRIPTION

The clock gate cell naming style specified using **power_cg_cell_naming_style** has multiple occurences of '%d'. **power_cg_cell_naming_style** can only contain utmost one occurrance of '%d'.

WHAT NEXT

Change **power_cg_cell_naming_style** variable to contain only one or no occurrence of '%d' identifiers and re-invoke **insert_clock_gating**.

PWR-482 (Error) Clock gate cell naming style contains an

unknown format identifier '%s'.

DESCRIPTION

The clock gate cell naming style specified using **power_cg_cell_naming_style** variable contains an unknown format identifier. The supported format identifiers are,

WHAT NEXT

Change **power_cg_cell_naming_style** variable to contain only legal format identifiers and re-invoke **insert_clock_gating**.

PWR-483 (Error) Gated clock net naming style has multiple occurrences of '%%d' identifier.

DESCRIPTION

The gated clock net naming style specified using **power_cg_gated_clock_net_naming_style** has multiple occurences of '%d'. **power_cg_module_naming_style** can only contain utmost one occurrance of '%d'.

WHAT NEXT

Change **power_cg_gated_clock_net_naming_style** variable to contain only one or no occurrence of '%d' identifiers and re-invoke **insert_clock_gating**.

PWR-484 (Error) Gated clock net naming style contains an unknown format identifier '%s'.

DESCRIPTION

The gated clock net naming style specified using **power_cg_gated_clock_net_naming_style** variable contains an unknown format identifier. The supported format identifiers are,

WHAT NEXT

Change **power_cg_gated_clock_net_naming_style** variable to contain only legal format identifiers and re-invoke **insert_clock_gating**.

PWR-485 (Error) The "integrated" argument of the set_clock_gating_style command contains an unknown integrated clock gating cell type %s.

DESCRIPTION

Invalid integrated clock gating cell type in the "integrated" argument for the set_clock_gating_style command. Valid integrated clock gating cell types are, 1. active_low_enable 2. invert_gclk

WHAT NEXT

Re-enter the set_clock_gating_style command.

PWR-486 (Error) Latch specification should be the first in the gate_list specified for %s.

DESCRIPTION

When you specify a gate_list for positive or negative edge logic, latch style (if any) should be the first in the list. Another option is to specify the latch style using **-sequential** option.

WHAT NEXT

Re-issue the set_clock_gating_style command with latch style moved to the first position in the gate list.

PWR-487 (information) Clock object is not specified, all clock nets of the design are considered.

DESCRIPTION

If no clock object is specified in **report_clock_tree_power** command, Power Compiler will perform **report_clock_tree_power** on all clock objects found in the design.

WHAT NEXT

reserved

PWR-488 (error) Power Compiler could not find any clock objects in the design, report_clock_tree_power command cannot be executed.

DESCRIPTION

reserved

WHAT NEXT

Please make sure that **create_clock** command is executed before **report_clock_tree_power** command.

PWR-489 (warning) clock net %s has no driver pin

DESCRIPTION

clock net does not have a driver pin (DC_DRIVER). **report_clock_tree_power** command cannot perform netlist traversal.

WHAT NEXT

Please double check the clock net that you specified, or check the netlist correctness.

PWR-490 (Warning) %d out of %d pins of the clock gating cell '%s' could not be identified.

DESCRIPTION

The functionality of one or more pins of a clock gate could not be identified. This will cause the clock gate to be not identified correctly.

If this error happens for an ICG cell, probably the ICG library has problems.

For dicrete clock gates, the identification uses a mixture of functionality, connectivity and names. Make sure the Power Compiler assigned circuitry and the port names are not changed.

If this is a manually inserted clock gate, try to use a configuration and port names similar to what Power Compiler uses.

WHAT NEXT

Check the ICG cell library for pin attributes or check the names of clock gate pins and reissue **identify_clock_gating** command.

PWR-491 (Warning) No clock period specified; characterization may be inaccurate.

DESCRIPTION

This warning is specific to activity based clock gating. This is currently a beta feature of Power Compiler.

WHAT NEXT

Contact your Power Compiler representative if you would like more information on this feature, or if you want to participate in the beta testing program.

PWR-492 (error) Option '%s' for command '%s' is only available in XG mode.

DESCRIPTION

The specified option for this command is only available in XG mode.

WHAT NEXT

Please use XG mode to run this command option.

PWR-493 (error) The specified clock period must be positive.

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-494 (error) The specified number of equivalent inverters cannot be negative.

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-495 (error) The '%s' command cannot be performed if no clock gating style has been set.

DESCRIPTION

You need to set the clock gating style using the command set_clock_gating_style before this particular command can be performed. The command is terminated.

WHAT NEXT

Specify the clock gating style.

PWR-496 (error) Command '%s' can only be executed when activity based clock gating is enabled.

DESCRIPTION

You need to enable activity based clock gating by specifying the -activity_based option with the set_clock_gating_style command. The command is terminated.

WHAT NEXT

Enable activity based clock gating.

PWR-497 (error) Can't find consistent 'power_gating_pin' attributes for pin '%s'

on retention registers in the technology library.

DESCRIPTION

set_power_gating_signal command has an option *-library_pin* to specify a common pin name which is one of the control pins of the retention registers in the library. If *-type* is also specified for the command, the common pin name is for the retention registers of a certain type, otherwise, it's for all the retention registers in the library. It's required that the same power_gating_pin attribute should be specfied on the control pins with same name for retention registers in the library. Power Compiler will stitch the control pins of retention registers in the design with **hookup_power_gating_ports** command based on the value of the related attribute. The error occurs when there are different values of power_gating_pin attributes on the pin with this name for the retention registers in the library.

WHAT NEXT

Check *-library_pin* option of the **set_power_gating_signal** command and the 'power_gating_pin' attribute of retention registers in the libraries and make sure they match.

PWR-498 (warning) Can't find pin '%s' on retention register '%s'.

DESCRIPTION

set_power_gating_signal command has an option *-library_pin* to specify a common pin name which is one of the control pins of the retention registers in the library. If *-type* is also specified for the command, the common pin name is for the retention registers of a certain type, otherwise, it's for all the retention registers in the library. The warning occurs when no pin with this name can be found for the retention register.

WHAT NEXT

Check the retention register in the library.

PWR-499 (warning) Can't find 'power_gating_pin' attribiute on pin '%s' of retention register '%s' in the library.

DESCRIPTION

set_power_gating_signal command has an option *-library_pin* to specify a common pin

name which is one of the control pins of the retention registers in the library. If *-type* is also specified for the command, the common pin name is for the retention registers of a certain type, otherwise, it's for all the retention registers in the library. It's required that the same power_gating_pin attribute should be specfied on the control pins with same name for the retention registers in the library. Power Compiler will stitch the control pins of retention registers in the design with **hookup_power_gating_ports** command based on the values of the attribute. The warning occurs when no such an attribute can be found for the pin of this retention register.

WHAT NEXT

Check the retention register in the library.

PWR-500 (warning) Clock gating with elaborate -gate_clock is obsolete; instead use the insert_clock_gating command.

DESCRIPTION

The **insert_clock_gating** command provides additional features compared to the **elaborate -gate_clock** command. In addition to the regular clock gating also performed by **elaborate -gate_clock**, the **insert_clock_gating** command attempts to find even more clock gating opportunities by combing different register banks that share common enable conditions. Furthermore, it can create multi-stage clock gating designs by factoring common enable conditions from the inserted clock gates. This can further reduce the power dissipation.

WHAT NEXT

Use the **insert_clock_gating** command to introduce clock gating in your design.

SEE ALSO

set_clock_gating_style (2), **insert_clock_gating** (2).

PWR-501 (warning) The low effort leakage power optimization algorithm cannot run in on_route mode.

DESCRIPTION

This warning occurs during **physoptP command, if set_max_leakage_power -effort low** has been set and the **-on_route** flag has been used in invoking **physopt**. The warning indicates that the leakage power optimization algorithm will not be run, although **physopt** will continue to run.

WHAT NEXT

This is a warning. Either use **physoptP with high effort leakage power optimization algorithm (the default), or use the command without the -on_route** flag.

PWR-502 (error) The toggle rate cannot be negative.

DESCRIPTION

A negative toggle rate was specified. The toggle rate should be zero (no activity) or positive (a certain activity).

WHAT NEXT

Reissue the command with a non-negative value for the toggle rate.

PWR-503 (warning) Clock gating could not be performed because of issues with the target library.

DESCRIPTION

Clock gating relies on the current target library. If the target library cannot be loaded, clock gating cannot be performed.

WHAT NEXT

Verify the *target_library* and the *search_path* variables and ensure that all libraries are existent and available from the search path.

PWR-504 (warning) There are no library cells with the specified power gating style '%s' and the operating condition. Regular flip flop(s) will be mapped instead.

DESCRIPTION

This error occurs when the library(s) does not have any power gating cell of the specified operating condition with the power gating style set by *set_power_gating_style* command. *compile* cannot map the cells to the library cell with expected power gating style, instead, it will map to the appropriate regular flip flops.

WHAT NEXT

Update the library(s) to include library cells with the specified power gating style and operating condition.

PWR-505 (error) Unknown power gating style '%s'.

DESCRIPTION

This error occurs when the user specify the power gating style with **set_power_gating_style** or **set_power_gating_signal** command but the style does not match the "power_gating_cell" attribute of any cells in the target libraries.

WHAT NEXT

Check -type option of the **set_power_gating_style** or **set_power_gating_signal** command and the 'power_gating_cell' attribute in the libraries and make sure they match.

PWR-506 (error) Can't find hdl block '%s'.

DESCRIPTION

This error occurs when hdl block name specified by -hdl_block option of **set_power_gating_style** command can not be found in the design.

WHAT NEXT

Check -hdl_block option of the **set_power_gating_style** command and make sure the hdl block name is correct.

PWR-507 (error) Can't find any hdl block matching name or name pattern '%s' in 'set_power_gating_style' command.

DESCRIPTION

This error occurs when the command can't find any hdl block matching the name or name pattern specified by the -hdl_block option of the **set_power_gating_style** command.

WHAT NEXT

Check -hdl_block option of the **set_power_gating_style** command and make sure the hdl block name is correct.

PWR-508 (error) The power gating style '%s' of cell '%s' conflicts with
the power gating style '%s' of the example library cell '%s' in the 'set_register_type' command.

DESCRIPTION

This error occurs when both *set_power_gating_style* and *set_register_type -exact* are used. If the power gating style of the example flip flop is different from the power gating style set by *set_power_gating_style* command, *compile* can not resolve the conflicts between them.

WHAT NEXT

Check the *set_power_gating_style* and *set_register_type* commands and correct the inconsistences.

PWR-509 (warning) The expected power gating style '%s' of cell '%s' conflicts
with the power gating style '%s' of library cell '%s' implementing this cell.

DESCRIPTION

This error occurs when the library cell implementing the cell has different power gating style from the one set by *set_power_gating_style* command. For this cell, *compile* does not map it to the library cell with expected power gating style successfully.

WHAT NEXT

Check the *set_power_gating_style* command and the warning and error messages during *compile* and correct the setting.

PWR-510 (error) *power_cg_equivalence_check_effort* variable has an unsupported value '%s'.

DESCRIPTION

Commands like *identify_clock_gates* try to detect which clock gates are equivalent in a design. Two clock gates are equivalent if they both have equivalent enable and clock signals. The effort used in this detection process can be controlled by the variable, *power_cg_equivalence_check_effort*.

This error occurs when the variable *power_cg_equivalence_check_effort* has an invalid value. Valid values for this variable are low, medium and high.

WHAT NEXT

Set *power_cg_equivalence_check_effort* variable to a valid value and rerun the command.

PWR-511 (error) '%s' is not a recognized characterization type.

DESCRIPTION

This warning is specific to activity based clock gating. This is currently a beta feature of Power Compiler.

WHAT NEXT

Contact your Power Compiler representative if you would like more information on this feature, or if you want to participate in the beta testing program.

PWR-512 (error) '%s' is not a recognized edge type.

DESCRIPTION

This warning is specific to activity based clock gating. This is currently a beta feature of Power Compiler.

WHAT NEXT

Contact your Power Compiler representative if you would like more information on this feature, or if you want to participate in the beta testing program.

PWR-513 (error) The set_clock_gating_characterization command expects exactly 8 parameter values.

DESCRIPTION

This warning is specific to activity based clock gating. This is currently a beta feature of Power Compiler.

WHAT NEXT

Contact your Power Compiler representative if you would like more information on this feature, or if you want to participate in the beta testing program.

PWR-514 (error) The characterization clock period must be explicitly specified with the set_clock_gating_characterization command.

DESCRIPTION

This warning is specific to activity based clock gating. This is currently a beta feature of Power Compiler.

WHAT NEXT

Contact your Power Compiler representative if you would like more information on this feature, or if you want to participate in the beta testing program.

PWR-515 (error) Object '%s' is not an operator or hierarchical instance.

DESCRIPTION

You receive this message if you issue the **set_operand_isolation_cell** command and specify as part of the *object_list* an object that is not an operator or (hierarchical) cell instance. You can specify only operator cells or cell instances for this command. This error could possibly be caused by a spelling error or typo.

WHAT NEXT

Check the items in the *object_list* and verify that all are operator cells or cell

instances and that the spelling is correct. Then reissue the **set_operand_isolation_cell** command with the correct *object_list*.

SEE ALSO

set_operand_isolation_cell (2).

PWR-516 (error) Object '%s' is of the wrong type.

DESCRIPTION

The specified object is a library cell or design. You can get this error when issuing the **set_operand_isolation_cell** or the **set_operand_isolation_scope** command. The former does not allow designs as arguments. The latter does, but the design must have a proper hierarchy; i.e. it cannot be a black box. In either case library cells are not allowed.

WHAT NEXT

Check the items in the *object_list* and verify that all objects are of the right type and that the spelling is correct. Then reissue the **set_operand_isolation_cell** or **set_operand_isolation_scope** command with the correct *object_list*.

SEE ALSO

set_operand_isolation_scope (2), **set_operand_isolation_cell** (2).

PWR-517 (warning) No operand isolation applied to hierarchical cell '%s' because it contains sequential arcs.

DESCRIPTION

This warning is issued when operand isolation was requested for a hierarchical cell, but the directive could not be honored. This is because the hierarchical cell instance contains sequential arcs, and operand isolation can only be applied to fully combinational hierarchical instances.

WHAT NEXT

Since this is only an informational warning, it can safely be ignored. It may be an indication that the user directive for operand isolation was meant for another object. In that case, set the directive correctly and rerun the script.

SEE ALSO

set_operand_isolation_style (2), **set_operand_isolation_cell** (2), **do_operand_isolation** (3).

PWR-518 (warning) No operand isolation applied to hierarchical cell '%s' because isolation of hierarchical cells is disabled.

DESCRIPTION

This warning is issued when operand isolation was requested for a hierarchical combinational cell, but the directive could not be honored. This is because operand isolation of hierarchical cell instances is disabled. Only operators can be isolated with the current settings.

WHAT NEXT

Since this is only an informational warning, it can safely be ignored. It may be an indication that the user directive for operand isolation was meant for another object. In that case, set the directive correctly and rerun the script.

SEE ALSO

set_operand_isolation_style (2), **set_operand_isolation_cell** (2), **do_operand_isolation** (3).

PWR-519 (warning) No operand isolation applied to cell '%s' because no opportunity for isolation was found.

DESCRIPTION

This warning is issued when operand isolation was requested for an operator or hierarchical combinational cell, but the directive could not be honored. This is because no state could be identified for which the output of the operator or hierarchical cell is unused.

WHAT NEXT

Since this is only an informational warning, it can safely be ignored. It may be an indication that the user directive for operand isolation was meant for another object. In that case, set the directive correctly and rerun the script.

SEE ALSO

set_operand_isolation_style (2), **set_operand_isolation_cell** (2), **do_operand_isolation** (3).

PWR-520 (warning) No operand isolation applied to cell '%s' because all inputs are driven by constant nets.

DESCRIPTION

This warning is issued when operand isolation was requested for an operator or hierarchical combinational cell, but the directive could not be honored. For optimal results, nets that are driven by a constant are never isolated. In this particular case, all inputs for the operator or hierarchical combinational cell are driven by constants, so none of the input nets are isolated.

WHAT NEXT

Since this is only an informational warning, it can safely be ignored. It may be an indication that the user directive for operand isolation was meant for another object. In that case, set the directive correctly and rerun the script.

SEE ALSO

set_operand_isolation_style (2), **set_operand_isolation_cell** (2), **do_operand_isolation** (3).

PWR-521 (warning) No operand isolation applied to cell '%s'.

DESCRIPTION

This warning is issued when operand isolation was requested for an operator or hierarchical combinational cell, but the directive could not be honored. The outputs of the operator or hierarchical combinational cell are never used. Since this object is redundant, it is not efficient to apply operand isolation to it. Instead, it should be removed altogether.

WHAT NEXT

Since this is only an informational warning, it can safely be ignored. It may be an indication that the user directive for operand isolation was meant for another object. In that case, set the directive correctly and rerun the script.

SEE ALSO

set_operand_isolation_style (2), **set_operand_isolation_cell** (2), **do_operand_isolation** (3).

PWR-522 (error) A non-empty collection of objects was specified together with one of the options '-isolated_objects', '-unisolated_objects' or '-all_objects'.

DESCRIPTION

When the **report_operand_isolation** command is used on a collection of specific objects, the report will be generated for those objects only. Reporting on all isolated, unisolated or simply all isolated objects is not allowed when a collection of objects is specified.

WHAT NEXT

Issue the **report_operand_isolation** command without the **-isolated_objects**, **-unisolated_objects** or **-all_objects**, or issue the command without a collection of specific objects.

SEE ALSO

report_operand_isolation (2).

PWR-523 (error) The '-verbose' option is used without either a collection of objects or one of the options '-isolated_objects' or '-all_objects'.

DESCRIPTION

The **report_operand_isolation** command can be issues with the **-verbose** option to get more detailed reporting for the isolated objects. To report isolated objects either the **-isolated_objects** or **-all_objects** options should be used, or a collection of specific objects should be specified.

This error is generated when the **report_operand_isolation** command is issued with the **-verbose** option, but reporting of isolated objects is not requested.

WHAT NEXT

If no reporting of isolated objects is requested, omit the **-verbose** option. If you are interested in details related to the isolated objects, specify the specific objects (operators or hierarchical combinational cells) or use the command with **-isolated_objects** or **-all_objects** in addition to **-verbose**.

SEE ALSO

report_operand_isolation (2).

PWR-524 (error) The options '-instances' and '-no_hier' are mutually exclusive for the report_operand_isolation command.

DESCRIPTION

The **report_operand_isolation** command with **-instances** option produces a breakdown per instance of the summary of isolated and unisolated operators and hierarchical cells. This is only meaningful when multiple instances are considered for reporting.

The **-no_hier** option limits reporting to just the top level. Since the number of instances is limited to one, the **-instances** option cannot be used in combination with the **-no_hier** option.

WHAT NEXT

Omit either the **-no_hier** or the **-instances** option.

SEE ALSO

report_operand_isolation (2).

PWR-525 (error) Object '%s' is neither an operator nor a hierarchical combinational cell.

DESCRIPTION

The **report_operand_isolation** command can be applied to a collection of specific objects. Each object should be either an operator or a hierarchical combinational cell. If an object does not meet these criteria (a leaf cell, black box or hierarchical cell that contains sequential arcs), this error is issued.

WHAT NEXT

Remove the objects that are not operators or hierarchical combinational cells from the collection and re-issue the **report_operand_isolation** command. Alternatively, the **-isolated_objects**, **-unisolated_objects** or **-all_objects** options can be used to apply the report to all (un-)isolated objects.

SEE ALSO

report_operand_isolation (2).

PWR-526 (error) Object '%s' is not within the current instance.

DESCRIPTION

The **report_operand_isolation** command can be applied to a collection of specific objects. If the current_instance is set to anything else than the top level of the design, the objects in the collection should all be within the scope of the current instance. Otherwise this error is generated.

WHAT NEXT

Remove the objects that are not within the scope of the current instance and re-issue the **report_operand_isolation** command. Alternatively, the **-isolated_objects**, **-unisolated_objects** or **-all_objects** options can be used to apply the report to all (un-)isolated objects within the current instance.

SEE ALSO

report_operand_isolation (2).

PWR-527 (error) Specified libcell '%s/%s' is marked pwr_dont_use.

DESCRIPTION

The specified for ICG library cell has pwr_dont_use attribute. Power Compiler can not use this lib cell for ICGC mapping.

WHAT NEXT

Remove the **set_dont_use -power** command (if any) from the script. Specify a different ICG libcell or remove the **pwr_cg_dont_use** attribute on the libcell.

PWR-528 (warning) Specified lib_cell '%s' is marked power_dont_use.

DESCRIPTION

One or more of the libraries does have the specified library cell, but it is marked *power_dont_use*.

WHAT NEXT

Specify a different ICG library cell or remove the *power_cg_dont_use* attribute on the libcell.

PWR-530 (error) There is no clock with name '%s' in the current design.

DESCRIPTION

The argument specified to the **regs_on_clocks** select type has to be the name of an existing clock. There is no clock in the current design with the specified clock name.

WHAT NEXT

Specify a valid clock name as argument to the **regs_on_clocks** select type; or apply the **set_switching_activity** command after creating the specified clock.

PWR-531 (warning) The value '%s' of the variable 'power_default_toggle_rate_type' is invalid. The default value of '%s' is used instead.

DESCRIPTION

The value of the variable **power_default_toggle_rate_type** can be either **"fastest_clock"** or **"absolute"**. This variable determines how the **default_toggle_rate** variable is used in determining the default toggle rates on unannotated primary input ports and black-box output pins. More information on these variables is available on the man page of **power_default_toggle_rate_type**.

WHAT NEXT

Set the value of the variable **power_default_toggle_rate_type** to **"fastest_clock"** or **"absolute"**.

SEE ALSO

power_default_toggle_rate_type (3), **power_default_toggle_rate** (3), **power_default_static_probability** (3).

PWR-532 (warning) The library cell '%s' contains an internal power table with the obsolete attribute '%s'.

DESCRIPTION

The internal power characterization of the specified cell contains an attribute that is obsolete or not supported. The power table with this attribute is ignored and will not be used for power calculations.

WHAT NEXT

Use a library with up-to-date power characterization.

PWR-533 (warning) The library cell '%s' contains an internal power table with an invalid or inconsistent value for the attribute '%s'.

DESCRIPTION

The internal power characterization of the specified cell is invalid and contains an unexpected value for the given attribute. The attribute value may be invalid, or it conflicts with the attribute values of the other power tables.

The invalid power table will not be used in power calculations.

WHAT NEXT

Use a library with valid internal power characterization. This warning message usually occurs when an obsolete or invalid library is compiled with an old version of Library Compiler that did not check for certain characterization errors. Check and fix the internal power characterization of the specified cell and recompile the library, preferably with a Library Compiler version having the same version number as that of the Power Compiler version being used.

PWR-534 (warning) The library cell '%s' contains invalid or inconsistent internal power characterization.

DESCRIPTION

The internal power characterization of the specified cell is invalid and not all internal power tables can be used for power calculation.

WHAT NEXT

Use a library with valid internal power characterization. This warning message usually occurs when an obsolete or invalid library is compiled with an old version of Library Compiler that did not check for certain characterization errors. Check and fix the internal power characterization of the specified cell and recompile the library, preferably with a Library Compiler version having the same version number as that of the Power Compiler version being used.

PWR-535 (information) Removing power SDPD switching activity information for multi-mode flow.

DESCRIPTION

User annotated state-dependent and/or path-dependet (SDPD) switching activity information is being removed because of multi-mode. Currently, user annotated SDPD switching activity cannot be used during multi-mode power optimization. Non-SDPD user annotated switching activity is used, and is user can annotate different non-SDPD information for each layer. SDPD switching activity is estimated on the fly from non-SDPD information for each layer during power calculations.

WHAT NEXT

This is an information message.

PWR-536 (information) The library cell '%s' in the library '%s' is not characterized for internal power.

DESCRIPTION

The given library cell is not characterized for internal power. The dynamic power of a cell consists of the internal power. An internal power of 0 is assumed for this cell; Since this internal power value may not be accurate, power optimizations may not use this cell effectively and power analysis of designs containing instances of

this cell may not be accuarte.

WHAT NEXT

This is an information message. Please contact your library vendor if you believe that this library cell needs internal power characterization.

PWR-537 (warning) The library cell '%s' contains multiple leakage power tables for the same condition.

DESCRIPTION

The given library cell contains more than one leakage power table for the same condition ("when" condition, or a combination of "when" and "power_level" conditions). In such cases, only one power table for each condition is used during power calculations.

An example when this warning message occurs is if the library cell characterization contains more than one leakage power table with a when condition logically equivalent to "0". Note that such tables do not contribute to the leakage power of instances of the library cell, so they are usually not included intentionally in the cell characterization; therefore this warning message may suggest that there is an error in the cell characterization. Another example is that the cell contains leakage power characterization with invalid state conditions that are all assumed to be default condition.

WHAT NEXT

Power calculations will proceed but will only use one of the multiple tables for the same condition. Check that the leakage power characterization of the particalular library cell is valid.

PWR-538 (information) %d path sources specified in '%s'. The specified toggle rate will be shared between each path source.

DESCRIPTION

Multiple path sources are specified with the same **set_switching_activity** command calls. The toggle rate given in the command will be shared equally between each path source.

WHAT NEXT

This is an information message. You can specify different path dependent toggle

rates for each path source using separate calls to the **set_switching_activity** command.

PWR-539 (information) The state condition '%s' matches %d power tables. The specified toggle rate is shared between all matches.

DESCRIPTION

The specified state condition matches more than one table, and the toggle rate given in the **set_switching_activity** will be shared equally between each match. You can use the **report_power** command with the **-cell -verbose -only** *cell* arguments to see all the state and path dependent conditions for the specified cell.

WHAT NEXT

This is an information message. You can specify different state/path dependent toggle rates for each state and path condition using separate calls to the **set_switching_activity** command using both the **-state_dep** and **-path_dep** arguments.

PWR-540 (information) No operand isolation was performed because no opportunity for isolation was encountered.

DESCRIPTION

This warning is issued when operand isolation was enabled during mapping, but no operand isolation was performed. This could be because there are no operators or hierarchical combinational cells that are used conditionally.

When there are such operators or hierarchical combinational cells, the isolation of these cells is only performed when a user directive has been specified for this object (user-driven mode) or when the switching activity indicates that it is favorable for dynamic power optimization to apply operand isolation.

WHAT NEXT

Since this is only an informational warning, it can safely be ignored. For user-driven operand isolation, specify user directives with the **set_operand_isolation_cell** command. For automatic isolation, make sure switching activity has been annotated before mapping to ensure best results.

SEE ALSO

set_operand_isolation_style (2), **set_operand_isolation_cell** (2), **do_operand_isolation** (3).

PWR-541 (warning) No operand isolation applied to operator '%s' because it contains sequential arcs.

DESCRIPTION

This warning is issued when operand isolation was requested for an operator, but the directive could not be honored. This is because the operator contains sequential arcs, and operand isolation can only be applied to fully combinational operators.

WHAT NEXT

Since this is only an informational warning, it can safely be ignored. It may be an indication that the user directive for operand isolation was meant for another object. In that case, set the directive correctly and rerun the script.

SEE ALSO

set_operand_isolation_style (2), **set_operand_isolation_cell** (2), **do_operand_isolation** (3).

PWR-542 (warning) The command '%s' is obsolete; use '%s' instead.

DESCRIPTION

To enable further enhancements it is sometimes required to abandon certain flows in favor of new, more advanced flows.

This command will be obsoleted soon. To ensure proper operation, change your script to use the suggested alternative command instead.

WHAT NEXT

Use the suggested alternative command instead.

PWR-543 (Error) Unscanning a scan replaced register failed.

Clock gating removal abandoned.

DESCRIPTION

Clock gating removal involves unscanning and rescanning the register if it is scan replaced. If the unscan step fails, clock gating removal will not be performed.

WHAT NEXT

Look for the reasons why unscan failed and fix the problem. Then re-issue **compile -incr**.

PWR-544 (error) Object '%s' is not a design or hierarchical instance.

DESCRIPTION

You receive this message if you issue the **set_operand_isolation_scope** command and specify as part of the *object_list* an object that is not a design or hierarchical instance. You can specify only designs or hierarchical instances for this command. This error could possibly be caused by a spelling error or typo.

WHAT NEXT

Check the items in the *object_list* and verify that all are designs or cell instances and that the spelling is correct. Then reissue the **set_operand_isolation_scope** command with the correct *object_list*.

SEE ALSO

set_operand_isolation_scope (2).

PWR-545 (Information) Added %d gates during splitting

DESCRIPTION

WHAT NEXT

PWR-546 (error) At least one of the options -from or -to must be

specified.

DESCRIPTION

The **remove_operand_isolation** command requires a set of path specified as a collection of start points (specified with the **-from** option) and/or a collection of end points (specified with the **-to** option).

WHAT NEXT

Issue the **remove_operand_isolation** command with the **-from** or **-to** options.

PWR-547 (Warning) For best performance, use the default minimum bitwidth of 1 when activity based clock gating is enabled.

DESCRIPTION

This warning is specific to activity based clock gating. This is currently a beta feature of Power Compiler.

WHAT NEXT

Contact your Power Compiler representative if you would like more information on this feature, or if you want to participate in the beta testing program.

PWR-548 (warning) Pin %s of cell %s is bidirectional; no clock gate replacement is performed on this branch.

DESCRIPTION

Clock gate replacement can only be performed on unidirectional clock trees. If a net on the clock tree is bidirectional. i.e. if there is a pin present on the clock tree that can act as both input and output, no replacement can be performed.

WHAT NEXT

There should be no need for bidirectional pins in the clock tree. Determine the proper pin direction, and define the clock ports as either module inputs or outputs.

PWR-549 (warning) Clock loop detected.

DESCRIPTION

identify_clock_gating detected a clock loop. *identify_clock_gating* will break the loop while doing clock tracing. Potentially some clock gates may be left unidentified because of this.

WHAT NEXT

Check if the design is linked properly with *link* command. Unlinked or wrong cells in the clock path may be interpreted as buffers by *identify_clock_gating*. Check if the design has any clock loops. Fix the problem and rerun *identify_clock_gating*.

PWR-550 (Information) No clock gate found for %s clock.

DESCRIPTION

Since clock has no gates, there is nothing to work on.

WHAT NEXT

No action is necessary.

PWR-551 (error) Physical design is not created for design '%s'.

DESCRIPTION

The phyiscal design is not created for the design. Power map features requires the physical design to be created.

WHAT NEXT

Check the script to see whether physical design is created when using the power map features.

PWR-552 (Information) Merging clock gates before splitting...

DESCRIPTION

Performing merge of clock gates before splitting.

WHAT NEXT

No action is necessary.

PWR-553 (Information) Performing clock gate analysis for %s clock...

DESCRIPTION

The tool performs clock gate analysis and splitting if necessary.

WHAT NEXT

No action is necessary.

PWR-554 (Information) Estimated clock latency is %f ns.

DESCRIPTION

Estimation mode came up with reported clock latency.

WHAT NEXT

No action is necessary.

PWR-555 (Information) Estimating delay for %s clock...

DESCRIPTION

Tool estimates clock latency to perform splitting.

WHAT NEXT

No action is necessary.

PWR-556 (Information) Fixing enable %s net...

DESCRIPTION

Tool fixes DRC in the enable net.

WHAT NEXT

No action is necessary.

PWR-560 (warning) The path source '%s' is not valid for the pin '%s'; the toggle rate portion for this path source is not annotated.

DESCRIPTION

This warning message occurs when multiple path sources have been specified and some or all of the path sources are not valid for the given cell. When multiple path sources are specified, the path dependent toggle rate given with the **set_switching_activity** command will be shared equally with all path sources. The toggle rate associated with an invalid path source will not be annotated, and therefore will not be used in power calculations. When specifying path dependent toggle rates the path source should match one of the internal power path sources given in the library cell characterization. To see the valid path sources and state conditions for this pin you can use the **report_power** command with the **-cell -verbose -only** *cell* arguments, where the specified *cell* contains the pin being annotated.

WHAT NEXT

To annotate switching activity on all specified path sources reissue the **set_switching_activity** command with a valid path source or sources.

PWR-561 (error) The path source%s '%s' %s not valid for the pin %s.

DESCRIPTION

The specified path source or sources are not valid and the toggle rate information

is not annotated. When specifying path dependent toggle rates the path source should match one of the internal power path sources given in the library cell characterization. To see the valid path sources and state conditions for this pin you can use the **report_power** command with the **-cell -verbose -only** *cell* arguments, where the specified *cell* contains the pin being annotated.

WHAT NEXT

Reissue the **set_switching_activity** command with a valid path source.

PWR-562 (error) The state '%s' is not valid for state dependent static probability specifications for the cell '%s'.

DESCRIPTION

The specified state condition is not valid and the static probability information is not annotated. When specifying state dependent static probabilities the state condition should match one of the leakage power state conditions given in the library cell characterization. To see the valid state conditions for this cell you can use the **report_power** command with the **-cell -verbose -only** *cell* arguments.

WHAT NEXT

Reissue the **set_switching_activity** command with a valid state condition.

PWR-563 (error) The state '%s' is not valid for state dependent toggle rate specifications for the pin '%s'.

DESCRIPTION

The specified state condition is not valid and the toggle rate information is not annotated. When specifying state dependent toggle rates the state condition should match one of the internal power state conditions given in the library cell characterization. To see the valid path sources and state conditions for this pin you can use the **report_power** command with the **-cell -verbose -only** *cell* arguments, where the specified *cell* contains the pin being annotated.

WHAT NEXT

Reissue the **set_switching_activity** command with a valid state condition.

PWR-564 (error) The state '%s' and path source%s '%s' are not valid for state dependent and path dependent toggle rate specifications for the pin '%s'.

DESCRIPTION

The specified state condition and path source(s) are not valid and the toggle rate information is not annotated. When specifying state dependent and path dependent toggle rates, the state condition and path sources should match one of the internal power state condition and path source combination given in the library cell characterization. To see the valid path sources and state conditions for this pin you can use the **report_power** command with the **-cell -verbose -only** *cell* arguments, where the specified *cell* contains the pin being annotated.

WHAT NEXT

Reissue the **set_switching_activity** command with a valid state condition and path source.

PWR-565 (error) The "-rise_ratio" argument cannot be specified without "-state_dep" or "-path_dep".

DESCRIPTION

Different rise/fall values can be used for state and path dependent (SDPD) toggle rates on cell pins, however non-SDPD toggle rates on nets, ports and pins are shared equally between rise and fall transitions, so a rise ratio of 0.5 is the only meaningful value. The **-rise_ratio** argument of the **set_switching_activity** command can be used to specify different rise/fall SDPD toggle rates and therefore can only be used with the **-state_dep** and **-path_dep** arguments which specify the state and path dependent conditions respectively.

WHAT NEXT

The **-rise_ratio** argument cannot be specified when setting non-SDPD toggle rates. To specify SDPD toggle rates use the **-state_dep** and/or **-path_dep** arguments.

PWR-566 (information) The path source '%s' matches %d power tables. The specified toggle rate is shared between all

matches.

DESCRIPTION

The specified path source matches more than one table, and the toggle rate given in the **set_switching_activity** will be shared equally between each match. You can use the **report_power** command with the **-cell -verbose -only** *cell* arguments to see all the state and path dependent conditions for the specified cell.

WHAT NEXT

This is an information message. You can specify different state/path dependent toggle rates for each state and path condition using separate calls to the **set_switching_activity** command using both the **-state_dep** and **-path_dep** arguments.

PWR-567 (warning) Ignoring invalid user-annotated SD static probability on cell '%s'.

DESCRIPTION

State-dependent static probability annotation on the specified cell is invalid and will not be used for power calculations. A likely reason for this problem is that the current link library and the link library used when the SD static probability was annotated have different states in their leakage power characterization for the specified cell.

WHAT NEXT

Check that the SD static probability values annotated on the given cell (with set_switching_activity or read_saif) are valid; also check that the link library used when annotating the SD static probabilities is the same as the current one or that it has the same states in the leakage power characterization.

PWR-568 (warning) Ignoring invalid user-annotated SDPD toggle rate on pin '%s'.

DESCRIPTION

State-dependent and/or path-dependent toggle rate annotation on the specified pin is invalid and will not be used for power calculations. A likely reason for this problem is that the current link library and the link library used when the SDPD toggle rate was annotated have different state/path conditions in their internal power characterization for the specified pin.

WHAT NEXT

Check that the SDPD toggle rate values annotated on the given pin (with set_switching_activity or read_saif) are valid; also check that the link library used when annotating the SDPD toggle rates is the same as the current one, or that it has the same state/path conditions in the internal power characterization.

PWR-569 (warning) Ignoring invalid user-annotated SDPD switching activity on cell '%s'.

DESCRIPTION

State-dependent and/or path-dependent toggle rate annotation and/or state-dependent static probabilities on the specified cell or its pins are invalid and will not be used for power calculations. A likely reason for this problem is that the current link library and the link library used when the SDPD switching activity was annotated have different state/path conditions in their internal power characterization and/or different state conditions in their leakage power characterization.

WHAT NEXT

Check that the SDPD switching activity values annotated on the given cell (with set_switching_activity or read_saif) are valid; also check that the link library used when annotating the SDPD switching activity is the same as the current one, or that it has the same SDPD conditions in the internal and leakage power characterization.

PWR-570 (warning) Cell %s is not a buffer or inverter and hence cannot be ungated; clock gate %s will not be removed.

DESCRIPTION

Clock gates which are driving combinational cells other than buffers or inverters cannot be ungated. Such combinational cells are considered manual inserted clock gating cells that are not recognized as Power Compiler clock gates.

WHAT NEXT

Replace the manual inserted clock gate with a Power Compiler clock gate by issuing the **replace_clock_gates** command.

PWR-571 (error) Cell %s is not a buffer or inverter and hence cannot be ungated; clock gate %s will not be removed.

DESCRIPTION

Clock gates which are driving combinational cells other than buffers or inverters cannot be ungated. Such combinational cells are considered manual inserted clock gating cells that are not recognized as Power Compiler clock gates.

WHAT NEXT

Replace the manual inserted clock gate with a Power Compiler clock gate by issuing the **replace_clock_gates** command.

PWR-572 (warning) Option -module_level is obsolete. Use the replace_clock_gates command instead.

DESCRIPTION

It is not recommended to perform replacement of manual inserted clock gates simultaneously with clock gate insertion. To replace existing clock gates with Power Compiler clock gates, use the **replace_clock_gates** command instead.

WHAT NEXT

Replace the manual inserted clock gate with a Power Compiler clock gate by issuing the **replace_clock_gates** command.

SEE ALSO

insert_clock_gating (2), **replace_clock_gates** (2).

PWR-573 (warning) Use of option -no_register_based is deprecated.

DESCRIPTION

It is not recommended to perform replacement of manual inserted clock gates simultaneously with clock gate insertion. To replace existing clock gates with Power Compiler clock gates, use the **replace_clock_gates** command instead. With the availability of this command there is no need for the **-no_register_based** option for

the **insert_clock_gating** command.

WHAT NEXT

Do not use the **-no_register_based** option with the **insert_clock_gating** command. If you do not want register-based clock gating, do not issue the **insert_clock_gating** command altogether.

SEE ALSO

insert_clock_gating (2), **replace_clock_gates** (2).

PWR-574 (information) For a multi-voltage design, library %s specified in the **set_clock_gating_style** command will be ignored. The library cell matching the correct operating condition will be used.

DESCRIPTION

The user specifies the clock gating cell of a specific library in **set_clock_gating_style** command. In a multi-voltage design, this library will be ignored by the linker inside **compile**. Instead, it will select the clock gating cell with the appropriate operating condition.

WHAT NEXT

In a multi-voltage design, the user do not need to specify the library name of the clock gating cell in the **set_clock_gating_style** command.

PWR-575 (warning) The library %s specified in the **set_clock_gating_style** will be ignored during clock gate mapping since the design is a multi-voltage design.

DESCRIPTION

The user specifies the clock gating cell of a specific library in **set_clock_gating_style** command. In a multi-voltage design, this library will be ignored by the linker inside **compile**. Instead, it will select the clock gating cell with the appropriate operating condition.

WHAT NEXT

In a multi-voltage design, the user do not need to specify the library name of the clock gating cell in the **set_clock_gating_style** command.

PWR-580 (Error) Could not make connection to pin '%s' because cell '%s' is marked dont_touch.

DESCRIPTION

hookup_testports had to create pins at intermediate levels of hierarchy to hooking up the specified pin to the *hookup_pin* specified. But one of the cells in the hierarchy was marked *dont_touch* and hence the connection could not be made.

WHAT NEXT

Remove the *dont_touch* on the specified cell and rerun hookup_testports if that is possible. **hookup_testports** has completed the rest of the connections. The user can choose to fix the failed connection with netlist editing commands also.

PWR-581 (warning) Clock-gating cell %s is a target cell for the rewire_clock_gating command.

DESCRIPTION

The **remove_clock_gating -all** command cannot mark clock gating cells for removal that are a target clock-gating cell for the **rewire_clock_gating** command.

WHAT NEXT

If a cell is a target clock-gating cell for the **rewire_clock_gating** command, it cannot be marked for removal. If you want to use the **compile** command with the **-incremental** option (or **physopt** and **physopt -incremental**) to remove the cell, use the **-undo** option of the **rewire_clock_gating** command with the **-gated_registers** option. Include as the argument to the **-gated_objects** option all the cells and pins that are marked to be moved to the new clock-gating cell. Then reissue the **remove_clock_gating** command.

SEE ALSO

compile (2), **remove_clock_gating** (2), **rewire_clock_gating** (2).

PWR-582 (error) The cell %s is marked dont_touch and cannot be removed.

DESCRIPTION

You receive this error message because you specified a clock-gating cell that is marked dont_touch as an argument of the **-gating_cell** option of the **remove_clock_gating** command. Cells that are marked dont_touch cannot be removed.

WHAT NEXT

Make sure the specified cell is not marked dont_touch. If the clock gating cell is marked dont_touch, use the **set_dont_touch command to explicitly set the dont_touch attribute to *false*** or the **remove_attribute** command to remove the dont_touch attribute.

SEE ALSO

remove_clock_gating (2), **report_clock_gating** (2), **set_dont_touch** (2), **remove_attribute** (2).

PWR-583 (warning) The cell %s is marked dont_touch and cannot be removed.

DESCRIPTION

You receive this error message because you issued the **remove_clock_gating** command with the **-all** option on a design that has a clock-gating cell that is marked dont_touch. Such cannot be removed.

WHAT NEXT

Make sure the specified cell is not marked dont_touch. If the clock gating cell is marked dont_touch, use the **set_dont_touch command to explicitly set the dont_touch attribute to *false*** or the **remove_attribute** command to remove the dont_touch attribute.

SEE ALSO

remove_clock_gating (2), **report_clock_gating** (2), **set_dont_touch** (2), **remove_attribute** (2).

PWR-584 (warning) Clock gate %s is marked for rewiring and cannot be removed.

DESCRIPTION

The **remove_clock_gating -all** command cannot mark clock gating cells for removal that are marked for rewiring by the **rewire_clock_gating** command.

WHAT NEXT

A clock gating cell that is marked for rewiring cannot be removed. If you want to use the **compile** command with the **-incremental** option (or **physopt** and **physopt -incremental**) to remove the cell, use the **-undo** option of the **rewire_clock_gating** command. Use the cell you specified as an argument for the **-gated_objects** option. Then reissue the **remove_clock_gating** command.

SEE ALSO

compile (2), **remove_clock_gating** (2), **rewire_clock_gating** (2).

PWR-585 (error) Either the option -all or one of the options -min_bitwidth, -gated_registers or -gating_cells must be used with the remove_clock_gating command.

DESCRIPTION

The **remove_clock_gating** command requires that you use either **-all** or one or a combination of the options **-min_bitwidth**, **-gated_registers**, or **-gating_cells**.

WHAT NEXT

To remove all the clock-gating cells in the current level of hierarchy, use the **-all option**. To remove only register that belong to banks smaller than a certain minimum size, use the **-min_bitwidth** option. Along with the **-all** and **-min_bitwidth** options, you can also use the **-no_hier** option to limit removal of clock-gating cells to the current level. To remove selected individual clock gating cells or registers in lower levels of the design hierarchy, give their complete path names from the current level of hierarchy as arguments to the **-gated_registers** option or the **-gating_cells** option of the **remove_clock_gating** command.

SEE ALSO

remove_clock_gating (2).

PWR-590 (Information) Datapath cell '%s' is gated with %s gating style.

DESCRIPTION

Power Compiler found that, datapath gating for the cell reduces dynamic power consumption and hence successfully gated the cell with the displayed style.

WHAT NEXT

No action is necessary.

PWR-591 (warning) Datapath cell '%s' is not considered for gating.

DESCRIPTION

This warning message occurs when the datapath gating engine encounters a DesignWare module cell with no dedicated pin to hook up the gating control signal. If datapath gating is supported for any DesignWare module, the low power DesignWare library (dw_lp_foundation.sldb) will have another similar module with an extra pin to which the gating control signal can be connected. When datapath gating is enabled, this gating-compatible DesignWare module is used for an operator instead of a normal module.

All of the most commonly used DesignWare modules have their gating-compatible modules. This warning is issued for those module cells that do not have their gating-compatible module.

WHAT NEXT

This is only a warning message. No action is required.

However, you can check if dw_lp_foundation.sldb is included in the synthetic_library list. If it is already included, it is likely that the gating-compatible module is not supported for the reported datapath cell. This warning can then be safely ignored.

SEE ALSO

set_datapath_gating_options(2)
power_enable_datapath_gating(3)

PWR-592 (information) Datapath cell '%s' is not gated because

no opportunity for gating was found.

DESCRIPTION

This information message occurs when no state can be identified for which the output of the datapath cell is unused.

WHAT NEXT

This is only an information message. No action is necessary.

SEE ALSO

set_datapath_gating_options(2)
power_enable_datapath_gating(3)

PWR-593 (information) Datapath cell '%s' is not gated because gating did not prove useful.

DESCRIPTION

This information message occurs when the datapath cell is not gated since there is no power gain seen after gating the cell.

WHAT NEXT

This is only an information message. No action is necessary.

SEE ALSO

set_datapath_gating_options(2)
power_enable_datapath_gating(3)

PWR-600 (error) No valid command argument is specified with saif_map.

DESCRIPTION

The **saif_map** command is called without an argument that specifies an action. The **saif_map** command requires one of the following arguments that specify an action: **-start**, **-end**, **-reset**, **-report**, **-get_name**, **-set_name**, **-add_name**, **-remove_name**, **-clear_name**, **-get_object_names**, **-create_map**, **-write_map**, **-read_map**, **-verbose** and **-**

non_verbose.

WHAT NEXT

Use one of the above arguments with **saif_map** in order to specify the action required.

PWR-601 (error) The saif_map arguments '%s' and '%s' specify different commands and cannot be used together.

DESCRIPTION

The **saif_map** command is called with multiple arguments that specify different actions. The following **saif_map** commands specify different actions and cannot be used together: **-start**, **-end**, **-reset**, **-report**, **-get_name**, **-set_name**, **-add_name**, **-remove_name**, **-clear_name**, **-get_object_names**, **-create_map**, **-write_map** and **-read_map**.

WHAT NEXT

Use only one of the above arguments when calling the **saif_map** command.

PWR-602 (information) The SAIF name-mapping information database is %s.

DESCRIPTION

An information message that explains whether the SAIF name mapping database is currently active or inactive. The SAIF name mapping mechanism can be activated using the **saif_map -start** command and deactivated using the **saif_map -end** command. The features of the SAIF name mapping mechanism are only available when the name mapping database is active.

WHAT NEXT

This is an information message.

SEE ALSO

saif_map (2).

PWR-603 (information) The verbose mode of the SAIF name-

mapping mechanism is %s.

DESCRIPTION

Specifies whether the SAIF name mapping mechanism is current in verbose moe or not. The name mapping mechanism can be put in verbose mode using the **saif_map -verbose** command. The name mapping mechanism can be put in non-verbose mode using the **saif_map -non_verbose** command.

WHAT NEXT

This is an information message.

PWR-604 (error) The SAIF name-mapping mechanism is not active.

DESCRIPTION

The required operation needs the SAIF name-mapping mechanism to be active. You can activate the name-mapping mechanism by invoking **saif_map -start**.

WHAT NEXT

Activate the name-mapping mechanism with **saif_map -start** and repeat the command.

PWR-605 (error) The '-create_map' argument is specified without the '%s' argument.

DESCRIPTION

The **saif_map** argument **-create_map** needs the following two arguments: **-input** *filename* and **-source_instance** *instance_name*. The **-input** specifies the SAIF file that will be used for creating the SAIF Names information in the name mapping database. The **-source_instance** argument specifies the instance name of the current design as used in the SAIF file (that is, as the instance name in the simulation testbench).

WHAT NEXT

Use both the **-input** and **-source_instance** arguments with the **saif_map** command argument **-create_map**.

PWR-606 (error) When used with the '%s' argument, the saif_map command also requires a single design object as an argument.

DESCRIPTION

The action specified with the **saif_map** command argument also requires a single design object (port, cell, net or pin) to be used by the **saif_mapfP command.**

WHAT NEXT

Specify the missing argument with the **saif_map** command.

PWR-607 (error) The saif_map arguments '%s' and '%s' are mutually exclusive.

DESCRIPTION

The two **saif_map** arguments specify contradictory actions and are therefore mutually exclusive.

WHAT NEXT

Specify **saif_map** with only one of the mutually exclusive arguments.

PWR-608 (error) The saif_map argument '%s' is currently unavailable.

DESCRIPTION

The specified argument is still under construction.

WHAT NEXT

Avoid using the specified argument for now.

PWR-609 (error) Cannot recognize the saif_map column or sort

type ’%s’.

DESCRIPTION

The value of the **saif_map** arguments **-columns** and/or **-sort** is invalid. The valid value of these arguments is a list of SAIF name mapping report column names; The valid column names are: **type** (the type of object, that is, port, cell, net or pin), **object_names** (the name of the design object), **saif_names** (the SAIF Name of the design object), **orig_names** (the Orig Name of the design object), **extended_orig_names** (the Orig Name of the design object in extended syntax), and **attributes** or **flags** (the name mapping flags on the design object).

WHAT NEXT

Use valid values for the **saif_map** command arguments **-columns** and **-sort**.

PWR-610 (error) The saif_map column or sort type ’%s’ is used multiple times.

DESCRIPTION

The value of the **saif_map** argument **-columns** or **-sort** is invalid because a column name is used multiple times. Valid values of these arguments are lists of column names without repetitions.

WHAT NEXT

Use a valid value for the **saif_map** arguments **-columns** and **-sort**.

PWR-611 (error) Cannot recognize the -type argument ’%s’ for the command saif_map ’%s’.

DESCRIPTION

The **saif_map** command argument **-type** is invalid. Valid values for the **-type** argument depend on the other arguments of the **saif_map** command.

If the **-set_name**, **-get_name** or **-get_object_names** arguments are used, then the valid values of the **-type** argument are: **saif_names**, **orig_names** and **extended_orig_names**.

If the **-clear_name** argument is used, then the valid values of the **-type** argument are: **saif_names**, **orig_names**, **extended_orig_names** and **all_names**.

If the **-write_map** argument is used, then the valid values of the **-type** argument are: **name_map** and **ptpx**.

WHAT NEXT

Use a valid value for the **saif_map** argument **-type**.

PWR-612 (error) Cannot use the -type argument with the saif_map command '%s'.

DESCRIPTION

The **saif_map** argument **-type** cannot be used with the specified argument. The action arguments that can be used with the **-type** argument are: **-set_name**, **-get_name**, **-get_object_names**, **-clear_name**, and **-write_map**.

WHAT NEXT

Use valid arguments with the **saif_map** command.

PWR-613 (error) Cannot use the -inverted flag with the saif_map command '%s'.

DESCRIPTION

The **saif_map** command flag **-inverted** cannot be used with the specified action argument. The **-inverted** can be used with the **-set_name** and **-add_name** action arguments.

WHAT NEXT

Use valid arguments with the **saif_map** command.

PWR-614 (error) Cannot specify the saif_map '%s' argument together with a list of objects.

DESCRIPTION

A number of **saif_map** arguments (such as **-clear_name** also require a list of objects

that can be specified explicitly as a list of objects or implicitly using the optional arguments **-instances**, **-hierarchical**, **-no_hierarchical**. It is not possible to specify the objects both explicitly and implicitly, so it is not possible to use the **-instances**, **-hierarchical**, **-no_hierarchical** arguments together with a list of options.

WHAT NEXT

Specify the required objects either explicitly or implicitly.

PWR-615 (error) Cannot use the -instances argument with the saif_map command argument '%s'.

DESCRIPTION

The **saif_map** argument **-instances** can only be used when the **saif_map** operation requires a list of objects that can be specified implicitly. The command arguments that can use an implicitly specified list of objects are: **-report**, **-clear_name** and **-get_object_names**.

WHAT NEXT

Use valid arguments with the **saif_map** command.

PWR-616 (error) Cannot use the '%s' flag with the saif_map command '%s'.

DESCRIPTION

The **saif_map** optional flags **-hierarchical** and **-no_hierarchical** can only be used when the **saif_map** operation requires a list of objects that can be specified implicitly. The command arguments that can use an implicitly specified list of objects are: **-report**, **-clear_name** and **-get_object_names**.

WHAT NEXT

Use valid arguments with the **saif_map** command.

PWR-617 (error) Cannot use the '%s' argument with the

saif_map command '%s'.

DESCRIPTION

The **saif_map** arguments **-columns**, **-sort**, **-rtl_summary** and **-missing_rtl** can only be used when using the **saif_map** command argument **-report** to report the SAIF name mapping information on the current design.

WHAT NEXT

Use valid arguments with the **saif_map** command.

PWR-618 (error) The saif_map -columns argument must have at least one of: saif_names, orig_names, extended_orig_names.

DESCRIPTION

A column type that specifies the SAIF Names or an Orig Names of the design objects is missing from the **-column** argument of the **saif_map** command.

WHAT NEXT

Specify at least one of **saif_names**, **orig_names**, **extended_orig_names** when using the **-column** argument.

PWR-619 (error) Cannot use the '%s' argument with the saif_map command '%s'.

DESCRIPTION

The **saif_map** command arguments **-input_name**, **-source_instance** and **-target_instance** can only be used when creating the name mapping information from a SAIF file using the **-create_map** argument.

WHAT NEXT

Use valid arguments when using the **saif_map** command.

PWR-620 (information) Reporting correlated power.

DESCRIPTION

Power Prediction mode is on. The reported power numbers include predicted power.

WHAT NEXT

This is an information message. No action required.

PWR-621 (error) Can’t report power unless Power Prediction mode is on.

DESCRIPTION

In Topographical mode, power is reported only when Power Prediction mode is on.

WHAT NEXT

Run **set_power_prediction** followed by **compile_ultra** or **compile_ultra -incremental** before running the power reporting command.

PWR-622 (error) Use at least one option with the ’%s’ command.

DESCRIPTION

This command requires at least one option. Run the command with the -help option to see a list of all available options.

WHAT NEXT

Re-issue the command with at least one of the available options.

PWR-623 (error) Can’t find correlated power.

DESCRIPTION

The last compile of the design was run with out Power Prediction.

WHAT NEXT

Run **set_power_prediction** followed by **compile_ultra** or **compile_ultra -incremental** before running the power reporting command.

PWR-624 (warning) Skipping Clock Tree Power Estimation in PDB based run.

DESCRIPTION

Power Correlation is not supported when using PDB libraries.

WHAT NEXT

Rerun *compile_ultra* using MilkyWay libraries after setting *use_pdb_lib_format* to false .

PWR-625 (error) Clock Tree Estimation failed.

DESCRIPTION

The clock tree estimation step failed.

WHAT NEXT

Please contact support.

PWR-626 (Error) Power Prediction mode can not be set since the design has cells that can not be uniquified.

DESCRIPTION

Power Prediction can not be turned on if the design has hierarchical cells which can not be uniquified. This happens if there are multiply instantiated cells with *dont_touch* attribute or there are multiply instantiated cells inside a dont_touched cell.

WHAT NEXT

Use **uniquify -force** before turning on Power prediction.

PWR-627 (Error) Power constraint can not be set without enabling power prediction.

DESCRIPTION

In DC-Topographical mode, power constraints can not be set if power prediction mode could not be set.

WHAT NEXT

Check previous error messages to see why setting power prediction mode failed.

PWR-628 (Error) Power-driven clock gating during compile can not be enabled without enabling power prediction.

DESCRIPTION

In DC-Topographical mode, power-driven clock gating during compile can not be enabled if power prediction mode could not be set.

WHAT NEXT

Check previous error messages to see why setting power prediction mode failed.

PWR-630 (error) Cannot use the -hsep argument with the saif_map command '%s'.

DESCRIPTION

The **saif_map** command argument **-hsep** specifies the hierarchical separator when displaying or parsing SAIF Names and Orig Name. The **saif_map** command arguments that can take the **-hsep** argument are: **-get_name**, **-set_name**, **-add_name**, **-remove_name**, **-clear_name**, **-get_object_names**, and **-report**.

WHAT NEXT

Use valid arguments with the **saif_map** command.

PWR-631 (error) Invalid -hsep argument value: '%s'.

DESCRIPTION

An invalid value for the **saif_map** command argument **-hsep** is used. The valid values for the **-hsep** argument are: **"/"** (default value), **"."** and **" "**.

WHAT NEXT

Use a valid argument value.

PWR-632 (error) Cannot use a list of objects as arguments to the saif_map command '%s'.

DESCRIPTION

A list of objects is specified as arguments to the **saif_map** command together with a command argument that does not require a list of objects. The **saif_map** command arguments that can use a list of objects are: **set_name**, **get_name**, **add_name**, **clear_name**, **remove_name**, and **report**.

WHAT NEXT

Use valid argument with the **saif_map** command.

PWR-633 (error) The read_saif flags '%s' and '%s' are mutually exclusive.

DESCRIPTION

The **read_saif** flags **-map_names**, **-auto_map_names**, and **-rtl_direct** specify different actions are pairwise mutually exclusive. Also, the **read_saif** flags **-map_names**, **-auto_map_names**, and **-names_file** are pairwise mutually exclusive.

WHAT NEXT

Use at most one of the mutually exclusive flags with the **read_saif** command.

PWR-634 (error) Unable to create name mapping for SAIF file;

The swtiching activity information in the SAIF file will not be annotated.

DESCRIPTION

The **read_saif** command is specified with the **-auto_map_names** to create SAIF name mapping information and use it to read the SAIF file, but the name mapping information could not be created.

WHAT NEXT

Fix the problem that causing the name mapping creating to fail. You can use the **saif_map** with the **-create_map** argument to just create the name mapping information and help you debug the problem.

SEE ALSO

saif_map (2).

PWR-635 (information) Writing SAIF name mapping information to file '%s'.

DESCRIPTION

Power Compiler is generating a SAIF name mapping file for the current design.

WHAT NEXT

This is an information message. The SAIF name mapping file can be read back in future using the **saif_map** command with the **-read_map** argument.

PWR-636 (information) Writing SAIF name mapping information into the PT-PX name mapping file '%s'.

DESCRIPTION

Power Compiler is generating a name mapping file to be read by PT-PX. The generated name mapping file contains PT-PX **set_rtl_to_gate_name** commands and cannot be read into Power Compiler.

WHAT NEXT

This is an information message.

PWR-637 (information) Reading SAIF name-mapping information from file '%s'.

DESCRIPTION

Power Compiler is reading the SAIF name-mapping information from the specified file.

WHAT NEXT

This is an information message.

PWR-638 (warning) Unable to process line %d of SAIF name mapping file '%s' starting with: '%s'.

DESCRIPTION

An error occured while processing the SAIF name-mapping file. The specified line in the SAIF name-mapping file is not in a format that is expected by the **saif_map** command. It is likely that the SAIF name-mapping file used to store the SAIF name-mapping information is invalid.

WHAT NEXT

Use a valid SAIF name mapping file generated by the **saif_map** command argument **-write_map** when reading SAIF name-mapping information.

PWR-639 (error) Cannot process the SAIF name-mapping file: '%s'.

DESCRIPTION

Too many errors occured while processing the SAIF name-mapping file and the read operation has been aborted. No SAIF name-mapping information has been read properly. The provided file is not in a format that can be understood by the **saif_map** command argument **-read_map**.

WHAT NEXT

Use a valid SAIF name mapping file generated by the **saif_map** command argument **-write_map** when reading SAIF name-mapping information.

PWR-640 (information) Annotating original name information on design object for SAIF name matching.

DESCRIPTION

SAIF name matching information is being stored on design objects. This information represents the original names of the design objects and can be used later for matching SAIF names in RTL backward SAIF files with design objects.

WHAT NEXT

This is an information message.

SEE ALSO

saif_map (2).

PWR-641 (warning) Unable to find the %s '%s' in the current design when reading line %d of SAIF name mapping file '%s'.

DESCRIPTION

A design object specified in the SAIF name mapping file cannot be found. It is likely that the specified SAIF name mapping file is not intended for the current design.

WHAT NEXT

Make sure that the SAIF name mapping file being read is intended for the current design.

PWR-642 (warning) The rtl2saif command will be obsoleted in future versions; use flows involving the saif_map command to

read RTL SAIF files.

DESCRIPTION

You are using the **rtl2saif** command to generate a forward RTL SAIF file, but flows involving the forward RTL SAIF file will be made obsolete in future. To generate and read backward RTL SAIF files, do not use forward RTL SAIF files and use the **saif_map** command and the **-auto_map_names** and/or **-map_names** arguments of **read_saif**. The following is a sample script template for reading RTL SAIF files:

```
saif_map -start
read... rtl_source
link
read_saif -auto_map_names -input rtl.saif -instance tb/u1
```

where the **rtl.saif** is a backward RTL SAIF file generated without using a forward RTL SAIF file. To properly generate a backward RTL SAIF file without using a forward SAIF file, the following guidelines should be followed:-

• When using the **vcd2saif** utility, the **-rtl** argument should not used.

• When using the direct SAIF generation of Synopsys VCS and VCS/MX, or the Synopsys SAIF generation PLI/FLI utilities, the gate/net monitoring policy should be set to **rtl_on** and an RTL SAIF file should not be read. To set the monitoring policy, use the PLI task **set_gate_level_monitoring** or the FLI task **set_net_monitoring_policy**.

WHAT NEXT

This is a warning message; for best performance use the **saif_map** flow for reading RTL backward SAIF files.

SEE ALSO

saif_map(2)
read_saif(2)

PWR-643 (information) The variable "power_preserve_rtl_hier_names" is set to "true"; This variable is not required when using the saif_map command and will be obsoleted in future releases.

DESCRIPTION

The **power_preserve_rtl_hier_names** is not required when using flows involving the **saif_map** command to read RTL SAIF files. The **power_preserve_rtl_hier_names** variable

is only required if using the **rtl2saif** command and/or the **-rtl_direct** option of **read_saif**; however, note that such flows will be unsupported in future versions of the tool.

WHAT NEXT

This is an information message; you do not need to set the **power_preserve_rtl_hier_names** variable if your flow does not involve the **rtl2saif** command or the **-rtl_direct** flag.

PWR-644 (warning) The **-rtl_direct** flag will be made obsolete; use flows involving the **-map_names** and/or **-auto_map_names** flags and the **saif_map** command to read RTL SAIF files.

DESCRIPTION

You are using the **-rtl_direct** flag to read a SAIF file, but this flag will be made obsolete in future. To generate and read backward RTL SAIF files, it is suggested to use the **saif_map** command and the **-auto_map_names** and/or **-map_names** arguments of **read_saif**. The following is a sample script template for reading RTL SAIF files:

```
saif_map -start
read... rtl_source
link
read_saif -auto_map_names -input rtl.saif -instance tb/u1
```

where the **rtl.saif** is a backward RTL SAIF file generated without using a forward RTL SAIF file. To properly generate a backward RTL SAIF file without using a forward SAIF file, the following guidelines should be followed:-

• When using the **vcd2saif** utility, the **-rtl** argument should not used.

• When using the direct SAIF generation of Synopsys VCS and VCS/MX, or the Synopsys SAIF generation PLI/FLI utilities, the gate/net monitoring policy should be set to **rtl_on** and an RTL SAIF file should not be read. To set the monitoring policy, use the PLI task **set_gate_level_monitoring** or the FLI task **set_net_monitoring_policy**.

WHAT NEXT

This is a warning message; for best performance use the **saif_map** flow for reading RTL backward SAIF files.

SEE ALSO

saif_map(2)

PWR-645 (error) Cannot use the saif_map arguments '%s' and '%s' together.

DESCRIPTION

A number of mutually exclusive arguments are used with the **saif_map** command argument **-report**.

The **-rtl_summary flag cannot be used with the -columns**, **-sort**, or **-hsep** arguments. The **-rtl_summary flag specifies that a summary report on synthesis invariants is to be reported, while the -columns**, **-sort** and **-hsep** arguments are used to control the full (non-summary) report.

WHAT NEXT

Use valid arguments with the **saif_map** command.

PWR-646 (error) Cannot use the '%s' flag with the saif_map command '%s'.

DESCRIPTION

The **-nosplit** flag can only be used with the **saif_map** command argument -report.

WHAT NEXT

Use valid arguments with the **saif_map** command.

PWR-647 (error) The '%s' flag can only be specified with the '%s' flag.

DESCRIPTION

The **-missing_rtl** flag can only be specified with both the **-report** and **-rtl_summary** flags of the **saif_map** command to include a list of synthesis invariant objects with no SAIF names when displaying a summary SAIF mapping report on synthesis invariant objects.

WHAT NEXT

Use valid arguments with the **saif_map** command.

PWR-648 (information) The clock '%s' does not have a period.

DESCRIPTION

The given clock does not have a period and will not be used in related clock inference or other power calculation steps.

WHAT NEXT

This is an information message; if the given clock is expected to have a period then check that it was created properly.

PWR-649 (warning) The clock '%s' associated with the %s '%s' does not have a period.

DESCRIPTION

The design object (net, pin, or port) given in the warning message has a clock associated with it that does not have a period. A clock can be associated to a design object by using the -clock option of the set_switching_activity command. The associated, or related, clock period is used to calculate the effective toggle rate of the object used in power calculations. The effective toggle rate is the annotated toggle rate divided by the period of the related clock. When a related clock is not specified, the annotated toggle rate relative to the library time unit is used. In this case, the related clock does not exists in the current design, and for power calculations, the related clock period is assumed to be 1.0.

The related clock is also used during the related clock inference mechanism. If a related clock has no period then it cannot be used to infer the related clock of other design objects.

WHAT NEXT

Check that the given clock was created properly, or use a different related clock on the specified object.

PWR-650 (warning) A minimum bit-width constraint has been

set; power-driven clock gating may yield inferior results.

DESCRIPTION

To obtain optimal results it is advised not to set a minimum bit-width constraint when performing power-driven clock gating. This allows the optimization algorithm to optimally clock gate the design based on the switching activity and dynamic power of the register banks.

WHAT NEXT

Do not explicitly specify a minimum bit-width constraint by not setting the -minimum_bitwidth option with the **set_clock_gating_style** command.

PWR-651 (warning) A GICG style is set; clock gate insertion will not be performed.

DESCRIPTION

Clock gating is not supported with generic integrated clock gating (GICG) styles.

WHAT NEXT

Specify a discrete or standard integrated clock gating (ICG) style with the **set_clock_gating_style** command.

PWR-652 (warning) The '-exact_map' option may not be honored for registers that are involved in clock gating optimization.

DESCRIPTION

Both the **-gate_clock** and **-exact_map** options were specified with **compile** or **compile_ultra**. Since registers can be remapped during both removal and insertion of clock gating, it may not always be possible to honor the **-exact_map** option for those registers that are involved with clock gating optimization.

WHAT NEXT

If honoring the exact_map option has the highest priority, do not use the **-gate_clock** option with **compile** or **compile_ultra**. Instead, use the

insert_clock_gating command to introduce clock gates in the design at the RT-level.

PWR-653 (warning) reserved for power-driven CG

DESCRIPTION

reserved for power-driven CG

WHAT NEXT

reserved for power-driven CG

PWR-654 (warning) reserved for power-driven CG

DESCRIPTION

reserved for power-driven CG

WHAT NEXT

reserved for power-driven CG

PWR-655 (warning) reserved for power-driven CG

DESCRIPTION

reserved for power-driven CG

WHAT NEXT

reserved for power-driven CG

PWR-656 (warning) reserved for power-driven CG

DESCRIPTION

reserved for power-driven CG

WHAT NEXT

reserved for power-driven CG

PWR-657 (warning) reserved for power-driven CG

DESCRIPTION

reserved for power-driven CG

WHAT NEXT

reserved for power-driven CG

PWR-658 (warning) reserved for power-driven CG

DESCRIPTION

reserved for power-driven CG

WHAT NEXT

reserved for power-driven CG

PWR-659 (warning) reserved for power-driven CG

DESCRIPTION

reserved for power-driven CG

WHAT NEXT

reserved for power-driven CG

PWR-660 (warning) Multiple threshold voltage groups were not detected from the library. Leakage power optimization will treat

the design as single threshold voltage.

DESCRIPTION

Multiple threshold voltage groups are identified by setting the *threshold_voltage_group* attribute on library cells or *default_threshold_voltage_group* on libraries. The threshold voltage group information helps **compile** to better optimize the leakage power of the design. These message indicate that no such attribute were set or the libraries only has one threshold voltage group.

WHAT NEXT

Check whether the design has single threshold voltage group or the threshold voltage group attributes are set.

PWR-661 (warning) A latch-based clock-gating style was chosen but no latches are in the technology library.

DESCRIPTION

The default clock-gating style or user defined clock-gating style use "latch" without a specific library as the *-sequential_cell* option but the technology library has no latch.

WHAT NEXT

Change the clock gating style to a latch-free style or add latches to the technology library.

PWR-662 (warning) Register ’%s’ (%s) will not be translated to the retention specification.

DESCRIPTION

This warning message occurs when the named register cannot be translated into a retention cell provided in the target_library. The most likely reason is that no library cell exists in the target_library that matches the asynchronous or clock-phase requirements of the register in the input netlist (for example, RTL), while still satisfying the specified retention style or retention library cells (using the **set_power_gating_style**, or **map_retention_cell** commands).

Other possible reasons are

• There is a dont_touch flag on the cell

• You are running **compile -incr** or **compile_ultra -incr**, which does not re-target cells from non-retention to retention.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, you can investigate the reason for not getting the desired mapping.

If it is because of library cells not meeting the asynchronous requirements, add a correctly-modeled retention cell to the target_library, or modify the RTL to change the asynchronous requirements.

If it is because of clock-phase, add a correctly-modeled retention cell to the target_library, or modify the RTL to change the clock-phase.

If you want to re-target a pre-mapped non-retention cell to a retention cell, run the full **compile_ultra** command.

SEE ALSO

compile(2)
compile_ultra(2)

PWR-663 (warning) Variable '%s' cannot be used in UPF mode (default mode).

DESCRIPTION

This warning message occurs because the variable used to enable power gating cannot be used in UPF mode. In UPF mode, power gating (retention) flow is automatically enabled by the existence of the set_retention strategy. This variable should not be used to force the flow.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this error, remove the setting of this variable in UPF mode.

PWR-670 (warning) sa error

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-671 (warning) sa error

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-672 (warning) sa error

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-673 (warning) sa error

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-674 (warning) sa error

DESCRIPTION

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WHAT NEXT

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PWR-675 (warning) sa error

DESCRIPTION

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WHAT NEXT

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PWR-676 (warning) sa error

DESCRIPTION

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WHAT NEXT

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PWR-677 (warning) sa error

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-678 (warning) sa error

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-679 (warning) sa error

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-680 (warning) merge_clock_gates will be obsolete in dc_shell in the next release.

DESCRIPTION

The command **merge_clock_gates** will be obsoleted in dc_shell in the next major release.

WHAT NEXT

Do not use **-max_fanout** option of **set_clock_gating_style** command to get maximally merged clock gate configuration. Also the command may still be available in icc_shell.

PWR-700 (error) Cannot specify the -reset flag with the

percentage value argument.

DESCRIPTION

The **-reset** flag of the **set_max_lvth_percentage** command specifies that the current max %lvth constraints will be removed and cannot be used with arguments that specify new max %lvth constraints.

WHAT NEXT

Use a valid set of arguments with the **set_max_lvth_percentage** command. To remove the current constraints use the **-reset** flag with no other arguments. To set new constraints specify the max %lvth percentage value as an argument to the command together with the list of vth groups to be considered as low vth using the **-lvth_groups** argument.

PWR-701 (error) Cannot specify the -reset flag with the -lvth_groups argument.

DESCRIPTION

The **-reset** flag of the **set_max_lvth_percentage** command specifies that the current max %lvth constraints will be removed and cannot be used with arguments that specify new max %lvth constraints.

WHAT NEXT

Use a valid set of arguments with the **set_max_lvth_percentage** command. To remove the current constraints use the **-reset** flag with no other arguments. To set new constraints specify the max %lvth percentage value as an argument to the command together with the list of vth groups to be considered as low vth using the **-lvth_groups** argument.

PWR-702 (error) Cannot specify the value argument without the -lvth_groups argument.

DESCRIPTION

The **set_max_lvth_percentage** argument can be used to set the max %lvt constraint by specifying the value of the constraint as a floating point value argument to the command and by specifying the list of vth groups to be considered as low vth using the **-lvth_groups** argument.

WHAT NEXT

Use a valid set of arguments with the **set_max_lvth_percentage** command. To set new constraints specify the max %lvth percentage value as an argument to the command together with the list of vth groups to be considered as low vth using the **-lvth_groups** argument.

PWR-703 (error) Cannot specify the -lvth_groups argument without a percentage value argument.

DESCRIPTION

The **set_max_lvth_percentage** argument can be used to set the max %lvt constraint by specifying the value of the constraint as a floating point value argument to the command and by specifying the list of vth groups to be considered as low vth using the **-lvth_groups** argument.

WHAT NEXT

Use a valid set of arguments with the **set_max_lvth_percentage** command. To set new constraints specify the max %lvth percentage value as an argument to the command together with the list of vth groups to be considered as low vth using the **-lvth_groups** argument.

PWR-704 (error) The -lvth_groups argument ’%s’ is not a valid vth group name.

DESCRIPTION

The **set_max_lvth_percentage** command is specified with an invalid **-lvth_groups** argument. The **-lvth_groups** argument is a list of strings specifying vth groups. Valid vth groups are non-empty strings and may contain alphanumeric characters and the underscore ("_") character.

WHAT NEXT

Specify a valid **-lvth_groups** argument to the **set_max_lvth_percentage** command.

PWR-705 (warning) Unable to parse the max_lvth information.

DESCRIPTION

The representation of the max %lvth information is not valid, and any max %lvth constraints will be ignored. This happens if the attributes representing the max %lvth constraint have been set incorrectly directly using the set_attribute command. The max %lvth information can be set correctly using the **set_max_lvth_percentage** command.

WHAT NEXT

Use the **fBset_max_lvth_percentage -reset** command to clear the current max %lvth constraint; then re-issue the **set_max_lvth_percentage** with valid arguments to set the max %lvth constraints if these are required.

PWR-706 (warning) mvt error

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-707 (warning) mvt error

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-708 (warning) mvt error

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-709 (warning) mvt error

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-710 (warning) mvt error

DESCRIPTION

reserved

WHAT NEXT

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PWR-711 (warning) mvt error

DESCRIPTION

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WHAT NEXT

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PWR-712 (warning) mvt error

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WHAT NEXT

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PWR-713 (warning) mvt error

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reserved

WHAT NEXT

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PWR-714 (warning) mvt error

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WHAT NEXT

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PWR-715 (warning) mvt error

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PWR-716 (warning) mvt error

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-717 (warning) mvt error

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-718 (warning) mvt error

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-719 (warning) mvt error

DESCRIPTION

reserved

WHAT NEXT

reserved

PWR-720 (error) report_power is disabled since the design has ILMs.

DESCRIPTION

Power reporting is not permitted currently in designs with ILMs.

WHAT NEXT

You can report power after linking in the original netlists for the ILM blocks.

PWR-721 (warning) Not setting Power Prediction mode, because the design has ILMs

DESCRIPTION

Power prediction mode is not turned on since the design has ILM blocks. But the power constraint specified will be used during optimization.

WHAT NEXT

Link in the original netlist for the ILM blocks if you want to turn on Power Prediction.

PWR-722 (error) Power Prediction mode can not be set, because the design has ILMs

DESCRIPTION

Power Prediction mode can not be turned on currrently on designs with ILMs

WHAT NEXT

Link in the original netlist for the ILM blocks before turning on Power Prediction.

PWR-723 (error) %s can not be used, because the design has

multiple scenarios.

DESCRIPTION

%s is not supported in a design with multiple scenarios.

WHAT NEXT

Remove %s from the multi-scenario design.

PWR-724 (error) %s cannot be used, because the design has multiple scenarios. Reset power_driven_clock_gating to false.

DESCRIPTION

This error message occurs when attempting to use power driven clock gating on a design that has multiple scenarios. Power-driven clock gating is not supported in a design with multiple scenarios.

WHAT NEXT

Set the **power_driven_clock_gating** variable to false and run the command again.

SEE ALSO

power_driven_clock_gating(3)

PWR-725 (Warning) Could not find correlated power.

DESCRIPTION

The last compile of the design was run with out Power Prediction.

WHAT NEXT

To report correlated power, run **set_power_prediction** followed by **compile_ultra** or **compile_ultra -incremental** before running the power reporting command.

PWR-726 (Warning) Power Prediction mode can not be set

since the design has cells that can not be uniquified.

DESCRIPTION

Power Prediction can not be turned on if the design has hierarchical cells which can not be uniquified. This happens if there are multiply instantiated cells with *dont_touch* attribute or there are multiply instantiated cells inside a dont_touched cell.

WHAT NEXT

Use **uniquify -force** before turning on Power prediction.

PWR-727 (Warning) Can not report correlated power unless power prediction mode is set.

DESCRIPTION

If power prediction is not set, correlated power will not be reported.

WHAT NEXT

To report correlated power, run **set_power_prediction** before running the power reporting command.

PWR-728 (information) set_clock_gating_registers directives on technology-mapped registers are honored only in compile -gate_clock flow.

DESCRIPTION

This information message advises you that the **insert_clock_gating** command flow does not honor **set_clock_gating_registers** directives on technology-mapped registers.

WHAT NEXT

This is an information message only. No action is required.

However, if you are using the **insert_clock_gating** command to insert clock gates, apply the clock gating directives and invoke **insert_clock_gating** before the registers are mapped. There is no restriction when this command is used with the

compile -gate_clock [-incr] or **compile_ultra -gate_clock [-incr]** commands.

SEE ALSO

compile(2)
compile_ultra(2)
insert_clock_gating(2)

PWR-729 (warning) Clock gating insertion with insert_clock_gating is deprecated and will be removed in a future release; instead use the compile -gate_clock command.

DESCRIPTION

The **compile -gate_clock** command provides additional features compared to the **insert_clock_gating** command. In addition to the regular clock gating also performed by **insert_clock_gating**, the **compile -gate_clock** command attempts to find even more clock gating opportunities by combing different register banks that share common enable conditions. Furthermore, it can create multi-stage clock gating designs by factoring common enable conditions from the inserted clock gates. This can further reduce the power dissipation.

WHAT NEXT

Use the **compile -gate_clock** command to introduce clock gating in your design.

SEE ALSO

set_clock_gating_style (2), **compile** (2).

PWR-730 (Information) Performing clock-gating on design %s.

DESCRIPTION

The tool is inserting clock gating on design %s. All gateable registers in this design based on the selected clock gating style will get gated.

Every clock gate inserted by this will be located on the same level of hierarchy as the registers. If you want clock gates to be shared between levels of hierarchy, set the variable **compile_clock_gating_through_hierarchy** to **true**

WHAT NEXT

This is an information message and no action is required. If you did not intend to insert clock gating on your design, remove **-gate_clock** from your **compile** or **compile_ultra** options.

PWR-731 (Information) Performing global clock-gating on design %s.

DESCRIPTION

The tool is inserting clock gating on design %s. All gateable registers in this design based on the selected clock gating style will get gated.

Every clock gate inserted by this will be shared between different levels of hierarchy. If you want clock gates to be on the same level of hierarchy as the registers, set the variable **compile_clock_gating_through_hierarchy** to **false**

WHAT NEXT

This is an information message and no action is required. If you did not intend to insert clock gating on your design, remove **-gate_clock** from your **compile** or **compile_ultra** options.

PWR-732 (Information) Performing power driven clock-gating.

DESCRIPTION

Registers will get clock gated only if they fulfil the restrictions set with the current selected clock gating style and if clock gate insertion reduces the overall power consumption of the design.

WHAT NEXT

This is an information message and no action is required. If you did not intend to use power driven clock gating, set the **power_driven_clock_gating** variable to false.

PWR-733 (Error) value ’%s’ for option ’-fanout_latency’ is not

valid.

DESCRIPTION

Syntax of argument given to option -fanout_latency for set_clock_gate_latency command is not valid.

The expected value is a comma separated list with the format {n1-m1 lat1, n2-m2 lat2, n3-m3 lat3, ...} where:

-
ni and mi are positive integer numbers representing respectively lower and upper limits for fanout ranges. The first fanout range must start from 1 and the last one must finish with the string 'inf'. The ranges should not overlap each other.

-
lati are floating point numbers representing a clock latency to be applied to each range.

WHAT NEXT

Supply a compatible value for the argument.

PWR-734 (Error) '%s' is not a floating point number.

DESCRIPTION

The substring of argument given to option -fanout_latency for set_clock_gate_latency command, which specifies the clock latency to be applied, is not a floating point number.

The expected value for this argument is a comma separated list with the format {n1-m1 lat1, n2-m2 lat2, n3-m3 lat3, ...} where:

-
ni and mi are positive integer numbers representing respectively lower and upper limits for fanout ranges. The first fanout range must start from 1 and the last one must finish with the string 'inf'. The ranges should not overlap each other.

-
lati are floating point numbers representing a clock latency to be applied to each range.

WHAT NEXT

Supply a compatible value for the argument.

PWR-735 (Error) '%s' is not a positive integer number.

DESCRIPTION

A substring of argument given to option -fanout_latency for set_clock_gate_latency command, which specifies an upper or lower limit for a fanout range is is not a positive integer number.

The expected value for this argument is a comma separated list with the format {n1-m1 lat1, n2-m2 lat2, n3-m3 lat3, ...} where:

- ni and mi are positive integer numbers representing respectively lower and upper limits for fanout ranges. The first fanout range must start from 1 and the last one must finish with the string 'inf'. The ranges should not overlap each other.

- lati are floating point numbers representing a clock latency to be applied to each range.

WHAT NEXT

Supply a compatible value for the argument.

PWR-736 (Error) wrong fanout range specified: %d-%d.

DESCRIPTION

A substring of argument given to option -fanout_latency for set_clock_gate_latency command, which specifies a fanout range is not valid because the lower limit is higher than the upper limit.

The expected value for this argument is a comma separated list with the format {n1-m1 lat1, n2-m2 lat2, n3-m3 lat3, ...} where:

- ni and mi are positive integer numbers representing respectively lower and upper limits for fanout ranges. The first fanout range must start from 1 and the last one must finish with the string 'inf'. The ranges should not overlap each other.

- lati are floating point numbers representing a clock latency to be applied to each range.

WHAT NEXT

Supply a compatible value for the argument.

PWR-737 (Warning) A fanout of 0 is invalid, value will be ignored.

DESCRIPTION

A substring of argument given to option -fanout_latency for set_clock_gate_latency command, which specifies the lower limit for a fanout range is the integer number 0. This value is ignored so the considered fanout range will start from 1.

The expected value for this argument is a comma separated list with the format {n1-m1 lat1, n2-m2 lat2, n3-m3 lat3, ...} where:

- ni and mi are positive integer numbers representing respectively lower and upper limits for fanout ranges. The first fanout range must start from 1 and the last one must finish with the string 'inf'. The ranges should not overlap each other.
- lati are floating point numbers representing a clock latency to be applied to each range.

WHAT NEXT

Supply a fanout range starting from 1.

PWR-738 (Warning) Lower limit of first fanout range was extended to 1.

DESCRIPTION

A substring of argument given to option -fanout_latency for set_clock_gate_latency command, which specifies the lower limit for the first fanout range is an integer number higher than 1.

Since the specified fanout values must cover the complete range from 1 to 'inf', the lower limit for this first fanout range is extended to start from 1.

The expected value for this argument is a comma separated list with the format {n1-m1 lat1, n2-m2 lat2, n3-m3 lat3, ...} where:

-
ni and mi are positive integer numbers representing respectively lower and upper limits for fanout ranges. The first fanout range must start from 1 and the last one must finish with the string 'inf'. The ranges should not overlap each other.

-
lati are floating point numbers representing a clock latency to be applied to each range.

WHAT NEXT

Supply a fanout range starting from 1.

PWR-739 (Warning) Upper limit of last fanout range was extended to 'inf'.

DESCRIPTION

A substring of argument given to option -fanout_latency for set_clock_gate_latency command, which specifies the upper limit for the last fanout range is not the string 'inf'.

Since the specified fanout values must cover the complete range from 1 to 'inf', the upper limit for this last fanout range is extended to finish at 'inf'.

The expected value for this argument is a comma separated list with the format {n1-m1 lat1, n2-m2 lat2, n3-m3 lat3, ...} where:

-
ni and mi are positive integer numbers representing respectively lower and upper limits for fanout ranges. The first fanout range must start from 1 and the last one must finish with the string 'inf'. The ranges should not overlap each other.

-
lati are floating point numbers representing a clock latency to be applied to each range.

WHAT NEXT

Supply a fanout range finishing at 'inf'.

PWR-740 (Warning) Fanout range %d-%d has no clock latency

information, value %.2f will be applied to it.

DESCRIPTION

No clock latency was specified for the listed fanout range. The tool will select for it the lowest latency value from the adjacent fanout ranges.

WHAT NEXT

Supply clock latency information for the complete fanout range going from 1 to 'inf'.

PWR-741 (Warning) One or more specified fanout ranges are overlapping.

DESCRIPTION

One or more fanout ranges specified as part of argument given to option -fanout_latency for set_clock_gate_latency command are overlapping.

The tool will select the lowest specified clock latency for those ranges with more than one value provided.

WHAT NEXT

Supply clock latency information for non overlapping fanout ranges.

PWR-742 (Warning) Clock latency of %.2f specified for fanout range %d-%d is lower than value %.2f specified for range %d-%s.

DESCRIPTION

The specified clock latency values are not decreasing with respect to fanout ranges. This may produce inconsistent clock latency settings and as a result a wrong timing analysis.

WHAT NEXT

Make sure that clock latency values are decreasing with respect to fanout ranges.

PWR-743 (Warning) Only one clock latency specification is meaningful for stage 0, value %.2f will be used.

DESCRIPTION

Argument given to option -fanout_latency for set_clock_gate_latency command specifies different fanout ranges, while value given for option -stage is 0.

Since the fanout range for "stage 0" is meaningless, the expected syntax for that argument in this case is {1-inf lat} where lat is a floating point number representing the clock latency to be applied to each gated register.

The tool will select the lowest specified clock latency value.

WHAT NEXT

Supply a compatible value for the argument.

PWR-744 (Warning) In clock gating latency settings specified for clock '%s', the max value for stage %d (%.2f) is higher than the min value for stage %d (%.2f)

DESCRIPTION

The specified clock latency values are not decreasing with respect to clock gating stages. This may produce inconsistent clock latency settings and as a result a wrong timing analysis.

WHAT NEXT

Make sure that clock latency values are decreasing with respect to clock gating stages.

PWR-745 (Warning) Clock latency settings are not available for clock gating stage %d with respect to clock %s.

DESCRIPTION

The tool has found one or more clock gating cells with a stage for which there is no clock latency specified by using set_clock_gate_latency command. The clock latency for these clock gating cells will be based on timer propagated values from the

previous stage.

WHAT NEXT

Make sure the supplied clock latency settings are the desired ones.

PWR-746 (Warning) Inconsistent clock latency specification found. Assuming value %f for cell %s.

DESCRIPTION

The tool has found an inconsistent clock latency specified on a clock gating cell in a clock path, for which, some clock latency settings have been provided by set_clock_gate_latency command.

The tool assumes the smaller value for clock latency annotation on clock gating cells, so that it is ensured that clock latencies are monotonically increasing values in the path going from the clock source to the gated registers.

WHAT NEXT

Make sure the supplied clock latency settings are the desired ones.

PWR-747 (Error) No clocks found on current design.

DESCRIPTION

It is not possible to specify clock latency values with **set_clock_gate_latency** command because there is no clock object defined for current design.

WHAT NEXT

Use **create_clock** command to apply clock constraints for current design.

PWR-748 (Error) No clocks found on current design.

DESCRIPTION

It is not possible to execute **reset_clock_gate_latency** command because there is no clock object defined for current design.

WHAT NEXT

Use **create_clock** command to apply clock constraints for current design.

PWR-749 (Error) No clock latency settings supplied for clock gating cells.

DESCRIPTION

apply_clock_gate_latency command has been executed with no previous call to **set_clock_gate_latency** command.

WHAT NEXT

Use **set_clock_gate_latency** command to provide some clock latency settings for clock gating cells.

PWR-750 (Warning) No clocks found on current design.

DESCRIPTION

Report generated by **report_clock_gating -structure** command is clock based. If no clock is defined for current design, only the summary report is printed.

WHAT NEXT

Use **create_clock** command to apply clock constraints for current design.

PWR-751 (Warning) Could not ungate register '%s'.

DESCRIPTION

Remove clock gating or clock gate clean up step could not remove the clock gating for the register mentioned.

WHAT NEXT

Please contact support.

PWR-752 (Error) Power unit not found in library. Power calculation will be aborted in create_ilm.

DESCRIPTION

Neither leakage power unit nor dynamic power unit is found in the library or the environment variable. The user encounters this error message because power units are needed to perform power calculation during create_ilm command.

WHAT NEXT

If user does not want power calculation performed in create_ilm command, user can disable it by issuing the following variable before create_ilm. **set ilm_enable_power_calculation FALSE** Otherwise, use a library that defines the units required for power.

PWR-753 (warning) Can not ungate register '%s' because it is scan stitched.

DESCRIPTION

A scan stitched register or a register where the scan related pins are used for functional logic can not be ungated.

WHAT NEXT

Invoke **remove_clock_gating** (or the optimization step that tried to ungate the register) before doing **insert_dft**.

PWR-754 (Error) Can not remove clock gating on a scan stitched design.

DESCRIPTION

Clock gating removal has to be performed before stitching the scan chains.

WHAT NEXT

Invoke **remove_clock_gating** before doing **insert_dft**.

PWR-755 (Warning) Skipping clock tree estimation because one or more irregular rows were found for site array.

DESCRIPTION

Clock Tree Estimation requires a regular site array, so that the width and the spacing between the sites are equal.

WHAT NEXT

Correct the site array definition and rerun **compile_ultra** command with power prediction turned on.

PWR-756 (warning) Design contains no clocks or clock sources.

DESCRIPTION

This warning message occurs because the tool cannot find any clocks or clock sources in the design when running the **identify_clock_gating** command. Identification of clock gates is not possible.

WHAT NEXT

This is only a warning message. No action is necessary.

However, if the result is not what you intended, you can run the **create_clock command with the *port_name*** parameter for all clocks in the design and recompile your design.

SEE ALSO

create_clock(2)
identify_clock_gating(2)

PWR-757 (information) Performing clock gating circuitry identification in design '%s'.

DESCRIPTION

This information message informs you that the tool is identifying clock gating logic on the specified design. All clock gates inserted by the tool in another run will be identified.

WHAT NEXT

This is an information only message. No action is required.

PWR-758 (Warning) Library cell %s is not present for the operating condition P=%f, V=%f, T=%f.

DESCRIPTION

This warning message occurs when the tool encounters a missing library cell. Library cells must be available for all of the operating conditions that are used by the active scenarios during compile. Power optimization cannot work correctly when a library cell is missing.

WHAT NEXT

Use the **set_check_library_options** command with the **-mcmm** option, followed by the **check_library** command to determine the library cells that are not available in all (P,V,T)s. Either use consistent libraries or set DONT_USE on the cells that are not available for all active operating conditions.

SEE ALSO

check_library(2)
list_libs(2)
set_check_library_options(2)

PWR-759 (warning) %d Library cells are not available for one of the leakage scenarios.

DESCRIPTION

This warning message is a summary message of PWR-758. Library cells should be available for all operating conditions that are used by the active scenarios during compile. Power optimization cannot work correctly because library cells are missing for one or more leakage operating conditions.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, use the **set_check_library_options -mcmm** command followed by the **check_library** command to determine the library cells that are not available in all of the (P,V,T)s. Either use consistent libraries or

set DONT_USE on the cells that are not available for all of the active operating conditions.

SEE ALSO

check_library(2)
list_libs(2)
set_check_library_options(2)

PWR-760 (warning) Specified clock gate '%s' is not a valid Power Compiler clock gate.

DESCRIPTION

This warning message occurs because Power Compiler does not support this type of clock gating. The cell will not be identified as a clock gate.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this message, run the command only on a valid Power Compiler clock gate.

PWR-761 (information) Correlated power is not available.

DESCRIPTION

Power Prediction is not supported for multi-scenario designs.

WHAT NEXT

This is an informational message only. No action is required.

PWR-762 (information) Clock gated %s '%s' will be ungated, since its clock-gating cell is being removed.

DESCRIPTION

This information message occurs when a clock gate is being removed as part of the optimizations. All the registers gated by this clock-gate cell become ungated.

WHAT NEXT

This is an information only message. No action is required.

PWR-763 (information) A library cell required for the %s edge clock gating style specified (%s) is not available for hierarchical block '%s'. %s edge registers in this block will not be clock gated.

DESCRIPTION

The *target_library* does not have any library cells that meets the specified clock gating style and operating conditions for this hierarchical block. Clock gate insertion can't be performed.

WHAT NEXT

Adjust your clock gating style and operating conditions for the available clock gating library cells.

PWR-781 (Warning) Hierarchical clock gating cell %s has its internal logic not connected to the clock or enable clock port.

DESCRIPTION

Can't obtain a path from the clock input port to the clock enabled output port. Hence can not determine if the cell is inverting.

WHAT NEXT

Check the clock gate has all this connections in place.

PWR-800 (warning) Use of %s is not recommended. This feature will be obsolete in a future release. Check the man page

for more information

DESCRIPTION

Use of %s is not recommended. This feature will be obsolete in a future release. Check the man page for more information

WHAT NEXT

Update your command usage as indicated in the man page.

PWR-1000 (warning) The value 'low' for option '-leakage_effort' is not supported with multiple scenarios.

DESCRIPTION

The message indicates that '-leakage_effort' with value 'low', in set_power_options command, is not supported with multiple scenarios(modes or corners). Users are recommanded to use leakage_effort high with multiple scenarios.

Although it may still work with '-leakage_effort' set to 'low', it will use current scenario for timing and leakage power calculations. To avoid excessive setup time degradation during leakage optimization set the current scenario to the worst setup scenario when using low effort.

WHAT NEXT

Change to high effort leakage optimization by setting '-leakage_effort' to 'high'.

PWR-2000 (information) Message %s has reached the maximum printing limit of %d.

DESCRIPTION

This information message occurs when a message is printed the maximum number of times. Some messages have limits on the number of times they are printed. This maintains the readability of logs. The suppression by itself does not fix any problems.

WHAT NEXT

Read the man page for the suppressed message and resolve the issue.

QTB

QTB-001 (error) There is no QTM model that is currently being defined - Please run create_qtm_model first.

DESCRIPTION

You received this message when you run any other QTM command before running *create_qtm_model* command. The QTM model creation is initiated by *create_qtm_model* command and finished by *save_qtm_model* command.

WHAT NEXT

Please start the QTM model creation by calling *create_qtm_model* command.

SEE ALSO

create_qtm_model(2), **save_qtm_model**(2),

QTB-002 (warning) QTM model with name '%s' already exists. Removing old QTM model.

DESCRIPTION

You received this message when you run *create_qtm_model* command twice with the same QTM model name. The existing QTM model is being removed and is being replaced by new QTM model.

WHAT NEXT

Please give a different name to the newly created QTM model by calling *create_qtm_model* command.

SEE ALSO

create_qtm_model(2), **save_qtm_model**(2),

QTB-003 (error) No Input Pin on cell '%s'.

DESCRIPTION

You received this message when you run *create_qtm_load_type* command with *-lib_cell* option but no *-input_pin_name* option. The QTM model creation is unable to find any input pin on the given library cell.

WHAT NEXT

Please change the library cell given in *-lib_cell* option by calling *create_qtm_load_type* command again.

SEE ALSO

create_qtm_load_type(2), **set_qtm_port_load**(2)

QTB-004 (error) No global timing found for %s command.

DESCRIPTION

You received this message when you run *create_qtm_global_parameter* command with *-lib_cell* option. The QTM model creation is unable to find any timing arc in the given library cell.

WHAT NEXT

Please change the library cell given in *-lib_cell* option by calling *create_qtm_global_parameter* command again.

SEE ALSO

create_qtm_global_parameter(2), **create_qtm_delay_arc**(2), **create_qtm_constraint_arc**(2)

QTB-005 (error) Pin Name '%s' not found.

DESCRIPTION

You received this message when you run *create_qtm_load_type* command with *-lib_cell* option and *-input_pin_name* option. This message may also be printed by *create_qtm_drive_type* and *create_qtm_path_type* commands, if they are run with pin option. The QTM model creation is unable to find any pin with given name on the

given library cell.

WHAT NEXT

Please correct the library pin name given in *-input_pin_name* option by calling *create_qtm_load_type* command again.

SEE ALSO

create_qtm_load_type(2), **set_qtm_port_load**(2)

QTB-006 (error) Drive Type '%s' not found.

DESCRIPTION

You received this message when you run *set_qtm_port_drive* command with *-type* option. The QTM model creation is unable to find any *create_qtm_drive_type* command with matching drive type.

WHAT NEXT

Please change the drive type given in *-type* option by calling *set_qtm_port_drive* command again.

SEE ALSO

create_qtm_drive_type(2), **set_qtm_port_drive**(2)

QTB-007 (error) Load Cell '%s' not found.

DESCRIPTION

You received this message when you run *create_qtm_load_type* command with *-lib_cell* option. The QTM model creation is unable to find any library cell with the given library name.

WHAT NEXT

Please change the library cell given in *-lib_cell* option by calling *create_qtm_load_type* command again.

SEE ALSO

create_qtm_load_type(2), **set_qtm_port_load**(2)

QTB-008 (error) Load Type '%s' not found.

DESCRIPTION

You received this message when you run *set_qtm_port_load* command with *-type* option. The QTM model creation is unable to find any *create_qtm_load_type* with matching load type.

WHAT NEXT

Please change the type given in *-type* option by calling *set_qtm_port_load* command.

SEE ALSO

create_qtm_load_type(2), **set_qtm_port_load**(2)

QTB-009 (error) Load value is invalid for lib pin '%s'.

DESCRIPTION

You received this message when you run *set_qtm_port_load* command with *-lib_cell* option. The QTM model creation is able to find the library pin on the library cell. But, there is no valid capacitance value at the library pin.

WHAT NEXT

Please change the library pin given in *-input_pin* option by calling *set_qtm_port_load* command.

SEE ALSO

create_qtm_load_type(2), **set_qtm_port_load**(2)

QTB-010 (error) No Drive Type specified when Value not

specified.

DESCRIPTION

You received this message when you run *set_qtm_port_drive* command with no *-type* option and no *-value* option. You must specify either of those two options.

WHAT NEXT

Please correct the *set_qtm_port_drive* command.

SEE ALSO

create_qtm_drive_type(2), **set_qtm_port_drive**(2)

QTB-011 (error) No Load Type specified with Load Factor.

DESCRIPTION

You received this message when you run *set_qtm_port_load* command with *-factor* option but no *-type* option. The QTM model creation expects both of these options to be used together.

WHAT NEXT

Please add the *-type* option by calling *set_qtm_port_load* command.

SEE ALSO

set_qtm_port_load(2)

QTB-012 (error) No delay type or value specified in create_qtm_constraint_arc command.

DESCRIPTION

You received this message when you run *create_qtm_constraint_arc* command with no *-type* option and no *-value* option. You must specify either of these two options in *create_qtm_constraint_arc* command.

WHAT NEXT

Please specify *-type* or *-value* option to *create_qtm_load_type* command.

SEE ALSO

create_qtm_constraint_arc(2)

QTB-013 (error) No global '%s' parameter defined for %s command.

DESCRIPTION

You received this message when you run *create_qtm_delay_arc* or *create_qtm_constraint_arc* command without running the corresponding *set_qtm_global_parameter* command.

The sequential delay arc requires the global parameter "clk_to_output". The setup constraint arc requires the global parameter "setup". The hold constraint arc requires the global parameter "hold".

WHAT NEXT

Please specify the global parameter calling *set_qtm_global_paraemter* command again.

SEE ALSO

create_qtm_delay_arc(2), **create_qtm_constraint_arc**(2), **set_qtm_global_parameter**(2)

QTB-014 (error) Path Type '%s' not found.

DESCRIPTION

You received this message when you run *create_qtm_constraint_arc* or *create_qtm_delay_arc* command with *-type* option. The QTM model creation is unable to find any *create_qtm_path_type* with matching path type.

WHAT NEXT

Please change the path type given in *-type* option of *create_qtm_constraint_arc* or *create_qtm_delay_arc* command. Or, please create the path type using *create_qtm_path_type* command.

SEE ALSO

create_qtm_constraint_arc(2), **create_qtm_delay_arc**(2), **create_qtm_path_type**(2)

QTB-015 (error) Failed in DB model creation for:

DESCRIPTION

You received this message when the QTM model creation is unable to create in-memory .db timing model for any QTM command. This message is followed by failing QTM command on next line. The QTM model creation has stopped abnormally.

Usually, this message will be preceded by a different message, showing the actual error message.

WHAT NEXT

Please check the error message(s) before this error to analyze the cause of this failure. Please update the QTM model appropriately.

SEE ALSO

create_qtm_model(2), **save_qtm_model**(2)

QTB-016 (error) Internal Error '%s'.

DESCRIPTION

You have received an internal debug message during ICC QTM Flow. Please report this error message along with the testcase to Synopsys.

WHAT NEXT

Please contact Synopsys for more information about this error message.

SEE ALSO

create_qtm_model(2), **save_qtm_model**(2)

QTB-017 (warning) No support for 2D table of '%d' and '%d'.

DESCRIPTION

You received this message when you run *create_qtm_constraint_arc* or *create_qtm_type_arc* command with *-type* option. The QTM model gets the delay arc from the library cell and puts that arc on the QTM model arc.

The message suggests that you are using a non-standard delay lookup table for the delay arc in the library cell.

WHAT NEXT

Please check the timing model of the library cell given in *-lib_cell* option of *create_qtm_load_type* or *create_qtm_path_type* or *create_qtm_drive_type* command.

SEE ALSO

create_qtm_load_type(2), **create_qtm_path_type**(2), **create_qtm_delay_arc**(2), **create_qtm_constraint_arc**(2)

QTB-018 (warning) Unable to get the library pin '%s' for library cell '%s'.

DESCRIPTION

You received this message when you run *create_qtm_constraint_arc* or *create_qtm_delay_arc* or *create_qtm_port_drive*command with *-lib_cell* option. The QTM model creation is unable to find any library cell pin by name on the given library cell.

WHAT NEXT

Please change the library cell or library cell given in *create_qtm_drive_type* or *create_qtm_path_type* command.

SEE ALSO

create_qtm_constraint_arc(2), **create_qtm_delay_arc**(2) **create_qtm_path_type**(2), **create_qtm_drive_type**(2)

QTB-019 (error) Arc to pin or related drive pin of port '%s' has

not been created in DB Design for create_qtm_delay_arc command.

DESCRIPTION

You received this message when you run *create_qtm_delay_arc* command. The QTM model creation is unable to find *create_qtm_port* command for the QTM port referred in *-to* option of *create_qtm_delay_arc* command.

WHAT NEXT

Please run *create_qtm_delay_arc* command before calling *create_qtm_delay_arc* command.

SEE ALSO

create_qtm_delay_arc(2), **create_qtm_port**(2)

QTB-020 (error) Design Port '%s' has not been created in before calling %s command.

DESCRIPTION

You received this message if you don't create a QTM model port, before referring to that port in a later QTM model.

WHAT NEXT

Please call *create_qtm_port* command to create the QTM model port, before calling a command which refers to that QTM model port.

SEE ALSO

create_qtm_port(2), **create_qtm_insertion_delay**(2), **set_qtm_port_drive**(2), **create_qtm_generated_clock**(2)

QTB-021 (error) Either From Pin '%s' or To Pin '%s' has not

been created in DB Design for %s command.

DESCRIPTION

You received this message when you run *create_qtm_delay_arc* or *create_qtm_constraint_arc* command with *-from* and *-to* option. The QTM model creation is unable find the ports referred in *-from* or *-to* option to be created by *create_qtm_port* command.

WHAT NEXT

Please create the missing port calling *create_qtm_port* command.

SEE ALSO

create_qtm_delay_arc(2), **create_qtm_constraint_arc**(2), **create_qtm_port**(2)

QTB-022 (error) No setup or hold flag specified in create_qtm_constraint_arc command

DESCRIPTION

You received this message when you run *create_qtm_constraint_arc* command with no *-setup* option and no *-hold* option. You must specify either of those two options.

WHAT NEXT

Please add *-setup* or *-hold* option to *create_qtm_constraint_arc* command.

SEE ALSO

create_qtm_constraint_arc(2)

QTB-023 (error) Unable to convert db lib->dc lib.

DESCRIPTION

You received this message when you run *save_qtm_model* command. The QTM model creation generates in-memory .db timing model for the QTM model. It then converts this .db timing model to a dc library. You are seeing this error message because there was an error during conversion to dc library.

WHAT NEXT

Please check any preceding error messages and rectify the reported problem(s).

SEE ALSO

save_qtm_model(2), **create_qtm_model**(2)

QTB-024 (warning) No QTM Models in Memory to Create DB Design. Please check the flow of QTM commands.

DESCRIPTION

You received this message when you run *save_qtm_model* command with no QTM models in memory.

WHAT NEXT

Please note that QTM model creation is started by *create_qtm_model* and finished by *save_qtm_model* command. Please check any preceding error messages and rectify the reported problem(s).

SEE ALSO

create_qtm_model(2), **save_qtm_model**(2)

QTB-025 (warning) Unable to get the library cell '%s' for path type '%s'.

DESCRIPTION

You received this message when you run *create_qtm_path_type* command with *-lib_cell* option. The QTM model creation is unable to find any library cell with the given library cell name.

WHAT NEXT

Please change the library cell name given in *-lib_cell* option by calling *create_qtm_path_type* command.

SEE ALSO

create_qtm_path_type(2)

QTB-026 (warning) Unable to set %s on Internal Pin Name '%s'.

DESCRIPTION

You received this message when you run *create_qtm_insertion_delay* or *create_qtm_port_load* command with port option referring to an internal QTM port. These commands are not expected to work on internal ports.

WHAT NEXT

Please change the port name in *port_list* option of *create_qtm_insertion_delay* or *create_qtm_port_load* command.

SEE ALSO

create_qtm_port_load(2), **create_qtm_insertion_delay**(2), **create_qtm_port**(2)

QTB-027 (warning) write_qtm_model has no in-memory db timing model to write to on-disk .db file.

DESCRIPTION

You received this message when you run *write_qtm_model* command with no in-memory db timing model. The QTM model creation is started by *create_qtm_model* and finished by *save_qtm_model*. The in-memory db timing model is created by *save_qtm_model*. The *write_qtm_model* command is expected to be called after *save_qtm_model* command.

WHAT NEXT

Please run *save_qtm_model* command before calling *write_qtm_model* command.

SEE ALSO

create_qtm_model(2), **save_qtm_model**(2), **write_qtm_model**(2)

QTB-028 (warning) %s command is not supported right now.

This command will be supported in later release.

DESCRIPTION

You received this message when you run *delete_qtm_constraint_arc* or *delete_qtm_delay_arc* or *get_qtm_ports* command. These QTM commands are not currently supported. These commands will be supported in later IC Compiler release.

WHAT NEXT

Please don’t use these unsupported QTM commands.

SEE ALSO

create_qtm_model(2), **save_qtm_model**(2)

QTB-029 (error) Unable to open QTM model file %s during write_qtm_model.

DESCRIPTION

You received this message when *write_qtm_model* command is unable open the text file to write out the QTM model.

WHAT NEXT

Please check the permissions of the directory given in *-out_dir* option. Please create this directory before calling *write_qtm_model* command.

SEE ALSO

write_qtm_model(2)

QTB-030 (error) The option ’%s’ cannot be used in conjunction with ’%s’.

DESCRIPTION

You received this message when you run mutually exclusive optons of a QTM command. Only one of these options is expected to be used at one time.

WHAT NEXT

Please use only one of the two options for the QTM command.

SEE ALSO

set_qtm_global_parameter(2), **set_qtm_port_load**(2), **set_qtm_port_drive**(2), **set_qtm_delay_arc**(2)

QTB-031 (error) To use option '%s', the option '%s' has to be used.

DESCRIPTION

You received this message when you run a QTM command with mutually dependent options. These two options must always be used together.

WHAT NEXT

Please change the QTM command to call both options for the QTM command.

SEE ALSO

set_qtm_global_parameter(2), **set_qtm_port_load**(2), **create_qtm_delay_arc**(2)

QTB-032 (warning) The port '%s' has already been created in the model. Replacing the original port with the new port.

DESCRIPTION

You received this message when you run *create_qtm_port* command twice with the same port name. The new port definition will replace the original port definition.

WHAT NEXT

Please check if the duplicate port name creation is expected behavior or not.

SEE ALSO

create_qtm_port(2)

QTB-033 (error) "Must specify one of '%s', or '%s' options.

DESCRIPTION

You received this message when you run a QTM command, which requires one of the two options.

WHAT NEXT

Please call this QTM command with one of the two options.

SEE ALSO

set_qtm_port_drive(2), **set_qtm_port_load**(2), **set_qtm_global_parameter**(2)

QTB-034 (error) Must specify one of '%s', '%s' or '%s' options.

DESCRIPTION

You received this message when you run a QTM command, which requires one of the three options.

WHAT NEXT

Please call this QTM command with one of the three options.

SEE ALSO

create_qtm_delay_arc(2)

QTB-035 (error) Parameter '%s' cannot be a negative number.

DESCRIPTION

You received this message when you run *create_qtm_delay_arc* or *set_qtm_technology* or *create_qtm_load_type* or *set_qtm_port_load* or *set_qtm_port_drive* command with one of the options that is not expected to take a negative number.

WHAT NEXT

Please call the QTM command with a positive number.

SEE ALSO

create_qtm_delay_arc(2), **set_qtm_technology**(2), **create_qtm_load_type**(2), **set_qtm_port_load**(2), **set_qtm_port_drive**(2)

QTB-036 (error) Unable to create internal clock '%s' on QTM model '%s' by create_qtm_clock command.

DESCRIPTION

You received this message when you run *create_qtm_clock* command with a clock name, that is the same name as the port name on the existing black box corresponding the the QTM model. This *create_qtm_clock* command is being ignored.

You cannot create a new internal clock port with the same name as existing port on the QTM model.

WHAT NEXT

Please call the *create_qtm_clock* command with a different clock name.

SEE ALSO

create_qtm_clock(2)

QTB-037 (error) -process, -voltage, and -temperature must be specified with -operating_condition.

DESCRIPTION

You received this message when you run *set_qtm_technology* command with one or more following options but not all: -operating_condition, -process, -voltage, -temperature.

These four options must be specified together.

WHAT NEXT

Please call the *set_qtm_technology* command with all four options mentioned above.

SEE ALSO

QTM-1 (error) Cannot create the QTM model '%s' before saving the existing one.

DESCRIPTION

You have tried to create a new QTM model before saving the current QTM model.

WHAT NEXT

Save the current QTM model using **save_qtm_model** and then create a a new QTM model.

QTM-2 (error) There is no QTM model that is currently being defined.

DESCRIPTION

You are using a QTM command without actually creating a QTM model.

WHAT NEXT

Use **create_qtm_model** to create a new QTM model. All QTM commands have to be between a **create_qtm_model** and **save_qtm_model** command.

QTM-3 (error) Unable to load the library '%s'

DESCRIPTION

QTM is unable to load the library you have specified. Perhaps you have not read in the library.

WHAT NEXT

Please make sure that the library is read in using the **read_db** command. QTM will not be able to auto load the library even if the library is in the search path.

QTM-4 (warning) Technology library '%s' has been already been loaded

DESCRIPTION

You have already defined the technology library. The existing technology library will be replaced with the new one.

WHAT NEXT

If you do not intend to overwrite the existing technology library please reload the existing technology library

QTM-5 (warning) The parameter '%s' has already been set to '%f', overriding with the new value.

DESCRIPTION

The global parameter has already been set, the existing value will be overridden with the new value.

WHAT NEXT

If you do not want to override the existing value of the global parameter, please set it back to the old value.

QTM-6 (warning) The parameter '%s' has already been set to '%s'; overriding with the new value.

DESCRIPTION

The global parameter has already been set, the existing one is overridden with the new value.

WHAT NEXT

If you do not want the overridden value, please replace it with the existing value.

QTM-7 (error) The option '%s' cannot be used in conjunction with '%s'

DESCRIPTION

The two options cannot be used together. Please use either one of them.

WHAT NEXT

Please use either one of the two options.

QTM-8 (error) To use option '%s', you must also use the option '%s'.

DESCRIPTION

The two options have to be used together, you cannot use one of them alone.

WHAT NEXT

Use the two options together.

QTM-9 (error) To use option '%s', a library should have been specified, but no library has been specified for this model

DESCRIPTION

You are attempting to use a lib_cell, but you have not set the technology library.

WHAT NEXT

Please set the technology library with **set_qtm_technology** with the -library option to set the technology library.

QTM-10 (warning) The path type '%s' has already been defined,

redefining the path type with the new one.

DESCRIPTION

The path type has already been defined. The existing path type definition will be replaced by the new path type definition.

WHAT NEXT

If you do not want the existing path type definition to be replaced by the new one, give unique names to the two different path types.

QTM-11 (error) The library cell '%s' is not present in the technology library you have specified.

DESCRIPTION

The specified lib_cell is not present in the technology library.

WHAT NEXT

Please provide the correct lib_cell name.

QTM-12 (error) The '%s' pin '%s' you have specified, is not present in the cell '%s'.

DESCRIPTION

The input/output pin name specified is not present in the lib_cell.

WHAT NEXT

Please provide the correct input/output pin name for the lib_cell you are using.

QTM-13 (warning) Fanout count not specified for the path type

’%s’;
using the default fanout of %d.

DESCRIPTION

You have not specified the fanout count for the path type definition. The tool uses a default count of 1.

WHAT NEXT

If you do not want to use the default fanout count (of 1), please provide the fanout count using the -fanout option.

QTM-14 (warning) The drive type ’%s’ has already been defined; redefining the drive type with the new one.

DESCRIPTION

The drive type has already been defined. The existing drive type definition will be replaced by the new drive type definition.

WHAT NEXT

If you do not want the existing drive type definition to be replaced by the new one, give unique names to the two different drive types.

QTM-15 (warning) The load type ’%s’ has already been defined; redefining the load type with the new one.

DESCRIPTION

The load type has already been defined. The existing load type definition will be replaced by the new load type definition.

WHAT NEXT

If you do not want the existing load type definition to be replaced by the new one, give unique names to the two different load types.

QTM-16 (warning) The port '%s' has already been created in the model.
Replacing the original port with the new port.

DESCRIPTION

A QTM port with the same name already exists; the original port will be replaced with the new port.

WHAT NEXT

If you want the original port direction, recreate the port.

QTM-17 (error) Must specify one of '%s', or '%s' options

DESCRIPTION

Must use either one of the two options in the command.

WHAT NEXT

Please use one of the two options in the command.

QTM-18 (error) The '%s' QTM parameter '%s' used has not been defined

DESCRIPTION

The QTM parameter you are using has not been defined. Please define the QTM parameters before using them. For e.g., if you are using a path type A in defining a timing arc, please define the path type A before using it in the timing arc.

WHAT NEXT

Please define the QTM parameters (path type, drive type, load type) before using them.

QTM-19 (error) The port '%s' used in the arc is not defined

DESCRIPTION

The port referred in the arc has not been defined.

WHAT NEXT

Please define the ports before using them in the timing arcs.

QTM-20 (error) The '%s' port for a '%s' arc must be a '%s' port , but port '%s' is of type '%s'.

DESCRIPTION

The port type for the type of arc you are defining is not of the correct type.

For a setup arc, the from port must be of type clock and the to port must be of type input/inout.

For an edge delay arc, the from port must be of type clock and the to port must be of type output/inout.

For a combinational delay arc, the from port must be of type input/inout and the to port must be of type output/inout.

WHAT NEXT

Create the arc between valid type of ports as explained above.

QTM-21 (error) The port '%s' is not a bus, but you have implied a bus structure.

DESCRIPTION

You have implied a bus structure for the port, but the port is not a bus.

WHAT NEXT

If the port is intended to be a bus, define the port to be of bus type, else use the port in a non bussed fashion.

QTM-22 (error) The bus index specified %d:%d for the bus '%s', is out of the bus array bounds %d:%d.

DESCRIPTION

The indicies used for the bus is not within the array bounds of the bus.

WHAT NEXT

Please check the array bounds of the bus and use the indicies with the array bounds.

QTM-23 (error) The arc that is an edge arc (launch) has more than one port (%d) as the from port.

DESCRIPTION

An edge delay arc can originate from a single port. In the edge delay arc you have defined, there is more than one 'from' port.

WHAT NEXT

If you want to define more than one edge delay arc to the same port, define different timing arcs, do not combine them in one.

QTM-24 (error) The global '%s' parameter has not been defined, you cannot define a '%s' arc

DESCRIPTION

Before defining setup/hold/edge delay timing arcs, the corresponding global parameter have to be defined.

Before defining setup arcs, define the global parameter, global setup time using **set_qtm_global_parameter** with -setup option.

Before defining hold arcs, define the global parameter, global hold time using **set_qtm_global_parameter** with -hold option.

Before defining edge delay arcs, define the global parameter, global clock to output time using **set_qtm_global_parameter** with -clk_to_output option.

WHAT NEXT

Define the corresponding global parameter before defining the setup/hold/edge delay arcs.

QTM-25 (error) Cannot get clock pin for the cell '%s'.

DESCRIPTION

The cell does not have a clock pin. If you are defining global setup/hold/ clk_to_output time using a lib_cell, the lib_cell should have the corresponding arc types, which means that the cell must have a clock pin too.

WHAT NEXT

Please use a lib_cell that has an arc corresponding to the global parameter you are defining.

QTM-26 (error) Cannot find a '%s' arc in the cell '%s' from the clock pin '%s'.

DESCRIPTION

If you are defining global parameter (setup/hold/clk_to_output) using lib_cell, the lib_cell must have corresponding arc. Further, if you specify the clock pin, there must be a corresponing arc from the clock pin.

WHAT NEXT

Please provide a lib_cell and a clock pin which has a timing arc corresponding to the global parameter you are defining. For example, If you are defining global setup time, the lib_cell must have a setup arc whith regard to the clock pin. If you are defining global hold time, the lib_cell must have a hold arc with regard to the clock pin. If you are defining global clk_to_output time, the lib_cell must have a clk_to_output arc originating from the clock pin.

QTM-27 (error) Cannot find the pin '%s' in the cell '%s'

DESCRIPTION

Cannot find the pin specifed in the lib_cell.

WHAT NEXT

Please check the pin name and give a valid pin name in present in the lib_cell.

QTM-28 (error) Pin '%s' is not of type '%s'

DESCRIPTION

The pin is not of the type desired.

WHAT NEXT

Provide a pin in the lib_cell which is of the type desired.

QTM-29 (error) Could not find arc of type '%s' coming %s the pin %s.

DESCRIPTION

QTM expects a timing arc to come into/go out of the specified pin. It did not find an arc of the corresponding type at the pin.

WHAT NEXT

Please specify a pin in the lib_cell to satisfy the above requirement.

QTM-30 (error) Could not find arc from clock '%s' to the output pin '%s'.

DESCRIPTION

The lib_cell does not have an edge delay arc from the clock pin to the output pin.

WHAT NEXT

Choose the clock pin and output pin such that there is an edge delay arc from the clock pin to the output pin.

QTM-31 (error) The port '%s' is not defined in the QTM model.

DESCRIPTION

The port you are referring to has not been defined in the QTM model.

WHAT NEXT

Please define the port before referring to the port.

QTM-32 (error) The port '%s' for which the drive is defined is neither an output port nor an inout port.

DESCRIPTION

Drive can be defined only on the output/inout ports.

WHAT NEXT

Please define drives only for output ports.

QTM-33 (error) The drive type '%s' used is not defined

DESCRIPTION

The drive type you have referenced has not been defined.

WHAT NEXT

Please define the drive type before refering to the drive type.

QTM-34 (error) The port '%s' for which the load is defined is not

an input port, a clock port, or an inout port.

DESCRIPTION

A load can be defined only on input/clock/inout ports, and not on output ports.

WHAT NEXT

Define the loads only on input/clock/inout ports.

QTM-35 (error) The load type '%s' used is not defined.

DESCRIPTION

The load type referenced has not been defined.

WHAT NEXT

Please define the load type first before referring to it.

QTM-36 (error) There is no pin '%s' of type %s in the cell '%s'.

DESCRIPTION

The input or output pin specified is not present.

WHAT NEXT

THe pin you specified is not present or the direction of the pin might not be right.

QTM-37 (error) No arc exists from '%s' to '%s' in the lib_cell %s.

DESCRIPTION

Could not find a combinational arc between the two specified pins.

WHAT NEXT

Please specify the pins between which there is a combinational arc.

QTM-38 (information) Path Type: %s, Cell: %s, Input Pin: %s, Output Pin: %s
Delay : %f.

DESCRIPTION

This is an informational message that provides the details of the path type defined.

WHAT NEXT

This is not an error message.

QTM-39 (information) Load Type: %s, Cell: %s, Pin: %s.

DESCRIPTION

This is an informational message which provides the details of the load type defined.

WHAT NEXT

This is an information message.

QTM-40 (information) Drive Type: %s, Cell: %s, Input Pin: %s, Output Pin: %s .

DESCRIPTION

This is an informational message which prints the details of the drive type defined.

WHAT NEXT

This is an informational message.

QTM-41 (information) Parameter: %s, Cell: %s, Clock Pin: %s, Input

Pin: %s, Constraint Value : %f.

DESCRIPTION

This informational message prints out the details of the global parameter defined.

WHAT NEXT

This is an informational message.

QTM-42 (information) Parameter: clk_to_output, Cell: %s, Clock Pin: %s, Output Pin: %s
Delay Value : %f

DESCRIPTION

This informational message prints the details of the clk_to_output parameter defined.

WHAT NEXT

This is an informational message.

QTM-43 (error) Parameter '%s' cannot be a negative number

DESCRIPTION

The parameter cannot have a negative value

WHAT NEXT

You have entered a negative for a parameter which is invalid. Please enter a value greater than 0 for the parameter

QTM-44 (error) Port '%s' not defined to be a clock

DESCRIPTION

For a constraint/clk_to_output arc, the from port must be a clock.

WHAT NEXT

Create the constraint/clk_to_output arc staring from a clock port.

QTM-45 (error) Port '%s' not of the type input/inout.

DESCRIPTION

The 'to' port of a constraint arc must be of the type input/inout. Any other port direction is illegal.

WHAT NEXT

Create the constraint arc ending in an input/inout port.

QTM-46 (error) Port '%s' not of the type output/inout.

DESCRIPTION

The 'to' port of a delay arc must be of the type output/inout.

WHAT NEXT

Create the delay arc ending in an output/inout port.

QTM-47 (error) Port '%s' not of the type input/inout.

DESCRIPTION

The 'from' port of a delay arc must be of the type input/inout.

WHAT NEXT

Create the delay arc starting from an input/inout port.

QTM-48 (warning) The port ’%s’ has invalid name.

DESCRIPTION

A QTM port with an invalid name is being created. Examples, are " ", "/".

WHAT NEXT

Check the name of the port that you are creating. If the ports are defined in a list, check the list.

QTM-49 (warning) Wire Load Model ’%s’ does not exist in the library.

Using 0 capacitance.

DESCRIPTION

The Wire Load Model specified must exist in the technology library.

WHAT NEXT

Specify a valid Wire Load Model name.

QTM-50 (error) Input transitions have already been defined for drive type ’%s’.

DESCRIPTION

The drive type you have referenced has been defined with rise and/or fall input transitions. You cannot specify the transition again for the port.

WHAT NEXT

Please define another drive type without transition specification before refering to it for this port.

QTM-51 (error) %s.

DESCRIPTION

This is a general error message due to some unexpected command options, and/or settings in creating the QTM.

WHAT NEXT

Please correct the indicated error and try again.

QTM-52 (error) Attribute '%s' for object class '%s' %s type '%s'.

DESCRIPTION

This is an error message indicating the specified attribute for the indicated QTM object class has already been defined to the given type, or it is an application reserved attribute of the specified type.

WHAT NEXT

Please correct the indicated error and try again.

QTM-53 (information) Defining new attribute '%s' of type '%s' for object class '%s'.

DESCRIPTION

This is an informational message indicating the specified attribute for the QTM object class has been successfully defined.

WHAT NEXT

No user action necessary.

QTM-54 (error) %s '%s' has not been defined.

DESCRIPTION

This is a general error message indicating the specified object has not been defined in the QTM, therefore it cannot be refered to in other commands.

WHAT NEXT

Please correct the indicated error and try again.

QTM-55 (error) No attribute named '%s' is defined for object class '%s'.

DESCRIPTION

This is an error message indicated the named attribute for the specifed object class has not been defined yet.

WHAT NEXT

Please define the attribute for the QTM object class before set it on objects.

QTM-56 (error) Attribute named '%s' for object class '%s' is not defined as type '%s'.

DESCRIPTION

This is an error message indicated the named attribute for the specifed object class has not been defined yet.

WHAT NEXT

Please define the attribute for the QTM object class before set it on objects.

QTM-57 (warning) Attribute '%s' is not defined for %s%s.

DESCRIPTION

This is a warning message indicating that the named attribute for the specifed object/class has not been defined yet.

WHAT NEXT

Please define the attribute for the QTM object class before set or remove it on objects.

QTM-58 (information) Attribute '%s' has already been set on%s'%s'
and is now replaced with the new value.

DESCRIPTION

This is an informational message indicating that the named attribute for the specifed object/class has not been re-defined, so the value is updated.

WHAT NEXT

No user action is necessary.

QTM-59 (error) The specified value '%s' does not match the defined
data type '%s'.

DESCRIPTION

This is an error message indicating the given attribute value does not match the type defined for the attribtue.

WHAT NEXT

Please correct the indicated error and try again.

QTM-60 (information) Attribute '%s' successfully removed for '%s'.

DESCRIPTION

This is an informational message indicating the specified attribute for the QTM object has been successfully removed.

WHAT NEXT

No user action necessary.

QTM-61 (error) Cannot find a proper timing arc in the specified lib cell to define the drive.

DESCRIPTION

This is an error message indicating that PrimeTime cannot find a proper delay arc in the specified cell to be used in defining the drive. There are 2 possible reasons for this: 1. the absense of a proper delay arc to be used as a driving arc. 2. there are ambiguities in deciding a specific arc that can be used to define the drive.

WHAT NEXT

If the error is caused by absense of proper timing arcs in the lib cell, please choose another lib cell with arcs providing the intended driving characteristics. If the error is caused by ambiguity, please use options such as -input_pin and -output_pin to tell PrimeTime exactly which timing arc should be used to define the drive.

QTM-62 (warning) Defining '%s' attribute on %s disables %s, %s.

DESCRIPTION

This is a general warning message. It may not be an error requiring corrective action, but it provides important information for your reference.

For example, the 'function' attribute for lib_pin, even thought QTM allows 'function' attribute be defined for ports, but it treats the boolean logic expressions as string literals, does not perform any syntax check, and only writes QTM with such attributes to .lib format, the correctness of the attributes therefore

only enforeced when compiled by LibraryCompiler.

WHAT NEXT

Please note and confirm the indicated reason/action and make any changes if necessary.

QTM-63 (error) Attribute ’%s’ for object class ’%s’ can not be defined for %s ’%s’, %s.

DESCRIPTION

This is an error message indicated the named attribute for the specifed object class is not applicable to the named object.

WHAT NEXT

Please correct the definition of the attribute for the indicated QTM object and try again.

RAIL-900 (error) %s

DESCRIPTION

Basic input error checking.

WHAT NEXT

Please re-check the command inputs and use '-help' option to verify if the input is correct.

RB

RB-1 (fatal) Rulebase name '%s' is already taken.

DESCRIPTION

This message indicates an internal Synopsys error.

WHAT_NEXT

Contact your Synopsys application engineer or the Synopsys hotline staff. Document beforehand the test case that produced the error to assist Synopsys personnel in analyzing your problem.

RB-2 (error) Rulebase divide by zero error.

DESCRIPTION

This message indicates an internal Synopsys error.

WHAT_NEXT

Contact your Synopsys application engineer or the Synopsys hotline staff. Document beforehand the test case that produced the error to assist Synopsys personnel in analyzing your problem.

RB-3 (error) Cannot insert atom '%s' in rulebase.

DESCRIPTION

This message indicates an internal Synopsys error.

WHAT_NEXT

Contact your Synopsys application engineer or the Synopsys hotline staff. Document beforehand the test case that produced the error to assist Synopsys personnel in analyzing your problem.

RB-4 (warning) Could not load rulebase utilities.

DESCRIPTION

This message indicates an internal Synopsys error.

WHAT_NEXT

Contact your Synopsys application engineer or the Synopsys hotline staff. Document beforehand the test case that produced the error to assist Synopsys personnel in analyzing your problem.

RB-5 (error) Could not open file '%s'.

DESCRIPTION

This message indicates an error in the installation of the Design Compiler (a missing rulebase file 'optimize.r') or an internal Synopsys error.

WHAT_NEXT

Contact your Synopsys application engineer or the Synopsys hotline staff. Document beforehand the test case that produced the error to assist Synopsys personnel in analyzing your problem.

RB-6 (fatal) Binary table format error.

DESCRIPTION

This message indicates that the rulebase file has been corrupted. The rulebase file is located in the installation directory *bin-'arch'/syn/auxx* and is named *optimize.r*. Make sure that this file is identical to the version shipped on your release tape. The Unix utility *diff* pinpoints any differences.

WHAT_NEXT

If the *optimize.r* file does not match the one on your tape, reinstall the file from the tape. If the *optimize.r* file appears to be identical, contact your Synopsys application engineer or the Synopsys hotline staff. Document beforehand the test case that produced the error to assist Synopsys personnel in analyzing your problem.

RB-7 (error) Cannot insert rule '%s' in rulebase.

DESCRIPTION

This message indicates an internal Synopsys error.

WHAT_NEXT

Contact your Synopsys application engineer or the Synopsys hotline staff. Document beforehand the test case that produced the error to assist Synopsys personnel in analyzing your problem.

RB-8 (error) Cannot insert class '%s' in rulebase.

DESCRIPTION

This message indicates an internal Synopsys error.

WHAT_NEXT

Contact your Synopsys application engineer or the Synopsys hotline staff. Document beforehand the test case that produced the error to assist Synopsys personnel in analyzing your problem.

RB-9 (fatal) Stream I/O error on '%s'.

DESCRIPTION

This message indicates that the rulebase file has been corrupted. The rulebase file is located in the installation directory *bin-`arch`/syn/auxx* and is named *optimize.r*. Make sure that this file is identical to the version shipped on your release tape. The Unix utility *diff* pinpoints any differences.

WHAT_NEXT

If the *optimize.r* file does not match the one on your tape, reinstall the file from the tape. If the *optimize.r* file appears to be identical, contact your Synopsys application engineer or the Synopsys hotline staff. Document beforehand the test case that produced the error to assist Synopsys personnel in analyzing your problem.

RCCALC-004 (warning) Failed to compute C-effective for the timing arc
(%s) %s/%s-->%s (%s %s)
%s
%s

DESCRIPTION

This message warns you that the cell delay calculation failed to compute the effective capacitance of the detailed RC network driven by a specific timing arc, so a lumped capacitance is being used to compute the cell delay. To ensure conservative results, the total capacitance of the RC network is used in max analysis mode, and zero capacitance in min analysis mode.

Reasons for this failure fall into three classes: library-related, parasitics-related, and design-related. Each is discussed in text that follows, along with possible soutions.

Library-Related Problems

One of the following messages is appended to this warning to explain the library-related reason for the C_effective failure:

1. "because the library data indicates a non-positive drive resistance"

This message is appended if the cell delay and/or output transition time does not increase with increasing output load capacitance. This condition can be caused by extrapolating too far outside the library table, or by problems in the table itself.

Solution: Check the timing arc on a lumped load using the **set_load** and **report_delay_calculation** commands; you might have to annotate delays and transition times until the library data can be fixed by the library vendor. Typically, extrapolations disappear when buffer trees are applied to large fanout networks.

2. "because the library data is inconsistent with a linear-driver model"

This message is appended if the parameters of the linear-driver model cannot be determined for this timing arc and/or RC network. Usually the trip-point variables have not been set correctly, or the library data is artificial. If generic_cmos library models are being used, ensure that the later slew trip-point is the same as the delay trip-point.

Solution: Double-check the settings of the RC delay-calculation thresholds using attributes or the **report_driver_model** command; if the library does not set these you will have to set the shell variables (c.f. DES-021). The attributes have the same

names as the shell variables and are annotated on the design. If the thresholds are correct, then there is a problem with the library data. If you have access to the library source, ensure that any generic_cmos library models present are used correctly (the later slew trip-point must be the same as the delay trip-point). If nonlinear delay models (a.k.a. tables) are used, confirm that the data was derived from transistor simulation with sufficient accuracy; sometimes libraries are characterized with insufficient accuracy or the data has been manually manipulated in some way. If you do not have access to the library source, then you can try as a temporary measure (i.e. until the library can be fixed) to relax DesignTime's effective-capacitance error tolerance; increase the value of the hidden shell variable **rc_ceff_delay_min_diff_ps** from its default value of 0.25 to 0.5 or greater. Please note that relaxing this error tolerance will help avoid falling-back to lumped RC delay-calculation in RCCALC-004 cases, but it will also adversely impact accuracy for those delay-calculations without RCCALC-004 messages.

Parasitics-Related Problems

One of the following messages is appended to this warning to explain the parasitics-related reason for the C_effective failure:

1. "because C_total is less than or equal to zero"

This message is appended if the total capacitance of the RC network is not positive, so that there is no way to determine an effective capacitance.

Solution: Check the network using **report_net -connections -verbose** and correct the parasitics file if necessary.

2. "because the RC network has an invalid reduced-order model"

This message is appended usually if the annotated connectivity does not match the logical connectivity; for example, if there is an unconnected pin in the design.

Solution: Look for earlier **link_design** (LNK) warnings pertaining to the problematic net. In rarer situations, there might be a non-positive resistive and/or capacitive path to ground. Check the network with **report_net -connections -verbose** and correct the parasitics file if necessary.

3. "because the RC network has an invalid pole-residue model"

This message is appended if the network has poles and residues that do not generate a converging waveform. Usually this is caused by problems in the network definition has problems.

Solution: Check the network with **report_net -connections -verbose** and correct the parasitics file if necessary. This reason applies only to pi-models (for example, RSPF and RNETs in SPEF).

Design-Related Problems

The following message is appended to this warning to explain the design-related reason for the C_effective failure:

"because the from_pin is unconnected"

This message is appended if a driving arc on a multi-driven network has an unconnected from_pin. In this case, there is no way of knowing the behavior of that arc relative to the other driving arcs of the network; this will prevent RC cell delay calculation from being performed.

Solution: Connect the from_pin or use commands **set_case_analysis** or **set_disable_timing** to fully qualify the unconnected arc.

TIMING ARC NOTATION

The timing arc is displayed by the warning message with the following six parts:

(1) 2/3-->4 (5 6)

In the above, "1" denotes the library cell name, "2" denotes the cell instance name, "3" denotes the from-pin, "4" denotes the to-pin, "5" denotes the sense direction (rising or falling), and "6" denotes the sense type and unateness.

SEE ALSO

rc_slew_lower_threshold_pct_rise (3), **rc_slew_lower_threshold_pct_fall** (3), **rc_slew_upper_threshold_pct_rise** (3), **rc_slew_upper_threshold_pct_fall** (3), **rc_input_threshold_pct_rise** (3), **rc_input_threshold_pct_fall** (3), **rc_output_threshold_pct_rise** (3), **rc_output_threshold_pct_fall** (3), **rc_slew_derate_from_library** (3), **report_net** (2), **report_delay_calculation** (2), **report_driver_model** (2), **set_annotated_transition** (2), **set_annotated_delay** (2), **set_load** (2).

RCCALC-005 (warning) Failed to compute the RC network delay
from the pin '%s'
to the pin '%s'
in the network '%s'.

DESCRIPTION

The RC network delay for the specified timing arc could not be computed. Common reasons for this are as follows:

1. Unsupported multi-drive scenarios

Support for RC networks with multiple strong drivers is currently limited to the case where all drivers are wired in parallel. Thus, if a from-pin on a driver connected to a network does not connect to a from-pin on all other drivers, DesignTime cannot perform RC delay calculation.

Solution: Directly annotate the delays and slews.

2. Networks without timing arcs

You can define networks that have only driver pins or only load pins. If no pins are bidirectional, DesignTime cannot perform RC delay calculation. You receive this warning message if you attempt to report from or to one of these pins.

3. Extremely under-driven networks

Networks that are extremely large for their drivers might not converge to one or more RC delay calculation thresholds. This sometimes occurs before layout for nets (for example, clock trees) when buffer insertion has not yet been performed.

Solution: Either adjust the RC threshold variables or directly annotate the delays and slews.

4. Incompatible voltage-swings

If the driver and load assume different voltage-swings, it is possible that the load waveform trip-point voltages are not sufficiently covered by the driver voltage-swing.

Solution: Verify whether the voltage-swing differences are valid. If so, different library trip-points must be used to ensure sufficient coverage. If the voltage-swing differences are invalid, then the design must be fixed. Another common cause of this problem is using a library without a default operating condition; when this occurs one can either fix the library or use the **set_operating_conditions** command on the affected cells.

WHAT NEXT

Check the network against the above situations and follow the suggested solutions.

SEE ALSO

rc_slew_lower_threshold_pct_rise (3), **rc_slew_lower_threshold_pct_fall** (3), **rc_slew_upper_threshold_pct_rise** (3), **rc_slew_upper_threshold_pct_fall** (3), **rc_input_threshold_pct_rise** (3), **rc_input_threshold_pct_fall** (3), **rc_output_threshold_pct_rise** (3), **rc_output_threshold_pct_fall** (3), **rc_slew_derate_from_library** (3), **set_annotated_transition** (2), **set_annotated_delay** (2), **set_operating_conditions** (2).

RCCALC-009 (warning) The drive-resistance for the timing arc (%s) %s/%s-->%s (%s %s) is much less than the network impedance to ground; DesignTime has adjusted

the drive-resistance to improve accuracy.

DESCRIPTION

DesignTime builds a driver model from library data in order to perform RC delay calculation. The driver model consists of a voltage ramp in series with a resistor; the resistor helps smooth out the voltage ramp so that the resulting driver waveform has similar curvature to that of an actual transistor driver. When the drive resistor is much less than the impedance of the network to ground, the smoothing effect is reduced, causing RC delay calculation to be potentially inaccurate. This condition can occur when a very strong driver is connected to a very resistive network. This condition does not arise out of a problem with library data.

When this condition occurs, DesignTime adjusts the drive resistance to improve accuracy; however, note that even with this adjustment the resulting accuracy might be insufficient. By default, extra pessimism is sought in min analysis mode by not using slew-degradation.

If you wish to turn-on slew degradation in min analysis mode, set the value of the shell variable **rc_degrade_min_slew_when_rd_less_than_rnet** to true.

Also by default, DesignTime will issue the RCCALC-009 message only for the subset of these conditions where net-delays are greater than driver transition times. This is because these net-delays have depended upon the portion of the driver waveform most affected by drive-resistance, namely that near and beyond the later slew trip-point.

If you wish to see the RCCALC-009 message whenever DesignTime overrides the drive-resistance (i.e. without the just-mentioned filtering), set the value of the shell variable **rc_filter_rd_less_than_rnet** to false.

With some designs you may get flooded with RCCALC-009 messages. This can occur for two reasons.

The first is that DesignTime uses a threshold parameter to determine when to override the drive-resistance, and the default value assumes well-distributed RC extraction (i.e. that very resistive nets are extracted with many RC segments). As a rule of thumb, there should not be more than 100 ohms per segment. If you are using too few RC segments, and you do not wish to increase the extraction resolution, then you can either (a) qualify DesignTime's accuracy in RCCALC-009 mode and suppress the messages with the **suppress_message** command, or (b) change the value of the shell variable **rc_rd_less_than_rnet_threshold** to optimize accuracy for your desired extraction methodology.

The second reason for getting flooded with RCCALC-009 messages is that there may just be a lot of very strong drivers connected to very resistive nets in the design. If this is so, then you can either (a) qualify DesignTime's accuracy in RCCALC-009 mode and suppress the messages, or (b) annotate delays and slews on the arcs of concern. Another, albeit seldomly possible solution is to use weaker/smaller drivers.

You can shut-off the RCCALC-009 feature completely by setting the shell variable **rc_adjust_rd_when_less_than_rnet** to false.

WHAT NEXT

Simulate the indicated timing arc with the network load to determine whether the accuracy of the DesignTime result is sufficient. Typically the number of these conditions in a design is very small, and the resulting delay calculations are overly pessimistic. You can back-annotate the simulator results with SDF, or use a weaker driver and/or less resistive network in the design.

TIMING ARC NOTATION

The timing arc is displayed by the warning message with the following six parts:

(1) 2/3-->4 (5 6)

In the above, "1" denotes the library cell name, "2" denotes the cell instance name, "3" denotes the from-pin, "4" denotes the to-pin, "5" denotes the sense direction (rising or falling), and "6" denotes the sense type and unateness.

SEE ALSO

rc_degrade_min_slew_when_rd_less_than_rnet (3), **rc_filter_rd_less_than_rnet** (3), **rc_rd_less_than_rnet_threshold** (3), **rc_adjust_rd_when_less_than_rnet** (3), **suppress_message** (2), **report_driver_model** (2), **report_delay_calculation** (2), **set_annotated_transition** (2), **set_annotated_delay** (2), **read_sdf** (2).

RCCALC-010 (warning) RC network is incomplete - load %s does not have dc_node.

DESCRIPTION

This message warns you that the accurate delay calculation cannot be done because the RC network is not complete. The specified load does not have RC node. WLM will be used for net delay calculation.

Solution: The RC network should be completed to perform delay calculation based on RC network.

SEE ALSO

RCCALC-011 (warning) An extrapolation far outside the library characterization range has been detected and the delay calculation uses the last library index incremented by %s

%S

DESCRIPTION

This message occurs when RC delay-calculation is attempted using slew or load that is much larger than the maximum library slew or load indices of a cell or a pin, or much smaller than the minimum library slew or load indices of a cell or a pin. Extrapolations can cause inaccurate and even unphysical data;

Presently this message is only issued when Composite Current-Source (CCS) driver modeling is used.

For driver slews, driver loads and receiver loads that exceed the maximum library index by more than 10%, delay calculation uses the last library index incremented by 10%, and the RC-011 message is issued.

For receiver slews that exceed the maximum library index by more than 10%, delay calculation uses the last library index incremented by 10%. For these cases,the RC-011 messages are not issued since they have minimum or no impact on timing results, if the related driver slew RC-011 messages are addressed.

For slews or loads that are below the minimum library index by more than 80%, delay calculation uses the last library index decremented by 80%, and RC-011 messages are not issued, since they have minimum or no impact on timing results.

WHAT NEXT

The timing arc and pin should be characterized with enough capacitance and slew indices to cover the design, or the design should be changed to stay within the library slew and capacitance characterization ranges.

The following guidelines can be used to address RC-011 messages

Guidelines for Characterizing Design Rule Constraints The max_transition pin attributes are normally present on the input and output pins of library cells. For input pins, the max_transition attribute value should not exceed the maximum slew index in the nonlinear delay model (NLDM) and Composite Current Source (CCS) driver and CCS receiver_capacitance2 tables. The lowest value of the maximum slew index between the NLDM and CCS tables should be used as a reference. The tables used as reference are for the rising and falling timing arcs from the relevant input pin for which the max_transition attribute is being characterized. You should take both the arc-based and pin-based tables into account. The max_capacitance pin attributes are normally present on the output pins of library cells. For output pins, the max_capacitance attribute value should not exceed the maximum load index in the NLDM and CCS driver as well as CCS receiver_capacitance1 and receiver_capacitance2 tables. You should use the lowest value of the maximum load index between the NLDM and CCS tables as a reference. The tables used as reference are for the rising and falling timing arcs to the relevant output pin for which the max_capacitance attribute is being characterized. You should take both the arc-based and pin-based tables into account.

Guidelines for Fixing RC-011 Warning Messages If the libraries used in the design follow the guidelines outlined in the Guidelines for Characterizing Design Rule Constraints section, all RC-011 messages are addressed by fixing the max_transition and max_capacitance violations reported by the report_constraint command. If the libraries are not compliant with these guidelines, you should consider RC-011 warning messages to be important. You need to address the DRCs in the design to fix these warnings.

TIMING ARC NOTATION

The timing arc/pin is displayed by the warning message with the following six parts:

(1) 2/3-->4 (5 6)

In the above, "1" denotes the library cell/pin name, "2" denotes the cell/pin instance name, "3" denotes the from-pin of a cell, "4" denotes the to-pin of a cell, "5" denotes the sense direction (min/max rising/falling), and "6" denotes the sense type and unateness.

If the timing arc is through a port with a driving cell, then the message will show the name of the port and the direction (min/max rising/falling). You can use the **report_port -drive** command to get more information about the driving cell(s) set on the port.

SEE ALSO

report_net (2), **report_delay_calculation** (2).

RCCALC-012 (warning) RC network is incomplete - net %s is unconnected.

DESCRIPTION

This message warns you that the accurate delay calculation cannot be done because the RC network is not complete. An RC network for the specified net cannot be presented by a single contiguous graph. WLM will be used for net delay calculation.

Solution: The RC network should be completed to perform delay calculation based on RC network.

SEE ALSO

RCCALC-013 (information) Reached RCCALC-004 limit -

remainder will be suppressed

DESCRIPTION

This message informs the user that the limit for RCCALC-004 messages is reached.

WHAT NEXT

This is only an information message. No action is required.

RCCALC-014 (warning) Extrapolations far outside the library characterization range have been detected during the delay calculation in the number of %lu times.

DESCRIPTION

This message occurs when RC delay-calculation is attempted using slew or load that is much larger than the maximum library slew or load indices of a cell or a pin, or much smaller than the minimum library slew or load indices of a cell or a pin (RCCALC-011 warning). Extrapolations can cause inaccurate and even unphysical data;

Presently this message is only issued when Composite Current-Source (CCS) driver modeling is used.

To see the detailed RCCALC-011 message, please use check_timing commands.

SEE ALSO

check_timing , **RCCALC-011.**

RCEX-001 (error) The default conversion factor was not specified in the physical library (.pdb) file.

DESCRIPTION

This error occurs because you did not specify the conversion factor in the The conversion factor converts placement units to and from microns. Without it, the tool is not able to interpret the cell information in the library.

WHAT NEXT

Ask your library vendor to provide you with a Library Exchange Format (LEF) file with the conversion factor present. Use **lef2plib** command to the convert the LEF file to a .plib file. Use the **read_lib** command to convert the .plib file to a .pdb file and read it into the tool. Once the library is read in, use the **write_lib** command to create the physical library database.

SEE ALSO

lef2plib(1)
read_lib(2)
write_lib(2)

RCEX-002 (error) No routable layer information was found in the physical library (.pdb) file.

DESCRIPTION

This error occurs because your physical library does not contain routable layer information that is necessary for the interpretation of library cell and routing information.

WHAT NEXT

Ask your library vendor to provide you with a Library Exchange Format (LEF) file with the routable layer information present. Use the **lef2plib** command to convert the LEF file to a .plib file. Use the **read_lib** command to convert the .plib file to a .pdb file and read it into the tool. Once the library is read in, use the **write_lib** command to create the physical library database.

SEE ALSO

lef2plib(1)
read_lib(2)
write_lib(2)

RCEX-003 (error) The layer width for '%s' is either missing or illegal in the physical (.pdb) file.

DESCRIPTION

This error occurs because your physical library does not contain layer width information that is a mandatory parameter needed for RC computation and extraction and of crucial importance in determining route capacitances.

WHAT NEXT

Ask your library vendor to provide you with a Library Exchange Format (LEF) file with the layer width information present. Use the **lef2plib** command to convert the LEF file to a .plib file. Use the **read_lib** command to convert the .plib file to a .pdb file and read it into the tool. Once the library is read in, use the **write_lib** command to create the physical library database.

SEE ALSO

lef2plib(1)
read_lib(2)
write_lib(2)

RCEX-004 (error) The layer resistance for '%s' was not found in the physical (PDB) file.

DESCRIPTION

You receive this error message because your physical library does not contain layer resistance information, a mandatory parameter needed for RC computation and extraction that is crucial in determining route resistance.

WHAT NEXT

Please ask your library vendor to provide you with a LEF library file with the layer resistance information present. You can then convert the LEF to PLIB using the **lef2plib** command. Convert the PLIB file to a PDB by reading it into Physical Compiler or Design Compiler using the **read_lib** command. Once the library is read in,

issue the **write_lib** command to create the PDB.

SEE ALSO

lef2plib (1); **read_lib** (2), **write_lib** (2).

RCEX-005 (error) The preferred layer direction for '%s' was not found in the physical (.pdb) file.

DESCRIPTION

This error occurs because your physical library does not contain the preferred direction parameter. This information is crucial for RC computation and extraction and to help calculate resistive and capacitive components for routes.

WHAT NEXT

Ask your library vendor to provide you with a Library Exchange Format (LEF) file with the layer preferred direction information present. Use the **lef2plib** command to convert the LEF file to a .plib file. Use the **read_lib** command to convert the .plib file to a .pdb file and read it into the tool. Once the library is read in, use the **write_lib** command to create the physical library database.

SEE ALSO

lef2plib(1)
read_lib(2)
write_lib(2)

RCEX-006 (error) The layer pitch for '%s' was not found in the physical (.pdb) file.

DESCRIPTION

This error occurs because your physical library does not contain layer pitch information that is needed for RC computation and extraction to help calculate resistive and capacitive components for routes.

WHAT NEXT

Ask your library vendor to provide you with a Library Exchange Format (LEF) file with the layer pitch information present. Use the **lef2plib** command to convert the LEF file to a .plib file. Use the **read_lib** command to convert the .plib file to a

.pdb file and read it into the tool. Once the library is read in, use the **write_lib** command to create the physical library database.

SEE ALSO

lef2plib(1)
read_lib(2)
write_lib(2)

RCEX-007 (info) The distance unit in Capacitance and Resistance is %s micron.

DESCRIPTION

You receive this message because it provides information on the type of units in use. The unit used for capacitance is library capacitance units per micron. The unit used for resistance is library resistance units per micron.

WHAT NEXT

No action is necessary. The result is informative.

RCEX-008 (information) Using derived R and C coefficients.

DESCRIPTION

You receive this message to inform you that the capacitance and resistance values used for the horizontal and vertical routing layers are derived from the physical library.

WHAT NEXT

This is an informational message only. No action is required on your part.

RCEX-009 (info) %s is scaled by %5.2f

DESCRIPTION

You receive this message because it provides information on the type of scaling in use. They are the scale factors specified in Milkyway technology file.

WHAT NEXT

No action is necessary. The result is informative.

SEE ALSO

set_delay_estimation_options (2), **set_extraction_options** (2)

RCEX-010 (error) All nets are unrouted or skipped. Extraction cannot be done.

DESCRIPTION

You receive this message because your design does not have any routes defined, therefore, extraction cannot proceed. The problem is with the input database you read in. If you have routes in the input database, most likely an error occurred that prevented them from being read in.

WHAT NEXT

Use the **write_pdef** command to confirm that routes are present. If routes are present, look into error messages from the **extract_rc** command or the **read_pdef** command.

SEE ALSO

extract_rc (2), **read_pdef** (2), **write_pdef** (2).

RCEX-011 (information) %s : %.2g %.2g

DESCRIPTION

This message displays the library-derived min and max values for one of the RC coefficients used to calculate net capacitance and resistance. These coefficients include resistance and capacitance for each metal layer, average resistance and capacitance across all horizontal and vertical layers, and via resistance.

WHAT NEXT

This is an informational message only. No action is required on your part.

RCEX-012 (information) %s used : %.2g %.2g

DESCRIPTION

You receive this message to inform you of the value for the vertical or horizontal, capacitance or resistance coefficient used for delay estimation. Delay estimation is used in placement and routing estimation. The numbers displayed are the max and min values.

WHAT NEXT

This is an informational message only. No action is required on your part.

RCEX-013 (information) Using region-based R and C coefficients.

DESCRIPTION

You receive this message to inform you that the value is derived from the region for vertical and horizontal, capacitance and resistance coefficients used for delay calculation during placement and routing estimation.

If you explicitly specify the RC coefficients using **set_delay_estimation_options**, you will not see this message. Similarily, if you use 1D parameters, and specify weight for every metal layer, you will not see this message either.

WHAT NEXT

This is an informational message only. No action is required on your part.

RCEX-014 (information) %d region specific RC values are found.

DESCRIPTION

You receive this message to inform you the number of region specific RC values in the design.

WHAT NEXT

This is an informational message only. No action is required on your part.

RCEX-015 (information) The RC model used is %s.

DESCRIPTION

This message advises you of the RC model that the tool will use to compute the unit RC.

The valid RC models and their descriptions are shown below, starting with the highest priority and ending with the lowest priority.

• User - The model is based on user-specified RC parameters.

• TLUPlus - The model is based on TLUPlus parameters.

• TLU - The model is based on TLU parameters in Milkyway.

• Library extractor based - The model is based on extraction parameters.

• 2.5D - The model is based on 2.5D parameters and the user-specified routing wire model.

• Library 2.5D - The model is based on 2.5D parameters.

• Library 1D - The model is based on 1D parameters

WHAT NEXT

This is only an informational message. No action is required.

SEE ALSO

extract2plib(1)
set_delay_estimation_options(2)
set_routing_wire_model(2)
set_tlu_plus_files(2)

RCEX-016 (information) The routing wire model used is : %s

DESCRIPTION

This message advises you of which routing wire model the tool will use to compute the unit RC.

WHAT NEXT

This is only an informational message. No action is required.

SEE ALSO

set_routing_wire_model(2)
RCEX-15(n)

RCEX-017 (information) Use %s layer weight : %g %g

DESCRIPTION

This message informs you which layer weight and value is used. The numbers displayed are the max and min values.

WHAT NEXT

This is an informational message only. No action is required on your part.

RCEX-018 (warning) Inconsistent library data found for layer %s.

DESCRIPTION

This warning occurs because the library data for the specified layer is inconsistent. For example, you receive this message if the pitch is less than the width plus the spacing. The tool will continue to execute, assuming that the real pitch is the width plus the spacing. This will not impact congestion computation.

WHAT_NEXT

Check the library data for possible problems. Fix the library resistance and capacitance inconsistency problem, and regenerate the physical library.

RCEX-019 (information) Layer %s is ignored for resistance and capacitance computation.

DESCRIPTION

This message advises you that the tool will exclude this layer from resistance and capacitance computation. You can use the **set_ignored_layers** command to request the excluding of specific layers.

WHAT NEXT

This is only an informational message. No action is required.

SEE ALSO

set_ignored_layers(2)
RCEX-011(n)

RCEX-020 (Warning) Net '%s' is exceeding threshold (over %d pins) and will be skipped.

DESCRIPTION

This net has a very large number of pins so it will not be extracted. This net was probably not meant to be detail routed. There will be no parasitics and no back-annotated delay computed for this net. Timing analysis will use the wire load model with the high fanout threshold assumptions. The current default for the max number of pins is 1000. You can use command **set_extraction_options** to adjust it.

WHAT NEXT

Buffer this net and detail route it to be able to extract it.

SEE ALSO

extract_rc (2), **set_extraction_options** (2).

RCEX-021 (warning) Net '%s' is ideal and will be skipped.

DESCRIPTION

This warning message occurs when the specified ideal net is not considered for extraction. The ideal net is not extracted or considered when extracting the capacitance for any other nets. The **extract_ideal_nets** variable can be used to override this behavior.

WHAT NEXT

This is only a warning message.

If you want the extractor to process the ideal nets, set the **extract_ideal_nets** variable to **true** and run the command again. By default, the variable is set to **false**.

SEE ALSO

extract_rc(2)
extract_ideal_nets(3)

RCEX-022 (information) Using pre-route resistance and capacitance estimation during extraction.

DESCRIPTION

This message advises you that the tool performs extraction based on a pre-route estimation method for resistance and capacitance computation, instead of actually extracting the resistance and capacitance values.

The tool needs specific information to perform extraction, such as the process parameters. If any of the required parameters are missing, the tool cannot successfully extract resistance and capacitance, so it uses a pre-route estimation method to compute the resistance and capacitance values.

See the user manual for required parameters to perform extraction. See the **RCEX-015** error message for the pre-route estimation model used.

WHAT NEXT

This is only an informational message. No action is required.

SEE ALSO

extract_rc(2)
RCEX-011(n)
RCEX-015(n)

RCEX-023 (information) %s parasitic extraction.

DESCRIPTION

This message advises you that the tool is performing parasitic extraction.

WHAT NEXT

This is only an informational message. No action is required.

SEE ALSO

extract_rc(2)

RCEX-024 (warning) Incorrect TLU+ tech file '%s' specified.

DESCRIPTION

This warning occurs because the specified TLUPlus technology file is missing, cannot be opened, or is not in the correct format. As a result, the tool does not use TLUPlus to perform resistance and capacitance computation. Instead, the tool uses another resistance and capacitance computation method available in the physical library. See the **RCEX-015** error message for the computation method used.

WHAT NEXT

Ensure that the path to the TLUPlus technology file is correctly specified and that the file permission is correctly set. See the user manual for information on how to prepare a TLUPlus technology file.

SEE ALSO

extract_rc(2)
RCEX-015(n)

RCEX-025 (warning) Incorrect ITF TLUPlus technology files specified: %s.

DESCRIPTION

This warning message occurs because the specified Interconnect Technology Format (ITF) TLUPlus files are incorrect. The tool cannot use the specified files for the reason shown in the message.

The ITF TLUPlus technology files are output from the **grdgenxo** command (for the maximum or the minimum operating condition) and from the mapping file that maps the Synopsys physical library format (.plib layer name to the ITF mask layer name. As a result, the tool does not use TLUPlus to perform resistance and capacitance computation.

WHAT NEXT

Examine the ITF TLUPlus technology file and mapping file. Common mistakes include missing resistance values in ITF, missing via definitions in ITF, and incorrect layer names in the mapping file.

It is a good practice to ensure that the path to the ITF TLUPlus technology files is

correctly specified and verify that the file permission is correctly set.

See the user manual for details about preparing ITF TLUPlus technology files.

SEE ALSO

extract_rc(2)
RCEX-015(n)

RCEX-026 (warning) Incorrect mapping file '%s' specified. %s.

DESCRIPTION

This warning message occurs because the specified mapping file does not contain the information necessary to perform layer mapping due to the reason shown in the message. As a result, the tool does not use table lookup plus (TLUPlus) to perform resistance and capacitance computation. Instead, the tool uses other resistance and capacitance computation methods available in the technology library. See the **RCEX-015** error message for the computation method used.

The mapping file is necessary to map the technology library layer names to Interconnect Technology Format (ITF) layer names. It should at least contain the conducting_layers and via_layers sections. The conducting_layers section maps a routing_layer in the technology library to a conductor layer in ITF. The via_layers section maps a contact layer in the technology library to a via layer in ITF.

For example, given that you have the following information in your physical library:

```
   routing_layer ( "METAL1" ) {
   ...
   }
contact_layer ( "VIA1" );
```

and given that you have the following information in your ITF file:

```
CONDUCTOR metal1 {THICKNESS=0.53 WMIN=0.23 SMIN=0.23
   RPSQ=0.078 CAPACITIVE_ONLY_ETCH=0}
VIA via1 { FROM=metal1  TO=metal2 AREA=0.0169 RPV=1.6 }
```

Your mapping file should look like the following:

```
   conducting_layers
   METAL1 metal1
via_layers
 VIA1 via1
```

WHAT NEXT

Correct the reported error, and examine the mapping file to see whether it correctly maps the technology library layer names to ITF layer names.

See the user manual for information about preparing a correct mapping file.

SEE ALSO

extract_rc(2)
set_tlu_plus_files(2)
RCEX-015(n)

RCEX-027 (warning) Design is not global routed, use detail route extraction.

DESCRIPTION

This warning message occurs when global route is not performed for the design, so global route extraction cannot be done. Instead, detail route extraction is performed for this design.

WHAT NEXT

This is only a warning message.

If the result is not what you intended and you want global route extraction, rererun global route for this design.

SEE ALSO

extract_rc(2)
RCEX-015(n)

RCEX-028 (warning) Poly layer %s is defined as routable layer.

DESCRIPTION

This warning message occurs when a poly layer in your physical library is also defined as a routable layer. Since poly layers usually have higher resistance value, defining poly layers as routable could skew your average resistance computation.

WHAT NEXT

If the result is not what you intended and you dont want poly layers to be defined as routable layer, please make the correction to your physical library. Otherwise, you can discard this warning message.

SEE ALSO

extract-rc (2)

RCEX-029 (information) Running post route extraction in a separate process.

DESCRIPTION

This information message advises you that the post route extraction will run in a separate process. This is only valid with post route extraction using TLU or TLUPlus.

WHAT_NEXT

This is an information message only. No action is required.

SEE ALSO

physopt_enable_tlu_plus_process(3)

RCEX-030 (error) Initialization of the %s RC model failed.

DESCRIPTION

This error occurs because the tool fails to initialize the specified resistance and capacitance model.

The tool supports many RC models and each one requires specific parameters to be properly initialized. If none of the required parameters are present for an RC model, the tool ignores the initialization of the RC model and moves on to initialize the next available RC model. However, if some of the required parameters exist, the tool considers the RC model to be the desired one. This error message is the result of failing to initialize this RC model.

The following list shows each RC model and the condition that, once satisfied, causes the tool to consider it to be the RC model:

• User - Resistance and capacitance for horizontal and vertical directions

• TLUPlus - Specifies the **set_tlu_plus_files** or **create_mw_design** command with TLUPlus

• TLU - Milkyway is with TLU

• Library extractor based - Any extraction parameter, such as oxide thickness/ permittivity.

• 2.5D - Any 2.5D parameter (such as plate_cap), and a user-specified routing wire model

• Library 2.5D - Any 2.5D parameter (such as plate_cap)

• Library 1D - area_per_sq or res_per_sq

For example, if you use TLUPlus you can use the **set_tlu_plus_files** command to specify a TLUPlus technology file from the output of the **grdgenxo** command and a mapping file that maps the layer names between the physical library and the Interconnect Technology File (ITF). If you do not specify these files, the tool ignores TLUPlus and attempts to initialize other RC models.

However, if you use the **set_tlu_plus_files** command, the tool considers the TLUPlus RC model to be your desired RC model. This error message is the result of failing to initialize TLUPlus due to errors such as specifying an incorrect mapping file.

WHAT NEXT

Determine whether the RC model is your desired RC model. If not, remove all references to it in your physical library and/or script. The tool then ignores this RC model and initializes another available RC model.

If this is your desired RC model, check the error messages associated with the initialization of this RC model. Make appropriate changes to your physical library and/or script, and execute the command again.

SEE ALSO

extract2plib(1)
grdgenxo(1)
lef2plib(1)
create_mw_design(2)
set_tlu_plus_files(2)
RCEX-015(n)

RCEX-031 (information) Compact PV is saved to PARA view.

DESCRIPTION

This message advises you that the tool has saved the compact PV to PARA view.

Compact PV is a binary parasitic file that is attached to PARA view. The tool creates this attachment file during execution of the **extract_rc** command if the following conditions are all true.

- You are using the **extract_rc** command for post-route extraction.
- You are using the TLUPlus model.
- You are using the **read_milkyway** command to read the design.

Each time you run the **extract_rc** command, a new version of compact PV is attached to the PARA view.

WHAT NEXT

This is only an informational message. No action is required.

SEE ALSO

extract_rc(2)
read_milkyway(2)
set_tlu_plus_files(2)
RCEX-015(n)

RCEX-032 (error) Cannot write out parasitic files from an unextracted design.

DESCRIPTION

This error message occurs when using the **write_parasitics** command to write out parasitic files from a design that is not extracted. The design must be extracted with the **extract_rc** command before you can use **write_parasitics** to write out parasitic files.

WHAT NEXT

Read in a routed design, run **extract_rc**, and then run the **write_parasitics** command.

SEE ALSO

extract_rc(2)
write_parasitics(2)

RCEX-033 (error) Cannot write out COMPACT format without

TLUPlus.

DESCRIPTION

This error message occurs when using the **write_parasitics** command to write out parasitic files, on a design that does not use TLUPlus as the RC model.

WHAT NEXT

Set up the design to use TLUPlus or use another parasitic format and then run the command again.

SEE ALSO

extract_rc(2)
write_parasitics(2)
RCEX-015(n)

RCEX-034 (error) Cannot read in COMPACT format without TLUPlus.

DESCRIPTION

This error message occurs when using the **read_parasitics** command to read in parasitic files, and the design does not use TLUPlus as the RC model.

WHAT NEXT

Set up the design to use TLUPlus or use another parasitic format and then run the command again.

SEE ALSO

extract_rc(2)
read_parasitics(2)
RCEX-015(n)

RCEX-035 (information) Writing %s parasitics to file '%s'.

DESCRIPTION

The command **write_parasitics** is writing a parasitics file to disk. Check the **write_parasitics** man page for information on how to use the command. Use the **write**

command to write a netlist for the current design before using the **write_parasitics** command. This is because **write** can change names and the new names should appear in the parasitics file as well. This message indicates the disk location of the parasitics file created with **write_parasitics**.

WHAT NEXT

This is an informational message only. The parasitics file can be used in layout tools or other tools reading **write_parasitics** file formats.

SEE ALSO

extract_rc (2) ***RCEX-015*** (n)

RCEX-036 (Error) Writing parasitics file failed.

DESCRIPTION

The command **write_parasitics** fails to write parasitics file to disk. Check the **write_parasitics** man page for information on how to use the command.

WHAT NEXT

Check whether you have enough disk space for writing out the parasitic file.

SEE ALSO

extract_rc (2)

RCEX-037 (information) Reading %s parasitics from file '%s'.

DESCRIPTION

The command **read_parasitics** is reading a parasitics file from disk. Check the **read_parasitics** man page for information on how to use the command. This message indicates the disk location of the parasitics file created with **read_parasitics**.

WHAT NEXT

This is an informational message only.

SEE ALSO

extract_rc (2) ***RCEX-015*** (n)

RCEX-038 (Error) Reading parasitics file failed.

DESCRIPTION

The command **read_parasitics** fails to read a parasitics file from disk. Check the **read_parasitics** man page for information on how to use the command.

WHAT NEXT

Check whether the parasitic file is corrupted.

SEE ALSO

extract_rc (2)

RCEX-039 (warning) Running SI flow without coupling capacitances.

DESCRIPTION

When SI flow is enabled by **set_si_options**, coupling capacitances need to be explicitly extracted. By default, **extract_rc** and **read_parasitics** lump all coupling capacitances to ground. This warning message occurs when SI flow is enabled but coupling capacitances are still lumped to ground.

WHAT NEXT

You can eliminate this warning message by explicitly creating coupling capacitances instead of lumping them to ground. Please consult the appropriate man pages for the command that you are running to see how to enable this.

If your intention is to run SI flow without explicitly creating coupling capacitances, you can ignore this warning message.

SEE ALSO

set_si_options(2)
extract_rc(2)
read_parasitics(2)
RCEX-044(n)

RCEX-040 (information) Parasitic source is %s.

DESCRIPTION

This information message advises you of the source of the layer parasitic extraction. The values are as follows:

- LPE - layer parasitic extraction done by internal extractor
- PARA - parasitic is read in from compact PARA view
- COMPACT - parasitic is read in from compact file
- SBPF - parasitic is read in from a SBPF file
- SPEF - parasitic is read in from a SPEF file

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

extract_rc(2)
RCEX-015(n)

RCEX-041 (information) Parasitic mode is %s.

DESCRIPTION

This information message advises you of the mode of the layer parasitic extraction. The values are as follows:

- VirtualRC - using virtual resistance and capacitance
- RealRVirtualC - using real resistance and virtual capacitance
- RealRC - using real resistance and capacitance

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

extract_rc(2)
RCEX-015(n)

RCEX-042 (information) Extraction mode is %s.

DESCRIPTION

This information message advises you of the extraction mode. The values are as follows:

- MAX - only the max corner is extracted
- MIN_MAX - both the min and the max corners are extracted

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

extract_rc(2)
RCEX-015(n)

RCEX-043 (information) Extraction derate is %s.

DESCRIPTION

This information message advises you of the temperature derating used in extraction. It consists of three numbers that indicate the minimum temperature, the base temperature, and the maximum temperature. For example, an extraction derate value of -40/25/100 means the minimum temperature is -40 degrees, the base temperature is 25 degrees, and maximum temperature is 100 degrees.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

extract_rc(2)
RCEX-015(n)

RCEX-044 (information) Coupling capacitances are %s.

DESCRIPTION

This message advises you of the action that the tool takes for coupling capacitances during parasitic extraction. Coupling capacitances can either be lumped to ground or explicitly extracted. By default, the **extract_rc** command lumps all coupling capacitances to ground. However, if you use **extract_rc** with the **-coupling_cap** option (switch), the tool explicitly extracts coupling capacitances. Note that runtime and memory overhead occurs if coupling capacitances must be explicitly extracted.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

extract_rc(2)
RCEX-015(n)

RCEX-045 (error) Cannot read PARA view from Milkyway.

DESCRIPTION

This error message occurs when using the **read_parasitics** command to read in PARA view from Milkyway.

WHAT NEXT

Check whether PARA exists in the Milkway, and if PARA view does not exist, you can use **write_parasitics** command to create one.

Please note we cannot read in PARA view created by StarRCXT, and we cannot read in PARA view created by Astro with mesh coupling cap.

SEE ALSO

extract_rc(2)
read_parasitics(2)

RCEX-046 (error) Loading an attached TLUPlus File.

DESCRIPTION

You receive this warning message because you are using a TLUPlus file that has been attached to the Milkyway. The recommended usage is to use **set_tlu_plus_files** command.

WHAT NEXT

Use **set_tlu_plus_files** command to specify the TLUPlus file for **IC Compiler**.

SEE ALSO

set_tlu_plus_files(2)
extract_rc(2)

RCEX-047 (warning) Not enough nets are routed (%s); will do extraction by using placement congestion map as background.

DESCRIPTION

This warning message occurs when there are not enough routed nets in design when **extract_rc** is called. Extractor will honor the routed nets topology doing the R, C calculation. Since there is no complete aggressors information, extractor is using placement congestion map as aggressor information. Unrouted nets will still be estimated only.

WHAT NEXT

This warning message reflects the design has route(s) but the number of nets routed are less than 2/3 of the nets in the design. Extraction will use placement congestion map as neighboring information (background). When you have enough nets routed later, you will not see this warning message.

SEE ALSO

extract_rc(2)
RCEX-010(n)
RCEX-022(n)

RCEX-048 (warning) Failed to load resistance from TLUPlus.

The tool is continuing with resistance from the physical library.

DESCRIPTION

This warning occurs because of an error in loading the resistance portion of the TLUPlus file specified by the **set_tlu_plus_files** command. The tool is unable to load resistance information from TLUPlus. Instead, the tool uses resistance information from your physical library. This includes resistance for metal layers and resistance for vias.

The tool still uses the capacitance portion of TLUPlus.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by using a newer version of the **grdgenxo** command to regenerate TLUPlus.

SEE ALSO

grdgenxo(1)
set_tlu_plus_files(2)

RCEX-049 (Warning) TLU+ only supports one operating condition for process scaling.

DESCRIPTION

TLU+ (table lookup plus) mode supports only one operating condition for process scaling. If you specify different process scaling values for both minimum and maximum operating conditions, the lower (minimum) of the two conditions is applied to both operating conditions.

In the following example, 0.3 is used as the process scaling for both the minimum and maximum operating conditions during TLU+ based extraction.

```
set_extraction_options -max_process_scale 0.4 -min_process_scale 0.3
```

WHAT NEXT

Use the same process scaling value for both the minimum and maximum operating conditions. Model the difference in the minimum and maximum operating conditions using different extraction parameters.

SEE ALSO

set_extraction_options (2).

RCEX-050 (information) The process parameters are scaled by %g %g.

DESCRIPTION

You receive this information to let you know that the process parameters defined in your physical library will be scaled. The two numbers displayed are the process scaling factors for the max and min operating conditions. You can use **set_extraction_options** command to specify the scaling factors, or you can specify the scaling factors in your physical library. The command line scaling factors have higher priority than the values in your physical library.

WHAT NEXT

This is an informational message only.

SEE ALSO

set_extraction_options (2); **report_extraction_options** (2), **RCEX-015**

RCEX-051 (warning) The field oxide thickness was not found in the physical (.pdb) file. The tool is using '%f' for the field oxide thickness.

DESCRIPTION

This warning occurs because your physical library does not contain field oxide thickness information, which is needed for extraction to help calculate capacitive components for routes. If the field oxide thickness is not present in the Synopsys physical database format (.pdb) file, then the value for the TSMC 0.18 micron technology is used.

WHAT NEXT

Ask your library vendor to provide you with a Library Exchange Format (LEF) library file with the field oxide thickness information present. Then use the **lef2plib** command to convert the LEF file to a .plib file, or use the **extract2plib** command to convert the extraction process file. Use the **read_lib** command to convert the .plib file to a .pdb file and read it into the tool. Once the library is read in, use the **write_lib** command to create the physical library database.

SEE ALSO

extract2plib(1)

lef2plib(1)
read_lib(2)
write_lib(2)

RCEX-052 (warning) The field oxide permitivity was not found in the physical (.pdb) file. The tool is using '%f' for the field oxide permitivity.

DESCRIPTION

This warning occurs because your physical library does not contain field oxide permitivity information that is required for extraction to help calculate capacitive components for routes. If the field oxide permitivity information is not present in the (.pdb) file, the value for the TSMC 0.18 micron technology is used.

WHAT NEXT

Ask your library vendor to provide you with a Library Exchange Format (LEF) library file with the field oxide permitivity present. Then use the **lef2plib** command to convert the LEF file to a .plib file, or use the **extract2plib** command to convert the extraction process file. Use the **read_lib** command to convert the .plib file to a .pdb file and read it into the tool. Once the library is read in, use the **write_lib** command to create the physical library database.

SEE ALSO

extract2plib(1)
lef2plib(1)
read_lib(2)
write_lib(2)

RCEX-053 (warning) No layer spacing was found for '%s' in the physical (.pdb) file. The tool is using '%d micron' for the layer spacing.

DESCRIPTION

This warning occurs because your physical library does not contain layer spacing information that is required for extraction to help calculate resistive and capacitive components for routes. The layer spacing to be used is the minimum of the normal spacing and the width-based spacing for the layer. If you did not define either of these measurements, the spacing for the TSMC 0.18 micron technology is used.

WHAT NEXT

Ask your library vendor to provide you with a Library Exchange Format (LEF) library file with the layer spacing present. Then use the **lef2plib** command to convert the LEF file to a .plib file, or use the **extract2plib** command to convert the extraction process file. Use the **read_lib** command to convert the .plib file to a .pdb file and read it into the tool. Once the library is read in, use the **write_lib** command to create the physical library database.

SEE ALSO

extract2plib(1)
lef2plib(1)
read_lib(2)
write_lib(2)

RCEX-054 (warning) No layer thickness was found for '%s' in the physical (.pdb) file. The tool is using '%f micron' for the layer thickness.

DESCRIPTION

This warning occurs because your physical library does not contain layer thickness information that is required for extraction to help calculate capacitive components for routes. If you did not define this measurement, then the layer thickness for the TSMC 0.18 micron technology is used.

WHAT NEXT

Ask your library vendor to provide you with a Library Exchange Format (LEF) library file with the layer thickness present. Then use the **lef2plib** command to convert the LEF file to a .plib file, or use the **extract2plib** command to convert the extraction process file. Use the **read_lib** command to convert the .plib file to a .pdb file and read it into the tool. Once the library is read in, use the **write_lib** command to create the physical library database.

SEE ALSO

extract2plib(1)
lef2plib(1)
read_lib(2)
write_lib(2)

RCEX-055 (warning) No layer lateral oxide thickness was found for '%s' in the physical (.pdb) file. The tool is using '%f micron'

for the layer lateral oxide thickness.

DESCRIPTION

This warning occurs because your physical library does not contain layer lateral oxide thickness information that is required for extraction to help calculate capacitive components for routes. If the value is not present in your physical library, then the layer lateral oxide thickness for the TSMC 0.18 micron technology is used.

WHAT NEXT

Ask your library vendor to provide you with a Library Exchange Format (LEF) library file with the layer lateral oxide thickness present. Then use the **lef2plib** command to convert the LEF file to a .plib file, or use the **extract2plib** command to convert the extraction process file. Use the **read_lib** command to convert the .plib file to a .pdb file and read it into the tool. Once the library is read in, use the **write_lib** command to create the physical library database.

SEE ALSO

extract2plib(1)
lef2plib(1)
read_lib(2)
write_lib(2)

RCEX-056 (warning) No layer lateral oxide permitivity was found for '%s' in the physical (.pdb) file. The tool is using '%f' for the layer lateral oxide permitivity.

DESCRIPTION

This warning occurs because your physical library does not contain layer lateral oxide permitivity information that is required for extraction to help calculate capacitive components for routes. If you did not define this value, then the layer lateral oxide permitivity for the TSMC 0.18 micron technology is used.

WHAT NEXT

Ask your library vendor to provide you with a Library Exchange Format (LEF) library file with the layer lateral oxide permitivity present. Then use the **lef2plib** command to convert the LEF file to a .plib file, or use the **extract2plib** command to convert the extraction process file. Use the **read_lib** command to convert the .plib file to a .pdb file and read it into the tool. Once the library is read in, use the **write_lib** command to create the physical library database.

SEE ALSO

extract2plib(1)
lef2plib(1)
read_lib(2)
write_lib(2)

RCEX-057 (warning) No layer oxide thickness was found for '%s' in the physical (.pdb) file. Using '%f micron' for the layer oxide thickness.

DESCRIPTION

This warning occurs because your physical library does not contain layer oxide thickness information that is required for extraction to help calculate capacitive components for routes. If you did not define this value, then the layer oxide thickness for the TSMC 0.18 micron technology is used.

WHAT NEXT

Ask your library vendor to provide you with a Library Exchange Format (LEF) library file with the layer oxide thickness present. Then use the **lef2plib** command to convert the LEF file to a .plib file, or use the **extract2plib** command to convert the extraction process file. Use the **read_lib** command to convert the .plib file to a .pdb file and read it into the tool. Once the library is read in, use the **write_lib** command to create the physical library database.

SEE ALSO

extract2plib(1)
lef2plib(1)
read_lib(2)
write_lib(2)

RCEX-058 (warning) No layer oxide permitivity was found for '%s' in the physical (.pdb) file. Using '%f' for the layer oxide permitivity.

DESCRIPTION

This warning occurs because your physical library does not contain layer oxide permitivity information that is required for extraction to help calculate capacitive components for routes. If you did not define this value, then the layer oxide permitivity for the TSMC 0.18 micron technology is used.

WHAT NEXT

Ask your library vendor to provide you with a Library Exchange Format (LEF) library file with the layer oxide permitivity present. Then use the **lef2plib** command to convert the LEF file to a .plib file, or use the **extract2plib** command to convert the extraction process file. Use the **read_lib** command to convert the .plib file to a .pdb file and read it into the tool. Once the library is read in, use the **write_lib** command to create the physical library database.

SEE ALSO

extract2plib(1)
lef2plib(1)
read_lib(2)
write_lib(2)

RCEX-059 (warning) The die area is undefined for this design.

DESCRIPTION

You receive this warning because you have not defined the die area, which is used to optimize internal data structures used during extraction. If you do not define the die area, it is inferred by the routing and placement of cells in the design. The tool visits each route and cell and chooses the die area that covers all.

WHAT NEXT

Edit the PDEF file and add the correct die area for the design.

SEE ALSO

read (2).

RCEX-060 (warning) Net '%s' is not fully connected and will be estimated.

DESCRIPTION

You receive this warning because two route segments you specified are not connected and the compiler will estimate RC of the net.

Accurate extraction engine is only performed on completely routed nets. Resistances and capacitances for partially routed nets will be estimated as virtual routed. RC results of all nets will be output.

WHAT NEXT

Disconnection is reported for all DRC-open nets. Please refer to DRC for definition of open net.

RCEX-061 (error) Process parameter '%s' is required for extraction.

DESCRIPTION

This error occurs because you are not using the TLUPlus-based RC model, and your physical library does not contain the named process parameter that is required for extraction.

WHAT NEXT

This is only an informational message. No action is required.

It is recommended that you use TLUPlus based RC extraction. You can use the **set_tlu_plus_files** command to specify the necessary TLUPlus tables.

SEE ALSO

report_tlu_plus_files(2)
set_tlu_plus_files(2)

RCEX-062 (Error) Missing/Illegal Process parameter '%s' for layer '%s'.

DESCRIPTION

You receive this message because you are not using the TLUPlus based RC model, and your physical library either does not contain or has illegal value for the named process parameter, which is required for RC computation and extraction.

WHAT NEXT

It is recommended to use TLUPlus based RC extraction. Please use **set_tlu_plus_files** to specify the necessary TLUPlus tables.

SEE ALSO

set_tlu_plus_files (2); **report_tlu_plus_files** (2);

RCEX-063 (Warning) Zero width special segment (’%d’ ’%d’) (’%d’ ’%d’) ignored for layer ’%s’.

DESCRIPTION

You receive this message because your physical data contains special segments whose widths are zero.

WHAT NEXT

Check your PDEF to make sure that the route widths are greater than zero.

RCEX-064 (error) Cannot read ECO parasitic files without full parasitic.

DESCRIPTION

This error message occurs when using the **read_parasitics -eco** command to read in ECO parasitic files with a design that is not with full parasitic. The design must have full parasitic with the **read_parasitics** command before you can use **read_parasitics -eco** to read ECO parasitic files.

WHAT NEXT

Run **read_parasitics** to read in the full parasitic for the design, and then run the **read_parasitics -eco** command.

SEE ALSO

read_parasitics(2)
write_parasitics(2)
extract_rc(2)

RCEX-065 (error) Cannot read ECO parasitic files with different format.

DESCRIPTION

This error message occurs when using the **read_parasitics -eco** command to read in ECO parasitic files with different parasitic format comparing to the full parasitic.

Note that **IC Compiler** only supports ECO SPEF or ECO SBPF.

WHAT NEXT

You must use the same format with ECO parasitic files. If your full parasitic is read in with SPEF, the ECO parasitic files must be SPEF; if your full parasitic is read in with SBPF, the ECO parasitic files must be SBPF as well.

SEE ALSO

read_parasitics(2)
write_parasitics(2)
extract_rc(2)

RCEX-066 (warning) %s is ignored during ECO parasitic reading.

DESCRIPTION

The given option is ignored during ECO parasitic reading, thus, specifying that has no effect. The same option (or lack of) used during full parasitic reading is used during ECO parasitic reading as well.

WHAT NEXT

Change the options when reading full parasitic files.

SEE ALSO

read_parasitics(2)
write_parasitics(2)
extract_rc(2)

RCEX-067 (information) Poly pin geometries are detected.

DESCRIPTION

You receive this information message because we detect some pins have geometries on the POLY layer.

By default, we respect POLY pin geometry and POLY contact, but does not check POLY wires. If you have POLY wires, you need to define the POLY layer as a routable layer, otherwise, a net with POLY wires might be considered as disconnected.

WHAT NEXT

This is an information message only. However, if you have POLY wires, it is recommended that you define POLY layer as routable layer to avoid the disconnection problem.

SEE ALSO

extract_rc(2)

RCEX-068 (information) Poly contacts are used in signal routing.

DESCRIPTION

You receive this information message because we detect some poly contacts are used in signal routing.

By default, we respect POLY pin geometry and POLY contact, but does not check POLY wires. If you have POLY wires, you need to define the POLY layer as a routable layer, otherwise, a net with POLY wires might be considered as disconnected.

WHAT NEXT

This is an information message only. However, if you have POLY wires, it is recommended that you define POLY layer as routable layer to avoid the disconnection problem.

SEE ALSO

extract_rc(2)

RCEX-069 (warning) Poly wires are used in signal routing.

DESCRIPTION

You receive this warning message because we detect some poly wires are used in signal routing.

By default, we respect POLY pin geometry and POLY contact, but does not consider POLY wires. If you have POLY wires, you need to define the POLY layer as a routable layer, otherwise, a net with POLY wires might be considered as disconnected.

WHAT NEXT

It is recommended that you define POLY layer as routable layer to avoid the disconnection problem.

SEE ALSO

extract_rc(2)

RCEX-070 (error) File '%s' does not exist or it is unreadable.

DESCRIPTION

This error message occurs when using the **-max_tluplus**, **-min_tluplus**, **-tf2itf_map** or **-tech2itf_map** option to the **set_tlu_plus_files** command and specifying a file name that does not exist or cannot be read.

WHAT NEXT

Verify that the file exists and that the permissions are set correctly, and then run the command again.

SEE ALSO

set_tlu_plus_files(2)

RCEX-071 (information) No layer mapping file is specified. Assume layer names are the same between the technology library and the ITF.

DESCRIPTION

This message advises you that you are using the **set_tlu_plus_files** command without specifying the **-tech2itf_mapi** option (switch).

The tool requires a layer mapping file to map the layer names from technology library to the Interconnect Technology File (ITF). If the switch is omitted, the tool assumes that the layer maps are the same between your technology library and the ITF.

For example, if in the physical library, you have the following:

```
routing_layer ( "METAL1" ) {
```

```
   ...
   }
contact_layer ( "VIA1" );
...
```

and in the ITF, you have the following:

```
CONDUCTOR metal1 {THICKNESS=0.53 WMIN=0.23 SMIN=0.23
   RPSQ=0.078 CAPACITIVE_ONLY_ETCH=0}
...
VIA via1 { FROM=metal1     TO=metal2 AREA=0.0169 RPV=1.6 }
```

provide a mapping as follows:

```
   conducting_layers
   METAL1 metal1
   ...
via_layers
VIA1 via1
...
```

However, if the ITF contains the following information, you are not required to specify the layer mapping file because the layer names are the same between the technology library and ITF:

```
CONDUCTOR METAL1 {THICKNESS=0.53 WMIN=0.23 SMIN=0.23
   RPSQ=0.078 CAPACITIVE_ONLY_ETCH=0}
...
VIA VIA1 { FROM=METAL1    TO=METAL2 AREA=0.0169 RPV=1.6 }
```

WHAT NEXT

This is only an informational message. No action is required.

If the layer names are the same between the technology library and the ITF, you can ignore this message.

Otherwise, you can provide a layer mapping file by using the **set_tlu_plus_files** command specifying the **-tech2itf_mapi** option. See the user guide for the syntax of the extraction parameters.

SEE ALSO

set_tlu_plus_files(2)

RCEX-072 (warning) The parasitic file does not contain location

information.

DESCRIPTION

You receive this warning message because the parasitic file that you are reading does not have location information.

A location consists of three components: x coordinate, y coordinate, and metal layer information. Each node in the parasitic rc tree should have a location defined. This includes terminal nodes that are connected to a pin, or internal sub nodes in the rc tree.

```
|------| | gate o======o sub node |------| || terminal || || |------|
o=============o gate | |------|
```

If you don’t have location specified for a node in your parasitic file, we will use an estimation to determine where is the location for the node.

WHAT NEXT

If you are only running timing analysis with the parasitic file, you can ignore the warning since locations are not required for timing analysis.

However, if you want to run **on_route** with the given parasitic file, you need to specify the location information since that decides the initial location for the new cells.

Consult the user manual for the program that creates the parasitic file on how to add location information.

SEE ALSO

read_parasitics(2)
extract_rc(2)

RCEX-073 (warning) Some parasitic nodes have no location.

DESCRIPTION

You receive this warning message because some of the parasitic nodes in the parasitic file that you are reading do not have location.

A location consists of three components: x coordinate, y coordinate, and metal layer information. Each node in the parasitic rc tree should have a location defined. This includes terminal nodes that are connected to a pin, or internal sub nodes in the rc tree.

```
|------| | gate o======o sub node |------| || terminal || || |------|
o=============o gate | |------|
```

If you don’t have location specified for a node in your parasitic file, we will use an estimation to determine where is the location for the node.

WHAT NEXT

If you are only running timing analysis with the parasitic file, you can ignore the warning since locations are not required for timing analysis.

However, if you want to run **on_route** with the given parasitic file, you need to specify the location information since that decides the initial location for the new cells.

Consult the user manual for the program that creates the parasitic file on how to add location information.

SEE ALSO

read_parasitics(2)
extract_rc(2)

RCEX-074 (warning) All parasitic nodes have location at (0, 0).

DESCRIPTION

You receive this warning message because all parasitic nodes in the parasitic file that you are reading have location at (0, 0). Even though (0, 0) could be a legal value for location, having all nodes at (0, 0) is not legal.

WHAT NEXT

If you are only running timing analysis with the parasitic file, you can ignore the warning since locations are not required for timing analysis.

However, if you want to run **on_route** with the given parasitic file, you need to specify the location information since that decides the initial location for the new cells.

Consult the user manual for the program that creates the parasitic file on how to add location information.

SEE ALSO

read_parasitics(2)
extract_rc(2)

RCEX-075 (warning) Some parasitic nodes have location

outside block boundray.

DESCRIPTION

You receive this warning message because some of the parasitic nodes in the parasitic file that you are reading have location outside the block boundary.

WHAT NEXT

If you are only running timing analysis with the parasitic file, you can ignore the warning since locations are not required for timing analysis.

However, if you want to run **on_route** with the given parasitic file, you need to specify the location information since that decides the initial location for the new cells.

Consult the user manual for the program that creates the parasitic file on how to add location information.

SEE ALSO

read_parasitics(2)
extract_rc(2)

RCEX-076 (warning) Poly layer %s is ignored during extraction.

DESCRIPTION

This warning message occurs when a poly layer in your physical library is also defined as a routable layer, but **IC Compiler** ignores the poly layer during either pre-route or post-route extraction.

WHAT NEXT

If the result is not what you intended and you dont want poly layers to be defined as routable layer, please make the correction to your physical library. Otherwise, you can discard this warning message.

SEE ALSO

extract_rc(2)
RCEX-028(n)

RCEX-077 (info) 0 net is extracted. Proceed to estimation.

DESCRIPTION

You receive this message because your design have no routes defined or partial connected routes, therefore, full extraction cannot performed and the design will be estimated.

WHAT NEXT

Use the **write_pdef** command to confirm that routes are present. If routes are present, look into error messages from the **extract_rc** command or the **read_pdef** command.

SEE ALSO

extract_rc (2), **read_pdef** (2), **write_pdef** (2).

RCEX-080 (information) Using real metal fill extraction: %s model.

DESCRIPTION

This information message advises you of the real metal fill extraction mode. The values are as follows:

- grounded - fill polygons will be treated as ground nets
- floating - fill polygons will be treated as floating nets
- automatic - fill polygons will be treated as is

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

extract_rc(2)
RCEX-015(n)

RCEX-081 (information) Using virtual shield extraction.

DESCRIPTION

This information message tells you that ICC is using virtual shiled extraction.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

extract_rc(2)
RCEX-015(n)

RCEX-082 (warning) There is NO metal fill related information in emulation tluplus files %s.

DESCRIPTION

This warning message occurs when you specify an emulation tluplus file using **-max_emulation_tluplus** or **-min_emulation_tluplus**, but there is no metal fill related information found in that tluplus file. Metal fill related information includes FILL_RATIO, FILL_SPACING, FILL_WIDTH and/or FILL_TYPE.

WHAT NEXT

If you intend to do metal fill emulation extraction in **IC Compiler**, please specify metal fill related information in the emulation ITF files, and re-generate emulation tluplus files using **grdgenxo**. Then specify the emulation tluplus files using **set_tlu_plus_files**. Otherwise, you can discard this warning message.

SEE ALSO

set_tlu_plus_files(2)
extract_rc(2)

RCEX-083 (warning) There is metal fill related information in

normal tluplus file %s.

DESCRIPTION

This warning message occurs when you specify both normal tluplus files and emulation tluplus files using **set_tlu_plus_files**, but there is metal fill related information found in the normal tluplus file. Metal fill related information includes FILL_RATIO, FILL_SPACING, FILL_WIDTH and/or FILL_TYPE.

WHAT NEXT

If you intend to do real metal fill extraction in **IC Compiler**, please remove metal fill related information from the normal ITF files, and re-generate normal tluplus files using **grdgenxo**. Then specify the normal tluplus files using **set_tlu_plus_files**. Otherwise, you can discard this warning message.

SEE ALSO

set_tlu_plus_files(2)
set_extraction_options(2)
extract_rc(2)

RCEX-084 (information) Using emulation metal fill extraction.

DESCRIPTION

This information message tells you that ICC is using emulation metal fill extraction.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

extract_rc(2)
set_extraction_options(2)

RCEX-085 (error) Variable physopt_enable_virtual_shield is no longer supported, please use set_extraction_options -

virtual_shield_extraction true|false.

DESCRIPTION

This error message tells you that variable *physopt_enable_virtual_shield* is no longer supported since Y-2006.06-SP2 release. Virtual shield extraction has since been controlled using *set_extraction_options -virtual_shield_extraction true|false*. The default setting is *true*.

WHAT NEXT

Use *set_extraction_options -virtual_shield_extraction true* to enable virtual shield extraction. Use *set_extraction_options -virtual_shield_extraction false* to disenable virtual shield extraction.

SEE ALSO

extract_rc(2)
set_extraction_options(2)

RCEX-086 (information) Using the HALF_NODE_SCALE_FACTOR in TLUPlus for process scale.

DESCRIPTION

This information tells you that half node scale factor is defined in TLUPlus (**HALF_NODE_SCALE_FACTOR**). ICC will use this scale factor for process scaling. It will overwrite the scaling factors defined in **set_extraction_options** command or in your physical library.

Since in TLUPlus model, only one process scale factor is supported, it is expected that all TLUPlus files have the same half node scale factor defined. If not, a warning message will be issued and the smallest scale factor found will be used for porcess scaling.

WHAT NEXT

This is an informational message only.

SEE ALSO

set_extraction_options (2); **report_extraction_options** (2), **RCEX-015**

RCEX-087 (Warning) Process_scale in set_extraction_options and HALF_NODE_SCALE_FACTOR in TLUPlus cannot be used at the same time.

DESCRIPTION

This warning tells you that **HALF_NODE_SCALE_FACTOR** is defined in TLUPlus. At the same time, there is max_process_scale or min_process_scale defined in **set_extraction_options**. In ICC, they cannot be used together. ICC will use **HALF_NODE_SCALE_FACTOR** for process scaling. It will ignore the scaling factors defined in **set_extraction_options** command.

WHAT NEXT

Please choose one for process scaling. You can remove process_scale in **set_extraction_options** command. Or you can remove **HALF_NODE_SCALE_FACTOR** from TLUPlus.

SEE ALSO

set_extraction_options (2); **report_extraction_options** (2), **RCEX-015**

RCEX-088 (error) User specified TLUPlus signauture file does not match current extraction context.

DESCRIPTION

This error tells you that the TLUPlus signature file specified by **-tlup_file** in **read_parasitics -format compact** command does not match that derived from the current extraction context. This means that your compact parasitic files may have been generated in a different extraction context, for example, with different tluplus files or different operation conditions, or different scenario settings, etc. Therefore, they cannot be used in this extraction session. A TLUPlus signature file records essential extraction context information used to create the assoicated compact parasitic files.

WHAT NEXT

You need to restore the same extraction context in order to use the specified compact parasitic files using **read_parasitics -format compact** command.

SEE ALSO

read_parasitics (2).

RCEX-090 (information) Doing incremental extraction.

DESCRIPTION

You receive this message to inform you that incremental extraction is triggered in rc-extraction.

WHAT NEXT

This is an informational message only. No action is required on your part.

RCEX-091 (information) Incremental extraction not triggered due to too many changes.

DESCRIPTION

You receive this message to inform you that incremental extraction is not triggered in rc-extraction.

WHAT NEXT

This is an informational message only. No action is required on your part.

RCEX-092 (information) Incremental extraction does not work with non-detail-routed extraction.

DESCRIPTION

You receive this message to inform you that incremental extraction will not be triggered in rc-extraction.

WHAT NEXT

This is an informational message only. No action is required on your part.

RCEX-100 (information) Using fast ILM extraction.

DESCRIPTION

This information message tells you that ICC is using the new and fast ILM extraction methodology.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

extract_rc(2)

RCEX-140 (information) Extractor based RC computation is enabled.

DESCRIPTION

This message advises you that the tool performs automatic computation for capacitance that is based on the extraction parameters.

This feature does not support min/max RC computation. You must use scaling factors to model the minimum condition. You can specify scaling factors by using the **set_delay_estimation_options** command.

To turn off this feature, use: the **set physopt_enable_extractor_rc** variable set to FALSE.

The tool will do this only if all of the following conditions are true:

- User RC is not used.
- TLU+ RC model is not used.
- Optional extraction parameters are present in the physical library.

The tool must have the following extraction parameters in order to perform automatic computation:

- field oxide thickness
- field oxide permitivity

- layer thickness for all routable layers
- layer oxide thickness for all routable layers
- layer oxide permitivity for all routable layers
- layer lateral oxide thickness for all routable layers
- layer lateral oxide permitivity for all routable layers

See the user guide for extraction parameter syntax.

WHAT NEXT

This is only an informational message. No action is required.

SEE ALSO

set_delay_estimation_options(2)
RCEX-141(n)
RCEX-143(n)

RCEX-141 (information) TLUPlus based RC computation is enabled.

DESCRIPTION

This information message occurs when the tool will perform automatic computation for capacitance based on the TLUPlus model.

This message only appears when both of the following are true:

- User RC is not used.
- The TLUPlus technology file is available.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

RCEX-144(n)

RCEX-142 (information) TLU based RC computation is enabled.

DESCRIPTION

This information message occurs when the tool will perform automatic computation for capacitance based on the TLU model.

This message only appears when all of the following are true:

- User RC is not used.
- TLUPlus is not used.
- The TLU technology file is available.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

RCEX-145(n)

RCEX-143 (information) Extractor-based RC computation is disabled.

DESCRIPTION

This message advises you that the tool does not perform automatic computation for capacitance that is based on extraction parameters although you might have specified them in the physical library.

You will not see this message if your physical library does not contain any extraction parameters.

Extraction parameters used by the tool are the following:

- field oxide thickness
- field oxide permitivity
- layer thickness for all routable layers

• layer oxide thickness for all routable layers

• layer oxide permitivity for all routable layers

• layer lateral oxide thickness for all routable layers

• layer lateral oxide permitivity for all routable layers

See the user guide for extraction parameter syntax.

WHAT NEXT

This is only an informational message. No action is required.

SEE ALSO

RCEX-140(n)

RCEX-144 (information) TLUPlus based RC computation is disabled.

DESCRIPTION

This information message occurs when the tool will not perform automatic computation for capacitance based on the TLUPlus model.

The most common reasons for failure include:

• Cannot open file for reading: *search_path* is not used to search for TLUPlus files; use the absolute path instead.

• Incorrect mapping file: it should map the .plib layer name to the ITF layer name.

• Error while generating TLUPlus model from ITF technology files: use the latest **grdgenxo** utility to create the technology file.

WHAT NEXT

This is an informational message only. No action is required.

Refer to RCEX-141 for conditions under which this feature is enabled.

SEE ALSO

RCEX-141(n)

RCEX-145 (information) TLU based RC computation is disabled.

DESCRIPTION

This information message occurs when the will not perform automatic computation for capacitance based on the TLU model.

The most common reasons for failure include the following:

• Cannot open file for reading: *search_path* is not used to search for TLU files; use absolute path instead

• Incorrect technology file

WHAT NEXT

This is an informational message only. No action is required.

Refer to RCEX-142 for the conditions under which this feature is enabled.

SEE ALSO

RCEX-142(n)

RCEX-201 (information) All the nets in the design are routed. Extraction of all the nets has been performed.

DESCRIPTION

All the nets have been extracted with RC values.

WHAT NEXT

report_timing report_nets

RCEX-202 (information) The mixed mode parasitic extraction has been performed.

DESCRIPTION

Some nets are routed and some nets are not. Extraction will be performed on the

fully connected nets. For partially routed or unrouted nets, estimation will be performed.

WHAT NEXT

report_timing report_nets

RCEX-203 (information) None of the nets in the design are routed. Estimation of all the nets will be performed.

DESCRIPTION

All the nets in the design will be estimated since they are not fully connected for partially connected.

WHAT NEXT

report_timing report_nets

RCEX-204 (information) File r/w error, %s.

DESCRIPTION

A File can’t be created in directory or A file can’t be found for reading.

WHAT NEXT

check if the directory is full or write_protected

RCEX-205 (error) Extraction failed.

DESCRIPTION

Extraction failed, it may be caused by many reasons 1. case setup error 2. disk is full or write protected. 3. other run time error

WHAT NEXT

check log message to find error happened before RCEX-205

RCEX-206 (information) maxIntraCapDistRatio is set to %d.

DESCRIPTION

maxIntraCapDistRatio is used to control how far RC-engine will search neighbors. It affects both R and C value.

WHAT NEXT

User can dump technology file(tf) and set maxIntraCapDistRatio in tf. Then re-load tf to make it work.

SEE ALSO

set_mw_technology_file(2)

RCEX-207 (error) No TLU+ is found. Please set TLU+ and rerun.

DESCRIPTION

Extraction failed because TLU+ is not found.

WHAT NEXT

Set TLU+ and rerun.

RCEX-208 (information) extraction with %i threads

DESCRIPTION

Extraction use multi-thread to speed up extraction computing.

WHAT NEXT

Set set_host_options -max_cores.

RDB-1 (warning) Ignore old spacing rule attribute. Please regenerate db by reading pdef.

DESCRIPTION

This warning is issued when detect the old spacing rule attribute from the pdef.The spacing rule will be ignore.

WHAT_NEXT

Please regenerate db by reading pdef again.

REGDUP-1 (warning) No Register duplication will be done, as the register max fanout load is set below 1.0

DESCRIPTION

Register duplication is based on fanout load on output pin. And it’s value can’t be less than 1.0

WHAT NEXT

Set register max fanout load above 1.0

REGDUP-2 (warning) Register duplication can’t be done, as no Registers found to have fanout greater than value set on current_design or register appropriately.

DESCRIPTION

Register duplication happens only if there are registers having higher fanout load than the maximum fanout load set.

WHAT NEXT

REGDUP-3 (information) Duplicating register %s with fanout load of %.2f

DESCRIPTION

WHAT NEXT

REGDUP-4 (information) Register %s is driving %s, can’t

duplicate.

DESCRIPTION

Register duplication does special architecture specific checks, which determine if a register needs to be duplicated or. This is done even after qualifying with respect to fanout count.

WHAT NEXT

RGEN-1 (fatal) Topology error in target net near '%s'.

DESCRIPTION

This message indicates an internal Synopsys error.

WHAT_NEXT

Contact your Synopsys application engineer, or the Synopsys hotline staff with a test case.

RGEN-2 (fatal) Topology error in replacement net near '%s'.

DESCRIPTION

This message indicates an internal Synopsys error.

WHAT_NEXT

Contact your Synopsys application engineer, or the Synopsys hotline staff with a test case.

RGEN-3 (fatal) Cannot write a file in '%s'.

DESCRIPTION

This message indicates an internal Synopsys error.

WHAT_NEXT

Contact your Synopsys application engineer, or the Synopsys hotline staff with a test case.

RGEN-4 (fatal) Cannot find attribute '%s' on object '%s'.

DESCRIPTION

This message indicates an internal Synopsys error.

WHAT_NEXT

Contact your Synopsys application engineer, or the Synopsys hotline staff with a test case.

RMAP-001 (error) Can’t open file "%s".

DESCRIPTION

The specified file could not be opened for reading or writing. If reading, the file may not exist, or may have incorrect permissions. If writing, you may not have access to the directory.

WHAT NEXT

Verify the file name, directory name, and permissions and try again.

RMAP-002 (warning) Can’t close file "%s".

DESCRIPTION

The specified file could not be closed.

WHAT NEXT

Verify disk status and file permissions and try again.

RMAP-003 (error) File "%s" is an invalid rail map file.

DESCRIPTION

The specified file is not a valid rail map file.

WHAT NEXT

Verify the type of the file specified and try again.

RMAP-004 (error) Unsupported version %d.%d encountered

(should be %d.%d).

DESCRIPTION

The version of the specified file is unsupported. It is either too old or newer than the currently supported one.

WHAT NEXT

Use a compatible version of the rail analysis application to generate a file with a supported version of the file.

RMDB-1 Failed to Initialize MWX Api’s (error) code ’%d’ .

DESCRIPTION

WHAT NEXT

RMDB-2 (error) Failed to open lib ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-3 (warning) The logic db and CEL view netlist data maybe out of sync. Please sync up in milkyway before running read_mdb.

DESCRIPTION

WHAT NEXT

RMDB-4 (error) Failed to open lib ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-5 (info) The logic db and CEL view netlist data maybe out

of sync. Please sync up in milkyway before running read_mdb.

DESCRIPTION

WHAT NEXT

RMDB-6 (error) internal error reading the cells.

DESCRIPTION

WHAT NEXT

RMDB-7 (error) Failed to get instance name.

DESCRIPTION

WHAT NEXT

RMDB-8 (error) Failed to get cell instance name.

DESCRIPTION

WHAT NEXT

RMDB-9 (error) Failed to get cell instance name.

DESCRIPTION

WHAT NEXT

RMDB-10 (error) Failed to get the instance location for ’%s’ .

DESCRIPTION

WHAT NEXT

RMDB-11 (error) Failed to get the instance orientation for ’%s’ .

DESCRIPTION

WHAT NEXT

RMDB-12 (error) Failed to get the instance restriction for ’%s’ .

DESCRIPTION

WHAT NEXT

RMDB-13 (error) Failed to get the instance restriction for ’%s’ .

DESCRIPTION

WHAT NEXT

RMDB-14 (error) Failed to get the instance ’%s’ .

DESCRIPTION

WHAT NEXT

RMDB-15 (error) Failed to get the instance location for ’%s’ .

DESCRIPTION

WHAT NEXT

RMDB-16 (error) Failed to get the instance orientation for ’%s’ .

DESCRIPTION

WHAT NEXT

RMDB-17 (error) Failed to get the instance restriction for ’%s’ .

DESCRIPTION

WHAT NEXT

RMDB-18 (error) Failed to set the route data for net_name ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-19 (warning) Via name ’%s’ not found in Technology file .

DESCRIPTION

WHAT NEXT

RMDB-20 (warning) Via name ’%s’ not found in Technology file .

DESCRIPTION

WHAT NEXT

RMDB-21 (error) Failed to set the groute data for net_name

’%s’.

DESCRIPTION

WHAT NEXT

RMDB-22 (info) path not supported for net ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-23 (error) Failed to convert the sites .

DESCRIPTION

WHAT NEXT

RMDB-24 (warning) Split clock net not supported.

DESCRIPTION

WHAT NEXT

RMDB-25 (info) Pin got ’%d’ .

DESCRIPTION

WHAT NEXT

RMDB-26 (warning) No pins found in the design .

DESCRIPTION

WHAT NEXT

RMDB-27 (error) in setting the pin attributes .

DESCRIPTION

WHAT NEXT

RMDB-28 (warning) Ignoring nondefault rule ’%s’ .

DESCRIPTION

WHAT NEXT

RMDB-29 (warning) Group ’%s’ without region .

DESCRIPTION

WHAT NEXT

RMDB-30 (error) Failed to Initialize MWX Api’s (error) code ’%d’

.

DESCRIPTION

WHAT NEXT

RMDB-31 (error) Failed to open library .

DESCRIPTION

WHAT NEXT

RMDB-32 (warning) Failed to create obstruction for layer ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-33 (info) Signal Nets will be ignored for the design .

DESCRIPTION

WHAT NEXT

RMDB-34 (warning) No nets found in the design .

DESCRIPTION

WHAT NEXT

RMDB-35 (error) Failed to get net from the design.

DESCRIPTION

WHAT NEXT

RMDB-36 (info) Creating physical only net ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-37 (warning) Failed to create a physical only net ’%s’ .

DESCRIPTION

WHAT NEXT

RMDB-38 (warning) Failed to create non default rule for net

’%s’.

DESCRIPTION

WHAT NEXT

RMDB-39 (warning) Failed to get routing attribute for net ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-40 (error) Current design is not linked .

DESCRIPTION

WHAT NEXT

RMDB-41 (error) Failed to Initialize MWX Api’s (error) code ’%d’

.

DESCRIPTION

WHAT NEXT

RMDB-42 (error) Failed to set the current design ’%s’ .

DESCRIPTION

WHAT NEXT

RMDB-43 (info) Creating physical only cell ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-44 (error) Internal error to get the DB cell instance ’%s’ .

DESCRIPTION

WHAT NEXT

RMDB-45 (error) Failed to set the conversion factor.

DESCRIPTION

WHAT NEXT

RMDB-46 (error) Internal error Failed to add layer ’%s’ .

DESCRIPTION

WHAT NEXT

RMDB-47 (error) in setting the layer attribute .

DESCRIPTION

WHAT NEXT

RMDB-48 (warning) Failed to set tracks .

DESCRIPTION

WHAT NEXT

RMDB-49 (error) No library information present for design.

DESCRIPTION

WHAT NEXT

RMDB-50 (error) No library information present for design .

DESCRIPTION

WHAT NEXT

RMDB-51 (warning) Failed to set the non default rules.

DESCRIPTION

WHAT NEXT

RMDB-52 (warning) Route guides created in the non routing

layer ’%s’ are not supported .

DESCRIPTION

WHAT NEXT

RMDB-53 (error) Internal error in routing obstructions .

DESCRIPTION

WHAT NEXT

RMDB-54 (error) Failed to open library ’%s’ with cell ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-55 (error) Unable to set the design ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-56 (error) Top design is not set correctly .

DESCRIPTION

WHAT NEXT

RMDB-57 (info) Reading Cell information from MDB.

DESCRIPTION

WHAT NEXT

RMDB-58 (warning) Failed to create power/ground net .

DESCRIPTION

WHAT NEXT

RMDB-59 (info) Reading Route information from MDB.

DESCRIPTION

WHAT NEXT

RMDB-60 (info) Creating physical port for '%s'.

DESCRIPTION

WHAT NEXT

RMDB-61 (warning) Failed to create physical port '%s'.

DESCRIPTION

WHAT NEXT

RMDB-62 (warning) Failed to get port location for port '%s'.

DESCRIPTION

WHAT NEXT

RMDB-63 (error) Failed to set port location for port '%s'.

DESCRIPTION

WHAT NEXT

RMDB-64 (info) Signal Nets will be ignored for the design .

DESCRIPTION

WHAT NEXT

RMDB-65 (warning) Failed to create non default rule for net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-66 (warning) Failed to get routing attribute for net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-67 (warning) Failed to get routing attribute for physical

net ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-68 (error) Failed to get the layer name ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-69 (error) Error in setting the route segment for net ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-70 (error) Error in setting the route segment for net ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-71 (error) Failed to get the layer name ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-72 (warning) Net type cannot be global route type for net

name ’%s’ .

DESCRIPTION

WHAT NEXT

RMDB-73 (error) Error in setting the route segment for net ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-74 (error) Error in setting the route segment for net ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-75 (error) Failed to get the layer name ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-76 (error) Error in setting the route segment for net ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-77 (error) Error in setting the route segment for net ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-78 (warning) clock skew not supported .

DESCRIPTION

WHAT NEXT

RMDB-79 (warning) Shield net not supported for read_mdb .

DESCRIPTION

WHAT NEXT

RMDB-80 (warning) Failed to set wires for vias on net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-81 (error) Failed to get the via name '%s'.

DESCRIPTION

WHAT NEXT

RMDB-82 (error) Failed to set the route via for net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-83 (error) Failed to set the route via for net ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-84 (error) No library information present for design.

DESCRIPTION

WHAT NEXT

RMDB-85 (error) No library information present for design .

DESCRIPTION

WHAT NEXT

RMDB-86 (error) Cannot get via for ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-87 (error) Cannot create library via in design for ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-88 (error) Cannot create design via for ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-89 (error) No library information present for design.

DESCRIPTION

WHAT NEXT

RMDB-90 (error) Turn Vias are not supported at this time .

DESCRIPTION

WHAT NEXT

RMDB-91 (info) Stack Vias and Turn vias not supported.

DESCRIPTION

WHAT NEXT

RMDB-92 (error) Routing via not translated .

DESCRIPTION

WHAT NEXT

RMDB-93 (error) Via ’%s’ not translated .

DESCRIPTION

WHAT NEXT

RMDB-94 (Info) SDC information is not read by read_mdb.

DESCRIPTION

The SDC information is not read from the Milkyway database by read_mdb command. The designer has to explicitly read the SDC data from the Milkyway database.

WHAT NEXT

read_sdc(2)

RMDB-95 (error) Directory not writable '%s' .

DESCRIPTION

WHAT NEXT

RMDB-96 (warning) SDC file exists at '%s'.

DESCRIPTION

WHAT NEXT

RMDB-97 (warning) Could not reset incremental SDC flag in Milkyway.

DESCRIPTION

This warning message informs you that although the incremental Synopsys Design Constraints (SDC) may be written out, the flag for incremental SDC in Milkyway cannot not be reset.

Upon further use of this Milkyway database, it may appear that there is no

incremental SDC written out.

WHAT NEXT

This is a warning message only. No action is required on your part.

SEE ALSO

read_mdb (2).

RMDB-98 (error) Incremental SDC could not be found.

DESCRIPTION

This error message appears when there is an error in finding incremental Synopsys Design Constraints (SDC) in the Milkyway design database.

WHAT NEXT

Determine if the incremental SDC can be written out using Astro, and annotate that SDC to the design in the tool by sourcing that SDC.

SEE ALSO

read_mdb (2).

RMDB-99 (error) The specified cell ’%s’ doesn’t exists in design library ’%s’.

DESCRIPTION

WHAT NEXT

RMDB-100 (warning) Failed to set the min/max layer for net ’%s’

.

DESCRIPTION

WHAT NEXT

RMDB-101 (error) Unable to create net %s.

DESCRIPTION

Read_mdb failed to create a net. Probably the hierarchy information in CEL view is incorrect.

WHAT NEXT

Please run astRepairHierPreservation in Astro and rerun read_mdb command.

RMDB-103 (error) Port instance %s of cell inst %s not connected to hier net. Please run astRepairHierPreservation in Astro to fix.

DESCRIPTION

WHAT NEXT

RMDB-104 (error) Port instance %s of cell inst %s not connected to hier net. Please run astRepairHierPreservation in

Astro to fix.

DESCRIPTION

WHAT NEXT

RMDB-105 (error) Found new hierarchy %s in MW..

DESCRIPTION

Read_mdb unable to update the milkyway library because of the inconsistencies between the LOGIC view and CEL view.

WHAT NEXT

Fix the MDB and rerun read_mdb command.

There also exists a work-around. You can set variable "mw_create_netlist_from_CEL" to true so that the inconsistent LOGIC view will be ignored. Do not forget to explicitly load the SDC after read_mdb.

RMDB-106 (error) Failed to open the main library '%s'.

DESCRIPTION

Read_mdb cannot open the given MDB library.

WHAT NEXT

Double check the library name and path are correct and you have write permission.

RMDB-107 (error) Failed to open cell '%s' in view '%s' .

DESCRIPTION

Read_mdb unable to open the given cell for write.

WHAT NEXT

Make sure you have write permission to the cell. Also check the mw_reference_library variable to make sure that all the libraries are added correctly.

RMDB-108 (warning) Please update Hierarchy in Astro before running read_mdb.

DESCRIPTION

You get this error because Milkyway does not have a flag set which shows that the hierarchy perservation is not updated.

WHAT NEXT

Run astRepairHierPreservation in Astro before you save the cell and then run read_mdb.

RMDB-109 (error) Failed to close cell .

DESCRIPTION

Read_mdb unable to close the cell that opened earlier. This should be an internal error.

WHAT NEXT

Please check Synopsys for solutions.

RMDB-110 (error) Failed to open cell '%s' in view '%s' .

DESCRIPTION

WHAT NEXT

RMDB-111 (error) Failed to close cell .

DESCRIPTION

WHAT NEXT

RMDB-112 (error) Failed to get the Instances in the design .

DESCRIPTION

Read_mdb failed to get the instance from milkyway library.

WHAT NEXT

Make sure your milkyway library is correct and rerun read_mdb.

RMDB-113 (warning) No cell boundary defined for the design.

DESCRIPTION

Read_mdb could not get the boundary definition from the MDB.

WHAT NEXT

Make sure the boundary is defined before run read_mdb.

RMDB-114 (error) No sites found in the design .

DESCRIPTION

Read_mdb could not find the sites defined for current design.

WHAT NEXT

Make sure the site is defined before run read_mdb.

RMDB-115 (error) Failed to get the site row basearray.

DESCRIPTION

Read_mdb unable to get the site row base array. This usually means that the MDB library was not correctly prepared.

WHAT NEXT

Make sure the MDB library is correct before call read_mdb.

RMDB-116 (error) Failed to get the site for design.

DESCRIPTION

Read_mdb unable to get the site data from the library. This usually means that the MDB library was not correctly prepared.

WHAT NEXT

Make sure the MDB library is correct before call read_mdb.

RMDB-117 (error) Failed to set the site '%s' in the db .

DESCRIPTION

WHAT NEXT

RMDB-118 (warning) No tracks in the design.

DESCRIPTION

Read_mdb unable to get the track. This usually means that the MDB library was not correctly prepared.

WHAT NEXT

Make sure the MDB library is correct before call read_mdb.

RMDB-119 (error) Failed to set the track '%s' .

DESCRIPTION

read_mdb could not set the track. This could happened if running out of memory.

WHAT NEXT

Rerun the command with more memory.

RMDB-120 (warning) Maximum number of pins exceeded the equivalent pin class.

DESCRIPTION

The equivalent pin class number exceeded the predefined maximum number in MDB. This mostly happened because of some internal error.

WHAT NEXT

Make sure your MDB library is correct before call read_mdb. As a workaround, you can

also try to manually reduce the pin number.

RMDB-121 (warning) Maximum number of pins exceeded the equivalent pin class of 1000.

DESCRIPTION

Read_mdb limits the number of equivalent pin class to 1000. If the actual number is more than this, the pin information could not be saved into the db.

WHAT NEXT

Reduce the equivalent pin class number and rerun read_mdb.

RMDB-122 (warning) Pin '%s' not connected to any Net.

DESCRIPTION

The given pin is not connected to any net in the MDB library.

WHAT NEXT

RMDB-123 (error) Failed to set the rule '%s'.

DESCRIPTION

WHAT NEXT

RMDB-124 (warning) Poly shaped blockages are not supported.

DESCRIPTION

DB library does not support poly-shaped blockages. Read_mdb will drop these blockages if any.

WHAT NEXT

RMDB-125 (warning) No group associated with the region .

DESCRIPTION

WHAT NEXT

RMDB-126 (warning) No cells found in the group.

DESCRIPTION

WHAT NEXT

RMDB-127 (warning) No group associated with the region .

DESCRIPTION

WHAT NEXT

RMDB-128 (warning) No cells found in the group.

DESCRIPTION

WHAT NEXT

RMDB-129 (warning) Failed to set the min/max layer for net '%s' .

DESCRIPTION

```
Read_mdb unable to set the min/max layer for the given net. This could happen if
read_mdb cannot get the specified layer.
```

WHAT NEXT

Make sure the MDB library is correct before call read_mdb.

RMDB-130 (error) No nets in the design .

DESCRIPTION

Read_mdb could not find any nets defined in current design. No route information will be updated.

WHAT NEXT

Make sure the MDB library is correct before call read_mdb.

RMDB-131 (error) Failed to get the Net '%s'.

DESCRIPTION

Read_mdb could not find the specified net in the design.

WHAT NEXT

RMDB-132 (error) Failed to get the Net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-133 (error) Unable to create net %s.

DESCRIPTION

read_mdb failed to create a new net. Probably the hierarchy information in CEL view is incorrect.

WHAT NEXT

Please run astRepairHierPreservation in Astro.

RMDB-134 (info) Sourcing SDC from file %s.

DESCRIPTION

WHAT NEXT

RMDB-135 (error) Linking the design failed .

DESCRIPTION

read_mdb failed to link the design internally. No physical information could be transfered from the MDB library.

WHAT NEXT

Make sure to provide all the necessary libraries. Also check the link command for necessary steps.

RMDB-136 (error) Polygon with odd points!. Dropping last co-ordinate.

DESCRIPTION

WHAT NEXT

RMDB-137 (warning) Round type wire extensions are not supported.

DESCRIPTION

Round type wire extensions are not supported by DB library. Read_mdb will not be able to keep this extension info.

WHAT NEXT

RMDB-138 (info) Incremental SDC is at %s.

DESCRIPTION

An incremental Synopsys Design Constraints file is written in your current working directory with the name shown. You need to manually source this file to annotate this SDC to the design. If the switch -update_sdc is provided to read_mdb, the SDC will be automatically sourced. Incremental SDC are SDC constraints that were created during an Astro session and are additional to the existing SDC constraints that describe the constraints of the design.

WHAT NEXT

Source the incremental SDC which is shown, if you want the incremental SDC annotated on your design. If you have specified the switch -update_sdc to read_mdb, no action is required by you on this message.

RMDB-140 (error) Internal error in initializing the milkyway host.

DESCRIPTION

WHAT NEXT

RMDB-141 (Warning) Failed to open cell '%s' in view '%s'.

DESCRIPTION

The specified cell doesn't exist on the specified milkyway libraries.

WHAT NEXT

1. Check the mw_reference_library variable to make sure that all the libraries are added correctly.

RMDB-142 (information) The LOGIC view does not exist. The

tool is creating it in the memory database from a CEL view.

DESCRIPTION

This message advises you that the LOGIC view for the specified cell does not exist in the library. The tool uses the netlist by default and the Synopsys Design Constraints (SDC) information is not translated. The reason for this action is because this library was created by using a directory from another tool.

WHAT NEXT

This is only an informational message. No action is required.

However, if the result is not what you intended, you can explicitly read the SDC information from the other tool into the tool that is generating the message. You can run the **change_names** command to ensure that your data is consistent with the SDC that is output from the system.

SEE ALSO

change_names(2)

RMDB-143 (error) dixi2ax_mwUnInit called without Initializing.

DESCRIPTION

WHAT NEXT

RMDB-144 (warning) Failed to read the GCEL grid from milkway design library.

DESCRIPTION

WHAT NEXT

RMDB-145 (warning) Failed to create placement obstruction for

the design.

DESCRIPTION

Read_mdb unable to create the placement obstruction for current design.

WHAT NEXT

Make sure the MDB library is correct before call read_mdb.

RMDB-146 (warning) Failed to attach the TLu+ file for design '%s'.

DESCRIPTION

read_mdb unable to attach the TLu+ file to the design library.

WHAT NEXT

Please manually set the environment variable "tlu_plus_library" with correct value.

RMDB-147 (error) Non-rectangular edge for polygon.

DESCRIPTION

WHAT NEXT

RMDB-148 (warning) Less than 4 points: ignoring POLYGON definition.

DESCRIPTION

WHAT NEXT

RMDB-149 (information) Unable to get direction for port,

assuming INPUT.

DESCRIPTION

read_mdb failed to get the port direction, so just assume it is INPUT.

WHAT NEXT

SEE ALSO

RMDB-150 (information) Unable to get direction for ref port.

DESCRIPTION

read_mdb failed to get the port direction from MDB. Set the direction to UNKNOWN in DB.

WHAT NEXT

SEE ALSO

RMDB-151 (warning) Failed to get port type.

DESCRIPTION

read_mdb failed to get the port type from MDB.

WHAT NEXT

Check if the port type exists in the MDB and rerun read_mdb.

SEE ALSO

RMDB-152 (warning) Failed to get hierarchical net name.

DESCRIPTION

read_mdb unable to get the hierarchical net name from Milkyway library. This could be an internal error.

WHAT NEXT

Please try astRepairHierPreservation in Astro.

SEE ALSO

RMDB-153 (warning) More than one base array found.

DESCRIPTION

Read_mdb got more than one base array for the given design from MDB library.

WHAT NEXT

SEE ALSO

RMDB-154 (warning) Core area may not be set correctly.

DESCRIPTION

read_mdb failed to get the core area for the given design.

WHAT NEXT

Check the mdb library and rerun read_mdb.

SEE ALSO

RMDB-155 (warning) Failed to create routing obstruction.

DESCRIPTION

WHAT NEXT

RMDB-156 (information) Updating netlist from Milkyway database.

DESCRIPTION

This information message occurs when the tool is updating a netlist from the Milkyway database.

This message does not occur if the Milkyway database was initially created using a Jupiter or Astro flow.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

mw_create_netlist_from_CEL(2)

RMDB-157 (information) Processing master '%s'.

DESCRIPTION

This information message occurs when the **read_mdb** command is processing the specified design master.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

`read_mdb(2)`

RMDB-158 (error) Failed to get cell name.

DESCRIPTION

WHAT NEXT

RMDB-159 (error) Failed to initiate an iterator through ports in the cell.

DESCRIPTION

WHAT NEXT

RMDB-160 (error) Failed to initiate an iterator through cell instances in the cell.

DESCRIPTION

WHAT NEXT

RMDB-161 (error) Failed to initiate an iterator through port instances in the cell.

DESCRIPTION

WHAT NEXT

RMDB-162 (error) Voltage area %s contains no hierarchical

objects.

DESCRIPTION

read_mdb could not find any hierarchical cell belong to the given voltage area. This usually means that the voltage attribute was not correctly set for the cells. read_mdb does not recognize the voltage attribute set only to the leaf cells.

WHAT NEXT

Update the voltage area attribute for the hierarchical cells and do read_mdb again.

RMDB-163 (warning) Exclusive plan group '%s' is translated to non-exclusive bounds in the tool.

DESCRIPTION

This warning occurs because the tool does not support exclusive plan groups. These plan groups are treated as non-exclusive plan groups (bounds) for reading and writing purposes. Any subsequent writing would transfer the exclusive plan groups to non-exclusive bounds in this tool.

The hardness level of the bound is determined by the rigidity on the plan group. The tool considers anything other than rigidity of 10 to be soft bounds.

WHAT NEXT

You can create non-exclusive plan groups for a smooth flow between JXT/Astro. You can also convert all of the exclusive plan groups to voltage areas before doing any reading.

RMDB-164 (info) Successfully read SDC file attached to CEL view.

DESCRIPTION

JupiterXT and Astro can attach the SDC file to the CEL view. Read_mdb will read the attachment and invoke 'read_sdc' to import the SDC constraints. This message indicates this operation has completed successfully.

WHAT NEXT

ROPT-001 (error) Qor does not converge. Exitting.

DESCRIPTION

You receive this error message because the design does not converge during route_opt. The tool is expecting better result after optimization but it got worse and stop continue to optimize.

WHAT NEXT

Please check if there is any issue in the following areas: constraints, congestion, routing, and utilization.

SEE ALSO

route_opt (2), **set_route_opt_strategy** (2),

ROPT-002 (warning) The design has too many route violation.

DESCRIPTION

You receive this warning message because the tool sees many route violations in the design. When the design has many route violation, the search and repair step takes a lot longer and will have impact overall runtime of route_opt. When the tool detects too many route violations, the tool will run only one loop of search and repair for the following steps regardless of the original search and repair loop settings to reduce runtime impact. Also, it is recommended that route violation should be taken care of before proceed further.

WHAT NEXT

Please check the source of route violation. If you want to ignore route violation checking, please refer set_route_opt_strategy.

SEE ALSO

route_opt (2), **set_route_opt_strategy** (2),

ROPT-003 (error) To run xtalk_reduction, please enable SI.

DESCRIPTION

You receive this error message because xtalk_reduction is enabled but SI flow is not enabled. The xtalk_reduction is effective on delta delay, switching noise and static noise. To run xtalk_reduction, at least one of SI effects such as delta delay, switching noise and static noise has to be used. To enable SI effect, please use "set_si_options".

WHAT NEXT

Please set any one of SI effects through "set_si_options".

SEE ALSO

route_opt (2), **set_si_options** (2),

ROPT-004 (error) To specify -only_ options, please set -incr option.

DESCRIPTION

All only options in route_opt, -only_hold_time and -only_wire_size, are supported only in incremental run. To enable -only settings, -incremental has to be set.

WHAT NEXT

Please set -incremental option in route_opt command.

SEE ALSO

route_opt (2),

ROPT-005 (information) Discontinue %s due to too many changes occurred.

DESCRIPTION

You receive this message because the tool sees too many changes were made in one optimization stage. When the tool made too many chnages, there will be potential

convergence problems and to prevent the convergence problem, the tool stops optimization and move on to the detail placement and ECO route. To turn off this feature, please set routeopt_disable_cpulimit to true.

WHAT NEXT

Please check the number of violations in the design. If there are too many violations from different constraints, it is recommended to fix violations before running route_opt using psynopt.

SEE ALSO

route_opt (2), **set_route_opt_strategy** (2), **psynopt** (2), **routeopt_disalbe_cpulimit(3)**

ROPT-006 (information) max_design_rules cost has higher priority than the max delay cost.

DESCRIPTION

You receive this message because the tool is fixing design rule violtion with max_design_rule cost as the highest priority. With this setup, the tool will fix design rule violation even it degrades timing.

WHAT NEXT

To disable this setup, please set routeopt_drc_over_timing to false.

SEE ALSO

route_opt (2), **set_route_opt_strategy** (2), **psynopt** (2), **routeopt_drc_over_timing(3)**

ROPT-007 (Error) -power_mode is an obsolete option, use -power

DESCRIPTION

-power_mode option is obsolete. To enable leakage optimzation inside route_opt, please use -power option instead.

WHAT NEXT

Please set -power option in route_opt command.

SEE ALSO

route_opt (2) ~

ROPT-008 (error) Invalid specification for %s switch.

DESCRIPTION

The current specification for that switch is not valid one.

WHAT NEXT

Please use one of valid specification for the switch. To find out the valid specifications, please refer man page of route_opt.

SEE ALSO

route_opt (2)

ROPT-009 (Error) More than one -only_ options are specfied.

DESCRIPTION

To enable any -only_ options in route_opt, single -only_ option should be specified. route_opt can’t support multiple -only_ options.

WHAT NEXT

Please set only one -only_ option.

SEE ALSO

route_opt (2)

ROPT-010 (Error) Invalid option with -initial_route_only.

DESCRIPTION

The specified options is not valid with -initial_route_only.

WHAT NEXT

Please check man page for -initial_route_only to see which options are supported with -initial_route_only.

SEE ALSO

route_opt (2)

ROPT-011 (Error) -route_mode is obsoleted.

DESCRIPTION

Starting from 2007.03-SP2, the option -route_mode is no longer used in set_route_opt_strategy. All route settings come from set_route_options and set_si_options. If nothing is specified, route_opt will perform timing driven global route and crosstalk prevention track assign.

WHAT NEXT

Please check ROPT-013 and ROPT-014 for what settings are used for global route timing driven and track assign xtalk prepvention inside route_opt.

SEE ALSO

route_opt (2), **set_route_options** (2), **set_si_options** (2)

ROPT-012 (Warning) Setting high density limit will cause convergence issue.

DESCRIPTION

You receive this message because you set the density limit for route_opt too high. There will be potential convergence problems due to large displacements.

WHAT NEXT

Please make sure the setting is intended one.

SEE ALSO

route_opt (2)

ROPT-013 (Information) Running global route with timing driven mode %d (%s).

DESCRIPTION

This message informs you that global route is running timing driven mode or not inside route_opt. By default, route_opt is running timing driven global route. To change the setting of global route timing driven, please use set_route_option. When the message is saying "user_define", that means the setting is coming from set_route_option.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

route_opt (2), **set_route_option** (2)

ROPT-014 (Information) Running track assign route with crosstalk prevention mode %d (%s).

DESCRIPTION

This message informs you that track assign route is running crosstalk prevention mode or not inside route_opt. By default, route_opt is running crosstalk prevention in track assign route. To change the setting of crosstalk prevention in track assign route, please use set_si_options. driven, please use set_route_option. When the message is saying "user_define", that means the setting is coming from set_si_options.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

route_opt (2), **set_si_options** (2)

ROPT-015 (Information) Using user defined cost priority %s.

DESCRIPTION

This message informs you that post_route optimization is using user defined cost priority to optimize the design. The user defined cost prioity is coming from set_cost_priority command.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

route_opt (2), **set_cost_priority** (2)

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ROPT-016 (Information) Ignoring routeopt_drc_over_timing setting due to user defined cost priority.

This message informs you that route_opt ignores routeopt_drc_over_timing setting because user defined cost priority is specified in the design.

This is an informational message only. No action is required on your part.

route_opt (2), **set_cost_priority** (2)

ROPT-017 (Error) Invalid options specified with -only_ options.

DESCRIPTION

To enable any -only_ options in route_opt, -only_ option can only be specified with -incr option.

WHAT NEXT

Please remove extra options from route_opt command.

SEE ALSO

route_opt (2) ~

ROPT-020 (Information) Running %s with timing driven mode

%s (%s).

DESCRIPTION

This message informs you that the specified routing stage is running timing driven mode or not inside route_opt. By default, route_opt (when using zrt router) is running timing driven global route, track assign and detail route. To change the setting of timing driven in the respective stages, please use set_zrt_groute_options|set_zrt_route_track_options|set_zrt_droute_options respectively. When the message is saying "user_define", that means the setting is coming from set_zrt_*_options commands.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

route_opt (2), **set_zrt_groute_options** (2), **set_zrt_droute_options** (2), **set_zrt_route_track_options** (2)

ROPT-021 (Information) Running %s with crosstalk driven mode %s (%s).

DESCRIPTION

This message informs you that the specified routing stage is running crosstalk driven mode or not inside route_opt. By default, route_opt (when using zrt router) is running crosstalk driven global route, track assign. To change the setting of crosstalk driven in the respective stages, please use set_zrt_groute_options|set_zrt_route_track_options|set_zrt_droute_options respectively. When the message is saying "user_define", that means the setting is coming from set_zrt_*_options commands.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

route_opt (2), **set_zrt_groute_options** (2), **set_zrt_droute_options** (2), **set_zrt_route_track_options** (2)

ROPT-022 (Error) Invalid option %s when using route_opt zroute flow.

DESCRIPTION

The specified options is not valid when we are in route_opt zroute flow. That is, when set_route_mode_options -zroute is set to true.

WHAT NEXT

Please check man page for set_route_opt_strategy or route_opt to see which options are supported in the zroute flow.

SEE ALSO

route_opt (2) **set_route_opt_strategy** (2)

ROPT-023 (Warning) User has disabled timing-driven detail route in zroute crosstalk flow. Routing result may not be optimal.

DESCRIPTION

User is recommended to turn on timing-driven for detail route when using zrt router in crosstalk-enabled flow for optimal routing result.

WHAT NEXT

Set timing driven is true using set_route_zrt_detail_options for optimal detail routing result.

SEE ALSO

route_opt (2) **set_route_zrt_detail_options** (2)

ROPT-024 (Warning) You’re using a hidden variable which will cause longer runtime.

DESCRIPTION

You receive this message because you set a hidden variable which will cause longer

runtime during route_opt.

WHAT NEXT

Please make sure the setting is intended one.

SEE ALSO

route_opt (2)

ROPT-025 (Error) Hold fixing cannot be performed because set_fix_hold is not defined for any clock.

DESCRIPTION

You receive this message because "set_fix_hold" is not defined for any clock. Thus, hold fixing cannot performed.

WHAT NEXT

Please make sure the setting is intended one.

SEE ALSO

route_opt (2), **set_fix_hold** (2)

ROPT-026 (Warning) route_opt -power/-only_power or set_route_opt_strategy -power_aware_optimization true is not valid when set_power_options -leakage false is specified.

DESCRIPTION

The specified options are not valid when leakage optimization is turned off. The flow will run without leakage optimization.

WHAT NEXT

Please check man page for set_power_options, set_route_opt_strategy or route_opt. If leakage optimization is needed, use set_power_options -leakage true; otherwise, turn off -power_aware_optimization or remove -power/-only power option.

SEE ALSO

route_opt (2) **set_route_opt_strategy** (2)

ROPT-027 (Warning) Some buffers have been defined as preferred buffer during hold fixing. However, no preferred buffer is available for hold fixing in certain operation conditions.

DESCRIPTION

You receive this warning messagee because of the following reason. Some buffers have been defined as preferred buffers for hold fixing by "set_prefer -min". However, there exist one or more operation conditions where any of hold fixing preferred buffers aren't available. Thus, unexpetecd buffers might be used during hold fixing.

WHAT NEXT

Please, make sure preferred buffers are defined properly to fix hold violation for all operation conditions.

SEE ALSO

route_opt (2), **set_fix_hold** (2)

RPGP-001 (error) Compression does not work with alignment type '%s'

DESCRIPTION

This error message occurs when the **create_rp_group** command detects that you specified compress with incompatible alignment type.

WHAT NEXT

Choose either a different alignment type or compress so that they are compatible. After making any changes, rerun the command.

SEE ALSO

create_rp_group(2)

RPGP-002 (error) Alignment type '%s' requires that you also provide a -pin_align_name.

DESCRIPTION

This error message occurs when the **create_rp_group** command detects that you specified an alignment type that requires the additional specification of a pin alignment name.

WHAT NEXT

Choose either a different alignment type that does not require a pin alignment name or provide a pin alignment name. After making any changes, rerun the command.

SEE ALSO

create_rp_group(2)

RPGP-003 (warning) Spurious -pin_align_name '%s' provided

for alignment type ’%s’.

DESCRIPTION

This warning message occurs when the **create_rp_group** command detects that you specified an alignment type that does not require the specification of a pin alignment name, so the given pin alignment name will be ignored.

WHAT NEXT

This is only a warning message. No action is required. You can eliminate this warning message by following the instructions below.

Choose either a different alignment type that requires a pin alignment name or do not provide a pin alignment name. After making any changes, rerun the command.

SEE ALSO

create_rp_group(2)

RPGP-004 (error) Duplicate instantiation: the instance %s is already being used to instantiate the group %s inside the group %s.

DESCRIPTION

This error message occurs when you instantiate a group twice using the same instance while using the **add_to_rp_group** command. A group may only be instantiated once per instance.

WHAT NEXT

Choose a different instance of the same design to instantiate it multiple times and then run the command again.

SEE ALSO

add_to_rp_group(2)

RPGP-005 (error) Non-positive keepout width: %d.

DESCRIPTION

This error message occurs when the **add_to_rp_group** command detects that you specified a keepout width that is non-positive.

WHAT NEXT

Choose a positive keepout width or do not provide a keepout width. After making any changes, rerun the command.

SEE ALSO

add_to_rp_group(2)

RPGP-006 (error) Non-positive keepout height: %d.

DESCRIPTION

This error message occurs when the **add_to_rp_group** command detects that you specified a keepout height that is not positive.

WHAT NEXT

Choose a positive keepout height or do not provide a keepout height. After making any changes, rerun the command.

SEE ALSO

add_to_rp_group(2)

RPGP-007 (information) No groups were removed.

DESCRIPTION

This information message occurs when the **remove_rp_group** command detects that no groups were removed. You specified the **-all** option, but no groups are loaded into memory yet, so there are no groups to remove.

WHAT NEXT

To suppress this informational message from being emitted, add the **-quiet** flag to the **write_rp_group** command.

SEE ALSO

add_to_rp_group(2)
create_rp_group(2)
read_milkyway(2)
remove_rp_group(2)
write_milkyway(2)
write_rp_group(2)

RPGP-008 (error) Keepout option%s specified for '%s' add.

DESCRIPTION

This error message occurs when the **add_to_rp_group** command detects that you specified an option that is only used for keepouts but the **add_to_rp_group** argument is not **-keepout**.

WHAT NEXT

Either remove the keepout options or change the **add_to_rp_group** argument to **-keepout**. After making any changes, rerun the command.

SEE ALSO

add_to_rp_group(2)

RPGP-009 (error) Circular: attempt to include group '%s' within '%s' creates a circle.

DESCRIPTION

This error message occurs when the **add_to_rp_group** command detects an attempt to create a hierachical inclusion that would result in a chain of inclusions, such that a group would include itself by the transitive clousure of inclusions.

WHAT NEXT

Eliminate any cycles in your hierarchy inclusion. After making any changes, rerun the command.

SEE ALSO

add_to_rp_group(2)

RPGP-010 (error) Relative Placement (RP) command %s requires that a physical design is loaded, but none is in memory.

DESCRIPTION

This error message occurs when the Relative Placement (RP) command you tried to evaluate detects that no physical design is loaded. A physical design must be loaded in memory in order to evaluate any RP commands.

WHAT NEXT

Load a physical design into memory and rerun the command.

SEE ALSO

add_to_rp_group(2)
create_rp_group(2)
read_milkyway(2)
remove_rp_group(2)
write_milkyway(2)
write_rp_group(2)

RPGP-011 (error) Hierarchical instantiation option%s specified for ’%s’ add.

DESCRIPTION

This error message occurs when the **add_to_rp_group** command detects that you specified an option that is only used for hierarchical instantiations, but the **add_to_rp_group** argument is not **-hierarchy**.

WHAT NEXT

Either remove the hierarchical instantiation options or change the **add_to_rp_group** argument to **-hierarchy**. After making any changes, rerun the command.

SEE ALSO

add_to_rp_group(2)

RPGP-012 (error) The -hierarchical or -leaf option%s specified for '%s' add.

DESCRIPTION

This error message occurs when the **add_to_rp_group** command detects that you specified an option that is only used for the **-hierarchy** or **-leaf** argument, and the **-keepout** argument was used.

WHAT NEXT

Either remove the options or change the **add_to_rp_group** argument to **-hierarchy** or **-leaf**. After making any changes, rerun the command.

SEE ALSO

add_to_rp_group(2)

RPGP-013 (error) A group named %s already exists in design %s.

DESCRIPTION

This error message occurs when **create_rp_group**, **extract_rp_group** or **order_rp_groups** command detects that you tried to create a new group using a name that is already being used for another group in the same design.

WHAT NEXT

Choose a new unique name for the group within the given design, and rerun the command.

SEE ALSO

create_rp_group(2)
extract_rp_group(2)
order_rp_groups(2)

RPGP-014 (error) Add at row %d is out of range for RP group

%s that has only %d rows.

DESCRIPTION

This error message occurs when the **add_to_rp_group** command detects that you tried to add an item to a Relative Placement (RP) group in a row that is out of range of the rows for that group. If the object being added is a cell in multiple rows then some specified rows are out of range.

WHAT NEXT

Choose a new row that is within the rows of the RP group, or modify the RP group to have more rows using the **set_rp_group_options** command. After making any changes, rerun the command.

SEE ALSO

add_to_rp_group(2)
set_rp_group_options(2)

RPGP-015 (error) Add at column %d is out of range for RP group %s that has only %d columns.

DESCRIPTION

This error message occurs when the **add_to_rp_group** command detects that you tried to add an item to a Relative Placement (RP) group in a column that is out of range of the columns for that group.If the object being added is a cell in multiple columns then some specified columns are out of range.

WHAT NEXT

Choose a new column that is within the columns of the RP group, or modify the RP group to have more columns using the **set_rp_group_options** command. After making any changes, rerun the command.

SEE ALSO

add_to_rp_group(2)
set_rp_group_options(2)

RPGP-016 (error) Cannot find cell '%s' in design '%s' as %s for

group ’%s’.

DESCRIPTION

This error message occurs when the **add_to_rp_group**, **remove_from_rp_group** or **extract_rp_group** command detects that you passed in a cell name that could not be located in the design of the group.

WHAT NEXT

Check the spelling of the cell name and confirm that the cell you are providing is in the same design as the Relative Placement (RP) group to which you are trying to add/remove it. After making any changes, rerun the command.

SEE ALSO

add_to_rp_group(2)
remove_from_rp_group(2)

RPGP-017 (error) Duplicate hierarchical inclusion of group ’%s’.

DESCRIPTION

This error message occurs when the **add_to_rp_group** command detects that you tried to include a group that is already included elsewhere. A group may only be included once.

WHAT NEXT

Either remove the other inclusion, skip this one, or switch to hierarchy instantiation. After making any changes, rerun the command.

SEE ALSO

add_to_rp_group(2)

RPGP-018 (information) No groups were written.

DESCRIPTION

This information message occurs when the **write_rp_group** command detects that no groups were written. You specified the **-all** option but since no groups are loaded into memory yet, no groups can be written.

WHAT NEXT

This is only an informational message. You can eliminate this message by following the instructions below.

To prevent message from being emitted, add the **-quiet** flag to the **write_rp_group** command.

SEE ALSO

add_to_rp_group(2)
create_rp_group(2)
read_milkyway(2)
remove_rp_group(2)
write_milkyway(2)
write_rp_group(2)

RPGP-019 (error) Unable to add '%s' to column %d and row %d of group '%s' because that location is already occupied.

DESCRIPTION

This error message occurs when the **add_to_rp_group** command detects that you tried to add an item to a column and row position that is already occupied by another item. Each lattice position of a Relative Placement (RP) group can only contain one item.

WHAT NEXT

Either remove the item already located at the given lattice position before inserting another item at that location, or choose another location that is empty. After making any changes, rerun the command.

SEE ALSO

add_to_rp_group(2)

RPGP-020 (warning) Hierarchical RP group '%s' has an offset value that will be ignored.

DESCRIPTION

This warning message occurs because while processing a hierarchical Relative Placement (RP) group, an **-x_offset** or **-y_offset** value was present. However, offset values are not yet implemented for hierarchical RP, so the value is ignored. Offset

values can be provided when creating RP groups with the **create_rp_group** command.

WHAT NEXT

RP group offsets are not supported for hierarchical RP. This is only a warning message. You can eliminate this warning message by following the instructions below.

In the future, do not provide offset values for any RP groups that are hierarchical when creating them.

SEE ALSO

create_rp_group(2)

RPGP-021 (error) Cannot find cell '%s' in design '%s'.

DESCRIPTION

This error message occurs when the **all_rp_references** command detects that you passed in a cell name that could not be located in the given design.

WHAT NEXT

Check the spelling of the cell name and confirm that the cell you looking up is in the same design as the design given. Note that if **-design** is not supplied, the design in which the cell is looked up defaults to the current_design. After making any changes, rerun the command.

SEE ALSO

all_rp_references(2)
current_design(2)

RPGP-022 (warning) Ignored spurious -design argument.

DESCRIPTION

This warning message occurs when the **all_rp_references** command detects that you passed in a **-design** argument when no *cell_list* argument was supplied.

The **-design** argument is used to determine the context within which the *cell_list* argument is interpreted. Without any *cell_list* argument the **-design** argument does not have any meaning and is ignored.

WHAT NEXT

Either omit the **-design** argument or provide a *cell_list* argument to make this warning go away.

SEE ALSO

all_rp_references(2)

RPGP-023 (error) RP in Milkyway requires manual schema evolution.

DESCRIPTION

This error message occurs when the **read_milkyway** command detects that the database you are reading contains old format Relative Placement (RP) data. All old format Relative Placement (RP) data gets removed, so if you need to recover the RP data then do manual schema evolution or source RP information again.

WHAT NEXT

To do manual schema evolution, locate the old version of physical compiler that was used to create the Milkyway database you are now failing to read. Load that database using that old version and dump out all the RP annotations with **write_rp_groupfp -all -output *filename***. Next, remove all the RP annotations with **remove_rp_groupfp -all. With the RP now stored as a TCL script in *filename*** and removed from memory, write back out a new Milkyway database with **write_milkywayfp.**

Go back to the new version of physical compiler where you first got this error and load in the newly created Milkyway database you just created with all the RP information stripped. Once it is loaded, execute the script stored in *filename* to reannotate your RP. Lastly, write back out the Milkyway again with **write_milkywayfp to create your manual schema evolved database.**

Now you can resume your prior work by replacing the old Milkyway database with the new schema evolved one you just created.

SEE ALSO

read_milkyway(2)
remove_rp_group(2)
write_milkyway(2)
write_rp_group(2)

RPGP-024 (error) Relative Placement (RP) %s failed.

DESCRIPTION

This error message occurs when an unexpected error condition arises while manipulating RP in a Milkyway CEL view.

WHAT NEXT

You may continue to work, however, any RP stored in your Milkyway CEL view should be considered corrupt and not used. You should report this problem to Synopsys with a testcase to reproduce it.

You can try to work around the limitation by a method similar to the manual schema evolution described in RPGP-023. This is done by dumping your RP as TCL commands via the **write_rp_groupfp command, and then deleting all the RP via the remove_rp_groupfp command, and then writing out your Milkyway database without any RP. Finally, start a new session of this tool, load the Milkyway database you just created which has no RP, and reannotate the RP using the TCL commands you created earlier with the write_rp_groupfp command.**

SEE ALSO

read_milkyway(2)
remove_rp_group(2)
write_milkyway(2)
write_rp_group(2)

RPGP-025 (error) Cannot find '%s' '%s' in rp group '%s'.

DESCRIPTION

This error message occurs when the **remove_from_rp_group** command detects that you passed in an item (cell,keepout,hierarchical or instance) name that could not be located in the rp group you provided.

WHAT NEXT

Check the spelling of the item name and confirm that the item belongs to the rp group you have provided. After making any changes, rerun the command.

SEE ALSO

remove_from_rp_group(2)

RPGP-026 (warning) Could not get legal location for placing cell '%s' in RP group '%s'.

DESCRIPTION

This is not a failure but a warning indicating that the location for the RP cell is reserved; Coarse placement will continue and will find next non-reserved location. If legal location can not be found then RP group placement may fail.

WHAT NEXT

See the placement results and use the command **check_rp_groups** for finding any RP constraint violations.

SEE ALSO

check_rp_groups(2)

RPGP-027 (warning) Possible placement failure of relative placement group '%s'.

DESCRIPTION

No enough area for the entire relative placement group to be placed together because of overlapping with fixed cells or placement obstruction. Note that the search region for the relative placement group in the core area is based on the value that you specify to the -move_effort option. The relative placement cells will be placed around blockages if possible. The relative placement group constraints might not be respected.

WHAT NEXT

Bring up the ICC GUI and check the placement results. Use the command **check_rp_groups** for finding any relative placement constraint violations. You might need to modify -move_effort for the relative placement group.

SEE ALSO

check_rp_groups(2)
create_rp_group(2)
set_rp_group_options(2)

RPGP-028 (warning): The height '%f' of the RP group '%s' is

more than the height ’%f’ of the core area.

DESCRIPTION

You receive this warning message because the RP group does not fit in the current core area. This might be due to overestimating the size of the RP group for the current core area.

WHAT NEXT

Redo the floorplan to increase the core area, or use Module Compiler shrink the RP group.

SEE ALSO

check_rp_groups (2).

RPGP-029 (warning) The width ’%f’ of RP group ’%s’ is more than the width ’%f’ of the core area.

DESCRIPTION

You receive this message because the RP group might be overlapped with other cells in the current core area. This is might be due to over-estimating the RP group for the current core area.

WHAT NEXT

If placement fails, redo the floorplan to increase the core area, or use Module Compiler to shrink the RP group.

RPGP-030 (warning) RP Group ’%s’ needed to move beyond specified movement limit to respect RP.

DESCRIPTION

The RP group can not be placed within the specified movement limit. RP Group will not be moved beyond specified limits so could result in violation of RP constraints.

WHAT NEXT

See the placement results and use the command **check_rp_groups** for finding any RP constraint violations. If RP placement fails then increase the movement limits, which can be set using the variables **physopt_rp_allow_x_move** and **physopt_rp_allow_y_move**.

SEE ALSO

check_rp_groups(2)

RPGP-031 (warning) POSSIBLE RP ALIGNMENT FAILURE: Failure in finding legal locations for maintaining RP Constraints of cluster '%s'.

DESCRIPTION

If the location of cell(s) is not legal and is overlapped with blockages, other cells etc then the RP constraints may be violated.

WHAT NEXT

See the placement results and use the command **check_rp_groups** for finding any RP constraint violations. If RP placement fails then increase the floorplan area.

SEE ALSO

check_rp_groups(2)

RPGP-032 (warning) Could not set user-specified orientations for cell '%s'.

DESCRIPTION

The user specified orientations can not be set because none of them are allowed at the legal location of the cell.

WHAT NEXT

Add more orientations to the list, so that one of them will be legal. If you add more orientations for one cell, consider adding similar orientations for the other cells in the same column to maximize the possibility of getting straight routes.

SEE ALSO

check_rp_groups(2)

RPGP-033 (warning) Possible failure of relative placement within the voltage region. Could not place the relative placement group '%s' within the voltage region.

DESCRIPTION

This warning occurs because of no area that is free of placement obstruction or fixed cells to place the entire relative placement group together in the voltage region. The relative placement cells are placed inside the voltage area if possible. The relative placement group constraints might not be respected.

WHAT NEXT

Bring up the GUI and check the placement results. You can use the **check_rp_groups** command to find any relative placement constraint violations. You might need to increase the size of voltage area if the relative placement group size is bigger than the size of voltage area. You might also need to use the **modify** command with the **-move_effort** option for the relative placement group.

SEE ALSO

check_rp_groups(2)
create_rp_group(2)
set_rp_group_options(2)

RPGP-034 (warning) All cells of the relative placement group '%s' do not belong to the same voltage region. This group is ignored during placement.

DESCRIPTION

This warning occurs because all of the cells of the relative placement group do not belong to the same voltage region. The voltage region has a higher priority than the relative placement group. During placement, this relative placement group is ignored, but voltage regions are honored.

WHAT NEXT

You can recreate the relative placement group with all the cells in one voltage

region.

SEE ALSO

check_rp_groups(2)
create_rp_group(2)

RPGP-035 (warning) Relative Placement leaf cell data may have been lost.

DESCRIPTION

The relative placement leaf cell data has been corrupted during placement optimizations. The reason may be because you may not have used the recommended RP flow, set_dont_touch or set_size_only on all RP cells, before doing placement. If RPGP-024 is concurrently issued with RPGP-035 then RPGP-024 may be ignored.

WHAT NEXT

Please use set_dont_touch or set_size_only on all RP cells before running placement.

SEE ALSO

create_rp_group(2)
add_to_rp_group(2)

RPGP-036 (warning) The x offset specified for the RP group '%s' has not been satisfied. The movement from the specified location is '%f'.

DESCRIPTION

This warning message occurs because while processing a Relative Placement (RP) group, an **x_offset** was present, and the RP group could not be placed at the requested location.

WHAT NEXT

This is only a warning message. The movement may not be significant. If it is significant then it may be caused by obstructions/blockages around that area. In such a case please speCIFY appropriate x and y offsets.

SEE ALSO

create_rp_group(2)
set_rp_group_options(2)
remove_rp_group_options(2)
report_rp_group_options(2)

RPGP-037 (warning) The y offset specified for the RP group '%s' has not been satisfied. The movement from the specified location is '%f'.

DESCRIPTION

This warning message occurs because while processing a Relative Placement (RP) group, an **y_offset** was present, and the RP group could not be placed at the requested location.

WHAT NEXT

This is only a warning message. The movement may not be significant. If it is significant then it may be caused by obstructions/blockages around that area. In such a case please specify appropriate x and y offsets.

SEE ALSO

create_rp_group(2)
set_rp_group_options(2)
remove_rp_group_options(2)
report_rp_group_options(2)

RPGP-038 (warning) The alignment has not been respected for RP group '%s'.

DESCRIPTION

This warning occurs when the alignment specified for an RP group or any of its hierarchical RP groups has not been met. The warning indicates failure of column alignment of non-compressed RP groups or row alignment of compressed RP groups.

WHAT NEXT

You may open up the GUI and check the alignment of the RP groups. The specified alignment may not be met after placement because of overlap with fixed placement objects.

SEE ALSO

check_rp_groups(2)
create_rp_group(2)
set_rp_group_options(2)
set_attribute(2)

RPGP-039 (warning) The utilization has not been respected for the RP group '%s'.

DESCRIPTION

This warning occurs because the actual utilization is lower than the specified utilization. The default utilization is 1.0. The utilization has not been respected such that column alignment could be maintained for relative placement (RP) columns; this can occur when tap cell arrays or other fixed physical cells or blockages are present.

WHAT NEXT

Bring up the concerned relative placement group in the GUI to analyze the exact reason for the utilization constraint violation.

SEE ALSO

check_rp_groups(2)
create_rp_group(2)
set_rp_group_options(2)

RPGP-040 (warning) Relative placement group '%s' contains too many objects and cannot be created.

DESCRIPTION

You received this message because the relative placement group you are trying to create contains too many objects. The relative placement group was not created.

WHAT NEXT

You can continue to work, however this relative placement group was not created in the database and subsequent add_to_rp_group commands for this group will fail. A single flat relative placement group must contain less than 4194299 objects for efficient handling of relative placement during placement. To create a larger relative placement group, you can use hierarchical relative placement groups.

SEE ALSO

create_rp_group(2)
add_to_rp_group(2)

RPGP-041 (warning) The relative placement constraints cannot be honored for relative placement group %s, because all cells of relative placement group does not belong to same move bound.

DESCRIPTION

You received this message because all cells of the relative placement group does not belong to the same move bound. The move bounds have higher priority than the relative placement group. During placement, the relative placement group is ignored, but the move bounds are honored.

WHAT NEXT

If you use both relative placement groups and move bounds, make sure that all cells of a relative placement group are in the same move bound.

SEE ALSO

create_rp_group(2)
add_to_rp_group(2)
create_bounds(2)

RPGP-042 (warning) Possible placement failure of relative placement keepout '%s'.

DESCRIPTION

You received this message because the specified hard keepout would have been overlapped with tap cell if placed at the intended location.

WHAT NEXT

You can continue to work, however this particular rp keepout will not be placed. If you want keepouts of rp group to be overlapped with tap cell, please set "-allow_keepout_over_tapcell true" for that rp group using command "set_rp_group_options" and re-run the command again.

SEE ALSO

create_rp_group(2)
set_rp_group_options(2)

RPGP-043 (information) The size_only value for cts_option attribute of relative placement group is only applicable to clock_opt, not to '%s'. '%s' will use fixed_placement for each relative placement group, which has size_only value specified for cts_option.

DESCRIPTION

The commands compile_clock_tree and optimize_clock_tree does not support size_only value for cts_option and these commands use fixed_placement value for each relative placement group, which has size_only value specified for cts_option.

SEE ALSO

create_rp_group(2)
set_rp_group_options(2)

RPGP-044 (warning) The given name '%s' is ambiguous and %d cells matched that name.

DESCRIPTION

The given cell name matches with more than one cell, so no object is being added into the relative placement group.

WHAT NEXT

To add a leaf or instance in relative placement group please specify a name which can be uniquely determined. You may specify the full hierarchical name of the object to be added.

SEE ALSO

add_to_rp_group(2)
write_rp_groups(2)

RPGP-045 (warning) Can’t find specified relative placement group(s) in design ’%s’.

DESCRIPTION

None of the specified relative placement group is found in the design.

WHAT NEXT

Please provide the correct relative placement group name. You may use "get_rp_groups" command to see relative placement groups that are present in the design.

SEE ALSO

get_rp_groups(2)
write_rp_groups(2)

RPGP-046 (warning) Orientation on hierarchical inclusions and instantiations is not supported, and will be ignored during placement.

DESCRIPTION

Orientation on hierarchical inclusions and instantiations is not supported. The option will be ignored.

SEE ALSO

report_rp_group_options(2)
report_attribute(2)
write_rp_groups(2)

RPGP-047 (error) The value ’%s’ for option ’-allow_keepout_over_tapcell’ is not valid.

DESCRIPTION

The value for option "-allow_keepout_over_tapcell" can either be true or false.

WHAT NEXT

Please provide the correct value for the option.

SEE ALSO

create_rp_group(2)
set_rp_group_options(2)

RPGP-048 (information) There are no relative placement groups in design '%s'

DESCRIPTION

There are no relative placement groups in the design.

SEE ALSO

create_rp_group(2)
set_rp_group_options(2)

RPGP-049 (Error) Keepout '%s' already exists in '%s' relative placement group.

DESCRIPTION

The keepout already exists in the relative placement group. So this keepout will not be added into the relative placement group.

WHAT NEXT

You may add the keepout with different name in the relative placement group.

SEE ALSO

get_rp_group_keepouts(2)
write_rp_groups(2)

RPGP-050 (Information) The ignore option of the relative placement group '%s' is being removed because it is not a top

level group anymore.

DESCRIPTION

The ignore option is supported for top level relative placement group only. The ignore option of the relative placement group is being removed, because it is being added as hierarchical relative placement group in another relative placement group, and can not be ignored anymore.

WHAT NEXT

If you want to ignore the relative placement group then do not add it as a hierarchical relative placement group.

SEE ALSO

create_rp_group(2)
set_rp_group_options(2)

RPGP-051 (error) The -cts_option option should have a value of fixed_placement or size_only.

DESCRIPTION

This error occurs because the **-cts_option** option has been given a value other than **fixed_placement** or **size_only** in the **create_rp_group** or **set_rp_group_options** command.

WHAT NEXT

You can continue to work, but the command that is responsible for producing the error is not implemented. Alternatively, the you can rerun the same command using the **fixed_placement** or **size_only** value for the **-cts_option** option.

SEE ALSO

create_rp_group(2)
set_rp_group_options(2)

RPGP-052 (error) The -route_opt_option option should have a

value of fixed_placement or in_place_size_only.

DESCRIPTION

This error occurs because the **-route_opt_option** option has a value other than **fixed_placement** or **in_place_size_only** in the **create_rp_group** or **set_rp_group_options** command.

WHAT NEXT

You can continue to work, but the command that is producing the error is not implemented. Alternatively, the you can rerun the same command using the **fixed_placement** or **in_place_size_only** value for the **-route_opt_option** option.

SEE ALSO

create_rp_group(2)
set_rp_group_options(2)

RPGP-053 (error) The -psynopt_option option should have a value of fixed_placement or size_only.

DESCRIPTION

This error occurs because the **-psynopt_option** option has a value other than **fixed_placement** or **size_only** in the **create_rp_group** or **set_rp_group_options** command.

WHAT NEXT

You can continue to work, but the command that is producing the error is not implemented. Alternatively, the you can rerun the same command using the **fixed_placement** or **size_only** value for the **-psynopt_option** option.

SEE ALSO

create_rp_group(2)
set_rp_group_options(2)

RPGP-054 (error) The functionality for multiple RP locations for a cell is not currently supported. The tool is skipping add of '%s'

into ’%s’ since it is already in relative placement group ’%s’.

DESCRIPTION

This error occurs because you attempted to include a leaf cell in two different relative placement (RP) groups.

WHAT NEXT

You can continue to work, although the attempted addition of a leaf cell to the RP group has not occurred.

SEE ALSO

add_to_rp_group(2)

RPGP-055 (Error) Relative Placement (RP) group ’%s’ is corrupted and is being removed.

DESCRIPTION

This error occurs when the tool removes a relative placement group because its data has been corrupted. The corrupted relative placement group along with its hierarchical groups has been removed.

WHAT NEXT

The user may continue working, although the relative placement group, for which this error was thrown, has been removed. Alternatively, the user may recreate the affected relative placement group, and then continue working.

SEE ALSO

write_rp_groups(2)
get_rp_groups(2)

RPGP-056 (error) Cannot have "::" in the name specified for a relative placement group.

DESCRIPTION

This error occurs because the tool prepends the design name to the given relative

placement (RP) group name and stores it in the following format:

```
design_name::group_name
```

Hence, the RP group name you specify should not include "::".

WHAT NEXT

The RP group has not been created. Remove the "::" and rerun the command to create the RP group.

SEE ALSO

create_rp_group(2)
extract_rp_group(2)
order_rp_groups(2)

RPGP-057 (error) No valid leaf cells are found in the list of cells for extract_rp_group.

DESCRIPTION

This error occurs because no leaf cells are found in the list of cells for the **extract_rp_group** command. The **extract_rp_group** command filters out macros, hierarchical cells, cells belonging to other RP groups, and unplaced cells if you specify the **-coordinates** or **-physical** option.

WHAT NEXT

Ensure that the *coordinates_list* or *objects_list* value lists cells that are not macros or hierarchical and which do not belong to any other RP group. If you use the **extract_rp_group** command with the **-coordinates** or **-physical** option, the tool considers only cells that are placed.

SEE ALSO

add_to_rp_group(2)
extract_rp_group(2)

RPGP-058 (error) The number of RP cells is more than the grid

size (rows*columns) you provided for extract_rp_group.

DESCRIPTION

This error occurs because the number of relative placement (RP) cells in the list you specified by the **-coordinates** or **-objects** option of **extract_rp_group** command is more than the grid size provided.

WHAT NEXT

The RP group is not created. Ensure that the number of cells you specify matches the grid size (rows*columns) and that the cells are not hierarchical cells and do not belong to another existing RP group.

SEE ALSO

extract_rp_group(2)

RPGP-059 (information) '%s' coordinate specified as -coordinates option for extract_rp_group is outside the core. Moving it inside the core.

DESCRIPTION

This message advises you if any of the coordinates specified in the **-coordinates** option of the **extract_rp_group** command falls outside the core area.

WHAT NEXT

This is only an informational message. No action is required. The specified relative placement (RP) group is created by using the modified coordinates. If this is not the intended result, you can rerun the command specifying the correct values for **-coordinates** option.

SEE ALSO

add_to_rp_group(2)
extract_rp_group(2)

RPGP-060 (error) The region provided in the -coordinates

option of extract_rp_group is incorrect.

DESCRIPTION

This error occurs because, for the values specified by the **-coordinates** option or the **extract_rp_group** command, the lower-left x-coordinate is greater than the upper-right x-coordinate or the lower-left y-coordinate is greater than the upper-right y-coordinate.

WHAT NEXT

The specified relative placement (RP) group is not created. Rerun the command using the correct values for the xy-coordinates.

SEE ALSO

add_to_rp_group(2)
extract_rp_group(2)

RPGP-061 (Warning) The number of RP cells is less than the grid size (rows*columns) provided by the user for extract_rp_group

DESCRIPTION

This warning occurs when the number of RP cells in the list provided via -cordinates or -objects_list by the user is less than the grid size provided.

WHAT NEXT

The specified relative placement group will be created, but the grid would not be fully occupied by relative placement cells.

SEE ALSO

extract_rp_group

RPGP-062 (warning) Compress does not work with alignment

type ’%s’

DESCRIPTION

This error message occurs when the tool detects that you specified compress with incompatible alignment type.

WHAT NEXT

You can continue, however compress will be ignored and alignment type will be respected. If you don’t want that, choose either a different alignment type or compress so that they are compatible. After making any changes, rerun the command.

SEE ALSO

create_rp_group(2)
set_rp_group_options(2)
remove_rp_group_options(2)

RPGP-063 (warning) Compress does not work with alignment type ’%s’

DESCRIPTION

This error message occurs when the tool detects that you are trying to override the alignment type of an element of a relative placement group with an alignment type which is incompatible with compress. compress is set for parent relative placement group.

WHAT NEXT

You can continue, however alignment type of the element will not be overridden. If you don’t want that, choose either a different alignment type or compress so that they are compatible. After making any changes, rerun the command.

SEE ALSO

add_to_rp_group(2)
set_rp_group_options(2)
remove_rp_group_options(2)

RPGP-064 (error) bit stack placement is not supported for

hierarchical relative placement group.

DESCRIPTION

This error message occurs when the tool detects that you are trying do bit stack placement for hierarchical relative placement group which is not supported.

WHAT NEXT

Please set physopt_use_bit_stacked_placement to FALSE and re run the command.

SEE ALSO

add_to_rp_group(2)
remove_from_rp_group(2)

RPGP-065 (error) Keepout '%s' will not be placed.

DESCRIPTION

The relative placement group which need to be compressed does not support keepout for which width or height is not provided.

WHAT NEXT

Please provide height and width of the keepout or remove this keepout from relative placement group or remove the compress flag from the relative placement group which contains that keepout.

SEE ALSO

add_to_rp_group(2)
remove_from_rp_group(2)
remove_rp_group_options(2)

RPGP-066 (warning) The size_only flow is used for relative placement group '%s', because fixed_placement flow is not supported during place_opt.

DESCRIPTION

This warning occurs because the '-psynopt_option' value specified for a relative

placement group is fixed_placement, so it will be ignored during place_opt. Instead, place_opt performs size_only for cells in the relative placement groups.

WHAT NEXT

You can continue working. However the size_only is used as the '-psynopt_option', instead of fixed_placement during place_opt.

SEE ALSO

create_rp_group(2)
remove_rp_group_options(2)
set_rp_group_options(2)

RPGP-067 (error) Hard macros cannot be added to a relative placement group. Skipping addition of hard macro '%s' to relative placement group '%s'.

DESCRIPTION

This error occurs when 'add_to_rp_group' or 'extract_rp_group' attempts to add a hard macro to a relative placement group. Only non-macro cells can be added as leaf cells of relative placement groups.

WHAT NEXT

You may continue to work. The addition of hard macro cells to the relative placement group will be skipped.

SEE ALSO

add_to_rp_group(2)
extract_rp_group(2)

RPGP-068 (warning) physopt_use_bit_stacked_placement variable is obsolete. Please use -compress switch of create_rp_group or set_rp_group_options command instead.

DESCRIPTION

You receive this warning message because you used a variable that is obsolete. Use -compress option of command create_rp_group or set_rp_group_options as described in

their corresponding man pages.

WHAT NEXT

Remove the obsolete variable, and use new switch of create_rp_group or set_rp_groups_options.

SEE ALSO

create_rp_group(2) set_rp_groups_options(2) remove_rp_group_options(2)

RPGP-069 (warning) The Relative Placement group '%s' has multiple instances and will not be removed.

DESCRIPTION

The command remove_rp_groups when called with -hier option will not remove any Relative Placement groups instantiated down the hierarchy of the Relative Placement groups specified, unless all its instantiations have been removed.

WHAT NEXT

You may call remove_rp_groups command for the Relative Placement group that is not removed, to remove it from the design.

SEE ALSO

remove_rp_groups(2) write_rp_groups(2)

RPGP-070 (Error) Multiple locations are not supported for '%s'.

DESCRIPTION

The options num_rows and num_columns of command add_to_rp_group can be used to add a cell in multiple locations of relative placement group. Multiple locations are not supported for non-leaf objects.

WHAT NEXT

Please add the object without options num_rows and num_cols.

SEE ALSO

add_to_rp_group(2)

RPGP-071 (Error) The alignment bottom-right and bottom-pin are not supported for multiple column cell.

DESCRIPTION

A RP cell is allowed in multiple columns of a relative placement group. Only bottom-left alignment is supported for such kind of cells. This error gets issued when bottom-right or bottom-pin alignnment is being set on multiple column cell or on the relative placement group which contains multiple column cell.

WHAT NEXT

Please add the multiple column cell to the relative placement group with bottom-left alignment, using option -alignment of command add_to_rp_group.

SEE ALSO

add_to_rp_group(2)

RPGP-072 (Error) The multiple location cell is not supported with compress mode.

DESCRIPTION

The options -num_rows and -num_columns of command add_to_rp_group can be used to add a cell in multiple locations of relative placement group. The compress mode is not allowed for the relative placement group that contains multiple location cell.

WHAT NEXT

Please either remove compress mode from RP group using remove_rp_group_options command or try to add cell again with no multiple locations.

SEE ALSO

create_rp_group(2)
add_to_rp_group(2)
set_rp_group_options(2)
remove_rp_group_options(2)

RPGP-074 (error) Width or height for space keepout %s need to be specified.

DESCRIPTION

This error message occurs when the **add_to_rp_group** command detects that either you have not specified width or height (or both) for a space keepout or the corresponding values are not greater than zero.

WHAT NEXT

Choose appropriate value for keepout height and width and rerun the command.

SEE ALSO

add_to_rp_group(2)

RPGP-075 (information) The bottom-pin alignment is being ignored for multiple location cell '%s'.

DESCRIPTION

A RP cell is allowed in multiple columns of a relative placement group. Only bottom-left alignment is supported for such kind of cells.

WHAT NEXT

Please add the multiple column cell to the relative placement group with bottom-left alignment, using option -alignment of command add_to_rp_group.

SEE ALSO

add_to_rp_group(2)

RPGP-076 (information) No pin named "%s" exists in cell "%s" in RP group "%s". Pin alignment will be ignored for this cell.

DESCRIPTION

The pin align name specified for the given leaf cell, either set on the RP group or set on the leaf cell, does not exist. Hence the pin alignment will not be honored

for this cell.

WHAT NEXT

Please check the pin align name specified for the leaf cell and the RP group. You may specify the pin align name for the leaf cell via the set_attribute command or you can specify the pin align name of the RP group by using -pin_align_name option in the set_rp_group_options command.

SEE ALSO

set_attribute(2)
set_rp_group_optiomns(2)

RPGP-077 (information) The list specified for check_rp_groups contains a hierarchical RP group "%s" which will be ignored.

DESCRIPTION

check_rp_groups checks and reports failures on only top-level relative placement groups, not on hierarchical RP groups.

WHAT NEXT

Please use check_rp_groups for the parent RP group of a hierarchical RP group to find out the failures.

SEE ALSO

check_rp_groups(2)
write_rp_groups(2)

RPGP-078 (information) There are no RP group failures in the specified RP groups.

DESCRIPTION

This message occurs when the check_rp_groups command finds no RP failure on top-level RP groups in the specified list. Notice that errors on hierarchical RP groups will also be reported on the top-level group.

WHAT NEXT

SEE ALSO

check_rp_groups(2)

RPGP-079 (warning) The cell '%s' is not in any relative placement group.

DESCRIPTION

This error message occurs when the **all_rp_references** command detects that the specified cell name is not in any relative placement group either as a cell or as a hierarchical cell for relative placement instantiation.

WHAT NEXT

Check the spelling of the cell name and make sure that the specified cell is in a relative placement group.

SEE ALSO

all_rp_references(2)

RPGP-080 (information) The variable '%s' will be obsolete in ICC release '%s'. There will not be any alternative to control the funtionality.

DESCRIPTION

The variable will not be available from the displayed release onwards.

WHAT NEXT

Please contact Synopsys if you still need the funtionality executed by variable.

SEE ALSO

create_rp_group(2)

RPGP-081 (information) The variable '%s' will be obsolete in next ICC release. The associated functionality is being provided using 'orient_opt' option of relative placement group.

DESCRIPTION

The variable will not be available from the displayed release onwards.

WHAT NEXT

Please set **orient_opt** option of relative placement group using the command **create_rp_group** or **set_rp_group_options**, instead of using the variable.

SEE ALSO

create_rp_group(2)
set_rp_group_options(2)

RPGP-082 (information) The command '%s' will be obsolete in next ICC release. The associated functionality is being provided using 'orient_opt' option of relative placement group.

DESCRIPTION

The command will not be available from the displayed release onwards.

WHAT NEXT

Please use **orient_opt** option of relative placement group using the command **create_rp_group** or **set_rp_group_options**, instead of commands to disable/enable orientation optimization.

SEE ALSO

create_rp_group(2)
set_rp_group_options(2)

RPT-1 (warning) Reports may be inaccurate and/or incomplete due to interrupt.

DESCRIPTION

WHAT NEXT

RPT-2 (warning) %d unresolved references are not included in this report.

DESCRIPTION

WHAT NEXT

RPT-3 (warning) No timing information for '%s'.

DESCRIPTION

WHAT NEXT

RPT-4 (information) Reported the %d requested paths; other

paths have identical delays.

DESCRIPTION

WHAT NEXT

RPT-5 (error) Illegal -%s list.

DESCRIPTION

WHAT NEXT

RPT-6 (error) No match for %s '%s'.

DESCRIPTION

WHAT NEXT

RPT-7 (information) This design contains unmapped logic.

DESCRIPTION

WHAT NEXT

RPT-8 (information) This design contains black box (unknown) components.

DESCRIPTION

This informative message is printed during report when the current design contains black box components. The purpose of the message is to remind users that the contents of black box components are not reported.

WHAT NEXT

RPT-9 (information) This design contains at least one timing loop at pin: '%s'.

DESCRIPTION

WHAT NEXT

RPT-10 (warning) Design '%s' has no schematic.

DESCRIPTION

WHAT NEXT

RPT-11 (error) This design has no %ss.

DESCRIPTION

WHAT NEXT

RPT-12 (warning) This design has no %s.

DESCRIPTION

WHAT NEXT

RPT-13 (warning) The replace_fpga command has been run on portions
of this design. Since replace_fpga replaces fpga resources by gates the

report you are about to see may not accurately convey table lookup usage
information. It is better to use report_fpga BEFORE replace_fpga.

DESCRIPTION

This error may be seen during **report_fpga**, if the **replace_fpga** command was used to replace programmable cells by gates in the design, before running the report. Since the programmable cells are no longer present in the design, their resource usage cannot be reported, and the resulting report will not be correct. As a methodology, it is best to run **report_fpga** BEFORE running **replace_fpga**.

WHAT NEXT

Use the **report_fpga** prior to using the **replace_fpga** command.

RPT-14 (error) A %s report can not be generated for %s designs.

DESCRIPTION

The named report command is not valid for the specified type of designs.

WHAT NEXT

Check the documentation for that specific report command to verify what types of designs it can accept. Also make sure that your design has been linked to the correct library.

RPT-15 (error) Conflicting inputs for the options '%s'.

DESCRIPTION

Some input option combinations are not legal.
For example, report_cache -larger 5 -smaller 5 is not allowed.

WHAT NEXT

RPT-16 (warning) Corrupt or unreadable pathname.
The problem is at the pathname '%s',
one of the components of the pathname, or one level below the pathname.
Aborting processing for this pathname.

DESCRIPTION

A file or directory is nonexistent, unreadable, or has the wrong format.

WHAT NEXT

Remove the entire directory structure that contains the corrupted cache. Examine for corrupted format the pathname, its components, and the files one level below. Use the UNIX **ls -l** command. Examine filename formats of similar files. Frequently the *cache_read* or *cache_write* variable lists directory X as a cache directory, but the directory X/synopsys_cache_v*.* does not exist.

RPT-17 (warning) Missing synthetic library information for the cache entry
'%s'.
This report will use parameter names like 'unknown_param_1'.

DESCRIPTION

There is no information about this cache entry from the files listed in the synthetic_library variable. Frequently, an entry will be written into the cache when
a specific .sldb file is included in synthetic_library.
But later, when the cache is searched, that file is not
included so the number of parameters is unknown.

WHAT NEXT

Use report_lib to examine the contents of .sldb files.
Place the .sldb file that contains the cache entry into
the synthetic_library variable.

RPT-18 (error) Syntax error in -parameters input option at or near '%s'.

DESCRIPTION

Error occurred while parsing or interpreting the user's input option for -parameters.

WHAT NEXT

See man page for the command.

RPT-19 (warning) Inconsistent number of parameters for the cache entry '%s'. This report will use parameter names like 'unknown_param_1', if there are parameters.

DESCRIPTION

There is an inconsistency between the number of parameters found in the cache directory and the number of parameters defined for the module in the synthetic library (.sldb file). The corresponding synthetic library may not be defined in the *synthetic_library* variable, or the cache directory structure could be corrupted.

WHAT NEXT

Check that the module's .sldb file is listed in the *synthetic_library* variable. Use **report_synlib** to examine the parameters defined by the .sldb files. To see if this pathname differs from other pathnames, look at the cache directory structure.

RPT-20 (information) This design has been annotated with physical cluster hierarchy.

DESCRIPTION

The **read_clusters** command has been used to annotate onto this design physical cluster hierarchy information. Physical cluster hierarchy is used to direct the **reoptimize_design** command to optimize only those cells located in the same physical region on the chip. This leads to more predictable wiring delay estimates.

WHAT NEXT

RPT-21 (error) The report_clusters command cannot be specified for the design '%s', which has no physical cluster hierarchy.

DESCRIPTION

No physical cluster hierarchy has been associated with the design. The **report_clusters** command makes sense only when physical cluster hierarchy information is present on a design.

You can use the **read_clusters** command to annotate physical cluster hierarchy information onto a design. Physical cluster hierarchy is used to direct the **reoptimize_design** command to optimize only those cells located in the same physical region on the chip. This leads to more predictable wiring delay estimates.

WHAT NEXT

RPT-22 (error) The design '%s' has no cluster named '%s'.

DESCRIPTION

No physical cluster of the name given is associated with the current design.

WHAT NEXT

Use the **report_clusters** command to list all the valid names, and reissue the command.

RPT-23 (error) The -cells option can be supplied only if a -cluster is specified.

DESCRIPTION

Only the cells contained within a cluster may be listed with the report_clusters command.

WHAT NEXT

RPT-24 (warning) Problems encountered with removing the file or directory
'%s'.

DESCRIPTION

The attempt to remove the file or directory failed.

WHAT NEXT

Look at the protection modes of the file and its directory.

RPT-25 (error) Clock '%s' cannot be used for all_registers because it has no period.

DESCRIPTION

The **all_registers -clock** *clock_name* command only works when the specified clock has a valid period. This is because the timing verifier needs to know the periodic waveform of a clock object.

WHAT NEXT

Use **create_clock -period** *period_value* **-waveform** *waveform_spec object_list* to describe the clock properly, then reissue the **all_registers** command.

RPT-26 (error) Unable to find clock '%s'.

DESCRIPTION

The timing verifier was unable to find the specified clock.

WHAT NEXT

Use **report_clock** to see if the clock is described correctly. Use

report_transitive_fanout -clock_tree to list the transitive fanout of the clock sources.

RPT-27 (warning) Some clocks have no period defined. These clocks will not be considered for timing.

DESCRIPTION

Some of the clocks in the design do not have a period defined. To affect timing of the design, a period is required for the clock.

WHAT NEXT

To set a period on a clock, use **create_clock -period** or **max_period**. The period value must be zero or greater.

RPT-30 (error) Cannot find wire load '%s' in design '%s'.

DESCRIPTION

The **report_wire_load** command could not be executed because the wire-load model defined could not be found on the design or in the libraries linked to the design.

WHAT NEXT

Use **report_wire_load** to list the wire-load models on the design and its clusters. Use **list link_library** to list the link library, and use **report_lib** to list the wire-load models in a library.

RPT-31 (warning) There is no porosity information in library '%s'.

DESCRIPTION

The **report_routability** command reports the "porosity" of the current design. The named library does not contain porosity information. Porosity is a measure of the number of channels available for routing over the cells in the design. Some technologies, such as FPGA, do not have porosity information in their libraries. Standard cells and gate-array technology libraries do contain porosity information.

WHAT NEXT

If you have Library Compiler, add the porosity information for each cell. If you don’t have Library Compiler, contact the owners of the library and ask them to include porosity information in their next library release.

RPT-32 (warning) There is no porosity information in link libraries.

DESCRIPTION

The **report_routability** command cannot report the "porosity" of the design because the libraries on the link path do not contain porosity information. Porosity is a measure of how many channels are available for routing over the cells in the design. Some technologies, such as FPGA, do not have porosity information in their libraries. Standard cells and gate-array technology libraries do contain porosity information.

WHAT NEXT

If you have Library Compiler, add the porosity information for each cell in the libraries on the link path. If you don’t have Library Compiler, contact the owners of the link libraries and ask them to include porosity information in their next library release.

RPT-33 (error) Could not find the specified %s pin.

DESCRIPTION

This error will be seen during **report_delay_calculation** if the specified pin can not be found in the current design.

WHAT NEXT

Check the current design to see if the pin name was entered correctly.

RPT-34 (error) Library cell delay information is protected.

DESCRIPTION

This error is seen during **report_delay_calculation** if the technology library associated with a cell delay arc has not been loaded with the read_lib command or if

the technology library does not have the library feature report_delay_calculation enabled.

WHAT NEXT

Load the ASCII version of the library with the read_lib command or modify the library source to add the library feature report_delay_calculation.

RPT-35 (error) There is no cell or net delay arc between pins '%s' and '%s'. The pins must be on the same net or the same cell.

DESCRIPTION

This error will be seen during **report_delay_calculation** if there is not delay arc (either a net arc or a cell arc) between the 'from' and 'to' pins given to this command. The specified pins should be driver and load pins on the same net to see a net delay arc calculation, and should be input and output pins of a cell to see the details of a cell delay arc calculation.

WHAT NEXT

Check the pin names against those in the design to see if they were specified correctly.

RPT-36 (error) There is no library associated with the cell attached to the 'to' pin.

DESCRIPTION

This error will be seen during **report_delay_calculation** if pins on a non-leaf cell are specified for cell delay arc. Cell delay data is only available for leaf cells from a technology library.

WHAT NEXT

Move down the design hierarchy to a leaf cell.

RPT-37 (error) Must specify exactly one '%s' pin for this

command.

DESCRIPTION

This error will be seen during **report_delay_calculation** if more than one pin is specified via either the -from or -to options.

WHAT NEXT

Try again, specifying exactly one pin for both the -from, and -to options.

RPT-38 (error) Timing arc type '%s' is not supported for this command.

DESCRIPTION

This error will be seen during **report_delay_calculation** if delay information is requested for an unsupported arc type. Supported arc types include: . See the Library Compiler manual for details about arc types.

WHAT NEXT

RPT-40 (warning) The '-insts' option is available only with a TestManager license.
It will be ignored.

DESCRIPTION

The '-insts' option on 'report_test -faults' and 'report_test -coverage' is not available without a TestManager license.

WHAT NEXT

RPT-41 (warning) The faults annotated on the design are being

ignored.

DESCRIPTION

The design has fault information annotated on it. This is probably because the 'atpg_keep_faults_data' variable was set when writing out the design. This variable is not supported with the TestManager and the faults on the design will be ignored.

WHAT NEXT

The 'restore_test' command provides a much more powerful and flexible mechanism to save fault information.

RPT-42 (warning) Constraint generation interrupted. Constraint file may be incomplete or inaccurate.

DESCRIPTION

Constraint generation was interrupted by Ctrl-C from the keyboard. Constraints will still be written out but the generated file may be incomplete or inaccurate.

WHAT NEXT

The safest course of action is to re-run write_constraints without interruption. However, if the constraint file is manually validated and appears correct, you can probably use it.

RPT-45 (warning) The value for '%s' must be between '%s' and '%s'.
Using default value of '%s' instead.

DESCRIPTION

The value specified is out of range. A default value was used instead.

WHAT NEXT

Enter the command again with a number in the range if the default was inappropriate.

RPT-46 (warning) Command specific default precision will be used while performing report.

DESCRIPTION

The variable report_default_significant_digits is set to a value -1. This causes command specific default precision to be used while reporting, on the listed report commands.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

report_cell (2), **report_constraint** (2), **report_clock_gating_check** (2), **report_net** (2), **report_path_budget** (2), **report_port** (2), **report_qor** (2), **report_timing** (2), **write_constraints** (2), **write_sdf** (2).

RPT-50 (error) Could not report timing and area information for the cache model due to missing %s.

DESCRIPTION

You receive this error message because you specified the **-statistics** option of the **report_cache** command. But missing from the search path are one or more synthetic libraries specified in the synthetic library list or one or more target libraries specified in the synlib target library list of the cached models.

WHAT NEXT

Verify that all specified synthetic libraries and target libraries are available in the search path.

SEE ALSO

report_cache (2).

RPT-51 (Information) report_cache -statistics implies that only

cached models will be reported.

DESCRIPTION

You receive this informational message because you have specified the **-statistics** option with the **report_cache** command. This means that only cached models will be reported.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

report_cache (2).

RPT-52 (error) Could not find module '%s' or implementation '%s' in the synthetic libraries.

DESCRIPTION

You receive this error message because you executed the **report_cache** command with the **-statistics** option, and the module or implementation of the cached model is not in the synthetic libraries.

WHAT NEXT

Add to the synthetic library list the synthetic library used at the creation of the cache model.

SEE ALSO

report_cache (2).

RPT-53 (error) Could not read the cache entry '%s'.

DESCRIPTION

You receive this error message when you execute the **report_cache** command and the cache entry is either not readable or corrupted.

WHAT NEXT

Verify that the entry is available.

SEE ALSO

report_cache (2).

RPT-54 (Error) -voltage and/or -temperature options are supported only in multi-voltage mode.

DESCRIPTION

Voltage and temperature options can be used only when design is multi voltage. Multi voltage design contains blocks specified with different operating conditions.

WHAT NEXT

RPT-77 (error) Cell '%s' is invalid for scan. %s.

DESCRIPTION

The error shows an issue with scan-replacement or scan-insertion.

WHAT NEXT

You need to check the specification and configuration settings and see if something is wrong.

RPT-78 (Information) There are '%d' more cells with the same error.

DESCRIPTION

The error shows an issue with scan-replacement. This accompanies RPT-77 message.

WHAT NEXT

You need to check the RPT-77 message shown before this to see the actual error.

RPT-79 (warning) Cell ’%s’ is not valid for scan. %s.

DESCRIPTION

The warning shows an issue with scan-replacement or scan-insertion. This may nt be critical for scan-insertion.

WHAT NEXT

You need to check the specification and configuration settings and see if something is wrong.

RPT-80 (Information) All the ’%d’ sequential cells are valid for scan.

DESCRIPTION

The message shows that all sequential cells are valid after scan-replacement or or scan-insertion.

WHAT NEXT

RPT-81 (Warning) Relative Scope of the object "%s" not reported as the object lies in a higher logical scope.

DESCRIPTION

This message warns that one of the object whose relative scope is being reported is above the current logical level of hierarchy.

WHAT NEXT

RPT-90 (error) The options -bucket_range and -bucket_number are mutually exclusive.

DESCRIPTION

Both options -bucket_range and -bucket_numbers were used in the report_histogram

command.

WHAT NEXT

Please use either the **-bucket_range** or the **-bucket_number** option. The **-bucket_range** option allows you to specify the slack range for one bucket (in library units). The **-bucket_number** option allows you to specify how many buckets should be used in the histogram.

RPT-91 (error) The value of the -bucket_number option should be at least 1.

DESCRIPTION

The option **-bucket_number** was used with an argument smaller or equal to 0.

WHAT NEXT

Please use a positive, non-zero number for the option **-bucket_number**. This option defines how many buckets will be used in the histogram.

RPT-92 (error) %s is not an active scenario.

DESCRIPTION

The option -scenario was used and one of the scenarios given was not recognized as an active scenario.

WHAT NEXT

Please check that all the scenario names used are valid scenario names. Please use the command **set_active_scenarios** to activate any scenarios used that are currently inactive.

RPT-93 (error) options define empty range.

DESCRIPTION

The options **-range_maximum** and **-range_minimum** were used and their values define an empty range.

WHAT NEXT

Please check that the value given for the option **-range_maximum** is larger than the value given for the option **-range_minimum**.

RPT-101 (error) Can not find PatternExec with name '%s'.

DESCRIPTION

The error occurs when you run the command **report_fault** but the pattern exec name you specified does not exist in the CTL model.

WHAT NEXT

You need to check the CTL model and specify the correct pattern exec name. The pattern exec name should NOT be quoted.

RPT-102 (warning) Can not find the corresponding core instance for pattern '%s".

DESCRIPTION

In the top level CTL model, each pattern should be correspondent to one core instance. You receive this error message when the corresponding core instance can not be found.

WHAT NEXT

You need to check the CTL model to see if the pattern block was named correctly.

RPT-103 (warning) Can not find top level pattern instance for design '%s'.

DESCRIPTION

You receive this error message when you execute command **report_fault** to report fault coverage for the design, but the CTL model of this design does not contain the top level pattern instance. For core designs, the top level pattern instance is used to test the core. For top level deisgn, the top level pattern instance is used to test the UDL logic at top level.

WHAT NEXT

You need to check the CTL model to see if the top level pattern instance is there and the domain references for top level pattern instance are consistent with those defined in the environment block.

RPT-104 (warning) No pattern info found for pattern '%s'. The fault coverage report may be inaccurate.

DESCRIPTION

You receive this error message when you execute command **report_fault** to report overall fault coverage for the design, but the pattern referred does not have associative pattern infomation. So, the overall fault coverage report may be inaccurate.

WHAT NEXT

You need to read in the corresponding patinfo file for pattern.

SEE ALSO

read_pattern_info (2).

RPT-105 (error) The CTL model does not include valid patinfo.

DESCRIPTION

You receive this error message when you execute command **report_fault** to report overall fault coverage for the design, but the CTL model for the design does not have patinfo or the patinfo included is invalid.

WHAT NEXT

You need to check the CTL model for those patinfo block to see if they are there and valid.

RT-001 (error) Cannot find Astro executable file, Astro router failed.

DESCRIPTION

WHAT NEXT

Please make sure that "Astro" command is in your search path.

RT-002 (error) write_mdb failed.

DESCRIPTION

When each time 'route' command is called, internally we will call 'write_mdb' and 'read_mdb' command. Astro router will not run if 'write_mdb' failed.

WHAT NEXT

Please check messages from 'write_mdb' and fix the problems first before calling 'route' command.

RT-003 (error) read_mdb failed.

DESCRIPTION

When each time 'route' command is called, internally we will call 'write_mdb' and 'read_mdb' command. After Astro finishes, we call 'read_mdb' command. This message tells you that 'read_mdb' failed and routing data did not get read back.

WHAT NEXT

Please check messages from 'read_mdb' and fix the problems first before calling 'route' command.

RT-004 (error) Astro router failed, please check file '%s' for error

messages.

DESCRIPTION

Astro router failed and routing data did not get read back.

WHAT NEXT

Please check the log file for Astro running results.

RT-005 (error) Incorrect option combination.

DESCRIPTION

The options you specified for 'route' command are wrong combinations.

WHAT NEXT

Check 'route' command syntax.

RT-006 (error) Failed to save CEL "%s".

DESCRIPTION

This error message indicates that the design CEL could not be saved into the Milkyway library. The reasons for this could be one of the following.

- No write permission for the Library/CEL.
- No disk space is available.

WHAT NEXT

Please check that the Milkyway design library and CEL are writeable and that there is sufficient disk space available.

RT-007 (error) Unknown parameter %s found.

DESCRIPTION

The parameter you specified is not defined for the command.

WHAT NEXT

Check the command syntax.

RT-008 (error) %s is obsolescent, please use %s.

DESCRIPTION

The command is no more used, please use the new one.

WHAT NEXT

Update script with the new key word.

RT-011 (error) Can not use -effort_level option.

DESCRIPTION

WHAT NEXT

Check 'route' command syntax.

RT-012 (error) Wrong effort level specified.

DESCRIPTION

-effort_level allows you to specify "fast", "medium" or "slow". You specified a effort name other than these three names.

WHAT NEXT

Use the right effort level name and rerun this command again.

RT-013 (error) Cannot use -groute_timing_effort option.

DESCRIPTION

When you use the **route** command **-groute_timing_effort** option, you must specify an effort level of low, medium or high, and include the **-global**, **-eco_global**, or **-signal** option.

WHAT NEXT

Check the **route** command syntax for the correct use of the option.

SEE ALSO

route (2).

RT-014 (error) Wrong timing effort level specified.

DESCRIPTION

The **route** command allows you to specify the timing effort level as low, medium or high with the **-groute_timing_effort** and the **-track_assign_timing_effort** options. Only low, medium and high are accepted level names.

WHAT NEXT

Correct the timing effort level name and run the command again.

SEE ALSO

route (2).

RT-015 (error) Wrong crosstalk effort level specified.

DESCRIPTION

-xtalk_effort allows you to specify "low", "medium" or "high". You specified a crosstalk effort name other than these three names.

WHAT NEXT

Use the right crosstalk effort level name and rerun this command again.

RT-016 (error) File '%s' does not exist or it is unreadable.

DESCRIPTION

When using the **-scheme_rail**, **-scheme** or **-post_scheme** option of the **route** command, specify a file name that exists and that is readable.

WHAT NEXT

Check that the file exists and that the correct access permission is set.

SEE ALSO

route (2).

RT-017 (error) Option -track must be combined with -global or -eco_global option.

DESCRIPTION

WHAT NEXT

Check 'route' command syntax.

RT-018 (error) Invalid value specified for '%s' option.

DESCRIPTION

WHAT NEXT

Check 'set_astro_routing_options' command syntax.

RT-019 (error) Cannot use -track_assign_timing_effort option.

DESCRIPTION

When you use the **route** command **-track_assign_timing_effort** option, you must also specify the **-track** or **-signal** option.

WHAT NEXT

Check the **route** command syntax for the correct use of the option.

SEE ALSO

route (2).

RT-020 (error) insert_metal_filler expects a list with option "%s".

DESCRIPTION

You should provide a list of layer name and number for this option.

WHAT NEXT

Check "insert_metal_filler" command syntax.

RT-021 (error) Failed to get %s from %s. %s

DESCRIPTION

This error message is for command signoff_metal_fill. The command failed to get necessary information from your inputs. The reason might be:

1. There is no GRAPHICS/GRAPHICS_NETLIST/WRITE_MILKYWAY command in your runset.

2. There is no layer assignment in your GRAPHICS/GRAPHICS_NETLIST/WRITE_MILKYWAY command.

3. The layer assignment in your runset is not consistent with MW database or the map file.

WHAT NEXT

Please

1. Add GRAPHICS/GRAPHICS_NETLIST/WRITE_MILKYWAY command in your runset.

2. Make sure the GRAPHICS command in your input runset is not commented out. Then, parse your runset by running "evp -O parsed_fill_runset.ev original_fill_runset.ev", and then re-run signoff_metal_fill with the runset "parsed_fill_runset.ev".

3. Make sure the layer numbers in your runset are consistent with those in MW database, or specify a map file.

Please refer to the man page of the command for more information.

RT-022 (error) %s has not been specified.

DESCRIPTION

The command failed since you did not specify necessary inputs. You may specify the inputs by the options of this command, or via another command prior to executing this command.

WHAT NEXT

Specify necessary inputs and then execute this command again. Please refer to the man page of the command for more information.

RT-023 (error) The number of density rules of layer '%s' in technology file exceeds the maximum number %d.

DESCRIPTION

The number of density rules of the specified layer in the technology file exceeds the maximum number of density rules.

WHAT NEXT

Please use "write_mw_lib LIB_NAME -technology -output TECH.tf", and then open TECH.tf to check and fix the setting of DensityRule. Then, use "set_mw_technology_file LIB_NAME -technology TECH.tf" to replace the technology file as the correct one.

RT-031 (error) Maximum layer name must be on the top of minimum layer name.

DESCRIPTION

This error message occurs when running the **set_net_routing_layer_constraints** command with the **-min_layer_name** and **-max_layer_name** options incorrectly specified.

Specify the **-max_layer_name** with a higher layer than **-min_layer_name** as shown in the following example:

-min_layer_name = m1 (first routing layer)
-max_layer_name = m3 (third routing layer

The error message occurs if you reversed the values in the example above.

WHAT NEXT

Correct the values specified for the **-min_layer_name** and the **-max_layer_name**, and then run the command again.

SEE ALSO

set_net_routing_layer_constraints (2).

RT-032 (error) Specified via '%s' does not exist in physical library.

DESCRIPTION

You receive this message because you are trying to use a via that does not exist in physical library.

WHAT NEXT

RT-033 (error) Specified via '%s' is not a default via.

DESCRIPTION

You receive this message because you are trying to use a via which is a non-default via in physical library.

WHAT NEXT

RT-034 (error) Syntax error in '%s' option.

DESCRIPTION

You receive this message because you used a wrong command option syntax.

WHAT NEXT

Check the command syntax from the man page and use correct syntax.

RT-035 (error) Taper level must be equal or larger than 0.

DESCRIPTION

You receive this message because you used a taper level smaller than 0.

WHAT NEXT

Check the command syntax from the man page and use correct value.

RT-036 (error) Layer ’%s’ does not exist in design.

DESCRIPTION

You receive this message because you used a layer that does not exist in design.

WHAT NEXT

Check the layers from the design and use the right routing layer name.

RT-037 (error) Specified via ’%s’ does not exist in reference routing rule ’%s’.

DESCRIPTION

You receive this message because you are trying to use a via that does not exist in the reference routing rule.

WHAT NEXT

RT-038 (error) There are two vias (%s and %s) corresponding

to same layer level in one routing rule, it’s not allowed.

DESCRIPTION

You receive this message because you are trying define two vias that corresponding to same layer level. For example: two vias for M1 and M2. In one routing rule, it is not allowed. syntax.

WHAT NEXT

RT-039 (info) Creating routing rule (%s) failed.

DESCRIPTION

Creating routing rule failed. Please check the -via_cuts list, if there are more than one vias for same layer level, that is the reason. For example: there are two vias for metal1 and metal2.

WHAT NEXT

RT-040 (error) %s option is incorrect.

DESCRIPTION

Creating routing rule failed. Please check the option list. You can use m1 to m15 to represent metal layers; however, ap cannot represent ap layer; only m1 to m15 are legal expressions

WHAT NEXT

RT-041 (error) Please specify target nets!

DESCRIPTION

Routing cannot be done without target nets.

WHAT NEXT

RT-042 (error) Please specify one net only!

DESCRIPTION

Neighbor sweeping can have one target net only.

WHAT NEXT

RT-043 (error) The number of CPUs should be greater than or equal to 1.

DESCRIPTION

You receive this message because you used number of CPUs smaller than 1.

WHAT NEXT

Check the command syntax from the man page and use correct value.

RT-044 (error) Invalid bounding box specified.

DESCRIPTION

You receive this message because the coordinates of a bounding box are not given in order from the lower-left corner to the upper-right corner.

WHAT NEXT

Place the lower-left corner coordinates before the upper-right corner coordinates, and ensure that it forms a valid bounding box.

RT-045 (warn) The options '%s' and '%s' are mutually exclusive.

'%s' option will be ignored.

DESCRIPTION

This warning message occurs when you use two options which are mutually exclusive.

WHAT NEXT

Please refer to the man page for the command for more information.

RT-046 (error) Illegal error cell name.

DESCRIPTION

You receive this message because the specified error cell name is illegal.

WHAT NEXT

Please check the command syntax from the man page and use correct error cell name.

RT-047 (info) Create error cell %s ...

DESCRIPTION

This information message notifies you that a new error cell will be created if it does not exist in physical library.

WHAT NEXT

This is an informational message only. No action is required on your part.

RT-048 (info) No DRC error is reported!

DESCRIPTION

This information message notifies you that there is no DRC violation after running this command.

WHAT NEXT

This is an informational message only. No action is required on your part.

RT-049 (error) Cannot find %s from user path.

DESCRIPTION

You receive this message because the executable is missing.

WHAT NEXT

Please run this command after setting environment of the executable.

RT-050 (error) Failed in executing %s.

DESCRIPTION

Command has failed.

WHAT NEXT

Please check the log file and correct any errors reported.

RT-051 (info) Use machine '%s' to run Astro.

DESCRIPTION

WHAT NEXT

RT-052 (info) The placement is illegal, but we will continue to run Astro router.

DESCRIPTION

Since the placement is illegal, you may end up with DRC violations after running Astro router.

WHAT NEXT

Run ’legalize_placement’ before calling ’route’ command.

RT-053 (info) Running Astro rail router ...

DESCRIPTION

WHAT NEXT

RT-054 (info) Running Astro clock detail router ...

DESCRIPTION

WHAT NEXT

RT-055 (info) Running Astro global router ...

DESCRIPTION

WHAT NEXT

RT-056 (info) Running Astro incremental global router ...

DESCRIPTION

WHAT NEXT

RT-057 (info) Running Astro track assignment ...

DESCRIPTION

WHAT NEXT

RT-058 (info) Running Astro detail router ...

DESCRIPTION

WHAT NEXT

RT-059 (info) Astro router finished successfully, please check file '%s' for detail Astro running results.

DESCRIPTION

WHAT NEXT

RT-060 (info) Running Astro router with customer scheme file.

DESCRIPTION

This information message notifies you that the customer Astro router is using the customer scheme script and the only other option you can use is the **-overwrite** option.

WHAT NEXT

This is an informational message only. No action is required on your part.

You can refer to the **route** command syntax for the correct use of the option.

SEE ALSO

route (2).

RT-061 (warn) The width of m%d (%d)is defaultwidth %d.

DESCRIPTION

Please make sure if you want to apply default width on stack-via creating. You can use set_route_flip_chip_options to set the width of stack-vias.

WHAT NEXT

RT-062 (warning) Port at [%f,%f..%f,%f], layer(%s), is completely blocked by fixed obstructions (net %s)

DESCRIPTION

This message is produced by the check_routeability command when it detects that a pin is completely blocked by fixed obstructions. Since the fixed obstructions cannot be changed during routing, it will be impossible for the router to connect the port without causing at least one DRC violation.

WHAT NEXT

The pin and/or some fixed obstruction must be moved. Examine the port in the GUI and determine how to correct the problem by modifying the floorplan, placement, clock tree routing, etc.

SEE ALSO

check_routeability(2)

RT-063 (warning) The design cannot be cleanly routed because it has %d completely blocked ports

DESCRIPTION

This message is produced by the check_routeability command when there are one or more blocked ports. For each of the blocked ports summarized by this message, check_routeability also produced an RT-062 message.

WHAT NEXT

Find the RT-062 messages that precede this message in the log. Those messages give more detailed information about each of the ports that are blocked.

SEE ALSO

check_routeability(2)

RT-064 (warning) The design has already been assigned layer

constraints and we will overwrite the constraints.

DESCRIPTION

WHAT NEXT

RT-065 (warning) Net ’%s’ has already been assigned ’%s’ routing rule and we will overwrite the constraints.

DESCRIPTION

WHAT NEXT

RT-066 (warning) The ’%s’ via enclosure width is less than NDR width constraint of ’%s’ layer.

DESCRIPTION

```
You receive this message because the via enclosure width is less than NDR width
constraint of the layer. Zroute may report "Less than NDR width" violation for these
via enclosure.
```

WHAT NEXT

```
Please increase NDR via enclosure to meet metal layer NDR width.
```

RT-067 (error) Must specify at least one route type.

DESCRIPTION

```
You receive this message because no route type was specified in the command.
```

WHAT NEXT

```
Correct the option.
```

RT-068 (error) The NDR %s width (%g) is greater than signal route max width (%g) of %s layer.

DESCRIPTION

You receive this message because the NDR wire width or shield width is greater than signal route max width of the layer.

WHAT NEXT

Correct the option.

RT-070 (warning) There is no via landing solution in Port (%s,%s)

DESCRIPTION

All pins of the port may have design-rule (min-spacing, min-width) violations or may be blocked in all directions.

WHAT NEXT

Please open the layout and check if the FRAME view is ok. Please check via-regions, blockages and pins of the port to see if the blockage blocks all routable places or other geometry issues. Please check the layout of top design to see if there is any object blocking the pin. (Ex. P/G straps...) Please check if standard cells overlap.

RT-080 (info) %s

DESCRIPTION

As described in the message.

WHAT NEXT

This is for your information.

RT-101 (warning) Option -scheme_rail will be ignored because

-rail is specified.

DESCRIPTION

WHAT NEXT

RT-102 (warning) Can not use machine '%s' to run Astro.

DESCRIPTION

When you run Astro on a remote machine, you must make sure that the machine is accessible.

WHAT NEXT

We will use the current machine to run Astro. If you really want to run Astro on the remote machine, please specify the correct name and make sure that you can access the remote machine.

RT-103 (warning) All other options will be ignored since -default is specified.

DESCRIPTION

You get this message because when you specify options for Astro routing, -default is used, so all of the other options will be ignored.

WHAT NEXT

You need to reset those old options (if you have any) if you want to use those options to be kept.

RT-104 (warning) Net '%s' has already been assigned layer

constraints and we will overwrite the constraints.

DESCRIPTION

WHAT NEXT

RT-105 (warning) You are changing GCELL size, you may have potential problems if you want to run ECO global routing.

DESCRIPTION

WHAT NEXT

RT-106 (warning) You have specified init_scheme file in set_routing_options, and it will be overwritten by the same option in ’route’ command.

DESCRIPTION

WHAT NEXT

RT-107 (warning) File ’%s’ you specified in set_routing_options

does not exist or it is unreadable.

DESCRIPTION

WHAT NEXT

RT-110 (error) Net '%s' can not be found.

DESCRIPTION

WHAT NEXT

RT-111 (warn) set_route_type did not find any object to set route type.

DESCRIPTION

Just to let you know that set_route_type did not set route type for any object.

WHAT NEXT

Check "set_route_type" command syntax.

RT-112 (warn) Specified reference rule name does not exist.

DESCRIPTION

The specified reference rule name does not exist. Using default reference rule.

WHAT NEXT

Verify that the reference rule name has been defined.

RT-113 (warn) Net pattern did not match any nets.

DESCRIPTION

The net pattern specified did not match with any nets.

WHAT NEXT

Verify that the net pattern specified is correct.

RT-114 (warn) %s

DESCRIPTION

An unexpected failure has occured.

WHAT NEXT

Please notify your AC.

RT-115 (warn) %s

DESCRIPTION

Basic input error checking.

WHAT NEXT

Please recheck the command inputs and use the -help option to verify the input is correct.

RT-116 (warn) %s

DESCRIPTION

Command has failed.

WHAT NEXT

Please check the log file and correct any errors reported.

RT-117 (error) Invalid route type specified.

DESCRIPTION

You receive this message because you used an invalid route type. The valid values for route types are user_enter, signal_route_detail, clk.

WHAT NEXT

Check the command syntax from the man page and use correct value.

RT-118 (error) Cannot get current working directory.

DESCRIPTION

You receive this message because the current working directory cannot be found.

WHAT NEXT

Check whether current working directory exists and permission of the directory.

RT-119 (error) %s

DESCRIPTION

An unexpected error has occured.

WHAT NEXT

Please check the log file and correct any errors reported.

RT-120 (error) %s

DESCRIPTION

Basic input error checking.

WHAT NEXT

Please recheck the command inputs and correct any errors reported in the log file.

RT-131 (error) Some setting(s) in technology file is(are) not correct.

DESCRIPTION

Incorrect setting in technology file can lead to catastrophic result and must be fixed. The possible reasons include: Some non-zero values are set to be zero. For example, the pitch, minSpacing and minWidth of each layer should never be zero. Some values are set to unreasonably large or small. For example, the minSpacing of certain layer is set to 10000 nm.

WHAT NEXT

Please use "write_mw_lib LIB_NAME -technology -output TECH.tf". Then open TECH.tf and correct the incorrect setting. Then use "set_mw_technology_file LIB_NAME -technology TECH.tf" to replace the technology file as the correct one.

RT-151 (warn) The P/G nets of the diode instances are not connected.

DESCRIPTION

There are opens in the P/G nets

WHAT NEXT

Please use "connect_pg_nets" command to connect P/G nets.

RT-152 (warn) geNewDRC only supports maxNumMinEdge = 1,

skip minEdgeLength checking.

DESCRIPTION

minEdgeLength checking will be skipped since maxNumMinEdge is not 1.

WHAT NEXT

As matter of fact, you should use verify_drc.

RT-153 (error) Antenna checking is not turned on.

DESCRIPTION

Antenna checking is not turned on. There will be no antenna checking.

WHAT NEXT

Please use "set_parameter doAntennaConx value" command or specify -signal_route_options.

RT-154 (error) Cannot find Hercules antenna report in database.

DESCRIPTION

The Hercules antenna report is missing.

WHAT NEXT

Please run antenna check with Hercules before using -antenna_check_engine Hercules option.

RT-155 (error) Unknown antenna_check_engine "%s".

DESCRIPTION

wrong antenna_check_engine is specified.

WHAT NEXT

Please check the antenna_check_engine option, it should be Internal or Hercules.

RT-156 (error) Failed to find spare diodes.

DESCRIPTION

no spare diodes in design.

WHAT NEXT

Please insert spare diode before using connect_spare_diode.

RT-157 (error) Failed to complete routing of spare diodes.

DESCRIPTION

eco routing failed.

WHAT NEXT

Please check the error message issued during eco route.

RT-158 (error) No cell is opened.

DESCRIPTION

No cell is opened.

WHAT NEXT

Please check cell name.

RT-159 (error) Unknown internal_check_option "%s".

DESCRIPTION

wrong internal_check_option is specified.

WHAT NEXT

Please check the internal_check_option option, it should be all or top_layer_only.

RT-160 (error) Unknown antenna violation file format "%s".

DESCRIPTION

wrong file format is specified.

WHAT NEXT

Please check the format opton, it should be Hercules.

RT-161 (error) Fail to get library Id.

DESCRIPTION

WHAT NEXT

RT-162 (error) Fail to delete the previous antenna report.

DESCRIPTION

WHAT NEXT

RT-163 (error) Fail to copy the new antenna report.

DESCRIPTION

WHAT NEXT

RT-164 (error) Fail to store the new antenna report.

DESCRIPTION

WHAT NEXT

RT-165 (error) Cannot create diode cell instance "%s".

DESCRIPTION

WHAT NEXT

RT-166 (error) Cannot get diode port instance ID of [%s,%s].

DESCRIPTION

WHAT NEXT

RT-167 (warn) Cannot freeze diode (%s) for ECO.

DESCRIPTION

WHAT NEXT

RT-168 (error) Cannot connect net (%s) and port (%s) in diode (%s).

DESCRIPTION

WHAT NEXT

RT-169 (error) Cannot update ECO file.

DESCRIPTION

WHAT NEXT

RT-170 (warn) Cannot set diode port [%s,%s] max route layer to (%s).

DESCRIPTION

WHAT NEXT

RT-171 (warn) Fail to attach diode instance cell to hier cell

instance.

DESCRIPTION

WHAT NEXT

RT-172 (warn) No antenna violation is found.

DESCRIPTION

WHAT NEXT

RT-201 (error) Internal error in global routing stage.

DESCRIPTION

This is an internal error.

WHAT NEXT

Contact your Synopsys CAE immediately.

RT-202 (error) Failed to find required node:Net %s

DESCRIPTION

Global router cannot find the required node of specified net.

WHAT NEXT

RT-203 (error) No more pins of net %s to route.

DESCRIPTION

Internal error in global routing stage.

WHAT NEXT

RT-204 (error) Internal error in global routing stage. Failed in %s

DESCRIPTION

This is an internal error in global routing stage.

WHAT NEXT

Contact your Synopsys CAE immediately.

RT-205 (error) Pin (%d %d) (%d %d) not on minGrid.

DESCRIPTION

Check tech file to see if this pin location is really not on minGrid.

WHAT NEXT

Check the input to Global route and find why the location is not on minGrid. It could be a bad input or a bug in the previous program.

RT-206 (warn) port %s in inst %s has no pin%s.

DESCRIPTION

WHAT NEXT

RT-207 (warning) zero pin of port (%s), inst (%s)

DESCRIPTION: Cannot connect the port because no pin is found.

WHAT NEXT: Please check the design to see if this is an unexpected issue.

RT-301 (info) MustJoin Pin (%s,%s,%d) = %d

DESCRIPTION

This is an informational message about MustJoin Pin.

WHAT NEXT

RT-302 (error) It is not recommended to use classic router commands after Zroute commands.

DESCRIPTION

Routing was done with Zroute on the current design. Now an attempt is made to run commands of classic router. This is not recommended because the DRC analysis and routing graph interpretations are different between the two routers.

WHAT NEXT

Continue to run all the routing commands in Zroute. If the intention to use the classic router for the flow, delete all the existing routes and start the flow with classic router.

RT-303 (WARNING) %s

DESCRIPTION

Router will continue to route. However there will be more tracks than defined by pitch of the layer. This may cause CPU, memory or QOR impact.

WHAT NEXT

Please fix the track definition if it is not intention for the design.

RT-401 (warn) Total number of fully blocked pins = %4d

DESCRIPTION

check_routeability has detected pins which are most likely inaccessible.

WHAT NEXT

Use error_browser to examine the blocked pins. If necessary, modified the design to enable access to these pins.

RT-402 (warn) %d pin have design-rule errors

DESCRIPTION

check_routeability has detected pins with design-rule violations and/or shorts.

WHAT NEXT

Use error_browser to examine the detected violations. If necessary, modified the design to enable access to these pins.

RT-403 (warn) Fat-merge at (%.2f %.2f, %.2f %.2f, %s) skipped. It has %d thin slices, out of %d rectangles

DESCRIPTION

Fat-merge has detected a geometry which has too many thin slices. The merging

process of this geometry is disabled, to save cpu time.

Fat-merge is a process which merges items in order to identify fat geometries.

Shapes with many thin slices may be generated by fracturing diagonal items, sometimes found at chip corners. A thin slice is a rectangle with width smaller than minWidth for its layer. "too many" means more than the number specified by ignoreFatMergeIfThinSlices (default is 80) and more than twice the number of non-thin rectangles in the same shape.

WHAT NEXT

Use gui to identify the skipped shape. If it may affect routing or verify_route results, you may set higher number for ignoreFatMergeIfThinSlices. For example, use: set_app_var droute_ignoreFatMergeIfThinSlices 120

Or set 0 to disable this Fat-merge skipping: set_app_var droute_ignoreFatMergeIfThinSlices 0

RT-501 (warn) fail to build %s stage congestion map.

DESCRIPTION

track / detail stage congestion map is not available for reporting.

WHAT NEXT

Please recheck the command inputs and make sure the design is track assigned or detail routed.

RT-502 (warn) %s

DESCRIPTION

WHAT NEXT

Please recheck the command inputs and make sure the design is verified.

RT-503 (warn) %s

DESCRIPTION

WHAT NEXT

Please recheck the command inputs and make sure the design is verified.

RT66-001 (error) Cannot detect current design name.

DESCRIPTION

You receive this message because no design has been loaded into the system.

WHAT NEXT

Load a design, and ensure that the **current_design** variable is defined.

SEE ALSO

current_design (3).

RT66-003 (error) Inconsistent database.

DESCRIPTION

You receive this message because an internal error has occurred in the design database.

WHAT NEXT

Attempt to reload the design database from the file.

RT66-004 (error) No physical library loaded.

DESCRIPTION

You receive this message because no library containing a physical description of the design has been loaded.

WHAT NEXT

Load the physical library.

RT66-005 (error) Cannot find library %s.

DESCRIPTION

You receive this message because the specified library cannot be found.

WHAT NEXT

Examine the library name and the **search_path** variable.

SEE ALSO

search_path (3).

RT66-006 (error) Cannot detect value of %s.

DESCRIPTION

You receive this message because the specified value is not defined.

WHAT NEXT

Define the value, and then start routing again.

RT66-007 (error) Preferred direction for routing layer '%s' is not defined.

DESCRIPTION

You receive this message because the preferred routing direction for the layer is not defined.

WHAT NEXT

Define the direction, and then start routing again.

RT66-008 (error) Class of site '%s' is not defined.

DESCRIPTION

You receive this message because the class (CORE or I/O) of the site is not defined.

WHAT NEXT

Define the site class, and then start routing again.

RT66-009 (error) Size of site '%s' is not defined.

DESCRIPTION

You receive this message because either the horizontal or vertical size of the site is not defined.

WHAT NEXT

Define the site size, and then start routing again.

RT66-010 (warning) Height and/or width of die area are undefined

DESCRIPTION

This message indicates that width and/or height of die area are not defined. Route66 requires these parametes.

WHAT NEXT

Define die width and die height and run route66 again.

RT66-011 (error) A shape object of unknown type detected.

DESCRIPTION

This message indicates an internal error in the design database.

RT66-012 (error) Routing segment of invalid direction is detected.

DESCRIPTION

You receive this message because an internal error has occurred in the design database.

RT66-013 (error) Invalid specification of ’%s’ detected.

DESCRIPTION

You receive this message because there is an internal error in the design database.

RT66-014 (error) Internal error.

DESCRIPTION

You receive this message because an internal error has occurred in the design database.

RT66-015 (error) Size of component ’%s’ is not defined.

DESCRIPTION

You receive this message because either the horizontal or vertical size of the component is not defined.

WHAT NEXT

Define the component size, and then start routing again.

RT66-016 (error) Offset of component ’%s’ is not defined.

DESCRIPTION

You receive this message because the offset of the component is not defined.

WHAT NEXT

Define the component offset, and then start routing again.

RT66-019 (error) Default routing width of layer '%s' is not defined.

DESCRIPTION

You receive this message because the default routing width of the layer is not defined.

WHAT NEXT

Define default routing width for the layer, and then start routing again.

RT66-020 (warning) Placement grid is not defined in horizontal direction.

DESCRIPTION

You receive this message because no site array is defined in the core area. If the design contains core components, the site array must be defined in the core area.

WHAT NEXT

Examine the design data.

RT66-021 (warning) Placement grid is not defined in vertical direction.

DESCRIPTION

You receive this message because no site array is defined in the core area. If the design contains core components, the site array must be defined in the core area.

WHAT NEXT

Examine the design data.

RT66-022 (error) Routing grid is not defined.

DESCRIPTION

You receive this message because the routing grid is not defined for the design.

WHAT NEXT

Define the routing grid, and then start routing again.

RT66-023 (error) Undefined reference: '%s' '%s'.

DESCRIPTION

You receive this message because a reference to a nonexistent object is detected.

WHAT NEXT

Check the data consistency.

RT66-024 (warning) Via '%s' has only one routing layer defined.

RT66-025 (warning) Via '%s' has more than two routing layers defined.

DESCRIPTION

WHAT NEXT

RT66-030 (error) Component '%s' is not defined in physical library.

DESCRIPTION

You receive this message because a component used in the netlist is not defined in the physical library.

WHAT NEXT

This message may appear in case of hierarchical presentation of the design. In this case, flatten the design using the **ungroup** command with the **-all** and **-flatten** options and the start router.

RT66-050 (error) Cannot open '%s' file.

RT66-051 (error) Cannot create '%s' directory.

RT66-053 (error) Cannot read from '%s' file.

RT66-055 (error) Cannot detect host name of current machine.

RT66-056 (error) Cannot open '%s' or '%s' file.

RT66-057 (error) The design is hierarchical. %s

DESCRIPTION

You receive this message because design is hierarchical.

WHAT NEXT

use command ungroup -all -flatten -force to remove all levels of hierarchy.

SEE ALSO

RT66-058 (error) The design database is incompleted. Cannot

open ’%s’ file.

DESCRIPTION

You receive this message because design database is incompleted. Some important files are missing.

WHAT NEXT

Please check the database.

SEE ALSO

RT66-059 (error) The directory ’%s’ is not existing or no read permission.

DESCRIPTION

You receive this message because the directory is not accessible. are missing.

WHAT NEXT

Please check if directory exist and permission of the directory.

SEE ALSO

RT66-060 (error) The directory ’%s’ is locked with process ID %d. %s

DESCRIPTION

You receive this message because the directory is locked.

WHAT NEXT

You can kill the process according the ID from the error message. Then the directory will be unlocked.

SEE ALSO

RT66-070 (error) Cannot find ’%s’ net.

RT66-071 (error) Error in routing ’%s’ control file is detected.

RT66-072 (error) Error in routing database file is detected.

DESCRIPTION

You receive this message because an internal error has occurred in the routing database.

RT66-101 (warning)

DESCRIPTION

This message may indicate an inconsistency in routing data.

RT66-102 (error)

DESCRIPTION

This message indicates an inconsistency in routing data.

RT66-103 (error)

DESCRIPTION

This message indicates that the flow cannot continue because of critical error.

RT66-104 (error) "Invalid index value %d in array with %d elements

"

DESCRIPTION

This message means some unexpected (for RtC) situation in the database.

When you see this message, please file a STAR and provide the data to let R&D reproduce and analyze the problem. R&D are working on creating a separate clear message for each of these situations.

RT66-105 (error) "Condition violated: %s, file %s, line %d
"

DESCRIPTION

This message means some unexpected situation in the soft.

When you see this message, please file a STAR and provide the data to let R&D reproduce and analyze the problem. R&D are working on creating a separate clear message for each of these situations.

RT66-106 (error) "Component ’%s’ is connected to net ’%s’ but undefined in list of components
"

DESCRIPTION

RTC-001 (error) Cannot detect current design name.

DESCRIPTION

You receive this message because no design has been loaded into the system.

WHAT NEXT

Load a design, and ensure that the **current_design** variable is defined.

SEE ALSO

current_design (3).

RTC-002 (error) File .rhosts does not exist in your home directory.

DESCRIPTION

Detail router requires file .rhosts to exist in user's home directory. This file must contain hostname of machines where router may run. Symbol '+' in the .rhosts file indicates that router may run on any machine.

WHAT NEXT

Create the .rhosts file with the hostname in it in your home directory, and start the router again.

SEE ALSO

route (2).

RTC-003 (error) Inconsistent database.

DESCRIPTION

You receive this message because an internal error has occurred in the design database.

WHAT NEXT

Attempt to reload the design database from the file.

RTC-004 (error) No physical library loaded.

DESCRIPTION

You receive this message because no library containing a physical description of the design has been loaded.

WHAT NEXT

Load the physical library.

RTC-005 (error) Cannot find library %s.

DESCRIPTION

You receive this message because the specified library cannot be found.

WHAT NEXT

Examine the library name and the **search_path** variable.

SEE ALSO

search_path (3).

RTC-006 (error) Cannot detect value of %s.

DESCRIPTION

You receive this message because the specified value is not defined.

WHAT NEXT

Define the value, and then start routing again.

RTC-007 (error) Preferred direction for routing layer '%s' is not defined.

DESCRIPTION

You receive this message because the preferred routing direction for the layer is not defined.

WHAT NEXT

Define the direction, and then start routing again.

RTC-008 (error) Class of site '%s' is not defined.

DESCRIPTION

You receive this message because the class (CORE or I/O) of the site is not defined.

WHAT NEXT

Define the site class, and then start routing again.

RTC-009 (error) Size of site '%s' is not defined.

DESCRIPTION

You receive this message because either the horizontal or vertical size of the site is not defined.

WHAT NEXT

Define the site size, and then start routing again.

RTC-010 (warning) Height and/or width of die area are undefined

DESCRIPTION

This message indicates that width and/or height of die area are not defined. Route66

requires these parametes.

WHAT NEXT

Define die width and die height and run route66 again.

RTC-011 (error) A shape object of unknown type detected.

DESCRIPTION

This message indicates an internal error in the design database.

RTC-012 (error) Routing segment of invalid direction is detected.

DESCRIPTION

You receive this message because an internal error has occurred in the design database.

RTC-013 (error) Invalid specification of ’%s’ detected.

DESCRIPTION

You receive this message because there is an internal error in the design database.

RTC-014 (error) Internal error.

DESCRIPTION

You receive this message because an internal error has occurred in the design database.

RTC-015 (error) Size of component '%s' is not defined.

DESCRIPTION

You receive this message because either the horizontal or vertical size of the component is not defined.

WHAT NEXT

Define the component size, and then start routing again.

RTC-016 (error) Offset of component '%s' is not defined.

DESCRIPTION

You receive this message because the offset of the component is not defined.

WHAT NEXT

Define the component offset, and then start routing again.

RTC-019 (error) Default routing width of layer '%s' is not defined.

DESCRIPTION

You receive this message because the default routing width of the layer is not defined.

WHAT NEXT

Define default routing width for the layer, and then start routing again.

RTC-020 (warning) Placement grid is not defined in horizontal direction.

DESCRIPTION

You receive this message because no site array is defined in the core area. If the design contains core components, the site array must be defined in the core area.

WHAT NEXT

Examine the design data.

RTC-021 (warning) Placement grid is not defined in vertical direction.

DESCRIPTION

You receive this message because no site array is defined in the core area. If the design contains core components, the site array must be defined in the core area.

WHAT NEXT

Examine the design data.

RTC-022 (error) Routing grid is not defined.

DESCRIPTION

You receive this message because the routing grid is not defined for the design.

WHAT NEXT

Define the routing grid, and then start routing again.

RTC-023 (error) Undefined reference: '%s' '%s'.

DESCRIPTION

You receive this message because a reference to a nonexistent object is detected.

WHAT NEXT

Check the data consistency.

RTC-024 (warning) Via ’%s’ has only one routing layer defined.

RTC-025 (warning) Via ’%s’ has more than two routing layers defined.

DESCRIPTION

WHAT NEXT

RTC-030 (error) Component ’%s’ is not defined in physical library.

DESCRIPTION

You receive this message because a component used in the netlist is not defined in the physical library.

WHAT NEXT

This message may appear in case of hierarchical presentation of the design. In this case, flatten the design using the **ungroup** command with the **-all** and **-flatten** options and the start router.

RTC-050 (error) Cannot open ’%s’ file.

RTC-051 (error) Cannot create ’%s’ directory.

RTC-053 (error) Cannot read from ’%s’ file.

RTC-055 (error) Cannot detect host name of current machine.

RTC-056 (error) The tool cannot open the %s or %s file.

DESCRIPTION

This error occurs because the tool failed to open the temporary files specified in the message. This is a program error in the tool.

WHAT NEXT

Contact the Synopsys Customer Support Center by doing one of the following:

- Send an e-mail message to support_center@synopsys.com.
- From the Web, go to http://solvnet.synopsys.com and click the "Enter a Call" link.

RTC-057 (error) The %s design is hierarchical.

DESCRIPTION

You receive this message because the specified design is hierarchical.

WHAT NEXT

Use the **ungroup** command with the **-all**, **-flatten**, and **-force** options to remove all levels of the hierarchy.

SEE ALSO

ungroup (2).

RTC-058 (error) The design database is incomplete. The program cannot open the %s file.

DESCRIPTION

You receive this message because the design database is incomplete. Some important, necessary files are missing.

WHAT NEXT

Please examine the database for completeness.

RTC-059 (error) The %s directory does not exist or has no read permission.

DESCRIPTION

You receive this message because the specified directory is missing entirely or is not accessible, possibly due to not having read permission.

WHAT NEXT

Determine that directory actually exists and examine the permissions on it to ensure that read permission is set.

RTC-060 (error) The %s directory is locked with process ID %d.

DESCRIPTION

You receive this message because the specified directory is locked.

WHAT NEXT

You can unlock the directory by using the process ID specified in the message to kill the process.

RTC-070 (error) Cannot find '%s' net.

RTC-071 (error) Error in routing '%s' control file is detected.

RTC-072 (error) Error in routing database file is detected.

DESCRIPTION

You receive this message because an internal error has occurred in the routing database.

RTC-101 (warning) A routing data inconsistency might exist.

DESCRIPTION

You receive this message because an inconsistency in routing data might exist.

RTC-102 (error) A routing data inconsistency exists.

DESCRIPTION

You receive this message because an inconsistency in routing data exists.

RTC-103 (error) A critical error has occurred, so the flow cannot continue.

DESCRIPTION

You receive this message because the flow cannot continue due to the occurrence of a critical error.

RTC-104 (error) The %d invalid index value has occurred in an

array with %d elements.

DESCRIPTION

You receive this message because an unexpected database situation has occurred for Route Compiler.

WHAT NEXT

File a Synopsys Technical Action Request (STAR), and provide the data necessary for Synopsys to reproduce and analyze the problem. Synopsys is in the process of creating a separate, clear message for each situation that might result in this error.

RTC-105 (error) Internal fatal error: unexpected database violation.

DESCRIPTION

You receive this message because an unexpected database situation has occurred in the Route Compiler software.

WHAT NEXT

File a Synopsys Technical Action Request (STAR), and provide the data necessary for Synopsys to reproduce and analyze the problem. Synopsys is in the process of creating a separate, clear message for each situation that might result in this error.

RTC-106 (error) Cell ’%s’ is undefined in list of cells, but defined in netlist as connected to net ’%s’.

DESCRIPTION

You receive this message because the specified component is connected to the specified net, but is undefined in the list of components. To be recognized by a net, a component must be defined in the list of components for that net.

RTC-107 (warning) Nondefault routing rule %s does not define

width for layer %s.

DESCRIPTION

Nondefault routing rule does not define wire width for specified layer. For the router it means that routing of nets assigned to this rule is prohibited on this layer. If there is a pre-routed segment of this rule on this layer, it will have the default width.

RTC-108 (warning) There is no minimal-area rule compliant via defined within the routing rule '%s' for layer '%s'.

DESCRIPTION

RTC-109 (warning) Logical pin '%s' of component '%s' does not have physical port.

DESCRIPTION

RTC-110 (warning) Via %s is not Route66-compatible (asymmetrical):
Layer %s: outline box: X: %d,%d; Y: %d,%d.

DESCRIPTION

RTC-111 (warning) Via %s is not Route66-compatible (non-concentric pads).

DESCRIPTION

RTC-112 (information) Connectivity to net '%s' from pin '%s' of

cell ’%s’ defined twice.

DESCRIPTION

RTC-113 (error) Extensions part of "design.lib

DESCRIPTION

RTC-114 (warning) P/G-route: undefined fragment type %s.

DESCRIPTION

RTC-115 (information) Pin ’%s’ of cell ’%s’ is defined connected to net ’%s’ in netlist: ignore wildcard connectivety to net ’%s’.

DESCRIPTION

RTC-116 (error) Pin ’%s’ is undefined in reference ’%s’, but defined in netlist for cell ’%s’.

DESCRIPTION

RTC-117 (information) Wildcard connection: net ’%s’, cells ’%s’, pin ’%s’.

DESCRIPTION

RTC-118 (error) Undefined via id=’%d’ encountered in db: via

ignored.

DESCRIPTION

RTC-119 (error) Component '%s' not placed (has reference '%s' of type %s).

DESCRIPTION

RTC-120 (warning) Reference '%s' has no pins.

DESCRIPTION

RTC-121 (warning) Spacing for UP & UP vias on layer '%s' has different definition (%d and %d): will use maximum value.

DESCRIPTION

RTC-122 (warning) Undefined routing grid. New grid will be created..

DESCRIPTION

RTC-123 (warning) Routing grid and/or port coordinates are out of die area; adjusting die size.

DESCRIPTION

RTC-124 (error) Number of %s routing tracks is %d: exceed

maximum value %d.

DESCRIPTION

RTC-125 (error) Global segment of net ’%s’ (routing rule ’%s’) is detected on layer ’%s’ that is not allowed by routing rule.

DESCRIPTION

RTC-126 (warning) Routing grid defines for invalid layer ’%s’.

DESCRIPTION

RTC-127 (warning) Undefined routing grid for routing layer ’%s’.

DESCRIPTION

RTC-128 (warning) Wire rule ’%s’ does not exist. Net ’%s’ which is assigned to this rule will have default rule applied.

DESCRIPTION

RTC-129 (warning) Regular (non-special) routing for net ’%s’ contains generated via ’%s’; putting the via into special routing.

DESCRIPTION

RTC-130 (error) The routing database in directory ’%s’ is out-of-

date with the version of the software being used.

DESCRIPTION

RTC-131 (error) You try to use old version of soft (%d) to work with routing data base created by soft version (%d). Please, upgrade soft version.

DESCRIPTION

RTC-132 (error) Undefined layer reference in same_net spacing definition '%s'.

DESCRIPTION

RTC-133 (error) Undefined layer '%s' refered in samenet spacing definition.

DESCRIPTION

RTC-134 (error) Samenet definition for different routing layers is

incorrect.

DESCRIPTION

RTC-135 (error) Undefined spacing for routing layer ’%s’.

DESCRIPTION

RTC-136 (warning) No %s found matching ’%s’ in set_fat_contact_options %s.

DESCRIPTION

RTC-137 (warning) No pin of reference ’%s’ found matching ’%s’ in set_fat_contact_options %s.

DESCRIPTION

RTC-138 (error) Via ’%s’ has no corresponding wire/via codes in routing data base: ignored.

DESCRIPTION

RTC-139 (error) Net %s: via %s has no corresponding type in

net group: ignored.

DESCRIPTION

RTC-140 (warning) Via %s: defines on %d routing layers.

DESCRIPTION

RTC-141 (warning) Via %s: defined on non nearest routing layers.

DESCRIPTION

RTC-142 (warning) Via %s: defines on %d cut layers.

DESCRIPTION

RTC-143 (warning) Wire code for TURN VIA '%s': duplicate

definition.

DESCRIPTION

RTC-144 (warning) Via %s has one routing layer and cut layers.

DESCRIPTION

RTC-145 (warning) Via %s: no objects on routing layers defined.

DESCRIPTION

RTC-146 (warning) Via %s: has no any objects.

DESCRIPTION

RTC-147 (warning) Site ’%s’ of reference ’%s’ has no definition in any library.

DESCRIPTION

RTC-148 (warning) Undefined taperrule for net %s.

DESCRIPTION

RTC-149 (error) Nondefault wire rule ’%s’ is not defined in

physycal library: ignoring routing object.

DESCRIPTION

RTC-150 (warning) Layer %s: undefined ID number in DB.

DESCRIPTION

RTC-151 (warning) Masterslice layer %s is defined after cut layer %s.

DESCRIPTION

RTC-152 (warning) Masterslice layer %s is defined after routing layer %s.

DESCRIPTION

RTC-153 (warning) No metal or masterslice layer was defined before cut layer %s.

DESCRIPTION

RTC-154 (warning) No cut layer was defined before routing layer %s.

DESCRIPTION

RTC-155 (warning) Routing group %s includes %d via codes

between layers %s and %s: will leave only 8.

DESCRIPTION

RTC-156 (warning) Routing group ’%s’: missing via-code between routing layers ’%s’ and ’%s’.

DESCRIPTION

RTC-157 (error) Invalid layers definition.

DESCRIPTION

RTC-158 (information) Additional number of joined pins - %d.

DESCRIPTION

RTC-159 (information) Additional number of joined nets - %d.

DESCRIPTION

RTC-160 (warning) Maximum number of pins for regular net is %d.

DESCRIPTION

RTC-161 (warning) Net ’%s’ has pairwise isolation with itself.

Isolation ignored.

DESCRIPTION

RTC-162 (warning) Incorrect %s net name '%s'.

DESCRIPTION

Power or ground net name is setting in tcl-veriable **physopt_route66_ground** or **physopt_route66_power**. Net with this name is present in database but has different type.

WHAT NEXT

Type of net will be changed from current to 'power' or 'ground'. Check correct definition tcl-veriables and power/ground nets in database.

RTC-310 (error) Cannot find reference rule %s.

DESCRIPTION

You receive this message because the routing rule specified in the -reference_rule_name option is not defined among either library-specific or design-specific routing rules.

WHAT NEXT

Correct the reference rule name or use the -default_reference_rule option

SEE ALSO

report_routing_rules (2).

RTC-311 (error) Layer %s is not defined in physical library.

DESCRIPTION

You receive this message because the layer specified for the routing rule is not defined in physical library.

WHAT NEXT

Correct layer name

SEE ALSO

report_lib (2) **report_routing_rules** (2).

RTC-312 (error) Cannot set %s for non-routing layer %s.

DESCRIPTION

You receive this message because either wire width or minimum routing spacing was specified for a non-routing layer.

WHAT NEXT

Correct the option

SEE ALSO

report_lib (2) **report_routing_rules** (2).

RTC-313 (error) Incorrect syntax: %s.

DESCRIPTION

You receive this message because of a syntax violation.

WHAT NEXT

Re-enter the command following syntax rules

SEE ALSO

define_routing_rule (2) **report_lib** (2) **report_routing_rules** (2).

RTC-314 (error) Routing rule %s already exists.

DESCRIPTION

You receive this message the rule being defined already exists.

WHAT NEXT

Change the rule name or remove existing rule.

SEE ALSO

remove_routing_rules (2) **report_lib** (2) **report_routing_rules** (2).

RTC-315 (warning) Physical library distance unit (1/%dum) is smaller than the design distance unit (1/%fum). The ’width’ and ’spacing’ attributes that are not specified explicitly may lose precision.

DESCRIPTION

You receive this message because the physical library distance unit is smaller than smaller than the design distance unit. As a result the distance attributes that are not explicitly specified may lose their precision.

WHAT NEXT

Specify all the spacings and widths for the new rule explicitly or use a design-specific reference rule.

SEE ALSO

remove_routing_rules (2) **report_lib** (2) **report_routing_rules** (2).

RTC-316 (error) Number of cuts cannot be set for non-contact

layer %s.

DESCRIPTION

You receive this message because number of cuts was specified for a non-contact layer.

WHAT NEXT

Correct the option

SEE ALSO

report_lib (2) **report_routing_rules** (2).

RTC-317 (error) Same-net spacing is not defined for contact layer %s; cannot generate via.

DESCRIPTION

You receive this message because neither reference wire rule nor physical library defines same-net spacing for the specified layer. This value is required to generate multi-cut vias.

WHAT NEXT

Add the required data to physical library.

SEE ALSO

report_lib (2) **report_routing_rules** (2).

RTC-318 (error) There is no default_via_generate_rule defined for contact layer %s; cannot generate via.

DESCRIPTION

You receive this message because physical library does not contain default_via_generate_rule for the specified layer. This rule is required to generate multi-cut vias.

WHAT NEXT

Add the required data to physical library.

SEE ALSO

report_lib (2) **report_routing_rules** (2).

RTC-319 (error) The value of %s is wrong; cannot generate vias.

DESCRIPTION

The space of cut_to_cut is incorrect, please check you physical library.

WHAT NEXT

Add the required data to physical library.

SEE ALSO

report_lib (2) **report_routing_rules** (2).

RTC-350 (warning) Cannot find nondefault rule %s.

DESCRIPTION

You receive this message because the nodefault routing rule specified in the -rule option is not defined among either library-specific or design-specific routing rules.

WHAT NEXT

Correct the rule name

SEE ALSO

report_routing_rules (2).

RTC-351 (warning) Cannot find layer %s in the reference rule.

DESCRIPTION

You receive this message because the layer specified in -widths option or the -spacings option can not be found in the reference rule specified in the -reference_rule option.

WHAT NEXT

The layer will be ignored in the new nondefault routing rule. If you don’t want to see this message, use layers that exist in the reference rule when specifying -widths or the -spacings option.

SEE ALSO

report_routing_rules (2).

RTC-411 (error) Layer %s is not a routing layer in physical library.

DESCRIPTION

You receive this message because the layer specified for the routing rule is not a routing layer in physical library.

WHAT NEXT

Correct layer name

SEE ALSO

report_lib (2) **report_shielding_options** (2).

RTC-412 (error) Incorrect syntax: %s.

DESCRIPTION

You receive this message because of a syntax violation.

WHAT NEXT

Re-enter the command following syntax rules

SEE ALSO

set_shielding_options (2) **report_lib** (2) **report_shielding_options** (2).

RTC-450 (error) Turn via ’%s’: missing or incorrect definition in db.

DESCRIPTION

Router can’t find the turn via’s definition in db.

WHAT NEXT

Please check your db, and add definition for the turn via.

SEE ALSO

RTC-470 (error) Missing layer ’%s’ definition.

DESCRIPTION

Can’t found layer’s definition from pdb, when RC generated via ’%s’.

WHAT NEXT

Please check your pdb, and add layer definition.

RTC-501 (warning) No genereated vias to fix ’%s’ rule.

DESCRIPTION

There are violations of the rule, but there are no generated vias to fix them. It may happens in case if via rules are not defined or defined incorrectly.

WHAT NEXT

Check correctnes of the via rule definition inside of corresponded fat contact rule '%s'.

SEE ALSO

set_fat_contact_options(2), RTC-503

RTC-502 (warning) Unknown detection method '%s' - cut_inside is used.

DESCRIPTION

The warning means that incorrect string was used to define fat contact detection method. There are three keywords: cut_inside, cut_cross, cut_around, which are allowed either in 'method' attribute of PLIB fat_contact_settings section or in -method option of **set_fat_contact_options** command.

WHAT NEXT

Make sure that 'method' of both PLIB and set_fat_contact_options contains correct value.

SEE ALSO

set_fat_contact_options(2)

RTC-503 (warning) %s in rule '%s'.

DESCRIPTION

The warning happens in case of wrong definition of fat via generation parameters inside of PLIB fat_contact_rule section. If you see the warning it means fat vias will not be generated for that '%s' rule. There are the following first strings:

"Incorrect bottom layer" - bottom layer of the via is the top metal of the design.

"Min threshold is more than max threshold" - minimim threshold can't be more or equal to maximum one.

"Size of cuts is less or equal to 0" - size of cut should be more than 0.

"Up enclosure is less than 0", "Down enclosure is less than 0",

"Up end-of-line is less than 0", "Down end-of-line is less than 0" - enclosure and end-of-line parameters should be 0 or more.

"Number of cuts is less than 1 or more than 4" - number of cuts should be more or equal to 1 and less or equal to 4

WHAT NEXT

Make sure that via generation parameters are correct.

SEE ALSO

set_fat_contact_options(2), RTC-501

RTDC-3 (warning) The sequential cell '%s' drives the clock in this design. The cell will not be moved by retiming.

DESCRIPTION

If a sequential cell drives the clock pin(s) of one or more other sequential cells, this sequential cell cannot be moved by retiming.

WHAT NEXT

No action is necessary. If the cell in question should not be driving clock pins check the original netlist.

RTDC-4 (error) The cell '%s' drives the clock in this design. Only buffer and inverter cells are allowed on the clock network.

DESCRIPTION

The use of non-buffer and non-inverter cells in the clock network may introduce different clock domains into the design.

WHAT NEXT

Exclude the clock generation logic from the design to be retimed.

RTDC-5 (warning) No clock net driving clock pin of cell '%s'.

DESCRIPTION

The clock pin of the cell is either not connected to a net or there is no clock source if the net connected to the clock pin is traced back across unate and inverting cells. Retiming cannot retime such cells. They will be treated like dont-touched registers.

WHAT NEXT

You should check whether it is your intention to have such a cell in your design or whether there are any non-unate gating cells in the clock network driving this cell. You might need to change the design if you want to move these registers or get the best possible results from retiming.

RTDC-6 (error) Retiming cannot be performed with this clocking scheme.

DESCRIPTION

This error should only occur in combination with one or more other errors that have been reported earlier. These can be a flip-flop drives a clock net (RTDC-3), both normal and fake master slave sequential cells exist (RTDC-106), or a clock pin of a flip-flop is not connected to any net at all (RTDC-5).

WHAT NEXT

Look through the dc_shell log and find one of the previous error messages and fix the cause for this problem.

RTDC-7 (error) The following cell(s) contain sequential elements
and have the dont_touch attribute set. Cannot retime.

DESCRIPTION

The modelling capabilities of the retiming package do not allow this.

WHAT NEXT

Remove the dont_touch attribute from the cell.

RTDC-8 (error) Sequential cell '%s' is neither a flip-flop nor

a latch. Cannot retime.

DESCRIPTION

The cell is a sequential cell, which is not an edge triggered flip-flop Nor is it a latch. The retiming commands do not work on designs that contain such cells.

WHAT NEXT

Exclude the cell from the design. This can be done by putting it into its own hierarchical module. Then retime only the other hierarchical modules.

RTDC-9 (error) More than one clock signal has been detected. Multiple clock signals not allowed for retiming. The different clocks have sources in '%s' and '%s'.

DESCRIPTION

Retiming only works on designs where all registers and latches are driven by the same clock. Gated clocks that are derived from the same based clock are allowed.

WHAT NEXT

Try to retime only for one clock signal at a time. This could be achieved by the following steps: Group all the registers in the design that are driven by one clock or by gated clocks derived from the same base clock into a hierarchical cell of their own. Then set the current design to the design for this new hierarchical cell. Constrain the new design. Retime the new design. Proceed in the same way for all other clocks in the original design.

RTDC-10 (warning) No movable flip-flops in design. Nothing to retime.

DESCRIPTION

There must at least be one movable flip-flop in the design. Otherwise retiming cannot perform any optimization. Flip-flops can become not movable for the following reasons, which are indicated by other warning messages: A dont_touch attribute has been set on them. They are the endpoint of a point to point exception such as false or multicycle path. There is not enough information available about its functionality. Some retiming commands also do not move flip-flops with asynchronous reset. 'balance_registers' does this in general, while 'optimize_registers' allows

to control this with command line options.

WHAT NEXT

Find out what makes the flip-flops in your design not movable by looking at other warning messages. You can also use the check_design and verbose options of optimize_registers. Then take the appropriate measures to make some or all of the cells movable.

RTDC-12 (warning) No designs have the balance_registers, optimize_registers or pipeline_design attribute set. Nothing to retime.

DESCRIPTION

The **optimize_registers**, **balance_register**, **pipeline_design**, **set_optimize_registers** and **set_balance_registers** commands put attributes on designs or subdesigns to be retimed. The inner retiming algorithm looked for these attributes and did not find any.

WHAT NEXT

Use one of the commands on an existing design.

RTDC-13 (error) Retiming interrupted.

DESCRIPTION

The Control-c key or another key for interruption was hit during retiming and the retiming was stopped.

WHAT NEXT

Start the retiming command again and do not interrupt it.

RTDC-14 (warning) Retiming failed. No registers have been

moved.

DESCRIPTION

The retiming failed. A previous error message should give you a detailed reason for the failure.

WHAT NEXT

Find the previous error message by looking for the string RTDC in your dc_shell log file. Fix the problem as described in the documentation for that error message.

RTDC-15 (warning) Design contains registers that will be retimed.
Cannot verify.

DESCRIPTION

The current design contains a part that has the balance_registers, optimize_registers or pipeline_design attribute set. The system moves registers of this part to minimize/optimize the maximum register-to-register delay. Because of the movement, the pre- and post-compiled designs cannot be verified.

WHAT NEXT

If you want to retime a design, you cannot verify it, so remove the -verify option from the compile command. However, if you do not want to retime the design, remove the balance_registers, optimize_registers or pipeline_design attribute from the design, using the remove_attribute command.

RTDC-16 (error) The design contains generic combinational logic. Cannot retime.

DESCRIPTION

The current design contains generic logic. Since this logic does not have any delay associated with it, it cannot be retimed.

WHAT NEXT

Compile the design so that it is completely mapped and then issue the retiming command again.

RTDC-17 (error) Design contains unmapped DesignWare parts. Cannot retime.

DESCRIPTION

The current design contains an unmapped DesignWare part. Since there are no gates associated with this part, the register cannot be moved with respect to the parts delay.

WHAT NEXT

If you want to retime this design, but do not want the registers pushed into the DesignWare part, perform a dont_touch on that part. If you do want the registers to be pushed into the DesignWare part, then it must be mapped by performing a compile.

RTDC-19 (warning) Clock period after accounting for worst case set-up and median clock to Q/QN delay is non-positive. Original clock period is %.2f, estimated clock period is %.2f. Using a zero target clock period.

DESCRIPTION

By default, the clock period that retiming tries to achieve is computed in the following way: The desired clock period, which you specified either through the create_clock command or the -period option is corrected by subtracting the setup time of the preferred flip-flop or latch and the median clock-to-Q delay of the design. In this case, the resulting number is negative. Retiming will try to achieve a clock period that is as small as possible. Note that for latch retiming we operate with a clock period that is half the nominal clock period.

WHAT NEXT

If you wanted the smallest possible clock period, you need not change anything. Otherwise you should check whether the clock period that is specified by the **create_clock** command for your design or by the -period option of your retiming command is a realistic value and correct it if necessary. Then start retiming again.

RTDC-20 (error) Negative clock cycle specified with -period option.

DESCRIPTION

The value for the desired clock period that was provided with the -period option is negative. Even with retiming a negative clock period cannot be achieved for any design.

WHAT NEXT

Check the command line for your retiming command and correct the value provided for the -period option. The smallest possible value is 0.

RTDC-21 (warning) No clock connected to flip-flops. Using clock period of zero.

DESCRIPTION

The retiming command could not find a clock port while tracing back from the clock pins of the sequential cells in the design. Some sequential cells in the design have a clock pin that is not connected to any clock port. A clock period of zero will be used for retiming these sequential cells.

WHAT NEXT

If you want to retime with a clock period other than zero, modify the design so that all flip-flop clock pins are connected to the clock port and create a clock at the clock port.

RTDC-22 (warning) No clock period specified with clock %s.

DESCRIPTION

The retiming command could find a clock port of the design while tracing back from the clock pins of the flip-flops, but this clock port had no period assigned to it. There was also no desired clock period given by using the -period option of the retiming command.

WHAT NEXT

Please specify the clock period using the **create_clock** command with the period option or the -period option of **optimize_registers** or **pipeline_design**.

RTDC-23 (warning) No clock found on '%s'. Trying flip-flops in the design.

DESCRIPTION

The retiming command can trace back from the clock pins of the flip-flops to a clock port, but this clock port does not have clock attribute set on it.

WHAT NEXT

Set a clock attribute on your clock port by using the **create_clock** command.

RTDC-24 (error) Retiming is not supported for Xilinx 4000 designs.

DESCRIPTION

The design has been created with the Xilinx 4000 technology. Retiming cannot be performed for this technology.

WHAT NEXT

Use a different technology.

RTDC-25 (error) The target library does not contain an inverter.

DESCRIPTION

An inverter is required for retiming to handle registers with inverted outputs and to connect registers after retiming.

WHAT NEXT

Please add an inverter to the library (e.g. be removing dont_use commands).

RTDC-26 (warning) The flip-flop '%s' selected by 'set_register_type' is unacceptable for retiming because no setup time is available for this flip-flop. Attempting to search the target library for a D flip-flop with reasonable setup.

DESCRIPTION

This warning message occurs when a preferred flip-flop is selected using the **set_register_type** command. The selected flip-flop does not have a setup time specified in the library. The **set_register_type** specification is ignored and a preferred flip-flop is chosen from the library.

WHAT NEXT

This is a warning message only. No action is required on your part. However, it is good practice to choose a different flip-flop from the target library.

SEE ALSO

balance_registers (2), **optimize_registers** (2), **set_register_type** (2).

RTDC-27 (error) No good flip-flop found in library. Cannot model the design.

DESCRIPTION

Retiming selects a preferred flip-flop from the flip-flops in the technology library to perform clock correction using its setup time and the median clock-to-Q delay computed with this flip-flop. The selection is performed by using different criteria. In this case no suitable preferred flip-flop could be found. One potential reason for this might be that you forbid the use of flip-flops in the library with the **dont_use** command.

WHAT NEXT

Use the -check_design option of the retiming command to determine which flip-flops are candidates and why they are not selected. Check the **dont_use** commands in your script and correct them if too many flip-flops are excluded. Then retime again.

RTDC-29 (error) A combinational loop was found in design. Retiming cannot operate on such designs.

DESCRIPTION

A loop consisting only of combinational cells has been found in the design. There is no register in this loop. Retiming of a design with such a loop is not possible.

WHAT NEXT

Change your design to not contain such a loop or exclude the loop from the part of the design that has to be retimed.

RTDC-30 (error) The design has master-slave sequential elements as well as flip-flops. All sequential elements must be of the same kind.

DESCRIPTION

The design contains both single clock flip-flops and master-slave flip-flops. Retiming does not support a design that has both flip-flop types.

WHAT NEXT

Partition the design so that one subdesign has only single clock flip-flops and the other subdesign has only master-slave flip-flops. Then retime the two designs separately.

SEE ALSO

balance_registers (2), **optimize_registers** (2).

RTDC-31 (warning) The master clock has period %.2f, the slave

has period %.2f. Choosing master clock period as target for area
optimization.

DESCRIPTION

The design has a master-slave clock system. The retiming analysis of the clock networks and clock ports found that the master and slave clock have different clock period values defined. Retiming will use the value specified for the master clock as the target value for optimization.

WHAT NEXT

If the value for the master clock is indeed your target clock period, there is no need to change anything. Otherwise be sure to set the correct clock period for the master clock port using the **create_clock** command.

RTDC-32 (warning) Cell '%s' has no timing information. Treating it
like an external module.

DESCRIPTION

This warning indicates that the retiming command found a cell that contains no timing information. Because the retiming algorithm relies on having timing information for every cell, the cell is being modeled as if it is external to the **current_design**; that is, no registers may move across it.

WHAT NEXT

No further action is indicated.

RTDC-33 (warning) Must have BOA-BRT license to handle cells without timing information.

DESCRIPTION

This warning indicates that **balance_registers** found a module that contains no timing information. Because the retiming algorithm relies on having the timing information for every cell, it cannot handle the **current_design**.

WHAT NEXT

Use the **externalize_cell** command to externalize the cells that do not have timing information. Then re-execute **balance_registers**.

RTDC-34 (warning) The following registers are considered to be 'fixed' during retiming. They are end-points of timing exceptions such as 'set_false_path'.

DESCRIPTION

Some registers in the **current_design** are start- or endpoints for timing exceptions defined by one of the following commands: **set_multicycle_path**, **set_max_delay**, **set_min_delay**, **set_false_path**. To avoid a violation of the timing requirements, these registers will not be moved and no other registers will be moved across them.

WHAT NEXT

Use **report_timing_requirements** to get a list of start- and end-points of the timing exceptions mentioned above.

SEE ALSO

current_design (2); **set_multicycle_path** (2); **set_max_delay** (2); **set_min_delay** (2); **set_false_path** (2); **report_timing_requirements** (2).

RTDC-35 (error) Designs with flip-flops driving a reset pin cannot be retimed.

DESCRIPTION

The current functionality for retiming of flip-flops with asynchronous resets does not allow resets that are not controlled by primary inputs of the design. A flip-flop has been detected where a reset pin is driven by the output of another flip-flop.

WHAT NEXT

Exclude the flip-flop that has a reset pin that is not driven by a primary input from retiming. You can do this by either putting the dont_touch attribute on the flip-flop or by excluding it from the part of the design that is to be retimed.

RTDC-36 (error) Designs using gated resets cannot be retimed.

DESCRIPTION

The current functionality for retiming of flip-flops with asynchronous resets does not allow resets that are not controlled by primary inputs of the design. A flip-flop has been detected where a reset pin is not connected (either directly or through buffers and inverters) by a reset port of the design.

WHAT NEXT

Exclude the flip-flop that has a reset pin that is not driven by a primary input from retiming. You can do this by either putting the dont_touch attribute on the flip-flop or by excluding it from the part of the design that is to be retimed.

RTDC-37 (error) Cannot retime a design with several driving pins for the asynchronous set or clear. One pin found is '%s', another one is '%s'.

DESCRIPTION

The not dont_touched asynchronous set or clear registers in the design are either connnected to one net with more than one driving pin or to multiple reset nets driven by different pins.

WHAT NEXT

Replace the multiple driver net in the reset logic by a net consisting of simple adder and inverter cells driven by an external port or (in case of multiple reset nets) put a dont_touch attribute on all cells on one reset net while retiming those on the other one.

RTDC-38 (error) Cannot retime flip-flops with asynchronous set and clear at the same time.

DESCRIPTION

The design contains flip-flops that have the asynchronous clear pin connected as well as flip-flops that have the asynchronous set pin connected.

WHAT NEXT

Retime one group of flip-flops at a time by dont_touching the
other group.

RTDC-40 (error) Flip-flop with two asynchronous pins connected. Cannot retime.

DESCRIPTION

A flip-flop has been detected that has two of its asynchronous pins connected. The current version of retiming cannot move this flip-flop.

WHAT NEXT

Exclude the flip-flop that has two reset pins connected from being retimed. You can do this by either putting the dont_touch attribute on the flip-flop or by excluding it from the part of the design that is to be retimed.

RTDC-41 (error) The following cell(s) have at least one pin, which is bidirectional (inout) or for which the direction cannot be inferred (for example because the the cell itself is an unresolved
reference). Cannot retime.

DESCRIPTION

Bidirectional pins or pins for which the direction cannot be inferred are introduced by certain types of black boxes or unresolved references in the design. The retiming methodology does not allow to optimize designs with such pins.

WHAT NEXT

Replace the (black box) cell with a cell having only directed (in or out) pins or provide a reference to the cell giving the pin directions.

RTDC-42 (warning) Port '%s' has negative %s %s delay set. Retiming will operate as if the delay is zero.

DESCRIPTION

This warning indicates that the retiming command found an input or output of the design that has a negative delay set by **set_input_delay** or **set_output_delay** commands. The retiming algorithm does not support this and will work with an input delay of zero (0.0) for this port.

WHAT NEXT

Check your design constraints and try to set a correct non-negative I/O delay for all ports. Use these delays already for logic synthesis.

RTDC-43 (warning) The input port '%s' has input %s delay that is smaller than the clock-to-Q delay used by the retiming algorithm.For optimal results, make sure to set an input delay that is realistic. This can be done by using the 'set_input_delay' or 'characterize' commands.

DESCRIPTION

This warning indicates that the retiming command found an input port of the design that has a delay set by **set_input_delay** that is less than the clock-to-Q delay used by retiming. **optimize_registers** uses the median clock-to-Q delay. **balance_registers** uses the maximum clock-to-Q delay found in the design. The retiming algorithm might provide non-optimal timing and area results.

WHAT NEXT

Check your design constraints and try to find a correct and sufficiently high input delay characterization for all ports. At least a typical clock to Q delay must be used at all input ports in any realistic environment for your design. Use those delays already used for logic synthesis.

RTDC-44 (warning) The output port '%s' has output %s delay that is smaller than the estimated average setup time used by the retiming algorihm. For optimal results make sure to set an

output
delay that is realistic. This can be done by using the 'set_output_delay' or 'characterize' commands.

DESCRIPTION

This warning indicates that the retiming command found an output port of the design that has a delay set by **set_output_delay** which is less than the setup time used by retiming. The retiming algorithm may provide results (timing and area), which are worse than you expect.

WHAT NEXT

Check your design constraints and try to find a correct and sufficiently high output delay characterization for all ports. At least a typical flip-flop setup time must be used at each output port in any realistic environment for your design. Use these delays already for logic synthesis.

RTDC-45 (error) The clock tree is configured such that cell '%s' and cell '%s' are sensitive to opposite edges of the clock applied to the clock port of the design. Cannot retime.

DESCRIPTION

The number of inverters on the path from the external clock port to the clock pin of one of the two sequential cells is even, while the number on the path to the other cell is odd. Thus the cells are driven by opposite edges of the external clock. This is not allowed for retiming.

WHAT NEXT

Check whether your clock tree is build correctly and whether you really need these differently triggered flip-flops in your design.

RTDC-46 (error) The clock tree feeds cell '%s' which is non sequential and does not feed any sequential cells. Cannot

remove the clock tree.

DESCRIPTION

The cell in question was not encountered when backtracing the clock tree from the sequential elements, but is connected to the clock tree. Therefore removing the clock tree may change the functionality of the circuit.

WHAT NEXT

Check whether your clock tree is build correctly and whether you really need this cell connected to the clock tree.

RTDC-47 (warning) There are buffer or inverter cells in the clock tree. The clock tree has to be recreated after retiming.

DESCRIPTION

Since retiming moves flip-flops in the design and changes their
numbers. The clock tree needs to be rebuild after retiming.

WHAT NEXT

Continue with retiming and recreate the clock tree.

RTDC-48 (error) A master-slave flip-flop has been chosen as the preferred flip-flop for a normal flip-flop type design. Cannot retime.

DESCRIPTION

For normal (single-phase) clock designs a corresponding flip-flop must be chosen from the library.

WHAT NEXT

If you want to have a normal (single-phase) clock design either chose a corresponding flip-flop from your library using 'set_register_type' or use a target library containing single-phase clock flip-flops. If you want to have a master-slave

design compile the existing design for master-slave first use a slave clock port and then the 'set_signal_type' command.

RTDC-49 (error) A single-phase clock flip-flop has been chosen as the preferred flip-flop for a master-slave type design. Cannot retime.

DESCRIPTION

For master-slave type designs a corresponding flip-flop must be chosen from the library.

WHAT NEXT

If you want to have a master-slave clock design either chose a corresponding flip-flop from your library using 'set_register_type' or use a target library containing master-slave flip-flops. If you want to have a single-phase design compile the existing design for master-slave first removing the slave clock port and the 'set_signal_type' command.

RTDC-50 (error) Cell '%s' has too many pins. Cannot retime.

DESCRIPTION

The number of pins per cell is limited for memory efficiency during retiming.

WHAT NEXT

If the cell is a hierarchical cell that you have dont_touched try removing the dont_touch attribute from this cell, so that the lower level cells (with less pins) form the basic elements for retiming. If the cell is a leaf cell (an instance of a technology library cell) with a large number of pins try to resynthesize the design after putting a dont_use attribute on the library cell. Another solution would be to regroup the design and externalize the inflicting cell.

RTDC-51 (Warning) The clock tree feeds cell '%s' which is non

sequential and does not feed any sequential cells.

DESCRIPTION

The cell in question was not encountered when backtracing the clock network from the sequential elements, but is connected to the clock network. Maybe you intended to have a gated clock?

WHAT NEXT

Check whether your clock tree is build correctly and whether you really need this cell connected to the clock tree.

RTDC-52 (error) The following cell(s) are tristate cells. Cannot retime.

DESCRIPTION

For retiming the design may no contain tristate cells, because moving registers across tristate cells may cause bus systems not to work properly.

WHAT NEXT

Extract the part of your design containing the tristate cells and the bus and retime only the remaining design.

RTDC-53 (error) The design '%s' is not purely combinational. It cannot be pipelined.

DESCRIPTION

The **pipeline_design** command only handles purely combinational designs.

WHAT NEXT

Extract a combinational part for retiming from your design.

RTDC-54 (error) The target library does not contain any edge triggered

flip-flops.

DESCRIPTION

The **pipeline_design** command needs edge triggered flip-flops for retiming.

WHAT NEXT

Select a different library.

RTDC-55 (error) The target library does not contain a simple D flip-flop without additional logic.

DESCRIPTION

The **pipeline_design** command needs this simple flip-flop to construct the initial circuit prior to retiming.

WHAT NEXT

Select a different library.

RTDC-56 (error) Could not find the port '%s' in the design.

DESCRIPTION

The control and clock ports must already exist in the design, before **pipeline_design** is applied.

WHAT NEXT

Add a port with this name.

RTDC-57 (warning) The value provided by the '-period' option for optimize_registers will now be corrected by the setup time and

clock-to-Q delay of the preferred flip-flop.

DESCRIPTION

The default behavior was changed to prevent a common mistake that led to worse results than expected.

WHAT NEXT

To obtain the old default behavior, use the '-no_clock_correction' option.

RTDC-58 (error) A loop without registers on the net was detected in the design taking into account hierarchical cells with the dont_touch attribute set to true. I.e. these cells are viewed as a single cell. Retiming cannot operate on such designs, although the netlist on the leaf cell level does not contain combinational feedback loops.

DESCRIPTION

The loop was created by putting a dont_touch attribute on a hierarchical cell.

WHAT NEXT

Remove the dont_touch attribute from the cell(s) in the loop causing the problem. It may be possible to put the dont_touch attribute on lower level cells in the hierarchy instead.

RTDC-59 (warning) The 'optimize_registers' attribute or the 'pipeline_design' attribute has been set on a design but no license for this feature is authorized. The retiming will be performed using the 'balance_registers' functionality.

DESCRIPTION

The 'optimize_registers' and 'pipeline_design' attributes require a special license during compile. In this case there is no key for this key in the license file. Instead the 'balance_registers' functionality is used, which performs no register count optimization.

WHAT NEXT

You can purchase a license key to allow retiming with optimize_registers and pipeline_design functionality from Synopsys.

RTDC-60 (warning) The design contains the following cells which have no influence on the design's function but cannot be removed (e.g. because a dont_touch attribute has been set set on them). Retiming will ignore these cells in order to achieve good results:

DESCRIPTION

Even if a cell is unconnected at all output ports or feeds only cells that are unconnected at all output ports it cannot be removed if there is an attribute forbidding this. Retiming will disconnect these cells from the rest of the circuit and will not further regard them.

WHAT NEXT

Since these cells are of no importance. They should be removed. It will happen automatically if any dont_touch attributes on them or on the nets they are connected to are removed.

RTDC-61 (warning) The design contains the following cells from the GTECH library. The results of retiming may not be

valid:

DESCRIPTION

The GTECH library contains generic cells without timing. Retiming results obtained using these cells, may become useless once the GTECH cells are mapped.

WHAT NEXT

Map the entire design using the compile command before retiming.

RTDC-62 (warning) The design contains the following multibit registers, which can be moved by retiming. For retiming they will be decomposed into single bit registers. To avoid this put a ’dont_touch’ attribute on these cells.

DESCRIPTION

To be able to retime movable registers have to be single bit.

WHAT NEXT

Put the dont_touch attribute on these cells or (if you want them to be retimed) try to group the single bit registers after retiming to compile to multibit registers.

RTDC-63 (warning) The flip-flop ’%s’ selected by ’set_register_type’ is unacceptable for retiming because it cannot be used to represent all necessary flip-flop functions. Attempting to search the target library for a suitable D flip-flop.

DESCRIPTION

It must be possible to represent any generic flip-flop of the correct reset type (synchronous / asynchronous) with the preferred flip-flop. If the library description of a flip-flop does not allow this.

WHAT NEXT

Accept the flip-flop selected automatically or select a different one using 'set_register_type'.

RTDC-64 (warning) The flip-flop '%s' selected by 'set_register_type' is unacceptable for retiming because it is not a scan flip-flop. Since this is a scan replaced design, the flip flop will only be used for retiming calculations. Another flip-flop may be used for replacement.

DESCRIPTION

A 'test_ready' design must contain scan flip-flops. Therefore scan flip-flops have to be inserted after retiming.

WHAT NEXT

Accept the flip-flop selected automatically or select a different one using 'set_register_type'.

RTDC-65 (error) The current (sub)-design is scan routed. Retiming would invalidate the scan routing.

DESCRIPTION

Scan routing depends on the a register distribution. Retiming will change this distribution.

WHAT NEXT

Create scan routing and scan logic after retiming.

RTDC-66 (error) The current (sub)-design has scan logic. Retiming would invalidate the scan

logic.

DESCRIPTION

Scan logic depends on the a register distribution.
Retiming will change this distribution.

WHAT NEXT

Create scan routing and scan logic after retiming.

RTDC-67 (warning) A timing arc with a negative delay was found. Will use a delay of zero during retiming.

DESCRIPTION

Retiming does only work on netlists with non-negative
delay cells.

WHAT NEXT

No action is necessary. However, you should check the correctness of your cell library the accuracy of retiming and synthesis may be compromised.

RTDC-68 (warning) There is not enough information available about the
functionality of the library cell of flip-flop cell
%s.
It cannot be retimed. It will be treated as a fixed flip-flop.

DESCRIPTION

In order to retime a sequential cell certain information on its functionality such as reset, clear, or load enable pins must be available. If this information is not, or not completely available in the technology library, no retiming that ensures the correct functionality of the circuit can be performed. The particular cell will remain in place. The quality of results might or might not deteriorate.

WHAT NEXT

Let the retiming run complete and check whether the results are acceptable. If they are not acceptable, try to compile the circuit again starting from the HDL source code while forbidding the use of the library cell. You can accomplish this with the **dont_use** command. Then retime again.

RTDC-69 (warning) The flip-flop cell %s has either the force_00 or the force_11 input connected, or it has both the force_01 and the force_10 connected to a non-constant net. This type of cell cannot be supported by retiming. Therefore it will not be moved.

DESCRIPTION

It is required that the Q and QN output of a flip-flop cell always have complementary values. This cell does not fulfill this requirement.

WHAT NEXT

Let the retiming run complete and check whether the results are acceptable. If they are not acceptable, try to synthesize the circuit again not using cells with this reset capability.

RTDC-70 (warning) The flip-flop cell %s is a multibit cell. For retiming the cell’s synchronous set, clear or load enable capabilities will not be utilized.

DESCRIPTION

If the decompose option has not been utilized and the decompose attribute has not been set on the sequential cell, **optimize_registers** will try to make use of synchronous set, clear, or load_enable inputs for better results, or for single bit flip-flops if these exist. For multibit cells this does not happen.

WHAT NEXT

If the multibit registers doesn't have synchronous set, synchronous clear, or synchronous load enable, there is no deterioration in the quality of result. However, if it does and you suspect retiming results could be better, try recompiling your original design without the use of multibit registers and retime again.

RTDC-71 (warning) The flip-flop cell %s is connected at both the asynchronous preset pin and the asynchronous clear pin. The library cell for this cell has identical reset values for the Q and the QN output in case both the preset and the clear are active simultaneously. If this situation can occur in the circuit the retimed circuit may have a behavior differing from that of the original circuit.

DESCRIPTION

The retiming commands rely on the fact that the Q and QN outputs of flip-flops have always opposing values to disconnect one of them and drive its net by the inverted output of the other. Some library cells such as the one in this case allow to connect two asynchronous initialization signals to the cell. To allow proper initialization the library cell's specification must include the values for the Q and the QN pin in case both preset and clear are active at the same time. In this case the basic assumption for the retiming command's transformation is violated.

WHAT NEXT

If you are sure that preset and clear for the cell are never active at the same time, there is no need for any action. Otherwise there are two possibilities to deal with this situation. The first one is to put a dont_touch attribute on the cell. In this case it will not be retimed and there is no problem. If this first solution decreases the quality of results of retiming, you can apply the second solution: Synthesize your circuit again and forbid the use of the particular library cell by using the 'dont_use' command. Then retime again.

RTDC-72 (error) The target technology library does neither contain a two input AND nor a two input NAND gate. On of these is

necessary to
connect flip-flops with two reset inputs correctly after retiming.

DESCRIPTION

Under certain circumstances it is necessary to construct a new reset signal from two other reset signals after retiming in order to create correct reset behavior for flip-flops with two resets of the same type (synchronous/asynchronous) connected. In this case either a two input AND gate or a two input NAND gate and an inverter were searched but not found.

WHAT NEXT

Check whether the use of these cells has been forbidden by the dont_use command. If yes, remove the dont_use commands and rerun your script. If the library indeed does not contain such cells, try to modify your design such that it does not use flip-flops that have two resets of the same type connected simultaneously.

RTDC-73 (error) The target technology library does neither contain
a two input OR nor a two input NOR gate. On of these is necessary to
connect flip-flops with two reset inputs correctly after retiming.

DESCRIPTION

Under certain circumstances it is necessary to construct a new reset signal from two other reset signals after retiming in order to create correct reset behavior for flip-flops with two resets of the same type (synchronous/asynchronous) connected. In this case either a two input OR gate or a two input NOR gate and an inverter were searched but not found.

WHAT NEXT

Check whether the use of these cells has been forbidden by the dont_use command. If yes, remove the dont_use commands and rerun your script. If the library indeed does not contain such cells, try to modify your design such that it does not use flip-flops that have two resets of the same type connected simultaneously.

RTDC-74 (error) The retiming graph that has been constructed

for the design to be retimed does not contain any nodes.

DESCRIPTION

Retiming optimizations are executed on graphs. In this case the graph does not contain any nodes. The reason for this could be that all cells in the current design are considered unused. This in turn could be caused be the fact that none of the output pins is really a function of the inputs or the internal registers.

WHAT NEXT

Check the netlist of the design to be retimed. Especially check whether at least one output port is really driven by an internal gate or an input port.

RTDC-77 (error) The cell %s has has an illegal value of the transform_for_retiming attribute.

DESCRIPTION

Only the values multiclass (0), dont_retime (1) or decompose (2) are legal for the transform_for_retiming attribute.

WHAT NEXT

Decide which value you want for this cell. Then set it using the set_transform_for_retiming command.

RTDC-78 (error) The cell %s has has an illegal value of the state_for_retiming attribute.

DESCRIPTION

Only the values preserve (0) or dont_care (1) are legal for the state_for_retiming attribute.

WHAT NEXT

Decide which attribute value you want for this cell. Then set it using the set_state_for_retiming command.

RTDC-79 (warning) The cell %s has the dont_touch or dont_retime and the dont_care attribute set. Using preserve instead.

DESCRIPTION

If a sequential cell has the dont_touch or the dont_retime attribute set the state represented by it is automatically preserved. The dont_care attribute does not make any sense for retiming.

WHAT NEXT

No action is necessary. The correction has been performed automatically. If you want to avoid this message in the future, remove the dont_care_for_retiming attribute from the cell.

RTDC-80 (warning) The cell %s has the decompose and the dont_care attribute set. Using decompose and preserve instead.

DESCRIPTION

If a sequential cell has the decompose attribute set the state represented by it is automatically preserved. The dont_care attribute does not make any sense for retiming.

WHAT NEXT

No action is necessary. The correction has been performed automatically. If you want to avoid this message in the future, remove the dont_care_for_retiming attribute from the cell.

RTDC-81 (error) The clock system is too complicated for retiming.

DESCRIPTION

The retiming algorithms cannot only handle a subset of designs with multiple clocks involving multiple periods, phases and clock gating. The current design is too

complicated.

WHAT NEXT

Read the retiming user manual for a description of the allowed clocking schemes. Try to partition your design into smaller parts that have only a single clock for all registers.

RTDC-82 (warning) The backward justification during retiming failed.

DESCRIPTION

In order to be able to move registers including their reset connections retiming needs to compute the equivalent initial state of the circuit after retiming. In this case the computation of the equivalent state for registers moved backward has failed. This is most likely caused by runtime or capacity limits.

WHAT NEXT

If the design has synchronous reset and you decompose all or part of the registers using the -sync_trans option of the retiming command or the set_transform_for_retiming command the computation of the initial states for the registers is no longer necessary. If there are registers in the design that need to have an initial state upon reset but the particular value is of no relevance applying the -sync_state, -async_state options and the set_state_for_retiming commands will help. Further on it may help to remove the dont_touch attribute from complex cells such as multipliers or adders in the design, if these exist.

If these suggestions are not applicable, then the following might help:

Try to recode the RTL description for the design such that the registers are initially located at the primary inputs instead of the primary outputs. That would assure that registers are only moved forward and the initial state computation for forward moves is much easier than that for backward moves.

RTDC-83 (error) The forward justification during retiming failed.

DESCRIPTION

In order to be able to move registers including their reset connections retiming needs to compute the equivalent initial state of the circuit after retiming. In this case the computation of the equivalent state for registers moved forward has failed. This is most likely caused by runtime or capacity limits.

WHAT NEXT

It may help to remove any dont_touch attribute from complex cells such as multipliers or adders in the design, if these exist. If the design has synchronous reset and you decompose all or part of the registers using the -sync_trans option of the retiming command or the set_transform_for_retiming command the computation of the initial states for the registers is no longer necessary. If there are registers in the design that need to have an initial state upon reset but the particular value is of no relevance applying the -sync_state, -async_state options and the set_state_for_retiming commands will help.

RTDC-84 (warning) The cell %s has at least one asynchronous pin connected and the decompose transform attribute is set for it. The any synchronous functionality of this cell will be handled by decomposing. Asynchronous clear or set will be handled using multiclass functionality.

DESCRIPTION

Asynchronous functionality of sequential cells cannot be decomposed. Therefore only the synchronous functionality of the cell will be decomposed.

WHAT NEXT

No action is necessary. If you want the cell to be not moved or moved using the multiclass algorithm entirely, use the set_transform_for_retiming command.

RTDC-85 (warning) The cell %s has at least one asynchronous pin connected and the decompose transform attribute is set for it. Since the default transformation for asynchronous cells is dont_touch, this cell will not be moved.

DESCRIPTION

Asynchronous functionality of sequential cells cannot be decomposed. Because it is requested that asynchronous cells are not moved This cell will not be moved.

WHAT NEXT

No action is necessary. If you want the cell to be moved using the multiclass algorithm use the set_transform_for_retiming command.

RTDC-86 (warning) One or more cells in the design to be retimed have the retiming state attribute set to dont_care. The behavior of the retimed circuit may differ from that of the original circuit.

DESCRIPTION

The dont_care attribute allows retiming to achieve better quality of results or use less CPU time of optimization. However, the initial state of the retimed circuit not equivalent to that of the original circuit. This may be acceptable for registers on data paths. In general it is not acceptable for registers in control parts (finite state machines) of the circuit.

WHAT NEXT

No action is necessary. If you want the cell not to use the dont_care attributes for some or all cells use the set_state_for_retiming command or the -sync_state or -async_state attributes of the optimize_registers command.

RTDC-87 (warning) Net %s has the synch_set_reset attribute set. The following sequential cells in the net’s fanout may be moved away from the net during retiming.

DESCRIPTION

A synch_set_reset attribute on a net may indicate that the sequential cells in the fanout of this net should be connected to the net by as few logic levels as possible. The register movement during retiming may change this.

WHAT NEXT

If it is not important to you that registers are kept close to the net in question, no action is necessary. However, if you want to have the synchronous set or clear moved with the registers during retiming, use the following steps. 1. Analyze and elaborate the design from the HDL description using the HDL attribute sync_set_reset or the dc_shell variable hdlin_ff_always_sync_set_reset = true. 2. Put a dont_touch attribute on all the sequential cells in the elaborated design. 3. Compile the

combinational logic in the design. 4. Remove the dont_touch attribute from the sequential cells. 5. Run optimize_registers with the -sync_trans multiclass option.

RTDC-88 (warning) The optimize_registers or the pipeline_design attribute has been set on a design but the BOA-BRT license is not available.

DESCRIPTION

Retiming during compile requires a BOA-BRT license for the optimize_registers and pipeline_design attributes. In this case there is a key for the BOA-BRT license in the license file, but all BOA-BRT licenses are currently in use.

WHAT NEXT

The setting of the variable 'compile_retiming_license_behavior' determines whether, the execution of compile stops ("stop"), or waits for a license to become available ("wait"), or use the balance_registers functionality instead ("next") if the DC-Expert license is available. It has to be set before the start of compile. Another solution is to obtain the necessary license before the start of compile using the get_license command.

RTDC-89 (warning) A retiming attribute (optimize_registers, balance_registers, pipeline_design) has been set on a design but the DC-Expert license has not been authorized. Retiming cannot be performed.

DESCRIPTION

Retiming during compile requires a DC-Expert license for the balance_registers attribute and also for the optimize_registers and pipeline_design attributes, if the BOA-BRT license is not available. In this case no key for the DC-Expert license exists in the license file.

WHAT NEXT

You can purchase a license key for DC-Expert from Synopsys.

RTDC-90 (warning) A retiming attribute (optimize_registers,

balance_registers, pipeline_design) has been set on a design but the DC-Expert license is not available.

DESCRIPTION

Retiming during compile requires a DC-Expert license for the balance_registers attribute and also for the optimize_registers and pipeline_design attributes, if the BOA-BRT license is not available. In this case there is a key for the DC-Expert license in the license file, but all DC-Expert licenses are currently in use.

WHAT NEXT

The setting of the variable 'compile_retiming_license_behavior' determines whether, the execution of compile stops ("stop"), or waits for a license to become available ("wait"). It has to be set before the start of compile. Another solution is to obtain the necessary license before the start of compile using the get_license command.

RTDC-91 (warning) The design contains combinational cells that are not from the target library.

DESCRIPTION

The current design contains combinational cells that are not in the target library. This can happen for three reasons:

- The cell is not yet mapped.

- A dont_use attribute has been put on the library cell after the first compile but before retiming.

- One or more of the library cells in the netlist are marked as dont_use in the library itself. This can happen, if the netlist was created by a a software not respecting library defined dont_use attributes.

WHAT NEXT

Set all the dont_use attributes for on target library cells before the first compile. Make sure any dont_touch attributes on generic combinational cells are removed before the first compile. If your library description has internally dont_use attributes on various cells you have two options: Either make sure the tool creating the netlist is respecting these attributes or run an incremental compile on the netlist in Design Compiler before retiming.

RTDC-92 (warning) A timing arc with a negative delay was found found on cell %s (%s) from pin %s to pin %s. Using zero delay instead.

DESCRIPTION

```
Retiming does only work on netlists with non-negative
 delay cells.
```

WHAT NEXT

```
No action is necessary. However, it would be best to check your technology library
for correctness. If you want to avoid these warnings do not use the negative delay
library cell by putting a dont_use attribute on it before compiling your design for
the first time.
```

RTDC-93 (warning) A latch cell %s is found in retiming procedure. It will be treated as a fixed flip-flop.

DESCRIPTION

```
Retiming can not work on latches. A latch will not
 be moved, which might affect the quality of retiming.
```

WHAT NEXT

```
No action is necessary. However, it would be best to check what is the functionality
of the latch. Try to avoid using a latch in data path.
```

RTDC-94 (error) The clock signal of cell %s can not be reached from any clock port(s) via combinational logic.

DESCRIPTION

```
All the sequential cells in the retiming circuit must be
 controlled by any clock signal defined by the user.
```

WHAT NEXT

Please check the clock pin of the cell and make sure it is connected to a clock port defined by using create_clock command. Or you can exclude the cell from the design. This can be done by putting it into its own hierarchical module. Then retime only the other hierarchical modules.

SEE ALSO

create_clock.

RTDC-95 (error) The clock gating cell %s is controlled by more than one clock signal or by the rising and falling edge of the same clock. The clock signals are from cells %s and %s.

DESCRIPTION

The input signals of the clock gating cells can contain only one clock signal.

WHAT NEXT

Please check the clock nets connected to the gating cell and remove the extra clock signal(s).

RTDC-96 (error) The clock signal from %s is used as both master and slave clock.

DESCRIPTION

A clock signal can be used only as either master clock or slave clock of the sequential cell in the circuit. Using a clock signal as both make it impossible for the retiming tool to calculate the timing constraints of the circuit.

WHAT NEXT

Please check all the master-slave registers in the circuit and make sure that the master pins and slave pins are connected correctly.

RTDC-97 (warning) The output pin %s of the gating cell %s is

not unate with respect to the clock signal input pin %s.

DESCRIPTION

The output of a clock gating cell has to be unate to its clock input. Otherwise the clock might and might not be inverted when it passes through the gating cell, depending on the other control signals of the gating cell. Therefore it is impossible for the retiming tool to calculate the timing constraints. Any registers driven by this output pin of the clock gating cell will not be moved.

WHAT NEXT

If no register is driven by the particular pin of the clock gating cell no action it necessary. Otherwise correct your clock gating logic.

RTDC-98 (error) One of the following two registers is sensitive to the rising edge of their common base clock the other to the falling edge: %s %s

DESCRIPTION

There can be two causes of this problem. The first is that the number of inverters on the path from the clock driving pin to the clock pin of certain sequential cell is even, while the number on the path to the clock pin of some other sequential cell is odd. The other is that the library cells used for the registers are sensitive to different edges of the clock. Thus there are cells driven by opposite edges of the clock. This is not allowed for retiming.

WHAT NEXT

Check whether your clock tree is build correctly and whether you really need these differently triggered flip-flops in your design.

RTDC-99 (error) The master clock from %s and slave clock from

%s used to control cell %s are not matched.

DESCRIPTION

The master clock and slave clock form a pair to control the master-slave sequential cells. Neither a master clock nor a slave clock can be paired multiple times with different clock signals. Either the master clock or the slave clock has already been used with a third clock signal, therefore they are not allowed to used together.

WHAT NEXT

Check whether your clock tree is build correctly and check whether the master and slave clock pins of all the sequential cells are connected correctly.

RTDC-100 (warning) The clock signal generated from %s is connected to the non-clock pin of the sequential cell %s. The sequential cell will not be moved.

DESCRIPTION

The clock signal is connected to a non-clock pin of a sequential cell, such as the next-state input, or reset, or load-enable.

WHAT NEXT

If this is intended, no action is necessary. Otherwise please correct your circuit or your ’create_clock’ commands.

RTDC-101 (error) The output of the gating cell %s has 2 or more outputs. Cannot retime.

DESCRIPTION

In this version of the retiming package, the complexity of the gating cell is limited. Only cells with one output pin are allowed

WHAT NEXT

Please check whether the gating cell is correctly designed. Try to partition the gating cell into many blocks with only one output pin each.

RTDC-102 (warning) There is at least one clock which is not connected to any sequential cells directly.

DESCRIPTION

A clock signal, which does not directly control any sequential cell, exists. However it might be used to control one or more sequential cells through clock gating cell or simply pass through the circuit block.

WHAT NEXT

No action is necessary. However, it would be best to check when the clock tree is designed correctly.

RTDC-103 (warning) A black box cell %s is found on the clock tree.

DESCRIPTION

A black box cell is found on the clock tree. The clock tree analysis can not go into the cell. A black box cell can affect the quality of retiming because no sequential cells can be move across it.

WHAT NEXT

No action is necessary. However, it would be best to check whether the black box cell is designed correctly. Try to avoid black box cell in the circuit because it might affect the quality of retiming.

RTDC-104 (error) Two cells %s and %s drive clock net.

DESCRIPTION

A clock cell can not be driven by more than one cell. Cannot retime.

WHAT NEXT

Redesign the clock tree so that each clock net is driven by only one cell.

RTDC-105 (error) No clock is found.

DESCRIPTION

No clock port is defined by the user and no port is found to connect to any existing sequential cells.

WHAT NEXT

Please check the design of the clock tree and make sure that the clock pins of all the sequential cells are connected correctly and the clock source is connected to a port. In the pipeline design, a clock port has to be defined.

RTDC-106 (error) The both normal master slave sequential cells and fake master slave sequential cells exist. Cannot retime.

DESCRIPTION

A normal master slave sequential cell is controlled by two clock nets, i.e. a master clock and a slave clock. While a fake master slave sequential cell is controlled by only one master clock. Its slave pin is connected to a net with constant value. Retiming can handle a single clocking scheme, therefore these two types of cells can not co-exist.

WHAT NEXT

Please replace one type of sequential cells by the other.

RTDC-107 (information) The design contains the following cells in the master clock tree. Retiming will not try to improve timing for paths along these cells:

DESCRIPTION

Cells that have a master clock net connected to a non-clock input pin are not taken into account in the retiming timing analysis.

WHAT NEXT

No action is necessary.

RTDC-108 (information) The design contains the following cells in the slave clock tree. Retiming will not try to improve timing for paths along these cells:

DESCRIPTION

Cells that have a slave clock net connected to a non-clock input pin are not taken into account in the retiming timing analysis.

WHAT NEXT

No action is necessary.

RTDC-109 (error) Retiming with gated clocks is not supported with the balance_registers command.

DESCRIPTION

The design contains gated clocks. The balance_registers command is not allowed on such design.

WHAT NEXT

Use optimize_registers.

RTDC-110 (warning) Sequential cell %s is driven by an output of hierarchy cell %s which is being retimed. The registers in the hierarchy cell have a different clock than the sequential cell. The delay may not be correctly

optimized by retiming.

DESCRIPTION

Only part of the design is retimed. There are registers outside the part of the design being retimed and there is a combinational path from internal registers to these external registers. The registers at the endpoints of this path are driven by different clocks. The delay may not be correctly optimized by retiming.

WHAT NEXT

You can either use a bottom up compile strategy or change your design so that the retimed registers are only connected to registers driven by the same clocks.

RTDC-111 (warning) Sequential cell %s drives an input of hierarchy cell %s which is being retimed. The registers in the hierarchy cell have a different clock than the sequential cell. The delay may not be correctly optimized by retiming.

DESCRIPTION

Only part of the design is retimed. There are registers outside the part of the design being retimed and there is a combinational path from external registers to these internal registers. The registers at the endpoints of this path are driven by different clocks. The delay may not be correctly optimized by retiming.

WHAT NEXT

You can either use a bottom up compile strategy or change your design so that the retimed registers are only connected to registers driven by the same clocks.

RTDC-112 (warning) The design contains cells that have been used by Power Compiler’s clock gating. After retiming Power Compiler

clock gating commands will no longer work:

DESCRIPTION

Retiming cannot maintain the relations between clock gating cells and the registers gated by them. Therefore Power Compiler commands such as 'report_clock_gating' will no longer work correctly after retiming. The design is still functionally correct.

WHAT NEXT

No action is necessary.

RTDC-113 (error) The design the following nets that have multiple drivers.

DESCRIPTION

Retiming cannot operate on designs with nets with multiple drivers.

WHAT NEXT

Replace the multiple driver nets by cells calculating the desired logic function of the drivers.

RTDC-114 (error) The flip-flop %s selected with set_register_type or set_register_type_for_retiming cannot be used.

DESCRIPTION

A preferred flip-flop for retiming was specified with the set_register_type command but it cannot be used. Possible reasons are that no flip-flop with this name exists in the library or a dont_use attribute has been put on the flip-flop.

WHAT NEXT

Check whether a flip-flop of this name exists. If yes, remove the dont_use attribute from it.

RTDC-115 (warning) The following cells only drive asynchronous pins of sequential cells which have no timing constraint. Therefore retiming will not optimize delay through them:

DESCRIPTION

This warning message occurs when any paths to asynchronous cells of sequential cells do not have timing constraints. Therefore, retiming does not include cells on these paths that only drive such pins into the retiming optimization.

WHAT NEXT

This is a warning message only. No action is required on your part.

SEE ALSO

balance_registers, (2), **optimize_registers** (2).

RTDC-116 (error) The clock name '%s' which you selected is not among the clocks of the design. Possible clock names are:
'%s'

DESCRIPTION

If the user specifies the name of a single clock to retime, this name must be a name of one of the clocks that have been created on the design.

WHAT NEXT

Choose one of the legal clock names given in the error message or do not specify a clock name at all.

RTDC-117 (warning) A clock period has been specified at the command line. However, more than one clock in the

design will be retimed. The clock period will be ignored.

DESCRIPTION

If there are multiple clocks being retimed it does not make sense to specify a single clock period.

WHAT NEXT

You can just ignore this warning. Or you can limit the retiming to one clock using the 'clock' option.

RTDC-118 (warning) No movable %s for %s edge of base clock(s): '%s'.

DESCRIPTION

There must at least be one movable sequential cell (register or latch) for a particular edge of a base clock to be able to perform retiming. Sequential cells can become not movable for the following reasons, which are indicated by other warning messages: A dont_touch attribute has been set on them. They are the endpoint of a point to point exception such as false or multicycle path. There is not enough information available about its functionality. Depending on the options you used for the retiming command sequential cells without asynchronous set/clear or sequential cells with asynchronous set/clear may not be retimed either.

WHAT NEXT

This is just a warning. If you do not need to have any sequential cells triggered by this edge of the base clock retimed, no further action is necessary. Otherwise, find out what makes the sequential cells in your design not movable by looking at other warning messages. You can also use the check_design and verbose options of optimize_registers. Then take the appropriate measures to make some or all of the cells movable.

RTDC-119 (warning) Clock '%s' has its source in the movable sequential cell '%s'. The cell will not be moved.

DESCRIPTION

If a register with is the source of a clock is moved the clock would be lost.

Therefore it will not be moved.

WHAT NEXT

Check whether the clock should really come from this cell. If not correct your constraints. Otherwise no action is needed.

RTDC-120 (warning) No information can be found about the function of cell %s. Registers might not be moved across this cell because retiming cannot compute the equivalent reset state.

DESCRIPTION

The cell has no description of its function in the library. To improve delay or area retiming would like to move registers with set or clear signal across this cell. However, it cannot do so because it is not possible to compute the equivalent reset state. Therefore a retiming solution will be attempted that does not move any registers with set or clear functionality across this cell.

WHAT NEXT

No action is necessary. However, if you want registers to move across the cell you can do one of the following things:

Provide functionality of the cell in the library.

Use the decompose option for the registers that should move across the cell, if they have synchronous but no asynchronous set or clear.

Use the dont_care option on the registers in question or all registers, if the correct reset state is not important to you.

RTDC-121 (warning) The following registers are triggered by both the rising and the falling edge of the clock. They will not be moved during retiming.

DESCRIPTION

Instances of flip-flops which have setup or hold times, or clock-to-Q delays defined

for both the rising and the falling edge of the clock cannot be retimed.

WHAT NEXT

If you have to retime these registers implement them as single edge triggered flip-flops.

RTDC-122 (warning) The pin %s of the clock tree cell %s drives pins that are not part of the clock network.

DESCRIPTION

Retiming cannot handle cells that are both for the propagation of the clock signals and for operations on data signals accurately. Retiming results may not be the best possible.

WHAT NEXT

Try to change the circuit such that clock-tree and non-clock-tree functionality are never combined in the same cell.

RTDC-123 (warning) The design %s will not be retimed because the Formality-friendly flow is active.

DESCRIPTION

Retiming is suppressed in most cases during Design Compiler synthesis if the Formality-friendly flow is in effect. Only pipelined DesignWare multipliers are still retimed.

WHAT NEXT

If you want to have retime despite of the Formality-friendly flow set the dc_shell variable "optimize_reg_skip_retiming_for_formal_verification" to "false".

RTDC-124 (warning) Formal verification with the original design

will fail after the pipeline_design command.

DESCRIPTION

The pipeline_design command inserts additional registers into the circuit. The behavior of the modified circuit is no longer equivalent to that of the original circuit. Equivalence checking with the original design will fail.

WHAT NEXT

If you want to retime pipelined data path and be able to verify the design afterward with a formal verification tool, insert the registers into the original design and use the optimize_registers command.

RTDC-125 (warning) The Formality-friendly flow is active but retiming has been enabled.

DESCRIPTION

The Formality-friendly flow is active but retiming has been enabled. Retiming might make formal verification inconclusive.

WHAT NEXT

If you do not want to retime set the dc_shell variable "optimize_reg_skip_retiming_for_formal_verification" to "true".

RTDC-126 (warning) The design contains a min-delay path or an exception for hold time violations. Retiming results may be worse than expected.

DESCRIPTION

During retiming sequential cells that are start- or end-points of timing exceptions are not moved. If these timing exceptions are only addressing minimum delays or hold-time violations it might be worth while to remove them during retiming and reapply them after retiming to have them fixed during and incremental compile.

WHAT NEXT

If you think retiming results may be influenced negatively try removing these

exceptions during retiming.

RTDC-127 (Error) The design cannot be pipelined because the design contains the following cells with bidirectional pins.

DESCRIPTION

The pipeline_design cannot work on designs that contain bidirectional ports or cells with bidirectional pins.

WHAT NEXT

Remove the bidirectional ports and cells with bidirectional pins from the design or insert registers yourself and use the optimize_registers command.

RTDC-128 (Warning) The following clock-gating latches will not be moved during retiming.

DESCRIPTION

Clock-gating latches are latches that drive clock-gating cells to avoid glitches in gated-clock signals. These latches will not be moved during retiming.

WHAT NEXT

There is no need for any action.

RTDC-129 (Error) Did not find two-phase latch system for clock %s.

DESCRIPTION

When retiming latches using the **-latch** option of the **optimize_registers** command the latches have to be clocked by a two-phase clock system. I.e. every other latch must be transparent at a time when the intermediate latches are not transparent and vice versa. This can be achieved by several different clocking systems. E.g. a clock can drive the latches for one phase while an inverted version of the same clock drives the latches for the other phase. Or the same clock drives the latches for both phases but the latches for one of the phase are transparent when the clock is high, while those for the other phase are transparent when the clock is low. Or you have

to separate clocks one driving the latches for phase one and the other (with a waveform shifted by half a clock period compared to the first) driving the latches for the other phase.

WHAT NEXT

Check your design's clock network and check whether you have specified the correct clock for latch retiming.

SEE ALSO

optimize_registers (2).

RTDC-130 (Warning) The following latches are out of phase. They will not be moved during retiming.

DESCRIPTION

When retiming latches using the **-latch** option of the **optimize_registers** command the latches have to be clocked by a two-phase clock system. I.e. every other latch must be transparent at a time when the intermediate latches are not transparent and vice versa. The latches reported here have at least one neighbor which has the same phase as they. Therefore they will not be moved during retiming.

WHAT NEXT

Check your design's clock network to see whether you might have connected some of your latches to the wrong phase of the clock. If you did so on purpose no further action is necessary. If not, correct the design.

SEE ALSO

optimize_registers (2).

RTDC-131 (warning) Reset state justification was terminated early to reduce runtime.

DESCRIPTION

In order to be able to move registers including their reset connections, retiming needs to compute the equivalent initial state of the circuit after retiming. In this case the computation of the equivalent state for registers moved backward has failed. This is most likely caused by runtime or capacity limits.

Please switch to medium effort. However, using medium effort could lead to very long runtime.

WHAT NEXT

If you are not satisfied with the delay and area results, you may want to use medium justification effort in the optimize_registers or set_optimize_registers command. Please be aware that the medium effort level may greatly increase runtime, while an improvement in QoR is not guaranteed.

RTDC-132 (warning) Reset state justification was terminated early to reduce runtime.

DESCRIPTION

In order to be able to move registers including their reset connections, retiming needs to compute the equivalent initial state of the circuit after retiming. In this case the computation of the equivalent state for registers moved backward has failed. This is most likely caused by runtime or capacity limits.

Please recode the RTL such that registers are located at the primary inputs. Having registers at the primary inputs is suggested because forward justification of registers doesn’t take a long time. You could even use high justification effort. However, using high effort could lead to very long runtime.

WHAT NEXT

Please recode the RTL to have registers at the primary inputs. You could even try using high justification effort in the optimize_registers or set_optimize_registers command, if you are not satisfied with the delay and area results. Please be aware that the high effort level may greatly increase runtime, while an improvement in QoR is not guaranteed.

RTDC-133 (warning) QoR may not be optimal with medium justifcation effort.

DESCRIPTION

The QoR obtained with medium justification effort may not be optimal. Please recode the RTL such that registers are located at the primary inputs. Having registers at the primary inputs is suggested because forward justification of registers doesn’t take a long time. You could even use high justification effort. However, using high effort could lead to very long runtime.

WHAT NEXT

Please recode the RTL to have registers at the primary inputs. You could even try using high justification effort in the optimize_registers or set_optimize_registers command, if you are not satisfied with the delay and area results. Please be aware that the high effort level may greatly increase runtime, while an improvement in QoR is not guaranteed.

RTDC-134 (warning) Using high justification effort could lead to very long runtime.

DESCRIPTION

Using high justification effort could lead to very long runtime. You could avoid this problem by recoding the RTL to have registers at the primary inputs. Having registers at the primary inputs is suggested because forward justification of registers doesn’t take a long time.

WHAT NEXT

If justification doesn’t complete within a finite amount of time, please recode the RTL to have registers at the primary inputs. You could even try using medium justification effort in the optimize_registers or set_optimize_registers command to reduce runtime.

RTDC-135 (warning) Retiming is likely to run for an extended period of time due to the large design size.

DESCRIPTION

Global retiming is the most effective on pipelined datapath designs,
which are usually not very large. Retiming a large non-pipeline design
can incur very long run time, and in some cases, it may never finish.
Viable alternatives include retiming smaller sub-designs or using
adaptive retiming instead.

WHAT NEXT

Continue with retiming.

RTLE

RTLE-000 (error) Internal error.

DESCRIPTION

Some unspecified internal error occured. This is a bug.

WHAT NEXT

Please file a bug report.

RTLE-001 (warning) Cannot open input file '%s'.

DESCRIPTION

The listed file cannot be opened for input. Either it does not exist, or you don't have read permission.

WHAT NEXT

Ensure that the listed file is the desired file, that it exists, and that it is readable.

RTLE-002 (warning) Cannot access output directory '%s'.

DESCRIPTION

The listed directory cannot be used for output. Either it is a file, or it is a directory for which you don't have write permission, or it cannot be created.

WHAT NEXT

Ensure that the listed directory is the desired directory. If it exists, it must be writable. If it does not exist, its parent must be writable.

RTLE-003 (information) Writing edited '%s' to '%s'.

DESCRIPTION

This is a simple information message stating that the edited version of the specified source file is written out at the specified location. As a result of writing out this file, it is removed from memory. It is no longer available for further editing.

WHAT NEXT

No action required.

RTLE-004 (information) Writing edited '%s' as an sed script to %s.

DESCRIPTION

This is a simple information message stating that the edited version of the specified source file is written out as an sed script at the specified location. As a result of writing out this file, it is removed from memory. It is no longer available for further editing.

WHAT NEXT

The sed script can be played back on the original file to obtain the edited version as 'sed -e <orig_file>'.

RTLE-005 (warning) There are no files to write.

DESCRIPTION

A write command was issued, but there are no files to write.

WHAT NEXT

Ensure that the desired file was previously read in, but not already written out. Note that files are removed from active memory when they are written to disk.

RTLE-006 (warning) File '%s' is not currently loaded in the

editor; it cannot be written out.

DESCRIPTION

A write command was issued, but the specified file is not currently loaded in the editor.

WHAT NEXT

Ensure that the desired file was previously read in, but not already written out. Note that files are removed from active memory when they are written to disk.

RTLE-010 (warning) Syntax errors while reading file '%s'.

DESCRIPTION

Some syntax errors occured while reading the specified file. The file is not completely read into memory. The units in which the errors occured are missing. This will affect the editing commands pertaining to these units.

WHAT NEXT

From the strict point of view of this session, only the syntax errors affecting editing commands need be addressed. Look at the following messages to see what further commands are affected, if any. Look at the previous messages to understand the details of the syntax error.

RTLE-011 (warning) Overwriting unit '%s'.

DESCRIPTION

The last read file redefines the specified unit. The previous definition is discarded.

WHAT NEXT

Decide for yourself if this is desirable or not.

RTLE-012 (warning) Cannot find unit '%s'.

DESCRIPTION

The specified unit is not currently loaded in memory.

WHAT NEXT

Verify that the specified unit is the desired unit. Ensure that the file defining this unit was read.

RTLE-013 (warning) Cannot find %s '%s' in unit '%s'.

DESCRIPTION

The specified object cannot be found in this unit.

WHAT NEXT

Verify that the specified object is the desired object, of the desired type. Correlate with source code.

RTLE-014 (warning) %s '%s' already exists in unit '%s'.

DESCRIPTION

The specified object already exists. It cannot be created.

WHAT NEXT

Verify that the specified object is the desired object, of the desired type. Correlate with source code.

RTLE-015 (information) Module '%s' is not loaded.

DESCRIPTION

The specified module or entity is not currently loaded in memory. For the operation requiring it, it will be treated as a black box. In particular, the actual existence of such a module is assumed, not verified. The specifics of its interface--name and

direction of ports--is not known. As a result, there is no guarantee that the edited design will properly link.

WHAT NEXT

If full validation is required, the module should be read in. Otherwise, if script is known to be correct, no action is required.

RTLE-016 (information) Reading file '%s'.

DESCRIPTION

This is a simple information message stating that the specified file is read into the editor.

WHAT NEXT

No action required.

RTLE-017 (information) Copying unit '%s' to '%s'.

DESCRIPTION

This is a simple information message stating that the specified unit is duplicated. This enables different editing commands to be applied on the two copies, depending on the context.

WHAT NEXT

No action required.

RTLE-018 (information) Renaming unit '%s' to '%s'.

DESCRIPTION

This is a simple information message stating that the specified unit is renamed.

WHAT NEXT

No action required.

RTLE-019 (warning) Unit '%s'already exists; it cannot be %s over.

DESCRIPTION

The specified unit already exists. The copy or rename command has no effect. In particular, the existing unit is not modified.

WHAT NEXT

Check the script.

RTLE-020 (Warning) Output directory '%s' cannot be created.

DESCRIPTION

The specified directory does not currenlty exist but it cannot be created. Look at the following messages to see what recovery action was taken.

WHAT NEXT

Validate that the specified path is legal, and that its parent is writable. Ensure that there is some free space on the disk.

RTLE-021 (Information) Output directory '%s' is used.

DESCRIPTION

This simple information message states that a directory different than the one specified by the user is used. See the previous message to get some indication of why the original directory was not used.

WHAT NEXT

No action required.

RTLE-022 (Warning) '%s' exists, but it is not a writable directory.

DESCRIPTION

The specified pathname refers to an existing object on the file system, but it cannot be used as an output directory. Either it is not a directory, or it is not writable. Look at the following messages to see what recovery action was taken.

WHAT NEXT

Modify the directory specification or clean-up.

RTLE-023 (Error) No valid output directory.

DESCRIPTION

The write command fails as it cannot compute a valid output directory from the user specification.

WHAT NEXT

Ensure that the editor has access to a writable directory and that this directory is correctly specified.

RTLOUT-1 (warning) The designware operation '%s' is not one of the predefined designware operations. As a result, a call to a function with the same name of the operator will be written out, and the contents of that function will need to be provided.

DESCRIPTION

The levelized netlister currently does not understand all possible designware operators. For those operators that it doesn't understand, a function call will be written out with no body for the function. The user will then need to provide the contents of that function in order to simulate.

WHAT NEXT

There are two possible choices. First, the command **replace_synthetic** can be used to implement all synthetic parts. This is the most convenient solution, but it has the disadvantage of being slow, and writing out a slower and less comprehensible hdl netlist.

The second alternative is to supply the definition of the function. If VHDL is being written out, then the function can be encapsulated in a package, and that package can be included using the variable **vhdlout_use_pacakges**. For verilog, this can be done using a file that is included using the variable **verilogout_include_files**.

NAME **RTLOUT-2** (warning)

The DesignWare operator '%s' has a port '%s'
for which HDL type information could not be extracted. This port will be declared as a vector of bits (for example, std_logic_vector in VHDL), in the generated RTL code. This can result in errors during subsequent analysis of the HDL code.

DESCRIPTION

You receive this warning when Behavioral Compiler cannot determine the HDL type of a parameter to a subprogram call in the RT-level HDL description it is generating. This lack of type information can cause subsequent analysis of this HDL description to fail.

When Behavioral Compiler encounters a subprogram in the input behavioral HDL that is preserved as a level of hierarchy by the **map_to_operator** or the **preserve_function** pragmas, Behavioral Compiler gathers and stores information about the types of each of the parameters of the subprogram call.

Later, when RT-level HDL is output, the synthetic operator to which this subprogram call was mapped (or the subdesign formed by preserving the subprogram) is replaced by a call to a subprogram representing the combinational simulation model for the operator (or subdesign). The user must supply a package containing this combinational simulation model.

The behavioral subprogram can be used as the combinational simulation model only if the parameter list of the subprogram containing the combinational simulation model is identical to that of the original behavioral subprogram. Thus, Behavioral Compiler must ensure that the types of the parameters at the RT-level are the same as those of the parameters in the original behavioral subprogram declaration. This prevents "type mismatch" errors when the RT-level HDL code is analyzed prior to simulation.

This warning message means that Behavioral Compiler was unable to find the necessary typing information for a port of a subprogram call and cannot guarantee that the original behavioral subprogram body can be used as the combinational simulation model.

WHAT NEXT

Identify the reason why Behavioral Compiler was unable to find the typing information. There are two possibilities, as follows:

1. You might have constrained a previously declared unconstrained range in the parameter declarations of the subprogram, as in the following example:

```
procedure my_proc (
    I1 : in integer range 0 to 7;
    ...
);
```

The recommended methodology is to create a named subtype for this constrained range in the original behavioral description, and re-synthesize; for example,

```
subtype my_integer_type is integer range 0 to 7;
procedure my_proc (
          I1 : in my_integer_type;
  ...
          );
```

2. The design from which the levelized RT-level HDL code is being generated might not contain the necessary information; this can happen if you write out a design generated using an earlier version of Behavioral Compiler.

In this case, you can ignore the warning messages. The generated RT-level HDL should work correctly with combinational simulation models that worked with the earlier version of Behavioral Compiler.

NAME **RTLOUT-3** (information) Synthesizable RTLOUT is being written.

DESCRIPTION

Behavioral Compiler generates an HDL (Verilog or VHDL) output using write command. This message informs that the HDL output is being generated. You must have invoke write command with -rtl_script option to get this message. Synthesizable hdl output is a description of a scheduled design from Behavioral Compiler, and this output can be an input to many Synopsys RTL-level tools like Design Compiler, FPGA Compiler II, or Formality. Especially for Design Compiler, BC also generates a script file which constains a set of design constraints which are necessary for a consistent synthesis.

WHAT NEXT

Please look at the man page for write command. Synthesizable RTLOUT is generated only when -rtl_script option is given. The file format (-format), hierarchy (-hierarchy) and output (-output) options must also be given.

NAME **RTLOUT-4** (error) Only non-levelized (structural) %s shall be generated with -rtl_script option.

DESCRIPTION

Synthesizable RTLOUT is a description which contains both functional and structural RTL-level description. Though, most of the part is structural. So it cannot generate a levelized RTLOUT. Please change the variable setting of vhdlout_levelize or verilogout_levelize to false to generate a synthesizable RTLOUT. To see the current value of those variables, please use: list vhdlout_levelize (or verilogout_levelize). Even though the simulation speed is not as fast as the levelized output, the synthesizable RTLOUT is also simulatable. To run simulation with synthesizable RTLOUT, you must provide a simulation model for the components that are instantiated. For combinational logic gates, either the target library must have a simulation model or you may set vhdlout_equations (verilogout_equation) to true. With vhdlout_equations (or verilogout_equation) set to true, combinational logic is written as technology-independent Boolean equations. To determine the current value of this variable, use **list vhdlout_equations (or verilogout_equation)**. For a list of all **vhdlio** variables and their current values, use the **list -variables vhdlio** command.

WHAT NEXT

Please read manpages for vhdlout_levelize (verilogout_levelize) and vhdlout_equations (or verilogout_equation).

NAME **RTLOUT-5** (error) Writing synthesizable RTLOUT was not successful.

DESCRIPTION

This message simply indicates that the execution of writing synthesizable RTLOUT was not successful. There may be several reasons to get this error. First, the current design must have been generated by a correct version of schedule (2000.0x version or newer) which is designed to provide an appropriate information for synthesizable RTLOUT generation. Or another reason may be the incorrect command line options. Also, when the input description has at least one RTL block (process) is specified with behavioral processes, synthesizable RTLOUT will not be generated. Further detailed messages are printed along with this message most of the time.

WHAT NEXT

Please read write (2) manpage for the detailed description of write command with -rtl_script option.

NAME **RTLOUT-6** (error) Currently we do not allow a subdesign to be written for synthesizable RTLOUT. When we use ‘write -script_file’ command, please do not specify any design name.

DESCRIPTION

Currently only the implicit current design is written. To tell the name of the design to be written, use ’list current_design’. The current_design to be written must be a top design. Even though you set the current_design to be a subdesign, write -rtl_script command will not write out the subdesign since it’s not a top design. All the subdesigns instantiated under the top design (current_design) are automatically written. The constraint file whose name is specified with -rtl_script option contains Design Compiler constraints and the file will contain the constraints for all the (and only the) designs that are to be written.

WHAT NEXT

Please read write (2) command manpage with option -script_file.

NAME **RTLOUT-7** (information) %s is an alias for %s.

DESCRIPTION

In the scheduled design, all the register banks (bc registers) are uniquified, which implies that there is one-to-one correspondance between a design and an instantiation. Since many register banks may have the same bit width, reset values and reset characteristics, one design can be shared by multiple instantiations. This message informs which registers are sharing the same design, i.e. if A is an alias for B, only A design is written in synthesizable RTLOUT, then A is instantiated in replace of B.

WHAT NEXT

Please see write (2) command manpage to know more about synthesizable RTLOUT.

NAME **RTLOUT-8** (error) Design %s didn’t link properly.

DESCRIPTION

It’s actually the same error as LINK-5. This warning is issued when a suitable design can not be found to link a cell reference to. This will result in any cells using that reference being left as "black boxes". Generally this will happen because of one of two reasons: (1) either a design with the same name as the reference does not exist in the database, link libraries and the directories specified by the search_path, or, (2) the design exists but there are port mismatches between the reference and the design. In the second case an additional error message indicating the exact nature of the mismatch would be given.

WHAT NEXT

More information is available at LINK-5 manpage.

RTLOUT-9 (error) Unable to process design for writing synthesizable RTL output.

DESCRIPTION

You receive this error message because Behavioral Compiler is unable to process the design for writing out synthesizable RTL output.

This error can happen in a variety of circumstances:

1. Your design contains an RTL process.

2. Your design is missing implementation directives. This happens if you are trying to write synthesizable RTL output for a design scheduled with a version of Behavioral Compiler earlier than 2000.05.

3. Behavioral Compiler failed to implement the components used by your design.

WHAT NEXT

Typically, this message is preceded by another message regarding the specific error that caused Behavioral Compiler to fail processing. Refer to the manual page (manpage) for the specific error message issued.

SEE ALSO

write (2), **write_rtl** (2).

NAME **RTLOUT-10** (error) Option -rules_name should only be used to generate a synthesizable RTLOUT. Hence, -rtl_script must be given at the same time.

DESCRIPTION

This message is issued when write -rules_name is called without -rtl_script option. -rules_name is used for users to add more renaming rules in addtion to the default renaming rules. will generate a synthesizable HDL out which can be synthesized by Design Compiler.

WHAT NEXT

Please read write.2.

NAME **RTLOUT-11** (information) User-specified rename rules

shall be applied.

DESCRIPTION

There is a set of default renamings applied when we write an HDL (VHDL and Verilog). This set of rules is language specific. Since synthesizable RTLOUT generates both an HDL file and a constraint.scr file, the naming should be consistent. Therefore, we apply the same set of renaming rules for the object names in the constraint.scr file. In addition to this, an additional set of renaming rules may be defined by the user. This can be done by specifying -rules_name option in write command. This informs that a user has defined a certain renaming rules which shall be applied to

the script file that write -rtl_script command generates.

WHAT NEXT

Please read write -rtl_script <script_file> -rules_name <rules_name> manpage.

NAME **RTLOUT-12** (error) Applying user-specified rule %s was not successful.

DESCRIPTION

This message says that the user defined rename rule was not successfully applied. One obvious reason to get this error will be the named rule is not existent for some reason. When we applied a user defined rule, we show the renamed objects verbosely.

WHAT NEXT

NAME **RTLOUT-13** (information) Default rename rules are applied to pass design constraints from Behavioral Compiler to Design Compiler.

DESCRIPTION

When we write out an HDL output, a set of renaming rules is applied to the HDL output. In synthesizable RTLOUT, a constraint.scr file is also generated. When we write out a constraint script file, we have to apply the same set of renaming rules in order to maintain consistency between the script and the generated HDL file. Since the renaming is applied unconditionally, we do not provide an option not to apply the default renaming rules. So it’s not possible to disable the application of default renaming rules. When there is a set of user-defined renaming rules, the user-defined renaming rules will be applied first, and the default renaming rules will be the last one to be applied. A brief summary of renaming for each design is printed. Basically, the default renaming consists of renaming to remove illegal characters. The users are not encourage to check why a certain renaming is done because some renaming is forced to be done just to match the names between an HDL output and a constraint.scr file.

WHAT NEXT

Please look at change_names and define_name_rules to apply a user-specified rename rule. Also see write commmand manpage, especially, -rtl_script and -rules_name option to apply addtional user defined rules for synthesizable HDLOUT and its corresponding constraint.script file.

NAME **RTLOUT-14** (error) Application of default renaming rules was not successful.

DESCRIPTION

This is an error flag which says that the default renaming rule is not successful. This is very unlikely to happen though. This just checks the status of the command.

WHAT NEXT

This may be issued when the behavior of change_names or define_name_fuleschanges.

NAME **RTLOUT-15** (error) Option -rtl_script should only be used for a BC design which has been manipulated for synthesizable RTLOUT.

DESCRIPTION

The write command with -rtl_script will generate a synthesizable HDL out which can be synthesized by Design Compiler. This message is issued when write -rtl_script is called with a design which is not generated (scheduled) by Behavioral Compiler.

WHAT NEXT

Please read write command manpage with -rtl_script option.

NAME **RTLOUT-16** (error) Currently, write -rtl_script command should be used to write only the entire design hierarchy. Please use -hierarchy option with -script_file option.

DESCRIPTION

Only the entire design is written for synthesizable RTLOUT. Currently no design_list should be given when you invoke write -rtl_script commmand. The current_design should be set to the top design. We may support to write out a synthesizable sub-design in the future. Also a script file will be created and the created script file will contrain compile constraints for all the designs under the top design.

WHAT NEXT

Please understand 'current_design' command and design hierarchy. The design to be written as a synthesizable rtlout must be a top-design.

NAME **RTLOUT-17** (error) You may not use %s option with -rtl_script option.

DESCRIPTION

This message is printed when there is an incompatible option specified with -rtl_script option. Since we only support a limited form of write command, the option -rtl_script is not compatible with several options of write command. Here is a summary on how to use write command for synthesizable RTLOUT.

The option -rtl_script followed by a file name (constraint.scr file) must be given. Option -hierarchy, -output and -format must be given as well. The file name specified with -output option is the name of an HDL while which contains the synthesizable RTLOUT. The format name must be either Verilog or VHDL. No other format is allowed. -rules_name option may or may not given depending on the existence of user-defined renaming rules. The following options must not be used with -rtl_script option: -name_files, -library, -modified and -no_implicit. Also the design_list must not be given, and the 'current_design' should be set to the top design.

WHAT NEXT

See manpage for write (2) commmand.

NAME **RTLOUT-18** (error) -rules_name option should be used with -rtl_script option.

DESCRIPTION

-rules_name option must be used only with -rtl_script option. It is used to specify a user-defined renaming rules in addition to the default renaming rules applied to object names in the design. The renaming rules are applied to the objects in the constraint file, not the real HDL files. When write command is writing an HDL file, there is a set of renaming rules applied to the names of the object unconditionally. They are mainly to remove illegal characters. To maintain the consistency between the names in the HDL file and those in the constraint.scr file, the default renaming rule of the synthesizable RTLOUT is applied. When user wants to apply additional renaming rules, then she/he can use -rules_name option. However, it is important to remember that the default renaming rule is the one which will be applied last to give the highest priority among the renaming rules.

WHAT NEXT

Please see the man page for define_name_rules, change_names, and write command.

NAME **RTLOUT-19** (error) The design is not scheduled by Behavioral Compiler.

DESCRIPTION

The write command with -rtl_script option should be called only with the design which is scheduled by Behavioral Compiler. Otherwise, this error shall be issued. One important thing to remember is to use a new version of schedule command (2000.05 or newer) to generated the scheduled db. Otherwise, the write -rtl_script command will not recognize the scheduled db as an input for writing synthesizable RTLOUT. Also when the write -rtl_script is invoked, the current_design must be set to the top-level design. The preprocessing for synthesizable RTLOUT inside the schedule command is not computation or memory intensive. Therefore, the preprocessing step should not cause more computation time or memory requirement.

WHAT NEXT

Please see the manpage for write command, and also read manpage for schedule command.

NAME **RTLOUT-20** (error) Missing implementation directives for design %s.

DESCRIPTION

Implementation directive should have been attached during scheduling. But when it’s not existent this error is issued. This implementation directive will be used to instantiate a DesignWare component for each synthetic operator in the synthesizable RTLOUT. You have to use a new schedule executable which enables synthesizable RTLOUT (either 2000.05 version or newer). As long as you use an appropriate schedule command, it’s very unlikely that you shall get this error.

An example of information when there is no problem is:

Information: Sharing and implementation directives for process ’P’: (RTLOUT-22) Instance 0: Processor ’DW02_mult’ Implementation ’csa’ Operations: mul_23, binding ’b4’ mul_21, binding ’b4’

This message shows that two operations mult_21 and mult_23 will share a functional unit DW02_mult with the implementation ’csa’.

WHAT NEXT

Please see man page for schedule and write command.

RTLOUT-21 (error) Design %s contains RTL process %s, which is not supported while writing synthesizable RTL output.

DESCRIPTION

Behavioral Compiler does not support writing out synthesizable RTL output for a design that contains both behavioral and RTL processes.

WHAT NEXT

Do one of the following:

1. Separate the behavioral and RTL processes into different designs.

2. Use the **write_rtl** command with the **-ignore_rtl** argument to write out synthesizable RTL output. The RTL processes are removed from the design prior to writing synthesizable RTL output. You must manually insert the original RTL processes into the synthesizable RTL model prior to logic synthesis.

SEE ALSO

write (2), **write_rtl** (2).

NAME **RTLOUT-22** (information) Sharing and implementation directives for process ’%s’:

DESCRIPTION

This informs directives for sharing and implementation module for each process in the design. To print this information, you have to set bc_synrtl_debug_mode to TRUE.

An example of information with this message is:

Information: Sharing and implementation directives for process ’P’: (RTLOUT-22)
Instance 0: Processor ’DW02_mult’ Implementation ’csa’ Operations: mul_23, binding ’b4’ mul_21, binding ’b4’

This message shows that two operations mult_21 and mult_23 will share a functional unit DW02_mult with the implementation ’csa’.

WHAT NEXT

NAME **RTLOUT-23** (information) Sharing is prohibited on the process.

DESCRIPTION

A hidden flag is create to prohibit a sharing for a set of constructs which are not allowed to be shared. This message is only printed when bc_synrtl_debug_mode is true, and normally when this message is issued, generating synthesizable HDL out is not successful. One typical case is where there is a mixture of behavioral processes and RTL processes. For RTL processes, the hidden flag is set to prohibit sharing.

WHAT NEXT

NAME **RTLOUT-24** (error) Output file name must be specified with -output option when you write a synthesizable RTLOUT.

DESCRIPTION

The write command line options are checked for synthesizable RTLOUT, and this message is issued when -rtl_script option is given without -output option. Unlike the original write command, the output file name must be provided when you write a synthesizable RTLOUT with -rtl_script option. When write command is called with arguement -script_file, -format option must be given with vhdl or verilog, and -hirarchy option must be given too.

WHAT NEXT

Please see manpage for write command.

NAME **RTLOUT-25** (information) %s name '%s' changed to '%s'

DESCRIPTION

This message is issued when the name changes by the renaming routines for synthesizable RTLOUT. While generating synthesizable RTLOUT, several types of objects are renamed to make the names consistent with the names in the synthesizable HDL file. The reason is depending on the format of the HDL file, there are different sets of renaming applied. These renamed names will be used to write the synthesizable HDL file. Therefore, we need to apply the same set of renaming to

match the name of the objects in the constraint.scr file. Port names and designs names with illegal characters are changed. Note that the renaming by synthesizable RTLOUT will be used to write constraints.scr file, and it will not affect the HDL file.

WHAT NEXT

Please see manpage for write command with -rtl_script option.

NAME **RTLOUT-26** (error) The format should be either VHDL or Verilog for synthesizable HDLOUT.

DESCRIPTION

The synthesizable HDLOUT only writes out VHDL or Verilog RTL-level code. Where there is no -format option, the option is set to "db" format by default. Therefore, you should specify the format name either as VHDL or Verilog to generate a synthesizable RTLOUT. A different set of constraint.scr file shall be created depending on the output language format. This is because the hierarchical structure of the output file is different and also the names in the script file may have gone through a different renaming rule application.

WHAT NEXT

See manpage for write command with -rtl_script option.

NAME **RTLOUT-27** (information) Register bank, %s’s enable signal is masked by M port. In synthesizable HDLOUT, the register bank will be written in bit-level instead of word-level to indicate which bits are masked.

DESCRIPTION

M port is to selectively mask the enable signal so that we can update the contents of a register bank selectively. The enable signal is shared by all the bits in the register bank which makes impossible to update the contents partially. BC has made M port available to provide a way to do it. In the synthesizable RTLOUT, all register banks are written at a word-level by default. For those register banks with M port connected, they shall be written at bit-level to represent the masking of individual bits.

WHAT NEXT

Please see manpage for write command.

NAME **RTLOUT-28** (information) %s %s is written in the rtlout.

DESCRIPTION

This message shows the value of bc_synrtl_write_preserved_functions or bc_synrtl_write_precompiled_designware is TRUE. If they are true, the design for preserved_function or precompiled designware is written in the synthesizable rtlout. If they are FALSE (by dafault), all such components have instantiations only and then you have to provide a db (design) file under the design library.

WHAT NEXT

Please see manpage for bc_synrtl_write_preserved_fucntions and bc_synrtl_write_precompiled_designware variable.

NAME **RTLOUT-29** (information) %s %s is instantiated, and must be resolved via link.

DESCRIPTION

This message shows the value of bc_synrtl_write_preserved_functions or bc_synrtl_write_precompiled_designware is FALSE. If they are FALSE (by dafault), all such components have instantiations only and then you have to provide a db (design) file under the design library. If they are true, the design for preserved_function or precompiled designware is written in the synthesizable rtlout.

WHAT NEXT

Please see manpage for bc_synrtl_write_preserved_fucntions and bc_synrtl_write_precompiled_designware variable.

NAME **RTLOUT-30** (information) Mapping to target_library %s.

DESCRIPTION

This message shows the value of bc_synrtl_map_to_gtech. By default the value is TRUE. When it’s TRUE, the target library is set to be GTECH. And components are mapped to GTECH components. If you want to use a real target library, you have to

set the variable bc_synrtl_map_to_gtech to be false. To see the current value, please use list bc_synrtl_map_to_gtech.

WHAT NEXT

Please see manpage for bc_synrtl_map_to_gtech.

NAME **RTLOUT-31** (information) Synthesizable RTLOUT will generate constraint.script in both dcsh and dctcl because bc_synrtl_write_dcsh_and_dctcl is on. The current dc_shell is running in %s mode. Therefore, the given file name is used to write in %s script, and %s is used to generate a %s script.

DESCRIPTION

Synthesizable RTLOUT generates a constraint.script file. The format is either dcsh or dctcl and is automatically selected according to the current running mode of the dc_shell. Under some circumstance, user may want to generate constraint.script file in both format. For example, user is running dc_shell in eqn mode, and wants to generate a constraint.script file in dctcl. In this case, they can set variable: bc_synrtl_write_dcsh_and_dctcl to true. Then two copies of the constraint script file will be generated, one is in dcsh and the other one is in dctcl. By default the value is false.

When a single script is generated, the name of the script file will be the same as the given as the arguement, regardless of the format. When both are generated, the script in the same format as the current dc_shell mode will have the same name as the arguement, and the other script will have a name which contains some suffix. The suffix will be "-t" for a tcl script, and "-eqn" for a dcshl script.

For example, when a dc_shell is running in normal (non-Tcl) mode, if the variable bc_synrtl_write_eqn_tcl_script is true, when write -rtl_script <file_name> is called, <file_name>-t is generated as the constraint script file in tcl format in addition to <file_name> as the constraint script file in eqn format.

WHAT NEXT

Please see manpage for bc_synrtl_write_dcsh_and_dctcl.

RTLOUT-32 (information) write_rtl has successfully generated

%s RTLOUT.

DESCRIPTION

You receive this informational message because the **write_rtl** command has successfully generated a synthesizable RTL model or a simulation RTL model.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

write_rtl (2).

RTLOUT-33 (error) write_rtl has failed to generate %s RTLOUT.

DESCRIPTION

You receive this error message because the **write_rtl** command has failed while generating a synthesizable RTL model or a simulation RTL model.

WHAT NEXT

This error message is always preceded by other error messages that provide details about the failure. See the man pages for those error messages to determine how to recover from this error.

SEE ALSO

write_rtl (2).

NAME **RTLOUT-34** (information) By default, %s is set to TRUE when synthesizable RTLOUT is generated. Use -use_gates

option if you need to set the variable to FALSE.

DESCRIPTION

WHAT NEXT

NAME **RTLOUT-35** (error) You must provide the %s option.

DESCRIPTION

WHAT NEXT

NAME **RTLOUT-36** (error) Translation of tech-mapped gates into gtech gates is effective only when precompiled netlist or preserved function is written out. Please use -translate option with -precompiled_designware and/or -preserved_functions.

DESCRIPTION

WHAT NEXT

NAME **RTLOUT-37** (warning) Functional model for DW components shall be written. Note that not all the DW instantiations can map to a functional operator.

DESCRIPTION

```
Here is a list of designware components that we can map to a functional model:
DW01_add, DW01_inc, DW01_dec, DW01_sub, DW01_incdec, DW01_addsub, DW02_mult,
DW02_divide, DW01_cmp2, DW01_cmp6.
```

WHAT NEXT

```
See man page for write_rtl command.
```

NAME **RTLOUT-38** (error) Argument(s) which is not relevant to the %s RTLOUT is given.

DESCRIPTION

WHAT NEXT

NAME **RTLOUT-39** (error) ‘-rtl_script’ option is required to generate the synthesizable RTLOUT.

DESCRIPTION

WHAT NEXT

NAME **RTLOUT-40** (error) ‘-syn’ and ’-sim’ options are given at the same time. Either synthesizable or simulatable RTLOUT is generated using the write_rtl command.

DESCRIPTION

WHAT NEXT

RTLOUT-41 (information) Translating design %s from %s to GTECH succeeded.

DESCRIPTION

```
You receive this message because translation of the specified design from the target
library to a Synopsys GTECH netlist representation succeeded. This is an
intermediate step in the generation of a synthesizable RTL model.
```

WHAT NEXT

```
This is an informational message. No action is required on your part.
```

SEE ALSO

write_rtl (2).

RTLOUT-42 (error) Translating design %s from %s to GTECH failed.

DESCRIPTION

You receive this error message because certain components in the design for which the synthesizable RTL model is being generated contain target library components that cannot be translated into GTECH components. The generated synthesizable RTL model will contain instantiations of the target library components.

WHAT NEXT

Provide synthesis models of the target library components.

SEE ALSO

write_rtl (2).

RTLOUT-43 (information) %s is written as a functional model.

DESCRIPTION

You receive this message because while writing a synthesizable RTL model, the specified component was written out functionally instead of being instantiated. For example, a DW01_add component would be written out at a "+" operator.

Replacing components with functional models wherever possible removes the dependence of the RTL model on any specific component library and allows RTL synthesis tools the freedom to select their own implementations for the operators.

WHAT NEXT

This is an informational message. No action is required on your part.

SEE ALSO

write_rtl (2).

RTLOUT-44 (warning) %s is being instantiated but has no model.

DESCRIPTION

You receive this warning message because Behavioral Compiler has detected a synthetic DesignWare component in the specified design for which there is no implementation or functional representation available. You must supply an implementation for the component prior to running RTL synthesis on the synthesizable RTL output. In the synthesizable RTL output, this component will be instantiated. The implementation for the component exists inside a synthetic library of DesignWare parts. Each component of a synthetic library has a VHDL or Verilog model that defines the component.

WHAT NEXT

If you are writing out a synthesizable RTL model in VHDL, you must include the package that contains this model. You can do this using the **-use_packages** argument of the **write_rtl** command. For example:

```
dc_shell> write_rtl -use_packages { dw01.dw01_components } -f vhdl -o my_synrtl.vhd
```

If you are writing out a synthesizable RTL model in Verilog, you must read in the Verilog model for the component into the relevant tool when using the synthesizable model in simulation or RTL synthesis.

SEE ALSO

write_rtl (2).

NAME **RTLOUT-45** (error) The format should be either VHDL or Verilog for ‘write_rtl’ command.

DESCRIPTION

WHAT NEXT

RTLOUT-46 (information) For the preprocessing of synthesizable RTLOUT, target_library is temporarily set to { %s } from { %s }. The original target_library will be restored after the

preprocessing step.

DESCRIPTION

You receive this message because during the generation of a synthesizable RTL model, the target library is temporarily modified. The target library will be restored to its original value after preprocessing.

WHAT NEXT

This is an informational message. No action is required on your part.

SEE ALSO

write_rtl (2).

RTLOUT-47 (information) Translating design %s from %s to GTECH succeeded.

DESCRIPTION

You receive this message because the translation of the specified design from the target library to a Synopsys GTECH netlist succeeded. This is an intermediate step in the generation of a synthesizable RTL model.

WHAT NEXT

This is an informational message. No action is required on your part.

SEE ALSO

write_rtl (2).

RTLOUT-48 (error) Translating design %s from %s to GTECH failed.

DESCRIPTION

You receive this message because certain components in the design for which the synthesizable RTL model is being generated contain target library components that cannot be translated into GTECH components. The generated synthesizable RTL model

will contain instantiations of the target library components.

WHAT NEXT

To perform RTL synthesis on the synthesizable RTL model, provide synthesis models of the target library components.

SEE ALSO

write_rtl (2).

RTLOUT-49 (information) Mapping to target library %s.

DESCRIPTION

You receive this message because the synthesizable RTL model being generated will contain instantiations of components from the specified target library. To perform RTL synthesis using this model, you must provide synthesis models of the components from the target library.

WHAT NEXT

This is an informational message. No action is required on your part.

SEE ALSO

write_rtl (2).

RTLOUT-50 (error) Only simulatable (levelized) %s output can be generated with the -format systemc option.

DESCRIPTION

You receive this message because

although the **write** command can generate RTL-level output in the systemc language once a behavior-level design has been synthesized through the SystemC compiler, currently support exists only for a simulatable model of the RTL output. The **systemcout_levelize** variable must be set to **true** to generate this output. To see the current value of this variable, use **list systemcout_levelize**.

Note that the input behavior-level language must be SystemC. Use of any other HDL language (VHDL, VERILOG) as the input language may not result in a usable RTL-level output.

WHAT NEXT

See man page for the **systemcout_levelize** variable.

RTLOUT-51 (warning) The RTLOUT writer cannot determine if the input HDL was SystemC or finds that the input is in a language different from SystemC.

DESCRIPTION

You receive this message because the RTLOUT writer is writing out in the SystemC language but cannot determine that the input design was also written in SystemC. RTLOUT writer either could not determine the input format or found that the input format is in some other language (for example, VHDL or Verilog).

This may result in interface port type information not being available to the RTLOUT writer. The ports of the RTL module being written out may not match those of the input behavior, resulting in compilation mismatches with the testbench.

This may mean that any information about the types of various interfaces (input, output ports, and function calls) may not be available to the RTLOUT writer. The output then uses a default type. This may result in compilation mismatches with the testbench.

WHAT NEXT

Identify the reason why the RTLOUT writer finds a mismatch in the input language and the output format it is expected to write in. The two possibilities for this are as follows:

• The input language is some other HDL/ High Level language. Since this is not supported, the you must use this flow at your own risk.

• If the input language is SystemC, the SystemC Compiler was not used to synthesize the design.

RTLOUT-52 (error) Output format must be specified as VHDL, Verilog, or SystemC.

DESCRIPTION

You receive this error message because you have not specified a valid output format with the **write_rtl** command. The **write_rtl** command requires that you specify a valid

output format as an argument.

WHAT NEXT

Reexecute the **write_rtl** command and specify a valid output format.

SEE ALSO

write_rtl (2).

RTLOUT-53 (error) Output file name must be specified.

DESCRIPTION

You receive this error message because you did not specify an output file name with the **write_rtl** command. You must specify an output file name with this command.

WHAT NEXT

Reexecute the **write_rtl** command and specify an output file name.

SEE ALSO

write_rtl (2).

RTLOUT-54 (error) The %s argument is invalid when used with the %s output format.

DESCRIPTION

You receive this error message because, with the **write_rtl** command, the specified argument cannot be used with the specified output format.

WHAT NEXT

Reexecute the **write_rtl** command and specify a valid argument.

SEE ALSO

write_rtl (2).

RTLOUT-55 (error) Synthesizable SystemC RTL output is not currently available.

DESCRIPTION

You receive this error message because you have used the **write_rtl** command to write synthesizable RTL output with SystemC as the output format. This is not currently supported.

WHAT NEXT

Either use VHDL or Verilog as your output format for synthesizable RTL output, or specify the **-simulation** argument to write a simulation RTL model in SystemC.

SEE ALSO

write_rtl (2).

RTLOUT-56 (warning) The %s argument has no effect when the %s argument is used.

DESCRIPTION

You receive this warning message because you have executed the **write_rtl** command and have specified an argument that will be ignored in the presence of the second argument.

WHAT NEXT

Verify that you want the first argument to be ignored. Remove one of arguments to prevent this warning message from being generated.

SEE ALSO

write_rtl (2).

RTLOUT-57 (warning) The %s argument has no effect when

used without the %s argument.

DESCRIPTION

You receive this warning message because you have executed the **write_rtl** command with an argument that will be ignored unless you also include the second argument.

WHAT NEXT

If you do not want the specified argument to be ignored, reexecute the **write_rtl** command and specify both arguments.

SEE ALSO

write_rtl (2).

RTLOUT-58 (error) The -rtl_script argument must be specified when writing synthesizable RTL output.

DESCRIPTION

You receive this error message because you have executed the **write_rtl** command without the **-rtl_script** argument. You must specify this argument so that the **write_rtl** command has a place to write the constraints needed to guide synthesis of the synthesizable RTL model that is written out.

WHAT NEXT

Reexecute the **write_rtl** command and specify the **-rtl_script** argument.

SEE ALSO

write_rtl (2).

RTLOUT-59 (information) RTL synthesis constraints will be written to RTL synthesis script file %s.

DESCRIPTION

You receive this message because you have executed the **write_rtl** command but have not specified the **-rtl_script** argument. The necessary RTL synthesis constraints will

be written into a script file with the name specified in the information message.

WHAT NEXT

This is an informational message. No action is required on your part.

SEE ALSO

write_rtl (2).

RTLOUT-60 (error) The simulation optimized RTL output option is not available for a design configured for behavioral synthesis targeting an FPGA.

DESCRIPTION

You receive this message because simulation optimized RTL output is not available on a design configured for behavioral synthesis targeting an FPGA. Use the default RTL output, which can also be simulated.

WHAT NEXT

Use the **write_rtl** command to generate a synthesizeable, simulatable RTL model. Be careful not to use the **-simulation** option of **write_rtl**.

EXAMPLES

The following example shows how to use **write_rtl** to generate an appropriate RTL model.

```
dc_shell> write_rtl -format vhdl -output \
my_rtl_design.vhd
```

SEE ALSO

set_fpga (2), **write_rtl** (2).

SAIF-1 (error) The SAIF file contains switching data for the design '%s';
this switching data cannot be annotated on the design '%s'.

DESCRIPTION

This message indicates that the design for which the switching data was written, as indicated by the DESIGN construct of the SAIF file, is not the **current_design**. The name in the DESIGN construct of the SAIF file must be the name of the **current_design**.

WHAT NEXT

Verify that the SAIF file was created for the **current_design**, and if so, edit the SAIF file so that the DESIGN construct contains the name of the **current_design**.

SAIF-2 (warning) The SAIFVERSION values we accept is '%s'.

DESCRIPTION

This message indicates that the current SAIF file was written using an unrecognized revision of the SAIF language. Revisions recognized by the current version of the **read_saif** command are listed in the message.

This message is a warning only; **read_saif** attempts to read the file. However, if syntactic or semantic errors occur, suspect version incompatibility.

WHAT NEXT

If the file is read successfully, you need to do nothing. However, if the file is not read successfully, verify that the SAIF file created is compatible with one of the versions indicated by this warning message.

SAIF-3 (error) The time unit in a SAIF file must be one of these:

s, ms, us, ns, ps, fs.

DESCRIPTION

The SAIF language syntax requires that the timing unit must be either s, ms, us, ns, ps, or fs. Check your SAIF file and make sure this is the case.

WHAT NEXT

This is an error.

SAIF-4 (error) The time_scale in a SAIF file must be one of these:
1, 10, 100.

DESCRIPTION

The SAIF language syntax requires that the time_scale must be either 1, 10, or 100. Check your SAIF file and make sure this is the case.

WHAT NEXT

This is an error.

SAIF-5 (error) %s at or near token '%s'.

DESCRIPTION

A lexical or syntactic error has occurred in processing this SAIF file.

WHAT NEXT

Look at the line and token indicated in the message, and fix the problem.

SAIF-6 (warning) The object '%s' does not belong to

the instance '%s'. The object is ignored.

DESCRIPTION

The -instance option specifies the design instance and its sub-design instances that will be annotated into DesignPower. Any other object is ignored by the read_saif command. This warning message means that the specific object does not belong to the design instance or any of it sub-design instances, and is therefore ignored.

WHAT NEXT

This is a warning.

SAIF-7 (warning) The -instance parameter, '%s' is a substring of the object '%s', but it is not a complete name. The object is ignored.

DESCRIPTION

The -instance option must specify a full path name. For example, "-instance TOP/TEST" is a valid option for an object name "TOP/TEST/design/cell/A", but "-instance TOP/TE" is not.

WHAT NEXT

Please check your read_saif command to make sure you have specified a correct -instance option.

SAIF-8 (warning) The object '%s' has been found without a containing module, after '%s' is stripped off. The object is ignored.

DESCRIPTION

It is most likely that you did not appropriately specify the -strip_module option. Check the option and make sure you did NOT strip off the instance name of the top design module where the SAIF file is applied.

WHAT NEXT

This is a warning.

SAIF-9 (error) The simulation duration time is less or equal to 0.

DESCRIPTION

The duration field specified in the SAIF file must be a positive value.

WHAT NEXT

This is an error.

SAIF-10 (error) The read_saif command can only read a backward-annotation SAIF file.

DESCRIPTION

The **read_saif** command only supports a backward-annotation SAIF file.

WHAT NEXT

This is an error. Check you SAIF file again and verify that it is a backward-annotation SAIF file.

SAIF-11 (error) This file has a version number greater than 2.0, but it does not contain the "DIRECTION ..." construct.

DESCRIPTION

The SAIF file with version 2.0 or greater must have the "DIRECTION ..." construct to specify if this is a forward or backward-annotation SAIF file.

WHAT NEXT

This is an error.

SAIF-12 (error) Unable to open file %s.

DESCRIPTION

The **read_saif** command can not open the SAIF file.

WHAT NEXT

Make sure the file exists.

SAIF-13 (warning) Cannot find the equivalent %s pin of the cell %s.

DESCRIPTION

The pin name "Q" or "Z" for a virtual instance in SAIF is a logical name. The **read_saif** command tried to find the equivalent pin in the actual library cell but failed. The likely cause is pin name in the SAIF file has been manually changed, or the library cell information is not available.

WHAT NEXT

This is a warning.

SAIF-14 (error) Path dependent switching activity has to be specified inside the state dependent switching activity.

DESCRIPTION

SAIF syntax does not allow both path depedent and state dependent switching activity appear at the same level. You have to embedded path dependent switching activity inside state dependent switching activity.

WHAT NEXT

This is an error.

SAIF-15 (error) Only timing attribute information can be

specified inside the LEAKAGE construct.

DESCRIPTION

SAIF syntax does not allow toggle data appear inside the LEAKAGE construct. The LEAKAGE construct is used to capture state dependent static probability. Therefore, only timing attribute information can be specified here.

WHAT NEXT

This is an error.

SAIF-16 (warning) Can’t find object ’%s’.

DESCRIPTION

A specific object, net/pin/port, can not be found in the current design.

WHAT NEXT

This is a warning.

SCALING

SCALING-001 (Error) Tried to set library into multiple scaling library groups.

DESCRIPTION

In scaling mode, a particular library can be put in only one scaling library group. Otherwise, tool will not know which scaling library group should be used to perform scaling on the library cell.

WHAT NEXT

Check there is not overlap between any two scaling library group

SCALING-002 (Error) Arc mismatching error. The arc '%s' on cell '%s' does not exist on cell '%s'.

DESCRIPTION

In scaling mode, all cells, which are treated as the different versions of the same cell by the linker, will be link to a unique library cell. Therefore, in order to acquire the accurate timing with scaling, tool require all arcs should match exactly between cells when they are linked together. If arc mismatching exist between libraries, those mismatched arcs could be possibly ignored to accommodate scaling. The timing accuracy could be lost in such case.

WHAT NEXT

Fix the library to revise the mismatched arcs.

SCALING-003 (Warning) set_min_library command is obsolete in scaling mode, please use set_scaling_lib_group -min instead.

DESCRIPTION

In scaling mode, there is no need to use set_min_library any more. The command set_scaling_lib_group -min can serve all set_min_library command purpose and provide more flexibility.

WHAT NEXT

Replace set_min_library with set_scaling_lib_group -min

SCALING-004 (Warning) Duplicated arcs in one cell. The arc '%s' on cell '%s'is duplicated.

DESCRIPTION

In scaling mode, in order to do arc scaling within a scaling library group, all the corresponding arcs from the libraries in the group are found to fetch the needed data. In the case there are multiple exactly same arc in one library cell, the first incoming will be pickup as the scaling candidate and all other duplicated peers are ignored. If this arc is not the one desired, unexpected result will appear.

WHAT NEXT

Make sure the first arc is the desired arc to be used for scaling. Try to remove other duplicated arcs if they are unnecessary.

SCAN

SCAN-1 (error) Can’t open init file ’%s’.

DESCRIPTION

WHAT NEXT

SCAN-2 (error) Init file ’%s’ has improper format.

DESCRIPTION

WHAT NEXT

SCAN-3 (error) Invalid data format.

DESCRIPTION

WHAT NEXT

SCAN-4 (error) %s: Lexical Error on line %d at or near ’%s’.

DESCRIPTION

WHAT NEXT

SCD-2 (error) Operations in resource ’%s’ can not be shared because they may execute in the same control step %s

DESCRIPTION

WHAT NEXT

SCD-4 (error) Operations in resource %s are part of a combinational feedback loop(%s).

DESCRIPTION

You receive this message if the **compile** command finds that a combinational feedback loop would occur in the final design as a result of manual resource sharing directives. Operations cannot be shared if doing so causes a combinational feedback loop.

WHAT NEXT

Review your manual resource sharing directives for the specified resources, and modify them so that they do not create a combinational feedback loop. For information about how sharing can create a combinational feedback loop, see the section on Data Flow Conflicts in either the *VHDL Compiler Reference Manual* or the *HDL Compiler for Verilog Reference Manual*.

SCD-7 (error) You must specify the module using ’map_to_module’ if you want to set the implementation%s

DESCRIPTION

WHAT NEXT

SCD-9 (information) Additional cells were grouped along with

specified cells
because they must be in the same design as the grouped logic which they control.

DESCRIPTION

WHAT NEXT

SCD-10 (information) Some cells were not grouped because they must be in the same
design as the logic which they control.

DESCRIPTION

WHAT NEXT

SCD-11 (information) Some cells were duplicated in both the original and grouped
design because these cells control logic in both the original and grouped design.

DESCRIPTION

WHAT NEXT

SCD-12 (warning) Operation '%s' can not be included in a resource. It will not be implemented on '%s' %s

DESCRIPTION

WHAT NEXT

SCHD-1 (error) %s ’%s’ in design ’%s’ has no symbol.

DESCRIPTION

WHAT NEXT

SCHD-2 (error) %s ’%s’ in design ’%s’ has no symbol library.

DESCRIPTION

WHAT NEXT

SCHD-3 (error) The symbol library of %s ’%s’ in design ’%s’ has no name.

DESCRIPTION

WHAT NEXT

SCHD-4 (warning) Symbols were generated because they were

not found in any library.

DESCRIPTION

WHAT NEXT

SCHD-5 (error) %s '%s' has no symbol.

DESCRIPTION

WHAT NEXT

SCHD-6 (error) Could not load bitmap file '%s'.

DESCRIPTION

WHAT NEXT

SCHD-7 (error) Could not find reference name for cell '%s' on the schematic.
Was this schematic created with an older version of Synopsys software?

DESCRIPTION

WHAT NEXT

SCHD-8 (error) '%s' is not a valid justification specification.

DESCRIPTION

WHAT NEXT

SCHV-1 (error) Plot command is not available.

DESCRIPTION

WHAT NEXT

SCO-001 (error) Cannot open net components net ID:%d.

DESCRIPTION

You received this error message because scan chain optimization failed to access net data for buffering.

WHAT NEXT

Verify netlist.

SDC-1 (information) Setting sdc_version outside of an SDC file has no effect

DESCRIPTION

You set the **sdc_version** variable outside of the context of an SDC file. In that context, changing the variable has no effect.

WHAT NEXT

No action necessary.

SDC-2 (warning) SDC version in file (%s) does not match the version you requested
from read_sdc (%s). Some constraints and options may not function.

DESCRIPTION

The version indicated by the setting of the **sdc_version** variable in your SDC file does not match the version requested by the **read_sdc** command.

WHAT NEXT

Ensure that you select the correct version when issuing the **read_sdc** command.

SDC-3 (warning) Constraint '%s' is not supported by %s.

DESCRIPTION

Not all Synopsys Design Constraints are supported by all applications. The specified constraint is not supported by the current application, and it is ignored. For example, test constraints are not recognized by PrimeTime. One SDC-3 message is issued per instance of the constraint which is ignored. Then, after **read_sdc** completes, an SDC-4 summary message will tell you how many of each constraint was ignored.

WHAT NEXT

SDC-4 (information) Ignored %d unsupported '%s' constraint%s.

DESCRIPTION

This is a summary message indicating how many instances of a particular constraint were ignored by **read_sdc** because the constraint is unsupported.

WHAT NEXT

SDC-5 (error) Errors reading SDC file: %s. Use error_info for more info.

DESCRIPTION

This message is generated by **read_sdc** when an syntax error occurs during the read. The specific error is shown in the text of the message.

WHAT NEXT

You can use **error_info** to help trace the cause of the error. For example, it might show the file and line number of the syntax error.

SDFN-1 (warning) The delay type variables must be: 'minimum' 'typical' or 'maximum'. '%s' is invalid, '%s' will be used by default.

DESCRIPTION

The delay type variable is invalid, it must be 'minimum', 'typical' or 'maximum'. Read the man pages of variables **sdfin_rise_net_delay_type**, **sdfin_fall_net_delay_type**, **sdfin_rise_cell_delay_type** and **sdfin_fall_cell_delay_type** for explanations on how these variables are used.

WHAT NEXT

The type specified is invalid, the default is to read the 'maximum' delay value from the timing fields in the SDF file.

SDFN-2 (warning) The library '%s' has no time unit specified, '%s' is assumed.

DESCRIPTION

The library has no time unit specified. By default the time unit is nanosecond and time scale is 1. The only valid library time unit for the sdf format are 0.001, 0.01, 0.1, 1, 10 and 100. The time unit is specified in the library with the attributes **time_scale** and **time_unit_name**. For example, a library with timing values in 10 picoseconds unit is specified with the attributes: **time_scale = 10** and **time_unit_name = ps read_timing** assumes the technology library time unit is 1ns. The time unit in the sdf file is specified with TIMESCALE construct.

WHAT NEXT

If this assumption is incorrect, modify the scale and time unit of the sdf timing file before reading it in Design Compiler.

SDFN-3 (warning) No library was found on the search path, time unit '%s'

is assumed.

DESCRIPTION

There was no library found on the search path.

WHAT NEXT

Verify the search path with **list search_path** and verify the link library is under the search path. The link library is specified with **link_library**. Use **link** to verify the design has necessary libraries on the search path. Read the timing file once again after fixing the link errors.

SDFN-4 (error) The SDF file contains delays for the design '%s', they cannot be annotated on design '%s'.

DESCRIPTION

The current design and the design the SDF file was written for are not the same. They must be the same. The DESIGN construct in the sdf file contains the name of the design the timing file was written for. This name should be the same as the **current_design**.

WHAT NEXT

Verify the sdf file was created for the current design, the DESIGN construct in the sdf file should contain the name of the current design. Check the usage of the **read_timing** command, you might need to use the **-path** option.

SDFN-6 (warning) Cell delay could not be annotated between pin '%s', and pin '%s' for the design '%s'.

DESCRIPTION

The sdf timing file contains an IOPATH construct, specifying a cell delay between the pins specified in this warning message. The delay could not be annotated on the current design, the reason should be explained from a previous error message. The timing values in the sdf file could be invalid. The sdf file could be invalid if it contained references of non leaf cell pins. Only top level ports and leaf cell pins must be in the sdf file. The sdf file might have been created for a different level of the design hierarchy. The design names might have been renamed since the sdf file

was created, if so regenerate a sdf file. The sdf file is case sensitive. Other delays in the sdf file have been annotated on the design.

WHAT NEXT

Check the sdf file was created for the current design, verify the use of **read_timing**, you might need to use the **-path** option. Make sure there was no renaming performed in the design, regenerate the sdf file if this was the case.

SDFN-7 (warning) Interconnect delay could not be annotated between pin '%s', and pin '%s' for the design '%s'.

DESCRIPTION

The sdf timing file contains an INTERCONNECT construct, specifying a net delay between the pins specified in this warning message. The delay could not be annotated on the current design, the reason should be explained from a previous error message. The timing values in the sdf file could be invalid. The sdf file could be invalid if it contained references of non leaf cell pins. Only top level ports and leaf cell pins must be in the sdf file. The sdf file might have been created for a different level of the design hierarchy. The design names might have been renamed since the sdf file was created, if so regenerate a sdf file. The sdf file is case sensitive. Other delays from the sdf file have been annotated on the design.

WHAT NEXT

Check the sdf file was created for the current design, verify the use of **read_timing**, you might need to use the **-path** option. Make sure there was no renaming performed in the design, regenerate the sdf file if this was the case.

SDFN-9 (warning) Instance '%s' could not be found.

DESCRIPTION

The sdf timing file contains an instance that could not be found in the design. The instance name is specified with the construct INSTANCE in the sdf file. The sdf file is invalid if it contains references to instances not in the current design. Note the sdf file is case sensitive. Also the design must be free of link errors before annotating delays with **read_timing**. The design names might have been renamed since the sdf file was created, if so regenerate a sdf file. Some delays might have been annotated on the design before the error occured. **sdfin_top_instance_name** must be used if the SDF instance names contain the top level name of the design. Synopsys SDF reader assumes the top level name of the design is not included in the instance names.

WHAT NEXT

Verify the design does not have link errors, with the **link** command. Make sure there was no renaming performed in the design, regenerate the sdf file if this was the case. Check with **report_annotated_delay** if any delay have already been annotated. Use **remove_annotated_delay** to remove unwanted annotated delays. Set **sdfin_top_instance_name** to the top design name if SDF instance names contain the top level design name.

SDFN-10 (warning) Pin '%s'/'%s' could not be found.

DESCRIPTION

The sdf timing file contains a pin that could not be found in the design. The sdf file could be invalid if it contains references of non leaf cell pins. The sdf file might have been created for a different level of the design hierarchy. The design names might have been renamed since the sdf file was created, if so regenerate a sdf file. Note, the sdf file is case sensitive. Some delays might have been annotated on the design before the error occured. **sdfin_top_instance_name** must be used if the SDF instance names contain the top level name of the design. Synopsys SDF reader assumes the top level name of the design is not included in the instance names.

WHAT NEXT

Check the sdf file was created for the current design, verify the use of **read_timing**, you might need to use the **-path** option. Make sure you have no link error, with the **link** command. Make sure there was no renaming performed in the design, regenerate the sdf file if this was the case. Set **sdfin_top_instance_name** to the top design name if SDF instance names contain the top level design name.

SDFN-11 (error) Port '%s' could not be found.

DESCRIPTION

The sdf timing file contains a port that could not be found in the design. The sdf file could be invalid if it contained references of non leaf cell pins. Only top level ports and leaf cell pins must be in the sdf file. The sdf file might have been created for a different level of the design hierarchy. The design names might have been renamed since the sdf file was created, if so regenerate a sdf file. Note, the sdf file is case sensitive. Some delays might have been annotated on the design before the error occured. **sdfin_top_instance_name** must be used if the SDF instance names contain the top level name of the design. Synopsys SDF reader assumes the top level name of the design is not included in the instance names.

WHAT NEXT

Check the sdf file was created for the current design, verify the use of **read_timing**, you might need to use the **-path** option. Check with **link** that your design has no link error. Make sure there was no renaming performed in the design, regenerate the sdf file if this was the case. Check with **report_annotated_delay** if any delay have already been annotated. Use **remove_annotated_delay** to remove unwanted annotated delays. Set **sdfin_top_instance_name** to the top design name if SDF instance names contain the top level design name.

SDFN-12 (warning) Net delay could not be annotated on pin or port '%s' for design '%s'.

DESCRIPTION

The delay specified with PORT construct in the SDF file could not be annotated on the design. The reason should be explained from a previous error message. The sdf file could be invalid if it contained references of non leaf cell pins. Only top level ports and leaf cell pins must be in the sdf file. The sdf file might have been created for a different level of the design hierarchy. The design names might have been renamed since the sdf file was created, if so regenerate a sdf file. The sdf file is case sensitive. Other delays from the sdf file have been annotated on the design.

WHAT NEXT

Use the **link** command to check if the design has link errors. The design must be free of link errors before using **read_timing**. Check the sdf file was created for the current design, verify the use of **read_timing**, you might need to use the **-path** option. Make sure there was no renaming performed in the design, regenerate the sdf file if this was the case.

SDFN-13 (warning) The SDF file contains negative cell delays.

DESCRIPTION

Negative cell delays are supported within Design Compiler. It is very strange to back-annotate negative cell delays. You can use **report_annotated_delay -cell** to see the back-annotated cell delays.

WHAT NEXT

Use **report_annotated_delay -cell** to see which cells are annotated with negative delays. Verify with the person who wrote the SDF file if negative delays make sense.

SDFN-14 (warning) The SDF file contains negative net delays.

DESCRIPTION

Negative net delays are supported within Design Compiler. It is very strange to back-annotate negative net delays. You can use **report_annotated_delay -net** to see the back-annotated net delays.

WHAT NEXT

Use **report_annotated_delay -net** to see which nets are annotated with negative delays. Verify with the person who wrote the SDF file if negative delays make sense.

SDFN-15 (error) SDF version '%s' is not supported. Use version '%s'.

DESCRIPTION

The sdf file was written in a format not supported by Design Compiler. Design compiler read_timing reads only files written in SDF version 1.0, 1.1 and 2.1. In the SDF file, the SDFVERSION field indicates the SDF version. This field must contain a ratified OVI version like '1.0', or '1.1', or '2.1'. Note, Design Compiler does not support SDF version 2.0.

WHAT NEXT

Write from the layout tool a SDF in v1.0, v1.1 or v2.1 format. Reading other format version than 1.0, 1.1 or 2.1 might generate syntax errors.

SDFN-16 (information) Reading '%s' values for '%s'.

DESCRIPTION

The sdf file can contain minimum, typical, or maximum values for each delay. This message indicates if **read_timing** has back-annotated the minimum, typical or maximum value onto the design.

WHAT NEXT

If this setting is not correct, use the variables **sdfin_rise_cell_delay_type**, **sdfin_fall_cell_delay_type**, **sdfin_rise_net_delay_type**, **sdfin_fall_net_delay_type**.

SDFN-17 (warning) ’%s’ is read as an instance of ’%s’ but is linked to design ’%s’.

DESCRIPTION

The sdf file contains delays for the specified instance. But this instance’s reference in the SDF file is different from the instance’s reference in the current design. The SDF file is invalid for the current design. This situation can happen if the design has been changed and an old SDF file is read onto the design.

WHAT NEXT

Use **remove_annotated_delay** to remove the back-annotated values. Then use **read_timing** again with a new SDF file.

SDFN-18 (error) Cell ’%s’ is not hierarchical.

DESCRIPTION

Currently, we only support hierarchical cell as possible instances when option ’-instance’ used in command write_sdf.

WHAT NEXT

SDF writing will stop after this message.

SDFN-19 (information) Multiple instances found, only instance %s be dumped into SDF file.

DESCRIPTION

This prompt message will be seen when option ’-instance’ feed with multiple instances collection.

WHAT NEXT

Change your own definition for ’-instance’ to make sure only unique instance will be selected.

SDFN-20 (error) ’%s’ is not a valid triplet name for max.

DESCRIPTION

The valid triplet names for the -max_triplet option are maximum, typical, or none.

WHAT NEXT

Change the triplet name in the read_timing command.

SDFN-21 (error) ’%s’ is not a valid triplet name for min.

DESCRIPTION

The valid triplet names for the -min_triplet option are minimum, typical, or none.

WHAT NEXT

Change the triplet name in the read_timing command.

SDFN-22 (error) If minimum triplet name is ’none’, the maximum triplet
name cannot be ’none’.

DESCRIPTION

Both minumum triplet and maximum triplet names are set to ’none’. At least one of these names must be set to a value other than ’none’.

WHAT NEXT

Change the triplet name in the read_timing command.

SEC-0 (error) Software is not licensed for this machine.

DESCRIPTION

Could not find a valid matching key in the key file for this feature

WHAT NEXT

Check to see that the machine hostid, using the machine_id utility provided by Synopsys, matches the hostid in the key file for the feature.

SEC-1 (error) %s

DESCRIPTION

The key file with all of the license information cannot be opened.

WHAT NEXT

Check directory and file read permissions.

SEC-2 (error) Cannot open key file '%s' or a licensing environment parameter has not been set correctly.

DESCRIPTION

The keyfile cannot be read.

WHAT NEXT

Check the location of the keyfile to see if a keyfile is present and it is readable.

SEC-3 (error) Encryption file header is corrupt.

DESCRIPTION

WHAT NEXT

SEC-4 (error) Unknown encryption method.

DESCRIPTION

The application is trying to match the encryption with that in the keyfile. The encryption being used is not correct.

WHAT NEXT

Make sure that the executable is not corrupt or has not been changed.

SEC-5 (warning) License for '%s' expires within %2d days.

DESCRIPTION

The license for the listed feature is going to expire within 2 days.

WHAT NEXT

Contact your Synopsys support representative.

SEC-6 (warning) License for '%s' has expired.

DESCRIPTION

The license for the listed feature has expired.

WHAT NEXT

Please contact your Synopsys support representative.

SEC-10 (error) Software is not licensed for this machine.

DESCRIPTION

There was a problem matching the key file information to the machine you are trying to run the software on.

Possible causes are bad encryption code and the hostid specified in the license file does not match the node on which the software is running.

WHAT NEXT

Check to see if the hostid in the key file matches the machine hostid.

Check to make sure that the key certificate encryption code exactly matches the key file encryption code.

Contact your Synopsys support representative.

SEC-11 (error) Software is not yet enabled or has expired.

DESCRIPTION

The feature trying to be used does not have a valid license. Either the date may be wrong or the encryption may be wrong.

WHAT NEXT

Check the start date of the feature. It may not have been reached. Contact your Synopsys support representative.

SEC-12 (error) Can’t communicate with the license server.

DESCRIPTION

The machine you are running the software on is having trouble communicating with the license server.

The attempt to the connect to the vendor daemon on all SERVER nodes was unsuccessful.

WHAT NEXT

Check to make sure that the daemon name in the license file FEATURE line matches the

vendor daemon name.

Check to see that the ethernet device can be located.

Check network connections from node running software to server node(s).

Contact local System Adminitrator.

SEC-13 (error) The date/time difference between your host and the license server host is too great.

DESCRIPTION

The date/time difference between your host and the license server host cannot be greater than 4 hours.

WHAT NEXT

Contact local System Administrator to synch client/host times.

SEC-14 (error) Key file syntax error: %s.

DESCRIPTION

The start or expiration date is invalid.

WHAT NEXT

Check the dates in the license file.

Contact your Synopsys support representative.

SEC-15 (error) Key file '%s' has an unrecognized format.

DESCRIPTION

The keyfile is unreadable.

WHAT NEXT

Check the permissions on the file. It may also not be a text file.

SEC-16 (error) Can't read the '%s' file.

DESCRIPTION

The file /dev/kmem or /vmunix is not readable on this system.

WHAT NEXT

Contact you local System Administrator.

SEC-17 (error) Internal licensing error number %d: %s.

DESCRIPTION

A possible reason is a bad encryption handshake with the server. The client performs an encryption handshake operation with the daemon prior to any licensing operations. This handshake operation failed.

A possible reason is the feature database got corrupted in the daemon. The daemon's run-time feature data-structures have somehow become corrupted. This is an internal daemon error.

A possible reason is that there is no TCP/IP service "license." This happens if a SERVER line does no specify a TCP/IP port number, and the TCP service does not exist. There is no socket to talk to the server on.

WHAT NEXT

Make sure that there is a socket number in the SERVER line of the key file. Also check with your system administrator.

SEC-18 (error) Unknown internal licensing error number: %d.

DESCRIPTION

Unknown error has occurred.

WHAT NEXT

Check the status of the license server and the vendor daemon. Try bringing down the license server and bringing it back up again.

SEC-20 (error) This site is not authorized for license(s): %s

DESCRIPTION

This site is not licensed to use this product.

WHAT NEXT

Make sure that the required features are in the key file.

Use lmstat to make sure that the server has enabled the required features.

Contact your local Synopsys Support Center.

SEC-21 (error) Failed to checkout license for feature(s): %s

DESCRIPTION

The application failed to check out the licenses required to enable this product. It may be that all the licenses are in use or the site is not licensed to use this product.

WHAT NEXT

Make sure that the required features are in the key file.

Use lmstat to make sure that the server has enabled the required features and to find the current users of the features.

Contact your local Synopsys Support Center.

SEC-22 (information) %s feature '%s'.

DESCRIPTION

This is an informational message indicating the feature that has been queued, checked-out, or checked-in.

WHAT NEXT

If the feature has been queued for sometime, then you can find out the current users of this feature (by using the lmstat -A command) and request them to release it.

SEC-23 (information) Waiting for required feature(s). (%s)

DESCRIPTION

This is an informational message that is displayed periodically when the process is queued for required set of features. You can find out the current users of all the required features by using the lmstat -A command.

WHAT NEXT

Request the current users to release the licenses, if possible.

Let the process wait in queue for indicated period of time to acquire the license.

SEC-50 (error) All '%s' licenses are in use.

DESCRIPTION

The maximum number of licenses has been reached.

WHAT NEXT

Contact your Synopsys support representative to order more licenses.

SEC-51 (error) This site is not licensed for '%s'.

DESCRIPTION

A possible cause is that no such feature exists. The feature could not be found in the license file.

A possible problem is that the version is not supported at the server end. The version specified in the checkout request is greater than the highest version number the daemon supports.

A possible problem is that the server does not support this feature or the feature has expired or has not yet started (on the server node).

WHAT NEXT

Check to make sure that the license file supports this version.

SEC-52 (error) Requested more licenses for '%s' than supported in the key file.

DESCRIPTION

A checkout request was made for more licenses than are supported in the license key file.

WHAT NEXT

Make sure that you hvae enough licenses in the keyfile.

SEC-53 (error) The end-user license options EXCLUDE you from using '%s'.

DESCRIPTION

The user/host/display has been excluded from this feature by an end-user's daemon option file.

WHAT NEXT

Contact your local System Administrator to have your name removed from the EXCLUDE list in the options file.

SEC-54 (error) The end-user license options don’t INCLUDE you for using ’%s’.

DESCRIPTION

The user/host/display has NOT been included in this feature by an end-user’s daemon option file.

WHAT NEXT

Contact your local System Administrator to include you in the options file.

SEC-55 (error) Can’t remove your ’%s’ license. You must always have one or more of the following license(s): %s.

DESCRIPTION

A request was received to remove a license that is necessary for the application to be run. At least one of these licenses is required for the application to be running.

WHAT NEXT

Make sure that you are removing the right license.

SEC-80 (information) Attempting to reacquire license for ’%s’; wait %d minutes.

DESCRIPTION

The node has lost communication with the license server and is attempting to reacquire a license. It will try to reestablish connection every minute for the first X minutes (default is 10, but it will use the number supplied with the *-timeout* option). It will retry for four days.

WHAT NEXT

Contact your local system administrator to check to see whether the license server or network is hung.

SEC-81 (information) Reacquired license for '%s' after %d minutes.

DESCRIPTION

The application lost the license due to some reason. It could be that the vendor daemon died or the license daemon died and it was brought back up again. The application tries to reconnect to the daemon a few times.

WHAT NEXT

Make sure that the license and vendor daemons are running.

SEC-82 (warning) License server is busy, retrying.

DESCRIPTION

The application server is "busy" trying to connect. The license server is busy establishing a quorum of server nodes so that licensing can start.

WHAT NEXT

Wait a few minutes. If the license daemon does not start up, bring it down and back up again. It could also be that one of the servers in the redundant server configuration is down.

SEC-83 (warning) Timeout value must be between %d and %d; using default of %d.

DESCRIPTION

The timeout value used is not correct.

WHAT NEXT

Use the correct timeout value.

SEC-84 (warning) Unable to obtain a license for '%s'. Obtained a license for '%s' instead.

’%s’ contains these features:%s.

DESCRIPTION

Not all licenses for the application could be checked out.

WHAT NEXT

Check the keyfile amd make sure that you have the licenses for all the features in the product.

SEC-85 (error) Communication with the license server failed; error number %d.

DESCRIPTION

Bad return from server. The port number returned from lmgrd is invalid. An attempted connection to a vendor daemon did not result in a correct acknowledgement from the daemon. The daemon did not send back a message within the timeout interval. A message from the daemon had an invalid checksum.

Cannot read from server. The process cannot read data from the daemon within the timeout interval. The connection was reset by the daemon (usually because the daemon exited) before the process attempted to read data.

Cannot write to server The process could not write data to the daemon after the connection was established.

Feature checkin failed at daemon end The checkin request did not receive proper reply from the vendor daemon (the license might still be considered in use).

WHAT NEXT

Make sure that the port number and the path to the daemon in the keyfile are correct. Either the daemon is down or the machine is not alive. Try checkin again or try removing the license for that feature.

SEC-86 (error) This site is not licensed for third party software; error number %d.

DESCRIPTION

A possible cause is that no such feature exists. The feature could not be found in

the license file.

A possible problem is that the server does not support this feature or the feature has expired or has not yet started (on the server node).

WHAT NEXT

Check to make sure that the license file supports this version.

SEC-87 (error) Unable to obtain license for '%s'. Feature is suppressed.

DESCRIPTION

The functionality cannot be invoked for this product package. Possible cause is the functionality is not supposed to be supported for this product package, eventhough the license key is available.

WHAT NEXT

If the functionality should be within the product package, contact your Synopsys support representative.

SEC-88 (warning) Unable to set precedence for key '%s'. Cyclic dependency detected.

DESCRIPTION

Cyclic dependency on the prerequisite licenses detected. Some features may not execute because of inability to obtain license. If you encounter this warning, please report it to your Synopsys sypport representative.

WHAT NEXT

Contact your Synopsys support representative.

SEC-89 (information) Unable to set precedence for key '%s'.

Precedence already exists.

DESCRIPTION

Order of prerequisite licenses has already existed. Re-setting the precedence is redundant, and does not cause any harm.

WHAT NEXT

Contact your Synopsys support representative to ensure that the redundant order setting is removed in the next product release.

SEC-100 (error) This can only be used with software that is network licensed.

DESCRIPTION

The application is licensed to run only with network licensing. You may be running the application by using a node locked license.

WHAT NEXT

Check the keyfile being used.

SEC-101 (information) No one is using any feature from the license server.

DESCRIPTION

No features from the keyfile are being used.

WHAT NEXT

Nothing needs to be done.

SEC-102 (error) Unable to get an optimize license.

DESCRIPTION

The license cannot be obtained.

WHAT NEXT

Check the keyfile for this feature. Check the location of the keyfile, default or SYNOPSYS_KEY_FILE.

SEC-103 (error) You must have a Design-Analyzer or one of the optimize licenses to use this feature.

DESCRIPTION

The keyfile must have a Design-Analyzer or an optimize license to use this application.

WHAT NEXT

Check to see if the keyfile has these features. Check whether the correct keyfile is being used.

SEC-104 (information) Checking out the license '%s'.

DESCRIPTION

This is a message from the daemon that the license for this feature is being checked out.

WHAT NEXT

Check whether you are using this feature. If so, nothing needs to be done.

SEC-105 (information) Checking in the license '%s'.

DESCRIPTION

This is a message from the daemon that the license for this feature is being released.

WHAT NEXT

Nothing need to be done.

SEC-106 (information) Checking out '%s' implies that '%s' is also available. Checking '%s' back in to avoid duplicate license checkout.

DESCRIPTION

The new license key, "DesignWare", is issued to replace the following old license keys: "DesignWare-Foundation", "SynLib-ALU", "SynLib-AdvMath", "SynLib-Control", "SynLib-FltTol", "SynLib-Seq". When the new key is checked out, no old key will be checked out. If any of the old keys are already checked out, they are checked back in to avoid having duplicate licenses checked out.

This is a message from the daemon that the license for the specified feature is being released, because it is not needed.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEL-001 (error) No such collection '%s'

DESCRIPTION

The collection which you specified does not exist.

WHAT NEXT

Verify that the collection is the one you want. It is possible that it existed, but was transient. Transient collections are automatically garbage-collected and cannot be relied upon across command boundaries. In order to make a collection persistent, set it to a variable, and then use it. For example:

```
set uPorts [get_ports U*]
command_for_ports $uPorts
```

SEL-002 (warning) Collection '%s' has inappropriate type (%s).

DESCRIPTION

The collection which you specified contains objects which are not acceptable for this command. Either the data type of the objects is incorrect, or the objects are out of context (for example, they are not in the current design).

WHAT NEXT

Check the command to determine the allowable object types for it, or specify objects that are in the correct context.

SEL-003 (warning) Nothing implicitly matched '%s'

DESCRIPTION

The pattern which you specified did not match any objects of the classes acceptable for this command.

WHAT NEXT

Check the pattern to see if it is what you expected.

SEL-004 (warning) No %s objects matched '%s'

DESCRIPTION

The pattern which you specified did not match any objects of the class acceptable for this command.

WHAT NEXT

Check the pattern to see if it is what you expected.

SEL-005 (error) Nothing matched for %s

DESCRIPTION

The pattern(s) which you specified did not match any objects.

WHAT NEXT

Check the values which you entered.

SEL-006 (error) More than one object matched for '%s'.

DESCRIPTION

The pattern(s) which you specified matched more than one object. This command option accepts only a single object.

WHAT NEXT

Check the values which you entered.

SEL-007 (error) Invalid index %d for collection %s

DESCRIPTION

During an iteration over a collection (with foreach_in_collection), an invalid index was generated.

WHAT NEXT

Contact your application consultant.

SEL-008 (warning) Collection/attribute class '%s' has not been defined

DESCRIPTION

The collection class which you specified does not exist. Classes of objects include designs, cells, etc.

WHAT NEXT

Verify that the class name is spelled correctly, or that the class of objects is applicable for this product.

SEL-009 (warning) Collection class '%s' cannot be %s

DESCRIPTION

The collection class which you specified cannot be used for the operation you attempted. Some collection classes cannot be queried, indexed, or copied, so they cannnot be used as an argument to query_objects, index_collection, or copy_collection.

WHAT NEXT

Only use collections of this class as arguments to appropriate commands.

SEL-010 (warning) %s objects from '%s' were of the %scorrect class.

DESCRIPTION

A heterogeneous collection was passed to another command. This collection contained some objects that were of a class which is not accepted by the command. The message will indicate whether some objects or no objects were accepted by the command.

WHAT NEXT

Some commands continue to operate when only a subset of the patterns match. Other commands only perform their action when all patterns match something. So, verify that the command was applied to the objects which were expected.

SEL-011 (warning) Some objects (%s) could not be queried.

DESCRIPTION

A heterogeneous collection was passed into query_objects. This collection contained some objects that were of a class which cannot be the target of a query.

WHAT NEXT

There is no adverse affect of this situation.

SEL-012 (information) Iteration for collection %s was terminated because the collection was modified or deleted.

DESCRIPTION

Commands in the body of a **foreach_in_collection** can affect the collection which is currently in iteration. Some commands can cause objects to be removed from the collection, and others can cause the collection to be deleted. When such events occur, the iterator is modified and in some cases will terminate. This message advises you of that event.

For example:

foreach_in_collection itr [get_cells *] { remove_design [current_design] }
would cause the collection of cells to be deleted, and the iteration would be terminated.

WHAT NEXT

No action is required.

SEL-013 (error) Regular expression error: %s.

DESCRIPTION

While using a regular expression with a collection command, you entered an invalid regular expression. For example, use of the * (zero or more) or + (one or more) operators alone always yields the empty set; therefore, ".*" or ".+" would be appropriate. Other errors such as unmatched parens or invalid characters within square braces will also cause this error.

WHAT NEXT

Take action based on the error that occurred.

SEL-014 (error) At least one %scollection required for argument '%s'%s

DESCRIPTION

Some commands do not allow heterogeneous collections as arguments, whereas others allow them only in some contexts. Other commands require at least one collection as an argument. You entered a variation of a command which requires at least one collection (either homogeneous, or of either type) for the named argument.

WHAT NEXT

Consult the man page from the command which failed for further information.

SEL-015 (warning) Ignored all implicit elements in argument '%s'%s

DESCRIPTION

Many commands allow implicit searches for objects - an argument can be a list of collections or patterns which are searched for in a documented set of object classes. However, in some cases, it is not possible to determine any object classes in which to search for an implicit pattern. For example, attempting to add an implicit pattern to a heterogeneous collection with **add_to_collection** would cause this warning.

WHAT NEXT

Consult the man page from the command which failed for further information.

SEL-016 (error) Name patterns are not allowed in this argument context - the pattern %s will be skipped/ignored; use only collections in this argument context.

DESCRIPTION

Many commands allow implicit searches for objects - an argument can be a list of collections or name patterns which are searched for in a documented set of object classes. However, in some cases, when there is more than one object class to be searched, it is not allowed to include name patterns, and only collections should be included in such an argument.

WHAT NEXT

In the argument context in which this error happened, remove all name patterns from the offending argument, and make sure that only collections are included in the argument. You can typically use a "get" command to convert a name pattern to a collection.

SEQMERGE-1 (information) Merging duplicate register '%s' of '%s'.

DESCRIPTION

This information message pops up as you have enabled Register merging. Please note that **compile -verify** verification may fail as duplicate registers are removed.

You can do formalty verification by setting verification_merge_duplicated_registers variable to true.

```
fm_shell> set verification_merge_duplicated_registers true true
```

WHAT NEXT

You can disable Register merging using variable **fpga_enable_merge_register**.

SI-007 (warning) Cannot calculate noise immunity for library pin %s due to invalid CCS-noise information.

DESCRIPTION

You received this warning message because the indicated pin does not have valid CCS-noise information to calculate noise immunity.

You may have to set noise immunity on the pin manually by yourself. Otherwise, you may miss a violation if no slack value is available from the pin.

WHAT NEXT

Check if the characterization on this pin has been done properly.

SI-101 (error) Cannot find mask name for layer '%d'.

DESCRIPTION

SI command **report_signal_em** uses layer maskname to determine a constraint is setup for metal or via layers. If the maskname cannot be found, the constraint data in the design may be incomplete or corrupted.

WHAT NEXT

Check if the layer has been assigned a mask name.

SI-102 (error) Unable to retrieve signal EM's constant constraint object for layer '%s' from Milkyway database.

DESCRIPTION

SI command **report_signal_em** accesses Milkyway database to get EM constraints. This

error happens when the command cannot find the constant constraint data even though the constraint’s model type is labeled as ’constant’.

WHAT NEXT

Check if the current constraint on this layer has been defined properly.

SI-103 (error) Unable to retrieve signal EM’s table constraint object for layer ’%s’ from Milkyway database.

DESCRIPTION

SI command **report_signal_em** accesses Milkyway database to get EM constraints. This error happens when the command cannot find the constraint table data even though the constraint’s model type is labeled as ’EM table’.

WHAT NEXT

Check if the current constraint on this layer has been defined properly.

SI-104 (error) Unknown signal EM model type for layer ’%s’.

DESCRIPTION

SI command **report_signal_em** accesses Milkyway database to get EM constraints. This error happens when the command cannot recognize the type of model specified. We support ’constant’ and ’table’ type of constraint models.

WHAT NEXT

Check if the current constraint on this layer has been defined properly.

SI-105 (error) failed in the signal EM analysis of net ’%s’.

DESCRIPTION

SI command **report_signal_em** has failed on the net. This is a general error message when the signal EM analysis has failed for a net for any reason. Watch for error messages preceding to this.

WHAT NEXT

SI-106 (error) net '%s' is skipped in signal EM analysis because it doesn't have an RC network.

DESCRIPTION

SI command **report_signal_em** has skipped the analysis on the net because the RC network of the net is not found, or the size is zero.

WHAT NEXT

Check if the net is extracted or annotated correctly.

SI-107 (warning) Variable routing rule table cannot be initialized.

DESCRIPTION

Variable routing rule table cannot be initialized correctly in signal EM analysis. This table will be used to merge existing variable routing rules with those generated from signal EM. If a design doesn't have existing variable routing rules stored in the database, the table cannot be initialized.

WHAT NEXT

SI-108 (warning) Variable routing rules cannot be merged for net '%s'.

DESCRIPTION

SI command **report_signal_em** has failed merging the new variable routing rule with an existing one in the database.

WHAT NEXT

Check if the width of the net is adjustable. Also check the mask names of the metal

and contact layers in the design. For metals, it should start with 'poly' or 'metal'. For vias, it should start with 'cont' or 'polyCont'. This warning can be ignored if you have made sure there is no existing routing rule for the net.

SI-109 (error) Variable routing rules cannot be printed out for net '%s'.

DESCRIPTION

SI command **report_signal_em** has failed printing the new variable routing rule.

WHAT NEXT

Check if for the specified output file name, the file is writable.

SI-110 (warning) Location missing for a resistive edge (%g) of net '%s'.

DESCRIPTION

SI command **report_signal_em** uses location information to access EM constraints. Without the location information, signal EM cannot calculate relative average, RMS, or peak values.

WHAT NEXT

Check if the parasitics is loaded with command **read_parasitics**. The command doesn't load location information with parasitics in .spef format. Either extract RC with ICC internal extracor, or load parasitics in .sbpf format.

SI-111 (warning) physical via cannot be found for a via resistance edge between layers '%s' and '%s'.

DESCRIPTION

SI command **report_signal_em** needs physical via to process signal EM constraints properly. With the warning message, signal EM cannot correctly calculate relative average, RMS, or peak values.

WHAT NEXT

Check if the parasitics is reduced. Signal EM cannot process reduced RC netlist.

SI-112 (error) min delta delay is not enabled.

DESCRIPTION

The command **report_delay_calculation** with options -crosstalk and -min requires that min delta delay is enabled.

WHAT NEXT

Enable min delta delay with command set_si_options.

SI-113 (error) no net timing arc from pin to pin for report_noise_calculation.

DESCRIPTION

The command **report_noise_calculation** requires that the net arc exists for the pair of pins.

WHAT NEXT

Check the names of both pins and existence of net arc.

SI-114 (warning) Skipping net '%s' because it has too many connections.

.

DESCRIPTION

The SI computation is not done since net exceeds high fanout threshold .

WHAT NEXT

Change high fanout threshold or perform buffer insertion for this net.

SI-115 (error) delta delay is not enabled.

DESCRIPTION

The command **report_delay_calculation** with option -crosstalk requires that delta delay is enabled.

WHAT NEXT

Enable delta delay with command set_si_options.

SI-116 (error) the number of worst pins is less than 1.

DESCRIPTION

In the command **report_noise** with option -nworst_pins , the number equal to 1 or greater than 1 is accepted.

WHAT NEXT

Change the number of worst pins.

SI-117 (warning) ’reselect_slack_less_than’ option is ignored because ’timing_window’ is not on

.

DESCRIPTION

-reselect_slack_less_than option is only effective if timing window is enabled.

WHAT NEXT

enable timing window in ’set_si_options’ command.

SI-118 (information) Number of nets reselected for next iteration: %d.

DESCRIPTION

This information message advises you the number of nets that are reselected in the second timing and SI iteration. Normally the smaller the number is, the faster the second iteration will be. You can influence the reselection strategy using SI commands such as ’set_si_options’.

WHAT NEXT

This is an informational message only. No action is required.

SEE ALSO

set_si_options(2)

SI-119 (error) Pin ’%s’ is not found.

DESCRIPTION

The command **report_noise** cannot find the pin specified in the argument.

WHAT NEXT

Check the name of the pin and correct accordingly.

SI-120 (error) can’t set ’%s’.

DESCRIPTION

The variable has to be set larger than or equal to zero.

SI-121 (warning) can’t perform signal EM analysis on dangling

net ’%s’.

DESCRIPTION

This net doesn’t have any load pins and doesn’t need to be analyzed for EM.

SI-122 (warning) the following pins have no noise model specified in library.

DESCRIPTION

This warning message occurs when check_noise command finds pins without noise model specified in library. This may result in inaccurate results. It is very important that all pins in the design have correct noise information.

SEE ALSO

check_noise (2).

SI-130 (error) the option -exclude_all can not be used with other options.

DESCRIPTION

The commands **set_si_delay_analysis** and **remove_si_delay_analysis** with option -exclude_all , can not be used with other options.

WHAT NEXT

Remove other options.

SI-131 (warning) Reading the old effective aggressor model in hierarchical si.

DESCRIPTION

The old effective aggressor model is read in hierarchical si , which can affect the results.

WHAT NEXT

Re-generate the model with create_ilm.

SI-132 (warning) max_current_dc_avg for layer '%s' from Milkyway database is not supported for signal EM analysis and optimization.

DESCRIPTION

You received this warning message because there is 'max_current_dc_avg' type of EM constraints in your library. Currently signal EM doesn't support this type of constraints and they will be ignored.

WHAT NEXT

SI-133 (warning) different rail voltage found for pin and library pin.

DESCRIPTION

The command **set_noise_lib_pin** should not be used for pins and library pins with different rail voltages.

WHAT NEXT

Choose another library pin with proper rail voltage.

SI-134 (error) improper pin direction for report_noise_calculation.

DESCRIPTION

In the command **report_noise_calculation** input pin or output port should not be used for from pin and output pin or input port should not be used for to pin.

WHAT NEXT

Choose another pins for report_noise_calculation.

SI-135 (warning) Signal EM cannot find all requierd ICC licenses.

DESCRIPTION

SI Signal EM requires Galaxy-FP, Galaxy-PSYN and Galaxy-Power licenses.

If Galaxy-FP or Galaxy-PSYN is not found, SI commands **report_signal_em**, **report_signal_em_calculation**, **fix_signal_em** will not run.

If Galaxy-Power license is missing, switching activity will not be automatically propagated in SI commands **report_signal_em**, **report_signal_em_calculation**, **fix_signal_em**. All nets with missing switching activity use 1.0 as the default switching activity.

WHAT NEXT

use set_switching_activity or read_saif to set switching activities explicitly.

SI-136 (warning) This net is inside ILM cell or is connected to ILM cell.

DESCRIPTION

SI signal EM will analyze the nets in the top cell and also the nets on the boundary of ILM.

For nets on the boundary of ILM, which are either inside ILM cell or connected to ILM cell, the signal EM report will be given. However, the violations inside ILM cell cannot be fixed at the top level.

WHAT NEXT

Analyze and fix the signal EM violations inside ILM cell at block level.

SIF

SIF-1 (error) Parse error near symbol "%s

DESCRIPTION

WHAT NEXT

SIF-2 (error) Package "%s

DESCRIPTION

WHAT NEXT

SIF-3 (error) Illegal port direction %s

DESCRIPTION

WHAT NEXT

SIF-4 (error) Parameter "%s

DESCRIPTION

WHAT NEXT

SIF-5 (error) Variable "%s

DESCRIPTION

WHAT NEXT

SIF-6 (error) Block "%s

DESCRIPTION

WHAT NEXT

SIF-7 (error) Instance "%s

DESCRIPTION

WHAT NEXT

SIF-8 (error) Label "%s

DESCRIPTION

WHAT NEXT

SIF-9 (error) Port "%s

DESCRIPTION

WHAT NEXT

SIF-10 (error) Can’t exit block "%s

DESCRIPTION

WHAT NEXT

SIF-11 (error) For loop variable "%s

DESCRIPTION

WHAT NEXT

SIF-12 (error) Illegal block direction %s

DESCRIPTION

WHAT NEXT

SIF-13 (error) Right-hand-side must be attribute, type(), or

const() %s

DESCRIPTION

WHAT NEXT

SIF-14 (error) Symbol "%s

DESCRIPTION

WHAT NEXT

SIF-15 (error) Can’t get attribute "%s

DESCRIPTION

WHAT NEXT

SIF-16 (error) Can’t find attribute "%s" of "%s

DESCRIPTION

WHAT NEXT

SIF-17 (error) Port "%s

DESCRIPTION

WHAT NEXT

SIF-18 (error) Illegal character or symbol (%d) %s

DESCRIPTION

WHAT NEXT

SIF-19 (error) Attributes may not not be nested %s

DESCRIPTION

WHAT NEXT

SIF-20 (error) Malformed attribute specification %s

DESCRIPTION

WHAT NEXT

SIF-21 (error) Varargs too big in ’%s’ %s

DESCRIPTION

WHAT NEXT

SIF-22 (warning) Built-in function %s does not exist (ignored).

DESCRIPTION

WHAT NEXT

SIF-23 (warning) Inout port ’%s’ drives a scan-in pin. This

VHDL design cannot support parallel-loading.

DESCRIPTION

Parallel-loading input vectors require that values be forced onto scan-in nets. The scan-in nets are replaced by global signals. If the scan-in net is driven by an in/out port, however, the scan-in net must be driven directly by the in/out port, and a global signal cannot be inserted.

WHAT NEXT

Replace the in/out port with an input port or an output port, but do not drive scan-in nets directly with in/out ports.

SIF-24 (error) No primary input bidirectional control signal specified. No vectors generated.

DESCRIPTION

This design contains at least one bidirectional signal. But it contains no primary input signal for controlling the direction of the bidirectional signals. LSI scan rules require such signals. The error is specific to writing LSI CTV vectors.

WHAT NEXT

Before invoking the **create_test_patterns** command, use the **set_signal_type**, **test_bidir_control**, or **test_bidir_control_inverted** command to define all primary inputs controlling bidirectional signals. Then, reinvoke the **create_test_patterns** command, and regenerate the vectors.

SIF-25 (warning) Scan cell "%s" is within a hierarchical design module and references a non-unique instance in the design. This VHDL design cannot support parallel loading.

DESCRIPTION

Parallel-loading input vectors require the forcing of values onto scan-in nets. Therefore, these scan-in nets must be unique. However, the **current_design** has a level of hierarchy and the scan cells are referencing the same component. The scan cell must reference either a leaf-level library cell or a unique component.

WHAT NEXT

The scan cells must be uniquified or flattened to reference a leaf-level library cell.

SIF-26 (error) Port "%s port BEFORE invoking create_test_patterns. No vectors generated.

DESCRIPTION

LSI CTV interface specific requirement. Bidirectional control ports need to be specified using the set_signal_type command with either a test_bidir_control attribute or with a test_bidir_control_inverted attribute BEFORE generating vectors. Use the test_bidir_control attribute for those bidirectional control ports that need to be set to logic 1 to drive all bidirectionals to input mode. Use the test_bidir_control_inverted attribute for those bidirectional control ports that need to be set to logic 0 to drive all bidirectionals to input mode.

WHAT NEXT

Specify bidirectional control ports in the aforementioned manner before invoking create_test_patterns command.

SIF-27 (error) Apparent inconsistency between vector data base and netlist data base. Could not find ’%s’ in vector data base.

DESCRIPTION

A potential inconsistency exists between the vector database and the scan design database.

It’s possibly because a vector database file (.vdb file) has been used with an incompatible scan database file (.db file). Or perhaps it’s because there are errors in custom test protocol.

An example of an inconsistency is when the **write_test command** is invoked using an older version of a .vdb file. This inconsistency might occur when a user rerouted or altered the scan chain and did not invoke **create_test_patterns** before issuing the **write_test** command.

WHAT NEXT

Invoke **write_test** with compatible vector and scan database files. Try to run **check_test** and **create_test_patterns** before invoking **write_test** to generate vectors. If custom test protocol is used, also make sure that no error message is produced

when reading in the custom test protocol.

SIF-28 (error) Trying to specify parallel load for a protocol that is incapable of supporting it.

DESCRIPTION

Write_test is incapable of formating parallel load vectors for custom test protocols.

WHAT NEXT

Reissue the write_test command without the -parallel option, or use an infered or initialization protocol.

SIF-29 (warning) Maximum number of input timing definitions supported by the TSTL2 format exceeded. Subsequent specifications will be ignored.

DESCRIPTION

Toshiba/TSTL2 supports a maximum of six input timing definitions. Of these, you can allocate a maximum of four to clock waveforms. The number of clock waveforms defined for the current design exceeds the maximum value.

WHAT NEXT

Use the **report_test -port** command to report the clocks (and their waveforms) for the current design. Use the **create_test_clock** command (or modify your test protocol file) to define a maximum of four unique clock waveforms for the clocks in your design.

If you must change the clock waveforms, rerun **check_test** to verify that test design rule-checking passes and that the clock capture groups have not been modified due to the clock timing changes. If the clock capture groups have been modified, rerun **create_test_patterns** to avoid the possibility of bad vectors.

SIF-30 (warning) write_test_max_cycles value specified is too

small, value will be ignored

DESCRIPTION

The write_test_max_cycles value specified does not permit writing the next test pattern into a file, even at one pattern per file. To prevent infinite looping, write_test uses the default value of the write_test_max_cycles variable, which implies that the patterns will be written in a single file.

WHAT NEXT

Specify a value which is at least sufficient for a single pattern.

SIF-31 (warning) Cell '%s' does not have its set and observe pins specified

DESCRIPTION

You receive this message if **write_test** detects that the specified cell in your design does not have one or both of its set or observe pins specified. The LSI Logic interface requires each scan cell in the design to have set and observe pins specified.

When **write_test** detects unspecified set and observe pins, it assumes a default name of S2(A) for the set pin, and Q(Z) for the observe pin name.

WHAT NEXT

If the default names **write_test** has assumed for the set and observe pins of this cell are acceptable to you, no action is required on your part.

Otherwise, to change set and observe pin names, choose one of these alternatives:

1. Use the **set_attribute** command to specify the set and observe pin names for the specified cell, write out the .db file, and re-run **create_test_patterns** before re-running **write_test.**

For example, to specify the set and observe pin names for a FD1S scan cell in lsi_10k.db library to IN(A) and OUT(Z), use these commands:

```
dc_shell> set_attribute lsi_10k/FD1S set_pin "IN(A)" -type string
dc_shell> set_attribute lsi_10k/FD1S observe_pin "OUT(Z)" -type string
dc_shell> write lsi_10k.db -out scan_lsi_10k.db
```

2. Alternatively, you can change the set and observe pin names manually by editing the "PATTERN BPAT" and "SAVE" statements of the .SCL file.

SEE ALSO

create_test_patterns(2), set_attribute (2), **write_test** (2).

SIF-32 (warning) Scan chain '%s' does not have a scan %s port.

DESCRIPTION

This particular scan chain appears not to possess a scan input port or a scan output port.

WHAT NEXT

If this is not the expected configuration, you can use the report_test -scan_path and report_test -port commands to obtain more information about existing scan chains in the design. You may also want to check your (custom) test protocol as well as the outputs of check_test command.

SIF-33 (warning) Output net '%s' seems to be shorted to output net '%s', and they both drive the same scan data pin of scan cell '%s'.

DESCRIPTION

A scan data in port is driven by two nets that seems to be shorted together. This may cause simulation mismatches when simulating the parallel vectors produced.

WHAT NEXT

Perform check_test to identify shorted nets and remove them as needed.

SIF-34 (error) Can not find library needed by this design

DESCRIPTION

The link libraries needed to generate vectors for this design can not be found

WHAT NEXT

Check for errors in specifying the link_library. An example of this is a typo error

in issuing the command, e.g. issuing 'link_libray = ...' instead of 'link_library = ...'

SIF-35 (error) %s , scan package for parallel-loading is not created.

DESCRIPTION

Scan package for parallel loading is not created due to the aforementioned error(s)

WHAT NEXT

Run check_test first to identify scan path and other potential error(s)

SIF-36 (error) Could not find data base reference for scan cell '%s' .

DESCRIPTION

Inconsistent or missing data base in conjunction with the used vector data base, vectors generated may be bad due to missing scan chain structural information

WHAT NEXT

Parallel vector generation and fault simulation needs design information, this design has to be the exact design used to generate the .vdb file used as the input to the write-test command.

SIF-37 (error) Could not get bit value for primary port '%s' in test program. This port is present in the current design.

DESCRIPTION

This message indicates that the test program does not match the design. It does not contain value(s) for the aforementioned primary port. The design has probably been changed since the test program was written.

WHAT NEXT

If you need to use this test program, you must change the design back to what it was when the test program was written out. Otherwise, the test program cannot be used and a new one will have to be generated.

SIF-38 (error) Clock port '%s' can not be found in test protocol. This port is present in the current design.

DESCRIPTION

This message indicates that the test protocol does not match the design. The clock port in the design can not be obtained from the protocol.

WHAT NEXT

Check if current test program contains the correct protocol by writing out protocol file. If not, generate a new test program.

SIF-39 (error) Scan chain number '%d' can not be found. Possible test protocol problem.

DESCRIPTION

The test protocol used may not match the design. The indicated scan chain can not be found in the list of scan chains obtained from the protocol.

WHAT NEXT

Check if current test program contains the correct protocol by writing out protocol file. If not, generate a new test program.

SIF-40 (error) The vector file '%s' created by TestSim has been corrupted.

DESCRIPTION

Write_test uses the vector file written by the 'fault_simulate' command. This file appears to have been corrupted.

WHAT NEXT

Rerun the fault_simulate command to regenerate the vector file.

SIF-41 (error) Can not find scan %s port of scan chain number '%d'. Possible test protocol problem.

DESCRIPTION

The test protocol used may not match the design. The named scan port can not be found in the specified scan chain obtained from the protocol.

WHAT NEXT

Check if current test program contains the correct protocol by writing out protocol file. If not, generate a new test program.

SIF-42 (error) Can not find data for scan port named '%s' in test protocol. Possible test protocol problem.

DESCRIPTION

The test protocol used may not match the design. The named scan port can not be found in the specified scan chain obtained from the protocol.

WHAT NEXT

Check if current test program contains the correct protocol by writing out protocol file. If not, generate a new test program.

SIF-43 (error) Can not find vector index '%d' for port '%s' in test protocol. Possible test protocol problem.

DESCRIPTION

The test protocol used may not match the design. The named scan port can not be found in the specified scan chain obtained from the protocol.

WHAT NEXT

Check if current test program contains the correct protocol by writing out protocol file. If not, generate a new test program.

SIF-44 (error) Using bidirectional port '%s' as clock is currently unsupported

DESCRIPTION

DFT Compiler does not currently support using a bidirectional port as clock port. The named port will not be used as a clock port.

WHAT NEXT

Do not use bidirectional ports as clock ports

SIF-45 (error) Scan chains in this design are not parallel loadable because not all scan cells are both controllable and observable.

DESCRIPTION

There is a scan cell in the current design which is either controllable only or observable only. As a result, write_test cannot reliably generate a parallel loadable test program.

WHAT NEXT

Use a serial format or fix the test design rule violations on the scan chains. See the results of the check_test command.

SIF-46 (warning) Bidirectional ports switch mode after/during some clock pulses. You may get mismatches when simulating these vectors.

DESCRIPTION

In the test protocol for LSI formats, bidirectional ports must switch mode before

the active edge of the clock. The bidirectional delay value is specified using the environment variable 'test_default_bidir_delay'. write_test reports this warning if the leading edge time of any clock pulse is less than the bidirectional delay value.

WHAT NEXT

If there any bidirectional ports that switch mode after the active edge of the corresponding clock, change the value of the environment variable 'test_default_bidir_delay' and rerun check_test, create_test_patterns and write_test. Otherwise, you can ignore this message.

SIF-47 (error) Formatting of vectors in this format is not currently supported for designs with multibit cells.

DESCRIPTION

You receive this message if your design contains multibit cells and you have used the parallel Verilog, parallel VHDL, or LSI MDE vector format. DFT Compiler does not support these formats for multibit cells.

In parallel load formats, values are forced onto scan-in nets during the scan shift cycle. Multibit cells have internal scan chains, so scan-in nets of some bits are not accessible. Thus, DFT Compiler cannot support vectors in these formats.

WHAT NEXT

Please use serial vector formats instead.

SIF-48 (information) Design has multibit cells. Please make sure your WGL translator can correctly interpret the WGL output generated.

DESCRIPTION

You receive this message if your design contains multibit cells. This message is to remind you that in WGL files generated by DFT Compiler, the cell name corresponding to each bit is printed in the "scancell" statement. Thus, for a multibit cell, the cell name is printed once for each bit. Some WGL translators might incorrectly interpret the multiple appearances of the cell name.

WHAT NEXT

Work with the provider of your WGL translator to ensure that the WGL file is

translated correctly.

SIF-49 (warning) Some timing values are being rounded to integers. This may cause simulation mismatches.

DESCRIPTION

You receive this message if **write_test** finds a non-integer timing value in your design. If the variable **write_test_round_timing_values** is set to *true* (the default), **write_test** rounds all timing values to the nearest integer. This message informs you that some timing values in your design have been rounded to the nearest integer.

WHAT NEXT

If rounding timing values to integers does not cause simulation mismatches, no action is required on your part. However, if rounding timing values to integers **does** cause simulation mismatches, do one of the following:

1. If your test environment can accept noninteger timing, set the variable **write_test_round_timing_values** to **false**, and rerun **write_test**.

2. If your test environment cannot accept noninteger timing, reset the timing values using the environment variables **test_default_delay**, **test_default_bidir_delay**, and **test_output_strobe**; and the command **create_test_clock**. Rerun **check_test** and **create_test_patterns**, then rerun **write_test**.

SEE ALSO

check_test (2), **create_test_patterns** (2), **write_test** (2); **test_default_bidir_delay** (3), **test_default_delay** (3), **test_output_strobe** (3), **write_test_round_timing_values** (3).

SIF-50 (error) Multiple declaration of terminal '%s' in instance '%s'

DESCRIPTION

Multiple declarations of terminals of an instance are not allowed.

WHAT NEXT

Remove declarations of terminals such that there is only one declaration of the terminal.

SPEF-1 (warning) Missing or unknown library unit.

DESCRIPTION

There is no library unit available or the library unit is invalid (valid library units are ps, ns, or us). As default unit, ns is assumed.

WHAT NEXT

Check the library unit for correctness if ns is not the unit you want to use.

SPEF-2 (information) Path delimiter = %s.

DESCRIPTION

In the SPEF file, this character is used to separate elements in the path of an hierarchical object.

SPEF-3 (information) Pin delimiter = %s.

DESCRIPTION

In the SPEF file, this character is used to separate the path name from the pin name.

SPEF-4 (warning) Missing or unknown capacitance library unit.

DESCRIPTION

There is no cpacitance library unit available or the library unit is invalid. As default unit, pF is assumed.

WHAT NEXT

Check the library unit for correctness if pF is not the unit you want to use.

SPEF-5 (warning) Missing or unknown resistance library unit.

DESCRIPTION

There is no resistance library unit available or the library unit is invalid. As default unit, kOhm is assumed.

WHAT NEXT

Check the library unit for correctness if kOhm is not the unit you want to use.

SPEF-6 (warning) Failed to lookup annotated delay between '%s' and '%s'.

DESCRIPTION

This error points to an iconsistency of the timing data structures. There is supposed to be a backannotated delay between the two pins, but the attempt to read the delay fails. Under normal conditions, this error should not occur.

WHAT NEXT

Try to remove all backannotated delays with **remove_annotated_delays** and execute **read_parasitics** again.

SPEF-7 (warning) Failed to lookup elmore node for '%s'.

DESCRIPTION

The backannotation algorithm assumes that there is already an elmore node for the specified pin, but it cannot be found. This error is usually caused by inconsistent SPEF files. I.e., this error can happen if there is a pin mentionend in the *RES section of the SPEF file, but it isn't mentioned in the *CAP section.

WHAT NEXT

Check your SPEF file and make sure that all pins occuring in the *RES section also occur in the *CAP section. Also make sure that all pins occuring in the *CAP section also occur in the *RES section.

SPEF-8 (warning) Uncomplete RC annotation between '%s' and '%s'.

DESCRIPTION

The backannotation algorithm has detected a gap in the RC tree. This is most likely caused by an SPEF file containing incomplete parasitic information. However, this error should only occur if 'automatic tree completion' is switched off. By default, incomplete RC trees are automatically expanded and all gaps resulting from incomplete parasitic information are automatically bridged.

WHAT NEXT

Check if the tree completion algorithm has been disabled and check your SPEF file for inconsistencies.

SPEF-9 (warning) Inconsistent backannoted data detected.

DESCRIPTION

The **read_parasitics** command computes a single delay value for each pin pair. In the backannotation phase, the max rise delay, max fall delay, min rise delay, and min fall delay are all set to this single value. This error message is printed if a pin is encountered that doesn't contain the same delay value for each delay type. This error message may occur if a different command than **read_parasitics** has been used to backannotate delays.

WHAT NEXT

Remove all backannotated data by executing **remove_annotated_delays** before executing **read_parasitics**.

SPEF-10 (information) Library unit = %f %s.

DESCRIPTION

This message shows the unit that has been found in the mail library. All values that are read in from an parasitics file will be scaled to match the unit given in the main library. If the library base unit is missing or unknown, a warning message is issued and default units are assumed. The default units are ns for delays, pF for capacitances, and Ohm for resistances.

SPEF-11 (information) Derived delay scale factor = %f.

DESCRIPTION

The delay scale factor expresses the main library unit in terms of 1ns. More precisely, the value to be backannotated is calculated by (delay in ns) * scale_factor = value to be backannotated.

SPEF-12 (information) Derived capacitance scale factor = %f.

DESCRIPTION

The scale factor expresses the main library unit for capacitances in terms of 1pF. More precisely, the value to be backannotated is calculated by (capacitance in pF) * scale_factor = value to be backannotated.

SPEF-13 (information) Derived resistance scale factor = %f.

DESCRIPTION

The scale factor expresses the main library unit for resistances in terms of 1 Ohm. More precisely, the value to be backannotated is calculated by (capacitance in Ohm) * scale_factor = value to be backannotated.

SPEF-14 (warning) Pins '%s' and '%s' are not on the same net.

DESCRIPTION

This warning message indicates that the loaded SPEF file is inconsitent with the logical design in memory. The two involved pins belong to the same parasitic network given by the SPEF file, but do not belong to the same net in the logical design. In other words, the SPEF topology and the topology of the design in memory are out of sync. The warning message strongly indicates that the logical design has been changed after the SPEF file has been generated.

WHAT NEXT

Regenerate the SPEF data with the current logical design.

SPEF-15 (error) User specified path-prefix '%s' does not exist.

DESCRIPTION

This warning message indicates that the user-specified path ("-path" option) does not exist. The argument to the "-path" option must be a relative path from the current design to a hierarchical design for which the parasitics file has been created.

WHAT NEXT

Check the "-path" argument for typos. Check if the SPEF file and the current design in memory fit together.

SPEF-16 (error) User specified strip-path '%s' does not exist.

DESCRIPTION

This warning message indicates that the user-specified strip-path ("-strip_path" option) is incorrect. The argument to the "-strip_path" option must be a path prefix. When an SPEF file is read, this prefix is stripped off from the name of each read object. If the name of an object in the SPEF file does not start with the strip-path prefix, the name remains unchanged. This message is issued if no object in the SPEF file has a name starting with the specified prefix. This means that the strip path option had no effect.

WHAT NEXT

Check the "-strip_path" argument for typos. Check if the SPEF file and the current design in memory fit together.

SPEF-17 (error) No DC design in memory.

DESCRIPTION

There is no DC design in memory for the current design. This error occurs if there is no design currently loaded or if a design is loaded, but you haven't executed **read_parasitics** prior to this command.

WHAT NEXT

Make sure that a design has been loaded and you have backannotated parasitic information with the **read_parasitics** command.

SPEF-18 (warning) Cannot associate pins of net '%s' with pins of the current design.

DESCRIPTION

This warning message is printed if none of the pin-names read from the parasitics file can be associated with any pin of the current design. Usually, this is a strong indication that the parasitics file and the design in memory do not match.

WHAT NEXT

Take either of the following actions:

- Check if the design in memory and the specified parasitics file belong together.
- Check if the current design is set correctly.
- Check the value of parameter **-path** is applicable.
- Check the value of parameter **-strip_path** is applicable.

SEE ALSO

read_parasitics (2), **SPEF-15** (3), **SPEF-16** (3).

SPEF-19 (warning) Net '%s' contains an interconnection loop. The delays and transition times computed for this net may be inaccurate.

DESCRIPTION

This warning message is printed if the SPEF file contains an RC tree with interconnection loops for the specified net. Depending on the selected delay calculator, loops may be substituted internally by a corresponding spanning tree which can influence the accuracy of the computed delays and transition times.

This message is printed out only for the first net containg interconnection loops. Please refer to the SPEF-21 warning message for the total number of nets having interconnection loops.

WHAT NEXT

Take either of the following actions:

- Generate a parasitics file without interconnection loops.
- Select the Arnoldi delay calculator.

SEE ALSO

read_parasitics (2).

SPEF-21 (warning) '%d' nets with interconnection loops have been read.

DESCRIPTION

This warning message indicates that the currently read SPEF file contains RC trees with interconnection loops for the specified number of nets. For these nets, the computed delay and transition times may be inaccurate, depending on the selected delay calculator. If the Elmore delay model is selected, loops are substituted internally by a corresponding spanning tree that can influence the accuracy of the computed delays and transition times.

WHAT NEXT

This is a warning message only. No action is required on your part. However, to recompute more accurate delay and transition times, you can take one of the following actions and then run the command again.

- Generate a parasitics file without interconnection loops
- Select the Arnoldi delay calculator.

SEE ALSO

read_parasitics (2).

SPEF-23 (information) Output limit reached for message '%s'.

DESCRIPTION

This information message occurs when the number of printed messages for the specified message is exceeded. The number of printed messages is restricted for some warning and error messages, in order to prevent unlimited growth of the printed output or log files.

WHAT NEXT

This is an informational message only. No action is required on your part.

Further occurrences of this message are suppressed.

SEE ALSO

SPEF-22 (n).

SPEF-24 (information) Message '%s' occurred '%d' times.

DESCRIPTION

This information message occurs when the number of printed messages exceeds the number of messages allowed. The messages shows the total number of times the error or warning condition appears.

Some warning and error messages restrict the number of printed messages allowed in order to avoid unlimited growth of the printed output or log files.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

SPEF-21 (n).

SPFP-001 (error) Cannot open file '%s'.

DESCRIPTION

The named parasitics file cannot be opened.

WHAT NEXT

Validate that the file name is correct.

SPFP-002 (error) Could not determine the format of parasitics file:
'%s'

DESCRIPTION

The named parasitics file was opened, but the format of the file (DSPF, RSPF, SPEF) could not be determined.

WHAT NEXT

Validate that the file is a properly formatted parasitics file in one of the supported formats.

SPFP-010 (error) %s syntax error: %s
at line %d near '%s' in file '%s'

DESCRIPTION

A syntax error was found while reading the indicated type of parasitics file. A nearby line is given to help you isolate the problem.

WHAT NEXT

This message covers a wide variety of syntax errors. Review the line number reported in the message and determine if the writer of the parasitics file has introduced a syntax error.

SPFP-011 (error) Unknown %s construct '%s' at line %d in file '%s'

DESCRIPTION

An unexpected or unknown construct was found while reading a parasitics file of the indicated format, This will often be followed by a general syntax error, **PARA-010**.

WHAT NEXT

Review the line number reported in the message and determine if the writer of the parasitics file has introduced an unknown construct.

SPFP-012 (warning) Missing '*|GROUND_NET' statement in SPF file '%s' Using 'vss', 'VSS', 'gnd' and 'GND'

DESCRIPTION

The GROUND_NET statement is missing from the named DSPF or RSPF file.

WHAT NEXT

This is just a warning to indicate that default values will be used.

SPFP-013 (warning) name DELIMITER and hierarchy DIVIDER are the same! Some objects may not be found, and performance may be affected.

DESCRIPTION

The hierarchy divider and pin delimiter in the named parasitics (SPEF, DSPF, RSPF) file are the same. This may not be completely supported. Some net or pin objects may not be found, and performance may be adversely affected.

WHAT NEXT

Modify your use of the application which generated the parasitics file and

regenerate it using different (or default) DELIMITER and DIVIDER. Synopsys strongly recommends that for the best performance, you should use different characters for the hierarchy delimiter and name delimiter.

SPFP-014 (warning) %s value %g exceeds user-defined threshold at line %d in file '%s'.

DESCRIPTION

You receive this message if the parasitics file contains a capacitance value (in picofarads) or a resistance value (in ohms) that exceeds user-defined thresholds, as specified by the **parasitics_cap_warning_threshold** and **parasitics_res_warning_threshold** variables. This warning is intended to assist you in detecting large, unexpected values generated by other applications. The specified value is still used by the application.

WHAT NEXT

This is a warning message only; no action on your part is required. However, you can change the thresholds by setting the **parasitics_cap_warning_threshold** and **parasitics_res_warning_threshold** variables to different values, or to 0.0 (the default) to suppress the generation of this message. For more information, see the manual pages of these variables.

SEE ALSO

parasitics_cap_warning_threshold (3), **parasitics_res_warning_threshold** (3).

SPFP-100 (error) Expected %skeyword %s but found '%s' at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a syntax error where a specific keyword was expected (for example, *D_NET), but something else was found. The file name and line number are given so you can isolate the problem.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-101 (error) Invalid %s '%s'%s at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a syntax or semantic error in a number of different constructs. The message will indicate the type of construct and what part of it is invalid. Some examples include:

- You specified a DIVIDER, DELIMITER, or BUS_DELIMITER which is outside of the allowed set of values for the construct
- Any of the header unit constructs has an invalid number or multiplier string.
- A port or D_NET connectivity entry has an invalid direction.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-102 (error) NAME_MAP syntax error at '%s' at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a syntax or semantic error in an entry in the NAME_MAP section of the file.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-103 (error) %s requires %d or more %s's

at line %d in file '%s'.

DESCRIPTION

Many sections of the SPEF file require one or more sub sections of a specific type. You receive this message if the SPEF file violates that semantic. Some examples include:

- The *CAP section of a D_NET, if specified, requires one or more capacitor elements.
- The *RES section of a D_NET, if specified, requires one or more resistor elements.
- The connectivity section of a D_NET requires one or more *P or *I sub sections.
- The *POWER_NETS and *GROUND_NETS sections, if specified, require one or more net names.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-104 (error) %s requires %s at line %d in file '%s'.

DESCRIPTION

Some sections of the SPEF file require a specific sequence of sub sections. You receive this message if the SPEF file violates that semantic. Generally, this message is reserved for some rarely used sections of the file, like *DEFINE.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-105 (error) Invalid node name '%s'

at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a syntax or semantic error in a node name, which is used in several places in the *RES and *CAP sections. The specific node name which is in error is shown in the message. A node name is either a port name, an instance pin name (an instance name or name map id, followed by the pin delimiter, followed by a pin name or name map id), or an internal node name (a net name, followed by the pin delimiter, followed by a positive integer).
The SPEF specification details the various possible forms for a node name.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-106 (error) Strict SPEF syntax error: invalid %s %s at line %d in file '%s'.

DESCRIPTION

Historically, there are a number of SPEF writers which write illegal SPEF. For backward compatibility with existing questionable SPEF files, the parser allows a number of forms which are strictly illegal. If the parser is in *strict* mode, you will receive this error when one of these strict-SPEF rules is violated.

WHAT NEXT

The first thing to try is to turn off strict mode. Or, you can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-107 (error) Expected %s but found '%s' at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a construct in the wrong place or out of order. Some examples include:

• The *D_NET section expects a certain series of optional sub sections. A SPEF keyword which is not a valid *D_NET sub section was found where a *D_NET sub section was expected.

• The *S connectivity attribute has some optional thresholds which must be positive fractions (between 0 and 1). The value found is not a positive fraction.

• Several sections of the SPEF file require a positive integer, and that was not found.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-108 (error) Invalid value '%s' at line %d in file '%s'.

DESCRIPTION

Many sections of the SPEF file use values, or triplets of values. You receive this message if the SPEF file has a syntax error in a value. Values are used in the *L and *S connectivity attributes, total capacitance of a D_NET or R_NET, capacitances, resistances, poles and residues, and so on.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-109 (error) Syntax error in complex number: '%s %s%s%s%s%s' at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a syntax error in a complex number. Complex numbers are used in the specification of poles and residues. They can be specified as (r i), or as a triplet such as (r i):(r2 i2):(r3 i3). The message will

indicate the specific problem number.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-110 (error) Syntax error near '%s' at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a syntax error not covered by any of the other syntax error messages. The token in question, as well as the file name and line number, will be given in the message.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-111 (error) Undefined name map index *%d referenced at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file finds a syntactically correct name map reference, such as *2379, but no such entry was ever defined in the NAME_MAP section.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-112 (error) Non-terminated comment starting at line %d

of '%s'

DESCRIPTION

You receive this message if the SPEF file contains a multi-line comment, which begins with /*, but does not end. This message is intended to help you find the line where the non-terminated comment starts.

WHAT NEXT

You can try to correct this error manually by terminating or removing the comment. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-113 (error) Premature end-of-file reading '%s'.

DESCRIPTION

You receive this message if the SPEF file ends unexpectedly, for example, in the middle of parsing required header sections, or before any D_NET or R_NET sections were found. A missing double quote in the header section can cause this error.

WHAT NEXT

You might be able to correct this error manually if this is caused by missing header sub-sections, or by a missing closing quote in one of the header sub sections. But, generally, it will be difficult to isolate the problem in a large file.

SPFP-114 (information) Ignored unsupported %s section starting at line %d of '%s'

DESCRIPTION

You receive this informational message if the SPEF file contains a construct which is being ignored, such as D_PNET and R_PNET.

WHAT NEXT

No action is necessary.

SPFP-115 (error) BUS_DELIMITER cannot be the same as %s at line %d in '%s'.

DESCRIPTION

You receive this message if the BUS_DELIMITER is found to be the same as either the DIVIDER or the DELIMITER. SPEF does not allow this combination.

WHAT NEXT

The SPEF file will almost certainly need to be regenerated.

SPFP-116 (error) Semantic error near '%s': %s at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file reader has found a semantic error. The token in question, the specific problem, and the file name and line number will be given in the message.

WHAT NEXT

You can try to correct the error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the problem corrected.

SPFP-117 (error) SENSITIVITY syntax error at '%s' at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a syntax or semantic error in an entry in the SENSITIVITY section of the file.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-118 (error) Sensitivity factor syntax error at '%s' at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has an invalid value for a sensitivity factor. A sensitivity factor is supposed to be a floating point number.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-119 (error) Invalid parameter ID '%d' value in sensitivity at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has an invalid value for a variation parameter ID in the sensitivity section. The variation parameters are defined in the *VARIATION_PARAMETERS section and are supposed to be within the values defined in this section. This error indicates that the current parameter ID is outside the valid range.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-120 (error) Invalid parameter types for process parameter '%s' at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has an invalid type of process variation parameter. The variation parameters are defined in the *VARIATION_PARAMETERS section and allowed values are 'D', 'N' or 'X' type of process variation parameters. This indication implies whether the parameter affects capacitance, resistance and inductance in numerator (for 'N'), denominator (for 'D') or does not affect resistance (for 'X').

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-121 (error) Syntax error at line %d in file '%s'. Cannot define process variations after temperature variations.

DESCRIPTION

You receive this message if the SPEF file has temperature variations followed by process variations. It is expected that the file contains process variation parameters followed by temperature variations. The variation parameters are defined in the *VARIATION_PARAMETERS section.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-122 (warning) Invalid sensitivity for capacitance at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has sensitivities for ground or coupling capacitances with respect to temperature variations or 'N' parameters to inform you that these sensitivities are illegal.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-123 (error) Syntax error at line %d in file '%s'. Expected

to see keyword CRT2.

DESCRIPTION

You receive this message if the SPEF file has syntax errors in the definition of temperature variations. The variation parameters are defined in the *VARIATION_PARAMETERS section.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-124 (error) Illegal name map index *%d referenced at line '%d' in file '%s'.

DESCRIPTION

You receive this message if the SPEF file finds a syntactically illegal name map reference, such as *-1. Such lines will be ignored.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPG

SPG-001 (error) The design does not have a user-specified core area.

DESCRIPTION

This error message occurs because the core area is not specified for this design. The floorplan information is not automatically generated in SPG.

WHAT NEXT

To run this design in SPG mode, use the **extract_physical_constraints** command and ensure that the placement area is specified.

SEE ALSO

extract_physical_constraints(2)
report_physical_constraints(2)

SPG-002 (error) The port %s does not have a user-specified location.

DESCRIPTION

This error message occurs when the port does not have a user-specified location.

WHAT NEXT

To run this design in SPG mode, use the **extract_physical_constraints** command and ensure that the placement area is specified.

SEE ALSO

extract_physical_constraints(2)
report_physical_constraints(2)

SPG-003 (error) The %s %s does not have a user-specified

location.

DESCRIPTION

This error message occurs because the macro does not have a user-specified location. The **compile_ultra -spg** command does not generate macro locations for unplaced macros.

WHAT NEXT

To run this design in SPG mode, use the **extract_physical_constraints** command and ensure that the placement area is specified.

SEE ALSO

extract_physical_constraints(2)
report_physical_constraints(2)

SPG-004 (error) The cell %s is a black box. Black boxes are not supported in ’compile_ultra -spg’.

DESCRIPTION

This error message occurs because the black box cells are not allowed in the SPG flow.

WHAT NEXT

To run this design in SPG mode, update the target libraries and the physical libraries to include the specified cell.

SEE ALSO

extract_physical_constraints(2)
report_physical_constraints(2)

SPG-005 (error) The ILM %s is a DCT ILM. DCT ILMs are not supported in ’compile_ultra -spg’.

DESCRIPTION

This error message occurs because Design Compiler topographical ILMs are not allowed

in the SPG flow. Only IC Compiler ILMs are allowed in the SPG flow.

WHAT NEXT

To run this design in SPG mode, create an IC Compiler ILM for this ILM or replace the ILM with the complete model.

SEE ALSO

extract_physical_constraints(2)
report_physical_constraints(2)

SPG-006 (error) The ILM %s does not have a user-specified location.

DESCRIPTION

This error message occurs because the unplaced ILMs are not allowed in the SPG flow. You must provide a location for this ILM.

WHAT NEXT

To run this design in SPG mode, place the ILM.

SEE ALSO

extract_physical_constraints(2)
report_physical_constraints(2)

SPG-007 (error) DCT physical blocks are not supported in 'compile_ultra -spg' %s.

DESCRIPTION

This error message occurs because the specified physical block is not allowed in the SPG flow.

WHAT NEXT

To run this design in SPG mode, remove the specified physical block.

SEE ALSO

extract_physical_constraints(2)
report_physical_constraints(2)

SPG-008 (error) The design was optimized using compile_ultra -spg. Cannot update the physical constraints using the %s command.

DESCRIPTION

This error message occurs when you update the physical constraints for the design. You must provide this information before running the **compile_ultra -spg** command.

WHAT NEXT

Apply this constraint before running **compile_ultra -spg** for the first time.

SEE ALSO

extract_physical_constraints(2)
report_physical_constraints(2)

SPG-009 (error) The design was optimized using compile_ultra -spg. Cannot update the physical constraints.

DESCRIPTION

This error message occurs when you update the physical constraints for the design. You must provide this information before running the **compile_ultra -spg** command.

WHAT NEXT

Apply this constraint before running **compile_ultra -spg** for the first time.

SEE ALSO

extract_physical_constraints(2)
report_physical_constraints(2)

SPG-100 (Error) RTL was not optimized using "compile_ultra -

spg" in Design Compiler Graphical.

DESCRIPTION

You receive this error message because you are using -spg option with the command and it is required that you synthesise this design using -spg in DC Topographical.

WHAT NEXT

You could either not use -spg option or synthesise this design using DC Topographical.

SEE ALSO

place_opt (2)

SPG-101 (Error) Design does not have Physical guidance Information.

DESCRIPTION

You receive this error message because you are using -spg option with this command. It is required that you use -spg option when you use compile_ultra or compile_ultra -incr in DC Topographical.

WHAT NEXT

You could either not use -spg option or synthesise this design using DC Topographical with -spg option.

SEE ALSO

place_opt (2)

SPG-102 (Error) Failed to restore DC Graphical Physical guidance Information, please remove -spg option.

DESCRIPTION

You receive this error message because you are using -spg option with this command. This command is unable to restore all placement information passed on from DC

Topographical.

WHAT NEXT

You can remove -spg option from this command and run again.

SEE ALSO

place_opt (2)

SPG-103 (Error) Design RTL was optimized using "compile_ultra -spg", please use -spg in place_opt.

DESCRIPTION

You receive this error message because you are not using -spg option with this command. It is required that you use -spg option when you use compile_ultra or compile_ultra -incr in DC Topographical.

WHAT NEXT

You could either not use -spg option or synthesise this design using DC Topographical with -spg option.

SEE ALSO

place_opt (2)

SPG-104 (Error) Cell ’%s’ does not have placement information.

DESCRIPTION

You receive this error message because you are using -spg option with this command. This cell does not have any placement, fixed on spg information from design compiler compile_ultra

WHAT NEXT

You could either not use -spg option or synthesise this design using DC Topographical with -spg option.

SEE ALSO

place_opt (2)

SPG-105 (Warning) Cell '%s' has both DC Graphical physical guidance and fixed location.

DESCRIPTION

You receive this warning message because you are using -spg option with this command. This cell does not have any placement, fixed on spg information from design compiler compile_ultra.

This cell has both the spg placement and fixed location, we will restore only the spg location.

WHAT NEXT

You could either not use -spg option or synthesise this design using DC Topographical with -spg option.

SEE ALSO

place_opt (2)

SPG-106 (Warning) Cell '%s' has both DC Graphical physical guidance and placed location.

DESCRIPTION

You receive this error message because you are using -spg option with this command. This cell does not have any placement, placed on spg information from design compiler compile_ultra.

This cell has both the spg placement and placed location, we will restore the spg location for this cell.

WHAT NEXT

You could either not use -spg option or synthesise this design using DC Topographical with -spg option.

SEE ALSO

place_opt (2)

SPG-120 (Warning) Number of %s provided in DC Graphical %d does not match ICC %d.

DESCRIPTION

You receive this warning message because you are using -spg option with this command. This commands checks to see if the floorplan informaiton provided in DCT matches the one provided in ICC. If they do not then there could be correlatio issues.

WHAT NEXT

You should check to see if the floorplan input matches between ICC and DCT. You can make necessary changes that you floorplan such that this constraint is same in both DCT and ICC.

SEE ALSO

place_opt (2)

SPG-121 (Warning) %s information does not match.

DESCRIPTION

You receive this warning message because you are using -spg option with this command. This commands checks to see if the floorplan informaiton provided in DCT matches the one provided in ICC. If they do not then there could be correlatio issues. This will compare the signature created in DCT with the signature created in ICC.

WHAT NEXT

You should check to see if the floorplan input matches between ICC and DCT. You can make necessary changes that you floorplan such that this constraint is same in both DCT and ICC.

SEE ALSO

place_opt (2)

SPG-122 (Warning) Could not find comparison data for %s.

DESCRIPTION

You receive this warning message because you are using -spg option with this command. This commands checks to see if the floorplan informaiton provided in DCT matches the one provided in ICC. This command is unable to find the comparision data for the DCT run.

WHAT NEXT

This is a rare issue, please ensure that you are using recommended versions of DC Topographical.

SEE ALSO

place_opt (2)

SR-1 (error) Can’t find a module to implement operation ’%s’ in process %s.

DESCRIPTION

The **compile** command could not find a module to implement the specified operation. Either the module was not present in any of the synthetic libraries in the **synthetic_library** variable, or the module might be present but disabled with the **set_dont_use command.**

WHAT NEXT

First, examine the contents of the **synthetic_library** variable and ensure that the required module is present; extend the synthetic library if necessary. Next, check your **set_dont_use** statements, and remove any that prevent the required module from being used. Then reexecute the command.

SR-2 (error) Can’t implement all operations of resource(s) ’%s’ on any available module in process %s.

DESCRIPTION

The **compile** command could not find a module to implement some operations in the specified resource. Either some modules were not present in any of the synthetic libraries in the **synthetic_library** variable, or the modules might be present but disabled with the **set_dont_use** command.

WHAT NEXT

First, examine the contents of the **synthetic_library** variable and ensure that the required modules are present; extend the synthetic library if necessary. Next, check your **set_dont_use** statements, and remove any that prevent the required modules from being used. Then reexecute the command.

SR-3 (error) Can’t find implementation ’%s’ for module ’%s’

%s

DESCRIPTION

The given implementation cannot be found in your synthetic libraries. Either the name is misspelled or the implementation is declared in a synthetic library which is not included in "synthetic_library". Another possibility is that the USE of the implementation in your design cannot be determined, and therefore the proper license was not checked out at the right time. Check the contained_operators/module/ implementations attribute for modules that use this part in the .sl file.

WHAT NEXT

SR-4 (error) Data class '%s' is not recognized.

DESCRIPTION

You receive this message if you use an illegal data class value in the synthetic library. Allowed values are *signed* and *unsigned*.

WHAT NEXT

Check your synthetic library source code, and ensure that you use either *signed* or *unsigned* as the data class value. Then reexecute the command.

SR-5 (error) Can't find the %s '%s' in synthetic_library. Resource sharing has been aborted %s

DESCRIPTION

The set of Synthetic libraries specified by the synthetic_library variable must contain the specified part.

WHAT NEXT

SR-7 (error) Cannot find instantiated synthetic module '%s'

in the libraries listed in 'synthetic_library'.

DESCRIPTION

The given synthetic module was identified because it was contained in a synthetic library listed in the *link_library* variable. You must also list the synthetic library in the *synthetic_library* variable to generate an implementation for the module.

WHAT NEXT

List the synthetic libraries from your *link_library* variable in your *synthetic_library* variable.

SR-8 (error) The %s is shorted to the %s. Resource sharing does not support operations that are shorted together.

DESCRIPTION

This error is most likely caused by a bug in the user's source code. An example that would trigger this error is:

```
C <= A + B; C <= A - B;
```

Note that the signal must be driven in two separate blocks and/or concurrent statements.

WHAT NEXT

The most likely fix is to find the two outputs that are shorted together, and to remove the short. However, if the shorted outputs are really what the user wants, then the resource sharing code can be fooled by instantiating a buffer after one of the operations so that the operations don't appear to be shorted together.

SR-9 (warning) The operation '%s' has been deleted because it was not needed.

DESCRIPTION

In general, redundant operations are removed when elaborating the HDL design. However, some operations are not necessarily deleted then because it takes logic

synthesis to run to determine that the operations are redundant.

Consider the following VHDL fragment:

```
process ( in1, in2 )
    constant table : bit_vector( 3 downto 0 ) := "0000";
    variable tmp : integer range 0 to 3;
begin
    tmp := in1 + in2;
    out1 <= table( tmp );
end process;
```

The adder assigned to "tmp" is actually redundant since all values of the array "table" are the same. As a result, the value of "tmp" does not affect the output "out1" which will always be zero. During logic synthesis, the adder assigned to "tmp" will be deleted, and this warning will be issued.

WHAT NEXT

Check the deleted operation and make sure that it is okay for this operation to be deleted. If not, check to logic to see if you can determine why the operation is being deleted.

SR-10 (Information) Reporting of resource costs is no longer supported.

DESCRIPTION

This SII interpreter command has been discontinued.

WHAT NEXT

No action on your part is required; there is no workaround. Normally, customers do not see this message.

SR-11 (error) Net %s has multiple drivers. High Level Optimization does not support synthetic operators/modules

whose outputs drive the same net.

DESCRIPTION

This error is most likely caused by a bug in the user's source code. An example that would trigger this error is:

```
DW01_csa #(16) DW01_csa_1 (.a(a_1), .b(b_1), .c(c_1), .ci(1'b0), .carry(carry_1),
.sum(sum_1), .co(co)); DW01_csa #(16) DW01_csa_2 (.a(a_2), .b(b_2), .c(c_2),
.ci(1'b0), .carry(carry_2), .sum(sum_2), .co(co));
```

WHAT NEXT

The most likely fix is to find the multiple driver net and fix it.

SSH

SSH-1 (error) Unknown host ’%s’.

DESCRIPTION

WHAT NEXT

SSH-2 (error) Can’t execute program ’%s’.

DESCRIPTION

WHAT NEXT

SSH-3 (error) File ’%s’: Permission Denied.

DESCRIPTION

WHAT NEXT

SSH-4 (error) Could not connect to %s subshell

DESCRIPTION

WHAT NEXT

SSH-5 (information) Abnormal Exit -- program %s function %s

host %s

DESCRIPTION

WHAT NEXT

SSH-6 (error) ’%s’ is not a valid feature name for ’%s’.

DESCRIPTION

The given feature name cannot be checked out for the given tool. This can happen if the feature name doesn’t exist or you are not authorized to use that feature.

WHAT NEXT

Choose another feature name. Check the reference manual of the tool in question for a list of valid feature names.

STIL-101 (error) %s

DESCRIPTION

This error is generated when you try to read a STIL file with syntax error. The syntax error happens at the next symbol.

WHAT NEXT

Fix the syntax error and read in the file again.

STIL-102 (error) %s block is not a top level STIL block.

DESCRIPTION

This error is generated when you try to read a STIL file without any top level STIL blocks. At least one top level STIL block (except STIL & Header) is required for a valid STIL file.

WHAT NEXT

modify the STIL file to make it valid.

STIL-103 (error) Can’t read version %s of STIL.

DESCRIPTION

This error is generated when the STIL parser can not parse the STIL version mentioned. It is usually caused by reading in a ctldb file that was generated by early version of dft compiler.

WHAT NEXT

User have to regenerate the ctldb file with current version of dft compiler.

STIL-104 (information) Using CTL parser version %s on a

version %s model.

DESCRIPTION

The model’s CTL version is no longer supported. This message informs you that the tool will attempt to read the model using a parser designed for a later version of CTL. Most constructs in newer versions are backwards compatible. In all likelihood, the read will be successful.

WHAT NEXT

Pay attention to the next messages. They will inform you whether the read was successful or not.

STIL-301 (error) Illegal STIL string: %s.

DESCRIPTION

This error is generated when the mentioned string in is illegal according to STIL syntax.

WHAT NEXT

Check with STIL syntax, modify the string to make it legal.

STIL-302 (error) Illegal STIL identifier: %s.

DESCRIPTION

This error is generated when the mentioned identifier is illegal according to STIL syntax.

WHAT NEXT

Check with STIL syntax and modify it to legal identifier.

STIL-303 (error) Cannot find PatternExec with name %s

DESCRIPTION

This error is generated when the PatternExec with the specified name is not found in the STIL file.

WHAT NEXT

Specify another PatternExec name or modify the existing PatternExec name in STIL file.

STIL-304 (error) Signal %s already defined.

DESCRIPTION

This error is generated when the concerned signal is previously defined in the STIL file. Redefinition of signal is not allowed in STIL file.

WHAT NEXT

Remove the one of the dual signal definitions.

STIL-305 (error) Variable %s redefined.

DESCRIPTION

This error is generated when the concerned variable is previously defined in the same domain. Redefinition of variable is not allowed in the same domain.

WHAT NEXT

Remove one of the dual variable definitions.

STIL-306 (error) Signals block redefined.

DESCRIPTION

This error is generated when the Signals block was redefined. Only one and anonymous Signals block is allowed in STIL syntax.

WHAT NEXT

Remove the duplicated definition of Signals block.

STIL-307 (error) Anonymous SignalGroups block redefined.

DESCRIPTION

This error is generated when the anonymous SignalGroups block was redefined. Only one anonymous SignalGroups block is allowed in STIL syntax.

WHAT NEXT

Remove the duplicated definition of the anonymous SignalGroups block.

STIL-308 (error) Named %s domain not allowed in this context.

DESCRIPTION

This error is generated when it is not allowed to defined a named domain in the current context. e.g. when you try to define a named SignalGroups domain in the CoreTypes block. Only an anonymous SignalGroups domain is allowed to be defined there.

WHAT NEXT

Modify the named domain to an anonymous(unnamed) domain.

STIL-309 (error) Cann’t define SignalVariables in %s block.

DESCRIPTION

This error is generated when user try to define SignalVariables in the block mentioned. This definition is not supported currently.

WHAT NEXT

Remove the SignalVariable definition from the concerned block.

STIL-310 (error) Cann’t define SignalVariableEnums in %s block.

DESCRIPTION

This error is generated when user try to define SignalVariableEnums in the block mentioned. This definition is not supported currently.

WHAT NEXT

Remove the SignalVariableEnum definition from the concerned block.

STIL-311 (error) ScanChain Length and number of scancells don’t match in ScanChain %s.

DESCRIPTION

This error is generated when the specified scan chain length doesn’t match the number of scan cells in the ScanChain mentioned.

WHAT NEXT

Check to make them consistent.

STIL-312 (error) Time expression format are supported.

DESCRIPTION

This error is generated when the format of time expression user specified is not supported now. Currently only numerical time expression format is supported.

WHAT NEXT

Modify the concerned time expression to numerical only format.

STIL-313 (error) The ScanInversion must be 0 or 1 in

ScanChain %s.

DESCRIPTION

This error is generated when the user specify the ScanInversion value as neither 0 nor 1. The ScanInversion value means the overall inversion from before the first scan cell to after the last scan cell.

WHAT NEXT

Correct the ScanInversion value to either 0 or 1.

STIL-314 (error) Anonymous ScanStructures block redefined.

DESCRIPTION

This error is generated when the anonymous ScanStructures block was redefined. Only one anonymous ScanStructures block is allowed in STIL syntax.

WHAT NEXT

Remove the duplicated definition of the anonymous ScanStructures block.

STIL-315 (error) %s Domain %s redefined.

DESCRIPTION

This error is generated when the Domain mentioned above is redefined. The Domain can be SignalGroups, ScanStructures, Timing, Procedures or MacroDefs. Each named domain can only be defined once.

WHAT NEXT

Remove the duplicated domain definition.

STIL-316 (error) Anonymous Variables block redefined.

DESCRIPTION

This error is generated when the anonymous Variables block was redefined. Only one

anonymous Variables block is allowed in STIL syntax.

WHAT NEXT

Remove the duplicated definition of the anonymous Variables block.

STIL-317 (error) Duplicated signal %s in the signal expression.

DESCRIPTION

This warning is generated when there exists duplicate signals in a signal expresion.

WHAT NEXT

Check each element in the signal expression, find out and remove the duplicates.

STIL-318 (error) Non-cyclized data is not supported.

DESCRIPTION

This error is generated when user includes non-cyclized data in a vector statement. Currently the STIL reader only support single cyclized data in a vector statement. For exact meaning of cyclized and non-cyclized data, please refer to STIL syntax.

WHAT NEXT

You may need to remove non-cyclized data and find alternative ways to express that.

STIL-319 (warning) Only constant expression is allowed in %s.

DESCRIPTION

This error is generated under given context, integer expression or sigvar expression can only contains constant variables or values, while non-constant variables were used in those expressions.

WHAT NEXT

Replace the non-constant variables with constant variables or values.

STIL-320 (error) %s domain %s does not exist.

DESCRIPTION

This error is generated when the specified STIL domain was not defined before. The STIL domain can be SignalGroups, ScanStructures, Timing, Procedures or MacroDefs.

WHAT NEXT

Please check if the domain is referred or defined correctly.

STIL-324 (error) Can’t create PatternBurst %s.

DESCRIPTION

This error is generated when PatternBurst mentioned above can not be created during model construction. The most probable reason is that the PatternBurst with the same name has already been created before.

WHAT NEXT

Check if the duplicated PatternBurst has already been created.

STIL-326 (error) PatternExec block has multiple Timing statements.

DESCRIPTION

This error is generated when the PatternExec block has multiple Timing statements. Only one Timing statement is allowed according to STIL syntax.

WHAT NEXT

Remove the duplicated Timing statements in PatternExec block.

STIL-327 (error) PatternBurst %s does not exist.

DESCRIPTION

This error is genenrated when the PatternBurst mentioned in the PatternExec block was not defined before. It is required by the STIL syntax to define PatternBurst before referencing.

WHAT NEXT

Check if the PatternBurst was referred or defined correctly.

STIL-328 (error) PatternExec block has multiple PatternBurst statements.

DESCRIPTION

This error is generated when multiple PatternBurst statements is included in the PatternExec block. Currently only PatternBurst statement is allowed in PatternExec block according to STIL syntax.

WHAT NEXT

Define a new PatternBurst block to include the multiple PatternBurst statements, and put the new defined PatternBurst in the PatternExec block.

STIL-329 (error) Can’t create PatternExec %s.

DESCRIPTION

This error is generated when PatternExec mentioned above can not be created during model construction. The most probable reason is that the PatternExec with the same name has already been created before.

WHAT NEXT

Check if the duplicated PatternExec has already been created.

STIL-330 (error) Too many events in event list.

DESCRIPTION

This error is generated when you define a waveform character list, the number of events in the event list is more than the number of wfcs in the wfc list.

WHAT NEXT

Modify your wfc defintion to make them consistent.

STIL-331 (error) Waveform inheritance not supported.

DESCRIPTION

This error is generated when the user specify an InheritWaveform statement in WaveformTable definition. Currently, the waveform inheritance is not supported.

WHAT NEXT

Try alternative ways to reach the goal.

STIL-332 (warning) Unsupported construct in waveform definition.

DESCRIPTION

This warning is generated when the construct in the waveform definition is legal but not supported now. e.g. in the definition list of wfcs, currently we only support time-value pair definition. Other constructs are not recognized.

WHAT NEXT

Try alternative ways to reach the goal.

STIL-333 (error) Incomplete time-value pair in waveform

definition.

DESCRIPTION

This error is generated when there is an imcomplete time-value pair in waveform definition. Currently we only support time-value pair as the definition of wfcs.

WHAT NEXT

Correct it or try alternative ways to reach the goal.

STIL-334 (error) Waveform inheritance not supported.

DESCRIPTION

WHAT NEXT

STIL-335 (error) WaveformTable inheritance not supported.

DESCRIPTION

This error is generated when the user specify an InheritWaveformTable statement in WaveformTable definition. Currently, the waveform table inheritance is not supported.

WHAT NEXT

Try alternative ways to reach the goal.

STIL-336 (error) SubWaveforms not supported.

DESCRIPTION

This error is generated when the user specify an SubWaveforms statement in WaveformTable definition. Currently, the SubWaveforms is not supported.

WHAT NEXT

Try alternative ways to reach the goal.

STIL-337 (error) WaveformTable %s redefined.

DESCRIPTION

This error is generated when user redefined a WaveformTable in the same Timing domain. The WaveformTable definition should be unique within one Timing domain.

WHAT NEXT

Remove the duplicated definition of WaveformTable.

STIL-339 (error) Single signal expected for %s.

DESCRIPTION

This error is generated when a signal bus is passed in when a single signal is expected. e.g. in the scan chain definition, the scan in and scan out are required to be a single signal.

WHAT NEXT

Modified the signal bus to a single signal.

STIL-340 (error) Signal or SignalGroup %s not defined.

DESCRIPTION

This error is generated when user tries to refer to an undefined signal or signal group. Signals and SignalGroups must be defined before being referenced.

WHAT NEXT

Define the signal or signal group before using it.

STIL-341 (error) ScanCell %s not defined.

DESCRIPTION

This error is generated when user tries to refer to an undefined scancell. ScanCells must be defined before being referenced. They are defined in the ScanStructures

blocks.

WHAT NEXT

Define the scancell before using it.

STIL-342 (error) Anonymous BistStructures block redefined.

DESCRIPTION

This error is generated when the anonymous BistStructures block was redefined. Only one anonymous BistStructures block is allowed in STIL syntax.

WHAT NEXT

Remove the duplicated definition of the anonymous BistStructures block.

STIL-345 (error) Ambigous parameter matching '%s' in call to '%s'.

DESCRIPTION

This error is issued when a parameter is multiple defined in a macro or procedure call.

WHAT NEXT

Modify the macro or procedure call and remove the multiple defined parameter.

SEE ALSO

read_test_protocol(2).

STIL-401 (warning) Domain name '%s' already exists in the test model. Overwriting the old one.

DESCRIPTION

This warning is issued when a domain name in a STIL file read by read_test_protocol

command already exists in the existing test model.

The old domain in the test model will be replaced by the new one.

WHAT NEXT

If you do not want to overwrite the old one, remove the '-overwrite' argument from the read_test_protocol command. This will ignore the new one and keep the old one.

SEE ALSO

read_test_protocol(2).

STIL-402 (warning) Domain name '%s' already exists in the test model. Ignoring the new one.

DESCRIPTION

This warning is issued when a domain name in a STIL file read by read_test_protocol command already exists in the existing test model.

The old domain in the test model will be preserved, and the domain in the protocol file will be ignored.

WHAT NEXT

If you want to overwrite the old one, specify the '-overwrite' argument in the read_test_protocol command. This will replace the old one by the new one.

SEE ALSO

read_test_protocol(2).

STIL-403 (warning) Overwriting the existing waveform table with new timing.

DESCRIPTION

This warning is issued when the existing waveform talbe is overwritten by a new waveform table defined in the test protocol read by read_test_protocol command.

WHAT NEXT

Check if the new waveform table is compatible with the timing in other test modes.

SEE ALSO

read_test_protocol(2).

STIL-404 (error) The timing of signal '%s' is different from the existing one.

DESCRIPTION

This error is issued when the waveform of the signal in the test protocol is different from the existing one.

The sequence of events in a waveform should be in canonical order, and the waveforms in the test protocol read and in the existing protocol (or model) should be equal.

DFTCompiler allows only one timing block and waveform table. You cannot read a test protocol that has different timing block from the one in other test protocols in different test modes.

You can replace the old timing with the new timing only if you have no protocol, or you have only one test protocol and replace it in the same test mode.

WHAT NEXT

Write out the existing test protocol, and compare the timing block against the timing block of the test protocol you want to read.

SEE ALSO

read_test_protocol(2).

STIL-406 (Error) Signal or SignalGroup %s used in test setup procedure is not defined.

DESCRIPTION

This error is generated when user tries to refer to an undefined signal or signal group in test setup. Signals and SignalGroups must be defined before being referenced. Make sure all referenced signals are within double quotes.

WHAT NEXT

Define the signal or signal group before using it.

SYMB-1 (warning) The symbol attribute '%s' was lost during translation to db.

DESCRIPTION

This warning should never come out during production code. It is an internal warning.

WHAT NEXT

Call support and file a bug report.

SYMB-2 (error) Couldn't write to the file '%s'.

DESCRIPTION

This error should only come out if there is a file system error.

WHAT NEXT

Check the disks capacity ... the job may have run out of disk space while writing to the disk.

SYMB-3 (warning) Encountered an end of file before processing was finished in file '%s'.

DESCRIPTION

This should only happen when a ".syn" file has been corrupted or if there is a file in a design library that ends in a .syn suffix that was not generated by the dc_shell read or analyze commands.

WHAT NEXT

If the .syn file is corrupt, regenerate the .syn file by re-analyzing its source code. However, if the file was not generated by design_compiler, then the file

should be moved from the design library.

SYMB-4 (warning) Corrupted data file '%s' ... %s.

DESCRIPTION

The specified .syn file is corrupt. It should be regenerated by re-analyzing its source code.

WHAT NEXT

Regenerate the .syn file by re-analyzing its source code.

SYMB-5 (warning) The file '%s' is not a symb file.

DESCRIPTION

There is a file in a design library that has a .syn suffix, but it is not a .syn file.

WHAT NEXT

Remove (or move) the file.

SYMB-6 (warning) Can't read in this version of data file ... please regenerate the data file '%s' by re-analyzing its source.

DESCRIPTION

The file mentioned in the error message was created with a different version of the software.

WHAT NEXT

The file should be recreated by analyzing its source using the current analyzer.

SYMB-7 (warning) The value of the current time in the operating system
is earlier than the time of the source file.
The timestamp that will be used to save the .syn file
will be the time of the source file.

DESCRIPTION

This error message indicates that the timestamp used to create the source file is "in the future" compared to what the current machine thinks the time is. This is probably due to the fact that the filesystem’s time is ahead of the machine being run on.

WHAT NEXT

Get the UNIX system administrator to synch up the clocks on the network.

SYNDB-1 (error) Could not find parameter ’%s’ on module ’%s’.

DESCRIPTION

WHAT NEXT

SYNDB-2 (warning) Could not find design ’%s’ associated with module ’%s’.

DESCRIPTION

WHAT NEXT

SYNDB-3 (error) A port could not be found on the %s ’%s’ which matches
the port ’%s’ on the %s ’%s’.

DESCRIPTION

WHAT NEXT

SYNDB-5 (error) A design named ’%s’ has already been associated with module ’%s’.

DESCRIPTION

WHAT NEXT

SYNDB-6 (error) The port ’%s’ on the module has a different

direction than the port '%s' on the design.

DESCRIPTION

WHAT NEXT

SYNDB-7 (error) A parameter could not be found on the %s '%s' which matches
the parameter '%s' on the %s '%s'.

DESCRIPTION

WHAT NEXT

SYNDB-8 (error) Could not compile the synthetic design '%s'.

DESCRIPTION

WHAT NEXT

SYNDB-9 (error) Could not model the compiled synthetic design '%s'.

DESCRIPTION

WHAT NEXT

SYNDB-10 (error) The parameter '%s' for the module '%s' hasn't been specified

on the reference ’%s’.

DESCRIPTION

WHAT NEXT

SYNDB-11 (error) Could not build the synthetic design ’%s’.

DESCRIPTION

WHAT NEXT

SYNDB-12 (warning) A reference has been made to the module ’%s’ which has
had no designs specified which can implement it.

DESCRIPTION

WHAT NEXT

SYNDB-13 (error) Could not find the required attribute ’default_implementation’
on the module ’%s’

DESCRIPTION

WHAT NEXT

SYNDB-14 (warning) The attribute ’default_implementation’ is required on the

synthetic library module ’%s’.

DESCRIPTION

WHAT NEXT

SYNDB-15 (error) Module ’%s’ has an implementation ’%s’ which has a syntax error in the contained implementation ’%s’.

DESCRIPTION

WHAT NEXT

SYNDB-16 (error) In module ’%s’ implementation ’%s’, the contained operator ’%s’ cannot be found.

DESCRIPTION

```
Contained operators must be defined in one of the .sldb files
 in the ’synthetic_library’ variable.
```

WHAT NEXT

SYNDB-17 (error) In module ’%s’ implementation ’%s’, the contained module ’%s’ cannot be found.

DESCRIPTION

```
Contained modules must be defined in one of the .sldb files
 in the ’synthetic_library’ variable.
```

WHAT NEXT

SYNDB-18 (error) The synthetic library operator '%s' is referred to in the (linked) current design, but it cannot be found among the .sldb files.

DESCRIPTION

All synthetic library instantiations must be defined in
one of the .sldb files from the 'synthetic_library' dc_shell variable.

WHAT NEXT

SYNDB-19 (error) The synthetic library module '%s' is referred to in the (linked) current design, but it cannot be found among the .sldb files.

DESCRIPTION

All synthetic library instantiations must be defined in
one of the .sldb files from the 'synthetic_library' dc_shell variable.
Moreover, the instantiation cannot have a dont_use applied to it.

WHAT NEXT

SYNDB-20 (error) Cannot find the synthetic library implementation '%s' of module '%s'.

DESCRIPTION The implementation is referred to in the current

design hierarchy through inferencing, instantiation, or a contained_implementation attribute in a .sldb file. But the implementation declaration could not be found among the files listed in the *synthetic_library dc_shell* variable. Alternatively, a license could not be obtained for this implementation, the implementation had a **dont_use** applied to it, or the implementation is not valid with the specified target library technology.

WHAT NEXT

The .sldb file that contains the offending implementation should be listed in the *synthetic_library* variable and the *link_library* variable. Use **report_synlib** to see the contents of a .sldb file. Licenses are automatically checked out, unless the *synlib_dont_get_license* variable prevents them from being checked out or all the licenses are currently in use.

Check the legality and technology attributes of the implementation within the synthetic library (if possible) to determine applicability.

SYNDB-21 (error) The stall pin attribute is illegal on module %s.

DESCRIPTION

The *stall pin* attribute is valid only for modules associated with behavioral synthesis sequential operators. A behavioral synthesis sequential operator has a *clocking_scheme* group defined for the module.

WHAT NEXT

Check the module to see if it has a *clocking_scheme* group.

SYNDB-22 (error) %s binding '%s' must be associated with a %s module '%s'.

DESCRIPTION

Combinational bindings are bindings without *state* groups. Sequential bindings have state groups. A combinational module is a module without a *clocking_scheme* group. A sequential module has a *clocking_scheme* group.

WHAT NEXT

Reexamine your binding and module definitions to insure that both are either combinational or sequential.

SYNDB-23 (error) Improper use_resource name '%s' in binding

'%s' of module '%s'.

DESCRIPTION

The *use_resource* names in bindings must be declared as resources in the sequential module.

WHAT NEXT

Add the resource declaration to the sequential module.

SYNDB-24 (error) Stable pin '%s' of binding '%s' of module '%s' has a changed value in the next state.

DESCRIPTION

A pin that has the *stable* attribute in one state must have the same binding in the next state, so that its value remains stable between the two states.

WHAT NEXT

Change the pin association in the next state, or remove the *stable* attribute.

SYNDB-25 (error) Unable to use implementation '%s' in module '%s'.

DESCRIPTION

This error occurs due to conflicting specified information. This implementation cannot be both a user selected implementation as well as an implicit dont_use implementation.

WHAT NEXT

Either change the value of the set_dont_use command or unselect implementation.

SYNDB-26 (warning) Implementation '%s' in module '%s' has a

"dont_use"
implementation as a result of "dont_use" lower level synthetic part ’%s’

DESCRIPTION

This implementation will not be considered during implementation selection phase

WHAT NEXT

Check the value of the set_dont_use command

SYNDB-27 (error) Referenced module ’%s’ has no implementation.

DESCRIPTION

The specified module has no implementation as a result of all of its implementations have become "dont_use" implementations.

WHAT NEXT

Change the value of the set_dont_use command to allow more implementations to be selected.

SYNDB-28 (warning) Module ’%s’ has no implementation. This module
will not be considered during resource sharing.

DESCRIPTION

This module will not be considered during implementation selection. This occurs when all of its implementations have become implicit "dont_use" implementations.

WHAT NEXT

Change the value of the set_dont_use command.

SYNDB-30 (error) Cannot find valid synthetic library implementations for module '%s'.

DESCRIPTION

The module is referred to in the current design hierarchy. But no implementation declaration could be found among the files listed in the *synthetic_library dc_shell* variable. Alternatively, no implementations is valid for this module in current design hierarchy because: no license could be obtained for any available implementations or the implmentations had a **dont_use** applied to them.

WHAT NEXT

The .sldb file that contains the offending implementations should be listed in the *synthetic_library* variable and the *link_library* variable. Use **report_synlib** to see the contents of a .sldb file. Licenses are automatically checked out, unless the *synlib_dont_get_license* variable prevents them from being checked out or all the licenses are currently in use.

SYNDB-31 (error) The check implementation reference group '%s' within module '%s' refers to an implementation, '%s', which is not found in the current set of synthetic libraries.

DESCRIPTION

The *check_implementation* group of the named module contains the verify_use_implementation attribute. The value of this attribute names an implementation within the same module to be used as the verification implementation. This error signifies that no implementation named by the verify_use_implementation attribute was found within any of the synthetic libraries specified by the synthetic_library variable.

WHAT NEXT

Ensure that the synthetic_library variable enumerates all required synthetic libraries. Examine the contents of each synthetic library with the **report_synlib** command to ensure that the named implementation exists and is spelled correctly.

If the set of libraries passes the **check_synlib** command, yet still fails, examine the implementation used for verification purposes for attributes specifying technology libraries, legality checks, and so on.

SYNDB-32 (error) The generator named '%s' does not exist within the '%s' library.

DESCRIPTION

A *uses_generator* attribute has specified the use of a generator which does not exist within the scope of the named library. This error typically results from an incorrectly written synthetic library.

WHAT NEXT

Verify that the spelling of the generator specified by the *uses_generator* attribute matches the appropriate generator within the synthetic library source file.

SYNDB-33 (error) Implementation '%s' of module '%s' is not a valid implementation for the design when 'synlib_enable_dpgen = false'.

DESCRIPTION

When synlib_enable_dpgen = false, it is illegal to set forced implementations to generated implementations.

WHAT NEXT

Set the forced implementations to DesignWare Foundation parts, or turn on synlib_enable_dpgen to use generated implementations.

SYNDB-34 (error) Cannot find valid synthetic library module for operator '%s'.

DESCRIPTION

The operator is inferred in the current design. But no synthetic module could be found to implement the operator. This would cause problem during resource sharing.

WHAT NEXT

Check synthetic libraries to make sure there are synthetic modules to implement each synthetic operator.

SYNDB-35 (error) The design has set_implementation on the obsolete implementation '%s' of module '%s'.

DESCRIPTION

The module is referred to in the current design hierarchy, and the set_implementation command was performed to specify an obsolete implementation on a cell in the design. The obsoleted implementation is no longer supported and has no replacement implementation. Cannot find valid synthetic library implementations for the module.

WHAT NEXT

Call command report_attribute -cell -hierarchy. Find the cell that has 'implementation' attribute and the value of the attribute is the obsoleted implementation. Use command 'remove_attribute' to remove the attribute.

SYNDB-36 (warning) Implementation '%s' of module '%s' is replaced by '%s'. The design has 'set_implementation' to the obsolete implementation.

DESCRIPTION

The module is referred to in the current design hierarchy, and set_implementation command was performed to spedify an obsoleted implementation on a cell in the design. The obsoleted implementation is no longer supported and is replaced by the replacement implementation.

WHAT NEXT

The design compiler will automatically modify the implementation attribute on the cell to use the replacement implementation. If you do not want to use the replacement implementation, call command report_attribute -cell -hierarchy to find the cell that has attribute implementation and the value of the attribute is the obsoleted implementation. Use command remove_attribute to remove attribure implementation from the cell. Or use set_implementation command to choose another implementation.

SYNDB-37 (information) Implementation '%s' of module '%s' is

replaced by '%s'.

DESCRIPTION

The module is referred to in the current design hierarchy. The implementation is replaced by the replacement implementation.

The implementation that is been replaced is obsoleted and permanently replaced by the new implementation.

If a design is set_implementation to a MC architecture, the set_implementation will be morphed to use the architecture from the advanced generator.

WHAT NEXT

The design compiler will use the replacement implementation. The obsoleted implementation will no longer be used in the design.

SEE ALSO

synlib_enable_dpgen(3)

SYNDB-38 (information) Implementation '%s' of module '%s' is obsoleted.

DESCRIPTION

The module is referred to in the current design hierarchy. The implementation obsoleted and will no longer be used.

WHAT NEXT

The design compiler will choose other implementations for the module. The obsoleted implementation will no longer be used in the design.

SYNDB-39 (error) Could not find the replacement implementation '%s' of obsoleted implementation '%s'. No valid

synthetic implementation for module '%s'.

DESCRIPTION

The module is referred to in the current design hierarchy. And set_implementation command was performed to spedify an obsoleted implementation on a cell in the design. The obsoleted implementation is replaced by the replacement implementation. The attempt to find the replacement implementation among the files listed in the *synthetic_library dc_shell* variable has failed. Alternatively, the replacement implementation is not valid because: no license could be obtained for any available implementations or the implmentations had a **dont_use** applied to them.

WHAT NEXT

The .sldb file that contains the offending implementations should be listed in the *synthetic_library* variable and the *link_library* variable. Use **report_synlib** to see the contents of a .sldb file. Licenses are automatically checked out, unless the *synlib_dont_get_license* variable prevents them from being checked out or all the licenses are currently in use.

Alternatively, remove the implementation attribute from the cell to allow automatic selection of implementations for the module. report_attribute -cell command can be used to find the cell that has the implementation attribute. Use command remove_attribute to remove the attribure from the cell.

SYNDB-40 (warning) The 'implementation' attribute on cell '%s' in design '%s' is changed from '%s' to '%s'.

DESCRIPTION

The module is referred to in the current design hierarchy, and set_implementation command was performed to spedify an obsoleted implementation on the cell in the design. The obsoleted implementation is no longer supported and is replaced by the replacement implementation. The value of 'implementation' attribute on the cell is modified to use the replacement implementation.

WHAT NEXT

The replacement implementation will be chosen for the cell. If you do not want to use the replacement implementation, use remove_attribute command to remove the implementation attribute from the cell.

SYNDB-41 (warning) Syntax error in property '%s' set on %s.

DESCRIPTION

This warning message occurs when there is a syntax error in a property set on the module or implementation.

The format of the syntax is as follows:

```
<property_type>:<property_name>:<property_value>
```

Separate multiple property definitions with white spaces.

The supported property types are Boolean, string, and integer. For a Boolean property, the value can only be **true** or **false**.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you expected, correct the syntax error in the synthetic library file and run the command again.

SYNDB-42 (warning) Property '%s' of type '%s' exists %s

DESCRIPTION

There are duplicated properties on the synthetic library module or implementation. The new property will be ignored.

WHAT NEXT

Remove the duplicated property name in synthetic library file.

SYNDB-43 (Error) DesignWare operator '%s' has interface change.

DESCRIPTION

The interface of the DesignWare operator has been change since the design was elaborated. The DW operator can not be linked correctly. Please re-elaborate the rtl design use the latest Design Compiler.

WHAT NEXT

Re-elaborate the rtl design use the latest Design Compiler.

SYNDB-44 (warning) The implementation attribute (%s, %s) on cell %s in design %s is removed.

DESCRIPTION

This warning message notifies you that the implementation attribute on the cell has been removed. The module is referred to in the current design hierarchy, and the **set_implementation** command was performed to specify a free implementation on a cell in the design. The generated implementation provides better QoR. Free implementations are no longer used in the compile flow where generated implementations are available.

WHAT NEXT

This is only a warning message and no action is required. However, to get better QoR, do not **set_implementation** to a free implementation. If you need to use the free implementation, do not add dw_foundation.sldb in your synthetic_library list, and do not use **compile_ultra** flow.

SEE ALSO

set_implementation(2)

SYNDB-45 (information) Implementation ’%s’ of module ’%s’ is replaced by ’%s’.

DESCRIPTION

This information message advises you that the module is referred to in the current design hierarchy. The implementation is replaced by the replacement implementation in the compile_ultra flow. The replacement implementation provides better QoR.

WHAT NEXT

Design Compiler will use the replacement implementation.

SYNDB-46 (information) Implementation ’%s’ of module ’%s’ is

dont use as a result of dont use implementation ’%s’.

DESCRIPTION

This information message advises you that you set *dont use* on the free implementation. This implies that the generated implementation that covers the same QoR range is also *dont use*.

WHAT NEXT

Design Compiler will not use the generated implementation.

SYNENC-1 (error) Syntax error in HDL source file "%s".

DESCRIPTION

"synenc" has encountered syntax errors. The specified source file is not legal VHDL or Verilog. This may be caused by non-standard statements or comments near the beginning of the file.

WHAT NEXT

If this error occurs, please use your VHDL or Verilog compiler to identify and correct any syntax problems in the source file.

SYNENC-2 (error) "%s" is not a plain file.

DESCRIPTION

The file system path specified did not reference a text file. It looks like a directory or other special file.

WHAT NEXT

Check the path to make sure it is a valid VHDL or Verilog source file.

SYNENC-3 (error) cannot open file ’%s’ for reading.

DESCRIPTION

The specified input file is not readable.

WHAT NEXT

Check the Unix permissions on the specified file.

SYNENC-4 (error) cannot open file ’%s’ for writing.

DESCRIPTION

The specified output file cannot be opened for writing. ’synenc’ always writes encrypted source files to the user’s current working directory and gives them the name "inputfilename.e". Either the file already exists and is write protected or the user doesn’t have correct permissions to create a file in the current working directory.

WHAT NEXT

Delete old encrypted files. ’cd’ to a directory for which you have write permissions.

SYNENC-5 (error) Error while reading source file for encryption.

DESCRIPTION

Some unexpected condition caused the read of the source file to fail. This could be caused by a network failure or some similar transient condition.

WHAT NEXT

Try to encrypt the file again.

SYNENC-6 (error) Internal encryptor error.

DESCRIPTION

WHAT NEXT

SYNENC-7 (information) Processed file ’%s’.

DESCRIPTION

WHAT NEXT

SYNH-1 (information) The synthetic implementation was read from a cache.

DESCRIPTION

There is an obsolete or invalid implementation contained in a synthetic library cache(s) specified by your cache_read variable.

WHAT NEXT

Remove the old, incorrect implementation from the cache.

SYNH-2 (information) Read implementation '%s' for synthetic design '%s' from design library '%s'.

DESCRIPTION

The named synthetic implementation was extracted from the named library.

A faster way to retreive synthetic implementations is to store them in and retreive them from a synthetic cache. An installation program (install_synlib) puts simple synthetic parts in the system cache.

WHAT NEXT

Store synthetic implementations you use often in a synthetic cache. Refer to the DesignWare reference manual for more details.

SYNH-3 (information) Modeled %s(%s). (Timing Model = %s Operating Conditions = %s)

DESCRIPTION

You receive this message because the named synthetic design was optimized to obtain representative timing and area numbers for the part. These numbers are used to model the part in subsequent optimizations.

Once a part is modeled, it can be stored in a synthetic cache. Thus, subsequent compiles will not have to recreate the model. Use the variable's **cache_read** and **cache_write** to set up your cache. You can also use the **create_cache** command to store parts in your cache.

WHAT NEXT

Store in a synthetic cache the synthetic implementations you often use. For more information, see to the *DesignWare Reference Manual*.

SEE ALSO

create_cache (2).

SYNH-4 (information) The synthetic model was read from a cache.

DESCRIPTION

There is an obsolete or invalid model in a synthetic library cache(s) specified by your cache_read variable.

WHAT NEXT

Remove the old, incorrect model from the cache.

SYNH-7 (error) Module '%s', implementation '%s' does not have a library attribute.

DESCRIPTION

When Design Compiler tries to build a synthetic module/implementation, it needs to know which design library the netlist is in. This information is an attribute of either the module (which provides a default for all implementations), or of the implementation itself.

WHAT NEXT

Modify the synthetic library source to add the library attibute to either the module or implementation. Also, if it has not already been done, store the source for the design's netlist in the library. For VHDL/verilog, use the **analyze** command; for db designs, use the **writefP command.**

SYNH-8 (error) Can’t link to module ’%s’ implementation ’%s’ in synthetic part ’%s’.

DESCRIPTION

This error occurred when linking a synthetic part that contains another synthetic part (the subpart). One possible problem is that one part comes from one synthetic library while the subpart comes from another synthetic library, and both libraries are not in the synthetic_library variable. Another possible problem is that the subpart is not mentioned as a contained operator/module/implementation of the parent part, so the license for the subpart was not checked out and the subpart was not considered an authorized synthetic library part.

WHAT NEXT

Add the subpart’s .sldb file to the synthetic_library variable. Ensure that the subpart is listed as a contained operator/module/implementation of the parent part in the parent part’s

SYNH-9 (warning) Synthetic library implementation ’%s’ in module ’%s’ is an empty netlist.

DESCRIPTION

The given synthetic implementation either has no description for the netlist or the entire netlist has been optimized away. This may cause problems in your final netlist.

WHAT NEXT

You do not need to take any action regarding this message.

SYNH-10 (error) Port number %d of implementation ’%s’ of synthetic module ’%s’ should be ’%s’.

DESCRIPTION

The netlist or hdl description of the named implementation does not match the module declaration in the synthetic library.

WHAT NEXT

Make sure that the ports in your netlist or hdl description match your module declaration exactly, both in name and order.

SYNH-11 (error) Direction of port '%s' in implementation '%s' does not match the declared synthetic module '%s'.

DESCRIPTION

The netlist or hdl description of the named implementation does not match the module declaration in the synthetic library.

WHAT NEXT

Make sure that the netlist or hdl description has the correct direction for the named port.

SYNH-12 (error) Width of port '%s' in implementation '%s' does not match the declared synthetic module '%s'.

DESCRIPTION

The netlist or hdl description of the named implementation does not match the module declaration in the synthetic library.

WHAT NEXT

Make sure that the netlist or hdl description has the correct width for the named port. The width must match for all possible parameter values.

SYNH-13 (error) Port '%s' in implementation '%s' is not declared in the synthetic module '%s'

DESCRIPTION

The netlist or hdl description of the named implementation does not match the module declaration in the synthetic library.

WHAT NEXT

Make sure that the netlist or hdl description has the same ports as the synthetic module.

SYNH-14 (error) Cannot find a valid implementation for module '%s'.

DESCRIPTION

This message indicates that the specified module does not have a valid implementation, possibly because of problems that occurred during linking of a synthetic part that contains another synthetic part (the subpart). Here are some possible reasons for the lack of a valid implementation:

1. The **legal** parameter of the implementations might have made them all illegal. If a module uses legality, there must be at least one legal implementation for all parameter value combinations.

2. The part and the subpart might come from different synthetic libraries, and both libraries might not be in the **synthetic_library** variable.

3. The subpart might not be mentioned as a contained operator/module/implementation of the parent part, so the license for the subpart might not have been checked out and thus was not considered an authorized synthetic library part.

4. All of the module's implementations might require licenses, and perhaps none of those licenses have been purchased at the site.

WHAT NEXT

1. Ensure that there is at least one legal implementation for all parameter value combinations. For more information, refer to the *DesignWare Developer's Guide*.

2. Add the subpart's **.sldb** file to the **synthetic_library** variable.

3. Ensure that the subpart is listed as a contained operator/module/implementation of the parent part in the parent part's **.sl** file.

4. Examine the key file to determine whether a license has been purchased for the module's implementations. If not, purchase the required licenses.

SYNH-15 (error) Missing connection for input pin '%s' for binding

’%s’ in module ’%s’ for operation ’%s’.

DESCRIPTION

Each binding must specify how to connect ALL inputs of a module.

WHAT NEXT

SYNH-16 (error) Design hierarchy is not allowed inside a synthetic library part. The module ’%s’ implementation ’%s’ has hierarchy in it.

DESCRIPTION

We support only hierarchy that is a technology library or a synthetic library module or operator.

WHAT NEXT

If the hierarchy is a technology library or a synthetic library, check the *synthetic_library* and *link_library* variables and the *set_local_link_library* directive.

SYNH-17 (error) Cannot find a legal implementation of any module to implement the operations bound to the resource ’%s’.

DESCRIPTION

An attempt to build the netlist for the module failed. One possible cause is that the module has no implementations in the synthetic library. This can happen if no implementations are declared for the module in synthetic libraries or if all implementations have a *dont_use* on them.

WHAT NEXT

SYNH-18 (error) Cannot find a legal implementation of any

module
to implement the operator '%s'.

DESCRIPTION

While performing resource sharing, no legal implementation of ANY synthetic module was found which could implement the named operator. Check legality specifications in the synthetic libraries.

WHAT NEXT

SYNH-19 (warning) Module '%s' was not found in the files of synthetic_library. Implementation of synthetic design '%s' (cell '%s') is not being reconsidered.

DESCRIPTION

Synthetic implementation selection is not being reconsidered because the synthetic module for this design can no longer be found. Either the synthetic library that contains the module is not listed in the *synthetic_library* variable, or the module has been marked *dont_use*.

WHAT NEXT

Add the appropriate synthetic library, or remove the **dont_use** attribute.

SYNH-20 (warning) set_implementation '%s' was not found in the files of synthetic_library. Implementation of synthetic design '%s' (cell '%s') is not being reconsidered.

DESCRIPTION

The **set_implementation** command on this cell cannot be performed because the synthetic implementation specified cannot be found. Either the synthetic library that contains the implementation is not listed in the *synthetic_library* variable, or the implementation has been marked *dont_use*.

WHAT NEXT

Correct your **set_implementation** command, add the appropriate synthetic library, or remove the *dont_use* attribute.

SYNH-21 (information) Modeled %s(%s).

DESCRIPTION

The named synthetic design was optimized to obtain representative timing and area numbers for the part. These numbers will be used to model the part in subsequent optimizations.

Once a part is modeled, it can be stored in a synthetic cache. This way, subsequent compiles will not have to recreate the model. Use the variables "cache_read" and "cache_write" to set up your cache. You can also use the "create_cache" command to store parts in your cache.

WHAT NEXT

Store synthetic implementations you use often in a synthetic cache. Refer to the DesignWare reference manual for more details.

SYNH-22 (warning) Current implementation '%s' of module '%s' was not found in the files of synthetic_library. Implementation selection of synthetic design '%s' (cell '%s') will take longer.

DESCRIPTION

Either the synthetic library that contains the implementation is not listed in the *synthetic_library* variable, or the implementation has been marked *dont_use*. When the current implementation cannot be found in the synthetic library, the implementation selection algorithm cannot use cached models to make design trade-offs. This makes it necessary to compile trial designs on-the-fly, and slows down the process.

WHAT NEXT

If you wish to increase your CPU performance you may choose to: add the appropriate synthetic library; remove the *dont_use* attribute; use *set_implementation* to change the implementation of the cell; use *set_implementation* to lock the implementation of the cell to its current value; or set *compile_implementation_selection* to false.

SYNH-30 (error) An incorrect range has been specified for parameter ’%s’.

DESCRIPTION

The defined parameter range is invalid because the end value is equal or larger than the start value.

WHAT NEXT

Provide a correct range for the parameter.

SYNH-31 (error) The specified parameter set doesn’t match the required parameter set for module %s.

DESCRIPTION

The specified parameters doesn’t match the required parameters of the module.

WHAT NEXT

Provide a correct parameter set.

SYNH-32 (error) Failed to generate the module due to previous errors.

DESCRIPTION

The tools failed to create a netlist and cache it. The reason for failure is reported by other error messages. This inform the user that the requested module was not created.

WHAT NEXT

Fix the problem and try again.

SYNH-33 (warning) Cannot find any module with the given

name.

DESCRIPTION

The requested module cannot be found in the synthetic libraries pointed to by the cache_read and cache_write variables. It is very likely that the user mistyped the name of the module on the command line.

WHAT NEXT

Check the name of the module, and try again.

SYNH-34 (error) Cannot find any valid implementation for module '%s' to match the requested implementation name.

DESCRIPTION

The requested implementation cannot be found in the synthetic libraries pointed to by the cache_read and cache_write variables. It is very likely that the user mistyped the name of the implementation on the command line.

WHAT NEXT

Check the name of the implementation, and try again.

SYNH-35 (error) Too many parameters have been specified.

DESCRIPTION

The requested module requires less parameters than those specified by the user. This is most certainly a user error.

WHAT NEXT

Re-run the command with the correct number of parameters.

SYNH-36 (error) Too few parameters have been specified.

DESCRIPTION

The requested module requires more parameters than those specified by the user. This is most certainly a user error.

WHAT NEXT

Re-run the command with the correct number of parameters.

SYNH-37 (error) Parameter name mismatch. This module requires parameter '%s'.
The provided parameter name is '%s'.

DESCRIPTION

The requested module requires a parameter with a certain name. The parameter name provided by the user does not contain a reference to required parameter.

WHAT NEXT

Re-run the command with the correct parameter set.

SYNH-38 (warning) '%s' is not a valid wire load in the specified technology library.

DESCRIPTION

The requested wire-load model cannot be found in any of the technology libraries identified by the *target_library* variable.

WHAT NEXT

Check the name of the wire-load model, and make sure it is a valid wire-load model within the identified target technology libraries.

SYNH-39 (error) '%s' is not a valid operating condition in the

specified technology libraries.

DESCRIPTION

The requested operating condition cannot be found in any of the technology libraries identified by the *target_library* variable.

WHAT NEXT

Check the name of the operating condition, and make sure it is valid within the identified target technology libraries. To check the name of the operating condition, run the **report_lib** command.

SYNH-40 (warning) No known implementation matched '%s'.

DESCRIPTION

The requested implementation for the synthetic module is not valid. If the implementation name contained a wild-card character, there was no match.

WHAT NEXT

Check the implementation name, and make sure it is a valid implementation of the module.

SYNH-41 (error) The implementation '%s' is not legal for implementing
the operations bound to resource '%s'.

DESCRIPTION

User used manual resource sharing directives to implement one or more operations on an implementation which is not legal for the operations. For example, the bit width might be outside the legal range.

WHAT NEXT

SYNH-42 (warning) IIS optimization was skipped because the appropriate license could not be checked out.

DESCRIPTION

Incremental Implementation Selection requires a HDL-Compiler or VHDL-Compiler license. The quality of results may be suboptimal.

WHAT NEXT

Explicitly grab a license (get_license) and make sure the variable hdl_keep_licenses is set true.

SYNH-43 (warning) Syntax error in the 'synthetic_library' variable assignment. Default value will be used.

DESCRIPTION

An error occurred during a parse of the value of the *synthetic_library* variable. The variable should be set to a list of .sldb files. For example: *synthetic_library = { dw01.sldb dw02.sldb }*. The default value {} will be used. Note that standard.sldb is automatically included in the *synthetic_library value*.

WHAT NEXT

Change the value of your *synthetic_library* variable.

SYNH-44 (warning) The synthetic library module '%s' implementation '%s' failed to link.

DESCRIPTION

This error occured when linking a synthetic part. One possible problem is that the part has illegal hierarchy (for example, a level of hierarchy that is not a synlib part). Another possible problem is that there one synlib part contains another part (or technology cell) and both part's .sldb files are not in the synthetic_library variable. Another possible problem is that the subpart is not mentioned as a contained operator/module/implementation of the parent part, so the license for the subpart was not checked out and the subpart was not considered an authorized synthetic library part. Another possible problem is the local_link_library variable was not set correctly.

WHAT NEXT

Make sure the parts linked are synlib parts, technology cells, or GTECH cells. Add the subpart's .sldb file to the synthetic_library variable. Ensure that the subpart is listed as a contained operator/module/implementation of the parent part in the parent part's .sl file. Make sure the local_link_path is set correctly.

SYNH-45 (warning) Test logic has been inserted in %s. Skipping incremental implementation selection for that design.

DESCRIPTION

Incremental implementation selection attempts to change the implementation of a DesignWare part during compile. This attempt is being skipped for the named design because test logic has already been inserted into the design. Changing the implementation at this point would invalidate the test connections.

WHAT NEXT

If constraints are not being met through the design and incremental implementation selection is desired. Swap out the design for the non-test equivalent, and do the compile again.

SYNH-46 (error) Could not find port '%s' in implementation '%s' of synthetic module '%s'.

DESCRIPTION

This message indicates that the named port could not be found in the definition for the implementation as given in the synthetic library.

WHAT NEXT

Verify the set of defined ports in the synthetic library for the implementation with the report_synlib command. See the DesignWare Developer Guide for further information on these topics.

SYNH-47 (warning) No stall value has been specified for processor input pin

%s for binding %s in module %s and operation %s.

DESCRIPTION

The binding in the synthetic library does not contain any specification of a stall value. This implies, that whenever no operation is performed on this module, you can not make any assumptions about the driving value of this pin. This can have serious effects on the behavior of your circuit e.g. if the input pin is the read_write_enable for a memory you will want it to default to read.

WHAT NEXT

Check carefully, whether you are relying on certain inputs being fed to the module when it is not actively executing an operation.

SYNH-48 (warning) The following module/implementation/ parameters are invalid combinations, they were ignored: %s

DESCRIPTION

The parameters in the module/implementation/parameters combination were out of the module or implementation's legal range. They were silently skipped in 'create_catch' command.

WHAT NEXT

SYNH-49 (warning) No default operating condition found.

DESCRIPTION

There is no operating condition specified for the create_cache command. We are trying to get the default operating condition from the target library. But There is no default operating condition found in the target library. No operating condition is used when creating DW models.

WHAT NEXT

Please specify an operating condition to be used when creating DW model cache.

SYNH-50 (warning) Select operator cannot be built through the MGI.

DESCRIPTION

Currently the MGI does not facilitate the creation of select operators.

WHAT NEXT

Create select operators using a conventional synthetic library. See the DesignWare Developer’s Manual for more information.

SYNH-51 (warning) The array naming style of the synlib part %s is different than the current bus_naming_style setting %s. Skipping Incremental Implementation Selection for the design.

DESCRIPTION

Incremental implementation selection attempts to change the implementation of a Synthetic part during compile. This attempt is being skipped for the named design because the array naming style of the design is different than the current global bus_naming_style setting, thus the port names will not match on busses.

WHAT NEXT

Check the bus_naming_style setting, make sure it is consistant with the synlib part’s setting.

SYNH-52 (error) DC failed to elaborate netlist for ’%s’, implementation ’%s’.

DESCRIPTION

DC(Presto) failed to retrieve the netlist of the synthetic part. Possible causes of the failure are: 1. The source files of the synthetic component or implementation are not analyzed by the current release of the DesignCompiler; 2. There are syntax errors in the source file of the synthetic component or implementation.

WHAT NEXT

If the synthetic component or implementation are user defined, please re-analyze the source files using the current DesignComplier release. If the synthetic component and implementation are Synopsys component and implementation, please contact Synopsys DesignWare support.

SYNL-4 (information) Ignoring dont_touch on synthetic instance ’%s’ of ’%s’.

DESCRIPTION

WHAT NEXT

SYNL-5 (error) Can’t find parameter ’%s’ in specification "%s

DESCRIPTION

WHAT NEXT

SYNL-6 (error) Malformed parameter specification "%s

DESCRIPTION

WHAT NEXT

SYNL-7 (error) ’%s’ is an invalid or out-of-date synthetic library.

DESCRIPTION

There is a bad module-to-operator binding in this synthetic library. Or this synthetic library is out_of_date with respect to other synthetic libraries.

WHAT NEXT

Use the up to date synthetic library; Or remove the offended binding from the module in this synthetic library; Or remove this synthetic library from the synthetic library and the link library lists.

SYNL-8 (warning) Can’t find operator ’%s’ for binding ’%s’ in module ’%s’.
Binding ignored.

DESCRIPTION

WHAT NEXT

SYNL-9 (error) Can’t find oper_pin ’%s’ for binding ’%s’ in module ’%s’.

DESCRIPTION

There is a pin mis-match between the operator and the associated module. The attempt to bind the operator to the module failed.

WHAT NEXT

Check the oper_pin declaration in the binding of this module; Or update this synthetic library; Or remove the offended synthethic library from the synthetic library and the link library lists.

SYNL-10 (error) Direction of operator pin ’%s’ does not match direction
of module pin ’%s’ in binding ’%s’ of module ’%s’.

DESCRIPTION

WHAT NEXT

SYNL-11 (error) Cannot find a module for ’%s’.

Synthetic libraries disabled.

DESCRIPTION

WHAT NEXT

SYNL-12 (error) Can’t find synthetic file ’%s’ in the synlib_search_path.

DESCRIPTION

WHAT NEXT

SYNL-13 (error) %s.

DESCRIPTION

This message may have several different outputs. Below is information on each one:

No formula or specified value for parameter ’%s’ in library specification for module ’%s’, implementation ’%s’. The synthetic module or implementation requires the given parameter. When instantiating the module, the parameter was not specified.

Remember, synthetic library parameter names are case-sensitive. Keep in mind that the offending part instantiation might be nested inside another synthetic implementation.

WHAT NEXT

No formula or specified value for parameter ’%s’ in library specification for module ’%s’, implementation ’%s’. Make sure you specify the required parameter. If you are using DesignWare developer, you can modify the module/implementation definition in your *.sl file so that the parameter is derived automatically (via a formula attribute).

SYNL-14 (error) Parameter ’%s’ does not evaluate to %s

%s.

DESCRIPTION

WHAT NEXT

SYNL-15 (error) Parameter '%s' not defined

%s.

DESCRIPTION

WHAT NEXT

SYNL-16 (error) All of the following regular licenses have been checked out:

%s.

The users of the licenses are listed in the following error message.

DESCRIPTION

The licenses for all implementations are checked out early in the **compile** command. If the license for one implementation cannot be obtained, the Design Compiler command is terminated because the missing implementation may affect compile results.

WHAT NEXT

Request that one of the users with a license release the license using the **remove_license** command.

SYNL-17 (error) Unknown input oper_pin '%s' specified as

permutable on operator '%s'.

DESCRIPTION

The specified input pin name in the permutable_inputs attribute is not on the operator.

WHAT NEXT

Changes this pin name to match with the pin name on the synthetic operator.

SYNL-18 (warning) Input oper_pin '%s' multiply specified as permutable.

DESCRIPTION

WHAT NEXT

SYNL-19 (warning) The limited license '%s' is being checked out to enable the synthetic library part implementation '%s'. Note: designs cannot be written out if they have synthetic library parts enabled with limited licenses.

DESCRIPTION

WHAT NEXT

SYNL-20 (error) The synthetic library part implementation '%s' should be available for use during the compile command, but the implementation is not enabled because all of the following limited licenses have been checked out:

%s.
The users of the licenses are listed in the following error message.

DESCRIPTION

The licenses for all implementations are checked out early in the **compile** command. If the license for one implementation cannot be obtained, the Design Compiler command is terminated because the missing implementation may affect compile results.

WHAT NEXT

Request that one of the users with a license release the license using the **remove_license** command.

SYNL-21 (warning) The license '%s' is not legal and will be ignored
for the synthetic library part implementation '%s'.

DESCRIPTION

WHAT NEXT

SYNL-22 (warning) The write cache directory '%s' is not listed as one of the read cache directories.
Synthetic library parts written out to the cache cannot be read back from the cache.

DESCRIPTION

WHAT NEXT

SYNL-23 (error) Synthetic module '%s' cannot be linked

because port width(s) cannot be determined.

DESCRIPTION

The port width of the given instantiated module could not be determined. This has two probable causes. The first is that the parameters (generics) which you specified were named incorrectly and did not match the synthetic library part.

The second cause may be that you linked to a synthetic library part by accident, and you actually wanted a technology library part. You should check to make sure that the names in your synthetic library do not clash with the names in other libraries. (Be careful, VHDL references are case-insensitive, so you may be linking to a module called ’add’ from a synthetic library when you wanted to link to cell ’ADD’ from a technology library.)

WHAT NEXT

SYNL-24 (error) Synthetic library ’%s’ is from an incompatible version of the software.

DESCRIPTION

You cannot use the given synthetic library with this version of the software. If you are worried about obtaining "standard.sldb", don’t worry. An up-to-date standard.sldb always used, no matter how the synthetic_library variable is set. The correct default setting for synthetic_library is **{}**.

WHAT NEXT

SYNL-25 (error) Pin association ’%s’ does not correspond to a module pin in binding ’%s’ for module ’%s’.

DESCRIPTION

WHAT NEXT

SYNL-26 (warning) Binding ’%s’ multiply defined for module ’%s’.

Binding ignored.

DESCRIPTION

WHAT NEXT

SYNL-27 (warning) Priority for implementation '%s' of module '%s' is out of range. Using the default value '%d'.

DESCRIPTION

The priority formula for the given implementation evaluated to a value outside of the legal priority range.

WHAT NEXT

SYNL-28 (warning) Can't find operator pin '%s' for binding '%s' in module '%s'.
Binding ignored.

DESCRIPTION

The argument for the constraint or *unbound_oper_pin* groups must be an operator input pin name.

WHAT NEXT

SYNL-29 (error) Could not check out '%s' or '%s' license. Cannot continue to process the libraries listed in the 'synthetic_library' variable.

Set "synlib_evaluation_mode = true" to evaluate parts.

DESCRIPTION

Processing synthetic libraries other than the baseline 'standard.sldb' requires a license. This error message is issued when you attempt to use a non-baseline synthetic library and the license cannot be obtained. Following this error, the current command will probably abort. Some commands (such as report) do not strictly need synthetic libraries and may continue to run.

This error will also be triggered if you add your own parts to standard.sldb (because the added non-baseline parts require a license). You should not add parts to standard.sldb.

WHAT NEXT

You either need to obtain a license or give up using non-baseline synthetic libraries. If you don't require synthetic libraries for the current command, simply set "synthetic_library = {}", and no license will be required.

In addition, you should routinely set "synthetic_library = {}" when you don't require synthetic libraries. This will prevent your process from checking out a license, and will leave licenses free for other's use.

SYNL-32 (warning) The synthetic library part implementation '%s' should be available for use during the compile command, but the implementation is not enabled because all of the following licenses have been checked out: %s. Waiting for a license to become available. Press <ctrl>-C to interrupt the command. The users of the licenses are listed in the following error message.

DESCRIPTION

The current design contains inferred or instantiated DesignWare parts for which licensed implementations are available. All of the licenses that enable the use of one or more of the licensed implementations are currently in use. The current

command will wait until a license becomes available.

WHAT NEXT

Request that one of the users with a license release the license using the **remove_license** command. Interrupt the command using <ctrl>-C.

SYNL-33 (error) Missing clock polarity for pipelined part '%s'.

DESCRIPTION

Clock port is specified on the encapsulated function reference but there is polarity specified.

WHAT NEXT

SYNL-34 (error) Missing polarity for asynchronous reset pin '%s' on pipelined part '%'.

DESCRIPTION

Asynchronous reset pin is specified on the encapsulated function but without the polarity.

WHAT NEXT

SYNL-35 (error) Missing polarity for synchronous reset pin '%s' on pipelined part '%'.

DESCRIPTION

Synchronous reset pin is specified on the encapsulated function but without the polarity.

WHAT NEXT

SYNL-36 (error) Missing polarity for pipeline stall pin '%s' on

pipelined part ’%s’.

DESCRIPTION

Pipeline stall pin is specified on the encapsulated function but without the polarity.

WHAT NEXT

SYNL-37 (error) Invalid pipeline stages ’%s’ is detected on pipelined part’%s’.

DESCRIPTION

The number pipeline stages that is specified on the encapsulated function must be greater than 1.

WHAT NEXT

SYNL-38 (error) Missing pipeline stages for this pipelined part ’%s’.

DESCRIPTION

The number of pipeline stages is not specified on the encapsulated pipelined function.

WHAT NEXT

Specify the pipeline stages using bc command, set_pipeline_design.

SYNL-39 (error) Data_class attribute on operator ’%s’ contains invalid value ’%s’.

DESCRIPTION

The string value of the data_class attribute is not one of the "unsigned", "signed" strings.

WHAT NEXT

SYNL-40 (warning) Invalid string format '%s' for the permutable_inputs is detected on operator '%s'.

DESCRIPTION

The string value of the permutable_inputs attribute is not in the correct format.

WHAT NEXT

Change the value to conform to the "name1 name2 nam3..." format.

SYNL-41 (error) Unable to read netlist '%s' for function reference '%s'.

DESCRIPTION

The specified netlist (through the "use_netlist" pragma) is not found (or has no read permission) in the search path.

WHAT NEXT

Check the permission and/or the location of the specified netlist.

SYNL-42 (error) Unable to find design '%s' in the specified file '%s' for function reference '%s'.

DESCRIPTION

The specified design (through the "use_netlist" pragma) is not found in the netlist db file.

WHAT NEXT

Make sure that the design in the specified netlist db has the same prefix as the

netlist db file.

SYNL-43 (error) Design '%' contains generic logic element '%s' which is not allowed in an encapsulated function.

DESCRIPTION

The external netlist that is refered to in the encapsulated function contains generic (unmapped) element. The current release does not support these types of components.

WHAT NEXT

Make sure that all cells in the netlist are mapped by compiling the design.

SYNL-44 (error) Design '%' contains synthetic component '%s' which is not allowed in an encapsulated function.

DESCRIPTION

The external netlist that is refered to in the encapsulated function contains unmapped synthetic component. The current release does not support these types of components.

WHAT NEXT

Make sure that all cells in the netlist are mapped by compiling the design.

SYNL-45 (error) Design '%' contains hierarchical component '%s' which is not allowed in an encapsulated function.

DESCRIPTION

The external netlist that is refered to in the encapsulated function contains hierarchical component. The current release does not support these types of

components.

WHAT NEXT

Make sure that all hierarchical cells in the netlist are flatten (ungrouped).

SYNL-46 (error) Unable to find function design '%s' for reference '%s' in '%s' root.

DESCRIPTION

The function design has either been deleted or renamed.

WHAT NEXT

If the function design is deleted, it must be recreated and relinked. If it is renamed to a different name, it must be renamed to match the design name and relinked.

SYNL-47 (error) Function '%s' does not have all required attributes of an encapsulated function. Therefore, this function will not be treated as a synthetic operator; It will remain to be just a hierarchical component.

DESCRIPTION

Some required attributes of the encapsulated function are missing. This function will remain to be just a hierarchical component.

WHAT NEXT

SYNL-48 (warning) Binding '%s' in module '%s' cannot be bound to

preserved function operator ’%s’. Binding is ignored.

DESCRIPTION

The binding of a static module (that is defined in a synthetic library) specifies a preserved function operator as bound operator - which is illegal. This error is typically occurred when converting an existing function/subprogram from being a designware component to become a preserved function. This binding is ignored.

WHAT NEXT

Remove the offended binding from the library on the synthetic library and link library lists.

SYNL-49 (warning) External binding ’%s’ in library ’%s’ cannot be
associated with preserved function module ’%s’. Binding is ignored.

DESCRIPTION

This external binding is associated to a module that is reserved for a preserved function. This error is typically occurred when converting an existing function/ subprogram from being a designware component to become a preserved function. This binding is ignored.

WHAT NEXT

Remove the offended binding from the library on the synthetic library and link library lists.

SYNL-52 (error) Unable to obtain DesignWare license to generate
synthetic parts.

DESCRIPTION

You specified DesignWare synthetic library in your synthetic_library list. And the licensed DesignWare building blocks might be used by the design. A DesignWare Foundation license must be available to enable licensed DesignWare componentent in

the design.

WHAT NEXT

Use the variable synlib_wait_for_design_license to enable DC to wait for a Foundation license when they are all in use.

Remove synthetic libraries contain Foundation parts from your synthetic library line.

SYNL-54 (error) No technology library is specified for mce generator to build netlist. Terminate the process.

DESCRIPTION

MCE generator needs to have at least one technology library specified for synthesis. Normally the technology libraries are the ones in target_library list. But mce doesn’t handle gtech library.

WHAT NEXT

Make sure target_library list is set and contains mce compatible technology libraries.

SYNL-55 (warning) Unable to obtain DesignWare-LP license to use the low power DesignWare implementation ’%s’.

DESCRIPTION

You specified DesignWare low power synthetic library in your synthetic_library list. And the low power DesignWare implementations might be used by the design. However you do not have the DesignWare-LP license to use the low power DesignWare building blocks. A DesignWare-LP license must be available to enable licensed low power DesignWare implementations in the design. The low power implementations will not be considered during compile.

WHAT NEXT

In order to utilize the low power DesignWare implementations, please obtain the DesignWare-LP license.

SYNOPT-1 (warning) Cache element %s could not be written.

DESCRIPTION

An error occurred while trying to write a cache element to the specified file. This is most likely due to file permissions problems, system's limitation on file name, or a full disk.

WHAT NEXT

Resolve the problem with the specified file/directory and try the failing command again.

SYNOPT-2 (warning) Port %s of synthetic library part %s has invalid direction.

DESCRIPTION

WHAT NEXT

SYNOPT-3 (warning) Synthetic library models may be inaccurate because
wire load information is not available from the technology library (ie: did not find wire_load_from_area or default_wire_load statement in library).
User may want to remove from the cache the models created during this compile command.

DESCRIPTION

Models in the cache will not be as accurate as they could have been if wire load information had been available. For that reason it is a good idea not to keep them around.

WHAT NEXT

Remove the models and (ideally) investigate why there is no wire load data available from the technology library.

SYNOPT-4 (warning) Improper octal value for variable cache_file_chmod_octal or cache_dir_chmod_octal: %s

DESCRIPTION

The value specified for either cache_file_chmod_octal or cache_dir_chmod_octal was invalid. These values are used to set the directory and file permissions on directories and files created inside of a Synopsys cache. The values must be octal numbers and less than 0777 for file permissions and less than 01777 for directory permissions.

WHAT NEXT

Check the values of these two variables and update them so that they have valid values.

SYNOPT-5 (warning) Cannot chmod the cache file or directory %s

DESCRIPTION

After creating the specified directory, an attempt was made to chmod it to the permissions specified by the cache_dir_chmod_octal variable. The chmod system call failed.

WHAT NEXT

Fix the problem that prevented the chmod from succeeding if possible. Otherwise try creating the directory and setting the permissions manually.

SYNOPT-6 (warning) The synthetic library 'optimize' parameter value '%s' is not supported.

A parameter value of ’fastest’ will be used.

DESCRIPTION

WHAT NEXT

SYNOPT-7 (warning) The value ’scaled_to_fastest’ for the synthetic library ’optimize’ parameter requires the ’scaled_to_fastest_scale’ parameter to be set. A default value of 1.1 will be used.

DESCRIPTION

WHAT NEXT

SYNOPT-8 (information) Wrote %s as a cache element.

DESCRIPTION

Indicates that the specified design was written to the current Synopsys cache.

WHAT NEXT

No action is required as this is just an information message.

SYNOPT-9 (information) Read %s as a cache element.

DESCRIPTION

Indicates that the specified design was read from the current Synopsys cache.

WHAT NEXT

No action is required as this is just an information message.

SYNOPT-10 (warning) The cache_read directory %s is not readable.

DESCRIPTION

The cache_read variable is supposed to contain a set of directory names. These names indicate locations of Synopsys caches which are to be searched when a cached part is required. The specified directory name was found to be unreadable.

WHAT NEXT

Remove or correct the offending directory name in the cache_read variable. If the directory name is correct and the directory does exist, make sure the permissions are such that the directory can be read from.

SYNOPT-11 (warning) The cache_write directory %s is not writable.
So, no cache elements can be written.

DESCRIPTION

The cache_write variable is supposed to contain a directory name. The named directory is supposed to indicate the root of a Synopsys cache to which cached designs are to be written. The specified directory name was found to be unwritable.

WHAT NEXT

Correct the offending directory name in the cache_write variable. If the directory name is correct and the directory does exist, make sure the permissions are such that the directory can be written to.

SYNOPT-12 (warning) Cannot open file %s for writing. Check directory mode bits.

DESCRIPTION

The specified file can not be opened for write due to permission problems on the directory the file resides in.

WHAT NEXT

```
Check the permission bits on the directory and make sure that you have write
permission.
```

SYNOPT-14 (warning) Synthetic library part ’%s’ does not have an ’optimize’ parameter.
The optimize value ’fastest’ will be used.

DESCRIPTION

WHAT NEXT

SYNOPT-15 (information) The cache entry ’%s’
is out of date with respect to its entry
in the design library ’%s’
(module ’%s’, implementation ’%s’).
The cache entry has been removed.

DESCRIPTION

```
A cache entry is tagged with a timestamps from the design library entry
 it was created from.
 If the design library is updated, then the cache entry
 may not be valid, so it is removed.
```

WHAT NEXT

SYNOPT-16 (warning) The cache entry ’%s’
should be removed, but the attempt to remove it has failed.
The entry should be removed because either it is corrupted
or it is out of date.
An entry can be out of date with respect to either its entry
in the design library ’%s’

(module '%s', implementation '%s')
or its target library '%s'.

DESCRIPTION

A cache entry is tagged with a timestamps from the design library entry
it was created from and a timestamp from the target library it was
created from.
If either of these is updated, then the cache entry
may not be valid, so it is removed.
Alternatively, if the cache entry is corrupted, it should be removed.
The attempt to remove it failed.
If it is not removed manually, it may cause the compile command
to take more time while it optimizes that synthetic library part.

WHAT NEXT

SYNOPT-17 (information) The cache entry '%s' is obsolete or has been corrupted, so it is being removed.

DESCRIPTION

The cache is a directory structure and the files in it have
a predefined format. The entry listed above does not conform
to the format.

WHAT NEXT

No action is necessary; the file has been removed.

SYNOPT-18 (information) The cache entry '%s' is out of date with respect to its target library '%s'. The cache entry has been removed.

DESCRIPTION

A cache entry is tagged with a timestamp from the target library it was
created from.
If the target library is updated, then the cache entry
may not be valid, so it is removed.

WHAT NEXT

SYNOPT-19 (warning) The cache entry '%s' should be removed, but the attempt to remove it has failed. The entry should be removed because either it is corrupted or it is out of date. The entry is out of date with respect to its entry in the design library '%s' (module '%s', implementation '%s').

DESCRIPTION

```
A cache entry is tagged with a timestamps from the design library entry
 it was created from.
 If the design library is updated, then the cache entry
 may not be valid, so it is removed.
 Alternatively, if the cache entry is corrupted, it should be removed.
 The attempt to remove it failed.
 If it is not removed manually, it may cause the compile command
 to take more time while it optimizes that synthetic library part.
```

WHAT NEXT

SYNOPT-20 (warning) The cache entry '%s' should be removed, but the attempt to remove it has failed. The entry should be removed because either it is corrupted or it is out of date. The entry is out of date with respect to its target library '%s'.

DESCRIPTION

```
A cache entry is tagged with a timestamp from the target library it was
 created from.
 If the target library is updated, then the cache entry
 may not be valid, so it is removed.
```

```
Alternatively, if the cache entry is corrupted, it should be removed.
The attempt to remove it failed.
If it is not removed manually, it may cause the compile command
to take more time while it optimizes that synthetic library part.
```

WHAT NEXT

SYNOPT-21 (warning) The cache_read variable should be a list variable,
but it was read as the string variable '%s'.

DESCRIPTION

```
There can be more than one directory to read from, so the cache_read variable
 is interpreted to be a list variable. But, the cache_read variable has been
 read as a string variable and will be converted to a one element list.
```

WHAT NEXT

```
The variable should be a list variable and its type should have been set
 by SYNOPSYS_ROOT + .synopsys_dc_setup. Check that this system file
 sets cache_read to a list variable.
```

SYNOPT-22 (information) The v3.3b cache element format has changed; removing cache entry
'%s'

DESCRIPTION

```
A new cache element will be built and cached.
```

WHAT NEXT

```
Nothing is required.
```

SYNOPT-23 (error) There are %d legal implementations for the sequential module '%s',
but the variable synlib_sequential_module is set to 'one_implementation_choice'.

DESCRIPTION

This message indicates that the variable **synlib_sequential_module** is set to *one_implementation_choice* on the specified sequential module, but in fact there is more than one legal implementation, as stated in the message. You must have only one implementation choice if you set **synlib_sequential_module** to *one_implementation_choice*. With *one_implementation_choice*, specific timing calculations can be skipped and the overall optimization can proceed significantly faster.

WHAT NEXT

Make the number of implementations agree with the value of **synlib_sequential_module**, in one of these two ways:

1. Ensure that there is only one legal implementation, using **set_implementation** or **set_dont_use**; or

2. Change the value of the variable **synlib_sequential_module** to another value. For information about other allowed values and their meanings, refer to the **synlib_sequential_module** manual page.

SYNOPT-24 (warning) The variable synlib_sequential_module is
no longer supported.

DESCRIPTION

This message warns you that the variable **synlib_sequential_module** is longer supported. Setting the variable will have no effect on the compile flow.

WHAT NEXT

Remove the variable from the dc script.

SYNOPT-25 (warning) The dont_touch on the synthetic library implementation '%s' (module '%s') will be ignored.

DESCRIPTION

A dont_touch attribute on a top-level design is ignored. When a synthetic library implementation is modelled, it is treated as a top-level design. Later in the compile process, the implementation is a sub-design and the dont_touch will be adhered to. One consequence of this is that the model may be inaccurate.

WHAT NEXT

Remove the dont_touch on the design and apply the dont_touch to the cells in the implementation that the user wants to be dont_touched.

SYNOPT-26 (information) The time stamp of the cache entry '%s' does not match the time stamp of its target library '%s'.

DESCRIPTION

You receive this message because a cache entry is tagged with a time stamp from the target library it was created from. If the target library is updated, the cache entry will no longer be valid.

WHAT NEXT

This is an informational message. No action is required on your part.

SEE ALSO

report_cache (2).

SYNOPT-27 (warning) The cache entry '%s' is corrupt or not readable and should be removed, but the attempt to remove it has failed.

DESCRIPTION

You receive this message because the cache entry is either not readable or has been

corrupted. Design Compiler (DC) could not read the cache element.

WHAT NEXT

Check the readability of the cache entry.

SYNOPT-28 (warning) Cell '%s' is not found in design, ignoring force hiis on this cell.

DESCRIPTION

You receive this message because an invalid cell name is specified in list synlib_hiis_force_on_cells. Force hierarchical incremental implementation selection will not be performed on invalid cells.

WHAT NEXT

Check to make sure all cells in synlib_hiis_force_on_cells list are valid.

SYNOPT-29 (information) The cache element for %s(%s) is not the optimal circuit. It is not used in the current design.

DESCRIPTION

Datapath optimization feature is enabled on the DesignWare RTL architectures in the current command. The cache element read in is not the optimal circuit. Discard this cache element and re-build the optimal circuit.

WHAT NEXT

No action is required as this is just an information message.

TDB

TDB-1 (error) Subrange direction does not match array declaration.

DESCRIPTION

WHAT NEXT

TEST-101 (error) No ports included in the BSR. A register consisting of a single shift-register stage must be provided.

DESCRIPTION

The JTAG Boundary Scan Register (BSR) associates a register with each I/O pad of a device. These registers can either 'capture' (observe) or 'apply' (control) values at the pads. The registers are serially chained together to form the BSR. Values are set and read serially through the BSR. Typically, all non-TAP (Test Access Port) ports are included in the BSR.

All non-TAP ports will be processed for inclusion in the BSR unless they have been explicitly excluded using the **set_jtag_port FALSE {port_list}** command.

Typically, excluding ports from the BSR is a *tolerable* violation of the IEEE 1149.1 standard that does not otherwise modify the structure of the JTAG logic. However, in the extreme case where either there are no ports to include in the BSR or *all* ports have been excluded from the BSR, Rule 10.2.1(i) of the standard applies. Rule 10.2.1(i) states that "In the event that no boundary-scan register cells are required for a component, a register consisting of a single shift-register stage shall be provided. NOTE- This situation will arise where a component only contains test logic as defined or permitted by this standard. Such a component could be described as being dedicated to testing; it will not contribute to the system function of an assembled board."

Designs that contain violations of the 1149.1 standard are referred to as non-compliant JTAG architectures. 1149.1 standard violations fall into two categories: *tolerable* and *intolerable*. We define *intolerable* violations as those that render the JTAG access protocol inoperable or which make the behavior of the JTAG logic unpredictable.

We define *tolerable* violations of the standard as those that neither render the JTAG access protocol inoperable nor make the behavior of the JTAG logic unpredictable, but which do violate some rule in the 1149.1 standard.

WHAT NEXT

Since the DFT Compiler JTAG synthesis capability does not currently support synthesis of the 'zero-length' BSR required by 10.2.1.(i), include at least one non-TAP port in the BSR. Use **set_jtag_port TRUE {port_list}** to establish such a condition.

To include all non-TAP ports in the BSR, execute **set_jtag_port TRUE find (port,"*")** on the current_design.

TEST-102 (information) GLOBAL tracing enabled for these nets in design '%s':

DESCRIPTION

BACKGROUND INFORMATION

Using the **check_test** command, DFT Compiler design rule checking (DRC) is performed by doing a symbolic simulation of the test protocol for a design.

If the data applied at the scan in ports is successfully and predictably loaded into the scan chain, the cells are scan controllable. If data can be captured into the scan cells during the parallel capture cycle, and successfully and predictably unloaded, the cells are scan observable. When sequential cells are neither fully scannable (both scan controllable and scan observable) nor valid nonscan cells (for partial scan designs), fault coverage suffers.

DFT Compiler provides a net tracing capability which allows you to view the results of the symbolic simulation to help in the identification and correction of test protocol problems. DFT Compiler displays the logic values of the nets as information messages. All output from the design rule checker, including information messages, is linked to the design schematic. You can debug your protocol by selecting nets with certain values, then viewing the corresponding section in the schematic through the Design Analyzer.

Net tracing is enabled in either of two fashions. If **trace_nets** *statements* are added to vector or stream groups within a custom test protocol supplied by the designer, they enable tracing within a *local* scope limited to that vector or stream group. Alternatively, by specifying nets using the **trace_nets** *command*, nets can be traced within the *global* scope of the entire current test protocol. The **untrace_nets** command only acts on nets specified by the **trace_nets** command.

MANIFESTATION

This information message is generated to indicate that one or more nets specified by the **trace_nets** command will undergo *gobal* tracing during DRC of the currently active test protocol.

WHAT NEXT

If you do not want *global* net tracing for one or more of the nets listed (TEST-103), disable net tracing for them using the **untrace_nets** command.

TEST-103 (information) Output port '%s' is a user-specified three-state

enable signal requiring a BSR control cell.

DESCRIPTION

When the three-state elements driving three-state and bidirectional *outputs* are found in the core logic of the IC (i.e. not embedded in the pads themselves) DFT Compiler requires that these three-state elements be located at the top hierarchy of the core of the design so that Boundary Scan Register (BSR) cells can be placed on the **inside** of the three-state elements in order to control and observe the data and enable lines. In these cases, only a single three-state line exits the core logic.

However, in the cases where the three-state controller for output signals will be embedded in the three-state output or bidirectional input/ouput *pad* associated with these ports of a design two signals exit the core logic; a *data* line and an *enable* line. Unless, TC knows the distinction between these two types of exit lines, it will always assume that they are data lines and not insert the correct type of BSR cell on the enable lines. By specifying "enable" or "data" on a port the designer instructs TC on which type of BSR cell to place on these output ports. It is the responsability of the designer to correctly connect these signals to the proper pads in a post-processing step of adding pads to the design.

This information message is produced when an output port has been specified by the designer to be the enable signal for a three-state ouput or bidirectional pad.

WHAT NEXT

The designer must exercise caution to connect the proper data and enable signals to the three-state and bidirectional pads of the design.

TEST-104 (information) Nets '%s' have been specified for LOCAL tracing during this vector or stream simulation.

DESCRIPTION

BACKGROUND INFORMATION

Using the **check_test** command, DFT Compiler design rule checking (DRC) is performed by doing a symbolic simulation of the test protocol for a design.

If the data applied at the scan in ports is successfully and predictably loaded into the scan chain, the cells are scan controllable. If data can be captured into the scan cells during the parallel capture cycle, and successfully and predictably unloaded, the cells are scan observable. When sequential cells are neither fully scannable (both scan controllable and scan observable) nor valid nonscan cells (for partial scan designs), fault coverage suffers.

DFT Compiler provides a net tracing capability which allows you to view the results of the symbolic simulation to help in the identification and correction of test

protocol problems. DFT Compiler displays the logic values of the nets as information messages. All output from the design rule checker, including information messages, is linked to the design schematic. You can debug your protocol by selecting nets with certain values, then viewing the corresponding section in the schematic through the Design Analyzer.

Net tracing is enabled in either of two fashions. If **trace_nets** *statements* are added to vector or stream groups within a custom test protocol supplied by the designer, they enable tracing within a *local* scope limited to that vector or stream group. Alternatively, by specifying nets using the **trace_nets** *command*, nets can be traced within the *global* scope of the entire current test protocol. The **untrace_nets** command only acts on nets specified by the **trace_nets** command.

MANIFESTATION

This information message is generated to indicate that, using a **trace_nets statement**, the specified nets have been marked for **LOCAL** tracing within the current vector or stream.

WHAT NEXT

This message is generated because in some cases simulation of the target vector or stream does not produce any activity on the specified net. In such cases, in the absense of additional tracing information, it is useful to know that the net was in fact explicitly targeted for local tracing.

TEST-105 (information) Driven port '%s' characteristic '%s' changed to driving port '%s' characteristic '%s' due to BSR cell optimization.

DESCRIPTION

When DFT Compiler executes IEEE 1149.1 Standard mandated Boundary Scan Register optimizations, BSR cell optimization can push the BSR cell associated with an output (*Bdriven*) onto an input port (*Bdriving*). In these cases, it is possible that the BSR cell characteristics specified for the output port no longer coorespond with the BSR cell implementation serving that port if the characteristics specified for the input port and the output port BSR cells differed.

This information message is produced when such a difference has been encountered and reports those differences.

WHAT NEXT

If the characteristics of the optimized BSR register no longer meet your needs, set the BSR cell characteristics of the driving port to be those of the driven port.

TEST-106 (error) Critical missing connection(s) encountered while processing bidirectional port ‘%s’.

DESCRIPTION

DFT Compiler has encountered at least one missing connection while processing the designated bidirectional port. Bidirectional I/O ports must be connected to a net that both drives the port in output mode and is driven in input mode.

During boundary scan synthesis, three BSR cells must be associated with each bidirectional port: one with its input mode and two with its output mode.

This error message is generated when one or both of these net connections is missing. One possible cause is that the net could be connected to an unresolved reference. DFT Compiler has generated this error message and gracefully aborted JTAG synthesis.

WHAT NEXT

Run the dc_shell **link** command to get a list of unresolved references and fix the critical ones. Otherwise, verify that this port is indeed supposed to be bidirectional, and verify its connectivity.

TEST-107 (error) Port ‘%s‘ can not be a TAP TDO. It is not an output port.

DESCRIPTION

The **insert_jtag** command lets you select TDO ports using **jtag_tdo signal_type** attributes. You must identify output ports as TDO ports.

You see this message when you select input or bidirectional ports as TDO ports. The **insert_jtag** command aborts.

WHAT NEXT

Use the **remove_attribute** command to remove the **signal_type** attribute from the offending port. Choose another design port.

TEST-108 (Warning) Internal failure: scan equivalence could not

create a pseudo-hierarchy for cell %s/%s.

DESCRIPTION

Scan equivalence generates this warning when it fails to create the pseudo-hierarchy it uses to constrain sequential-mapping based scan equivalence. This is an internal problem and should be handled gracefully, but should be reported to Synopsys R&D for further diagnosis.

WHAT NEXT

Study tool output for additional errors and warnings that involve the cell. Use check_test to establish whether insert_scan scan replaces the cell and includes it in a scan chain. File a Synopsys Technical Action Request, if at all possible.

TEST-109 (warning) Design '%s' has invalid scan chain information.

DESCRIPTION

This message tells you that **report_test -scan_path** produces invalid scan chain information for a design. Hierarchical scan insertion uses this information to infer that there are scan segments in the design. Invalid information confuses this process.

You can use **check_test** to restore the scan chain information. It is important that you do this before using **insert_scan** to attempt hierarchical scan operations.

WHAT NEXT

Run **check_test** on the design to restore scan chain information.

TEST-110 (warning) Cell %s of type %s is not a test cell.

DESCRIPTION

This message indicates that the cell in question is not defined as a test cell in the target library. A test cell must be declared with the keyword test_cell().

WHAT NEXT

Check your library description.

TEST-111 (warning) Test cell %s of type %s is not consistent with the methodology.

DESCRIPTION

WHAT NEXT

TEST-112 (warning) Cell %s (%s) is unknown (black box).

DESCRIPTION

This message identifies a cell for which no functional model exists. DFT Compiler needs a functional model for every type of cell used in a design so it can generate test patterns and calculate fault coverage. DFT Compiler treats a cell without a functional model as a *black-box*, which means that faults on the pins of the cell and the surrounding circuitry are untestable. Depending on the number and location of such cells, the effect on overall fault coverage may or may not be significant.

WHAT NEXT

This message appears when a model exists for the cell in a Synopsys library file, but the model does not contain any functional information. Add the functional model with the **function** statement. For sequential cells, use the **state** group and related statements.

This message also appears when the cell is an unresolved reference, which means no description of the design referenced by the cell could be found when the design was linked. Use the **check_design** command to locate unresolved references.

To see whether the incorrect library was used when the design was linked, check the **link_library** variable. Check the **search_path** variable to see whether a library was omitted or not located.

If the message refers to a simple cell that was not included in any library, try developing a model and adding it to the library.

For complex cells, the functional model is more involved. For example, the cell may be a RAM, microprocessor core or some other type of embedded hierarchical block. In such situations, you may want to develop an abstract functional model for the cell in VHDL or Verilog. Read these models in so they can be used for test pattern generation. Alhough DFT Compiler cannot develop test patterns for the circuitry within the cell, the surrounding logic can be tested.

TEST-113 (information) Cell %s (%s) is generic.

DESCRIPTION

This message identifies a generic logic cell in the design. A generic logic cell represents an abstract logical function before it is mapped into a target technology library. Generic logic is generated after a functional description of a design is read in, and before the **compile** command synthesizes an implementation of the design from the target technology library.

If your design has generic logic cells, you can still use most of DFT Compiler, but your results will not be valid for the final (synthesized) design. For example, you can run the **check_test** command on designs with generic logic, and DFT Compiler will correctly identify scan design-rule violations.

You can also run the **create_test_patterns** command on designs with generic logic. However, since test pattern generation considers "stuck-at" faults on physical cell pins, the test patterns for the generic logic will be meaningless. If patterns are generated for designs that have generic logic, the faults considered will not correspond to the defects that may occur in the manufacture of the chip. Consequently, the generated patterns are not valid, and the reported fault coverage only approximates the possible fault coverage for the final design.

However, you cannot perform partial scan insertion using the **insert_test** command since generic cells have no scan equivalent and no area or timing information. This type of information is essential to make meaningful testability trade-off analysis.

Note: DFT Compiler reports only the first generic logic cell it finds.

WHAT NEXT

Use the **compile** command to map generic logic cells into cells from the selected technology library.

TEST-114 (warning) Type of wired net %s is unknown.

DESCRIPTION

The test design rule checker has encountered a wired (multiple-driver) net whose function is not understood. (That is the net is not a wired-AND, wired-OR or three-state net.) The values on such nets can not be predicted for the purposes of automatic test pattern generation. This means faults on the cells driving the net and driven by the net will not be testable. In addition the test design rule checker may generate further warnings as a consequence of being unable to understand the behavior of the net. For example any clock signals driven by the net will become unknown.

WHAT NEXT

You should always check messages of this form. They may be related to features of the original design description or the library in use. For example a missing library model may cause a cell to appear as a "black-box" which could give rise to problems if it was connected to a wired-net.

TEST-115 (warning) Three-state net %s is not properly driven.

DESCRIPTION

The value of a three-state node is unpredictable if that node is driven by a non-three-state driver. If there are multiple drivers, and one or more of them are not three-state drivers, bus contention or bus float can occur.

The DFT Compiler design rule checking (DRC) rigidly checks for this type of violation and generates this warning message when it encounters such a condition. You will also see an informational message immediately after this message to indicate where the problem lies.

If the problem is an incorrect design, you will see either a TEST-180 or TEST-182 message, which will indicate the problem cell or port.

However, you will also see the TEST-115 message in the following cases:

- When a RAM cell is driving a three-state bus. If the three-state driver is internal to the RAM cell, **dft_drc** will not recognize the function of the RAM cell and then issues the warning. You will see a TEST-199 message in this case.

- When the driver cell is a black box (not supported by DFT Compiler or has no reference in the working libraries) or was subject to another violation. Again you will see a TEST-199 message in these cases.

- When the **set_test_isolate** command is applied on a three-state driver’s instance or output pin. Such a command is used to indicate to DFT Compiler that a cell or a pin has an unknown value during test. It has the effect of logically cutting the nets at a pin or around a cell. The test_isolated driver then behaves like an x-generator on the three-state net. In this case you will also see a TEST-198 message.

WHAT NEXT

Determine the cause for the existence of the non-three-state driver and eliminate it. See the appropriate man page for TEST-180, TEST-182, TEST-198, or TEST-199 for more detailed information.

When **dft_drc** finds a TEST-115 violation on a three-state net, in a scan-routed design, by default ATPG may not run because of the high risk of producing wrong patterns. However, in a pre-scan design ATPG will run, because it does not generate any patterns that can be saved and so there is no risk of you handing off bad patterns. However, be aware that your fault coverage can be extremely low if there are TEST-115 violations on a key bus in your design.

TEST-116 (warning) Asynchronous pins of cell %s (%s) are uncontrollable.

DESCRIPTION

When scan data is shifted in and out of the design-under-test, the asynchronous preset and clear pins of sequential cells must be held in an inactive state. The test design rule checker tries to derive a set of values to apply at the external ports of the design to ensure this condition is met. For the reported cell, no such values could be found to force the asynchronous preset and clear pins to inactive values. This problem usually occurs when the asynchronous preset or clear signal is generated from the state of other sequential devices, as with an asynchronously resetting counter.

WHAT NEXT

To maximize fault coverage, try to make all internal asynchronous preset and clear pins externally controllable. You can do this by introducing additional logic to disable internal preset and clear signals either throughout testing or just during scan shift.

TEST-117 (warning) Combinational feedback loop broken at pin %s of cell %s (%s).

DESCRIPTION

Test design rule checking has identified a combinational feedback loop in the design. Such loops introduce uncontrollable states, so faults in the region of the loop, and specifically faults at the cell pin specified in the message cannot be tested.

This violation usually has only a minor impact on overall fault coverage. However, in some cases the testability of other parts of the design is significantly reduced. For example, if the untestable loop circuitry controls the enables for a three-state bus, fault coverage suffers because the outputs on the bus are unpredictable. If the loop circuitry controls the asynchronous preset or clear inputs of a number of sequential cells, these inputs cannot be rendered inactive during test pattern generation, so the sequential cells are also untestable.

WHAT NEXT

Establish the impact of the combinational feedback loop on the total possible fault coverage for the design with the **create_test_patterns** command, which generates a fault coverage report. If the effect is significant, you can try to redesign the circuitry to remove the loop.

TEST-118 (warning) The design contains unreachable circuitry (closed loops).

DESCRIPTION

Test design rule checking has identified redundant gates that are not connected to other gates, or to the outputs of the design. Such circuitry typically forms a closed loop. Closed loops are untestable and result in reduced fault coverage for the overall design.

WHAT NEXT

Since redundant gates have no purpose, you may want to remove them from the design.

TEST-120 (warning) No scan equivalent exists for cell %s (%s).

DESCRIPTION

In the scan design technique, the state of internal sequential cells must be easily controllable and observable. DFT Compiler automatically replaces sequential cells with functionally equivalent cells that also perform a scan shift function. These cells are connected into chains through which their states can be controlled and observed.

This message identifies a cell for which no equivalent scan cell can be found in the library for the given scan style. Either the library does not contain scan cells, or it contains scan cells that do not functionally match the cell in question.

For a full-scan design, all cells of the type listed in the warning message are treated as *black boxes*. Therefore, faults on these cells and in the surrounding circuitry are not testable.

For a partial-scan design, the impact is less severe. Because the constraints you set for area, performance, and fault coverage determine which cells should be replaced with their scannable equivalents, DFT Compiler is limited to choosing only those cells for which a scannable equivalent exists. If other cells in the design can be scanned, this usually does not significantly affect overall fault coverage.

WHAT NEXT

If your design has many cells for which scan equivalents do not exist, you should modify the design so you can achieve high fault coverage, particularly for a full-scan design.

If your library has no scan cells, you may want to work with your ASIC vendor to add scan cells.

If your library has scan cells, but none functionally match the cells you are using, you can either try an alternative scan style or use different types of sequential cells.

You can use Design Compiler to translate the sequential cells in the design into different sequential cells, together with associated logic.

TEST-121 (warning) Cell %s (%s) can't be made scannable because it is dont_touched.

DESCRIPTION

If you set the dont_touch attribute on a cell in your design, that cell is not modified or replaced when you optimize the design with the compile command.

The **insert_scan** command also respects the **dont_touch** command during both scan replacement and design optimization. However, sequential cells that are both scan replaced and have a dont_touch attribute will be routed onto scan chains by **insert_scan**.

The **check_test** command issues this message (TEST-121) when it finds a nonscan replaced sequential element that has a dont_touch attribute.

WHAT NEXT

If you don't want **insert_scan** to scan replace or to optimize the sequential cell, no action is necessary.

If you don't want **insert_scan** to scan replace, but you want to optimize the sequential cell during the constraint violation fixing phase, remove the dont_touch attribute and use **set_scan_element false**.

If you want **insert_scan** to scan replace a particular sequential cell, but not to optimize the scan replacement, yet still allow global optimization, you need to use two passes of **insert_scan**. First remove the dont_touch attribute and run **insert_scan** with all user defined constraint violation fixing and compile design rule fixing disabled. Then, reapply the dont_touch attribute and run a second pass of **insert_scan** to fix user defined constraint violations and compile design rule violations *only*. The following script shows you how to do this.

```
remove_attribute inst1/dff1 dont_touch test_dont_fix_constraint_violations = true
check_test preview_scan insert_scan -ignore_compile_design_rules check_test

set_scan_configuration -replace false -route false
test_dont_fix_constraint_violations = false set_dont_touch inst1/dff1 check_test
preview_scan insert_scan check_test
```

An alternative approach is to run an incremental compile instead of the second pass of **insert_scan**. However, if your pre-scan design is constraint violation free, using **insert_scan** rather than **compile -incremental** to fix constraint violations introduced

by adding scan will run faster.

TEST-122 (warning) Cell %s (%s) is an unsupported complex latch.

DESCRIPTION

This message identifies a latch cell whose behavior is too complex to understand. Such a cell is treated as a *black box* for the purposes of test pattern generation. As a result, faults on the cell and the surrounding circuitry are untestable.

The scan design technique requires that the state of sequential cells (flip-flops and latches) can be controlled and observed. Therefore, the behavior of the cells must be readily understood. For example, clock pins and data pins must be identified. A *complex* latch is one with data, enable *and* asynchronous set or clear pins, whose behavior is not easily understood.

WHAT NEXT

If there are relatively few of these cells in the design, the impact on overall fault coverage is minor. If you can, place the latches in transparent mode for the purposes of testing.

If your design has many of these latches, you may need to modify the design. You could replace the complex latches with simple D-type latches and associated circuitry using Design Compiler. Design Compiler translates the complex latches into functionally equivalent simpler latches and combinational gates.

TEST-123 (information) Test design rule checking completed.

DESCRIPTION

The test design rule checking (DRC) command issues this message when it completes checking the current design against the test design rules of the scan test implementation, specified by the **set_scan_configuration** (-style and -methodology options) command.

WHAT NEXT

Read the Test Design Rule Violation Summary and the Sequential Cell Summary at the end of the test DRC report. If there are any violations, you need to understand the violations and their causes before you proceed. Either fix the violations or decide that you can accept the violation before you proceed. To understand the violations, read the two Summaries and the more detailed information generated by the test DRC command. If you need details of all the violations found by test DRC, rerun test DRC in verbose mode (-verbose option).

It is very important that you do not proceed to scan insertion or to ATPG without checking the violations reported by test DRC.

TEST-124 (warning) Violations occurred during test design rule checking.

DESCRIPTION

If the test design rule checking (DRC) information is out of date, **preview_scan** and **insert_scan** invoke the test design rule checking. The test DRC checks the current design against the test design rules of the scan test implementation specified by the **set_scan_configuration** (-style and -methodology options) command. When the test DRC completes, it issues this message if it found any violations. However, the **preview_scan** and **insert_scan** commands will continue to execute.

WHAT NEXT

It is very important that you do not proceed to scan insertion or to ATPG without checking the violations found by the test DRC.

If you did not run test DRC explicitly and the scan insertion or ATPG are unsatisfactory, run test DRC explicitly. Then read the Test Design Rule Violation Summary and the Sequential Cell Summary at the end of the test DRC report. If there are any violations, you need to understand the violations and their causes before you proceed. Either fix the violations or decide that you can accept the violation before you proceed. To understand the violations, read the two Summaries and the more detailed information generated by the test DRC command. If you need details of all the violations found by test DRC, rerun test DRC in verbose mode (-verbose option).

It is a much better practice to run test DRC explicitly and to read the violation reports before you run **preview_scan** or **insert_scan**. Because **preview_scan** and **insert_scan** only run test DRC if you have not run it explicitly, you do not save any time by not running test DRC explicitly.

TEST-125 (warning) Clock/enable pin %s of cell %s (%s) tied constant.

DESCRIPTION

During scan shift, the clock/enable pin is tied to a constant value.

WHAT NEXT

This may be due either to the clock/enable being held to a constant value or to the

clock/enable being gated by a *test_scan_enable* signal. If you find that the clock is not tied to a constant value, look at the *test_scan_enable* and *test_scan_enable_inverted* signals to see if they hold the clock/enable at a constant value during scan shift.

TEST-126 (warning) Cell %s (%s) is not scannable.

DESCRIPTION

In the scan design technique, the state of internal sequential cells must be easily controllable and observable. By default, DFT Compiler automatically replaces sequential cells with functionally equivalent cells that also perform a scan shift function. These cells are connected into chains through which their states can be controlled and observed.

You can also decide not to perform scan replacement if your design has already gone through this process. This control is available through *-replace* option of the *set_scan_configuration* command.

This message identifies a cell that is not scannable, that is, it cannot be part of any scan chain. This happens when you explicitly set *-replace* option of the *set_scan_configuration* to FALSE, and you have one of the following two situations: i) the cell has not been scan replaced yet, or ii) the cell is scan replaced but with a different scan style than the one being used.

WHAT NEXT

You can ignore the message and leave the cell as a valid non-scan cell, not being part of any scan chain. You can also opt for scan replacement (set *replace* to TRUE) and rerun the *dft_drc* command.

TEST-130 (warning) Clock gating cell %s has unconnected test pin.

DESCRIPTION

The reported clock gating cell has an unconnected test pin. *dft_drc* will check to ensure that the register bank driven by this clock gating cell is not DRC violated and gets scan stitched. If the *set_dft_configuration -connect_clock_gating* is enabled (default behavior), *insert_dft* will connect the test pin to the appropriate ScanEnable or TestMode port. Test pins are not connected until *insert_dft* is run. If left unconnected (or -connect_clock_gating is disabled at the time of insert_dft), then Post-DFT DRC will report a violations for the register bank driven by this clock gating cell.

This message is issued irrespective of the *set_dft_configuration* -

connect_clock_gating feature being enabled or disabled.

WHAT NEXT

This message is primarily an information for user. If the set_dft_configuration -connect_clock_gating feature is enabled, then insert_dft will connect the appropriate test pin to the test signal. No further action is required from the user. However, if the user disables the feature, insert_dft will not make the connection and the cells being driven by the clock gating cell will not be put in the scan chain. The user can either enable the feature or choose to have these cells Auto-fixed thereby bypassing the Clock Gating cell. The cells will then be included on the scan chain.

SEE ALSO

set_dft_configuration(2)
report_dft_configuration(2)
set_dft_signal(2)

TEST-131 (warning) Data pin %s of cell %s (%s) is driven by a clock/enable signal.

DESCRIPTION

This message identifies a pin whose value is sensitive to the state of a clock signal. Faults on that pin, and in the logic in the immediate fanout of the pin and cell, are not testable. The message that follows this one lists the pins that comprise the clock network for the signal in question.

The scan design technique requires that *clock* signals must not drive, either directly or indirectly, the data pins of sequential cells or output ports of the design. This restriction ensures that automatic test pattern generation can correctly predict the test response values that are captured into sequential cells or observed at primary outputs. If these response values are sensitive to clock transitions (rising and falling edges), the captured or observed values cannot be reliably predicted.

WHAT NEXT

You should always check violations of this form to ensure that the violations are not design errors. In general, you should redesign the circuitry to avoid such violations.

This type of rule violation typically has only a local effect on fault coverage. Unless many pins are affected, the impact on overall fault coverage may not be significant.

TEST-132 (Warning) Sequential cell %s (%s) is a black box in combinational scan style

DESCRIPTION

In combinational scan style, clocks are not pulsed. Therefore, sequential cells cannot be used for testing. They are black-boxed.

WHAT NEXT

Even if no scan chain is present, either use a non-combinational scan style (multiplexed flip-flop, LSSD or clocked scan), or use a full scan methodology.

TEST-135 (information) Clock port %s captures data on both edges.

DESCRIPTION

This message indicates that for the identified clock ports, data is captured into sequential cells (flip-flops or latches) on both the rising and falling transitions of the clock signal. That is, there are either flip-flops sensitive to both edges or there are latches that become transparent on both levels of the clock.

This design practice is supported by DFT Compiler, but it can cause some testability problems so be careful using it. Specifically, any state changes caused by the first clock edge cannot affect the data captured on the second clock edge. If this problem occurs, DFT Compiler issues a warning of unreliable capture (TEST-478) or a warning that cells do not cature (TEST-310).

WHAT NEXT

If no warning messages are issued, and you intended to capture data on both edges, you can ignore this message. If you do get subsequent warning messages, you might want to review the use of both clock edges.

TEST-140 (warning) The clock signal to cell %s (%s) is illegally gated.

DESCRIPTION

During the parallel cycle of the scan-test sequence, the response of internal combinational logic to the applied test pattern is captured into the sequential

cells in the design. This is usually done by applying a system (normal operation) clock pulse.

To ensure that data is reliably captured, all clock gating conditions must remain stable while the clock pulse is applied. In this case, the gating condition for the clock of the identified cell is itself changed when the clock pulse is applied. That is, the gating condition depends on the state of cells that have the same clock as the identified cell.

The message following this one indicates an example of a path by which the gating condition is changed at the time the clock pulse is applied.

The impact of this rule violation is that the specified cell cannot be used to observe the combinational logic block driving it. This results in lower fault coverage at the cell, and in the driving logic network.

WHAT NEXT

If your design has many cells with illegally gated clock signals, you should ensure that your design has been correctly constructed. Problems of this type may also affect the reliable normal operation of your design, as gated clock pulses may be truncated, causing glitches.

If you must gate clocks, you may want to consider alternative implementations that would be more reliable. One option would be to delay the change in the clock gating condition during the time the clock is active (typically high). You can add a delay by inserting a latch that is transparent only when the clock signal is at an inactive level (typically low).

Another alternative is to change the sense of the clock pulse and the gating logic, so that changes in the gating condition only occur when the clock is returning to the inactive level (which is high, due to the sense change).

TEST-141 (warning) There is an illegal path to cell %s (%s).

DESCRIPTION

During the parallel cycle of the scan-test sequence, the response of internal combinational logic to the applied test pattern is captured into the sequential cells in the design. This is usually done by applying a system (normal operation) clock pulse.

To ensure that data is reliably captured, the values being captured must remain stable for a certain length of time. For latch-based designs in particular, the data being captured must remain stable throughout the time the latch is transparent (the duration of the clock pulse).

This message indicates that data values being captured into the specified cell change before they can be latched. This usually happens because the sequential cell which is the origin of the data is being clocked at the same time as the specified cell. For example, if there is a path between two transparent latches with a common

latch enable signal, data cannot be reliably passed between the two latches. In this case, the data would fall through the second latch.

The message following this one gives an example of a path where the data value being captured changes when the clock pulse is applied.

The impact of this rule violation is that the specified cell cannot be used to observe the combinational logic block driving it. This results in lower fault coverage at the cell, and in the driving logic network.

WHAT NEXT

If your design has many cells with illegal data paths, you should ensure that your design has been correctly constructed. Problems of this type may also affect the reliable normal operation of your design.

You can resolve this problem by ensuring that different clock signals are used for different sequential elements, or by replacing level-sensitive elements (latches) with edge-triggered elements (flip-flops).

TEST-142 (warning) Sequential cell %s (%s) has constant logic 1/0 state.

DESCRIPTION

The scan-test approach requires that the state of the sequential cells in the design can be set to different values to enable thorough testing of the design's combinational logic. (This applies to both full-scan and partial-scan designs, although with partial scan, an initialization sequence may be required.)

This message identifies a sequential cell whose state, for the purposes of testing, is held at a constant logic 1 or logic 0 value. This means that some faults associated with the cell and the surrounding combinational logic cannot be tested.

This situation arises for designs with on-chip test control logic that is set to a specific state to enable scan-testing. One example is a JTAG TAP controller.

WHAT NEXT

If you expect the cell to be at a constant state (such as when it is part of some on-chip test control logic), you can ignore this message. In this case, you should supplement the automatically-generated test patterns with functional patterns that exercise the test control logic.

If this message is unexpected, examine the circuitry surrounding the specified cell to determine why the cell's state is constant during scan-test. For example, check whether the data input pin is tied high or low.

TEST-143 (error) Dont_touch has been applied to three-state cell ‘%s‘.
JTAG synthesis cannot proceed since Boundary Scan Register (BSR) cells
cannot be associated with this three-stated port.

DESCRIPTION

During JTAG synthesis, BSR cells are associated with ports of the design. Where ports are controlled by three-state cells, the BSR cells are connected before the inputs to these three-states. In some cases, complex three-state cells from the original design must be mapped into simpler logic constructs, in order to be compliant with the IEEE 1149.1 JTAG standard. If the *dont_touch* command has been executed on a three-state associated with a port to be included in the BSR, then the BSR cells cannot be attached to it and the synthesized JTAG would be non-compliant. This error message is generated when such a dont_touch three-state cell has been encountered.

WHAT NEXT

Remove the dont_touch attribute using the *remove_attribute* command.

TEST-144 (error) Encountered critical unresolved reference trying to
process cell ‘%s’.

DESCRIPTION

DFT Compiler has come across an unresolved reference during its traversal of portions of the design. It makes the traversal to determine where to insert JTAG boundary scan register (BSR) cells. In particular, it must recognize any three-state devices associated with design I/O. Having come across an unresolved reference, DFT Compiler has generated this error message and terminated JTAG synthesis.

WHAT NEXT

Run the dc_shell **link** command to get a list of unresolved references. Fix the critical ones.

TEST-145 (Warning) Pad-mapped JTAG is not IEEE 1149.1

compliant for port ‘%s‘.
Cell ‘%s‘ (library cell type ‘%s‘) has been inserted between the port pad
cell and the Boundary Scan Register (BSR) cell.

DESCRIPTION

You receive this message because Rule 10.1.1(a) of the IEEE 1149.1 JTAG Standard has been violated.

When JTAG synthesis is invoked with pad mapping, DFT Compiler attempts to add pads to all ports having the port_is_pad attribute set to **TRUE**. Based on area and performance constraints, DFT Compiler selects (from among the pads available in the target library) the optimal pad for each port.

In some cases, if the target library does not have an appropriate pad, DFT Compiler selects a combination of a different pad and some core logic. For example, if the target library contains only active-high-enable three-state output pads, but a given port is an active-low-enable three-state port, then pad-mapping selects the active-high-enable three-state pad but inverts the enable signal using an inverter in the core.

Rule 10.1.1(a) of the IEEE 1149.1 JTAG Standard specifies that "Boundary-scan register cells shall be connected *between* each digital system pin and the on-chip system logic to allow the state of the system pin and, where appropriate, the system logic connection to be controlled or observed or both." This rule is violated if pad-mapping has introduced logic between the pad and the BSR cell.

WHAT NEXT

Such a violation may result from one of the following situations:

• If the target library does not have a pad with the proper characteristics to map this port without introducing core logic, Test Compiler attempts to find another pad and introduce core logic. In such a case, you can either use a target library with the proper pad type or modify the offending design port characteristic so that pad-mapping can complete without the necessity of additional logic.

• If the pad-mapping algorithm has not selected a pad that could have been placed at this port without the necessity of additional core logic in the design, you can force pad-mapping to use the correct pad. (See the documentation on pad mapping by Design Compiler.)

TEST-146 (warning) testability configuration is not set.

DESCRIPTION

You receive this warning message because testability configuration must be set as follows to run TDVR (test data volume reduction) flow:
set_dft_configuration -testability

WHAT NEXT

No action is required on your part, if you do not intend to set testability configuration. However, if you want to set testability configuration, change your script to include **set_dft_configuration -testability**.

SEE ALSO

set_dft_configuration (2).

TEST-147 (warning) the required number of observe test points can not be met.

DESCRIPTION

You receive this warning message because several observe test points are defined too large and TetraMAX cannot meet this constraint. TetraMAX automatically defines an appropriate number of test points for the design.

WHAT NEXT

No action is required on your part if you want accept the observe test points number defined by TetraMAX. Change the user specifications to specify another number.

TEST-148 (warning) A new port will be created for "tpclk" clock.

DESCRIPTION

You receive this warning message because no clock is defined for the new observe scan flip-flops inserted in the design, so the tool creates the clock.

WHAT NEXT

No action is required on your part if you want to accept this change.

However, you can define a clock using the **set_dft_signal** command.

SEE ALSO

set_dft_signal (2).

TEST-149 (Error) The scan utility has to be enabled for the scan compression feature.

DESCRIPTION

You receive this error message because you enabled the scan compression and you disabled the scan utility.

WHAT NEXT

Enable the scan utility with the -scan option in set_dft_configuration.

SEE ALSO

set_dft_configuration (2), **set_scan_compression_configuration** (2).

TEST-150 (Error) The -no_scan option cannot be an option of insert_dft when scan compression is enabled.

DESCRIPTION

You receive this error message because you enabled the scan compression feature and you invoked insert_dft -no_scan.

WHAT NEXT

Remove the -no_scan option for insert_dft and reissue the command.

SEE ALSO

insert_dft (2), **set_dft_configuration** (2), **set_scan_compression_configuration** (2).

TEST-151 (Error) Scan compression and %s cannot be enabled

in the same flow.

DESCRIPTION

You receive this error message because you enabled the scan compression feature and the %s feature.

WHAT NEXT

Disable the %s feature with set_dft_configuration.

SEE ALSO

insert_dft (2), **set_dft_configuration** (2), **set_scan_compression_configuration** (2).

TEST-152 (warning) Design has no scan-in port.

DESCRIPTION

DFT Compiler has not found any port with signal type *test_scan_in*. This situation can cause all the cells of the design to be "scan uncontrollable," if no custom test protocol is used. It also prevents the checking of scan-chain connectivity.

WHAT NEXT

Define the **test_scan_in** ports of the design.

TEST-153 (Error) The scan utility has to be enabled for the logic BIST feature.

DESCRIPTION

You receive this error message because you enabled the logic BIST feature and you disabled the scan utility with the command set_dft_configuration -scan disable

WHAT NEXT

Enable the scan utility with the -scan disable option in set_dft_configuration and reissue the command preview_dft or insert_dft.

SEE ALSO

insert_dft (2), **preview_dft** (2), **set_dft_configuration** (2), **set_lbist_onfiguration** (2).

TEST-160 (information) BSR cell port drive limit '%d' exceeded. Another BSR cell will be added to drive signal '%s'.

DESCRIPTION

Simultaneous switching of multiple I/O ports can produce VCC and VSS glitches that could exceed the tolerance level of the IC. Such a danger can occur when JTAG is in test mode. The problem arises when the pins of a chip that does not normally support simultaneous switching or enabling of all outputs are controlled from the Boundary Scan Register (BSR), rather than from the on-chip system logic. For example, this situation arises when the EXTEST instruction is selected. It is possible that the tests supplied through the boundary-scan path will cause all outputs to change state and/or be active simultaneously. If precautions are not taken, the sum of the switching currents of all pins may produce VCC and VSS glitches that could exceed the tolerance level of the IC, and the core logic as well as the BSR cells and TAP would then be subject to interference. The power consumption could be increased beyond the capacity of the power pins for a prolonged period, perhaps resulting in incorrect operation of the chip.

Delays that only effect the signal path when the chip is in JTAG test mode can be added to prevent simultaneous switching of outputs when pins are driven from the BSR. The added delays should be small in comparison with the minimum period of TCK, but should be sufficient to ensure that the power-current demand arising from the change of state at one pin or group of pins does not overlap with that from another group producing the excessive power consumption.

However, if the process to optimize the number of BSR cells results in a single BSR cell (for example a bus three-state enable signal) driving too many enable signals there is no way to introduce delays between the signals controlled by that BSR cell and ground bounce may not be prevented.

As a safety precaution DFT Compiler places an default cap on the number of I/O ports that can be driven by a single BSR cell. This message signals that this limit has been reached and another BSR cell has been added to drive outputs driven by this signal.

A detailed discussion of the Ground-Bounce problems is presented in Chapter 15, 'Providing Boundary-Scan on Chips with Power or Output-Switching limitations' of 'The Test Access Port and Boundary-Scan Architecture' by Colin M. Maunder and Rodham E. Tulloss, IEEE Computer Society Press Tutorial, 1990.

WHAT NEXT

The environmental variable **test_jtag_bsr_cell_port_drive_limit** has been added to the .synopsys setup environment to provide the user with a mechanism to ensure that the

'ground bounce' problem does not occur for designs with JTAG synthesized by DFT Compiler.

test_jtag_bsr_cell_port_drive_limit puts a cap on the number of ouputs that can be driven by a single BSR cell. For this design, the limit is shown by the value in the error message. The user can establish another positive non-zero limit, by changing the value of the variable in the .synopsys_dc.setup file.

It can be set in the global or local .synopsys file. Alternately, the ground bounce attribute can be set on a design by executing **set_attribute** <design_name> **jtag_bsr_cell_port_drive_limit** <positive_integer> **-type integer** before JTAG synthesis.

The value of the ground-bounce limit for a particular JTAG design can be determined by executing **report_test -jtag**.

TEST-163 (warning) User scan-chain %d has length %d which exceeds desired maximum.

DESCRIPTION

The **insert_test** command issues this message when you use its -max_scan_chain_length option to specify a maximum length that is less than the length of a scan chain you already defined. The **insert_test** command implements the scan chain that you defined but warns you that, in doing so, it has violated your specification for maximum scan chain length.

You can define scan chains with **set_scan_chain** or with **set_test_routing_order**. The **set_scan_chain** command specifies membership of the scan chain, but not the order of scan cells on the chain. Thus, the following commands give a **TEST-163** violation:

```
set_scan_chain 1 {"dff1", "dff2"} insert_test -max_scan_chain_length 1
```

The **set_test_routing_order** command specifies the order of scan cells on the chain. Thus, the following commands also give a **TEST-163** violation:

```
insert_test -no_route set_test_routing_order {"dff2", "dff1"} -scan_chain_index 1
insert_test -no_insert -max_scan_chain_length 1
```

WHAT NEXT

If the scan chain you specified with **set_scan_chain** or **set_test_routing_order** is the scan chain you require, no action is necessary. However, if you need to reduce the length of the chain, correct the **set_scan_chain** or **set_test_routing_order** specification and rerun **insert_test**.

TEST-164 (warning) There are %d user scan-chains against

only %d requested.

DESCRIPTION

The **insert_test** command issues this message when you use its -scan_chains option to specify a number of scan chains that is less than the number of scan chains you previously defined. The **insert_test** command implements the scan chains you defined but warns you that, in doing so, it violated your specification for the number of scan chains. You can define scan chains with **set_scan_chain** or with **set_test_routing_order**.

The **set_scan_chain** command specifies membership of the scan chain, but not the order of scan cells on the chain. Therefore, the following commands give a **TEST-164** violation:

```
set_scan_chain 1 {"dff1", "dff2"} set_scan_chain 2 {"dff3", "dff4"} insert_test -
scan_chains 1
```

The **set_test_routing_order** command specifies the order of scan cells on the chain. Thus, the following commands also give a **TEST-164** violation:

```
insert_test -no_route set_test_routing_order {"dff2", "dff1"} -scan_chain_index 1
set_test_routing_order {"dff3", "dff4"} -scan_chain_index 2 insert_test -no_insert -
scan_chains 1
```

WHAT NEXT

If the scan chains you specified with **set_scan_chain** or **set_test_routing_order** are the scan chains you require, no action is necessary. However, if you need to reduce the number of scan chains, correct the **set_scan_chain** or **set_test_routing_order** specifications and rerun **insert_test**.

TEST-165 (warning) There are too few scan-cells (%d) to build requested chains

DESCRIPTION

The **insert_test** command issues this message when you use its -scan_chains option to specify a number of scan chains that is more than the sum of the number of scan chains that you already defined and the number of scan cells that you have not yet allocated to scan chains. The message reports the number of scan cells that you have not yet allocated to scan chains.

The **insert_test** command implements the scan chains you defined but warns you that, in doing so, it was not able to implement the number of scan chains requested. You can define scan chains with **set_scan_chain** or with **set_test_routing_order**.

The **set_scan_chain** command specifies membership of the scan chain, but not the order

of scan cells on the chain. Therefore, for a design with only four scan cells {"dff1", "dff2", "dff3", "dff4"} the following commands give a **TEST-165** violation:

```
set_scan_chain 1 {"dff1", "dff2"} set_scan_chain 2 {"dff3", "dff4"} insert_test -scan_chains 3
```

The **set_test_routing_order** command specifies the order of scan cells on the chain. Therefore, the following commands also give a **TEST-165** violation for the same design:

```
insert_test -no_route set_test_routing_order {"dff2", "dff1"} -scan_chain_index 1 set_test_routing_order {"dff3", "dff4"} -scan_chain_index 2 insert_test -no_insert -scan_chains 1
```

Finally, the following command gives you a **TEST-165** violation even though you defined no scan chains for the same design.

```
insert_test -scan_chains 5
```

WHAT NEXT

If the scan chains you specified with **set_scan_chain** or **set_test_routing_order** are the scan chains you require, no action is necessary. However, if you need to increase the number of scan chains, correct the **set_scan_chain** or **set_test_routing_order** specifications and rerun **insert_test**.

TEST-169 (warning) Normal mode clock pin %s of cell %s (%s) is uncontrollable.

DESCRIPTION

A normal mode clock pin is a clock pin that is active during normal operation of the design. Depending on the scan style, the clock pin might be active or inactive during scan shift. A typical example is an LSSD C Clock. In normal operation this captures data into the LSSD cell’s master latch, but is held inactive during a scan shift while the A and B clocks are active. Another example is the clock pin of a multiplexed flip-flop scan cell, which is active in both normal operation and in scan shift.

The **check_test** command issues the **TEST-169** warning when it finds a normal mode clock pin that is in an unknown state when all clock ports of the design are held inactive.

The most frequent cause of this violation is invalid clock gating, where the value on the clock pin is determined by the value in another sequential element when the clock port is held inactive.

When **check_test** can identify the source of this violation it also issues a **TEST-281** to identify the network that causes the clock pin to be in an unknown state.

For prescan designs, it is important that you review this warning and correct it, otherwise the cell will not be scan replaced by **insert_scan** and so your fault coverage will be reduced.

WHAT NEXT

Review the accompanying **TEST-281** message to identify the source of the uncontrollable clock. If the source is a clock gating circuit, consider adding test-mode gating to ensure that the clock pin can be controlled from an external clock port for test purposes. For example, add a multiplexer to the clock gating circuit so when a test_mode port is held to logic 1 a clock port drives the clock pin. Now apply a **set_test_hold 1** command to the test_mode port and rerun **check_test**.

If you think that the clock gating is valid and should be accepted by **check_test**, review the sense of the clock signals inferred by **check_test**. (Check the **TEST-169** messages to see if DFT Compiler inferred a return-to-zero or a return-to-one clock.)

Consider a clock gating circuit that ANDs together an internal signal and a signal from a clock port, CLK. If CLK is inferred as a return to one clock, **check_test reports a TEST-169** violation because the clock gating's output is controlled by the internally generated signal when CLK is in its off-state of logic one. However, if you explicitly instruct Test Compiler to use a return-to-zero clock, no **TEST-169** violation is issued because the clock gating's output is at logic 0 when CLK is in its inactive state of logic zero. You can instruct DFT Compiler to use a return-to-zero clock with the **create_test_clock** command. For example,

```
create_test_clock CLK -period 100.0 -waveform {30.0 40.0}
```

TEST-170 (information) There are %d other pins with the same violation.

DESCRIPTION

When **check_test** runs in ordinary (nonverbose) mode it lists warnings only for the first pin that violates a rule, followed by the number of additional violations. The **TEST-170** messages shows the number of additional violations.

WHAT NEXT

The warning message that appears before this one indicates the design rule violation. (There might also be additional information messages that provide more details about the first violation).

If you want to see details of all the violations of a rule, run **check_test** in verbose mode. For example **check_test** might return the following messages:

```
Warning: Clock/enable pin CLK of cell a_out_reg[1] (DTN11) tied constant. (TEST-125)
Information: There are 3 other pins with the same violation. (TEST-170)
```

However, if you run **check_test -verbose**, you will see details of all four violations:

```
Warning: Clock/enable pin CLK of cell a_out_reg[1] (DTN11) tied constant. (TEST-125)
Information: Pins with this violation : a_out_reg[1]/CLK, a_out_reg[2]/CLK,
b_out_reg[0]/CLK, b_out_reg[1]/CLK. (TEST-284)
```

TEST-171 (information) There are %d other cells with the same violation.

DESCRIPTION

When **check_test** runs in ordinary (nonverbose) mode, it lists warnings only for the first cell that violates a rule, followed by the number of additional violations. The **TEST-170** messages show the number of additional violations.

WHAT NEXT

The warning message that appears before this one indicates the design rule violation. (There might be additional information messages that provide more details about the first violation.)

If you want to see details of all the violations of a rule, run **check_test** in verbose mode. For example, **check_test** might produce the following messages:

```
Warning: No scan equivalent exists for cell a_out_reg[2] (FD1). (TEST-120)
Information: There are 2 other cells with the same violation. (TEST-171)
```

However, if you run fbcheck_test -verbose, you see details of all three violations:

```
Warning: No scan equivalent exists for cell a_out_reg[2] (FD1). (TEST-120)
Information: Cells with this violation : a_out_reg[0], a_out_reg[1], a_out_reg[2].
(TEST-283)
```

TEST-172 (information) There is one other pin with the same violation.

DESCRIPTION

When **check_test** runs in ordinary (nonverbose) mode, it lists warnings only for the first pin that violates a rule, followed by the number of additional violations. The **TEST-172** message shows that there is one additional violation.

WHAT NEXT

The warning message that appears before this one indicates the design rule violation. (There might also be additional information messages that provide more details about the first violation.)

If you want to see details of both the violations of a rule, run **check_test** in verbose mode. For example **check_test** might produce the following messages:

```
Warning: Clock/enable pin CLK of cell b_out_reg[0] (DTN11) tied constant. (TEST-125)
Information: There is one other pin with the same violation. (TEST-172)
```

However, if you run **check_test -verbose**, you will see details of both violations:

```
Warning: Clock/enable pin CLK of cell b_out_reg[0] (DTN11) tied constant. (TEST-125)
Information: Pins with this violation : b_out_reg[0]/CLK, b_out_reg[1]/CLK. (TEST-284)
```

TEST-173 (information) There is 1 other cell with the same violation.

DESCRIPTION

When **check_test** runs in ordinary (nonverbose) mode, it lists warnings only for the first cell that violates a rule, followed by the number of additional violations. The **TEST-170** message shows that there is one additional violation.

WHAT NEXT

The warning message that appears before this one indicates the design rule violation. (There might also be additional information messages that provide more details about the first violation).

If you want to see details of both the violations of a rule, run **check_test** in verbose mode. For example **check_test** might produce the following messages:

```
Warning: No scan equivalent exists for cell a_out_reg[2] (FD1). (TEST-120)
Information: There is 1 other cell with the same violation.
```

However, if you run **check_test -verbose**, you will see details of both violations:

```
Warning: No scan equivalent exists for cell a_out_reg[2] (FD1). (TEST-120)
Information: Cells with this violation : a_out_reg[1], a_out_reg[2]. (TEST-283)
```

TEST-174 (warning) %d scan-chains will be needed, against %d

requested.

DESCRIPTION

The **insert_test** command issues this message when you use its -scan_chains option to specify a number of scan chains that conflicts with one of the following:

a) The number of clock domains in the design, when you have not used the -multiple_clocks_chains option and the scan style is multiplexed flip-flop

b) The maximum scan chain length that you specified with the -max_scan_chain_length option

c) Scan chains that you defined with set_scan_chain or set_test_routing_order

d) A combination of the aforementioned.

For case a), if you do not specify that **insert_test** can mix elements clocked by different clocks on the same scan chain, **insert_test** will not mix clocks on the same scan chain. Therefore, if you specify fewer clocks than scan chains without specifying that clock mixing is allowed, **insert_test** is unable to satisfy both your requirements.

When **insert_test** issues the **TEST-174** warning, it gives precedence to your implicit specification not to mix clocks on the scan chain.

For example, you see the following message after the command **insert_test -scan_chains 1** for a design of two clock domains (clk1 and clk2):

Warning: 2 scan chains will be needed, against 1 requested. (TEST-174)

Then **insert_test** inserts two scan chains, one of elements clocked by clk1 and one of elements clocked by clk2.

For case b), if you specify a maximum scan chain length and a number of scan chains so that **insert_test** cannot honor both requirements, **insert_test** issues the **TEST-174** warning and gives precedence to the maximum scan chain length.

For example, you see the following message after the command **insert_test -scan_chains 1 -max_scan_chain_length 2000** for a design of 4000 scannable elements and a single clock domain:

Warning: 2 scan chains will be needed, against 1 requested. (TEST-174)

Then insert_test inserts two scan chains, each of length 2000.

For case c), if you specify more scan chains with **set_scan_chain** and **set_test_routing_order** than the number of scan chains you specify with the -scan_chains option and a number of scan chains, **insert_test** issues the **TEST-174P warning and gives precedence to the scan chains that you specified with set_scan_chain** or **set_test_routing order**.

For example, after the commands:

set_scan_chain 1 {U1/DFF1} set_scan_chain 2 {U1/DFF2} insert_test -scan_chains 1

You see the following message:

Warning: 2 scan-chains will be needed, against 1 requested. (TEST-174)

and insert_test will build two scan chains.

WHAT NEXT

If the number of scan chains that **insert_test** inserted is acceptable to you, no action is necessary. However, if you need to reduce the number of scan chains, you need to correct your specification and rerun **insert_test**.

To determine the conflict in your specification it might be useful to run **check_test** and **report_test -scan_path** to examine the scan architecture that **insert_test** created. This should give you some insight into what was inconsistent in your specification.

TEST-175 (information) The loop contains: %s.

DESCRIPTION

This message provides additional information in support of other messages. For example, it may report the cell pins that comprise a combinational feedback loop.

WHAT NEXT

The message that appears before this message indicates the actual problem.

TEST-176 (information) Scan insertion did not build any scan chains.

DESCRIPTION

This message tells you that scan insertion did build any scan chains.

WHAT NEXT

Study accompanying warning and error messages for the reasons why no scan chains were built.

TEST-179 (warning) Design has no scan-out port.

DESCRIPTION

DFT Compiler has not found any port with signal type **test_scan_out**. This situation can cause all the cells of the design to be "scan unobservable" if no custom test protocol is used. It also prevents checking the scan chain connectivity.

WHAT NEXT

Define the **test_scan_out** ports of the design.

TEST-180 (information) Because pin %s of cell %s (%s) is not a three-state driver.

DESCRIPTION

This message provides additional information in support of the TEST-115 (Three-state net %s is not properly driven) warning message.

The message indicates either

a) A serious design problem where you have connected together a two-state driver and a three-state driver

b) A link problem where no model can be found for the cell, and so is modeled by DFT Compiler as a black box. When a cell is modeled as a black box, DFT Compiler treats its outputs as two-state drivers that drive an unknown (or logic X) value.

WHAT NEXT

Use the information from the TEST-180 message and the TEST-115 messages to identify the two-state driver and the three-state net.

If you have a design violation, review your design to determine if the two-state driver should really be a three-state driver, or if you have connected its output to the wrong net. Correct your design and rerun **dft_drc**.

If there is a link problem, identify the missing information (link_library or search_path) and rerun **dft_drc**.

TEST-182 (information) Because input port %s is not a three-

state driver.

DESCRIPTION

This message provides additional information in support of the TEST-115 (Three-state net %s is not properly driven) warning message. The message indicates a serious design problem where you have connected together a port and three-state drivers.

WHAT NEXT

Use the information from the TEST-182 message and the TEST-115 messages to identify the input port and the three-state net. Review your design to determine if the port should really be connected to a three-state buffer, or if you have connected its output to the wrong net. Correct your design and rerun **dft_drc**.

TEST-186 (warning) Shift clock pin %s of cell %s (%s) is illegally gated.

DESCRIPTION

A shift clock pin is a clock pin that is active during scan shift while shifting data through the scan chain. Depending on the scan style a shift clock pin can be active or inactive during normal-mode operation.

The **check_test** command issues the TEST-169 warning for pre-scan designs when it finds a shift clock pin that is in an inactive state when all clock ports of the design are held inactive, but is in an unknown state when the clock port pulses. Since **check_test** only issues this message for pre-scan designs, you only see this violation message for clock pins that are active in both scan shift and normal-mode operations. Therefore, you only see this violation for the clock pin of multiplexed flip-flop scan cells or for the B clock of LSSD scan cells.

A shift clock pin that is in an unknown state when a shift clock pulses is a violation because it means that during scan shift the sequential element will not always receive a clock pulse in a scan shift cycle. Therefore, any scan chain that includes a cell with this violation will not shift reliably and so cannot be used to load and unload test data.

The most frequent cause of this violation is invalid clock gating, where the value on the clock pin is determined by the value in another sequential element when the clock port pulses. When **check_test** can identify the source of this violation it also issues a TEST-281 message to identify the network that causes the clock pin to be in an unknown state.

For pre-scan designs it is important that you review this warning and correct it; otherwise the cell will not be scan replaced by **insert_scan** and so your fault coverage will be reduced.

WHAT NEXT

For the multiplexed flip-flop scan style with a return to zero clock, this warning message indicates that you probably have an internal clock signal to a flip-flop generated by (N)ANDing the clock port with an internally generated signal from a sequential cell. When the clock port is in its inactive state (0), the internal clock signal is at a steady logic value: logic 1 for a NAND gate, logic 0 for an AND gate. However, when the clock port pulses the behavior of the internal clock signal depends upon the value of the internally generated signals.

For the multiplexed flip-flop scan style with a return to one clock, this warning message indicates that you have an internal clock signal to a flip-flop generated by (N)ORing the clock port with an internally generated signal. When the clock port is in its inactive state (1), the internal clock signal is at a steady logic value: logic 0 for a NOR gate, logic 1 for an OR gate. However, when the clock port pulses, the behavior of the internal clock signal depends upon the value of the internally generated signals.

Review the accompanying TEST-281 message to identify the source of the uncontrollable clock. If the source is a clock gating circuit, consider adding test-mode gating to ensure that the clock pin can be controlled from an external clock port for test purposes. For example, add a multiplexer to the clock gating circuit so that, when a test_mode port is held to logic 1, a clock port drives the clock pin. Now apply a **set_test_hold 1** command to the test_mode port and rerun **check_test**.

TEST-188 (warning) BSR cell optimization has pushed the cell associated with output port '%s' onto input port '%s'. The BSR cell for this input port has been specified as 'observe-only'. This is not compliant with the IEEE 1149.1 JTAG standard.

DESCRIPTION

Using the **set_jtag_port_mode** command, this input port has been specified to be 'observe-only'. However since, BSR cell optimization has pushed the BSR cell associated with an output onto this input port, and *all* output port BSR cells must be controllable, the mode specification for this input is in fact non-compliant with the standard.

Unless the user requests a user-defined Boundary Scan Register (BSR) cell implementation using the **set_jtag_implementation** command, the Test Compiler selects 1149.1 compliant BSR cells from among the following 10 defined types:

TypeDefault NameBSR Cell Function

BSRINBOTHJTAG_BSRINBOTHset & observe data input cell

BSRINSETJTAG_BSRINSETset-only data input cell
BSRINOBSJTAG_BSRINOBSobserve-only data input cell
BSRINCLKBOTHJTAG_BSRINCLKBOTHset & observe clock input cell
BSRINCLKSETJTAG_BSRINCLKSETset-only clock input cell
BSRINCLKOBSJTAG_BSRINCLKOBSobserve-only clock input cell
BSROUTBOTHJTAG_BSROUTBOTHset & observe data output cell
BSROUTSETJTAG_BSROUTSETset-only data output cell
BSROUTOBSJTAG_BSROUTOBSobserve-only data output cell
BSRCTLJTAG_BSRCTLcontrol cell

IEEE 1149.1 Standard rule 10.1.1 specifies legal boundary scan register cell types. Several of the 10 types listed above are not compliant with the standard. Nonetheless, DFT Compiler supports them in order to allow designers the greatest possible flexibility when using Programmable JTAG.

> **10.1.1(b)** "For a unidirectional system input pin (clock or nonclock), a boundary-
> scan register cell shall be connected between the system pin and the on-
> chip system logic to allow the state of the system pin to be observed and, optionally, for the state of the system logic to be controlled."

Thus, legal data and clock input BSR cell types for unidirectional system input pins are observe-only and both control and observe. BSRINSET and BSRINCLKSET are non-compliant types.

> **10.1.1(c)** "For 2-state and open-collector system output pins, a boundary-
> scan register cell shall be provided to allow the state of the system pin to be controlled and the state of the on-
> chip system logic output to be observed."

Thus, the legal output BSR cell type for system 2-state and open-collector output pins is both control and observe. BSROUTSET and BSROUTOBS are non-compliant types.

> **10.1.1(d)** "For 3-state system output pins, boundary-scan register cells shall be provided to allow both the data value and the output drive state
> (active or inactive) to be controlled and for the corresponding system logic
> outputs to be observed."

Thus, the legal output BSR cell type for system 3-state output pins is both control and observe. BSROUTSET and BSROUTOBS are non-compliant types.

> **10.1.1(e)** "For a bidirectional system pin, boundary-scan register cells shall be provided to allow the value and direction of data at the system pin to
> be controlled *or* observed and, where appropriate, for the corresponding system logic inputs to be controlled."

This is somewhat ambiguous. DFT Compiler interprets this rule to indicate that as applied to bidirectional signals BSRINSET, BSROUTSET and BSROUTOBS are non-compliant types.

The types '**BSR**xxx**BOTH**' (control and observe) '**BSR**xxx**SET**' (control-only) and '**BSR**xxx**OBS**' (observe-only) differ. They correspond respectively to the three modes 'both', 'control' and 'observe' specified with the **set_jtag_port_mode** command. When this command is invoked for one or more ports of the design, BSR cells for those ports will have BSR cells of the specified type associated with them.

If the specified type will result in a non-compliant BSR cell being synthesized for a port, this warning message is issued.

WHAT NEXT

Determine whether non-compliant BSR cells can be tolerated in your design. If not, modify the port mode settings for the offending port and reinvode **insert_jtag**.

TEST-189 (error) Three-state cell '%s' (library cell '%s') with missing or erroneous enable pin.

DESCRIPTION

When determining where to insert boundary scan register (BSR) cells, Test Compiler processes any three-state drive cells associated with the I/O ports.

Where ports are controlled by three-state cells, the BSR cells are connected before the inputs to the three-states. In some cases, to be compliant with the IEEE 1149.1 JTAG standard, complex three-state cells from the original design must be mapped into simpler logic constructs.

This message is generated when DFT Compiler encounters a three-state cell whose enable signal is either missing or erroneously modeled.

The error message is also generated if the target cell is an unresolved reference or is in the design. One cause of an unresolved reference is the existence of generic logic in the design. Another cause for the error may be definition of the three-state cell as a black box.

In all cases JTAG synthesis of BSR cells for three-state controlled ports requires mapping the three-state controller to logic, which includes a simple generic logic gate comprised of single data, control, and output signals. One BSR cell is placed in front of both the control and data signal inputs. Thus, a black box definition of the three-state control cell is also erroneous.

WHAT NEXT

Verify the cell and check the library description of the offending cell for correctness. If the cell is an unresolved reference, resolve it. One way to discover errors in the library is to recompile it using the Library Compiler.

TEST-191 (error) Probable library error associated with cell '%s'.
No three-state enable signal associated with pin '%s'.

DESCRIPTION

This error message is generated when a three-state output signal does not have a three-state attach associated with it. The situation is probably caused by an incorrectly modeled library cell.

WHAT NEXT

Recompile the library using the Library Compiler, and correct any errors to this and other cells.

TEST-192 (error) Dangling port '%s'
cannot be included in the JTAG Boundary Scan Register (BSR).

DESCRIPTION

DFT Compiler has encountered a top-level I/O port that is unconnected to any net, because of which DFT Compiler cannot determine the optimal configuration of the JTAG Boundary Scan Register (BSR) and has aborted JTAG synthesis. A 1149.1-compliant JTAG architecture requires that *all* ports of a design, except those comprising the JTAG Test Access Port (TAP), be included in the BSR. Optimal determination of the number of cells in the BSR requires that the connectivity of each port be traversed. It is possible to instruct DFT Compiler to synthesize a noncompliant BSR by explicitly excluding certain ports from the BSR.

WHAT NEXT

To distinguish *true* I/O ports of a design (which are to be included in the BSR) from *pseudo* ports (which are, in fact, internal signals that will be connected to other internal signals at a future date), the *true* ports are identified by executing **set_port_is_pad <list_of_true_IO_ports>** prior to invoking **insert_jtag**. If you want to proceed with JTAG synthesis and exclude a *true* "dangling" port from the BSR, specify the exclusion with the command **set_jtag_port FALSE <list_of_ports_to_be_excluded_from_the_BSR>**. If you want to include this dangling

port in the BSR, you must connect it correctly to the design. It is not necessary to create the TAP ports for the design prior to invoking JTAG synthesis; these ports are automatically created. Although DFT Compiler will identify pre-existing TAP ports (if they have been given the correct design attributes using **set_signal_type <signal_type> <port_name>**), it is simpler to rename automatically synthesized TAP ports after JTAG synthesis than to create them in advance. To identify pre-existing TAP ports, identify each TAP port with the correct **signal_type** from among **jtag_tdi**, **jtag_tck**, **jtag_tms**, **jtag_trst** and **jtag_tdo**.

TEST-193 (error) Default JTAG component '%s', of component type '%s' not found in the JTAG component library associated with this design.

DESCRIPTION

DFT Compiler selects the various JTAG components (the TAP controller, Bypass, Instruction, and Identification registers, and the various types of Boundary Scan Register cells) from a JTAG component library.

In the absence of explicit instruction from the user (using the **set_jtag_implementation** command), DFT Compiler synthesizes JTAG using a set of **default** components from the jtag.db library. This error message is produced if the jtag.db library associated with the current design has been modified so that the default component specified has been removed. Under no circumstances should a default component be removed from the jtag.db since if the component is required for this JTAG architecture and the user has not specified an alternative implementation for this component, JTAG synthesis would fail. Absense of this default component causes **insert_jtagP to gracefully abort.**

WHAT NEXT

Rebuild the jtag.db to include all default components contained in the jtag.db library provided with DFT Compiler.

TEST-194 (error) -- Intolerable 1149.1 Violation -- Three-stated port '%s' is controlled by a feed-through input port '%s' that is excluded from the Boundary Scan Register.

DESCRIPTION

Designs that contain violations of the 1149.1 standard are referred to as non-compliant JTAG architectures. 1149.1 standard violations fall into two categories:

tolerable and *intolerable*. We define *intolerable* violations as those that render the JTAG access protocol inoperable or which make the behavior of the JTAG logic unpredictable.

We define *tolerable* violations of the standard as those that neither render the JTAG access protocol inoperable nor make the behavior of the JTAG logic unpredictable, but which do violate some rule in the 1149.1 standard.

In most cases exclusion of a non-TAP I/O port of a circuit from the Boundary Scan Register (BSR) is a violation of the standard and will result in reduced controllability and observability at the board and system levels, but is not an intolerable violation. However, in this case the exclusion of the feedthrough input port that drives the three-state control signal of an ouput port that is not excluded from the BSR is an *intolerable* violation of the IEEE 1149.1 standard because it renders that output port uncontrollable in 1149.1 test mode.

For this reason, it is not supported by DFT Compiler.

WHAT NEXT

Either exclude the associated output port(s) or include the feed-through input port in the Boundary Scan Register.

TEST-195 (information) JTAG pad synthesis will NOT include the following ports:

DESCRIPTION

The JTAG Boundary Scan Register (BSR) associates a register with each I/O pad of a device. These registers can either 'capture' (observe) or 'apply' (control) values at the pads. The registers are serially chained together to form the BSR. Values are set and read serially through the BSR. Typically, all non-TAP (Test Access Port) ports are included in the BSR.

Unless **insert_jtag** is invoked with the **-no_pads** option, Test Compiler will execute pad synthesis along with JTAG synthesis on all ports having the **port_is_pad** attribute set using **set_port_is_pad**. Ports not having this attribute set will be processed for inclusion in the BSR (provided they have not been excluded using **set_jtag_port FALSE {port_list}** command) but will not have pads synthesized for them.

This information message is issued when **insert_jtag** has been invoked without the **-no_pads** option, and the **port_is_pad** attribute has been set on some BSR or TAP ports, but other ports do not have the **port_is_pad** attribute set. In this case, JTAG synthesis will *only* include pad synthesis on the ports with the **port_is_pad** attribute set.

The list of BSR or TAP ports without the **port_is_pad** attribute set follows this message.

WHAT NEXT

If you require pad synthesis as a part of JTAG synthesis, set the **port_is_pad** attribute using the **set_port_is_pad** command on each port you want DFT Compiler to include in the BSR or existing TAP port. Do *not* assign the **port_is_pad** attribute to internal module ports.

One way to specify ports as pads is to execute **set_port_is_pad find (port,"*")** on the current_design.

If you do not want pad synthesis as a by-product of JTAG synthesis, execute **insert_jtag -no_pads**.

'BACKDOOR' PAD SYNTHESIS WITH JTAG

There is a 'backdoor' method for doing JTAG pad synthesis without using **set_port_is_pad** using **insert_jtag -no_pads**.

Using **set_jtag_implementation** *<component_type> <implementation> [list_of_ports]* where the *<implementation>* is in fact a pad cell, along with **insert_jtag -no_pads** will synthesize JTAG with pads, provided those pad cells have the satisfactory JTAG BSR logic in them. The following *WILL* synthesize JTAG with pads.

```
set_jtag_implementation BSRINBOTH some_inboth_pad_cell {list_of_input_ports}
set_jtag_implementation BSROUTBOTH some_outboth_pad_cell {list_of_output_ports}

insert_jtag -no_pads
```

TEST-196 (information) Port '%s' will not have a pad.

DESCRIPTION

The JTAG Boundary Scan Register (BSR) associates a register with each I/O pad of a device. These registers can either 'capture' (observe) or 'apply' (control) values at the pads. The registers are serially chained together to form the BSR. Values are set and read serially through the BSR. Typically, all non-TAP (Test Access Port) ports are included in the BSR.

Unless **insert_jtag** is invoked with the **-no_pads** option, Test Compiler will execute pad synthesis along with JTAG synthesis on all ports having the **port_is_pad** attribute set using **set_port_is_pad**. Ports not having this attribute set will be processed for inclusion in the BSR (provided they have not been excluded using **set_jtag_port FALSE {port_list}** command) but will not have pads synthesized for them.

This information message is issued when **insert_jtag** has been invoked without the **-no_pads** option, and the **port_is_pad** attribute has been set on some BSR or TAP ports, but other ports do not have the **port_is_pad** attribute set. In this case, JTAG synthesis will *only* include pad synthesis on the ports with the **port_is_pad** attribute set.

This BSR or TAP port does not have the **port_is_pad** attribute set.

WHAT NEXT

If you require pad synthesis as a part of JTAG synthesis for this port, set its' **port_is_pad** attribute using **set_port_is_pad {<port_name>}**.

One way to specify ports as pads for all ports is to execute **set_port_is_pad find (port,"*")** on the current_design.

If you do not want pad synthesis as a by-product of JTAG synthesis, execute **insert_jtag -no_pads**.

'BACKDOOR' PAD SYNTHESIS WITH JTAG

There is a 'backdoor' method for doing JTAG pad synthesis without using **set_port_is_pad** using **insert_jtag -no_pads**.

Using **set_jtag_implementation** *<component_type> <implementation> [list_of_ports]* where the *<implementation>* is in fact a pad cell, along with **insert_jtag -no_pads** will synthesize JTAG with pads, provided those pad cells have the satisfactory JTAG BSR logic in them. The following *WILL* synthesize JTAG with pads.

```
set_jtag_implementation BSRINBOTH some_inboth_pad_cell {list_of_input_ports}
set_jtag_implementation BSROUTBOTH some_outboth_pad_cell {list_of_output_ports}

insert_jtag -no_pads
```

TEST-197 (warning) Cell %s (%s) is not scan controllable because it has overlapping master/slave clocks.

DESCRIPTION

The waveforms on **scan clock A** and **scan clock B** are overlapping. The cell is not scan controllable.

When scan data is shifted in and out of the design-under-test, the overlapping scan clocks will cause the scan data to be corrupted.

WHAT NEXT

Make the waveforms of **scan clock A and scan clock B** non-overlapping.

TEST-198 (information) Because pin %s of cell %s (%s) has a

test_isolate attribute.

DESCRIPTION

This message provides additional information in support of the TEST-115 (Three-state net %s is not properly driven) warning message.

The design rule checker issues this message when it finds a pin with a set_test_isolate attribute driving a three-state net. Remember that a set_test_isolate inserts an X driver into the ATPG view of the circuit, and this X driver is a two-state driver. You see this message when you apply a set_test_isolate either directly to such a pin, or to the entire cell.

WHAT NEXT

Remove the set_test_isolate attribute with **remove_attribute**. However, if you applied the set_test_isolate attribute to a black box cell that drives a three-state net and which is in high impedance throughout scan testing, you still need to solve the problem of how to tell DFT Compiler that the output is a constant Z. The only way to do this is to write your own "wrapper" in Verilog or VHDL and to link the wrapper to this model instead of to the library cell.

For example, if you can guarantee that the cell will always be in high impedance during scan testing, you could write a model that sets the outputs of the cell to Z at all times. Be very careful with this option! If you write an incorrect model, or your assumptions on the cell’s behavior are incorrect, bad patterns can easily result.

TEST-199 (information) Because driver %s is a three-state pin of black box cell %s (%s).

DESCRIPTION

You receive this message because it provides additional information in support of the TEST-115 warning message (Three-state net %s is not properly driven).

The design rule checker issues this message when a cell with a three-state pin is black boxed. Cells are black boxed when either of the following occurs:

• The library description of the cell’s function missing or incomplete.

• The cell’s functionality is not supported by DFT Compiler. The most common examples are RAMs.

WHAT NEXT

If the library cell can be modeled with Library Compiler and supported by DFT Compiler, you should contact your vendor/library developer to fix this cell. Otherwise, if you are sure that you can correctly model the functionality of the cell for test purposes, you can write your own wrapper in Verilog or VHDL and link the wrapper to this model instead of to the library cell.

For example, if you can guarantee that the cell is always in high impedance during scan testing, you can write a model that sets the outputs of the cell to *Z* at all times. Use caution with this option: If you write an incorrect model, or your assumptions on the cell's behavior are incorrect, it may result in bad patterns.

SEE ALSO

TEST-115 (n).

TEST-200 (information) Faults on unused cell outputs are not considered, for example pin %s of cell %s (%s).

DESCRIPTION

Cells that have output pins that are not connected to any other gates will not be added to the master fault list that **create_test_pattern** uses. Consequently **create_test_patterns** will not attempt to detect faults on these output pins. Unused cell output pins will not reduce your fault coverage.

WHAT NEXT

This message is purely an informational message; no action is required.

TEST-201 (information) Faults on unconnected ports are not considered, for example port %s.

DESCRIPTION

Faults on ports that are not connected to any gates will not be added to the master fault list that **create_test_pattern** uses. Consequently **create_test_patterns** will not attempt to detect faults on these output pins. Unused ports will not reduce your fault coverage.

WHAT NEXT

This message is purely an informational message; no action is required.

TEST-202 (information) Cell %s (%s) will not be scanned due to the set_scan_element command.

DESCRIPTION

The **check_test** command issues this message when it finds a sequential cell to which you applied **set_scan_element false**.

If the cell is mapped, but not yet scan replaced, this message tells you that when you run **insert_scan**, scan synthesis will NOT scan replace this cell.

If the cell is scan replaced, this message tells you that when you run **insert_scan**, the cell will be unscanned. That is, the cell is removed from a scan chain if the design is scan routed and remapped to a nonscan cell.

WHAT NEXT

If you want to make the cell a nonscan cell, no action is necessary. If you want to make (or keep) the cell a scan cell, correct the scan specification you created with **set_scan_element**. You need to ensure that that you apply a **set_scan_element true** to the cell.

TEST-203 (information) Faults on bidirectional (INOUT) pins are not considered, e.g. pin %s of cell %s (%s).

DESCRIPTION

Faults on bidirectional pins will not be added to the master fault list that **create_test_pattern** uses. Consequently **create_test_patterns** will not attempt to detect faults on these bidirectional pins. However, pins of gates that are connected to bidirectional pins will be added to the master fault list.

WHAT NEXT

This message is purely an informational message; no action is required.

TEST-204 (information) Latch cell %s (%s) assumed nonscan and using transparent latch model for testing.

DESCRIPTION

The **check_test** command issues this message to inform you that the specified level-

sensitive sequential element will be modeled using a transparent latch model during automatic test pattern generation (ATPG). The transparent latch model treats the latch as a buffer (data input to latch drives data output of latch) when the enable is in its active state. However, when the latch enable is in its inactive state, the latch output is treated as unknown (a logic X).

DFT Compiler models nonscan latches in four ways for ATPG:

a) As black boxes
b) As synchronization elements
c) As transparent devices
d) As sequential elements (in partial scan only)

By default, the **create_test_patterns** command treats all nonscan level-sensitive sequential elements in the design as black boxes during ATPG, except for elements that are recognized by **check_test** as synchronization elements.

However, you can choose to have ATPG use the transparent model by using the **set_scan_transparent true -existing** command. This command sets a **scan_latch_transparent** attribute on latch cells. (For details, see the **set_scan_transparent** man page.)

WHAT NEXT

This is an informational message; therefore, if you want to accept the use of the transparent latch model for the specified latch, no action is necessary. However, be advised that treating synchronization latches or scan-out lock-up latches as transparent causes more design rule violations and can significantly lower the fault coverage that ATPG can achieve.

If you do not want the transparent model to be used for the specified latch cell, set the **set_scan_transparent** attribute to *false* by executing **set_scan_transparent -false**, and re-run **check_test**. Alternatively, to remove individual **scan_latch_transparent** attributes, use the **remove_attribute** command.

SEE ALSO

check_test (2), **set_scan_transparent** (2).

TEST-206 (error) Required logic %d on pin %s/%s conflicts with required logic %d on pin %s/%s.

DESCRIPTION

The DFT Compiler **create_test_patterns** command issues this message when it detects contradictory requirements between two pins directly connected by a net.

When DFT Compiler issues this violation, it does not generate test vectors, since it is impossible for any vector to fullfil both requirements.

WHAT NEXT

Identify the unnecessary **set_test_require** and remove it using **remove_attribute**. Rerun **create_test_patterns**.

You can generate a report of the assertions that you specified (effects of **set_test_hold** and **set_test_require**) by entering

report_test -assertions

TEST-207 (error) Required logic %d on pin %s/%s conflicts with required logic %d on port %s.

DESCRIPTION

The DFT Compiler **create_test_patterns** command issues this message when it detects contradictory requirements between a pin and a port directly connected by a net. The required value on the port may have been specified using the **set_test_hold** command if the port is an input port, or using the **set_test_require** command.

When DFT Compiler issues this violation, it does not generate test vectors, since it is impossible for any vector to fullfil both requirements.

WHAT NEXT

Identify the unnecessary **set_test_require** or **set_test_hold** and remove it using **remove_attribute**. Rerun **create_test_patterns**.

You can generate a report of the assertions that you specified (effects of **set_test_hold** and **set_test_require**) by entering

report_test -assertions

TEST-208 (information) No tests generated - conflicting signal requirements in design. Use the ’report_test -atpg_conflicts’ command for more information.

DESCRIPTION

DFT Compiler issues this message when it detects a condition that prevents valid test patterns from being generated.

Possible sources of conflicting signal requirements include:

- Three-state decoding logic that cannot be operated without creating float or

contention.

- Requirements that you defined with **set_test_require** and **set_test_hold** that create contention or float on a three-state net.

- Contradictory requirements that you defined with **set_test_hold** and **set_test_require** that cannot be satisfied. For example, requiring that the output of an AND gate is a logic 1 while also requiring that an input of the gate is at a logic 0.

WHAT NEXT

Generate a report that identifies the causes of the conflicts and lists the circuit elements involved. To generate a report of ATPG conflicts enter

report_test -atpg_conflicts

You might also find it useful to generate a report of the assertions (effects of **set_test_hold** and **set_test_require**) by entering

report_test -assertions

If the conflict is due to constraints that you defined, remove the condition that cannot be satisfied and rerun **create_test_patterns**.

If the conflict is due to the design of three-state decoding logic, you need to correct the logic; otherwise, if you can accept the float or contention, run **create_test_patterns** with -check_contention false or -check_float false. Be very careful with disabling contention checking; it might result in test vectors that can cause damage to your ASIC during manufacturing test.

TEST-210 (error) Generation of test vectors terminated abnormally.

DESCRIPTION

This message tells you that DFT Compiler could not recover from processing errors that occurred during test pattern creation.

WHAT NEXT

Study accompanying error messages and fix the problems reported.

TEST-211 (information) DFT insertion was not successful.

There were unrecoverable processing errors.

DESCRIPTION

This message tells you that DFT Compiler could not recover from processing errors that occurred during DFT insertion. DFT insertion has exited, without modifying your design.

WHAT NEXT

Study accompanying error messages and fix the problems reported.

TEST-212 (error) Checking of test design rules terminated abnormally.

DESCRIPTION

This message tells you that DFT Compiler could not recover from processing errors that occurred during test design rule checking.

WHAT NEXT

Study accompanying error messages and fix the problems reported.

TEST-213 (warning) Making scan cells non-scan to meet area constraints.

DESCRIPTION

DFT Compiler can make scan cells nonscan to meet area constraints. Use this capability when you need to back off scan in a small percentage of cells to meet critical area constraints.

Fault coverage results can degrade significantly if you apply unrealistic area constraints. For example, if you **set_max_area 0**, it only scans cells that have **true set_scan_element** attributes.

WHAT NEXT

Check design fault coverage. Relax area constraints to improve results.

TEST-214 (warning) Flip-flop-based clock gating is not supported. Cell %s is treated as an ordinary flip-flop and is not scan-replaced.

DESCRIPTION

You receive this message if your design uses flip-flop-based clock gating, which is not currently supported by DFT Compiler. This message is to warn you that Power Compiler sets the **dont_touch** attribute on the logic it inserts for clock gating; thus, flip-flops used for clock gating are not scan replaced, and are treated as non-scan cells.

WHAT NEXT

If the clock gating logic was not inserted by Power Compiler, set the **dont_touch** attribute on the clock gating flip-flops yourself. Otherwise, these flip-flops might be scan-replaced.

If the ATPG coverage is not acceptable, use latch-based clock gating instead.

TEST-215 (information) No test design rule violation needs to be fixed by Autofix.

DESCRIPTION

The purpose of AutoFix is the following: Each scan flip-flop in a design must be clocked by a signal that can be controlled by a primary input port. Otherwise, clocking of data into the flip-flop cannot be controlled during test. In addition, the asynchronous preset and clear inputs of each flip-flop must be inactive during test. Otherwise, the data in the flip-flop can be set or cleared at any time, leaving unknown data in the flip-flop.

If the clock input and/or the asynchronous signals of a flip-flop are not controllable, the test design rule checker flags that the flip-flop has a test design rule violation that needs to be fixed during AutoFix.

The TEST-215 message indicates that the test design rule checker does not report uncontrollable clock and/or uncontrollable asynchronous signals to allow the activation of the AutoFix feature.

The TEST-215 information message might be followed by the TEST-211 information message if no DFT logic needs to be inserted into the design.

WHAT NEXT

Check the test design rule checker violations and apply the correct DFT technique.

If no AutoFix test point is required, you might want to directy apply the full scan technique.

SEE ALSO

dft_drc (2), **preview_dft** (2), **insert_dft** (2).

TEST-217 (information) Starting test protocol inference for existing scan design.

DESCRIPTION

The infer_test_protocol command issues this message for exisitng scan design. An existing scan design is a design where all the sequential elements that you selected as scannable are scan replaced and the scan chains have been routed.

WHAT NEXT

No action is required.

TEST-218 (information) Starting test protocol inference for unrouted scan design.

DESCRIPTION

The infer_test_protocol command issues this message when it is dealing with unrouted scan design. An unrouted scan design is a design where all the sequential elements that you selected as scannable are scan replaced, but the scan chains are not routed.

WHAT NEXT

No action is required.

TEST-219 (information) Starting test protocol creation.

DESCRIPTION

You receive this information message when you execute the **create_test_protocol** command. The message indicates the start of the test protocol creation.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

create_test_protocol (2).

TEST-220 (information) Starting test design rule checking for existing scan design.

DESCRIPTION

An existing scan design is a design where all the sequential elements that you selected as scannable are scan replaced and the scan chains have been routed. For example, if you issue the commands

set_scan_configuration -replace true -route true insert_scan check_test

check_test classifies your design as an existing scan design.

Note that the design has been scan replaced, but not scan routed. Now, you will not see this message, but you will see TEST-221 instead.

If you are reading in a design from a gate-level ASCII format (Verilog, VHDL, or EDIF), which is existing scan, you should issue the command

set_scan_configuration -existing_scan true

before running check_test to indicate that the design has existing scan.

WHAT NEXT

No action is required.

TEST-221 (information) Starting test design rule checking for unrouted scan design.

DESCRIPTION

An unrouted scan design is a design where all the sequential elements that you selected as scannable are scan replaced, but the scan chains are not routed. For example, if you issue the commands

set_scan_configuration -replace true -route false insert_scan check_test

check_test classifies your design as an unrouted scan design.

Similarly, if you issue the commands

compile -scan check_test

check_test classifies your design as an unrouted scan design.

Note that if the design has been both scan replaced and scan routed, you will not see this message, but you will see TEST-220 instead.

If you are reading in a design from a gate-level ASCII format (Verilog, VHDL, or EDIF) which is an unrouted scan design, you should issue the command

set_scan_configuration -existing_scan true

before running check_test to indicate that the design has unrouted scan.

WHAT NEXT

No action is required.

TEST-222 (information) Starting test design rule checking.

DESCRIPTION

The check_test command issues this message for nonscan designs. A nonscan scan design is a design where the sequential elements are not scan replaced.

For example, if you issue the commands

compile check_test

check_test classifies your design as a nonscan scan design.

The check_test command can also classify designs as existing scan (TEST-220) or unrouted scan (TEST-221).

If you are reading in a design from a gate-level ASCII format (Verilog, VHDL, or EDIF), by default, check_test classifies the design as nonscan unless you issue the commands

set_scan_configuration -existing_scan true check_test

You can also explicitly indicate that a design is nonscan by issuing the command

set_scan_configuration -existing_scan false

before running check_test.

WHAT NEXT

If you want check_test to classify the design as nonscan, no action is required. However, if you want check_test to classify the design as existing scan or unrouted scan, issue the command

```
set_scan_configuration -existing_scan true
```

before running check_test.

TEST-223 (warning) Ignoring set_test_hold on test port '%s'.

DESCRIPTION

The **set_test_hold** command is ignored on the TAP port signals because DFT Compiler must control all these signals automatically.

WHAT NEXT

To tell DFT Compiler that BSD logic has been added you can specify the TAP ports and set the BSD attributes as follows: current_design TOP set_signal_type "tdi" my_tdi set_signal_type "tdo" my_tdo set_signal_type "tms" my_tms set_signal_type "tck" my_tck set_signal_type "trst" my_trst set_attribute current_design is_bsd_inserted true -type boolean

Once these attributes are set, **insert_scan** will automatically control the trst pin so that the BSD logic is in bypass mode.

TEST-224 (warning) Target library for design contains no scan-cell models.

DESCRIPTION

Many DFT Compiler capabilities require additional information in the Synopsys library models for scan cells. In this case, the selected target library (or libraries) contain no such extended models.

Depending on the application, the lack of scan cell models may or may not be serious. You will not be able to insert scan cells with the **insert_test** command, and test pattern generation may also be affected.

WHAT NEXT

If you are using an ASIC vendor-supplied library, contact them to confirm whether scan cell models have been included in the library.

If you develop your own Synopsys libraries, refer to the *Library Compiler Reference Manual* in the chapter on modelling scan cells. You can usually supply the additional information very quickly.

TEST-225 (Information) Design has scan chains and unmapped logic.

DESCRIPTION

This message is issued during DFT DRC when the design has unmapped components and also has scan chains. The tool will run PRE DFT DRC in this case.

WHAT NEXT

If the message is issued after insert_dft, recheck whether all logic has been mapped during insertion. Also ensure that the target library has all the needed replacements.

TEST-230 (information) No BSR or TAP ports with port_is_pad attribute 'TRUE' encountered.
JTAG synthesis will not include pad synthesis.

DESCRIPTION

The JTAG Boundary Scan Register (BSR) associates a register with each I/O pad of a device. These registers can either 'capture' (observe) or 'apply' (control) values at the pads. The registers are serially chained together to form the BSR. Values are set and read serially through the BSR. Typically, all non-TAP (Test Access Port) ports are included in the BSR.

Unless **insert_jtag** is invoked with the **-no_pads** option, Test Compiler will execute pad synthesis along with JTAG synthesis on all ports having the **port_is_pad** attribute set using **set_port_is_pad**. Ports not having this attribute set will be processed for inclusion in the BSR (provided they have not been excluded using **set_jtag_port FALSE {port_list}** command) but will not have pads synthesized for them.

This information message is issued when **insert_jtag** has been invoked without the **-no_pads** option, but no existing JTAG TAP ports or BSR ports have the **port_is_pad** attribute set. In this case, JTAG synthesis will *NOT* include pad synthesis. In other words, JTAG synthesis will proceed as if it had been invoked with **insert_jtag -no_pads**.

WHAT NEXT

If you require pad synthesis as a part of JTAG synthesis, set the **port_is_pad** attribute using the **set_port_is_pad** command on each port you want DFT Compiler to include in the BSR or existing TAP port. Do *not* assign the **port_is_pad** attribute to internal module ports.

One way to specify ports as pads is to execute **set_port_is_pad find (port,"*")** on the current_design.

If you do not want pad synthesis as a by-product of JTAG synthesis, execute **insert_jtag -no_pads**.

'BACKDOOR' PAD SYNTHESIS WITH JTAG

There is a 'backdoor' method for doing JTAG pad synthesis without using **set_port_is_pad** using **insert_jtag -no_pads**.

Using **set_jtag_implementation** *<component_type> <implementation> [list_of_ports]* where the *<implementation>* is in fact a pad cell, along with **insert_jtag -no_pads** will synthesize JTAG with pads, provided those pad cells have the satisfactory JTAG BSR logic in them. The following *WILL* synthesize JTAG with pads.

```
set_jtag_implementation BSRINBOTH some_inboth_pad_cell {list_of_input_ports}
set_jtag_implementation BSROUTBOTH some_outboth_pad_cell {list_of_output_ports}

insert_jtag -no_pads
```

TEST-231 (warning) Specified Instruction Register (IR) size (%d) is larger than the minimum (%d) required by the %d JTAG instructions recognized. (Size specified will be used.)

DESCRIPTION

The IEEE 1149.1 JTAG Standard requires that the JTAG Instruction Register (IR) be at least two bits wide. DFT Compiler supports IRs from 2 to 32 bits wide. You can set the size of the IR in 3 ways:

1. Specify the size using **insert_jtag -ir_size** *bit_width*.
2. Force the IR size by specifying an instruction code **set_jtag_instruction -code** "*code*".
3. Let DFT Compiler automatically infer the IR size from the set of specified and mandatory instructions you selected.

If you use one of the first two methods for fixing IR size, the IR may end up larger than required by the number of instructions recognized by DFT Compiler. If you use

the third method, DFT Compiler selects the smallest possible IR size (bit-width).

IR size affects test application time, since instructions are loaded serially into the IR from the JTAG TDI port. The smaller the IR, the faster the serial load.

WHAT NEXT

If IR size has been determined by user-specified instruction codes, reduce the size to the minimum shown in this message by shortening these codes.

If IR size has been determined by a call to **insert_jtag -ir_size** *number_of_cells*, change the *number_of_cells* to the number reported in this warning message.

If you do not specify any instruction codes, DFT Compiler automatically infers the IR size and generates the codes.

TEST-232 (information) %d-bit JTAG Instruction Register (IR) being synthesized.

DESCRIPTION

The IEEE 1149.1 JTAG Standard requires that the JTAG Instruction Register (IR) be at least two bits wide. DFT Compiler supports IRs from 2 to 32 bits wide. You can set the size of the IR in 3 ways:

1. Specify the size using **insert_jtag -ir_size** *bit_width*.
2. Force the IR size by specifying an instruction code **set_jtag_instruction -code** "*code*".
3. Let DFT Compiler automatically infer the IR size from the set of specified and mandatory instructions you selected.

This information message tells you the size of the IR being synthesized.

WHAT NEXT

To change the size of the IR, use one of the three methods described above.

TEST-233 (error) Conflicting routing positions have been assigned to a Boundary Scan Register cell. The conflict occurs because a BSR cell assigned routing position %d associated with port '%s' has been merged with

a BSR cell assigned routing position %d associated with port '%s'.

DESCRIPTION

In some cases, several BSR cells can be merged into a single BSR cell. For example, a single BSR control cell can control multiple three-state outputs. Another example is when a design contains a feed-through where an input port drives only an output port. In both of these cases, only a single BSR cell is required. If you assign different routing positions to two or more BSR cells that are merged into a single BSR cell, this conflict occurs.

Since a single JTAG BSR control cell can control the three-state drivers of a number of output or bidirectional ports, routing position conflicts cannot be checked if that BSR cell has been identified with different annotated port names.

For example, suppose ports **X** and **Y** have the same control cell, and you assign **X/ctl** and **Y/ctl**. When you issue the **insert_jtag** command, DFT Compiler determines whether a single control cell can control multiple ports. The **set_jtag_port_routing_order** command does not identify potential conflicts in control cell assignments.

WHAT NEXT

Assign a single routing position to the unique BSR cell formed. Eliminate duplicate specifications of routing position for control cells specified more than once. To identify duplicate specifications, check the routing positions reported in the warning message.

TEST-234 (error) JTAG component library '%s' not found.

DESCRIPTION

DFT Compiler synthesizes JTAG logic from a library of generic JTAG components called **jtag.db**. The generic components include the TAP controller, the BYPASS register, the ID register and I/O pad JTAG logic for the Boundary Scan Register (BSR) input, output and control cells.

WHAT NEXT

Since DFT Compiler must have access to **jtag.db** to synthesize JTAG logic, include **jtag.db** in the search path.

TEST-235 (information) Conflicting JTAG Boundary Scan Register (BSR) membership

specifications encountered. BSR cell optimization has pushed the '%s' BSR cell associated with port '%s' onto a port which has been excluded from the JTAG BSR.

DESCRIPTION

This error occurs when you set conflicting BSR cell requirements by excluding necessary ports from the BSR. In such cases, DFT Compiler issues warning messages TEST-236 and TEST-240, as well as this information message.

You can exclude ports from the BSR with the **set_jtag_port FALSE** *list_of_ports* command. When DFT Compiler optimizes your design, it uses the fewest BSR cells possible, and the port you excluded may be required for the BSR. For example, a single BSR control cell can control the three-state controls of many different output ports. Similarly, in the case of a feed-through line (where an input *only* feeds an output), only a single BSR cell is required.

If you exclude an input port that acts as the three-state control signal for a set of output ports, for example, the BSR will not have any control cells associated with these ports. The IEEE 1149.1 JTAG standard does not allow such a configuration.

WHAT NEXT

The name of the excluded port that caused the conflict is reported by message TEST-240. Use the **set_jtag_port TRUE** command to include the port in the BSR.

TEST-236 (warning) JTAG configuration synthesized is not compliant with the IEEE 1149.1 JTAG Standard.

DESCRIPTION

The IEEE 1149.1 JTAG Standard specifies implementations for JTAG Boundary Scan. Certain user-specified constraints cause **insert_jtag** to synthesize JTAG logic which does not comply with the standard.

WHAT NEXT

This message is always issued in conjunction with an information message that specifies the reason the configuration does not comply. Determine what action is required based on that information message.

TEST-237 (error) Unable to find pin '%s' of JTAG component '%s'
in the JTAG component library '%s'.

DESCRIPTION

DFT Compiler synthesizes JTAG logic from a library of generic JTAG components. These components include the TAP controller, the BYPASS register, the ID register and I/O pad JTAG logic for the Boundary Scan Register (BSR) input, output and control cells. All JTAG components must have the I/O pins required by the IEEE 1149.1 standard.

If DFT Compiler cannot access one of the required pins of a JTAG component, this error message is issued.

WHAT NEXT

Verify the specified component to determine whether all its pins are properly named.

TEST-238 (error) JTAG component '%s', associated with option string '%s' not found in the JTAG component library associated with this design.

DESCRIPTION

DFT Compiler selects the various JTAG components (the TAP controller, Bypass, Instruction, and Identification registers, and the various types of Boundary Scan Register cells) from a JTAG component library. You must specify a path to this library. This message is generated if DFT Compiler cannot find the component you requested in this JTAG component library.

WHAT NEXT

If the missing component is a user-specified component, check that it has been correctly identified and that it has been included in the JTAG component library under this name. If the missing component is a default component, rebuild the jtag.db to include all default components contained in the jtag.db library provided with DFT Compiler.

TEST-239 (information) %d core scan chain(s) recognized.

DESCRIPTION

DFT Compiler's JTAG synthesis supports connection of, and access to, internal (core) scan chains via the chip's JTAG Test Access Port (TAP). Core scan chains differ from the JTAG boundary scan chain, in that they are dedicated to the testing of the core design itself. In order to generate the appropriate number of JTAG instructions, DFT Compiler first analyzes the design to determine how many core scan chains exist.

If the designer has selected parallel (not daisy-chained) connection of core scan chains, a unique JTAG instruction will be defined for each core scan chain. Thus the number of core scan chains recognized will effect the size of the JTAG Instruction register (IR).

This information message simply provides information about the number of core scan chains recognized in the design by DFT Compiler.

WHAT NEXT

To recognize core scan chains, DFT Compiler keys off the port attribute and scan index number specifying each scan chain. If the number of scan chains recognized seems to be incorrect, check that each scan chain port has the proper assignment of these attributes.

If you do not want to connect internal scan chains to the TAP, invoke **insert_jtag -no_internal_scan**.

TEST-240 (information) Port '%s' BSR cell '%s' is excluded from the BSR.

DESCRIPTION

It is possible for the user to establish conflicting membership requirements when excluding certain ports from the BSR. If, for instance, using **set_jtag_port FALSE** *list_of_ports*, s/he excludes an input port which is the three-state control signal for a set of output ports, then no BSR control cells associated with these ports will exist. This is a configuration which is *not* compliant with the IEEE 1149.1 JTAG standard. When such cases are encountered by DFT Compiler, warning messages TEST-235 and TEST-236 are issued as well as this information message.

In most cases, the reported BSR cell name identifies the excluded port causing the reported port's BSR cell to be excluded.

The type (input, output or control) of BSR cell excluded is reported by TEST-235.

WHAT NEXT

To remove the non-compliance, resolve the conflict.

TEST-241 (information) BSR cell ‘%s’ shifted from position %d to position %d.

DESCRIPTION

It is possible for the user to specify erroneous Boundary Scan Register (BSR) routing order criteria if ports have been excluded from the BSR. While some of these cases can be trapped when **set_jtag_port_routing_order** is invoked, other cases can only be trapped after DFT Compiler determines which BSR cells are associated with which ports. If for instance, using **set_jtag_port FALSE** *list_of_ports*, the user excludes an input port which is the three-state control signal for a set of output ports, then no BSR control cells associated with these ports will exist. Yet if the user has specified a routing order for one or more of these excluded control cells, then the positions s/he specifies for later cells shift ‘forward’ in the BSR.

When DFT Compiler encounters such a case, it automatically shifts the positions of the remaining BSR cells. This information is reported in this error message and is duplicated in the **report_test -port** report.

This is a configuration which is *not* compliant with the IEEE 1149.1 JTAG standard. When such cases are encountered by DFT Compiler, warning messages TEST-235, TEST-236 and TEST-240 are issued as well as this information message.

WHAT NEXT

To remove the non-compliance, resolve the conflict.

TEST-242 (Warning) TAP input signal ‘%s‘ shared with a non-JTAG port.

DESCRIPTION

For JTAG TAP input ports (**TDI**, **TMS**, **TCK** and **TRST**), it is possible to synthesize a JTAG implementation where the signal fans out to the JTAG logic and the (non-JTAG) core logic. Such an implementation is not compliant with the IEEE 1149.1 JTAG standard.

WHAT NEXT

Ensure that your TAP input signal is not shared with non-JTAG logic.

TEST-243 (error) Shared output signal ‘%s‘ cannot be used as TDO.

DESCRIPTION

For JTAG TAP input ports (**TDI**, **TMS**, **TCK** and **TRST**), it is possible to synthesize a JTAG implementation where the signal fans out to the JTAG logic and the (non-JTAG) core logic. Such an implementation is not compliant with the IEEE 1149.1 JTAG standard. However is not possible to support a dual purpose **TDO** signal since this would require either synthesis of a MUX (with its associated JTAG/non-JTAG control signal) or tolerate a wired AND/wired OR configuration for this output port. Both options compromise the operation of the JTAG TDO.

Therefore in the case of a dual purpose **TDO**, this error message is generated, and JTAG synthesis is aborted.

WHAT NEXT

Remove the **set_signal_type jtag_tdo** attribute from the offending port, or ensure that that port is *not* connected to a core net.

TEST-244 (Warning) TAP port ‘%s‘ is not dedicated to JTAG. Implementation will be non-compliant.

DESCRIPTION

Rule 3.1.1(c) of the IEEE 1149.1 standard specifies that "All TAP inputs and outputs shall be dedicated connections to the component (i.e., the pins used shall not be used for any other purpose)."

Thus it is non compliant with the standard to share TAP ports with other signals (such as core scan ports). If the user executes a

set_signal_type jtag_tdi <existing_port>
set_signal_type jtag_tdo <existing_port>,
set_signal_type jtag_tms <existing_port>,
set_signal_type jtag_tck <existing_port>, or
set_signal_type jtag_trst <existing_port>Pf

where the existing port is connected to a non-TAP signal, then the synthesized JTAG implementation will be non-compliant with the standard.

One of the reasons that the resulting implementation is non-compliant with the standard is that TAP ports are automatically excluded from the JTAG Boundary Scan Register. (See warning message **UIT-93**).

WHAT NEXT

Remove the **set_signal_type** attribute from the offending port.

TEST-245 (error) Component ‘%s‘ of type ‘%s‘ is missing signal ‘%s‘.

DESCRIPTION

When DFT Compiler executes JTAG synthesis, it uses several JTAG component building blocks that are selected from the JTAG component library. These components include the TAP controller, Bypass Register, ID register, and I/O pad JTAG logic. DFT Compiler recognizes and selects JTAG library components by their names. The following default components are supplied with the JTAG component library:

	TYPE	**DEFAULT NAME**	**FUNCTION**
-	TAP	JTAG_TAP	TAP controller
-	BR	JTAG_BR	Bypass register
-	ID	JTAG_ID	Device ID register
-	IR	JTAG_IR	Instruction register
-	BSRINBOTH	JTAG_BSRINBOTHBSR	input cell
-	BSRINSET	JTAG_BSRINSETBSR	input set-only cell
-	BSRINOBS	JTAG_BSRINBOPBSR	input observe-only cell
-	BSROUTBOTH	JTAG_BSROUTBOTHBSR	output cell
-	BSROUTSETG	_BSROUTSETBSR	output set-only cell
-	BSROUTOBS	JTAG_BSROUTOBSBSR	output observe-only cell
-	BSRCTL	JTAG_BSRCTL	BSR control cell
-	BSRINCLKBOTH	JTAG_BSRINCLKBOTHBSR	clock driver cell
-	BSRINCLKSETG	_BSRINCLKSETBSR	clock driver set-only cell
-	BSRINCLKOBS	JTAG_BSRINCLKOBSBSR	clock driver observe-only cell

JTAG synthesis can be invoked using JTAG component implementations that differ from the DFT Compiler default component implementations. When the designer specifies an alternate implementation, DFT Compiler checks to see that the mandatory I/O pins associated with the specified component type exist and have the correct signal direction. These signals are specified by the IEEE 1149.1 JTAG standard.

This error message is generated if DFT Compiler could not find one of these mandatory signals. The signal may be missing or misnamed.

Checking JTAG Instruction Register (IR) implementations poses problems.

DFT Compiler supports IRs of length *N*, where 2 <= *N* <= 32 bits wide. Error-checking is executed to ensure that the required signals exist so as to permit successful JTAG synthesis.

Mandatory signals include

- **CLOCKIR**,
- **SHIFTIR**,
- **UPDATEIR**,

- **TDI** and
- **TDO**.

Certain signals must exist for all *N* bits of the IR:

- **CLEAR***N*,
- **SET***N*,
- **DI***N* and
- **DO***N*

For IRs, this check is potentially executed twice during JTAG synthesis. If the user invokes **set_jtag_implementation IR** <*custom_implementation*>, the check is executed. It is difficult to identify the desired length of the IR, however, so the check is made only for the two lowest-order bits of the IR. This is a basic sanity check for the **set_jtag_implementation** command.

When **insert_jtag** is invoked, the check is reexecuted. Now, however, DFT Compiler knows the desired size, *N*, of the IR, so it checks for the *N* low-order bits. If a problem occurs, **insert_jtag** ends gracefully.

WHAT NEXT

Correct the alternate JTAG component implementation to conform with the IEEE 1149.1 standard and DFT Compiler's JTAG signal naming conventions.

TEST-246 (error) JTAG component '%s' of type '%s': Erroneous signal '%s' direction '%s'. Must have direction '%s'.

DESCRIPTION

When DFT Compiler executes JTAG synthesis, it uses several JTAG component building blocks that are selected from the JTAG component library. These components include the TAP controller, the Bypass Register, the ID register and I/O pad JTAG logic. DFT Compiler recognizes and selects JTAG library components by their names. The following default components are supplied with the JTAG component library:

TYPEDEFAULT NAME	FUNCTION
TAPJTAG_TAP	TAP controller
BRJTAG_BR	Bypass register
IDJTAG_ID	Device ID register
IRJTAG_IR	Instruction register
BSRINBOTHJTAG_BSRINBOTH	BSR input cell
BSRINSETJTAG_BSRINSET	BSR input set-only cell
BSRINOBSJTAG_BSRINOBS	BSR input observe-only cell
BSROUTBOTHJTAG_BSROUTBOTH	BSR output cell
BSROUTSETJTAG_BSROUTSET	BSR output set-only cell
BSROUTOBSJTAG_BSROUTOBS	BSR output observe-only cell
BSRCTLJTAG_BSRCTL	BSR control cell

- **BSRINCLKBOTHJTAG_BSRINCLKBOTH**BSR clock driver cell
- **BSRINCLKSETJTAG_BSRINCLKSET**BSR clock driver set-only cell
- **BSRINCLKOBSJTAG_BSRINCLKOBS**BSR clock driver observe-only cell

JTAG synthesis can be invoked using JTAG component implementations that differ from the DFT Compiler default component implementations. When the designer specifies an alternate implementation, DFT Compiler checks to see that the mandatory I/O pins associated with the specified component type exist and have the correct signal direction. These signals are specified by the IEEE 1149.1 JTAG standard.

This error message is generated if one of the mandatory signals has an incorrect sense.

WHAT NEXT

Correct the alternate JTAG component implementation to conform with the IEEE 1149.1 standard and DFT Compiler's JTAG signal naming convention.

TEST-247 (information) Conflicting JTAG Boundary Scan Register (BSR) membership.
BSR cell optimization has pushed the BSR cell associated with port
'%s' onto JTAG Test Access Port (TAP) '%s'
which is excluded from the JTAG BSR.

DESCRIPTION

DFT Compiler optimizes the number of BSR cells required. For example, if the design includes a feed-through line (where an input only drives an output), only a single BSR cell is required. The BSR cell associated with the output port can be merged with the BSR cell associated with the input port.

However, it is an error for one of JTAG Test Access Port (TAP) signals to be included in the BSR.

- TDI: JTAG Test Data In
- TDO: JTAG Test Data Out
- TMS: JTAG Test Mode Select
- TCK: JTAG Test Clock
- TRST: JTAG Test Reset

Thus, if one of these ports acts as a feed-through line, none of the driven logic can be controlled through the BSR, and BSR cell optimization fails. Such a design is not compliant with the IEEE 1149.1 standard. If such a condition is uncovered, this error message is generated and DFT Compiler aborts JTAG synthesis.

WHAT NEXT

A design containing such a conflict probably is incorrect since TAP ports should not effect non-JTAG functionality. Make sure the driven signal is driven by a input port that can be included in the BSR.

TEST-248 (warning) JTAG Test Access Port (TAP) does not include the asynchronous reset signal TRST. A Default protocol placing the JTAG logic in transparent mode cannot be automatically generated.

DESCRIPTION

In order to automatically generate the Test Protocol required to generate test vectors for a design, DFT Compiler *must* first simulate that design. In order to execute test pattern generation on a design containing JTAG logic, the JTAG logic must be placed in transparent mode since in transparent mode, DFT Compiler can recognize and manipulate scan chains in the design. To place the JTAG logic in transparent mode, the JTAG TAP controller must be reset. There are two ways to do this; synchronously and asynchronously. If the JTAG TAP does not include an asynchronous reset signal, the TAP controller must be reset synchronously. Unfortunately, since a simulator cannot infer a known state from an unknown state, only a JTAG TAP controller with an asynchronous reset can be simulated. This error message is generate if the TAP does not include the asynchronous reset.

WHAT NEXT

If you require that DFT Compiler automatically generate the Test Protocol, invoke **insert_jtag** without the **-no_asynchronous_reset** option. If you require a design without the TAP asynchronous reset signal, manually generate the Test Protocol required for test vector generation.

TEST-249 (error) Pad exists on port '%s' to be included in the JTAG Boundary Scan Register. The pad must be removed.

DESCRIPTION

Circuits with existing pads pose a special case for JTAG synthesis. Whether or not

JTAG is invoked in **-no_pads** mode, these existing I/O pads must be removed prior to JTAG synthesis.

If the preexisting I/O pads already contain some functional logic (perhaps complete JTAG logic, perhaps just a MUX, and so on), we are unable to recognize the nature of that functionality and decide what additional JTAG logic must be synthesized for the boundary scan register (BSR). In addition, in the case of complex I/O pads (ranging from bidirectionals and three-states to complex pads containing JTAG), it is not easy to know where the "inside" of the pad is or where it ends and where the core begins. The problem is made more difficult in those technology libraries where a complex pad may be built up of some standard core components and some components that are placed in the pad region of the IC package.

For this reason, JTAG synthesis gracefully terminates in the presence of pads on those ports that are included in the BSR, and this error message is produced.

We encourage the designer to adopt a design flow that completes core design and adds test logic prior to adding pads.

WHAT NEXT

If the designer is sure that the existing I/O pads of his or her design will not conflict functionally with the synthesized JTAG logic, it is sufficient to do a group of all the core logic except the pads, submit the core to TC for **insert_jtag -no_pads**, and then replace the old core with the new core (new core to comprise the old core and the synthesized JTAG logic).

If the designer must use a specific I/O pad containing complete JTAG logic, one acceptable approach is to use

set_jtag_implementation *<bsr_component_type>* *<my_I/O_pad_type>* [*list_of_ports*]

and invoke **insert_jtag -no_pads**.

The *<bsr_component_type>* is one of the **Type**s listed below and results in replacing the associated generic component with the associated **Default Name** by *<my_I/O_pad_type>*.

TypeDefault NameBSR Cell Function

BSRINBOTHJTAG_BSRINBOTHset and observe data input cell
BSRINSETJTAG_BSRINSETset-only data input cell
BSRINOBSJTAG_BSRINOBSobserve-only data input cell
BSRINCLKBOTHJTAG_BSRINCLKBOTHset and observe clock input cell
BSRINCLKSETJTAG_BSRINCLKSETset-only clock input cell
BSRINCLKOBSJTAG_BSRINCLKOBSobserve-only clock input cell
BSROUTBOTHJTAG_BSROUTBOTHset and observe data output cell
BSROUTSETJTAG_BSROUTSETset-only data output cell
BSROUTOBSJTAG_BSROUTOBSobserve-only data output cell
BSRCTLJTAG_BSRCTLcontrol cell

This will result in instantiating the proper I/O pads with built-in JTAG logic. See

the DFT Compiler reference manual for further details.

TEST-250 (warning) Design has no bidirectional port mode information.

DESCRIPTION

During **check_test**, protocol inference needs to establish whether bidirectionals are turned inwards or outwards during scan shift.

If you used DFT Compiler to insert scan into the design, the information is annotated on the design.

This message is generated if scan is not inserted into the design, or DFT Compiler is not used, and **check_test** has to infer the direction bidirectional ports turn during scan shift.

WHAT NEXT

Study associated information messages and verify that **check_test** has inferred the correct direction.

TEST-251 (information) Test protocol assumes that bidirectional ports are turned %s during scan shift.

DESCRIPTION

During **check_test**, protocol inference needs to establish whether bidirectionals are turned inwards or outwards during scan shift.

If you used DFT Compiler to insert scan into the design, the information is annotated on the design.

If scan is not inserted into the design, or DFT Compiler is not used, **check_test** has to infer the direction bidirectional ports turn during scan shift.

This message tells you that protocol inferencing sees that you used **set_scan_configuration**, and assumes that you are preparing the design for **insert_scan**. It uses either the value you set using the **-bidi_mode** option, or the **insert_scan** default of "inwards".

WHAT NEXT

If **check_test** has not inferred the correct direction, use the **-bidi_mode** option of the **set_scan_configuration** to specify the correct direction, and run **check_test**

again.

TEST-252 (information) Test protocol assumes that bidirectional ports are turned %s during scan shift.

DESCRIPTION

During **check_test**, protocol inferencing needs to establish whether bidirectionals are turned inwards or outwards during scan shift.

If you used DFT Compiler to insert scan into the design, the information is annotated on the design.

If scan is not inserted into the design, or DFT Compiler is not used, **check_test** has to infer the direction that bidirectional ports are turned during scan shift.

This message tells you that protocol inferencing sees that you did not used the **set_scan_configuration** command, but set the value of environment variable **test_force_bidir_pads_inwards**. It assumes that you are preparing the design for **insert_test** and uses the direction appropriate to the environment variable value.

WHAT NEXT

If **check_test** has not inferred the correct direction, change the value of environment variable **test_force_bidir_pads_inwards** and run **check_test** again.

TEST-253 (information) Test protocol assumes that bidirectional ports are turned %s during scan shift.

DESCRIPTION

During **check_test**, protocol inferencing needs to establish whether bidirectionals are turned inwards or outwards during scan shift.

If you have used DFT Compiler to insert scan into the design, the information is annotated on the design.

If scan is not inserted into the design, or DFT Compiler is not used, **check_test** has to infer the direction that the bidirectional ports are turned during scan shift.

This message tells you that protocol inferencing sees that you did not used the **set_scan_configuration** command, and did not set the value of environment variable **test_force_bidir_pads_inwards**. It assumes that you are going to use the default behavior of **insert_scan** to insert scan into your design, and uses the default direction of "inwards".

WHAT NEXT

If **check_test** has not inferred the correct direction and you do not intend using **insert_test** to put scan into your design, use **set_scan_configuration** to specify the correct direction and run **check_test** again.

If you want to use **insert_test**, change the value of environment variable **test_force_bidir_pads_inwards** and run **check_test** again.

TEST-254 (information) Scan insertion turned bidirectional ports %s during scan shift.

DESCRIPTION

During **check_test**, protocol inferencing needs to establish whether bidirectionals are turned inwards or outwards turned during scan shift.

If you used DFT Compiler to insert scan into the design, the information is annotated on the design.

This information message tells you the direction that DFT Compiler turned bidirectionals.

Note that this direction does not apply to scan ports, or degenerated bidirectional ports.

WHAT NEXT

Check your test protocol.

TEST-255 (error) Can not find pin %s in the design.

DESCRIPTION

This message indicates that an internal pin of the design can not be found during insert_dft. This situation generally occur when specific synthesis options that modify the design are applied.

WHAT NEXT

Please review your synthesis options in your script before using "insert_dft" command.

TEST-258 (error) Post-insertion DRC not supported in ScanCompression mode with integration or hybrid flow

DESCRIPTION

You received this message because you are trying to run **dft_drc** post insertion in ScanCompression mode with hybrid or integration enabled, in a hierarchical adaptive scan flow. This is not supported.

WHAT NEXT

You can use TetraMAX to run DRC.

SEE ALSO

dft_drc (2)

TEST-260 (information) Inferred %s clock port %s (%.1f,%.1f).

DESCRIPTION

If you do not specify a test protocol for a design, the test design rule checker automatically infers a default protocol. Part of this process involves identifying the various clock ports of the design. The clock ports are identified by type (system, test, system/test or unused), sense (active high or active low), and default timing values (rise time and fall time as shown in this message).

WHAT NEXT

Check that the details of the inferred clock ports are suitable for your design. Use the **set_signal_type** and **create_clock** commands to specify the type and timing of clock ports if the default values are unsuitable.

TEST-261 (information) Inferred active %s asynchronous control port %s.

DESCRIPTION

If you do not specify a test protocol for a design, the test design rule checker automatically infers a default protocol. This involves identifying the ports of the design which control the state of asynchronous preset and clear signals of sequential cells. These ports are held inactive during serial shifting of scan data.

This message indicates when such a port has been inferred, and the sense (active high or active low) determined for the port.

WHAT NEXT

Check that the details of the inferred asynchronous control ports are appropriate for your design.

You can override the default protocol and the asynchronous control ports it identified by using a custom test protocol. See the **read_test_protocol** command for details.

TEST-262 (information) Inferred capture clock group : %s.

DESCRIPTION

During the parallel cycles of the scan-test sequence, the response of the design's combinational logic to applied test patterns is captured into the design's sequential cells. This is usually done by pulsing the system clocks while scan cells are configured in normal operation (parallel) mode.

For designs with multiple system clocks, not all clocks are usually active in one cycle. This is because when data is captured into cells controlled by one clock, the data at the inputs of cells controlled by a second clock may change. If both clocks were active in the same cycle, the data captured would be unpredictable. This situation occurs with two-phase latch-based design.

To ensure that data is reliably captured, test design rule checking analyzes all the clocks used to capture data and organizes them into compatible groups. All the clocks in a group can be active in the same cycle without causing unpredictable data to be captured. In many cases, each group will contain only one clock.

This message lists all the compatible clock ports which form a clock group.

WHAT NEXT

Check that the details of the inferred clock groups are appropriate for your design. The way clocks are grouped for test purposes usually reflects how they are to be used in normal operation.

TEST-263 (warning) Ignoring "test-hold" on port %s.

DESCRIPTION

This message indicates that there is a conflict between a custom test protocol (read in using the **read_test_protocol** command) and values set with the **set_test_hold**

command. The protocol and the **set_test_hold** command identify different values to be held at an input port during the parallel (normal) operation cycles of the scan-test sequence. The value (if any) specified in the protocol file takes precedence over the values set with the **set_test_hold** command.

WHAT NEXT

Edit your protocol file to reflect the values you wish to hold at input ports, or remove the attributes set with the **set_test_hold** command.

TEST-264 (information) This is a(n) %s test protocol

DESCRIPTION

This message informs you of the type of test protocol **check_test** is using in this run. The three possible types are

- inferred
- initialization
- custom

Test design rule check infers the inferred protocol from your design and test contraints. The initialization protocol comes from **read_init_protocol** for the initialization section; then, **check_test** infers the rest of the protocol. Custom test protocols are specified by the user using **read_test_protocol**.

WHAT NEXT

If the type of test protocol displayed is the type that you intended, then no further action is needed. However, if you had intended a type other than the one displayed in this message, then read in the desired type. For more information, refer to the manual pages for **read_test_protocol** and **read_init_protocol**.

TEST-265 (information) Identified %s clock port %s (%.1f,%.1f).

DESCRIPTION

You receive this information message identifying the various clock ports of the design when you run the **create_test_protocol** command.

The clock ports are identified by type (system, test, system/test or unused), sense (active high or active low), and default timing values (rise time and fall time, as shown in this message).

WHAT NEXT

Check the details of the identified clock ports and ensure that they are suitable for your design. No action is required if you want to use the default values shown.

If the default values are unsatisfactory, you can specify the clock port type with the **set_signal_type** command and specify the clock port timing with the **create_clock** command.

SEE ALSO

create_clock (2), **create_test_protocol** (2), **set_signal_type** (2).

TEST-266 (information) Identified active %s asynchronous control port %s.

DESCRIPTION

You receive this information message because you specified asynchronous signals in your design.

The test design rule checker automatically identifies the ports of the design that control the state of asynchronous preset and clear signals of sequential cells. These ports are held inactive during serial shifting of scan data.

This message indicates that such a port has been identified, and it shows the sense (active high or active low) determined for the port.

WHAT NEXT

Check that the details of the asynchronous control ports are appropriate for your design. No action is required on your part if the details are satisfactory.

However, you can override the default protocol and the asynchronous control ports it identified by using a custom test protocol. See the **read_test_protocol** command for details.

SEE ALSO

read_test_protocol (2).

TEST-267 (error) The options -infer_clock or -infer_asynch

cannot be used in the presence of an initialization test protocol.

DESCRIPTION

You receive this error message because DFT Compiler detected that a test protocol has already been loaded. This is due to a read_test_protocol -section command issued previously.

You should not infer clocks and asynchronous signals in the presence of a test protocol initialization.

WHAT NEXT

Please, use set_dft_signal command to specify clocks and asynchronous signals or do not read a test protocol if you want DFT Compiler to infer clocks and asynchronous.

SEE ALSO

read_test_protocol (2). **set_dft_signal** (2).

TEST-268 (warning) The current design contains unmapped components. The output netlist might not be read back into the system.

DESCRIPTION

This warning occurs because dft_drc detects that there are references to GTECH components in the current design. When the design is not mapped, the tool might not be able to process a netlist with unmapped components.

TEST-280 (warning) Cell %s (%s) is always asynchronously set/cleared.

DESCRIPTION

When scan data is being shifted in and out of the design under test, the asynchronous preset and clear pins of sequential cells must be held inactive. The reported cell is always asynchronously preset or cleared, so the required condition for shifting scan data cannot be met.

WHAT NEXT

To maximize fault coverage, make all internal asynchronous preset and clear pins externally controllable. You can modify the design to introduce additional logic that disables internal preset and clear signals throughout testing, or just during scan shift.

TEST-281 (information) The network contains: %s.

DESCRIPTION

This message provides additional information in support of other messages. For example, it may report the cell pins that comprise an uncontrollable asynchronous preset/clear network.

WHAT NEXT

The message that appears before this message indicates the actual problem.

TEST-282 (information) The path contains: %s.

DESCRIPTION

This message provides additional information in support of other messages. For example, it can list the pins that form a path through the circuit between two sequential cells.

WHAT NEXT

The message that appears before this one indicates the actual problem.

TEST-283 (information) Cells with this violation : %s.

DESCRIPTION

This message supports other messages that identify specific scan-test design rule violations. If multiple cells have the same rule violation, and you specified the **-verbose** option for rule checking, this message lists all the cells with the same violation.

WHAT NEXT

The message that appears before this one indicates the actual problem.

TEST-284 (information) Pins with this violation : %s.

DESCRIPTION

This message supports other messages that identify specific types of scan-test design rule violations. If there are multiple pins with the same rule violation, and the *-verbose* option is specified for rule checking, this message lists all the violated pins.

WHAT NEXT

The message preceding this message indicates the actual problem.

TEST-285 (information) Cells with this condition : %s.

DESCRIPTION

This message supports other messages that identify specific types of scan-test design rule conditions. If there are multiple cells with the same rule conditions, and the *-verbose* option has been specified for rule checking, this message lists all the similar cells.

WHAT NEXT

The message preceding this message indicates the actual condition.

TEST-286 (information) Pins with this condition : %s.

DESCRIPTION

This message supports other messages that identify specific types of scan-test design rule conditions. If there are multiple pins with the same rule condition, and the *-verbose* option is specified for rule checking, this message lists all of the similar pins.

WHAT NEXT

The message preceding this message indicates the actual condition.

TEST-287 (information) Nets with this violation : %s.

DESCRIPTION

This message supports other messages that identify specific scan-test design rule violations. If multiple nets have the same rule violation, and you specified the **-verbose** option for rule checking, this message lists all the nets with the same violation.

WHAT NEXT

The message that appears before this one indicates the actual problem.

TEST-288 (information) There is 1 other net with the same violation

DESCRIPTION

When **check_test** runs in ordinary (nonverbose) mode, it lists warnings only for the first net that violates a rule, followed by the number of additional violations. The **TEST-298** message shows that there is one additional net that violates the same rule.

WHAT NEXT

The warning message that appears before this one indicates the design rule violation. (There might also be additional information messages that provide more details about the first violation).

If you want to see details of both the violations of a rule, run **check_test** in verbose mode (check_test -verbose).

TEST-289 (information) There are %d other nets with the same violation.

DESCRIPTION

When **check_test** runs in ordinary (nonverbose) mode, it lists warnings only for the first net that violates a rule, followed by the number of additional violations. The **TEST-299** message shows the number of additional nets that violate the same rule.

WHAT NEXT

The warning message that appears before this one indicates the design rule violation. (There might also be additional information messages that provide more details about the first violation).

If you want to see details of all the violations of a rule, run **check_test** in verbose mode (check_test -verbose).

TEST-296 (information) There are %d cell%s not scanned because of area constraint.

DESCRIPTION

DFT Compiler could not satisfy the area constraint and scan as many cells as it would have liked in order to meet the fault coverage target range. Since you have specified that the area constraint takes precedence over the fault coverage target (through the **set_min_fault_coverage -area_critical** command), DFT Compiler has left out enough cells from the scan set to meet the area constraint. The set of left-out cells was chosen to have a minimal impact on testability.

WHAT NEXT

It may be that DFT Compiler is still able to meet the fault coverage target. Run the **create_test_patterns command to find out. If not, and if the fault coverage target cannot be relaxed, then the area constraint will need to be relaxed or otherwise violated.**

TEST-297 (information) There are %d cell%s not scanned because of timing constraints: %s.

DESCRIPTION

DFT Compiler could not satisfy the timing constraints and scan as many cells as it would have liked to, in order to meet the fault coverage target range. If you have specified that the timing constraints take precedence over the fault coverage target (through the **set_min_fault_coverage -timing_critical** command), DFT Compiler has left out from the scan set all the cells that would violate the timing constraints if scanned. If you have specified that the fault coverage target takes precedence, DFT Compiler has left out only the cells that would have the largest effect on timing and the smallest effect on fault coverage. In this last case, the timing constraints may be violated.

WHAT NEXT

It may be that DFT Compiler is still able to meet the fault coverage target. Run the **create_test_patterns command** to find out. If it is not able, and if the fault coverage target cannot be relaxed, you may want to resynthesize the partial scan chain forcing some or all of the rejected cells onto the scan chain (using the **set_scan true** command). Then perform a **compile -incremental** to optimize the critical paths.

TEST-298 (information) There is 1 other port with the same violation

DESCRIPTION

When **check_test** runs in ordinary (nonverbose) mode, it lists warnings only for the first port that violates a rule, followed by the number of additional violations. The **TEST-298** message shows that there is one additional port that violates the same rule.

WHAT NEXT

The warning message that appears before this one indicates the design rule violation. (There might also be additional information messages that provide more details about the first violation).

If you want to see details of both the violations of a rule, run **check_test** in verbose mode (check_test -verbose).

TEST-299 (information) There are %d other ports with the same violation.

DESCRIPTION

When **check_test** runs in ordinary (nonverbose) mode, it lists warnings only for the first port that violates a rule, followed by the number of additional violations. The **TEST-299** message shows the number of additional ports that violate the same rule.

WHAT NEXT

The warning message that appears before this one indicates the design rule violation. (There might also be additional information messages that provide more details about the first violation).

If you want to see details of all the violations of a rule, run **check_test** in

verbose mode (check_test -verbose).

TEST-300 (information) Ports with this violation : %s.

DESCRIPTION

This message supports other messages that identify specific scan-test design rule violations. If multiple ports have the same rule violation, and you specified the **-verbose** option for rule checking, this message lists all the ports with the same violation.

WHAT NEXT

The message that appears before this one indicates the actual problem.

TEST-301 (information) Extending scan in by one cycle because during the first cycle, some scan chains do not shift in data.

DESCRIPTION

The first scan-in cycle has no visible effect on the state of some scan chains.

DFT Compiler automatically adds a clock cycle to the scan pattern in order to get the last bit loaded in the scan chain.

Late-arriving data can cause this problem. The data application time is specified either in the protocol file or through the variables **test_default_delay** for input ports and **test_default_bidir_delay** for bidirectional ports. If, within a cycle, the active edges of the test clocks are before the data application time, the loading of the scan chain would be late by one clock cycle.

Other, more obvious causes of this problem include the absence of scan-in port or the presence of a scan chain break between the scan-in port and the first scan cell, or even the absence of scan chain.

WHAT NEXT

Check the presence of well-defined scan-in ports. Check the connection between the scan-in ports and the first cells of the scan chains. Check the data application time; make sure it is before the active edges of the test clocks.

TEST-302 (warning) Cell %s (%s) is not scan controllable.

DESCRIPTION

The scan-test technique depends on the ability to control (scan) and observe (measure) the state of sequential cells in the design. The state of a sequential cell is controlled by shifting scan data serially through the scan chain that contains that cell.

This technique requires that each sequential cell in a scan chain be externally controllable as well as capable of retaining a value independent of values in the other cells at the end of the scan-in sequence.

A TEST-302 violation indicates that the state of the specified cell cannot be controlled. Cells become not scan controllable due to problems involving either the asynchronous pins, data pins or clock pins. For example, if an asynchronous pin of a cell cannot be controlled (e.g. the asynchronous pin has value 'X') during scan, then the cell will fall into this category. If the clock is uncontrollable or if the clock is not pulsed, then scan-in data will not be clocked into the cell. Data cannot be successfully loaded into the cell if 1) the scan-in pin is unknown or connected to a clock signal, 2) the cell is illegally clocked, or 3) not clocked enough times during the scan-in sequence.

The local cause of the violation is printed as an information message after the TEST-302 warning message. The local cause is the event at an input pin of the cell which caused the violation. There are eight categories which define the local cause of a problem. They are the following:

(TEST-511) Asynchronous pin is uncontrollable
(TEST-515) Clock pin is uncontrollable
(TEST-512) Unknown data is clocked into cell
(TEST-518) Illegal input combinational applied to cell
(TEST-519) Clock is used as data
(TEST-516) Cell did not receive a clock pulse
(TEST-517) Cell does not contain scan-in data
(TEST-520) set_scan false applied to cell

If the problem does not fall into one of these eight categories, then no further messages will be printed.

The TEST-517 information message is used in cases where the cell was clocked, but it does not contain scan-in data from an input port at the end of the scan-in sequence. This message is followed by another information message which indicates where the data was located at the start of the scan-in sequence (TEST-525).

If TEST-511, TEST-512, or TEST-515 messages are generated due to the value of the pin being an 'X' or a 'Z', then check_test will attempt to trace back the network to find the source of the problem. Tracing will continue until an 'X' is found that cannot be traced back further in the circuit. At this point, one of six messages will be provided with the cell/pin information or port information of where tracing stopped. These six messages include:

(TEST-514) Port is unknown

(TEST-523) Port is unknown due to a set_test_isolate
(TEST-524) Port is unknown due to a previous violation
(TEST-513) Cell/pin is unknown
(TEST-521) Cell/pin is unknown due to a set_test_isolate
(TEST-522) Cell/pin is unknown due to a previous violation

Additional information about the value of the input pins for the cell where the backtracing stopped will be provided following a TEST-513 warning message. If no backtracing occurred when TEST-511, TEST-512, or TEST-515 was issued, additional information about the value of that pin will be provided. These additional information messages are TEST-541 to TEST-548:

(TEST-541) Port is <value>
(TEST-542) Port is unknown due to a set_test_isolate
(TEST-543) Port is unknown due to a previous violation
(TEST-544) Port is a scan-in value
(TEST-545) Cell/pin is <value>
(TEST-546) Cell/pin is unknown due to a set_test_isolate
(TEST-547) Cell/pin is unknown due to a previous violation
(TEST-548) Cell/pin is a scan-in value

PRIMARY AND SECONDARY VIOLATIONS

TEST-302 violations are frequently not independent, and some problems are more severe than others. One cell that is not scan controllable will cause the rest of the scan chain to be not scan controllable. Therefore check_test reports on independent and derived "not scan controllable" violations differently.

TEST-302 warning messages are only issued for cells which contain inherent controllability problems; these are considered "primary" violations. The "secondary" TEST-302 violations are cells that are not controllable as a result of primary TEST-302 violations. The secondary violations are grouped with their corresponding primary violations using the "As a result" information messages (TEST-501 and TEST-502).

Cells with primary TEST-302 violations are also included in the check_test summary section in verbose mode under "identified causes of other reported violations".

VERBOSE AND NON-VERBOSE MODE

When check_test is run in verbose mode (check_test -verbose), all primary TEST-302 violations will be printed. In non-verbose mode, one primary TEST-302 of each category (i.e. TEST-511, TEST-512, TEST-515, TEST-516, TEST-517, TEST-518, TEST-519, TEST-520) will be printed, with a count of other violations of that category. This gives an indication of the different types of scan controllability problems present in a design without listing every cell that is not scan controllable.

The number of cells with secondary TEST-302 violations is given with the corresponding primary TEST-302, and in verbose mode, the names of the cells with secondary TEST-302 violations are also provided.

The following is an example of a TEST-302 violation in verbose and non-verbose mode. The circuit consists of two 3-bit scan chains U1, U2, U3, and U4, U5, U6. In this example, the designer did not add the scan_in attribute to the scan in ports SI1 and SI2, so no scan in values are loaded into the scan chains. The check_test output in

verbose mode is as follows:

```
  Warning: Cell U1 (FD1S) is not scan controllable.
  (TEST-302)
  Information: Because it clocks in an unknown value
  from pin TI. (TEST-512)
  Information: Because port SI1 is unknown. (TEST-514)
  Information: As a result, 2 other cells are not scan
  controllable. (TEST-502)
  Information: Cells with this violation : U2, U3.
  (TEST-283)
  Warning: Cell U4 (FD1S) is not scan controllable.
  (TEST-302)
  Information: Because it clocks in an unknown value
  from pin TI. (TEST-512)
  Information: Because port SI2 is unknown. (TEST-514)
  Information: As a result, 2 other cells are not scan
  controllable. (TEST-502)
  Information: Cells with this violation : U5, U6.
  (TEST-283)
```

"Not scan controllable" messages are only printed for cells U1 and U4 although all the cells in the design are not scan controllable. These are the cells with primary TEST-302 violations and need to be investigated. In both cases, the cells clock in an 'X' from the scan-in pin, which is traced back to the values of the ports being unknown. The non-verbose check_test output for the same example is as follows:

```
  Warning: Cell U1 (FD1S) is not scan controllable.
  (TEST-302)
  Information: Because it clocks in an unknown value
  from pin TI. (TEST-512)
  Information: Because port SI1 is unknown. (TEST-514)
  Information: There is 1 other cell with the same
  violation. (TEST-173)
  Information: As a result, 4 other cells are not scan
  controllable. (TEST-502)
```

The two primary TEST-302 violations are grouped together in the non-verbose output because they are of the same category (unknown data is clocked into cell). As a result of the two primary TEST-302 violations, another 4 cells are not scan controllable.

WHAT NEXT

If your design has many sequential cells that are not scan-controllable, fault coverage may be significantly affected. Use the diagnostic messages to assist you in addressing the causes of the TEST-302 violations. Note that only cells with "primary" or independent TEST-302 violations need to be investigated. Cells with primary TEST-302 violations are also included in the check_test summary section in verbose mode in the section "identified causes of other reported violations".

You should expect some sequential cells that are not scan controllable, since this is unavoidable. An example is a JTAG boundary scan input register that only supports some of the 1149.1 instructions.

SEE ALSO

check_test

TEST-303 (information) Because asynchronous pin %s is uncontrollable.

DESCRIPTION

This message complements the uncontrollable cell warning (TEST-302) just above it.

WHAT NEXT

Examine the network driving the uncontrollable asynchronous pin to determine the deeper cause of the problem.

TEST-304 (information) Because clock pin %s is uncontrollable.

DESCRIPTION

This message complements the uncontrollable cell warning (TEST-302) just above it.

WHAT NEXT

Examine the network driving the uncontrollable clock pin to determine the deeper cause of the problem.

TEST-305 (information) Because it clocks in an unknown value from pin %s.

DESCRIPTION

This message complements the uncontrollable cell warning (TEST-302) just above it.

WHAT NEXT

Examine the network driving the uncontrollable data pins to determine the deeper cause of the problem.

TEST-306 (information) Because it scans in an unknown value from cell %s.

DESCRIPTION

This message complements the uncontrollable cell warning (TEST-302) just above it. It indicates that the source of the unknown value scaned into the violated cell is the scan cell just prior to it in the scan chain.

Note that the cell refered to in this message need not have a problem of its own: it may scan in an unknown value from its immediate predecessor.

WHAT NEXT

Examine the violations on the upstream scan cell to determine the deeper cause of the problem.

TEST-307 (warning) Segment of cell %s (%s) is not scan controllable.

DESCRIPTION

The TEST-307 warning has exactly the same meaning as TEST-302. The difference is that this message is issued in the SoC DRC context for a segment within a core instance rather than a simple sequential cell.

WHAT NEXT

Refer to the manpage for TEST-302 for more details..

Check the scan controllability of the scan segment within the cell.

SEE ALSO

check_test

TEST-308 (warning) Segment %s has sequential length

superior as chain length specified.

DESCRIPTION

You receive this warning message because a segment specified with the **-longest_chain_length** option has a sequential length superior to the chain length requested.

The DFT Compiler permits the use of the **-longest_chain_length** option of the **set_scan_configuration** command to specify the scan length you want in your design.

The DFT Compiler issues this warning message when a **-longest_chain_length** specification cannot be used.

WHAT NEXT

No action is required on your part.

However, you can eliminate the warning message by increasing the **-longest_chain_length**.

SEE ALSO

set_scan_configuration (2).

TEST-310 (warning) Data can not be captured into cell %s (%s).

DESCRIPTION

In the scan-test sequence, after pattern data has been loaded into the design (through serial shifting), the response of the design's combinational logic to the data is *captured* into the sequential cells of the design. Data is captured by pulsing the system clocks while scan cells are configured in normal operation (parallel) mode. This occurs for both full-scan and partial-scan designs, although for partial-scan designs, the cells into which the data is captured may not be scannable.

This message identifies a cell for which data cannot be captured in this manner. This is usually due to the way the cell is clocked. For example, the cell may use an internally-generated clock signal that cannot be controlled.

If data cannot be captured into a cell, faults on the data input pins of that cell and the logic connected to those pins will not be testable.

WHAT NEXT

If your design has many sequential cells into which data cannot be captured, check

the reason. In particular, check the way the cell is clocked. You may need to modify the clocking scheme by selecting an external clock rather than an internal clock for the purposes of testing.

In some cases, sequential cells into which data cannot be captured are to be expected, and are unavoidable. For example a JTAG boundary scan register contains multiple sequential cells, but system data can only be captured into one.

TEST-311 (warning) Data was captured in the master state of cell %s (%s) but scanned out of the slave state.

DESCRIPTION

There is an inconsistency between the capture of system response data and the scan-out operation for this cell. The system response data was captured in the master state of the cell, but the value in the slave state of the cell was scanned out.

There is a corresponding message (TEST-312) for the opposite problem, i.e. data was captured in the slave state of the cell, but scanned out of the master state.

WHAT NEXT

It is necessary to synchronize the captured response with the scan-out operation. In most cases this can be done by either pulsing the slave clock after the capture operation, or changing the sequence of the shift clocks to shift out of the correct state.

If your design has an inferred or initialization test protocol, you can force all slave clocks to pulse after capture by setting the variable test_infer_slave_clock_pulse_after_capture to "pulse". Similarly, you can force all the slave clocks to not pulse after capture by setting the variable to "no_pulse". To let check_test infer the behavior of the slave clocks, set the variable to "infer".

If your design has a custom test protocol, change the protocol to add a slave clock pulse after capture or modify the sequence of the shift clocks.

SEE ALSO

check_test, TEST-312

TEST-312 (warning) Data was captured in the slave state of cell

%s (%s) but scanned out of the master state.

DESCRIPTION

There is an inconsistency between the capture of system response data and the scan-out operation for this cell. The system response data was captured in the slave state of the cell, but the value in the master state of the cell was scanned out.

There is a corresponding message (TEST-311) for the opposite problem, i.e. data was captured in the master state of the cell, but scanned out of the slave state.

WHAT NEXT

It is necessary to synchronize the captured response with the scan-out operation. In most cases this can be done by either not pulsing the slave clock after the capture operation, or changing the sequence of the shift clocks to shift out of the correct state.

If your design has an inferred or initialization test protocol, you can force all slave clocks to not pulse after capture by setting the variable test_infer_slave_clock_pulse_after_capture to "no_pulse". Similarly, you can force all the slave clocks to pulse after capture by setting the variable to "pulse". To let check_test infer the behavior of the slave clocks, set the variable to "infer".

If your design has a custom test protocol, change the protocol to remove the slave clock pulse after capture or modify the sequence of the shift clocks.

SEE ALSO

check_test, TEST-311

TEST-313 (warning) Data was captured in cell %s (%s) but was lost before it was scanned out of the cell.

DESCRIPTION

There is an inconsistency between the capture of system response data and the scan-out operation for this cell.

WHAT NEXT

It is necessary to synchronize the captured response with the scan-out operation.

SEE ALSO

check_test, TEST-311, TEST-312

TEST-314 (warning) Invalid value for variable test_infer_slave_clock_pulse_after_capture, assuming "infer".

DESCRIPTION

For master-slave sequential cells it is necessary to ensure that the capture operation is synchronized with the scan-out operation. Problems include capturing in the master state and scanning out of the slave state (TEST-311), or capturing in the slave state and scanning out of the master state (TEST-312). For inferred protocols, the default behavior is for check_test to determine whether the slave clock needs to be pulsed or not after the capture operation for correct scan-out.

The variable test_infer_slave_clock_pulse_after_capture is used to override the behavior of check_test for inferred protocols. A value of "pulse" (or "true") forces all slave clocks (e.g. clocks with set_signal_type test_scan_clock_b) to pulse after capture, and a value of "no_pulse" (or "false") forces all slave clocks to not pulse after capture. The default value is "infer".

This violation indicates that the value of the variable is not one of the valid values mentioned above. check_test continues as if the value was "infer".

WHAT NEXT

Set the variable test_infer_slave_clock_pulse_after_capture to the value "infer" if you want check_test to determine whether to pulse slave clocks after capture, or set it to either "pulse" or "no_pulse" to force the behavior of slave clocks after capture.

SEE ALSO

check_test, TEST-311, TEST-312

TEST-315 (Error) Multiple clock groups cannot be pulsed in the same capture cycle.

DESCRIPTION

The variable test_force_capture_clocks indicates that all the capture clocks must be active during all capture cycles. However, the current design consists of multiple disjoint clock groups. Simultaneously pulsing clocks from different clock groups will likely result in unusable ATPG vectors. This is an error condition. No ATPG

vectors will be generated.

WHAT NEXT

In order to generate vectors, reset the test_force_capture_clocks to its default value of FALSE.

TEST-320 (warning) No nets identified for tracing by name %s.

DESCRIPTION

To debug complex scan test protocols and scan design rule violations, DFT Compiler traces the values of specified nets during rule-checking simulation. These values are identified with the **trace_nets()** statement within test protocol files. Individual hierarchical nets or hierarchical cell instances can be named with the **trace_nets()** statement. Hierarchical cell instances indicate that all nets within a cell should be traced.

This message indicates that for a name given in a **trace_nets()** statement, it was not possible to identify any nets or hierarchical cells of that name within the design.

WHAT NEXT

To resolve this problem, edit the appropriate **trace_nets()** statement within the test protocol file currently in use. After correcting the statement, read in the file again using the **read_test_protocol** command.

TEST-321 (information) Trace nets @ %.1f value %s : %s.

DESCRIPTION

To debug complex scan-test protocols and scan design rule violations, DFT Compiler traces the values of specified nets during the rule checking simulation. You can specify these values with the **trace_nets()** statement in the test protocol file.

This message reports the values at traced nets when the scan-test protocol is simulated for the design in question. The message indicates the time (within each test cycle), and value associated with the set of listed nets.

WHAT NEXT

The information in this message can help you pin-point problems in the test protocol or scan design rule violations in the design. If test design rule checking is invoked from within the Synopsys Design Analyzer, the linked report capability can select and highlight the listed nets. This allows you to see a schematic

representation of the values on different nets.

TEST-330 (error) Protocol foreach_pattern missing "parallel" cycles.

DESCRIPTION

The test protocol for a design defines the scan-test sequence by which that design is tested. The sequence must at some point place the design under test in "parallel" (normal) operation, apply patterns values to the inputs of the design, and measure the response at the outputs of the design. This message indicates that the user-specified protocol (read in with the **read_test_protocol** command) does not do what the previous sentence describes.

This failure may occur because the **foreach_pattern** loop is missing, contains no vectors, or does not contain vectors that place the design in parallel operation. Parallel operation is indicated by the presence of the pattern input/response values *Pi,Pio,Po* in the vector.

WHAT NEXT

You cannot continue with further test commands, such as the generation of test patterns, until the problem is corrected. Modify the protocol file appropriately, and read it in again using the **read_test_protocol** command.

TEST-331 (error) Pullup/pulldown net %s has illegal driver(s).

DESCRIPTION

The **check_test** command issues this message when it finds a pullup or pulldown on a net that is driven by two-state drivers.

WHAT NEXT

Correct the design violation by either a) Replacing the two-state drivers with three-state drivers or b) Removing the pullup or pulldown

TEST-332 (warning) Input pin %s of cell %s (%s) is

unconnected. It is assumed 'X' for the purpose of test.

DESCRIPTION

The specified pin has no driver. This problem was previously reported as warnings LINT-0 or LINT-3, if you have run 'check_design'. Note however that for the purpose of test generation, pins that are not properly driven are unknown. So, contrary to what was reported by check_design, DFT Compiler makes no assumption about the missing connection.

This may cause a loss in fault coverage.

WHAT NEXT

Explicitly connect the pin to an appropriate driver.

TEST-333 (information) Test pin %s of cell %s (%s) is unconnected. It is assumed inactive ('%s') for the purpose of test.

DESCRIPTION

The specified pin has no driver. This problem was previously reported as warnings LINT-0 or LINT-3, if you have run 'check_design'. Note however that since the test circuitry is not fully synthesized, DFT Compiler will assume that the pin is in its inactive state. This assumption may be different from the one stated in the LINT message, but it is consistent with the connection that will be introduced when the circuit is completed with the insert_scan command.

WHAT NEXT

Complete the synthesis of the test circuitry.

TEST-334 (information) Test pin %s of cell %s (%s) is unconnected. It is assumed inactive (0) for the purpose of test.

DESCRIPTION

You receive this information message because the specified pin does not have a driver.

If you ran the **check_design** command, you received warning messages (LINT-0 or LINT-

3) about this problem.

Since the test circuitry is not fully synthesized, the DFT Compiler assumes that the pin is in its inactive state (0). This assumption may be different from the one stated in the LINT warning message, but it is consistent with the connection that will be introduced when the circuit is completed with the **insert_scan** command.

WHAT NEXT

Complete the synthesis of the test circuitry.

SEE ALSO

check_design (2), **insert_scan** (2).

TEST-335 (information) Test pin %s of cell %s (%s) is unconnected. It is assumed inactive (1) for the purpose of test.

DESCRIPTION

You receive this information message because the specified pin does not have a driver.

If you ran the **check_design** command, you received warning messages (LINT-0 or LINT-3) about this problem.

Since the test circuitry is not fully synthesized, the DFT Compiler assumes that the pin is in its inactive state (1). This assumption may be different from the one stated in the LINT message, but it is consistent with the connection that will be introduced when the circuit is completed with the **insert_scan** command.

WHAT NEXT

Complete the synthesis of the test circuitry.

SEE ALSO

check_design (2), **insert_dft** (2).

TEST-337 (warning) Port ’%s’ cannot be used as a scan port. It

has been previously inferred as an asynchronous signal.

DESCRIPTION

You receive this warning message because the specified scan signal is ignored during test logic previewing or during the test logic insertion of your design. The test design rule checking process, run explicitly by the **check_scan** command or in the background by **scan_preview** or **scan_insertion**, inferred the specified port as an asynchronous port. The same port has been specified as a scan signal using the **set_scan_signal** command. To ensure the correct functioning of your design during test, this port must be dedicated as an asynchronous port.

WHAT NEXT

Remove the scan signal specification for this port and reexecute the command.

SEE ALSO

insert_dft (2), **preview_dft** (2), **scan_insertion** (2), **scan_preview** (2), **set_scan_signal** (2).

TEST-340 (error) Partial scan logic cannot be inserted in the presence of generic logic.

DESCRIPTION

To compute the performance and area of the design for meaningful testability trade-off analysis, partial scan designs must not contain generic logic. Generic logic is generated after a functional description of a design is read in, and before the **compile** command synthesizes an implementation of the design from the target technology library.

WHAT NEXT

Use the **compile** command to map the design to the target technology library.

TEST-341 (warning) User specification of chain '%s' has been split.

DESCRIPTION

You receive this message because DFT Compiler has been unable to determine a

functional scan chain that meets the specification, has split the specification into pieces, and has interspersed these with cells that have not been allocated to chains.

You can use the **set_scan_path** command to specify the sequence of scan cells in a chain.

WHAT NEXT

DFT Compiler builds functional chains such that each cell captures before the preceding cell launches. The specification is split to ensure this when unallocated cells are added to the chain.

You can use any of the three following ways to change the behavior:

• To direct DFT Compiler not to add cells to the chain, use the **set_scan_path** command with the **-complete** option.

• To strengthen clock domain constraints, use the **set_scan_configuration** command and do not allow DFT Compiler to mix clocks or clock edges on the same chain.

• To change test clock timing, use the **set_test_clock** command.

SEE ALSO

set_scan_configuration (2), **set_scan_path** (2), **set_test_clock** (2).

TEST-342 (warning) User specification of chain '%s' has been reordered.

DESCRIPTION

You can use the **set_scan_path** command to specify the sequence of scan cells in a chain. This message tells you that DFT Compiler has not been able to come up with a functional scan chain that meets the specification. It has had to reorder the specification.

WHAT NEXT

You see this message because DFT Compiler builds functional chains: each cell captures before its preceding cell launches. DFT Compiler has had to reorder your specification because it would have resulted in a chain that could not shift properly.

To change the behavior, add lockup latches using the **set_scan_configuration -**

add_lockup true command or modify test clock timing using the **set_test_clock** command.

TEST-343 (warning) A user-specified wire scan link overrides the insertion of a lock-up latch before cell '%s'.

DESCRIPTION

You receive this message because DFT Compiler cannot automatically insert a lock-up latch because you executed the **set_scan_path** command with a wire scan link that you defined by using the **set_scan_link** command at the lock-up latch position. DFT Compiler does not override this specification.

When you use the **set_scan_path** command to specify the sequence of scan cells in a chain, DFT Compiler analyzes the specification to ensure that it is functional; entailing that each cell must capture before its preceding cell launches. DFT Compiler may encounter cell pairs that violate this condition. It can fix the problem by automatically inserting lock-up latches if you execute the **set_scan_configuration** command with the **-add_lockup** option set to **true**.

WHAT NEXT

Decide whether you want a lock-up latch before the segment. If not, ignore the warning. Otherwise, execute the **set_scan_path** command again, omitting the offending scan link.

Alternately, you can let DFT Compiler automatically order chain elements so that lock-up latches are not needed by using the **set_scan_configuration** command with the **-add_lockup** option set to **false** before you use the **preview_scan** command.

SEE ALSO

preview_scan (2), **set_scan_configuration** (2), **set_scan_link** (2), **set_scan_path** (2).

TEST-344 (error) Cannot synchronize scan chain cells '%s' and '%s'. Both edges of clock '%s' occur before clock '%s' triggers.

DESCRIPTION

You can use the **set_scan_path** command to specify the sequence of scan cells in a chain. DFT Compiler analyzes the specification to ensure that it is functional: each cell must capture before its preceding cell launches. DFT Compiler can encounter cell pairs that violate this condition. You can let DFT Compiler resynchronize the

scan chain by automatically inserting lockup latches, by executing the command **set_scan_configuration -add_lockup true** DFT Compiler only implements lockup latch designs that are recognized by test design rule checking. Because of this, there are situations where it cannot resynchronize the scan chain. This message tells you that you have encountered one such situation. DFT Compiler has not been able to resynchronize the scan chain because both edges of the upstream clock arrive before the downstream clock trigger time.

WHAT NEXT

Let DFT Compiler order chain elements automatically so that lockup latches are not needed, by executing **set_scan_configuration -add_lockup false** before you **analyze_scan**. Alternately, study whether you can change your test clock waveforms.

TEST-345 (error) Cannot synchronize scan chain. Connects cell '%s' (triggered by an early transition of clock '%s') to cell '%s' (triggered by a later transition).

DESCRIPTION

You can use the **set_scan_path** command to specify the sequence of scan cells in a chain. DFT Compiler analyzes the specification to ensure that it is functional: each cell must capture before its preceding cell launches. DFT Compiler can encounter cell pairs that violate this condition. You can let DFT Compiler resynchronize the scan chain by automatically inserting lockup latches, by executing the command **set_scan_configuration -add_lockup true** DFT Compiler only implements lockup latch designs that are recognized by test design rule checking. Because of this, there are situations where it cannot resynchronize the scan chain. This message tells you that you have encountered one such situation. DFT Compiler has not been able to resynchronize the scan chain because it connects a cell that is triggered by an early clock transition to a cell that is triggered by a later transition.

WHAT NEXT

Let DFT Compiler order chain elements automatically so that lockup latches are not needed, by executing **set_scan_configuration -add_lockup false** before you **analyze_scan**.

TEST-346 (warning) There are %d specified scan chains. Cannot honor -chain_count specification of %d.

DESCRIPTION

DFT Compiler lets you use the **-chain_count** option of the **set_scan_configuration**

command to specify how many scan chains you want in your design. DFT Compiler also lets you specify scan chains using the **set_scan_path** command. You see this warning when DFT Compiler cannot honor your **-chain_count** specification because there are more specified scan chains than chains requested.

WHAT NEXT

Increase your **-chain_count** to make the warning go away. Alternatively, rework your **set_scan_path** assignments.

TEST-347 (warning) All specified chains are complete but %d %s not been assigned to a scan chain. Cannot honor -chain_count specification of %d.

DESCRIPTION

You receive this message because DFT Compiler cannot honor your chain count specification because it has **-chain_count** complete chains, but you have not assigned any cells to scan chains.

DFT Compiler lets you use the **set_scan_configuration** command with the **-chain_count** option to specify how many scan chains you want in the design. It also lets you use the **set_scan_path** command to specify scan chains. You can direct DFT Compiler to not add cells to chains you specify using the **set_scan_path** command with the **-complete** option.

WHAT NEXT

If you want to reduce the number of scan chains implemented, assign all cells to scan chains or use the **set_scan_path** command without the **-complete** option for specified scan chains. Otherwise, use the **set_scan_configuration** command with the **-chain_count** option to increase the **-chain_count** value to eliminate the warning.

SEE ALSO

set_scan_configuration (2), **set_scan_path** (2).

TEST-348 (warning) Only %d scan chain %s free. Cannot honor -chain_count specification of %d.

DESCRIPTION

DFT Compiler lets you use the **-chain_count** option of the **set_scan_configuration**

command to specify how many scan chains you want in your design. You will see this warning when DFT Compiler cannot honor your **-chain_count** specification because there are not enough free scan chain elements.

WHAT NEXT

If you want to increase the number of scan chains implemented, use the **-rebalance** option of the **set_scan_configuration** command to break up inferred segments. Alternatively, rework **set_scan_path** assignments. Otherwise, reduce your **-chain_count** to make the warning go away.

TEST-349 (error) Scan logic cannot be inserted in the presence of generic logic.

DESCRIPTION

To correctly identify scan equivalents and to compute the performance and area of the design for meaningful testability trade-off analysis, the design must not contain generic logic. Generic logic is generated after a functional description of a design is read in, and before the **compile** command synthesizes an implementation of the design from the target technology library.

WHAT NEXT

Use the **compile** command to map the design to the target technology library.

TEST-350 (warning) Cannot identify the core side pin of complex pad %s.
Connecting test signal to the port side.

DESCRIPTION

There is a pad on the test signal port to which the current test signal must be connected. This pad has multiple pins on its core (i.e., circuit) side. DFT Compiler cannot determine which is the data pin of the pad and what its functional relation to the port is. Therefore, the connection of the test signal is made between the port and the pad. This connection is incorrect and must somehow be modified.

Note that after the connection of test signals, the pads synthesized using the **insert_pads** command may no longer be optimal. To ensure optimal pads, the pad insertion should be done after the routing of test signals.

WHAT NEXT

You may either correct the connection by hand; choose a padless port for test signal connection and rerun **insert_test**; or remove the offending pad on the current port, rerun **insert_test** and reinsert the pad.

TEST-351 (warning) Cannot load object '%s' into chain '%s'.

DESCRIPTION

DFT Compiler recognizes sub-design scan chains, and lets users include them in scan chains using the **set_scan_path** command. This message tells you that DFT Compiler has had a problem loading a sub-design scan chain, and is discarding the specification.

WHAT NEXT

Run **check_test** on the sub-design. Make sure that **check_test** identifies the scan chain, and reports no design rule violations.

TEST-352 (warning) Scan chain '%s' has zero elements.

DESCRIPTION

DFT Compiler can generate zero-length chains when user-specified chains end up with no elements.

For example, suppose instance a of design A has two scannable cells b1 and b2. Scan specification

```
set_scan_path chain-1 a
set_scan_path chain-2 { a/b1, a/b2 }
```

produces zero-length chain chain-1.

We don't want to keep zero length chains because we don't want to synthesize feed-throughs. Instead, we delete the chain and issue this warning.

WHAT NEXT

Check your scan specification to verify that the deleted scan chain is redundant.

TEST-353 (warning) %s '%s' has elements clocked by different

clocks.

DESCRIPTION

You receive this warning message because you used the **set_scan_configuration** command with the **-clock_mixing** option to direct the DFT Compiler not to mix elements that are clocked by different clocks on the same scan chain or wrapper chain and you have violated this directive. This occurs because you can still specify scan segments, scan chains, and wrapper chains or build subdesign chains that violate the directive. The DFT Compiler then generates this warning message.

WHAT NEXT

If you intend for the identified segments or chains to violate your directive, no action is required on your part. Otherwise, respecify the segments or chains as necessary.

SEE ALSO

set_scan_configuration (2).

TEST-354 (warning) %s '%s' has elements clocked by different clock edges.

DESCRIPTION

You receive this message because you used the **set_scan_configuration** command with the **-clock_mixing** option to direct DFT Compiler not to mix elements that are clocked by different clocks or clock edges on the same scan chain and have violated this directive. This occurs because you can still specify scan segments and scan chains or build sub-design chains that violate the directive. DFT Compiler then generates this warning.

WHAT NEXT

If you intend for the identified segments or chains to violate your directive, do nothing. Otherwise, respecify them as necessary.

SEE ALSO

set_scan_configuration (2).

TEST-355 (warning) Cells with %d new incompatible clock %s

have not been assigned to scan chains. Cannot honor -chain_count specification of %d. %s

DESCRIPTION

DFT Compiler lets you say how many scan chains you want in your design. DFT Compiler also lets you specify whether to mix elements clocked using different clocks or clock edges on the same chain. You will see this warning when DFT Compiler cannot honor your **-chain_count** specification because there are more incompatible clock domains than chains requested.

Here are examples of incompatible clock domains in hierarchical scan stitching flows.

1. When the set_scan_configuration -chain_count is specified as 1, and there are two CTL segments with the capture edge as falling and the launch edge as rising (with or without latches), with a return-to-zero scan clock. These are incompatible because, if they were serially connected, the same clock pulse would shift the same data into the last scan cell of the first segment and the first scan cell of the second segment. Since these cells could not hold independent data, ATPG fault coverage would be reduced. Hence it is necessary to keep such CTL segments in two separate scan chains. In this case, since the chain count requested is 1, and two scan chains are required to accommodate the CTL segments, TEST-355 will be issued.

2. When the set_scan_configuration -chain_count is specified as 1, and all CTL segments with capture edge as falling have a latch at the end of the segment, and segments with capture edge as rising also exist in the design. This makes it impossible to avoid a falling-edge flip-flop followed by a high-enabled lockup latch followed by a rising-edge flip-flop. The high-enabled lockup latch followed by the rising-edge flip-flop creates a race condition. When no compatible falling edge segments are available, such CTL segments will be kept in a separate scan chain, and the chain count will not be respected. Hence TEST-355 will be issued.

WHAT NEXT

If you want to reduce the number of scan chains implemented, use the **-clock_mixing** option of the **set_scan_configuration** command to relax clock domain constraints. Otherwise, increase your **-chain_count** to make the warning go away.

TEST-356 (error) Segment ’%s’ has no scan-in pin.

DESCRIPTION

DFT Compiler lets you specify scan segments using the **set_scan_segment** command. This message tells you that you have specified a segment that does not have a scan-in pin. DFT Compiler then aborts.

WHAT NEXT

Add a scan-in pin to the scan segment specification using the **-access** option of the **set_scan_segment** command.

TEST-357 (error) Segment '%s' has no scan-out pin.

DESCRIPTION

DFT Compiler lets you specify scan segments using the **set_scan_segment** command. This message tells you that you have specified a segment that does not have a scan-out pin. DFT Compiler then aborts.

WHAT NEXT

Add a scan-out pin to the scan segment specification using the **-access** option of the **set_scan_segment** command.

TEST-358 (warning) Cannot use port '%s' as a '%s'. It's net has a dont_touch attribute.

DESCRIPTION

DFT Compiler lets you identify design scan ports using **set_signal_type** commands. This message tells you that you have specified a port, whose connected net is dont_touched. DFT Compiler warns you about this and uses another port.

Note that the dont_touch only affects test logic insertion. Test design rule checking will respect port protocol semantics.

WHAT NEXT

If you want DFT Compiler to use the port, remove the dont_touch attribute from the net

TEST-359 (warning) %d bidirectional %s degenerated. Please check the test protocol.

DESCRIPTION

The default protocol inferred by DFT Compiler assumes that all bidirectional ports

are turned in the same direction during scan shift. They are turned inwards or turned outwards.

This message tells you that your design has bidirectional ports whose associated pads are degenerated. They do not have bidirectional capabilities, and can only function as inputs or outputs.

WHAT NEXT

Get the test protocol inferred by DFT Compiler using **write_test_protocol**. Study how it treats the degenerated ports. If it does not treat the ports correctly, you need to develop a corrected custom test protocol.

TEST-360 (information) Because independent scan data cannot be shifted into cells %s from cell %s.

DESCRIPTION

This information message always immediately follows a TEST-361 message flagging a scan divergence.

WHAT NEXT

Check the TEST-361 message that precedes this message.

TEST-361 (Warning) Scan chain originating from port '%s' diverges after %s.

DESCRIPTION

DFT Compiler has identified a diverging scan chain. A diverging scan chain occurs when the same bit of scan data is loaded, in parallel, in at least two cells. Such scan topologies are not currently supported since it implies dependencies among the inputs of the ATPG network. DFT Compiler retains one of the diverging branches as the scan chain and marks the other branches as uncontrollable.

This message is followed by two information messages, the first one giving more details on the nature and location of the divergence, and the second one listing the cells that DFT Compiler has made uncontrollable.

WHAT NEXT

This message may be indicative of a faulty scan topology. Modify the design to fix it. If the scan topology is correct, you can suppress the warning message by

performing a **set_scan** FALSE or a **set_test_isolate** on the first diverging cell, which is listed first in the ignored cells list.

TEST-362 (Warning) Scan chain originating from '%s' is not scan observable. The chain terminates at cells %s.

DESCRIPTION

DFT Compiler has identified a scan structure originating from a **scan_in** port but not observable on any **scan_out port**. The cells listed in the message are those that are controllable from the **scan_in** port, but the cells do not propagate the scan data to any other cell. To find the wrong connection of the scan chain, these cells are the prime candidates to examine.

Note that this warning may flag a perfectly acceptable scan topology, one that has been designed *not* to be observable, such as certain forms of user-loadable registers. There is no way for DFT Compiler to guess your intent.

WHAT NEXT

This message may be indicative of a faulty scan topology. If so, fix it by modifying the design.

TEST-363 (Warning) Scan chain terminating at '%s' is not scan controllable. The chain originates from cell %s.

DESCRIPTION

DFT Compiler has identified a scan structure terminating at a scan_out port but not controllable from any scan_in port. The cell listed in the message is the one that is observable at the scan_out port but which does not propagate the scan data from any other cell. It is the prime candidate to look at for wrong connection of the scan chain. If some scan input pin of a scan cell was left unconnected, however, this message would not point to the cell with the floating input. The Design Compiler will issue a message (LINT-0 or LINT-30) and assume that this pin is tied to logic zero. As a result, DFT Compiler will not identify this cell, nor its downstream neighbors, as scan cells, since they will have constant value in scan mode. DFT Compiler will explicitly flag the constant cells as such by issuing the TEST-142 warning.

Note that this warning may flag a perfectly acceptable scan topology, one that has been designed not to be controllable, as, for example, certain forms of user-observable registers. There is no way for DFT Compiler to guess your intent.

WHAT NEXT

This message may be indicative of a faulty scan topology. If such is the case, modify the design to fix it. For more information, see messages LINT-0, LINT-30, and TEST-142.

TEST-364 (warning) Clock pin(s) of cell %s (%s) are not correctly set to their inactive state.

DESCRIPTION

The clock waveform for this clock is incorrect. If this clock waveform was inferred by **check_test**, the problem is an incorrect modeling of the library cell by the semiconductor vendor: the *clocked_on* and *timing_arcs* provide conflicting data.

To determine which pins are asynchronous, the test design rule checker checks to see whether the clocks and asynchronous pins are set to their inactive state. If so, the sequential cell will have no events. If this message occurs, the clocks are not correctly set to their inactive state. The problem is with the polarity of the clock waveforms.

WHAT NEXT

You can fix the incorrect clock waveform by using **create_test_clock**, swapping the rise and fall times to create the correct clock.

If the problem is with the library cell, contact your semiconductor vendor to correct the cell description. However, the above workaround can be used in the meantime.

TEST-365 (information) As a result, the following cells are not scan controllable: %s.

DESCRIPTION

This information message describes the effect of the warning immediately preceding it.

A sequential cell is scan controllable when it can be set to a known state by serially shifting in specific logic values during a scan shift operation. Scan cells that are not scan controllable will cause a loss in the fault coverage that the DFT Compiler ATPG can otherwise achieve.

WHAT NEXT

Study the preceding violation messages to identify the source of the problem and resolve this problem.

TEST-366 (warning) %d conditioned bidirectional %s not being forced %s. Please check the test protocol.

DESCRIPTION

The default protocol inferred by DFT Compiler assumes that all bidirectional ports are turned in the same direction during scan shift. They can be turned inwards or outwards.

This message tells you that your design has bidirectional ports that are turned in the opposite direction during scan shift.

WHAT NEXT

Get the test protocol inferred by DFT Compiler using **write_test_protocol**. Study how it treats the conditioned bidirectional ports. If it does not treat them correctly, develop a corrected custom test protocol.

TEST-367 (warning) Scan link '%s' cannot be inserted inside the segment '%s'. It will be inserted at the end of this segment.

DESCRIPTION

DFT Compiler lets you specify the order of the objects in the scan chain using the set_scan_path command. This message tells you that you have specified a scan link inside a segment. However, inserting a scan link within a segment will violate the specification of the segment. Instead insert_scan will add the link to the scan-out of the last cell in the segment.

WHAT NEXT

To suppress this warning modify the set_scan_path specification to place the link at the end of the segment.

TEST-368 (warning) Cannot build functional scan chain for segment '%s', because the user specification violates the clock

domain constraint.

DESCRIPTION

You receive this message if **preview_scan** or **insert_scan** finds a segment in your design that violates the clock domain constraint. A functional scan chain cannot be built for the specified segment unless you correct this violation.

The clock domain constraint states that sequential cells must be serially connected with regard to the clocking scheme, and the sequential cell to be clocked first must be placed at the end of the register chain. When this clock domain constraint is satisfied, each cell captures before its preceding cell launches.

WHAT NEXT

You can correct the clock domain constraint violation in one of two ways:

1. Use the **set_scan_segment** command to define a new segment specification that does not violate the clock domain constraint.

2. Alternatively, you can change the test clock timing using the **set_test_clock** command.

Then, re-execute **preview_scan** or **insert_scan**.

SEE ALSO

insert_scan (2), **preview_scan** (2), **set_scan_segment** (2), **set_test_clock** (2).

TEST-370 (warning) Scan chain %d comprises user-specified cells from different clock domains.

DESCRIPTION

By invoking the **set_scan_chain** command or the **set_test_routing_order** command, you have identified cells from different clock domains to be part of the same scan chain.

In certain instances, this situation can lead to *check_test* problems. Or, in the case of layout-dependent clock skew, it can lead to nonfunctional scan chains. To determine the pairs of consecutive cells that are clocked by different clocks, look at error messages TEST-371 and TEST-372.

WHAT NEXT

If you suspect skew problems in a scan operation, reallocate cells so that each

chain is clocked by a unique clock.

TEST-371 (warning) Consecutive scan cells %s and %s are clocked by different clocks.

DESCRIPTION

The scan chain crosses clock-domain boundaries between the two flagged cells. This situation may be of no consequence if the skew between the two clocks is well controlled. But it can result in a non-functional scan chain if the clock of the second cell is slow. Scan data would then skip this cell.

This message is a result of defining the *-multiple_clocks_chains* option of *insert_test*, or explicitly assigning cells to scan chains using the **set_scan_chain** command or the **set_test_routing_order** command.

WHAT NEXT

If there is a chance that the scan chain will be nonfunctional, undo the offending scan chain assignation command and redo *insert_test* without the *-multiple_clocks_chains*.

TEST-372 (warning) Consecutive scan cells %s and %s are clocked by different edges of the same clock.

DESCRIPTION

The scan chain crosses from a leading-edge clocked cell to a trailing-edge clocked cell. This situation usually results in a nonfunctional scan chain since scan data present at the scan input of the first cell is visible at the scan output of the second cell within one clock cycle.

This message is a result of defining the *-multiple_clocks_chains* option of *insert_test*, or explicitly assigning cells to scan chains using the **set_scan_chain** command or the **set_test_routing_order** command.

WHAT NEXT

Undo the offending scan chain assignation command and redo *insert_test* without the *-multiple_clocks_chains*.

TEST-373 (error) Sequential cell %s (%s) has no clock

information.
It will not be assigned to a scan chain.

DESCRIPTION

DFT Compiler is unable to determine what clock domain this cell belongs to. It is therefore impossible to assign this cell to a scan chain.

One possible cause of this problem is the absence of test-clock information on the library model for this cell. This problem also manifests itself if the scan-clock pin of this cell is unconnected while the rest of the design is scan routed.

WHAT NEXT

Verify the clock attributes on the library model for this cell. Make sure the design is either *fully* scan routed or *not* scan routed.

TEST-374 (warning) Clock information for all sequential cells of design is missing.

DESCRIPTION

DFT Compiler is unable to determine clock domains of any cell of the design. It is therefore impossible to assign cells to scan chains based on clock information. If no assignment is specified manually, all cells will be put in a unique chain.

One possible cause of this problem is the absence of test-clock information on the library models. This problem also manifests itself if the scan-clock pins are unconnected while the rest of the design is scan routed.

WHAT NEXT

Verify the clock attributes on the library models. Make sure the design is either *fully* scan routed or *not* scan routed.

TEST-375 (warning) Cannot add ’%s’ to chain ’%s’. It already belongs to another chain.

DESCRIPTION

DFT Compiler lets users specify scan chains using **set_scan_path** commands. This message tells you that DFT Compiler has been unable to add an element to a scan

chain because it already belongs to another chain. DFT Compiler discards the specification.

WHAT NEXT

Remove the element from the **set_scan_path** argument list to suppress the warning.

If you do want to add the element to the chain, check earlier **set_scan_path** commands to ensure that you have not specified the element inadvertently. Be particularly aware of hierarchical cell specifications. If casual inspection fails, execute the **set_scan_path** that generates the warning first. The conflicting **set_scan_path** command will fail.

TEST-376 (warning) Cannot add '%s' to chain '%s'. The element is not being scanned.

DESCRIPTION

You receive this message because DFT Compiler has been unable to add an element to a scan chain because it is not being scanned.

DFT Compiler enables you to use the **set_scan_path** command to specify scan chains. This message warns you that DFT Compiler has discarded the specification.

WHAT NEXT

Remove the element from the **set_scan_path** argument list to suppress the warning. If you want to add the element to the chain, examine earlier **check_test** commands, **set_scan** commands, and partial scan output to determine why the element is not being scanned.

SEE ALSO

check_test (2), **set_scan** (2), **set_scan_path** (2).

TEST-377 (warning) Cannot add '%s' to chain '%s'. The element already belongs to chain '%s'.

DESCRIPTION

DFT Compiler lets you specify scan chains using **set_scan_path** commands. This message tells you that DFT Compiler is unable to add an element to a scan chain because it already belongs to another chain. DFT Compiler discards the specification.

WHAT NEXT

Remove the element from the **set_scan_path** argument list to suppress the warning.

If you do want to add the element to the chain, use **remove_scan_specification** to delete the conflicting chain specification.

TEST-378 (warning) Cannot add '%s' to chain '%s'. The element already belongs to user segment '%s'.

DESCRIPTION

DFT Compiler lets you specify scan chains using **set_scan_path** commands. This message tells you that DFT Compiler is unable to add an element to a scan chain because it already belongs to a scan segment you defined using the **set_scan_segment** command. DFT Compiler discards the specification.

WHAT NEXT

Remove the element from the **set_scan_path** argument list to suppress the warning.

If you do want to add the element to the chain, use **remove_scan_specification** to delete the conflicting scan segment specification.

TEST-380 (warning) Force simulation of multiple capture clocks.

DESCRIPTION

You have defined multiple capture clocks in your test protocol.

WHAT NEXT

Remove multiple capture clocks from your test protocol.

TEST-381 (warning) Clock net '%s' is dont_touch.

DESCRIPTION

To implement the partial-scan test methodology with the multiplexed flip-flop scan style, non-scan elements that share a clock with scan elements must have their clock gated. This gating requires changes to some clock nets; the designated net has been marked by the user as *dont_touch*, preventing the modification.

WHAT NEXT

Remove the *dont_touch* attribute on the indicated net.

TEST-382 (error) Clock gating for partial scan aborted since nets that will be modified are marked as dont_touch.

DESCRIPTION

To implement the partial scan test methodology with the multiplexed flip-flop scan style, non-scan elements that share a clock with scan elements must have their clock gated. This gating requires changes to some clock nets; in this design some of these nets have been made *dont_touch*. As a result, **insert_test** has gracefully aborted.

WHAT NEXT

These nets, identified by warning **TEST-381**, should have the *dont_touch* attribute removed.

TEST-383 (warning) Cell %s (%s) is not supported because it is a sequential cell with tristate outputs. Treating as black box.

DESCRIPTION

This message indicates that the specified cell, a sequential cell with tristate outputs, is not supported by DFT Compiler. DFT Compiler treats this type of cell as a black box, which means that faults on the pins of the cell and the surrounding circuitry are untestable. Depending on the number and location of such cells, the effect on overall fault coverage may or may not be significant.

WHAT NEXT

Replace the offending cell with two separate cells: one tristate and one sequential.

TEST-384 (warning) Can’t find clock to gate for non-scan cell ’%s’.

DESCRIPTION

DFT Compiler gates the clock of valid non-scan cells to ensure that they hold their

states during scan-shift. This message tells you that DFT Compiler could not find the clock to gate for a non-scan cell.

WHAT NEXT

Examine the circuit to establish why DFT Compiler could not trace back from the cell clock pin. Look for nets that do not have exactly one driver. Expect **check_test** to warn you about the cell, and fault coverage to be reduced.

TEST-385 (warning) Cannot find the core-side hookup pin for port %s.
There are %d %s connected to it that are tristate or on pads.
Connecting test signal to a new, dedicated test signal port.

DESCRIPTION

DFT Compiler finds core-side hookup pins for test signal ports. This message tells you that DFT Compiler has not succeeded because there is not exactly one candidate pin. DFT Compiler creates a new, dedicated test signal port, and connects the test signal to that port.

WHAT NEXT

If you do not want a dedicated test signal port, you can correct the connection by hand.

TEST-386 (warning) Cannot find the core-side hookup pin for port %s.
Connecting test signal to a new, dedicated test signal port.

DESCRIPTION

DFT Compiler finds core-side hookup pins for test signal ports. This message tells you that DFT Compiler has not succeeded because a test signal port has illegal active drivers. DFT Compiler creates a new, dedicated test signal port, and connects the test signal to that port.

WHAT NEXT

If you do not want a dedicated test signal port, you can correct the connection by hand.

TEST-387 (warning) Cannot find the core-side hookup pin for port %s.
Hookup pin design instance %s has a dont_touch attribute.
Connecting test signal to a new, dedicated test signal port.

DESCRIPTION

DFT Compiler finds core-side hookup pins for test signal ports. This message tells you that DFT Compiler has not succeeded because the hookup pin it identifies is in a design instance that has a dont_touch attribute. DFT Compiler creates a new, dedicated test signal port, and connects the test signal to that port.

WHAT NEXT

If you do not want a dedicated test signal port, remove the dont_touch attribute from the design instance.

TEST-388 (warning) Cannot identify the core side pin of complex cell %s.
Connecting test signal to a new, dedicated test signal port.

DESCRIPTION

There is a cell on the test signal port to which the current test signal must be connected. This cell has multiple pins on its core (i.e., circuit) side. DFT Compiler cannot determine which is the data pin of the pad and what its functional relation to the port is. Therefore, a new, dedicated test signal port is created, and the connection of the test signal is made to the port.

WHAT NEXT

If you do not want a dedicated test signal port, you may either correct the connection by hand; choose another port for test signal connection and rerun **insert_test**; or remove the offending cell on the current port, rerun **insert_test** and reinsert the cell.

TEST-389 (warning) Cannot identify the core side pin of complex pad %s.

Connecting test signal to a new, dedicated test signal port.

DESCRIPTION

There is a pad on the test signal port to which the current test signal must be connected. This pad has multiple pins on its core (i.e., circuit) side. DFT Compiler cannot determine which is the data pin of the pad and what its functional relation to the port is. Therefore, a new, dedicated test signal port is created, and the connection of the test signal is made to the port.

WHAT NEXT

If you do not want a dedicated test signal port, you may either correct the connection by hand; choose a padless port for test signal connection and rerun **insert_test**; or remove the offending pad on the current port, rerun **insert_test** and reinsert the pad.

TEST-390 (Warning) Multiple pullups and/or pulldowns found for net '%s'.

DESCRIPTION

More than a single pullup and/or pulldown has been found for the same net. Only one is considered in test generation. A pullup and a pulldown for a single net does not make sense.

WHAT NEXT

Use only one pullup or pulldown for a net, but not both.

TEST-391 (Warning) Net '%s' is not three stateable. Removing all pullups and/or pulldowns.

DESCRIPTION

Nets that are not three statable cannot contain pullups and/or pulldowns. This warning message indicates that the offending pullups and/or pulldowns have been removed; therefore, the ATPG results will not reflect the presence of these pullups/pulldowns.

WHAT NEXT

In the future, use pullups and/or pulldowns only on three stateable nets.

TEST-392 (Warning) Disconnecting pin '%s' to route global signals.

DESCRIPTION

Scan insertion connects global methodology signals, such as test clocks and enables.

The message tells you that scan insertion has encountered a mandatory methodology signal pin that is already functionally connected. DFT Compiler removes the functional connection to route the methodology signal.

WHAT NEXT

Verify that the mission mode functionality of the circuit is not impacted.

To leave the pin functionally connected, omit it from **set_scan_segment -access** specifications.

TEST-393 (Warning) Pin '%s/%s' has a signal_type attribute %s that conflicts with its access pin type %s.

DESCRIPTION

Scan insertion lets you specify scan segments using the **set_scan_segment** command.

Scan insertion also connects up global methodology signals, such as test clocks and enables. From this, scan insertion can encounter methodology signal pins that are also scan segment access pins. The message tells you that a methodology signal pin has a signal_type attribute that conflicts with its access pin type.

The scan segment access specification overrides.

WHAT NEXT

Check the scan segment access pin type. Change it if necessary.

To remove the warning, remove the signal_type attribute from the design port that corresponds to the pin.

TEST-394 (warning) Disconnecting pin '%s' to route scan enable.

DESCRIPTION

This warning message occurs because scan insertion, which routes the scan enable signal, has encountered a scan enable pin that is already functionally connected. DFT Compiler removes the functional connection to route the scan enable.

WHAT NEXT

Verify that the mission mode utility of the circuit is not impacted. To leave the pin functionally connected, omit it from the specification set by the **set_scan_group** command **-access** option.

SEE ALSO

set_scan_group(2)

TEST-395 (Warning) Can not unscan cell '%s' of type '%s'. No target library cell has it as its scan equivalent.

DESCRIPTION

The **insert_scan** command can unscan cells that have been scan replaced by DFT Compiler.

You may unscan cells during bottom-up scan insertion. Suppose you include a cell in a scan chain at the module level. If you execute the **check_test** command at the chip level, you may discover that the cell violates a test design rule that was not visible at the module level. You may want **insert_scan** to take the cell off the scan chain and unscan it.

You will also want to unscan violated cells if you are running **insert_scan** after a test-ready compile.

DFT Compiler unscans a scan cell by searching through the target technology library for cells that have it as their scan equivalent. This warning is generated when there are no such cells. The cell is not unscanned.

WHAT NEXT

Ensure that there is at least one cell in the target technology library that has the cell that is being unscanned as its function id-based scan equivalent.

TEST-396 (warning) Cannot find the core-side hookup pin for port %s. Net %s, driven by this port, has illegal active drivers. Connecting test signal to a new, dedicated test signal port.

DESCRIPTION

You receive this message if **insert_scan** cannot find a core-side hookup pin for a test signal port, because the port has illegal active drivers. (A core-side hookup pin is the pin that connects the pad cell (port) to the design core.) This message informs you that **insert_scan** has created a new, dedicated test signal port, and connected the test signal to that port.

WHAT NEXT

If you can accept the dedicated signal port that **insert_scan** created, no action is required on your part. However, if you do not want a dedicated test signal port, you can correct the connection manually.

SEE ALSO

insert_scan (2).

TEST-397 (Warning) The scan out pin on cell '%s' in chain '%s' already drives the scan out port '%s'. No new dedicated scan out ports will be created on subdesigns.

DESCRIPTION

You receive this message if the environment variable **test_dedicated_scan_out_ports** is set to *true* but **insert_scan** cannot create a dedicated scanout port for the scanout pin on the specified cell and chain. The specified cell already drives the specified scanout port.

WHAT NEXT

If this condition is acceptable to you, no action on your part is required. Otherwise, examine the specified cell, chain, and port of your design to verify that they are as you intended. Make any changes necessary, then reexecute **insert_scan**.

SEE ALSO

insert_scan (2); **test_dedicated_scan_out_ports** (3).

TEST-398 (Warning) Can not unscan cell '%s' of type '%s'.

DESCRIPTION

You receive this message if **insert_scan** cannot unscan a test design rule violated cell. The reason the cell is unscannable could be that it has a dedicated scanout pin that drives functional logic.

You can force **insert_scan** to unscan cells that have previously been scan replaced, by executing **set_scan_element -false** and reexecuting **insert_scan**. **insert_scan** unscans a scan cell by searching through the target technology library for cells that have the specified cell as their scan equivalent.

You can unscan cells during bottom-up scan insertion. If, for example, you include a cell in a scan chain at the module level and then execute the **check_test** command at the chip level, you might discover that the cell violates a test design rule that was not visible at the module level. This could be a reason for forcing **insert_scan** to take the cell off the scan chain and unscan it.

You might also want to unscan violated cells if you are running **insert_scan** after a test-ready compile.

WHAT NEXT

If it is acceptable to you that the specified cell was not unscanned, no action on your part is required. However, if you still want the specified cell to be unscanned, first ensure that the dedicated scanout pin on the scan cell does not drive any functional logic. Then reexecute **insert_scan**.

TEST-399 (Warning) Proper hookup-pin missing for port '%s' .

DESCRIPTION

You receive this message if **insert_scan** cannot find a proper pins to the core side of identified signal ports, after jumping pads, and buffers, as needed. Specify a proper hookup-pin for the bidi port.

WHAT NEXT

See **set_scan_signal** to specify hookup pin.

TEST-400 (warning) %s '%s' has elements clocked by different clocks or same clock but different edges. Scan group

specification will be ignored.

DESCRIPTION

You receive this warning message because you used the **set_scan_group** command with elements that are clocked by different clocks or same clock but different edges. A scan group can have elements as part of its -include_elements option, that are clocked by only one clock domain of one edge only. When this message is showed, the scan group specification will be ignored during scan architecting. In other words the scan chains will be constructed without respecting the scan group specification.

If the scan group has a design instance name as part of include_elements which is already scan inserted and has scan chain elements clocked by more than one clock, the scan group specification will be ignored and the model for that instance will not be used for constructing the scan chains. Hence the elements/cells within this design instance will be considered as if it is not scan inserted and new scan chains will be constructed accordingly.

In case if the scan group needs to be respected, please ensure to respecify the set_scan_group command with elements that are clocked by only one clock and one edge.

SEE ALSO

set_scan_group

TEST-401 (warning) Synchronization element %s(%s), clocked by capture clock %s, is in an unsupported configuration.

DESCRIPTION

DFT Compiler's design rule checker (**check_test**) recognizes latches as synchronization elements when they satisfy the following criteria:

1. The enable pin is controlled from a clock port during scan shift.

2. The asynchronous control pins (if any) are held inactive during scan shift.

3. There is no set_scan false or set_scan_transparent attribute on the latch.

4. The latch has a single data port and single enable pin.

5. The latch is transparent at time of scan-in binding. (Essentially this means the enable pin is in its active state when the clock port controlling that pin is in its inactive state).

However, even if **check_test** recognizes a latch as a synchronization element, it still has to check that the particular circuit configuration, including the

synchronization element, is supported by DFT Compiler. Unsupported configurations all introduce sequential complexities that cannot be handled by ATPG or timing hazards. Therefore, if **check_test** finds an unsupported configuration, it issues a TEST-401 message and violates the synchronization element. When **check_test** violates the element, it models it as an X generator so that ATPG will not create bad patterns.

The **check_test** command uses zero-delay simulation to check the timing relationships between sequential elements in both the transitive fanin and the transitive fanout of the synchronization element. (The fanin is the cone of logic that drives the data input pin of the synchronization element. The transitive fanout is the cone of logic driven by the data output pin of the synchronization element.)

The **check_test** command checks for two unsupported configurations:

1. Sequential elements in both the transitive fanin and transitive fanout that are clocked by a different clock port, or clock ports, than the clock port driving the synchronization element's enable

If **check_test** finds this configuration, it also issues a TEST-402, with supporting TEST-403 and TEST-404 information messages to help you identify the problem.

(Note that DFT Compiler supports configurations where registers in the transitive fanin or transitive fanout of the synchronization element are clocked by one or more other clock ports. It is only when these other clock ports drive registers in both the transitive fanin and the transitive fanout that the configuration is unsupported.)

2. A synchronization element driving the data input of another synchronization element

If **check_test** finds this configuration, it also issues a TEST-405 information message, with supporting TEST-406 information messages to help you identify the problem.

WHAT NEXT

To correct the violation, you must change the circuit. Read the information messages (TEST-402 to TEST-406) that follow the TEST-401 message. Identify the circuit configuration that is not supported and correct it.

If you do not want to change the circuit configuration, you will find that the test coverage that DFT Compiler can achieve will be lowered. Try running **create_test_patterns** to see if you can still achieve a test coverage that meets your requirements.

SEE ALSO

TEST-402, **TEST-403**, **TEST-404**, **TEST-405**, **TEST-406**.

TEST-402 (information) Because some sequential cells in its

transitive fan-in and some sequential cells in its transitive fan-out are not clocked by capture clock %s.

DESCRIPTION

The **check_test** command issues this information message in support of a TEST-401 information message. It also issues one or more TEST-403 and one or more TEST-404 messages to give you more details on the unsupported configuration.

The **check_test** command issues this information message when it finds sequential elements in both the transitive fanin and transitive fanout that are clocked by a different clock port, or clock ports, than the clock port driving the synchronization element's enable.

(Note that DFT Compiler supports configurations where registers in the transitive fanin or transitive fanout of the synchronization element are clocked by one or more other clock ports. It is only when these other clock ports drive registers in both the transitive fanin and the transitive fanout that the configuration is unsupported.)

WHAT NEXT

To correct the information, you must change the circuit. Read the information messages (TEST-403 and TEST-404) that follow the TEST-402 information. These messages indicate the elements in the transitive fanin and fanout that are clocked by clocks other than the clock port that drives the synchronization element. You will need to modify your circuit such that the unsupported configuration (as previously described) no longer exists.

If you do not want to change the circuit configuration, you will find that the test coverage that DFT Compiler can achieve will be lowered. Try running **create_test_patterns** to see if you can still achieve a test coverage that meets your requirements.

SEE ALSO

TEST-401, **TEST-403**.

TEST-403 (information) Pin %s of cell %s in the transitive fan-in is clocked by capture clock %s.

DESCRIPTION

The **check_test** command issues this message in support of a preceding TEST-401 violation message and TEST-402 information message. The message identifies a sequential element in the transitive fanin of synchronization element and the

capture clock associated with it. The transitive fanin is the cone of logic that drives the data input pin of the synchronization element.

WHAT NEXT

Note the clock ports and the cells identified by this message and by any other TEST-403 and TEST-404 messages that immediately precede or follow this message.

Use this information and the WHAT NEXT section of the TEST-402 man page to identify the circuit configuration that DFT Compiler cannot support and determine if you want to fix the violation.

SEE ALSO **TEST-401**, **TEST-402**, **TEST-404**.

TEST-404 (information) Pin %s of cell %s in the transitive fan-out is clocked by capture clock %s.

DESCRIPTION

The **check_test** command issues this message in support of a preceding TEST-401 violation message and a TEST-402 information message.

The message identifies both a clock port that clocks a sequential element in the transitive fanout of the synchronization element and the sequential element that it captures. The transitive fanout is the cone of logic that the data output pin of the synchronization element drives.

WHAT NEXT

Note the clock ports and the cells identified by this message and by any other TEST-403 and TEST-404 messages that immediately precede or follow this message.

Use this information and the WHAT NEXT section of the TEST-402 man page to identify the circuit configuration that DFT Compiler cannot support and determine if you want to fix the violation.

SEE ALSO

TEST-401, **TEST-402**, **TEST-403**.

TEST-405 (information) Because a synchronization element is

in its transitive fan-in.

DESCRIPTION

The **check_test** command issues this message in support of a TEST-401 violation message. The **check_test** command also issues a TEST-406 message to identify the synchronization element in the transitive fanin.

DFT Compiler does not support two synchronization elements connected in series because this configuration is inherently subject to timing hazards. For example, if two synchronization elements with a common clock signal are in series, only detailed timing simulation can determine the final state of the second element when both latches switch off. DFT Compiler uses zero-delay simulation in ATPG and so cannot safely predict the state of the second element.

DFT Compiler will black box both synchronization elements and **create_test_patterns** will treat both of them as X sources. This will lower the fault coverage that DFT Compiler can achieve.

WHAT NEXT

To correct the violation, you must change the circuit so that you no longer have two synchronization elements connected in series. Use the TEST-401 and TEST-406 messages to identify the two synchronization elements.

If you do not want to change the circuit configuration, you will find that the test coverage that DFT Compiler can achieve will be lowered. Try running **create_test_patterns** to see if you can still achieve a test coverage that meets your requirements.

SEE ALSO

TEST-401, **TEST-406**.

TEST-406 (information) Pin %s of synchronization element %s(%s) is in the transitive fan-in.

DESCRIPTION

The **check_test** command issues this message in support of the preceding TEST-401 violation and TEST-405 information messages. The message identifies the synchronization element that is in the transitive fanin of the synchronization element identified in the preceding TEST-401 violation. The transitive fanout is the cone of logic that drives the data input pin of the synchronization element.

WHAT NEXT

To correct the violation, you must change the circuit so that you no longer have two synchronization elements connected in series. Use this message and the preceding TEST-401 message to identify the two synchronization elements.

If you do not want to change the circuit configuration, you will find that the test coverage that DFT Compiler can achieve will be lowered. Try running **create_test_patterns** to see if you can still achieve a test coverage that meets your requirements.

SEE ALSO

TEST-401, **TEST-405**.

TEST-407 (error) %s time (%10.2f) must be less than %s (%10.2f).

DESCRIPTION

Data application time/delay must happen before strobe time.

WHAT NEXT

Change strobe time, and/or delay or bidirectional delay time such that data application time happens before strobe time, and rerun create_test_patterns

SEE ALSO

create_test_clock (2), **test_default_delay** (3), **test_default_bidir_delay** (3), **test_default_strobe** (3)

TEST-421 (information) ‘SAMPLE’ instruction renamed ‘SAMPLE/PRELOAD’.

DESCRIPTION

This information message indicates that DFT Compiler considers both ‘SAMPLE/PRELOAD’ and ‘SAMPLE’ as two names for the same instruction. This instruction is called ‘SAMPLE/PRELOAD’.

WHAT NEXT

Since renaming the instruction as SAMPLE/PRELOAD does not affect the instruction codes associated with this command, there is no need to make any additional changes to the db design.

TEST-422 (warning) Mandatory instruction opcodes are not specified when using custom tap controller.

DESCRIPTION

You receive this warning message when you are using a custom tap controller during boundary scan insertion and have not specified the opcodes for the mandatory BYPASS, EXTEST and SAMPLE instructions (unless specified otherwise, SAMPLE and PRELOAD instructions are merged and share their opcodes for IEEE1149.1-2001 std. insertion).

Instruction opcodes might be implemented (fully or partially) within the tap custom controller. You must specify such opcodes (else the tool will proceed with default opcode assignments which might be inconsistent). Not doing so for mandatory instructions can potentially result in an incompliant boundary scan design.

WHAT NEXT

Examine the boundary scan preview report carefully to make sure that the opcode assignments are correct. If the automatic opcode assignment is not correct, specify the correct opcodes using set_bsd_instruction command and rerun.

SEE ALSO

insert_bsd (2), **preview_bsd** (2). **set_bsd_instruction** (2).

TEST-424 (information) TCK clock frequency ‘%e’, calculated from clock period ‘%f’, and technology library ‘%s’ time scale ‘%d’ in units of ‘%s’.

DESCRIPTION

The 1149.1 Boundary Scan Test Access Port (TAP) clock signal TCK drives the boundary scan test logic. The speed at which TCK will be operated is a function of the maximum speed of the tester and the board component in the chain of boundary scan components with the slowest TCK clock. Typically, TCK is operated at between 10 and 25 MHz. In the absense of any specification by the designer, DFT Compiler will synthesize a TCK clock which operates at 20MHz.

BSDL descriptions of 1149.1 boundary scan logic require explicit specification of TCK clock frequency.

Synthesis tasks associated with design clocks are executed using unitless specification of clock period (e.g. ‘create_clock myTCK -period 31’).

In order to calculate clock frequency, determination of the period units is required. This is done by querying the technology library into which the target design has been mapped. Two global attributes of the technology library are the time_unit_name (e.g. ns, ps) and the time_scale (e.g. 1, 10, 100) which acts as a multiplier of the period in the specified time units. For example a clock period specified as 31 in time units of ps (picoseconds) and a time_scale of 10 has a frequency = 1 / (31 * (10 * (1 / 1.0e12)).

WHAT NEXT

If this appears to be an incorrect TCK frequency, verify that the correct technology library is associated with the db design. If necessary, manually edit the generated BSDL file to provide the required frequency information.

You can specify a custom TCK clock frequency by executing boundary scan synthesis using ‘insert_jtag -tck_period <custom_period>’.

TEST-425 (warning) Unable to calculate TCK frequency for technology library ‘%s’.

DESCRIPTION

Synthesis tasks associated with design clocks are executed using unitless specification of clock period (e.g. ‘create_clock myTCK -period 31’).

BSDL files require explicit specification of TCK clock frequency. In order to calculate clock frequency, determination of the period units is required. This is done by querying the technology library into which the target design has been mapped. Two global attributes of the technology library are the time_unit_name (e.g. ns, ps) and the time_scale (e.g. 1, 10, 100) which acts as a multiplier of the period in the specified time units. For example a clock period specified as 31 in time units of ps (picoseconds) and a time_scale of 10 has a frequency = 1 / (31 * (10 * (1 / 1.0e12)).

This warning message is produced if either the time_scale or time_unit_name were unavailable for the specified library.

WHAT NEXT

First verify that the correct library is be targetted for the calculation of frequency. If not, associate the correct library with the db design. If the correct library has been identified, but one or both of the time_scale and time_unit_name attributes do not exist, work with your technology vendor to provide this

information. Then reextract the BSDL file using the write_jtag_bsdl command.

Alternately, manually edit the generated BSDL file to provide the required TCK frequency information.

TEST-427 (information) TCK clock frequency '%e', calculated from default clock period '%f', and technology library '%s' time scale '%d' in units of '%s'.

DESCRIPTION

The 1149.1 Boundary Scan Test Access Port (TAP) clock signal TCK drives the boundary scan test logic. The speed at which TCK will be operated is a function of the maximum speed of the tester and the board component in the chain of boundary scan components with the slowest TCK clock. Typically, TCK is operated at between 10 and 25 MHz. In the absense of any specification by the designer, DFT Compiler will synthesize a TCK clock which operates at 20MHz.

BSDL descriptions of 1149.1 boundary scan logic require explicit specification of TCK clock frequency.

Synthesis tasks associated with design clocks are executed using unitless specification of clock period (e.g. 'create_clock myTCK -period 31').

In order to calculate clock frequency, determination of the period units is required. This is done by querying the technology library into which the target design has been mapped. Two global attributes of the technology library are the time_unit_name (e.g. ns, ps) and the time_scale (e.g. 1, 10, 100) which acts as a multiplier of the period in the specified time units. For example a clock period specified as 31 in time units of ps (picoseconds) and a time_scale of 10 has a frequency = 1 / (31 * (10 * (1 / 1.0e12)).

WHAT NEXT

If this appears to be an incorrect TCK frequency, verify that the correct technology library is associated with the db design. If necessary, manually edit the generated BSDL file to provide the required frequency information.

If you are not satisfied with the default TCK clock frequency chosen by DFT Compiler, execute boundary scan synthesis by invoking 'insert_jtag -tck_period <custom_period>'.

TEST-428 (warning) The length of the RUNBIST signature (%d) does not equal the length of the '%s' register selected by the

RUNBIST instruction.

DESCRIPTION

This error message indicates that there is a mismatch in between the length of the Test Data Register selected by the RUNBIST instruction and the length of the signature that you have specified using the **set_bsd_runbist** command.

WHAT NEXT

Re-issue the **set_bsd_runbist** command with the correct signature length.

TEST-429 (warning) The parameters for the '%s' instruction have been defined but the instruction could not be found in the design '%s'.

DESCRIPTION

This error message indicates that you have defined the parameters for the INTEST/ RUNBIST instruction using the **set_bsd_intest** or **set_bsd_runbist** commands but the ANSI/IEEE Std.1149.1 Compliance Checker could not find the corresponding instuction in the Boundary Scan Design.

WHAT NEXT

Make sure that the RUNBIST/INTEST instructions have been implemented for the Boundary Scan Design and that the implementation is compliant with ANSI/IEEE Std.1149.1.

TEST-430 (warning) The subdesign scan chain '%s' is assumed to be non-inverting.

DESCRIPTION

You have asked scan synthesis to create non-inverting scan chains. Scan synthesis assumes that all subdesign scan chains are non-inverting. If this assumption is not true, you may end up with a scan chain that has inversions in it, even when you have asked scan synthesis to create non-inverting scan chains.

WHAT NEXT

Make sure that the specified subdesign scan chain does not have any inversions in it.

TEST-431 (warning) The scan segment '%s' is assumed to be non-inverting.

DESCRIPTION

You have asked scan synthesis to create non-inverting scan chains. Scan synthesis assumes that all scan segments that you have specified using the **set_scan_segment** are non-inverting. If this assumption is not true, you may end up with a scan chain that has inversions in it, even when you have asked scan synthesis to create non-inverting scan chains.

WHAT NEXT

Make sure that the specified scan segment does not have any inversions in it.

TEST-432 (warning) Enable pin(s) attached to the tristate port "%s" always drive the port to a high impedance value. The control port is ignored for boundary-scan insertion.

DESCRIPTION

You receive this warning message because the output port specified in your design is constantly driven to a high impedance value. If the specified port is a bidirectional port, this warning holds for the output side of the port and a BSR cell is still inserted for the input side of the port.

WHAT NEXT

Check the design and verify that you intended to always drive the output port to high impedance. Check all the enable pins on the specified port to verify that each enable pin is driven appropriately.

SEE ALSO

insert_bsd (2), **preview_bsd** (2).

TEST-433 (warning) Enable pin(s) attached to the tristate port "%s" always enable the port. The port functionality is reduced to a simple two-state output port, and no control BSR cell is attached.

DESCRIPTION

You receive this warning message when the specified output port in your design is constantly enabled. If the specified port is a bidirectional port, this warning holds for the output side of the port.

WHAT NEXT

Check the design and verify that you intended to use the tristate output port as a simple output port.

SEE ALSO

insert_bsd (2), **preview_bsd** (2).

TEST-434a (warning) Boundary-cell type BC_4 specified for the input port %s cannot be implemented. Ignoring the specification and using BC_1 type instead.

DESCRIPTION

You receive this warning message in DB mode when INTEST is implemented and you use the **set_bsd_data_cell** command to specify BC_4 to be used at a nonclock input port.

You receive this warning message in XG mode when INTEST is implemented and you use the **set_boundary_cell** command to specify BC_4 to be used at a nonclock input port.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_bsd (2), **insert_dft** (2), **preview_bsd** (2), **preview_dft** (2), **set_bsd_data_cell(2), set_boundary_cell(2), set_bsd_instruction(2).**

TEST-434 (warning) Boundary-cell type BC_2 specified for the output port %s cannot be implemented. Ignoring the specification and using BC_1 type instead.

DESCRIPTION

You receive this warning message in DB mode when INTEST is implemented and you use the **set_bsd_data_cell** command to specify BC_2 to be used at an output port.

You receive this warning message in XG mode when INTEST is implemented and you use the **set_boundary_cell** command to specify BC_2 to be used at an output port.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_bsd (2), **insert_dft** (2), **preview_bsd** (2), **preview_dft** (2), **set_bsd_data_cell(2), set_boundary_cell(2), set_bsd_instruction(2).**

TEST-435 (warning) Pad design %s cannot be validated as its access list does not specify the signal type ’port’.

DESCRIPTION

This warning message occurs when you specify the pad design to get validated (by the **-check_pad_designs** argument of the **set_bsd_configuration** command), and the **-interface** option of the **define_dft_design** command does not specify the signal type **port**.

The signal type **port** specifies the pin in the pad design instance that is connected to the design port.

WHAT NEXT

Specify the signal type **port** with the **-interface** option for the pad design in the **define_dft_design** command.

SEE ALSO

define_dft_design(2)
set_bsd_configuration(2)

TEST-436 (warning) Pin %s of pad design instance %s is not a valid enable pin.

DESCRIPTION

This warning message occurs when you specify the pad design to be validated (using the **-check_pad_designs** argument of the **set_bsd_configuration** command), and an active low value at the specified enable pin does not make the pad output inactive (high impedance). The enable pin functionality is validated for tristate and bidirectional pad designs.

WHAT NEXT

Specify the correct pin for the **enable** or **enable_inverted** signal type in the **-access_list** of the pad design in DB mode. If applicable, use the **set_bsd_compliance** command to specify a compliance enable pattern at the compliance enable ports of the design.

Specify the correct polarity for the **enable** signal type in the **-interface** of the pad design in XG mode. If applicable, use the **set_bsd_compliance** command to specify a compliance enable pattern at the compliance enable ports of the design.

SEE ALSO

define_dft_design(2)
set_bsd_compliance(2)
set_bsd_configuration(2)

TEST-437 (warning) Data cannot propagate correctly from pin %s to pin %s of pad design instance %s.

DESCRIPTION

This warning message occurs when you specify the pad design to be validated (using the **-check_pad_designs** argument of the **set_bsd_configuration** command), and the functionality of the data pin could not be established during validation.

WHAT NEXT

Verify that the following information is correct:

• Specify the correct pin in the **-access_list** for the pad design for the **data_in**, **data_in_inverted**, **data_out**, and **data_out_inverted** signal types in DB mode.

• Specify the correct pin polarity in the **-interface** for the pad design for the **data_in**, **data_out** signal types in XG mode.

• Check that the signal types polarities are correct.

• Specify the correct **enable** or **enable_inverted** pin for tristate and bidirectional pads in DB mode.

• Specify the correct polarity of **enable** pin for tristate and bidirectional pads in XG mode.

• Specify the correct **port** pin.

• If applicable, use the **set_bsd_compliance** command to specify a compliance enable pattern at compliance enable ports of the design.

SEE ALSO

define_dft_design(2)
set_bsd_compliance(2)
set_bsd_configuration(2)

TEST-438 (error) TDO port (%s) pad does not have an enable pin.

DESCRIPTION

This error message occurs because the enable pin was not found for the TDO (test data out) port pad. The TDO port must have a 3-state pad and an enable pin.

WHAT NEXT

Correct the design, ensuring that the following information is accurate:

• Specify the correct pin in the **-access_list** for the pad design for the **data_in**, **data_in_inverted**, **data_out**, and **data_out_inverted** signal types in DB mode.

• Specify the correct pin polarity in the **-interface** for the pad design for the **data_in**, **data_out** signal types in XG mode.

• Specify the signal types with the correct polarities.

• Specify the correct **port** pin for tristate and bidirectional pads.

• Specify the correct **enable** or **enable_inverted** pin in DB mode.

• Specify the correct polarity of **enable** pin in XG mode.

• If required, use the **set_bsd_compliance** command to specify the values to put on other pins.

SEE ALSO

define_dft_design(2)
set_bsd_compliance(2)
set_bsd_configuration(2)

TEST-439 (error) %s port(%s) is not a valid TAP port.

DESCRIPTION

You get this error when a bidirection port is used as a TAP port and the port pad is not of the correct type. The port pad for TCK, TMS, TDI or TRST should be either an input pad or a bidirectional pad reduced to an input pad by disabling the output side. The port pad used for the TDO port should be either a tristate pad or a bidirectional pad whose input side is not used. According to section 3.1.1(c) IEEE std. 1149.1, all TAP inputs and outputs should be dedicated connections to the component and should not be used for any other purpose.

WHAT NEXT

Correct the design by providing correct pad configuration at the specified TAP port. Make sure that the TAP port is not used for any other purpose.

SEE ALSO

check_bsd (2), **insert_bsd** (2), **insert_dft** (2), **define_dft_design** (2).

TEST-440 (information) Combinational feedback loop is disabled at pin %s of cell %s (%s) by constant values.

DESCRIPTION

Test design rule checking has identified a combinational feedback loop in the design which was disabled by logic 0 in the circuit, logic 1 in the circuit, set_test_assumes, or set_test_holds. The command set_test_hold does not have any effect on custom test protocols. However, for custom test protocols, constants are those values which are the same through the foreach pattern section of the test protocol.

check_test has broken the combinational feedback loop at the point where it was logically disabled so no additional coverage was lost because of the break point. **create_test_patterns** requires all feedback loops to be disabled because in the faulty state of the circuit, the feedback loop may no longer be disabled.

WHAT NEXT

If you don’t agree with the break point, change the constant values in the circuit.

TEST-441 (information) Combinational feedback loop is disabled at pin %s of cell %s (%s) by logical values present during initialization.

DESCRIPTION

Test design rule checking has identified a combinational feedback loop in the design which was disabled by logic values present in the circuit after simulating the foreach program section of the test protocol.

The logic values present at this point may not be present for the rest of the protocol.

WHAT NEXT

If this is a bad place to break the combinational feedback loop, use set_test_isolate to break it in a particular place. You can also use set_test_hold to create constants in the circuit which break the feedback loop.

TEST-442 (error) Length not specified for the test data register %s.

DESCRIPTION

You get this error message during "insert_bsd" or "preview_bsd" in the debug flow (i.e. when the value of the "-flow" option of "set_bsd_configuration" is set to debug and the length is not specified for the user test data register.

WHAT NEXT

Specify the length of the test data register and rerun insert_bsd/preview_bsd.

SEE ALSO

set_bsd_configuration (2). **set_bsd_register** (2).

TEST-443 (error) Undefined BSR %s cell %s specified for port %s.

DESCRIPTION

You get this error message in DB mode during "insert_bsd" or "preview_bsd" when the set_bsd_data_cell or set_bsd_control_cell specification provided for a port refers to a bsr element that has not been defined. This may happen either due to incorrect BSR element name used in the set_bsd_data_cell or set_bsd_control_cell specification or due to a missing definition of the intended BSR element.

You get this error message in XG mode during "insert_dft" or "preview_dft" when the set_boundary_cell specification provided for a port refers to a bsr element that has not been defined. This may happen either due to incorrect BSR element name used in the set_boundary_cell specification or due to a missing definition of the intended BSR element.

WHAT NEXT

Correct the BSR element name in the set_bsd_data_cell or set_bsd_control_cell command OR provide a set_bsd_bsr_element definition for the named BSR and rerun insert_bsd/preview_bsd in DB mode.

Correct the BSR element name in the set_boundary_cell OR provide a define_dft_design definition for the named BSR and rerun insert_dft/preview_dft in XG mode.

SEE ALSO

set_bsd_bsr_element (2), **define_dft_design** (2), **set_bsd_data_cell** (2), **set_bsd_control_cell** (2), **set_boundary_cell** (2).

TEST-444 (error) Invalid type %s of BSR data cell %s specified for the direction %s of port %s.

DESCRIPTION

You get this error message in DB mode during "insert_bsd" or "preview_bsd" when the set_bsd_data_cell specification provided for a port is found to be invalid, due to the invalid bsr cell type for the port direction.

You get this error message in XG mode during "insert_dft" or "preview_dft" when the set_boundary_cell specification provided for a port is found to be invalid, due to the invalid bsr cell type for the port direction.

The allowed BSR cell types are as follows:

Input (or input side of an Inout port) - BC_1, BC_2, BC_4 Output (or output side of an Inout port) - BC_1, BC_2 Inout - BC_7

WHAT NEXT

Specify a correct type of BSR element at the port and rerun insert_bsd/preview_bsd in DB mode.

Specify a correct type of BSR element at the port and rerun insert_dft/preview_dft in XG mode.

SEE ALSO

set_bsd_bsr_element (2), **define_dft_design** (2), **set_bsd_data_cell** (2), **set_boundary_cell** (2).

TEST-445 (error) BSR element %s type %s does not match with the type %s in control cell specification.

DESCRIPTION

You get this error message in DB mode during "insert_bsd" or "preview_bsd" when the set_bsd_control_cell specification provided for a port refers to a bsr element whose type that does not match with the control cell type specified in the command. Note that the allowed types for control bsr cells are BC_1 and BC_2.

You get this error message in XG mode during "insert_dft" or "preview_dft" when the set_boundary_cell specification provided for a port refers to a bsr element whose type that does not match with the control cell type specified in the command. Note that the allowed types for control bsr cells are BC_1 and BC_2.

WHAT NEXT

Specify a control bsr cell with correct type and rerun insert_bsd/preview_bsd in DB mode.

Specify a control bsr cell with correct type and rerun insert_dft/preview_dft in XG mode.

SEE ALSO

set_bsd_bsr_element (2), **define_dft_design** (2), **set_bsd_control_cell** (2), **set_boundary_cell** (2).

TEST-446 (error) %s is not a valid compliance enable port.

DESCRIPTION

This error message occurs when a bidirectional port is used as a compliance enable port and the port pad is not of the correct type. The port pad for a compliance enable port must be either an input pad or a bidirectional pad reduced to an input pad.

WHAT NEXT

Correct the design by providing the correct pad configuration at the specified compliance enable port. Make sure that the compliance enable port is not used for any other purpose.

SEE ALSO

check_bsd(2)
define_dft_design(2)
insert_bsd(2)

TEST-447 (error) Non-compliant Boundary Scan logic will be synthesized.
Inverting three-state output drivers encountered.

DESCRIPTION

The IEEE 1149.1 Boundary Scan Standard requires that the output of a Boundary Scan Register (BSR) cell not be inverted before it exits the chip through the chip’s io pad. Rules 10.4.1e and 10.6.1l of IEEE Std 1149.1a-1993 require that the polarity of the system output equal the polarity of the TDO output of the BSR cell.

This error message is generated because one or more output ports have three-state drivers that invert their data signals. As a result, the BSR cells associated with these output ports will also have their data signals inverted, in violation of the Boundary Scan Standard.

This error invalidates some of the fundamental assumptions about data accessed through the chip’s TAP port by downstream test tools. In particular, by violating rule 10.4.1e, it violates rule 10.6.1l of the standard. As a result, Boundary Scan Description Language (BSDL) file descriptions of these ports by downstream tools will be misleading.

WHAT NEXT

Modify your design so that that the boundary-scan configuration complies with the

standard; otherwise, there will be significant problems with downstream testing. You can make the boundary-scan configuration compliant in one of two ways.

First, if your library contains non-inverting three-state output cells, for each output port in the boundary scan register, replace each inverting three-state output cell in your original design by a non-inverting three-state output cell, preceded by an inverter. (If necessary, use the *set_dont_use* command to ensure selection of the correct library cells.) Then, reinvoke **insert_jtag**.

Second, as an alternative, modify the configuration synthesized by DFT Compiler by inserting an inverter on each side of the BSR cell associated with the data signal of each offending port. Insert one inverter directly in front of the DI port of the BSR cell. Insert the other inverter directly after the DO port of the BSR cell. While Rule 10.4.1 (e) of IEEE Std 1149.1-1990 states that there shall be no logic between any boundary-scan register cell and the system pin to which that cell is connected, transparent devices such as buffers and I/O buffers are not considered to be "logic" and may exist outside the boundary-scan register. Inverters may also exist outside the boundary-scan register subject to conformance to rules 10.5.1h, 10.5.1i, 10.6.1i, 10.6.1k, 10.6.1l, 10.6.1m, and 10.6.1n. (Gates, flip-flops, latches, and other devices that perform logical operations are considered to be logic devices and must not be placed outside the boundary-scan register.)

For example, consider this illegal configuration:

```
        CORE-------->inverting_buffer
```

To achieve a legal boundary scan configuration while maintaining the desired logical behavior, place the serial string inverter->BSR_Cell->inverter between the CORE and the inverting buffer, as follows:

```
CORE----->inverter----->BSR_Cell---->inverter---->inverting_buffer
```

Notice that, although the inverted output still occurs before the BSR cell, the net output of the BSR cell itself is not inverted. The inverters meet the requirements of rules 10.6.1l and 10.6.1m.

TEST-448 (warning) %s instruction cannot be implemented as the user data register %s specified for the instruction is not found. Removing the instruction.

DESCRIPTION

You get this warning when the test data register specified for a user instruction does not exist. This may happen either due to a missing specification for the test data register or due to incorrect test data register name used in the set_bsd_instruction command.

WHAT NEXT

Check the test data register specified for the instruction. Either correct the test data register name or provide a definition for the test data register using set_bsd_register command in DB mode.

Check the test data register specified for the instruction. Either correct the test data register name or provide a definition for the test data register using set_scan_path and set_dft_signal commands in XG mode.

SEE ALSO

insert_bsd (2), **insert_dft** (2), **set_bsd_instruction(2), set_bsd_register(2), set_scan_path(2), set_dft_signal(2).**

TEST-449 (error) Wired logic driving output port '%s' encountered.

DESCRIPTION

Currently DFT Compiler's boundary scan synthesis capability does not support designs containing output ports driven by wired logic.

WHAT NEXT

It is possible that the wired logic is the result of a user error. Run **check_design** on your design and make sure that all warning messages can be ignored.

TEST-451 (warning) Cell %s (%s) is unknown (black box) because functionality for output pin %s is bad or incomplete.

DESCRIPTION

Test design rule checking has identified that this output or three-state pin does not have a function described in the library. Test design rule checking requires that all outputs/three-states have functions defined in order to recognize the functionality of the cell. If any output/three- state does not have a function specified, the entire cell will be black-boxed as is the case here.

check_test, **create_test_patterns**, and **write_test** will treat this cell as a black box.

WHAT NEXT

You should either use a different library cell or contact your vendor/library developer to fix this cell.

TEST-452 (warning) Cell %s (%s) is unknown (black box) because output pin %s is always an X.

DESCRIPTION

Test design rule checking has identified that this output or three-state pin's function specifies that this output is always an X. Test design rule checking requires that all outputs/three-states have functions other than an X in order to recognize the functionality of the cell. If any output/three-state can only be an X, the entire cell will be black-boxed as is the case here.

check_test, **create_test_patterns**, and **write_test** will treat this cell as a black box.

WHAT NEXT

You should either use a different library cell or contact your vendor/library developer to fix this cell.

TEST-453 (warning) Cell %s (%s) is unknown (black box) because output pin %s is three-state but does not have a three-state function specified.

DESCRIPTION

Test design rule checking has identified that this pin is a three-state through attributes on the library cell. However, the three_state function is not specified in the library for this particular cell. In other words, there is no function specified for the tree-state enable. Test design rule checking requires that all three-state outputs have functions specifed for their enable pins. If this is not the case, the entire cell will be black-boxed as is the case here.

check_test, **create_test_patterns**, and **write_test** will treat this cell as a black box.

WHAT NEXT

You should either use a different library cell or contact your vendor/library developer to fix this cell.

TEST-454 (information) Because the information in the library db is incomplete
or inconsistent. For this cell, the current version of Library Compiler
issues the following message(s):
"%s"

DESCRIPTION

DFT Compiler requires that the functionality of all sequential cell be unique and explicit. The information about this perticular cell is either incomplete or inconsistent, preventing the construction of a DFT Compiler usable model. Please refer to the reported LIBG message(s) to understand the exact nature of the problem.

WHAT NEXT

You should either use a different library cell or contact your vendor/library developer to fix this cell.

TEST-455 (Error) Protocl cannot be generated for %s instruction as the instruction is not implemented."

DESCRIPTION

You get this error when you try to generate the protocol for an instruction which is not implemented. Check the preview_bsd report to make sure that the instruction exists there.

WHAT NEXT

Implement the instruction first by providing a specification for the instruction. Then rerun insert_bsd and the write_bsd_protocol command.

SEE ALSO

set_bsd_instruction insert_bsd preview_bsd

TEST-456 (Warning) OBSERVE_ONLY BSR cell %s specified for port % is not of the type BC_4. Using the default BC_4 BSR

cell.

DESCRIPTION

You get this warning in DB mode during insert_bsd/preview_bsd when you specifed BSR cell with '-function OBSERVE', but the type of the BSR cell is not BC_4.

You get this warning in XG mode during insert_dft/preview_dft when you specifed BSR cell with '-function OBSERVE', but the type of the BSR cell is not BC_4.

WHAT NEXT

Specifiy a BSR cell of type BC_4 and rerun insert_bsd/preview_bsd in DB mode.

Specifiy a BSR cell of type BC_4 and rerun insert_dft/preview_dft in XG mode.

SEE ALSO

set_bsd_data_cell (2) **set_boundary_cell** (2) **insert_bsd** (2), **insert_dft** (2), **preview_bsd** (2), **preview_dft** (2).

TEST-457 (warning) Pin '%s' is not found in design, the UDR '%s' is ignored.

DESCRIPTION

This warning message occurs when the user test data register (UDR) specified has a pin that is not found in the design. The **insert_dft** command ignores the user test data register after displaying this error message. The hookup pins specified in the scan path of user data registers with the **set_scan_path** command, or hookup pins specified with the **set_dft_signal** command must be present in the design.

WHAT NEXT

Check the user test data register specified for the instruction. When using the **set_dft_signal** or **set_scan_path** command, use only the pins in the hookup pins list that are present in the design.

SEE ALSO

insert_dft(2)
set_bsd_instruction(2)
set_dft_signal(2)
set_scan_path(2)

TEST-461 (warning) Generic sequential cell %s (%s) is not supported because both clocks are used. This cell is being black-boxed.

DESCRIPTION

Test design rule checking has identified that this cell is not supported because this cell is using a generic sequential cell with both clocked_on and enable hooked up to the circuit. A supported sequential element cannot have more than one non-test clock. If both the edge sensitive, clocked_on, and level sensitive, enable, clocks are hooked up for generic sequential cells, the cell will be black boxed by test design rule checking.

check_test, **create_test_patterns**, and **write_test** will treat this cell as a black box.

WHAT NEXT

You should not use both an edge sensitive and level sensitive clock for a single sequential cell.

TEST-462 (warning) Cell %s (%s) is not supported because it has too many states (%s states). This cell is being black-boxed.

DESCRIPTION

Test design rule checking has identified that this cell is not supported because the corresponding library cell is not a supported single bit device. A supported single bit device cannot have more than 4 states. The only supported single bit device with four states is a master-slave latch pair with set/reset pins on each state. If the cell has more than 4 states, it is black-boxed. The warning message specifies how many states were found for this library cell.

check_test, **create_test_patterns**, and **write_test** will treat this cell as a black box.

WHAT NEXT

You should either use a different library cell or contact your vendor/library developer to fix this cell.

Library cell developers should use report_lib -table to determine the number of states in a library cell.

TEST-463 (warning) Master-slave cell %s (%s) is not supported because state pin %s is neither a master nor a slave. This cell is being black-boxed.

DESCRIPTION

Test design rule checking has identified that this master-slave cell is not really a master-slave cell. The only cells that we support are single bit flip flops and master-slave latch pairs. Although this cell has more than one state, this cell is not a master-slave latch pair. A master-slave latch pair must have level-sensitive latches where the master latch feeds the slave latch. The slave latch must only get its data from the master latch. If the cell is not a recognized flip-flop or master-slave latch pair, then it is black-boxed.

check_test, **create_test_patterns**, and **write_test** will treat this cell as a black box.

WHAT NEXT

You should either use a different library cell or contact your vendor/library developer to fix this cell.

Library cell developers should use report_lib -table to look at the library description of the cell.

TEST-464 (warning) Master-slave cell %s (%s) is not supported because there are two or more master states. This cell is being black-boxed.

DESCRIPTION

Test design rule checking has identified that this master-slave cell is not really a master-slave cell. The only cells that we support are single bit flip flops and master-slave latch pairs. Although this cell has more than one state, this cell is not a master-slave latch pair. A master-slave latch pair must have level-sensitive latches where the master latch feeds the slave latch. The slave latch must only get its data from the master latch. In this case, test design rule checking determined that two distinct states fed slave state(s). However, test design rule checking only allows one master latch to feed a slave latch. If the cell has more than one master-state, then it is black-boxed.

check_test, **create_test_patterns**, and **write_test** will treat this cell as a black box.

WHAT NEXT

You should either use a different library cell or contact your vendor/library developer to fix this cell.

Library cell developers should use report_lib -table to look at the library description of the cell.

TEST-465 (warning) Master-slave cell %s (%s) is not supported because there are two or more slave states. This cell is being black-boxed.

DESCRIPTION

Test design rule checking has identified that this master-slave cell is not really a master-slave cell. The only cells that we support are single bit flip flops and master-slave latch pairs. Although this cell has more than one state, this cell is not a master-slave latch pair. A master-slave latch pair must have level-sensitive latches where the master latch feeds the slave latch. The slave latch must only get its data from the master latch. In this case, test design rule checking determined that two distinct states are fed from a master latch. However, test design rule checking only allows one slave latch. If the cell has more than one slave state, then it is black-boxed.

check_test, **create_test_patterns**, and **write_test** will treat this cell as a black box.

WHAT NEXT

You should either use a different library cell or contact your vendor/library developer to fix this cell.

Library cell developers should use report_lib -table to look at the library description of the cell.

TEST-466 (warning) Cell %s (%s) is not supported because the state pin %s has no clocks. This cell is being black-boxed.

DESCRIPTION

Test design rule checking has identified that this cell is not supported because all sequential cells must have clocks. Test design rule checking has determined that this state of this cell does not have any clocks, therefore it is black-boxed.

check_test, **create_test_patterns**, and **write_test** will treat this cell as a black

box.

WHAT NEXT

You should either use a different library cell or contact your vendor/library developer to fix this cell.

Library cell developers should use report_lib -table using libgen_debug_ebst=87 to determine the clocks of each state.

TEST-467 (warning) Cell %s (%s) is not supported because the state pin %s is multi-port. This cell is being black-boxed.

DESCRIPTION

Test design rule checking has identified that this cell is not supported because it requires that all states of sequential cells can only have one non-test clock and one data input. Test design rule checking has determined that this state of this cell has too many data or non-test clocks. Therefore it is black-boxed.

check_test, **create_test_patterns**, and **write_test** will treat this cell as a black box.

WHAT NEXT

You should either use a different library cell or contact your vendor/library developer to fix this cell.

Library cell developers should use report_lib -table using libgen_debug_ebst=87 to determine the clocks of each state.

TEST-468 (warning) Cell %s (%s) is not supported because it is a sequential cell with three-state outputs. This cell is being black-boxed.

DESCRIPTION

This message identifies sequential cells with three-state outputs. This type of cell is treated as a *black-box*, which means that faults on the pins of the cell and the surrounding circuitry are untestable. Depending on the number and location of such cells, the effect on overall fault coverage may or may not be significant.

check_test, **create_test_patterns**, and **write_test** will treat this cell as a black box.

WHAT NEXT

This message appears when you are using a sequential cell with tristate outputs. This cell is not supported. This cell will be treated as a black-box cell.

The only way to get around this problem is to replace this cell with two distinct cells, separate tristate and sequential cells.

TEST-469 (Information) Test protocol inference terminated with errors.

DESCRIPTION

This message tells you that **infer_test_protocol** terminated because of errors. The user must fix these errors before continuing. The error(s) are usually associated with user specifications.

WHAT NEXT

Provide the spcifications requested.

TEST-470 (Information) Test design rule checking terminated with errors.

DESCRIPTION

This message tells you that **check_test** terminated because of errors. The user must fix these errors before continuing. The error(s) are associated with the timing specified by the user.

WHAT NEXT

Fix the timing by using **create_test_clock**, **test_default_period**, **test_default_delay**, **test_default_bidir_delay**, **test_default_strobe**, or **test_default_strobe_width**.

TEST-471 (warning) Asynchronous control pin %s of cell %s (%s) can change in the capture cycle. This can cause the cell to

capture unreliably.

DESCRIPTION

You receive this warning message if **check_test** detects a condition where an asynchronous control pin might not remain stable while response data is being captured. This condition causes a capture violation, so that ATPG cannot predict the captured state, regardless of the input pattern applied. Warning messages indicate a test design rule violation and warn you of the possibility of reduced fault coverage. If you want this cell to be testable, you must correct the situation that causes the unreliable capture.

During the parallel cycle of the scan-test sequence, the response of internal combinational logic to the applied test pattern is captured into the sequential cells in the design. This is usually done by applying a system (normal operation) clock pulse.

To ensure that data is reliably captured, the values being captured into a cell must depend on the scanned-in state of sequential cells in the fan-in cone of that cell. In general, the captured data value must depend only on scanned-in state, valid non-scan state (for partial scan), and primary input values. In addition, asynchronous control pins of the cell must remain remain inactive when response data is being captured by the data pins of a sequential cell.

Unreliable capture can occur when the response value captured in a register can asynchronously affect the response value captured in another register. This condition can occur if there is a combinational path between the output of one sequential cell and the asynchronous control pin of another sequential cell, the source and destination registers are clocked by the same clock port, and the combinational path between the two registers is not disabled by constants present in the design.

Examples of unreliable capture conditions caused by an asynchronous path between source register and destination register include the following:

• A combinational path between the output of a negative edge-triggered flip-flop and the asynchronous control pin of a positive edge-triggered flip-flop, clocked by the same clock port.

• A combinational path between the output of a latch and the asynchronous control pin of another register, both clocked by the same clock port.

When DFT Compiler detects an unreliable capture condition of this type, it marks the asynchronous control pin of the destination register with a violation, and ATPG does not use the cell for observing fault effects.

Following this message, DFT Compiler issues diagnostic messages describing the conditions at the source and destination registers that cause this violation.

WHAT NEXT

If you receive this message, proceed as follows:

1. Locate and identify the cause of the unreliable capture, by doing any or all of the following:

• Read the diagnostic messages that follow this warning message, and the messages following **check_test** execution.

• Use **Design Analyzer** to view the violation. For more information, see the *Design Analyzer Reference Manual*.

• Read the related extended error messages TEST-472, TEST-476, TEST-479, and TEST-559.

2. Modify your design to correct the violating condition. For more information, see Chapter 6 of the *DFT Compiler Test Design Rule Checking User Guide*.

3. Re-execute **check_test** to verify that the violation has been corrected.

SEE ALSO

check_test (2); **TEST-472** (n), **TEST-476** (n), **TEST-479** (n), **TEST-559** (n); *Design Analyzer Reference Manual*, *DFT Compiler Test Design Rule Checking User Guide*.

TEST-472 (information) Cell %s launches response data from pin %s at %s edge of clock port %s (pin %s) at time %s.

DESCRIPTION

This is one of the diagnostic messages, issued following the unreliable capture warning messages (TEST-471 and TEST-478) to help you identify and correct the cause of the unreliable capture problem.

This message is a companion message to TEST-473 or TEST-476, and describes the cause of the unreliable capture problem as it relates to the source register when response data is launched from that register at a clock transition in the capture cycle. The message is to be interpreted as follows:

• Cell %s is the source register from which response data launches.

• pin %s is the output pin of the source register.

• %s edge is the transition (rising or falling) of the clock when response data launches.

• clock port %s is the name of the clock port that is the source of the clock signal.

• (pin %s) is the launching register’s clock pin that is affected by the transition at the clock port.

• time %s is the time that the clock transition occurs in the capture cycle, assuming zero delay.

WHAT NEXT

Follow the instructions in the WHAT NEXT section of the TEST-471 or TEST-478 extended warning messages, using the information in this diagnostic message to help find the cause of the problem.

SEE ALSO

check_test (2); **TEST-471** (n), **TEST-473** (n), **TEST-476** (n), **TEST-477** (n), **TEST-478** (n), **TEST-479** (n), **TEST-559** (n); *Design Analyzer Reference Manual*, *DFT Compiler Test Design Rule Checking User Guide*.

TEST-473 (information) Cell %s captures data on pin %s at %s edge of clock port %s (pin %s) at time %s.

DESCRIPTION

This is one of the diagnostic messages, issued following the unreliable capture warning message TEST-478 to help you identify and correct the cause of the unreliable capture problem.

This message is a companion message to TEST-472, and describes the cause of the unreliable capture problem as it relates to the destination register. The message is to be interpreted as follows:

• Cell %s is the destination register where response data is to be captured.

• pin %s is the synchronous input pin of the destination register.

• %s edge is the transition (rising or falling) of the clock when response data is to be captured in the destination register.

• clock port %s is the source of the clock signal.

• (pin %s) is the target register's clock pin that is affected by the transition at the clock port.

• time %s is the time that clock transition occurs in the capture cycle, assuming zero delay.

WHAT NEXT

Follow the instructions in the WHAT NEXT section of the TEST-478 extended warning message, using the information in this diagnostic message to help find the cause of the problem.

SEE ALSO

check_test (2); **TEST-472** (n), **TEST-476** (n), **TEST-477** (n), **TEST-478** (n), **TEST-479** (n), **TEST-559** (n); *Design Analyzer Reference Manual*, *DFT Compiler Test Design Rule Checking User Guide*.

TEST-474 (information) There is a path from %s to %s.

DESCRIPTION

This is one of the diagnostic messages, issued following the unreliable capture warning messages (TEST-478 and TEST-471) to help you identify and correct the cause of the unreliable capture problem.

This message tells you that there is a path from the source (identified by the preceding TEST-472, TEST-479 or TEST-559 violation) to the destination register (identified by the preceeding TEST-473, TEST-476 or TEST-477 violation).

Details of the path are shown in the companion TEST-282 violation that immediately follows this violation message.

WHAT NEXT

Follow the instructions in the WHAT NEXT section of the TEST-471 or TEST-478 extended warning message, using the information in this, and the accompanying diagnostic messages to help find the cause of the problem.

SEE ALSO

check_test (2); **TEST-282** (n), **TEST-471** (n), **TEST-472** (n), **TEST-473** (n), **TEST-476** (n), **TEST-477** (n), **TEST-478** (n), **TEST-479** (n), **TEST-559** (n); *Design Analyzer*

Reference Manual, DFT Compiler Test Design Rule Checking User Guide.

TEST-476 (information) Response data launched from the source register can cause a change on asynchronous control pin %s of cell %s.

DESCRIPTION

This is one of the diagnostic messages, issued following the unreliable capture warning message TEST-471 to help you identify and correct the cause of the unreliable capture problem.

Unreliable capture can occur when the response value captured in a register can asynchronously affect the response value captured in another register. This condition can occur if there is a combinational path between the output of one sequential cell and the asynchronous control pin of another sequential cell, the source and destination registers are clocked by the same clock port, and the combinational path between the two registers is not disabled by constants present in the design. When DFT Compiler detects this condition, it issues the TEST-471 warning.

This message describes the cause of the unreliable capture problem as it relates to the destination register. The message is to be interpreted as follows:

• pin %s is the asynchronous control pin of the destination register affected by the launche of captured response data from the source register.

• cell %s is the destination register.

WHAT NEXT

Follow the instructions in the WHAT NEXT section of the TEST-471 extended warning message, using the information in this diagnostic message to help find the cause of the problem.

SEE ALSO

check_test (2); **TEST-471** (n), **TEST-472** (n), **TEST-479** (n).

TEST-477 (information) Enable pin %s of cell %s becomes

active at %s edge of clock port %s at time %s.

DESCRIPTION

This is one of the diagnostic messages, issued following the unreliable capture warning message TEST-478 to help you identify and correct the cause of the unreliable capture problem.

This message describes the cause of the unreliable capture problem as it relates to the destination register when that register is level-sensitive and becomes transparent at the resting value of the clock. The message is to be interpreted as follows:

• Enable pin %s is the destination register enable pin that is affected by the transition at the clock port.

• Cell %s is the destination register where response data is to be captured.

• %s edge is the transition (rising or falling) of the clock when the clock returns to its resting value. The enable pin of the destination register becomes active at this edge.

• clock port %s is the source of the clock signal.

• time %s is the time that clock transition occurs in the capture cycle, assuming zero delay.

This diagnostic message is displayed, for example, when there is a Q-to-D path between a negative edge-triggered flip-flop and an enabled low latch, clocked by the same return-to-zero clock source. In this case, the destination latch captures response data at the rising edge (first edge) of the clock. The source flip-flop launches captured (or response) data at the falling edge (second edge) of the clock. However, the destination latch becomes transparent at the falling edge of the clock and the initial captured value of that cell is overwritten by the newly-launched response data from the source register.

WHAT NEXT

Follow the instructions in the WHAT NEXT section of the TEST-478 extended warning message, using the information in this diagnostic message to help find the cause of the problem.

SEE ALSO

check_test (2); **TEST-472** (n), **TEST-473** (n), **TEST-478** (n), **TEST-479** (n), **TEST-559** (n); *Design Analyzer Reference Manual*, *DFT Compiler Test Design Rule Checking User Guide*.

TEST-478 (warning) Pin %s of cell %s (%s) cannot capture reliably.

DESCRIPTION

You receive this warning message if **check_test** detects a condition that causes a capture violation, so that ATPG cannot predict the captured state, regardless of the input pattern applied. Warning messages indicate a test design rule violation and warn you of the possibility of reduced fault coverage. If you want this cell to be testable, you must correct the situation that causes the unreliable capture.

During the parallel cycle of the scan-test sequence, the response of internal combinational logic to the applied test pattern is captured into the sequential cells in the design. This is usually done by applying a system (normal operation) clock pulse.

To ensure that data is reliably captured, the values being captured into a cell must depend on the scanned-in state of sequential cells in the fan-in cone of that cell. In general, captured data value must depend only on scanned-in state, valid non-scan state (for partial scan), and primary input values.

Unreliable capture occurs if a combinational path exists between two sequential elements that are clocked by the same clock source, and the signals at the clock pins of these two elements are not properly aligned. The captured value of the destination element depends on the response value of the source element instead of the scanned-in value.

This message indicates that a particular pin of the sequential cell cannot perform the capture operation reliably because one or more of the sequential cells in the fan-in cone of that pin launches response (captured) data before response data is captured by that pin.

For example, for a combinational path between two enabled-high latches clocked by the same return-to-zero clock, both devices are transparent while the clock is active. When the clock becomes inactive (falling edge of the clock), the destination latch can capture the value originally on its data pin or the response (capture) value launched from the source latch at the rising edge of the clock. This depends on the relationship between the clock width and the delay on the data path, and causes the destination latch to capture unreliably.

Other examples of unreliable capture conditions caused by source register launch before destination register capture include the following:
• A Q-to-D path between a positive edge-triggered flip-flop and a negative edge-triggered flip-flop, clocked by the same return-to-zero clock source. In this case, the response data launched from the source flip-flop at the rising edge of the clock can arrive at the synchronous input of the destination register before the falling edge of the clock.

• Q-to-D path between a negative edge-triggered flip-flop and an enabled low latch, clocked by the same return-to-zero clock source. In this case, the destination latch captures response data at the rising edge (first edge) of the clock. The source flip-flop launches captured (or response) data at the falling edge (second edge) of

the clock. However, the destination latch becomes transparent at the falling edge of the clock and the initial captured value of that cell is overwritten by the newly-launched response data from the source register.

When DFT Compiler detects an unreliable capture condition of this type, the pin of the destination register, indicated in the TEST-477 message, is marked with a violation; ATPG does not use this pin for observing fault effects in the register. Note that ATPG uses other data pins of the cell (if any) for observing fault effects as long as those pins are not violated.

Following this message, DFT Compiler issues diagnostic messages describing the conditions at the source and destination registers that cause this violation.

WHAT NEXT

If you receive this message, proceed as follows:

1. Locate and identify the cause of the unreliable capture, by doing any or all of the following:

• Read the diagnostic messages that follow this warning message, and the messages following **check_test** execution.

• Use **Design Analyzer** to view the violation. For more information, see the *Design Analyzer Reference Manual*.

• Read the related extended error messages TEST-472, TEST-473, TEST-477, TEST-479, and TEST-559.

2. Modify your design to correct the violating condition. For more information, see Chapter 6 of the *DFT Compiler Test Design Rule Checking User Guide*.

3. Re-execute **check_test** to verify that the violation has been corrected.

SEE ALSO

check_test (2); **TEST-472** (n), **TEST-473** (n), **TEST-477** (n), **TEST-479** (n), **TEST-559** (n); *Design Analyzer Reference Manual*, *DFT Compiler Test Design Rule Checking User Guide*.

TEST-479 (information) Cell %s launches response data from pin %s prior to the start of the capture cycle.

DESCRIPTION

This is one of the diagnostic messages, issued following the unreliable capture

warning messages (TEST-478 and TEST-471) to help you identify and correct the cause of the unreliable capture problem.

This message describes the cause of the unreliable capture problem as it relates to the source register when response data is launched from that register before the start of the capture cycle. The message is to be interpreted as follows:

- Cell %s is the source register where response data is launched.

- pin %s is the output pin of the register that launches response data.

This diagnostic message is displayed, for example, if the source register is an enabled-low latch clocked by a return-to-zero clock. In this case, the latch is transparent at the start of the capture cycle, and response data is launched from that register before the start of the capture cycle (at the one-to-zero transition of the clock in the last scan shift cycle).

WHAT NEXT

Follow the instructions in the WHAT NEXT section of the TEST-478 extended warning message, using the information in this diagnostic message to help find the cause of the problem.

SEE ALSO

check_test (2); **TEST-471** (n), **TEST-472** (n), **TEST-473** (n), **TEST-476** (n), **TEST-477** (n), **TEST-478** (n), **TEST-559** (n); *Design Analyzer Reference Manual*, *DFT Compiler Test Design Rule Checking User Guide*.

TEST-480 (error) The following compliance enable port is a TAP port: '%s'.

DESCRIPTION

The **set_bsd_compliance** command lets you specify a compliance enable pattern for a Boundary Scan design. Each compliance enable pattern consists of a set of port_name-value pairs. No compliance enable pattern may include a TAP port.

WHAT NEXT

Remove the TAP ports from the compliance pattern specification.

TEST-481 (error) The following compliance enable ports are

TAP ports:

DESCRIPTION

The **set_bsd_compliance** command lets you specify a compliance enable pattern for a Boundary Scan design. Each compliance enable pattern consists of a set of port_name-value pairs. No compliance enable pattern may include a TAP port.

WHAT NEXT

Remove the TAP ports from the compliance pattern specification.

TEST-482 (error) The '%s' port in the port-to-pin map for the package '%s' is not a port of the design '%s'.

DESCRIPTION

You receive this message if **read_pin_map** finds a port in the port-to-pin mapping file that is not found in the design db file. The signal ports in each port-to-pin mapping file must match those in the design db file.

WHAT NEXT

If you receive this message, proceed as follows:

1. Check the port-to-pin mapping file and the design db file for syntax errors and any spelling errors or typos that would cause the port names to not match.

2. If no such errors are found, either remove the port from the port-to-pin mapping file or add it to the design db file.

SEE ALSO

create_bsd_patterns (2), **read_pin_map** (2), **write_bsdl** (2).

TEST-484 (warning) The '%s' port of the design '%s' is missing from the port-to-pin map for the package '%s'.

DESCRIPTION

You receive this message if **read_pin_map** finds a port in the design db file that is not found in the port-to-pin mapping file. The signal ports in each port-to-pin

mapping file must match those in the design db file.

WHAT NEXT

If you receive this message, proceed as follows:

1. If this port is a no-connect port, nothing needs to be done.

2. Otherwise, check the port-to-pin mapping file and the design db file for syntax errors and any spelling errors or typos that would cause the port names to not match.

3. If no such errors are found, either remove the port from the design db file or add it to the port-to-pin mapping file.

SEE ALSO

create_bsd_patterns (2), **read_pin_map** (2), **write_bsdl** (2).

TEST-485 (warning) The following ports of the design '%s' are missing from the port-to-pin map for the package '%s'.

DESCRIPTION

You receive this warning message when the **read_pin_map** command finds ports in the design db file that are not found in the port-to-pin mapping file. The signal ports in each port-to-pin mapping file must match those in the design db file.

WHAT NEXT

No action is required if the ports are no-connect ports.

Otherwise, check the port-to-pin mapping file and the design db file for syntax errors, spelling errors, or typos that might cause differences between the port names.

If no such errors are found, either remove the port from the design db file or add it to the port-to-pin mapping file.

After your changes are complete, rerun the **read_pin_map** command.

SEE ALSO

create_bsd_patterns (2), **read_pin_map** (2), **write_bsdl** (2).

TEST-486 (warning) The maximum line length specified must be at least %d. Using a value of %d as the maximum line length.

DESCRIPTION

You receive this message if the environment variable **test_bsdl_max_line_length** has a value less than 50 characters. The maximum line length must be at least as many characters as 50; if it is not, **write_bsdl** uses 50 as the line length.

WHAT NEXT

If it is acceptable for **write_bsdl** to use a maximum line length of 50 characters, you do not need to do anything. However, if you want the maximum line length to be greater than 50 characters, set the value of the **test_bsdl_max_line_length** to the value you want, and re-execute **write_bsdl**.

SEE ALSO

write_bsdl (2); **test_bsdl_max_line_length** (3).

TEST-486b (warning) The maximum line length specified must be at most %d. Using a value of %d as the maximum line length.

DESCRIPTION

You receive this message if the environment variable **test_bsdl_max_line_length** has a value greater than 132 characters. The maximum line length must be at most 132 characters; if it is not, **write_bsdl** uses 132 as the line length.

WHAT NEXT

If it is acceptable for **write_bsdl** to use a maximum line length of 132 characters, you do not need to do anything. However, if you want the maximum line length to be less than 132 characters, set the value of the **test_bsdl_max_line_length** to the value you want, and re-execute **write_bsdl**.

SEE ALSO

write_bsdl (2); **test_bsdl_max_line_length** (3).

TEST-487 (Information) Opened BSDL file '%s' for writing.

DESCRIPTION

This message informs you that the BSDL generation subsystem has successfully opened the specified output file for writing.

WHAT NEXT

This is an informational message only. No action is required on your part.

TEST-488 (error) No valid packages were found for the design '%s'.

DESCRIPTION

This error message indicates that either no packages were found for the Boundary Scan Design, or that the pin map files read in for the Boundary Scan Design have errors.

WHAT NEXT

Check the pin map files and ensure that there is at least one valid package read in for the design. Correct any typos or spelling errors that might prevent packages from being read in. Then re-execute **read_pin_map**.

TEST-489 (warning) No default device package has been specified for the design '%s'.

DESCRIPTION

You receive this warning message if **insert_bsd** detects that you have multiple packages in your pin map file but have not selected a default package for the Boundary Scan Design.

WHAT NEXT

Use **set_bsd_configuration -default_package** to specify which of the packages in your pin map file you want to use as the default. Or, modify your pin map file so that it contains only the package you want to use.

TEST-490 (error) No signal ports were found for the design '%s'.

DESCRIPTION

This error message indicates that no signal ports were found for the design.

WHAT NEXT

Make sure that the design has at least one port.

TEST-491 (warning) No linkage ports were found for the design '%s'.

DESCRIPTION

This warning message indicates that no linkage ports were found for the design.

WHAT NEXT

Any design typically has at least one VDD and at least one GND port. Add these ports to the port-to-pin map files for the design.

TEST-492 (warning) BSDL atom '%s' is longer than the maximum number of characters allowed in a line.

DESCRIPTION

The BSDL generation subsystem fits as many BSDL atoms on a line as possible without exceeding the maximum line length permissible. If an atom is longer than the maximum permissible line length, the BSDL generation subsytem generates this warning and prints the atom by itself on a new line.

WHAT NEXT

Make sure that the atom length is smaller than maximum permissible line length.

TEST-493 (warning) The following %s name %sis an illegal

BSDL identifier: ’%s’.

DESCRIPTION

Valid BSDL identifiers can only have letters, digits, underscores, or periods. Valid BSDL identifiers must start with a letter. They cannot end with an underscore or have adjacent underscores. The BSDL generation subsystem produces this warning if an identifier in the design does not obey the previous rules.

WHAT NEXT

Make sure that the identifier obeys the BSDL naming rules.

TEST-494 (warning) The following %s names %sare illegal BSDL identifiers:

DESCRIPTION

Valid BSDL identifiers can only have letters, digits, underscores, or periods. Valid BSDL identifiers must start with a letter. They cannot end with an underscore or have adjacent underscores. The BSDL generation subsystem produces this warning if an identifier in the design does not obey the previous rules.

WHAT NEXT

Make sure that the identifier obeys the BSDL naming rules.

TEST-495 (warning) The following %s name %sis a %s reserved word: ’%s’.

DESCRIPTION

This warning message indicates that an identifier in the design is a BSDL or VHDL reserved word.

WHAT NEXT

Make sure that the identifier is not a BSDL or VHDL reserved word.

TEST-496 (warning) The following %s names %sare %s

keywords:

DESCRIPTION

This warning message indicates that some identifiers in the design are BSDL or VHDL reserved words.

WHAT NEXT

Make sure that the identifiers are not BSDL or VHDL reserved words.

TEST-497 (warning) The TCK frequency has not been specified. Using a default value of 10.0 MHz as the TCK frequency.

DESCRIPTION

This warning message is produced if the Boundary Scan Test Clock frequency has not been specified.

WHAT NEXT

Use the **create_clock** command to specify the Boundary Scan Test Clock frequency.

TEST-498 (information) Successfully generated BSDL file '%s'.

DESCRIPTION

This information message indicates that the BSDL generation subsytem has successfully generated the BSDL file for the Boundary Scan Design.

WHAT NEXT

No further action is needed.

TEST-499 (warning) Violations occurred during IEEE 1149.1

compliance checking.

DESCRIPTION

This warning message indicates that the boundary scan design has certain features that are not compliant with ANSI/IEEE Std. 1149.1. Therefore, BSDL generation cannot proceed.

WHAT NEXT

Run the **check_bsd** command and fix the compliance problems.

TEST-500 (warning) Physical design information is not available. The preview_scan command is running in -command insert_scan mode.

DESCRIPTION

This warning message indicates that the physical design information is not present so that the command **preview_scan** can be used in the reoptimize_design context.

The **preview_scan** is then run in default mode, the insert_scan mode.

WHAT NEXT

You need to run the **read_clusters** command in order to read in the physical design information. Please see the **reoptimize_design** documentation for more details.

TEST-501 (information) As a result, 1 other cell is not scan controllable.

DESCRIPTION

This message is used in conjunction with the TEST-302 violation message just above it.

Cells which contain inherent controllability problems are reported as TEST-302 violation messages. The number of cells which are uncontrollable as a result of the TEST-302 violation is provided in this message, which in this case is one.

This message is issued in both the verbose and non-verbose modes of check-test. In verbose mode this message is followed by a list of the cell names.

WHAT NEXT

Investigate the reason why the cell given in the TEST-302 message is uncontrollable, and re-run check_test when this problem is fixed.

SEE ALSO

check_test, TEST-302

TEST-502 (information) As a result, %d other cells are not scan controllable.

DESCRIPTION

This message is used in conjunction with the TEST-302 violation message just above it.

Cells which contain inherent controllability problems are reported as TEST-302 violation messages. The number of cells which are uncontrollable as a result of the TEST-302 violation is provided in this message.

This message is issued in both the verbose and non-verbose modes of check-test. In verbose mode this message is followed by a list of the cell names.

WHAT NEXT

Investigate the reason why the cell given in the TEST-302 message is uncontrollable, and re-run check_test when this problem is fixed.

SEE ALSO

check_test, TEST-302

TEST-503 (information) As a result, 1 other cell is not scan controllable : %s.

DESCRIPTION

This message is generated as a result of an earlier rule violation.

WHAT NEXT

Check other error violation messages preceding this one.

TEST-504 (warning) Cell %s has constant 0 value.

DESCRIPTION

This message is issued by dft_drc if it finds a cell that has a constant 0 value at its output.This means that the cell is violated and will not be included in a scan chain.

WHAT NEXT

Validate the condition that results in the output of the cell being constant. If this is intentional, the violation can be ignored. If not fix the condition. Cells with constant outputs will not be autofixed.

TEST-505 (warning) Cell %s has constant 1 value.

DESCRIPTION

This message is issued by dft_drc if it finds a cell that has a constant 1 value at its output.This means that the cell is violated and will not be included in a scan chain.

WHAT NEXT

Validate the condition that results in the output of the cell being constant. If this is intentional, the violation can be ignored. If not fix the condition. Cells with constant outputs will not be autofixed.

TEST-511 (information) Because asynchronous pin %s is uncontrollable.

DESCRIPTION

This message is used in conjunction with the TEST-302 warning message. This message states that the cause of the uncontrollable cell provided in the previous TEST-302 message is due to the specified asynchronous pin being uncontrollable.

WHAT NEXT

Check to see if there are any subsequent information messages associated with the TEST-302 message. If the asynchronous pin is either an 'X' or 'Z', then check_test will attempt to trace back the network to find the source of the problem. Tracing will continue until an 'X' is found that cannot be traced back further in the

circuit. Note that backtracing will terminate when 1) an input port has been reached, 2) there is more than one 'X' on the sensitized paths to the asynchronous pin, or 3) a scan value is found (the output of a scan cell is an input to the asynchronous pin).

Then, examine the network which drives the asynchronous pin to determine why the pin is uncontrollable. For example, verify that there is not a misplaced 'X' in the custom test protocol or there is no uninitialized cell feeding into an asynchronous pin.

EXAMPLE

```
Warning: Cell X2 (FD2S) is not scan controllable. (TEST-302)
Information: Because asynchronous pin CD is uncontrollable. (TEST-511)
Information: Because port RESET is unknown. (TEST-514)
```

SEE ALSO

check_test, TEST-302

TEST-512 (information) Because it clocks in an unknown value from pin %s.

DESCRIPTION

This message is used in conjunction with the TEST-302 warning message. This message states that the cause of the uncontrollable cell provided in the previous TEST-302 message is due to an unknown value on the data pin specified.

WHAT NEXT

Check to see if there are any subsequent information messages associated with the TEST-302 message. If the data pin is either an 'X' or 'Z', then check_test will attempt to trace back the network to find the source of the problem. Tracing will continue until an 'X' is found that cannot be traced back further in the circuit. Note that backtracing will terminate when 1) an input port has been reached, 2) the output of a scan cell has been reached or 3) there is more than one 'X' or scan value (i.e. outputs from two distinct scan cells) on sensitized paths to the data pin.

Check to see if there are any additional information messages associated with the TEST-302 message which traces back the network for the cause of this unknown data pin, and then examine the network which drives the data pin to determine why the data pin is unknown.

For example, verify that there are no missing or incorrect test_holds or test_isolates in the design, or that there is not a misplaced 'X' in the custom test protocol.

EXAMPLE

```
Warning: Cell U1 (FD1S) is not scan controllable. (TEST-302)
Information: Because it clocks in an unknown value from
pin TI. (TEST-512)
Information: Because port SCAN_IN is unknown. (TEST-514)
```

SEE ALSO

check_test, TEST-302

TEST-513 (information) Because pin %s of cell %s (%s) is unknown.

DESCRIPTION

This message is used in conjunction with other TEST-xxx warning or error messages just above it. It provides additional information regarding an unknown value (X) in network which may have caused the previous warning/error message to be generated.

If this message has been issued in connection with a "not scan controllable" (TEST-302) violation, then it will be followed by additional information messages (e.g. indicating all the input values of a cell, if the output of the cell is unknown).

WHAT NEXT

Use any additional information messaged to determine why the indicated pin is unknown.

If this pin is expected to be unknown, then verify that this is the correct path to be sensitized from the pin given in this message to the pin/cell given in the violation message just above it.

SEE ALSO

check_test

TEST-514 (information) Because port %s is unknown.

DESCRIPTION

This message is used in conjunction with other TEST-xxx warning or error messages just above it. It provides additional information regarding an unknown value (X) at a port which may have caused the previous warning/error message to be generated.

WHAT NEXT

Verify that the port has the necessary test attributes. Possible problems include missing test_holds on "Test Mode" ports, or missing test attributes such as scan_in or scan_enable on test ports.

If this port is expected to be unknown, then verify that this is the correct path to be sensitized from the port given in this message to the pin/cell given in the violation message just above it.

SEE ALSO

check_test

TEST-515 (information) Because clock pin %s is uncontrollable.

DESCRIPTION

This message is used in conjunction with the TEST-302 warning message. This message states that the cause of the uncontrollable cell provided in the previous TEST-302 message is due to the clock pin being uncontrollable.

WHAT NEXT

Check to see if there are any subsequent information messages associated with the TEST-302 message. If the clock pin is either an 'X' or 'Z', then check_test will attempt to trace back the network to find the source of the problem. Tracing will continue until an 'X' is found that cannot be traced back further in the circuit. Note that backtracing will terminate when 1) an input port has been reached, 2) there is more than one 'X' on the sensitized paths to the clock pin, or 3) a scan value is found (the output of a scan cell is an input to the clock pin).

Then, examine the network which drives the clock pin to determine why the pin is uncontrollable. For example, verify that there is no clock reconvergence or unintended clock gating feeding into the clock pin, or a misplaced 'X' in the custom test protocol.

If the clock pin is uncontrollable due to a clock reconvergence at a net (e.g. when using parallel clock buffers), this reconvergence can be allowed by setting the variable test_allow_clock_reconvergence to true.

EXAMPLE

```
Warning: Cell U5 (FD1S) is not scan controllable. (TEST-302)
Information: Because clock pin CP is uncontrollable. (TEST-515)
Information: Because pin A of cell X3 (IV) is unknown. (TEST-513)
```

SEE ALSO

check_test, TEST-302, test_allow_clock_reconvergence

TEST-516 (information) Because cell did not receive a clock pulse.

DESCRIPTION

This message is used in conjunction with the TEST-302 warning message. This message states that the cause of the uncontrollable cell provided in the previous TEST-302 message is because there is no clock pulse on the clock pins of this cell during the scan-in sequence.

The causes for such violations fall into two general classes:

1) There is a clock pulse on a top-level port that should drive the clock pin of the uncontrollable cell, but for some reason the clock pulse does not reach the clock pin.

Possible causes include:

- A missing connection between the top-level clock port and the clock pin

- A **set_test_hold** in the wrong state, which blocks the clock pulse from reaching the clock pin

- A missing **set_test_hold** resulting in an X reaching the clock pin instead of a clock pulse

- Reconvergent clocks

2) There is no clock pulse on the top-level port that drives the clock pin during the scan-shift sequence.

Possible causes include:

- A missing clock character from a Custom Test Protocol

- The **check_test** command fails to infer a clock pulse on the top-level port

The most common cause for **check_test** failing to infer a clock pulse during the scan-shift sequence is that the test attributes on the design are in an inconsistent state. In general, if you inserted scan using **insert_scan** and stored the design in db format, you do not need to set any test attributes from the command line. However, if you read in a scan inserted design from a Verilog, VHDL, or EDIF, you need to set test attributes from the command line.

WHAT NEXT

You must first try to determine if there is a missing clock in the scan-shift section of the test protocol. You can write the test protocol out (simply enter **write_test_protocol** after you run **check_test**) or examine the diagnostic messages from **check_test**.

Verify that the clock feeding into the non-scan controllable cell has been inferred (TEST-260) or defined (create_test_clock) as a test clock, or that there is a clock pulse on the corresponding clock port in the custom test protocol during scan.

If no clock pulse has been inferred, determine and correct the cause of the missing clock pulse. Review your script carefully.

Possible causes include:

- A missing **create_test_clock** in the script

- A missing clock character in a Custom Test Protocol

- Missing "test_scan_in" and "test_scan_out" attributes on the scan ports of existing scan designs that are scan routed. (If there are no such attributes, the default test protocol will not pulse the shift clock during the scan-in sequence, which results in this message.)

- Issuing a set_scan_configuration -existing_scan true for a test-ready design (compile -scan) when you have not run **insert_scan** to route the scan design. (Setting existing_scan true on such a design confuses **check_test** and causes it to not infer a clock pulse on the clock ports.)

If the correct clock pulses are inferred on the top-level ports during the scan-shift sequence, you need to determine why the clock pulse does not reach the clock pin of the element.

Examine the network driving the clock pins, looking particularly for

- A signal that must be held in a particular state for the clock pulse to propagate

- Bad logic that prevents the propagation of a clock pulse

- Reconvergent clock signals that cause the output of a gate to go to X

EXAMPLE Warning: Cell U4 (FD1S) is not scan controllable. (TEST-302) Information: Because cell did not receive a clock pulse. (TEST-516)

SEE ALSO

check_test (2), **write_test_protocol** (2), **TEST-302.**

TEST-517 (information) Because cell did not receive scan-in

data from an input port.

DESCRIPTION

This message is used in conjunction with the "not scan controllable" warning (TEST-302) just above it and the information message (TEST-525) just below it.

This message states that the cell was clocked, but it does not contain scan-in data from an input port at the end of the scan-in sequence.

The data which originated from the "TEST-525" cell at the beginning of the scan sequence, has reached the "TEST-302" cell at the end of the scan-in sequence.

WHAT NEXT

Use this message in conjunction with the corresponding TEST-525 message and other scan messages (e.g. "scan chain terminating at <cell> is not scan controllable" (TEST-363)) to determine if the cause of the problem is either 1) a scan-in sequence that is shorter than the length of the scan chain, or 2) a circular scan chain in the design.

EXAMPLE

```
Warning: Cell X3 (FD1S) is not scan controllable. (TEST-302)
Information: Because cell did not receive scan-in data from
an input port. (TEST-517)
Information: Because cell contains data that was in cell X2 (FD1S)
at the start of scan shift. (TEST-525)
```

SEE ALSO

check_test, TEST-302, TEST-525

TEST-518 (information) Because an illegal input combination was applied: Pin %s was %s.

DESCRIPTION

This message is used in conjunction with the TEST-302 warning message. It indicates that an input combination was applied to the cell that is not allowed, so the output is unknown.

There is a separate TEST-518 information message for each pin of the cell that contributed to the illegal input combination.

A common situation which results in this message is if multiple clock pins of a cell are active at the same time.

WHAT NEXT

Examine the network driving the mentioned pins to see why there is an illegal input combination. If any of the pins are clocks, also verify the clock waveforms.

EXAMPLE

```
Warning: Cell U2 (C_SCAN_FF) is not scan controllable. (TEST-302)
Information: Because an illegal input combination was applied:
Pin C was rising. (TEST-518)
Information: Because an illegal input combination was applied:
Pin SC was rising. (TEST-518)
```

SEE ALSO

check_test, TEST-302

TEST-519 (information) Because clock is used as data on pin %s.

DESCRIPTION

This message is used in conjunction with the TEST-302 warning message. This message states that the cause of the uncontrollable cell provided in the previous TEST-302 message is due to the fact that there is a clock on a data pin of this cell.

WHAT NEXT

Examine why a transition has occurred at the data input of the cell being clocked.

EXAMPLE

```
Warning: Cell U3 (FD1S) is not scan controllable. (TEST-302)
Information: Because clock is used as data on pin TI. (TEST-519)
```

SEE ALSO

check_test, TEST-302

TEST-520 (information) Because cell is set_scan or

set_scan_element false.

DESCRIPTION

This message is used in conjunction with the TEST-302 violation message previously given. This cell is not scanned since a set_scan or set_scan_element false command was issued by you on the cell.

WHAT NEXT

Verify that a set_scan or set_scan_element false command is desirable for this cell.

If this cell is correctly marked with this attribute, this message is for informational purposes only.

EXAMPLE

```
Warning: Cell U3 (FD1) is not scan controllable. (TEST-302)
Information: Because cell is set_scan or set_scan_element false. (TEST-520)
```

SEE ALSO

check_test

TEST-521 (information) Because pin %s of cell %s (%s) is unknown due to a set_test_isolate command.

DESCRIPTION

This message is used in conjunction with the TEST-xxx violation message just above it. The value of the pin is unknown (X) due to a set_test_isolate command issued by the user on either the pin or the cell.

WHAT NEXT

Verify that a set_test_isolate command is desirable for this cell or pin. The command "report_test -assertions" will list all the test_isolate attributes in a design.

If this cell/pin is correctly marked with this attribute, then verify that this is the correct path to be sensitized from the pin given in this message to the pin/cell given in the violation message just above it.

SEE ALSO

check_test

TEST-522 (information) Because pin %s of cell %s (%s) is unknown due to a previously reported violation.

DESCRIPTION

This message is used in conjunction with the TEST-xxx violation message just above it. The value at the pin is unknown (X) due to another violation that was found by check_test.

WHAT NEXT

Fix the preceding violations in the check_test output which appear above this message that are on or near this pin.

Also verify that this is the correct path to be sensitized from the pin given in this message to the pin/cell given in the violation message just above it.

SEE ALSO

check_test

TEST-523 (information) Because port %s is unknown due to a set_test_isolate command.

DESCRIPTION

This message is used in conjunction with the TEST-xxx violation message just above it. The value at the port is unknown (X) due to a set_test_isolate command issued by the user on the port.

WHAT NEXT

Verify that a set_test_isolate command is desirable for this port. The command "report_test -assertions" will list all the test_isolate attributes in a design.

If this port is correctly marked with this attribute, then verify that this is the correct path to be sensitized from the port given in this message to the pin/cell given in the violation message just above it.

SEE ALSO

check_test

TEST-524 (information) Because port %s is unknown due to a previously reported violation.

DESCRIPTION

This message is used in conjunction with the TEST-xxx violation message just above it. The value at the port is unknown (X) due to another violation that was found by check_test.

WHAT NEXT

Fix the preceding violations in the check_test output which appear above this message that are on or near this port.

Also verify that this is the correct path to be sensitized from the port given in this message to the pin/cell given in the violation message just above it.

SEE ALSO

check_test

TEST-525 (information) Because cell contains data that was in cell %s (%s) at the start of scan shift.

DESCRIPTION

This message is used in conjunction with the "not scan controllable" warning (TEST-302) and "no scan-in data" information message (TEST-517) just above it.

There are two scan cells involved; one is the cell referenced in the TEST-302 message and the other is the scan cell referenced in this TEST-525 message. The data which originated from the "TEST-525" cell at the beginning of the scan sequence, has reached the "TEST-302" cell at the end of the scan-in sequence. If the scan chain was operating properly, the data in the "TEST-525" cell should have been shifted out of the scan-out pin.

WHAT NEXT

Use this message in conjunction with other scan messages (e.g. "scan chain terminating at <cell> is not scan controllable" (TEST-363)) to determine if the

cause of the problem is either 1) a scan-in sequence that is shorter than the length of the scan chain, or 2) a circular scan chain in the design.

SEE ALSO

check_test, TEST-302, TEST-517

TEST-526 (information) Because input pin %s of cell %s (%s) is unconnected.

DESCRIPTION

This message is used in conjunction with the TEST-xxx violation message just above it. The value at the pin is unknown (X) due to the absence of driver. The unconnected input was previously reported as a violation (TEST-332).

WHAT NEXT

Explicitly connect the pin to the appropriate driver.

Also verify that this is the correct path to be sensitized from the pin given in this message to the pin/cell given in the violation message just above it.

SEE ALSO

check_test

TEST-540 (information) The drivers of the cone of logic ending at pin %s of cell %s (%s) are listed below.

DESCRIPTION

This message indicates that the following information messages list the drivers of the cone of logic ending at the indicated pin. The drivers of the cone of logic include ports, outputs of sequential cells, and pins that are unknown due to previous violations found by check_test or set_test_isolate commands.

WHAT NEXT

The following messages contain the pins driving the cone of logic, as well as their values. Possible problems include missing test_holds on "Test Mode" ports, or missing test attributes such as scan_in or scan_enable on test ports.

TEST-541 (information) Port %s is %s.

DESCRIPTION

This message is used in conjunction with the TEST-xxx violation message previously given. It provides the logic value of the port at the currently simulated protocol vector.

WHAT NEXT

Check if the logic value of the port provided in this message contributes to the violation message which precedes this message.

SEE ALSO

check_test

TEST-542 (information) Port %s is %s due to a set_test_isolate command.

DESCRIPTION

This message is used in conjunction with the TEST-xxx violation message previously given. Since a set_test_isolate command is applied to the port, the value of the port is unknown (X).

WHAT NEXT

Check if the set_test_isolate attribute on the port provided in this message contributes to the violation message which precedes this message. The command "report_test -assertions" lists the test_isolate attributes in a design.

SEE ALSO

check_test

TEST-543 (information) Port %s is %s due to a previously

reported violation.

DESCRIPTION

This message is used in conjunction with the TEST-xxx violation message previously given. It provides the logic value of the port at the currently simulated protocol vector. Another violation that has been reported by check_test is the reason that the value of the port is unknown (X).

WHAT NEXT

Examine the violations in the check_test output which appear prior to this message that are on or near this port. An example is a "Three-state net %s has non three-state driver(s). (TEST-115)" violation on the net connected to the port.

SEE ALSO

check_test

TEST-544 (information) Port %s is a scan-in value.

DESCRIPTION

This message is used in conjunction with the TEST-xxx violation message previously given. It indicates that the port has a valid scan-in value at the currently simulated protocol vector.

WHAT NEXT

Check if the logic value of the port provided in this message contributes to the violation message which precedes this message.

SEE ALSO

check_test

TEST-545 (information) Pin %s of cell %s (%s) is %s.

DESCRIPTION

This message is used in conjunction with the TEST-xxx violation message previously given. It provides the logic value of the pin at the currently simulated protocol vector.

WHAT NEXT

Check if the logic value of the pin provided in this message contributes to the violation message which precedes this message.

SEE ALSO

check_test

TEST-546 (information) Pin %s of cell %s (%s) is %s due to a set_test_isolate command.

DESCRIPTION

This message is used in conjunction with the TEST-xxx violation message previously given. Since a set_test_isolate command is applied to either the cell or the pin, the value of the pin is unknown (X).

WHAT NEXT

Check if the test_isolate attribute on the pin provided in this message contributes to the the violation message which precedes this message. The command "report_test -assertions" lists the test_isolate attributes in a design.

SEE ALSO

check_test

TEST-547 (information) Pin %s of cell %s (%s) is %s due to a previously reported violation.

DESCRIPTION

This message is used in conjunction with the TEST-xxx violation message previously given. It provides the logic value of the pin at the currently simulated protocol vector. Another violation reported by check_test is the reason that the value of the pin is unknown (X).

WHAT NEXT

Examine the violations in the check_test output which appear above this message that are on or near this pin. A simple example is a cell that is a "black box" because it has no function associated with it.

SEE ALSO

check_test

TEST-548 (information) Pin %s of cell %s (%s) is a scan-in value.

DESCRIPTION

This message is used in conjunction with the TEST-xxx violation message previously given. It indicates that the pin has a valid scan-in value at the currently simulated protocol vector.

WHAT NEXT

Check if the logic value of the pin provided in this message contributes to the violation message which precedes this message.

SEE ALSO

check_test

TEST-549 (information) Pin %s of cell %s (%s) is the value of pin %s of sequential cell %s (%s).

DESCRIPTION

This message complements the previous information message, and informs you that the specified pin has the same value as the specified pin of the specified sequential cell in the design.

WHAT NEXT

This is an informational message only. No action is required on your part.

TEST-550 (error) %s condition detected on bidirectional port

%s.

DESCRIPTION

This message indicates that there is a contention or float condition on a bidirectional port when the DFT Compiler's test design rule checker, check_test, simulates in a particular vector in the test protocol.

A contention condition will occur, for example, when the three-state driver associated with a bidirectional port is enabled, and the test protocol specifies an input value (e.g. '0', '1', 'X', 'Pi') for the bidirectional port in a particular vector. Another example of a contention condition is when the net connected to the bidirectional port has multiple three-state drivers, and two to more of these drivers are enabled. Note that DFT Compiler will flag a contention condition even if the values driven by the enabled three-states are the same.

A float condition will occur, for example, if all three-state drivers associated with a bidirectional port are disabled, the test protocol specifies an output value (e.g. 'Po', 'M') for the bidirectional port, and there are no pull-ups, pull-downs, or bus-holds on the net connected to the bidirectional port.

Currently, check_test checks for contention or float conditions on bidirectional ports only in the parallel measure vector of the test protocol.

A contention or float violation does not stop check_test from continuing its check of other test design rules. However, DFT Compiler commands which run check_test as a preprocessor (e.g. create_test_patterns, insert_scan, preview_scan, and insert_test) will not proceed if a contention or float condition is detected by check_test.

WHAT NEXT

If a contention condition is due to the three-state drivers associated with a bidirectional port, then examine the enable cone of logic associated with the three-state driver(s) of the port, and the protocol values which enable the driver(s). If a contention condition is due to a protocol value associated with the bidirectional port, then either modify the protocol value of the port, or examine the enable cone of logic associated with the three-state drivers of the port.

In case of a float condition, either follow one of the steps described above, or consider adding a pull-up or pull-down to the net connected to the bidirectional port.

Note that contention and float checking in check_test can be turned off by the "-check_contention" and "-check_float" options of the command. For example, if you would like check_test not to check for float conditions on bidirectional ports, then issue the following check_test command:

```
dc_shell> check_test -check_float false;
```

The corresponding command for bypassing contention checking in check_test is

```
dc_shell> check_test -check_contention false
```

If check_test is being run as a preprocessor to another DFT Compiler command, and you would like to allow for contention or float on bidirectional ports, then run check_test with the "-check_contention" and/or "-check_float" option immediately before issuing the desired DFT Compiler command. Note that depending on the DFT Compiler command being issued, you may have to turn off contention and/or float checking in that command as well.

Consider an example where you would like to generate test patterns using the create_test_patterns command, and create_test_patterns has stopped after the test design rule checker (check_test) has detected a float condition. You must use the following command sequence in order to turn off float checking and generate patterns.

```
dc_shell> check_test -check_float false;
dc_shell> create_test_patterns -check_float false;
```

SEE ALSO

check_test, TEST-551.n, TEST-552.n, read_test_protocol

TEST-551 (information) Because the value of port %s in the protocol is %s.

DESCRIPTION

You receive this message because it reports the protocol value of a port for a particular protocol vector simulated by the **check_test** command and a brief description of that value. This message supports other messages issued by DFT Compiler.

Symbolic protocol values and their descriptions are as follows:

0 - Applied logic zero value 1 - Applied logic one value X - Input does not care value Z - High impedance C - Applied clock pulse Cp - Applied Capture clock pulse Si - Applied scan data So - Measured scan data Pi - Applied parallel data Po - Measured parallel data U - Value not changed M - Output does not care value Pio - Either applied parallel input data or measured output data, depending on the state of the circuit (bidirectional pin only)

WHAT NEXT

Check your test protocol.

SEE ALSO

check_test (2), **read_test_protocol** (2), **TEST-550** (n), **TEST-557** (n), **TEST-558** (n).

TEST-552 (information) The three-state cell %s is %s because of the following input pin values: %s.

DESCRIPTION

This message supports other messages issued by **check_test**, and informs you of the state (active or inactive) of the specified three-state cell instance during simulation of a particular protocol vector by **check_test**. This message also provides the names and values of input pins that have values of logic 1 or logic 0 for this particular vector and are in the three-state support of the cell.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

check_test (2), **TEST-550** (n), **TEST-557** (n), **TEST-558** (n).

TEST-554 (warning) Three-state net %s has both pull-up and pull-down resistor cells.

DESCRIPTION

You receive this message if **check_test** detects the existence of both pull-up and pull-down cells on the same net. The pull-up (pull-down) cell could be embedded in an existing three-state cell, or could be an independent library cell driving the net.

After **check_test** issues this message, it continues to check the design, assuming that there are no pull-up or pull-down cells present on the net. If all drivers of a three-state net of this type are inactive, **check_test** flags a float condition on the net. Similarly, **create_test_patterns** assumes that there are no pull-up or pull-down cells on the net, and does not generate patterns where all drivers of the net are inactive. Thus this condition (a net having both pull-up and pull-down cells) could lead to a loss of coverage.

This message is followed by informational messages that list the pull-up and pull-down cells on the net.

WHAT NEXT

To prevent a possible loss of test coverage, proceed as follows:

1. Read the informational messages to identify the pull-up and pull-down cells on the net.

2. Modify the design so that the specified net does not have both pull-up and pull-down cells.

3. Re-execute **check_test**.

SEE ALSO

check_test (2), **create_test_patterns** (2), **TEST-555** (n), **TEST-556** (n).

TEST-555 (information) Pull-up cell%s: %s.

DESCRIPTION

This message supports other messages issued by **check_test**, and indicates the list of pull-up cells on a net in the design.

WHAT NEXT

Use the information in this message to correct the condition flagged by **TEST-554**, following the instructions in that extended error message.

SEE ALSO

check_test (2), **TEST-554** (n).

TEST-556 (information) Pull-down cell%s: %s.

DESCRIPTION

This message supports other messages issued by **check_test**, and indicates the list of pull-down cells on a net in the design.

WHAT NEXT

Use the information in this message to correct the condition flagged by **TEST-554**, following the instructions in that extended error message.

SEE ALSO

check_test (2), **TEST-554** (n).

TEST-557 (warning) Bidirectional port %s with test_isolate attribute has inconsistent protocol value %s. Protocol value is ignored.

DESCRIPTION

This message indicates that DFT Compiler's test design rule checker, check_test, has detected an inconsistency while simulating the current protocol vector. The inconsistency is between the protocol value of a bidirectional port and the test_isolate attribute on that port.

This condition can occur if the protocol value of a bidirectional port in a particular vector is '1' or '0', and the port has a test_isolate attribute.

The test_isolate attribute can be placed on a port by the set_test_isolate command. The presence of this attribute on a port forces test pattern generation to not use that port. Test pattern generation (create_test_patterns), and test design rule checking (check_test) assume that the value of the port is unknown. A protocol value of '1' or '0' on a bidirectional port, however, indicates to check_test and create_test_patterns that the port is to be used as input, and that the value driven by that port is '1' or '0'. This is inconsistent with the test_isolate attribute on the port.

When check_test detects such a condition, it honors the test_isolate attribute and ignores the '1' or '0' value in the test protocol.

WHAT NEXT

Either remove the test_isolate attribute from the port, or change the protocol value of the port to 'X', 'Pi', 'Pio', 'Po', or 'M' as appropriate.

SEE ALSO

check_test, set_test_isolate, read_test_protocol

TEST-558 (error) The variable atpg_bidirect_output_only is set to "true", but the bidirectional port %s cannot be forced into output mode. No vectors can be generated.

DESCRIPTION

You receive this message if **check_test** detects an inconsistency between the setting of the variable **atpg_bidirect_output_only**, and the mode of the identified bidirectional port.

When the variable **atpg_bidirect_output_only** is set to *true*, **create_test_patterns** generates patterns that force all bidirectionals in the design into output mode. However, if the state of the three-state driver(s) associated with a bidirectional port is inactive because of constant values present in the design; or if the bidirectional port has an input protocol value, then DFT Compiler cannot force the bidirectional port into output mode in all patterns. This condition prevents **create_test_patterns** from generating test vectors.

This condition does not prevent **check_test** from checking other test design rules, but it does prevent execution of DFT Compiler commands that run **check_test** as a preprocessor (for example, **create_test_patterns**, **insert_scan**, **preview_scan**, and **insert_test**).

WHAT NEXT

If you receive this message, do one or more of the following:

1. Set **atpg_bidirect_output_only** to *false*.

2. Modify the test constraints (**set_test_hold**, **set_test_assume**, **set_test_require**) or modify the test protocol to allow DFT Compiler to force the bidirectional ports into output mode.

3. As a last resort, you might need to modify your design.

Then re-execute **check_test**.

SEE ALSO

check_test (2); **atpg_bidirect_output_only** (3); **TEST-551** (n), **TEST-552** (n).

TEST-559 (information) Bidirectional port %s changes value to %s at time %s.

DESCRIPTION

This is one of the diagnostic messages, issued following the unreliable capture warning messages (TEST-478 and TEST-471) to help you identify and correct the cause of the unreliable capture problem.

This message describes the cause of an unreliable capture problem when the value applied to a bidirectional port in the parallel measure cycle changes before response data is captured into sequential cells driven by that port. The message is to be interpreted as follows:

• port %s is the name of the bidirectional port whose change causes the unreliable capture.

• %s is the new protocol value of the bidirectional port after the change occurs. Possible protocol values include the following:

```
0     Applied logic zero value
1     Applied logic one value
X     Input don't care value
Si    Applied scan data
M     Output don't care value
```

• time %s is the time (within a cycle) when the change occurs.

DFT Compiler's automatic test pattern generation (ATPG), invoked by the **create_test_patterns** command, assumes that values applied to primary inputs in the parallel measure cycle are stable while response data is measured at primary output ports and captured in scan (or valid non-scan) sequential cells. This assumption is also true for a bidirectional port when that port is used as input. Therefore, if the value applied to a port in the parallel measure cycle changes before response data is captured into sequential cells, this would invalidate the patterns generated by **create_test_patterns**.

The default test protocol inferred by **check_test** ensures that during the parallel measure cycle the values applied to primary inputs (and bidirectionals when used as input) do not change until response data is measured at primary outputs and captured into sequential cells. However, a change to the default test timing can cause **check_test** to infer a protocol that changes the value applied to bidirectional ports before response data is captured into sequential cells.

For example, if the bidirectional delay is set to a value smaller than the active (capture) edge of the clocks, the protocol value of a bidirectional port is 'M' (output don't care) in the capture cycle, and the port can be used as input by ATPG. This condition can cause a mismatch between the actual values captured into sequential cells driven by this port and the expected values of these sequential cells in the generated patterns. An input value is applied to the bidirectional port at the bidirectional delay time in the parallel measure cycle. However, the bidirectional port is released (changes to **'M'**) in the capture cycle at the bidirectional delay time. This is before the capture edge of the clock(s).

While simulating the test protocol, **check_test** detects any change in the value applied to a bidirectional port in the parallel measure cycle that can cause an unreliable capture in the sequential cells driven by that port. All sequential cell pins reached by the change are marked as violated. **create_test_patterns** does not use the violated pins for observing fault effects, and considers them as unknown when expecting response values.

If the variable **test_check_port_changes_in_capture** is set to *false*, **check_test** does not perform the previously-mentioned checks.

WHAT NEXT

Follow the instructions in the WHAT NEXT section of the TEST-471 or TEST-478 extended warning messages, using the information in this diagnostic message to help find the cause of the problem.

SEE ALSO

check_test (2), **create_test_patterns** (2); **test_check_port_changes_in_capture** (3); **TEST-471** (n), **TEST-478** (n), *Design Analyzer Reference Manual*, *DFT Compiler Test Design Rule Checking User Guide*.

TEST-560 (information) check_test will not check for port changes that cause unreliable capture, because the variable test_check_port_changes_in_capture is set to "false".

DESCRIPTION

check_test issues this message if the variable **test_check_port_changes_in_capture** is set to *false*. By default, when **check_test** simulates the test protocol, it checks for any change to the value applied to a bidirectional port in the parallel measure cycle that can cause an unreliable capture in the sequential cells driven by that port. Setting the variable **test_check_port_changes_in_capture** to *false* disables this check.

WHAT NEXT

If you want **check_test** to check for port changes that cause unreliable capture, set **test_check_port_changes_in_capture** to *true*, and re-execute **check_test**.

SEE ALSO

check_test (2); **test_check_port_changes_in_capture** (3); **TEST-471** (n), **TEST-478** (n), **TEST-559** (n).

TEST-561 (information) Because bidirectional port driver %s is active.

DESCRIPTION

This message provides additional information in support of the TEST-115 (Three-state net %s is not properly driven) warning message. You receive this message when more than two bidirectional ports are driving the three-state net.

WHAT NEXT

Eliminate the problem by only enabling one bidirectional port driver at a time. Then re-run **check_test**.

TEST-562 (error) %s condition detected on bidirectional port %s during scan shift.

DESCRIPTION

This message is generated by the DFT Compiler design rule checker, check_test, when a net is connected to more than one bidirectional port and two or more ports have input values during scan shift. For example, if a net is connected to two bidirectional ports and the two ports are attributed as scan-in (test_scan_in signal_type attributes), contention can occur when scan-in values are applied to both ports during scan shift.

When inferring the test protocol, check_test checks the condition of all bidirectional ports to make sure that contention and float conditions are avoided during scan shift. Check_test establishes the simulation state of the design in scan shift by simulating any initialization sequence, the active value of all ports being held constant throughout testing, any assumed values, and the active value of the scan enable. It then checks for contention and float conditions on the nets connected to bidirectional ports. This is done by checking the mode of the three-state driver(s) associated with the port as well as port attributes. Port attributes (for example signal_type or test_hold attributes) indicate whether a value is applied to the port during scan shift. If a net is connected to multiple bidirectional ports, and values are applied to two or more of these ports during scan shift, check_test flags the contention condition.

This violation stops test pattern generation (create_test_patterns command) and scan insertion (insert_scan command).

WHAT NEXT

Check_test identifies the bidirectional ports that cause the contention condition as well as the attributes that indicate that values are to be applied to these ports in scan shift. This information is printed in the information messages (TEST-564) following this message. Remove the extra attributes from all but one of the ports.

If you do not want to remove any port attributes and want to proceed with test pattern generation or scan insertion despite the contention condition, run check_test with the check_contention option set to the value "none" or "capture_only" prior to the create_test_patterns or insert_scan command. For example:

```
dc_shell> check_test -check_contention capture_only; dc_shell> create_test_patterns;
```

SEE ALSO

check_test, TEST-564

TEST-563 (warning) Net %s, connected to bidirectional port %s,

has three-state driver(s) with unknown mode during scan shift.

DESCRIPTION

You receive this message because a bidirectional port's three-state driver (buffer or pad) is not forced to be active or inactive throughout the scan shift operation. This message is generated by the DFT Compiler design rule checker, the **check_test** command.

During scan shift, bidirectional ports must be forced into either input or output mode to avoid contention or float conditions on these ports during scan shift. If the enable of the three-state driver associated with a bidirectional port is not held constant during scan shift, the mode of the bidirectional can change, thus causing a contention or float condition. Note that the bidirectional port enable does not have to be held constant in parallel measure and capture cycles because the port's state is controlled by the scanned-in state of the circuit.

A bidirectional port's three-state driver enable can be held constant during scan shift by gating the enable with a scan enable or test mode signal. DFT Compiler scan synthesis (the **insert_scan** command) automatically adds conditioning logic to force bidirectionals into input or output mode throughout scan shift. This gating uses the scan enable signal.

This message is followed by several diagnostic messages. The first diagnostic message (TEST-552) gives information about the bidirectional port's three-state driver(s) and logic values on its enable during scan shift. The second diagnostic message (TEST-565) indicates the protocol value that is inferred for the bidirectional port during scan shift.

WHAT NEXT

If logic exists for forcing bidirectional ports into input or output mode throughout scan shift and you still receive this message, the design is missing protocol information or port attributes. Ensure that the following are attributed:

- All test-related ports, such as scan enable.
- Test bidirectional control (for LSI Logic vector formats only).
- Ports that are held constant throughout scan testing (test-hold). If an initialization sequence is required to condition the bidirectional ports to input or output, ensure that the corresponding initialization protocol is read in.

If conditioning logic does not exist and the design is pre-scan, add conditioning logic to the bidirectional ports' three-state enables during the scan insertion process. The **insert_scan** command performs this by default. If the design is scan replaced only or scan routed, you can still use the **insert_scan** command to add conditioning logic to the bidirectional ports' three-state drivers. See the **set_scan_configuration** command man page the for appropriate scan configuration specification that adds only three-state conditioning logic to the design (no scan replacement or routing).

NOTES

If the design is scan routed and bidirectional ports are not conditioned into input or output mode throughout scan shift, the DFT Compiler automatic test pattern generator (**create_test_patterns** command) does not generate test patterns. This is because the generated patterns would cause contention or float during scan shift. If you would like DFT Compiler to proceed with pattern generation even when bidirectionals are not conditioned throughout scan shift, you must run **check_test** with the **-check_contention** and **-check_float** options set to *false* or *capture_only* prior to using the **create_test_patterns** command. For example:

```
dc_shell> check_test -check_contention capture_only\
          -check_float capture_only;
dc_shell> create_test_patterns;
```

SPECIAL NOTE

Note the following information on conditioning bidirectionals into input mode during scan shift.

By default, the **insert_scan** command conditions bidirectional ports into input mode during scan shift. The inferred test protocol for the design then places an *X* (value is unimportant to input) on the bidirectional ports for all scan shift vectors. The formatted test vectors therefore indicate that the tester must apply a value to the bidirectional ports during scan shift.

In the default inferred test protocol, the scan shift vectors are followed by the parallel measure vector. In this vector, primary inputs are applied at a time corresponding to the input delay, and primary outputs are strobed at the specified strobe time. Similarly, bidirectional ports used as inputs are applied at the time corresponding to the bidirectional delay, and bidirectional ports that are used as output are strobed at strobe time.

A contention condition may occur on bidirectional ports in the parallel measure cycle when both of the following situations are true:

• Bidirectionals are conditioned as inputs during scan shift by using the scan enable signal (the **insert_scan** command default).

• Input delay (the time at which primary inputs such as scan enable change in each cycle) is less than the bidirectional delay (time at which bidirectional ports change in each cycle).

The contention occurs between the input delay and bidirectional delay times.

For example, if the input delay (specified by the **test_default_input_delay** variable) has a default value of *5*ns and the bidirectional delay (specified by the **test_default_bidir_delay** variable) has a default value of *55*ns, a *50*ns contention can occur for patterns in which automatic test-pattern generation (ATPG) uses a bidirectional as output. In these patterns, the bidirectional's three-state becomes active at time *5* in the parallel measure cycle when scan enable changes to its inactive value. This is because the scanned-in state of circuit conditions the port

into output mode. However, since the bidirectionals change at bidirectional delay time, the value applied to the bidirectional throughout scan shift is not released until time *55*ns in the parallel measure cycle.

In order to avoid this type of contention you can use a scan configuration that specifies bidirectionals to be in output mode during scan shift. Thus, the **insert_scan** command adds the appropriate conditioning logic, which forces the three-state driver of each bidirectional port to be active during scan shift.

SEE ALSO

check_test (2), **create_test_patterns** (2), **insert_scan** (2), **set_scan_configuration** (2), **test_default_bidir_delay** (3), **TEST-552** (n), **TEST-564** (n), **TEST-565** (n).

TEST-564 (information) Port %s is attributed as %s.

DESCRIPTION

This is one of the diagnostic messages issued by **check_test** in addition to messages related to conflict (contention or float) on bidirectional ports during scan shift (TEST-566 and TEST-562). This message indicates which port attribute causes the conflict in scan shift as well as the effect of that attribute on protocol inference.

When inferring the test protocol, **check_test** checks the condition of all bidirectional ports to ensure that contention and float conditions are avoided during scan shift. **check_test** establishes the simulation state of the design in scan shift by first simulating any initialization sequence, and then by simulating the design. During the simulation of the design, the following values are applied to the appropriate ports:

1) The active value is applied to all ports that are held constant throughout testing.

2) The **test_hold** values specified with the **set_test_hold** command are applied to input ports in the design.

3) The **test_assume** values specified with the **set_test_assume** command are applied to output pins of black box cells.

4) The active value of the scan enable is applied to the scan enable port.

check_test then checks for contention or float conditions on the nets connected to bidirectional ports, by checking the mode of the three-state driver(s) associated with the port as well as port attributes. Port attributes (for example, **signal_type** or **test_hold** attributes) indicate whether a value is applied to the port during scan shift.

WHAT NEXT

Check the specified port attribute, and its value, and determine whether it is in conflict with the mode of the port. If so, remove or correct the attribute by using **remove_attribute**, **set_test_hold**, or **set_signal_type** as appropriate. Then re-execute **check_test**.

SEE ALSO

check_test TEST-562 (n), **TEST-566** (n).

TEST-565 (information) Bidirectional port %s is inferred as %s.

DESCRIPTION

You receive this message because a bidirectional port's three-state driver (buffer or pad) is not forced active or inactive throughout the scan shift operation. You receive this message following the **TEST-563** warning message. This message informs you that **check_test** is inferring the specified bidirectional port as having the specified protocol value *M* (value is unimportant to output) or *X* (the value is unimportant to input).

If the inferred protocol value is *M*, the test vectors do not apply any value to the bidirectional port during scan shift. If the inferred protocol value is *X*, the test vectors apply a value to the bidirectional port during scan shift, either *1*, *0*, or *X*, as determined by the **write_test_input_dont_care_value** variable (the default is *X*).

If you continue with **create_test_patterns** without fixing the **TEST-563** violation, you will lose test coverage because the scan chain is not observable. If the scan chain contains a high percentage of the scan cells in your design, the loss in test coverage will be severe.

WHAT NEXT

Use the information in this message to help fix the **TEST-563** violation. Read the **TEST-563** extended warning message, then do one or more of the following:

1. Change the value of the **write_test_input_dont_care_value** variable.

2. Modify the test constraints (**set_test_hold**, **set_test_assume**, **set_test_require**) or modify the test protocol to allow DFT Compiler to force the bidirectional port either active or inactive during scan shift.

3. As a last resort, you may have to modify your design.

4. Execute the **check_test** command again.

SEE ALSO

check_test (2), **set_test_assume** (2), **set_test_hold** (2), **set_test_require** (2), **write_test_input_dont_care_value** (3), **TEST-552** (n), **TEST-563** (n).

TEST-566 (warning) %s condition detected on bidirectional port %s during scan shift.

DESCRIPTION

This message is generated by the DFT Compiler design rule checker, check_test, when a net connected to a bidirectional port does not have one and only one driver active during scan shift. Contention can occur, for example, if the three-state driver associated with the bidirectional is active during scan shift and the bidirectional port is attributed as scan-in (test_scan_in signal_type attribute). For example, float can occur if the three-state driver associated with the bidirectional is inactive during scan shift and the bidirectional port is attributed as scan-out (test_scan_out signal_type attribute).

When inferring the test protocol, check_test checks the condition of all bidirectional ports to make sure that contention and float conditions are avoided during scan shift. Check_test establishes the simulation state of the design in scan shift by simulating any initialization sequence, the active value of all ports being held constant throughout testing, any assumed values, and the active value of the scan enable. Check_test then checks for contention or float conditions on the nets connected to bidirectional ports. This is done by checking the mode of the three-state driver(s) associated with the port as well as port attributes. Port attributes (for example signal_type or test_hold attributes) indicate whether a value is applied to the port during scan shift.

If more that one of the drivers associated with the bidirectional is active, check_test flags the contention. This can occur if the net connected to the bidirectional port has more than one active three-state driver. It can also occur if the net’s three-state driver is active and a value is being applied to the bidirectional port during scan shift.

If all of the drivers associated with the bidirectional are inactive, and there is no pull-up, pull-down, or bus-holder on the net, check_test flags a float condition. This can occur if all of the net’s three-state drivers are inactive, and the bidirectional port has been attributed as an output (for example scan-out).

This violation stops test pattern generation (create_test_patterns command) if the design is scan routed. It does not stop scan insertion (insert_scan command).

WHAT NEXT

Check_test identifies the bidirectional port or three-state driver(s) which cause the contention or float condition. This is printed in the information messages (TEST-564 and TEST-552) following this message.

Make sure that all test related ports such as scan enable, test bidirectional control (for LSI Logic vector formats only) and ports which are held constant throughout testing (test-hold) are attributed with their correct sense. For example, if the scan enable signal is inverted, make sure that the scan enable port is attributed with the test_scan_enable_inverted signal_type. If an initialization sequence is required to condition the bidirectional ports to input or output, make sure that the correct initialization sequence is used.

If the design is attributed correctly, you can use the insert_scan command to fix the contention or float condition identified by check_test. DFT Compiler scan insertion (insert_scan command) automatically adds conditioning logic to the enable of the three-state drivers to insure that one and only one net driver (including the bidirectional port) is active during scan shift. You can use this command to fix conflict conditions identified by this message even if the design is scan routed.

For example, if the contention condition is due to multiple active three-state drivers, insert_scan adds disabling logic to one of the three-state drivers so that only one is active during scan shift.

As another example, consider a float condition in a pre-scan design. If the float is due a the bidirectional port being attributed as scan-out and the three-state driver associated with the port is inactive during scan shift, insert_scan adds enabling logic to the three-state driver’s enable and uses the port as a scan-out.

For more information refer to the insert_scan, set_scan_configuration, and set_scan_signal man pages.

If the design is scan routed and you do not want to take any actions to fix the conflict violation prior to test pattern generation, you must run check_test with the check_contention (or check_float) option set to the value "none" or "capture_only" prior to the create_test_patterns command. For example if check_test has identified a float condition in your scan routed design and you want to proceed with test pattern generation despite the identified float, use the following command sequence:

```
dc_shell> check_test -check_float capture_only; dc_shell> create_test_patterns;
```

SEE ALSO

check_test, TEST-564, TEST-552, insert_scan, set_scan_configuration, set_scan_signal

TEST-567 (information) The preceding violation will prevent test pattern generation.

DESCRIPTION

This message indicates that the preceding warning message issued by **check_test** is a severe rule violation that prevents test pattern generation. The create_test_patterns command will not proceed with pattern generation because of the rule violation identified by the preceeding warning message.

WHAT NEXT

Read the preceding warning message and correct the rule violation. Then re-execute **check_test** before proceeding with test pattern generation.

SEE ALSO

check_test (2), **create_test_patterns** (2); **TEST-566** (n), **TEST-563** (n).

TEST-568 (error) Some test design rule checking violations prevent test vector generation.

DESCRIPTION

You receive this message because DFT Compiler identifies a severe design rule violation that prevents test pattern generation. It is issued by the **create_test_patterns** command when the DFT Compiler design rule **check_test** command identifies a violation such as contention on bidirectional ports during scan shift. The **create_test_patterns** command does not proceed with pattern generation if the rule checker identifies severe violations.

WHAT NEXT

You can run the **check_test** command, which issues a **TEST-567** message after warning messages (rule violations) that prevent test pattern generation. You must address these rule violations before proceeding with test pattern generation. The **check_test** violation summary also indicates the number of rule violations (warnings) that stop test pattern generation.

SEE ALSO

check_test (2), **create_test_patterns** (2), **TEST-563** (n), **TEST-566** (n), **TEST-567** (n).

TEST-569 (information) The open-drain or open-source port %s cannot be used as a scan output.

DESCRIPTION

This message follows the warning message **TEST-362**, and informs you that the specified port cannot be used as a scan output because it does not have a pullup or pulldown resistor cell attached to it.

An open-drain (or open-source) output can have only two values: logic 0 and High-Z. Such an output cannot be used as a scan output unless a pullup (or pulldown)

resistor cell is attached to it. When the pullup/pulldown cell is missing, **check_test** considers the scan chain reaching this output as not observable and issues first **TEST-362** and then this informational message.

WHAT NEXT

If you continue with **create_test_patterns** without correcting the **TEST-362** violation, you will lose test coverage because the scan chain is not observable. If the scan chain contains a high percentage of the scan cells in your design, the loss in test coverage will be severe.

Correct the situation by attaching a pullup or pulldown resistor cell to the specified port. Then re-execute **check_test**.

SEE ALSO

check_test (2); **TEST-362** (n).

TEST-570 (error): Invalide clock offstate (Offstate of clock %s is incompatible with clock gating optimization).

DESCRIPTION

You receive this message because the clock offstate is not consistent with the clock gating optimizations. This message is generated by the DFT Compiler test design rule checker, the **dft_drc** command. This message tells you that DFT Compiler could not recover from processing errors that occurred during test design rule checking. Others test design rule checker violations might exist.

When the variable **test_dft_drc_ungate_clocks** is set to true, the test design rule checker performs clock gating optimizations. A count is maintained to establish which transformation will affect the least number of flip-flops. The clock gating optimizations are then performed and the test design rule checker checks if the clock offstate is consistent with the clock gating optimizations. Both methods of defining clock through the **create_test_clock** command or through the STIL procedure file (with the **read_test_protocol** command) are checked.

WHAT NEXT

Change the clock offstate by using the **create_test_clock** command or by modifying the STIL procedure file. Then, rerun the test design rule checker, the **dft_drc** command.

SEE ALSO

dft_drc (2), **create_test_clock** (2), **read_test_protocol** (2), **test_dft_drc_ungate_clocks** (3).

TEST-580 (Warning) All cells in multibit '%s' will not be scanned due to an explicit specification on cell '%s'.

DESCRIPTION

Some cells in the specified multibit are candidates for scan replacement, while at least one cell is explicitly marked as a non scan cell. In order to preserve the homogeneity of function in the multibit, DFT Compiler chooses to extent the dont_scan specification to all the cells of the multibit.

WHAT NEXT

If the whole bag is not to be scan replaced, perform a 'set_scan_element FALSE' on the complete multibit, otherwise remove the 'scan' and 'scan_element' attributes from all the cells in the multibit.

TEST-582 (Warning) All the cells in multibit '%s' are violated.

DESCRIPTION

Since a multibit structure must be homogeneous, any violation on a cell of a multibit which prevents scan replacement must also prevent scan replacement of all other cells in the multibit. This message notifies you that such a violation occured. The next message, TEST-583, points to the cell with the original violation.

WHAT NEXT

Look for the following information message to determine which cell of the multibit is previously violated. Study the previous messages to understand the original violation.

TEST-583 (Information) Because multibit member cell '%s' is previously violated.

DESCRIPTION

This message always follows a TEST-582 message. It makes explicit the violated cell that caused the whole muhltibit to become violated.

WHAT NEXT

Search for the original violation on the cell reported in the message and fix it.

TEST-584 (Information) The multibit contains: %s.

DESCRIPTION

This message lists the newly violated cells in the multibit refered to in the previous message.

WHAT NEXT

No action required.

TEST-585 (information) There are %d other multibits with the same condition.

DESCRIPTION

The preceeding set of messages flag a problem about a multibit. This message informs you that other multibits have the same condition.

WHAT NEXT

Use the verbose option of check_test to get individual messages for each multibit. Refer to the description of the previous set of messages.

TEST-586 (information) There is 1 other multibit with the same condition.

DESCRIPTION

The preceeding set of messages flag a problem about a multibit. This message informs you that exactly one multibit that has the same condition.

WHAT NEXT

Use the verbose option of check_test to get individual messages for each multibit. Refer to the description of the previous set of messages.

TEST-587 (warning) Multibits are ignored for partial scan

selection.

DESCRIPTION

Partial scan synthesis will not honor multibit specifications. This means that some cells in a multibit bag may get scan replaced while some may not. This non-uniform scan replacement may make multibit bag invalid as they contain cells of different functionality.

WHAT NEXT

To suppress this message, either remove the multibits from your design, or use a full scan methodology.

TEST-588 (warning) Cannot model multibit cell %s; treating it as a black box.

DESCRIPTION

The multibit cell cannot be modeled for one of the following reasons:

1. The target_library or target_libraries (as specified by the **dc_shell target_library** variable) do not contain a cell that is the single-bit degenerate of the multibit cell.

2. The target_library/libraries do not contain the multibit library cell. You must specify the library that contains the multibit with the **dc_shell target_library** variable.

3. Local optimization is disabled. This can be controlled using **set_compile_directives**.

WHAT NEXT

Check the possible causes listed above, and fix the problem.

TEST-590 (Warning) Multibit specification on multibit component '%s' ignored.

DESCRIPTION

This message indicates that scan synthesis cannot perform multibit optimization on the specified multibit component; the multibit specification is being ignored. As a

consequence of ignoring the multibit specification, scan synthesis will treat each bit of the the multibit component as an independent cell and might assign those individual cells to different scan chains.

The reason why the multibit specification is being ignored could be one of the following:

1. The component might contain a **dont_touch** attribute.

2. Local optimization might be disabled. This can be controlled using **set_compile_directives**.

3. The multibit component might not be wide enough, as specified by **set_multibit_options**.

4. The multibit component might contain cells with different functionalities.

WHAT NEXT

If it is acceptable for the multibit specification to be ignored for the specified design object, no action is required. Otherwise, check the specified multibit component or cell for conditions 1-4.

1. If the component contains **dont_touch** attributes, remove them with **set_dont_touch false** or **remove_attribute**.

2. If local optimization is disabled, enable it with **set_compile_directives -local_optimization true**.

3. If the multibit component is not wide enough, adjust the minimum width using **set_multibit_options -minimum_width**, or make the component wider.

4. Ensure that the multibit component contains cells with the same functionalities.

Use the **create_multibit** or **remove_multibit** commands to manipulate multibit components, then re-execute the **check_test** command.

TEST-591 (Warning) There exists a cell %s on the bus which is not controllable. So the tristate disabling logic on this bus is not synthesized.

DESCRIPTION

This happens when a cell driving a bus has a tristate pin but no way of controlling it. This wil prevent addition of any disabling logic to this tristate-bus.

WHAT NEXT

Update the cell and rerun the command.

TEST-592 (Warning) There is a contention while controlling cell %s on the bus. So the tristate disabling logic on this bus is not synthesized.

DESCRIPTION

This happens when a cell driving a bus has a tristate pin and the logic to control it contradict another driver of the same bus. This wil prevent addition of any disabling logic to this tristate-bus.

WHAT NEXT

Update the cell and rerun the command.

TEST-593 (Information) All cells in multibit component '%s' are violated.

DESCRIPTION

This message informs you that all the cells is the given multibit are violated. This is necessary in order to ensure that all the cells in the multibit are either scan replaced together, or not at all.

WHAT NEXT

Refer to the previous message to understand why some cell in the multibit component was violated.

TEST-594 (warning) Clock pin %s of cell %s (%s) has active or unknown value at off state of clock %s.

DESCRIPTION

You receive this warning message because clock pins controlled by a system clock have active or unknown values at the beginning of the system clock cycle.

This warning message is issued by the **check_dft**, **check_scan**, and **check_test** commands for a level-sensitive scan design (LSSD) pre-scan.

The result is that scan chains are improperly constructed with some scan cells having the system clock and the test clock active at the same time.

WHAT NEXT

Correct the design by ensuring that all of the clock pins driven by a system clock are at their inactive values when the system clock is at its off state.

SEE ALSO

check_dft (2), **check_scan** (2), **check_test** (2).

TEST-595 (information) There are %d other such violation(s).

DESCRIPTION

When **dft_drc** runs in ordinary (nonverbose) mode,it only lists the first instance of certain violations. This message shows the number of additional such violations.

WHAT NEXT

The warning message that appears before this one indicates the design rule violation. (There might be additional information messages that provide more details about the first violation.)

If you want to see details of all the violations of a rule, run **dft_drc** in verbose mode. For example, **check_test** might produce the following messages:

Warning: Warning: Chains 1 and 15 always have the same load value. (R9-1)
Information: There are 1 other such violation(s). (TEST-595)

However, if you run fbdft_drc -verbose, you see details of all the violations:

TEST-600 (Warning) All cells in multibit %s are violated because multibit cell %s is previously violated.

DESCRIPTION

You receive this warning message when all of the cells in the specified multibit are violated because of a prior violation on one of the cells of the multibit. This action is necessary to ensure that all cells in the multibit are either scan replaced together, or not at all.

WHAT NEXT

Search for and fix the original violation on the cell reported in the message.

TEST-601 (warning) Inferring default device package '%s'.

DESCRIPTION

This warning message indicates that you have not selected any default package for the Boundary Scan Design using the **set_bsd_configuration** command. However, as only one port-to-pin map file was read in, this package is assumed to be the default device package.

WHAT NEXT

Nothing

TEST-602 (error) '%s' is not an RTL file. The following modules cannot be modifed: %s.

DESCRIPTION

The specified modules have been identified as part of the named file. This file is apparently not an RTL source file, so the modification of the source cannot be performed. File names are stored at the time of the reading of the RTL if the variable 'hdlin_enable_rtldrc_info' is set to true. Otherwise the source is assumed to be a non-editable db file.

Be aware that when the 'hdlin_enable_rtldrc_info' is set to true, the internally represented RTL enables the tracing of the circuit topology back to the source, at the expense of synthesizability. You should not assert this variable if the RTL is meant to be synthesized without modification, least you accept significant degradation in QoR.

WHAT NEXT

Ensure that the variable 'hdlin_enable_rtldrc_info' is set to true.

TEST-603 (information) The following RTL modules, from file

’%s’, are edited: %s.

DESCRIPTION

This is a simple information message that lists the modules of a file that require modification at the RTL source. The actual modification is performed immediately after the issuing of this message.

WHAT NEXT

Continue reading.

TEST-604 (information) Uniquifying ’%s’ into %d new modules.

DESCRIPTION

This is a simple information message stating that the named module has multiple instances requiring different modifications. The module itself is uniquified into as many copies as required to satisfy all the modification requirements. The copies are stored in the same file as the original, immediately before it. The references, from other modules, are adjusted in consequence.

WHAT NEXT

Continue reading.

TEST-605 (error) The RTL Editor executable ’%s’ is not found.

DESCRIPTION

The RTL Editor executable is not found. No modification of RTL can be performed. Typically, the executable is obtained from the root. The cause of this message is either an unsupported platform, an incorrect specification of the root, or faulty installation.

WHAT NEXT

Check the availability of the RTL editing feature for the current platform in the Release Notes. Check the specification of the Synopsys root. Contact your systems administrator.

TEST-606 (error) Cannot start the RTL Editor.

DESCRIPTION

The RTL Editor executable cannot be started. No modification of RTL can be performed. This is most likely due to a runtime configuation issue.

WHAT NEXT

Check execute permissions on the RTL Editor.

TEST-610 (warning) Static X cell analysis may be inaccurate on design containing cells with CTL models.

DESCRIPTION

This warning message indicates that the current design has cells with CTL models therefore static X cell analysis may be inaccurate.

TEST-700 (warning) %s '%s' %s '%s' does not exist and hence will be ignored. The remaining valid non empty scan group specification will be accepted.

DESCRIPTION

You receive this warning message because the **set_scan_group** command was issued with non-existing elements or invalid elements. A scan group can have elements as part of its -include_elements option, that could be a valid sequential cell name, or a core segment name, or a design instance name. Scan groups cannot have nested scan groups has part of its specification. Also Scan groups cannot have elements that belong to different clock domains or different clock edges. In other words, scan group can accept only elements from same clock and edge. When this message is showed, the element will be ignored from the scan group specification during scan architecting.

If the scan group has a design instance name as part of include_elements which is already scan inserted and has scan chain elements clocked by more than one clock, the scan group specification will be ignored and the model for that instance will not be used for constructing the scan chains. Hence the elements/cells within this design instance will be considered as if it is not scan inserted and new scan chains will be constructed accordingly.

SEE ALSO

set_scan_group

TEST-801 (information) There is 1 such other violation.

DESCRIPTION

This message is issued by the check_bsd command in conjunction with the violation message just above it.

This message is issued in both the verbose and non-verbose modes of check_bsd. In verbose mode this message is followed by the name of the object with the same violation.

WHAT NEXT

Investigate the reason for the previous violation, and re-run check_bsd when this problem is fixed.

SEE ALSO

check_bsd.

TEST-802 (information) There are %d such other violations.

DESCRIPTION

This message is issued by the check_bsd command in conjunction with the violation message just above it.

This message is issued in both the verbose and non-verbose modes of check_bsd. In verbose mode this message is followed by the name of the objects with the same violation.

WHAT NEXT

Investigate the reason for the previous violation, and re-run check_bsd when this problem is fixed.

SEE ALSO

check_bsd.

TEST-811 (error) Mandatory IEEE 1149.1 test port %s missing.

DESCRIPTION

The mandatory 1149.1 boundary scan Test Access Port is missing. You are suppose to specify at least the four mandatory Test Access Ports.

WHAT NEXT

Use the command set_bsd_port <tdi | tdo | tms | tck | trst> <port_name> to specify the four or five Test Access Ports in DB mode.

Use the command set_dft_signal -type <tdi | tdo | tms | tck | trst> -port <port_name> -view existing_dft to specify the four or five Test Access Ports in XG mode.

TEST-812 (error) NO IEEE 1149.1 test ports have been identified.

DESCRIPTION

None of the Test Access Ports have been defined. You are suppose to specify at least the four mandatory Test Access Ports.

WHAT NEXT

Use the command set_bsd_port <tdi | tdo | tms | tck | trst> <port_name> to specify the four or five Test Access Ports in DB mode.

Use the command set_dft_signal -type <tdi | tdo | tms | tck | trst> -port <port_name> -view existing_dft to specify the four or five Test Access Ports in XG mode.

TEST-813 (error) %s TAP Controller state flops have been found, which is an insufficient number of state flops. There must be at least four.

DESCRIPTION

The tool is unable to find the minimum number of TAP Controller states. The 1149.1 TAP Controller has 16 states which can be realize by at least 4 state elements. Hence this TAP controller is either not compliant to the standards or there is some

design problem. If it is a design problem then the diagnostic will be able to specify it. If the problem is of not setting of compliance ports, then these ports should be specified.

WHAT NEXT

1. Use set_tap_elements to specify the TAP state elements as follows : set_tap_elements -state_cells <list of TAP state elements> 2. Specify the compliance enable ports as follows if not specified and diagnostic finds it to be a problem. set_bsd_compliance {<port_name> <pattern>} 3. If there is some design problem then it should be rectified before running check_bsd again.

TEST-814 (error) TAP controller makes an illegal transition from state %s to state %s with TMS at logic value %s. The TAP controller should make transition to state %s.

DESCRIPTION

The 1149.1 TAP Controller has 16 states and a well defined state transition diagram is defined in chapter 5 of IEEE Std 1149.1. The TAP Controller has made an illegal transition to a state. This can occur a. If the synchronizing sequence of "11111" doesn’t take the TAP Controller to Test-Logic-Reset state. b. If the TAP Controller state machine is malfunctioning. Diagnostic will not help in this case.

WHAT NEXT

You should correct the functioning of synchronizing sequence or the TAP Controller state machine before re-running **check_bsd**.

TEST-815 (error) Low halt state for TCK does not exist.

DESCRIPTION

As defined in chapter 3 of IEEE Std 1149.1, the dedicated TCK input is provided to permit shifting of test data concurrently with system operation of the component. This require TCK to be stopped for a period to do other support functions during test, for example an ATE needs to fetch test data from backup memory. Hence, the standard requires that TCK can be stopped at 0 indefinitely without causing any change to state of test logic. Therefore, while TCK is stopped at 0, state devices are required to retain their state so that the test logic can continue its operation when the clock operation restarts. The tool was able to find the TAP Controller state devices are not able to retain their state, when TCK is stopped at 0.

WHAT NEXT

You should rectify this problem by making the state devices of TAP Controller to retain their state, when TCK is stopped at 0.

TEST-816 (error) TRST does not reset TAP controller asynchronously. TRST specification ignored.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 3 that the TAP controller shall be asynchronously reset to the Test-Logic-Reset controller state when a logic 0 is applied to TRST port. The design port which has been specified as TRST doesn’t reset the TAP controller asynchronously, hence the specification is being removed. The cause might be the problem with the TAP controller reset operation or the specification of a wrong design port have been done as TRST.

WHAT NEXT

You can do the following : 1. use set_tap_elements to specify all the TAP state elements or 2. correct the reset problem of TAP controller or 3. assign attribute to correct the design port as TRST.

TEST-816a (warning) TRST reset TAP controller synchronously but not asynchronously. TRST specification ignored.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 3 that the TAP controller shall be asynchronously reset to the Test-Logic-Reset controller state when a logic 0 is applied to TRST port. The design port which have been specified as TRST reset the TAP controller synchronously. This is not correct and hence the specification is being removed. The cause might be the problem with the TAP controller reset operation.

WHAT NEXT

You should correct the reset problem of TAP controller before re-running check_bsd.

TEST-816b (warning) TAP controller is not reset at power up.

DESCRIPTION

The IEEE Std 1149.1 states in chapter 5 that TAP controller should either be initialized by TRST port or at power-up by operation of circuitry built into the test logic. Because the design doesn't specify any TRST port and power-up initialization is not correct. Hence, it is not possible to externally control the TAP controller.

WHAT NEXT

Check the power-up circuitry if it exists; otherwise, assign the TRST port to the design if you forgot to.

SEE ALSO

set_bsd_power_up_reset (2)

TEST-817 (warning) TDO driver can not be active in the TAP controller state %s.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 3 and 5 that the TDO driver shall be set to inactive state except when the scanning of data is in progress.

WHAT NEXT

Check the TDO logic to put the TDO driver into inactive state during this TAP controller state.

TEST-818 (error) TDO driver must be active in TAP Controller state %s.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 3 and 5 that the TDO driver shall be set to active state when the scanning of data is in progress.

WHAT NEXT

Check the TDO logic to put the TDO driver into active state during this TAP controller state.

TEST-819 (warning) Undriven input port %s is floating. When undriven, this port should behave as though it was driven by logic one.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 3 that the design of circuitry fed from the Test Access Ports TMS, TDI and TRST shall be such that an undriven input produces a response identical to the application of a logic 1.

WHAT NEXT

You should correct the problem with the specified Test Access Port before re-running check_bsd.

TEST-820 (error) EXTEST opcode is not specified.

DESCRIPTION

You get this error message during check_bsd when you are using the 2001 revision(default) of the IEEE1149.1 standard for the compliance check and have not specified the opcode for the EXTEST instruction.

In the 2001 revision of the IEEE1149.1 standard, all-0's is no longer the default opcode for the EXTEST instruction, so user needs to explicitly specifiy the EXTEST opcode for the check_bsd using the set_bsd_instruction command.

WHAT NEXT

CaseI: If you are checking the conformance against the 2001 revision(default) of the IEEE1149.1 standard, then specify the EXTEST opcode using the set_bsd_instruction command and rerun check_bsd.

Example: set_bsd_instruction EXTEST -code {0010}

CaseII: If you are not upgraded to the 2001 revision of the IEEE1149.1 standard, and still following the 1993 version, you can switch back to the older version (non default mode) using the set_bsd_configuration command and rerun check_bsd. In this mode check_bsd assumes all-0's opcode for the EXTEST instruction and user does not need to specifiy the EXTEST opcode.

Example: set_bsd_configuration -ieee1149.1_1993

SEE ALSO

set_bsd_instruction set_bsd_configuration check_bsd

TEST-821 (warning) TDO should not change on the rising edge of TCK in the TAP controller state %s.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 3 that to ensure a race-free operation, changes in the sate of the signal driven through TDO shall occur only on the falling edge of TCK.

WHAT NEXT

You should correct the behavior of test logic at TDO to change on the falling edge of TCK.

TEST-822 (warning) TAP Controller should not be reset by the functional input %s. A dedicated reset port or power-up sequence is required.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 5 that TAP controller shall not be initialized by operation of any system input, such as system reset.

WHAT NEXT

You should fix the design by removing initialization by any system input of the TAP controller.

TEST-823 (error) TAP controller can not be initialized by the

synchronizing sequence of 11111 on TMS.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 5 that no matter what the original state of TAP controller, it should enter Test-Logic-Reset when TMS is held high for at least five rising edges of TCK.

WHAT NEXT

Check the TAP controller logic and rectify the synchronizing sequence problem.

TEST-824 (warning) Data is inverted during shift from TDI to TDO.

DESCRIPTION

The IEEE Std 1149.1 stated in Chapter 6 and 8 that there can be no inversion of data between the serial input and serial output of IR (instruction register) or any TDRs (test data register).

WHAT NEXT

Rectify the logic at the cell of the shift register.

TEST-824a (information) Data is inverted during shift from TDI to TDO at the TDO port cell %s.

DESCRIPTION

The IEEE Std 1149.1 states in Chapter 6 and 8 that there can be no inversion of data between the serial input and serial output of IR (instruction register) or any TDRs (test data register).

WHAT NEXT

Rectify the TDO logic.

TEST-824b (warning) Data is inverted during shift from TDI to

TDO at cell %s of the shift register.

DESCRIPTION

The IEEE Std 1149.1 stated in Chapter 6 and 8 that there can be no inversion of data between the serial input and serial output of IR (instruction register) or any TDRs (test data register).

WHAT NEXT

Rectify the logic at the cell of the shift register.

TEST-825 (error) Cannot access Instruction Register during the shift-IR TAP controller state.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 6 that a shift register of length at least 2 should be put between TDI and TDO in the TAP controller Shift-IR state. As no shift register is inferred the tool can not progress. It is a non-tolerable violation and should be fixed.

WHAT NEXT

Fix the IR (instruction Register) problem. If the diagnostic provides a port controlling the inference, then this port should be set as compliance enable port using the command.

TEST-826 (error) Illegal Instruction Register Length %s.

DESCRIPTION

The IEEE Std 1149.1 states in Chapter 6, section 6.1.1.8 that the instruction register (IR) shall include at least TWO shift-register-based cells capable of holding instruction data.

WHAT NEXT

Correct your design to include, at a minimum, two IR cells for the instruction register length.

TEST-827 (error) TAP controller state flops make state transitions at the falling edge of TCK instead of on the rising edge of TCK.

DESCRIPTION

The IEEE Std 1149.1 states in Chapter 6, section 6.1.1(b) that the transitions of the TAP controller shall occur based upon the value of TMS at the rising edge of TCK.

WHAT NEXT

Examine and correct the TAP controller FSM architecture to conform with the rule 6.1.1(b).

TEST-828 (error) The capture value of the least significant bits in the instruction register is %s%s. It must be the fixed pattern "01".

DESCRIPTION

The IEEE Std 1149.1 states in Chapter 6 that the two least significant instruction register (IR) cells (that is those nearest the serial output) must load a fixed binary "01" pattern (the 1 into the least significant bit location) in the Capture-DR controller state.

WHAT NEXT

Correct the IR design.

TEST-829 (warning) The length of Device Identification Register is %s. It should be 32.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 11 that the component shall contain a vendor-defined identification code, containing four fields (32 bits) [Version (4 bits), Part Number(16 bits), Manufacturer identity (11 bits), 1]. Hence the Device Identification Register should be of length 32 bits.

WHAT NEXT

You should correct the design of Device Identification Register.

TEST-830a (warning) Unable to access any Register to be serially connected between TDI and TDO in the Test-Logic-Reset state.

DESCRIPTION

The IEEE Std 1149.1 states in chapter 5 that IR initialize to either IDCODE or, if the optional DIR (device identification register) is not provided, BYPASS instruction. No register is found during the Capture-DR state after the TAP Controller has been taken through the Test-Logic-Reset state. This indicate a problem with either a. DIR to be serially connected between TDI and TDO b. Not a proper instruction is loaded during the Test-Logic-Reset state

WHAT NEXT

Correct the design of IR to load either BYPASS or IDCODE instruction or correct the design of DIR.

TEST-831 (error) Mandatory BYPASS instruction is not implemented with all-ones opcode.

DESCRIPTION

You get this error message when **-infer_instructions** option of the **check_bsd** command is set to false(default) and **check_bsd**finds that all-ones opcode does not implement the mandatory **BYPASS** instruction .

The IEEE Std 1149.1 state in chapter 7 that each component shall provide a BYPASS instruction with all-ones opcode.

WHAT NEXT

Correct the design to implement the BYPASS instruction with all-ones opcode.

TEST-832 (error) Cannot access BYPASS Register during the shift-DR TAP controller state with the "all ones" instruction

opcode.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 7 that a binary code for BYPASS instruction shall be {111...1) (i.e., a logic 1 entered into every instruction register cell).

WHAT NEXT

You should correct the design of BYPASS instruction to include an "all ones" opcode.

TEST-834 (error) Cannot access Boundary Scan Register during the shift-DR TAP controller state with the "%s" instruction opcode.

DESCRIPTION

The IEEE Std 1149.1-1993 state in chapter 7 that a binary code for the EXTEST instruction shall be {000...0} (i.e., a logic 0 is loaded into every IR cell).

Later versions of IEEE 1149.1 allow any opcode for EXTEST instruction.

The above error message is issued when Boundary Scan Register is not selected to connect between TDI and TDO during the EXTEST instruction opcode in Shift-DR Tap state.

WHAT NEXT

If EXTEST instruction doesn’t use "all zeros" opcode for IEEE Std 1149.1-1993 implementation, you should correct the EXTEST instruction to include an "all zeros" opcode.

If EXTEST instruction uses the correct opcode, check if there is a breakage in the Boundary Scan Regsiter accseesed by the EXTEST instruction in Shift-DR Tap state.

TEST-835 (error) The capture value of the least significant bit in the Device Identification Register is logic zero. It must be logic

one.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 11 that a DIR (device identification register) should load a constant logic 1 into its LSB in the Test-Logic-Reset TAP Controller state.

WHAT NEXT

You should correct the design of DIR.

TEST-836 (Error) Illegal manufacturing code %s has been captured in the Device Identification Register.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 11 that the manufacturer code 00001111111 shall not be used in components that are otherwise compatible with this standard.

WHAT NEXT

You should correct the design of device identification register.

TEST-837 (Warning) No Register is selected to connect between TDI and TDO during instruction opcode %s.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 7 that each instruction shall completely define the set of TDRs (test data register) that may operate while the instruction is current.

WHAT NEXT

You should either map this opcode to select BYPASS if unused otherwise correct the design of instruction opcode to select a TDR(s).

TEST-838 (warning) An INPUT boundary scan register cell is

missing on design port %s.

DESCRIPTION

The IEEE Std 1149.1 states in Chapter 10 that one or more boundary scan register cells must be provided at each system input of the on-chip system logic.

WHAT NEXT

Provide the missing boundary scan register cell on this port.

TEST-838a (warning) An OUTPUT boundary scan register cell is missing on design port %s.

DESCRIPTION

The IEEE Std 1149.1 states in Chapter 10 that one or more boundary scan register cells must be provided at each system output of the on-chip system logic.

WHAT NEXT

Provide the missing boundary scan register cell on this port.

TEST-839 (error) A boundary scan register cell %s cannot be placed on TAP port %s.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 10 state that boundary-scan register cells shall not be provided at: TAP pins (TCK, TDI, TDO, TMS, and TRST*).

WHAT NEXT

Remove the boundary-scan register cell from the TAP port.

TEST-840 (warning) A boundary scan register cell %s cannot be

placed on compliance port %s.

DESCRIPTION

The IEEE Std 1149.1 states in chapter 10 that boundary-scan register cells shall not be provided at pins that enable compliance to this standard.

WHAT NEXT

Remove the boundary-scan register cell from this port.

TEST-841 (error) Not able to infer the mandatory SAMPLE/PRELOAD instruction.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 7 that each component shall provide a SAMPLE/PRELOAD instruction. The SAMPLE/PRELOAD instruction is inferred by analyzing the capturing of input ports by the boundary-scan register cells on the design input ports and the conditioning of design output ports.

WHAT NEXT

Correct the design to provide a SAMPLE/PRELOAD instruction or correct the capturing of boundary-scan register cells on the design input ports or conditioning of design output ports as defined.

TEST-842 (error) Mandatory SAMPLE/PRELOAD instruction is not implemented (or not specified).

DESCRIPTION

You get this error message when **-infer_instructions** option of the **fBset_bsd_configuration** command is set to false(default) and **check_bsd** does not find the mandatory **SAMPLE/PRELOAD** instruction.

The IEEE Std 1149.1 state in chapter 7 that each component shall provide a SAMPLE/PRELOAD instruction. The SAMPLE/PRELOAD instruction is inferred by analyzing the capturing of input ports by the boundary-scan register cells on the design input ports and the conditioning of design output ports.

If you are running **check_bsd** on a design for which boundary-scan synthesis is done by BSD compiler then **check_bsd** analyzes the opcode(s) for SAMPLE/PRELOAD passed by

insert_bsd else **check_bsd** looks for the opcodes for SAMPLE/PRELOAD specified by the **set_bsd_instruction** command.

WHAT NEXT

If you are running **check_bsd** on a design for which boundary-scan synthesis is not done by BSD compiler then make sure that you specify correct opcode(s) for the implemented SAMPLE/PRELOAD instruction and make sure that the design implements the SAMPLE/PRELOAD instruction correctly. If you do not know the SAMPLE/PRELOAD instruction opcode(s), set the **-infer_instructions** option of the **set_bsd_configuration** command to true and rerun **check_bsd**. This will let **check_bsd** examine all opcodes for SAMPLE/PRELOAD.

TEST-843 (error) Logic cannot exist between boundary scan cell %s and design port %s.

DESCRIPTION

The IEEE Std 1149.1 states in Chapter 10 that there cannot be logic between any boundary scan register cell and the system pin to which that cell is connected.

WHAT NEXT

Correct the design by removing the logic between the boundary scan register cell and the design port.

TEST-844 (error) The Instruction Register Update flops update on the rising edge of TCK instead of falling edge of TCK.

DESCRIPTION

The IEEE Std 1149.1 states in Chapter 5 and 6 that the instruction shifted into the instruction register is latched onto parallel output from the shift-register path on the falling edge of TCK. This error shows that the output is not latched on the falling edge but on the next rising edge.

WHAT NEXT

Correct the design by making the update stage latch on the falling edge of TCK.

TEST-845 (warning) The compliance-enable pattern %s do not

cause the component to be fully compliant with this standard. This pattern is being removed from the set of patterns.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 3 that any one of the compliance-enable patterns, when applied to the compliance-enable inputs without regard to preceding patterns on these inputs, shall cause the component to be fully compliant with this standard.

WHAT NEXT

Correct the design to meet this requirement or remove the pattern from the compliance enable list.

TEST-846 (error) The Boundary Scan Register Update flops update on the rising edge of TCK instead of falling edge of TCK.

DESCRIPTION

The IEEE Std 1149.1 states in Chapter 5 and 7 that the data shifted into the BS register is latched onto parallel output from the shift-register path on the falling edge of TCK. This error shows that the output is not latched on the falling edge but on the next rising edge.

WHAT NEXT

Correct the design by making the update stage latch on the falling edge of TCK.

TEST-847 (warning) The BSR Update flops illegally update during Update-DR under CLAMP instruction.

DESCRIPTION

The IEEE Std 1149.1 states in Chapter 10 that all latched output of BSR should retain their states until 1. The Test-Logic-Reset controller state is entered as a result of application of a logic ’0’ at TRST* or 2. The first falling edge of TCK occurs in Test-Logic-Reset controller state when that state is entered as a result of signals applied at TCK and TMS and the instruction selects the BSR between TDI and TDO.

This error shows that the output is latched on the falling edge of TCK in Update-DR

while CLAMP is selected. CLAMP selects the BYPASS register between TDI and TDO (not the BSR), so the BSR Update flops should not update during Update-DR under CLAMP instruction.

WHAT NEXT

Correct the design by making the update stage unchanged during CLAMP.

Case1: If you are using synchronous implementation then you can correct the design by driving the BSR cell's update_en from Tap controller's sync_update_dr signal gated with the decoded instruction opcodes which select the BSR between TDI and TDO, instead of driving it directly from the Tap controller's sync_update_dr signal.

Case2: If you are using asynchronous implementation then you can correct the design by driving the BSR cell's update_clk from Tap controller's update_dr signal gated with the decoded instruction opcodes which select the BSR between TDI and TDO, instead of driving it directly from the Tap controller's update_dr signal.

Example: ---------- Suppose Tap/I[3..0] is the instruction bus, and you have the following opcode assignments in your boundary-scan design:

EXTEST Instruction(Selcting BSR between TDI and TDO) = 0000 0010 SAMPLE Instruction(Selcting BSR between TDI and TDO) = 0111 1000 CLAMP Instruction(Selcting BYPASS between TDI and TDO) = 1001 1010 HIGHZ Instruction(Selcting BSR between TDI and TDO) = 1011 1110 BYPASS Instruction(Selcting BYPASS between TDI and TDO) = 1111 & the remaining opcodes

Opcodes selecting the BSR = 0000 0010 0111 1000 1011 1110

Depending upon whether you have a synchronous or asynchronous design, you will fix this violation as follows.

Case1: If you are using a synchronous implementation then you can derive the BSR cell's update_en signal as follows:

update_en = (Tap Controller's sync_update_dr) & (!I3&!I2&!I1&!I0 | !I3&!I2&I1&!I0 | !I3&I2&I1&I0 | I3&!I2&!I1&!I0 | I3&!I2&I1&I0 | I3&I2&I1&!I0) (Most probably what you were generating update_en = (Tap Controller's sync_update_dr))

Case2: If you are using a asynchronous implementation then you can derive the BSR cell's update_clk signal as follows:

update_clk = (Tap Controller's update_dr) & (!I3&!I2&!I1&!I0 | !I3&!I2&I1&!I0 | !I3&I2&I1&I0 | I3&!I2&!I1&!I0 | I3&!I2&I1&I0 | I3&I2&I1&!I0) (Most probably what you were generating update_clk = (Tap Controller's update_dr))

TEST-848 (warning) The BSR Update flops illegally update during Update-DR under RUNBIST instruction, while selecting

annother TDR as shift register.

DESCRIPTION

The IEEE Std 1149.1 states in Chapter 10 that all latched output of BSR should retain their states until 1. The Test-Logic-Reset controller state is entered as a result of application of a logic ’0’ at TRST* or 2. The first falling edge of TCK occurs in Test-Logic-Reset controller state when that state is entered as a result of signals applied at TCK and TMS.

This error shows that the output is latched on the falling edge of TCK in Update-DR while RUNBIST is selected.

WHAT NEXT

Correct the design by making the update stage unchanged during RUNBIST.

TEST-849 (warning) The tristate pin %s on the cell %s has multiple Boundary-Scan Register controlling cells.

DESCRIPTION

A pad cell was found with controlling input being driven by multiple BSR cell, which is a violation of IEEE Std 1149.1 rule 10.6.1c.

WHAT NEXT

Correct the logic so that one boundary-scan register cell drives the control input.

TEST-850 (Warning) Initialization using TMS synchronizing sequence "11111" does not match the initialization using the TRST port or power-up sequence. This process will continue by using the TMS synchronizing sequence.

DESCRIPTION

The IEEE Std 1149.1 states in chapter 5 that the TAP controller can be initialized into the Test-Logic-Reset state by one of the following: a. At power-up either by either using the TRST* signal or as a result of circuitry built into the test logic.

b. By holding TMS high for at least five rising edges of TCK. On this design the two initialized states are not same.

WHAT NEXT

Check the design of TAP controller and verify the initialization by both of the aforementioned methods to be Test-Logic-Reset state.

TEST-850a (warning) No external method to reset the TAP controller (such as TRST port or power-up) has been provided. This process will continue by forcing logic values on the TAP controller state elements.

DESCRIPTION

The IEEE Std 1149.1 states in chapter 5 that the TAP controller can be initialized into the Test-Logic-Reset state at power-up either by using the TRST* signal or as a result of circuitry built into the test logic. Because neither of these have been provided to initialize that TAP controller, there isn’t an external way to control the TAP controller.

WHAT NEXT

You should correct the TAP controller design and provide, at least, one of the specified initialization mechanism.

SEE ALSO

set_bsd_power_up_reset (2)

TEST-851 (Error) The shift flops of Instruction Register are not clocking on the positive edge of TCK during the Capture-IR TAP Controller state.

DESCRIPTION

While checking for capture value in the Instruction Register during Capture-IR, it is found that the shift flops of the Instruction Register are not clocked on the positive edge of the TCK. IEEE Std. 1149.1 in rule 6.2.1(c) states that all operations of shift-register stages shall occur on the rising edge of TCK following entry into a controller state.

WHAT NEXT

Correct the design to clock the IR shift flops on the positive edge of TCK during the Capture-IR state and rerun **check_bsd**.

TEST-852 (Warning) Opcode %s specified for %s instruction does not select the specified/implied %s register. Removing the opcode.

DESCRIPTION

You get this warning message when **check_bsd** finds that the opcode you specified by **set_bsd_instruction** command for the instruction does not select the correct test data register for the instruction. When **-infer_instructions** option of the **fBset_bsd_configuration** command is set to false(default) and **check_bsd** uses the implemented instructions information provided by the **set_bsd_instruction** command.

WHAT NEXT

Make sure that you specify the correct opcode and check the design for implemented behavior of the opcode.

TEST-853 (Warning) Opcode %s specified for %s instruction does not cause valid conditioning. Removing the opcode.

DESCRIPTION

You get this warning message when **check_bsd** finds that the opcode you specified by **set_bsd_instruction** command for the instruction does not comply to the input/output conditioning for the instruction. When **-infer_instructions** option of the **fBset_bsd_configuration** command is set to false(default) and **check_bsd** uses the implemented instructions information provided by the **set_bsd_instruction** command.

WHAT NEXT

Make sure that you specify the correct opcode and check the design for implemented behavior of the opcode.

TEST-854 (information) There is a break in the shift register

chain at flop %s.

DESCRIPTION

During the inference of the shift-register stage between the TDI and TDO, a break at the cell was found. The break is because the cell driving is not active. Diagnostic will find a cause of unknown in full.

WHAT NEXT

Correct the design by removing the cause and rerun **check_bsd**.

TEST-855 (information) There is a break in the shift register chain
due to test data out (TDO) port not being driven by the shift register chain.

DESCRIPTION

During the inference of the shift-register stage between the TDI and TDO, a break at TDO was found. This shows the TDO logic is not enabled. Diagnostic will find an actual cause of this.

WHAT NEXT

Check your design for proper the shift enable connection, missing clocks, or broken internal nets. Correct the design by removing the cause and rerun check_bsd.

TEST-856 (warning) The design TDO port %s is not enabled.

DESCRIPTION

During the inferences, the design TDO port was found not to be enabled. Hence, no simulation token can propagate to the TDO port. This can cause problems at both the traversing of TAP states, as well as the inference of shift register stage. Diagnostics can help to pin-point the cause.

WHAT NEXT

Run the software in verbose mode to find the actual cause of the break. Correct the design by removing the cause and rerun.

TEST-857 (warning) Synchronous mode for the shift register was not inferred. There seems to be break in the shift register.

DESCRIPTION

During the inference of shift-register stage between the TDI and TDO, a break at the cell has been found. The break is due to the fact that the cell driving is not active. Diagnostic will find a cause of unknown in full.

WHAT NEXT

Run the software in diagnostic mode to know the actual cause of the break. Correct the design by removing the cause and re-run check_bsd.

TEST-858 (warning) The update elements of the instruction register should not be reset on the rising edge of test clock TCK.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 6, section 6.2.1(d) that the data present at the parallel output of the instruction register shall be latched from the shift-register state on the falling edge of TCK in the Update-IR controller state.

WHAT NEXT

Correct the design to latch the data from the shift-register flip-flops into the parallel hold latches on the falling edge of TCK during the Update-IR controller state.

TEST-859 (error) Unable to find the Boundary Scan Register Update flops on falling edge of TCK.

DESCRIPTION

The IEEE Std 1149.1 states in Chapter 5 and 7 that the data shifted into the boundary-scan register is latched onto parallel output from the shift-register path on the falling edge of TCK. This error shows that the output is not latched on the falling edge of TCK. The boundary scan register update flops are either missing or not designed according to the IEEE 1149.1 Standard (10.3.1.b).

WHAT NEXT

Correct the design for one of the following three possible causes: 1. No update flip flop exists in the update register. 2. There are multiple flip flops in the update register. 3. The update register is not being clocked by the negative edge of TCK.

TEST-859a (warning) Boundary Scan Register Update Flops change state during BYPASS Update-DR operation.

DESCRIPTION

The IEEE Std 1149.1 states in Chapter 10 (10.3.1c) that when the boundary scan register is NOT selected between TDI and TDO, all latched parallel outputs should retain their last state until the Test-Logic-Reset controller state is entered asynchronously(Logic 0 at TRST) or the first falling edge of TCK occurs when the Test-Logic-Reset controller state is entered synchronously(as a result of signals applied at TCK and TMS).

WHAT NEXT

Correct the design. Make sure that all the boundary scan register update flops are clocked in the Update-DR state only when either of the instructions selecting BSR is active and not otherwise.

Case1: If you are using synchronous implementation then you can correct the design by driving the BSR cell’s update_en from Tap controller’s sync_update_dr signal gated with the decoded instruction opcodes which select the BSR between TDI and TDO, instead of driving it directly from the Tap controller’s sync_update_dr signal.

Case2: If you are using asynchronous implementation then you can correct the design by driving the BSR cell’s update_clk from Tap controller’s update_dr signal gated with the decoded instruction opcodes which select the BSR between TDI and TDO, instead of driving it directly from the Tap controller’s update_dr signal.

Example: ---------- Suppose Tap/I[3..0] is the instruction bus, and you have the following opcode assignments in your boundary-scan design:

EXTEST Instruction(Selcting BSR between TDI and TDO) = 0000 0010 SAMPLE Instruction(Selcting BSR between TDI and TDO) = 0111 1000 CLAMP Instruction(Selcting BYPASS between TDI and TDO) = 1001 1010 HIGHZ Instruction(Selcting BSR between TDI and TDO) = 1011 1110 BYPASS Instruction(Selcting BYPASS between TDI and TDO) = 1111 & the remaining opcodes

Opcodes selecting the BSR = 0000 0010 0111 1000 1011 1110

Depending upon whether you have a synchronous or asynchronous design, you will fix this violation as follows.

Case1: If you are using a synchronous implementation then you can derive the BSR cell’s update_en signal as follows:

update_en = (Tap Controller's sync_update_dr) & (!I3&!I2&!I1&!I0 | !I3&!I2&I1&!I0 | !I3&I2&I1&I0 | I3&!I2&!I1&!I0 | I3&!I2&I1&I0 | I3&I2&I1&!I0) (Most probably you were genrating update_en = (Tap Controller's sync_update_dr))

Case2: If you are using a asynchronous implementation then you can derive the BSR cell's update_clk signal as follows:

update_clk = (Tap Controller's update_dr) & (!I3&!I2&!I1&!I0 | !I3&!I2&I1&!I0 | !I3&I2&I1&I0 | I3&!I2&!I1&!I0 | I3&!I2&I1&I0 | I3&I2&I1&!I0) (Most probably what you were generating update_clk = (Tap Controller's update_dr))

TEST-859b (warning) Boundary Scan Register shifts data during BYPASS Shift-DR operation.

DESCRIPTION

You get this warning when the the boundary scan register shifts data during the Shift-DR state of the BYPASS instruction. The IEEE Std 1149.1 states in Chapter 8 (8.3.1g) that when no operation of a selected test data register is required in a given controller state, the register shall retain its last state unchanged.

WHAT NEXT

Correct the design. Make sure that all the boundary scan register shift flops are clocked in the Shift-DR state only when either of the instructions selecting BSR is active and not otherwise.

Case1: If you are using synchronous implementation then you can correct the design by driving the BSR cell's update_en from Tap controller's sync_update_dr signal gated with the decoded instruction opcodes which select the BSR between TDI and TDO, instead of driving it directly from the Tap controller's sync_update_dr signal.

Case2: If you are using asynchronous implementation then you can correct the design by driving the BSR cell's update_clk from Tap controller's update_dr signal gated with the decoded instruction opcodes which select the BSR between TDI and TDO, instead of driving it directly from the Tap controller's update_dr signal.

Example: ---------- Suppose Tap/I[3..0] is the instruction bus, and you have the following opcode assignments in your boundary-scan design:

EXTEST Instruction(Selcting BSR between TDI and TDO) = 0000 0010 SAMPLE Instruction(Selcting BSR between TDI and TDO) = 0111 1000 CLAMP Instruction(Selcting BYPASS between TDI and TDO) = 1001 1010 HIGHZ Instruction(Selcting BSR between TDI and TDO) = 1011 1110 BYPASS Instruction(Selcting BYPASS between TDI and TDO) = 1111 & the remaining opcodes

Opcodes selecting the BSR = 0000 0010 0111 1000 1011 1110

Depending upon whether you have a synchronous or asynchronous design, you will fix this violation as follows.

Case1: If you are using a synchronous implementation then you can derive the BSR cell's capture_en signal as follows:

capture_en = (Tap Controller's sync_capture_en) & (!I3&!I2&!I1&!I0 | !I3&!I2&I1&!I0 | !I3&I2&I1&I0 | I3&!I2&!I1&!I0 | I3&!I2&I1&I0 | I3&I2&I1&!I0) (Most probably you were genrating capture_en = (Tap Controller's sync_capture_en))

Case2: If you are using a asynchronous implementation then you can derive the BSR cell's capture_clk signal as follows:

capture_clk = (Tap Controller's clock_dr) & (!I3&!I2&!I1&!I0 | !I3&!I2&I1&!I0 | !I3&I2&I1&I0 | I3&!I2&!I1&!I0 | I3&!I2&I1&I0 | I3&I2&I1&!I0) (Most probably what you were generating capture_clk = (Tap Controller's clock_dr))

TEST-860 (warning) Boundary scan register cell %s is illegally merged. Only an input function can be merged with an output or control function.

DESCRIPTION

The IEEE Std 1149.1 states in chapter 10, section 10.9, that in a case in which a system input is used solely as a source of control or solely as a source of data for a system output pin, a single cell can be provided that meets the rules of 10.5.1 for the input pin and 10.6.1 for the output pin.

WHAT NEXT

Correct the design of the boundary-scan register cell to either A. Include two separate boundary-scan cells. B. Combine both the input pin and the contol cell of the output pin into a single cell.

For more information, see the *Boundary Scan Reference Manual*.

TEST-860a (warning) Boundary scan register cell %s is illegally merged. The merged cell contains more than two functions.

DESCRIPTION

A merged cell can, at most, contain two functions. Here, the cell was found to either control more than one output ports or have more than two functions.

WHAT NEXT

You should correct the design of the boundary-scan register cell to drive only one

output port or have only at most two functions.

TEST-861 (warning) The boundary scan register cells are not able to update the update flops, when the TAP Controller changes state from Capture-DR to Update-DR through Exit-DR only. These cells do update the update flops, when the TAP Controller changes state from Capture-DR to Update-Dr through Shift-DR.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 5 that whatever may be the path to Update-DR, the update-flops should be updated by the latest values from the boundary-scan shift-register stage.

WHAT NEXT

You should correct the design of boundary-scan register cell.

TEST-862 (error) Mandatory BYPASS instruction is not implemented.

DESCRIPTION

You get this error message when **check_bsd** finds that either 1. all-ones opcode does not implement the mandatory **BYPASS** instruction or 2. the output of some boundary scan register cell is not being driven by the input pin during the **BYPASS** instruction with the specified opcode (i.e TEST-877 has occured).

The IEEE Std 1149.1 state in chapter 7 that each component shall provide a BYPASS instruction with all-ones opcode.

WHAT NEXT

Correct the design to implement the BYPASS instruction with all-ones opcode.

TEST-863 (error) Mandatory EXTEST instruction is not

implemented with all-zeros opcode.

DESCRIPTION

You get this error message when **-infer_instructions** option of the **check_bsd** command is set to false(default) and **check_bsd** finds that all-zeros opcode does not implement the mandatory EXTEST instruction .

The IEEE Std 1149.1 state in chapter 7 that each component shall provide a EXTEST instruction with all-zeros opcode.

WHAT NEXT

Correct the design to implement the EXTEST instruction with all-zeros opcode.

TEST-864 (information) This problem occurred because TDO port %s is
driven by a constant source.

DESCRIPTION

Diagnostics found a constant source driving the TDO port. If it comes through any sequential elements, those elements become non-active for shift-register inference. Hence, it becomes impossible to find the shift-register.

WHAT NEXT

Correct the design so as not to drive the TDO during shifting by a constant source.

TEST-865 (information) The TDO port %s is not enabled during the shift-DR TAP controller state.

DESCRIPTION

The IEEE Std 1149.1 states in Chapter 5 that the test data out (TDO) port must be active during Shift-DR TAP controller state to facilitate the serial shifting of data. Diagnostic can pin-point the cause.

WHAT NEXT

Correct the enabling logic of TDO. You can run the **check_bsd** in diagnostic mode to

find the real cause of the problem. Rectify the design and rerun **check_bsd**.

TEST-866 (warning) Ignoring instruction %s, as opcode(s) is not specified for the instruction.

DESCRIPTION

You get this warning message when **-infer_instructions** option of the **check_bsd** command is set to false(default) and **check_bsd** looks for the implemented instructions information provided by the **set_bsd_instruction** command, for the designs in the verification flow for which there is no implemented instructions information passed by **insert_bsd** command is found. If opcode is not specified for an instruction (besides BYPASS and EXTEST instructions, which have reserved and mandatory opcodes), the instruction will be ignored by check_bsd.

WHAT NEXT

Specifiy the opcode of the instruction by the **set_bsd_instruction** command and rerun check_bsd. If complete and accurate information about the implemented instructions is not known, turn on the **-infer_instructions** option of the **check_bsd** command and rerun check_bsd.

TEST-867 (warning) Opcode %s specified for instruction %s is not implemented because the instruction register width %d is insufficient.

DESCRIPTION

You get this warning message when you are using a custom TAP controller and the opcode you specified for an instruction is not implemented because the instruction register does not have sufficient number of bits.

WHAT NEXT

Use another opcode that fit into the instruction register or use another TAP controller with sufficient instruction register width. If you use a DW TAP then instruction register width is automatically selected to accommodate all the opcodes.

TEST-868 (warning) Opcode %s of instruction %s has a different signature that opcode %s. A new instruction will be

inferred for the opcode %s.

DESCRIPTION

When the -infer_instructions switch in the command **set_bsd_configuration** is set to the value false, then **check_bsd** does not infer the instructions of the current boundary-scan inserted design, but it looks for the implemented instructions information already stored with the design by the **insert_bsd** command during boundary-scan synthesis.

This error message appears when you have set the -infer_instructions switch in the command **set_bsd_configuration** to a value false and **check_bsd** is finds that two opcodes for the same instruction have different signatures. In such a case **check_bsd** infers a new instruction for the opcode whose signature is different.

WHAT NEXT

Insure that the functionality of the IEEE 1149.1 boundary-scan logic is enabled in the design. You may be required to use set_bsd_compliance to specify the compliance enable ports and patterns that enable the IEEE 1149.1 boundary-scan functionality for a design.

TEST-869 (error) Could not find implemented instructions information for the design.

DESCRIPTION

DB Mode When the -infer_instructions switch in the command **set_bsd_configuration** is set to the value false, then **check_bsd** does not infer the instructions of the current boundary-scan inserted design, but it looks for the implemented instructions information already stored with the design by the **insert_bsd** command during boundary-scan synthesis.

This error message appears when you have set the -infer_instructions switch in the command **set_bsd_configuration** to a value false and **check_bsd** is not able to find the implemented instructions information in the current boundary-scan inserted design.

XG Mode When the -infer_instructions switch in the command **check_bsd** is set to the value false, then **check_bsd** does not infer the instructions of the current boundary-scan inserted design, but it looks for the implemented instructions information already stored with the design by the **insert_dft** command during boundary-scan synthesis.

This error message appears when you have set the -infer_instructions switch in the command **check_bsd** to a value false and **check_bsd** is not able to find the implemented instructions information in the current boundary-scan inserted design.

WHAT NEXT

DB Mode Insure that boundary-scan synthesis has been done with a version which supports the feature of passing the implemented instructions information from **insert_bsd** to **check_bsd**. If the boundary-scan synthesis has been done with an older version, then set the -infer_instructions switch to the value true in the command **set_bsd_configuration** before invoking the **check_bsd** command.

XG Mode Insure that boundary-scan synthesis has been done with a version which supports the feature of passing the implemented instructions information from **insert_dft** to **check_bsd**. If the boundary-scan synthesis has been done with an older version, then set the -infer_instructions switch to the value true in the command **check_bsd** before invoking the **check_bsd** command.

TEST-870 (warning) Design port %s is not forced to inactive state during the instruction opcode %s.

DESCRIPTION

During the inference of the HIGHZ instruction, it was found that there are some design ports that are put into inactive state during this instruction, but there are still some design ports left that are not put into inactive state. This instruction might not be HIGHZ, but half conditioning of a design port is not proper for any instruction except for a private instruction.

WHAT NEXT

Ignore the warning if this instruction is private and the output conditioning of design ports is to be like this. Otherwise, correct the design of the instruction to have a proper output conditioning of design ports.

TEST-871 (error) Illegal capture descriptor on the bsr cell %s for the instruction opcode %s for instruction %s. The capture source is %s.

DESCRIPTION

The IEEE Std 1149.1 states in chapter 10 that the signal loaded into the shift-register stage of each cell on the rising edge of TCK in the Capture-DR controller state is listed in table 10-1 for boundary-scan register cells at system logic inputs and in table 10-4 for cells at system logic outputs. The software finds a different capture source than what is listed in the tables for that instruction. The reason can be a. The instruction is not the one it has been inferred as. b. The design of boundary-scan register cell used is not correct.

WHAT NEXT

Fix the design to capture the correct source if the instruction inferred is correct; otherwise, check the conditions that makes the instruction being inferred as public instruction.

TEST-872 (warning) Illegal Capture source descriptor for the EXTEST instruction on the input bsr cell %s. It should be primary input ports.

DESCRIPTION

The IEEE Std 1149.1 states in chapter 7 and 10 that the signal loaded into the shift-register stage of each cell on design input ports on the rising edge of TCK in the Capture-DR controller state is the following:

The signal driven to the system logic input from the external source.

WHAT NEXT

Correct the design of boundary-scan register cell on the design input.

TEST-873 (error) Illegal output conditioning during the EXTEST instruction on the output bsr cells. It should be conditioned by BSR cells.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 7 and 10 that the signal driven from the parallel output of each control-and-observe cell when EXTEST is selected should be: The latched parallel output of shift-register stage.

WHAT NEXT

You should correct the design of EXTEST or boundary-scan register cell at system output ports.

TEST-874 (warning) The logic state of design port %s is not driven by the boundary scan register BSR cell %s during the

instruction opcode %s.

DESCRIPTION

During the inference of the CLAMP instruction it was found that for this instruction opcode there are some design output ports that are driven by the boundary-scan register cell, but there exists some other design ports that are not driven by their boundary-scan register cells. This might be due to a. The instruction is not CLAMP but a private instruction. b. The design of CLAMP instruction is not proper.

WHAT NEXT

If the instruction opcode belongs to a private instruction, ignore the warning. Otherwise, correct the design of CLAMP to make signals from the boundary-scan register cells drive all the design ports.

TEST-875 (warning) The boundary scan register cell %s is not able to capture the logic state of design input port during the instruction opcode %s.

DESCRIPTION

While inferring an instruction to be SAMPLE/PRELOAD, it was found that for this instruction there exists some boundary scan cells on design input ports that capture the value at these ports. However, there are some other cells that cannot capture the value at the design input ports that they observe. This might be due to the following:

a. The instruction might not be SAMPLE/PRELOAD but a private instruction.
b. The design of SAMPLE/PRELOAD is not correct.
c. The design of boundary scan register cell is not correct.

WHAT NEXT

Ignore this warning if this is a private instruction; otherwise, correct the design of the problems. Some suggestions are to try tracing the shift_dr or the capture_clk of the BSR shift register when inferring the SAMPLE/PRELOAD instruction. Also, try tracing the connection of the input or output port to the BSR shift register.

TEST-876 (error) The output pin of the boundary scan register cell %s is not being driven by the update flop during EXTEST

instruction with opcode %s.

DESCRIPTION

The IEEE Std 1149.1 states in Chapter 7 that when EXTEST is selected, the state of all signals driven from system output pins shall be completely defined by the data held in the boundary-scan register and change only on the falling edge of TCK in the Update-DR controller state.

WHAT NEXT

You should correct the design of EXTEST in the circuit. Some suggestions are to verify that the mode signal is getting the correct value and that the data is latched on the negative edge of TCK for the update register.

TEST-877 (error) The output pin of the boundary scan register cell %s is not being driven by the input pin during the instruction %s with opcode %s.

DESCRIPTION

This message occurs with BSR cells having both PI and PO. The IEEE Std 1149.1 states in Chapter 7 that when SAMPLE/PRELOAD, BYPASS, IDCODE, and USERCODE is selected, the operation of test logic has no affect on the operation of the on-chip system logic or on the flow of signals between the system pins and the on-chip system logic. This shows that either the design of the boundary scan register cell doesn’t allow the primary input to drive the primary output or the design of the instruction with this opcode is not correct.

WHAT NEXT

Correct the design for the problem outlined. A sugesstion is to review the BSR design to verify it functions properly.

TEST-878 (warning) The capture value of the boundary scan register cell %s is not from the input pin %s during instruction with opcode %s.

DESCRIPTION

The IEEE Std 1149.1 state in Chapter 7 and 10 that the signal loaded into the shift-

register stage of each cell on design input ports on the rising edge of TCK in the Capture-DR controller state is the signal driven to the system logic input from the external source.

WHAT NEXT

You should correct the design of boundary-scan register cell on the design input ports to capture the correct input value.

TEST-879 (error) Not able to locate a parallel output for the input boundary scan register cell %s.

DESCRIPTION

It was not possible to find the primary input to an input boundary-scan cell and hence will not be able to process any further. Diagnostic should be able to outline the cause of this problem.

WHAT NEXT

You should run with diagnostics on. Correct the cause of the problem before rerunning check_bsd.

TEST-880 (warning) A shift register of length %s has been selected for the BYPASS instruction with "all-ones" instruction opcode. The register should be of length one.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 7 that a binary code for the BYPASS instruction shall be {111...1} (i.e., a logic 1 entered into every instruction register cell). Here the "all-ones" instruction opcode doesn’t select a single bit BYPASS register or BYPASS register contains more than one cell.

WHAT NEXT

You should either correct the all-ones instruction to map to BYPASS instruction or correct the BYPASS register design to make it single stage.

TEST-881 (error) Illegal capture value of BYPASS register.

DESCRIPTION

The IEEE Std 1149.1 state in Chapter 9 that the shift-register stage of BYPASS register shall be set to a logic zero on the rising edge of TCK following entry into the Capture-DR controller state.

WHAT NEXT

You should correct the design of the BYPASS register to capture logic zero on the rising edge of TCK.

TEST-882 (warning) Illegal number of capture descriptors for the boundary scan register cell %s.

DESCRIPTION

In order to assign a type to boundary-scan register cell between BC_0 to BC_7, the capture descriptor for each cell under the instructions EXTEST, INTEST, and SAMPLE/PRELOAD is captured. For this cell the number of such capture descriptor is less than the required. This shows a problem in analyzing the mandatory instructions of EXTEST and SAMPLE/PRELOAD.

WHAT NEXT

Check the descriptor of the BSR as suggested by the IEEE Std 1149.1 when implementing the EXTEST and SAMPLE/PRELOAD instruction. All BSR cells with illegal capture descriptors default to BC_0.

EXAMPLE In the following example, the cell is used as an input cell while EXTEST is in effect, and the capture flip-flop loads the parallel input data at the capture_dr state.

NOTE: INTEST is not supported for BC_2 cells on output2, because it will result in an illegal descriptor BSR.

TEST-883 (warning) The TAP controller makes an illegal state transition from state %s to state %s with test clock TCK at the

low halt state.

DESCRIPTION

The TAP controller transition has taken place at TCK low halt state. It is mandatory by the standard to provide at least the TCK low halt state.

WHAT NEXT

You should correct the TCK halt state if it has one or introduce at least the LOW halt state.

TEST-884 (error) Illegal change in the TAP Controller state %s to state %s at TCK high halt state.

DESCRIPTION

The TAP controller transition has taken place at TCK high halt state. Hence the TCK will have only the LOW halt state if implemented.

WHAT NEXT

You should correct the TCK halt state if it has none, to introduce at least the LOW halt state.

TEST-885 (error) Illegal test clock TCK halt state.

DESCRIPTION

As defined in chapter 3 of IEEE Std 1149.1, the dedicated TCK input is provided to permits shifting of test data concurrently with system operation of the component. This require TCK to be stopped for a period to do other support functions during test, e.g. an ATE needs to fetch test data from backup memory. Hence the standard requires that TCK can be stopped at 0 indefinitely without causing any change to state of test logic. Hence while TCK is stopped at 0, state devices are required to retain their state so that the test logic may continue its operation when the clock operation restarts. The tool was able to find the TAP Controller state devices are not able to retain their state, when TCK is stopped at 0.

WHAT NEXT

You should rectify this problem by making the state devices of TAP Controller to retain their state, when TCK is stopped at 0.

TEST-886 (warning) The parallel output of the boundary scan register cell %s is not driven by the update flop using opcode %s, which is the INTEST instruction.

DESCRIPTION

The IEEE Std 1149.1 states in chapter 7 and 10 that the signal driven from the parallel output of each control-and-observe cell while INTEST is selected is either a. The latched parallel output of shift-register stage b. The value that disables connected output.

As in these cases many output boundary-scan register cells have been found to be driven by latched parallel output of their shift-register stage. There seems to be design problems with INTEST implementation on the cell in question.

WHAT NEXT

You should correct the design of INTEST instruction to route the boundary-scan register cell properly.

TEST-887 (warning) The parallel output of a clock boundary scan register cell %s is not driven according to rule 10.5.1g during %s with opcode %s.

DESCRIPTION

The IEEE Std 1149.1 states in chapter 10 that for clock inputs, when the INTEST instruction is selected, the signal driven to the on-chip system logic shall be one of the following: 1. The signal received at the connected system pin 2. The TCK signal, controlled such that the on-chip system logic changes state only in the Run-Test/idle controller state 3. The parallel output of the shift-register stage

WHAT NEXT

Correct the INTEST routing for the boundary-scan register cell on the clock system pins.

TEST-888 (error) The parallel output of an input boundary scan register cell %s is not driven by the parallel input with opcode

%s, which is the SAMPLE instruction.

DESCRIPTION

The IEEE Std 1149.1 state in chapter 7 and 10 that when the SAMPLE/PRELOAD instruction is selected, the states of all signals flowing through system pins shall be loaded into the boundary-scan register on the rising edge of TCK in the Capture-DR controller state.

WHAT NEXT

You should correct the routing of the BSR cell during SAMPLE/PRELOAD instruction.

TEST-889 (warning) Boundary scan register cell %s is not standard(BC_0 to BC_7). This will be defaulted to BC_0 in the output BSDL.

DESCRIPTION

In order to associate a cell type from BC_0 to BC_7, the BSR cells on system inputs and outputs are analyzed under the influence of EXTEST, SAMPLE/PRELOAD, and INTEST (if implemented) to find the captured source. The BSR cells are structurally analyzed to find other characteristics. Based on the information gathered, the BSR cell is assigned the type BC_0 to BC_7. The BSR cell in question was found to have characteristics that are different either in functional respect or structural from the standard BSR cell type BC_0 to BC_7.

WHAT NEXT

Check the analysis of the instructions EXTEST, SAMPLE/PRELOAD, and INTEST to know more about functional problems, if problems exist.

TEST-890 (warning) Not able to locate the parallel input for the boundary scan register cell %s.

DESCRIPTION

In order to analyze the instructions in detail and to analyze the characteristics of boundary scan register (BSR) cell, the Primary Input (PIs) and Primary Output (POs) of the cells are inferred. The reason for not finding a PI of observable and controllable BSR cell can be as follows:

a. BSR cell is not compliant to the IEEE 1149.1, the reason being the PI is not driving the set of POs during SAMPLE/PRELOAD instruction.
b. The PI is not being captured into the shift_flop properly.

WHAT NEXT

Correct the BSR cell implementation if you want to check further compliance. The BSDL output cannot be generated.

TEST-891 (error) Not able to locate the parallel output for the %s boundary scan register cell %s.

DESCRIPTION

In order to analyze the instructions in detail and to analyze the characteristics of boundary scan register (BSR) cell, the Primary Inputs (PI) and Primary Outputs (PO) of the cells are inferred. The reason for not finding a PO of observable and controllable BSR cell can be because of the following:

BSR cell is not compliant to the IEEE 1149.1, the reason being the PO is not driven by the PI during SAMPLE/PRELOAD instruction.

WHAT NEXT

Correct the BSR cell implementation if you want to check further compliance. The BSDL output cannot be generated.

TEST-892 (error) Not able to locate the parallel output for the control boundary scan register cell %s.

DESCRIPTION

In order to analyze the instructions in detail and to analyze the characteristics of BSR cell, the PIs (Primary Input) and POs (Primary Output) of the cells are inferred. The reason for not finding a PO of observable and controllable BSR cell can be as follows: a. BSR cell is not compliant to the IEEE 1149.1, the reason being the PO is not driven by the PI during SAMPLE/PRELOAD instruction.

WHAT NEXT

You need to correct the BSR cell implementation if you want to check further compliance. The BSDL output cannot be generated.

TEST-893 (error) Not able to locate the parallel input for the CONTROL boundary scan register cell %s.

DESCRIPTION

In order to analyze the instructions in detail and to analyze the characteristics of BSR cell, the PIs (Primary Input) and POs (Primary Output) of the cells are inferred. The reason for not finding a PI of any BSR cell can be as follows: a. BSR cell is not compliant to the IEEE 1149.1, the reason being either the PI is not captured by the BSR cell shift-register stage or the PO is not driven by the PI during SAMPLE/PRELOAD instruction.

WHAT NEXT

You need to correct the BSR cell implementation if you want to check further compliance. The BSDL output cannot be generated.

TEST-894 (error) Not able to locate the parallel input for the OUTPUT boundary scan register cell %s.

DESCRIPTION

In order to analyze the instructions in detail and to analyze the characteristics of BSR cell, the PIs (Primary Input) and POs (Primary Output) of the cells are inferred. The reason for not finding a PI of any BSR cell can be as follows: a. BSR cell is not compliant to the IEEE 1149.1, the reason being either the PI is not captured by the BSR cell shift-register stage or the PO is not driven by the PI during SAMPLE/PRELOAD instruction.

WHAT NEXT

You need to correct the BSR cell implementation if you want to check further compliance. The BSDL output cannot be generated.

TEST-895 (error) Not able to locate the parallel output for the input boundary scan register cell %s.

DESCRIPTION

In order to analyze the instructions in detail and to analyze the characteristics of BSR cell, the PIs (Primary Input) and POs (Primary Output) of the cells are inferred. The reason for not finding a PO of observable and controllable BSR cell

can be as follows: a. BSR cell is not compliant to the IEEE 1149.1, the reason being the PO is not driven by the PI during SAMPLE/PRELOAD instruction.

WHAT NEXT

You need to correct the BSR cell implementation if you want to check further compliance. The BSDL output cannot be generated.

TEST-896 (error) Mandatory SAMPLE instruction is not implemented (or not specified).

DESCRIPTION

You get this error message during **check_bsd** when the mandatory SAMPLE instruction is not found to be implemented in the design. The IEEE Std 1149.1(2001) states in chapter 8 that each component shall provide a SAMPLE instruction. The SAMPLE instruction is inferred by analyzing the capturing of input ports by the boundary-scan register cells on the design input ports.

WHAT NEXT

Case I: If you are running **check_bsd** on a design for which boundary-scan synthesis is not done by BSD compiler then make sure that you specify correct opcode(s) for the implemented SAMPLE instruction and make sure that the design implements the SAMPLE instruction correctly. Example: set_bsd_insruction SAMPLE -code {101}

CaseII: If you do not know the SAMPLE instruction opcode(s), set the **-infer_instructions** option of the **set_bsd_configuration** command to true and rerun **check_bsd**. This will let **check_bsd** examine all opcodes for SAMPLE. Example: set_bsd_configuration -infer_instructions true

CaseIII: If you are not upgraded to the 2001 revision of the IEEE1149.1 standard, and still following the 1993 version, you can switch back to the older version (non default mode) using the set_bsd_configuration command and rerun check_bsd. In this mode check_bsd looks for the merged SAMPLE/PRELOAD instruction instead of separate SAMPLE and PRELOAD instructions. Example: set_bsd_configuration -ieee1149.1_1993

SEE ALSO

set_bsd_instruction set_bsd_configuration check_bsd

TEST-897 (error) Mandatory PRELOAD instruction is not

implemented (or not specified).

DESCRIPTION

You get this error message during **check_bsd** when the mandatory PRELOAD instruction is not found to be implemented in the design. The IEEE Std 1149.1(2001) states in chapter 8 that each component shall provide a PRELOAD instruction. The PRELOAD instruction is inferred by analyzing the update beahvior of the boundary-scan register. The output update flops should load the data held in the associated shift register cells on the fallicng edge of TCK in the UPDATE-DR state.

WHAT NEXT

Case I: If you are running **check_bsd** on a design for which boundary-scan synthesis is not done by BSD compiler then make sure that you specify correct opcode(s) for the implemented PRELOAD instruction and make sure that the design implements the PRELOAD instruction correctly.

Example: set_bsd_insruction PRELOAD -code {101}

CaseII: DB Mode If you are running **check_bsd** on a design for which boundary-scan synthesis is not done by BSD compiler and you do not know the PRELOAD instruction opcode(s), set the **-infer_instructions** option of the **set_bsd_configuration** command to true and rerun **check_bsd**. This will let **check_bsd** examine all opcodes for PRELOAD.

XG Mode If you are running **check_bsd** on a design for which boundary-scan synthesis is not done by BSD compiler and you do not know the PRELOAD instruction opcode(s), set the **-infer_instructions** option of the **check_bsd** command to true and rerun **check_bsd**. This will let **check_bsd** examine all opcodes for PRELOAD.

CaseIII: If you are not upgraded to the 2001 revision of the IEEE1149.1 standard, and still following the 1993 version, you can switch back to the older version (non default mode) using the set_bsd_configuration command and rerun check_bsd. In this mode check_bsd looks for the merged SAMPLE/PRELOAD instruction instead of separate SAMPLE and PRELOAD instructions.

Example: set_bsd_configuration -ieee1149.1_1993

SEE ALSO

set_bsd_instruction set_bsd_configuration check_bsd

TEST-898 (error) The boundary scan register cell %s is not a

valid cell type.

DESCRIPTION

The BSR cell's primary type as per IEEE Std 1149.1b-1994, can be one of the following only: a. INPUT b. OUTPUT2 c. CLOCK d. OUTPUT3 e. CONTROL f. CONTROLR g. INTERNAL h. BIDIR i. OBSERVE_ONLY

WHAT NEXT

You need to correct the design and functionality of the BSR cells to proceed further.

TEST-899 (Information) Scan routing is not complete. Signals '%s' need to be routed.

DESCRIPTION

The scan is not complete because some route signals have been not routed yet.

WHAT NEXT

Set the signals to be routed by **set_scan_configuration**, and run **insert_scanFP again.**

SEE ALSO

set_scan_configuration and insert_scan

TEST-900 (information) This problem occurred because tristate output (or output side of bidirectional) port %s is disabled and is driven to high impedance value.

DESCRIPTION

This may happen when the the enable pin of the pad is tied to a constant value and is constantly driving the tristate output (or output side of bidirectional) port to HIGHZ value. This might be the case when a bidirectional port is intended to be used as reduced input port.

WHAT NEXT

Check if you that you intend to disable the tristate output (or output side of bidirectional) port, else check the connection(s) of the enable pin(s) of the port pad.

TEST-900a (information) This problem occurred because tristate output (or output side of bidirectional) port %s is enabled and is reduced to a two state port.

DESCRIPTION

This may happen when the the enable pin of the pad is tied to a constant value and is constantly enabling the tristate output (or output side of bidirectional) port to HIGHZ value. This might be the case when a bidirectional port is intended to be used as reduced output port or a tristate output port is intended to be used as a two-state port.

WHAT NEXT

Check if you that you intend to enable the tristate output (or output side of bidirectional) port, else check the connection(s) of the enable pin(s) of the port pad.

TEST-901 (information) This problem occurred because design input
port %s controls the logic.

DESCRIPTION

A design input port was found to be controlling the logic during diagnostic.

WHAT NEXT

Either correct the logic or set the design port as a compliance enable port with a relevant value.

TEST-902 (information) This problem occurred because %s has an unknown value ’X’ due to being driven by multiple drivers:

%s.

DESCRIPTION

A multiple driver net was found. This might be due to unresolved reference making the input port as I/O.

WHAT NEXT

Resolve all the references or correct the design.

TEST-903 (information) This problem occurred because %s has an unknown value ’X’, due to black box cell %s driving it.

DESCRIPTION

A design cell was found to be black boxed (reference not found) during diagnostic. All pins of a black-boxed cell are considered to be bidirectional pins. This in turn results in an unknown value at a pin actually intended to be driving a pin of the black-boxed cell.

WHAT NEXT

Either correct the logic or set the design cell reference properly.

TEST-904 (information) This problem occurred because pin %s of
the cell %s is driven by a constant source.

DESCRIPTION

A design pin of a cell was found to be driven by a constant source.

WHAT NEXT

Correct the logic.

TEST-905 (information) This problem occurred because %s has

an unknown value ’X’, due to pin %s being in a high impedance state.

DESCRIPTION

A design cell input pin of was found to be in an inactive drive state value, causing an unknown value at another design pin.

WHAT NEXT

Correct the logic.

TEST-906 (information) This problem occurred because cell %s has multiple inputs with indexed scan tokens.

DESCRIPTION

A design cell is found with multiple indexed scan token which has resulted in ’x’ on its output.

WHAT NEXT

Correct the logic.

TEST-907 (information) This problem occurred because x-bdd of pin %s of cell %s is one.

DESCRIPTION

A design cell was found with x-bdd of its pin as one.

WHAT NEXT

Correct the logic.

TEST-908 (information) This problem occurred because the asynchronous input to cell %s is unknown.

DESCRIPTION

A design cell was found with an unknown asynchronous input.

WHAT NEXT

Correct the logic.

TEST-909 (information) Because the clock input to cell %s is unknown.

DESCRIPTION

A design cell is found with unknown clock input.

WHAT NEXT

Correct the logic.

TEST-910 (information) This problem occurred because the TMS port is controlled by design input port %s.

DESCRIPTION

A design input port was found to be controlling the TMS port logic during diagnostic.

WHAT NEXT

Either correct the logic or set the design port as a compliance enable port with a relevant value.

TEST-911 (information) This problem occurred because TRST port
is controlled by design input port %s.

DESCRIPTION

A design input port was found to be controlling the logic on the TRST TAP port during diagnostic.

WHAT NEXT

Either correct the logic or set the design port as a compliance enable port with a relevant value.

TEST-912 (information) This problem occurred because TCK port is
controlled by design input port %s.

DESCRIPTION

A design input port was found to be controlling the logic on the TCK TAP port during diagnostic.

WHAT NEXT

Either correct the logic or set the design port as a compliance enable port with a relevant value.

TEST-913 (information) The sequential cell %s is driven by constant source.

DESCRIPTION

A sequential cell is found to be driven by a constant source during diagnostic.

WHAT NEXT

Correct the logic.

TEST-914 (information) This problem occurred because %s has an unknown value ’X’, due to pin %s left unconnected.

DESCRIPTION

A design cell input pin of was found unconnected, causing an unknown value at another design pin.

WHAT NEXT

Correct the logic.

TEST-915 (information) This problem occurred because pin %s on
the cell %s has controlling value.

DESCRIPTION

A cell was found with controlling input forced on the pin, and hence, the signal from PI cannot be captured.

WHAT NEXT

Correct the logic.

TEST-916 (information) This problem occurred because port %s is unconnected.

DESCRIPTION

A port was found unconnected.

WHAT NEXT

Correct the logic.

TEST-917 (information) This problem occurred because the

tristate pin %s on
the cell %s has multiple controlling cells.

DESCRIPTION

A pad cell was found with controlling input being driven by multiple BSR cell, which is a violation of rule 10.6.1c.

WHAT NEXT

Correct the logic.

TEST-918 (information) This problem occurred because the pin %s on
the cell %s is driven by multiple BSR cells.

DESCRIPTION

A cell was found with multiple input being driven by BSR cells.

WHAT NEXT

Correct the logic.

TEST-920 (Error) No pad type found for the pad design %s.

DESCRIPTION

You did not specify a pad type with the **set_bsd_pad_design -pad_type** command. As a result, when you execute the **insert_bsd** or the **preview_bsd** command, you receive this error message in DB mode.

You did not specify a pad type with the **define_dft_design -param { pad_type** command. As a result, when you execute the **insert_dft** or the **preview_dft** command, you receive this error message in XG mode.

WHAT NEXT

Reexecute the **set_bsd_pad_design** command with the **-pad_type** option, and specify a valid pad type. Then, rerun the **insert_bsd** or **preview_bsd** command in DB mode.

Reexecute the **define_dft_design** command with the **-param {pad_type** option, and specify a valid pad type. Then, rerun the **insert_dft** or **preview_dft** command in XG mode.

SEE ALSO

insert_bsd (2), **insert_dft** (2), **preview_bsd** (2), **preview_dft** (2), **set_bsd_pad_design** (2), **define_dft_design** (2).

TEST-921 (Error) Data output pin not found in the input pad design %s.

DESCRIPTION

DB Mode You receive this error message because you have not specified a data_out or data_out_inverted signal type pin in the access list for the **set_bsd_pad_design** command, or the specified pin does not exist in the pad design. For the input pad type data_out or data_out_inverted, a pin is expected. This message is generated by the **preview_bsd** command and the **insert_bsd** command.

XG Mode You receive this error message because you have not specified a data_out signal type pin in the access list for the **define_dft_design** command, or the specified pin does not exist in the pad design. For the input pad type data_out pin is expected. This message is generated by the **preview_dft** command and the **insert_dft** command.

WHAT NEXT

Provide a valid pad design pin name for the data_out or data_out_inverted signal type in the access list of the **set_bsd_pad_design** command, and rerun the **insert_bsd** or **preview_bsd** command in DB mode.

Provide a valid pad design pin name for the data_out signal type in the interface list of the **define_dft_design** command, and rerun the **insert_dft** or **preview_dft** command in XG mode.

SEE ALSO

insert_bsd (2), **insert_dft** (2), **preview_bsd** (2), **preview_dft** (2), **set_bsd_pad_design** (2), **define_dft_design** (2).

TEST-922 (Error) Data input pin not found in the output pad

design %s.

DESCRIPTION

DB Mode You receive this error message because you have not specified a data_in or a data_in_inverted signal type pin in the access list of the **set_bsd_pad_design** command, or the specified pin does not exist in the pad design. For an output pad type, a data_in or data_in_inverted output pin is expected. This message is generated by the **preview_bsd** or **insert_bsd** command.

XG Mode You receive this error message because you have not specified a data_in signal type pin in the access list of the **define_dft_design** command, or the specified pin does not exist in the pad design. For an output pad type, a data_in pin is expected. This message is generated by the **preview_dft** or **insert_dft** command.

WHAT NEXT

Specify a valid pad design pin name for the data_in or data_in_inverted signal type in the access list of **set_bsd_pad_design** command, and rerun the **insert_bsd** or **preview_bsd** command in DB mode.

Specify a valid pad design pin name for the data_in signal type in the interface list of **define_dft_design** command, and rerun the **insert_dft** or **preview_dft** command in XG mode.

SEE ALSO

insert_bsd (2), **insert_dft** (2), **preview_bsd** (2), **preview_dft** (2), **set_bsd_pad_design** (2), **define_dft_design** (2).

TEST-923 (Error) Enable pin not found in the tristate output or open drain pad design %s.

DESCRIPTION

DB Mode You receive this error message because you have not specified an enable or enable_inverted signal type pin in the access list of the **set_bsd_pad_design** command. For pad types of tristate_output, open_drain_output or open_drain_bidirectional, an enable or enable_inverted signal type pin is expected. This message tells you that you have either not specified an enable or enable_inverted signal type pin in the access list with the **set_bsd_pad_design** command, or the specified pin does not exist in the pad design. This message is generated by the **preview_bsd** or **insert_bsd** command.

XG Mode You receive this error message because you have not specified an enable signal type pin in the interface list of the **define_dft_design** command. For pad types of tristate_output, open_drain_output or open_drain_bidirectional, an enable

signal type pin is expected. This message tells you that you have either not specified an enable signal type pin in the interface list with the **define_dft_design** command, or the specified pin does not exist in the pad design. This message is generated by the **preview_dft** or **insert_dft** command.

WHAT NEXT

DB Mode Specify valid pad design pin name for the enable or enable_inverted signal type in the access list of the **set_bsd_pad_design** command and rerun the **insert_bsd** or **preview_bsd** command.

XG Mode Specify valid pad design pin name for the enable signal type in the interface list of the **define_dft_design** command and rerun the **insert_dft** or **preview_dft** command.

SEE ALSO

insert_bsd (2), **insert_dft** (2), **preview_bsd** (2), **preview_dft** (2), **set_bsd_pad_design** (2), **define_dft_design** (2).

TEST-924 (Error) Cannot generate protocol for unimplemented instruction "%s".

DESCRIPTION

DB Mode You receive this error message during the **write_bsd_protocol** command, when you ask the protocol to be generated for an instruction which is not implemented. STIL protocol can be generated only for instructions which are implemented by the **insert_bsd** command.

For instance, suppose that you specified the HIGHZ instruction, which could not be implemented the **insert_bsd** command (due to the reason that not all the port-pads are tristate - you will get TEST-943 warning during **preview_bsd** and **insert_bsd**). If you try to generate bsd protocol after **insert_bsd** for HIGHZ instruction, you will get the current error message.

XG Mode You receive this error message during the **write_bsd_protocol** command, when you ask the protocol to be generated for an instruction which is not implemented. STIL protocol can be generated only for instructions which are implemented by the **insert_dft** command.

For instance, suppose that you specified the HIGHZ instruction, which could not be implemented the **insert_dft** command (due to the reason that not all the port-pads are tristate - you will get TEST-943 warning during **preview_dft** and **insert_dft**). If you try to generate bsd protocol after **insert_dft** for HIGHZ instruction, you will get the current error message.

WHAT NEXT

Specify a correct instruction name to generate the protocol for and rerun the command. Look at the **preview_bsd** report in DB mode for a list of the implemented instructions.

Specify a correct instruction name to generate the protocol for and rerun the command. Look at the **preview_dft** report in XG mode for a list of the implemented instructions.

SEE ALSO

insert_bsd (2), **insert_dft** (2), **preview_bsd** (2), **preview_dft** (2), **write_bsd_protocol** (2), **set_bsd_instruction**

TEST-925 (Error) Differential pad design %s is not connected to two ports of the same type.

DESCRIPTION

You receive this error message because you have executed the **insert_bsd** or the **preview_bsd** command and specified a pad design that is not connected to two ports of the same type.

WHAT NEXT

Modify the design so that the differential pad design is connected to two ports of the same type and reexecute the **insert_bsd** or **preview_bsd** command.

SEE ALSO

insert_bsd (2), **preview_bsd** (2).

TEST-926 (Warning) Ignoring the unnecessary signal type pin(s) specified for the pad design %s.

DESCRIPTION

DB Mode You received this warning message because some of the signal type pins specified in the access list of the **set_bsd_pad_design** command are not required for the pad type you specified and will be ignored.

XG Mode You received this warning message because some of the signal type pins specified in the access list of the **define_dft_design** command are not required for

the pad type you specified and will be ignored.

WHAT NEXT

Because the extra pins specified are not used in BSD synthesis, no action is required on your part.

SEE ALSO

set_bsd_pad_design (2). **define_dft_design** (2).

TEST-927 (Error) Internal development error related to the pad design %s.

DESCRIPTION

You receive this error message because an internal error occurred while performing BSD synthesis in the presence of pad designs.

WHAT NEXT

For more information, contact Synopsys.

TEST-928 (Warning) Output disable result value not specified for the tristate pad design %s.

DESCRIPTION

DB Mode You receive this warning message because you have not specified a value for the **-disable_res** option of the **set_bsd_pad_design** command. This message is generated by the **insert_bsd** or **preview_bsd** command.

XG Mode You receive this warning message because you have not specified a value for the **-param {$disable_res$** option of the **define_dft_design** command. This message is generated by the **insert_dft** or **preview_dft** command.

WHAT NEXT

Specify a valid disable result value for the **-disable_res** option with the **set_bsd_pad_design** command and reexecute the **insert_bsd** or **preview_bsd** command in DB mode.

Specify a valid disable result value for the **-param {$disable_res$** option with the

define_dft_design command and reexecute the **insert_dft** or **preview_dft** command in XG mode.

SEE ALSO

insert_bsd (2), **insert_dft** (2), **preview_bsd** (2), **preview_dft** (2), **set_bsd_pad_design** (2), **define_dft_design** (2).

TEST-929 (Warning) Enable pin not found or not specified for the bidirectional pad design %s. The pad design will be treated as an open drain bidirectional pad.

DESCRIPTION

DB Mode You receive this warning message because you have not specified an enable or an enable_inverted signal type in the access list of the **set_bsd_pad_design** command, or the specified pin is not found. The pad design will be treated as an open drain bidirectional pad.

XG Mode You receive this warning message because you have not specified an enable signal type in the access list of the **define_dft_design** command, or the specified pin is not found. The pad design will be treated as an open drain bidirectional pad.

WHAT NEXT

If the specified bidirectional pad design is used in BSD synthesis, specify the enable pin for correct BSD synthesis. The synthesized BSD design might not be correct if the enable pin is not specified.

SEE ALSO

set_bsd_pad_design (2), **define_dft_design** (2).

TEST-930 (Error) NO Pad cell have been found on the design port %s.

DESCRIPTION

There is no PAD cell present on the design port. It is a neccesary condition to have Pad cells on the design.

WHAT NEXT

Correct the design or give the top level design and not the core. You may also use the set_bsd_linkage_port command to exclude the port from boundary-scan logic insertion.

TEST-931 (Error) Multiple Pad cells have been found on the design port %s.

DESCRIPTION

More than the required Pad cells have been found on the design port.

WHAT NEXT

Correct the design.

TEST-931b (warning) Shift Register Flop '%s' captures data on negative edge of TCK.

DESCRIPTION

Rule 9.3.1b of IEEE Std. 1149.1-2001 states that Test Data Register connected between TDI and TDO shall shift data one stage towards TDO following each rising edge of TCK in Shift-Dr state.

This warning is issued by the tool when it detects a shift register flop of the Test Data Register that shifts data on negative edge of TCK.

WHAT NEXT

Rectify the logic at the cell of the shift register to be in full compliance with the Std.

TEST-932 (Error) Pad cell %s attached to design port %s is a black box.

DESCRIPTION

The attached Pad cell to the design port is not modelled correctly.

WHAT NEXT

Check the library model for the PAD cell and correct it.

TEST-932b (warning) Pad design %s has black box attributes.

DESCRIPTION

The attached pad design is not modelled correctly. Pad design is observed to have black box attributes. TAP ports should not be connected to black box pad designs, otherwise check_bsd will fail.

WHAT NEXT

Check the library model for the PAD cell and correct it.

TEST-933 (Error) The Bi-directional Pad cell %s attached to design port %s has no core logic output pin.

DESCRIPTION

The attached Bi-directional Pad cell to the design port is not modelled correctly. The pad cell doesnot have any core logic output pin.

WHAT NEXT

Check the library model for the PAD cell and correct it.

TEST-934 (Error) The Input Pad cell %s attached to design port %s has no core logic output pin.

DESCRIPTION

The attached Input Pad cell to the design port is not modelled correctly. The pad cell doesnot have any core logic output pin.

WHAT NEXT

Check the library model for the PAD cell and correct it.

TEST-935 (Error) The 3-State Output Pad cell %s attached to design port %s has no core logic input pin.

DESCRIPTION

The attached Output Pad cell to the design port is not modelled correctly. The pad cell doesnot have any core logic input pin.

WHAT NEXT

Check the library model for the PAD cell and correct it.

TEST-936 (Error) The 2-State Output Pad cell %s attached to design port %s has no core logic input pin.

DESCRIPTION

The attached Output Pad cell to the design port is not modelled correctly. The pad cell doesnot have any core logic input pin.

WHAT NEXT

Check the library model for the PAD cell and correct it.

TEST-937 (Error) The 3-State Output Pad cell %s attached to design port %s has no enable pin.

DESCRIPTION

The attached 3-State Pad cell to the design port is not modelled correctly. The pad cell doesnot have any 3-state enable pin.

WHAT NEXT

Check the library model for the PAD cell and correct it.

TEST-938 (warning) Design ’%s’ must be scan-replaced or

scan-routed.

DESCRIPTION

This message tells you that your design must be either scan-replaced or scan-routed before you invoke one of the 'reoptimize_design -reorder_scan_chains' or the 'preview_scan -command reoptimize_design' commands.

WHAT NEXT

At least get sequential cells replaced by scan cells from your technology library or simply run **insert_scan** command on your design in either replace-only or replace_and_route mode.

TEST-939 (information) Scan chain reordering was not successful. There were unrecoverable processing errors.

DESCRIPTION

This message tells you that DFT Compiler could not recover from processing errors that occurred during scan chain reordering. Scan chain reordering has exited, without modifying your design.

WHAT NEXT

Study accompanying error messages and fix the problems reported.

TEST-940 (information) Cumulated distance before and after scan reordering
could not be computed because XY information for scan cells is partial or unexistent.

DESCRIPTION

This information messages tells you that the XY information for scan cells is partial or unexistent. You get this message when you are using PDEF 1.0 which does not support XY coordinates for cells and clusters. In this case, XY information is unexistent. You may also get this message while working with PDEF 2.0 early in the optimization process. At that level, the physical information coming from a floorplanner may be incomplete as the placement of some cells can be still fluid.

WHAT NEXT

If you are working with PDEF 2.0, you can wait till the XY coordinates for scan cells become available before invoking scan chain reordering.

TEST-941 (information) Scan chain is user specified with '-complete true'.
The initial ordering of segments is not disturbed.

DESCRIPTION

This information message tells you that scan chain reordering does not modify scan segment positions when those positions are specified by the designer through the **set_scan_path** command with '-complete' option set to 'true'. The only case in which user specification is modified by scan chain reordering is when it violates clock domain constraint.

WHAT NEXT

If you want your scan chain to get reordered you need to change your scan path specification before invoking scan chain reordering.

TEST-942 (information) Scan chain is user specified with '-complete false'
or split/reordered to meet clock domain constraints.
The reordering is done respecting user-segment positions.

DESCRIPTION

Scan chain reordering does not modify user-specified scan segment positions unless the specification violates clock domain constraints. This information message is issued when you are in this case or simply when your specification is incomplete (use of the **set_scan_path** command with '-complete' option set to 'false').

WHAT NEXT

If you don't want your scan chain to get disturbed you need to change your scan path specification before invoking scan chain reordering.

TEST-943 (Warning) HIGHZ instruction cannot be implemented

as the following design output port(s) are not driven by 3-state pad pin: %s. Removing the HIGHZ specification.

DESCRIPTION

A necessary requirement to implement the HIGHZ instruction is that all the output ports should have 3-state pads and the pad pin driving the design port should also be a s-state pin. Because HIGHZ is specified and not all the output design ports have three-state pads in order to synthesize logic for the HIGHZ instruction, the specification will be removed.

WHAT NEXT

Check the design and insert three-state pads on all the output ports causing the problem. Make sure that the pad pins driving all the output ports are also 3-state.

TEST-944 (Warning) The IDCODE instruction has been specified, but an appropriate environment variable has not been set to specify a valid, nonzero manufacturer identity.

DESCRIPTION

You receive this message because you have specified the IDCODE instruction but have not assigned a valid value to the **test_bsd_manufacturer_id** environment variable. To synthesize a Device Identification register, BSD Compiler requires a valid, nonzero value for this parameter. By default, this variable is set to 0.

WHAT NEXT

Do the following:

1. Assign an appropriate integer value to the **test_bsd_manufacturer_id** environment variable.

2. Execute the **set_bsd_instruction** command again.

SEE ALSO

insert_bsd (2), **preview_bsd** (2), **set_bsd_instruction(2), test_bsd_manufacturer_id** (3), **test_bsd_part_number** (3), **test_bsd_version_number** (3).

TEST-945 (Warning) Illegal value for manufacturer_id. It can not be 00001111111 (127 decimal).

DESCRIPTION

The IEEE Std 1149.1 state in chapter 11 that the manufacturer code 00001111111 shall not be used in components that are otherwise compatible with this standard.

WHAT NEXT

You can assign another id and rerun the command.

TEST-946 (Warning) Overflow in the value asigned to manufacturer_id, part_number or version_number.

DESCRIPTION

The IEEE Std 1149.1 states in chapter 11 that the manufacturer code should have the following fields with specific width: Version 4bits Part Number 16 bits Manufacturer Id 11 bits 1 in LSB

There seems to be overflow in the values assigned to the aforementioned fields.

WHAT NEXT

Reassign values to these fields and re-run the command.

TEST-947 (Error) Boundary-Scan has already been inserted using ’insert_bsd’ command..

DESCRIPTION

The **insert_bsd** can be invoked only once. If the Boundary-Scan circuitry is already synthesized, it can be re-synthesized but it can be optimized using **optimized_bsd**.

WHAT NEXT

Run **optimize_bsd** if you want to optimize the synthesized boundary scan.

TEST-948 (error) LSI 4-pattern STIL protocol could not be generated because no primary input bidirectional control signal has been specified.

DESCRIPTION

This design contains at least one bidirectional signal, but it contains no primary input signal for controlling the direction of the bidirectional signals. LSI scan rules require such signals. The error is specific to writing LSI STIL protocol file.

WHAT NEXT

Before invoking the **check_test** command, use the **set_signal_type**, **test_bidir_control**, or **test_bidir_control_inverted** command to define all primary inputs controlling bidirectional signals. Then, reinvoke the **check_test** command in order to generate the LSI 4-pattern STIL protocol file.

TEST-949 (Error) Protocol could not be generated as the design is not boundary-scan inserted.

DESCRIPTION

You get this error when "write_bsd_protocol" is used is generate protocol on a design which does not have boundary-scan circuitry inserted by the "insert_bsd" command.

WHAT NEXT

Insert boundary-scan circuitry using the "insert_bsd" command and rerun "write_bsd_protocool".

SEE ALSO

insert_bsd(2), write_bsd_protocol(2)

TEST-950 (warning) Enable pin '%s' of pad '%s' is selected for BSR cell (or TAP controller) connection, from the multiple enable

pins found for the pad: %s.

DESCRIPTION

DB Mode You receive this warning message during **preview_bsd** or **insert_bsd** if there exist multiple enable pins for the specified pad. In this case the first eligible enable pin is selected by the BSD Compiler for connection to the BSR cell (or TAP controller connection in case of TAP ports). This warning informs about the enable pin selected and the displays the list of all enable pins found.

XG Mode You receive this warning message during **preview_dft** or **insert_dft** if there exist multiple enable pins for the specified pad. In this case the first eligible enable pin is selected by the BSD Compiler for connection to the BSR cell (or TAP controller connection in case of TAP ports). This warning informs about the enable pin selected and the displays the list of all enable pins found.

WHAT NEXT

DB Mode Check what enable pin is selected for the connection. If required, drive the other enable pins to constant logic 0 or logic 1 through compliance ports and use the command **set_bsd_compliance** to spececifiy the compliance pattern. If you want to specify any other enable pin, use the command **set_bsd_pad_design** with option **-lib_cell** set to true.

XG Mode Check what enable pin is selected for the connection. If required, drive the other enable pins to constant logic 0 or logic 1 through compliance ports and use the command **set_bsd_compliance** to spececifiy the compliance pattern. If you want to specify any other enable pin, use the command **define_dft_design**.

SEE ALSO

set_bsd_pad_design (2), **define_dft_design** (2), **set_bsd_compliance** (2), **check_bsd** (2).

TEST-951 (Error) Protocol could not be generated as the test_access_port %s port is not specified.

DESCRIPTION

You get this error when "write_bsd_protocol" is used to generate protocol for a boundary-scan design and the test access port is not specified.

WHAT NEXT

Use the command set_bsd_signal <tdi | tdo | tms | tck | trst> <port_name> to specify the test access ports in DB mode.

Use the command set_dft_signal -type <tdi | tdo | tms | tck | trst> -port <port_name> to specify the test access ports in XG mode.

SEE ALSO

write_bsd_protocol(2)

TEST-952 (Warning) USERCODE instruction cannot be implemented as the IDCODE instruction is not implemented. Ignoring the USERCODE specification.

DESCRIPTION

You get this warning during preview_bsd or insert_bsd when you have specified the USERCODE instruction and a valid IDCODE specification is not found. IDCODE instruction must be implemented in order for the USERCODE instruction to be implemented.

One case You get this warning is, when you have specified the USERCODE instruction and have not specified the IDCODE instruction.

Another case you might get this warning is, when you have specified both the IDCODE and USERCODE instructions but IDCODE cannot be implemented due to appropriate environment variables not set to specify valid version number, part number and manufacturer identity.

WHAT NEXT

Provide a valid specification for the IDCODE instruction including the appropriate environment variables to specify valid version number, part number and manufacturer identity

SEE ALSO

set_bsd_instruction

TEST-953 (warning) Signal %s(%s, %s) drives clock inputs of %d flip-flops but is not reached by any test clock.

DESCRIPTION

You receive this warning message if your design contains a flip-flop clock signal that is uncontrollable. All flip-flops and latches must be controlled by clocks in

order for ATPG to generate patterns to test the surrounding logic.

The most basic check is whether a clock I/O signal controls the state of the flip-flop's clock or the state of the latch's enable at the beginning of the cycle, where they are at the clock off state.

This violation can be caused by clocks not being defined or conditioned before **rtldrc** is run. **rtldrc** does not infer clocks, but depends on the commands **create_test_clock**, **set_signal_type**, and **set_test_hold** to define the clocks and condition them to reach their destinations. If all signal definitions have been made correctly before **rtldrc** is run, this violation indicates that there are registers that cannot be controlled by ATPG. If the violation is not corrected, these registers will be unscannable and fault coverage will be reduced.

If left uncorrected, unless DFT Compiler can infer the clock, this condition will result in a TEST-169 (normal mode clock pin is uncontrollable) violation from check_scan, and the flip-flop will be declared a black box. This will cause it to be excluded from the scan chain.

WHAT NEXT

You must correct this violation to make the violated registers scannable and to increase fault coverage. This violation can be corrected using Autofix. See insert_dft(2) for details. Otherwise, proceed as follows:

1. Ensure that you have defined the test clocks using **create_test_clock**, and conditioned them using **set_signal_type** and **set_test_hold**.

2. Examine the specified flip-flops to determine why they have uncontrollable clock signals, and fix the violations.

3. Reexecute **rtldrc**.

SEE ALSO

check_scan(2), create_test_clock(2), insert_dft(2), preview_dft(2), rtldrc(2), set_test_hold(2), set_signal_type (2).

TEST-954 (warning) Signal %s(%s, %s) drives clock inputs of %d latches but is not reached by any test clock.

DESCRIPTION

You receive this warning message if your design contains a latch clock signal that is uncontrollable. All flip-flops and latches must be controlled by clocks in order for ATPG to generate patterns to test the surrounding logic.

The most basic check is whether a clock I/O signal controls the state of the flip-flop's clock or the state of the latch's enable at the beginning of the cycle, where

they are at the clock off state.

This violation can be caused by clocks not being defined or conditioned before **rtldrc** is run. **rtldrc** does not infer clocks, but depends on the commands **create_test_clock**, **set_signal_type**, and **set_test_hold** to define the clocks and condition them to reach their destinations. If all signal definitions have been made correctly before **rtldrc** is run, this violation indicates that there are registers that cannot be controlled by ATPG. If the violation is not corrected, these registers will be unscannable and fault coverage will be reduced.

If left uncorrected, unless DFT Compiler can infer the clock, this condition will result in a TEST-169 (normal mode clock pin is uncontrollable) violation from check_scan, and the latch will be declared a black box. This will cause it to be excluded from the scan chain.

WHAT NEXT

You must correct this violation to make the violated registers scannable and to increase fault coverage. This violation can be corrected using Autofix. See insert_dft(2) for details. Otherwise, proceed as follows:

1. Ensure that you have defined the test clocks using **create_test_clock**, and conditioned them using **set_signal_type** and **set_test_hold**.

2. Examine the specified latches to determine why they have uncontrollable clock signals, and fix the violations.

3. Reexecute **rtldrc**.

SEE ALSO

check_scan(2), create_test_clock(2), insert_dft(2), preview_dft(2), rtldrc(2), set_test_hold(2), set_signal_type (2).

TEST-955 (Warning) Tap controller %s does not have the required access to implement the

DESCRIPTION

You this message when the tap controller does not have the required access signal types, to implement the instruction.

Following access types are required to implement the USERCODE instruction. You must provide the required interface in order to implement the USERCODE instruction: device_id_sel (scalar) user_code_sel (scalar) user_code_val (bus [31:0])

Following access types are required to implement the IDCODE instruction: device_id_sel (scalar) ver (bus [3:0]) ver_sel (scalar) part_num (bus [15:0]) part_num_sel (scalar) mnfr_id (bus [10:0]) mnfr_id_sel (scalar)

WHAT NEXT

Case 1: If you are using not using a custom tap controller: In this case the default DesignWare tap controller is used. The default DW tap controller has the required access signals for USERCODE and IDCODE instruction support. Make sure that you have NOT set the variable bsd_use_old_tap(default false) to true. Setting bsd_use_old_tap to true will use an older version of theDesignWare tap controller, which does not support USERCODE and IDCODE instruction implementation.

case 2: If you are using custom tap controller: Make sure that your tap implementation has the required interface signals for USERCODE and IDCODE instruction support.For the bus interfaces check that the required range of bits exist.

SEE ALSO

set_bsd_tap_element set_bsd_instruction insert_bsd preview_bsd

TEST-956 (Information) Following access pins are missing from the %s tap controller interface: %s.

DESCRIPTION

You this information message showing which of the access pins are missing from the tap controller interface.

Following access types are required to implement the USERCODE instruction. You must provide the required interface in order to implement the USERCODE instruction: device_id_sel (scalar) user_code_sel (scalar) user_code_val (bus [31:0])

Following access types are required to implement the IDCODE instruction: device_id_sel (scalar) ver (bus [3:0]) ver_sel (scalar) part_num (bus [15:0]) part_num_sel (scalar) mnfr_id (bus [10:0]) mnfr_id_sel (scalar)

WHAT NEXT

Case 1: If you are using not using a custom tap controller: In this case the default DesignWare tap controller is used. The default DW tap controller has the required access signals for USERCODE and IDCODE instruction support. Make sure that you have NOT set the variable bsd_use_old_tap(default false) to true. Setting bsd_use_old_tap to true will use an older version of theDesignWare tap controller, which does not support USERCODE and IDCODE instruction implementation.

case 2: If you are using custom tap controller: Make sure that your tap implementation has the required interface signals for USERCODE and IDCODE instruction support. For the bus interfaces check that the required range of bits exist.

SEE ALSO

set_bsd_tap_element set_bsd_instruction insert_bsd preview_bsd

TEST-957 (information) There are %d asyncs in the design.

DESCRIPTION

You receive this message to inform you that **rtldrc** has identified the specified number of asynchronous control ports (asyncs) in your design. This message also lists all asyncs in the design, along with their back-annotated file names and line numbers. Back-annotated information for asyncs in other violation messages can be found here.

WHAT NEXT

If the specified number of asyncs is what you intended, no action is required on your part. Otherwise, redefine the asyncs using **set_signal_type**.

SEE ALSO

rtldrc (2), **set_signal_type** (2).

TEST-958 (information) There are %d test clocks in the design.

DESCRIPTION

You receive this message to inform you that **rtldrc** has identified the specified number of test clocks in your design. This message also lists all test clocks in the design, along with their back-annotated file names and line numbers. Back-annotated information for test clocks in other violation messages can be found here.

WHAT NEXT

If the specified number of test clocks is what you intended, no action is required on your part. Otherwise, redefine the test clocks using **create_test_clock**.

SEE ALSO

create_test_clock(2), rtldrc (2).

TEST-959 (information) There are %d blackboxes in the design.

DESCRIPTION

You receive this message to inform you that **rtldrc** has identified the specified number of objects in your design as black boxes. This message also lists the black boxes, along with their back-annotated file names and line numbers. Back-annotated information for black boxes in other violation messages can be found here.

WHAT NEXT

Examine your design for the objects that were reported as black boxes, and ensure that these black boxes are as you intended. If necessary, modify the design to eliminate some or all of the black boxes.

SEE ALSO

rtldrc (2),

TEST-960 (warning) Sensitizable feedback loop detected at %s(%s, %s).

DESCRIPTION

You receive this message to warn you that **rtldrc** found a sensitizable (active) feedback loop at the specified location. Such feedback loops can decrease fault coverage by ATPG, because paths are difficult to control if they are part of feedback loops.

If left uncorrected, this condition will result in a B23 (Feedback path) violation from TetraMAX, and often also an X1 (Feedback path is sensitizable) violation. This condition does not result in a violation from check_scan, but check_test will give a TEST-117 (combinational feedback loop) violation. All of these violations result in reduced fault coverage from ATPG.

WHAT NEXT

If you are using the loop as a latch, convert the combinational elements that make up this feedback loop into a latch from your ASIC vendor library. Otherwise, use **set_test_hold** to place known values on the loop’s inputs.

SEE ALSO

check_scan (2), **check_test** (2), **set_test_hold** (2), **rtldrc** (2).

TEST-961 (warning) Clock pins of %d flip-flops are floating.

DESCRIPTION

You receive this message to warn you that **rtldrc** has found floating clock pins on the specified flip-flops. All flip-flops and latches must be controlled by clocks in order for ATPG to generate patterns to test the surrounding logic.

The most basic check is whether a clock I/O signal controls the state of the flip-flop’s clock or the state of the latch’s enable at the beginning of the cycle, where they are at the clock off state.

This violation can be caused by clocks not being defined or conditioned before **rtldrc** is run. **rtldrc** does not infer clocks, but depends on the commands **create_test_clock**, **set_signal_type**, and **set_test_hold** to define the clocks and condition them to reach their destinations. If all signal definitions have been made correctly before **rtldrc** is run, this violation indicates that there are registers that cannot be controlled by ATPG. If the violation is not corrected, these registers will be unscannable and fault coverage will be reduced.

WHAT NEXT

You must correct this violation to make the violated registers scannable and to increase fault coverage. Proceed as follows:

1. Ensure that you have defined the test clocks using **create_test_clock**, and conditioned them using **set_signal_type** and **set_test_hold**.

2. Examine the specified flip-flops to determine why they have floating clock pins, and fix the violations.

3. Reexecute **rtldrc**.

SEE ALSO

create_test_clock(2), create_test_patterns (2), **rtldrc** (2), **set_test_hold(2), set_signal_type** (2).

TEST-962 (warning) Clock pins of %d latches are floating.

DESCRIPTION

You receive this message to warn you that **rtldrc** has found floating clock pins on the specified latches. All flip-flops and latches must be controlled by clocks in order for ATPG to generate patterns to test the surrounding logic.

The most basic check is whether a clock I/O signal controls the state of the flip-flop’s clock or the state of the latch’s enable at the beginning of the cycle, where

they are at the clock off state.

This violation can be caused by clocks not being defined or conditioned before **rtldrc** is run. **rtldrc** does not infer clocks, but depends on the commands **create_test_clock**, **set_signal_type**, and **set_test_hold** to define the clocks and condition them to reach their destinations. If all signal definitions have been made correctly before **rtldrc** is run, this violation indicates that there are registers that cannot be controlled by ATPG. If the violation is not corrected, these registers will be unscannable and fault coverage will be reduced.

WHAT NEXT

You must correct this violation to make the violated registers scannable and to increase fault coverage. Proceed as follows:

1. Ensure that you have defined the test clocks using **create_test_clock**, and conditioned them using **set_signal_type** and **set_test_hold**.

2. Examine the specified latches to determine why they have floating clock pins, and fix the violations.

3. Reexecute **rtldrc**.

SEE ALSO

create_test_clock(2), create_test_patterns (2), **rtldrc** (2), **set_test_hold(2), set_signal_type** (2).

TEST-963 (warning) Clock %s reaches %d flip-flops but does not control them at beginning of cycle.

DESCRIPTION

You receive this message to warn you that **rtldrc** has found flip-flops that are not controlled by the specified clock signal. All flip-flops and latches must be controlled by clocks in order for ATPG to generate patterns to test the surrounding logic.

The most basic check is whether a clock I/O signal controls the state of the flip-flop’s clock or the state of the latch’s enable at the beginning of the cycle, where they are at the clock off state.

This violation can be caused by clocks not being conditioned before **rtldrc** is run. **rtldrc** does not infer clocks, but depends on the commands **create_test_clock**, **set_signal_type**, and **set_test_hold** to define the clocks and condition them to reach their destinations. If all signal definitions have been made correctly before **rtldrc** is run, this violation indicates that there are registers that cannot be controlled by ATPG. If the violation is not corrected, these registers will be unscannable and fault coverage will be reduced.

If left uncorrected this condition will result in a TEST-169 (normal mode clock pin is uncontrollable) violation from check_scan, and the flip-flop will be declared a black box. This will cause it to be excluded from the scan chain.

WHAT NEXT

You must correct this violation to make the violated registers scannable and to increase fault coverage. This violation can be corrected using Autofix. See insert_dft(2) for details. Otherwise, proceed as follows:

1. Ensure that you have conditioned the test clocks using **set_signal_type** and **set_test_hold**.

2. Examine the specified flip-flops to determine why they are not controlled by the clock signal, and fix the violations.

3. Reexecute **rtldrc**.

SEE ALSO

check_scan(2), create_test_clock(2), insert_dft (2), **preview_dft** (2), **rtldrc** (2), **set_test_hold(2), set_signal_type** (2).

TEST-964 (warning) Clock %s reaches %d latches but does not control them at beginning of cycle.

DESCRIPTION

You receive this message to warn you that **rtldrc** has found latches that are not controlled by the specified clock signal. All flip-flops and latches must be controlled by clocks in order for ATPG to generate patterns to test the surrounding logic.

The most basic check is whether a clock I/O signal controls the state of the flip-flop’s clock or the state of the latch’s enable at the beginning of the cycle, where they are at the clock off state.

This violation can be caused by clocks not being conditioned before **rtldrc** is run. **rtldrc** does not infer clocks, but depends on the commands **create_test_clock**, **set_signal_type**, and **set_test_hold** to define the clocks and condition them to reach their destinations. If all signal definitions have been made correctly before **rtldrc** is run, this violation indicates that there are registers that cannot be controlled by ATPG. If the violation is not corrected, these registers will be unscannable and fault coverage will be reduced.

If left uncorrected this condition will result in a TEST-169 (normal mode clock pin is uncontrollable) violation from check_scan, and the latch will be declared a black box. This will cause it to be excluded from the scan chain.

WHAT NEXT

You must correct this violation to make the violated registers scannable and to increase fault coverage. This violation can be corrected using Autofix. See insert_dft(2) for details. Otherwise, proceed as follows:

1. Ensure that you have conditioned the test clocks using **set_signal_type** and **set_test_hold**.

2. Examine the specified latches to determine why they are not controlled by the clock signal, and fix the violations.

3. Reexecute **rtldrc**.

SEE ALSO

check_scan(2), create_test_clock(2), insert_dft (2), **preview_dft** (2), **rtldrc** (2), **set_test_hold(2), set_signal_type** (2).

TEST-965 (warning) Clock %s reaches %d latches but does not hold data in them at beginning of cycle.

DESCRIPTION

You receive this message to warn you that **rtldrc** has found that the clock does not hold data in the specified latches at the beginning of the cycle. This check is to ensure that a latch can be made scannable. For scannable latches, the latch must be forced to hold its value at the beginning of the cycle, where it is at the clock off state.

This violation is checked with the assumption that the latches should be scanned. This violation is not checked when the scan style is set to multiplexed flip-flop, unless the **test_rtldrc_latch_check_style** variable is set to **scan**.

This violation can be caused by clocks not being defined or conditioned before **rtldrc** is run. **rtldrc** does not infer clocks, but depends on the commands **create_test_clock**, **set_signal_type**, and **set_test_hold** to define the clocks and condition them to reach their destinations. If all signal definitions have been made correctly before **rtldrc** is run, this violation indicates that there are registers that cannot be controlled by ATPG. If the violation is not corrected, these registers will be unscannable and fault coverage will be reduced.

WHAT NEXT

You must correct this violation to make the violated registers scannable and to increase fault coverage. This violation can be corrected using Autofix. See insert_dft(2) for details. Otherwise, proceed as follows:

1. Ensure that you have defined the test clocks using **create_test_clock**, and

conditioned them using **set_signal_type** and **set_test_hold**.

2. Examine the specified latches to determine why the clock does not hold data in them, and fix the violations.

3. As an alternative, enable latch transparency checks in place of latch scan ability checks.

4. Reexecute **rtldrc**.

SEE ALSO

create_test_clock(2), insert_dft(2), preview_dft(2), rtldrc (2), **set_test_hold(2), set_signal_type** (2), **test_rtldrc_latch_check_style** (4).

TEST-966 (warning) No asynch reaches %d flip-flops with asynch control.

DESCRIPTION

You receive this message to warn you that **rtldrc** has found flip-flops whose asynchronous pins are not controlled by an asynchronous control signal. All flip-flops and latches with asynchronous controls must be able to have these controls held inactive in order to be made scannable.

This violation can be caused by asynchronous controls (asynchs) not being defined or conditioned before **rtldrc** is run. **rtldrc** does not infer asynchs, but depends on the commands **create_test_clock**, **set_signal_type**, and **set_test_hold** to define the asynchs and condition them to reach their destinations. (A signal defined as a **test_asynch** has a disabled value of 0, and one defined as a **test_asynch_inverted** has a disabled value of 1.)

If all signal definitions have been made correctly before **rtldrc** is run, this violation indicates that there are registers that cannot be controlled by ATPG. If the violation is not corrected, these registers will be unscannable and fault coverage will be reduced.

If left uncorrected this condition will result in a TEST-116 (asynchronous pins are uncontrollable) violation from check_scan, and the flip-flop will be declared a black box. This will cause it to be excluded from the scan chain.

WHAT NEXT

You must correct this violation to make the violated registers scannable and to increase fault coverage. This violation can be corrected using Autofix. See insert_dft(2) for details. Otherwise, proceed as follows:

1. Ensure that you have defined the test clocks using **create_test_clock**, and defined asynchronous control signals using **set_signal_type**.

2. Examine the design, locate the flip-flops whose asynchronous pins are not being controlled by an asynchronous control signal, and fix the violations.

3. Reexecute **rtldrc**.

SEE ALSO

check_scan(2), create_test_clock(2), insert_dft (2), **preview_dft** (2), **rtldrc** (2), **set_test_hold(2), set_signal_type** (2).

TEST-967 (warning) No asynch reaches %d latches with asynch control.

DESCRIPTION

You receive this message to warn you that **rtldrc** has found latches whose asynchronous pins are not controlled by an asynchronous control signal. All flip-flops and latches with asynchronous controls must be able to have these controls held inactive in order to be made scannable.

This violation can be caused by asynchronous controls (asynchs) not being defined or conditioned before **rtldrc** is run. **rtldrc** does not infer asynchs, but depends on the commands **create_test_clock**, **set_signal_type**, and **set_test_hold** to define the asynchs and condition them to reach their destinations. (A signal defined as a **test_asynch** has a disabled value of 0, and one defined as a **test_asynch_inverted** has a disabled value of 1.)

If all signal definitions have been made correctly before **rtldrc** is run, this violation indicates that there are registers that cannot be controlled by ATPG. If the violation is not corrected, these registers will be unscannable and fault coverage will be reduced.

If left uncorrected this condition will result in a TEST-116 (asynchronous pins are uncontrollable) violation from check_scan, and the latch will be declared a black box. This will cause it to be excluded from the scan chain.

WHAT NEXT

You must correct this violation to make the violated registers scannable and to increase fault coverage. This violation can be corrected using Autofix. See insert_dft(2) for details. Otherwise, proceed as follows:

1. Ensure that you have defined the test clocks using **create_test_clock**, and defined asynchronous control signals using **set_signal_type**.

2. Examine the design, locate the latches whose asynchronous pins are not being controlled by an asynchronous control signal, and fix the violations.

3. Reexecute **rtldrc**.

SEE ALSO

check_scan(2), create_test_clock(2), insert_dft (2), **preview_dft** (2), **rtldrc** (2), **set_test_hold(2), set_signal_type** (2).

TEST-968 (warning) Asynch %s reaches %d flip-flops but can not disable their asynch controls.

DESCRIPTION

You receive this message to warn you that **rtldrc** has found flip-flops whose asynchronous control signal ("Asynch") reaches a register but cannot disable the asynchronous pin. All flip-flops and latches with asynchronous controls must be able to have these controls held inactive in order to be made scannable.

This violation can be caused by asynchronous controls (asynchs) not being defined or conditioned before **rtldrc** is run. **rtldrc** does not infer asynchs, but depends on the commands **create_test_clock**, **set_signal_type**, and **set_test_hold** to define the asynchs and condition them to reach their destinations. (A signal defined as a **test_asynch** has a disabled value of 0, and one defined as a **test_asynch_inverted** has a disabled value of 1.)

If all signal definitions have been made correctly before **rtldrc** is run, this violation indicates that there are registers that cannot be controlled by ATPG. If the violation is not corrected, these registers will be unscannable and fault coverage will be reduced.

If left uncorrected this condition will result in a TEST-116 (asynchronous pins are uncontrollable) violation from check_scan, and the flip-flop will be declared a black box. This will cause it to be excluded from the scan chain.

WHAT NEXT

You must correct this violation to make the violated registers scannable and to increase fault coverage. This violation can be corrected using Autofix. See insert_dft(2) for details. Otherwise, proceed as follows:

1. Ensure that you have defined the test clocks using **create_test_clock**, and defined asynchronous control signals using **set_signal_type**.

2. Examine the design, locate the flip-flops whose asynchronous pins are not being controlled by an asynchronous control signal, and fix the violations.

3. Reexecute **rtldrc**.

SEE ALSO

check_scan(2), create_test_clock(2), insert_dft (2), **preview_dft** (2), **rtldrc** (2), **set_test_hold(2), set_signal_type** (2).

TEST-969 (warning) Asynch %s reaches %d latches but can not disable their asynch controls.

DESCRIPTION

You receive this message to warn you that **rtldrc** has found latches whose asynchronous control signal ("Asynch") reaches a register but cannot disable the asynchronous pin. All flip-flops and latches with asynchronous controls must be able to have these controls held inactive in order to be made scannable.

This violation can be caused by asynchronous controls (asynchs) not being defined or conditioned before **rtldrc** is run. **rtldrc** does not infer asynchs, but depends on the commands **create_test_clock**, **set_signal_type**, and **set_test_hold** to define the asynchs and condition them to reach their destinations. (A signal defined as a **test_asynch** has a disabled value of 0, and one defined as a **test_asynch_inverted** has a disabled value of 1.)

If all signal definitions have been made correctly before **rtldrc** is run, this violation indicates that there are registers that cannot be controlled by ATPG. If the violation is not corrected, these registers will be unscannable and fault coverage will be reduced.

If left uncorrected this condition will result in a TEST-116 (asynchronous pins are uncontrollable) violation from check_scan, and the latch will be declared a black box. This will cause it to be excluded from the scan chain.

WHAT NEXT

You must correct this violation to make the violated registers scannable and to increase fault coverage. This violation can be corrected using Autofix. See insert_dft(2) for details. Otherwise, proceed as follows:

1. Ensure that you have defined the test clocks using **create_test_clock**, and defined asynchronous control signals using **set_signal_type**.

2. Examine the design, locate the latches whose asynchronous pins are not being controlled by an asynchronous control signal, and fix the violations.

3. Reexecute **rtldrc**.

SEE ALSO

check_scan(2), create_test_clock(2), insert_dft (2), **preview_dft** (2), **rtldrc** (2), **set_test_hold(2), set_signal_type** (2).

TEST-970 (warning) Clock %s affects data inputs of %d flip-

flops.

DESCRIPTION

You receive this warning message if **rtldrc** finds flip-flops whose data inputs are driven by the specified clock signal. ATPG pulses only one clock at a time, keeping all other clocks in their off state. Thus, a clock driving the data inputs of flip-flops or latches reduces the fault coverage because ATPG cannot determine the captured input value when that clock is in its off state. Overcoming this behavior to test this logic within ATPG is not recommended, because multiple ATPG iterations and possibly special scan chain redesign would be required.

If left uncorrected this condition will result in a TEST-131 (data pin is driven by a clock/enable signal) violation from check_test. No violation will be given by check_scan because it is not related to scan shifting. TetraMAX will give a C26 (clock used as data is different from capture clock) violation.

WHAT NEXT

Modify your design so that the logic feeding the data inputs of all flip-flops is independent of clocks.

SEE ALSO

check_scan (2), **check_test** (2), **rtldrc** (2).

TEST-971 (warning) Clock %s affects data inputs of %d latches.

DESCRIPTION

You receive this warning message if **rtldrc** finds latches whose data inputs are driven by the specified clock signal. ATPG pulses only one clock at a time, keeping all other clocks in their off state. Thus, a clock driving the data inputs of flip-flops or latches reduces the fault coverage because ATPG cannot determine the captured input value. Overcoming this behavior to test this logic within ATPG is not recommended, because multiple ATPG iterations and possibly special scan chain redesign would be required.

If left uncorrected this condition will result in a TEST-131 (data pin is driven by a clock/enable signal) violation from check_test. No violation will be given by check_scan because it is not related to scan shifting. TetraMAX will give a C26 (clock used as data is different from capture clock) violation.

WHAT NEXT

Modify your design so that the logic feeding the data inputs of all latches is independent of clocks.

SEE ALSO

check_scan (2), **check_test** (2), **rtldrc** (2).

TEST-972 (warning) Clock %s affects both clock and data of %d flip-flops.

DESCRIPTION

You receive this warning message if **rtldrc** finds flip-flops for which the specified clock signal affects both the clock and the data input pin. A clock affecting both clock and data of a flip-flop or latch sets up a race condition. ATPG does not consider timing, so it can generate vectors that will fail functional simulation or fail on the tester.

If left uncorrected this condition will result in a TEST-131 (data pin is driven by a clock/enable signal) violation from check_test. No violation will be given by check_scan because it is not related to scan shifting. TetraMAX will give a C12 (LE port captured data affected by clock) violation.

WHAT NEXT

Modify the logic leading to the data paths to eliminate dependency on the clock.

SEE ALSO

check_scan (2), **check_test** (2), **rtldrc** (2).

TEST-973 (warning) Clock %s affects both clock and data of %d latches.

DESCRIPTION

You receive this warning message if **rtldrc** finds latches for which the specified clock signal affects both the clock and the data input pin. A clock affecting both clock and data of a flip-flop or latch sets up a race condition. ATPG does not consider timing, so it can generate vectors that will fail functional simulation or fail on the tester.

If left uncorrected this condition will result in a TEST-131 (data pin is driven by a clock/enable signal) violation from check_test. No violation will be given by check_scan because it is not related to scan shifting. TetraMAX will give a C15 (LS port captured data affected by clock) violation.

WHAT NEXT

Modify your design so that the logic leading to the data paths is independent of the clock.

SEE ALSO

check_scan (2), **check_test** (2), **rtldrc** (2).

TEST-974 (warning) Latch enabled by clock %s affects data inputs of %d latches on the same clock.

DESCRIPTION

You receive this warning message if **rtldrc** finds latches that are enabled by the same clock, but have a combinational data path between them. Thus, data is propagated through both latches in a single clock cycle, which reduces the ability of ATPG to observe logic along this path. In some cases, ATPG could generate vectors that fail functional simulation or fail on the tester.

If left uncorrected this condition will result in a TEST-478 (pin cannot capture reliably) violation from check_test. No violation will be given by check_scan because it is not related to scan shifting. TetraMAX will give a C5 (LS port captured data affected by new capture) violation.

WHAT NEXT

Modify your design so that the logic leading to the affected latches does not contain paths affected by latches enabled by the same clock.

SEE ALSO

check_scan (2), **check_test** (2), **rtldrc** (2).

TEST-975 (warning) Latch enabled by clock %s affects data inputs of %d flip-flops clocked by the trailing edge of the same clock.

DESCRIPTION

You receive this warning message if **rtldrc** finds flip-flops that receive data from latches enabled by the same clock, such that the clock's trailing edge both clocks the flip-flops and disables the latches so that their data is held. In this case,

race conditions could result.

If left uncorrected this condition will result in a TEST-478 (pin cannot capture reliably) violation from check_test. No violation will be given by check_scan because it is not related to scan shifting. TetraMAX will give a C6 (TE port captured data affected by new capture) violation. This is a relatively minor violation for TetraMAX, since it can generate good vectors in this situation without loss of fault coverage.

WHAT NEXT

Consider modifying your design so that the logic feeding the data inputs of the flip-flops does not go through the latches.

SEE ALSO

check_scan (2), **check_test** (2), **rtldrc** (2).

TEST-976 (warning) Clocks %s and %s cannot capture on %d latches with the other off.

DESCRIPTION

You receive this warning if **rtldrc** finds latches that capture as a result of more than one clock, but cannot capture with one clock active and all others off. ATPG pulses only one clock at a given time, keeping all other clocks in their off states. Thus, if multiple clocks must be active, the latches cannot capture and fault coverage is reduced.

If left uncorrected this condition will result in a TEST-310 (data cannot be captured into cell) violation from check_test. No violation will be given by check_scan because it is not related to scan shifting. TetraMAX will give a C15 (scan cell port unable to capture) violation.

WHAT NEXT

Modify your design so that the the clock gating logic for latches is as follows:

Clock and Data are ANDed
The two clocks are ORed

SEE ALSO

check_scan (2), **check_test** (2), **rtldrc** (2).

TEST-977 (warning) Clocks %s and %s both capture on %d flip-flops.

DESCRIPTION

You receive this warning message if **rtldrc** finds flip-flops that can capture as a result of two different clocks. This situation allows a write-over write operation without an intermediate read, so that one of the values is not observable.

If left uncorrected this condition will result in a TEST-310 (data cannot be captured into cell) violation from check_test. No violation will be given by check_scan because it is not related to scan shifting. TetraMAX will give a C15 (scan cell port unable to capture) violation.

WHAT NEXT

Modify your design so that the flip-flops capture as a result of only one clock.

SEE ALSO

check_scan (2), **check_test** (2), **rtldrc** (2).

TEST-978 (warning) Signal %s(%s, %s) illegally combines clock %s and latch data to clock %d flip-flops.

DESCRIPTION

You receive this warning message if **rtldrc** finds a clock gated with the output of a latch clocked by it. This is an illegal combination, and results in timing hazards, including clock glitches and delayed clocks. In some cases, ATPG can generate vectors that will fail functional simulation or fail on the tester.

If left uncorrected this condition will result in a TEST-140 (clock signal is illegally gated) violation from check_test. No violation will be given by check_scan because it is not related to scan shifting. TetraMAX will give a C8 (LS port clock path affected by new capture) violation.

WHAT NEXT

Modify your design so that the clock gating logic leading to the affected registers do not contain paths affected by latches enabled by the same clock.

SEE ALSO

check_scan (2), **check_test** (2), **rtldrc** (2).

TEST-979 (warning) Signal %s(%s, %s) illegally combines clock %s and latch data to clock %d latches.

DESCRIPTION

You receive this warning message if **rtldrc** finds a clock gated with the output of a latch clocked by it. This is an illegal combination, and results in timing hazards including clock glitches and delayed clocks. In some cases, ATPG can generate vectors that will fail functional simulation or fail on the tester.

If left uncorrected this condition will result in a TEST-140 (clock signal is illegally gated) violation from check_test. No violation will be given by check_scan because it is not related to scan shifting. TetraMAX will give a C8 (LS port clock path affected by new capture) violation.

WHAT NEXT

Modify your design so that the clock gating logic leading to the affected registers do not contain paths affected by latches enabled by the same clock.

SEE ALSO

check_scan (2), **check_test** (2), **rtldrc** (2).

TEST-980 (warning) Signal %s(%s, %s) illegally combines clock %s and flip-flop data to clock %d flip-flops.

DESCRIPTION

You receive this warning message if **rtldrc** finds a clock gated with the output of a flip-flop clocked by it. This is an illegal combination, and results in timing hazards including clock glitches and delayed clocks. In some cases, ATPG can generate vectors that will fail functional simulation or fail on the tester.

If left uncorrected this condition will result in a TEST-140 (clock signal is illegally gated) violation from check_test. No violation will be given by check_scan because it is not related to scan shifting. TetraMAX will give a C8 (LS port clock path affected by new capture) violation.

WHAT NEXT

Modify your design so that the clock gating logic leading to the affected registers do not contain paths affected by flip-flops enabled by the same clock.

SEE ALSO

check_scan (2), **check_test** (2), **rtldrc** (2).

TEST-981 (warning) Signal %s(%s, %s) illegally combines clock %s and flip-flop data to clock %d latches.

DESCRIPTION

You receive this warning message if **rtldrc** finds a clock gated with the output of a latch clocked by it. This is an illegal combination, and results in timing hazards including clock glitches and delayed clocks. In some cases, ATPG can generate vectors that will fail functional simulation or fail on the tester.

If left uncorrected this condition will result in a TEST-140 (clock signal is illegally gated) violation from check_test. No violation will be given by check_scan because it is not related to scan shifting. TetraMAX will give a C8 (LS port clock path affected by new capture) violation.

WHAT NEXT

Modify your design so that the clock gating logic leading to the affected registers do not contain paths affected by latches enabled by the same clock.

SEE ALSO

check_scan (2), **check_test** (2), **rtldrc** (2).

TEST-982 (warning) Black box instance %s(%s, %s) feeds data inputs of %d flip-flops.

DESCRIPTION

You receive this warning message if **rtldrc** finds flip-flops whose data inputs are driven by black boxes. Logic that drives or is driven by black boxes cannot be tested, because it is unobservable or uncontrollable. Usually this condition has a minor effect on fault coverage, unless the logic driven by black boxes feeds clock or asynchronous control inputs of registers. In that case, the registers can become unscannable and have a large effect on coverage.

WHAT NEXT

Modify your design to eliminate the specified black box instance.

SEE ALSO

create_test_patterns (2), **rtldrc** (2).

TEST-983 (warning) Black box instance %s(%s, %s) feeds data inputs of %d latches.

DESCRIPTION

You receive this warning message if **rtldrc** finds latches whose data inputs are driven by black boxes. Logic that drives or is driven by black boxes cannot be tested, because it is unobservable or uncontrollable. Usually this condition has a minor effect on fault coverage, unless the logic driven by black boxes feeds clock or asynchronous control inputs of registers. In that case, the registers can become unscannable and have a large effect on coverage.

WHAT NEXT

Modify your design to eliminate the specified black box instance.

SEE ALSO

create_test_patterns (2), **rtldrc** (2).

TEST-984 (warning) Black box instance %s(%s, %s) feeds clock inputs of %d flip-flops.

DESCRIPTION

You receive this warning message if **rtldrc** finds flip-flops whose clock inputs are driven by black boxes. Logic that drives or is driven by black boxes cannot be tested, because it is unobservable or uncontrollable. Usually this condition has a minor effect on fault coverage, unless the logic driven by black boxes feeds clock or asynchronous control inputs of registers. In that case, the registers can become unscannable and have a large effect on coverage.

WHAT NEXT

Modify your design to eliminate the specified black box instance.

SEE ALSO

create_test_patterns (2), **rtldrc** (2).

TEST-985 (warning) Black box instance %s(%s, %s) feeds clock inputs of %d latches.

DESCRIPTION

You receive this warning message if **rtldrc** finds latches whose clock inputs are driven by black boxes. Logic that drives or is driven by black boxes cannot be tested, because it is unobservable or uncontrollable. Usually this condition has a minor effect on fault coverage, unless the logic driven by black boxes feeds clock or asynchronous control inputs of registers. In that case, the registers can become unscannable and have a large effect on coverage.

WHAT NEXT

Modify your design to eliminate the specified black box instance.

SEE ALSO

create_test_patterns (2), **rtldrc** (2).

TEST-986 (warning) Black box instance %s(%s, %s) feeds asynchronous control inputs of %d flip-flops.

DESCRIPTION

You receive this warning message if **rtldrc** finds flip-flops whose asynchronous control inputs are driven by black boxes. Logic that drives or is driven by black boxes cannot be tested, because it is unobservable or uncontrollable. Usually this condition has a minor effect on fault coverage, unless the logic driven by black boxes feeds clock or asynchronous control inputs of registers. In that case, the registers can become unscannable and have a large effect on coverage.

WHAT NEXT

Modify your design to eliminate the specified black box instance.

SEE ALSO

create_test_patterns (2), **rtldrc** (2).

TEST-987 (warning) Black box instance %s(%s, %s)

feeds asynchronous control inputs of %d latches.

DESCRIPTION

You receive this warning message if **rtldrc** finds latches whose asynchronous control inputs are driven by black boxes. Logic that drives or is driven by black boxes cannot be tested, because it is unobservable or uncontrollable. Usually this condition has a minor effect on fault coverage, unless the logic driven by black boxes feeds clock or asynchronous control inputs of registers. In that case, the registers can become unscannable and have a large effect on coverage.

WHAT NEXT

Modify your design to eliminate the specified black box instance.

SEE ALSO

create_test_patterns (2), **rtldrc** (2).

TEST-988 (warning) Black box instance %s(%s, %s) receives data from %d flip-flops.

DESCRIPTION

You receive this warning message if **rtldrc** finds flip-flops that drive the specified black box instance. Logic that drives or is driven by black boxes cannot be tested, because it is unobservable or uncontrollable. Usually this condition has a minor effect on fault coverage, unless the logic driven by black boxes feeds clock or asynchronous control inputs of registers. In that case, the registers can become unscannable and have a large effect on coverage.

WHAT NEXT

Modify your design to eliminate the specified black box instance.

SEE ALSO

create_test_patterns (2), **rtldrc** (2).

TEST-989 (warning) Black box instance %s(%s, %s)

receives data from %d latches.

DESCRIPTION

You receive this warning message if **rtldrc** finds latches that drive the specified black box instance. Logic that drives or is driven by black boxes cannot be tested, because it is unobservable or uncontrollable. Usually this condition has a minor effect on fault coverage, unless the logic driven by black boxes feeds clock or asynchronous control inputs of registers. In that case, the registers can become unscannable and have a large effect on coverage.

WHAT NEXT

Modify your design to eliminate the specified black box instance.

SEE ALSO

create_test_patterns (2), **rtldrc** (2).

TEST-990 (warning) Black box instance %s(%s, %s) feeds %d output ports.

DESCRIPTION

You receive this warning message if **rtldrc** finds output ports driven by the specified black box instance. Logic that drives or is driven by black boxes cannot be tested, because it is unobservable or uncontrollable. Usually this condition has a minor effect on fault coverage, unless the logic driven by black boxes feeds clock or asynchronous control inputs of registers. In that case, the registers can become unscannable and have a large effect on coverage.

WHAT NEXT

Modify your design to eliminate the specified black box instance.

SEE ALSO

create_test_patterns (2), **rtldrc** (2).

TEST-991 (warning) Black box instance %s(%s, %s)

receives data from %d input ports.

DESCRIPTION

You receive this warning message if **rtldrc** finds input ports that drive the specified black box instance. Logic that drives or is driven by black boxes cannot be tested, because it is unobservable or uncontrollable. Usually this condition has a minor effect on fault coverage, unless the logic driven by black boxes feeds clock or asynchronous control inputs of registers. In that case, the registers can become unscannable and have a large effect on coverage.

WHAT NEXT

Modify your design to eliminate the specified black box instance.

SEE ALSO

create_test_patterns (2), **rtldrc** (2).

TEST-992 (warning) The argument to set_scan_register_type -type
does not contain a valid scan equivalent for cell or design %s.
Ignoring the -type specification and replacing it with the best match.

DESCRIPTION

You receive this message if none of the scan cells you supplied as arguments to **set_scan_register_type -type** are valid scan equivalents of the specified nonscan cell or design. In this case, **insert_scan** and **compile -scan** disregard the **-type** specification, search the target library for a scan cell that is the best possible match, and replace the nonscan cell with that best match.

WHAT NEXT

If you can accept the scan replacement implemented by **insert_scan** or **compile -scan**, no action is required on your part. However, if you still want to specify a scan replacement for the nonscan cell, first, ensure that you did not make any typing or spelling errors when you issued the **set_scan_register_type** command. Then proceed as follows:

1. Look for a closer match for the nonscan cell within the target library.

Alternatively, if the specification is set on the RTL netlist, use the **set_register_type** command to match the nonscan cell more closely to the scan cell.

2. Reissue **set_scan_register_type** with the appropriate arguments.

3. Reissue **insert_scan** or **compile -scan**.

SEE ALSO

compile (2), **insert_scan** (2), **set_scan_register_type** (2).

TEST-993 (error) Design has more than 6 TEST CLOCKs and TEST ASYNCs.

DESCRIPTION

You receive this message if **rtldrc** finds more than 6 test-related clocks and asynchronous signals in your design. The current implementation of RTL DRC can accept only six or fewer.

WHAT NEXT

Modify your design so that the total number of test clocks and asynchronous signals is six or fewer.

SEE ALSO

rtldrc (2).

TEST-994 (warning) Clock %s affects multiple clock or asynch ports of %d registers.

DESCRIPTION

You receive this message if **rtldrc** finds a clock that affects more than one clock port or asynchronous control port of flip-flops or latches. This situation prevents ATPG from capturing data with the registers, and reduces fault coverage.

If left uncorrected this condition will result in a TEST-131 (data pin is driven by a clock/enable signal) violation from check_test. No violation will be given by check_scan because it is not related to scan shifting.

WHAT NEXT

Modify your design so that the specified clock affects only one port on each flip-flop or latch. The specific data that is captured should be determined at the data input of the register.

SEE ALSO

check_scan (2), **check_test** (2), **rtldrc** (2).

TEST-995 (information) %s (%s, %s)

DESCRIPTION

The register is affected by the RTLDRC violation.

WHAT NEXT

Correct the logic.

TEST-996 (Error) Can not optimize the Boundary-Scan logic. Boundary-Scan logic is not inserted using 'insert_bsd' command.

DESCRIPTION

The **insert_bsd** command should be invoked before invoking the **optimize_bsd** command. If the Boundary-Scan circuitry is not inserted using **insert_bsd** command, the **optimize_bsd** command cannot be used to optimize the boundary-scan logic. Make sure to run **insert_bsd** before running **optimize_bsd**.

WHAT NEXT

Run **insert_bsd** if you want to add boundary-scan logic to the design.

TEST-997 (information) Design has %d transparent latches.

DESCRIPTION

You receive this message to inform you that **rtldrc** has found in your design the

specified list of transparent latches in the off state.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

rtldrc (2).

TEST-998 (error) Design has %d ports defined as both TEST CLOCKs and TEST ASYNCs.

DESCRIPTION

You receive this message if **rtldrc** finds ports that are defined both as test clocks and test asynchronous signals (asyncs). You cannot define a port as both a test clock and an async.

WHAT NEXT

Reexecute **create_test_clock** or **set_signal_type -test_asych** to ensure that you define each of the specified ports as either a test clock or a test asynch, but not both.

SEE ALSO

create_test_clock (2), **rtldrc** (2), **set_signal_type** (2).

TEST-999 (warning) Removing the 'set_scan_register_type' on the bit %s of multibit.

DESCRIPTION

You receive this warning message if the **scan_register_type** attribute is set on some, but not all, of the bits of a multibit register. You must set this attribute either on all or on none of the bits of a multibit register. This message informs you that the **scan_register_type** attribute is being removed from the specified bit.

WHAT NEXT

If removing the **scan_register_type** attribute from the specified bit is acceptable to you, no action is required on your part. Otherwise, use the **set_scan_register_type**

command to set the attribute on all bits of the multibit register, and reexecute.

SEE ALSO

set_scan_register_type (2).

TEST-1000b (warning) Mismatch in the value of variable %s.Its current value is %s and its value during last check_bsd run was %s. Current value is used.

DESCRIPTION

You receive this warning message because the current value of the environment variable is different from its value during the previous **check_bsd** command run. This difference triggers an invisible run of **check_bsd** using the current value of the variable.

The warning message appears while executing either the **write_bsdl** command or the **create_bsd_patterns** command.

The result of **write_bsdl** or **create_bsd_patterns** reflects the results of the invisible **check_bsd** run instead of the previous **check_bsd** run.

WHAT NEXT

No action is required on your part.

However, if you want to suppress the invisible **check_bsd** rerun, ensure that the environment variable during the previous **check_bsd** run is the same environment variable that was used during the **write_bsdl** or **create_bsd_patterns**.

SEE ALSO

check_bsd (2), **create_bsd_patterns** (2), **write_bsdl** (2).

TEST-1000a (warning) Mismatch in the value of variable %s. Its current value is %d and its value during last check_bsd run was %d. Current value is used.

DESCRIPTION

You receive this warning message because the current value of the environment

variable is different from its value during the previous check_bsd command run. This difference triggers an invisible run of **check_bsd** using the current value of the variable.

The warning message occurs while executing either the **write_bsdl** command or the **create_bsd_patterns** command.

The result of **write_bsdl** or **create_bsd_patterns** reflects the results of the invisible **check_bsd** run, instead of the previous **check_bsd** run.

WHAT NEXT

No action is required on your part.

However, if you want to suppress the invisible **check_bsd** rerun, ensure that the environment variable during the previous **check_bsd** run is the same environment variable that was used during **write_bsdl** or **create_bsd_patterns**.

SEE ALSO

check_bsd (2), **create_bsd_patterns** (2), **write_bsdl** (2).

TEST-1001 (error) Cannot open file %s in read or write mode.

DESCRIPTION

You receive this message if **preview_scan** or **insert_scan** cannot open the place and route report file for reading, or if **write_layout_scan** cannot open the scan chain information output file (*design*.def or a user-specified filename) for writing.

By default, **write_layout_scan** writes scan chain information required for third party place and route tools into a file *design*.def. You can override the default filename and specify another filename by executing **write_layout_scan** with the **-output** option. If you receive this message from **write_layout_scan**, you might not have permission to write a file to that directory, or the file might already exist and be write-protected.

When **preview_scan** and **insert_scan** route scan chains, they use information in the place and route report file previously specified by **set_scan_configuration -prfile**. If you receive this message from **preview_scan** or **insert_scan**, the specified place and route report file might not exist or might be read-protected.

WHAT NEXT

If the file specified in this error message is the scan chain information file to be generated by **write_layout_scan**, proceed as follows:

1. Check whether the file already exists and is write-protected. If so, change the permissions so that you can overwrite the file.

2. If the file does not already exist, determine whether you have write permission for the directory, and if not, change the permissions so that you can write a file to the directory. If you cannot change the permissions on that directory, change your working directory to one in which you have write permission.

3. Re-execute **write_layout_scan**.

If the file specified in this error message is the place and route report file to be read by **preview_scan** or **insert_scan**, proceed as follows:

1. Verify that the place and route report file exists. If it does not, execute the place and route tool to generate the report file using as input the *design*.def file generated by **write_layout_scan**. For more information, see the **write_layout_scan** manual page.

2. Examine the filename and verify that you entered it correctly, without typos or spelling errors.

3. Verify that you have read permission for the file. If not, change the permissions accordingly.

4. Re-execute **preview_scan** or **insert_scan**.

SEE ALSO

insert_scan (2), **preview_scan** (2), **set_scan_configuration** (2), **write_layout_scan** (2).

TEST-1002 (error) Error %s near %s at line number %d.

DESCRIPTION

You received this message because **preview_scan** or **insert_scan** found a syntax error at the specified line number of the place and route report file specified through **set_scan_configuration -prfile**.

This error could occur for one of the following reasons:

- The wrong filename was specified for the **-prfile** option.
- The file has been corrupted.
- The place and route tool has introduced syntax unknown to **preview_scan** or **insert_scan**.

WHAT NEXT

If you receive this message, proceed as follows:

1. Verify whether the correct filename was specified. If not, re-execute **set_scan_configuration -prfile** with the correct filename, then re-execute **preview_scan** or **insert_scan**.

2. Examine the line where the error occurred and try to determine whether the file is corrupted. If it is, re-execute the place and route tool to regenerate the file, then re-execute **preview_scan** or **insert_scan**.

3. If the error persists, contact Synopsys Technical Support.

SEE ALSO

insert_scan (2), **preview_scan** (2), **set_scan_configuration** (2), **write_layout_scan** (2).

TEST-1003 (error) Syntax errors found while parsing file %s.

DESCRIPTION

You receive this message if the **insert_scan** or **preview_scan** command encounters syntax errors while parsing the place and route report file you specified through **set_scan_configuration -prfile**. If the file has syntax errors, the tool cannot parse it.

WHAT NEXT

Examine the report file for syntax errors, and correct them. For assistance in locating the errors, contact Synopsys Technical Support.

SEE ALSO

insert_scan (2), **preview_scan** (2), **set_scan_configuration** (2).

TEST-1004 (error) Scan flip-flop %s, specified in the place and route report file, was not found in scan chain %s of design.

DESCRIPTION

You receive this message if a scan flip-flop in a particular scan chain, specified in the place and route report file, cannot be found by **insert_scan** or **preview_scan**. The place and route report file was specified through **set_scan_configuration -prfile**.

This error message could have been caused by a spelling error or a typo in the name of the scan flip-flop. Or, you might have changed test constraints after using

write_layout_scan to generate the place and route scan information file (*design*.def), which the place and route tool uses to generate the place and route report file.

WHAT NEXT

First, check for and correct spelling errors and typos.

Next, if you want the specified scan flip-flop to be in the scan chain, proceed as follows:

1. Examine the place and route report file, and verify that it contains the flip-flop.

2. Execute **set_scan_configuration** with options such that **check_test** can extract the flip-flop along with the scan chain information.

3. Execute **check_test** and correct any violations.

4. Re-execute **preview_scan** or **insert_scan**.

Alternatively, if you have changed your test constraints and no longer want the scan flip-flop to be in the scan chain, proceed as follows:

1. Execute **check_test** to extract the updated scan chain information.

2. Execute **write_layout_scan** to generate an updated *design*.def file.

3. Execute the place and route tool to generate an updated place and route report file.

4. Execute **set_scan_configuration** with appropriate options.

5. Re-execute **check_test**.

6. Re-execute **preview_scan** or **insert_scan**.

SEE ALSO

check_test (2), **insert_scan** (2), **preview_scan** (2), **set_scan_configuration** (2).

TEST-1005 (error) You must specify a target place and route tool using **set_scan_configuration -prtool**.

DESCRIPTION

You receive this message if you issue the **write_layout_scan** command without having specified the target place and route tool to be used for scan chain reordering. Before issuing **write_layout_scan**, you must use **set_scan_configuration -prtool** to

specify the required place and route tool.

WHAT NEXT

Execute **set-scan_configuration -prtool** and specify the target place and route tool to be used. Then re-execute **write_layout_scan**.

SEE ALSO

set_scan_configuration (2), **write_layout_scan** (2).

TEST-1006 (error) Combinational logic found between %s and %s; you cannot use combinational logic other than buffers and inverters in the scan path between scan flip-flops

DESCRIPTION

You receive this message if your design contains combinational logic other than buffers and inverters in a scan path between scan flip-flops. The scan chain reordering using third party place and route tools does not support combinational logic between scan paths.

Please note that you may get TEST-1006 message while writing out the scan def, if you are using extraction flow with the input netlist, which was originally written in multi-mode scan insertion flow or Adaptive Scan flow. The support for scan def is not available in this type of extraction flows.

WHAT NEXT

Modify your design so that it does not contain combinational logic between scan states.

TEST-1007 (error) Cannot create a net between two pins.

DESCRIPTION

While restitching the netlist using placement order, the tool could not create nets between two pins.

WHAT NEXT

This is an internal error. Contact Synopsys Technical Support.

TEST-1008 (error) Cannot find a scan-in pin for cell %s.

DESCRIPTION

You receive this message if **insert_scan**, **preview_scan**, or **write_layout_scan** could not find a scan-in pin for the specified cell; this scan-in pin should have been extracted by **check_test** while extracting scan chain information. The placement-based scan chain ordering requires a scan-in pin for each cell.

This error would occur if you did not execute **check_test**, or if **check_test** did not extract the scan chain information correctly.

WHAT NEXT

Try to extract the missing scan-in pin by re-executing **check_test**. Then re-execute **insert_scan**, **preview_scan**, or **write_layout_scan**. If the scan-in pin is still missing, contact Synopsys Technical Support for assistance.

SEE ALSO

check_test (2), **insert_scan** (2), **preview_scan** (2), **write_layout_scan** (2).

TEST-1009 (error) Cannot find a scan-out pin for cell %s.

DESCRIPTION

You receive this message if **insert_scan**, **preview_scan**, or **write_layout_scan** could not find a scan-out pin for the specified cell; this scan-out pin should have been extracted by **check_test** while extracting scan chain information. The placement-based scan chain ordering requires a scan-out pin for each cell.

This error would occur if you did not execute **check_test**, or if **check_test** did not extract the scan chain information correctly.

WHAT NEXT

Try to extract the missing scan-out pin by re-executing **check_test**. Then re-execute **insert_scan**, **preview_scan**, or **write_layout_scan**. If the scan-out pin is still missing, contact Synopsys Technical Support for assistance.

SEE ALSO

check_test (2), **insert_scan** (2), **preview_scan** (2), **write_layout_scan** (2).

TEST-1010 (error) Scan chain name %s in place and route report file differs from original name.

DESCRIPTION

You receive this message if **preview_scan** or **insert_scan** finds that the name of the specified scan chain in the place and route report file differs from the name of the same scan chain in the file originally generated by **write_layout_scan**. The scan chain names specified in the report file must match the scan chain names originally exported to the place and route tools.

This error could have been caused by a spelling error or typo; by entering the wrong filename when you specified the **-prfile** option; or by manually changing the scan chain name while in the place and route tool.

WHAT NEXT

If you receive this message, first check for and correct spelling errors or typos, and examine the place and route report file to verify that it is the correct one for this design.

If you still need to correct the error, decide which of the conflicting names you want to use. Then do one of the following:

1. If you want to change the name of the scan chain in the design, do so using **set_scan_path**. Then execute **set_scan_configuration**, **check_test**, **write_layout_scan**, and the place and route tool; then re-execute **preview_scan** or **insert_scan**.

2. Alternatively, if you want to keep the name of the scan chain in the design, first try using the existing *design*.def file to regenerate the report file using the place and route tool, then re-execute **preview_scan** or **insert_scan**. If the problem persists, execute **set_scan_configuration**, **check_test**, **write_layout_scan**, and the place and route tool; then re-execute **preview_scan** and **insert_scan**.

SEE ALSO

check_test (2), **insert_scan** (2), **preview_scan** (2), **set_scan_configuration** (2), **set_scan_path** (2).

TEST-1011 (error) Scan cell pins are not loaded properly for scan def generation.

DESCRIPTION

You receive this message if **write_scan_def** could not load scan cell input and output pins properly while generating scan def ASCII file for the place and route tool to

perform scan reordering and repartitioning. Please make sure after scan insertion, **dft_drc** command successfully traced all the scan chains without any scan chain violations. Please also make sure that the CTL ASCII file generated after scan insertion using **write_test_model** command represents all the scan chain information correctly.

This error would occur if the CTL model is not correctly updated with the scan chain information or if **dft_drc** did not extract the scan chains post scan insertion.

This error can also happen in a Hierarchical Scan Synthesis flow, where the CTL models for the blocks are corrupted or not read correctly. Please make sure that such occurrences, if any, are addressed.

WHAT NEXT

If you did not execute **dft_drc**, do so now; then re-execute **write_scan_def** command. Otherwise, re-execute **set_scan_configuration** and ensure that you do not use any options that might prevent **dft_drc** from extracting the scan chain information. Re-execute **dft_drc**, correct any violations, and then re-execute **write_scan_def**. If still the message is displayed, re-execute **write_test_model** command and analyze the scan chain structures for correctness.

SEE ALSO

dft_drc (2), **insert_dft** (2), **preview_dft(2), write_scan_def(2), write_test_model(2), set_scan_configuration** (2).

TEST-1012 (error) Invalid scan configuration. The number of scan chains, %d, specified by **set_scan_configuration -chain_count**, does not agree with the number of scan chains, %d, in the place and route report file.

DESCRIPTION

You receive this message from **preview_scan** or **insert_scan** if the number of scan chains specified with **set_scan_configuration -chain_count** does not agree with the number of scan chains in the place and route report file. This condition invalidates the scan configuration specified while restitching scan chains using the place and route report file.

WHAT NEXT

Examine the place and route report file to find the number of scan chains specified. Re-execute **set_scan_configuration -chain_count** and specify the same number, then re-execute **check_test** and **preview_scan** or **insert_scan**.

SEE ALSO

check_test (2), **insert_scan** (2), **preview_scan** (2), **set_scan_configuration** (2).

TEST-1013 (error) Invalid scan configuration. The **set_scan_configuration -add_lockup** is set to *false*, but there are lockup latches in the place and route report file.

DESCRIPTION

You receive this message from **preview_scan** or **insert_scan** if **set_scan_configuration -add_lockup false** is specified but there are lockup latches in the place and route report file. This condition invalidates the scan configuration specified while restitching scan chains using the place and route report file.

WHAT NEXT

Verify that there are lockup latches in the place and route report file. Then execute **set_scan_configuration -add_lockup true** and re-execute **check_test** and **preview_scan** or **insert_scan**.

SEE ALSO

check_test (2), **insert_scan** (2), **preview_scan** (2), **set_scan_configuration** (2).

TEST-1014 (error) Invalid scan configuration. The clock mixing specification is inconsistent between the place and route report file and the scan configuration.

DESCRIPTION

You receive this message from **preview_scan** or **insert_scan** if you execute the **set_scan_configuration** command with no clock mixing, but the place and route report file contains scan chains that have clock mixing. This condition invalidates the scan configuration specified while restitching scan chains using the place and route report file.

WHAT NEXT

Examine the place and route report file to find out the type of clocking specified. Then re-execute **set_scan_configuration -clock_mixing** and specify the appropriate argument for **-clock_mixing**. Re-execute **check_test**, **preview_scan**, and **insert_scan**.

SEE ALSO

check_test (2), **insert_scan** (2), **preview_scan** (2), **set_scan_configuration** (2).

TEST-1015 (error) Physical design information is not available for scan cells.

DESCRIPTION

You receive this error message because you executed the **preview_scan** or the **insert_scan** command with the **-physical** option and the physical design information is not present.

WHAT NEXT

Run the **physopt** or the **compile_physical** command with the **-scan** option to read in physical design information.

SEE ALSO

compile_physical (2), **insert_scan** (2), **physopt** (2), **preview_scan** (2).

TEST-1016 (Warning) XY locations are missing for %s scan cell or scan port.

DESCRIPTION

You receive this error message because the x and y locations of certain scan cells or ports are not present to run the commands **preview_scan -physical** or **insert_scan -physical**.

WHAT NEXT

Run the **physopt** command or the **compile_physical -scan** command to place the scan cells and the ports.

SEE ALSO

compile_physical (2), **insert_scan** (2), **physopt** (2), **preview_scan** (2).

TEST-1017 (Warning) Serial port %s of scan chain %s does not exist in floorplan.

DESCRIPTION

You receive this error message because you executed the **preview_scan -physical** or the **insert_scan -physical** command, but the scan-in or scan-out ports are not present in the floorplan. Serial ports such as scan-in and scan-out must have a valid floorplan before **preview_scan -physical** or **insert_scan -physical** are used.

WHAT NEXT

Create scan-in and scan-out ports and include them in your design floorplan. Then, reexecute the command.

SEE ALSO

insert_scan (2), **preview_scan** (2).

TEST-1018 (error) Cells (%s, %s) have locations overlapping.

DESCRIPTION

You receive this error message because you specified cells having the same location when you executed the **preview_scan -physical** or **insert_scan -physical** command.

All scan cells in the design must have valid locations before you can run the **preview_scan -physical** or **insert_scan -physical** command.

WHAT NEXT

Reexecute the **preview_scan -physical** or **insert_scan -physical** command and specify a valid placement using the proper **physopt** commands.

SEE ALSO

insert_scan (2), **preview_scan** (2).

TEST-1019 (warning) Scan cells reordering can not be applied

on the scan chain (%s).

DESCRIPTION

You receive this warning message because all of the cells have a user-specified position in the current scan chain. This position is defined first by using the **set_scan_path** command.

WHAT NEXT

No action is required on your part.

However, you can use the **remove_scan_specification** command on the current scan chain and reexecute the **preview_scan -physical** or **insert_scan -physical** command to apply physical ordering.

SEE ALSO

insert_scan (2), **preview_scan** (2), **remove_scan_specification** (2), **set_scan_configuration** (2), **set_scan_path** (2).

TEST-1020 (warning) Chain length requirements can not be honored on scan chain '%s'. Scan architect will ignore this specification.

DESCRIPTION

You receive this warning message when scan architect is unable to build a scan chain with the sequential length required.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_scan (2), **preview_scan** (2), **set_scan_configuration** (2), **set_scan_path** (2).

TEST-1021 (warning) Chain clock requirements is only considered with no mixing clock configuration. Scan architect

will ignore this specification.

DESCRIPTION

You receive this warning message because the global scan clock specification is not equal to no mixing clock, and the clock specification is required for a scan chain.

WHAT NEXT

No action is required on your part.

However, if you want the scan architect to use the scan chain, set the global scan clock specification to no mixing clock.

SEE ALSO

insert_scan (2), **preview_scan** (2), **set_scan_configuration** (2), **set_scan_path** (2).

TEST-1022 (error) Cannot find the lockup latch clock for the segment '%s'.

DESCRIPTION

You receive this error message because the **insert_dft** or **preview_dft** command cannot not find a clock for the lockup latch associated with the segment while designing scan chains.

WHAT NEXT

Verify that the segment defined with the **set_scan_segment** command is correct. If necessary, correct the definition and run the **insert_dft** or **preview_dft** command again.

If the lockup clock is still missing, contact Synopsys Technical Support for assistance.

SEE ALSO

insert_dft (2), **preview_dft** (2), **set_scan_segment** (2).

TEST-1023 (warning) Core scan segment '%s' has a lockup

latch on the output.

DESCRIPTION

You receive this warning message when any of the following are true:

• You specified to mix edges or mix clocks in your scan configuration.

• The reported core scan segment has a lockup latch placed at the end of the segment.

• You have other core scan segments triggered by the same clock on a different edge in your design.

The scan architecture is prevented from putting that segment in a chain with segments triggered by a different edge of the same clock and causing scan shift violations.

WHAT NEXT

No action is required on your part.

However, to avoid this warning message, specify no edge mixing or no clock mixing in your scan configuration.

SEE ALSO

check_dft (2), **insert_dft** (2), **preview_dft** (2), **set_scan_configuration** (2).

TEST-1024 (warning) Flop '%s' specified in set_scan_replacement is not valid for the corresponding methodology.

DESCRIPTION

You receive this warning message, when the flop you specified thru **set_scan_replacement** for a given methodology is not valid for the methodology. This won't stop the scan replacement and the tool tries to find a valid scan replacment by other methods.

WHAT NEXT

Specify a valid scan flop for the options of set_scan_replacement.

SEE ALSO

set_scan_replacement(2).

TEST-1025 (warning) No vectors are allowed between the forcePI and measurePO cycles in the %s procedure.

DESCRIPTION

You receive this warning message because vectors in the CTL model and/or the test protocol are between the forcePI and measurePO cycles. This will not stop or invalidate the post insert_dft DRC. This warning can be ignored in case of PLL flows when the reference clocks are expected to pulse during the capture procedures.

WHAT NEXT

Analyze the CTL model or the test protocol to check what vectors are between forcePI and measurePO cycles. In PLL flow, the reference clocks are pulsed during the F cycle of the capture procedure.

SEE ALSO

set_dft_clock_controller(2).

TEST-1026 (warning) elements are supplied by different voltages.

DESCRIPTION

You receive this warning message because you used the **set_scan_configuration** command with the **-voltage_mixing** option to direct the DFT Compiler not to mix elements that are supplied by different voltages on the same scan chain or wrapper chain and you have violated this directive. This occurs because you can still specify scan segments, scan chains, and wrapper chains or build subdesign chains that violate the directive. The DFT Compiler then generates this warning message.

WHAT NEXT

If you intend for the identified segments or chains to violate your directive, no action is required on your part. Otherwise, respecify the segments or chains as necessary.

SEE ALSO

set_scan_configuration (2).

TEST-1027 (Error) Scan compression requires serial signals to be routed

DESCRIPTION

You cannot insert scan compression logic without routing serial signals

WHAT NEXT

Set the signals to be routed by **set_scan_configuration** or **set_dft_insertion_configuration** (dcxg mode), and run **insert_dftFP again.**

SEE ALSO

set_scan_configuration and insert_dft

TEST-1028 (error) Scan output of chain %s could not be traced.

DESCRIPTION

You receive this message if your design contains combinational logic other than buffers and inverters in a scan path between the last scan flip-flop and the scan output port. The scan chain reordering using third party place and route tools does not support combinational logic between scan paths.

WHAT NEXT

Modify your design so that it does not contain combinational logic between the last flop and the scan output port.

TEST-1029 (warning) scan elements are supplied in different power domains.

DESCRIPTION

You receive this warning message because you instructed DFT Compiler not to mix scan

cells across different power domains, and at the same time you are trying to violate that specification.

This situation occurs when you specify scan groups, scan paths, and wrapper chains or build subdesign scan chains that have scan cells already mixed across different power domains.

WHAT NEXT

To avoid getting this message, you need to change your specifications or allow power domain mixing by setting the **-power_domain_mixing** option of the **set_scan_configuration** command to true.

SEE ALSO

set_scan_configuration (2).

TEST-1030 (error) Parameter value for reserved parameter '%s' is not specified.

DESCRIPTION

You receive this error message when dft architect tries to create a reserved parameter for a test component without specifying the parameter value. Reserved parameters can't be created if the parameter values are not specified.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1031 (error) Parameter type '%s' is not a valid type for reserved parameter '%s', expected parameter type '%s'.

DESCRIPTION

You receive this error message when dft architect tries to create a reserved parameter of incorrect parameter type. Reserved parameters have predetermined parameter types. If the parameter type is incorrect, the parameter is not created.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1032 (error) Invalid value '%s' specified for reserved parameter '%s', valid values are : '%s'.

DESCRIPTION

You receive this error message when dft architect tries to create a reserved parameter with invalid parameter values. Resreved parameters are not created when incorrect parameter values are specified.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1033 (error) No such %s - %d exists.

DESCRIPTION

You receive this error message when dft architect tries to access an unexisting test object with the specified identifier.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1034 (warning) Parameter by name '%s' already exists in the specified params, ignoring the passed parameter.

DESCRIPTION

You receive this warning message when dft architect tries to add a parameter to a set of parameters that already include the specified parameter.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1035 (warning) Duplicate pin type '%s' found, not adding it to the component type.

DESCRIPTION

You receive this warning message when dft architect tries to create a component type with a set of pin types that has a duplicate pin type.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1036 (error) Component type '%s' already exists.

DESCRIPTION

You receive this error message when dft architect tries to create a component type which already exists.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1037 (warning) Duplicate pin name '%s' found, not adding it to the pin map.

DESCRIPTION

You receive this warning message when dft architect tries to create a pin map with duplicate pin names.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1038 (error) No such component type '%s' exists.

DESCRIPTION

You receive this error message when dft architect tries to access an unexisting component type.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1039 (warning) Specified pin map %d is incompatible with

comp type ’%s’.

DESCRIPTION

You receive this error message when dft architect tries to create a component with incompatible pin map and component type. If the pin names used in a pin map are not described in a component type, they become incompatible.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1040 (error) Component of type ’%s’ already exists in library ’%s’.

DESCRIPTION

You receive this error message when dft architect tries to create a component which already exists in the specified library.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1041 (warning) Parameter ’%s’ doesn’t exists on the component %d.

DESCRIPTION

You receive this warning message when dft architect tries to create a component instance with parameters that doesn’t exist on the instance’s component.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1042 (error) Parameter '%s' type '%s' doesn't match the component parameter type '%s'.

DESCRIPTION

You receive this error message when dft architect tries to add a parameter to a component instance with incompatible parameter type. The type of the component instance's parameter doesn't match that of the component's parameter.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1043 (error) Value of parameter '%s' is unspecified.

DESCRIPTION

You receive this error message when dft architect tries to create a component instance with incomplete parameters.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1044 (error) Legality check for the component instance '%s' of library '%s' failed.

DESCRIPTION

You receive this error message when dft architect tries to create a component instance that has incorrect parameter values. All components used in insert_dft has legal formulas that specify the allowed parameter values for the components. When a component instance is created, the parameter values of the instance are checked to see if they violate the legal values allowed for the component. component instance is not created if the legality check is failed for the component instance.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1045 (error) Component instance '%s' already exists in library '%s'.

DESCRIPTION

You receive this error message when dft architect tries to create a component instance that already exists in then specified library.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1046 (error) Library with name '%s' already exists.

DESCRIPTION

You receive this error message when dft architect tries to create a library that

already exists.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1047 (error) Mapping lib cell '%s' of component instance '%s' failed.

DESCRIPTION

You receive this error message when dft insertion tries to create a mapped lib cell for the specified component instance. Please look at prior messages for information on the reasons for the failure to create a lib cell and map it.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1048 (error) Couldn't find the test model template for component instance '%s'.

DESCRIPTION

You receive this error message when dft architect tries to create a test model for the specified component instance. Test model template may not be found either there is no template available for the specified component instance or due to incomplete DW installation.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2)

TEST-1049 (error) Command estimate_test_coverage is not supported in the current (HSS) flow.

DESCRIPTION

You receive this error message because you are running **estimate_test_coverage** command in hierarchical scan synthesis (HSS) DFT flow. The HSS flow uses test models which are used only for scan synthesis purposes and are insufficient to estimate test coverage. If test coverage estimation is necessary, use regular scan insertion flow.

WHAT NEXT

If test coverage estimation is necessary, use regular scan insertion flow.

SEE ALSO

test_use_test_models (3)

TEST-1050 (warning) IO bound register '%s' is used in a user %s, register is not reused in core wrapping.

DESCRIPTION

DFT Compiler does not allow an IO bound register to be reused in core wrapping if the register is already part of a user segment or user scan chain specification. This warning tells you that the IO register is already used in an earlier **set_scan_path** or **set_scan_segment** command. Core wrapping will add a dedicated wrapper cell for the IO associated with the register.

WHAT NEXT

If the IO bound register should be reused in core wrapping, remove the register from user segment or user scan chain specifications.

TEST-1051 (warning) Shared wrapper cell can't be used for the

port ’%s’, using a dedicated wrapper cell.

DESCRIPTION

DFT Compiler does not allow a shared wrapper cell to be used for wrapping an IO that is not connected to a register. This warning tells you that there is no register connected to the port and user specified a shared wrapper cell to be used for wrapping the port. A dedicated wrapper cell will be used to wrap the port.

WHAT NEXT

If the register for the port is missing, add the register and rerun the tool again.

TEST-1052 (warning) Pin ’%s’ of IO register ’%s’ is of unknown type, not reusing the IO register in wrapper chains.

DESCRIPTION

DFT Compiler does not allow an IO bound register to be reused in core wrapping if the type of a pin of the register is unknown. This warning tells you that the type of the pin is unknown. A dedicated wrapper cell will be used to wrap the associated port of the design.

WHAT NEXT

Add any missing pin attributes that are making the tool not understand the pin functionality.

TEST-1053 (warning) %s pin missing for IO register ’%s’, not reusing the IO register in wrapper chains.

DESCRIPTION

DFT Compiler does not allow an IO bound register to be reused in core wrapping if the the required pins are missing from the register. This warning tells you that the specified type of pin is missing on the register. A dedicated wrapper cell will be used to wrap the associated port of the design.

WHAT NEXT

Check if the specified type of pin is missing for the register.

TEST-1054 (warning) IO register '%s' is shared between %s %s%s, using dedicated wrapper cell to wrap the output port%s.

DESCRIPTION

DFT Compiler does not allow a shared wrapper cell to be shared between multiple ports. This warning tells you that there is a valid IO register that is connected to multiple ports. A dedicated wrapper cell will be used to wrap the port.

WHAT NEXT

If the IO register is connected to multiple ports, specify the register to be reused for only one port to avoid the warning message.

SEE ALSO

set_core_wrapper_configuration (2), **set_core_wrapper_cell** (2)

TEST-1055 (warning) IO register '%s' associated with port '%s' can't be swapped with a shared wrapper cell, adding a dedicated wrapper cell to wrap the port.

DESCRIPTION

DFT Compiler does not allow an IO register to be swapped with a shared wrapper cell, if the register is constrained with test hold constraints. This warning tells you that the IO register is not valid for swapping with a shared wrapper cell. A dedicated wrapper cell will be used to wrap the port.

WHAT NEXT

Check if the IO register has test hold constraints. If dedciated wrapper cell is not desirable, specify that in place implementation of shared wrapper cell is needed for the port with the IO register.

SEE ALSO

set_core_wrapper_configuration (2), **set_core_wrapper_cell** (2)

TEST-1056 (warning) Scan Enable pin of IO register '%s' is functionally connected, not reusing the register in wrapping the

port '%s'

DESCRIPTION

DFT Compiler does not allow an IO register with functional connections to be used in wrapping a port. This warning tells you that the IO register is functionally used in the design. The IO register is not reused in wrapping the associated port.

WHAT NEXT

Check if the scan enable pin of IO register is connected to functional logic. If so, specify that a dedicated wrapper cell to be added for the associated port if there is only one IO register connected to the port to avoid the warning.

SEE ALSO

set_core_wrapper_configuration (2), **set_core_wrapper_cell** (2)

TEST-1057 (warning) More than one data_in pins found for IO bound register '%s', not reusing the register for wrapping the port '%s'

DESCRIPTION

DFT Compiler does not allow an IO register with multiple data in pins to be used for wrapping a port. This warning tells you that the IO register has multiple data in pins. The IO register is not reused in wrapping the associated port.

WHAT NEXT

Check if there are multiple data in pins to the specified IO register. If there are multiple data in pins, see if the pins can be constrained such that only one pin is active and is connected an IO for DFT Compiler to reuse the IO register in wrapping the associated port.

SEE ALSO

set_core_wrapper_configuration (2), **set_core_wrapper_cell** (2)

TEST-1058 (warning) No data_in pin found for IO bound register

'%s', not reusing the register for wrapping the port '%s'

DESCRIPTION

DFT Compiler does not allow an IO register that doesn't have an active data in pin to be used for wrapping a port. This warning tells you that the IO register data in pin(s) are tied to constant drivers or constrained to constant signals. The IO register is not reused in wrapping the associated port.

WHAT NEXT

Check if the data in pins of the specified IO register are tied off to constant signals or constrained to constant signals. If so, check if constraints can be relaxed so that there is an active data in pin of the register connected to an IO of the design so that DFT Compiler can reuse the register in wrapping the associated port.

SEE ALSO

set_core_wrapper_configuration (2), **set_core_wrapper_cell** (2)

TEST-1059 (warning) More than %s (%d) %s pins found on IO register '%s', not reusing the register for wrapping the port '%s'

DESCRIPTION

DFT Compiler does not allow an IO register with more than the normal number of allowed pins to be reused in wrapping a port. This warning tells you that there are more pins than required on the IO register. The IO register is not reused in wrapping the associated port.

WHAT NEXT

To avoid the warning specify that a dedicated wrapper cell to be used to wrap the associcated port.

SEE ALSO

set_core_wrapper_configuration (2), **set_core_wrapper_cell** (2)

TEST-1060 (warning) Port '%s' is connected to %d input

register%s%s%s, IO register%s not used to wrap the port.

DESCRIPTION

DFT Compiler does not allow an IO register to be uresued in wrapping the associated input port, if the port is connected to multiple IO registers or connected to other logic in addition to IO register. This warning tells you that the specified IO is connected to an IO register and also fans out other registers or otyher logic. A dedicated wrapper cell will be used to wrap the port.

WHAT NEXT

To avoid the warning, specify that a dedicated wrapper cell need to be used to wrap the port.

SEE ALSO

set_core_wrapper_configuration (2), **set_core_wrapper_cell** (2)

TEST-1061 (warning) Creating a shared wrapper cell for port '%s' is not successfull, using a dedicated wrapper cell to wrap the port.

DESCRIPTION

DFT Compiler is not able to create a shared wrapper cell successfully for the specified port. This warning tells you that the tool is not able to create a shared wrapper cell. A dedicated wrapper cell will be added to wrap the associated port.

WHAT NEXT

Check if the IO register connected to the port is a complex register.

SEE ALSO

set_core_wrapper_configuration (2), **set_core_wrapper_cell** (2)

TEST-1062 (warning) Reduced %s port to %s : %s.

DESCRIPTION

This warning message informs you that the core wrapper architect detected that the bidirectional/tri-state port is reduced. If a bidirectional port is reduced to two-state output, only output wrapper cell is added to the port. If a bidirection port is reduced to input, only input wrapper cell is added to the port. If a tri-state port is reduced to two-state output, only output wrapper cell is added to the port.

WHAT NEXT

Check if any test hold constraints or constant logic is causing the reduction of bidirectional/tri-state ports. If this is the intended behavior, no action is required from the user.

SEE ALSO

set_dft_configuration (2), **set_core_wrapper_cell** (2), **set_core_wrapper_configuration** (2).

TEST-1063 (warning) Can’t use WC_S1_S cell for the port ’%s’, using a WC_S1 cell instead, safe logic will be implemented outside the wrapper cell.

"

DESCRIPTION

This warning message informs you that the core wrapper architect detected an IO register attached to an output port which also fans out to other functional logic. Allowing a shared wraper cell with builtin safe logic will affect the test coverage as the safe values driven out of the cell affect functional logic during Internal test of the core. Core wrapper uses a shared wrapper cell without builtin safe logic to wrap such ports. The safe logic will be implmented outside the wrapper cell and placed just before the port so that functional logic is not affected by the safe values driven out of the safe logic.

WHAT NEXT

No action is required from the user.

SEE ALSO

set_dft_configuration (2), **set_core_wrapper_cell** (2), **set_core_wrapper_configuration**

(2).

TEST-1064 (warning) IO register '%s' is dont_scan, the register is not used to wrap the port.

DESCRIPTION

DFT Compiler does not allow an IO register to be uresued in wrapping the associated input port, if the register has a dont_scan attribute.

WHAT NEXT

If the register needs to be used to wrap the associated port, remove the dont_scan attribute from the register.

SEE ALSO

set_core_wrapper_configuration (2), **set_core_wrapper_cell** (2)

TEST-1065 (warning) IO register '%s' is dont_touch, the register is not used to wrap the port.

DESCRIPTION

DFT Compiler does not allow an IO register to be uresued in wrapping the associated input port, if the register has a dont_touch attribute.

WHAT NEXT

If the register needs to be used to wrap the associated port, remove the dont_touch attribute from the register.

SEE ALSO

set_core_wrapper_configuration (2), **set_core_wrapper_cell** (2)

TEST-1066 (warning) IO register '%s' is violated by drc, the

register is not used to wrap the port.

DESCRIPTION

DFT Compiler does not allow an IO register to be uresued in wrapping the associated input port, if the register is violated by drc.

WHAT NEXT

If the register needs to be used to wrap the associated port, fix the drc violation with the register.

SEE ALSO

set_core_wrapper_configuration (2), **set_core_wrapper_cell** (2)

TEST-1067 (warning) IO register '%s' is part of a multi-bit scan segment, the register is not used to wrap the port.

DESCRIPTION

DFT Compiler does not allow an IO register to be uresued in wrapping the associated input port, if the register is part of a scan segment of size greater than 1.

WHAT NEXT

If the register needs to be used to wrap the associated port, remove the register from the multi-bit segment specification.

SEE ALSO

set_core_wrapper_configuration (2), **set_core_wrapper_cell** (2)

TEST-1068 (warning) IO register '%s' is part of an unknown segment, the register is not used to wrap the port.

DESCRIPTION

DFT Compiler does not allow an IO register to be uresued in wrapping the associated input port, if the register is part of a scan segment which is not a single bit scan or inferred segment.

WHAT NEXT

Check if the register is part of a structured segment, remove the register from any scan segment specification.

SEE ALSO

set_core_wrapper_configuration (2), **set_core_wrapper_cell** (2)

TEST-1069 (error) Can’t Synthesize Wrapper Cell, turning off dft insertion.

DESCRIPTION

This error message tells you that the core wrapper insertion couldn’t synthesize wrapper cells. Wrapper insertion can’t proceed without synthesizing wrapper cells. DFT insertion will be turned off.

WHAT NEXT

Check if link library is setup properly to include the design ware libraries dw04.sldb or dw_foundation.sldb used in mapping the wrapper cells. Check if there are any errors issued during mapping wrapper cells.

SEE ALSO

insert_dft (2)

TEST-1070 (warning) Test Model of core instance ’%s’ is not valid for integration, not creating any top level test modes to test the core.

DESCRIPTION

The system-on-chip (SoC) BIST does not allow integration of unencapsulated cores during core integration. This warning message occurs when a specified core instance of the current design is not encapsulated or not encapsulated properly, so no top level test modes are created during core integration to test the core instance.

WHAT NEXT

This is a warning message only. No action is required on your part.

However, to avoid the warning, make sure that only encapsulated cores are present during core integration. An encapsulated core is defined as follows:

- A scan wrapped core
- A dbist encapsulated core
- An xdbist encapsulated core
- An mbist encapsulated core
- A scan wrapped core with mbist logic.

SEE ALSO

create_test_schedule (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1071 (Warning) No domain based scan enable specified for sub-design '%s' in hierarchical scan flow.

DESCRIPTION

You receive this warning message because you did not specify domain based scan enable for the given sub-block, and specified domain based scan enable on the top level. This can create issues for domain based scan enable at top level for preview_dft or insert_dft

WHAT NEXT

Turn on domain based scan enable for sub-blocks using set_scan_configuration -domain_based_scan_enable if you have turned it on at the top level.

SEE ALSO

preview_dft (2), **set_scan_configuration** (2).

TEST-1072 (Warning) Scan enable per domain specified along

with dedicated scan enable for chain’%s’.

DESCRIPTION

You receive this warning message because you specified domain based scan enable and also specified a seperate scan enable for a given chain. This may not give the right results expected.

WHAT NEXT

Remove dedicated scan enable for the scan chain and run the command preview_dft/ insert_dft

SEE ALSO

preview_dft (2), **set_scan_configuration** (2).

TEST-1073 (Error) Fan-out limit ’%d’ specified for pipelining scan enable is less than minimum required ’%d’.

DESCRIPTION

You receive this warning message because you specified a pipeline fanout limit specified for pipelining scan-enable is much less than required for drving all the logic driven by scan-enable port and internal pipeline flops. With a single level of pipelining the fanout should be atleast square root of the no of pins that need to be driven by scan enable.

WHAT NEXT

Increase fan-out limit sufficiently to handle all the logic using set_scan_configuration -pipelining_fanout_limit.

SEE ALSO

preview_dft (2), **preview_scan** (2), **set_scan_configuration** (2).

TEST-1074 (Error) Pipelining Scan enable is not supported with

flow having '%s'.

DESCRIPTION

You receive this warning message because you specified to do pipelining of scan-enable with a mentioned flow. Pipelining scan-enable is supported as of now only for basic scan flow, hss flow with Autofix and bidi fixing.

WHAT NEXT

Change the flow or disable pipelining of scan enables.

SEE ALSO

preview_dft (2), **preview_scan** (2), **set_scan_configuration** (2).

TEST-1075 (Error) Internal pins flow is not supported with lbist, core wrapping, for non multiplexed_flip_flop scan styles and Sequential Compression Post-DFT DRC.

DESCRIPTION

You receive this error message because you specified to use internal pins flow with lbist, core wrapping or with a design with non multiplexed_flip_flop scan style or in Post-DFT DRC after Sequential Compression insertion. Internal pins flow is not supported for either of the clients or scan style mentioned above.

WHAT NEXT

Please use the command **set_dft_configuration** to disable the clients mentioned above, or use the command **set_dft_drc_configuration** to disable the internal pins flow or use the command **set_scan_configuration** to set the scan style to multiplexed_flip_flop.

SEE ALSO

set_dft_configuration (2), **set_dft_drc_configuration** (2), **set_scan_configuration** (2).

TEST-1076 (Warning) The specification for the hookup signal

%s specified before will be overwritten.

DESCRIPTION

You receive this warning message because you specified a hookup signal which has been specified before as a hookup for a port or an independent hookup signal. The existing hookup signal specification will be overwritten with the new specification.

WHAT NEXT

Please use the command **remove_dft_signal** to remove the existing specification and use the command **set_dft_signal** to give new specifications.

SEE ALSO

set_dft_signal (2), **remove_dft_signal** (2), **set_dft_drc_configuration** (2).

TEST-1077 (Error) Post-insertion DFT DRC is not supported in this mode.

DESCRIPTION

Post insertion **dft_drc** is an optional step to validate scan_chains inserted by **insert_dft**. You receive this error message because you specified to run **dft_drc** after insertion in one of the following unsupported scenarios.

1) In ScanCompression mode when internal pins flow is enabled and Internal pins of type ScanDataIn, ScanDataOut and TestMode are used.

2) In Multimode when internal pins flow is enabled and Internal pins of type ScanDataIn, ScanDataOut and TestMode are used.

3) In ScanCompression mode when hybrid or integration is enabled in hierachical adaptive scan flow.

WHAT NEXT

You can write out the netlist and protocol file from DFT Compiler and run DRC in TetraMAX.

You can also use the command **set_dft_drc_configuration** to disable the internal pins flow or use the command **remove_dft_signal** to remove the signals of type scan in, scan out and test mode as internal pins, for the first two scenarios.

SEE ALSO

set_dft_signal (2), **set_dft_drc_configuration** (2), **remove_dft_signal** (2).

TEST-1078 (warning) Scan core segment %s has no element.

DESCRIPTION

You receive this message if **preview_dft** or **insert_dft** finds that the specified core segment has no element defined.

WHAT NEXT

If you receive this message, check the CTL model attached to your sub-design.

SEE ALSO

read_test_model (2), **use_test_model** (2),

TEST-1079 (Warning) Chain %s has both X and Non-X cells.

DESCRIPTION

You receive this message if you have specified a scan path with a mix of X and Non-X cells, using **set_scan_path** command. The scan chain will not be considered as X chain.

WHAT NEXT

If the scan chain not being considered as a X chain is acceptable, no action is required on your part. Otherwise redefine a scan path with only X cells to be considered as X chain.

SEE ALSO

set_scan_path (2),

TEST-1080 (error) The sum of strobe time (%10.2f) (specified with test_bsd_default_strobe) and strobe width value (%10.2f) (specified with test_bsd_default_strobe_width) is required to be

less than period value (%10.2f) (specified with test_default_period).

DESCRIPTION

You have specified a strobe time and strobe width value such that the end of the strobe period stretches beyond the period.

The following variables are used to set the timing for BSD.

test_default_period test_bsd_default_delay test_bsd_default_bidir_delay test_bsd_default_strobe test_bsd_default_strobe_width

WHAT NEXT

Check your strobe time specifications.

TEST-1081 (error) %s time (%10.2f) (specified with test_bsd_default_delay or test_bsd_default_bidir_delay) must be less than strobe time (%10.2f) (specified with test_bsd_default_strobe).

DESCRIPTION

Data application time/delay must happen before strobe time.

The following variables are used to set the timing for BSD.

test_default_period test_bsd_default_delay test_bsd_default_bidir_delay test_bsd_default_strobe test_bsd_default_strobe_width

WHAT NEXT

Change strobe time, and/or delay or bidirectional delay time such that data application time happens before strobe time, and rerun create_bsd_patterns. To set the strobe time use the test_bsd_default_strobe variable, and to set the bidirectional delay time use the test_bsd_default_bidir_delay variable.

TEST-1082 (error) %s time (%1f) (specified with test_bsd_default_delay or test_bsd_default_bidir_delay) must

be less than period (%1f) (specified with test_default_period).

DESCRIPTION

You have specified input or bidir delay time beyond the period.

The following variables are used to set the timing for BSD.

test_default_period test_bsd_default_delay test_bsd_default_bidir_delay
test_bsd_default_strobe test_bsd_default_strobe_width

WHAT NEXT

Check your input or bidir delay time specifications.

TEST-1083 (error) %s time (%10.2f) (specified with test_bsd_default_delay or test_bsd_default_bidir_delay) must be less than %s (%10.2f).

DESCRIPTION

Data application time/delay must happen before strobe time.

WHAT NEXT

Change strobe time, and/or delay or bidirectional delay time such that data application time happens before strobe time, and rerun create_bsd_patterns.

The following variables are used to set the timing for BSD.

test_default_period test_bsd_default_delay test_bsd_default_bidir_delay
test_bsd_default_strobe test_bsd_default_strobe_width

SEE ALSO

create_test_clock (2), **test_bsd_default_delay** (3), **test_bsd_default_bidir_delay** (3), **test_bsd_default_strobe** (3)

TEST-1084 (error) %s time (%10.2f) must be less than %s

(%10.2f) (specified with test_bsd_default_strobe).

DESCRIPTION

Data application time/delay must happen before strobe time.

WHAT NEXT

Change strobe time, and/or delay or bidirectional delay time such that data application time happens before strobe time, and rerun create_bsd_patterns.

The following variables are used to set the timing for BSD.

test_default_period test_bsd_default_delay test_bsd_default_bidir_delay test_bsd_default_strobe test_bsd_default_strobe_width

SEE ALSO

create_test_clock (2), **test_bsd_default_delay** (3), **test_bsd_default_bidir_delay** (3), **test_bsd_default_strobe** (3)

TEST-1085 (warning) Bidir delay (%10.2f) (specified with test_bsd_default_bidir_delay) must be less than strobe time (%10.2f) (specified with test_bsd_default_strobe), setting bidir delay to input delay (%10.2f) (specified with test_bsd_default_delay).

DESCRIPTION

You have specified bidirectional delay time greater than the strobe time. Bidurectional delay time is reset to input delay time.

The following variables are used to set the timing for BSD.

test_default_period test_bsd_default_delay test_bsd_default_bidir_delay test_bsd_default_strobe test_bsd_default_strobe_width

WHAT NEXT

Check your test_bsd_default_strobe and test_bsd_default_bidir_delay variables.

SH SEE ALSO **create_bsd_patterns** (2), **test_bsd_default_bidir_delay** (3).

TEST-1086 (warning) Bidir delay (%10.2f) (specified with test_bsd_default_bidir_delay) must be less than period (%10.2f) (specified with test_default_period), setting bidir delay to input delay (%10.2f) (specified with test_bsd_default_delay).

DESCRIPTION

You have specified bidirectional delay time greater than the period. Bidurectional delay time is reset to input delay time.

The following variables are used to set the timing for BSD.

test_default_period test_bsd_default_delay test_bsd_default_bidir_delay test_bsd_default_strobe test_bsd_default_strobe_width

WHAT NEXT

Check your test_default_period and test_bsd_default_bidir_delay variables.

SH SEE ALSO **create_bsd_patterns** (2), **test_bsd_default_bidir_delay** (3).

TEST-1087 (warning) Bidir delay (%10.2f) (specified with test_bsd_default_bidir_delay) must be less than TCK rise time (%10.2f), setting bidir delay to input delay (%10.2f) (specified with test_bsd_default_delay).

DESCRIPTION

You have specified bidirectional delay time greater than the TCK rise time. Bidurectional delay time is reset to input delay time.

The following variables are used to set the timing for BSD.

test_default_period test_bsd_default_delay test_bsd_default_bidir_delay test_bsd_default_strobe test_bsd_default_strobe_width

WHAT NEXT

Check your test_bsd_default_bidir_delay variable and rise time of TCK.

SH SEE ALSO **create_bsd_patterns** (2), **test_bsd_default_bidir_delay** (3).

TEST-1088 (Warning) Static X chain isolation is ignored in %s as high xtolerance is not enabled.

DESCRIPTION

You receive this message if you have specified static X chain isolation without high xtolerance in a Scan Compression mode, using **set_scan_compression_configuration** command. Static X Chain isolation will be ignored for this mode.

WHAT NEXT

Enable high xtolerance if you would like the static X chains to be isolated in the Scan Compression mode.

SEE ALSO

set_scan_compression_configuration (2),

TEST-1089 (warning) User defined '%s' is ignored for bsd synthesis.

DESCRIPTION

This message is issued when you have specified a Tap using define_dft_design command and not specified bsd_use_old_tap variable appropriately.

Dft design of type TAP is used to specify old Tap. Dft design of type TAP_UC is used to specify new Tap.

Old Tap is used in bsd synthesis only when the variable bsd_use_old_tap is set to TRUE. New Tap is used in bsd synthesis only when the variable bsd_use_old_tap is set to FALSE(default).

WHAT NEXT

Make sure that when old Tap is specified, the variable bsd_use_old_tap is set to TRUE. Make sure that when new Tap is specified, either the variable bsd_use_old_tap is not specified or set to FALSE.

SH SEE ALSO **insert_dft** (2), **define_dft_design** (2).

TEST-1090 (Error) Too many X cells in design. Cannot isolate

static X cells as seperate X chains.

DESCRIPTION

You receive this message if you have specified static X chain isolation in a Scan Compression mode and more than 20% of valid scan cells have static X (D39) violations.

WHAT NEXT

You could either disable static X isolation or reduce the number of D39 violations.

SEE ALSO

set_scan_compression_configuration (2),

TEST-1091 (Error) Test mode %s cannot be removed after DFT insertion.

DESCRIPTION

You receive this message if you are removing a test mode after DFT insertion.

WHAT NEXT

You cannot remove a test mode in post-DFT insertion.

SEE ALSO

define_test_mode (2).

TEST-1092 (Error) Sequential Compression cannot be generated with the current scan and sccomp configuration.

DESCRIPTION

You receive this message because the current scan configuration and scan compression configuration do not allow a correct implementation of the Sequential compression.

WHAT NEXT

You should change the chain_count in scan configuration or in scan compression configuration.

SEE ALSO

set_scan_configuration (2), **set_scan_compression_configuration** (2),

TEST-1093 (error) Size of the Deserializer and Serializer are not equal.

DESCRIPTION

This error message occurs when different sizes are specified for the Serializer and Deserializer. The Deserializer and Serializer size is specified using the **-inputs** and **-outputs** options of the **set_scan_compression_configuration** command, respectively.

WHAT NEXT

Change the **-inputs** and **-outputs** specification in **set_scan_compression_configuration** to be equal.

SEE ALSO

set_scan_compression_configuration(2)

TEST-1094 (error) The number of Deserializer inputs and Serializer outputs are not equal.

DESCRIPTION

This error message occurs when the specified number of inputs and outputs for the Deserializer and Serializer, respectively, are different. The number of Deserializer inputs and Serializer outputs are specified using the **-inputs** and **-outputs** options of the **set_serialize_configuration** command.

WHAT NEXT

Change the **-inputs** and **-outputs** specification in **set_serialize_configuration** to be equal.

SEE ALSO

set_serialize_configuration(2)

TEST-1095 (error) Scan compression mode chains that are outside the CODEC, are not supported in the Serializer flow.

DESCRIPTION

This error message occurs when there are scan chains outside the CODEC in a scan compression mode with Serializers. Non-CODEC chains are not supported in the Serializer flow.

WHAT NEXT

Disable the Serializer for that mode using the **set_scan_compression_configuration** command. If you have defined the scan chain with the **set_scan_path** command, you can remove the **-scan_data_in** or **-scan_data_out** specification, or remove the scan path specification using the **remove_scan_path** command.

SEE ALSO

remove_scan_path(2)
set_scan_compression_configuration(2)
set_scan_path(2)

TEST-1096 (error) The head and tail pipeline flip-flops are not triggered by the same clock in the Serializer flow.

DESCRIPTION

This error message occurs when there are head and tail pipeline flip-flops that are triggered by different clocks in the Serializer flow. This is not supported.

WHAT NEXT

You can either reassign the same clock for the head and tail pipeline flip-flops using the **set_pipeline_scan_data_configuration** command, or disable Serializer using the **set_scan_compression_configuration** command.

SEE ALSO

set_pipeline_scan_data_configuration(2)
set_scan_compression_configuration(2)

TEST-1097 (error) Pipeline clock is not dedicated to pipeline flip-flops in the Serializer flow.

DESCRIPTION

This error message occurs when there are head and tail pipeline flip-flops that are triggered by a clock that also triggers a scan flip-flop in the Serializer flow. A non-dedicated pipeline clock is not supported in the Serializer flow.

WHAT NEXT

You can either create a dedicated pipeline clock and assign it to head and tail pipeline flip-flops using the **set_pipeline_scan_data_configuration** command, or disable the Serializer using the **set_scan_compression_configuration** command.

SEE ALSO

set_scan_compression_configuration(2)
set_pipeline_scan_data_configuration(2)

TEST-1098 (error) Chain count cannot be determined with the specified number of inputs or outputs in %s mode.

DESCRIPTION

This error message occurs when the number of scan inputs or scan outputs specified for the compression mode exceeds the number of scan chains in the base scan mode and the chain count cannot be determined.

WHAT NEXT

You can specify the chain count or maximum length for the compression mode to avoid this error. You can also reduce the number of scan inputs or scan outputs to be less than the number of base scan mode chains. Use the **set_scan_compression_configuration** command with the **-chain_count**, **-max_length**, **-inputs**, and **-outputs** options.

SEE ALSO

set_scan_compression_configuration(2)

TEST-1099 (error) Clock chains that are outside the CODEC are

not supported in Sequential Compression.

DESCRIPTION

This error message occurs when you specify a dedicated clock chain in Sequential Compression flow. The clock chains must be inside the compressor and the decompressor in the Sequential compression flow.

WHAT NEXT

If you have defined the scan chain with the **set_scan_path** command, you can remove the **-scan_data_in** or **-scan_data_out** specification, or specify a test mode that is different from the scan compression mode using the **-test_mode** option, or remove the scan path specification using the **remove_scan_path** command. Also check that the **test_occ_sccomp_old_architecture** environment variable is set to FALSE (default value).

SEE ALSO

remove_scan_path(2)
set_scan_compression_configuration(2)
set_scan_path(2)

TEST-1100 (error) Cannot architect compressor with %d inputs and %d outputs.

DESCRIPTION

This error message occurs when the compressor cannot be architected with the given set of parameters.

WHAT NEXT

You can specify a different chain count or maximum length for the compression mode to avoid this error. You can also change the number of scan inputs or scan outputs for the compression mode. Use the **set_scan_compression_configuration** command with the **-chain_count**, **-max_length**, **-inputs**, and **-outputs** options.

SEE ALSO

set_scan_compression_configuration(2)

TEST-1110 (information) Values at the TDO port pad pins: %s.

DESCRIPTION

You receive this information message because the values of the TDO port pad pins helps you to determine the reason why the TDO drive is not enabled. The symbolic values and descriptions of the TDO port pad pins are as follows:

```
 0 - logic zero value
 1 - logic one value
 X - unknown value
 Z - high impedance
Di - valid input data
Do - valid output data
```

WHAT NEXT

Correct the design using this diagnostic information and rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1110a (information) This problem occurred because pad cell is missing at the TDO port %s.

DESCRIPTION

You receive this information message because a pad cell at the TDO port is missing, so the TDO driver is not enabled, or a break in the shift register chain is due.

WHAT NEXT

Correct the design using this diagnostic information and then rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1111 (information) Values at the flop %s pins: %s.

DESCRIPTION

You receive this diagnostic information message showing the values at the pins of the shift flip-flop, to help you find the cause of a break in the shift register chain. The symbolic values and their descriptions are as follows:

```
 0  - logic zero value
 1  - logic one  value
 X  - unknown value
 Z  - high impedance
Di - valid input data
Do - valid output data
```

WHAT NEXT

This is an informational message only. No action is required on your part.

However, you can correct the design and rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1112 (information) Break in shift register chain at %s is caused by pin %s of flop %s driving pin %s of flop %s with an unknown value 'X'.

DESCRIPTION

You receive this information message when diagnosing the the cause of a break in the shift register chain.

WHAT NEXT

This is an informational message only. No action is required on your part.

However, you can correct the design and rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1113 (information) Break in shift register chain at %s is caused by a feedback loop from cell %s.

DESCRIPTION

You receive this information message when the cause of a break in a shift register chain is diagnosed as a feedback loop from a specific cell.

WHAT NEXT

This is an informational message only. No action is required on your part.

However, you can correct the design by removing and and rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1114 (information) TDO port %s is driven by the shift flop %s.

DESCRIPTION

You receive this information message when diagnosing the cause of inversion in the shift register chain.

WHAT NEXT

This is an informational message only. No action is required on your part.

However, you can correct the design and rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1115 (information) Data is inverted between TDI and TDO at the following cell(s):

DESCRIPTION

You receive this information message when the cause of inversion in the shift register chain is diagnosed as inverted data between TDI and TDO.

WHAT NEXT

This is an informational message only. No action is required on your part.

However, you can correct the design and rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1116 (information) This problem occured because BSR cell %s connected to the port does not capture the port data.

DESCRIPTION

You receive this information message when the cause of a missing input BSR cell is diagnosed as a probale BSR cell at the port which is not being able to capture the port data when EXTEST instruction is active. As per section 8.8 of the IEEE 1149.1 std. an input BSR cell should capture the sensed port data in the Capture-DR TAP Controller state for the EXTEST instruction.

WHAT NEXT

If the BSR cell shown in the message is intended to be the input BSR cell at the port, examine the circuit between the input port and the BSR cell and make sure that the path from the port to the BSR cell shift flop is enabled and clocked correctly under the above condition.

Correct the design and rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1117 (information) Shift Register cells selected between

TDI and TDO by the "all-ones" opcode are: %s.

DESCRIPTION

You receive this information as diagnostic information showing the shift register cells selected between TDI and TDO, when the "all-ones" opcode selects a register of length more than one.

WHAT NEXT

Use this diagnostic information to debug why the all-ones opcode select the displayed cells instead of 1-bit BYPASS register between TDI and TDO.

Correct the design and rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1118 (information) This problem occured because BSR cell %s connected to the port does not drive the port.

DESCRIPTION

You receive this information message when the cause of a missing output BSR cell is diagnosed as a probale BSR cell at the port which is not being able to drive the port when EXTEST instruction is active. As per section 8.8 of the IEEE 1149.1 std. an output BSR cell should drive the port data during the EXTEST instruction.

WHAT NEXT

If the BSR cell shown in the message is intended to be the output BSR cell at the port, examine the circuit between the BSR cell update flop and the ouput port and make sure that the path is enabled under the above condition. Check that the mode signal for the output mux select has the correct logic.

Correct the design and rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1119 (Error) This command works only when Stitch Only

option is enabled. Use set_dft_optimization_configuration -none to enable Stitch Only option.

DESCRIPTION

You receive this error message because the command typed can be used only with stitch only option. The stitch only option is enabled first by using the **set_dft_optimization_configuration -none** command.

WHAT NEXT

No action is required on your part.

SEE ALSO

set_dft_optimization_configuration (2), **insert_scan** (2),

TEST-1121 (information) Input BSR cell at bidirectional port %s is not detected because control BSR cell is missing at the output side of the port %s.

DESCRIPTION

You receive this information message when the input BSR cell is missing at the bidirectional port, because the output side is missing a control BSR.

WHAT NEXT

Correct the design by doing one of the following:

- Insert a control BSR cell at the output side of the port.

- If you intend to use only the input side of the bidirectional port, disable the output side of the port.

Run the **check_bsd** command again.

SEE ALSO

check_bsd (2).

TEST-1122 (information) Input BSR cell is not detected at port %s because the pad is not able to propagate data. Values at the pad pins: %s.

DESCRIPTION

You receive this information message when data is stuck at the input pad, preventing input BSR from capturing the data correctly.

WHAT NEXT

Correct the problem at the input pad and rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1123 (information) Output BSR cell %s connected to port %s is not detected because the pad is not able to propagate data. Values at the pad pins: %s.

DESCRIPTION

You receive this information message when the data coming from the output BSR cell is stuck at the output pad and cannot be captured at the output port.

WHAT NEXT

Correct the problem at the output pad and rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1124 (information) BSR cell %s connected to port %s is not detected because control BSR cell is not found at the port.

DESCRIPTION

You receive this information message because the output BSR cell is missing at the port due to a missing control BSR.

WHAT NEXT

Correct the design by inserting a control BSR cell at the output port and then running the **check_bsd** command again.

SEE ALSO

check_bsd (2).

TEST-1125 (information) Reason for not able to find BSR cell at port %s
is caused by the BSR cell update stage flop %sr:
%s.

DESCRIPTION

You receive this information message as diagnostic for a missing output BSR cell.

WHAT NEXT

Use this diagnostic information to correct the design and then rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1126 (Error) The scan state is invalid for running this

command. The scan state should be scan_existing.

DESCRIPTION

You receive this error message because the scan state should be either **scan_existing** (scan routed) for the **disconnect_scan_chains** command to run. If the current state of the design is not scan existing, this error message prevents disconnect_scan_chains command from proceeding.

WHAT NEXT

Set the scan state using the **set_scan_state** command before using the **disconnect_scan_chains** command.

SEE ALSO

set_dft_optimization_configuration (2), **disconnect_scan_chains** (2), **insert_dft** (2),

TEST-1128 (information) This problem occurred because following port(s) are not driven by their BSR cell shift stage.

DESCRIPTION

You receive this information message as diagnostic for invalid output conditioning on output BSR cells during EXTEST.

WHAT NEXT

Use this diagnostic information to correct the design and then rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1129a (information) Illegal capture descriptor for the BSR cell %s:

DESCRIPTION

You receive this information message as diagnostic for a nonstandard BSR cell or an illegal number of capture descriptors.

The capture descriptors of a BSR cell are a set of triplets showing the behavior of the BSR cell under the standard instructions, and in the following form:

(<BSR Cell Context>, <Capture Instruction>, <Data Source for the value captured in the Cell>)

Refer to Annex B of the supplement to the *IEEE Std 1149.1* for more information on capture descriptors.

WHAT NEXT

Ensure that the BSR cell design is compliant with the *IEEE Std 1149.1*, and that the BSR cell type is appropriate for the instructions you implement.

TEST-1129 (information) Capture descriptor found for the BSR cell %s:

DESCRIPTION

You receive this information message when diagnosing the cause of a nonstandard BSR cell or an invalid number of capture descriptors.

The capture descriptors of a BSR cell are a set of triplets showing the behavior of the BSR cell under the standard instructions, and in the following form:

(<BSR Cell Context>, <Capture Instruction>, <Data Source for the value captured in the Cell>)

Refer to Annex B of the supplement to *IEEE Std 1149.1* for more information on capture descriptors.

WHAT NEXT

Ensure that the BSR cell design is compliant with the *IEEE Std 1149.1* standard and that the BSR cell type is appropriate for the instructions you implement.

TEST-1130 (information) As INTEST instruction is implemented, INPUT BSR cell %s is found to be of type BC_0 instead of BC_4.

DESCRIPTION

You receive this information message as diagnostic for a nonstandard BSR cell. The INTEST instruction is not supported on input by a BSR cell of type BC4.

WHAT NEXT

Use this diagnostic information to correct the design and then rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1131 (information) Specified INTEST instruction is not implemented as BSR cell %s at the output port '%s' is found to be of type BC2.

DESCRIPTION

You receive this information message because an INTEST instruction cannot be implemented when a BSR cell of type BC2 is used on an output port.

This message is the result of the following actions:

- You are executing the **check_bsd** command.

- The **infer_instructions** option of the **set_bsd_configuration** command is set to false, which is the default.

- You specify INTEST instruction on a design having a BSR cell of type BC2 as an output port.

WHAT NEXT

Correct the design by replacing BC2 BSR cell by a BSR cell of type BC1 on the specified output port.

SEE ALSO

check_bsd (2), **set_bsd_configuration** (2).

TEST-1133 (information) Values at the port and BSR cell shift flops:

DESCRIPTION

You receive this information message when as diagnostic for a port that is not driven or captured by the BSR cell.

WHAT NEXT

Use this diagnostic information to correct the design and then rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1134 (warning) Invalid capture value "%s" for %s instruction.

DESCRIPTION

You get this warning when there is an unknown capture value bit in the IDCODE or USERCODE capture value.

WHAT NEXT

Analyze the design for the cpature value bit position.

If a compliance enable pattern is missing in the specifications, then specify the complaince enable pattern using the set_bsd_compliance command and rerun check_bsd.

SEE ALSO

check_bsd (2). **set_bsd_compliance** (2).

TEST-1136 (information) Following update flops reset illegally:%s.

DESCRIPTION

You receive this information message as diagnostic for update flops and their pin values that reset illegally during RUNBIST or CLAMP.

WHAT NEXT

Use this diagnostic information to correct the design and then rerun the **check_bsd** command.

SEE ALSO

check_bsd (2).

TEST-1137 (information) Values on instruction register update flops after synchronous reset %s.

DESCRIPTION

You receive this information message when the values on an instruction register update flip-flop. The values flip-flop after a synchronizing sequence of five 1s is applied on the test mode select (TMS) port of the test access port (TAP). The symbolic values and their descriptions are as follows:

```
0 - logic zero value
1 - logic one  value
X - unknown value
Z - high impedance
Di - valid input data
Do - valid output data
```

WHAT NEXT

This is an informational message only. No action is required on your part.

TEST-1138 (information) Values on instruction register update

flops after asynchronous reset %s.

DESCRIPTION

You receive this information message when the values on an instruction register update flip-flop. This occurs after the asynchronous test logic reset port of the test access port (TAP) is set to 0. The symbolic values and their descriptions are as follows:

```
0  - logic zero value
1  - logic one  value
X  - unknown value
Z  - high impedance
Di - valid input data
Do - valid output data
```

WHAT NEXT

This is an informational message only. No action is required on your part.

TEST-1139 (information) This problem occured because there is no pin which drives the BSR cell's shift flop as well as the BSR cell's primary output when SAMPLE/PRELOAD instruction is loaded.%s

DESCRIPTION

You receive this information message because the primary input of a BSR cell is recognized based upon the cell's behavior under the SAMPLE/PRELOAD instruction, as described in *IEEE Std 1149.1*, section 7.6.

WHAT NEXT

Correct the BSR cell design and rerun the **check_bsd** command. Refer to Chapter 10 of *IEEE Std 1149.1* for guidelines on BSR cell design.

SEE ALSO

check_bsd (2).

TEST-1140 (information) This problem occurred because data

is inverted %s.

DESCRIPTION

This is a diagnostic information about inverting logic between boundary scan cell and a design port. Inversion is considered as a logic. The two consecutive pins are shown between which the data is inverted. Following are the most common design errors leading to this:

1. The port pad inverts the data 2. You are using a differential pad and the attributes "master_complementary_pin", "complementary_pin" & "differential_cell" are NOT correctly set 3. You are using a differential soft macro and the "port" and "port_inverted" signal types are NOT correctly set or are swapped

WHAT NEXT

Correct the design and rerun check_bsd.

SEE ALSO

check_bsd (2).

TEST-1141 (error) Incorrect number of arguments specified for bsr_segment '%s' of pad desgn '%s', Discarding specification.

DESCRIPTION

You receive this error message when you specify incorrect BSR segment spec. BSR segment specs are used to describe a BSR cell embedded in a pad. They are specified with **define_dft_design** command in XG mode and with **set_bsd_pad_design** in DB mode. BSR segment spec. syntax is as follows.

<BSR cell position> <BSR cell type> <BSR cell PI> <BSR cell PO> <BSR cell disable/ safe value> <Position of control BSR cell>

The above error is issued as the BSR spec. doen't contain all the required values.

WHAT NEXT

Reexecute the **define_dft_design** command (XG mode) or **set_bsd_pad_design command (DB mode) and specify a valid BSR segment spec. for the command.**

SEE ALSO

define_dft_design (2). **set_bsd_pad_design** (2).

TEST-1142 (error) Incorrect BSR cell type '%s' specified for pad design '%s' in BSR segment spec, Discarding specification.

DESCRIPTION

You receive this error message when you specify incorrect BSR cell type in BSR segment spec. BSR segment specs are used to describe a BSR cell embedded in a pad. They are specified with **define_dft_design** command in XG mode and with **set_bsd_pad_design** in DB mode. BSR segment spec. syntax is as follows.

<BSR cell position> <BSR cell type> <BSR cell PI> <BSR cell PO> <BSR cell disable/ safe value> <Position of control BSR cell>

Legal values of <BSR cell type> are :

BC0 BC1 BC2 BC3 BC4 BC5 BC6 BC7 BC8 BC9 BC10 AC1 AC2 AC7 AC8 AC9 AC10 ACSelX ACSelU

The above error is issued as the BSR spec. contains an incorrect BSR cell type.

WHAT NEXT

Reexecute the **define_dft_design** command (XG mode) or **set_bsd_pad_design command (DB mode) and specify a valid BSR segment spec. for the command.**

SEE ALSO

define_dft_design (2). **set_bsd_pad_design** (2).

TEST-1143 (error) Incorrect bus format '%s' specified for PI/PO of BSR segment spec of pad design '%s', Discarding specification.

DESCRIPTION

You receive this error message when you specify incorrect bus format for PI/PO in BSR segment spec. BSR segment specs are used to describe a BSR cell embedded in a pad. They are specified with **define_dft_design** command in XG mode and with **set_bsd_pad_design** in DB mode. BSR segment spec. syntax is as follows.

<BSR cell position> <BSR cell type> <BSR cell PI> <BSR cell PO> <BSR cell disable/ safe value> <Position of control BSR cell>

Bus format for PI/PO pins are as follows.

<name_of_bus_pin>[<start_index>:<end_index>]

The above error is issued as the BSR spec. contains an incorrect bus pin.

WHAT NEXT

Reexecute the **define_dft_design** command (XG mode) or **set_bsd_pad_design command (DB mode) and specify a valid BSR segment spec. for the command.**

SEE ALSO

define_dft_design (2). **set_bsd_pad_design** (2).

TEST-1144 (error) Incorrect disable value '%s' specified for a BSR segment spec of pad design '%s', Discarding specification.

DESCRIPTION

You receive this error message when you specify incorrect disable value in a BSR segment spec. BSR segment specs are used to describe a BSR cell embedded in a pad. They are specified with **define_dft_design** command in XG mode and with **set_bsd_pad_design** in DB mode. BSR segment spec. syntax is as follows.

<BSR cell position> <BSR cell type> <BSR cell PI> <BSR cell PO> <BSR cell disable/ safe value> <Position of control BSR cell>

Legal values for <BSR cell disable/safe value> field are :

0 1 X Z

The above error is issued as the BSR spec. contains an incorrect disable value.

WHAT NEXT

Reexecute the **define_dft_design** command (XG mode) or **set_bsd_pad_design command (DB mode) and specify a valid BSR segment spec. for the command.**

SEE ALSO

define_dft_design (2). **set_bsd_pad_design** (2).

TEST-1145 (error) Incorrect position field '%s' specified for a

BSR segment spec of pad design '%s', Discarding specification.

DESCRIPTION

You receive this error message when you specify incorrect BSR cell position in a BSR segment spec. BSR segment specs are used to describe a BSR cell embedded in a pad. They are specified with **define_dft_design** command in XG mode and with **set_bsd_pad_design** in DB mode. BSR segment spec. syntax is as follows.

<BSR cell position> <BSR cell type> <BSR cell PI> <BSR cell PO> <BSR cell disable/ safe value> <Position of control BSR cell>

Here <BSR cell position> is a decimal integer.

Here <Position of control BSR cell> can be either '-' or a decimal integer pointing to another BSR cell of the pad.

The above error is issued as the BSR spec. contains a non decimal position field.

WHAT NEXT

Reexecute the **define_dft_design** command (XG mode) or **set_bsd_pad_design command (DB mode) and specify a valid BSR segment spec. for the command.**

SEE ALSO

define_dft_design (2). **set_bsd_pad_design** (2).

TEST-1146 (error) Incorrect Control BSR position '%d' specified for a BSR segment spec of pad design '%s', Discarding specification.

DESCRIPTION

You receive this error message when you specify incorrect control BSR cell position in a BSR segment spec. BSR segment specs are used to describe a BSR cell embedded in a pad. They are specified with **define_dft_design** command in XG mode and with **set_bsd_pad_design** in DB mode. BSR segment spec. syntax is as follows.

<BSR cell position> <BSR cell type> <BSR cell PI> <BSR cell PO> <BSR cell disable/ safe value> <Position of control BSR cell>

Here <Position of control BSR cell> can be either '-' or a decimal integer pointing to another BSR cell of the pad.

The above error is issued as the BSR spec. contains an incorrect control BSR cell

position field.

WHAT NEXT

Reexecute the **define_dft_design** command (XG mode) or **set_bsd_pad_design command (DB mode) and specify a valid BSR segment spec. for the command.**

SEE ALSO

define_dft_design (2). **set_bsd_pad_design** (2).

TEST-1147 (error) Missing PO for Control BSR cell of a BSR segment spec of pad design '%s', Discarding specification.

DESCRIPTION

You receive this error message when you specify a control BSR cell with no PO in a BSR segment spec. BSR segment specs are used to describe a BSR cell embedded in a pad. They are specified with **define_dft_design** command in XG mode and with **set_bsd_pad_design** in DB mode. BSR segment spec. syntax is as follows.

<BSR cell position> <BSR cell type> <BSR cell PI> <BSR cell PO> <BSR cell disable/ safe value> <Position of control BSR cell>

The above error is issued as the BSR spec. contains a control BSR cell with no PO.

WHAT NEXT

Reexecute the **define_dft_design** command (XG mode) or **set_bsd_pad_design command (DB mode) and specify a valid BSR segment spec. for the command.**

SEE ALSO

define_dft_design (2). **set_bsd_pad_design** (2).

TEST-1148 (error) Invalid Control BSR cell type '%s' specified for a BSR segment spec of pad design '%s', Discarding specification.

DESCRIPTION

You receive this error message when you specify an incorrect BSR cell type for a

control BSR cell of a BSR segment spec. BSR segment specs are used to describe a BSR cell embedded in a pad. They are specified with **define_dft_design** command in XG mode and with **set_bsd_pad_design** in DB mode. BSR segment spec. syntax is as follows.

<BSR cell position> <BSR cell type> <BSR cell PI> <BSR cell PO> <BSR cell disable/ safe value> <Position of control BSR cell>

A control BSR cell is identified as a BSR cell referenced in another BSR cell spec through <Position of control BSR cell> field.

Only the following BSR cell types are legal for a control BSR cell.

BC1 BC2 AC1 AC2

The above error is issued as the BSR spec. contains an incorrect control BSR cell type.

WHAT NEXT

Reexecute the **define_dft_design** command (XG mode) or **set_bsd_pad_design command (DB mode) and specify a valid BSR segment spec. for the command.**

SEE ALSO

define_dft_design (2). **set_bsd_pad_design** (2).

TEST-1150 (Warning) Scan Chain '%s' can not be optimized due to a MilkyWay corruption.

DESCRIPTION

You get this error when the scan chain datas are not correct. This may be due to a bad scan DEF file.

WHAT NEXT

Review the scan def file generation.

SEE ALSO

write_scan_def(2), place_opt(2), report_scan_chain(2), check_scan_chain(2),

TEST-1151 (warning) Ignoring the variable '%s' to specify IDCODE capture value, use set_bsd_instruction to specify

IDCODE capture value in XG mode.

DESCRIPTION

You receive this error message when you specify IDOCDE capture values using variables test_bsd_manufacturer_id, test_bsd_part_number, test_bsd_version_number. These variables are not used in XG mode to specify IDCODE capture value.

WHAT NEXT

Use **-capture_value** option of command **set_bsd_instruction** to specify IDCODE capture value in XG mode.

SEE ALSO

set_bsd_instruction (2).

TEST-1152 (Warning) The IDCODE instruction has been specified, but capture value has not been set to specify a valid, nonzero manufacturer identity.

DESCRIPTION

You receive this message because you have specified the IDCODE instruction but have not assigned a valid capture value to the instruction.

To synthesize a Device Identification register, BSD Compiler requires a valid, nonzero value for manufacturer id.

WHAT NEXT

Do the following:

Assign an appropriate capture value to IDCODE instruction with manufacturer id other than 0 and 127.

SEE ALSO

insert_dft (2), **preview_dft** (2), **set_bsd_instruction(2).**

TEST-1153 (Error) Pad access pin '%s' is not found in the pad design %s.

DESCRIPTION

You receive this error message because you have not specified a mandatory pad access pin. For all pad designs access pin of type 'port' is mandatory. For differential pads, access pin of type 'port inverted' is also mandatory.

WHAT NEXT

Provide the mandatory pad access pin and rerun **preview_dft** or **insert_dft** command.

SEE ALSO

insert_dft (2), **preview_dft(2), define_dft_design** (2).

TEST-1154 (Warning) Pad access pin '%s' is not required for the pad design %s, the pin is ignored.

DESCRIPTION

You receive this error message because you have specified a pad access pin which is not required for the specified pad design. This pad pin is ignored. For example pad access pin of type 'port inverted' is not required for a non differential pad design.

WHAT NEXT

Eithe correct the pad design specification or ignore this message.

SEE ALSO

insert_dft (2), **preview_dft(2), define_dft_design** (2).

TEST-1155 (warning) Boundary-cell type AC_2 specified for the output port %s cannot be implemented. Ignoring the

specification and using AC_1 type instead.

DESCRIPTION

You receive this warning message when INTEST is implemented and you use the **set_boundary_cell** command to specify AC_2 to be used at an output port.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_dft (2), **preview_dft** (2), **set_boundary_cell(2), set_bsd_instruction(2).**

TEST-1156 (warning) Highz bsd pins are not connected as HIGHZ instruction is not architected.

DESCRIPTION

You receive this warning message when HIGHZ is not implemented and you use the **define_dft_design** command to specify access pins of type **highz** for pad designs.

WHAT NEXT

Specify HIGH instruction if these **highz** pad pins need to be controlled by HIGHZ instruction, otherwise you can ignore the warining message.

SEE ALSO

insert_dft (2), **preview_dft** (2), **set_boundary_cell(2), set_bsd_instruction(2).**

TEST-1157 (error) '%s' is not a port.

DESCRIPTIONi

You receive this error message when your autofix element is not a port regarding the bidirectional type definition.

WHAT NEXT

Find the correct port.

SEE ALSO

set_autofix_element (2).

TEST-1160 (Error) Scan Def File is corrupted.

DESCRIPTION

You get this error when the scan def file you are using while performing the place_opt -reorder_scan" command is not correct.

WHAT NEXT

Review the scan def file generation.

SEE ALSO

write_scan_def(2),

TEST-1161 (Warning) scan flop replacement has to be set at FALSE.

DESCRIPTION

You receive this warning because the "replace" option of the "set_scan_configuration" command is set to TRUE. FALSE value for the option will be considered.

SEE ALSO

set_scan_configuration(2),

TEST-1170 (error) The -num_cpus option (%d) conflicts with the value set with ’set_host_options -max_cores’ (%d). The -num_cpus option is

obsolete and will be removed in a future release. Please use 'set_host_options -max_cores' only.

DESCRIPTION

This error message occurs when you use the **-num_cpus** option to the **insert_dft** command and provide a value that is different than the value that was set with the **set_host_options -max_cores** command. The command cannot proceed. The **-num_cpus** option is obsolete. Use the **set_host_options -max_cores** command to set the number of processor cores to use for parallel execution.

WHAT NEXT

Run the **set_host_options -max_cores** command before running **insert_dft**, and remove the **-num_cpus** option from the **insert_dft** command.

SEE ALSO

insert_dft(2)
set_host_options(2)

TEST-1171 (information) Running insert_dft using a maximum of %d cores.

DESCRIPTION

This information message advises you that the **insert_dft** command is running in multicore mode. You can specify the maximum number of CPU cores to be used with the **set_host_options** command.

WHAT NEXT

This is an information only message. No action is required.

SEE ALSO

insert_dft(2)
set_host_options(2)

TEST-1180 (information) No I/O registers are found for port '%s';

not adding any dedicated wrapper cells to the port.

DESCRIPTION

This informational message occurs during Core Wrapping. DFT Compiler did not find any I/O registers for the specified port. No dedicated wrapper cell is added for the specified port.

WHAT NEXT

This is an information only message. No action is required.

However, if a dedicated wrapper cell is needed for the port, use the **set_boundary_cell** command for the specification.

SEE ALSO

set_boundary_cell(2)
set_wrapper_configuration(2)

TEST-1181 (warning) Multiple clocks are used for I/O registers of port '%s'.

DESCRIPTION

This warning message occurs during Core Wrapping. DFT Compiler found multiple clock domains being used in I/O registers associated with a port. If a dedicated wrapper cell is added to the port, the clock domain most used is used as the clock for the dedicated wrapper cell.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this warning, make sure that all I/O registers of a port use the same clock domain.

SEE ALSO

set_boundary_cell(2)
set_wrapper_configuration(2)

TEST-1182 (information) Using clock '%s_%d_%d' for the

dedicated wrapper cell of port '%s'.

DESCRIPTION

This informational message occurs during Core Wrapping. The message is issued when multiple clock domains are used in I/O registers of the port. The message shows the clock domain used for the dedicated wrapper cell of the port. By default, the clock domain most is used as the clock domain for the dedicated wrapper cell.

WHAT NEXT

This is an information only message. No action is required.

However, if a different clock domain should be used for the dedicated wrapper cell, use the **set_boundary_cell** command for this specification.

SEE ALSO

set_boundary_cell(2)
set_wrapper_configuration(2)

TEST-1183 (warning) Port '%s' is connected to a clock gating cell '%s'; a dedicated wrapper cell is added to the port.

DESCRIPTION

This warning message is occurs during Core Wrapping. DFT Compiler found a clock gating cell in the fan out cone of a port. A dedicated wrapper cell is added to the port.

WHAT NEXT

This is only a warning message. No action is required.

However, if no wrapper cell is needed for the port, use the **set_boundary_cell** command for this specification.

SEE ALSO

set_boundary_cell(2)
set_wrapper_configuration(2)

TEST-1184 (warning) Port '%s' is connected to cell '%s' which

is inside a DFT Model, dedicated wrapper cell is added to the port.

DESCRIPTION

This warning message occurs during Core Wrapping. DFT Compiler found an I/O register of a port inside a DFT Model cell. A dedicated wrapper cell is added to the port.

WHAT NEXT

This is only a warning message. No action is required.

However, if no wrapper cell is needed for the port, use the **set_boundary_cell** command for this specification.

SEE ALSO

set_boundary_cell(2)
set_wrapper_configuration(2)

TEST-1185 (warning) Port '%s' is connected to %d %s registers, which exceeds reuse threshold %d; dedicated wrapper cell is added to the port.

DESCRIPTION

This warning message occurs during Core Wrapping. DFT Compiler found more I/O registers for a port than the reuse threshold limit specified with the following command:

set_wrapper_configuration -class core_wrapper -reuse_threshold <limit>

A dedicated wrapper cell is added to the port.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, you can do one of the following:

• If all I/O registers of the port need to be reused as shared wrapper cells, increase the threshold value.

• If all I/O registers of all ports need to be reused as shared wrapper cells,

specify the threshold as 0, which disables the threshold check and causes the tool to reuse all I/O registers in wrapping.

SEE ALSO

set_boundary_cell(2)
set_wrapper_configuration(2)

TEST-1186 (warning) Port '%s' is connected to %d input registers and %d output registers, which exceeds reuse threshold %d; dedicated wrapper cell is added to the port.

DESCRIPTION

This warning message occurs during Core Wrapping. DFT Compiler found more I/O registers for a port than the reuse threshold limit specified with the following command:

set_wrapper_configuration -class core_wrapper -reuse_threshold <limit>fp

Both input I/O registers and output I/O registers detected for the input port are considered for the threshold check. A dedicated wrapper cell is added to the port.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, you can do one of the following:

• If all I/O registers of the port need to be reused as shared wrapper cells, increase the threshold value.

• If all I/O registers of all ports need to be reused as shared wrapper cells, specify the threshold as 0, which disables the threshold check and causes the tool to reuse all I/O registers in wrapping.

SEE ALSO

set_boundary_cell(2)
set_wrapper_configuration(2)

TEST-1187 (error) Multiple clocks are used for IO Registers of

Port '%s'.

DESCRIPTION

This warning message is seen during Core Wrapping. DFT Compiler found multiple clock domains are used in IO registers associated with a port. This error is seen when the wrapper configuration option '-use_system_clock_for_dedicated_wrp_cells' is set to enable.

WHAT NEXT

To avoid this error, make sure that all IO registers of a port use the same clock domain.

SEE ALSO

set_wrapper_configuration (2), **set_boundary_cell** (2)

TEST-1188 (information) %s wrapper cell is added to the port '%s', the port is connected to hierarchical cell '%s'.

DESCRIPTION

This informational message is seen during Core Wrapping when maximize_reuse option of set_wrapper_configuration command is enabled. DFT Compiler found a port connected to a hierarchical cell and user has specified with set_boundary_cell command that either no wraper cell should be added to such ports or a dedicated wrapper cell should be added to such ports. The tool honors tyhe user specification and issues this informational message when such ports are found.

WHAT NEXT

This is just a information message only and no action is required from the user.

SEE ALSO

set_wrapper_configuration (2), **set_boundary_cell** (2)

TEST-1201 (warning) The bidirectional port '%s' is degenerated.

Please check the test protocol.

DESCRIPTION

This message tells you that the pad associated with a bidirectional port is degenerated. This port does not have bidirectional capabilities, and can only function as an input or an output.

WHAT NEXT

Get the test protocol inferred by DFT Compiler using **write_test_protocol**. Study how it treats the degenerated ports. If it does not treat the port correctly, you need to develop a corrected custom test protocol.

TEST-1202 (warning) The conditioned bidirectional port '%s' is not being forced '%s'. Please check the test protocol.

DESCRIPTION

You can use the **set_scan_bidir** and **set_scan_configuration** commands to control the direction of a bidirectional port in scan shift.

This message tells you that a bidirectional port is turned in a direction opposite to the one specified during scan shift prior to adding disabling logic.

WHAT NEXT

Get the test protocol inferred by DFT Compiler using **write_test_protocol**. Study how it treats the conditioned bidirectional port. If it does not treat it correctly, develop a corrected custom test protocol.

TEST-1203 (error) '%s' is not a valid disable type for the internal tristate net '%s'.

DESCRIPTION

You receive this message if **preview_scan** or **insert_scan** finds an invalid disabling option for an internal tristate net. Valid disabling options are *disable_all*, *enable_one*, or *no_disabling*.

WHAT NEXT

Use the **set_scan_tristate** or **set_scan_configuration** commands to specify a valid disabling option for this internal three-state net and re-issue the **preview_scan** or **insert_scan** command.

SEE ALSO

insert_scan (2), **preview_scan** (2), **set_scan_configuration** (2), **set_scan_tristate** (2).

TEST-1204 (error) '%s' is not an internal or external tristate net.

DESCRIPTION

You receive this message if you execute the **set_scan_tristate** command and specify a net that is not a tristate net, or is a net connected to a bidirectional port. You can use **set_scan_tristate** only on tristate nets.

WHAT NEXT

If the specified net is connected to a bidirectional port, use the **set_scan_bidir** command to specify the bidirectional port conditioning during scan shift. Reexecute **set_scan_tristate** and specify only tristate nets.

SEE ALSO

set_scan_tristate (2).

TEST-1205 (error) Multiple conflicting disabling options found for net.

DESCRIPTION

You receive this error message if you have performed **set_scan_tristate** multiple times on segments of the given net and the disabling options specified for at least two net segments are not the same.

WHAT NEXT

Resolve the conflicting disabling options for the net and reissue **preview_scan** or **insert_scan**.

SEE ALSO

insert_scan (2), **preview_scan** (2) **set_scan_tristate** (2).

TEST-1206 (error) Multiple conflicting bidirectional conditioning specifications found.

DESCRIPTION

You receive this message if you have issued the **set_scan_bidi** command multiple times and specified different conditioning in scan shift for two or more bidirectional ports connected together. "Conditioning" means specifying whether bidirectional ports are to be configured as inputs or outputs, or be left untouched, during scan shift. This message informs you that you have made conflicting specifications to two or more bidirectional ports that are connected together.

WHAT NEXT

Resolve the conflicting specifications and reissue the **preview_scan** or **insert_scan** command.

SEE ALSO

insert_scan (2), **preview_scan** (2) **set_scan_bidi** (2).

TEST-1207 (warning) Tristate net '%s' has some drivers with the **dont_touch** attribute; cannot add disabling logic.

DESCRIPTION

You receive this message if the **insert_scan** or **insert_dft** command detects a tristate net that contains one or more drivers with the **dont_touch** attribute. By default, **insert_scan** and **insert_dft** attempt to disable all drivers on external tristate nets and all but one driver on internal tristate nets, but they cannot disable drivers with the **dont_touch** attribute. Similarly, **insert_scan** and **insert_dft** cannot perform bidirectional port conditioning for a bidirectional port that has one or more drivers with the **dont_touch** attribute.

WHAT NEXT

If it is acceptable to you for the specified net to have no drivers disabled during scan shift, no action is required on your part. Otherwise, remove the **dont_touch** attribute from the drivers on the specified net, and reissue the **insert_scan** or **insert_dft** command.

SEE ALSO

insert_dft (2), **insert_scan** (2), **remove_attribute** (2), **set_dont_touch** (2), **set_scan_bidi** (2), **set_scan_tristate** (2).

TEST-1208 (information) Cells with the **dont_touch** attribute : %s

DESCRIPTION

This informational message lists all hierarchical cells that have the **dont_touch** attribute and also drive a tristate net or a bidirectional port. The **insert_scan** and **insert_dft** commands do not add disabling logic for tristate nets, or conditioning logic to bidirectional ports, if the ports have the **dont_touch** attribute. This message informs you that the cells on this list will not be disabled or conditioned during scan shift.

WHAT NEXT

If it is acceptable to you for tristate nets and bidirectional ports driven by the listed cells to remain enabled during scan shift, no action is required on your part. Otherwise, remove the **dont_touch** attribute from all cells that drive a tristate net or bidirectional port, and reissue the **insert_scan** command.

SEE ALSO

insert_dft (2), **insert_scan** (2), **preview_scan** (2), **remove_attribute** (2), **set_dont_touch** (2) **set_scan_bidi** (2), **set_scan_tristate** (2).

TEST-1209 (warning) Clock %s reaches %d flip-flops but does not control them throughout the cycle.

DESCRIPTION

You receive this warning message because the **rtldrc** command has found flip-flops that are not controlled by the specified clock signal. This warning occurs if the flip-flop clocks are controllable at the beginning of the cycle, but cannot be controlled in the opposite state when the clock pulse is active. This prevents scan insertion using the multiplexed flip-flop scan style.

This violation is only checked if the scan style is set to multiplexed flip-flop. The check is not made for other scan styles.

The violation can be caused by not defining or conditioning clocks before running the **rtldrc** command. The **rtldrc** command does not infer clocks, but depends on the

create_test_clock, **set_signal_type**, and **set_test_hold** commands to define the clocks and condition them to reach their destinations.

If all signal definitions are made correctly before **rtldrc** is run, the warning indicates that there are registers that cannot be controlled by ATPG. If the violation is not corrected, the registers are unscannable and fault coverage is reduced.

WHAT NEXT

No action is required on your part. However, you can determine the cause of the violation and correct the error so that the violated registers are scannable and the fault coverage is increased.

Make the corrections either by using Autofix (refer to the **insert_dft** command man page for details), or by following the procedure below.

1. Ensure that the test clocks are defined using **create_test_clock** command and that they are conditioned using **set_signal_type** and **set_test_hold**.

2. Examine the specified flip-flops to determine why they are not controlled by the clock signal and then fix the violations.

3. As an alternative, select a different scan style.

4. Reexecute the **rtldrc** command.

SEE ALSO

create_test_clock (2), **insert_dft** (2), **preview** (2), **rtldrc** (2), **set_scan_configuration** (2), **set_signal_type** (2), **set_test_hold** (2); **test_default_scan_style** (3).

TEST-1210 (warning) Clock %s reaches %d latches but does not control them throughout the cycle.

DESCRIPTION

You receive this warning message because the **rtldrc** command has found latches that are not controlled by the specified clock signal. The warning occurs if the latch clocks are controllable at the beginning of the cycle, but cannot be controlled in the opposite state when the clock pulse is active. This prevents scan insertion using the multiplexed flip-flop scan style.

The violation is checked with the assumption that the latches should be scanned. This violation is only checked if the scan style is set to multiplexed flip-flop. The check is not made for other scan styles. In addition, the **test_rtldrc_latch_check_style** variable must be set to **scan**.

The warning can be the result of clocks not being defined or conditioned before running the **rtldrc** command. The **rtldrc** command does not infer clocks, but depends on the **create_test_clock**, **set_signal_type**, and **set_test_hold** commands to define the clocks and condition them to reach their destinations.

If all signal definitions are made correctly before **rtldrc** is run, the violation indicates that there are registers that cannot be controlled by ATPG. If the cause of the violation is not fixed, the registers will be unscannable and fault coverage will be reduced.

WHAT NEXT

No action is required on your part. However, you can determine the cause of the violation and correct the error so that the registers are scannable and the fault coverage is increased.

Make the corrections either by using Autofix (refer to the **insert_dft** command man page for details), or by using the following procedure.

1. Ensure that the test clocks are defined using the **create_test_clock** command and that they are conditioned using **set_signal_type** and **set_test_hold**.

2. Examine the specified latches to determine why they are not controlled by the clock signal and then fix the violations.

3. As an alternative, select a different scan style.

4. Reexecute the **rtldrc** command.

SEE ALSO

create_test_clock (2), **insert_dft** (2), **preview** (2), **rtldrc** (2), **set_scan_configuration** (2), **set_signal_type** (2), **set_test_hold** (2); **test_default_scan_style** (3), **test_rtldrc_latch_check_style** (3).

TEST-1211 (warning) Clock %s reaches %d latches but does not hold them transparent at beginning of cycle.

DESCRIPTION

You receive this warning message because the **rtldrc** command has found that the specified clock does not hold the specified latches transparent at the beginning of the cycle. This check is to ensure that a non-scan latch does not introduce sequential behavior into the circuit.

The design is checked with the assumption that the latches should not be scanned. The design is checked for this violation only when the scan style is set to multiplexed flip-flop, unless the **test_rtldrc_latch_check_style** variable is set to **transparent**. The **rtldrc** command checks the design for latch transparency only when

specified.

This violation can be caused by clocks not being defined or conditioned before **rtldrc** is run. The **rtldrc** command does not infer clocks, but depends on the **create_test_clock**, **set_signal_type**, and **set_test_hold** commands to define the clocks and condition them to reach their destinations.

If all signal definitions are made correctly before **rtldrc** is run, this violation indicates that there are registers that cannot be controlled by ATPG. If the violation is not corrected, these registers are hard to control and fault coverage is reduced.

WHAT NEXT

No action is required on your part. However, you can correct this violation as follows:

1. Ensure that the test clocks are defined using the **create_test_clock** command and that they are conditioned using **set_signal_type** and **set_test_hold**.

2. Examine the specified latches to determine why the clock does not hold them transparent, and then fix the violations.

3. As an alternative, enable latch scan ability checks instead of latch transparency checks by changing the value of the **test_rtldrc_latch_check_style** variable to **scan**.

4. Reexecute the **rtldrc** command.

SEE ALSO

create_test_clock (2), **rtldrc** (2), **set_signal_type** (2), **set_test_hold** (2); **test_rtldrc_latch_check_style** (3).

TEST-1212 (information) Scan style is '%s'.

DESCRIPTION

You receive this information message when determining the scan style that was used for this **rtldrc** command run.

The scan style is set using either the **set_scan_configuration** command or the **test_default_scan_style** variable. If neither of these is used, the scan style defaults to multiplexed flip-flop.

WHAT NEXT

This is an informational message only. No action is required on your part. However, if the wrong scan style was used, you can change the style and then rerun **rtldrc**.

SEE ALSO

rtldrc (2), **set_scan_configuration** (2); **test_default_scan_style** (3).

TEST-1213 (error) Cell '%s' is not a mapped cell.

DESCRIPTION

You receive this error message because the design used with the **preview_dft** or the **insert_dft** command contains unmapped cells.

WHAT NEXT

Run the **compile** command in dc_shell to get a successful compile, and then rerun **preview_dft** or **insert_dft**.

SEE ALSO

insert_dft (2), **preview_dft** (2).

TEST-1214 (warning) Following drivers cause contention on bus %s.

DESCRIPTION

You receive this warning message because **rtldrc -tristate** found a bus that might cause a contention state. This occurs when a pattern is found that can simultaneously enable two or more tristate drivers to the same net.

WHAT NEXT

No action is required on your part. However, you can correct your design and eliminate this warning message.

SEE ALSO

rtldrc (2).

TEST-1215 (warning) Following drivers cause contention on net

%s.

DESCRIPTION

You receive this warning message because **rtldrc -tristate** found a multi-driver net that might cause a contention state. A violation occurs when a pattern is found that simultaneously drives a different value on the outputs of two gates driving a wire.

WHAT NEXT

No action is required on your part. However, you can correct your design and eliminate the warning message.

SEE ALSO

rtldrc (2).

TEST-1216 (warning) Bus '%s' (%s,%s) is capable of being in floating state.

DESCRIPTION

You receive this warning message because **rtldrc -tristate** found a bus that is capable of being in a **floating state**. The tool found a pattern that can simultaneously disable all tristate drivers to the same net.

WHAT NEXT

No action is required on your part. However, you can correct your design and eliminate the warning message.

SEE ALSO

rtldrc (2).

TEST-1217 (Error) Wrapped core '%s' has '%d' '%s' modes.

DESCRIPTION

You receive this error message because the DFT Compiler found a wrapped core that does not have all of the modes required for core integration. The DFT Compiler requires one or more Internal test modes, one External test mode, one Normal mode,

and an optional Isolate mode for a wrapped core to use it in core integration. If Isolate mode is not present, Normal mode is used to put the core in a safe state during core integration.

WHAT NEXT

Verify that Internal test mode, External test mode, and Normal mode are correctly defined for the specified wrapped core. If any of these test modes are missing, add these test modes. Ensure that there is only one External mode, one Normal mode, and one Isolate mode. before integrating the core.

SEE ALSO

check_dft (2).

TEST-1220 (Warning) More than one '%s' mode found on the core '%s', using the '%s' mode '%s' in core integration.

DESCRIPTION

You receive this warning message because the DFT Compiler found more modes than the required number of modes for core integration. The DFT Compiler requires one External test mode, one Normal mode, and an optional Isolate mode for a wrapped core to use it in core integration. If more than one of these modes are found, one of the modes is will be used in core integration.

WHAT NEXT

If the specified mode is not the correct mode, ensure that the model contains only the desired mode of the specified mode type. Otherwise, no action is required on your part.

SEE ALSO

check_dft (2).

TEST-1221 (Error) No '%s' mode found for the core '%s'.

DESCRIPTION

You receive this error message because the DFT Compiler cannot find a required mode for core integration. The DFT Compiler requires at least one External test mode and one Normal mode for a wrapped core to use it in core integration.

WHAT NEXT

Add the missing mode to the core so that the core can be used in core integration and then run the command again.

SEE ALSO

check_dft (2).

TEST-1222 (Warning) No ’Isolate’ mode found for the core ’%s’, using ’Normal’ mode.

DESCRIPTION

You receive this warning message because the DFT Compiler did not find Isolate mode for the specified core. The DFT Compiler requires the optional Isolate mode for all cores to use them in core integration. If an Isolate mode is not found, Normal mode is used for core integration.

WHAT NEXT

If Normal mode is not a safe mode for use with core integration, add Isolate mode to the core before trying core integration again. Otherwise, no action is required on your part.

SEE ALSO

check_dft (2).

TEST-1223 (Warning) TCM controller is already inserted for the design ’%s’, not inserting or modifying the controller logic.

DESCRIPTION

You receive this warning message because the DFT Compiler found TCM controller in the specified design. The DFT Compiler does not modify the existing controller logic or insert a new controller if there is a controller already in the design.

WHAT NEXT

No action is required on your part. However if you intend to run core integration again, run the scan insertion on the design prior to inserting the controller.

SEE ALSO

check_dft (2).

TEST-1224 (Error) The scan state is invalid for -physical option in insert_scan, preview_scan, insert_dft and preview_dft

DESCRIPTION

You receive this error message because the scan state should be either **test_ready** (scan replaced) or **scan_existing** (scan routed) for the **-physical** option in the **insert_scan**, **preview_scan**, **insert_dft**, and **preview_dft** commands. If the current state of the design is unknown, this error message prevents a preview or insertion from proceeding.

WHAT NEXT

Set the state using the **set_scan_state** command before using the **-physical** option with the commands mentioned above.

SEE ALSO

insert_dft (2), **insert_scan** (2), **preview_dft** (2), **preview_scan** (2).

TEST-1225 (Error) BIST does not support more than 512 scan chains.

DESCRIPTION

You receive this error message because the BIST Controller supports a maximum of 512 scan chains.

WHAT NEXT

Rerun the BIST Ready step and limit the number of scan chains to less than 512.

SEE ALSO

set_dft_configuration (2), **set_bist_configuration** (2).

TEST-1226 (Error) Could not establish link with Tmax.

DESCRIPTION

You receive this error message because the DFT Compiler is unable to communicate with the TetraMAX process.

WHAT NEXT

Ensure that the TetraMAX executable is installed and then run the DFT Compiler again.

SEE ALSO

set_dft_configuration (2), **set_bist_configuration** (2).

TEST-1227 (Error) Could not access BIST Controller from DesignWare.

DESCRIPTION

You receive this error message because the DFT Compiler is unable to access the BIST Controller from DesignWare.

WHAT NEXT

Check your **search_path** variable and include **dft_lbist.sldb** in your **synthetic_library** variable. Rerun the DFT Compiler.

SEE ALSO

search_path (3), **synthetic_library** (3).

TEST-1228 (Error) Could not find "%s" cell in "%s

DESCRIPTION

You receive this error message because the DFT Compiler is unable to find the core cell *core_i* in the TOP design.

WHAT NEXT

If you have instantiated the core design with a cell name other than *core_i* in the TOP design, pass on the core cell name to the **set_bist_configuration** command using the **-core_cell** option.

SEE ALSO

set_bist_configuration (2).

TEST-1229 (Error) Desired cycle compression cannot be achieved. It should be lower than %d.

DESCRIPTION

You receive this error message because your specified cycle compression ratio is too high. It should be lower than the indicated value.

WHAT NEXT

Specify lower cycle compression ratio with -cycle_compression option in set_bist_auto_parameters.

SEE ALSO

set_dft_configuration (2), **set_bist_configuration** (2), **set_bist_auto_parameters** (2).

TEST-1230 (Error) Auto architecting parameters are not specified.

DESCRIPTION

You receive this error message because you specified -auto switch in set_bist_configuration command, but didn’t specify required auto architecting parameters.

WHAT NEXT

Specify auto architecting parameters with set_bist_auto_parameters command.

SEE ALSO

set_dft_configuration (2), **set_bist_configuration** (2), **set_bist_auto_parameters** (2).

TEST-1231 (Error) Number of fuses '%d' are not sufficient for the repair chain of length '%d'.

DESCRIPTION

You receive this error message because Core Integration(DFT Compiler - SOC) cannot find sufficient number of fuses to integrate with all MBIST(Tech2) core repair chains. Core Integration requires the number of fusees to be atleast the number of repair bits of all MBIST core repair chains.

WHAT NEXT

Add sufficient fuses for Core Integration to integrate fusees with MBIST core repair chains correctly.

SEE ALSO

set_dft_configuration (2). **preview_dft** (2). **insert_dft** (2).

TEST-1232 (Warning) Fuse Box '%s' segment '%s' is not controlled by a valid clock, ignoring the segment for integration.

DESCRIPTION

You receive this warning message because Core Integration(DFT Compiler - SOC) cannot find a valid clock for the specified fuse box segment. The fuse box segment will be excluded from Core/BSD Integration. Please note that this may cause insufficient number of fuses to integrate with all MBIST(Tech2) core repair chains.

WHAT NEXT

Check if the clock pin of the fuse box segment is connected to a clock port of the current design. If the connected clock port is not recognized by **create_test_protocol**, run **create_test_protocol** with **-infer_clock -infer_async** option. Also make sure that the connected clock port is specified as dft signal of type **bist_clk_lu** so that this clock is also used to connect the MBIST(Tech2) core repair chains. In case of BSD Integration, the connected clock port can also be specified as TAP TCK port.

If the clock pin of fuse box segment is not connected to any clock, Core Integration

will automatically connect it to a /fBbist_clk_lu/fP signal if the clock pin has **User snps_bist_clk_lu** attribute in CTL section of the fuse box model for mode type Repair.

If the clock pin of fuse box segment is not connected to any clock, BSD Integration will automatically connect it to TAP TCK port if there is no /fBbist_clk_lu/fP dft signal specified by the user and the fuse box clock pin has **User snps_bist_clk_lu** attribute in CTL section of the fuse box model for mode type Repair. If there is a /fBbist_clk_lu/fP dft signal, fuse box clock pin is connected to the dft signal.

Fuse Box segment is also not used in integration if the segment is violated by drc. if the segment is violated, fix the violation and rerun integration.

SEE ALSO

set_dft_configuration (2), **preview_dft** (2), **insert_dft** (2), **create_test_protocol** (2), **dft_drc** (2).

TEST-1250 (error) No TCK clock information found.

DESCRIPTION

This message is printed out when there is no TCK clock information in the list of input signals in the CTL model.

WHAT NEXT

Make sure that TCK is part of the input signal list in the design.

SEE ALSO

create_bsd_patterns (2), **write_test** (2).

TEST-1251 (error) Unable to get BSD waveform table data from CTL.

DESCRIPTION

This message is printed out when the BSD waveform table information is not found in the CTL.

WHAT NEXT

Make sure that BSD waveform data is available in the CTL for the design.

SEE ALSO

create_bsd_patterns (2), **write_test** (2).

TEST-1252 (information) Printing variables in the Verilog test bench file ...

DESCRIPTION

This message is displayed when the tool is printing variables in the Verilog test bench file.

SEE ALSO

write_test (2).

TEST-1253 (error) The location/name of the stil2wgl executable specified is incorrect.

DESCRIPTION

This message is displayed when the location/name of the stil2wgl executable specified is incorrect.

WHAT NEXT

Make sure the name of the executable is correctly specified. Also, make sure that you are executable is for your opearting system and that the executable location is included in your search path.

SEE ALSO

write_test (2).

TEST-1254 (error) The location/name of the stil2wgl has not

been specified.

DESCRIPTION

This message is displayed when the location/name of the stil2wgl has not been specified.

WHAT NEXT

Make sure the name of the executable is correctly specified. Also, make sure that you are executable is for your opearting system and that the executable location is included in your search path.

SEE ALSO

write_test (2).

TEST-1255 (information) Generating native Verilog test bench...

DESCRIPTION

This message is displayed when the tool starts generating the native Verilog test bench.

SEE ALSO

write_test (2).

TEST-1256 (information) Generating STIL-DPV test bench...

DESCRIPTION

This message is displayed when the tool starts generating the STIL-DPV test bench.

SEE ALSO

write_test (2).

TEST-1257 (information) Printing the MBIST trace (if any) in the

test bench file ...

DESCRIPTION

This message is displayed when the tool starts printing the MBIST trace if any in the Verilog test bench file.

SEE ALSO

write_test (2).

TEST-1258 (information) Diagnosis trace file is %s...

DESCRIPTION

This message is displayed when the tool is printing the diagnosis trace file.

SEE ALSO

write_test (2).

TEST-1259 (information) Writing test program to ctldb...

DESCRIPTION

This message is displayed when the tool writing the test program to ctldb.

SEE ALSO

write_test (2).

TEST-1260 (information) Writing test program to ctldc...

DESCRIPTION

This message is displayed when the tool writing the test program to ctldc.

SEE ALSO

write_test (2).

TEST-1261 (error) Internal error in translating BSD pattern bit '%c' of vector '%s' to CTL format.

DESCRIPTION

This message is displayed when there is an internal error in translating BSD pattern bit to CTL format and the specific bit of the vector that is the cause of this failure is known.

WHAT NEXT

Make sure that the BSD patterns are correct. In case, the issue is still not resolved, inform Synopsys Inc citing the details of the failure.

SEE ALSO

create_bsd_patterns (2). **write_test** (2).

TEST-1262 (error) Internal error in translating BSD vector '%s' to CTL format.

DESCRIPTION

This message is displayed when there is an internal error in translating BSD pattern bit to CTL format.

WHAT NEXT

Make sure that the BSD patterns are correct. In case, the issue is still not resolved, inform Synopsys Inc citing the details of the failure.

SEE ALSO

create_bsd_patterns (2). **write_test** (2).

TEST-1263 (error) Invalid port type %s specified.

DESCRIPTION

This message is displayed when the port type displayed is neither an input port, output port or a BiDi port.

WHAT NEXT

Make sure that the port under consideration can be identified either as an input port, output port or BiDi port.

SEE ALSO

write_test (2), **create_bsd_patterns** (2).

TEST-1264 (error) Incorrect test bench format %s specified.

DESCRIPTION

This message is displayed when the format of test bench is incorrectly specified.

WHAT NEXT

Make sure that the test bench format specified is either "verilog" or "stil_testbench".

SEE ALSO

write_test (2), **create_bsd_patterns** (2).

TEST-1265 (information) Printing the design instance name in the test bench file...

DESCRIPTION

This message is displayed when the design instance name is being printed in the test bench file.

SEE ALSO

write_test (2).

TEST-1266 (information) Printing the clock assignment statement in the test bench file ...

DESCRIPTION

This message is displayed when the clock assignment statement is written out in the test bench file.

SEE ALSO

write_test (2).

TEST-1267 (information) Printing the input assignment in the test bench file ...

DESCRIPTION

This message is displayed when the input assignment statement is written out.

SEE ALSO

write_test (2).

TEST-1268 (information) Printing the output assignment in the test bench file...

DESCRIPTION

This message is displayed when the output assignment statement is written out.

SEE ALSO

write_test (2).

TEST-1269 (information) Printing the observed BiDi assignment in the test bench file...

DESCRIPTION

This message is displayed when printing the observed BiDi assignment in the test bench file...

SEE ALSO

write_test (2).

TEST-1270 (information) Printing the BiDi assignment in the Verilog test bench file ...

DESCRIPTION

This message is displayed when the BiDi assignment port statement is written out.

SEE ALSO

write_test (2).

TEST-1271 (information) Printing the routines that check the output responses in the test bench file ...

DESCRIPTION

This message is displayed when the routines that check the output responses in the test bench file are written out.

SEE ALSO

write_test (2).

TEST-1272 (information) Printing the pattern information in the

test bench file...

DESCRIPTION

This message is displayed when the pattern information in the test bench file is written out.

SEE ALSO

write_test (2).

TEST-1273 (error) An error occurred when writing the ports in the Verilog test bench file.

DESCRIPTION

This message is displayed when an internal tool error is encountered when writing the ports in the Verilog test bench file.

WHAT NEXT

Please contact Synopsys Inc citing the error number.

SEE ALSO

write_test (2).

TEST-1274 (error) An error occurred when writing the register assignments in the Verilog test bench file.

DESCRIPTION

This message is displayed when an internal tool error is encountered when writing the register assignments in the Verilog test bench file.

WHAT NEXT

Please contact Synopsys Inc citing the error number.

SEE ALSO

write_test (2).

TEST-1275 (error) An error occurred when writing the design instance name in the Verilog test bench file.

DESCRIPTION

This message is displayed when an internal tool error is encountered when writing the design instance name in the Verilog test bench file.

WHAT NEXT

Please contact Synopsys Inc citing the error number.

SEE ALSO

write_test (2).

TEST-1276 (error) An error occurred when writing the MBIST trace in the Verilog test bench file.

DESCRIPTION

This message is displayed when an internal tool error is encountered when writing the MBIST trace in the Verilog test bench file.

WHAT NEXT

Please contact Synopsys Inc citing the error number.

SEE ALSO

write_test (2).

TEST-1277 (error) An error occurred when writing the STIL DPV

test bench file.

DESCRIPTION

This message is displayed when an internal tool error is encountered when writing the STIL DPV test bench file.

WHAT NEXT

Please contact Synopsys Inc citing the error number.

SEE ALSO

write_test (2).

TEST-1278 (error) No pattern exec found in CTL file for the design.

DESCRIPTION

This message is displayed when No pattern exec found in CTL file for the design.

WHAT NEXT

Make sure that there does exist a pattern exec statement in the CTLfile for the sdesign.

SEE ALSO

write_test (2).

TEST-1279 (error) Internal Error in translating CTL pattern bit %c of vector %s to Verilog format.

DESCRIPTION

This message is displayed when an internal tool error is encountered when translating a specific CTL pattern bit of a apecific vector to Verilog format.

WHAT NEXT

Please contact Synopsys Inc citing the error number.

SEE ALSO

write_test (2).

TEST-1280 (error) NULL string supplied for translation from CTL to Verilog format.

DESCRIPTION

This message is displayed when a NULL string supplied for translation from CTL to Verilog format.

WHAT NEXT

Please contact Synopsys Inc citing the error number.

SEE ALSO

write_test (2).

TEST-1281 (error) TCK is not a positive-edge clock.

DESCRIPTION

This message is displayed when a rise time of the TCK is greater than or equal to the fall time of TCK.

WHAT NEXT

Please make sure that the TCK rise & fall times are compatible,

SEE ALSO

write_test (2).

TEST-1282 (error) Patterns in CTL refer to unknown signal

groups.

DESCRIPTION

Signal groups should be one of the following: all_inputs, all_outputs or all_bidirectionals. No other signal group labels are recognized.

WHAT NEXT

Please make sure that the signal groups have been named correctly & the signal in each of the group matches the group name.

SEE ALSO

write_test (2).

TEST-1301 (warning) No of Chains '%d' exceeds the count supported by the Tester '%d'.

DESCRIPTION

You receive this warning message because the scan chain count exceeds the limits of the Tester specified in the Tester rule file. The warning message occurs when executing the **preview_dft** and **preview_scan** commands.

The warning does not affect the execution of the commands that perform tester rule checking.

WHAT NEXT

No action is required on your part. However, you can set the chain count with the **set_scan_configuration** command and then run **preview_dft** or **preview_scan** again.

SEE ALSO

preview_dft (2), **preview_scan** (2), **set_scan_configuration** (2).

TEST-1302 (warning) Chain length '%d' for chain '%s' exceeds

the Tester limt ‘%d’.

DESCRIPTION

You receive this warning message because the scan chain length exceeds the limits of the Tester specified in the Tester rule file. The warning message occurs when executing the **preview_dft** and **preview_scan** commands.

The warning does not affect the results of the commands that perform tester rule checking.

WHAT NEXT

No action is required on your part. However, you can set the chain length with the **set_scan_path** command and run **preview_dft** or **preview_scan** again.

SEE ALSO

preview_dft (2), **preview_scan** (2), **set_scan_path** (2).

TEST-1303 (warning) No of pins ’%d’ exceeds the count supported by Tester ’%d’.

DESCRIPTION

You receive this warning message because the pin count exceeds the limits of the Tester specified in the Tester rule file. The warning message occurs when executing the **preview_dft** and **preview_scan** commands.

The warning does not affect the results of the commands that perform tester rule checking.

WHAT NEXT

No action is required on your part.

SEE ALSO

preview_dft (2), **preview_scan** (2).

TEST-1304 (warning) Clock period ’%f’ns is less than minimun

Tester limit '%f'ns'.

DESCRIPTION

You receive this warning message because the clock period is less than the minimum limit of the Tester specified in the Tester rule file. The warning message occurs when executing the **preview_dft** and **preview_scan** commands.

The warning does not affect the results of the commands that perform tester rule checking.

WHAT NEXT

No action is required on your part. However, you can set the clock period with the **test_default_period** environment variable and then run **preview_dft** or **preview_scan** again.

SEE ALSO

preview_dft (2), **preview_scan** (2); **test_default_period** (3).

TEST-1305 (warning) Clock period '%f'ns is greater than maximum Tester limit '%f'ns.

DESCRIPTION

You receive this warning message because the clock period is more than the maximum limit of the Tester specified in the Tester rule file. The warning message occurs when executing the **preview_dft** and **preview_scan** commands.

The warning does not affect the results of the commands that perform tester rule checking.

WHAT NEXT

No action is required on your part. However, you can set the clock period with the **test_default_period** environment variable and then run **preview_dft** or **preview_scan** again.

SEE ALSO

preview_dft (2), **preview_scan** (2); **test_default_period** (3).

TEST-1306 (warning) Shift clock period '%f'ns is less than minimun Tester limit '%f'ns.

DESCRIPTION

You receive this warning message because the test clock period is less than the minimum limit of the Tester specified in the Tester rule file. The warning message occurs when executing the **preview_dft** and **preview_scan**.

The warning does not affect the results of the commands that perform tester rule checking.

WHAT NEXT

No action is required on your part. However, you can set the clock period with the **test_default_period** environment variable and then run **preview_dft** or **preview_scan** again.

SEE ALSO

preview_dft (2), **preview_scan** (2); **test_default_period** (3).

TEST-1307 (warning) Shift clock period '%f'ns is greater than maximum Tester limit '%f'ns.

DESCRIPTION

You receive this warning message because the clock period is more than the maximum limit of the Tester specified in the Tester rule file. The warning message occurs when executing the **preview_dft** and **preview_scan** commands.

The warning does not affect the results of the commands that perform tester rule checking.

WHAT NEXT

No action is required on your part. However, you can set the clock period with the **test_default_period** environment variable and then run **preview_dft** or **preview_scan** again.

SEE ALSO

preview_dft (2), **preview_scan** (2); **test_default_period** (3).

TEST-1308 (warning) Checks for Tester '%s' defined in file

DESCRIPTION

You receive this warning message indicating the Tester and the name of the file for which the tester rule checking is done. Tester rule checking is done for the **preview_dft**, **preview_scan**, **insert_dft**, and **insert_scan** commands.

The message appears for **preview_dft** and **preview_scan** only after displaying any messages for violations.

The message does not affect the result of these commands.

WHAT NEXT

No action is required on your part.

SEE ALSO

preview_dft (2), **preview_scan** (2).

TEST-1309 (warning) Tester rule checking violations for Tester '%s' in file %s.

DESCRIPTION

You receive this warning message indicating the Tester and the name of the file for which the tester rule checking is done and the violations found. Tester rule checking is done for the **preview_dft**, **preview_scan**, **insert_dft**, and **insert_scan** commands.

The message appears for **insert_dft** and **insert_scan** only after doing the checks and only if there is a violation.

The message does not affect the result of these commands.

WHAT NEXT

Correct the design using this diagnostic information and run the command again.

SEE ALSO

insert_dft (2), **insert_scan** (2).

TEST-1310 (Error) Invalid test protocol. Create a test protocol again.

DESCRIPTION

You receive this error message because design rule checking is unable to find a valid test protocol for the current design.

The test protocol is created using the **create_test_protocol** command or is specified using the **read_test_protocol** command. Once created, the protocol is invalidated by changes to the design or specifications.

For example, suppose you have created a test protocol in TOP design. Running insert_dft in sub designs might invalidate the protocol of TOP design because it might have caused design change, and the protocol no longer matches the changed design.

WHAT NEXT

Check your specifications and recreate the protocol using the **create_test_protocol** command. If necessary, first remove the existing protocol using the **remove_test_protocol** command.

EXAMPLES

The following example removes a existing test protocol, and creates a new test protocol in memory for the current design:

```
dc_shell> remove_test_protocol
dc_shell> create_test_protocol
```

SEE ALSO

create_test_protocol (2), **read_test_protocol** (2), **remove_test_protocol** (2), **dft_drc** (2).

TEST-1311 (Error) Could not perform design rule checking.

DESCRIPTION

You receive this error message because the **dft_drc** command did not complete successfully.

WHAT NEXT

Look at the preceding messages for an explanation. The most common reasons are:

- Invalid protocol
- Bad specification

Correct the condition and rerun the **dft_drc** command.

SEE ALSO

create_test_protocol (2), **insert_dft** (2), **insert_scan** (2), **preview_dft** (2), **preview_scan** (2), **read_test_protocol** (2), **remove_test_protocol** (2), **dft_drc** (2).

TEST-1312 (Error) Could not create test protocol.

DESCRIPTION

You receive this error message because the **create_test_protocol** command could not create a test protocol.

WHAT NEXT

Check your design and specification. It is good practice to specify all your clocks and asynchs before creating a test protocol.

SEE ALSO

create_test_protocol (2), **read_test_protocol** (2), **remove_test_protocol** (2), **dft_drc** (2).

TEST-1313 (Error) Could not run pre-dft design rule checking.

DESCRIPTION

You receive this error message because test design rule checking was not performed while running the **preview_dft** or **insert_dft** command.

Test design rule checking is invoked when **preview_dft** or **insert_dft** is run with test-point applications (such as Autofix) specified using the **set_dft_configuration** command.

Test design rule checking performs two functions:

1. Performs pre-DFT test design rule checking
2. Designs test-points for the specified DFT applications.

WHAT NEXT

Review the preceding messages for the cause of the failure. The most common reasons for test design rule checking failure are as follows:

- Invalid test protocol
- Invalid specifications
- Incorrect designs
- Incorrect TMAX installation
- Problem while designing test-points

Correct the condition and rerun the **preview_dft** or **insert_dft** command.

SEE ALSO

create_test_protocol (2), **insert_dft** (2), **insert_scan** (2), **preview_dft** (2), **preview_scan** (2), **read_test_protocol** (2), **remove_test_protocol** (2), **set_dft_configuration** (2), **dft_drc** (2).

TEST-1314 (Error) Test design rule checking reported FATAL violations.

DESCRIPTION

You receive this error message because test design rule checking (DRC) found test design rule violations that must be corrected.

If the **dft_drc** information is out-of-date, the **preview_scan**, **insert_scan**, **preview_dft**, or **insert_dft** commands invoke the test DRC. The test DRC checks the current design against the test design rules of the scan test implementation specified by the **set_scan_configuration** command with the **-style** and **-methodology** options. When the test DRC completes, it issues this message if the tool found any fatal violations. Fatal violations prevent you from continuing with the **preview_scan**, **insert_scan**, **preview_dft**, or **insert_dft** commands.

WHAT NEXT

Check the violations found by the test DRC. Do not proceed to scan insertion or to ATPG without first checking the violations.

If you did not run **dft_drc** explicitly and the scan insertion or ATPG is unsatisfactory, run the **dft_drc** command. Read the Test Design Rule Violation Summary and the Sequential Cell Summary at the end of the **dft_drc** report. If there are any violations, review the violations and their causes before you proceed. Fatal violations must be fixed before you can proceed.

To understand the violations, read the two Summaries and the more detailed information generated by the **dft_drc** command. If you need details of all of the violations found by **dft_drc**, rerun **dft_drc** in verbose mode (**dft_drc -verbose**).

The best practice is to run **dft_drc** explicitly and read the violation reports before you run **preview_scan** or **insert_scan**. Because **preview_scan** and **insert_scan** only run **dft_drc** if you have not run **dft_drc** explicitly, you do not save any time by not running **dft_drc** explicitly.

SEE ALSO

insert_dft (2), **insert_scan** (2), **preview_dft** (2), **preview_scan** (2), **set_scan_configuration** (2), **dft_drc** (2).

TEST-1315 (warning) Ignoring attribute '%s' on pin '%s', because the cell value '%s' does not refer to a valid BIST-wrapped memory.

DESCRIPTION

You receive this warning message when you use the **set_attribute** command to manually specify the mapping of a BIST-wrapped memory cell to the MBIST controller port associated with the pin that holds the attribute. The specified cell is not recognized as a BIST-wrapped memory, so the attribute is ignored.

WHAT NEXT

No action is required on your part if you are satisfied with the current result.

However, to eliminate the warning message, ensure that the cell name used in the attribute is correct. Also ensure that the CTL model is present and correct. The cell is not recognized as a BIST-wrapped memory when the CTL model is missing or incorrect. Use the **read_test_model** command to read the correct model for the BIST-wrapped memory.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_attribute** (2), **set_dft_configuration** (2).

TEST-1316 (warning) Ignoring attribute '%s' on pin '%s', because the cell value '%s' refers to a BIST-wrapped memory that is incompatible with memory BIST controller port %d.

DESCRIPTION

You receive this warning message when you use the **set_attribute** command to manually specify the mapping of a BIST-wrapped memory cell to the MBIST controller port associated with the pin that holds the attribute. Each port of the MBIST controller is customized to support a particular type of memory. The warning message indicates that the specified BIST-wrapped memory is incompatible with the port associated with the pin attribute, so the attribute is ignored.

WHAT NEXT

No action is required on your part if you expected this result.

However, if you want to eliminate this warning message, use the **preview_dft** command to see how the BIST-wrapped memories are mapped to the ports of the MBIST controller. Determine which ports are assigned to the type of BIST-wrapped memory in this warning message, and use the **set_attribute** command on a pin associated with one of those ports.

SEE ALSO

insert_dft (2), **preview_dft** (2), **set_attribute** (2), **set_dft_configuration** (2).

TEST-1317 (warning) Ignoring attribute '%s' on pin '%s', because the BIST-wrapped memory '%s' is already mapped to port %d of the same memory BIST controller.

DESCRIPTION

You receive this warning message when you use the **set_attribute** command to manually specify the mapping of a BIST-wrapped memory cell to the MBIST controller port associated with the pin that holds the attribute. This warning message indicates that multiple ports of the same MBIST controller refer to the same BIST-wrapped memory cell. Since a BIST-wrapped memory must be associated with exactly one MBIST controller port, the second specification attribute is ignored.

WHAT NEXT

No action is required on your part if you expected this result.

However, to eliminate the warning message, use the **remove_attribute** command to remove excess specifications that refer to this BIST-wrapped memory.

SEE ALSO

insert_dft (2), **preview_dft** (2), **remove_attribute** (2), **set_attribute** (2), **set_dft_configuration** (2).

TEST-1318 (warning) Ignoring attribute '%s' on pin '%s', because the cell value '%s' refers to a BIST-wrapped memory that is mapped to another memory BIST controller.

DESCRIPTION

You receive this warning message when you use the **set_attribute** command to manually specify the mapping of a BIST-wrapped memory cell to the MBIST controller port associated with the pin that holds the attribute. This warning message indicates that the same BIST-wrapped memory cell is referenced by multiple MBIST controllers. Since a BIST-wrapped memory must be associated with exactly one MBIST controller port, the second specification attribute is ignored.

WHAT NEXT

No action is required on your part if you expected this result.

However, to avoid the warning message, use the **remove_attribute** command to eliminate excess specifications that refer to this BIST-wrapped memory.

SEE ALSO

insert_dft (2), **preview_dft** (2), **remove_attribute** (2), **set_attribute** (2), **set_dft_configuration** (2).

TEST-1319 (warning) MBIST controller port %d for cell %s is not connected to a BIST-wrapped memory.

DESCRIPTION

You receive this warning message when all available BIST-wrapped memories are assigned to the MBIST controller, and there are control ports remaining. The MBIST controller and BIST-wrapped memories are always generated so that there are no leftover control ports.

WHAT NEXT

No action is required on your part if you expected this result.

However, to avoid the warning message, ensure that all of the BIST-wrapped memory instances are instantiated in your design. Use the **read_test_model** command to read the correct models for all BIST-wrapped memories.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1320 (warning) BIST-wrapped memory %s is not connected to an MBIST controller.

DESCRIPTION

You receive this warning message because the BIST-wrapped memory could not be assigned to an MBIST controller. The warning message occurs if you load the incorrect model for the MBIST controller and/or the BIST-wrapped memory. The message also occurs when you instantiate more instances of the memory than were specified when you generated the MBIST logic.

WHAT NEXT

No action is required on your part if you expected this result.

However, to eliminate the warning message, examine your design to ensure that the MBIST controller and BIST-wrapped memories match what was specified during MBIST generation. Also, verify that you are loading the correct models by running the **read_test_model** command.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1321 (error) Port '%s' can not drive core cell '%s' pin '%s' and core cell '%s' pin '%s' in test mode '%s', because the cell designs are different.

DESCRIPTION

You receive this error message when you try to test two cores in parallel, but pins

from each core require potentially different input values on the same top-level port. In this case, the fact that the cells are different implies that the patterns are different, which causes the data conflict on the port.

WHAT NEXT

Use the **define_test_mode** and **set_test_target** commands to test these cores in separate test modes.

SEE ALSO

define_test_mode (2), **set_test_target** (2).

TEST-1322 (error) Port '%s' can not drive core cell '%s' pin '%s' and core cell '%s' pin '%s' in test mode '%s', because the pins are different.

DESCRIPTION

You receive this error message when you try to test two cores in parallel, but pins from each core require potentially different input values on the same top-level port. In this case, the fact that the pins are different implies that the pattern data for each pin is different, which causes the data conflict on the port.

WHAT NEXT

Use the **define_test_mode** and **set_test_target** commands to test these cores in separate test modes.

SEE ALSO

define_test_mode (2), **set_test_target** (2).

TEST-1323 (error) Port '%s' can not drive core cell '%s' pin '%s' and core cell '%s' pin '%s' in test mode '%s', because the core modes '%s' and '%s' are different.

DESCRIPTION

You receive this error message when you try to test two cores in parallel, but pins from each core require potentially different input values on the same top-level

port. In this case, the cells are the same and the pins are the same, but the cells are tested in different modes. The fact that the modes are different implies that the patterns are different, which causes the data conflict on the port.

WHAT NEXT

Use the **define_test_mode** and **set_test_target** commands to test these cores in separate test modes. You can also use the **set_test_target** command to test the cores in the same core mode.

SEE ALSO

define_test_mode (2), **set_test_target** (2).

TEST-1324 (error) Signal type is either invalid or bi-directional for signal %s in the CTL model for memory '%s'.

DESCRIPTION

You receive this message because either the signal type specified in the memory CTL model is invalid or the signal has been defined as a bidirectional pin. MBIST insertion flow does not accept either of the above two cases.

WHAT NEXT

Please change the signal type in the CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1325 (error) Value Range for all the address pins should be same in the CTL model for memory '%s'.

DESCRIPTION

You receive this message because the value range specified for the all the address pins in the memory CTL model is not same. MBIST insertion flow requires the value range of all the address pins to be same.

WHAT NEXT

Please change the value range for the address pins in the CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1326 (error) For every ‘Read’ port, there should be a separate ‘Write’ port in the CTL model for memory ’%s".

DESCRIPTION

You receive this message because the ports specified in the memory CTL model have either a common enable signal, an address port, a read port or a write port. The ports specified can only have a common clock signal. For every read port there should be a separate write port and vice versa.

WHAT NEXT

Please remove the common signal or port from the port declaration in the CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1327 (error) %s port in the CTL model for memory ’%s’ has invalid synchronous behavior.

DESCRIPTION

You receive this message because the output or input port(s) specified in the memory CTL model have invalid synchronous behavior. The output/input port(s) can be specified as synchronous under the following conditions.

a. If one input port is synchronous, all input ports should be synchronous.
b. If one output port is synchronous, all output ports should be synchronous.
c. If one output port is synchronous, all input ports should be synchronous.

WHAT NEXT

Please correct the synchronous behavior of the port in the CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1328 (error) DelayCycles cannot be specified for data %s in the CTL model for memory '%s'.

DESCRIPTION

You receive this message because DelayCycles cannot be specified in the memory CTL model for Tech1 output or input ports that are not Synchronous. Tech2 does not support DelayCycles at all (the value,if present, must be 0).

WHAT NEXT

Please remove the DelayCycles specification from the CTL model or, for Tech1, you can declare the signal as Synchronous.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1329 (error) Invalid signal 'ActiveState' specified for %s in the CTL model for memory '%s'.

DESCRIPTION

You receive this message because the signal Active State specified in the memory CTL model is invalid. The ActiveState should be either ForceUp or ForceDown.

WHAT NEXT

Please change the signal ActiveState in the CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1330 (error) Signal 'ActiveState' specified is not same for

all the control signals in the CTL model for memory '%s'.

DESCRIPTION

You receive this message because the signal Active State specified in the memory CTL model is different for the control signals of a port. For each port, the ActiveState for all control signals should be either ForceUp or ForceDown.

WHAT NEXT

Please change the signal ActiveState in the CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1331 (error) The mode type for current test mode "%s" is not valid.

DESCRIPTION

You receive this message because the mode type for the current test mode is not "InternalTestMode" or "DebugMode".

WHAT NEXT

Change the current test mode to a mode mode that has a valid test mode.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1332 (error) The current test mode is not a valid MBIST test mode.

DESCRIPTION

You receive this message because the family specified in the test model is not "SNPS_MBIST_encapsulated". This could be because the design does not correspond to a memory, the family has been wrongly specified or the current test mode is not a valid MBIST test mode.

WHAT NEXT

Please change the current test mode to a valid test mode or change the family name in the CTL test model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1333 (error) The integer constant %s is not defined in the encapsulated memory CTL model.

DESCRIPTION

You receive this message because the integer constant is not specified in the test model. This could be because either it is not specified or it is wrongly spelled in the CTL model for the current test mode.

WHAT NEXT

Please specify the integer constant in the current test mode in the CTL test model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1334 (error) Delay cycles value %s is more than 2 for data %s in the CTL model for memory '%s.

DESCRIPTION

You receive this message because delay cycles value cannot be greater than 2 in the memory CTL model for output or input ports.

WHAT NEXT

Please remove the delay cycles specified for the port in the CTL model or declare the port delay cycles to be less than 2.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1335 (error) Signal %s is not declared in the internal block of mode %s in the CTL model for memory %s.

DESCRIPTION

You receive this message because the signal declaration is missing in the internal block in the ctl model.

WHAT NEXT

Please remove the signal from the the CTL model or add declaration for the signal in the internal block. For muxed memories, BIST_mode must contain all signals - including the system signals that are bypassed by the embedded mux and all bypass signals. When in doubt, add the signal as DataType Unused.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1336 (error) Error: Memory %s signal %s is CTL DataType %s which must have Signals direction IN.

DESCRIPTION

You receive this message because the signal direction is not defined IN in the signals block of the ctl model.

WHAT NEXT

Please change the signal direction in the signals block of the CTL model or change the DataType for the signal in the internal block.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1337 (error) Memory %s signal %s is CTL DataType %s

which must have Signals direction OUT.

DESCRIPTION

You receive this message because the signal direction is not defined OUT in the signals block of the ctl model.

WHAT NEXT

Please change the signal direction in the signals block of the CTL model or change the DataType for the signal in the internal block.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1338 (error) Memory %s signal %s is CTL DataType %s which must have Signals direction IN or OUT.

DESCRIPTION

You receive this message because the signal direction should be either defined IN or OUT in the signals block of the ctl model.

WHAT NEXT

Please change the signal direction in the signals block of the CTL model or change the DataType for the signal in the internal block.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1339 (error) Memory %s CTL mode %s signal %s has unsupported DataType %s.

DESCRIPTION

You receive this message because the signal DataType specified for the signal in the ctl model is not supported. The valid DataTypes are MasterClock, CoreSelect, MemAddr, MemWrite, Constant, TestMode, MemData, Functional and Synchronous.

WHAT NEXT

Please change the DataType for the signal in the CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1340 (error) DataType MemoryData is mandatory for port %d in the Ctl model of memory %s.

DESCRIPTION

You receive this message because the signal of DataType MemoryData is not specified in the CTL model. The memory port in the CTL model should have atleast one signal of DataType MemoryData with signal direction IN and one signal of DataType MemoryData with signal direction OUT.

WHAT NEXT

Please add the signal of DataType MemoryData in the CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1341 (error) Port %d with input bus of DataType MemoryData must have a signal with DataType MemoryWrite in the Ctl model of memory %s.

DESCRIPTION

You receive this message because a port that has a signal of DataType MemoryData and signal direction IN is required to have a signal of DataType MemoryWrite in the CTL model.

WHAT NEXT

Please add the signal of DataType MemoryWrite to the port in the CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1342 (error) Port %d with signal DataType MemoryWrite should have input bus of DataType MemoryData in the Ctl model of memory %s.

DESCRIPTION

You receive this message because a port that has a signal of DataType MemoryWrite is required to have a signal of DataType MemoryData and signal direction IN in the CTL model.

WHAT NEXT

Please add the signal of DataType MemoryData with signal direction IN to the port in the CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1343 (error) No address bus defined for port %d in the Ctl model of memory %s.

DESCRIPTION

You receive this message because a port is required to have a signal of DataType Memoryaddr in the CTL model.

WHAT NEXT

Please add the signal of DataType MemoryAddr to the port in the CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1344 (error) Relation block does not exist in the Ctl model of memory %s.

DESCRIPTION

You receive this message because the relation block that contains the port specifictions is missing in the memory CTL model.

WHAT NEXT

Please add port declaration and the relation block in the memory CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1345 (error) No ports are defined in the relation block of the Ctl model of memory %s.

DESCRIPTION

You receive this message because the relation block does not contain the port specifictions in the memory CTL model.

WHAT NEXT

Please add port declaration in the relation block in the memory CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1346 (error) MasterClock must be defined for all of the Relation Ports, no Relation Ports, or just the write Relation Ports in the Ctl model for %s.

DESCRIPTION

You receive this message because the MasterClocks are inconsistent membership in the

Relation Ports of your memory model. You can explicitly include a MasterClock on every Port. Alternatively, you can exclude the MasterClock from all Ports. In this case, the MasterClocks are considered global to all Ports. In the special case where a memory has synchronous write and asynchronous read, you can assign MasterClocks only to write Ports.

WHAT NEXT

Please modify the Port declaration in the Relation block in the memory CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1347 (error) Signal %s of DataType MemData has not been assigned to any port in the Ctl model of memory %s.

DESCRIPTION

You receive this message because the signal declared in the Signals block of DataType MemData has not been assigned to any port in the Relation block in the memory CTL model. All the signals of DataType MemData have to be assigned to a port.

WHAT NEXT

Please assign the signal to a port in the relation block in the memory CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1348 (error) Signal %s of DataType %s can not have value range in the Ctl model of memory %s.

DESCRIPTION

You receive this message because the signal declared in the Internal block cannot have ValueRange specified in the memory CTL model. ValueRange can be specified only for signals of DataType MemAddr.

WHAT NEXT

Please remove the ValueRange for the signal in the internal block in the memory CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1349 (error) Signal %s of DataType %s can not be defined to be synchronous in the Ctl model of memory %s.

DESCRIPTION

You receive this message because the signal declared in the Internal block cannot be specified to be Synchronous in the memory CTL model. Signals of DataType MemData only can be specified to be Synchronous.

WHAT NEXT

Please specify the signal in the internal block as non-synchronous in the memory CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1350 (error) Signal %s of signalType Pseudo can not be defined in the port %d declaration of the Ctl model of memory %s.

DESCRIPTION

You receive this message because the signal declared in the port is of type Pseudo in the memory CTL model. Signals of type Pseudo cannot be specified in a port declaration.

WHAT NEXT

Please remove the signal from the port declaration in the memory CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1351 (error) Signal %s cannot be shared in port %d and port %d of the Ctl model of memory %s.

DESCRIPTION

You receive this message because the control signal declared in the port cannot be shared amongst different ports in the memory CTL model. The signals that fall in this category are of DataType MemWrite and CoreSelect.

WHAT NEXT

Please remove the signal that is being shared from the port declaration in the memory CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1352 (error) Width %d of signal %s of DataType %s does not match width %d of signal %s in the Ctl model of memory %s.

DESCRIPTION

You receive this message because the signals of the DataType declared in the memory CTL model have different widths. The valid CTL models require all the widths of the signals of the DataType MemAddr to be the same and the widths of all the signals of DataType MemData to be the same.

WHAT NEXT

Please change the widths to be the same for all the signals of the DataType in the memory CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1353 (error) Width %d of signal %s of DataType %s is not in the specified range of %d to %d bits in the Ctl model of memory %s.

DESCRIPTION

You receive this message because the signal of the DataType declared in the memory CTL model has a signal width that is not valid. The valid CTL models require all the widths of the signals of the DataType MemoryAddress to be in the range of 3 to 24 bits. The widths of all the signals of DataType MemoryData should be in the range 3 to 256 bits. When the MBIST technology is tech1 and a ValueRange is specified in the CTL model for a memory address buss, then the corresponding signal of DataType MemoryAddress must be in the range of 4 to 24 bits.

WHAT NEXT

Please change the widths for all the signals of the DataType in the memory CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **set_mbist_configuration** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1354 (error) Memory %s is missing required BIST_mode with TestMode InternalTest and required Mission_mode with TestMode Normal.

DESCRIPTION

You receive this message because the Environment block in the CTL model is missing the Mission_mode and the BIST_mode blocks. The Normal, SNPS_memory, and InternalTest tokens are required in the Mission_mode and BIST_mode blocks for MBIST automation to recognize the memory.

WHAT NEXT

Please add the Mission_mode and BIST_mode blocks in the memory CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1355 (error) Signal %s of DataType Constant cannot have an ActiveState in memory CTL model %s.

DESCRIPTION

You receive this message because the signal in the CTL model of DataType Constant cannot have an ActiveState.

WHAT NEXT

Please change the signal DataType or remove the ActiveState for the signal in the memory CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1356 (error) Signal %s of DataType Constant can only have signal direction In in memory CTL model %s

DESCRIPTION

You receive this message because the signal in the CTL model of DataType Constant does not have the signal direction In.

WHAT NEXT

Please change the signal DataType or change the the signal direction to In in the memory CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1357 (error) No. of controllers specified in the '-num_controllers' switch more than the no. of available

memories.

DESCRIPTION

You receive this message because the number of controllers that you want to create are more than the total number of memories available for MBIST insertion. MBIST insertion requires every controller to be connected to atleast one memory. This could be because you have already assigned all the memories to the user defined controllers.

WHAT NEXT

Please specify a lower number of controllers using ‘set_mbist_configuration’ command or remove some of the memories from the list of memories assigned to the user specified controllers.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_mbist_configuration** (2). **set_dft_configuration** (2).

TEST-1358 (error) All the memory BIST algorithms cannot be switched off simultaneously.

DESCRIPTION

You receive this message because you have turned off all the three MBIST algorithms i.e., Marchlr, Marchc and Mats. MBIST flow requires atleast one algorithm to be switched on.

WHAT NEXT

Please specify the MBIST algorithms to run using ‘set_mbist_run’ (or ’set_testbench_parameters’ in XG mode) command.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_mbist_configuration** (2). **set_dft_configuration** (2).

TEST-1359 (error) All the memories cannot be disabled

simultaneously in the current test mode.

DESCRIPTION

You receive this message because you have disabled all the memories connected to a controller in the current test mode. MBIST flow requires atleast one memory to be enabled.

WHAT NEXT

Please specify the memories to be enabled using ‘set_mbist_run’ (or ’set_testbench_parameters’ in XG mode) command.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_mbist_configuration** (2). **set_dft_configuration** (2).

TEST-1360 (error) Upper value %d for the ValueRange specified for signal %s of DataType %s is greater than %d in the memory Ctl model %s.

DESCRIPTION

You receive this message because the signal of the DataType MemAddr declared in the memory CTL model has an upper value for the ValueRange higher than the specified limit. The upper limit for the ValueRange for an address bus of width ’w’ should not exceed (2^w-1).

WHAT NEXT

Please change the ValueRange for the signal of the DataType in the memory CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1361 (error) Signal %s of DataType %s is specified in

both %s and Bypass_mode.

DESCRIPTION

You receive this message because the signal of a particular DataType is also specified in a mode other than Bypass_mode in the memory CTL model. The signals declared in the Bypass mode of DataType MemAddr, MemData, MemWrite and CoreSelect should be specified as Unused in all the other modes.

WHAT NEXT

Please change the DataType of the signal in other modes in the memory CTL model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1362 (error) Port %d in Bypass_mode should have at least one signal of DataType TestMode for memories with embedded multiplexer.

DESCRIPTION

You receive this message because the output port of the muxed-memory is missing the signal of DataType TestMode in the memory CTL model. Since the Bypass_mode has been declared, the output port should have a control signal to bypass the memory output.

WHAT NEXT

Please add a signal of DataType TestMode to the reported port in the Bypass_mode of the memory Ctl model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1363 (error) The input data bus width %d and output data bus width %d are not same for the Read/Write port %d in

memory Ctl model %s.

DESCRIPTION

You receive this message because the read/write port specified in the memory Ctl model has unequal widths for signals of DataType MemoryData. You either described a signal wrongly as of DataType MemoryData in Internal block and included it in the port declaration or you have specified multiple data buses for the same port by mistake. For example, if a two port memory has DA and DB as input buses and QA and QB as output buses, the correct declaration for the two ports is:

Port 'CLKA+CENA+OENA+WENA+AA[10..0]+DA[7..0]+QA[7..0]' 0; Port 'CLKB+CENB+OENB+WENB+AB[10..0]+DB[7..0]+QB[7..0]' 1;

Here the input data bus width = output data bus width = 8. The wrong port declaration is:

Port 'CLKA+CENA+OENA+WENA+AA[10..0]+DA[7..0]+QA[7..0]' 0; Port 'CLKB+CENB+OENB+WENB+AB[10..0]]+DA[7..0]+DB[7..0]+QB[7..0]' 1;

Here the input data bus width = 16 and output data bus width = 8.

WHAT NEXT

Please specify the signals of DataType MemoryData correctly in the port in the memory Ctl model.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1370 (error) The first rising or falling edge of clock '%s' should be greater than 0.0 (rise time = %.2f, fall_time = %.2f).

DESCRIPTION

You receive this error message because the timing waveform of any clock should have rising or falling edge greater than 0.

WHAT NEXT

Check your protocol file or your script file that specifies timing waveforms of clocks.

SEE ALSO

create_test_protocol (2), **create_test_clock** (2), **dft_drc** (2).

TEST-1371 (error) Strobe time %.2f is in the active state of clock '%s' (rise time = %.2f, fall_time = %.2f)

DESCRIPTION

You receive this error message because strobe time is in the active state of clock period. Strobe time should be before or after the active state of clock period.

WHAT NEXT

Check the value of variable 'test_default_strobe' and change it to specify correct timing.

SEE ALSO

create_test_protocol (2), **create_test_clock** (2), **dft_drc** (2).

TEST-1372 (error) Strobe time %.2f is between (clock A start time = %.2f, clock B end time = %.2f)

DESCRIPTION

You receive this error message because strobe time is in the active states of two LSSD clocks. The strobe time must be before or after the active state of clock period.

WHAT NEXT

Check the value of variable 'test_default_strobe' and change it to specify correct timing.

SEE ALSO

create_test_protocol (2), **create_test_clock** (2), **dft_drc** (2).

TEST-1373 (error) Cannot use PLL_BYPASS option if the

design does not support PLL.

DESCRIPTION

You receive this error message because you specified the PLL_BYPASS option in the command **set_mbist_run** (or **set_testbench_parameters** in XG mode). The use of this parameter is allowed only when the design supports PLL.

WHAT NEXT

Delete the PLL_BYPASS option specified in the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) .

SEE ALSO

preview_dft (2), **set_mbist_run** (2). **set_testbench_parameters** (2).

TEST-1374 (error) enable|disable are the only allowed values of PLL_BYPASS option.

DESCRIPTION

You receive this error message because you specified a wrong value of the PLL_BYPASS option in the command **set_mbist_run** (or **set_testbench_parameters** in XG mode). ENABLE|DISABLE are the only allowed values of PLL_BYPASS option.

WHAT NEXT

Use ENABLE|DISABLE as right values of the PLL_BYPASS option in the command **set_mbist_run** (or **set_testbench_parameters** in XG mode).

SEE ALSO

preview_dft (2), **set_mbist_run** (2). **set_testbench_parameters** (2).

TEST-1375 (error) Signal %s is a reference clock with a period which is different from the default tester period.

DESCRIPTION

You receive this message because you have specified another type on a signal

previously declared as reference clock. This reference clock signal has a period different from the default tester period (test_default_period). The command is therefore rejected.

WHAT NEXT

Please change the period of the reference clock to match the test_default_period value, using -period option. Or do not specify another type for this signal.

SEE ALSO

remove_dft_signal (2), **report_dft_signal** (2).

TEST-1376 (error) The -period option can only be used for signals of type refclock.

DESCRIPTION

You receive this message because you specified a period value for a signal which is not of type refclock.

WHAT NEXT

Please remove the -period option or change the type of your signal.

SEE ALSO

remove_dft_signal (2), **report_dft_signal** (2).

TEST-1377 (warning) Ignoring period specification.

DESCRIPTION

You receive this warning because you declare as a reference clock a port previously specified otherwise. In this case, a period different than the default test period is rejected.

WHAT NEXT

You can go through the rest of the flow (in this case, the period of the reference clock is the default tester period (default_test_period) or remove the previous specification of this signal.

SEE ALSO

remove_dft_signal (2), **report_dft_signal** (2).

TEST-1378 (information) Unspecified timing is set to rise_time = %.3f and fall_time = %.3f.

DESCRIPTION

You receive this message because you did not specify the timing of your reference clock signal. The default value for the rise time is 0.25*period and for the fall time 0.75*period.

WHAT NEXT

You can go through the rest of the flow or use "-timing

SEE ALSO

remove_dft_signal (2), **report_dft_signal** (2).

TEST-1379 (information) Unspecified timing has been set to rise_time = %.3f and fall_time = %.3f.

DESCRIPTION

You receive this message because you did not specify the timing of a reference clock. Its timing has been set to the previously specified timing.

SEE ALSO

remove_dft_signal (2), **report_dft_signal** (2).

TEST-1380 (warning) This signal should also be defined as MasterClock for dual usage.

DESCRIPTION

You receive this message because your reference clock has the default tester period.

Or you did not specify the period of your reference clock signal. In this case, you should also declare this signal as a MasterClock to avoid DRC errors.

WHAT NEXT

Please, specify the reference clock as a MasterClock in case of dual usage.

SEE ALSO

remove_dft_signal (2), **report_dft_signal** (2).

TEST-1381 (error) Incorrect size of the clock controller bit list.

DESCRIPTION

You receive this message because you have used an incorrect number of elements to specify the clock controller bit list. The size of the clock controller bit list should be a multiple of three.

WHAT NEXT

You can go through the rest of the flow or use "-ctrl_bits

SEE ALSO

set_dft_signal (2),

TEST-1382 (error) Incorrect cycle number %s in the clock controller bit list.

DESCRIPTION

You receive this message because you have specified at least one incorrect cycle number in the clock controller bit list. The type of the cycles should be an alpha numeric value.

WHAT NEXT

You can go through the rest of the flow or use "-ctrl_bits

SEE ALSO

set_dft_signal (2),

TEST-1383 (error) Pin %s doesn’t exist in the design.

DESCRIPTION

You receive this message because you have specified an inexistent pin name in the clock controller bit list.

WHAT NEXT

You can go through the rest of the flow or use "-ctrl_bits

SEE ALSO

set_dft_signal (2),

TEST-1384 (error) Invalid active value %s for a clock controller bit.

DESCRIPTION

You receive this message because you have specified an invalid active value for at least one clock controller bit. The active value of clock controller bits should be either 0 or 1.

WHAT NEXT

You can go through the rest of the flow or use "-ctrl_bits

SEE ALSO

set_dft_signal (2),

TEST-1385 (error) Clock generator %s not defined.

DESCRIPTION

You receive this message because the clock generator was not specified. The clock generator should be specified using "set_dft_signal" as a ScanMasterClock and as an Oscillator before using it in the "-pll_clock

SEE ALSO

set_dft_signal (2),

TEST-1386 (error) Clock controller bits not specified.

DESCRIPTION

You receive this message because the clock controller bits were not specified. The clock controller bits should be specified using "-ctrl_bits" switch of the "set_dft_signal

SEE ALSO

set_dft_signal (2),

TEST-1387 (warning) The %s value of signal %s has been changed to %.2f.

DESCRIPTION

You receive this message because the resolution of your reference clock signal exceeds Picosecond unit.

WHAT NEXT

DFT tool has automatically set the value to the corresponding integer value in Picosecond. User can always re-specify the reference clock timing values using **set_dft_signal** command.

SEE ALSO

remove_dft_signal (2), **report_dft_signal** (2).

TEST-1401 (warning) a protocol already exists in mode '%s' and will be deleted.

DESCRIPTION

This warning is issued when DFTC reads a new test protocol when it has a test protocol already. The DFTC will delete the existing test proocol and read the new test protocol.

WHAT NEXT

Check whether the new test protocol is compatible with other test modes.

SEE ALSO

read_test_protocol(2), remove_test_protocol(2).

TEST-1402 (warning) a protocol already exists in mode '%s.' Please use remove_test_protocol command to delete the existing test protocol.

DESCRIPTION

This warning is issued when DFTC attempts to read a new test protocol when it has a test protocol already. The DFTC cannot overwrite the existing test proocol.

WHAT NEXT

Check whether to delete the existing protocol or not. Use **remove_test_protocol** command to delete the protocol.

SEE ALSO

read_test_protocol(2), create_test_protocol(2), remove_test_protocol(2).

TEST-1403 (error) cannot delete protocol from the mode '%s'.

DESCRIPTION

This error is issued when DFTC cannot delete a test protocol from the specified test

mode. One of the common reasons is that this test mode has a protocol inherited from 'all_dft' mode, and there are more than one test modes that have test protocols inherited from the 'all_dft' mode.

WHAT NEXT

Check other test modes and see if their protocols are inherited from the parent test mode of this mode. Then, remove the test protocol from 'all_dft' mode.

You can always delete a protocol from 'all_dft' mode.

SEE ALSO

read_test_protocol(2), list_test_modes(2), create_test_protocol(2), remove_test_protocol(2).

TEST-1410 (error) PLL clock %s test model is missing or incomplete. Please check if you have a correct test model.

DESCRIPTION

This error is issued when DFTC cannot find a test model for clock controller/chain. You might have read a wrong test model or did not read any of them.

One of the common reasons is that the test model is missing 'SNPS_CLOCK_chain' or 'SNPS_CLOCK_controller' family type in the test model. Please check the model and consult with the CTL test model guide line.

WHAT NEXT

Check if you have read a test model for the clock controller/chain corretly. Check if there are any error messages during reading.

SEE ALSO

read_test_model(2), write_test_model(2), list_test_modes(2).

TEST-1500 (error) Specified test program "%s

DESCRIPTION

You receive this message because you have specified a test program that does not exists in the current CTL model or in the specified CTL model (if you called the 'define_mbist_program' command with the '-model' parameter). In order to copy test

programs in the current CTL model you have to use the "define_mbist_program" command.

WHAT NEXT

Please copy the MBIST test programs you want to use using the "define_mbist_program" command.

SEE ALSO

define_mbist_program (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1501 (error) Using different test programs types for a controller

DESCRIPTION

You receive this message because you have specified different test programs types for a controller (e.g. single port and multiple port test programs)

WHAT NEXT

Specify the same type of test algorithms for a controller

SEE ALSO

define_mbist_program (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1502 (error) Invalid test program "%s

DESCRIPTION

You receive this message because you have specified a test program that does not contain any algorithm or background or the algorithm is empty.

WHAT NEXT

Specify a canned algorithm or create a new one and use "define_mbist_program" command to copy it in the current CTL model.

SEE ALSO

set_mbist_controller (2) **define_mbist_program** (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (XG) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1503 (error) Too many sequences in the test "%s

DESCRIPTION

You receive this message because the number of sequences of the specified test exceeds the supported range.

WHAT NEXT

Specify a canned algorithm or create a new one with fewer sequences and use "define_mbist_program" command to copy it in the current CTL model.

SEE ALSO

set_mbist_controller (2) **define_mbist_program** (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1504 (error) Empty Sequence %d of test "%s

DESCRIPTION

You receive this message because the sequence is empty.

WHAT NEXT

Specify a valid and not empty test sequence.

SEE ALSO

set_mbist_controller (2) **define_mbist_program** (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1505 (error) Number of ports must be the same for all test

sequences of program "%s

DESCRIPTION

You receive this message because you specified a test that has different number of port sections for sequences.

WHAT NEXT

Specify a canned algorithm or create a new one and use "define_mbist_program" command to copy it in the current CTL model.

SEE ALSO

set_mbist_controller (2) **define_mbist_program** (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1506 (error) Too many port sections in test "%s

DESCRIPTION

You receive this message because you specified a test that has too many port sections in at least one sequence.

WHAT NEXT

Specify a valid test sequence.

SEE ALSO

set_mbist_controller (2) **define_mbist_program** (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1507 (error) Invalid port section %d in sequence %d of test "%s

DESCRIPTION

You receive this message because you specified a test that has an invalid port section

WHAT NEXT

Specify a canned algorithm or create a new one and use "define_mbist_program" command to copy it in the current CTL model.

SEE ALSO

set_mbist_controller (2) **define_mbist_program** (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1508 (error) Invalid number of operations in test "%s

DESCRIPTION

You receive this message because you specified a test that contains a MarchSweep sequence where not all port sections have the same number of operations. Reported port/sequence number starts from 0.

WHAT NEXT

Specify a canned algorithm or create a new one and use "define_mbist_program" command to copy it in the current CTL model.

SEE ALSO

set_mbist_controller (2) **define_mbist_program** (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1509 (error) Too many operations in test "%s

DESCRIPTION

You receive this message because you specified a test that contains a port section with too many operations

WHAT NEXT

Specify a canned algorithm or create a new one and use "define_mbist_program" command to copy it in the current CTL model.

SEE ALSO

set_mbist_controller (2) **define_mbist_program** (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1510 (error) Test data background value of test "%s

DESCRIPTION

You receive this message because you specified a test that contains an invalid test data background value

WHAT NEXT

Specify a canned algorithm or create a new one and use "define_mbist_program" command to copy it in the current CTL model.

SEE ALSO

set_mbist_controller (2) **define_mbist_program** (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1511 (error) Test data background size of test "%s

DESCRIPTION

You receive this message because you specified a test that contains an invalid test data background size or the specified test data background size is too small to code the test data background value

WHAT NEXT

Specify a canned algorithm or create a new one and use "define_mbist_program" command to copy it in the current CTL model.

SEE ALSO

set_mbist_controller (2) **define_mbist_program** (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1512 (error) Test background sizes must be the same for all the tests of the controller

DESCRIPTION

You receive this message because you have specified multiple test programs for a controller but tests using different test background sizes.

WHAT NEXT

Specify tests using the same test background size or create new test backgrounds using "define_mbist_program" command.

SEE ALSO

set_mbist_controller (2) **define_mbist_program** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1513 (error) Invalid value for the CNTRL_SEL or CONTROL_SEL_<CORE_ID> parameter: %s

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because the CNTRL_SEL or CONTROL_SEL_<CORE_ID> parameter is not valid. The CNTRL_SEL and CONTROL_SEL_<CORE_ID> parameters control which controllers are enabled on reset. The value is a hexadecimal digit in which each bit represents a controller. By default, all controllers are enabled on reset.

WHAT NEXT

Run "preview_dft" to see how controllers are mapped.

SEE ALSO

set_mbist_controller (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1514 (error) Invalid value for the FAIL_LIMIT parameter

DESCRIPTION

You receive this message because you have specified a wrong value for the FAIL_LIMIT parameter or the specified value does not address a valid controller in the current design. Should be a integer positive value greater than zero.

WHAT NEXT

Specify a positive integer value.

SEE ALSO

set_mbist_configuration (2) **set_mbist_controller** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1515 (error) Invalid memory IP parameter entry "%s

DESCRIPTION

You receive this message because you have specified a wrong memory IP parameter

WHAT NEXT

Re-specify the IP parameters

SEE ALSO

set_mbist_element (2) **or** set_mbist_wrapper **(2)** (XG) **define_mbist_program** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1516 (error) Invalid controller IP parameter entry "%s

DESCRIPTION

You receive this message because you have specified a wrong controller IP parameter

WHAT NEXT

Re-specify the IP parameters, using the "set_mbist_controller" command

SEE ALSO

set_mbist_controller (2) **define_mbist_program** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1517 (error) Specification of incompatible parameters

DESCRIPTION

You receive this message because you have specified in the "define_mbist_program" command the parameter "-CTL" simultaneously with "-algorithm_name" or "-background_name".

WHAT NEXT

Re-specify the command by using only the "-CTL" parameter

SEE ALSO

define_mbist_program (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1518 (error) Wrong Test in controller "%s" as the number of ports of test "%s

DESCRIPTION

You receive this message because you have specified a test program that contains a different ports number than the memories inside the controller.

WHAT NEXT

Re-specify the test programs for that controller

SEE ALSO

set_mbist_controller (2) **define_mbist_program** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1519 (error) Invalid value for the NUM_FAULTS_SWEEP

parameter

DESCRIPTION

You receive this message because you specified an invalid integer value for the NUM_FAULTS_SWEEPn parameter

WHAT NEXT

Specify an integer positive value

SEE ALSO

set_mbist_run (2) **or** set_testbench_parameters **(2)** (in **XG** mode)
set_mbist_configuration (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1520 (error) Incorrect number of memories %d assigned to controller "%s

DESCRIPTION

You receive this message because you specified an incorrect number of memories for a controller

WHAT NEXT

Re-specify the memories for that controller

SEE ALSO

set_mbist_controller (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1521 (error) Invalid Memory "%s" in Controller "%s

DESCRIPTION

You receive this message because you specified a memory with an incompatible number of test ports for the specified controller

WHAT NEXT

Re-specify the memories for that controller

SEE ALSO

set_mbist_controller (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1522 (error) Memory "%s" sizes of controller "%s

DESCRIPTION

You receive this message because you specified a memory which is incompatible with the MBIST IP technology

WHAT NEXT

Do not read the test model for that memory design.

SEE ALSO

set_mbist_controller (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1523 (error) Invalid Read Operation index %d in Port %d of MarchSweep %d of Test %s %s

DESCRIPTION

You receive this message because you specified an incorrect test algorithm that reads invalid data. There are two possible causes:

1) There is a Read Foreground operation after a Write Background or a Read Background after a Write Foreground.

2) The Read Operation is invalid, because the Read was performed before the Write Operation initialized the memory. This usually occurs on the first MarchSweep of the Algorithm when the memory is uninitialized. It may also occur during a MarchSweep that changes the Data Pattern, when the memory is initialized with a different pattern than the one you are trying to read.

WHAT NEXT

Re-specify the algorithm of the test program

SEE ALSO

define_mbist_program (2) **set_mbist_controller** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1524 (error) Multiple WRITE operations on the same port offsets operation index %d in port %d of sequence %d of test %s

DESCRIPTION

You receive this message because you specified an incorect test algorithm. There are simultaneous WRITE operations on ports having the same row and column offsets

WHAT NEXT

Re-specify the algorithm of the test program

SEE ALSO

define_mbist_program (2) **set_mbist_controller** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1525 (error) Diagnosis specific parameter "%s

DESCRIPTION

You receive this message because you have specified a parameter that is valid only for diagnosis modes

WHAT NEXT

Do not specify this parameter in a non-diagnosis mode.

SEE ALSO

set_mbist_run (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **set_mbist_configuration** (2) **set_mbist_controller** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1526 (error) The root clock period must be at least twice than the controller %d clock period when runtime programmability is enabled "%dns" "%dns

DESCRIPTION

You receive this message because you specified a wrong clock period for a controller. The clock of the controller must be at least two times faster than the clock of the root.

WHAT NEXT

Re-specify the controller clock or the root clock

SEE ALSO

set_mbist_run (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **set_mbist_configuration** (2) **set_mbist_controller** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1527 (error) The parameter FAIL_LIMIT is not valid when specifying a runtime programmable test program

DESCRIPTION

You receive this message because you specified the FAIL_LIMIT simultaneously with a runtime test program

WHAT NEXT

Re-specify the parameters

SEE ALSO

set_mbist_run (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **set_mbist_configuration** (2) **set_mbist_controller** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1528 (error) The parameter NUM_FAULTS_SWEEP is valid only when specifying a runtime programmable test

program

DESCRIPTION

You receive this message because you specified the FAIL_LIMIT without specifying a test program

WHAT NEXT

Re-specify the parameters

SEE ALSO

set_mbist_run (2) **or** set_testbench_parameters **(2)** (in **XG** mode)
set_mbist_configuration (2) **set_mbist_controller** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1529 (error) Unknown MBIST Technology. Aborting the command

DESCRIPTION

You receive this message because you did not specify a MBIST Technology.

WHAT NEXT

Specify the MBIST Technology using the "set_mbist_configuration" command with the parameter "-tech"

SEE ALSO

set_mbist_configuration (2) **set_mbist_controller** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1530 (error) Missing test program name

DESCRIPTION

You receive this message because you did not specify a name for the MBIST program definition

WHAT NEXT

Specify a name

SEE ALSO

define_mbist_program (2) **set_mbist_configuration** (2) **set_mbist_controller** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1531 (error) Invalid ValueRange specified for signal %s of DataType %s for the MBIST Technology tech2 in the memory CTL model %s

DESCRIPTION

You receive this message because the signal of the DataType MemAddr declared in the memory CTL model has an invalid ValueRange specified. The ValueRange must be in the range 0 to 2^addr_width-1.

WHAT NEXT

Please set the ValueRange for the signal of the DataType MemAddr in the memory CTL model to be within the acceptable range.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1532 (error) Invalid offsets specified for port section %d in sequence %d of test "%s

DESCRIPTION

You receive this message because you specified a row or column offsets for the first port section or an invalid value for these for the second port section. The row and the column offsets are only valid for the second or more port section, as it represents a value relative to the port section one. The row and column offsets can be 0 or 1.

WHAT NEXT

Specify the correct values for the row and column offsets (for the second port

section, not for the first one).

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1533 (error) Pipeline option can not be activated for memory "%s" because it is disabled in the containing controller "%s

DESCRIPTION

You receive this message because you activated the pipeline option for a memory but not for the controller which tests this memory.

WHAT NEXT

In order to use this option for the memory, you have to enable it first in the controller

SEE ALSO

set_mbist_element (2) **or** set_mbist_wrapper **(2)** (XG) **set_mbist_controller** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1534 (error) Asynchronous Memory "%s

DESCRIPTION

You receive this message because you are using an asynchronous memory with the MBIST technology tech2. This kind of memories are not yet supported by tech2.

WHAT NEXT

You should set the NOTOUCH option for this memory using the set_mbist_element command. Or in XG mode, you should exclude the memory using the set_mbist_configuration command.

SEE ALSO

set_mbist_element (2) **or** set_mbist_wrapper **(2)** (XG) **set_mbist_controller** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1535 (error) Invalid ColumnMultiplexing value "%d" in the MemoryProperties block of memory "%s

DESCRIPTION

You receive this message because you are using MBIST tech2 and the value for ColumnMultiplexing in your memory is invalid or missing. Here are conditions for ColumnMultiplexing:

- ColumnMultiplexing must always be specified - there is no default value.

- The maximum value is 64.

- The value must be a power of 2.

- The value must be an integer divisor of the number of words in your memory.

WHAT NEXT

You should set the NOTOUCH option for this memory using the set_mbist_element command. Or in XG mode, you should exclude the memory using the set_mbist_configuration command.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1536 (error) Man page not used any more

DESCRIPTION

You receive this message because...

WHAT NEXT

Re-specify the algorithm of the test program.

SEE ALSO

define_mbist_program (2) **set_mbist_controller** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1537 (error) Invalid NOP Operation index %d in Port %d of MarchSweep %d of Test %s. NOP not allowed for single-port Algorithms.

DESCRIPTION

You receive this message because you specified an incorrect single-port test algorithm. The NOP Operation is not supported for single-port Algorithms. In this case, the MBIST IP is designed to continuously read or write to the memory.

WHAT NEXT

Re-specify the algorithm of the test program.

SEE ALSO

define_mbist_program (2) **set_mbist_controller** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1538 (error) MBIST clock signal %s was specified without a corresponding scan clock definition.

DESCRIPTION

You receive this message because you specified an MBIST clock without specifying a corresponding scan clock. This is required to identify the clock for DRC clock tracing that maps the clock port to memory clock pins.

WHAT NEXT

Use the **create_test_clock** command to specify a scan clock for the same clock signal.

SEE ALSO

set_mbist_configuration (2) **create_test_clock** (2) **test_default_period** (3)

TEST-1539 (error) Clock period for MBIST clock signal %s is not twice as fast as the test default period.

DESCRIPTION

You receive this message because you either didn’t specify an MBIST clock for the given signal, or you specified an MBIST clock that runs at the same frequency as the tester period (test default period). For MBIST Tech2, the memory clock must be at least twice as fast as the tester clock that drives the MBIST root module. The clock differential is required to support the handshaking between the MBIST root and the MBIST controller(s).

WHAT NEXT

Use the **create_test_clock** command to specify a faster MBIST clock.

SEE ALSO

set_mbist_configuration (2) **create_test_clock** (2) **test_default_period** (3)

TEST-1540 (error) Simultaneous read and write operations from Test "%s" Operation index %d of MarchSweep %d are not supported by the global SimultaneousReadWrite capabilities "%s" of the controller "%s

DESCRIPTION

You receive this message because you specified an incorrect dual-port test algorithm for the respective controller. The memories contained controlled by this controller are not supporting the specified simultaneous read and write operations. Note that when combining memories with both SimultaneousRWStyle LaterVal and FormerVal capabilities, the simultaneous operation beside the read operation for a Write can only be a NOP, a Read DontCare or a Read Expected operation.

WHAT NEXT

Re-specify the algorithm of the test program or choose another test program. Try using Read Expected when not sure about the Read operation value.

SEE ALSO

define_mbist_program (2) **set_mbist_controller** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1541 (error) Expected data in Operation %d in Port %d of MarchSweep %d of Test "%s

DESCRIPTION

You receive this message because you specified a test algorithm which is containing operations using expected data. This is not supported in the current release.

WHAT NEXT

Re-specify the algorithm of the test program or choose another test program.

SEE ALSO

define_mbist_program (2) **set_mbist_controller** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1542 (error) Sequence %d of test %s does not contain enough operations. At least %d operations are required.

DESCRIPTION

You receive this message because you specified a run-time test algorithm with sequences that are too short for the choosen group of memories. When memories are very small, or the MBIST clock is very fast, the test sequence execution can complete before the programming stream has finished loading the next sequence. In this case, the MBIST IP restarts the original sequence and becomes unsynchronized with the protocol. If the estimated required number of operations depasses the maximal number of operations allowed per sequence, that you should try to lower the MBIST clock.

WHAT NEXT

Re-specify the algorithm of the test program or choose another test program.

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **set_mbist_controller** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1543 (error) Port section %d of MarchSweep %d of test

%s contains column offsets specification which is not supported for dual port RAMs from controller "%s

DESCRIPTION

You receive this message because you specified a test algorithm with sequences that contains port sections with column offsets specification for a controller that contains dual port memories with ColumnMultiplexing=1.

WHAT NEXT

Re-specify the algorithm of the test program or choose another test program.

SEE ALSO

define_mbist_program (2) **set_mbist_controller** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1544 (error) Memory signal "%s" of type %s is shared accross ports in the Relation section of the CTL model of memory "%s

DESCRIPTION

You received this message because you specified a CTL model that contains a Relation block incompatible with the MBIST IP technology.

WHAT NEXT

Re-specify the CTL model of the memory.

SEE ALSO

set_mbist_configuration (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1545 (error) Invalid MBIST configuration parameter entry

"%s

DESCRIPTION

You receive this message because you have specified an invalid MBIST configuration parameter. The parameter you specified may be an unrecognized parameter name or value, or it may be invalid for the MBIST technology that you have chosen.

WHAT NEXT

Review the valid parameters for your MBIST technology using the "man set_mbist_configuration" command, and re-specify the parameters.

SEE ALSO

set_mbist_configuration (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1546 (Error) Unable to read ROM initialization file "%s

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode). The command is not able to read the file specified due to errors given before.

WHAT NEXT

Check the content file syntax against the supported standard.

TEST-1547 (Error) Unable to find address and/or data out in CTL model for "%s

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode). The command is not able to find the definition of the data (MemoryData) output signal or/and the address (MemoryAddress) signals in the InternalTest section of the CTL memory model.

WHAT NEXT

Review the CTL memory model file corresponding to the memory instance.

SEE ALSO

read_test_model (2)

TEST-1548 (Error) The memory instance list includes RAM and ROM.

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode). The command cannot manage RAM and ROM instances in the same list because each ROM instance needs a corresponding content file.

WHAT NEXT

Split the **set_mbist_element** command line into two (or more) fB set_mbist_element command lines with different memory instance lists by taking care of not mixing RAM with ROM instances inside each list.

SEE ALSO

set_mbist_element (2) **set_mbist_wrapper** (2) **(for** XG **mode)**

TEST-1549 (Error) Content file list specified for RAM instances.

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode) because the content file list is specified for RAM instances. The content file list has to be specified only for ROM instances.

WHAT NEXT

Delete the content file list or change the RAM instance list to a ROM instance list.

SEE ALSO

set_mbist_element (2) **set_mbist_wrapper** (2) **(XG)**

TEST-1550 (Error) Unable to find content file list.

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode). The command is not able to find the content file list used to describe the ROM instance list.

WHAT NEXT

Add a content file name into the content file list for each ROM instance.

SEE ALSO

set_mbist_element (2) **set_mbist_wrapper** (2) **(XG)**

TEST-1551 (Error) Invalid content file list.

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode) because the content file number is not equal to the ROM instance number.

WHAT NEXT

Review the content file list or the ROM instance list.

SEE ALSO

set_mbist_element (2) **set_mbist_wrapper** (2) **(XG)**

TEST-1552 (error) Invalid value for the RETENTION parameter

DESCRIPTION

You receive this message because you did not specify a correct value for the RETENTION parameter. YES and NO are the only valid values. The default value for RETENTION is NO.

WHAT NEXT

Run "preview_dft" to see the algorithms that support retention test.

SEE ALSO

set_mbist_element (2) **or** set_mbist_wrapper **(2)** (XG) **set_mbist_controller** (2) **set_mbist_configuration** (2)

TEST-1553 (error) No retention test in diagnosis mode.

DESCRIPTION

You receive this message because you specified the RETENTION parameter in diagnosis mode. This version of Memory BIST Compiler supports retention test only in go nogo mode.

WHAT NEXT

Change the diagnosis mode in go nogo mode.

SEE ALSO

set_mbist_element (2) **or** set_mbist_wrapper **(2)** (XG) **set_mbist_controller** (2) **set_mbist_configuration** (2)

TEST-1554 (error) No retention test for Programmable BIST.

DESCRIPTION

You receive this message because you specify the RETENTION parameter for Programmable BIST. This version of Memory BIST Compiler supports retention test only for Synthesis BIST.

WHAT NEXT

Delete the RT_TEST parameter in order to perform retention test for Synthesis BIST.

SEE ALSO

set_mbist_element (2) **or** set_mbist_wrapper **(2)** (XG) **set_mbist_controller** (2) **set_mbist_configuration** (2)

TEST-1555 (Warning) the fail limit value is different from the

maximum number of test in a ROM controller (’%d’ in this case)

DESCRIPTION

You received this message because you specified a fail limit value smaller or greater than the maximum number of ROM controller tests. This fail limit value does not allow to run all the ROM tests (if smaller) or it waste test time (if greater) in the case of only ROM’s controllers.

WHAT NEXT

Review the Memory BIST preview and modify the fail limit value.

SEE ALSO

preview_dft (2)

TEST-1556 (Error) Invalid character %c detected at line %d

DESCRIPTION

This is issued from the command **report_mbist_trace** because the specified file contains illegal characters.

WHAT NEXT

Review the content of the trace file.

SEE ALSO

report_mbist_trace (2)

TEST-1557 (Error) An error occured in the translation of the diagnosis %s packet timer at line %d

DESCRIPTION

This is issued from the command **report_mbist_trace** because the content of the trace file does not match the current design

WHAT NEXT

Review the content of the trace file

SEE ALSO

report_mbist_trace (2)

TEST-1558 (Error) Invalid test algorithm %s used for a DPRAM memory at line %d

DESCRIPTION

This is issued from the command **report_mbist_trace** because the usage of an invalid algorithm has been detected.

WHAT NEXT

Review the content of the trace file or re-specify the algorithm

SEE ALSO

report_mbist_trace (2)

TEST-1559 (Error) Cannot extract field %s from trace file at line %d

DESCRIPTION

This is issued from the command **report_mbist_trace** because the content of the trace file is invalid for the current design

WHAT NEXT

Review the content of the trace file

SEE ALSO

report_mbist_trace (2)

TEST-1560 (Warning) Ignoring the value of Background field in test "%s

DESCRIPTION

You received this message because you specified a run-time test program that contains a value for the Background of the Test program different than zero. For the run-time programmability only the Background value zero is considered.

WHAT NEXT

Review the test program

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode)

TEST-1561 (Error) Unknown diagnosis trace version %d detected at line %d

DESCRIPTION

This is issued from the command **report_mbist_trace** because the content of the trace file is invalid for the current design

WHAT NEXT

Review the content of the trace file

SEE ALSO

report_mbist_trace (2)

TEST-1562 (Error) Invalid value for the memory ID field %d detected at line %d

DESCRIPTION

This is issued from the command **report_mbist_trace** because the content of the

trace file is invalid for the current design. The memory ID should be smaller than the total number of memories from the specified controller.

WHAT NEXT

Review the content of the trace file

SEE ALSO

report_mbist_trace (2)

TEST-1563 (Error) Invalid value for the packet ID field %d detected at line %d

DESCRIPTION

This is issued from the command **report_mbist_trace** because the content of the trace file is invalid for the current design. The packet ID field specifies the memory type SRAM or ROM.

WHAT NEXT

Review the content of the trace file

SEE ALSO

report_mbist_trace (2)

TEST-1564 (Error) Can not recover the test algorithm index %d of controller index %d from the current CTL model at line %d

DESCRIPTION

This is issued from the command **report_mbist_trace** because the content of the trace file is invalid for the current design. The packet ID field specifies the memory type SRAM or ROM.

WHAT NEXT

Review the content of the trace file

SEE ALSO

report_mbist_trace (2)

TEST-1565 (Error) The specified test program is not compatible with the controller index %d

DESCRIPTION

You received this message because you specified an SP-RAM test algorithm for a DP-RAM controller or vice versa.

WHAT NEXT

Specify a compatible test algorithm

SEE ALSO

report_mbist_trace (2)

TEST-1566 (Error) Operation %s is not supported in SPRAM test program "%s

DESCRIPTION

You received this message because you specified an Expected or DontCare Operation types inside a SP-RAM test algorithm.

WHAT NEXT

Rewrite the SP-RAM test algorithm without using Expected or DontCare Operation types.

SEE ALSO

define_mbist_program (2)

TEST-1567 (Error) Invalid %s Operation type for Write Operation %d of port %d in MarchSweep %d of test program

"%s

DESCRIPTION

You received this message because you specified an Expected or DontCare Operation types for a Write Operation.

WHAT NEXT

Rewrite the test algorithm without using Write Expected or Write DontCare Operation.

SEE ALSO

define_mbist_program (2)

TEST-1568 (Warning) Grouping Memories with incompatible R/W ports (Memory "%s" simultaneous read/write style is not compatible with the Controller "%s

DESCRIPTION

You received this message because you grouped memories with different simultaneous read/write capabilities in the same controller. This limits the simultaneous read/write test capabilities of the respective controller.

WHAT NEXT

Regroup the memories in different controllers.

SEE ALSO

set_mbist_controller (2) **preview_dft** (2)

TEST-1569 (Error) %d port memory "%s" is assigned to the controller "%s

DESCRIPTION

You received this message because you tried to group multiport memories in a controller with run-time programability capabilities.

WHAT NEXT

Regrop the memories in different controllers.

SEE ALSO

set_mbist_controller (2) **preview_dft** (2)

TEST-1570 (Error) The specified algorithm contains PAUSE sequences and can not be used for run-time programmability

DESCRIPTION

You received this message because you tried use a test program containing PAUSE sequences in run-time mode

WHAT NEXT

Respecify the test program

SEE ALSO

set_mbist_run (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **report_mbist_trace** (2) **define_mbist_program** (2)

TEST-1571 (Error) Cannot use content_file or content_format arguments

DESCRIPTION

You received this message because you tried to specify the content_file or content_format as arguments of set_mbist_element (or set_mbist_wrapper in XG mode). Those arguments are valid only for Memory BIST Compiler Tech 2

WHAT NEXT

Delete content_file or content_format arguments if you are using Memory BIST Compiler Tech 1 otherwise set the Memory BIST Compiler Tech 2 by using the set_mbist_configuration command

SEE ALSO

set_mbist_configuration (2)

TEST-1572 (error) %s Port %d of memories inside controller "%s" can not perform operation type %s index %d from Port section %d of MarchSweep sequence %d of test program "%s

DESCRIPTION

You receive this message because you specified a test algorithm that tries to Read from a Write Only memory port or to Write in a Read Only memory port. The controller global Read/Write properties corespond to the lowest capable memory inside that controller.

WHAT NEXT

Specify another test program

SEE ALSO

define_mbist_program (2) **set_mbist_controller** (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode)

TEST-1573 (error) misr_size parameter value %d must be in the range 2 to 128.

DESCRIPTION

You receive this message because you have specified an invalid misr_size parameter value.

WHAT NEXT

Specify a misr_size that is in the range 2 to 128.

SEE ALSO

set_mbist_element (2) **or** set_mbist_wrapper **(2)** (XG)

TEST-1574 (error) Test with no Background "%s" is not compatible with RAM controller "%s

DESCRIPTION

You receive this message because you have specified a test program that does not contain a background specification for a RAM controller. This kind of tests can be used only with controller of type ROM.

WHAT NEXT

Re-specify the test programs for that controller

SEE ALSO

set_mbist_controller (2) **define_mbist_program** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1575 (error) No contents file specified for ROM instance %s.

DESCRIPTION

You must specify the contents file for every ROM instance with the **set_mbist_element** (or **set_mbist_wrapper** in XG mode) command. The contents are used to calculate the expected MISR signature.

WHAT NEXT

Use the set_mbist_element command to specify the contents file for this ROM instance. If you think this memory is being erroneously treated as a ROM, check the model to make sure it has a data input port.

SEE ALSO

set_mbist_element (2) **or** set_mbist_wrapper **(2)** (XG)

TEST-1576 (error) Could not find any valid memories for MBIST

insertion.

DESCRIPTION

You received this message because the MBIST dft configuration is enabled, but no memories were identified for testing. Memories are identified through their CTL test models. The flow for using these models depends on which dc_shell mode you are using.

```
Flow for dcsh and dctcl modes
-----------------------------
1) Enable test models
dc_shell> set test_use_test_models true

2) Use the read_test_model command to load test models for all
   of your memory designs.

3) Link your design after you have read the test models.

Flow for dcxg mode
------------------
1) Enable test models
dc_shell> set test_xg_use_models true

2) Use the read_test_model command to load test models for all
   of your memory designs.

3) Use the use_test_model command to use the memory test models instead
   of the gate-level design.

4) Link your design at any time.
```

WHAT NEXT

Use the correct test model flow for your memory designs.

SEE ALSO

read_test_model (2), **use_test_model** (2), **set_dft_configuration** (2), **set_mbist_element** (2) **or** set_mbist_wrapper **(2)** (XG)

TEST-1577 (error) Memory %s is a %s, but controller %s can only test %ss.

DESCRIPTION

You received this message because you attempted to test RAMs and ROMs with the same

controller. A given controller can test either SPRAMs, DPRAMs or ROMs.

WHAT NEXT

Use the /fBset_mbist_controller/fP command to assign RAMs and ROMs to separate controllers.

SEE ALSO

set_mbist_controller (2)

TEST-1578 (error) Test "%s" is not compatible with ROM controller "%s

DESCRIPTION

You receive this message because you have specified a test program that contains a background specification, which cannot be used by a ROM controller. ROM Tests must contain only an Algorithm.

WHAT NEXT

Re-specify the test programs for that controller

SEE ALSO

set_mbist_controller (2) **define_mbist_program** (2) **set_mbist_configuration** (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1579 (Error) Invalid value for the controller ID field %d detected at line %d

DESCRIPTION

This is issued from the command **report_mbist_trace** because the content of the trace file is invalid for the current design. The controller ID should be smaller than the total number of controllers from the specified design.

WHAT NEXT

Review the content of the trace file

SEE ALSO

report_mbist_trace (2)

TEST-1580 (error) Scramble map %s is an invalid map type in the ScrambleMaps section of the CTL model of memory %s. The left-hand side of the scramble map must be LA (logical address).

DESCRIPTION

You received this message because you specified a CTL model with a ScrambleMaps block that is incompatible with the MBIST IP technology. Only topological address to logical address maps are supported. These maps are of the form:

LA[n] = TA[n];

WHAT NEXT

Re-specify the ScrambleMaps block of the CTL model of the memory.

If your memory requires data scramble maps, Memory BIST Compiler can not support your memory at this time. You should not load this memory model and leave the memory un-BISTed.

SEE ALSO

set_mbist_configuration (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1581 (error) Scramble map %s has an incompatible right-hand side term %s in the ScrambleMaps section of the CTL model of memory %s.

DESCRIPTION

You received this message because you specified a CTL model with a semantically incorrect ScrambleMaps block. There can be two causes for this error.

1) You specified a data bit (LD or TD) on the right-hand side of an address expression (LA). Address expressions can only have address terms on the right-hand side.

2) You specified the same topology (either L or T) on both sides of the assignment.

If the left-hand side is logical, all of the right-hand side terms must be topological.

WHAT NEXT

Re-specify the ScrambleMaps block of the CTL model of the memory.

SEE ALSO

set_mbist_configuration (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1582 (error) Scramble map %s is repeated in the ScrambleMaps section of the CTL model of memory %s.

DESCRIPTION

You received this message because you specified a CTL model with a ScrambleMaps block that contains a repeated scramble map. Each left-hand side term can be used only once.

WHAT NEXT

Remove the redundant map from the ScrambleMaps block of the CTL model of the memory.

SEE ALSO

set_mbist_configuration (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1583 (error) Scramble map term %s index is out of range in the ScrambleMaps section of the CTL model of memory %s. The index value must be in the range 0 to %d.

DESCRIPTION

You received this message because you specified a CTL model with a semantically incorrect ScrambleMaps block. The bit index refers to an address or data signal that doesn’t exist.

WHAT NEXT

Re-specify the ScrambleMaps block of the CTL model of the memory.

SEE ALSO

set_mbist_configuration (2) **insert_dft** (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1584 (error) Invalid MaskWrite Operation in test "%s

DESCRIPTION

You received this message because you specified a test program that contains a incorrect sequence. This sequence does not support MaskWrite Operations. This operation is only allowed in the FixedAddress blocks.

WHAT NEXT

Re-specify the test program

SEE ALSO

define_mbist_program (2) **preview_dft** (2),

TEST-1585 (error) Specified test program contains FixedAddress sequences which are not yet supported in the runtime programmable BIST

DESCRIPTION

You received this message because you specified a test program that contains FixedAddress sequences for the runtime programmable BIST. Only the Synthesis BIST supports the FixedAddress sequences.

WHAT NEXT

Re-specify the test program

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG**

mode) **report_mbist_trace** (2)

TEST-1586 (error) Specified test program "%s

DESCRIPTION

You received this message because you specified a test program that contains non zero Offset specifications inside an incorrect sequence. Only the MarchSweep sequences support column and row offsets.

WHAT NEXT

Re-specify the test program

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **report_mbist_trace** (2)

TEST-1587 (error) Specified test program "%s

DESCRIPTION

You received this message because you specified a test program that contains DontCare Operations inside a FixedAddress sequence. Only the MarchSweep sequences support DontCare Operations.

WHAT NEXT

Re-specify the test program

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **report_mbist_trace** (2)

TEST-1588 (error) Test program "%s

DESCRIPTION

You received this message because you specified a test program that contains

unsupported Mask type operation. Only Masks of type BinVal are supported for now.

WHAT NEXT

Re-specify the test program

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **report_mbist_trace** (2)

TEST-1589 (error) Invalid Mask size %d specified in test program "%s

DESCRIPTION

You received this message because you specified a test program that contains invalid Masks. The size of the Mask statement must not exceed the maximum supported.

WHAT NEXT

Re-specify the test program

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **report_mbist_trace** (2)

TEST-1590 (error) Invalid polarity for the Operation %d in Port %d of Sequence %d of test "%s" %s. The only accepted polarity for this Operation is "Expected

DESCRIPTION

You received this message because you specified an invalid test program. The Read Operations must respect the last written polarity. After a MaskWrite operation only a Read Expected is accepted.

WHAT NEXT

Re-specify the test program

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **report_mbist_trace** (2)

TEST-1591 (Warning) Replacing Read Expected Operation %d from Port %d sequence %d of test "%s

DESCRIPTION

You received this message because you specified an invalid test program. You are using a Read Expected operation before an initial write. You should always start with a Write or a global masked MaskWrite if the respective sequence is the first one in the algorithm or if there are changes in the pattern style, address value or sequence type.

WHAT NEXT

Re-specify the test program

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **report_mbist_trace** (2)

TEST-1592 (Error) Invalid MaskWrite Operation index %d in sequence %d of test %s %s after an Address change

DESCRIPTION

You received this message because you specified an invalid test program. A Write or a global masked MaskWrite operation is required after a Address value change before using MaskWrite. You should always start with a Write or a global masked MaskWrite if the respective sequence is the first one in the algorithm or if there are changes in the pattern style, address value or sequence type.

WHAT NEXT

Re-specify the test program

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG**

mode) **report_mbist_trace** (2)

TEST-1593 (Error) Invalid MaskWrite Operation index %d in sequence %d of test %s %s after a sequence type change

DESCRIPTION

You received this message because you specified an invalid test program. A Write or a global masked MaskWrite operation is required after a sequence type change before using MaskWrite. You should always start with a Write or a global masked MaskWrite if the respective sequence is the first one in the algorithm or if there are changes in the pattern style, address value or sequence type.

WHAT NEXT

Re-specify the test program

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **report_mbist_trace** (2)

TEST-1594 (Error) Wrong Memory "%s

DESCRIPTION

You received this message because you specified more than one mask in the CTL model of the memory. You must use only one specification, either use a write enable bus with size greater than 1 (or 2 for DPRAMs), either use a signal of type "User snps_memory_write_mask both in the same time.

WHAT NEXT

Re-specify the test program

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **report_mbist_trace** (2)

TEST-1595 (Error) FixedAddress statements are not supported

in ROM like algorithm "%s

DESCRIPTION

You received this message because you specified FixedAddress statements inside an algorithm that does not contain Write operations, which is most likely a ROM test program. FixedAddress statements are only supported for RAMs for now.

WHAT NEXT

Re-specify the test program

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **report_mbist_trace** (2)

TEST-1596 (Error) Memory "%s

DESCRIPTION

You received this message because you specified a memory to be part of more controllers in the same time. This is not allowed.

WHAT NEXT

Re-specify the controller configuration

SEE ALSO

set_mbist_controller (2)

TEST-1597 (error) No pause in controller’s hardwired algorithms.

DESCRIPTION

You receive this message because you set the RETENTION parameter to ON but there are no controller’s hardwired algoriths with pause.

WHAT NEXT

Look at the Memory BIST preview and specify an algorithm with pause for at least one controller.

SEE ALSO

preview_dft (2) **set_mbist_controller** (2)

TEST-1599 (error) Cannot specify AddressValue statements of type Absolute for test "%s

DESCRIPTION

You receive this message because you specified an AddressValue statement of type Absolute in the test program. This option is not yet supported in this release.

WHAT NEXT

Use Min or Max options instead.

SEE ALSO

define_mbist_program (2)

TEST-1600 (error) Can not enable "%s" and "%s" in the same time for memory "%s

DESCRIPTION

You receive this message because you specified an sequential bypass when the shadow logic is disabled. Shadow logic must be enabled in order to use the sequential bypass.

WHAT NEXT

Enable the shadow logic for the respective memory.

SEE ALSO

set_mbist_element (2) **or** set_mbist_wrapper **(2)** (XG)

TEST-1601 (error) Cannot architect load compressor with the given parameters: scan_inputs = %d and minimum_compression = %d. You should either increase the number of scan-inputs or decrease the compression factor.

DESCRIPTION

You receive this message because load compressor architecting failed for the given set of scan inputs and for the given minimum compression. The number of scan-inputs is derived from set_scan_configuration -chain_count. The minimum_compression is specified with the set_scan_compression_configuration command. The number of chains in the scan-compression mode is calculated based on these numbers.

WHAT NEXT

You should either increase the number of scan-inputs or decrease the compression factor.

SEE ALSO

set_scan_configuration (2) **set_scan_compression_configuration** (2) **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1602 (warning) Architecting of %s compressor failed with the given set of parameters. The number of Internal Scan Chains are reduced to %d.

DESCRIPTION

You receive this message because compressor architecting is not possible for the given set of paramemters.

WHAT NEXT

Load compressor architecting depends on number of scan input pins and number of internal chains. Please try either by increasing the number of scan inputs or by reducing the minimum_compression value.

Unload compressor architecting depends on the number of scan-ouputs, number of internal chains and and whether a compressor with diagnostics capability is being built. Please increse either the number of outputs or reduce the minimum_compression or disable compressed diagnositics with *set_scan_compression_configuration* command. Please note that disabling compressed diagnostics may also result in lower coverage.

Please rerun *preview_dft* to verify if the compressors with new parameters can be architected.

SEE ALSO

set_scan_configuration (2) **set_scan_compression_configuration** (2) **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1603 (warning) Compressor generated may have lower diagnostics precision.

DESCRIPTION

You receive this message because given the resources, a compressor cannot be architected to provide full diagnostics support. The compressor that is architected will have lower diagnostics precision.

If the -force_diagnosis switch of set_scan_compression_configuration is set to true, this becomes an error condition and the command will exit.

WHAT NEXT

Unload compressor architecting depends on the number of scan-ouputs, number of internal chains and and whether a compressor with diagnostics capability is being built. Please increse either the number of outputs or reduce number of internal chains or disable compressed diagnositics with *set_scan_compression_configuration* command. Please note that disabling compressed diagnostics may also result in lower coverage.

Please rerun *preview_dft* to verify if the compressors with new parameters can be architected.

SEE ALSO

set_scan_configuration (2) **set_scan_compression_configuration** (2) **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1604 (error) Scan Compression requires minimum of %d Scan Inputs. Design has %d Scan Inputs.

DESCRIPTION

You receive this message because architecting for scan compression failed for the given set of inputs.

WHAT NEXT

You should either increase the number of scan-inputs or decrease the compression factor.

SEE ALSO

set_scan_configuration (2) **set_scan_compression_configuration** (2) **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1605 (error) Equal number of decompressor inputs and outputs ’%d’

DESCRIPTION

You receive this message because architecting for scan compression resulted in equal number of decompressor inputs and outputs. This can be because the same number of chains was specified for the scan compression mode and reconfigurable scan mode

WHAT NEXT

Check the chain count specifications

SEE ALSO

set_scan_configuration (2) **set_scan_compression_configuration** (2) **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1606 (Error) The parameter "%s" of the decompressor IP does not match the one computed during scan compression architecting.

DESCRIPTION

You receive this message because architecting for scan compression failed for the given decompressor IP.

WHAT NEXT

Some options of the scan configuration and of the scan compression configuration should not be changed between the first pass run generating the decompressor and decompressor IPs and the second pass run loading these IPs and implementing them.

Option modifications might have an impact on the IP parameters, structures and the scan compression architecting will fail.

SEE ALSO

set_scan_configuration (2) **set_scan_compression_configuration** (2) **set_dft_insertion_configuration** (2) **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1607 (Error) The parameter "%s" of the compressor IP does not match the one computed during scan compression architecting.

DESCRIPTION

You receive this message because architecting for scan compression failed for the given compressor IP.

WHAT NEXT

Some options of the scan configuration and of the scan compression configuration should not be changed between the first pass run generating the decompressor and decompressor IPs and the second pass run loading these IPs and implementing them. Option modifications might have an impact on the IP parameters, structures and the scan compression architecting will fail.

SEE ALSO

set_scan_configuration (2) **set_scan_compression_configuration** (2) **set_dft_insertion_configuration** (2) **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1608 (Warning) Decompressor/Compressor IP parameters are not available in the decompressor/compressor IP model to perform parameter validation.

DESCRIPTION

You receive this message because architecting for scan compression cannot perform IP parameter validation for the decompressor and the compressor.

WHAT NEXT

While generating the IP RTL and the IP model, IP parameters should be part of the IP model in order to validate the parameters while architecting the scan compression.

SEE ALSO

set_scan_configuration (2) **set_scan_compression_configuration** (2) **set_dft_insertion_configuration** (2) **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1609 (Warning) ip_parameter %s is repeated. The accepted value is

DESCRIPTION

You receive this message because you are overriding the value that you previously specified for the given parameter. This occurs when you repeat a parameter within the same command, or accross different commands for the same controller.

WHAT NEXT

You can avoid this message by specifying each parameter only once per controller.

SEE ALSO

set_mbist_controller (2) **set_mbist_element** (2) **or** set_mbist_wrapper **(2)** (XG)

TEST-1610 (Warning) Cell %s/%s in chain %s not found.

DESCRIPTION

You receive this message because the preview_dft command showed the given cell, but it does not exist in the netlist. This happens when the CTL model for the IP block that contains the cell does not accurately predict some synthesis optimizations. This discrepancy may cause some slightly non-optimal scan chain balancing, because it is based on the DFT plan that is shown in preview_dft instead of the actual netlist. This issue has no effect on scan fault coverage.

WHAT NEXT

No action is required.

SEE ALSO

insert_dft (2), **preview_dft** (2).

TEST-1611 (error) Parameter %s is invalid, because memory-driven specification mode is enabled.

DESCRIPTION

Memory-driven specification mode was enabled by the test_mbc_memory_driven_spec environment variable. This imposes a requirement on the memory models to describe all the tests for that memory.

WHAT NEXT

All memory models should contain complete test specifications. You can not specify any tests with the **set_mbist_controller** command. This means all test parameters (ie test0, test1, ...) are invalid.

SEE ALSO

set_scan_configuration (2) **set_dft_insertion_configuration** (2) **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1612 (error) Memory %s has %d tests defined in the CTL model. The valid range is 1 to %d tests for memory-driven specification mode.

DESCRIPTION

Memory-driven specification mode was enabled by the test_mbc_memory_driven_spec environment variable. This imposes a requirement on the memory models to describe all the tests for that memory. In this case, your memory has the wrong number of tests in the MemoryTests block.

WHAT NEXT

Either add or remove tests from the MemoryTests block of the specified memory to make it within the supported range.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_mbist_configuration** (2), **set_mbist_controller** (2), **test_mbc_memory_driven_spec** (3), **test_varbiables** (3).

TEST-1613 (error) Memory %s is incompatible with controller %s, because its MemoryTests block does not match other memories that share the controller. This is a restriction of memory-driven specification mode.

DESCRIPTION

Memory-driven specification mode was enabled by the test_mbc_memory_driven_spec environment variable. This imposes a requirement that memories can only share a controller when their MemoryTests blocks are identical. They must contain the same tests in the same order.

WHAT NEXT

Change your memory to controller assignments using the **set_mbist_controller** command, so that only memories with identical MemoryTests blocks share the same controller. If the required change is not obvious, you should omit all memory to controller assignments and use the **preview_dft** command to show which memories can share the same controller.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_mbist_configuration** (2), **set_mbist_controller** (2), **test_mbc_memory_driven_spec** (3), **test_varbiables** (3).

TEST-1614 (error) ROM controller %s has %d tests. The maximum number is %d.

DESCRIPTION

You specified more tests than the MBIST ROM controller can support.

WHAT NEXT

Use the **remove_mbist_configuration** command to remove the extra tests (along with any other MBIST specifications you may have made). Then specify only the supported number of tests.

SEE ALSO

set_mbist_configuration (2), **remove_mbist_configuration** (2), **set_mbist_controller** (2).

TEST-1615 (error) Invalid RepairResource %s in the CTL model for memory %s. Reason: %s.

DESCRIPTION

The specified RepairResource block of the given memory model does not comply with Synopsys standards. This is usually caused by an error in creating the model, or a repair configuration that is not supported by Memory BIST Compiler.

Each message includes a specific reason for the error. There are many reasons why you get this message, so the reasons are identified with a letter a through v. You can look up the reason letter in the following section to find more details about the error.

a) An unexpected character was found in the AddressMap.
   For row repair:
     - the page and column address bits must be x
     - the row address that corresponds to the row repair address must be r, with log2 (width) LSBs optionally x
     - the bank address must be 1 or 0 to select the bank that is associated with this row
   For column repair:
     - the page address bits (if any) must all be r
     - the column address bits must be all r, but log2 (width) column LSBs must be x.
b) The only supported RepairTypes are Row, Column and DataBit. Page repair is not supported.
c) AccessCells is for memories where the repair resources are accessed through a serial chain. This is not supported.
d) All signals in the AccessSignals list must be declared as DataType User snps_repair_enable or snps_repair_address in the anonymous CTL block. Column and DataBit resources can also have DataType snps_repair_data_bit.
e) AccessSignals must be unique to each resource. They can not be members of multiple repair resources.
f) The AccessSignals list must contain a signal that is declared as DataType User snps_repair_enable in the anonymous CTL block.
g) The AddressMap shows how each address bit is used by or affected by the repair resource. You must either provide a complete map with all address bits, or omit the AddressMap and use the default.
h) For row resources, the AccessSignals must contain an r for every repair address bit. When the repair address is shorter than the row address, the remaining LSBs must in the AddressMap must be x.
i) The DataBitMap is not used by row repair resources, and must be omitted.
j) Only row resources of width 1 or 2 are supported.
k) When row resources are allocated on a per bank basis, the width must be 1. Double rows are not supported in this case.

l) When row resources are allocated on a per bank basis, the AddressMap must be included to show the bank association for this row resource. This is accomplished by putting 1s and 0s in the bank bits of the AddressMap.
m) When row resources are allocated on a per bank basis, each bank value in the AddressMap must be unique. Multiple rows in the same bank are not supported.
n) Any signal that is declared in an AccessSignals list of a RepairResource must only be declared in the Internal block of the anonymous mode, because their function is not mode dependent.
o) Column resource width must be a power of 2 less than or equal to the value of ColumnMultiplexing.
p) For column resources where the memory has a page address, all of the page bits in the AddressMap must be r, and the remainder of the AddressMap must be x.
q) For column resources where the memory has a page address, the width must be equal to the value of ColumnMultiplexing. MBC only supports replacing a full bit's worth of columns in each page.
r) For column resources, the number of repair data bits signals in the AccessSignals be ceil (log2 (1 bits in the DataBitMap)). This means that you must have exactly enough repair data bits to encode the target data bit within the bank of this resource.
s) For column resources, the DataBitMap must contain either 1s for each data bit (all Fs), or partition the data bus into two contiguous banks (i.e. one column resource has F0 and the other has 0F).
t) When column resources are allocated on a per bank basis, each DataBitMap value must be unique. Multiple column resources in the same bank are not supported.
u) For databit resources, the AddressMap should not be specified.
v) For databit resources, width, if specified, can not be greater than 1.
x) For databit resources, snps_repair_address signals should not be specified in th
e AccessSignals list.
y) Each repair signal specified in the AccessSignals list should have a unique repa
ir type.
z) For databit resources, the DataBitMap is optional and if specified must be enabl
ed (set to F..F value).

WHAT NEXT

Edit your memory model to comply with the Synopsys memory model standards. If your memory uses unsupported repair features, you should model the repair resource signals as DataType Constant to make Memory BIST Compiler pass them directly through the wrapper. In this case, it is the user's responsibility to disable these signals externally.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

TEST-1616 (error) Invalid value for the REPAIR_ENABLE or

REPAIR_VERIFY or REPAIR_UNLOAD parameter

DESCRIPTION

You receive this message because you did not specify a correct value for the REPAIR_ENABLE or REPAIR_VERIFY or REPAIR_UNLOAD parameter. YES and NO are the only valid values. The default value is NO.

WHAT NEXT

Run "preview_dft" to see if the system supports repair.

SEE ALSO

set_mbist_element (2) **or** set_mbist_wrapper **(2)** (XG) **set_mbist_controller** (2) **set_mbist_configuration** (2)

TEST-1617 (error) Test Program %s with Invalid OneDimensionalAddress Pattern specification in sequence %d

DESCRIPTION

You received this message because you specified a test program that contains a Pattern different than Solid in a OneDimensionalAddress sequence.

WHAT NEXT

Re-specify the test program

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (XG) **report_mbist_trace** (2)

TEST-1618 (error) Test Program "%s

DESCRIPTION

You received this message because you specified a test program that contains either a CountStyle PageOnly outside a OneDimensionalAddress sequence or a CountStyle different than PageOnly inside a OneDimensionalAddress sequence.

WHAT NEXT

Re-specify the test program

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (XG) **report_mbist_trace** (2)

TEST-1619 (error) The value specified with the %s parameter mismatches with the one represented using %s characters in the AddressOrg MemoryProperties field for %s

DESCRIPTION

You received this message because you are using multiple specifications for the same memory property with different values. RowCount, PageCount and BankCount parameters can be determined from the AddressOrg field.

WHAT NEXT

Re-specify the memory parameters in the MemoryProperties section of the memory CTL.

SEE ALSO

preview_dft (2) **insert_dft** (2)

TEST-1620 (error) Invalid value for %s parameter of memory %s, the valid range for this parameter is [1..%d]

DESCRIPTION

You received this message because the value of the specified parameter is not in the valid range.

WHAT NEXT

Re-specify the memory parameters in the MemoryProperties section of the memory CTL.

SEE ALSO

preview_dft (2) **insert_dft** (2)

TEST-1621 (error) Mismatch between the number of 'C' characters in AddressOrg field of MemoryProperties and the ColumnMultiplexing value for memory %s

DESCRIPTION

You received this message because the number of 'C' characters from AddressOrg should be equal to round up from log2(ColumnMultiplexing).

WHAT NEXT

Re-specify the memory parameters in the MemoryProperties section of the memory CTL.

SEE ALSO

preview_dft (2) **insert_dft** (2)

TEST-1622 (error) RowCount or AddressOrg and ValueRange can not be used together in memory %s

DESCRIPTION

You received this message because you used two parameters that can not be used together, as their values may be conflicting. Please use only one of them.

RowCount and AddressOrg are the preferred address specification. ValueRange is supported for backward compatability, but should not be used in new memory models.

WHAT NEXT

Re-specify the memory parameters in the MemoryProperties section of the memory CTL. It is best to remove ValueRange and use RowCount and AddressOrg as your address specification.

SEE ALSO

preview_dft (2) **insert_dft** (2)

TEST-1623 (error) Invalid length for the AddressOrg parameter of memory %s (%d instead of %d)

DESCRIPTION

You received this message because you specified a wrong AddressOrg string in the MemoryProperties section of the memory CTL.

WHAT NEXT

Re-specify the memory parameters in the MemoryProperties section of the memory CTL.

SEE ALSO

preview_dft (2) **insert_dft** (2)

TEST-1624 (error) AddressOrg field must be specified in the MemoryProperties CTL model of the memory %s as %s

DESCRIPTION

You received this message because you forgot to specify the AddressOrg field in the MemoryProperties of the memory CTL model. For the specified case, this field is mandatory.

WHAT NEXT

Re-specify the memory parameters in the MemoryProperties section of the memory CTL.

SEE ALSO

preview_dft (2) **insert_dft** (2)

TEST-1625 (warning) Background Pattern field is ignored for test %s as the Background Type is set to %s

DESCRIPTION

You received this message because the Background Pattern field value is ignored for the specified Background Type. The pattern values are generated automatically

internally in this case. When Background Type is Topological, a background equal to zero is used internally to perform the FixedAddress sequences.

WHAT NEXT

None

SEE ALSO

preview_dft (2) **insert_dft** (2) **define_mbist_program** (2)

TEST-1626 (error) Background Type field value of test %s is not yet supported

DESCRIPTION

You received this message because you specified an unsupported Background Type value

WHAT NEXT

Re-specify the Background Type as Topological or AlgorithmBased

SEE ALSO

preview_dft (2) **insert_dft** (2) **define_mbist_program** (2)

TEST-1627 (error) Cannot run all the MBIST cores in parallel because some of them share the same diagnosis output ports.

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because the CONTROL_SEL_<CORE_ID> parameter is not specified. In fact some cores share the same diagnosis output port; so they cannot be run in parallel in the case of diagnosis mode or ROMs controllers with external signature comparison in go_nogo mode. By default, all MBIST cores are run in parallel.

WHAT NEXT

Run "preview_dft" to see how MBIST core are mapped and use the CONTROL_SEL_<CORE_ID> parameter of the command **set_mbist_run** (or **set_testbench_parameters** in XG mode).

SEE ALSO

preview_dft (2), **set_mbist_run** (2).

TEST-1628 (error) CNTRL_SEL pararameter cannot be used in the case of Core Integration

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because the CNTRL_SEL parameter is not valid in the case of Core Integration.

WHAT NEXT

Use CONTROL_SEL_<CORE_ID> parameter if you want select a subset of controllers of one specific MBIST core.

SEE ALSO

set_mbist_run (2)

TEST-1629 (error) invalid CORE_ID value of CONTROL_SEL_<CORE_ID> parameter

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because the <CORE_ID> value specified in the CONTROL_SEL_<CORE_ID> parameter is not valid.

WHAT NEXT

Run "preview_dft" to see how MBIST cores are mapped.

SEE ALSO

preview_dft (2), **set_mbist_run** (2).

TEST-1630 (error) CONTROL_SEL_<CORE_ID> parameter

can be used only with Core Integration

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because the CONTROL_SEL_<CORE_ID> parameter is specified not in the case of Core Integration.

WHAT NEXT

Use the CNTRL_SEL parameter of **set_mbist_run** (or **set_testbench_parameters** in XG mode) if you want to select a subset of controllers in the case of model level protocol.

SEE ALSO

preview_dft (2), **set_mbist_run** (2).

TEST-1631 (error) REPAIR_ENABLE cannot be set to yes when a subset of controllers is specified or when Run Time Programmable BIST is selected

DESCRIPTION

You receive this message because you set the REPAIR_ENABLE parameter to YES in the case of subset of controller selection or Run Time Programmable BIST.

WHAT NEXT

Change the set_mbist_run command parameter setting.

SEE ALSO

set_mbist_run (2)

TEST-1632 (error) Test program %s contains sequences that requires that controller %s has enable_page_testing set to

TRUE

DESCRIPTION

Test programs containing sequences of type OneDimensionalAddress can only be assigned to controllers that has the Page testing enabled.

WHAT NEXT

Enable the page testing for the respective controller.

SEE ALSO

set_mbist_controller (2),

TEST-1633 (error) At least one memory containing AddressOrg property must be assigned to controller %s as %s is required

DESCRIPTION

When the page testing for a controller is required, at least one of his assigned memory models should have an AddressOrg statement.

WHAT NEXT

Specify the AddressOrg in the MemoryProperties block of the memory models.

SEE ALSO

set_mbist_controller (2),

TEST-1634 (error) Invalid position for the ’C’ characters in AddressOrg field of MemoryProperties for memory %s

DESCRIPTION

You received this message because the ’C’ characters should be the LSBs of the AddressOrg specified field.

WHAT NEXT

Re-specify the memory parameters in the MemoryProperties section of the memory CTL.

SEE ALSO

preview_dft (2) **insert_dft** (2)

TEST-1635 (error) Page testing is not allowed for ROM controller %s

DESCRIPTION

You received this message because the page testing is not allowed for ROM controllers

WHAT NEXT

Re-specify the controller parameters

SEE ALSO

preview_dft (2) **insert_dft** (2)

TEST-1636 (error) Run-time programability is not allowed for ROM controller %s

DESCRIPTION

You received this message because the run-time programability is not allowed for ROM controllers

WHAT NEXT

Re-specify the controller parameters

SEE ALSO

preview_dft (2) **insert_dft** (2)

TEST-1637 (error) invalid DIAG_OUT parameter value: only TDO and SCAN_OUT are valid values

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because you specified a wrong value of the DIAG_OUT parameter. Only TDO and SCAN_OUT are valid values.

WHAT NEXT

Modify the value of the DIAG_OUT parameter.

SEE ALSO

set_mbist_run (2).

TEST-1638 (error) Cannot specify TDO port to stream out diagnosis data in the case of multiple MBIST core run

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because the DIAG_OUT parameter is set to TDO. In fact the TDO BSD port cannot be used to stream out diagnosis data in the case of multiple MBIST cores run in parallel.

WHAT NEXT

Run "preview_dft" to see how MBIST core are mapped and use the CONTROL_SEL_<CORE_ID> parameter or modify the DIAG_OUT parameter value of the command **set_mbist_run** (or **set_testbench_parameters** in XG mode).

SEE ALSO

preview_dft (2), **set_mbist_run** (2).

TEST-1639 (error) Cannot set REPAIR_ENABLE to YES and

REPAIR_VERIFY to NO in diagnosis mode

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because you set REPAIR_ENABLE to YES and REPAIR_VERIFY to NO in diagnosis mode. In fact, you have to set REPAIR_ENABLE and REPAIR_VERIFY to YES to generate a correct STIL test bench in diagnosis mode.

WHAT NEXT

Set the REPAIR_VERIFY parameter value to YES in the command **set_mbist_run** (or **set_testbench_parameters** in XG mode).

SEE ALSO

set_mbist_run (2).

TEST-1640 (error) Can not specify the diagnosis output mode to tdo when the boundary scan is not implemented

DESCRIPTION

You received this message because you specified a diagnosis output mode which is not implemented in your current configuration. The tdo is only valid when boundary scan is present.

WHAT NEXT

Specify another diagnosis output mode.

SEE ALSO

preview_dft (2), **report_mbist_trace** (2), **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (XG **mode)**

TEST-1641 (error) Can not recover the name of the equivalent

signal for mbist_diag_out at top level from the current CTL

DESCRIPTION

You received this message because the command was not able to recover the name of the equivalent mbist_diag_out signal. This may come from a wrong specification of the report_mbist_trace parameters. Be sure to use options equivalent to the ones used with set_mbist_run (set_testbench_parameters in XG mode) command.

WHAT NEXT

Specify the correct options for report_mbist_trace.

SEE ALSO

preview_dft (2), **report_mbist_trace** (2), **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (XG **mode)**

TEST-1642 (error) Parameter core_index is required when core integration is implemented

DESCRIPTION

You received this message because you did not specify a greater or equal with zero value for the core_index parameter of the report_mbist_trace command. This parameter is required when core integration is implemented.

WHAT NEXT

Specify a -core_index for report_mbist_trace command

SEE ALSO

preview_dft (2), **report_mbist_trace** (2),

TEST-1643 (error) Test program %s must start with a Write operation %s

DESCRIPTION

You received this message because you did not specify a Write operation as the first

operation of the specified test. This is required to initialize the memory content. This situation is triggered also when you are specifying a ROM algorithm for a RAM controller.

WHAT NEXT

Specify a Write operation as the first operation of the test program.

SEE ALSO

preview_dft (2), **define_mbist_program** (2),

TEST-1644 (Warning) The default protocol in %s mode runs only the MBIST core of ID 0 because some cores share the same diagnosis output ports.

DESCRIPTION

You receive this warning message because some MBIST cores share the same diagnosis output ports. So they cannot be run in parallel in the case of diagnosis mode or ROMs controllers with external signature comparison in go_nogo mode. In those cases the default protocol runs only the MBIST core of ID 0.

WHAT NEXT

Use the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) to select one or more MBIST cores to be run in parallel.

SEE ALSO

preview_dft (2), **set_mbist_run** (2).

TEST-1645 (Warning) the value '%s' of the controller selection parameter specifies %d among %d controllers; the non specified controllers will not be selected

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because the number of bits, which the controller selection value is coded, is less than the controller number. The remaining controllers will not be selected.

WHAT NEXT

Specify a correct controller selection value.

SEE ALSO

preview_dft (2), **set_mbist_run** (2).

TEST-1646 (error) cannot find %s port/s in CTL top level model

DESCRIPTION

This is issued while MBISTC tries to build a new STIL test bench. The tool is not able to find the specified port/s in the CTL top level model. The generated STIL test bench is not correct.

WHAT NEXT

Verify the CTL top level model and re-run the **set_mbist_run** (or **set_testbench_parameters** in XG mode) UI command to build a new STIL test bench. If the problem subsist contact the Synopsys support.

SEE ALSO

preview_dft (2), **set_mbist_run** (2).

TEST-1647 (error) Background test program %s of type %s requires a Pattern specification

DESCRIPTION

You received this message because you did not specify a Pattern statement for an Background test program of type AlgorithmBased, which is required in this case.

WHAT NEXT

Specify a Pattern statement for the respective test program.

SEE ALSO

preview_dft (2), **define_mbist_program** (2),

TEST-1648 (warning) Can not find %s for -parameter %s.

DESCRIPTION

You received this message because you specified a test that does not exist. As the specified test program has not been found, a default test program will be implemented instead of it.

WHAT NEXT

Use the **define_mbist_program** command to define the test.

SEE ALSO

set_mbist_controller (2), **define_mbist_program** (2), **preview_dft** (2), **insert_dft** (2).

TEST-1649 (warning) Controller %s is empty and deleted.

DESCRIPTION

You received this message because you created an MBIST controller specification with the **set_mbist_controller** command, but there were no memories available to be tested by that controller. The controller specification is removed from the plan, because there is nothing for it to do.

WHAT NEXT

It is safe to ignore this warning, or you can prevent this warning by not creating the controller in the first place. Alternatively, you can ensure the controller's existence by assigning it at least one memory.

SEE ALSO

set_mbist_controller (2), **preview_dft** (2), **insert_dft** (2).

TEST-1650 (warning) Number of controllers specified is too big. Not enough memories to assign.

DESCRIPTION

You received this message because you specified more MBIST controllers than were needed, based on the number of memories to be tested.

WHAT NEXT

It is safe to ignore this warning, or you can prevent this warning by specifying a smaller number of controllers with the **set_mbist_configuration** command, or not specifying a number of controllers at all.

SEE ALSO

set_mbist_configuration (2), **preview_dft** (2), **insert_dft** (2).

TEST-1651 (warning) Number of controllers specified (%d) is too small to accomodate all the memories, %d controllers are created.

DESCRIPTION

You received this message because you specified fewer MBIST controllers than were needed, based on the number of memories to be tested.

WHAT NEXT

It is safe to ignore this warning, or you can prevent this warning by specifying a larger number of controllers with the **set_mbist_configuration** command, or not specifying a number of controllers at all.

SEE ALSO

set_mbist_configuration (2), **preview_dft** (2), **insert_dft** (2).

TEST-1652 (error) Parameter %s defined multiple times.

DESCRIPTION

You received this message because you repeated a port definition.

WHAT NEXT

Combine all signal definitions for each port into one parameter.

SEE ALSO

create_dft_model (2).

TEST-1653 (warning) Ignoring memory instance %s from MBIST insertion because it is not a valid memory.

DESCRIPTION

You received this message because you used the **set_mbist_controller** command to assign a memory to a controller, but the instance is not recognized as a memory.

WHAT NEXT

It is safe to ignore this warning, or you can prevent this warning by not assigning this instance to a controller. If this instance really is a memory, make sure it has a valid CTL memory model. In XG mode, be sure to use the **use_test_model** command for all memory models.

SEE ALSO

read_test_model (2), **use_test_model** (2), **set_mbist_controller** (2), **preview_dft** (2), **insert_dft** (2).

TEST-1654 (error) MBIST architect couldn’t get scan clock info. MBC does not support the -no_scan option.

DESCRIPTION

You received this message because MBIST architect could not get the scan clock info for the design. This information is used to assign memories to controllers, based on memory clock sources.

WHAT NEXT

Do not use the -no_scan option with MBIST.

SEE ALSO

preview_dft (2), **insert_dft** (2).

TEST-1655 (information) Memory is being treated as a non_muxed memory as signal %s is defined of type %s in both

Mission and BIST mode.

DESCRIPTION

You received this message because your memory model appeared to support embedded multiplexers, but the indicated signal is not multiplexed.

WHAT NEXT

If your memory has embedded multiplexers, modify your memory model so that the indicated signal is declared in only one mode.

SEE ALSO

read_test_model (2) **preview_dft** (2), **insert_dft** (2).

TEST-1656 (Error) The following cores have scan compression logic already inserted: %s

DESCRIPTION

You receive this message because you have not enabled scan compression integration but you have some cores in your design that contain scan compression logic.

WHAT NEXT

Check your specifications. Enable scan compression integration if required.

SEE ALSO

set_scan_compression_configuration (2) **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1657 (Error) Cell %s has %d scan compression modes and %d reconfigurable scan modes

DESCRIPTION

You received this message because you have enabled scan compression integration on a design that contains cores with more than one scan compression mode or more than one reconfigurable scan mode.

WHAT NEXT

Check your design. Scan Compression integration does not permit cores with more than one Scan Compression mode or more than one reconfigurable scan mode.

SEE ALSO

set_scan_compression_configuration (2) **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1658 (Error) Design has chip-level scan structures

DESCRIPTION

WHAT NEXT

SEE ALSO

set_scan_compression_configuration (2) **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1659 (Error) Design does not contain any cores with scan compression logic

DESCRIPTION

You receive this message because you have enabled scan compression integration but your design does not have any cores with scan compression logic.

WHAT NEXT

Check your specifications. Disable scan compression integration if required.

SEE ALSO

set_scan_compression_configuration (2) **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1660 (Warning) The DIAG_OUT parameter is ignored

because the use of this parameter is allowed only in the case of Boundary-Scan.

DESCRIPTION

You receive this warning message because you specified the DIAG_OUT parameter in the command **set_mbist_run** (or **set_testbench_parameters** in XG mode). The use of this parameter is allowed only in the case of Boundary-Scan.

WHAT NEXT

Delete the DIAG_OUT parameter specified in the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) .

SEE ALSO

preview_dft (2), **set_mbist_run** (2).

TEST-1661 (error) invalid BURN_IN parameter value: only YES and NO are valid values

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because you specified a wrong value of the BURN_IN parameter. Only YES and NO are valid values.

WHAT NEXT

Modify the value of the BURN_IN parameter.

SEE ALSO

set_mbist_run (2).

TEST-1662 (error) Invalid value for the BURN_IN_DURATION

parameter

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because you specified a wrong value for BURN_IN_DURATION parameter. Should be a positive integer value.

WHAT NEXT

Specify a positive integer value for BURN_IN_DURATION parameter.

SEE ALSO

set_mbist_run (2).

TEST-1663 (error) No BURN_IN support in MBIST system.

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because you set the BURN_IN parameter to YES but there is no BURN_IN support in MBIST system.

WHAT NEXT

Generate a MBIST system with BURN_IN support.

SEE ALSO

set_mbist_configuration (2) **preview_dft** (2)

TEST-1664 (error) No burn in test in diagnosis mode.

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because you specify the BURN_IN parameter in diagnosis mode. This version of Memory BIST Compiler supports burn_in test only in go nogo mode.

WHAT NEXT

Change the diagnosis mode in go nogo mode.

SEE ALSO

set_mbist_configuration (2) **preview_dft** (2)

TEST-1665 (error) No burn in test with run-time programmable test, retention test, repair test and controller selection.

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because you specified the BURN_IN parameter with run-time programmable test or retention test or repair test or controller selection. This version of Memory BIST Compiler supports burn in test only for Synthesis BIST with all controlles run in parallel.

WHAT NEXT

Delete the RT_TEST, RETENTION and CNTRL_SEL parameter in order to perform burn in test.

SEE ALSO

set_mbist_configuration (2) **preview_dft** (2)

TEST-1666 (Warning) the MBIST core of ID ’%d’ will not be run because it does not support burn in

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because the specified core does not support burn in test. The burn in test will run only MBIST cores with burn in support.

WHAT NEXT

Look at preview_dft report

SEE ALSO

preview_dft (2), **set_mbist_run** (2).

TEST-1667 (Warning) %s

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because the specified controller tests ROM/s with external signature computation. This version of Memory BIST Compiler does not support burn in test for ROMs with external signature computation.

WHAT NEXT

Look at preview_dft report

SEE ALSO

preview_dft (2), **set_mbist_run** (2).

TEST-1668 (Error) The reported diagnosis package is inconsistent

DESCRIPTION

You receive this message because the just printed diagnosis package contains inconsistent information. This may be caused by invalid input files, by an incorrect usage of the mbist report trace command or by an internal error.

WHAT NEXT

Check the input files and the command line.

SEE ALSO

insert_dft (2), **preview_dft** (2),

TEST-1669 (error) cannot use BURN_IN_DURATION

parameter without BURN_IN parameter set to YES.

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because you specified the BURN_IN_DURATION parameter without BURN_IN parameter set to YES.

WHAT NEXT

Specify BURN_IN parameter set to YES.

SEE ALSO

set_mbist_configuration (2) **preview_dft** (2) **set_mbist_run** (2)

TEST-1670 (Warning) the MBIST controller '%s' does not support burn in test because it tests ROMs with external signature computation.

DESCRIPTION

This is issued from the command **preview_dft** because the specified controller tests ROM/s with external signature computation. This version of Memory BIST Compiler does not support burn in test for ROMs with external signature computation.

WHAT NEXT

Change EXTERNAL to INTERNAL signature computation to run the ROM controller during the burn in test.

SEE ALSO

set_mbist_controller (2), **preview_dft** (2), **set_mbist_run** (2).

TEST-1671 (Warning) the BURN_IN_DURATION parameter

value is too small.

DESCRIPTION

This is issued from the command **preview_dft** because the specified BURN_IN_DURATION parameter value is too small and does not allow to perform one complete memory test.

WHAT NEXT

Change BURN_IN_DURATION parameter value.

SEE ALSO

set_mbist_controller (2), **preview_dft** (2), **set_mbist_run** (2).

TEST-1672 (Warning) the '%s' MBIST Controller is not optimal for burn-in test.

DESCRIPTION

You received this warning message because you specified a MBIST architecting setting that is not optimal for burn-in test. The condition for an optimal burn-in test is that the ratio between the biggest memory size and the smallest one within the same BIST Controller is lower or equal to 2.

WHAT NEXT

Modify the MBIST controller user architecting setting.

SEE ALSO

set_mbist_controller (2), **preview_dft** (2),

TEST-1673 (information) read_data_delayed parameter value for memory %s has been changed to NO due to diag_faulty_data_bits set to YES

DESCRIPTION

This message is issued when the read_data_delayed and diag_faulty_data_bits IP

parameters are both specified to YES (or 1) in the -ip_parameters (-parameters in XG mode) list. When enabled simultaneously, the diag_faulty_data_bits parameter has the priority.

WHAT NEXT

Nothing.

SEE ALSO

set_mbist_element (2). **set_mbist_wrapper** (2) **(in** XG **mode).**

TEST-1674 (Error) Incomplete MBIST controllers selection burn-in test

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because you use the CONTROL_SEL_<CORE ID> parameter to specify only some controllers of the selected MBIST core for the burn-in test. When you select a MBIST core for burn-in test, you must select all its controller.

WHAT NEXT

Modify the CONTROL_SEL_<CORE ID> parameter value to select all the controllers of the specified MBIST core.

SEE ALSO

set_mbist_run (2), **preview_dft** (2),

TEST-1675 (Information) the '%s' controller will test ROM/s with INTERNAL signature computation to support burn in.

DESCRIPTION

When the burn-in test is supported, the MBIST architect uses the INTERNAL signature computation (instead of the EXTERNAL) as default value.

WHAT NEXT

Use the **set_mbist_controller if you want to use the EXTERNAL signature computation**

for ROMs.

SEE ALSO

set_mbist_controller (2). **preview_dft** (2).

TEST-1676 (Warning) BURN_IN parameter will be ignored because all the MBIST controllers support ROM/s with external signature comparison.

DESCRIPTION

You received this warning message because you specified a burn-in test support (in the **set_mbist_controller** UI command) and all the MBIST controllers support ROM/s with external signature comparison. This version of MBISTC does not support burn-in test for controllers that test ROMs with external signature comparison, so the BURN_IN parameter will be ignored.

WHAT NEXT

Nothing

SEE ALSO

set_mbist_configuration (2), **set_mbist_controller** (2), **preview_dft** (2),

TEST-1677 (error) Cannot set REPAIR_UNLOAD or REPAIR_VERIFY to YES because REPAIR_ENABLE is disabled.

DESCRIPTION

This is issued from the command **set_mbist_run** (or **set_testbench_parameters** in XG mode) because you set the REPAIR_UNLOAD or REPAIR_VERIFY parameters to YES but the REPAIR_ENABLE parameter is disabled.

WHAT NEXT

Set REPAIR_ENABLE parameter to YES.

SEE ALSO

preview_dft (2) **set_mbist_run** (2)

TEST-1678 (error) Can not recover the CLK value from line %d of the processed log, the resulted diagnosis stream may be corrupted

DESCRIPTION

You received this message because an error occured during the simulation log conversion. This can be caused by a corrupted log file.

WHAT NEXT

Check the testbench and regenerate the log file.

SEE ALSO

set_mbist_run (2) **set_testbench_configuration** (2) **(XG** mode)

TEST-1679 (error) invalid wrapper specification (%s)

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode) because you have specified a non existing wrapper.

WHAT NEXT

Look at the MBIST and Core Integration previews and specify an existing wrapper.

SEE ALSO

preview_dft (2).

TEST-1680 (error) the specified wrapper (%s) does not test

ROM with external signature computation

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode) because the specified wrapper does not test ROM with external signature computation.

WHAT NEXT

Look at the MBIST and Core Integration previews and specify a wrapper that tests ROM with external signature computation.

SEE ALSO

preview_dft (2).

TEST-1681 (error) invalid '%s' parameter

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode) because you specified an invalid parameter of 'mem_id' option. 'root_id' (in the case of Core Integration), 'cntrl_id' and 'wrap_id' are the only valid parameters of 'mem_id' option.

WHAT NEXT

Look at **set_mbist_element** (or **set_mbist_wrapper** in XG mode) man page.

SEE ALSO

set_mbist_element (2). **set_mbist_wrapper** (2).

TEST-1682 (error) Can not recover the name of the equivalent signal for repair chain scan out at top level from the current CTL

DESCRIPTION

You received this message because the command was not able to recover the name of the equivalent repair chain scan out signal. This may come from a wrong specification of the report_mbist_trace parameters. Be sure to use options equivalent to the ones used with set_mbist_run (set_testbench_parameters in XG mode)

command.

WHAT NEXT

Specify the correct options for report_mbist_trace.

SEE ALSO

preview_dft (2), **report_mbist_trace** (2), **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (XG **mode)**

TEST-1683 (error) '%s' parameter missing in 'mem_id' option

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode) because the tool can not correcly identify a MBIST wrapper. 'root_id' (in the case of Core Integration), 'cntrl_id' and 'wrap_id' are the only valid parameters of 'mem_id' option.

WHAT NEXT

Specify the missing parameter in the 'mem_id' option.

SEE ALSO

set_mbist_element (2). **set_mbist_wrapper** (2).

TEST-1684 (error) 'root_id' parameter can be used only in the case of core integration

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode) because the 'root_id' can be used only in the case of core integration.

WHAT NEXT

Use 'cntrl_id' and 'wrap_id' as parameters of 'mem_id' option.

SEE ALSO

preview_dft (2). **set_mbist_element** (2). **set_mbist_wrapper** (2).

TEST-1685 (error) Invalid RepairResource %s in the CTL model for memory %s as Column repair resource with no repair address is really data bit repair

DESCRIPTION

You received this message as a Column repair resource with no repair address is really data bit repair. The type of the specified RepairResource should be changed to DataBit.

WHAT NEXT

Change the CTL model for the respective memory to use the DataBit repair type instead.

TEST-1686 (information) Width for RepairResource %s of memory %s is set to 1

DESCRIPTION

You received this message because the Width for the specified RepairResource has not been specified or it has been specified with an invalid integer value smaller than 1. In this case the value of the Width parameter is automatically set to 1.

WHAT NEXT

Set a correct value for the Width statement in the CTL model of the specified memory.

SEE ALSO

preview_dft (2) insert_dft (2)

TEST-1687 (error) Empty Test Algorithm "%s

DESCRIPTION

You received this message because you are using empty Algorithm CTL block with no sequences defined in it. These kind of algorithms can not be used in the MBIST flow.

WHAT NEXT

Change the CTL description of your test program.

TEST-1688 (error) Can not use the reserved name %s to define a test program

DESCRIPTION

You received this message because you are using a reserved name as the name of your test program. This test program with this name is internally defined and it is used for open address decoder faults detection.

WHAT NEXT

Use a different name for your test program.

SEE ALSO

define_mbist_program (2)

TEST-1689 (Information) The detailed description of the %s algorithm is provided in the MBISTC UG

DESCRIPTION

You received this message because you are using an internally predefined algorithm that tests for the open address decoder faults. The definition of this algorithm can be found in the MBISTC User Guide.

WHAT NEXT

See the User Guide for the algorithm detailed description.

SEE ALSO

preview_dft (2). **define_mbist_program** (2). **report_mbist_program** (2).

TEST-1690 (error) Can not use the %s algorithm in the controller "%s

DESCRIPTION

You received this message because you are using an algorithm that was not designed for the ROM memories.

WHAT NEXT

Use a different test program for the ROM controller.

SEE ALSO

set_mbist_controller (2). **define_mbist_program** (2). **report_mbist_program** (2).

TEST-1691 (error) DFT configuration clock controller is not compatible with the RTL flow.

DESCRIPTION

You receive this error message because you invoked the RTL insertion flow with the **preview_dft -rtl** or **insert_dft -rtl** command, but you also enabled the PLL clock controller flow with the **set_dft_configuration -clock_controller enable** command. The clock controller flow is an integral part of the scan insertion flow, but scan is not inserted at the RT level.

WHAT NEXT

You should activate the clock controller flow in the second pass of the RTL insertion flow. For now, you should **set_dft_configuration -clock_controller disable**.

SEE ALSO

set_dft_configuration (2), **preview_dft** (2), **insert_dft** (2).

TEST-1692 (error) Specified test program %s is not yet supported in the runtime programmable BIST

DESCRIPTION

You received this message because you are using a test program specific for open address decoder faults detection which is not yet supported in the runtime programmable BIST.

WHAT NEXT

Use a different test program for the runtime programmable BIST.

SEE ALSO

define_mbist_program (2) **set_mbist_run** (2) **or** set_testbench_parameters **(2)** (in **XG** mode) **report_mbist_trace** (2)

TEST-1693 (warning) Test program %s will not be redefined, using the existing definition from the MBIST test programs database

DESCRIPTION

You received this message because you are using a reserved name as the name of your test program. This test program with this name is internally defined and it is used for open address decoder faults detection. The internal definition of this test will be used instead of the specified custom definition.

WHAT NEXT

Use a different name for your test program if this is not the intended behaviour.

SEE ALSO

define_mbist_program (2)

TEST-1694 (error) Can not use the %s algorithm in the controller

%s containing only memories with write only and read only ports

DESCRIPTION

You received this message because you are using an algorithm that has been designed to work with controllers having at least one memory with a read/write port.

WHAT NEXT

Use a different test program for the specified controller.

SEE ALSO

set_mbist_controller (2). **define_mbist_program** (2). **report_mbist_program** (2).

TEST-1695 (Error) must specify content file name and memory IDs for ROM external signature change.

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode). The command needs content file name and memory IDs for ROM external signature change.

WHAT NEXT

Specify the content file name and memory IDs.

SEE ALSO

set_mbist_element (2) **or** set_mbist_wrapper **(2)** (XG)

TEST-1696 (Error) The value specified for parameter '-core_index' is out of the valid range (%d..%d)

DESCRIPTION

This is issued from the command **report_mbist_trace** as the specified core_index value is bigger than the maximal value accepted for this parameter.

WHAT NEXT

Specify a correct core_index value.

SEE ALSO

report_mbist_trace (2)

TEST-1697 (information) The value specified for parameter '-core_index' is ignored when core integration is not present

DESCRIPTION

This is issued from the command **report_mbist_trace** as the value specified for core_index is ignored when there is no core integration.

WHAT NEXT

Don't use this parameter when there is no core integration

SEE ALSO

report_mbist_trace (2)

TEST-1698 (error) The current design already has MBIST T2 encapsulated.

DESCRIPTION

The tool detects the presence of MBIST Tech 2 IPs in the current design. Cannot run MBISTC tool twice on the same design.

WHAT NEXT

Change input design.

SEE ALSO

preview_dft (2) **insert_dft** (2)

TEST-1699 (warning) Could not find mode %s in the model bin

DESCRIPTION

You receive this message because the specified mode can not be retrieved correctly from the model bin.

WHAT NEXT

Use the dft_drc supported flow instead by setting the test_enable_dft_drc variable to true and create a test protocol before running preview_dft or insert_dft.

SEE ALSO

preview_dft (2) **insert_dft** (2)

TEST-1700 (error) Number of scan paths specified with pipeline registers '%d' and scan chains specified '%d' mismatch.

DESCRIPTION

You receive this message when the pipeline scan data feature is enabled. You have defined a number of scan paths with their corresponding head and tail pipeline registers. But this number does not match the number of scan chains specified with **set_scan_configuration -chain_count**. Because of this, **preview_dft** or **insert_dft** will not proceed.

WHAT NEXT

Correct the chain count value in **set_scan_configuration** or specify additional scan paths with **set_scan_path**

SEE ALSO

set_scan_configuration (2). **set_scan_path** (2).

TEST-1701 (error) %s pipeline register '%s' is not a valid

sequential cell, check the dft_drc report

DESCRIPTION

You receive this message when the pipeline scan data feature is enabled. The head or tail pipeling register specified with the **set_scan_path** command was violated during test design rule checking. Because of this, **preview_dft** or **insert_dft** will not proceed.

WHAT NEXT

Run **dft_drc -verbose** again and analyze why the corresponding head or tail pipeline register is not valid.

SEE ALSO

set_scan_configuration (2). **set_scan_path** (2). **dft_drc** (2).

TEST-1702 (error) No scan %s port specified for chain '%s' with pipeline registers

DESCRIPTION

You receive this message when the pipeline scan data feaure is enabled. You have specified a scan path with its corresponding head and tail registers. But you did not associate a scan in port and a scan out port for this scan path. Because of this, **preview_dft** or **insert_dft** will not proceed.

WHAT NEXT

Define a scan input and a scan output port. Associate them with the scan path mentioned in this error message.

SEE ALSO

set_scan_path (2).

TEST-1703 (error) %s pipeline register '%s' does not exist in the

current design

DESCRIPTION

You receive this message when the pipeline scan data feature is enabled. You have specified a scan path with its corresponding head and tail registers. But the head or tail register cell you specified does not exist in the design.

WHAT NEXT

Verify with **get_cells** whether the cell instance name is right. Modify you specification accordingly.

SEE ALSO

set_scan_path (2). **get_cells** (2).

TEST-1704 (error) %s pipeline register '%s' is triggered by a different clock from previously specified %s register

DESCRIPTION

You receive this message when the pipeline scan data feature is enabled. You have specified several scan paths with their corresponding head and tail registers. All the head pipeline registers must be triggered by the same clock signal. All the tail pipeline registers must be triggered by the same clock signal. However, the head or tail register cell mentioned in the error message is triggered by a different clock.

WHAT NEXT

Verify that all head or tail pipeline registers get their clock from the same signal.

SEE ALSO

set_scan_path (2).

TEST-1705 (error) Unbalanced pipeline head or tail register

specifications

DESCRIPTION

You receive this message when the pipeline scan data feature is enabled. You have specified several scan paths with their corresponding head and tail registers. But the number of head pipeline stages is not the same across all chains or the number of tail pipeline stages is not the same across all chains.

WHAT NEXT

Verify the log from you set_scan_path commands. You probably got a UIT-911 error message.

SEE ALSO

set_scan_path (2).

TEST-1706 (Warning) Pipeline scan data feature is not supported with the current DFT configuration and will be ignored.

DESCRIPTION

You receive this message when the pipeline scan data feature is enabled. Pipeline scan data feature is only supported with Scan compression DFT client. Pipeline scan data feature is only supported with **multiplexed_flip_flop** scan style. A configuration setting any other client or scan style generates this message and the pipeline scan data feature is automatically disabled for the current command.

WHAT NEXT

Change your configuration with **set_dft_configuration** and **set_scan_configuration** commands

SEE ALSO

set_dft_configuration (2), **set_scan_configuration** (2), **preview_dft** (2), **insert_dft** (2),

TEST-1707 (error) The option ’-background_type’ must be

explicitly set to ’algorithm_based’ when specifying ’-pattern’

DESCRIPTION

You receive this message because you are trying to create a mbist program of type background using a pattern specification and the default value for the background type, which is topological. As a background of type topological is ignoring the specified pattern, you must explicitly set the value of the background type to ’algorithm_based’ in order to use the ’-pattern’ option.

WHAT NEXT

Add the option ’-background_type algorithm_based’ to your define_mbist_program command.

SEE ALSO

define_mbist_program (2)

TEST-1708 (error) The MBIST Spec does not exists

DESCRIPTION

You receive this message because there is no MBIST spec to be reseted/removed

WHAT NEXT

Nothing.

SEE ALSO

set_mbist_configuration (2) **reset_mbist_configuration** (2) **(XG** mode)
remove_mbist_configuration (2) **(DB** mode)

TEST-1709 (warning) Option %s is not available for ROM memory %s

DESCRIPTION

You receive this message because the specified option is not available on ROMs. The option will be automatically turned off.

WHAT NEXT

For better readability, you should not use this option in your scripts (commands: set_mbist_element in DB Mode or set_mbist_wrapper in XG mode)

SEE ALSO

set_mbist_element (2) **(DB** mode) **set_mbist_wrapper** (2) **(XG** mode) **preview_dft** (2) **insert_dft** (2)

TEST-1710 (warning) Diagnosis information can not be processed for test mode %s

DESCRIPTION

You receive this message because the specified test mode is not an MBIST diagnosis one. The '-trace_file' argument can only be processed for MBIST diagnosis test modes. The '-trace_file' argument will be automatically disabled.

WHAT NEXT

Specify an MBIST diagnosis test mode.

SEE ALSO

report_mbist_trace (2) **preview_dft** (2) **insert_dft** (2)

TEST-1711 (information) repair_algorithm will be ignored if the 2D repair is not enabled

DESCRIPTION

You received this message because the 'repair_algorithm' parameter is only valid for the 2D repair. The 2D repair is enabled by setting the 'repair_type' option to 'row_column'.

WHAT NEXT

No user action required.

SEE ALSO

set_mbist_wrapper (2) preview_dft (2) insert_dft (2)

TEST-1712 (Error) Design does not contain any chip level scan logic

DESCRIPTION

You received this message because you enable the hybrid flow for scan compression but the design does not have any scan logic that is not driven by scan compression structures

WHAT NEXT

Check your design. If you just want to integrate adaptive scan cores, use set_scan_compression_configuration -integration_only

SEE ALSO

set_scan_compression_configuration (2) **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1713 (Error) The Memory BIST product is no longer supported in DFT Compiler.

DESCRIPTION

You received this message because you tried to use an MBIST UI specific switch or command.

List of MBIST disabled specific switches: set_dft_configuration -mbist set_dft_signal -freq_mult create_test_clock -mbist_clock preview_dft -mbist preview_dft -rtl insert_dft -rtl

List of MBIST disabled specific commands: set_mbist_configuration reset_mbist_configuration remove_mbist_configuration set_mbist_controller reset_mbist_controller set_mbist_element set_mbist_wrapper reset_mbist_wrapper set_mbist_run set_testbench_parameters report_mbist_trace define_mbist_program report_mbist_program reset_mbist_programs create_mbist_standalone

WHAT NEXT

Don’t use MBIST specific switches or commands.

SEE ALSO

set_dft_configuration (2). **insert_dft** (2), **preview_dft** (2), **set_dft_signal** (2), **create_test_clock** (2)

TEST-1714 (warning) Reading in a test protocol after specifying signals will cause the signals to be cleared from the protocol and the model.

DESCRIPTION

You received this warning message to alert you; if you have specified signals using the **set_dft_signal** command prior to a **read_test_protocol** the signals will be removed once the **read_test_protocol** is executed.

WHAT NEXT

Always specify the signals after **read_test_protocol** to ensure that they will be present in the protocol and the model.

SEE ALSO

set_dft_signal (2), **read_test_protocol(2)**

TEST-1715 (error) The specification for the hookup signal nor the differential clock will not be accepted. They are mutually exclusive.

DESCRIPTION

You receive this error message because you specified a differential clock as a hookup pin. However, a differential clock must be specified with primary input ports.

WHAT NEXT

Remove the -hookup_pin and its corresponding port name in the command **set_dft_signal** . Instead specify a primary input port for the differential clock in the -port option of the **set_dft_signal** command.

SEE ALSO

set_dft_signal (2),

TEST-1716 (error) The specification for a differential clock can only have on reference clock port and one differential clock port. The specification of multiple reference clock ports and/or differential clock ports will be discarded.

DESCRIPTION

You receive this error message because you specified multiple ports for the reference clock port and/or differential clock port. A differential clock specification may only have a single reference clock port and differential clock port, and both should not have been used in a another differential clock specification.

WHAT NEXT

Remove the extra ports specified for the reference clock and/or the differential clock, and replace them with a single reference clock port and differential clock port in the **set_dft_signal**.

SEE ALSO

set_dft_signal (2),

TEST-1718 (warning) The specification for a differential clock does not require the user to specify the timing. The differential clock port will receive the complementary waveform of the reference clock supplied. The specification of the timing waveform will be ignored.

DESCRIPTION

You received this warning message because you specified a timing waveform for the differential clock port. However, the timing waveform for this port is unnecessary.

WHAT NEXT

You may choose to remove the timing specification for the differential clock when using the **set_dft_signal** to specify a differential clock, so that you wil no longer receive the warning message.

SEE ALSO

set_dft_signal (2),

TEST-1719 (error) The port %s was previously used, however the specification for a differential clock cannot have a port that was previously used to declare another differential clock signal. The specification will be discarded.

DESCRIPTION

You received this error message because you specified a port that was previously used to declare another differential clock signal. A unique pair of ports must be used to specify each differential clock.

WHAT NEXT

You must specify a pair of ports that has not been used to specify another differential clock when using the **set_dft_signal** .

SEE ALSO

set_dft_signal (2),

TEST-1720 (Error) Could not access %s component from DesignWare.

DESCRIPTION

You receive this error message because the DFT Compiler is unable to access the

WHAT NEXT

Check your **search_path** variable and include **dft_lbist.sldb** in your **synthetic_library** variable. Rerun the DFT Compiler.

SEE ALSO

search_path (3), **synthetic_library** (3).

TEST-1721 (error) %s pipeline register '%s' was specified as a non scan element. Check your scan specifications

DESCRIPTION

You receive this message when the pipeline scan data feature is enabled. The head or tail pipeling register specified with the **set_scan_path** command have been previously specified as non scan element through the command set_scan_element or set_scan_configuration -exclude. Because of this **preview_dft** or **insert_dft** will not proceed. Head and tail register are automatically handled by the tool. You should not explicitly declare them as non scan element.

WHAT NEXT

Declare your head or tail pipeling register as regular scan element using the command set_scan_element or set_scan_configuration -exclude

SEE ALSO

set_scan_configuration (2).

TEST-1722 (error) Architecting of %s/Unload compressor failed with the given set of parameters.

DESCRIPTION

You receive this message because compressor architecting is not possible for the given set of paramemters and you have specified a number of internal chains or a maximum scan chain length. This prevents preview_dft or insert_dft from proceeding.

WHAT NEXT

Load and unload compressor architecting depends on the number of scan input pins, scan output pins, internal chains specified and the number of clock chains architected. Scan configuration settings like clock mixing in the compression test mode may also have an effect on the number of clock chains architected. Either try to inrease the number of scan inputs and scan ouputs. Either try to reduce the chain count specifed with *set_scan_compression_configuration -chain_count* command. Either try to increase the max chain length specifed with *set_scan_compression_configuration -max_length* command. Either try to explicitly set

the clock mixing in the compression test mode. Rerun *preview_dft* to verify if the compressors with new parameters can be architected.

SEE ALSO

set_scan_configuration (2) **set_scan_compression_configuration** (2) **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1730 (information) Clock generator input '%s' is driven by clock generator output '%s'. The path is preserved.

DESCRIPTION

You receive this message when the on-chip clocking control feature is enabled. DFT Compiler has detected a path between two cells identified as clock generator cells. The second clock generator cell may drive a clock signal to the first clock generator cell. This clock signal may be used as a reference in the first clock generator cell. DFT Comiler will not insert a clock controller cell on a clock signal path between two clocks generator cells. DFT Compiler will preserve the connectivity between both cells. The net name linking them may change.

WHAT NEXT

Verify that you have identified the clock generator output pins at the right level of hierarchy.

SEE ALSO

set_dft_signal (2).

TEST-1731 (information) The specified rule '%s' has been ignored.

DESCRIPTION

You have received this message because you have specified a wrong rule violation or a not supported rule.

WHAT NEXT

Please, check the violated rules list and re-run the report_dft_drc_violation command.

SEE ALSO

dft_drc (2).

TEST-1732 (error) Violations cannot be reported because the design has changed since last dft_drc command.

DESCRIPTION

You receive this message because you have run a DC command and your design has changed since the last dft_drc command.

WHAT NEXT

Please, run dft_drc command, then re-run report_dft_drc_violations.

SEE ALSO

dft_drc (2).

TEST-1733 (error) Violations cannot be reported. Please, run dft_drc command first.

DESCRIPTION

You receive this message because you have run report_dft_drc_violations command before running dft_drc command.

WHAT NEXT

Please, run dft_drc command, then re-run report_dft_drc_violations.

SEE ALSO

dft_drc (2).

TEST-1734 (error) Scan group '%s' cannot have the -class occ

option set when SNPS clock controller insertion is selected.

DESCRIPTION

This error message occurs when you enable clock controller insertion and you select the SNPS clock controller IP for insertion. In this flow, the **-class occ** option of the **set_scan_group** command cannot be specified. It is only meant to identify existing clock control bits segments in the user-defined clock controller flow.

WHAT NEXT

Run the **set_scan_group** command without the **-class occ** option.

SEE ALSO

set_dft_clock_controller(2)
set_dft_configuration(2)
set_scan_group(2)

TEST-1800 (error) encoding specifications for modes '%s' and '%s' are identical.

DESCRIPTION

The encoding specification must be unique. User must re-define the encoding specification for the mode by using the **define_test_mode -encoding** command.

TEST-1850 (error) Required BSD design not found.

DESCRIPTION

BSD design information is to be made available for the read_bsdl command to execute successfully.

WHAT NEXT

Verify the BSD design information is available to the BSD Compiler before running the read_bsdl command.

SEE ALSO

read_bsdl(2)

TEST-1851 (error) Required DC design not found.

DESCRIPTION

DC design information is to be made available for the read_bsdl command to execute successfully.

WHAT NEXT

Verify the DC design information is available to the BSD Compiler before running the read_bsdl command.

SEE ALSO

read_bsdl (2)

TEST-1852 (error) BSD design name ('%s') is NOT same as the name of the top module specified in the input netlist ('%s').

DESCRIPTION

The BSD design name specified as part of the "entity" construct in the BSDL file should be the same as the name of the top module as specified in the input netlist.

WHAT NEXT

Make sure the above mentioned names are identical before running the read_bsdl command.

SEE ALSO

read_bsdl(2)

TEST-1853 (error) Incorrect ENTITY declaration in the input BSDL file. (Check if source file is BSDL).

DESCRIPTION

The read_bsdl command has detected a potential syntax error in the ENTITY specification in the input BSDL file. It is also likely that the input file does not contain valid BSDL syntax.

WHAT NEXT

Make sure the input file is a valid BSDl file and that the ENTITY declaration has no syntax errors.

SEE ALSO

read_bsdl(2)

TEST-1854 (error) Incorrect END_BSDL declaration in the input BSDL file.

DESCRIPTION

The read_bsdl command has detected a potential syntax error in the END_BSDL specification in the input BSDL file.

WHAT NEXT

Make sure that the END_BSDL declaration has no syntax errors in the input BSDL file.

SEE ALSO

read_bsdl(2)

TEST-1855 (error) Incorrect PORT declaration in the input BSDL file.

DESCRIPTION

The read_bsdl command has detected a potential syntax error in the PORT specification in the input BSDL file.

WHAT NEXT

Make sure that the PORT declaration has no syntax errors in the input BSDL file.

SEE ALSO

read_bsdl(2)

TEST-1856 (error) Incorrect PIN_MAP declaration in the input BSDL file.

DESCRIPTION

The read_bsdl command has detected a potential syntax error in the PIN_MAP specification in the input BSDL file.

WHAT NEXT

Make sure that the PIN_MAP declaration has no syntax errors in the input BSDL file.

SEE ALSO

read_bsdl(2)

TEST-1857 (error) Error in creation of BSD linkage port '%s'.

DESCRIPTION

After reading the contents of the input BSDL file, BSD linkage ports are created in the design. This error pertains to issues in creation of the specified BSD linkage port.

SEE ALSO

read_bsdl(2)

TEST-1858 (error) Error in creation of BSD port '%s'.

DESCRIPTION

After reading the contents of the input BSDL file, BSD ports are created in the design. This error pertains to issues in creation of the specified BSD port.

SEE ALSO

read_bsdl(2)

TEST-1859 (error) Incorrect port specifier attribute in the input

BSDL file. ’%s’ is not a valid port specifier.

DESCRIPTION

In BSDL, valid port attribute values are "in", "inout", "out", "linkage" or "buffer". Any other values or syntax errors would result in the generation of this error message.

WHAT NEXT

Make sure the port specifier attribute matches one of the above mentioned values.

SEE ALSO

read_bsdl(2)

TEST-1860 (error) Incorrect USE declaration in the input BSDL file.

DESCRIPTION

The read_bsdl command has detected a potential syntax error in the USE specification in the input BSDL file.

WHAT NEXT

Make sure that the USE declaration has no syntax errors in the input BSDL file.

SEE ALSO

read_bsdl(2)

TEST-1861 (error) Internal error encountered in BSD Compiler while updating BSD linkage ports in BSD design.

DESCRIPTION

Internal error encountered in BSD Compiler while updating BSD linkage ports in BSD design.

SEE ALSO

read_bsdl(2)

TEST-1862 (error) Error in assigning WAIT_DURATION (Real Time) to EXTEST_PULSE.

DESCRIPTION

The read_bsdl command has encountered an error of processing of the "real time" part of the WAIT_DURATION specification.

WHAT NEXT

Make sure that the WAIT_DURATION specification has no syntax errors in the input BSDL file.

SEE ALSO

read_bsdl(2)

TEST-1863 (error) Error in assigning WAIT_DURATION (clock cycles) to EXTEST_PULSE.

DESCRIPTION

The read_bsdl command has encountered an error of processing of the "clock cycle" part of the WAIT_DURATION specification.

WHAT NEXT

Make sure that the WAIT_DURATION specification has no syntax errors in the input BSDL file.

SEE ALSO

read_bsdl(2)

TEST-1864 (error) Error in assigning "train

DESCRIPTION

The read_bsdl command has encountered an error of processing of the "train" part of the EXTEST_TRAIN specification.

WHAT NEXT

Make sure that the EXTEST_TRAIN specification has no syntax errors in the input BSDL file.

SEE ALSO

read_bsdl(2)

TEST-1865 (error) Error in assigning "maximum_time

DESCRIPTION

The read_bsdl command has encountered an error of processing of the "maximum_time" part of the EXTEST_TRAIN specification.

WHAT NEXT

Make sure that the EXTEST_TRAIN specification has no syntax errors in the input BSDL file.

SEE ALSO

read_bsdl(2)

TEST-1866 (error) No [linkage] port named ’%s’ found in BSD design.

DESCRIPTION

The specified port name (as read from the input BSDL file) is not found in the BSD design.

WHAT NEXT

Make sure that the port name as specified in the BSDL file is consistent with the port name specified in the input netlist.

SEE ALSO

read_bsdl(2)

TEST-1867 (error) Error in BSD package creation.

DESCRIPTION

The package name as specified in the input BSDL file might be inconsistent with the specification in the input netlist.

WHAT NEXT

Make sure that the package name as specified in the input BSDL file is consistent with the specification in the input netlist.

SEE ALSO

read_bsdl(2)

TEST-1868 (error) Error in setting HP_Time for BSDL cell corresponding to port '%s'.

DESCRIPTION

The HP_Time setting for the specified port was unsuccessful.

WHAT NEXT

Make sure that the HP_Time value and the cell corresponding to the port name are corretcly mentioned in the input BSDL.

SEE ALSO

read_bsdl(2)

TEST-1869 (error) Error in setting LP_Time for BSDL cell corresponding to port '%s'.

DESCRIPTION

The LP_Time setting for the specified port was unsuccessful.

WHAT NEXT

Make sure that the LP_Time value and the cell corresponding to the port name are corretcly mentioned in the input BSDL.

SEE ALSO

read_bsdl(2)

TEST-1870 (error) BSD cell position '%d' in invalid.

DESCRIPTION

The position of the BSD cell as specified in the BOUNDARY_REGISTER of the input BSDL file is not consistent with the BOUNDARY_LENGTH.

WHAT NEXT

Make sure that the BSD cell position number is consistent with BOUNDARY_LENGTH specification.

SEE ALSO

read_bsdl(2)

TEST-1871 (error) Incorrect Standard_Attributes declaration in the input BSDL file.

DESCRIPTION

The read_bsdl command has detected a potential syntax error in the Standard_Attributes specification in the input BSDL file.

WHAT NEXT

Make sure that the Standard_Attributes declaration has no syntax errors in the input BSDL file.

SEE ALSO

read_bsdl(2)

TEST-1872 (error) Error in setting Receiver cell value to BSD cell '%s'.

DESCRIPTION

An error was encountered in setting the Receiver cell value of the specified BSD cell.

WHAT NEXT

Make sure that the cell number (port name) and the syntax of the Receiver cell value setting in the input BSDL file.

SEE ALSO

read_bsdl(2)

TEST-1873 (error) Error in processing the BOUNDARY_REGISTER attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the BOUNDARY_REGISTER attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the BOUNDARY_REGISTER specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1874 (error) Error in processing the INSTRUCTION_CAPTURE attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the INSTRUCTION_CAPTURE attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the INSTRUCTION_CAPTURE specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1875 (error) Error in processing the AIO_COMPONENT_CONFORMANCE attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the AIO_COMPONENT_CONFORMANCE attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the AIO_COMPONENT_CONFORMANCE specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1876 (error) Error in processing the

COMPONENT_CONFORMANCE attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the COMPONENT_CONFORMANCE attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the COMPONENT_CONFORMANCE specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1877 (error) Error in processing the PIN_MAP_STRING attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the PIN_MAP_STRING attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the PIN_MAP_STRING specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1878 (error) Error in processing the REGISTER_ACCESS attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the REGISTER_ACCESS attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the REGISTER_ACCESS specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1879 (error) Error in processing the INSTRUCTION_OPCODE attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the INSTRUCTION_OPCODE attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the INSTRUCTION_OPCODE specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1880 (error) Error in processing the USERCODE_REGISTER attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the USERCODE_REGISTER attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the USERCODE_REGISTER specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1881 (error) Error in processing the AIO_EXTEST_TRAIN_EXECUTION attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the AIO_EXTEST_TRAIN_EXECUTION attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the AIO_EXTEST_TRAIN_EXECUTION specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1882 (error) Error in processing the AIO_EXTEST_PULSE_EXECUTION attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the AIO_EXTEST_PULSE_EXECUTION attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the AIO_EXTEST_PULSE_EXECUTION specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1883 (error) Error in processing the IDCODE_REGISTER attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the IDCODE_REGISTER attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the IDCODE_REGISTER specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1884 (error) Error in processing the PORT_GROUPING attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the PORT_GROUPING attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the PORT_GROUPING specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1885 (error) Error in processing the COMPLIANCE_PATTERN attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the COMPLIANCE_PATTERN attribute specified in

the input BSDL file.

WHAT NEXT

Make sure that the syntax of the COMPLIANCE_PATTERN specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1886 (error) Error in processing the AIO_PIN_BEHAVIOR attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the AIO_PIN_BEHAVIOR attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the AIO_PIN_BEHAVIOR specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1887 (error) Error in processing the INSTRUCTION_PRIVATE attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the INSTRUCTION_PRIVATE attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the INSTRUCTION_PRIVATE specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1888 (error) Error in processing the BOUNDARY_LENGTH attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the BOUNDARY_LENGTH attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the BOUNDARY_LENGTH specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1889 (error) No BSD cells found corresponding to port '%s'.

DESCRIPTION

An error was encountered in retrieving the BSDL cells corresponding to the specified port from the BSD design.

WHAT NEXT

Make sure that the port name for which the error has been reported is correct.

SEE ALSO

read_bsdl(2)

TEST-1890 (error) Error in processing the INSTRUCTION_LENGTH attribute specified in the input BSDL

file.

DESCRIPTION

An error was encountered in processing the INSTRUCTION_LENGTH attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the INSTRUCTION_LENGTH specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1891 (error) Error in processing the TAP_SCAN_CLOCK attribute specified in the input BSDL file.

DESCRIPTION

An error was encountered in processing the TAP_SCAN_CLOCK attribute specified in the input BSDL file.

WHAT NEXT

Make sure that the syntax of the TAP_SCAN_CLOCK specification is correct.

SEE ALSO

read_bsdl(2)

TEST-1892 (error) Error in processing the RUNBIST_EXECUTION attribute specified in the input BSDL file.

DESCRIPTION

This error message indicates that an error occurred when processing the **RUNBIST_EXECUTION** attribute specified in the input BSDL file.

WHAT NEXT

See the IEEE Std 1149.1-2001 for the correct syntax. Make sure that the syntax of the **RUNBIST_EXECUTION** attribute specification is correct and then run the command again.

SEE ALSO

read_bsdl(2)

TEST-1893 (error) Error in processing the INTEST_EXECUTION attribute specified in the input BSDL file.

DESCRIPTION

This error message indicates that an error occurred when processing the **INTEST_EXECUTION** attribute specified in the input BSDL file.

WHAT NEXT

See the IEEE Std 1149.1-2001 for the correct syntax. Make sure that the syntax of the **INTEST_EXECUTION** attribute specification is correct and then run the command again.

SEE ALSO

read_bsdl(2)

TEST-1894 (error) Design contains cores with xtolerant and non-xtolerant compression logic.

DESCRIPTION

This error message occurs when you enable a scan compression integration/hybrid flow but your design has cores with both xtolerant and non-xtolerant compression logic. The mixing of cores with both xtolerant and non-xtolerant compression logic is only supported at the top level. If a core is integrated at a deeper hierarchy, it should not contain both xtolerant and non-xtolerant compression/decompression (CODEC) logic.

For example, if a the TOP design has three cores named core_a, core_b, and core_c, each of these cores individually can only have either xtolerant or non-xtolerant CODECs inside them. Assume core_a has all non-xtolerant CODECs, while core_b and core_c have all xtolerant CODECs, respectively. In this case, integration at the top

level can be performed. However, if core_c itself has 2 xtolerant and 1 non-xtolerant CODEC, the integration/hybrid flow cannot not be run at the top level.

WHAT NEXT

Generate cores with homogeneous CODECs so as to integrate at the top level.

SEE ALSO

insert_dft(2)
preview_dft(2)
set_dft_configuration(2)
set_scan_compression_configuration(2)

TEST-1900 (warning) Pipelining scan data is not supported for multiple compression modes in user defined pipeline flow.

DESCRIPTION

You receive this warning message if you have enabled user defined pipelining scan data in multimode flow. Pipelining scan data is supported for only for multiple scan modes and not multiple compression modes.

WHAT NEXT

Pipelining scan data is not supported for multimode flows. You can either disable pipelining scan data or have only one compression mode.

SEE ALSO

set_dft_configuration remove_test_mode

TEST-1901 (Warning) User defined pipeline scan data flow is enabled using set_scan_configuration command. Auto pipelining scan data will be disabled.

DESCRIPTION

You receive this message if you have enabled pipelining scan data using both **set_dft_configuration** and **set_scan_configuration** commands. Auto pipelining will be disabled. All specifications in **set_pipeline_scan_data_configuration** will be ignored.

WHAT NEXT

If you have specified head/tail pipeline registers using **set_scan_path** command, then you don't need to do anything. The scan-ins/scan-outs of the scan paths will be hooked up to their corresponding head/tail pipeline registers. If pipeline registers are not defined, you should disable pipeline scan data in scan configuration using **set_scan_configuration** -pipeline_scan_data FALSE. The tool will automatically insert pipeline registers.

SEE ALSO

set_scan_configuration set_dft_configuration set_pipeline_scan_data_configuration set_scan_path

TEST-1902 (Error) Pipelining scan data not enabled for design with pipelined compression cores.

DESCRIPTION

You receive this error message in hierarchical adaptive synthesis flow, if the design has compression cores with pipeline scan data registers and scan data pipelining is not enabled at the top level.

WHAT NEXT

Enable pipeline scan data using **set_dft_configuration**. Specify head/tail depths using **set_pipeline_scan_data_configuration**.

SEE ALSO

set_pipeline_scan_data_configuration set_dft_configuration

TEST-1903 (warning) Pipeline scan data registers are user defined. Pipeline scan data configuration specifications will be ignored.

DESCRIPTION

You receive this warning message if you have defined pipeline registers for scan paths and also enabled auto pipelining scan data. All specifications in **set_pipeline_scan_data_configuration** will be ignored.

WHAT NEXT

You don’t need to do anything. The scan-ins/scan-outs of the scan paths will be hookep up to their corresponding head/tail pipeline registers.

SEE ALSO

set_pipeline_scan_data_configuration set_scan_path set_dft_configuration

TEST-1904 (Error) Auto pipelining scan data failed.

DESCRIPTION

You receive this error message if auto pipelining scan data failed.

WHAT NEXT

TEST-1905 (warning) The specified number of Head and Tail pipeline scan data stages is 0. Pipeline registers will not be inserted.

DESCRIPTION

You receive this warning message if you have enabled pipeline san data using **set_dft_configuration** command and defined the number of both head and tail pipeline stages as 0.

WHAT NEXT

You don’t need to do anything, if this intended. Alternatively, you can specify head and tail pipeline depth using the **set_pipeline_scan_data_configuration** command to insert pipeline stages.

SEE ALSO

set_pipeline_scan_data_configuration set_dft_configuration

TEST-1906 (error) No of internal chains %d is less than no of

inputs %d.

DESCRIPTION

You receive this message because load decompressor architecting failed for the given set of scan inputs and for the given minimum compression. The number of scan-inputs is derived from set_scan_configuration -chain_count for the base mode. The minimum_compression is specified with the set_scan_compression_configuration command. The number of chains in the scan-compression mode is either calculated based on these numbers or derived from the set_scan_configuration -chain_count for the user defined compression mode.

WHAT NEXT

The number of scan inputs should be less than the number of compression mode chains. You can increase the number of compression mode chains, by either varying minimum compression or chain count for the compression mode. Also, check mode specific scan path and chain count specifications.

SEE ALSO

set_scan_configuration (2), **set_scan_compression_configuration** (2), **set_scan_path** (2), **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1907 (error) No of internal chains %d is less than no of outputs %d.

DESCRIPTION

You receive this message because unload compressor architecting failed for the given set of scan outputs and for the given minimum compression. The number of scan-outputs is derived from set_scan_configuration -chain_count for the base mode. The minimum_compression is specified with the set_scan_compression_configuration command. The number of chains in the scan-compression mode is either calculated based on these numbers or derived from the set_scan_configuration -chain_count for the user defined compression mode.

WHAT NEXT

The number of scan outputs should be less than the number of compression mode chains. You can increase the number of compression mode chains, by either varying minimum compression or chain count for the compression mode. Also, check mode specific scan path and chain count specifications.

SEE ALSO

set_scan_configuration (2), **set_scan_compression_configuration** (2), **set_scan_path** (2), **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1908 (Error) %s pipeline stages mismatch. Core %s has %d pipeline stages. Top level requires %d pipeline stages.

DESCRIPTION

You receive this message if you have enabled pipelining scan data in hiearchical adaptive synthesis flow and there is a mismatch between the number of pipeline stages in a core with scan compression, and the top level . All cores should have the same number of head and/or tail pipeline stages, which should be specified at the top level.

WHAT NEXT

Specify the number of head and/or tail pipeline stages at the top level using **set_pipeline_scan_data_configuration** command.

SEE ALSO

set_pipeline_scan_data_configuration (2)

TEST-1909 (Error) Top %s pipeline clock %s not compatible with core pipeline clock.

DESCRIPTION

You receive this message if you have enabled pipelining scan data in hiearchical adaptive synthesis flow and the specified top pipeline clock is incompatible with a core pipeline clock. When a pipeline clock is not specified, the tool creates a rise-to-1 clock "SNPS_PipeClk" for the pipeline registers. This error message is triggered when no pipeline clock is specified at the core level and the top pipeline clock is a rise-to-0 clock, which is incompatible with the core "SNPS_PipeClk" clock. Hence, the core "SNPS_PipeClk" clock cannot be stitched to the specified top level pipeline clock.

WHAT NEXT

Specify a pipeline clock that is compatible to the core pipeline clock using **set_pipeline_scan_data_configuration** command at the top level.

SEE ALSO

set_pipeline_scan_data_configuration (2), **set_dft_signal** (2)

TEST-1910 (Error) Stitching top pipeline clock to core pipeline clock failed.

DESCRIPTION

You receive this error message if stitching top pipeline clock to core pipeline clock "SNPS_PipeClk" failed.

WHAT NEXT

TEST-1911 (Error) Cannot architect load decompressor with %d inputs.

DESCRIPTION

You receive this message because load decompressor architecting failed with the given number of scan-ins. This message indicates that there are not sufficient number of scan-ins for the load decompressor to architect the required number of internal chains.

WHAT NEXT

You can increase the number of scan-ins for the load decompressor by increasing the base mode chain count. You can decrease the number of internal chains by decreasing minimum compression or chain count for the compression mode. Also, check compression mode scan path specifications. It is recommended, to specify the scan-ins and scan-outs only in the all_dft or base mode. The scan compression mode scan-in/scan-out specifications are used to guide the tool to build scan chains outside the codec and hence are not available for the load decompressor.

SEE ALSO

set_scan_configuration (2), **set_scan_compression_configuration** (2), **set_scan_path** (2), **set_dft_signal** (2), **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1912 (Error) Too small period (period=%d <

nload_inputs=%d).

DESCRIPTION

You receive this message because there are not sufficient number of scan-ins for the load decompressor to architect the required number of internal chains.

WHAT NEXT

You can increase the number of scan-ins for the load decompressor by increasing the base mode chain count. You can decrease the number of internal chains by decreasing minimum compression or chain count for the compression mode. Also, check compression mode scan path specifications. It is recommended, to specify the scan-ins and scan-outs only in the all_dft or base mode. The scan compression mode scan-in/scan-out specifications are used to guide the tool to build scan chains outside the codec and hence are not available for the load decompressor.

SEE ALSO

set_scan_configuration (2), **set_scan_compression_configuration** (2), **set_scan_path** (2), **set_dft_signal** (2), **insert_dft** (2), **preview_dft** (2), **set_dft_configuration** (2).

TEST-1920 (warning) Scan chain blockage in '%s' cell may be due to the function 0 in the lib_cell '%s' of library '%s'.

DESCRIPTION

This warning message occurs when **dft_drc** command reports scan chain blockage (S1) violations. These scan chain blockage violations may be due to the presence of function 0 on the output pin of some lib_cells of your libraries. Elements that are driven by function 0 pins are removed by Design Compiler tool during optimization. The scan chain may be broken if the logic 0 pin is connected to an element of the scan path.

WHAT NEXT

Remove function 0 from your libraries before running the **insert_dft** command.

SEE ALSO

get_libs(2)
insert_dft(2)
preview_dft(2)

TEST-2000 (Warning) There is no scan IN port for the Scan Chain '%s'.

DESCRIPTION

You get this Warning message when the scan IN pin of the scan Chain does not exist in the design.

WHAT NEXT

Review the scan def file and the design.

SEE ALSO

write_scan_def(2), place_opt(2), report_scan_chain(2), check_scan_chain(2),

TEST-2001 (Warning) There is no scan OUT port for the Scan Chain '%s'.

DESCRIPTION

You get this Warning message when the scan OUT pin of the scan Chain does not exist in the design.

WHAT NEXT

Review the scan def file and the design.

SEE ALSO

write_scan_def(2), place_opt(2), report_scan_chain(2), check_scan_chain(2),

TEST-2002 (Warning) The direction of the pin '%s' is not correct.

DESCRIPTION

You get this Warning message when the direction (input or output) of the expected pin is not correct.

WHAT NEXT

Review the scan def file and the design.

SEE ALSO

read_def(2), optimize_dft(2), report_scan_chain(2), check_scan_chain(2),

TEST-2003 (Error) Boundary-Scan has already been inserted using ’insert_dft’ command.

DESCRIPTION

This message is issued when boundary scan is already inserted into the design with **insert_dft** command and user runs **insert_dft** command again to insert boundary scan logic or user runs **preview_dft to preview boundary scan logic. Boundary scan logic can only be inserted once with insert_dft** command. And **preview_dft** can be used to preview boundary scan logic before inserting boundary scan.

WHAT NEXT

If user wants to change the boundary scan logic of the design, they need to run **insert_dft** on pre-boundary scan netlist.

TEST-2004 (Error) No pattern block found in the CTL for the design.

DESCRIPTION

This error is flagged when the write_test command does not see any pattern information in the CTL.

WHAT NEXT

Make sure that the create_bsd_patterns command was completed successfully.

SEE ALSO

create_bsd_patterns (2).

TEST-2005 (error) No CTL and/or Design Compiler design information found for this design.

DESCRIPTION

This error occurs when there is no valid CTL data or the Design Compiler design information is missing.

WHAT NEXT

Make sure that the **create_bsd_patterns** command was completed successfully.

SEE ALSO

create_bsd_patterns(2)

TEST-2006 (error) No valid library cell specified.

DESCRIPTION

This error message occurs when the tool cannot identify the specified library cell. The name of the library cell is either incorrect or the library cell does not exist.

WHAT NEXT

Make sure that all of the library cells needed for the design are completely specified and available in the search path. After making any changes, run the command again.

TEST-2008 (Error) -usage clock_gating is invalid when feature to connect unconnected test pins of clock gating cells is disabled.

DESCRIPTION

You received this error message because you disabled the feature to connect unconnected test pins of clock gating cells and are using the -usage clock_gating option with the set_dft_signal command.

WHAT NEXT

Enable the Clock gating feature using the set_dft_configuration -connect_clock_gating enable command and rerun. If you do not intend to connect test signal to the clock gating cells and have thus disabled the connect_clock_gating feature then remove the -usage clock_gating option from the set_dft_signal command.

SEE ALSO

set_dft_configuration(2)
set_dft_signal(2)

TEST-2009 (Error) Invalid usage '%s'.

DESCRIPTION

You received this error message because you have specified a wrong usage for a DFT Signal with -usage option of the **set_dft_signal** command.

WHAT NEXT

Specify a valid usage and issue the command again. See help for **set_dft_signal** command for valid usages.

SEE ALSO

set_dft_signal(2)

TEST-2010 (Error) -usage option is valid only with -type ScanEnable or -type TestMode.

DESCRIPTION

You received this error message because you have specified -type other than ScanEnable or TestMode to the set_dft_signal command when using the -usage option.

WHAT NEXT

The -usage option for the set_dft_signal command can only be used for -type ScanEnable or TestMode. Change the -type to one of these.

SEE ALSO

set_dft_signal(2)

TEST-2011 (Error) -usage option is invalid with -test_mode option.

DESCRIPTION

You received this error message because you have used the -usage option to the set_dft_signal command and have also specified the -test_mode option.

WHAT NEXT

The -usage option for the set_dft_signal command cannot be mode specific. Remove the -test_mode option to the set_dft_signal command when using -usage.

SEE ALSO

set_dft_signal(2)

TEST-2012 (Error) -usage option is invalid within the scope of a test mode.

DESCRIPTION

You received this error message because you have used the -usage option to the set_dft_signal command within the scope of a test mode.

WHAT NEXT

The -usage option for the set_dft_signal command cannot be mode specific. Remove it from the scope of test mode and rerun the command.

SEE ALSO

set_dft_signal(2)

TEST-2013 (Error) -usage option cannot be specified in existing_dft view.

DESCRIPTION

You received this error message because you have used the -usage option to the set_dft_signal command and have specified the -view as existing_dft.

WHAT NEXT

The -usage option for the set_dft_signal command can only be used if the -view is specification. Change the -view of the set_dft_signal command to -view specification

SEE ALSO

set_dft_signal(2)

TEST-2014 (Information) You are not running topographical mode. set_scan_compression_configuration congestion_optimization option has no effect.

DESCRIPTION

This message shows that your are not running DC-Topographic mode and you are setting congestion_optimization option to true for set_scan_compression_configuration. The "congestion_optimization" option only work for DC-Topographic. Hence, in non DC-Topographic mode, it has no effect.

WHAT NEXT

If you need to congestion optimization for DFT insertion, use DC-Topographic instead.

TEST-2015 (Error) To remove dft connectivity specification either a specification Label or -all must be specified.

DESCRIPTION

You received this warning message because you issued remove_dft_connect command without specifying, either a dft connectivity specification Label or -all. Any one of them is required. Both dft connectivity specification Label and -all are not allowed at the same time.

WHAT NEXT

Please specify either a dft connectivity specification Label or -all and issue the command again.

SEE ALSO

set_dft_connect(2)

TEST-2016 (Warning) Overwriting existing specification with same label '%s'

DESCRIPTION

You received this warning message because you specifed set_dft_connect command with a label that has already been used earlier.

WHAT NEXT

If you did not want to overwrite earlier specification then specify a new label and run the command again. Otherwise no action is required.

SEE ALSO

set_dft_connect(2)

TEST-2017 (Error) Invalid usage of signal.

DESCRIPTION

You received this error message because you specifed set_dft_connect command with a source which has either not been defined with -usage switch of set_dft_signal command or defined with a usage not valid for current use.

Specified source should be a ScanEnable or TestMode defined with valid -usage switch of set_dft_signal command.

A ScanEnable or TestMode port with usage "clock_gating" is required to specify DFT connectivity of clock gating cells by set_dft_connect command.

A ScanEnable with usage "scan" is required to specify DFT connectivity of scan cells by set_dft_connect command.

WHAT NEXT

Define ScanEnable or TestMode port and use it to specify connectivity again.

SEE ALSO

set_dft_connect(2)
set_dft_signal(2)

TEST-2018 (Error) Removal failed as no DFT connectivity specification exist.

DESCRIPTION

You received this error message because you tried to remove DFT connectivity specification which does not exist.

WHAT NEXT

You cannot remove a specification which does not exist. Use this command to remove an existing DFT connectivity specification.

SEE ALSO

set_dft_connect(2)
remove_dft_connect(2)

TEST-2019 (Error) Removal failed as no DFT connectivity specification with label '%s'.

DESCRIPTION

You received this error message because you tried to remove DFT connectivity specification which does not exist.

WHAT NEXT

You cannot remove a specification which does not exist. Specify a valid label and run the command again.

SEE ALSO

set_dft_connect(2)
remove_dft_connect(2)

TEST-2020 (Warning) Cell '%s' belongs to CTL modeled design

instance. It will be ignored.

DESCRIPTION

You received this warning message because you specified a cell with CTL model in either target or exclude list of objects of set_dft_connect command. It will be ignored.

WHAT NEXT

The cell is ignored by command. No action is required.

SEE ALSO

set_dft_connect(2)
remove_dft_connect(2)

TEST-2021 (Warning) Cell '%s' has 'dont_touch' attribute. It will be ignored.

DESCRIPTION

You received this warning message because you specified a cell with dont_touch attribute in either target or exclude list of objects of set_dft_connect command. It will be ignored.

WHAT NEXT

The cell is ignored by command. No action is required.

SEE ALSO

set_dft_connect(2)
remove_dft_connect(2)

TEST-2022 (Warning) Cell '%s' is combinational. It will be ignored.

DESCRIPTION

You received this warning message because you specified a combinational cell in either target or exclude list of objects of set_dft_connect command. It will be

ignored.

WHAT NEXT

The cell is ignored by command. No action is required.

SEE ALSO

set_dft_connect(2)
remove_dft_connect(2)

TEST-2023 (Warning) Cell '%s' is a CTL modeled design instance. It will be ignored.

DESCRIPTION

You received this warning message because you specified a CTL modeled design instance in either target or exclude list of objects of set_dft_connect command. It will be ignored.

WHAT NEXT

The cell is ignored by command.

SEE ALSO

set_dft_connect(2)
remove_dft_connect(2)

TEST-2024 (Warning) Cell '%s' belongs to CTL modeled design instance. It will be ignored.

DESCRIPTION

You received this warning message because you specified a cell with CTL model as argument to set_scan_suppress_toggling command.

WHAT NEXT

The cell is ignored by command. No action is required.

SEE ALSO

set_scan_suppress_toggling(2)
remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)

TEST-2026 (Warning) Cell '%s' is combinational. It will be ignored.

DESCRIPTION

You received this warning message because you specified a combinational cell as argument to set_scan_suppress_toggling.

WHAT NEXT

The cell is ignored by command. No action is required.

SEE ALSO

set_scan_suppress_toggling(2)
remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)

TEST-2027 (Warning) Cell '%s' has 'scan_exclude' attribute. It will be ignored.

DESCRIPTION

You received this warning message because you specified a cell with 'scan_exclude' attribute as argument to set_scan_suppress_toggling command. It will be ignored.

WHAT NEXT

The cell is ignored by command. No action is required.

SEE ALSO

set_scan_suppress_toggling(2)
remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)

TEST-2028 (Warning) Cell '%s' is a CTL modeled design instance. It will be ignored.

DESCRIPTION

You received this warning message because you specified a CTL modeled design instance as argument to set_scan_suppress_toggling.

WHAT NEXT

The cell is ignored by command. No action is required.

SEE ALSO

set_scan_suppress_toggling(2)
remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)

TEST-2029 (Warning) Cell '%s' has 'dont_touch' attribute. It will be ignored.

DESCRIPTION

You received this warning message because you specified a cell with 'dont_touch' attribute as argument to set_scan_suppress_toggling.

WHAT NEXT

The cell is ignored by command. No action is required.

SEE ALSO

set_scan_suppress_toggling(2)
remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)

TEST-2030 (Error) Scan style '%s' is not supported for power gating of scan flop outputs. Only Multiplexed Flip Flop scan style

is supported.

DESCRIPTION

You received this warning message because you specified a scan style other than 'multiplexed_flip_flop' scan style and issued set_scan_suppress_toggling command. set_scan_suppress_toggling supports only 'multiplexed_flip_flop' scan style.

WHAT NEXT

Change the scan style to 'multiplexed_flip_flop' and issue the command again.

SEE ALSO

set_scan_suppress_toggling(2)
remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)

TEST-2031 (Error) Library cell name '%s' unknown. Specifiction ignored.

DESCRIPTION

You received this warning message because you specified a library cell name as argument to set_scan_suppress_toggling which cannot be found in design.

WHAT NEXT

Give a valid library cell name and run the command or no action is required.

SEE ALSO

set_scan_suppress_toggling(2)
remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)

TEST-2032 (Error) Library cell name '%s' does not conform to the scan style used (%s). Specification is ignored.

DESCRIPTION

You received this warning message because you specified a library cell name as

argument to set_scan_suppress_toggling which does not conform to scan style specification.

WHAT NEXT

Give a valid library cell name with conforming scan style and run the command again else no action is required.

SEE ALSO

set_scan_suppress_toggling(2)
remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)

TEST-2033 (Error) Object type '%s' unknown.

DESCRIPTION

You received this Error message because you specifed an object in the include list of command set_scan_suppress_toggling which is neither a scan flip-flop instance, hierarchical cell (containing flip-flops), references of flip-flops or design.

WHAT NEXT

Specification is ignored. Specify a valid object and run the command again or no action is required.

SEE ALSO

set_scan_suppress_toggling(2)
remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)

TEST-2034 (Warning) Reference '%s' is a CTL modeled design. Specification is ignored.

DESCRIPTION

You received this warning message because you specified a reference cell which is CTL modeled design, as argument to set_scan_suppress_toggling command.

WHAT NEXT

Specification is ignored. Specify a valid object and run the command again or no

action is required.

SEE ALSO

set_scan_suppress_toggling(2)
remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)

TEST-2035 (Warning) Specification already entered for '%s' object with '%s' library association. Updating specification.

DESCRIPTION

You received this warning message because you specified an object in include list of set_scan_suppress_toggling command which has already been specified with by an earlier set_scan_suppress_toggling command specification. This specification will override earlier specification.

WHAT NEXT

This specification will overide earlier specification. If this is not what you intended then give a valid specification and run the command again else no action is required.

SEE ALSO

set_scan_suppress_toggling(2)
remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)

TEST-2036 (Information) You have enabled a compression type that is not supported with congestion optimization. DFT MAX Compression Congestion Optimization is disabled.

DESCRIPTION

This message shows that your are enabling both compression type and congestion optimization. The congestion optimization is disabled.

WHAT NEXT

TEST-2037 (Information) You have enabled DFT MAX Compression Congestion Optimization. This option is supported only if you start with a design that was compiled with congestion optimization enabled. DFT MAX Compression Congestion Optimization is disabled.

DESCRIPTION

This message shows that your are enabling DFT MAX congestion optimization for a design that was not compiled with "-congestion". DFT MAX Compression Congestion Optimization is disabled.

WHAT NEXT

You can re-compile the design with "-congestion" option.

TEST-2038 (Error) DFT signals of type CompressionClock can not be defined in the view "existing".

DESCRIPTION

You get this message because you are defining a signal of type CompressionClock with the option "-view" set to existing.

WHAT NEXT

You must set the option "-view" to "spec" for the command to be accepted. You may specify a given timing for your port of type CompressionClock using the command "set_dft_signal -view existing -type ScanClock -timing ...".

TEST-2039 (Error) -usage scan is valid only with -type ScanEnable.

DESCRIPTION

You received this error message because set_dft_signal command was issued with

signal type other than -type ScanEnable along with -usage scan option. Only ScanEnable signal can be used with -usage scan.

WHAT NEXT

Change the signal type to ScanEnable and issue the command.

SEE ALSO

set_dft_signal(2)

TEST-2040 (warning) dont_touch_network attribute on scan-enable port or signal '%s' can result in QoR degradation after scan insertion.

DESCRIPTION

This warning message occurs when there is a **dont_touch_network** attribute set on a scan-enable port or signal, which can lead to QoR degradation after scan insertion in the following cases:

• When shift registers are identified in the design and logic is inserted on the scan-enable signal during scan insertion

• When the functional output of scan flip-flops is gated to reduce power with the **set_scan_suppress_toggling** command

In these cases the extra logic added on the scan-enable signal, during scan insertion, leads to shared paths between the scan-enable signal and the functional logic. A **dont_touch_network** attribute on the scan-enable signal would propagate into functional logic paths, which would prevent optimization of those paths and could lead to QoR degradation.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this warning message, do not use a **dont_touch_network** attribute on scan-enable ports or signals. Instead, to disable timing optimization, use the **set_case_analysis** command on scan-enable ports. To disable DRC fixing, use the **set_ideal_network** command on the scan-enable ports. If you must use a **dont_touch_network** attribute, then use **dont_touch_network ,Äìno_propagate** instead, to avoid propagation of the dont_touch attribute into functional logic.

SEE ALSO

set_case_analysis(2)

set_dont_touch_network(2)
set_ideal_network(2)
set_scan_suppress_toggling(2)
compile_seqmap_identify_shift_registers_with_synchronous_logic(3)

TEST-2041 (error) Selection method is set to ’manual’ but no include list is specified.

DESCRIPTION

This error message occurs when the **set_scan_suppress_toggling** command is invoked with the **-selection_method** option set to **manual**, but no list of design objects is specified with the **-include_elements** option.

WHAT NEXT

Rerun the command and specify a list of design objects with the **-include_elements** option.

SEE ALSO

set_scan_suppress_toggling(2)

TEST-2042 (error) Include list must be provided for ’manual’ and ’mixed’ gating selection methods.

DESCRIPTION

This error message occurs when attempting to run the **set_scan_suppress_toggling** command with the **-selection_method** option set to **manual** or **mixed**. When the **-selection_method** is either **manual** or **mixed**, you must also use the **-include_elements** option to specify a list of design objects.

WHAT NEXT

Rerun the command using the **-include_elements** option in addition to the **-selection_method** option.

SEE ALSO

set_scan_suppress_toggling(2)

TEST-2043 (error) The total percentage gating must be 0.001 or any positive number up to 100.

DESCRIPTION

This error message occurs when attempting to run the **set_scan_suppress_toggling** command with the **-total_percentage_gating** option. The value specified with the **-total_percentage_gating** option is outside of the acceptable range.

WHAT NEXT

Specify the value for **-total_percentage_gating** as 0.001 or a positive number up to 100 and rerun the command.

SEE ALSO

set_scan_suppress_toggling(2)

TEST-2044 (error) The -include_elements option is not accepted when the selection method is 'auto'.

DESCRIPTION

This error message occurs when attempting to run the **set_scan_suppress_toggling** command with the **-selection_method** set to **auto**. You specified a list of design objects through the **-include_elements** option while asking for a power gating based on full automatic flip-flop selection.

WHAT NEXT

Rerun the command and omit the **-include_elements** option if you use the **auto** selection method.

SEE ALSO

set_scan_suppress_toggling(2)

TEST-2045 (error) The minimum timing slack after gating must

be 0 or any positive number to 1000.

DESCRIPTION

This error message occurs when attempting to run the **set_scan_suppress_toggling** command with an invalid value for the **-min_slack** option. The accepted value for minimum timing slack is 0 or a positive number to 1000.

WHAT NEXT

Rerun the command and specify a valid value for the **-min_slack** option.

SEE ALSO

set_scan_suppress_toggling(2)

TEST-2046 (information) Considering gating of '%d' over a total of '%d' valid scan cells.

DESCRIPTION

The **insert_dft** command issues this message when it is enabled by the **set_scan_suppress_toggling** command to perform the gating of scan cells' functional output pins for power reduction during scan shift. This message indicates the number of scan cells that is considered for gating among the total number of valid scan cells after filtering out all scan cells that cannot be gated. Cells that cannot be gated include cells with the 'dont_touch' attribute, cells belonging to CTL-modeled instances, cells that are the heads of identified shift registers, and so forth.

WHAT NEXT

This is an information-only message. No action is required.

However, you can review design constraints and the constraints you passed through the **set_scan_suppress_toggling** command, and make changes if desired.

SEE ALSO

remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)
set_scan_suppress_toggling(2)

TEST-2047 (information) Number of scan cells that were gated:

'%d' out of '%d' considered.

DESCRIPTION

The **insert_dft** command issues this message when it is enabled by the **set_scan_suppress_toggling** command to perform gating of scan cells' functional output pins for power reduction during scan shift. This message indicates the number of scan cells that were effectively gated by **insert_dft** over the total number of available valid scan cells.

WHAT NEXT

This is an information-only message. No action is required.

However, you can review the design constraints and the constraints you passed through the **set_scan_suppress_toggling** command, and make changes if necessary.

SEE ALSO

remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)
set_scan_suppress_toggling(2)

TEST-2048 (information) Number of user-provided scan cells that were gated: '%d'.

DESCRIPTION

The **insert_dft** command issues this message when it is enabled by the **set_scan_suppress_toggling** command to perform gating of scan cells' functional output pins for power reduction during scan shift. This message indicates the number of user-provided scan cells that were effectively gated by **insert_dft**.

WHAT NEXT

This is an information-only message. No action is required.

However, you can review the design constraints and the constraints you passed through the **set_scan_suppress_toggling** command, and make changes if necessary.

SEE ALSO

remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)
set_scan_suppress_toggling(2)

TEST-2049 (information) Number of scan cells that were rejected because of timing: '%d' out of '%d' considered.

DESCRIPTION

The **insert_dft** command issues this message when it is enabled by the **set_scan_suppress_toggling** command to perform gating of scan cells' functional output pins for power reduction during scan shift. This message indicates the number of scan cells that were not considered for power gating, since inserting a gate at their functional output pin would violate timing constraints.

WHAT NEXT

This is an information-only message. No action is required.

However, you can review the design constraints and the constraints you passed through the **set_scan_suppress_toggling** command, and make changes if necessary.

SEE ALSO

remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)
set_scan_suppress_toggling(2)

TEST-2050 (warning) The -min_slack option is ignored when the selection method is set to 'manual'.

DESCRIPTION

This warning message occurs when attempting to run the **set_scan_suppress_toggling** command with the **-selection_method** option set to **manual** and the **-min_slack** option. The **-min_slack** option has no effect when the **-selection method** is **manual**.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this warning message, do not use **-min_slack** when you specify **-selection_method manual**.

SEE ALSO

set_scan_suppress_toggling(2)

TEST-2051 (warning) The -min_slack option is ignored when the -ignore_timing_impact option is set to 'true'.

DESCRIPTION

This warning message occurs when attempting to run the **set_scan_suppress_toggling** command with the **-ignore_timing_impact** option and the **-min_slack** option. The **-ignore_timing_impact** option has higher priority, so the **-min_slack** option is ignored.

WHAT NEXT

This is only a warning message. No action is required.

However, you can avoid this message by not using the **-min_slack** and **-ignore_timing_impact** options together.

SEE ALSO

set_scan_suppress_toggling(2)

TEST-2052 (warning) No gating will be inserted on pin '%s' because of its timing slack '%f'.

DESCRIPTION

The **insert_dft** command issues this warning message when it is enabled by the **set_scan_suppress_toggling** command to perform gating of scan cells' functional output pins for power reduction during scan shift. This message occurs when the timing impact of gating is taken into account. The message indicates the candidate pin that was not considered for gating and its timing slack.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this message, review the design constraints and the constraints you passed through the **set_scan_suppress_toggling** command, and make changes if necessary.

SEE ALSO

remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)
set_scan_suppress_toggling(2)

TEST-2053 (warning) Output pin '%s' will be gated despite its timing slack '%f'.

DESCRIPTION

The **insert_dft** command issues this warning message when it is enabled by the **set_scan_suppress_toggling** command to perform gating of scan cells' functional output pins for power reduction during scan shift. This message occurs when you set the **-ignore_timing_impact** option to **true**. It indicates that the candidate pin is considered for gating, regardless of its timing slack.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this message, review the design constraints and the constraints you passed through the **set_scan_suppress_toggling** command, and make changes if necessary.

SEE ALSO

remove_scan_suppress_toggling(2)
report_scan_suppress_toggling(2)
set_scan_suppress_toggling(2)

TEST-2054 (warning) Constant pins of DFT-modeled instance %s(%s) are incorrectly controlled in all_dft mode.

DESCRIPTION

The **dft_drc** command issues this warning message while validating a test model instance connectivity. The warning may be serious. It indicates that at least one constant pin (with the Constant data type) on the DFT-modeled instance is not set to its expected logical value, as a result of the instance integration.

WHAT NEXT

This is only a warning message. No action is required.

However, you can look for the accompanying TEST-2055 information message(s) for the details on which pins are concerned.

SEE ALSO

TEST-2055(n)

TEST-2055 (information) Expected value on pin '%s/%s': %s, actual value is: %s.

DESCRIPTION

The **dft_drc** command issues this message while validating test model instance connectivity. This information message explains reason why the TEST-2054 warning was issued.

WHAT NEXT

This is an information-only message. No action is required.

SEE ALSO

TEST-2054(n)
TEST-2056(n)

TEST-2056 (information) Violating all segments of cell instance %s(%s).

DESCRIPTION

The **dft_drc** command issues this message while validating test model instance connectivity. This information message explains the consequence of getting the TEST-2054 warning message.

WHAT NEXT

This is an information-only message. No action is required.

SEE ALSO

TEST-2054(n)
TEST-2055(n)

TEST-2057 (warning) Mode control pins of DFT-modeled

instance %s(%s) are incorrectly controlled in all_dft mode.

DESCRIPTION

The **dft_drc** command issues this warning message while validating a test model instance connectivity. The warning is serious. It indicates that at least one test mode pin on the DFT-modeled instance is not set to its expected logical value, as a result of the instance integration.

WHAT NEXT

This is only a warning message. No action is required.

However, you can look for the accompanying TEST-2055 information message(s) for the details on which pins are concerned.

SEE ALSO

TEST-2055(n)
TEST-2056(n)

TEST-11120 (Error) The CTL model for the design ’%s’ does not have a mode of type ’Normal’. The model obtained after insert_dft may not be accurate.

DESCRIPTION

Core wrapping and Core Integration flows require that the test model for the current design have a mode with type ’Normal’. You get this message because the model found on the design does not have a normal mode. This typically occurs when you are in a scan chain re-ordering flow when you want to first infer scan structures and then re-order. The correct way to do this is to first run DRC to infer the mission mode of operation. This can be done by the command ’dft_drc -pre_dft’. Then you can infer the scan structures with the command ’dft_drc -infer_scan_structures’. Note that it must be done in two passes.

WHAT NEXT

Run 2 passes of DRC as explained above.

SEE ALSO

dft_drc (2), **insert_dft** (2),

TESTDB-1 (warning) Overwriting existing scan style %s.

DESCRIPTION

This warning tells you that you have overwritten the current scan style using a **set_scan_configuration -style** or **set_scan_style** command. Note that you see this warning if you overwrite the existing scan style with the same scan style.

WHAT NEXT

Check the setting of the scan style with **report_test -configuration**. If the scan style is correct, no action is necessary. However, if you accidentally set the wrong scan style, use the **set_scan_configuration** command to set the correct scan style.

TESTDB-2 (error) Unable to create test vectors database file.

DESCRIPTION

This message is created if there is some system constraint which does not allow creation of the .vdb file in the specified directory. For instance, if the user does not have write priviledge to the target directory, if the disk is full, or if the target machine is inaccessible.

WHAT NEXT

Check the possible causes listed above ensuring that the target directory is accessible, writable and not full.

TESTDB-3 (error) Unable to read test vectors database file '%s'.

DESCRIPTION

The **create_test_patterns** command creates a database file (a vdb file) that contains the generated test patterns. The **write_test** command reads the test patterns from this vdb file then writes the test patterns out to another file in the format you specified.

When **write_test** cannot read the vdb file, it issues this **TESTDB-3** message. This means that either **write_test** could not find the vdb file or it was unable to open the vdb file. Possible causes are

1. You specified an incorrect path name for the vdb file using the -input option of **write_test**.

2. There is some system problem that prevents **write_test** from accessing those vdb file you specified using the -input option of **write_test**. For example, you set protections on the vdb file that do not allow **write_test** to access the file.

3. You didn't run **create_test_patterns**, so no vdb file exists.

4. You created a vdb file in a previous dc_shell session but you didn't specifie the name of this vdb file using the -input option of **write_test**.

WHAT NEXT

Identify the problem, correct the cause, then rerun the **write_test** command.

If you specified a vdb file using the -input option of **write_test**,

* Check that you gave the correct path name for the vdb file.

* Check that the file is accessible if it is on a remote machine.

* Check that the protections on the file allow DFT Compiler to read the file.

If you didn't run **create_test_patterns** to create a vdb file, run **create_test_patterns**.

If you created the vdb file in a previous dc_shell session, explicitly specify the pathname of the vdb file using the -input option of **write_test**.

SEE ALSO

create_test_patterns (2), **write_test** (2).

TESTDB-4 (error) Invalid test vector database file '%s'.

DESCRIPTION

You see this message when **write_test** has opened, but is unable to process the vdb file you specified with the command's -input option. If you do not explicitly specify a vdb file with -input, the current vdb file that you created with **create_test_patterns** in the same dc_shell session will be opened.

If **write_test** is unable to process the file, either no vectors are saved in the vdb file or the vdb file is some how corrupted.

WHAT NEXT

Review the output from the **create_test_patterns** command that created the vdb file.

If **create_test_patterns** did not save any patterns, you get a warning message that gives you details as to why no patterns were saved. Identify and correct the cause then rerun **create_test_patterns** and **write_test**.

In particular, note that if the design's scan configuration indicates that a design is pre-scan, **create_test_patterns** will not save any patterns since without a scan chain the patterns cannot be applied to the design. You can check the scan state of a design with **report_test -scan_status**. If you did not insert scan into the design and there is no existing scan in the design, you must run **insert_scan** to insert scan before you can generate and save test patterns. If the design is an ASCII netlist with existing scan, you need to issue the command **set_scan_configuration -existing_scan true** and rerun **check_test** before **create_test_patterns** will save any patterns.

If **create_test_patterns** did save vectors, but **write_test_patterns** cannot process the file, either there is a defect in **create_test_patterns** or in some way the vdb file was corrupted after its creation, such as a bad disk. The vdb file is stored in a binary format, which you should not edit or modify. Try rerunning fbcreate_test_patterns and **write_test**. If the problem persists, contact local Synopsys support.

TESTDB-5 (warning) User defined test protocol deleted.

DESCRIPTION

This message indicates that a test protocol for the current design previously read in using the **read_test_protocol** command has been deleted. Deletion of the protocol occurs automatically if it becomes obsolete, which typically happens because the ports of the design have changed. An example is when the **insert_test** command is run, which adds extra ports for test signals. If further test commands are executed, for example **create_test_patterns**, a new protocol will be automatically inferred. However, this protocol may not have the same behavior as the previous user-supplied protocol.

WHAT NEXT

Assuming the **read_test_protocol** command had been used to supply a custom test protocol specifically developed for the design, it is necessary to re-execute the **read_test_protocol** command to read in the custom protocol. If the ports of the design have changed, for example, if additional scan test ports have been added by the **insert_test** command, then it may be necessary to edit the protocol file before it can be read.

TESTDB-6 (error) Port '%s' has an undefined direction.

Unpredictable behavior might result.

DESCRIPTION

If DFT Compiler encounters a port with unknown direction, DFT Compiler might exhibit unpredictable behavior during test-protocol generation and design-rule checking.

WHAT NEXT

Determine why the port was assigned an unknown direction. One possible cause is that if a hierarchical design has been read using Verilog, but a lower level of hierarchy has not be read in, the direction of a signal defined in the lower level will be unknown.

TESTDB-100 (warning) Renaming port from '%s' to '%s'.

DESCRIPTION

The **write_test** command issues this warning when a port name in the netlist does not conform to the naming rules of the vector format you specified with the -format option. The warning message shows you both the port name in the netlist format and the port name in the vector file it is creating.

WHAT NEXT

If your ASIC Vendor's sign-off flow can accept the different names in the netlist and in the vectors, no action is necessary. Otherwise, you need to change the names of the ports in the netlist so that the netlist and vector files use the same port names. You can achieve this by setting appropriate naming rules with the define_name_rules and the bus_naming_style variables and the **change_names** command.

If you use one of the CTV Formats, consult the CTV Formats Reference Manual for guidance. For other formats, consult your ASIC Vendor for guidance on port naming rules.

SEE ALSO

write_test (2), **define_name_rule** (2), **bus_naming_style,** (2), **change_names** (2).

TESTDB-223 (error) Value of attribute '%s' must be a float (line:

%d).

DESCRIPTION

The value should be a float number.

WHAT NEXT

Check your test protocol.

TESTDB-224 (error) Value of attribute '%s' must be a list of two float values (line: %d).

DESCRIPTION

The value of the attribute must be a list of two floating point values.

WHAT NEXT

Check your test protocol.

TESTDB-225 (error) Value of attribute '%s' must not be less than zero (line: %d).

DESCRIPTION

The value should be less than zero.

WHAT NEXT

TESTDB-254 (error) Scan chain specification '%s' includes repeated elements.

DESCRIPTION

A scan chain is a connected sequence of scan elements (scan cells, segments, links and design instances). A scan element can only appear at exactly one chain position. Scan chain specifications that include repeated elements are in error.

WHAT NEXT

Remove repeated elements from the chain, and reapply the **set_scan_path** command.

TESTDB-255 (warning) Scan chain '%s' overwrites an earlier specification.

DESCRIPTION

DFT Compiler does not allow scan chains to be specified using multiple **set_scan_path** commands. This warning tells you that an earlier specification is being overwritten.

WHAT NEXT

Establish whether you want the specification to be overwritten. If not, combine the two specifications into one **set_scan_path** command.

TESTDB-256 (error) Scan chains '%s' and '%s' have common elements.

DESCRIPTION

DFT Compiler does not let scan chains share scan elements (cells or design instances). This error tells you that some elements belong to more than one chain.

WHAT NEXT

If the common elements can be removed from the scan chain you're specifying, remove them and reapply the **set_scan_path** command. Otherwise, apply the **remove_scan_specifications** command and start again.

TESTDB-257 (warning) Overwriting previously specified '%s' port '%s'.

DESCRIPTION

DFT Compiler uses one scan enable signal to enable scan mode and one test mode signal to enable test mode. This message warns that either you used the **set_scan_signal** command to specify more than one scan enable, or you used the **set_dft_signal** command to specify more than one test mode signal. The second

specification overwrites the first.

WHAT NEXT

Verify that you do want to overwrite the specification. Repeat both the newest specification and the corrected specification if the overwrite was mistaken.

TESTDB-258 (warning) Overwriting previously specified signal on port '%s'. Signal type '%s' conflicts with old type '%s'.

DESCRIPTION

DFT Compiler only associates exactly one signal type with a design port. This message warns that you used the **set_scan_signal** or **set_dft_signal** command to associated a second type with a design port, and that the second specification has overwritten the first.

WHAT NEXT

Check that you do want to overwrite the specification. Repeat both it and the corrected specification if the overwrite was mistaken.

TESTDB-259 (warning) Overwriting previously specified scan signal on port '%s'. Access pin '%s' conflicts with old pin '%s'.

DESCRIPTION

DFT Compiler only associates exactly one access pin with a design port. This message warns that you have used the **set_scan_signal** command to associated a second access pin with a design port, and that the second specification has overwritten the first.

WHAT NEXT

Check that you do want to overwrite the specification. Repeat both it and the corrected specification if the overwrite was mistaken.

TESTDB-260 (warning) Overwriting previously specified '%s' for

chain '%s'.

DESCRIPTION

DFT Compiler only associates exactly one scan signal with a particular type to a scan chain. This message warns that you have used the **set_scan_signal** command to associate a second scan signal of a particular type with a scan chain, and that the second specification has overwritten the first.

WHAT NEXT

Check that you do want to overwrite the specification. Repeat both it and the corrected specification if the overwrite was mistaken.

TESTDB-261 (warning) Overwriting scan signal '%s'. Can not share access pin '%s' with signal '%s'.

DESCRIPTION

DFT Compiler only lets you associate a scan access pin with exactly one scan signal. This message warnings you that you have used the **set_scan_signal** command to associate a scan access pin with a second scan signal. The first specification is overwritten.

WHAT NEXT

Check that you do want to overwrite the specification. Repeat both it and the corrected specification if the overwrite was mistaken.

TESTDB-262 (warning) '%s' is the name of an existing scan link. It will be overwritten.

DESCRIPTION

You receive this message because you have used the **set_scan_link** command to specify a scan link that has the same name as an existing scan link. You cannot have more than one scan link with the same name. DFT Compiler is overwriting the previous specification with the current one.

WHAT NEXT

If you intended to overwrite the previous scan link specification, then no further

action is necessary. However, if the overwrite is not intended, determine and correct the cause of the error and use the **set_scan_link** command to respecify both scan links.

SEE ALSO

set_scan_link (2).

TESTDB-263 (error) Scan chains '%s' and '%s' have common elements. Segment states are considered.

DESCRIPTION

DFT Compiler does not let scan chains share scan elements (cells or design instances). This error tells you that some elements belong to more than one chain. Furthermore the conflict is only visible when segments states are considered. This mean that one chain has an element that belongs to a segment in another chain.

WHAT NEXT

If the common elements can be removed from the scan chain you're specifying, remove them and reapply the **set_scan_path** command. Otherwise, apply the **remove_scan_specifications** command or **set_scan_segment** commands and start again.

TESTDB-264 (error) An existing scan segment has the name '%s'. Scan link specification is discarded.

DESCRIPTION

When you specify a scan link, DFT Compiler checks that no scan segment has the same name. Otherwise scan chain specifications will be ambiguous. This message tells you that you have specified a scan link using the same name as an existing scan segment. Your scan link specification is discarded.

WHAT NEXT

Change the name of your scan link. Alternatively, apply the **remove_scan_specifications** command and start again.

TESTDB-265 (error) Scan segment specification '%s' includes

repeated elements.

DESCRIPTION

A scan segment is a connected sequence of scan elements (scan cells and design instances). A scan element can only appear at exactly one segment position. Scan segment specifications that include repeated elements are in error.

WHAT NEXT

Remove repeated elements from the segment, and reapply the **set_scan_segment** command.

TESTDB-266 (warning) Scan segment '%s' updates an earlier specification.

DESCRIPTION

DFT Compiler lets you specify scan segments using multiple **set_scan_segment** commands. This warning tells you that an earlier specification is being updated.

WHAT NEXT

Establish that you want the specification to be updated. If not, remove the scan segment using the **remove_scan_specifications** command, or specify the scan segment you want using a different name.

TESTDB-267 (error) Scan segments '%s' and '%s' have common elements.

DESCRIPTION

DFT Compiler does not let scan segments share scan elements (cells or design instances). This error tells you that some elements belong to more than one segments.

WHAT NEXT

If the common elements can be removed from the scan segments you're specifying, remove them and reapply the **set_scan_segments** command. Otherwise, apply the **remove_scan_specifications** command and start again.

TESTDB-268 (error) An existing scan link has the name '%s'. Scan segment specification is discarded.

DESCRIPTION

When you specify a scan segment, DFT Compiler checks that no scan link has the same name. Otherwise scan chain specifications will be ambiguous. This message tells you that you have specified a scan segment using the same name as an existing scan link. Your scan segment specification is discarded.

WHAT NEXT

Change the name of your scan segment. Alternatively, apply the **remove_scan_specifications** command and start again.

TESTDB-269 (warning) Scan segment '%s' shares elements with chain '%s'. Cannot use segment to specify chains.

DESCRIPTION

When you specify a scan segment, DFT Compiler checks that it shares no states with an existing scan chain. Otherwise you will not be able to use the segment to specify a scan chain until common elements are removed. This message tells you that you have specified a scan segment that shares elements with an existing scan chain.

WHAT NEXT

Specify your scan segment again, eliminating common elements, or remove common elements from the scan chain specification.

TESTDB-270 (warning) Scan segment '%s' overwrites an earlier specification that has a different scan style.

DESCRIPTION

DFT Compiler lets you specify scan segments using multiple **set_scan_segment** commands. This warning tells you that an earlier specification is being overwritten because it has a different scan style.

WHAT NEXT

Establish that you want the specification to be overwritten. If not, remove the scan segment using the **remove_scan_specifications** command, or specify the scan segment you want using a different name.

TESTDB-271 (warning) Your scan chain specification includes a sequence of %d scan links. All but the first is discarded.

DESCRIPTION

DFT Compiler lets you include scan links in scan chain specifications. These tell DFT Compiler how to connect two chain elements together. It makes no sense to use a sequence of scan links to connect scan elements. This message tells you that this condition has been identified. All but the first link is discarded.

WHAT NEXT

Check that you do want all but the first scan link discarded. If not, enter the correct specification.

TESTDB-272 (error) Scan chain specification '%s' includes repeated elements when segments are expanded.

DESCRIPTION

A scan chain is a connected sequence of scan elements (scan cells, segments, links and design instances). A scan element can only appear at exactly one chain position. Scan chain specifications that include repeated elements are in error, even if those elements are hidden by a segment specification.

WHAT NEXT

Remove repeated elements from the chain or segment, and reapply the **set_scan_path** command.

TESTDB-273 (warning) Net '%s' specified in trace_nets()

statement does not exist in the design (line: %d).

DESCRIPTION

The net specified by trace_nets() statement does not exist in the design.

WHAT NEXT

Check your design if the net exists.

TESTDB-274 (warning) Could not delete signal_type attribute on port '%s'.

DESCRIPTION

This warning message indicates that **remove_scan_specifications** could not remove the **signal_type** attribute from the specified port, probably because there is no **signal_type** attribute on that port.

WHAT NEXT

Verify that there is no **signal_type** attribute on the port.

TESTDB-275 (warning) Can not find scan chain '%s' to delete it.

DESCRIPTION

The remove_scan_specifications command deletes named scan chains. You see the following message when you've asked DFT Compiler to remove a scan chain, but DFT Compiler can't find it. This means that there is no such chain.

WHAT NEXT

Check the way you've spelled the scan chain name, and reapply the remove_scan_specifications command. If this doesn't work, make sure that you haven't removed the chain already.

TESTDB-276 (warning) Can not find scan segment '%s' to

delete it.

DESCRIPTION

The remove_scan_specifications command deletes named scan segments. You see the following message when you've asked DFT Compiler to remove a scan segment, but DFT Compiler can't find it. This means that there is no such segment.

WHAT NEXT

Check the way you've spelled the scan segment name, and reapply the remove_scan_specifications command. If this doesn't work, make sure that you haven't removed the segment already.

TESTDB-277 (warning) Can not find scan link '%s' to delete it.

DESCRIPTION

The remove_scan_specifications command deletes named scan links. You see the following message when you've asked DFT Compiler to remove a scan link, but DFT Compiler can't find it. This means that there is no such link.

WHAT NEXT

Check the way you've spelled the scan link name, and reapply the remove_scan_specifications command. If this doesn't work, make sure that you haven't removed the link already.

TESTDB-278 (warning) Can not find scan signal on port '%s' to delete it.

DESCRIPTION

The remove_scan_specifications command deletes scan signals associated with named ports. You see the following message when you've asked DFT Compiler to remove a scan signal, but DFT Compiler can't find it. This means that there is no such signal.

WHAT NEXT

Check the way you've spelled the port name, and reapply the remove_scan_specifications command. If this doesn't work, make sure that you haven't removed the signal already.

TESTDB-279 (information) Using default scan style '%s'.

DESCRIPTION

If you do not use the **set_scan_configuration** command to tell DFT Compiler what scan style to use, DFT Compiler will choose a default scan style by looking at the value of an environment variable. This message tells you that this has happened.

WHAT NEXT

If you don't like the scan style, specify another using the **set_scan_configuration** command, or change your environment.

TESTDB-281 (error) Unable to open '%s' for reading.

DESCRIPTION

The **read_pin_map** command lets you read the port-to-pin map files for Boundary Scan Designs. If the port-to-pin map file cannot be opened for reading, the **read_pin_map** command produces this error message.

WHAT NEXT

Ensure that the port-to-pin map file specified exists and has read permissions.

TESTDB-282 (error) %s at or near token '%s' (Line: %d).

DESCRIPTION

The **read_pin_map** command lets you read the port-to-pin map files for Boundary Scan Designs. If there is an error while parsing the port-to-pin map file, the **read_pin_map** command produces this error.

WHAT NEXT

Fix the syntax error in the port-to-pin map file and reissue the **read_pin_map** command.

TESTDB-283 (warning) The '%s' port does not map to any

package pin.

DESCRIPTION

The **read_pin_map** command lets you read the port-to-pin map files for Boundary Scan Designs. Each signal port in the design must map to a package pin. If a signal port in the design does not map to any package pin, the **read_pin_map** command produces this warning message.

WHAT NEXT

Specify a pin mapping for the port in the port-to-pin map file if necessary.

TESTDB-284 (error) The '%s' port maps to %d package pins.

DESCRIPTION

The **read_pin_map** command lets you read the port-to-pin map files for Boundary Scan Designs. Each signal port in the design must map to a single package pin. If a signal port in the design maps to multiple package pins, the **read_pin_map** command produces this error message.

WHAT NEXT

Ensure that the port maps to a single package pin in the port-to-pin map file.

TESTDB-285 (error) Multiple (%d) design ports map to the '%s' package pin.

DESCRIPTION

The **read_pin_map** command lets you read the port-to-pin map files for Boundary Scan Designs. Each signal port in the design must map to a single package pin. If multiple design ports map to the same package pin, the **read_pin_map** command produces this error message.

WHAT NEXT

Ensure that multiple ports do not to a single package pin in the port-to-pin map file.

TESTDB-286 (error) No package command found in the pin map file.

DESCRIPTION

The **read_pin_map** command lets you read the port-to-pin map files for Boundary Scan Designs. If the package name is missing from the port-to-pin map file, the **read_pin_map** command produces this error message.

WHAT NEXT

Add a package record to the port-to-pin map file.

TESTDB-287 (error) The %s index of the '%s' bus in the pin map file is inconsistent with the bounds for the corresponding design bus.

DESCRIPTION

The **read_pin_map** lets you read the port-to-pin map files for Boundary Scan Designs. If the bounds for a signal bus in a port-to-pin map file are not consistent with the bounds for the signal bus in the db design, the **read_pin_map** command produces this error message.

WHAT NEXT

Make sure that the bounds specified for the signal bus in the port-to-pin map file are consistent with those in the db design.

TESTDB-288 (error) The number of package pins specified (%d) does not match the width (%d) of the bus '%s'.

DESCRIPTION

The **read_pin_map** command lets you read the port-to-pin map files for Boundary Scan Designs. If the number of package pins specified for a bus is not equal to the width of the bus, the **read_pin_map** command produces this error message.

WHAT NEXT

Ensure that the number of package pins for a bus in the pin map file equals the width of the bus.

TESTDB-289 (warning) Overwriting the scan state of the design from '%s' to '%s'.

DESCRIPTION

Scan state is used to store the state of scan circuitry inserted. This scan state will be automatically updated when executing **insert_scan**. However, it can be unconditionally changed when the user adds attributes to the design to indicate that the design is **test_ready**, **scan_replaced**, or **test_cell**. You can use **report_test -state** to report the current scan state of a design.

WHAT NEXT

Changing the scan state of a design by setting attributes is not encouraged. Use the command **set_scan_configuration -existing_scan false** which can reset the design into its initial scan state.

TESTDB-290 (warning) The client %s specified is not a valid dft client.

DESCRIPTION

You receive this message during execution of **preview_dft** or **insert_dft** if the environment variable **test_default_client_order** is set with an invalid value for the dft client. Valid values are *autofix*, to specify the Autofix utility as dft client; or *wrapper*, to specify the Shadow LogicDFT utility as dft client.

WHAT NEXT

Set the **test_default_client_order** variable with a valid value. Then reexecute **preview_dft** or **insert_dft**.

SEE ALSO

insert_dft (2), **preview_dft** (2); **test_default_client_order** (3).

TESTDB-291 (information) reverting value of environment variable '%s' to its default value. The default value is set to no client.

DESCRIPTION

You receive this message during execution of **preview_dft** or **insert_dft** if the environment variable **test_default_client_order** is set with an invalid value for the dft client. Valid values are *autofix*, to specify the Autofix utility as client; and *wrapper*, to specify the Shadow LogicDFT utility as client. The default is the empty string {}, meaning that there is no client. This message informs you that the environment variable is being set to its default value.

WHAT NEXT

If it is acceptable to you that the **test_default_client_order** environment variable is set to the empty string, no action is required on your part. Otherwise, set the **test_default_client_order** variable with a valid nondefault value and reexecute **preview_dft** or **insert_dft**.

SEE ALSO

insert_dft (2), **preview_dft** (2); **test_default_client_order** (3).

TESTDB-292 (Warning) The test model does not match the '%s' interface.

DESCRIPTION

The Signals of the test model don't match the ports of the design. In order for a test model to be valid, its Signals must match one to one the ports of the design, by name and by direction.

WHAT NEXT

The next message tells you what the tool has done with the model.

SEE ALSO

TESTDB-293 (Information) The test model is %s.

DESCRIPTION

The tool has detected some inconsistency between the test model and the design. This message indicates what action the tool has taken.

WHAT NEXT

You may wish to review your scripts to understand the root cause of the inconsistency. If the action was 'deleted', the tool will attempt to regenerate a model. You should check the accuracy of this new model.

SEE ALSO

"

TESTDB-294 (error) Could not find bus bit '%s[%d]'.

DESCRIPTION

The **read_pin_map** command lets you read the port-to-pin map files for Boundary Scan Designs. You get this error message when the pin map file refers to a bus bit that **read_pin_map** cannot find in the design.

WHAT NEXT

Check to see if the bus bit in the error message indeed exists in the design. If not, fix the pin map file and re-issue the **read_pin_map** command.

"

TESTDB-295 (error) Could not find bus '%s'.

DESCRIPTION

The **read_pin_map** command lets you read the port-to-pin map files for Boundary Scan Designs. If the pin map file contains a line that maps an object to a list of pins, the **read_pin_map** command assumes that the object is a bus. You get this error message when the pin map file refers to a bus that that **read_pin_map** cannot find in

the design.

WHAT NEXT

Check to see if the object referred to in the error message is indeed a bus. If not, fix the pin map file and re-issue the **read_pin_map** command.

TESTDB-301 (warning) Can not find wrapper chain '%s' to delete it.

DESCRIPTION

The remove_core_wrapper_specification command deletes named wrapper chains. You see the following message when you've asked DFT Compiler to remove a wrapper chain, but DFT Compiler can't find it. This means that there is no such chain.

WHAT NEXT

Check the way you've spelled the wrapper chain name, and reapply the remove_core_wrapper_specification command. If this doesn't work, make sure that you haven't removed the chain already.

TESTDB-302 (error) Wrapper chains '%s' and '%s' have common elements.

DESCRIPTION

DFT Compiler does not let wrapper chains share wrapper cell elements. This error tells you that some elements belong to more than one chain.

WHAT NEXT

If the common elements can be removed from the wrapper chain you're specifying, remove them and reapply the **set_core_wrapper_path** command. Otherwise, apply the **remove_core_wrapper_specification** command and start again.

TESTDB-303 (warning) Wrapper chain '%s' overwrites an

earlier specification.

DESCRIPTION

DFT Compiler does not allow wrapper chains to be specified using multiple **set_core_wrapper_path** commands. This warning tells you that an earlier specification is being overwritten.

WHAT NEXT

Establish whether you want the specification to be overwritten. If not, combine the two specifications into one **set_core_wrapper_path** command.

TESTDB-304 (error) Wrapper chain specification '%s' includes repeated elements.

DESCRIPTION

A wrapper chain is a connected sequence of wraper cell elements. A wrapper cell element can only appear at exactly one chain position. Wrapper chain specifications that include repeated elements are in error.

WHAT NEXT

Remove repeated elements from the chain, and reapply the **set_core_wrapper_path** command.

TESTDB-501 (error) Incorrect number of ports and signal values in the test protocol.

DESCRIPTION

The ports and signal values specified in the test protocol does not match with the design.

WHAT NEXT

Check your design and the test protocol whether they have the same number of ports and signals, and the names are equivalent.

TESTGEN

TESTGEN-1 (information) reverting value of environment variable '%s' to its default value '%s'.

DESCRIPTION

DFT Compiler validates the values of environment variables it uses. You see this message when an environment variable value is invalid. DFT Compiler supplies a default.

WHAT NEXT

Confirm that the environment variable is invalid. Modify the environment variable value to remove the warning.

TESTGEN-2 (Warning) '%s' is not a valid scan style.

DESCRIPTION

DFT Compiler validates the values of environment variables it uses. You see this message when an environment variable that needs to specify a scan style specifies an invalid one. DFT Compiler will use a default scan style.

WHAT NEXT

Confirm that the environment variable is invalid. Modify the environment variable value to remove the warning.

TESTGEN-3 (Warning) '%s' is not 'true' or 'false'.

DESCRIPTION

DFT Compiler validates the values of environment variables it uses. You see this message when an environment variable that needs to specify either 'true' or 'false' specifies something else. DFT Compiler will use a default value.

WHAT NEXT

Confirm that the environment variable is invalid. Modify the environment variable value to remove the warning.

TESTGEN-4 (warning) Cannot associate a '%s' signal with chain '%s'.

DESCRIPTION

DFT Compiler uses one scan enable signal to enable scan mode. This message warns that you used the **set_scan_signal** command to associate a scan enable with a specific scan chain. Because the scan enable is associated with all scan chains, the specific association is ignored.

WHAT NEXT

Remove the association to suppress the warning.

TESTGEN-5 (information) reverting value of environment variable '%d' to its default value '%d'.

DESCRIPTION

DFT Compiler validates the values of environment variables it uses. You see this message when an environment variable value is invalid. DFT Compiler supplies a default.

WHAT NEXT

Confirm that the environment variable is invalid. Modify the environment variable value to remove the warning.

TESTGEN-6 (Warning) '%s' does not include the substring '%%s'.

DESCRIPTION

DFT Compiler validates the values of environment variables it uses. You see this message when an environment variable that needs include the substring "%s" does not. DFT Compiler will use a default value.

WHAT NEXT

Confirm that the environment variable is invalid. Modify the environment variable value to remove the warning.

TESTGEN-7 (warning) Hookup sense value '%s' conflicts with the old value '%s'.

DESCRIPTION

DFT Compiler only associates exactly one hookup sense between a design port and an internal hookup pin. This message warns that you have used the **set_scan_signal** command to associate a second hookup sense, and that the second specification has overwritten the first.

WHAT NEXT

Check that you do want to overwrite the specification. Repeat the correct specification if the overwrite was mistaken.

TESTXG-1 (error) Invalid Timing specification [%f, %f] or timing is not specified for the clock signal

DESCRIPTION

The rise time and fall time values specified by the -timing switch of the set_dft_signal command are not valid or not specified. Also the timing specification should be provided when -view option of set_dft_signal is existing_dft and not spec.

WHAT NEXT

Please check the timing values

SEE ALSO

set_dft_signal

TESTXG-2 (Warning) Model is user defined

DESCRIPTION

This message indicates that the model has been specified through a read_test_model command. Users must specify a complete model or let the tool create one. A user defined model cannot be modified through other command such as DFT signal specifications or scan path specifications.

WHAT NEXT

Check the specified model to ensure it is the one desired. Else remove the model and let the tool create one for you.

SEE ALSO

remove_test_model create_test_protocol set_dft_signal set_scan_path

TESTXG-3 (Error) Cannot associate multiple ports with hookup

pin

DESCRIPTION

This message indicates that and attempt has been made to associate more than one port to hookup pins using the set_dft_signal command. When using the -hookup option, only one port may be specified.

WHAT NEXT

Specify a single port or do not specify the -hookup option

SEE ALSO

remove_dft_signal

TESTXG-4 (Error) Scan-in and Scan-out ports not specified

DESCRIPTION

This message indicates that a set_scan_path -view existing_dft command has been issued to specify a scan chain, but the scan-in and scan-out ports for the chain have not been specified. The -view existing_dft option implies that the scan chain already exists in the design; therefore you must associate the scan access terminals with this scan chain.

WHAT NEXT

Specify the scan-in and scan-out ports for this scan path OR Remove the -view existing_dft specification

SEE ALSO

set_dft_signal remove_dft_signal remove_scan_path

TESTXG-5 (Error) Invalid design specification

DESCRIPTION

This message indicates that a design specification is required or that the specified design cannot be found

WHAT NEXT

Specify a valid design

SEE ALSO

read_test_model write_test_model

TESTXG-6 (Error) Mode %s already exists in view %s

DESCRIPTION

This message indicates that an attempt has been made to define a mode that already exists, in the specified view.

WHAT NEXT

Change the name of the mode to be defined or remove the existing mode first.

SEE ALSO

define_test_mode list_test_modes remove_test_mode

TESTXG-7 (Error) Mode %s does not exist

DESCRIPTION

This message indicates that the specified mode does not exist

WHAT NEXT

Check the name of the mode specified

SEE ALSO

list_test_modes

TESTXG-8 (Warning) Specifications will apply to custom

protocol

DESCRIPTION

This message indicates that the specification will apply to the custom protocol only and will be removed when the custom protocol is removed through a remove_test_protocol command. This message occurs when a specification is made after a custom protocol is read using the read_test_protocol command.

WHAT NEXT

Check the name of the mode specified

SEE ALSO

list_test_modes

TESTXG-9 (Error) Scan Path %s does not exist

DESCRIPTION

This message indicates that the specified scan path does not exist

WHAT NEXT

Check the name of the specified scan path

SEE ALSO

report_dft -scan preview_dft insert_dft dft_drc set_scan_path remove_scan_path

TESTXG-10 (Error) TestMode or ScanEnable signal type not specified for the port %s.

DESCRIPTION

This message indicates that a set_autofix_configuration -control_signal command or a set_autofix_element -control_signal command has been issued, but the TestMode or the ScanEnable signal type has not been specified for the port. Note that a ScanEnable port can only be used for the type set or reset and for the method gate.

WHAT NEXT

Specify the TestMode or the ScanEnable signal type for the port.

SEE ALSO

set_dft_signal reset_dft_signal set_autofix_configuration
reset_autofix_configuration set_autofix_element reset_autofix_element

TESTXG-11 (Error) TestData signal type not specified for the port %s.

DESCRIPTION

This message indicates that a set_autofix_configuration -test_data command or a set_autofix_element -test_data command has been issued, but the TestData signal type has not been specified for the port.

WHAT NEXT

Specify the TestData signal type for the port.

SEE ALSO

set_dft_signal reset_dft_signal set_autofix_configuration
reset_autofix_configuration set_autofix_element reset_autofix_element

TESTXG-12 (Error) ScanEnable signal cannot be used as a control signal for the method %s.

DESCRIPTION

This message indicates that a set_autofix_configuration -control command or a set_autofix_element -control command has been issued, but a ScanEnable signal can only be used as a control signal to autofix sets and resets when the specified method is gate.

WHAT NEXT

Specify a TestMode signal OR Specify a gate method when the type is set or reset .

SEE ALSO

set_dft_signal reset_dft_signal set_autofix_configuration
reset_autofix_configuration set_autofix_element reset_autofix_element

TESTXG-13 (Error) The method cannot be specified for the type %s.

DESCRIPTION

This message indicates that a set_autofix_configuration -method command or a set_autofix_element -method command has been issued, but either the -method option cannot not be specified for the specified type or the specified method is not correct for the specified type.

WHAT NEXT

Remove the -method option if you cannot define the -method option for the specified type OR Specify a method, which is allowed by the specified type.

SEE ALSO

set_dft_signal reset_dft_signal set_autofix_configuration
reset_autofix_configuration set_autofix_element reset_autofix_element

TESTXG-14 (Error) This option cannot be used with the type %s.

DESCRIPTION

This message indicates that a set_autofix_configuration -fix_latch or -fix_data command or a set_autofix_element -fix_latch or -fix_data command has been issued, but these options cannot be used with the specified type. These options are valid for the following types: set, reset and clock.

WHAT NEXT

Remove the -fix_latch and/or the -fix_data options.

SEE ALSO

set_autofix_configuration reset_autofix_configuration set_autofix_element
reset_autofix_element

TESTXG-15 (Error) A clock signal type has been specified for the port %s.

DESCRIPTION

This message indicates that a set_autofix_configuration -type set/reset -test_data command or set_autofix_element -type set/reset -test_data command has been issued, but the port to be used as a source to autofix asynchronous signals has been specified as a clock signal type.

WHAT NEXT

Specify another port which does not have a clock signal type OR Remove the clock signal type from the port and re-issue the command.

SEE ALSO

set_dft_signal reset_dft_signal set_autofix_configuration reset_autofix_configuration set_autofix_element reset_autofix_element

TESTXG-16 (Error) The element %s cannot be specified in both include_elements and exclude_elements options.

DESCRIPTION

This message indicates that a set_autofix_configuration -include_elements -exclude_elements command has been issued, but an element cannot included and excluded from being autofixed.

WHAT NEXT

Remove the element from exclude_elements, if you want the element to be autofixed OR Remove the element from include_elements, if you do not want the element to be autofixed.

SEE ALSO

set_autofix_configuration reset_autofix_configuration

TESTXG-17 (Error) The element %s is not in the

include_elements of the autofix configuration.

DESCRIPTION

This message indicates that a set_autofix_element command has been issued, but the element was not specified in the set_autofix_configuration -include_elements command for the specified type.

WHAT NEXT

Add the element to the include_elements of the autofix configuration for the specified type OR Remove the element from the elements of the set_autofix_element command.

SEE ALSO

set_autofix_configuration reset_autofix_configuration set_autofix_element reset_autofix_element

TESTXG-18 (Error) The element %s is in the exclude_elements of the autofix configuration.

DESCRIPTION

This message indicates that a set_autofix_element command has been issued, but the element was specified in the set_autofix_configuration -exclude_elements command for the specified type.

WHAT NEXT

Remove the element from the exclude_elements of the autofix configuration for the specified type OR Remove the element from the elements of the set_autofix_element command.

SEE ALSO

set_autofix_configuration reset_autofix_configuration set_autofix_element reset_autofix_element

TESTXG-19 (Information) Overwriting the default autofix

configuration for the type %s.

DESCRIPTION

This message indicates that a set_autofix_configuration command has been issued. The specified autofix configuration overwrites the default autofix configuration for the specified type.

WHAT NEXT

Reset the autofix configuration for the type if you want to get the default configuration.

SEE ALSO

set_autofix_configuration reset_autofix_configuration

TESTXG-20 (Warning) Overwriting the previous autofix configuration for the type %s.

DESCRIPTION

This message indicates that a set_autofix_configuration command has been issued. The specified autofix configuration overwrites the previous autofix configuration for the specified type.

WHAT NEXT

Reset the autofix configuration for the type if you want to get the default configuration.

SEE ALSO

set_autofix_configuration reset_autofix_configuration

TESTXG-21 (Error) A Reset signal type has been specified for the port %s.

DESCRIPTION

This message indicates that a set_autofix_configuration -type clock -test_data

command or a set_autofix_element -type clock -test_data command has been issued, but the port to be used as a source to autofix clocks has been specified as a Reset signal type.

WHAT NEXT

Specify another port which does not have a Reset signal type OR Remove the Reset signal type from the port and re-issue the command.

SEE ALSO

set_dft_signal reset_dft_signal set_autofix_configuration reset_autofix_configuration set_autofix_element reset_autofix_element

TESTXG-22 (Information) The default autofix configuration was already set for the type %s.

DESCRIPTION

This message indicates that a reset_autofix_configuration command has been issued, but the autofix configuration was already the default configuration for the specified type.

WHAT NEXT

Remove the reset_autofix_configuration command for the specified type.

SEE ALSO

set_autofix_configuration reset_autofix_configuration

TESTXG-23 (Error) No autofix configuration exists for the type %s.

DESCRIPTION

This message indicates that a reset_autofix_configuration command has been issued, but the autofix configuration was not set for the specified type.

WHAT NEXT

Remove the reset_autofix_configuration command.

SEE ALSO

set_autofix_configuration reset_autofix_configuration

TESTXG-24 (Information) Overwriting the default testability configuration for the type %s.

DESCRIPTION

This message indicates that a set_testability_configuration command has been issued. The specified testability configuration overwrites the default testability configuration for the specified type.

WHAT NEXT

Reset the testability configuration for the type if you want to get the default configuration.

SEE ALSO

set_testability_configuration reset_testability_configuration

TESTXG-25 (Warning) Overwriting the previous testability configuration for the type %s.

DESCRIPTION

This message indicates that a set_testability_configuration command has been issued. The specified testability configuration overwrites the previous testability configuration for the specified type.

WHAT NEXT

Reset the testability configuration for the type if you want to get the default configuration.

SEE ALSO

set_testability_configuration reset_testability_configuration

TESTXG-26 (Error) TestMode signal type not specified for the port %s.

DESCRIPTION

This message indicates that a set_testability_configuration -control_signal command has been issued, but the TestMode signal type to control the test points has not been specified for the port.

WHAT NEXT

Specify the TestMode signal type for the port.

SEE ALSO

set_dft_signal reset_dft_signal set_testability_configuration reset_testability_configuration

TESTXG-27 (Error) clock signal type not specified for the port %s.

DESCRIPTION

This message indicates that a set_testability_configuration -clock signal command has been issued, but a clock signal type has not been specified for the port.

WHAT NEXT

Specify a clock signal type for the port.

SEE ALSO

set_dft_signal reset_dft_signal set_testability_configuration reset_testability_configuration

TESTXG-28 (Error) The power_saving option cannot be used

with the type %s.

DESCRIPTION

This message indicates that a set_testability_configuration -type control -power_saving command has been issued, but this options cannot be used with the specified type. This option is valid for the type observe.

WHAT NEXT

Remove the -power_saving option.

SEE ALSO

set_testability_configuration reset_testability_configuration

TESTXG-29 (Information) The default testability configuration was already set for the type %s.

DESCRIPTION

This message indicates that a reset_testability_configuration command has been issued, but the testability configuration was already the default configuration for the specified type.

WHAT NEXT

Remove the reset_testability_configuration command for the specified type.

SEE ALSO

set_testability_configuration reset_testability_configuration

TESTXG-30 (Error) No testability configuration exists for the type %s.

DESCRIPTION

This message indicates that a reset_testability_configuration command has been issued, but the testability configuration was not set for the specified type.

WHAT NEXT

Remove the reset_testability_configuration command.

SEE ALSO

set_testability_configuration reset_testability_configuration

TESTXG-31 (Warning) Overwriting the previous autofix configuration for the element %s.

DESCRIPTION

This message indicates that a set_autofix_element command has been issued. The specified autofix configuration overwrites the previous autofix configuration for the specified element.

WHAT NEXT

Reset the autofix configuration for the element if you want to get the default configuration.

SEE ALSO

set_autofix_element reset_autofix_element

TESTXG-32 (Information) The default autofix element configuration is already set for the element of type %s.

DESCRIPTION

This message indicates that a reset_autofix_element command has been issued, but the autofix configuration was already the default configuration for the specified element.

WHAT NEXT

Remove the reset_autofix_element command for the specified element.

SEE ALSO

set_autofix_element reset_autofix_element

TESTXG-33 (Error) No autofix configuration exists for the element %s.

DESCRIPTION

This message indicates that a reset_autofix_element command has been issued, but the autofix configuration was not set for the specified element.

WHAT NEXT

Remove the reset_autofix_element command.

SEE ALSO

set_autofix_element reset_autofix_element

TESTXG-34 (Error) A Reset signal type has to be specified for the port %s.

DESCRIPTION

This message indicates that a set_autofix_configuration -type set/reset -test_data command or a set_autofix_element -type set/reset -test_data command has been issued, but the port to be used as a source to autofix asyncs has to be a Reset signal.

WHAT NEXT

Specify another port which has a Reset signal type OR Set the Reset signal type on the port and re-issue the command.

SEE ALSO

set_dft_signal reset_dft_signal set_autofix_configuration reset_autofix_configuration set_autofix_element reset_autofix_element

TESTXG-35 (Error) A Clock signal type has to be specified for

the port %s.

DESCRIPTION

This message indicates that a set_autofix_configuration -type clock -test_data command or a set_autofix_element -type clock -test_data command or a set_testability_configuration -type control/observe -clock_signal has been issued, but the port to be used as a source to autofix clocks or to be used as a clock for newly inserted control or observe scan registers has to be a Clock signal.

WHAT NEXT

Specify another port which has a Clock signal type OR Set a Clock signal type on the port and re-issue the command.

SEE ALSO

set_dft_signal reset_dft_signal set_autofix_configuration reset_autofix_configuration set_autofix_element reset_autofix_element set_testability_configuration reset_testability_configuration

TESTXG-37 (Error) No user-defined test point configuration exists for the type %s.

DESCRIPTION

This message indicates that a remove_test_point_element command has been issued, but the user-defined test point configuration was not set for the specified type.

WHAT NEXT

Remove the remove_test_point_element command.

SEE ALSO

set_test_point_element remove_test_point_element

TESTXG-38 (Error) Missing option for the set_autofix_element

command.

DESCRIPTION

This message indicates that a set_autofix_element command has been issued, but the autofix configuration for the specified element cannot be accepted due to missing options. At least, one of the following options has to be specified (if applicable for the type): -control_signal, -test_date, -method, -fix_data, -fix_latch

WHAT NEXT

Complete the options for the set_autofix_element command.

SEE ALSO

set_autofix_element reset_autofix_element

TESTXG-39 (Error) No autofix element configuration exists for the type %s.

DESCRIPTION

This message indicates that a reset_autofix_element command has been issued, but no autofix element configuration has been set for the type.

WHAT NEXT

Remove the reset_autofix_element command.

SEE ALSO

set_autofix_element reset_autofix_element

TESTXG-40 (Error) The pin %s cannot be found in the design %s.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but a pin in the list of pins does not exist in the design.

WHAT NEXT

Check the name of the pin and set the correct pin name OR Remove the pin from the list of the set_test_point_element command.

SEE ALSO

set_test_point_element remove_test_point_element

TESTXG-41 (Error) The type %s is not a valid type for the set_test_point_element command.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but the type is not a valid type for the command.

WHAT NEXT

Check the valid types in the manpage of the set_test_point_element, modify the type and re-issue the command.

SEE ALSO

set_test_point_element remove_test_point_element

TESTXG-42 (Warning) The -scan_test_point_enable option is ignored for the type %s.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but the -scan_test_point_enable option is not an option that can be specified for the type and the option is ignored. The -scan_test_point_enable option is a valid option for the control types.

WHAT NEXT

Remove the -scan_test_point_enable option.

SEE ALSO

set_test_point_element remove_test_point_element

TESTXG-43 (Warning) The -test_point_enable option is ignored for the type %s.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but the -test_point_enable option is not an option that can be specified for the type and the option is ignored. The -test_point_enable option is a valid option for the control types.

WHAT NEXT

Remove the -test_point_enable option.

SEE ALSO

set_test_point_element remove_test_point_element

TESTXG-44 (Warning) The -test_points_per_test_point_enable option is ignored for the type %s.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but the -test_points_per_test_point_enable option is not an option that can be specified for the type and the option is ignored. The -test_points_per_test_point_enable option is a valid option for the control types.

WHAT NEXT

Remove the -test_points_per_test_point_enable option.

SEE ALSO

set_test_point_element remove_test_point_element

TESTXG-45 (Error) A set_test_point_element command has already been specified for the pin %s and for the type %s.

DESCRIPTION

The pin has already been specified to be a candidate for a test point of this type. Two test points of the same type cannot be inserted on the same pin location.

WHAT NEXT

Remove the pin from the list OR Remove the previous test point element specification for this pin and this type with the remove_test_point_element command.

SEE ALSO

set_test_point_element remove_test_point_element

TESTXG-46 (Error) The parameter for the %s option has to be enable or disable.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but the parameter for the option is not a valid one. The valid parameters are enable or disable.

WHAT NEXT

Change the parameter for the option and re-issue the command.

SEE ALSO

set_test_point_element remove_test_point_element

TESTXG-47 (Error) The port or the pin %s does not have the correct direction.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but

the port or the pin does not have the correct direction according to the option in which the port or the pin has been specified.

WHAT NEXT

Specify another port or another pin with the correct direction and re-issue the command.

SEE ALSO

set_test_point_element remove_test_point_element

TESTXG-48 (Warning)The port or the pin %s is already connected, it cannot be used to observe data.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued for the type observe, but the port or the pin specified for the -source_or_sink option is already connected. As a consequence, the port or the pin cannot be used to observe data. DFT Compiler will either insert an observe register or create a new output port depending of the scan_source_or_sink value. By default, data are observed through an observe scan register.

WHAT NEXT

Specify another port or another pin that could be used to observe data and re-issue the command OR Let DFT Compiler insert a new observe scan register or create a new output port.

SEE ALSO

set_test_point_element remove_test_point_element

TESTXG-49 (Error) The pin %s does not have the correct direction for a test point location.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but a pin from the list does not have the correct direction. A test point location has to be an output pin.

WHAT NEXT

Specify another pin with the correct direction for the test point location and re-issue the command.

SEE ALSO

set_test_point_element remove_test_point_element

TESTXG-51 (Error) The output port %s cannot be specified for a test point location.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but an ouput port cannot be the location of a test point. A test point location has to be an input port or an output internal pin.

WHAT NEXT

Specify an input port or an internal output pin and re-issue the command.

SEE ALSO

set_test_point_element remove_test_point_element

TESTXG-52 (Error) The clock type %s is not a valid clock type for the testability configuration.

DESCRIPTION

This message indicates that a set_testability_configuration command has been issued, but the specified clock type is not a valid one for the testability configuration. The valid clock types are dominant or dedicated.

WHAT NEXT

Specify a valid clock type and re-issue the set_testability_configuration command.

SEE ALSO

set_testability_configuration reset_testability_configuration

report_testability_configuration

TESTXG-53 (Warning) Protocol generated after insertion in Internal Pins Flow is not accurate and can not be used.

DESCRIPTION

The Ctl model and the protocol available after insertion in the internal pins flow are not complete. They cannot be directly used by any other tool.

However, they are used internaly by DFTCompiler for running post dft drc for basic scan flows if the internal pins flow is enabled. Post dft drc cannot be run when multi mode and scan compression are enabled with the internal pins flow.

WHAT NEXT

If the design has no internal pins, please disable the internal pins flow by using the **set_dft_drc_configuration** command.

SEE ALSO

set_dft_drc_configuration set_dft_signal

TESTXG-54 (Error) DFT insertion in DC-Topographical flow is only supported for basic scan and adaptive scan flows.

DESCRIPTION

You get this error message becuase you are trying to use a DFT client that is not supported in the DC Topographical flow. The DFT clients that are valid are basic scan and adaptive scan. Following are the unsupported clients:

1. PLL 2. User defined test points 3. Logic BIST 4. Memory BIST 5. Core Wrapping 6. SOC 7. Boundary scan

WHAT NEXT

Please disable the unsupported client using the **set_dft_configuration** or the **remove_test_point_element** command.

SEE ALSO

set_dft_configuration set_scan_configuration remove_test_point_element

TESTXG-55 (Error) Scan configuration option -%s is not valid for DC-Topographical flow.

DESCRIPTION

You get this error message becuase you are trying to use the scan configuration option that is not supported for the DFT insertion in DC-Topological flow. The options that are not supported are:

1. minimize_hold_time_violations

WHAT NEXT

Please remove the unsupported option from the command **set_scan_configuration** and rerun the script.

SEE ALSO

set_dft_configuration set_scan_configuration remove_test_point_element

TESTXG-56 (warning) The multi-clock protocol requires that the strobe time be before a clock’s pulse if it is used for transition fault testing.

DESCRIPTION

You received this message because you are trying to strobe after the clock puslse. If you are performing transition fault testing then the multi-clock protocol requires that you strobe before the clock pulse for optimal results.

WHAT NEXT

If you wish to create a multi-clock protocol for transition fault testing set the variable test_default_strobe to a value less than the pulse of the clock(s). If you do not wish to create a multi-clock protocol then do not specify the option -capture_procedure with create_test_protocol.

SEE ALSO

create_test_protocol (2)

TESTXG-57 (warning) Scan compression xmasking requires that the strobe time be before a clock's pulse.

DESCRIPTION

You received this message because you are trying to strobe after the clock puslse. However, the scan compression xmasking requires that you strobe before the clock pulse for optimal results.

WHAT NEXT

If you wish to perform scan compression with xmasking set the variable test_default_strobe to a value less than the pulse of the clock(s). If you do not wish to perform xmasking with scan compression set xmask to false in set_scan_compression_configuration.

SEE ALSO

set_scan_compression_configuration (2)

TESTXG-58 (Warning) insert_dft does not perform synthesis optimization in DC-Topographical mode. Run incremental compile to reoptimize the design after insert_dft.

DESCRIPTION

You received this warning message because you are trying to use synthesis optimizations during insert_dft command with the DC-Topographical flow, which is not supported.

WHAT NEXT

The tool had turned off all synthesis optimizations. Please remove the unsupported option from the command **set_dft_insertion_configuration** and rerun the script. And please run incremental compile to reoptimize the design once insert_dft completes.

SEE ALSO

set_dft_insertion_configuration

TESTXG-59 (error) The transition fault protocol does not

support on chip clocking.

DESCRIPTION

You received this message because you are trying to use on chip clocking, and a transition fault protocol. However, the transition fault protocol created by DFT Compiler does not support on chip clocking.

WHAT NEXT

If you wish to create a transition fault protocol disable on chip clocking and then re-create the protocol. If you do not want to create a transition fault protocol then issue the create_test_protocol command without the -transition option.

SEE ALSO

set_dft_configuration (2)

TESTXG-60 (Warning) Tetramax '%s' option for dft_drc command is being overwritten.

DESCRIPTION

When **set_dft_drc_configuration** command is used to pass an option to Tetramax for dft_drc, this message indicates that an earlier specification is being overwritten.

For a single command if multiple options are to be passed to Tetramax DRC Engine then they must be separated by pipe "|"

Example: User wants to pass following 3 options to Tetramax "set drc" command.

```
set_drc -nodelete_unused_gates -merge equivalent_dlat_dff

set drc -pipeline -clock 12clk

set drc -oscillation 20 -store_setup
```

In DFT script user must write:

```
set_dft_drc_configuration -tmax_set_drc "-nodelete_unused_gates -merge
equivalent_dlat_dff | -pipeline -clock 12clk | -oscillation 20 -store_setup"
```

If user issues commands:

```
set_dft_drc_configuration -tmax_set_drc "-nodelete_unused_gates -merge
equivalent_dlat_dff "
```

```
set_dft_drc_configuration -tmax_set_drc "-pipeline -clock 12clk "

set_dft_drc_configuration -tmax_set_drc "-oscillation 20 -store_setup"

then TESTXG-60 will be issued after 2nd and 3rd commands.
```

WHAT NEXT

```
Check the script for any conflicts. If multiple directives are to be passed tp
Tetramax DRC engine then above described methodology must be followed.
```

SEE ALSO

```
set_dft_drc_configuration
```

TESTXG-61 (Error) In LSSD scan style Observe and Control test points are not supported.

DESCRIPTION

This message indicates that **set_dft_configuration** or **set_test_point_element** command has been issued to insert observe and/or control test points with LSSD scan style. Observe and Control test points are not supported with LSSD scan style.

WHAT NEXT

Remove Observe and Control test point specification when LSSD scan style is used.

SEE ALSO

set_dft_configuration

set_test_point_element

TESTXG-62 (Warning) The scan compression mode %s is exactly the same as %s.

DESCRIPTION

The two scan compression modes reported in the message have the same specifications and would lead to the creation of duplicate scan compression modes. This will cause more area overhead and routing congestion with no additional benefits in compression or pin count. Please remove one of the compression modes or change the

specifications.

WHAT NEXT

Please modify the scan compression specification using the **set_scan_compression_configuration** command.

SEE ALSO

set_dft_configuration set_scan_configuration set_scan_compression_configuration

TESTXG-63 (Information) Autofix cannot jump clock gating cell %s.

DESCRIPTION

This message indicates that autofix was unable to jump reported clock gating cell during test point optimization. Either the clock pin, net of clock pin or driver pin of this net are not accessible.

WHAT NEXT

Check the reported clock gating cell.

SEE ALSO

TESTXG-64 (Error) Scan path specification with pipeline registers is missing associated scan ports

DESCRIPTION

This message indicates that a set_scan_path command has been issued to specify pipeline registers for a scan chain, but the associated scan ports have not been specified. This is an incomplete specification.

WHAT NEXT

Specify the scan-in and scan-out ports associated with the corresponding pipeline registers.

SEE ALSO

set_dft_signal remove_dft_signal remove_scan_path

TESTXG-65 (warning) Specification for -synchronize_chains will be ignored, as %s is enabled.

DESCRIPTION

This warning message occurs when you specify a value using the **set_scan_compression_configuration -synchronize_chains** command to synchronize internal chains of the compression mode. The specification is ignored, as either pipelining or terminal lockup insertion is enabled.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, disable terminal lockup insertion or pipelining to honor the **-synchronize_chains** specification.

SEE ALSO

reset_scan_compression_configuration(2)
reset_scan_configuration(2)
set_scan_compression_configuration(2)
set_scan_configuration(2)

TESTXG-66 (information) Synchronizing %s of chains in %s.

DESCRIPTION

This information message occurs when you specify a non-default value for the **set_scan_compression_configuration -synchronize_chains** command. The tool inserts lockup latches at the head and/or tail of internal compression chains to operate on the same clock edge, as per the specification. This message indicates that the <head/tail> of internal compression chains in <mode_name> are synchronized.

WHAT NEXT

This is only an information message. No action is required.

However, you can disable or selectively synchronize the head or tail of compression chains using the options in **set_scan_compression_configuration -synchronize_chains**.

SEE ALSO

set_scan_compression_configuration(2)

TESTXG-67 (Information) Synchronization not needed for chains.

DESCRIPTION

This message indicates that the user has specified a value using set_scan_compression_configuration -synchronize_chains to synchronize head/tail of internal compression chains. However, sychronization is not needed as the head/tail of internal chains operate at the same clock edge. Hence, no lockup latches are inserted for synchronization in this mode.

WHAT NEXT

SEE ALSO

set_scan_compression_configuration

TESTXG-68 (error) Test model for core %s has internal pins and cannot be used for hierarchical integration.

DESCRIPTION

This error message occurs when a core that is being used for integration has internal pins specified in the corresponding core test model. Cores with internal pins cannot be integrated at the top level.

WHAT NEXT

Remove the specific core from the top level for integration or generate the test model for the core with internal pins turned off.

SEE ALSO

set_dft_drc_configuration(2)
use_test_model(2)

TESTXG-69 (error) Timing specifications are outside of the

default period %f ns.

DESCRIPTION

This error message occurs when the rise and/or fall timing values are not within the default period value.

WHAT NEXT

Specify the rise and fall time with values less than the default period value and rerun the command.

SEE ALSO

ui_set_dft_signal

TESTXG-70 (Warning) aux_clock_lssd scan style is not supported and will be obsoleted in next release.

DESCRIPTION

aux_clock_lssd scan style is not supported and will be removed in next release.

WHAT NEXT

Change the scan style.

SEE ALSO

TESTXG-71 (error) Clock signal not defined with set_dft_signal command.

DESCRIPTION

This error message occurs when a clock signal is specified in the set_scan_path command without a previous definition of this signal with the set_dft_signal command.

WHAT NEXT

Please Define/infer the clock signal with the set_dft_signal command and rerun the

set_scan_path command.

SEE ALSO

ui_set_dft_signal

TESTXG-72 (error) Top ATE clock not specified.

DESCRIPTION

This error message occurs when no clock signal is specified at the top level.

WHAT NEXT

Please specify the top ATE clock signal with the set_dft_signal command.

SEE ALSO

ui_set_dft_signal

TESTXG-73 (error) Accessp pin %s is located under the hierarchy of the internal clock pin %s.

DESCRIPTION

This error message occurs when the hierachy of a given access pin is inside the hierarchy of a given internal clock pin.

WHAT NEXT

Specify another internal clock pin positioned at a level of hierarchy that doesn’t include the level of hierarchy of the access pin.

TESTXG-74 (Warning) Scan chain terminals optimization for clock domain %s is not performed on the complete user chain

%s.

DESCRIPTION

Optimization is not performed on complete user chains.

WHAT NEXT

SEE ALSO

TESTXG-75 (Warning) Scan chain terminals optimization requires the clock mixing scheme to be set to "mix_edges".

DESCRIPTION

Scan chain terminals optimization requires mixed edges.

WHAT NEXT

Use **set_scan_configuration -clock_mixing mix_edges** command.

SEE ALSO

set_scan_configuration

TESTXG-76 (Warning) Scan chain terminals optimization not performed when scan compression is enabled.

DESCRIPTION

Scan chain terminals optimization not performed when scan compression is enabled.

WHAT NEXT

Disable scan compression with **set_dft_configuration -scan_compression disable** command.

SEE ALSO

set_dft_configuration

TESTXG-77 (Warning) Scan chain terminals optimization for clock domain %s is not performed when chains of length less or equal to 2 exist.

DESCRIPTION

Scan chain terminals optimization not performed when chains of length less or equal to 2 exist

WHAT NEXT

SEE ALSO

TESTXG-78 (Warning) Scan chain terminals optimization for clock domain %s is not performed when core segments are present.

DESCRIPTION

Scan chain terminals optimization not performed when core segments are present.

WHAT NEXT

SEE ALSO

TESTXG-79 (Warning) Scan chain terminals optimization for clock domain %s not performed because of insuficient positive segments.

DESCRIPTION

Insuficient positive segments for the optimization. Note that the optimization needs

at least two positive segments per negative scan chain.

WHAT NEXT

SEE ALSO

TESTXG-80 (Warning) Optimization not performed on the non complete user chain %s in clock domain %s, too much user included negative segments.

DESCRIPTION

Optimization is not performed on non complete user chains where the number of included negative segments are great than chain_length - 2.

WHAT NEXT

SEE ALSO

TESTXG-81 (Warning) optimization not performed on the non complete user chain %s in clock domain %s because of invalid configuration of head segments.

DESCRIPTION

Optimization is not performed on non complete user chains when the head segments are specified as: --, -+, +-+, -+-. Correct configurations for head segments are: ++, +- .

WHAT NEXT

SEE ALSO

TESTXG-82 (Warning) optimization not performed on the non complete user chain %s in clock domain %s because of invalid

configuration of tail segments.

DESCRIPTION

Optimization is not performed on non complete user chains when the tail segments are specified as: --, +-, +-+, -+-. Correct configurations for tail segments are: ++, -+.

WHAT NEXT

SEE ALSO

TESTXG-83 (Warning) optimization not performed on the non complete user chain %s in clock domain %s because of invalid configuration of ordered segments.

DESCRIPTION

Optimization is not performed on non complete user chains when the ordered segments are specified as: +-+, -+-. Correct configurations for ordered segments are: ++, --, +-, -+.

WHAT NEXT

SEE ALSO

TESTXG-84 (Warning) optimization not performed on the non complete user chain %s in clock domain %s because ordered segments not coherent with head segments.

DESCRIPTION

Optimization is not performed on non complete user chains when the ordered/head segments are under the following configurations: +-/+- Correct configurations for ordered/head segments are: ++/++, ++/+-, -+/+-, --/+-

WHAT NEXT

SEE ALSO

TESTXG-85 (Warning) optimization not performed on the non complete user chain %s in clock domain %s because ordered segments not coherent with tail segments.

DESCRIPTION

```
Optimization is not performed on non complete user chains when the ordered/tail
segments are under the following configurations: -+/-+ Correct configurations for
ordered/head segments are: ++/++, ++/-+, +-/-+, --/-+
```

WHAT NEXT

SEE ALSO

TESTXG-86 (Warning) Optimization not performed will not be performed because no falling edge segments for clock domain %s.

DESCRIPTION

```
Optimization will not be performed if no negative segments.
```

WHAT NEXT

SEE ALSO

TESTXG-87 (Error) Optimization not performed will not be performed because no positive edge segments of size 1 for

clock domain %s.

DESCRIPTION

Optimization will not be performed if no positive segments of size 1.

WHAT NEXT

SEE ALSO

TESTXG-88 (error) Wrong specification for associated clock in set_dft_signal command.

DESCRIPTION

This error message occurs because of two possible reasons: wrong type for the associated clock or wrong name specified for the associated clock pin/port (inexistent in the design).

WHAT NEXT

Please specify the name (string) of a valid pin/port in the design.

SEE ALSO

ui_set_dft_signal

TESTXG-89 (error) Clock pin output has no load in the design.

DESCRIPTION

This error message occurs because the clock pin has no load in the design.

WHAT NEXT

Please specify clock output pin having at least one load in the design.

SEE ALSO

ui_set_dft_signal

TESTXG-90 (error) Clock pin has a wrong direction.

DESCRIPTION

This error message occurs because the specified clock pin has an input direction in the design.

WHAT NEXT

Please specify clock pin having an output direction in the design.

SEE ALSO

ui_set_dft_signal

TESTXG-91 (Warning) The changes to design %s make the existing attached test-model invalid. So the test-model for the design %s will be removed and no longer be used.

DESCRIPTION

This error message occurs because the interface for the block has been modified making the attached model no longer valid.

WHAT NEXT

Do not modify the interface once the model for the block is frozen. Please plan to make any interface changes at the block level insertion flow itself.

SEE ALSO

insert_dft

TIM-001 (Error) There are no arcs from pin '%s' to pin '%s' on cell '%s'.

DESCRIPTION

No timing arcs exist between these pins of the cell. Therefore, we cannot time between them. We will either report no paths or for unmapped logic, assume 0.

WHAT NEXT

Fix the library to create the proper timing arcs.

TIM-002 (information) Timing loop detected.

DESCRIPTION

The design contains at least one timing loop. This message is followed by a list of pins on one loop, and then messages indicating which timing arcs are being automatically disabled to break the loop.

WHAT NEXT

To view all timing loops in your design, use **report_timing -loops**. To manually break loops, use **disable_timing**.

TIM-003 (warning) Disabling timing arc between pins '%s' and '%s' on cell '%s'%s

DESCRIPTION

This message is displayed when timing arcs are disabled by tool to break combinational feedback loops. It is not displayed for arcs that are manually disabled with the **set_disable_timing** command.

WHAT NEXT

If you want to manually break a timing loop, examine the design to see why there is combinational feedback and then choose a different point at which to break the loop.

To do this, use the **set_disable_timing** command instead of letting the tool automatically break the loop.

EXAMPLE MESSAGE

Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'u10'to break a timing loop (TIM-003)

TIM-004 (error) The pin '%s' which is a derived clock pin is either in a loop or is in the fanout of two clock sources

DESCRIPTION

The derived clock pin is either in a loop or is in the fanout of two clock sources. You cannot have loops in the clock network or can you have a derived clock in the fanout of two clock sources.

WHAT NEXT

If it is a loop, break the loop. If the derived clock is in the fanout of two clock sources, try to isolate it or use internal clocks.

TIM-005 (information) Invalidating all auto-disabled timing arcs.

DESCRIPTION

Some arcs have been enabled, forcing the tool to do loop detection from scratch. Therefore, the tool enables all auto-disabled arcs.

WHAT NEXT

To view all timing loops in your design, use **check_timing -loops**. To manually break the loops, use **disable_timing**.

TIM-006 (error) report_delay_calculation is not enabled for library '%s'.

DESCRIPTION

The delay calculation report shows detailed performance information about library

cells. By default, cell delay reporting is disabled. The technology library vendor can enable delay calculation for a library by specifying the following in the **.lib** source:

```
library_features(report_delay_calculation);
```

WHAT NEXT

Contact your library vendor to request a library with this feature enabled.

TIM-007 (error) The master clock %s has %d edges in a period. Cannot do frequency multiplication.

DESCRIPTION

If the master clock of a generated clock has more than 3 edges in a period, you cannot generate a frequency multiplied clock from that master clock.

WHAT NEXT

You can use -edges option to generate the clock.

TIM-008 (error) The generated clock '%s' is in the fanout of clock source %s.

DESCRIPTION

A generated clock can only be in the fanout of a clock source from which it is generated. Here the generated clock is found to be in the fanout of some other clock source.

WHAT NEXT

Generate this clock from a clock in whose fanout it is in.

TIM-009 (error) Generated clock '%s' is not in the fanout of its

master clock.

DESCRIPTION

The generated clock is not in the fanout of the master clock with respect to which it has been defined. A generated clock must be in the fanout of its master clock.

WHAT NEXT

Please check the design and redefine the generated clock to be in the fanout of its master clock.

TIM-010 (warning) The generated clock '%s' has not been expanded,
please create its master clock.

DESCRIPTION

A generated clock will not expand if the master clock from which it is generated has not been created.

WHAT NEXT

Please create the master of the generated clock.

TIM-011 (error) The following generated clocks '%s' form a loop.

DESCRIPTION

The generated clock listed are defined in a loop. A loop of generated clocks is formed in that there is a circular dependency of generated clock to master clock.

For example, if A and B are generated clocks, and A is generated from B, and B is generated from A, there is a circular dependency.

WHAT NEXT

Remove cirular dependency in the generated clock sources.

TIM-012 (error) The master of the generated clock '%s' is not

connected to any clock source.

DESCRIPTION

The master clock of a generated clock must be either a clock source, or must be connected to a clock source. If it is neither, it is an error.

WHAT NEXT

Make sure that the master source from which the clock is generated is a clock source or is connected to a clock source.

TIM-013 (information) Found %d generated clock master pins that are not connected to clock sources.

DESCRIPTION

It gives a summary of the number of generated clock master pins that are not connected to clock sources.

WHAT NEXT

For a more detailed description of which generated clock master pins are not connected to any source, do check_timing -with -verbose option.

TIM-014 (information) Found %d loops in the generated clock network.

DESCRIPTION

This message gives a summary of the number of loops in the generated clock network. If there is a circular dependency of generated clock sources and its master, there will be a loop in the generated clock network.

WHAT NEXT

To get a more detailed description of where the generated clock loops are, use check_timing -verbose.

TIM-015 (Error) The -edges spec of generated clock '%s' has

edge number
 less than 1, the edge number should be from 1 up.

DESCRIPTION

The -edge specification in creat_generated_clock command should use edge number of the master clock which should be from 1 up. Zero or negative number are not allowed.

WHAT NEXT

Change your -edge spec in create_generated_clock coommand.

TIM-016 (Error) In the -edge specification of create_generated_clock
 '%s', the edge numbers must be in increasing order.

DESCRIPTION

In the -edge specification of a create_generated_clock command, the edge numbers specified must be in increasing order.

WHAT NEXT

Check the -edge spec in create_generated_clock command and edge numbers increasing.

TIM-017 (warning) The master source of the generated clock '%s' is not known. Ignoring generated clock '%s'.

DESCRIPTION

You receive this warning because you did not specify the master clock source of the named generated clock. The master clock of a generated clock must be a specified clock source or be connected to a clock source. Otherwise, this error occurs.

WHAT NEXT

Make sure that the master source from which the clock is generated is a clock source or is connected to a clock source. See the man page for the **create_generated_clock** command.

SEE ALSO

create_generated_clock (2).

TIM-018 (warning) The source of the generated clock '%s' is not known. Ignoring generated_clock '%s'.

DESCRIPTION

You receive this warning because you did not specify the source of a generated clock. The source of a generated clock can be a list of ports or pins.

WHAT NEXT

Make sure that the generated clock has a source object. See the man page for the **create_generated_clock** command.

SEE ALSO

create_generated_clock (2).

TIM-019 (warning) Ignoring incorrectly specified library generated_clock '%s' in library cell '%s/%s'.

DESCRIPTION

You receive this warning because the library generated clock description does not have complete specification for creating the derived waveform. A generated_clock must have a 'master_pin', source 'clock_pin', and specification for 'divide_by' or 'multiply_by' or 'edge_spec'.

WHAT NEXT

Fix the description in the library to completely specify the generated_clock.

SEE ALSO

create_generated_clock (2).

TIM-020 (Error) '%s' is not a legal value for '%s'. The value

defaults to ’%s’.

DESCRIPTION

You have specified an invalid value for the variable. Therefore, the default value described will be used.

WHAT NEXT

If you do not want the default value, please specify a valid value for this variable.

TIM-021 (warning) The generated clock ’%s’ is being removed because the pin ’%s’ has been deleted and the clock no longer has a %s.

DESCRIPTION

Generated clocks require a master_pin and at least one clock source. If either of these is deleted, then the generated clock is deleted as well.

WHAT NEXT

Create a new generated clock with the same name using remaining pins.

SEE ALSO

create_generated_clock (2) **remove_cell** (2).

TIM-024 (information) Using CCS timing libraries.

DESCRIPTION

This message is produced if any libraries containing CCS timing information are used. It is only produced once per session when the first ccs timing library is read.

WHAT NEXT

No action is needed. This information may be helpful when determings whether a library contains ccs timing data.

TIM-025 (information) Using CCS timing info.

DESCRIPTION

This message is produced if any CCS delay information is used. It is only produced once per session when the first cell with CCS timing is loaded for delay calculation.

WHAT NEXT

No action is needed. This information may be helpful when examining delay correlation issues.

TIM-052 (warning) A non-unate path in clock network for clock '%s' from pin '%s' is detected.

DESCRIPTION

The clock tree for the specified clock contains non-unate paths. Clock networks normally do not contain cells such as exclusive-OR gates which have non-unate behavior. This implies that both inverting and noninverting clock waveforms reach the specified pin. The sense that is propagated from this pin is non-deterministic.

WHAT NEXT

Since there is ambiguity on which sense to choose to propagate, the tool picks one arbitrarily to propagate. If this is not acceptable, create a clock using the output of the non-unate gate as a source.

TIM-98 (Error) Minimum version must be a different library.

DESCRIPTION

The **set_min_library** command was used to set the minimum version of a library to be the same as the maximum version. This is not allowed.

WHAT NEXT

Enter the correct name of the minimum library, or use the '-none' option to revert to using the same library for both minimum and maximum analysis.

TIM-099 (Information) There are %d clock pins driven by multiple clocks, and some of them are driven by up-to %d clocks.

DESCRIPTION

timing_enable_multiple_clocks_per_reg is TRUE, and all clocks reaching the register are cost-ed simultaneously. Concurrent analysis of multiple clocks can result in significant runtime increase due to increased timing complexity. To improve runtime, the interactions between multiple clocks should be analyzed and **set_false_path** be used to remove invalid interactions between mutually exclusive clocks or use **set_clock_groups** to specify logically exclusive clocks.

WHAT NEXT

Analyze interaction between clock domains due to multiple clocks per register and use **set_false_path** or **set_clock_groups** to improve runtime. If concurrent analysis of multiple clocks per register is not required then set **timing_enable_multiple_clocks_per_reg** to FALSE or use **set_case_analysis** or **set_disable_timing** to select the clocks for driving the register.

TIM-100 (error) Unable to obtain a DC-Expert license.

DESCRIPTION

Timing commands such as **report_timing** or **highlight_path** require that a DC-Expert key, other appropriate technology key, or both be checked out.

WHAT NEXT

To determine who is using the DC-Expert, use the **license_users** command. Should problems occur with the license server, contact your system administrator.

TIM-101 (error) The '%s' command is not supported in dt_shell.

DESCRIPTION

This error occurs when a valid Design Compiler command is used, but the command is not supported in **dt_shell**, the timing analysis user interface. Commands such as **compile** are supported only in **dc_shell**, and are ignored in **dt_shell**.

WHAT NEXT

If you need to use the command, use the **dc_shell** program instead of **dt_shell**.

TIM-102 (Error) Ultra license is required for true path reporting.

DESCRIPTION

The **-justify** and **-true** options of **report_timing** require an Ultra license.

WHAT NEXT

TIM-103 (Warning) Reference %s contains internal pins with clock attribute.

DESCRIPTION

The reference contains internal/generated clocks on some internal pins which are not accessible to user to create clocks.

WHAT NEXT

~

TIM-104 (Warning) Worst timing paths might not be returned.

DESCRIPTION

Design Compiler static timing verifier is optimized for finding the longest paths (max delay) and the shortest paths (min delay) in the design. The timing verifier cannot always efficiently compute the longest path in the design, which is shorter than a given amount or the shortest path in the design, which is longer than a given amount. This warning indicates that the current **report_timing** command has made such a request that cannot be satisifed efficiently.

In this case, **report_timing** uses the -nworst option to limit its search for paths meeting the -greater or -lesser criteria. There is no guarantee that the paths returned will be the worst ones in the design that meet the criteria specified in the **report_timing** command. In fact, it is possible that no paths will be returned even though a path meeting the report_timing criteria does exist in the design.

WHAT NEXT

Increasing the number of paths to return using the -nworst option of **report_timing** increases the likelihood that the worst paths will be found. However, increasing this value also increases the memory and runtime needed by **report_timing**.

TIM-105 (Information) Converting time units for library '%s' since those in library '%s' differ.

DESCRIPTION

The time units specified in the first library differ from those in the second library. The second library is Design Compiler's "main" library and determines DC's default time units. DC reports use these units and all time values annotated on the design (using **create_clock**, **set_input_delay**, and so on.) are assumed to be in these units.

The informational message notifies you that Design Compiler is handling conversion of units so that delay calculation using cells in the first library use time values in its native units.

Design Compiler's "main" library is determined as follows: During reporting the main library is the first library in the link path that contains a cell that is used in the design. During optimization the main library is the first target library specified.

WHAT NEXT

To see the units that are specified for a library, use the **report_lib** command.

TIM-106 (Information) Converting capacitance units for library '%s' since those in library '%s' differ.

DESCRIPTION

The capacitance units specified in the first library differ from those in the second library. The second library is Design Compiler's "main" library and determines DC's default capacitance units. DC reports will use these units and all capacitance values annotated on the design (using **set_load**) are assumed to be in these units.

The informational message notifies you that Design Compiler is handling conversion of units so that delay calculation using cells in the first library will use capacitance values in its native units.

Design Compiler's "main" library is determined as follows: During reporting the main library is the first library in the link path that contains a cell that is used in the design. During optimization the main library is the first target library specified.

WHAT NEXT

To see the units that are specified for a library, use the **report_lib** command.

TIM-107 (Warning) Main library '%s' has no time units specified, but library '%s' does.

DESCRIPTION

Time units were not specified in the first (main) library, but time units were specified in the second library.

Design Compiler uses the main library to determine the default time units. The default time units are used in reports and all time values annotated on the design (using **create_clock**, **set_input_delay**, and so on.) are assumed to be in these units. However, this main library has no time units and as a result DC runs in a "unitless" mode. No time unit conversion is performed. This can result in incorrect analysis if different time units are actually required.

DC's main library is determined as follows: During reporting the main library is the first library in the link path that contains a cell that is used in the design. During optimization the main library is the first target library specified.

WHAT NEXT

To see the units that are specified for a library, use the **report_lib** command.

To change the main library to a different one with units specified, remove the local_link_library attribute on the current design if one is present and put the desired library first in the link_library or link_path variables.

To add units to a unitless library, the library source (.lib) must be modified and the library must be read in using **read_lib**.

TIM-108 (Warning) Main library '%s' has no capacitance units specified, but library '%s' does.

DESCRIPTION

Capacitance units were not specified in the first (main) library, but capacitance units were specified in the second library.

Design Compiler uses the main library to determine the default capacitance units. The default capacitance units are used in reports and all capacitance values annotated on the design (using **set_load**) are assumed to be in these units. However this main library has no capacitance units and as a result DC runs in a "unitless" mode. No capacitance unit conversion is performed. This can result in incorrect analysis if different capacitance units are actually required.

DC's main library is determined as follows: During reporting the main library is the first library in the link path that contains a cell that is used in the design.

During optimization the main library is the first target library specified.

WHAT NEXT

To see the units that are specified for a library, use the **report_lib** command.

To change the main library to a different one with units specified, remove the local_link_library attribute on the current design if one is present and put the desired library first in the link_library or link_path variables.

To add units to a unitless library, the library source (.lib) must be modified and the library must be read in using **read_lib**.

TIM-109 (Warning) Cell '%s' cannot be optimized because it has conflicting timing exceptions on pins '%s' and '%s'.

DESCRIPTION

The identified cell has multiple input pins with conflicting point-to-point timing exceptions on them. During optimization this cell is dont_touch'ed to prevent the point-to-point exceptions from being lost if the cell gets remapped to a configuration with fewer input pins. An example of such an optimization is pulling a multiplexer out of a mux'ed flip-flop. In this case, conflicts in timing exceptions could not be accurately resolved in the new, single input configuration.

Commands which create timing exceptions are **set_max_delay**, **set_min_delay**, **set_false_path**, **set_multicycle_path**, and **group_path**.

WHAT NEXT

To allow optimization to be performed on this cell, set timing exceptions on the cell such that both of the indicated pins have matching timing constraints. To analyze the timing exceptions that currently exist on the design, use the commands **report_timing_requirements** and **report_path_group**.

TIM-110 (Warning) Cell '%s' is being dont_touch'ed because of timing constraints on pin '%s'.

DESCRIPTION

The identified cell has timing constraints which cannot always be transferred to another cell during optimization. As a result, the cell is dont_touched to prevent it from being replaced and to prevent the timing constraints from being lost.

WHAT NEXT

To view the timing constraints set on the pin, use **report_timing_requirements**. If the cell is sequential, verify that the library cell has the correct timing arcs.

TIM-111 (warning) Clock port '%s' is assigned input delay relative to clock '%s'.

DESCRIPTION

This issue will be issued when setting an input delay on clock port, and it is not specified relative to the same clock.

WHAT NEXT

Remove the unneeded input delay value using the **remove_input_delay** command.

SEE ALSO

remove_input_delay(2)

TIM-112 (Information) Input delay ('%s') on clock port '%s' will be added to the clock's propagated skew.

DESCRIPTION

An input delay set on a clock port is interpreted as clock tree delay between the ideal clock source and the input port.

WHAT NEXT

If you don't want to have the input delay on the clock added to the clock skew, unset the input delay using the **remove_input_delay** command.

TIM-113 (Information) set_input_delay values are added to the propagated clock skew.

DESCRIPTION

When setting input delay on a clock signal, this value is added to the clock network

delay when calculating the skew at the clock pins.

WHAT NEXT

If you don’t want to have the input delay on the clock added to the clock skew, unset the input delay using the **remove_input_delay** command.

TIM-114 (Warning) File ’%s’ could not be opened.

DESCRIPTION

You receive this warning message because the log file specified by the **case_analysis_log_file** variable could not be opened. The case analysis information will not be output to a log file.

WHAT NEXT

Specify a valid file that can be opened by the **case_analysis_log_file** variable.

SEE ALSO

report_timing (2), **set_case_analysis** (2); **case_analysis_log_file** (3).

TIM-120 (Error) Cannot find library file named ’%s’.

DESCRIPTION

The file specified cannot be found or is not readable.

WHAT NEXT

Check to make sure that the filename exists, permissions are set correctly, and the search_path variable contains the directories that should be searched.

TIM-121 (warning) The -locations option of the report_timing command is now obsolete. Use the -physical option instead.

DESCRIPTION

You receive this message if you have issued **report_timing -locations**. This message

informs you that the **-locations** option is now obsolete and has been replaced by the **-physical** option. **-locations** continues to be supported for backward compatibility.

WHAT NEXT

Unless you need to use the **-locations** option for backward compatibility, the next time you use **report_timing**, use **-physical** instead of **-locations**.

SEE ALSO

report_timing (2).

TIM-125 (error) The pin '%s', which is a generated clock pin, is either in a loop or is in the fanout of two clock sources.

DESCRIPTION

The generated clock pin is in a loop or is in the fanout of two clock sources. You cannot have loops in the clock network, or can you have a generated clock in the fanout of two clock sources.

WHAT NEXT

If it is a loop, break the loop. If the generated clock is in the fanout of two clock sources, try to isolate it or use internal clocks instead.

TIM-128 (warning) No controlling value could be found for the clock gating cell '%s' for the clock pin '%s'.

DESCRIPTION

You receive this warning message because you executed the **set_clock_gating_check** command but did not specify a controlling value for the pin of the clock gating cell driven by the clock. Normally, clock gating checks are performed for the interval where the clock does not have the controlling value. If no controlling value can be determined, no clock gating check will be performed.

WHAT NEXT

Use the **-high** or **-low** option with the **set_clock_gating_check** command to specify the noncontrolling interval for the clock pin.

set_clock_gating_check (2).

TIM-129 (warning) User specified controlling value is different.

DESCRIPTION

User defined controlling value for the clock gating cell '%s' for the clock pin '%s' conflicts with the one calculated by the tool. But the user specified value takes precedence over the calculated value.

WHAT NEXT

The clock gating check is performed for the interval of the clock pin depending on the controlling value. See the manual page for the command **set_clock_gating_check** for detailed instructions on using -high and -low options.

TIM-130 (warning) The attribute '%s' is not supported.

DESCRIPTION

You receive this message because the attribute specified in the ftiming_report_attributes variable is not supported by the **report_timing** command with the **-attributes** option. Currently, only the **dont_touch**, **dont_use**, **map_only**, **ideal_net** and **size_only** attributes are supported.

The **timing_report_attributes** variable is in the system .synopsys_dc.setup file.

WHAT NEXT

Modify the **timing_report_attributes** variable.

SEE ALSO

report_timing (2).

TIM-131 (warning) There are no specified attributes to report.

DESCRIPTION

You receive this message because you used the the **report_timing** command with the **-attributes** option; but, because there was no variable in the **timing_report_attributes** variable, no attributes are printed.

The **timing_report_attributes** variable specifies the attributes to be reported by the **report_timing** command with the **-attributes** option. Currently, only the **dont_touch**, **dont_use**, **map_only**, **ideal_net** and **size_only** attributes are supported.

The **timing_report_attributes** variable is in the system .synopsys_dc.setup file.

WHAT NEXT

Modify the **timing_report_attributes** variable.

SEE ALSO

report_timing (2).

TIM-133 (warning) Setting clock gating check on multiplexer '%s'.

DESCRIPTION

You receive this warning message because you have executed the **set_clock_gating_check** command and specified a controlling value for a clock for a multiplexer. Generally, clock gating checks ensure that the enable signal does not change during the interval when the clock input has a noncontrolling value.

A multiplexer is a cell that has no controlling value. To perform a clock gating check on a multiplexer, you must specify the noncontrolling interval for the clock. Use the **-high** and **-low** options carefully, as the tool does not perform detailed analysis to determine if the selected signal changes only in the safe intervals.

WHAT NEXT

Use the **-high** or **-low** option for performing clock gating checks carefully on cells like multiplexers after understanding when it is safe to change the selected signal. There can be situations when there is no interval when it is safe to change the selected signal. Carefully analyze the consequences before using these options on cells like multiplexers.

SEE ALSO

set_clock_gating_check (2).

TIM-134 (warning) Design '%s' contains %d high-fanout nets. A fanout number of %d will be used for delay calculations involving

these nets.

DESCRIPTION

The design contains high-fanout nets whose delays will be computed using a simplified delay model that assumes a fixed fanout number. The rationale behind this is that delays of high-fanout nets are expensive to compute, but such nets are often unconstrained (as in the case of global reset nets, scan enable nets, and so on). Those high-fanout nets that are constrained should eventually be replaced by buffer trees. In both cases, detailed delay calculations are expensive and unnecessary.

The simplified net delay model is used only when computing data delays. Propagated clock latencies are always computed using the full accuracy net delay model.

WHAT NEXT

You can control the load pin threshold for high-fanout nets using the **high_fanout_net_threshold** variable. Setting the threshold to 0 (or to a very large number) ensures that no nets will be treated as high-fanout nets. However, you should be aware that forcing fully accurate delay calculations on all nets can significantly increase compilation runtime in some cases.

The pin capacitance for high-fanout nets is computed by multiplying the capacitance specified by the **high_fanout_net_pin_capacitance** variable times the high-fanout threshold.

EXAMPLE MESSAGE

Warning: Design 'reg_top' contains 3 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)

SEE ALSO

high_fanout_net_threshold (3), **high_fanout_net_pin_capacitance** (3).

TIM-135 (Warning) Net '%s' exceeds the high-fanout threshold. Using a fanout number of %d to calculate net delay and load.

DESCRIPTION

The named net is classified as a high-fanout net because its fanout number exceeds the threshold specified by the **high_fanout_net_threshold** variable. Delays of high-fanout nets are computed using a simplified delay model that assumes a fixed fanout number. The rationale behind this is that delays of high-fanout nets are expensive to compute, but such nets are often unconstrained (as in the case of global reset nets, scan enable nets, and so on). Those high-fanout nets that are constrained

should eventually be replaced by buffer trees. In both cases, detailed delay calculations are expensive and unnecessary.

The simplified net delay model is used only when computing data delays. Propagated clock latencies are always computed using the full accuracy net delay model.

WHAT NEXT

You can control the load pin threshold for high-fanout nets using the **high_fanout_net_threshold** variable. Setting the threshold to 0 (or to a very large number) ensures that no nets will be treated as high-fanout nets. However, you should be aware that forcing fully accurate delay calculations on all nets can significantly increase compilation runtime in some cases.

The pin capacitance for high-fanout nets is computed by multiplying the capacitance specified by the **high_fanout_net_pin_capacitance** variable times the high-fanout threshold.

SEE ALSO

high_fanout_net_threshold (3), **high_fanout_net_pin_capacitance** (3).

TIM-140 (warning) Gated clock latch is not created for pin '%s' because pin has a connection to a clock.

DESCRIPTION

You receive this warning because the tool has detected that you set the **set_clock_gating_check** command on a pin that is driven by a clock. Clock-gating checks are normally performed on the enable pins of the clock-gating cell. Setting a clock-gating check on a pin driven by the clock in the clock-gating cell has no effect.

WHAT NEXT

If you are not sure which pin to set the clock-gating check on, consider setting the check on the clock-gating cell. The clock-gating cell performs clock-gating checks on all the enable pins of the cell. See the man page for the **set_clock_gating_check** command for more detailed information on this command.

set_clock_gating_check (2).

TIM-141 (warning) Gated clock latch is not created for cell '%s'

on pin '%s' in design '%s'.

DESCRIPTION

You receive this warning because the tool has detected that you set the **set_clock_gating_check** command on a pin that is either a non-input pin or is driven by a clock. Clock-gating checks should be performed on input enable pins of the clock-gating cell. Setting clock-gating check on the pins driven by the clock in the clock-gating cell has no effect. Similarly, setting clock-gating check on an output pin has no effect.

WHAT NEXT

If you are not sure which pin to set the clock gating check on, consider setting the check on the clock-gating cell, which will then perform clock-gating checks on all the enable pins of the cell. See the man page for the **set_clock_gating_check** command for detailed information on this command.

SEE ALSO

set_clock_gating_check (2).

TIM-142 (warning) No gated clock latch created for cell '%s'.

DESCRIPTION

You receive this warning because the tool has detected that you set the **set_clock_gating_check** command on a pin that is a non-input pin or is driven by a clock. Clock-gating checks should be performed on input enable pins of the clock-gating cell. Setting a clock-gating check on the pins driven by the clock in the clock-gating cell has no effect. Similarly, setting clock-gating check on an output pin has no effect.

WHAT NEXT

If you are not sure which pin to set the clock-gating check on, consider setting the check on the clock-gating cell, which will then perform clock-gating checks on all the enable pins of the cell. See the man page for the **set_clock_gating_check** command for more detailed information.

SEE ALSO

set_clock_gating_check (2).

TIM-143 (warning) Converting propagated clock at '%s' to ideal clock.

DESCRIPTION

You receive this warning to let you know that because you set the **set_clock_latency** command on a propagated clock object, that clock object will be changed to ideal.

WHAT NEXT

If you want the clock to be propagated, do *not* specify **set_clock_latency** on the propagated clock object.

TIM-144 (warning) Ideal timing is specified on the non-ideal pin '%s'.

DESCRIPTION

Ideal latency and ideal transition are ignored if they are set on a non-ideal network.

WHAT NEXT

If the user wants to use ideal latency or ideal transition on a pin object, it must marked as ideal.

TIM-149 (warning) Cannot preserve timing constraints on IO pin '%s' during ungroup.

DESCRIPTION

This warning message occurs when the **ungroup** command cannot move constraints from an IO pin that has more than one driver or more than one receiver. Timing constraints on that pin are not preserved after the ungrouping.

WHAT NEXT

This is only a warning message. No action is required.

SEE ALSO

ungroup(2)

TIM-150 (warning) Cannot preserve timing constraints on pin '%s' during ungroup.

DESCRIPTION

You receive this warning to let you know that the **ungroup** command could not find the named pin and therefore cannot move constraints to that pin.

This warning message reports the situation. The pin might not be connected.

WHAT NEXT

Verify that you set the constraint on the correct pin. Then invoke the **ungroup** command again.

SEE ALSO

ungroup (2).

TIM-151 (warning) Cannot preserve the clock at source pin '%s' during ungroup.

DESCRIPTION

This warning lets you know that a clock with a hierarchical source pin cannot be preserved because the source cannot be moved to another pin on the same net. The clock source might not be connected. Or possibly you have defined another clock on the same net.

WHAT NEXT

Check to see if the clock source is unconnected or if there is another clock defined on the same net. Make any necessary corrections, and invoke the command again.

SEE ALSO

ungroup (2).

TIM-152 (warning) Cannot preserve the generated clock source pin '%s' during ungroup.

DESCRIPTION

You receive this warning to let you know that the generated clock with a hierarchical source pin will not be preserved because it is not possible to move the source pin to another pin on the same net.

WHAT NEXT

The **ungroup** command will automatically remove the generated clock.

SEE ALSO

ungroup (2).

TIM-154 (warning) Generated clock '%s' will be lost after ungroup.

DESCRIPTION

You receive this warning to let you know that the tool is not preserving a generated clock with a hierarchical master pin or hierarchical source pin, because it is not possible to move the source pin or the master pin to another pin on the same net.

WHAT NEXT

The **ungroup** command will automatically remove the generated clock.

SEE ALSO

ungroup (2).

TIM-155 (warning) The disable_timing constraint on pin '%s' will be lost after ungroup.

DESCRIPTION

You receive this warning to let you know that the disable_timing constraint that is

set on a hierarchical pin cannot be preserved because the **ungroup** command cannot find another pin on the same net where the constraint can be set.

WHAT NEXT

This is a warning only and requires no action on your part.

SEE ALSO

ungroup (2).

TIM-156 (warning) Case analysis on pin '%s' will be lost after ungroup.

DESCRIPTION

You receive this warning to let you know that the case-analysis value that you set on the named hierarchical pin cannot be preserved, because the **ungroup** command cannot find another pin in the same net on which to set the constraint.

WHAT NEXT

This is a warning only and requires no action on your part.

SEE ALSO

ungroup (2).

TIM-157 (warning) Generated clock '%s' will be lost after ungroup.

DESCRIPTION

You receive this warning because the named generated clock that has a hierarchical master pin or hierarchical source pin will not be preserved, because it is not possible to move either the source pin or the master pin to another pin on the same net.

WHAT NEXT

The **ungroup** command will automatically remove the generated clock.

SEE ALSO

ungroup (2).

TIM-158 (warning) Input/output delay on pin '%s' will be lost after ungroup.

DESCRIPTION

You receive this warning to let you know that the input delay or output delay that you set on a hierarchical pin will not be preserved because the **ungroup** command could not find another pin in the same net on which to set the constraint.

WHAT NEXT

This is a warning only and requires no action on your part.

SEE ALSO

ungroup (2).

TIM-159 (warning) Exception through pin '%s' is lost after ungroup.

DESCRIPTION

You receive this warning to let you know that timing exception through a hierarchical pin will not be preserved after the ungroup process because the **ungroup** command cannot find another pin in the same net on which to set the constraint.

WHAT NEXT

This is a warning only and requires no action on your part.

SEE ALSO

ungroup (2).

TIM-160 (warning) The variable named %s is set to an illegal

value (%g) and will be ignored.

DESCRIPTION

This warning message occurs when a variable is set to a value that is not within the range of acceptable values. The variable setting is ignored.

The following shows an example of the warning message.
Warning: The variable named rc_input_threshold_pct_rise is set to an illegal value (150) and will be ignored. (TIM-160)

WHAT NEXT

This is only a warning message. No action is required.

However, if you do not want the variable value to be ignored, reset the variable to an acceptable value. Refer to the man page for the variable shown in the message to determine the acceptable values. After making your changes, run the command again.

TIM-161 (warning) The variable named %s is set to a very low value (%g).

DESCRIPTION

This warning message occurs when a variable is set to a legal value that is well below the range of values that are normally used. This message warns you to check the variable’s value to make sure that it is correct.

The following shows an example of the warning message.
Warning: The variable named rc_input_threshold_pct_rise is set to a very low value (0.50). (TIM-161)

WHAT NEXT

This is a only a warning message. No action is required.

However, if the value of the variable is not the value you want, reset the variable to the correct value. Refer to the man page for the variable shown in the message to determine the range of values. After making your changes, run the command again.

TIM-162 (warning) The value of variable ’%s’ (%g) overrides the

original value (%g) in library '%s'.

DESCRIPTION

This warning message occurs when you set the named variable because you are overriding a library parameter that is specified by the creator of the library. This is not considered best practice because it can cause inaccurate or incorrect results.

Consult the creator of the library before attempting to override a library parameter.

The following shows an example of the warning message.
Warning: The value of variable 'rc_input_threshold_pct_rise' (80) overrides the original value (50) in library 'cmos_013_comb'. (TIM-162)

WHAT NEXT

This is a warning message only. If you are sure you want to override the library parameter value, no action is required.

However, to use the value defined in the library, unassign the variable and remove the variable assignment from any scripts. After completing your changes, rerun the command.

TIM-163 (warning) The library named %s specifies a very small trip-point value (%g).

DESCRIPTION

This warning message occurs when the library contains a trip-point value that is legal, but is well below the range of values that are typically used.

The following shows an example of the warning message.
Warning: The library named cmos_013_comb specifies a very small trip-point value (0.5). (TIM-163)

WHAT NEXT

This is a warning message only. No action is required.

However, it is best practice to ask the library creator to check the trip-point values in the library. You can use the **report_lib** command to see the trip-point values in the library.

SEE ALSO

report_lib(2)

TIM-164 (warning) The trip points for the library named %s differ from those in the library named %s.

DESCRIPTION

This warning message occurs when two libraries with different trip-point values are being used. This may result in a loss of timing accuracy when cells from one library are connected to cells of the other library.

The following shows an example of the warning message.
Warning: The trip points for the library named cmos_013_comb differ from those in the library named cmos_013_fflop. (TIM-164)

WHAT NEXT

This is a warning message only. No action is required.

However, you can check the trip points for a library using the **report_lib** command. It is best practice to use libraries that use the same trip-point values when cells from different libraries will be connected.

SEE ALSO

report_lib(2)

TIM-165 (warning) The library named %s contains an illegal trip-point value (%g) that will be ignored.

DESCRIPTION

This warning message occurs when a a library contains an illegal trip-point specification that is ignored.

The following shows an example of the warning message.
Warning: The library named cmos_013_comb contains an illegal trip-point value (150) that will be ignored. (TIM-165)

WHAT NEXT

This is only a warning message. No action is required.

However, you can check the trip points for a library using the **report_lib** command. Inform the library creator of the illegal trip-point value, because improper trip-point specifications may cause inaccurate timing results.

SEE ALSO

report_lib(2)

TIM-166 (error) For the library named %s, the lower %s slew trip point (%g) is larger than the upper trip point (%g). The trip points will be interchanged.

DESCRIPTION

This error message occurs when a lower slew trip point is set to a larger value than the corresponding upper trip point. This is not allowed. The upper trip point must always be larger than the lower trip point (even for falling transitions).

The following shows an example of the error message.
Error: For the library named cmos_013_comb, the lower fall slew trip point (75) is larger than the upper trip point (25). The trip points will be interchanged. (TIM-166)

WHAT NEXT

Check the trip points for the library using the **report_lib** command.

• If the incorrect values are specified in the library, inform the library creator.

• If the trip-point values are not coming from the library, they were set using variables such as **rc_slew_lower_threshold_pct_rise**. In this case, reset the variables to the correct values.

SEE ALSO

report_lib(2)
rc_slew_lower_threshold_pct_rise(3)

TIM-167 (error) For the library named %s, the lower %s slew trip point (%g) is the same as the upper trip point. The default values

of %g and %g will be used.

DESCRIPTION

This error message occurs when a lower slew trip point is set to the corresponding upper trip point of the same value. This is not allowed because it makes all transition times zero.

The following shows an example of the error message.
Error: For the library named cmos_013_comb, the lower fall slew trip point (75) is the same as the upper trip point. The default values of 20 and 80 will be used. (TIM-167)

WHAT NEXT

Check the trip points for the library using the **report_lib** command.

• If the incorrect values were specified in the library, inform the library creator.

• If the trip-point values are not coming from the library, they were set using variables such as **rc_slew_lower_threshold_pct_rise**. In this case reset the variables to the correct values.

SEE ALSO

report_lib(2)
rc_slew_lower_threshold_pct_rise(3)

TIM-168 (information) There are logic constants set for unused pins.

DESCRIPTION

This information message occurs when there are unused (hanging) pins in the design. The tool binds the unused pins to logic constants that may affect case analysis, arc disabling, and report_timing.

WHAT NEXT

This is only an information message. No action is required.

However, the tool ignores this setting if you set the **dont_bind_unused_pins_to_logic_constant** variable to true.

SEE ALSO

dont_bind_unused_pins_to_logic_constant(3)

TIM-169 (warning) Clock '%s' does not have edge values monotonically increasing, so waveform is adjusted.

DESCRIPTION

You receive this warning to let you know that the edge values of the clock is not in a monotonically increasing sequence. The reason that this is a TIM message instead of an UID message suggests that the waveform inferred from input delays could be violating the condition. In order to proceed with the analysis, the waveform edge values of the clock are adjusted.

WHAT NEXT

Clearly define the clock waveform to meet the conditions, or adjust external delays that could have led to this violation.

SEE ALSO

create_clock (2).

TIM-170 (warning) Restored the timing arcs disabled by loop breaking.

DESCRIPTION

When the timing graph is changed, the internally disabled timing arcs for loop breaking is restored.

WHAT NEXT

Exam the timing arcs to be sure they are correct for loop breaking.

SEE ALSO

set_disable_timing (2).

TIM-171 (warning) The hierarchical cell named %s that is being

ungrouped has derate. This derate will be set on the lower level leaf cells if the leaf cell does not have a derate itself. This may cause timing inconsistency before and after ungrouping.

DESCRIPTION

This warning message occurs when ungrouping a cell that has derate. The cell's derate factors are set on the lower level cells if the lower level cells do not have their own derate factors. Because the derate factor of library cells has has higher priority than hierarchical cells, this setting may cause the derate factors used in delay calculation to change after ungrouping.

WHAT NEXT

This is only a warning message. No action is required.

However, if this is not the result you intended, use the **set_timing_derate** command to change the derate factors.

SEE ALSO

set_timing_derate(2)

TIM-172 (error) For library pin %s, the lower %s slew trip point (%g) is larger than the upper trip point (%g). The trip points will be interchanged.

DESCRIPTION

This error message occurs when a lower slew trip point is set to a larger value than the corresponding upper trip point. This is not allowed. The upper trip point must be larger than the lower trip point (even for falling transitions).

The following shows an example error message:
error: For library pin clk, the lower fall slew trip point (75) is larger than the upper trip point (25). The trip points will be interchanged. (TIM-172)

WHAT NEXT

Check the trip points for the library pin. If the incorrect values are specified in the library, inform the library creator.

TIM-173 (error) For library pin %s, the lower %s slew trip point (%g) is the same as the upper trip point. The default values of %g and %g will be used.

DESCRIPTION

This error message occurs when a lower slew trip point is set to the same value corresponding upper trip point. This is not allowed, because it makes all transition times zero.

The following shows an example error message:
error: For library pin clk, the lower fall slew trip point (75) is the same as the upper trip point. The default values of 20 and 80 will be used. (TIM-173)

WHAT NEXT

Check the trip points for the library pin. If the incorrect values are specified in the library, inform the library creator.

TIM-175 (Warning) Breaking the timing path through pin '%s' due to user timing constraints.

DESCRIPTION

Some timing constraint commands can cause timing paths to be broken when placed on pins which are not normal timing startpoints or endpoints. Examples include **set_max_delay**, **set_min_delay**, **set_multicycle_path**, **set_false_path**, and **group_path**. Paths are broken by making the pin an endpoint for all timing paths leading to the pin. In addition, the pin becomes a startpoint for all timing paths going out of the pin.

WHAT NEXT

To avoid broken timing paths, try to set timing exceptions on ports and register clock or data input pins. For other types of pins, use -through pin exceptions rather than -from and -to pin exceptions. The major difference between the -from, -to, and -through options is that -from causes the path to be broken if the pin is not a normal timing startpoint, -to causes the path to be broken if the pin is not a normal timing endpoint, and -through does not break paths.

SEE ALSO

set_max_delay (2), **set_min_delay** (2), **set_multicyle_path** (2), **set_false_path** (2), **group_path** (2).

TIM-176 (information) Timer is not in zero interconnect delay mode.

DESCRIPTION

This information message advises you that the timer is no longer working in the zero interconnect delay mode. The timer is in normal mode so the net wire capacitance is restored from the back annotation or from the wire load model.

WHAT NEXT

This is an informational message only. No action is required.

However, if the result is not what you intended, you can enable zero interconnect delay mode by setting **set_zero_interconnect_delay_mode** to **true**.

SEE ALSO

get_zero_interconnect_delay_mode(2)
set_zero_interconnect_delay_mode(2)

TIM-177 (warning) Timer is in zero interconnect delay mode.

DESCRIPTION

This warning message occurs when the timer is working in the zero interconnect delay mode. The net wire capacitance is 0 when calculating the delay, for example, Cw = 0.

When you run the **set_zero_interconnect_delay_mode** command without specifying **true** or **false**, zero interconnect delay mode is enabled by default.

After you set the interconnect delay mode to zero, the **report_timing**, **report_constraint**, and all commands that use the wire delay reflect the zero Cw. This also affects optimization.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, it is considered best practice to set **set_zero_interconnect_delay_mode** to **false** before the timing optimization. Otherwise, the optimization does not see the interconnect delay, even if the design has the wire load model specified, the design is back annotated, or the design is routed.

WHAT NEXT

get_zero_interconnect_delay_mode(2)
set_zero_interconnect_delay_mode(2)

TIM-178 (warning) This '%s' constraint is no longer applicable to any path.

DESCRIPTION

This warning message occurs when pins or clocks have been removed from the timing path constraint to the extent that the constraint cannot be applied. For example, a false path from {A B} to {C D} is dropped if both C and D have been removed from the design.

This message is also issued when an ungroup is performed by first changing the current_design to a subdesign, and then back to top. The timing constraints set from the top level design might not apply after the ungroup and can be lost.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you expected, check the constraint file for any redundancies. If the message occurs because the ungroup was performed from a subdesign, run the **ungroup** command from the top level using the **-all_instances** option, if needed.

SEE ALSO

ungroup(2)

TIM-179 (warning) '%s' constraint made a reference '%s %s' which no longer exists.

DESCRIPTION

This warning message occurs when the pin or object specified in the timing constraint has been removed as the result of an optimization or constraint propagation. This can cause the constraint to no longer apply to the design.

This message is also issued when an ungroup is performed by first changing the current_design to a subdesign, and then back to top. The timing constraints set from the top level design might not apply after the ungroup and can be lost.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you expected, check the constraint file for any redundancies. If the message occurs because the ungroup was performed from a subdesign, run the **ungroup** command from the top level using the **-all_instances** option, if needed.

SEE ALSO

ungroup(2)

TIM-180 (information) Total %d nets in the design, %d nets have timing window.

DESCRIPTION

This message gives a summary of the number of nets in the design and how many of them have timing windows. This message is issued during timing update when SI analysis is enabled and timing windows are considered in SI analysis.

WHAT NEXT

This is an informational message only. No action is required.

TIM-181 (Error) Relationship between clocks %s and %s is already defined to be %s by group %s

DESCRIPTION

The clock pair already has a relationship defined by a set_clock_groups command prior to the current set_clock_groups command.

WHAT NEXT

If you want to change the clock relationship, remove the exisiting relationship by using the **remove_clock_groups** command. You can use **report_clock** command with fb-groups option to see more details.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

TIM-182 (Warning) Clock group %s has all design clocks in one group.

DESCRIPTION

The current set_clock_groups command specifies all the clocks in the same group. This is a valid setting if you plan to add more clocks. This command serves no prupose otherwise.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

TIM-183 (Warning) False path got overridden by set_clock_groups.

DESCRIPTION

The current set_clock_groups command overrode an existing false path between the specified clocks. The clocks are from different groups of set_clock_groups command.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_timing_requirements** (2), **report_clock** (2).

TIM-184 (Error) Clock group settings for %s and %s conflict with previously set clock group settings.

DESCRIPTION

This error message occurs when a set_clock_groups command conflicts with a previous set_clock_groups command. For example, if a previous command has specified a false path between a pair of asynchronous clocks, then a new command tries to allow paths between the pair of clocks, you will see this error message. Use report_clock -groups to see all clock groups. Remove the existing clock group if you want to change the clock group settings for the clock pair.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

TIM-185 (Error) Clock group %s not found.

DESCRIPTION

The error occurs if the clock group of given name is not found by remove_clock_group command. Use report_clock with -groups option to list all clock groups.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

TIM-186 (Error) Clock group %s already exists.

DESCRIPTION

The error occurs if the clock group of given name and given type already exists. Use report_clock with -groups option to list all clock groups.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

TIM-187 (Error) Clock group setting clash with false path settings of group %s (%s).

DESCRIPTION

The current set_clock_groups command conflicts with an earlier set_clock_groups setting issued for the group of clocks. This message usually occurs when all clocks in the design have been specified in the same group and their false path settings clash with another set_clock_groups command. For example, a previous set_clock_groups command specifies false path but the current command allows timing paths. Use report_clock -groups to see all clock groups. Remove the existing clock group if you want to change the clock group settings for the set of clocks.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

TIM-188 (Error) Clock group %s already defines the %s

relationship for given clocks.

DESCRIPTION

This error message occurs when a set_clock_groups command tries to redefine a relationship for the set of clocks. Use remove_clock_groups remove the existing clock group if you want to change the clock group settings. Use report_clock -groups to report all clock groups.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

TIM-189 (warning) there are conflicting senses converging for clock '%s' from pin '%s' in the clock network.

DESCRIPTION

The clock tree for the specified clock contains paths that have conflicting senses merging. This clock will not be propagated forward starting from this pin.

WHAT NEXT

Since there is ambiguity on which sense to choose to propagate, user could use set_clock_sense to pick which sense to propagate for the clock.

TIM-190 (warning) sense defined on pin '%s' cannot be honored for clock '%s'.

DESCRIPTION

The sense defined on the pin is not available and cannot be honored. This happens when the clock senses propagated to this pin doesn't contain the sense user has chosen. The defined sense is ignored and the original senses are propagated forward.

WHAT NEXT

A feasible clock sense has to be set by set_clock_sense, otherwise the defined sense is ignored.

TIM-193 (info) Generated Clock (%s) has non_unate sense on master source pin.

DESCRIPTION

For a generated clock if the master source pin has a non-unate sense, then by default the tool will only propagate the positive sense waveform from the generated clock source pin to the clock pins. This information will help the user understand which generated clock has non-unate sense on their master source pin.

WHAT NEXT

The user can create an additional generated clock with a -preinvert option to propagate the negative sense.

TIM-196 (warning) Clock group %s already defines the relationship for the given set of clocks.

DESCRIPTION

This warning message occurs when the clock group for the specified set of clocks and type already exists.

WHAT NEXT

Use the **report_clock** command with the **-groups** option to list all clock groups. Rerun the command with either a new clock group, or a new set of clocks.

SEE ALSO

remove_clock_groups(2)
report_clock(2)
set_clock_groups(2)

TIM-197 (error) Cannot find the definition of mode '%s'.

DESCRIPTION

This error message occurs when user tries to set an invalid mode value to cell, which is not defined in the reference library.

WHAT NEXT

Use the **report_mode** command to list all modes to look for which mode is you wanted.

SEE ALSO

TIM-200 (warning) Data Checks from-pin (%s) and to-pin (%s) are the same pin. Ignoring

DESCRIPTION

Datacheck from pin and to pin cannot be the same pin. The tool will ingore the data-check constaint in that case.

WHAT NEXT

Tool will issue a warning message and skip the constaint.

TIM-201 (Error) Generated clock (%s) (%s) is not satisfiable; zero source latency will be used.

DESCRIPTION

This is an error message whenever the clock network traverse can not find a path which satisfies the sense relationship defined by create_generated_clock command.

WHAT NEXT

Check for the generated clock definition to see if the generated clock is correctly defined. One example is that a divided_by 2 generated clock is driven by a inverter only. In this case, generated clock should be redefined with -invert with -divided_by 1. Another example is a divided_by 2 generated clock with preinverting. If master clock source pin is used as generated clock source pin, the warning message will be issued. In this case, generated clock source pin should be redefined to clock pin of divider.

TIM-202 (Error) The master of the following generated clock is

not connected to any clock source.

DESCRIPTION

This error message occurs when check_timing command finds generated clock in the design is not connect to any clock source.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-203 (Error) The following generated clocks form a loop.

DESCRIPTION

This error message occurs when check_timing command finds generated clocks in the design form a loop. For example, when the source pin of G_CLK1 is the definition point of G_CLK2, meanwhile the source pin of G_CLK2 is the definition point of G_CLK1, the tow generated clocks form a loop.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-204 (Warning) The following generated clock has no path to its master clock.

DESCRIPTION

This Warning message occurs when check_timing command finds the definition point of generated clock has no path to its master clock. For example, master clock CLK1 defines on point A, and its generated clock GCLK1 defines on B, if there’s no path from A to B, the Warning message will be printed out.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-205 (Warning) cross clocks found.

DESCRIPTION

This Warning message occurs when check_timing command finds clock interactions. If a clock launches one or more paths, which are captured by other clocks, it will have an entry in clock crossing report. If all paths between two clocks are false paths or the are exclusive/asynchronous clocks, the path is marked by *. If only part of paths are set as false paths, the path is marked by #.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-206 (Warning) following data check register reference pins are not driven by clocked signal.

DESCRIPTION

This warning message occurs when check_timing command finds no clocked signal reaches a data check register reference pin.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-207 (Warning) following data check register reference pins are driven by multiple clocked signals.

DESCRIPTION

This warning message occurs when check_timing command finds multiple clocked signals reach a data check register reference pin.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-208 (Warning) The following input ports have no

clock_relative delay specified, a default clock is assumed for these input ports.

DESCRIPTION

This warning message occurs when check_timing command finds no clock related delay specified on an input port, where it propagates to a clocked latch or output port. Note that with timing_input_port_default_clock set to 'true', a default clock will be assumed for the input port. Otherwise it will not be clocked, and the paths are unconstrained. In this case, if there is no input delay specified, check_timing will not generate warnings.

WHAT NEXT

Please manually set the input delay for the listed ports by using the command set_input_delay with -clock option.

SEE ALSO

check_timing (2), **timing_check_defaults** (3). **set_input_delay** (2)

TIM-209 (Warning) timing loops detected.

DESCRIPTION

This warning message occurs when check_timing command finds combinational feedback loops.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-210 (Warning) there are %d input ports without driving cell specified.

DESCRIPTION

This warning message occurs when check_timing command finds no driving cell specified on an input port. In such case, the accuracy of delay calculation could be impacted, as a default strong driver is assumed in absence of driving cell definition. Especially, in presence of crosstalk, a port with no driving cell could act as a strong aggressor which could lead to significant amount of pessimism in the

analysis. Also, a port with no driving cell could act as a string victim, which could underestimate the crosstalk effect. Command set_driving_cell could be used to specify a library cell or pin to drive ports.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-211 (Warning) there are %d ideal clocks.

DESCRIPTION

This warning message occurs when check_timing command finds ideal clocks. Generally, all clocks should be propagated so that the clock network timing is accurately calculated. Especially, in presence of crosstalk, the delay changes induced by other nets on the clock network will not be reflected in the calculated slacks in the design. Command set_propagated_clock could be used to define clock as propagated.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-212 (Warning) there are %d input ports that only have partial input delay specified.

DESCRIPTION

This warning message occurs when check_timing command finds partial input delay specified on an input port. This happens when set_input_delay -min is appliedon a port to set the min input delay with respect to a clock, however no set_input_delay -max is applied to that port to specify the max delay, or vice versa. As a result, some paths starting from the port with partially defined input delay may become unconstrained and some potential violations could be missed. Command set_input_delay could be used to set both min and max delay on the port.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-213 (warning) the specific arc is in clock path, report_delay_calculation result may not match with timing report

or clock skew report for this arc.

DESCRIPTION

This warning message occurs when both from pin and to pin are in clock network. In clock skew/latency calculation, tool use the slew from clock propagation path to calculate delay result. While in report_delay_calculation command, tool use the worst slew to calculate delay. This may cause different delay results.

SEE ALSO

report_delay_calculation (2),

TIM-214 (Warning) there are %d nets without driver pins.

DESCRIPTION

This warning message occurs when check_timing command finds nets without driver pins.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-215 (Warning) there are %d nets without timing arcs on driver pins.

DESCRIPTION

This warning message occurs when check_timing command finds no timing arcs defined on the driver pins of the net.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-250 (warning) At pin '%s' clock '%s' does not have the

needed ’%s’ edge.

DESCRIPTION

The clock tree contains half unate timing arcs or disable timing commands that have disabled the needed rise or fall edge. The register clock pin given will not have the clock assigned to it and will not be timed.

WHAT NEXT

Alter clock network to propagate the needed clock edge to this register.

TIM-300 (Error) Could not %s timing data %s %s: %s. Falling back to full update.

DESCRIPTION

The application sometimes saves timing data to a temporary file. Something went wrong either saving or restoring this data. For example, if the target disk was full, you would get this message. The program will continue as though the temporary directory was unavailable, possibly with some performance penalty.

WHAT NEXT

Files are saved either to /tmp or the value of the TMPDIR environment variable. If the message indicates that saving was in progress, most likely the temporary directory does not exist, you don’t have permissions to write to it, or it is full. The message will indicate the cause. In most cases, the disk is full. Either delete some files, or find a different temporary directory and set the TMPDIR environment variable to point at it. A problem during restore is rare. It might be that someone accidently deleted the file or the file became corrupt.

SEE ALSO

TM-001 (information) Design is in trace mode

DESCRIPTION

This message indicates that the design is in trace mode and the netlist is partially loaded into memory.

WHAT NEXT

set_fp_trace_mode(2) end_fp_trace_mode(2)

TM-002 (information) Design is not in trace mode

DESCRIPTION

This message indicates that the design is not in trace mode and the netlist is fully loaded into memory.

WHAT NEXT

set_fp_trace_mode(2) end_fp_trace_mode(2)

TM-003 (information) full netlist not loaded yet... Next command that needs full netlist will load it

DESCRIPTION

This message indicates that the design netlist is not loaded after we ended trace mode. The netlist was merely removed from memory, and will be loaded when the next command that needs the netlist is executed.

WHAT NEXT

set_fp_trace_mode(2) end_fp_trace_mode(2)

TPM-10 (error) Test program '%s' does not match the design '%s'.
Test program was not restored.

DESCRIPTION

This message indicates that the test program does not match the design. The design has probably been changed since the test program was written.

WHAT NEXT

If you need to use this test program, you must change the design back to what it was when the test program was written out. Otherwise, the test program cannot be used and a new one will have to be generated.

TPM-20 (error) '%s' is not a valid name for the test program because it matches the name of one of the test programs in the current sequence.

DESCRIPTION

This test generation or fault simulation run is an incremental run. This message indicates that the name being assigned to the incremental test program is not valid. (The -output option specifies the test program name. If you have not specified the name, then the default is the 'design' name). This is because the name is the same as that of one of the test programs in the sequence that this incremental test program depends on.

You should see this message when you are using TestManager and when the **multi_pass_test_generation** variable has the value TRUE.

WHAT NEXT

If you want this run to be an incremental run, then use a different name for this incremental test program.

If this is a new run targetting the entire fault list (i.e. it is not intended to be an incremental run), then first execute the command **delete_test** to remove the current test program.

You should set the **multi_pass_test_generation** variable to FALSE if you want every

run to be an independent run targetting the entire fault list.

TPM-30 (error) '%s' %s. It cannot be restored.

DESCRIPTION

The vdb file that is being restored does not have any fault information so it cannot be restored. Either this is a 3.0 format vdb or it has been corrupted.

WHAT NEXT

Regenerate the vdb file using the current version of DFT Compiler.

TPM-31 (warning) File '%s' contains only fault information but no vectors.

DESCRIPTION

The testprogram contained in this vdb file was probably created without scan insertion; hence, the vectors were not saved.

WHAT NEXT

If you want to save vectors in the **vdb** file for later fault simulation, first perform scan insertion using **insert_test** and then run **create_test_patterns**.

TPM-40 (warning) Deleting current test program '%s' because it is not consistent with the current design.

DESCRIPTION

The current test program is not compatible with the current design. This could be because you have changed the design or switched to another design.

The current test program will be deleted from memory and the next ATPG or fault simulation run will use a new initial fault list for the current design.

Note that the test program that was just deleted from memory is still available on disk.

WHAT NEXT

If you wish to restore the previous test program which was just automatically deleted, first restore the current design to its original state (i.e. its state when that test program was created), and then use the restore_test command.

TPM-41 (warning) Deleting current test program '%s' because it was generated
for the design '%s' but the current design is '%s'.

DESCRIPTION

The current test program is not compatible with the current design. This could be because you have changed the design or switched to another design.

The current test program will be deleted from memory and the next ATPG or fault simulation run will use a new initial fault list for the current design.

Note that the test program that was just deleted from memory is still available on disk.

WHAT NEXT

If you wish to restore the test program which was just automatically deleted, first restore the current design to its original state (i.e. its state when that test program was created), and then use the restore_test command.

TPM-50 (error) Current design is '%s', but trying to restore a test program for design '%s'.

DESCRIPTION

The current design name and the design name for the test program you are trying to restore are different.

WHAT NEXT

If you wish to restore the specified test program, first set the current design to the one in the specified test program and then use the restore_test command.

TPM-60 (information) This %s run is an incremental run. It will

target
  the faults left undetected by the preceding test program.

DESCRIPTION

This message informs you that this test generation or fault simulation run will be an incremental run. It will target only the faults which were not detected by the previous runs.

You will see this message when you are using TestManager and when the **multi_pass_test_generation** variable has the value TRUE.

WHAT NEXT

You should set this variable to FALSE if you want every run to be an independent run targetting the entire fault list.

TRANS-1 (warning) Cell '%s' (%s) not translated.

DESCRIPTION

The named cell could not be translated into the target_library. This error happens most often when the cell is specified with a **dont_touch** attribute; the cell has unknown functionality; or no replacement exists in the target_library.

WHAT NEXT

If the cell was not translated because of a **dont_touch** attribute, remove that attribute and translate again.

If the library cell has the **dont_use** attribute in the target_library, then you can consider removing that attribute from the library cell and translating again; otherwise, you must remove the **dont_touch** attribute from the cell and translate again.

If the cell was not translated because it has unknown functionality, either hand-translate the cell or functionally model it in the original technology library.

If the cell was not translated because no replacement exists in the target_library, then either the target_library actually doesn't have a replacement and you must add one; or the replacement is not functionally modeled and you must model it.

This error will not occur with combinational cells. If it understands the functionality, **translate** can map a combinational cell to a cell in the target_library. This error may occur with sequential cells if the original cell has a preset or clear and there is no similar cell in the target_library; or if the similar cell is not sequentially modeled.

Three-state cells might not translate if the target_library contains no three-state cells or the three-states cells are not functionally modeled. In these two cases the cells are left as generic flip-flops or generic three-states. You must add the correctly modeled cells to the target_library, or hand-translate the cells.

To hand-translate cells, create a netlist with the same port interface and name as the cell to be translated and instantiate the translation (cells from the target_library) inside this netlist. Then execute **link -all** to link this netlist in place of the cells from the original library so that they now appear as a level of hierarchy with the translation inside. Ungroup these levels of hierarchy to finish the translation.

This error may also occur with designs which contain references to synthetic library parts if the link_library variable does not list the proper synthetic library file.

TRANS-2 (warning) Flip-flop '%s' (%s) cannot be translated exactly into '%s'.

DESCRIPTION

The named flip-flop could not be translated into the type of cell specified with *set_register_type -exact* command. This error happens most often when the exact specified replacement does not match the asynchronous requirements of the original cell.

WHAT NEXT

If you do not require an exact replacement, consider this message informational and ignore it; the cell will be translated, but not into the exact specified cell.

If you want the cell to be translated into the exact replacement, check the modeling of the replacement cell in the target_library to make sure it is correly modeled. If this is the case, fix the sequential modeling of this cell in the target_library.

TRANS-3 (warning) Flip-flop '%s' (%s) cannot be translated to requested type.

DESCRIPTION

The named flip-flop could not be translated into the type of cell specified with *set_register_type* command. This error happens most often when no cell exists in the target_library that matches the specified type and asynchronous requirements of the original cell.

WHAT NEXT

If you do not require the specified replacement type, consider this message informational and ignore it.; the cell will be translated to something close but not the exact specified replacement type.

If you want the cell translated into the exact replacement type, check the modeling of the replacement cell in the target_library to make sure it is correctly modeled.

TRANS-4 (warning) Target library contains no replacement for

register ’%s’ (%s).

DESCRIPTION

The named register could not be translated into the target_library. The most likely reason is that no cell exists in the target_library that matches the asynchronous requirements of the original cell. Another possible reason is that the target_library contains no registers, or has not been sequentially modeled. The register is left as a generic flip-flop (**FFGEN**).

WHAT NEXT

Add a correctly-modeled sequential element to the target_library with the same asynchronous requirements as the cell that was not translated.

TRANS-5 (warning) Unable to determine wired-logic type for multiple-driver net ’%s’.

DESCRIPTION

The named net has more than one driver, but Design Compiler was unable to determine whether this should be considered a wired-AND, wired-OR, or three_state bus. This happens if all the cells connected to the net are unmapped or black boxes, and the technology cannot be determined.

WHAT NEXT

Design Compiler assumes the net is a wired-AND. If it is not, place an attribute on the net indicating the wired-logic function. To do this, use the *set_attribute* command to set one of the following Boolean attributes to *TRUE* on the net: *wired_and*, *wired_or*, or *three_state*.

TRANS-6 (information) Assuming multiple-driver net ’%s’ is a %s.

DESCRIPTION

The wired-logic type of the named net could not be determined. This usually occurs if the net’s drivers are unmapped cells or black-boxes. It may also occur if the wired-logic types of the drivers conflict. In these cases, Design Compiler assumes that the net is a wired-AND.

WHAT NEXT

If this is not the desired behavior, you should check the drivers of the net and make sure that they are correctly modeled to drive the desired wired-logic type.

TRANS-7 (warning) Net '%s' is not a legal wired_logic net. However, it will not be replaced because this is an in-place optimization.

DESCRIPTION

The named net was considered an illegal wired-logic net. Some of the reasons this may occur are: (1) if there is a wired-connection-class conflict on the net, or (2) if the number of emitters on the net exceeds max_wired_emitters, or (3) if any of the wired-logic drivers are not allowed to drive wired-logic. During a full or incremental compile, ECL Compiler would normally replace this illegal wired-logic net with the appropriate functionality. However, in this case, an in-place optimization has been requested, and, therefore, ECL Compiler can not change nets in that way. Instead, the net will be preserved in its illegal state. In-place optimization may sometimes correct wired-logic nets, but that can not always be guaranteed.

WHAT NEXT

Run the 'check_design' command for more information about the illegal net. In some cases, this warning message may be due to incorrect modeling of wired-logic in the technology library.

TRANS-8 (warning) Combinational cell '%s' (%s) cannot be translated exactly into '%s'.

DESCRIPTION

The named combinational cell could not be translated into the type of cell specified with *set_combinational_type* command. This warning happens most often when the exact specified replacement does not match the function of the original cell.

WHAT NEXT

If you do not require an exact replacement, consider this message informational and ignore it; the cell will be translated, but not into the exact specified cell.

If you want the cell to be translated into the exact replacement, check the modeling of the replacement cell in the target_library to make sure it is correly modeled. If

this is the case, fix the functional modeling of this cell in the target_library.

TRANS-9 (warning) Cell '%s' (%s) cannot be exactly translated 1 for 1 into target library. Ignoring set_compile_directives.

DESCRIPTION

The named cell could not be translated 1 for 1 into a corresponding cell in the target library. Therefore, the cell will be translated and the directives specified with **set_compile_directives** command will be ignored.

WHAT NEXT

set_size_only or **set_compile_directives** must not be applied on this cell.

TRANS-10 (warning) Cell '%s' (%s) has use_for_size_only attribute and cannot be translated 1 for 1 into target library .

DESCRIPTION

The named cell could not be translated 1 for 1 into a corresponding cell in the target library. Therefore, the cell will not be translated.

WHAT NEXT

This cell has to be translated manually.

TRANS-11 (warning) Target library contains no replacement for isolation cell '%s' (%s); it was not translated.

DESCRIPTION

The named isolation cell could not be translated into the target_library during the translate or compile commands. This error can happen when the cell is specified with a **dont_touch** attribute, or when no suitable replacement exists in the target_library. If voltages on the input and output of the isolation cell are the same, then a suitable replacement is a cell from the target_library with the same functionality as the named cell, which carries the is_isolation_cell attribute. If input and output voltages differ, a suiteable replacement cell is one from the target_library with the same functionality, with the is_level_shifter and

is_isolation_cell attributes, and input and output voltages that match the voltages on the cell being translated, .

WHAT NEXT

If the cell was not translated because of a **dont_touch** attribute, remove that attribute and translate again.

If the library cell has the **dont_use** attribute in the target_library, then you can consider removing that attribute from the library cell and translating again.

If the cell was not translated because no replacement exists in the target_library, then verify that the operating conditions on the cell are set correctly. If operating conditions are set correctly, but no matching cell exists in target_library, then replace the cell with one whose functionality and operating conditions are available in the library.

TRANS-12 (warning) Target library contains no replacement for level shifter cell '%s' (%s); it was not translated.

DESCRIPTION

The named level shifter cell could not be translated into the target_library during the translate or compile commands. This error can happen when the cell is specified with a **dont_touch** attribute, or when no suitable replacement exists in the target_library. A suitable replacement is a cell from the target_library with the same functionality as the current cell; with the is_level_shifter and is_isolation_cell attributes; and input and output voltages that match the voltages on the cell being translated.

WHAT NEXT

If the cell was not translated because of a **dont_touch** attribute, remove that attribute and translate again.

If the library cell has the **dont_use** attribute in the target_library, then consider removing that attribute from the library cell and translating again.

If the cell was not translated because no replacement exists in the target_library, then verify that the operating conditions on the cell are set correctly. If operating conditions are set correctly, but no matching cell exists in target_library, then replace the cell with one whose functionality and operating conditions are available in the library.

TRANS-13 (warning) Design %s is instantiated more than once.

It will not be translated.

DESCRIPTION

This warning message occurs when the specified design is instantiated more than once in the design hierarchy. When the **translate** command is run from the top level of the hierarchy, it can only translate subdesigns that appear once in the hierarchy.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this error, run the **uniquify** command before running **translate**. This makes copies of multiply-instantiated designs, so that each copy of the design appears in the hierarchy only once.

Alternatively, a subdesign can be translated by using the **current_design** command to make that subdesign the current design, and then run the **translate** command. Then you can run **current_design** to make the top-level design the current design.

SEE ALSO

uniquify(2)

TRANS-99 (error) Cell '%s' cannot be used in the relative placement group because it cannot be exactly translated 1 for 1 into the target library.

DESCRIPTION

This error message occurs when the named cell cannot be translated 1 for 1 into a corresponding cell in the target library. Therefore, the cell cannot be used in the relative placement group.

WHAT NEXT

Remove the cell from the relative placement group and run the command again.

TRANS-100 (information) Translate terminated abnormally.

DESCRIPTION

This message indicates that the **translate** command terminated and did not write the intermediate design back to the database. Since the design was not written back to the database, the original design remains unchanged. The reason for the abnormal termination should have appeared in an error message prior to this message. Some of the reasons include: licensing problems, problems loading the technology library(ies), the target library failed to meet minimum requirements, a user interrupt, or problems loading the design.

WHAT NEXT

Look for the error message immediately prior to this one for an indication of the source of the problem.

TRC-301 (warning) Direction given for Supply but ignored.

DESCRIPTION

This warning is generated when the user specifies the direction for signal of Supply type. The direction information is ignored.

WHAT NEXT

Remove the direction field if the signal is of type Supply.

TRC-302 (warning) Clock setting invalid in TRC block.

DESCRIPTION

This warning is generated when user specifies invalid signal type for a clock, e.g. Out or both In and Out. The setting will be ignored and type will set as ClockIn.

WHAT NEXT

Remove the incorrect setting for Clock TRC block.

TRC-303 (warning) Invalid Supply definition in TRC block.

DESCRIPTION

This warning is generated when the Supply is defined together with other Signal types in TRC block. The definition was ignored. Supply should be defined seperately.

WHAT NEXT

Define the supply seperately.

UCN-1 (warning) In the design %s, net '%s' is connecting multiple ports.

DESCRIPTION

This warning message indicates that the specified net is connecting to multiple ports. The net name is changed to a simpler name, which only contain alpha-numeric and underscore.

WHAT NEXT

Check your design and make the appropriate changes to avoid this warning.

SEE ALSO

change_names (2).

UCN-2 (Info) Please make sure that you have run the 'change_names' command on your design before saving files to disk.

DESCRIPTION

To ensure a smooth translation of data between tools in your flow, it is suggested that 'change_names' is ran prior to writing out any formatted file to disk. By applying 'change_names' to your design, you can make certain that the design DB netlist description matches the file description in other file formats, for example Verilog, VHDL, or EDIF. So, your steps would be :- compile or optimize your design run change_names write out your design DB write out your Verilog/VHDL/PDEF, etc.

If your flow is Verilog based, use change_names -rules verilog -hierarchy

If your flow is VHDL based, use change_names -rules vhdl -hierarchy

WHAT NEXT

Please reload the design DB and run change_names with the appropriate rule

SEE ALSO

change_names (2).

UCN-3 (Warning) The specified replacement character (%c) is conflicting with the specified set of allow characters.

DESCRIPTION

The replacement character either using the default value (x) or user specified is not a part of the allow character set for the object.

WHAT NEXT

Re-specify the replacement character that is within range of the allow characters by using define_name_rules -replacement_char.

SEE ALSO

change_names (2). **define_name_rules** (2).

UCN-4 (Warning) The specified replacement character (%c) is conflicting with the specified allowed or restricted character.

DESCRIPTION

The replacement character either using the default value (_) or user specified is not part of the allowed character set or is a part of the restricted character set. For some designs this might not be an issue. However, it is best to have the replacement character to be part of the allow character set and not the same as either first or last restricted character. NOTE: Verilog naming rule does not allow '_' to be the leading character, this warning will be issued if change_names -rule verilog is used.

WHAT NEXT

Re-specify the replacement character that is within range of the allow characters by using define_name_rules -replacement_char.

SEE ALSO

change_names (2). **define_name_rules** (2).

UCN-5 (warning) There are two different dummy net naming conventions defined in name rule ’%s’. ’%s’ defined in option "-add_dummy_nets_in_verilog_out" or "-add_dummy_nets_in_vhdl_out" will take precedence over ’%s’ defined in option "-dummy_net_prefix".

DESCRIPTION

There is a conflict in the dummy net naming convention created by two options in the define_name_rules command. The naming format defined in "-add_dummy_nets_in_verilog_out" or "add_dummy_nets_in_vhdl_out" option will take precendence over the format defined in "-dummy_net_prefix" option.

WHAT NEXT

Use report_name_rules command to determine which name format you want. Then use the define_name_rules command to set the dummy net naming format with the "-add_dummy_nets_in_verilog_out" or "-add_dummy_nets_in_vhdl_out" option instead of the "-dummy_net_prefix" option.

SEE ALSO

define_name_rules (2). **report_name_rules** (2).

UCN-6 (warning) Running change_names without the "-hierarchy" option turned on may result in bad logic.

DESCRIPTION

Change_names will create bad logic in hierarchical designs if the "-hierarchy" switch is not used. Without using the "-hierarchy" switch, name changes cannot propogate to lower levels of hierarchy.

WHAT NEXT

Rerun change_names with the "-hierarchy" switch on.

SEE ALSO

UCN-7 (Info) Options "-add_dummy_nets_in_verilog" and "-

add_dummy_nets_in_vhdl" have been deprecated in define_name_rules. Please use "-add_dummy_nets" in the future.

DESCRIPTION

Since options "-add_dummy_nets_in_verilog" and "-add_dummy_nets_in_vhdl" both create dummy nets to all unconnected pins, they have been combined to one option named "-add_dummy_nets". They have also been combined in the report_name_rules command.

WHAT NEXT

Use option "-add_dummy_nets" in future scripts/runs.

SEE ALSO

report_name_rules (2).

UCN-8 (warning) The first restricted character list conflicts with the name prefix(%s). The name prefix will still be used in change names.

DESCRIPTION

The first character of the name prefix is one of the characters of the first restricted characters list. The conflict will be ignored and the prefix will be used.

WHAT NEXT

Resolve the problem by changing the prefix or the first restricted characters list.

SEE ALSO

define_name_rules(2).

UCN-9 (error) Command options of change_names -instance

are wrong.

DESCRIPTION

This error message occurs when change_names -instance command options are wrong.

WHAT NEXT

Correct the command options and re-issue it.

SEE ALSO

change_names (2).

UCN-10 (error) New name '%s' for change_names -instance is not legal.

DESCRIPTION

This error message occurs when new name specified with -new_name option is not legal.

WHAT NEXT

Specify a legal new name and re-issue the command.

SEE ALSO

change_names (2).

UCN-11 (error) New name '%s' already exists as instance, port or net name in the design.

DESCRIPTION

This error message occurs when new name specified with -new_name option already exists as instance name or port name.

WHAT NEXT

Specify a legal new name and re-issue the command.

SEE ALSO

change_names (2).

UCN-15 (Error) Name too long (>%d bytes) in name_file %s.

DESCRIPTION

This error message occurs when the name in the name_file is too long and over the allowed range.

WHAT NEXT

Re-specify the name that is within range of the allow name in name_file.The allowed name length is 0~2047.

SEE ALSO

UCN-16 (Error) Invalid type "%s

DESCRIPTION

This error message occurs when the type is invalid.

WHAT NEXT

Re-specify the type in name_file that must be port, cell, or net .

SEE ALSO

change_names (2).

UCN-17 (Error) Can not specify both -allowed and -restricted

options. The rule is not created.

DESCRIPTION

This error message occurs when both -allowed and -restricted options are specified.

WHAT NEXT

Re-define the name rule by using define_name_rules -allowed or define_name_rules -restricted.

SEE ALSO

change_names (2). **define_name_rules** (2).

UCN-18 (Error) -type %s is not supported. Please specify it to be port, cell or net.

DESCRIPTION

This error message occurs when the specified rule type is not port or cell or net,we don’t support this type.

WHAT NEXT

Re-specify the rule type "-type", that must be port, cell or net.

SEE ALSO

change_names (2). **define_name_rules** (2).

UCN-19 (Error) dummy_net_prefix is invalid in format.

DESCRIPTION

This error message occurs when the format of the specified dummy_net_prefix is invalid.

WHAT NEXT

Re-specify dummy_net_prefix in correct format.

SEE ALSO

change_names (2). **define_name_rules** (2).

UCN-20 (Warning) Net '%s' is connected to more than one port. Equal ports and nets rule cannot be satisfied.

DESCRIPTION

If a net is connected to more than one port,the rule -equal_ports_nets cannot be satisfied. The net's name is not changed.

WHAT NEXT

SEE ALSO

change_names (2). **define_name_rules** (3).

UCN-21 (error) The defined maximum length is less than the lower limit of the -max_length rule (%d).

DESCRIPTION

This error message occurs when the specified maximum length is less than the lower limit of the **-max_length** rule. If the maximum length is too small, some changes for the **-max_length** rule are meaningless.

WHAT NEXT

Define a maximum length that is greater than the lower limit.

SEE ALSO

change_names(2)

UI-1 (error) Variable '%s' is undefined.

DESCRIPTION

The command referred to a variable that is not defined.

WHAT NEXT

Recheck the name of the variable you reffered to. Use the **list** command to list the variables that are currently defined.

UI-2 (error) No manual entry for ’%s’.

DESCRIPTION

WHAT NEXT

UI-3 (error) Number of commands to display must be an integer.

DESCRIPTION

WHAT NEXT

UI-4 (error) Invalid alias list.

DESCRIPTION

WHAT NEXT

UI-5 (warning) Alias ’%s’ is not defined.

DESCRIPTION

WHAT NEXT

UI-6 (error) Variable group ’%s’ is undefined.

DESCRIPTION

WHAT NEXT

UI-7 (error) Could not change directory to ’%s’.

DESCRIPTION

WHAT NEXT

UI-8 (error) Cannot issue the ’ls’ command.

DESCRIPTION

WHAT NEXT

UI-9 (error) Cannot issue the ’%s’ command.

DESCRIPTION

WHAT NEXT

UI-10 (error) ’%s’ not a valid type.

DESCRIPTION

WHAT NEXT

UI-11 (error) Line %d: argument ’%s’ of command ’%s’ is the

wrong type.

DESCRIPTION

WHAT NEXT

UI-12 (error) Synopsys software was incorrectly installed.

DESCRIPTION

WHAT NEXT

UI-13 (warning) The variable ’%s’ must be defined before

Design Compiler can be run.

DESCRIPTION

WHAT NEXT

UI-14 (error) Argument ’%s’ of command ’%s’ is the wrong type.

DESCRIPTION

WHAT NEXT

UI-15 (error) ’%s’ is expecting a %s, not a %s.

DESCRIPTION

WHAT NEXT

UI-16 (error) Line %d: missing arguments to command ’%s’.

DESCRIPTION

WHAT NEXT

UI-17 (error) Missing arguments to command ’%s’.

DESCRIPTION

WHAT NEXT

UI-18 (warning) Expecting ’%s’.

DESCRIPTION

WHAT NEXT

UI-19 (error) The name of a file to include was not specified.

DESCRIPTION

WHAT NEXT

UI-20 (error) Include file '%s' could not be opened.

DESCRIPTION

WHAT NEXT

UI-21 (error) Execution of include file '%s' was terminated because an error was generated.

DESCRIPTION

The **include** file was not 100% executed, because of an error generated by one of the commands contained in the file. The execution was terminated at the offending command.

WHAT NEXT

Examine the **include** file to determine why the command failed. Edit the **include** file to correct any errors, and re-execute **include**.

UI-22 (error) Log file ’%s’ could not be opened.

DESCRIPTION

WHAT NEXT

UI-23 (error) Log file ’%s’ was not completely written due to an error.

DESCRIPTION

WHAT NEXT

UI-24 (error) Aliases may contain only letters, digits or underscores.

DESCRIPTION

WHAT NEXT

UI-25 (error) The ’alias’ and ’unalias’ commands may not be

aliased.

DESCRIPTION

WHAT NEXT

UI-26 (error) Log file ’%s’ can’t be included.

DESCRIPTION

WHAT NEXT

UI-27 (error) You need write permissions on the current or home

directory to read an HDL file.

DESCRIPTION

WHAT NEXT

UI-30 (error) Unrecognized feature name ’%s’.

DESCRIPTION

WHAT NEXT

UI-31 (information) You already have a ’%s’ license.

DESCRIPTION

WHAT NEXT

UI-32 (error) You don’t have a ’%s’ license to remove.

DESCRIPTION

WHAT NEXT

UI-33 (error) List function ’-%s’ is not available.

DESCRIPTION

WHAT NEXT

UI-34 (error) Invalid feature list.

DESCRIPTION

A parameter to the **license_users** command is not a valid Synopsys licensed feature.

WHAT NEXT

Refer to the Synopsys Installation Reference Manual for a list of features supported by the current release, or determine from the key file all the licensed features at your site.

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UI-35 (error) Bad value ’%s’ specified for compatibility_version.

DESCRIPTION

WHAT NEXT

UI-36 (information) Acceptable values must look like ’v1.3’, ’v2.0’ (up to ’v3.5’), or ’1997.01’...

DESCRIPTION

WHAT NEXT

UI-37 (error) Value ’%s’ is greater than the current

product_version.

DESCRIPTION

WHAT NEXT

UI-38 (information) Value must be less than or equal to ’%s’.

DESCRIPTION

WHAT NEXT

UI-39 (error) Variable ’%s’ cannot be set; it is read-only.

DESCRIPTION

You attempted to set a read-only product variable. It automatically changes itself back. Variables like the date, the product version, and the synopsys root directory cannot be reset from a command line.

WHAT NEXT

Check this parameter in your environment before restarting the tool.

UI-40 (error) Cannot read include file ’%s’; it’s a directory.

DESCRIPTION

WHAT NEXT

UI-41 (error) Previous error has stopped execution of %s.

DESCRIPTION

WHAT NEXT

UI-42 (error) Can’t find the %s ’%s’ in memory.

DESCRIPTION

WHAT NEXT

UI-43 (error) No %s were specified to be deleted.

DESCRIPTION

WHAT NEXT

UI-44 (error) You can’t specify both a %s list and -all.

DESCRIPTION

WHAT NEXT

UI-45 (error) No %s were specified to be reported on.

DESCRIPTION

WHAT NEXT

UI-46 (error) Can’t remove system variable ’%s’.

DESCRIPTION

WHAT NEXT

UI-47 (error) Value required for the ’<variable_name>’

argument.

DESCRIPTION

WHAT NEXT

UI-48 (error) Unexpected arguments.

DESCRIPTION

WHAT NEXT

UI-49 (error) Bad variable name specified.

DESCRIPTION

WHAT NEXT

UI-50 (error) The ’%s’ command may not be aliased.

DESCRIPTION

WHAT NEXT

UI-51 (error) License ’%s’ is required by design ’%s’. You must remove the design before you can remove the license.

DESCRIPTION

WHAT NEXT

UI-52 (error) Design ’%s’ is a limited design and cannot be

written out.

DESCRIPTION

DESCRIPTION

A design can be limited for either of two reasons: (1) The design is fully licensed, but it has not yet been mapped. (2) The only licence that could be checked out for the design was a limited license. A limited design can not be written out to disk.

WHAT NEXT

If the design is simply not mapped, then compiling the design will allow you write it to disk. If the design is limited because of licenses, then the only way to get access to the design is to check out a license that gives full access.

UI-53 (error) Design '%s' has not been mapped yet and you can only write it out in db format.

DESCRIPTION

WHAT NEXT

UI-56 (warning) Illegal setting '%s' for the 'hdl_preferred_license' variable.

DESCRIPTION

Legal values are "VHDL" or "verilog".

WHAT NEXT

UI-57 (warning) The perferred license '%s' is already checked

out, it will try to get other equivalent sets of licenses.

DESCRIPTION

The possible values for BC preferred licenses are "bc_verilog", "bc_vhdl" , "bc_fpga_vhdl" or "bc_fpga_hdl.

WHAT NEXT

UI-58 (information) Created bus ’%s’: Start index ’%d’ is connected to ’%s’. End index ’%d’ is connected to ’%s’.

DESCRIPTION

WHAT NEXT

UI-60 (error) ’%s’ is an invalid value for the list variable ’%s’. The variable value has not been changed.

DESCRIPTION

WHAT NEXT

UI-61 (error) Cannot create temporary files in current working directory ’%s’.

DESCRIPTION

This error message informs you that you do not have permission to create the required temporary files in the current working directory.

WHAT NEXT

Change your current working directory to a directory in which you have the necessary permissions, or change the permissions of the current working directory. To

determine which permission is missing, see UI-62.n.

SEE ALSO

UI-62(n)

UI-62 (information) You do not have %s permission on this directory.

DESCRIPTION

This message indicates the type of permission (read, write, or execute) that you do not have on the current working directory. This man page accompanies other error messages.

WHAT NEXT

You can use this message to determine the type of permission missing on the directory, and change the permissions accordingly.

SEE ALSO

UI-61(n)

UI-63 (error) Invalid value ’%s’ for variable ’%s’. Setting the variable to its default value, ’%s’.

DESCRIPTION

You receive this message if you attempt to set an environment variable with a value that is not a valid value for that variable. Valid values are listed in each variable’s manual page, or in the group manual page for all variables in a particular group. This message informs you that the specified variable is currently being set to its default value.

WHAT NEXT

If it is acceptable to you that the specified variable is set to its default value, no action is required on your part. Otherwise, refer to the variable’s manual page, choose a valid value, and set the variable accordingly.

SEE ALSO

compile_variables (3).

UI-64 (information) Replacing old license key '%s' with new license key '%s'.

DESCRIPTION

You receive this message if you attempt to check out an old license key that has been replaced by the new license key. This message informs you that the new license key is being checked out instead of the old one.

WHAT NEXT

This is an informational message only. No action is required on your part.

UI-65 (warning) File %s is not readable and/or not writable and cannot be appended to. Creating new file %s.

DESCRIPTION

This warning message occurs when you are running the **set_svf** command and you attempt to append to a file that is not readable, not writable, or both.

WHAT NEXT

This is a warning message only. No action is required on your part. A new file is created in which to record changes.

However, you can avoid this warning message in the future by verifying that the file you want to append to has the correct read and write permissions before you use the **-append** option.

SEE ALSO

set_svf(2)

UI-66 (warning) File %s does not exist and so cannot be

appended to. Creating new file %s.

DESCRIPTION

This warning message occurs when you are running the **set_svf** command and you attempt to append to a file that does not exist.

WHAT NEXT

This is a warning message only. No action is required on your part. A new file is automatically created.

However, you can avoid this warning message in the future by making sure a file exists before using the **-append** option.

SEE ALSO

set_svf(2)

UI-67 (error) License %s is required by XG mode. You must end XG mode to remove the license.

DESCRIPTION

This error message occurs if you attempt to remove the license feature that is needed to enable XG mode operation.

WHAT NEXT

Quit XG mode or exit the product to make one token of this license feature available again.

UI-68 (error) -compress accepts only gzip for db output format.

DESCRIPTION

You receive this message if the output format is db and you specified a compression format other than gzip. Only gzip compression is supported for db files.

WHAT NEXT

Specify gzip for the compression format.

UI-69 (warning) The -compress option can only be used with the .ddc format.

DESCRIPTION

This warning message occurs when the **write** command is used with the **-compress** option for formats other than .ddc. The **write** command completes normally, but compression is not performed.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, and the file format is not .ddc, rerun the command without the **-compress** option.

SEE ALSO

write(2)

UI-70 (warning) Compression is turned on by default.

DESCRIPTION

You receive this message if you have already set write_compressed_db_files to true.

WHAT NEXT

Setting this variable makes all db files to be written out compressed. Use this only if you want db files in all subsequent write commands to be compressed. If you want compressed db in only one particular write command, then unset this variable and use -compress switch of write.

UI-71 (error) No permission to write into this %s directory

DESCRIPTION

This error message occurs when there is no read or write permission on this directory.

WHAT NEXT

Change the read and write permissions on the specified directory to allow new files and directories to be created inside the directory.

SEE ALSO

set_svf(2)

UI-72 (Error) Failed to create a directory %s to store multipliers' netlists.

DESCRIPTION

This error message occurs when the tool cannot create a subdirectory in the specified directory to store multipliers' netlists, possibly due to limitations of the UNIX system.

WHAT NEXT

Check the permissions on the file system and also check the limitations of the UNIX system.

SEE ALSO

set_svf(2)

UI-73 (error) Failed to write an architectures' db at %s.

DESCRIPTION

The Synopsys verification file (SVF) failed to write out the multipliers' DB due to an internal error.

WHAT NEXT

Contact the Synopsys Customer Support Center by sending an email message to support_center@synopsys.com.

SEE ALSO

set_svf(2)

UI-74 (Warning) Cannot use command line editor for terminal type '%s'.

DESCRIPTION

Command line editor has failed to initialize for terminal type '%s'. This can occur when terminfo database could not be found or the database does not have entry for terminal type '%s'. If this message is printed then advanced shell editing capabilities can not be used.

WHAT NEXT

Please see Design Compiler Command Line Interface Guide for more details.

UI-75 (Error) Command line length can not be more than %d characters.

DESCRIPTION

You see this message when you have typed in a long command line.

WHAT NEXT

When you enter long command with many options and arguments, you can split it across more than one line using the backslash (\) continue character.

UI-82 (error) -compress accepts only gzip or none for ddc output format.

DESCRIPTION

You receive this message when the output format is ddc and you have specified a compression format other than gzip or none. Compression is enabled by default for ddc files, so gzip normally has no effect. You may use "none" as the compression format to disable ddc compression.

WHAT NEXT

Specify gzip or none for the compression format.

UI-83 (Warning) Ignoring the cell_list parameter due to the presence of the '%s' switch.

DESCRIPTION

The switch to reset loop breaking does not need an argument.

WHAT NEXT

Consider whether the parameter was meant to be included. If the intent was to reattach a single arc, consider using remove_timing_disable. If the intent was to reset all loop breaking arcs, then the parameter is not necessary.

SEE ALSO

UI-84 (Error) The cell list is required.

DESCRIPTION

The cell list is a required parameter to the %s command, except when using the %s switch.

WHAT NEXT

SEE ALSO

UI-87 (error) ICC cannot use or check-out non Galaxy-key (legacy) license key '%s'.

DESCRIPTION

You receive this message if you attempt to check out a non Galaxy-key / legacy license key in ICC shell. ICC shell only use Galaxy-keys.

WHAT NEXT

Please consult admin or Synopsys for Galaxy-keys.

UI-88 (error) The tool is not authorized to check out the '%s' license key.

DESCRIPTION

This error occurs because the tool attempted to check out a certain license key or functionality that the tool prohibits, so the command failed. If you must run that particular functionality, please run it under the normal shell mode.

WHAT NEXT

Consider running the tool in full-mode.

UI-89 (error) ICC psyn-mode is not authorized to check out '%s' license key.

DESCRIPTION

You receive this message if you attempt to check out certain license key / functionality which is prohibited in ICC psyn. This message informs you that the command failed. If you need to run that particular functionality, please run them under normal ICC shell.

WHAT NEXT

Consider running ICC full-mode.

UI-90 (error) ICC dp-mode is not authorized to check out '%s' license key.

DESCRIPTION

You receive this message if you attempt to check out certain license key / functionality which is prohibited in ICC dp-shell. This message informs you that the command failed. If you need to run that particular functionality, please run them under normal ICC shell.

WHAT NEXT

Consider running ICC full-mode.

UI-91 (warning) No SVF file is currently open. Therefore, Formality recording cannot be turned off.

DESCRIPTION

This warning message occurs when you are running the **set_svf -off** command with an attempt to turn off Formality recording without a SVF file being currently active.

WHAT NEXT

Please check you indeed have a SVF file active prior to turning off recording. You can avoid this warning message in the future by making sure a file exists and is active for recording before using the **-off** option.

SEE ALSO

set_svf(2)

UI-92 (error) Command is not allowed in checkpointed design

DESCRIPTION

This error message occurs when you try to run commands that are not allowed on a checkpointed design. A checkpointed design is a snapshot of a design during optimization, and reoptimization on the snapshot is not allowed. Only analysis commands and non-optimization commands are allowed.

WHAT NEXT

Run only analysis or non-optimization commands

SEE ALSO

set_checkpoint_strategy(2)

UI-100 (Error) No net on pin %s.

DESCRIPTION

This error occurs because the pin specified is not connected to any net. It maybe a floating pin.

WHAT NEXT

Please check the pin list specified and the pin connections.

UI-101 (Error) Did not find any %s.

DESCRIPTION

This error message occurs when the above mentioned objects are not found.

WHAT NEXT

Please check object list specified.

UI-102 (Error) Missing or bad '%s' option.

DESCRIPTION

This error message occurs when the mentioned option is not provided or the specified argument is not in the required form.

WHAT NEXT

Please check the argument given for the option and also check the command man-page for further details about the option.

UI-103 (Error) Could not get name of %s.

DESCRIPTION

This error message occurs when the full name of the mentioned object is not found.

WHAT NEXT

Please check the object given in the command and also refer the command man-page.

UI-200 (Error) On Demand CCS library loading failed for %s: %s.

Falling back to standard mode.

DESCRIPTION

The application tried to load a db library which had CCS data and it failed to complete when making use of on demand loading of timing data. On demand loading of CCS libraries is enabled by setting of the variable **timing_ccs_load_on_demand** to TRUE.

The message will give a reason for the failure, which can be categorized as either a data error or file system error. A data error should be rare and indicates a corrupt or incompatible library. Since CCS library demand loading uses a temporary directory, a file system error will typically be due to insufficient space on the disk or permission problems.

WHAT NEXT

If library loading fails at this time, the library is still available, however, the on demand loading ability will be disabled for this library. This causes the entire CCS library to loaded at once, which can have an impact on memory usage. For a data error, you should contact the provider of the library to verify that the CCS data is specified correctly. For a file system error, check your TMPDIR environment variable and make sure you have write access to the temporary directory. Also ensure that there is sufficient space on that disk.

SEE ALSO

timing_ccs_load_on_demand(3)

UIAT-1 (error) Cannot specify %s for '%s' type.

DESCRIPTION

While defining a new user attribute, you specified (a) either or both of the options that define a range, but did not specify a data type that supports ranges, or (b) an option limiting a string type to a set of values without using a string data type.

WHAT NEXT

Ranges only work with integer and double data types. Limiting an attribute to a set of strings only works with the string data type.

UIAT-2 (error) Min of range (%s) cannot be greater than max (%s).

DESCRIPTION

While defining a new user attribute, you specified a numeric range, and the minimum value was greater than the maximum value.

WHAT NEXT

Complete ranges require that the max value is greater than min.

UIAT-4 (warning) Attribute '%s' is already defined in class '%s'

DESCRIPTION

While defining a new user attribute, you specified an attribute name that is already defined. There is no mechanism to change an attribute definition.

WHAT NEXT

UIAT-5 (warning) Cannot get attribute for more than one object.

DESCRIPTION

While getting the value of an attribute, you specified more than one object. You can only get the attribute for a single object.

WHAT NEXT

Specify a single object.

UIAT-7 (warning) Cannot import user attributes for %ss.

DESCRIPTION

While defining a new user attribute, you specified that the attribute should be imported from db files. However, the class of objects for which you are defining the attribute does not allow attributes to be imported.

WHAT NEXT

UIAT-8 (warning) Attribute '%s' is already defined as %s for another class.

DESCRIPTION

While defining a new user attribute, you specified an attribute name which is in use for another object class, but the data type which you specified was not the same as for the other object class. An attribute must have the same data type for all object classes for which it is defined.

WHAT NEXT

Determine which is the correct data type, and re-define the attribute for each affected class.

UIBS

UIBS-1 (error) No valid objects specified.

DESCRIPTION

WHAT NEXT

UIBS-2 (error) Objects must be either all ports or all nets.

DESCRIPTION

WHAT NEXT

UIBS-3 (error) Only ports of the same direction can be grouped.

DESCRIPTION

WHAT NEXT

UIBS-4 (error) Only port or net objects can be grouped.

DESCRIPTION

WHAT NEXT

UIBS-5 (error) Bus name '%s' conflicts with existing names.

DESCRIPTION

WHAT NEXT

UIBS-6 (error) All objects must be from the same design.

DESCRIPTION

WHAT NEXT

UIBS-7 (error) Type name ’%s’ conflicts with existing type.

DESCRIPTION

WHAT NEXT

UIBS-8 (error) No valid busses specified.

DESCRIPTION

WHAT NEXT

UIBS-9 (error) ’%s’ isn’t a bus.

DESCRIPTION

WHAT NEXT

UIBS-10 (error) At least one of the %s objects specified is already a member of a bus.

DESCRIPTION

WHAT NEXT

UIBS-11 (error) Cannot use sort and no_sort options in the

same command.

DESCRIPTION

The -no_sort option creates a multibit component with the cells in the same order as specified in the command. The -sort option sorts them in a lexicographically increasing order. Using both the -sort and -no_sort options simultaneously is not allowed.

WHAT NEXT

Please reissue the commands using either -sort or -no_sort.

UIBS-12 (error) Cell '%s' already belongs to a multibit component.

DESCRIPTION

A cell can belong to only one multibit component. This error gets issued when an attempt is made to insert a cell that already is a member of a multibit component into a multibit component.

WHAT NEXT

Please reissue the command without the cell specified in the error message. Alternatively, you can use remove_multibit to remove the cell from its current multibit component then reissue this command.

UIBS-13 (error) Multibit component '%s' already exists.

DESCRIPTION

Two multibit components in the same design are not allowed to have the same name. This prevents the tool from uniquely determining a multibit component from the name.

WHAT NEXT

Please reissue the command with a different name in the -name option.

UIBS-14 (warning) Set of cells specified have differing

functionality.

DESCRIPTION

The cells passed as argument to **create_multibit** are checked to verify that all of them have exactly the same functionality. This warning is issued if all cells do not have the same functionality.

A multibit component is created for the cells if none of them is a MUX_OP. If they do not share the same functionality, multibit mapping will not operate on the created component.

The references are compared on the basis of their single-bit functionality. Thus, a single-bit D flip-flop and a eight-bit wide D flop-flop will be not be considered as differing references.

WHAT NEXT

If the multibit component created is the one desired, then you can ignore this command. Otherwise, delete the created multibit component using the **remove_multibit** command, modify the set of cells passed as argument so that every cell has the same functionality, and invoke **create_multibit**.

UIBS-15 (warning) Duplicates in list of cells to create_multibit with no_sort option.

DESCRIPTION

The list of cells given as input has duplicates. The position of a multiply specified cell in the multibit component to be created is ambiguous if the -no_sort option is used with the command. The command uses the position of the first occurrence of every cell in determining the position in the multibit component.

WHAT NEXT

If the position for a cell in the created multibit component is not what was intended, remove the multibit component using **remove_multibit** and create a new one without multiply listed cells.

UIBS-16 (error) The '%s' command was not executed because

design ’%s’ could not be linked.

DESCRIPTION

The current design has to be linked in order to be able to run the **create_multibit** and **remove_multibit** commands. If the attempt to link the design fails, the command is terminated.

WHAT NEXT

Remove link errors and run the command again.

UIBS-17 (error) specified range is different from number of objects to be bussed.

DESCRIPTION

WHAT NEXT

UIBS-18 (error) At least one of the objects specified is already a member of a bus or there is conflict between the members.

DESCRIPTION

This error message is displayed if an attempt is made to insert an object that belongs to a bus into a new bus or there is conflict between the members.

WHAT NEXT

Re-issue the command with objects that do not belong to an existing bus or with objects that do not have conflicts.

UIBS-19 (error) Bus name %s conflicts with name of %s object of the design

DESCRIPTION

This error message is displayed if an attempt is made to create a bus whose name is

same as the name of the object of same type in the design.

WHAT NEXT

Re-issue the command with a different name for the bus.

UIC-1 (error) Cannot execute this command.

DESCRIPTION

No *current_design* has been specified, so the specified command cannot be executed.

WHAT NEXT

Specify a design explicitly or set the *current_design*.

UIC-2 (error) The design '%s' has no clusters.

DESCRIPTION

Attempted to execute a command which requires a design which has had associated with it clusters (via the *read_clusters* command). The design specified has no clusters.

WHAT NEXT

Try again.

UIC-3 (error) The file '%s' cannot be opened for writing.

DESCRIPTION

Attempted to execute the *write_clusters* command, but the file into which the clusters were to be written could not be opened.

WHAT NEXT

Specify a different file name, one which can be opened for writing by the command.

UIC-4 (information) No new cells were written to the file '%s'.

DESCRIPTION

In executing the write_clusters command with the *-new_cells_only* option, there were no new cells created by synthesis to report. Therefore, the PDEF file produced by **write_clusters** is an empty shell of clusters with no new instances. Such a file needn't be passed along, as it conveys no useful information to the floor-planning tool.

WHAT NEXT

Nothing needs to be done. This message merely relates that no new cells were introduced during optimization, so there is no new information to pass to the floor-planning tool via PDEF.

UIC-5 (warning) You need a DC-Expert license to compile or create wire loads using clusters.

DESCRIPTION

The **read_clusters** command and the **write_clusters** command are the interface to transfer cluster information to and from Design Compiler. To compile with clusters, you need a DC-Expert license.

WHAT NEXT

To save memory, remove the annotated clusters with **remove_clusters**.

UIC-6 (warning) The leaf cell '%s' cannot be annotated with clusters.

DESCRIPTION

The **update_clusters** command can only update the clusters associated with the **current_design** with clusters from cells which are themselves associated with designs. The cell specified is a leaf cell, and can have no clusters associated with it.

WHAT NEXT

Specify a different cell, one which has previously been characterized and which is

not a leaf cell.

UIC-7 (warning) The clusters associated with cell '%s' are not compatible with those associated with the current_design.

DESCRIPTION

The **update_clusters** command updates the clusters associated with the **current_design** by examining the clusters associated with the cells specified and seeing how they're different. The basic structure of the clusters of each cell must be a subset of the clusters associated with the **current_design**, or else it will not be clear how the clusters should be updated. In this case, a cluster was found on this cell's design which had no matching cluster on the top-level design.

WHAT NEXT

Use the **report_clusters** command to determine why differences exist between the clusters associated with the **current_design** and those associated with the cell specified.

UIC-8 (warning) Writing LOC attribute to a PDEF 1.x file.

DESCRIPTION

LOC attribute is defined only for version 2.0 and later. The current design contains LOC attributes but has PDEFVERSION attribute set to 1.x. This may either cause problems for other application or if other application ignores the LOC attributes in the PDEF file without warning the user, it may result in an unpredictable/inaccurate flow.

WHAT NEXT

The PDEFVERSION attribute on the design is set while reading in a PDEF file. The inconsistency here is mainly due to inconsistency in the original PDEF file (this application must have flagged a warning (PDEFP-22) on reading that file). Make sure that the PDEF writer that generated the file writes out correct PDEFVERSION. If you have a .db file with the PDEF information already annotated in it, you may manually modify the PDEFVERSION attribute to 2.0.

UIC-9 (warning) Can not find the reference design for cell '%s'.

DESCRIPTION

In the db, it is missing design description for this cell.

WHAT NEXT

Do report_referece to check list of refereces.

UIC-10 (warning) This %s '%s' does not have an assigned location.

DESCRIPTION

This message indicates that the defined object does not have a location assigned to it. After performing the **physopt** command or the **create_placement** command, every cell should have an assigned location. If not, this error message appears.

WHAT NEXT

Be sure you have performed the appropriate command for your design. If the error occurs again, there is a problem with the tool.

SEE ALSO

physopt (2), **create_placement** (2).

UIC-11 (warning) Original PDEF file is read but not used for identifying new cells added during reoptimization.

DESCRIPTION

You receive this message because the **pdefout_diff_original** variable is set to **false**, so the original pdef file is not used for identifying new cells. Instead, new cells added in the last run of the **reoptimize_design** command are written.

WHAT NEXT

See the man page for the **pdefout_diff_original** variable, and determine if you want to set the value of this variable to **true**.

SEE ALSO

reoptimize_design (2), **pdefout_diff_original** (3).

UIC-12 (warning) The routes in db have wire extensions which will be ignored.

DESCRIPTION

This message indicates that the internal database has wire extension values on the route segments of nets. The PDEF does not support wire extensions in its syntax. The wire extension values will be ignored by the **write_pdef**.

WHAT NEXT

You may see disconnects in the routes if you use the PDEF thus written out. You may want to consider other flow methodologies if you need the wire extensions to be in the routes.

SEE ALSO

write_pdef (2), **write_def** (2).

UID-2 (error) There are no designs to be linked.

DESCRIPTION

WHAT NEXT

UID-3 (warning) Can’t read link_library file ’%s’.

DESCRIPTION

This warning message will be printed out if the given link library file is protected or doesn’t exist. In the absense of the given library file, there will be some unresolved references during linking.

WHAT NEXT

Check the link_library and the search_path variables and set their value accordingly.

UID-4 (error) Current design is not defined.

DESCRIPTION

This error is generated when current design is not defined in the dc_shell.

WHAT NEXT

Use **list_designs** commands to see whether any design in the memory or use **read** command to read a design in. Then invoke **current_design** command to set the desired current design.

UID-5 (error) Current design ’%s’ has no schematic.

DESCRIPTION

The current design does not have a schematic.

WHAT NEXT

You can create a schematic with the **create_schematic** command. Check the man page by typing **help create_schematic**.

UID-6 (error) Technology library has not been specified.

DESCRIPTION

WHAT NEXT

UID-7 (error) Couldn’t read technology library ’%s’.

DESCRIPTION

WHAT NEXT

UID-8 (error) Technology library ’%s’ is not a library.

DESCRIPTION

WHAT NEXT

UID-9 (error) Can’t read ’%s’ files ’%s’.

DESCRIPTION

WHAT NEXT

UID-10 (error) Cannot specify output port %s as a path

startpoint.

DESCRIPTION

This error message occurs when the specified output ports are not valid as path startpoints. Output ports cannot be the startpoint for a timing path.

WHAT NEXT

Examine the design to determine the correct startpoint for the path. After correcting the startpoint, run the command again.

UID-11 (error) Cannot specify input port %s as a path endpoint.

DESCRIPTION

This error message occurs when the an input port is specified as a path endpoint. Input ports are not valid as timing path endpoints.

WHAT NEXT

Examine the design to determine the correct endpoint for the path. After correcting the endpoint, run the command again.

UID-12 (error) Cannot specify hierarchical cell %s as a path named %s.

DESCRIPTION

This error message occurs because hierarchical cell names are not valid as path startpoints or endpoints.

WHAT NEXT

Use a clock, port, leaf or hierarchical pin, or leaf cell as the path startpoint or endpoint.

UID-13 (error) ’%s’ doesn’t specify a unique design

Please use complete specification: full_file_name:design_name

DESCRIPTION

WHAT NEXT

UID-14 (error) Design ’%s’ is not in the system.

DESCRIPTION

This error indicates that the current command cannot find the design in the system.

WHAT NEXT

Provide the design in the system or load in a design.

UID-15 (error) ’%s’ doesn’t specify a unique library

Please use complete specification: full_file_name:library_name

DESCRIPTION

WHAT NEXT

UID-16 (warning) No input ports on design '%s'.

DESCRIPTION

WHAT NEXT

UID-17 (warning) No output ports on design '%s'.

DESCRIPTION

WHAT NEXT

UID-18 (error) Invalid pin list.

DESCRIPTION

WHAT NEXT

UID-19 (error) '%s' doesn't specify a unique instance

DESCRIPTION

The instance name given matches more than one instance.

WHAT NEXT

Specify a unique name for the instance you want.

UID-20 (error) Write command is not available.

DESCRIPTION

WHAT NEXT

UID-21 (error) Invalid file or design list.

DESCRIPTION

WHAT NEXT

UID-22 (error) No files or designs were specified.

DESCRIPTION

This error message is displayed when no files or design objects have been supplied to the **write** command, or when the specified files or design objects are not in memory.

WHAT NEXT

Re-issue the **write** command, correctly specifying the files or designs to be written.

UID-23 (error) Only designs can be specified with "-hierarchy

File ’%s’ is ignored.

DESCRIPTION

WHAT NEXT

UID-24 (error) No valid designs or design files were specified.

DESCRIPTION

WHAT NEXT

UID-25 (error) Write command failed.

DESCRIPTION

This error is generated when the **write** command failed. Errors include

- an invalid format (see EXPT-3), - writing to a write permission denied directory. (see UID-30) - no valid designs or design files. (see UID-24) - other causes during writing.

WHAT NEXT

Identify and correct the cause of the write command failed and reinvoke the **write** command.

UID-26 (warning) Can’t find in memory specified design or design file ’%s’.

DESCRIPTION

This error is generated when there is no specified design or design file in memory, but invoke the **write** command.

WHAT NEXT

Use **list_designs** commands to see whether given design in the memory or use **read**

command to read a design in. Then invoke **current_design** command to set the desired current design and reinvode **write** command.

UID-27 (error) '%s' doesn't specify a unique design file Please use complete path name to specify this file.

DESCRIPTION

The specified file is present in more than on directories listed in the search path.

WHAT NEXT

One possible solution is to use the complete path name to specify the file. Alternately, the search path can be modified so that only one of the directories in the path has the specified file.

UID-28 (error) Can't write design '%s', to '%s'.

DESCRIPTION

Failed to open or write to the specified file. There can be several reasons for this. The most common reasons are you do not have write permissions in the directory, the disk is full, or you already have a file with the same name that can't be deleted.

WHAT NEXT

Try to create a file with the same name from the C shell. Fix any problem that you might encounter. Make sure that there is sufficient disk space available. Delete the file and invoke the dc_shell command again.

UID-29 (error) Can't write file '%s'.

DESCRIPTION

Failed to open or write to the specified file. There can be several reasons for this. The most common reasons are: the user does not have write permissions in the directory, the disk is full or the user already has a file with the same name which can't be deleted.

WHAT NEXT

Try to create a file with the same name from the C shell. Fix any problem that you might encounter. Make sure that there is sufficient disk space available. Delete the file and invoke the dc_shell command again.

UID-30 (error) Couldn’t write specified designs to ’%s’.

DESCRIPTION

Failed to open or write to the specified file. There can be several reasons for this. The most common reasons are: the user does not have write permissions in the directory, the disk is full or the user already has a file with the same name which can’t be deleted.

WHAT NEXT

Try to create a file with the same name from the C shell. Fix any problem that you might encounter. Make sure that there is sufficient disk space available. Delete the file and invoke the dc_shell command again.

UID-31 (error) Multiple designs per file are not permitted by ’%s’ format.

DESCRIPTION

WHAT NEXT

UID-32 (error) Format ’%s’ is not a valid write format.

DESCRIPTION

This error is generated when **write** command encounters an invalid write format.

WHAT NEXT

Invoke **write** -help command for valid write formats. Identify and correct format, then reinvoke the **write** command.

UID-33 (error) LSI Netlist format is not enabled.

DESCRIPTION

The LSI Netlist format is not enabled.

WHAT NEXT

The LSI Netlist format is not enabled. Check your permissions.

UID-34 (error) TDL Netlist format is not enabled.

DESCRIPTION

The TDL Netlist format is not enabled.

WHAT NEXT

The TDL Netlist format is not enabled. Check your permissions.

UID-35 (warning) Option -add when timing_enable_multiple_clocks_per_reg is not set to true, creates the clock but analysis is not done with multiple clocks

DESCRIPTION

WHAT NEXT

Set variable timing_enable_multiple_clocks_per_reg to be true

UID-36 (error) Verilog netlist format is not enabled.

DESCRIPTION

The Verilog netlist format is not enabled.

WHAT NEXT

The Verilog netlist format is not enabled. Check your permissions.

UID-37 (error) Mentor format is not enabled.

DESCRIPTION

The Mentor format is not enabled.

WHAT NEXT

The Mentor format is not enabled. Check your permissions.

UID-38 (error) EDIF format is not enabled.

DESCRIPTION

The EDIF format is not enabled.

WHAT NEXT

The EDIF format is not enabled. Check your permissions.

UID-39 (error) Design '%s' isn't mapped.

DESCRIPTION

You are trying to write the current design to other format other than synopsys db format, but the design isn't mapped.

WHAT NEXT

Invoke compile -map_effort for mapping the current design, then reinvoke write command.

UID-40 (error) Wire load ’%s’ not found.

DESCRIPTION

WHAT NEXT

UID-41 (error) No files are specified.

DESCRIPTION

WHAT NEXT

UID-42 (error) Invalid file list.

DESCRIPTION

WHAT NEXT

UID-43 (warning) File ’%s’ was not found in the search_path.

DESCRIPTION

WHAT NEXT

UID-44 (error) Either -all or cell_list must be specified.

DESCRIPTION

WHAT NEXT

UID-45 (error) Invalid cell list.

DESCRIPTION

WHAT NEXT

UID-46 (error) No valid cells are specified for ungrouping.

DESCRIPTION

The ungroup command was called without any valid cells being specified for ungrouping.

WHAT NEXT

Call the ungroup command with a set of valid cells.

UID-47 (warning) Can’t %s unmapped logic cell ’%s’.

DESCRIPTION

Only hierarchical cells can be ungrouped. The cell mentioned in the error message is not hierarchical and so will be ignored by the ungroup command.

WHAT NEXT

No further action is required, this is merely a warning message.

UID-48 (warning) Can’t %s logic one cell ’%s’.

DESCRIPTION

Only hierarchical cells can be ungrouped. The cell mentioned in the error message is not hierarchical and so will be ignored by the ungroup command.

WHAT NEXT

No further action is required, this is merely a warning message.

UID-49 (warning) Can’t %s logic zero cell ’%s’.

DESCRIPTION

Only hierarchical cells can be ungrouped. The cell mentioned in the error message is not hierarchical and so will be ignored by the ungroup command.

WHAT NEXT

No further action is required, this is merely a warning message.

UID-50 (warning) Can’t %s cell ’%s’; its reference is unresolved.

DESCRIPTION

This error message is generated when you try to invoke a command on a cell that doesn’t have a reference.

WHAT NEXT

Use the **link** command, then reinvoke the current command.

UID-51 (warning) Can’t %s leaf cell ’%s’.

DESCRIPTION

Only hierarchical cells can be ungrouped. The cell mentioned in the error message is not hierarchical and so will be ignored by the ungroup command.

WHAT NEXT

No further action is required, this is merely a warning message.

UID-052 (warning) A non-unate path in clock network for clock ’%s’

from pin '%s' is detected.

DESCRIPTION

The clock tree for the specified clock contains non-unate paths. Clock networks normally do not contain cells such as exclusive-OR gates which have non-unate behavior. This implies that both inverting and noninverting clock waveforms reach the specified pin. The sense that is propagated from this pin is non-deterministic.

WHAT NEXT

Since there is ambiguity on which sense to choose to propagate, the tool picks one arbitrarily to propagate. If this is not acceptable, create a clock using the output of the non-unate gate as a source.

UID-53 (error) Cannot create_cell of type '%s' because the physical library cell has a non-power/ground pin '%s'. The cell type must be in the logical library for types with non-power/ground pins.

DESCRIPTION

This error occurs because you are trying to create a logical netlist cell with the wrong notation or you are using the **create_cell** command on a cell type that is only in the physical library, but has a non-power/ground pin. (In this tool, **create_cell** requires that any cell type with a non-power/ground pin be in the logical library.)

WHAT NEXT

If you are trying to create a logical netlist cell, you might have to specify a library by using the slash (/) notation; for example:

```
create_cell my_cell library_name/AND4.
```

If you are using the **create_cell** command on a cell type that is only in the physical library, but has a non-power/ground pin , add a logical library cell type to the logical library and rerun.

SEE ALSO

create_cell(2)

UID-56 (error) Read format '%s' is not supported.

DESCRIPTION

The specified read format is not supported.

WHAT NEXT

Please enter a valid read format.

UID-57 (error) No design file specified to read.

DESCRIPTION

WHAT NEXT

UID-58 (error) Cannot read file '%s'.

DESCRIPTION

This error is generated when you try to read a file which is protected or does not exist.

WHAT NEXT

Check and correct search_path, then reinvoke the read command.

UID-59 (error) Can't read '%s' file '%s'.

DESCRIPTION

This error is generated when reading a given format file unsuccessfully.

This error is generated when a file cannot be read successfully using the specified format.

WHAT NEXT

Check to make sure the correct file format is being specified and reinvoke the **read**

command. The problem persists, check the file contents.

UID-60 (error) Verilog HDL Compiler is not enabled.

DESCRIPTION

A license is not available for Verilog HDL Compiler.

WHAT NEXT

Check too see if your licenses have run out.

UID-61 (error) Invalid list of operating conditions.

DESCRIPTION

WHAT NEXT

UID-62 (error) No operating conditions were found.

DESCRIPTION

The named operating condition was not found in specified library or in any of the link libraries.

WHAT NEXT

Use the 'report_lib' command to see names of operating conditions available in your libraries.

UID-63 (warning) Operating conditions '%s' not found.

DESCRIPTION

The named operating condition was not found in specified library or in any of the link libraries.

WHAT NEXT

```
Use the 'report_lib' command to see names of operating conditions available in your
libraries.
```

UID-64 (error) Only one of: cell list, -pla, -leaf, -logic, -fsm, -hdl_all_blocks
or -hdl_bussed can be specified. -hdl_block can only be used separately
or with -hdl_all_blocks or -hdl_bussed.

DESCRIPTION

WHAT NEXT

UID-65 (error) Either cell list or -pla or -leaf or -logic must be specified.

DESCRIPTION

WHAT NEXT

UID-66 (error) No valid cells are specified for grouping.

DESCRIPTION

WHAT NEXT

UID-67 (error) A design with name '%s' already exists in the same

design file as the given design: '%s'.

DESCRIPTION

The design name you specified in the -design_name option of the 'group' command is already being used. The 'group' command needs to create a new design to represent the new level of hierarchy, so the name you specify must not conflict with existing designs in the system.

WHAT NEXT

Specify a unique design name.

UID-68 (error) A cell %s already exists in design '%s'.

DESCRIPTION

The cell name you specified in the -cell_name option of the 'group' command is already being used for another cell in the design. The 'group' command needs to create a new cell in the design to represent the new level of hierarchy, so the name you specify must not conflict with any existing cells in the design.

WHAT NEXT

Specify a unique cell name.

UID-69 (error) Except set option cannot be used with -hdl_block, -hdl_all, or -hdl_bussed option.

DESCRIPTION

WHAT NEXT

UID-70 (error) Can't find HDL block %s.

DESCRIPTION

The block name specified in the -hdl_block option of the 'group' command could not be found in the current_design. The named block needs to have been specified in the

HDL description using block labels. Block labels are separated by a backslash (/), for example, my_process/my_function.

WHAT NEXT

UID-71 (warning) No designs or libraries are available to free.

DESCRIPTION

WHAT NEXT

UID-72 (error) Only one type of object allowed.

DESCRIPTION

WHAT NEXT

UID-73 (error) Invalid %s list.

DESCRIPTION

WHAT NEXT

UID-74 (error) No valid %ss specified.

DESCRIPTION

WHAT NEXT

UID-75 (error) Unknown port '%s'.

DESCRIPTION

WHAT NEXT

UID-79 (warning) Timing options specified without -timing.

DESCRIPTION

WHAT NEXT

UID-80 (error) Illegal -path option of ’%s’.

DESCRIPTION

Valid options for -path are "short", "full", "only", "end". Type help ’report_timing’ to see a description of the options.

WHAT NEXT

Re-type command with correct options.

UID-81 (error) Illegal -delay option of ’%s’.

DESCRIPTION

Valid option strings for the -delay option are "min", "min_rise", "min_fall", "max", "max_rise", "max_fall". Type help ’report_timing’ to see a description of the options.

WHAT NEXT

Re-type command with correct options.

UID-82 (error) -max_paths cannot be negative.

DESCRIPTION

WHAT NEXT

UID-83 (information) Updating graph...

DESCRIPTION

This information message confirms that the timing graph update is in progress.

WHAT NEXT

This is only an information message. No action is required.

UID-84 (warning) Hierarchy options specified without -hierarchy.

DESCRIPTION

WHAT NEXT

UID-85 (information) Updating design information...

DESCRIPTION

This information message confirms that the design information update is in progress.

WHAT NEXT

This is only an information message. No action is required.

UID-86 (error) Could not update the design.

DESCRIPTION

```
Could not complete timing analysis because of an error.
```

WHAT NEXT

```
There should be another error message describing what went wrong.
```

UID-87 (error) Cannot read this library, it is old.

DESCRIPTION

WHAT NEXT

UID-88 (error) Invalid port list.

DESCRIPTION

WHAT NEXT

UID-89 (error) ’set_unconnected’ cannot be set on an input port ’%s’.

DESCRIPTION

WHAT NEXT

UID-90 (error) ’set_unconnected’ cannot be set on an unknown

port ’%s’.

DESCRIPTION

WHAT NEXT

UID-91 (error) ’%s’ cannot be set on an output port ’%s’.

DESCRIPTION

WHAT NEXT

UID-92 (error) ’%s’ cannot be set on an unknown port ’%s’.

DESCRIPTION

WHAT NEXT

UID-93 (error) Invalid object list.

DESCRIPTION

WHAT NEXT

UID-94 (error) ’%s’ is not a valid attribute type.

DESCRIPTION

WHAT NEXT

UID-95 (warning) Can’t find %s ’%s’ in design ’%s’.

DESCRIPTION

This error message is generated when you try to find a non existing object of a given type in the specified design or the design is hidden and so the object cannot be shown.

WHAT NEXT

Check the object by invoke report_<object>, then reinvoke the current command.

UID-96 (information) Creating new attribute '%s' on %s '%s'.

DESCRIPTION

WHAT NEXT

UID-97 (error) '%s' doesn't have an attribute '%s' type '%s'.

DESCRIPTION

WHAT NEXT

UID-98 (error) Invalid attribute type.

DESCRIPTION

WHAT NEXT

UID-99 (error) Attribute '%s' on %s '%s' is type boolean;

cannot be set to ’%s’.

DESCRIPTION

WHAT NEXT

UID-100 (warning) ’%s’ is not a valid object type.

DESCRIPTION

WHAT NEXT

UID-101 (warning) Attribute ’%s’ does not exist on %s ’%s’.

DESCRIPTION

This error message is issued by commands related to attributes of objects in a design like **get_attribute**, **remove_attribute**, or **report_attribute**. When the command does not find the given attribute, the tool prints out this warning message.

WHAT NEXT

Provide a correct attribute name for this object. If you are not sure about attribute names, do not specify this attribute.

UID-102 (warning) Ignoring %s ’%s’ type.

DESCRIPTION

This error message is issued when the type of object is not supported by the command you are running.

WHAT NEXT

Run the command with the **-help** option or check the man page of the current command for supported types of objects.

UID-103 (fatal) Synopsys database corrupted.

DESCRIPTION

WHAT NEXT

UID-104 (error) Design '%s' not found in target library.

DESCRIPTION

The design specified was not found in the target library which is specified by the variable target_library.

WHAT NEXT

Verify that the specified design is the correct one, set the correct target_library variable.

UID-105 (error) Example design '%s' is not a flip-flop.

DESCRIPTION

WHAT NEXT

UID-106 (error) Cannot determine flip-flop type of design '%s'.

DESCRIPTION

WHAT NEXT

UID-107 (warning) Multiple operating conditions specified;

only ’%s’ accepted.

DESCRIPTION

This error message is issued by the **set_operationg_conditions** command. It prints out this message when it can not process the command with multiple operating conditions. The command only accepts one of them.

WHAT NEXT

None.

UID-108 (error) Can’t find timing range ’%s’.

DESCRIPTION

The timing range specified could not be found in the specified library or in the local_link_library or link_library.

WHAT NEXT

Check that the correct timing range is specified and then check the library to make sure the timing range is present.

UID-109 (error) Can’t find %s ’%s’.

DESCRIPTION

The object of the specified type could not be found.

WHAT NEXT

Check the man page for the current command.

UID-110 (error) VHDL HDL Compiler is not enabled.

DESCRIPTION

WHAT NEXT

UID-111 (error) Can’t check security for format ’%s’.

DESCRIPTION

WHAT NEXT

UID-112 (error) ’%s’ is an invalid %s.

DESCRIPTION

WHAT NEXT

UID-113 (error) No report section specified.

DESCRIPTION

This error is issued by report_test command because there is an incorrect or missing option.

WHAT NEXT

Check the man page for report_test command.

UID-114 (warning) %s exists on port ’%s’. Cannot %s.

DESCRIPTION

This warning message is displayed when a conflict is found between a logic value that has already been set on a port and a command such as **set_logic_one**, **set_logic_zero**, or **set_logic_dc** attempting to set a different logical attribute

value. Each of these commands checks for pre-existing logic attributes, and issues this warning message when such attributes are found.

WHAT NEXT

Remove the conflicting logic attribute from the port via the **remove_attribute** or **reset_design** commands.

UID-115 (warning) '%s' is not a library cell.

DESCRIPTION

This error message is issued by the **set_prefer** command. The message is printed out when the command cannot find this cell in the target library.

WHAT NEXT

Use the **find** command to check for library cells in the target library, then reenter the **set_prefer** command with the correct library cell.

UID-117 (warning) Can't find %s '%s' in library '%s'.

DESCRIPTION

This message is issued when the current command cannot find this object in the specified library. Therefore, it does not perform the current command on this object.

WHAT NEXT

Provide the correct object in the specified library. You can use the **find** command to find objects in the library.

UID-118 (error) Port '%s' is in design '%s', but port '%s' is in design '%s'.

DESCRIPTION

This error message is displayed when ports in different designs are supplied as arguments to the **set_equal** or set_opposite command. These commands require their port arguments to be in the same design.

WHAT NEXT

Modify the arguments to only include ports on the same design and re-issue the command.

UID-119 (warning) %s '%s' is of the wrong type.

DESCRIPTION

This error message is generated when a command is called with wrong type object.

For example, the command all_connected accepts net, pin, or port object; but it is called with cell.

dc_shell> all_connected find(cell, U0) Warning: cell 'U0' is of the wrong type. (UID-119) {}

WHAT NEXT

Reinvoke the command with -help option to check for the correct type. Then recall the command.

UID-120 (error) The clock period value can't be negative.

DESCRIPTION

The clock period value specified in your command is negative. The command doesn't accept a negative clock period value.

WHAT NEXT

Provide the valid value.

UID-121 (error) Invalid timing range list; specify one or two timing range names.

DESCRIPTION

This error message is issued by the **set_timing_ranges** command. The comman accepts only one or two timing range names.

WHAT NEXT

Provide the valid timing range list.

UID-122 (error) The ’-exact’ option must be used when the example design is a latch.

DESCRIPTION

This error message is displayed when an example latch is given to the **set_register_type** command without using the command line switch ’-exact’. The **set_register_type** command requires that the ’-exact’ switch is used when specifying an example latch.

WHAT NEXT

Re-issue the **set_register_type** command using the ’-exact’ command line switch.

UID-123 (error) Can’t set flip-flop type on non sequential cell ’%s’.

DESCRIPTION

This error message is displayed because the **set_register_type** command requires that the components in the *cell_or_design_list* be valid sequential cells (latches or flip flops). Non-sequential cells are not valid arguments for the command.

WHAT NEXT

Modify the argument list so that it only includes valid sequential components.

UID-124 (error) Design ’%s’ is of "unknown" flip-flop type.

DESCRIPTION

This error message is displayed when an example flip flop given to the **set_register_type** command is not of the correct sequential type.

WHAT NEXT

Re-issue the command with a different example device.

UID-125 (error) Attribute ’%s’ can’t be %s on this %s with this command.

DESCRIPTION

WHAT NEXT

UID-126 (warning) Design ’%s’ is in state table format. Writing only port information.

DESCRIPTION

This error message is issued by the **write** command. When the command finds the design is in state table format, it writes only port information.

WHAT NEXT

None.

UID-127 (error) Can’t find library pin ’%s’.

DESCRIPTION

WHAT NEXT

UID-128 (error) No drive specified on library pin ’%s’.

DESCRIPTION

This message is issued by the **drive_of** command. The command prints out the message when it finds no drive on the specified pin.

WHAT NEXT

Provide the drive for the specified library.

UID-129 (error) Either wire load model or mode has to be specified.

DESCRIPTION

This error message is issued by the **set_wire_load** command. The command prints out this message when the wire load model or mode is missing in your current command input.

WHAT NEXT

Provide either wire load model or mode for the command.

UID-130 (error) Mode named %s is not a legal mode.

DESCRIPTION

This error message occurs if the argument to the **-mode** option of the **set_wire_load** command is not one of the recognized modes. The recognized modes are top, enclosed, or segmented.

WHAT NEXT

Check for a spelling mistake or missing argument for the **-mode** option of the **set_wire_load** command.

SEE ALSO

set_wire_load(2)

UID-131 (error) Can’t find the specified library ’%s’ in memory.

DESCRIPTION

This error indicates that the current command cannot find the specified library in the current memory database of the program.

WHAT NEXT

Check the search_path to include the path to the library. Otherwise, read in the library and rerun the command if you needs the information in the specified library to complete your work.

UID-132 (error) The write command cannot be used:
-- with the "-format %s" option
Use the "-hierarchy" option.

DESCRIPTION

For the *edif* and *vhdl* formats, there are restrictions when the design list must have only a single design. See the **write** command for details.

WHAT NEXT

Review the details in the help page for the **write** command for the format you have selected, and reissue the command either with the **-hierarchy** option or with a design list of only one design.

UID-133 (error) Attribute flag value must be either true or false.

DESCRIPTION

This error indicates the command you ran required an attribute flag value of either true or false.

WHAT NEXT

Provide the valid attribute flag value.

UID-134 (error) Clock ’%s’ is undefined for design ’%s’.

DESCRIPTION

This error indicates that the command cannot find the clock in the design.

WHAT NEXT

Provide the clock that is defined in the design.

UID-135 (error) No clock specified for remove_clock().

DESCRIPTION

This error is issued by the **remove_clock** command when a clock is missing in the command input.

WHAT NEXT

Provide the clock name for the command.

UID-136 (error) Non-boolean type in expression.

DESCRIPTION

The second argument to a filter command must be a Boolean expression which returns 1 for objects which pass the filter.

WHAT NEXT

Refer to the EXAMPLES section of the help page for **filter** and the help page for **dc_shell** for a description of Boolean expressions (also called conditional or logical expressions in some places).

UID-137 (error) Error in expression. '%c' must be followed by an attribute name.

DESCRIPTION

This error is issued by the **filter** command when the attribute is missing after the indicator in the expression.

WHAT NEXT

Provide the attribute name after the filter indicator.

UID-138 (warning) Attribute '%s' does not exist for %s '%s'.

DESCRIPTION

This error message is issued by commands related to attributes of objects in a design like **get_attribute**, **remove_attribute**, or **report_attribute**. When the command does not find the given attribute, it prints out this warning message.

WHAT NEXT

Provide a correct attribute name for this object. If you are not sure about attribute names, do not specify this attribute.

UID-139 (error) Invalid inferred bus naming style specification.

DESCRIPTION

The setting of the environment variable "bus_inference_style" is invalid, so the bussing of ports could not be inferred on the design which was read.

WHAT NEXT

Correct the setting of the "bus_inference_style" variable.

UID-140 (error) You cannot set the '%s' variable.

DESCRIPTION

The variable indicated is a derived variable. Its value is derived from some other information, so you cannot change its value directly.

WHAT NEXT

None.

UID-141 (error) Can not set -min_block_size if mode is not

"enclosed".

DESCRIPTION

Cannot use the *-min_block_size* option to **set_wire_load** without specifying *-mode enclosed*. The *-min_block_size* option makes sense only when used on a hierarchical design whose top level *-mode* is *enclosed*.

WHAT NEXT

Use *-mode enclosed* along with the *-min_block_size* option.

UID-142 (warning) Could not convert '%s' into a piece_index for library pin '%s. Using '%s' for index value instead.

DESCRIPTION

This error message is issued by the **drive_of** command when it cannot convert the piece index string for the library pin. The command uses the index value instead.

WHAT NEXT

None.

UID-143 (error) Cannot set a wire_load mode on a port. Only a wire_load model can be set on a port.

DESCRIPTION

This error message is issued by the **set_wire_load** command when it only accepts a wire_load model on a port.

WHAT NEXT

Provide the correct model to be set on a port.

UID-144 (error) %s not allowed in object_list.

DESCRIPTION

Objects of the specified type are not allowed in the command's *object_list*.

WHAT NEXT

Remove objects of the specified type from the *object_list* and try the command again. Please refer to the command's man-page for more information on the command's usage.

UID-145 (information) Truncating parameter value '%f' to '%d'.

DESCRIPTION

Some commands (and command options) only accept integer arguments. This information message informs the user that an integer is expected, but a floating-point value was supplied. As a result, the floating-point value will be truncated to the integer portion only.

WHAT NEXT

The parameter has been automatically truncated.

UID-146 (error) Invalid combination of options enabled.

DESCRIPTION

Not all options may be utilized simultaneously for certain commands. The specific combination of options that were enabled for this command was invalid.

WHAT NEXT

Please refer to the command's man-page for more information on the command's usage and valid option combinations.

UID-147 (error) Can not set a wire_load on a port

and a cluster at the same time.

DESCRIPTION

Tried to use both the port and the *-cluster* options to **set_wire_load_model** command simultaneously. The *-port* option can only be used when the wire_load is being set on a design; clusters do not have explicit ports.

WHAT NEXT

Specify either port or *-cluster*, as desired.

UID-148 (error) Cannot set a wire_load mode on a cluster.

DESCRIPTION

It does not make sense to set a *-mode* on a cluster, as mode makes sense only for a top-level design. On a cluster, it is meaningless.

WHAT NEXT

Remove the *-mode* switch from the command and run it again.

UID-149 (error) The design '%s' does not have a cluster named '%s'.

DESCRIPTION

Could not find the cluster specified in the design indicated.

WHAT NEXT

Run the **report_clusters** command to find out what clusters exist in this design, then re-execute the command which failed.

UID-150 (warning) Duplicate signals ignored.

DESCRIPTION

WHAT NEXT

UID-151 (error) Undeclared optional signals.

DESCRIPTION

WHAT NEXT

UID-152 (error) You cannot set a selection group on a port. Only a wire_load model can be set on a port.

DESCRIPTION

The **set_wire_load** command was used on a port and the **-selection_group** option was used. This combination is not valid.

WHAT NEXT

Either remove the **-selection_group** option or specify a design or cluster instead of a port.

UID-153 (error) You cannot set a selection group if the mode is not "enclosed".

DESCRIPTION

An attempt was made to use the **set_wire_load** command with the **-selection_group** option when the wire load mode was not "enclosed". This is not valid.

WHAT NEXT

Either change the wire load mode, or else do not use the **-selection_group** option.

UID-154 (error) Specified selection group '%s' not found.

DESCRIPTION

The wire load selection group name specified was not found in the user specified library or in the first library in the link library path. Therefore, it was not set on the design/cluster.

WHAT NEXT

Verify that the specified name is the correct one, specify on the command line the library which contains the selection group, or update the link library path such that the named group can be found.

UID-155 (error) Specified path group %s not found.

DESCRIPTION

This error message occurs when the specified path group name is not found. The path group must first be created with the **group_path** command.

WHAT NEXT

Verify that the specified name is correct. Use the **report_path_group** command to determine if the path group was created correctly. You can recreate the group using the **group_path** command.

SEE ALSO

group_path(2)
report_path_group(2)

UID-156 (error) Either -path_group or object list must be specified.

DESCRIPTION

This error message occurs when the **set_noise_slack_range** command requires that either a path group or a object list be specified.

WHAT NEXT

Execute the **set_noise_slack_range** command again and specify a path group with the **-path_group** option, an object list with the **object_list** option, or both a path group and an object list.

SEE ALSO

set_noise_slack_range(2)

UID-157 (error) '-to' option must be specified for bidirectional pin.

DESCRIPTION

The **set_annotated_delay** command requires that when a delay is annotated on a net from a bidirectional pin, that the load pin or pins also must be specified with the '-to' option.

WHAT NEXT

Use the '-to' option to specify the loads on the net that should be annotated.

UID-158 (warning) %s is a library. Use the find %s command.

DESCRIPTION

This warning message occurs because the **find** command in dc_shell-xg does not accept an object type cell when attempting to find a lib_cell, nor does it accept a pin when trying to find a lib_pin.

WHAT NEXT

This is a only a warning message. No action is required.

However, if this is not the result you expected, execute the **find** command again using either **find lib_cell** or **find lib_pin**.

SEE ALSO

find(2)

UID-159 (warning) Predefined methodology selected, other options ignored.

DESCRIPTION

WHAT NEXT

UID-160 (error) Pin %s is not a scan-out pin.

DESCRIPTION

WHAT NEXT

UID-161 (error) Cell %s does not have a scan-out pin.

DESCRIPTION

WHAT NEXT

UID-162 (error) Duplicate cell entries found in test routing order.

DESCRIPTION

The pin list to the **set_test_routing_order** contains some duplicates, which means the scan chain order is not well defined.

WHAT NEXT

Revise the pin list so that each pin occurs at most once. See the help page for **set_test_routing_order**.

UID-163 (error) Unrecognized test methodology %s.

DESCRIPTION

WHAT NEXT

UID-164 (error) Test report options selected without -test.

DESCRIPTION

WHAT NEXT

UID-165 (warning) Unknown test fault class, all classes will be displayed.

DESCRIPTION

WHAT NEXT

UID-166 (error) Fault report options selected without -fault.

DESCRIPTION

The **report_test** options "-class", "-incremental", and "-inst" only apply when selecting the "-fault" reporting option.

WHAT NEXT

Review the help page for **report_test**, and correct the options to the command. The most likely change is to add the "-fault" option.

UID-167 (error) Scan-chain index must be positive.

DESCRIPTION

WHAT NEXT

UID-168 (error) Non-sequential cell/reference %s can not be in a scan-chain.

DESCRIPTION

The reported cell or cell reference was in the argument list to a **set_scan_chain** command but it is not sequential. See the help page for **set_scan_chain**.

WHAT NEXT

One possibility is that the name of the cell is incorrect, such as forgetting some levels of hiearchy or a typing error, and a nonsequential cell has been selected by mistake. Either correct the name or remove it from the cell list.

UID-169 (error) Non-sequential cell/reference/design %s can not be made scannable.

DESCRIPTION

The design object list for the **set_scan** and **set_scan_element** commands must consist of sequential cells only. The indicated object is not sequential. See the help page for the command for details.

WHAT NEXT

One possibility is that the name of the cell is incorrect, such as forgetting some levels of hiearchy or a typing error, and a nonsequential cell has been selected by mistake. Either correct the name or remove it from the cell list.

UID-170 (warning) '%s' cannot be interpreted as a list of local

link library files.

DESCRIPTION

WHAT NEXT

UID-171 (warning) Design '%s' contains parameterized ECL components.
Writing this design to the '%s' netlist format will
cause a loss of parameterized information.

DESCRIPTION

WHAT NEXT

UID-172 (information) Writing synthetic library implementations for design '%s'.

Use "write -no_implicit" to get just the design.

DESCRIPTION

WHAT NEXT

UID-173 (warning) Can’t %s an uncompiled synthetic cell ’%s’.

DESCRIPTION

WHAT NEXT

UID-174 (error) Syntax error in line ’%s’.

DESCRIPTION

WHAT NEXT

UID-175 (warning) Design ’%s’ contains unmapped components.
The description might not simulate and might not be read back

into Design Compiler.

DESCRIPTION

WHAT NEXT

SEE ALSO

UID-177 (error) File ’%s’ is a directory name.

DESCRIPTION

WHAT NEXT

UID-178 (error) The ’%s’ attribute of a %s cannot be set with this command.

DESCRIPTION

WHAT NEXT

UID-179 (error) %s format is not enabled.

DESCRIPTION

WHAT NEXT

Invoke the **read** -help command for valid read formats. Identify and correct format, then reinvoke the **read** command.

UID-181 (warning) Can’t write sequential_type for %s ’%s’.

Cannot find example design in target_library.

DESCRIPTION

WHAT NEXT

UID-182 (warning) %s '%s' is of the wrong type. It seems to work but may not work in the future releases. Please fix the script.

DESCRIPTION

This error message is generated when a command is called with wrong type object. XG's backward compatibility mode for Tcl does a object search based on name, but wants to warn users to fix their Tcl scripts.

For example, the command all_connected accepts net, pin, or port object; but it is called with cell.

dc_shell-xg-t> get_clocks [get_ports A] Warning: port 'A' is of the wrong type. It seems to work but may not work in the future releases. Please fix the script. (UID-182) {}

WHAT NEXT

Reinvoke the command with -help option to check for the correct type. Then recall the command.

UID-183 (error) Unrecognized scan style '%s'.

DESCRIPTION

The specified scan style is not recognized by the **set_test_methodology** command.

WHAT NEXT

Review the help page for **set_test_methodology** for a description of the recognized styles, and correct the command.

UID-184 (error) Minimum fault coverage must be at least 80

percent.

DESCRIPTION

WHAT NEXT

UID-185 (error) Minimum fault coverage cannot exceed 100 percent.

DESCRIPTION

WHAT NEXT

UID-186 (information) Attribute ’%s’ is set on %d objects.

DESCRIPTION

WHAT NEXT

UID-188 (error) Data type ’%s’ does not match attribute type ’%s’.

DESCRIPTION

```
This error message is displayed if The data type for an attribute does not matech
predefined attribute type.
```

WHAT NEXT

```
Re-issue the command with correct data type.
```

UID-190 (error) The -design_name and -cell_name options are not used with the

-hdl_all_blocks or -hdl_bussed options.

DESCRIPTION

The **group** command has been used with conflicting options.

WHAT NEXT

Review the help page for the **group** command if necessary and change the options being used. The most likely change is to remove the use of the "-design_name" and "-cell_name" options.

UID-191 (error) The -design_name option is required unless you are using the -hdl_all_blocks, -hdl_bussed, or -hdl_block options.

DESCRIPTION

The "-design_name" option is required for the **group** command unless you have specified one of the following options: "-hdl_all_blocks", "-hdl_bussed", or "-hdl_block".

WHAT NEXT

Review the help page for the group **command if necessary, and then correct the options to your group** command.

UID-192 (error) -all_instances option must be used with instance cells when the parent instance is not unique.

DESCRIPTION

The **set_size_only** or **change_link** command has been used with conflicting options.

WHAT NEXT

Use -all_instances option together with cell instances. Either add -all_instances option to set_size_only command or uniquify the parent design instance of the cell before calling set_size_only.

UID-193 (information) %s %s for all instances of cell '%s' in subdesign '%s'.

DESCRIPTION

The **set_size_only** or **change_link** command has been applied to all instances of the cell in a design.

WHAT NEXT

UID-194 (error) -all_instances option must be used with instance cells.

DESCRIPTION

The **set_size_only** command has been used with conflicting options.

WHAT NEXT

Use -all_instances option together with cell instances. The most likely change is to add -all_instances option.

WARNING MESSAGE:

UID-195 (error) Cannot change current_design from '%s' to '%s' after Milkyway CEL has been written by IC Compiler.

DESCRIPTION

You receive this message if you are trying to change the current_design after a Milkyway CEL has already been written by IC Compiler. IC Compiler writes a Milkyway CEL automatically during **link**, **write_milkyway**, and some other commands.

Once a MW CEL is written the current_design cannot be changed to a sub-design.

WHAT NEXT

Utilize **current_design** to apply constraints, write reports, etc. without linking or writing to a Milkyway CEL. Then set the current_design to be the top-level design for physical synthesis. Perform **link** to write the Milkyway CEL and then proceed with physical synthesis commands.

You may also use **close_mw_cel** and **remove_design -all** to start again and establish a new current_design.

SEE ALSO

UID-200 (warning) Signal index values can not be negative.

DESCRIPTION

WHAT NEXT

UID-201 (warning) Cannot rename nets in buffer tree.

DESCRIPTION

When the variable **icc_track_net_names** is TRUE, IC Compiler renames the nets during **create_buffer_tree** and other optimizations so that the resulting nets have names with the same prefix as the original driving net. Note that nets touching (hierarchical) ports must have names the same as the (hierarchical) port name, so those nets cannot be renamed.

report_net_changes reports the groups of nets that are associated by being the result of the same optimization.

WHAT NEXT

Report the problem to Synopsys if it is important to have the net names in the buffer tree share the same prefix.

UID-202 (error) Design contains only combinational cells but scan style is not set to "combinational"; test patterns cannot be saved.

DESCRIPTION

You receive this message from **set_scan_configuration** if your design contains only combinational cells but the scan style is set to some value other than *combinational*. Although this condition does not prevent the **check_test** or **create_test_patterns** commands from running, **create_test_patterns** cannot save test patterns.

By default, DFT Compiler uses the scan style defined by the variable **test_default_scan_style**; the default value of this variable is *multiplexed_flip_flop*. You use **set_scan_configuration -style** to override the value of the **test_default_scan_style** variable for the current design. You have attempted to set a non-combinational scan style on a design with no sequential cell. The specification is rejected and the scan style remains unchanged.

You may specify the scan style for a design using the **set_scan_configuration -style** design. If you do not specify the scan style directly then DFT Compiler uses the default value defined in the variable **test_default_scan_style**.

WHAT NEXT

To avoid receiving this message, and to allow **create_test_patterns** to save the test patterns, explicitly set the scan style of the current design to *combinational* using the **set_scan_configuration -style combinational** command.

If you want only to run **check_test**, or if you want only to run **create_test_patterns** to analyze your design without saving the test patterns, you can ignore this message and continue.

SEE ALSO

check_test (2), **create_test_patterns** (2), **set_scan_configuration** (2); **test_default_scan_style** (3).

You can avoid this message by explicitly setting the scan style to combinational using the command **set_scan_configuration -style** combinational.

If you ignore this message, the scan style will remain unchanged. Check_test will run and report zero sequential cells. Test generation will run but will not save the vectors.

UID-207 (error) The %s command is only supported in xg mode.

DESCRIPTION

This error message occurs when the specified command is not supported in the dc_shell mode.

WHAT NEXT

Start the shell in xg mode and run your scripts again.

UID-208 (error) The cell %s is combinational. It cannot be the

startpoint or endpoint of an ignore-path for retiming.

DESCRIPTION

This error message occurs when a combinational cell is specified as the startpoint or endpoint of an ignore-path for retiming. Only ports, sequential cells, pins of sequential cells, and clocks can be startpoints and endpoints of ignore-paths for retiming.

WHAT NEXT

Use a suitable startpoint or endpoint for the path and reissue the command.

UID-209 (error) A %s license must be authorized for the set_retiming_ignore_path command.

DESCRIPTION

This error message occurs because the **set_retiming_ignore_path** command requires the authorization for the specified license.

WHAT NEXT

Check your license key file.

SEE ALSO

set_retiming_ignore_path(2)

UID-210 (error) Proprietary design ’%s’ can’t become the

current design.

DESCRIPTION

WHAT NEXT

UID-211 (warning) Can’t write proprietary design ’%s’.

DESCRIPTION

Proprietary designs cannot be written in the selected format, so the named design was skipped. This might occur for example if you try to do a hierarchical write on a design which instantiates a proprietary design.

WHAT NEXT

Normally there is nothing to do, but if the warning is unexpected, you can review the link step in case there is an problem, e.g., with the search path, which is causing a proprietary design to be linked when you were expecting a non-proprietary design.

UID-220 (error) Unrecognized test assert value ’%s’, (use one of "0","1").

DESCRIPTION

WHAT NEXT

UID-221 (error) Can’t set assume value as direction of pin %s not out/inout.

DESCRIPTION

This error message is displayed when a pin in the pin list supplied to the **set_test_assume** command is neither an output pin nor an inout pin. The **set_test_assume** command requires that all pin arguments have directions that are either ’out’ or ’inout’.

WHAT NEXT

Re-issue the **set_test_assume** command using only pins that have direction 'out' or 'inout'.

UID-222 (error) Can't set assume value as pin %s from a combinational cell.

DESCRIPTION

This error message is displayed when a pin in the pin list supplied to the **set_test_assume** command belongs to a combinational component. The **set_test_assume** command requires that none of its pin arguments are part of combinational components in the design.

WHAT NEXT

Re-issue the **set_test_assume** command without a pin list containing combinational pins.

UID-223 (error) Can't set assume value on pin %s as not test isolated.

DESCRIPTION

This error message is displayed when a pin in the pin list supplied to the **set_test_assume** command belongs to a sequential component which has not been marked as being test isolated via the **set_test_isolate** command. The **set_test_assume** command may only be used on pins of a sequential component if those pins (or their cells) have been marked as logically isolated via **set_test_isolate**.

WHAT NEXT

Remove the named pin from the argument list and then re-issue the **set_test_assume** command. Or, if it is correct to do so, use the **set_test_isolate** command on the pin or its cell, indicating that it is logically isolated and should be considered untestable during test design rule checking

UID-224 (error) Can’t set hold value as port %s is not an input.

DESCRIPTION

This error message is displayed when a port in the port list supplied to the **set_test_hold** command is not an input port. The **set_test_hold** command requires that all port arguments have direction ’in’.

WHAT NEXT

Re-issue the **set_test_hold** command using only ports that have direction ’in’.

UID-225 (error) Can’t set require value as direction of pin %s not in/out.

DESCRIPTION

This error message is displayed when a pin in the pin list supplied to the **set_test_require** command is neither an output pin nor an input pin. The **set_test_require** command requires that all pin arguments have directions that are either ’out’ or ’in’.

WHAT NEXT

Re-issue the **set_test_require** command, using only input or output pins in the list of pin arguments.

UID-226 (error) Can’t set require value as pin %s is test isolated.

DESCRIPTION

This error message is displayed when a pin in the pin list supplied to the **set_test_require** command belongs to a sequential component which has been marked as being test isolated via the **set_test_isolate** command. The **set_test_require** command may only be used on pins of a sequential component if those pins (or their cells) have not been marked as logically isolated via **set_test_isolate**.

WHAT NEXT

Remove the named pin from the argument list and then re-issue the **set_test_require** command. Or, if it is correct to do so, use the **remove_attribute** command on the pin or its cell, removing the test_isolate attribute.

UID-227 (error) Can’t set require value as pin %s from an unknown cell.

DESCRIPTION

This error message is displayed when a pin in the pin list supplied to the **set_test_require** command belongs to an unknown component. The **set_test_require** command may only be used on pins of a component which can be recognized by Design Compiler.

WHAT NEXT

Remove the named pin from the argument list and then re-issue the **set_test_require** command.

UID-228 (warning) Design has no hierarchy. No cells can be ungrouped.

DESCRIPTION

This warning message is displayed when the **ungroup** command is issued without a valid cell list, or in a design that contains no hierarchy. It indicates that without at least one valid hierarchical cell to operate on, the **ungroup** command will do nothing.

WHAT NEXT

Verify that the arguments supplied are correct, and that the design does indeed have hierarchy. Then, re-issue the **ungroup** command.

UID-229 (warning) All hierarchical cells are don’t touched. No cells can be ungrouped.

DESCRIPTION

WHAT NEXT

UID-230 (warning) All specified hierarchical cells are don’t

touched. No cells can be ungrouped.

DESCRIPTION

WHAT NEXT

UID-231 (warning) All designs specified are un-changed and not written.

DESCRIPTION

WHAT NEXT

UID-232 (information) Updating design information for flat timing report...

DESCRIPTION

WHAT NEXT

UID-233 (warning) Can’t resolve reference ’%s’ for cell ’%s’

DESCRIPTION

This error is generated when there is no design reference for the given cell.

WHAT NEXT

Check and correct the link_library and search_path. Invoke **link** command, then reinvoke the current command.

UID-234 (error) Invalid port direction '%s'.

DESCRIPTION

This error message is displayed when the **create_port** command is issued with an invalid port direction. Valid port directions for the **create_port** command are 'in', 'out', or 'inout'.

WHAT NEXT

Re-issue the **create_port** command using a valid direction argument.

UID-235 (error) Port '%s' already exists.

DESCRIPTION

WHAT NEXT

UID-236 (error) Cannot specify port_list with -unused.

DESCRIPTION

It is illegal to specify a port_list when using the "-unused" argument.

WHAT NEXT

Reissue the command either without the port list or without the "-unused" argument.

UID-237 (error) Unable to remove port '%s'.

DESCRIPTION

This error message is displayed when a port cannot be removed from a design. Ports which are bussed may not be removed individually from a design.

WHAT NEXT

Reissue the command without the named port.

UID-238 (error) The ’-associated_clock’ switch can only be used with ’clocked_on_also’ signal type.

DESCRIPTION

This error message is displayed when the **set_signal_type** command has been issued with the ’-associated_clock’ switch and the signal type being set is not ’clocked_on_also’. This is because the ’-associated_clock’ switch makes sense only in the context of defining Master and Slave clock ports with the ’clocked_on_also’ signal type.

WHAT NEXT

Re-issue the **set_signal_type** command either removing the ’-associated_clock’ switch, or changing the signal type to be ’clocked_on_also’.

UID-239 (error) Cannot run this command without the -mpc option.

DESCRIPTION

This error message is displayed when the **write_physical_script** command is called without the **-mpc** option.

The **write_physical_script** command will be enhanced in the future to print physical information other than mpc options. Always use the **-mpc** option to this command to avoid breaking the script later.

WHAT NEXT

Run the command again with the **-mpc** option.

SEE ALSO

write_physical_script(2)

UID-240 (error) Either the ’-flip_flop’ or the ’-latch’ argument

must be used.

DESCRIPTION

WHAT NEXT

UID-241 (error) Unable to find example %s '%s'.

DESCRIPTION

This error message is displayed when an example gate given to the **set_register_type** command cannot be found in the current target library. The **set_register_type** command requires that the example gate given with the '-latch' or '-flip_flop' switches exist in the target library.

WHAT NEXT

Change the target library, or change the argument given as an example gate to **set_register_type** and reissue the command.

UID-242 (error) Example design '%s' is not a %s.

DESCRIPTION

This error message is displayed when an example gate given to the **set_register_type** command is not a valid example component. The **set_register_type** command requires that the example gate given with the '-latch' or '-flip_flop' switches actually be a valid latch, or flip flop, respectively.

WHAT NEXT

Change the argument given as an example gate to **set_register_type** and reissue the command.

UID-243 (error) The %s design '%s' is of "unknown" sequential

type.

DESCRIPTION

This error message is displayed if the latch or flip-flop specified to the **set_register_type** command cannot be recognized by **Design Compiler**.

WHAT NEXT

Re-issue the **set_register_type** command with a recognizable sequential device.

UID-244 (error) Cell '%s' is a latch.
The latch type was NOT specified on the command line.

DESCRIPTION

WHAT NEXT

UID-245 (error) Cell '%s' is a flip-flop.
The flip-flop type was NOT specified on the command line.

DESCRIPTION

WHAT NEXT

UID-246 (error) Cell '%s' is neither a latch nor a flip flop.

DESCRIPTION

WHAT NEXT

UID-247 (error) Non-sequential cell/reference/design %s can

not be made transparent.

DESCRIPTION

Only level-sensitive sequential elements can be made transparent for ATPG.

WHAT NEXT

Verify that the list of devices given to the **set_scan_transparent** are all level-sensitive. The **all_registers** command can be used to get a list of such registers in the design.

UID-248 (error) The %s design '%s' is of "unknown" combinational type.

DESCRIPTION

The replacement gate in the set_combinational_type command does not have a recognized combinational function which can be used for exact replacement.

WHAT NEXT

The set_combinational_type command requires the replacement gate to have a recognized combinational function that can be used for exact replacement. Specify another gate as the replacement_gate for set_combinational_type.

UID-249 (error) Cell '%s' is not a combinational gate.

DESCRIPTION

One of the cells specified in the cell_list for set_combinational_type is not a combinational gate. All of these cells must be combinational gates. Set_combinational_type will only work on those cells in the cell list which are combinational.

WHAT NEXT

Only specify combinational cells in the cell list for set_combinational_type.

UID-250 (error) Cannot find %s '%s'.

DESCRIPTION

This error message occurs if the object of the given type and name could not be found.

WHAT NEXT

Correct the type or name of the object passed to the issued command and re-issue it.

UID-251 (error) Cannot specify both %s and %s.

DESCRIPTION

This error message is issued if a command is invoked with two incompatible options.

WHAT NEXT

Issue the command with only one of the two options displayed in the error message.

UID-252 (error) '%s' is not an instance of design '%s'.

DESCRIPTION

This error message is issued if a path to an instance does not represent a valid instance of the design.

WHAT NEXT

Correct the path to the instance and re-issue the command.

UID-253 (error) Cannot specify %s without %s.

DESCRIPTION

This error message is displayed if only one of two options, which need to be specified together, is specified.

WHAT NEXT

Specify both the options displayed in the error message and re-issue the command.

UID-254 (error) Invalid delay direction for port '%s'.

DESCRIPTION

This error message is displayed if a port argument to a command has a direction which is not valid for the command.

WHAT NEXT

Re-issue the command with ports of the required directions only.

UID-255 (error) Value for %s cannot be negative.

DESCRIPTION

WHAT NEXT

UID-256 (error) Either %s or %s must be specified.

DESCRIPTION

This error message is issued if a command is issued without one of the two mandatory options being specified.

WHAT NEXT

Re-issue the command with one of the two options in the error message.

UID-257 (error) Invalid waveform. Edges must be an even number of monotonically

increasing values less than one period in duration.

DESCRIPTION

This error message is displayed if the waveform specified for a clock is invalid. There must be an even number of numbers specifying the waveform of the clock. In addition, these numbers must be in a monotonically increasing sequence. This error message is issued if either of these rules is violated.

WHAT NEXT

Re-issue the **create_clock** command with a valid specification for the waveform.

UID-258 (error) Group weight must be between 0.0 and 100.0.

DESCRIPTION

WHAT NEXT

UID-259 (error) Must specify one of %s, %s, or %s.

DESCRIPTION

This error message is displayed if none of the three mandatory options for a command are specified.

WHAT NEXT

Re-issue the command by specifying one of the three options in the error message.

UID-260 (error) The '%s' command is obsolete. It is ignored.

DESCRIPTION

WHAT NEXT

UID-261 (error) Cannot set current instance to object '%s'.

DESCRIPTION

This error message is displayed if the **current_design** does not own the instance which is being set as the **current_instance**.

WHAT NEXT

Re-issue the **current_instance** command using an instance that is owned by the **current_design**.

UID-262 (error) '%s' doesn't specify a unique object.

DESCRIPTION

This error message is displayed if multiple objects are passed as an argument to a command that requires a single object only.

WHAT NEXT

Re-issue the command by specifying only a single object as argument.

UID-263 (error) Cannot specify multiple objects for command %s.

DESCRIPTION

This error message is displayed if multiple objects are specified as an argument to a command that requires only as single object.

WHAT NEXT

Re-issue the command with a single object as argument.

UID-264 (error) Cannot specify multiple objects.

DESCRIPTION

The error message is displayed if multiple objects are specified as an argument to a command that requires a single object.

WHAT NEXT

Re-issue the command with a single object as argument.

UID-265 (error) Cannot specify library object '%s' for command %s.

DESCRIPTION

This error message is displayed if library objects (library, library design, or library pin) are passed as an argument to a command that does not accept them.

WHAT NEXT

Re-issue the command without library objects in the argument.

UID-266 (error) Cannot specify library object '%s'.

DESCRIPTION

WHAT NEXT

UID-267 (error) Command %s cannot be performed on instance %s within a hierarchy.

Please re-issue the command in the design referenced by the

current instance.

DESCRIPTION

WHAT NEXT

UID-268 (error) Cannot perform this command on instance %s within a hierarchy.
Please re-issue the command in the design referenced by the current instance.

DESCRIPTION

WHAT NEXT

UID-269 (error) Can’t find design corresponding to instance ’%s’.

DESCRIPTION

WHAT NEXT

UID-270 (error) Can’t write script file ’%s’.

DESCRIPTION

Failed to open a script file in write mode. There can be several reasons for this. The most common reasons are: the user does not have write permissions in the directory, the disk is full or the user already has a file with the same name which can’t be deleted.

WHAT NEXT

Try to create a file with the same name from the C shell. Fix any problem that you might encounter. Delete the file and invoke the dc_shell command again.

UID-271 (error) Current instance is not defined.

DESCRIPTION

WHAT NEXT

UID-272 (error) Cannot set current design to library design '%s'.

DESCRIPTION

The current design can only be set to a non-library designs.

WHAT NEXT

check if the specified design is correct. Try specifying the complete path to the design as follows:

current_design = <db_file_name>:<design_name>

UID-273 (error) Command '%s' cannot be performed within a hierarchy.
Please re-issue the command in the design referenced by the current
instance or the top-level of the current design.

DESCRIPTION

The specified command can only be invoked from the top-level of the hierarchy. If the current instance is set to a subdesign, the command will fail.

WHAT NEXT

If you want to execute the command in the design reffered by the current instance, set the current design to point to the design current instance is pointing to. Now invoke the command. Otherwise, set current instance to the top-level design. See the man pages for commands current_design and current_instance for further details.

UID-274 (error) This command cannot be performed within a

hierarchy. Please re-issue it
in the design referenced by the current instance or the top-level of
the current design.

DESCRIPTION

The specified command can only be invoked from the top-level of the hierarchy. If the current instance is set to a subdesign, the command will fail.

WHAT NEXT

If you want to execute the command in the design reffered by the current instance, set the current design to point to the design current instance is pointing to. Now invoke the command. Otherwise, set current instance to the top-level design. See the man pages for commands current_design and current_instance for further details.

UID-275 (warning) No %s to list.

DESCRIPTION

WHAT NEXT

UID-276 (error) Can’t set current instance to leaf cell ’%s’.

DESCRIPTION

The **current_instance** command does not work on leaf cells. If you attempt to run **current_instance** on a leaf cell, you get this error.

WHAT NEXT

Make sure when you use **current_instance** the cell you specify is not a leaf cell.

UID-277 (warning) No library contain the wire load model ’%s’

set on design '%s'.

DESCRIPTION

The indicated design has a wire-load model that could not be found in the libraries in the search path. This situation can occur if the wire-load model was created with **create_wire_load**, which creates wire-load models and saves them on designs.

WHAT NEXT

To report on the specified wire load model, use **report_wire_load -name**. Here is an example of a report for a wire-load model:

```
****************************************
Report : wire loads
Design : counter
Version: v3.1-development
Date   : Mon Jan 25 10:47:24 1993
****************************************

Wire load model:   counter_wl
Location       :   counter
Resistance     :   2
Capacitance    :   1
Area           :   0
Slope          :   1.333
                              Average  Standard  % Standard
Fanout   Length   Points         Cap  Deviation  Deviation
------------------------------------------------------------
     1     0.58     1565        0.58     0.01       0.99
     2     1.46      168        1.46     0.04       2.78
     3     2.40       64        2.40     0.12       4.80
     4     3.33       56        3.33     0.15       4.59
     5     4.03       30        4.03     0.24       5.88
------------------------------------------------------------
Weighted Average Standard Deviation:                2.08


Write a technology file describing the wire-load model,
and update this file into a library on your search path
with update_lib.
Here is an example of a technology file with a
wire-load model described in the previous report:

wire_Load("counter_wl") {
resistance : 2;
capacitance : 1;
area : 0;
slope : 1.333;
fanout_length(1,0.58);
fanout_length(2,1.46);
fanout_length(3,2.4);
fanout_length(4,3.33);
```

```
fanout_length(5,4.03);
}
```

If the design still has the annotated capacitances
that were used to create the wire-load model,
use **create_wire_load -output** to write the
wire-load model directly to a technology file.

With **report_wire_load -name**, you can verify that the technology file describes the same model as the one described.

Then use **update_lib** to update the technology file into a library on your search path. The **set_wire_load_model** line in the script written can then be updated with the *-library* option to identify the library where the wire-load model can be found.

UID-278 (error) No annotated timing check information was removed.

DESCRIPTION

The timing checks defined in **remove_annotated_check** did not exist, and **remove_annotated_check** could not succeed.

WHAT NEXT

Use **report_annotated_check** to verify what timing checks are annotated.

UID-279 (error) Cannot have current_instance set for this command.

DESCRIPTION

This error message is displayed if the **current_instance** is defined. **Write_script** and **write_sdc** cannot recognize the current_instance because these commands write out information relative to the current_design.

WHAT NEXT

Re-issue the **current_instance** with no instance specified.

UID-280 (error) Period value conflicts with waveform on clock

’%s’.

DESCRIPTION

WHAT NEXT

UID-281 (warning) Path group ’%s’ has no paths; it will not affect optimization.

DESCRIPTION

The **group_path** command can be used to create or modify path groups. You can use **group_path -name clock -weight 5** to change the weight of an existing group. This warning is to let you know when you have created a path group that has no paths. This path group will not affect optimization unless paths are added to it by additional **group_path** commands.

WHAT NEXT

You should use **group_path -name clock -to clock** if you wish to include all paths to object "clock" in the path group. Use **report_path_group** to see the path groups that are currently defined.

UID-282 (information) Annotated ’%s’ delays are assumed to include load delay.

DESCRIPTION

Load delay (also known as extra source gate delay) is the portion of cell delay which is due to the capacitive load of the net being driven. Some SDF interfaces include load delay as part of the net delay - others include it as part of the cell delay. By default, Design Compiler assumes that load delay is included in cell delays.

WHAT NEXT

Make sure that you understand how both your SDF reader and writer will treat load delay. Use the -load_delay option of the read_timing, write_timing, write_constraints, or set_annotated_delay commands to specify whether Design Compiler should include load delay in cell or net delays.

UID-283 (error) Load delay location '%s' should be 'cell' or 'net'.

DESCRIPTION

Load delay (also known as extra source gate delay) is the portion of cell delay which is due to the capacitive load of the net being driven. Some SDF interfaces include load delay as part of the net delay - others include it as part of the cell delay. By default, Design Compiler assumes that load delay is included in cell delays.

WHAT NEXT

The allowable values for the -load_delay option are "cell" or "net".

UID-284 (warning) In ICC, use remove_buffer_tree instead of clean_buffer_tree.

DESCRIPTION

ICC does not support the **clean_buffer_tree** command.

Please use **remove_buffer_tree** instead.

WHAT NEXT

UID-285 (warning) '%f' value is negative.

DESCRIPTION

You receive this error message when a negative value has been specified with the **set_annotated_delay** command. Annotated delay values are usually positive, but negative delay values will be accepted.

WHAT NEXT

If you do not want the value to be negative, re-execute the **set_annotated_delay** command and specify a positive value.

UID-286 (error) Rise/fall exceptions not supported.

DESCRIPTION

You receive this error message when a **-rise_to**, **-fall_to**, **-rise_from**, **-fall_from**, **-rise_through**, or **-fall_through** option has been specified with any of the exception commands. Although these options are supported in PrimeTime, they are not supported in Design Compiler.

WHAT NEXT

Reexecute the desired command and specify the **-rise**, **-fall**, and **-through** options as necessary.

UID-290 (error) Can’t set test assertion on hierarchical object %s.

DESCRIPTION

WHAT NEXT

UID-295 (error) The command set_clock_skew is obsolete. It has been replaced by set_clock_latency, set_clock_uncertainty and set_propagated_clock commands.

DESCRIPTION

The **set_clock_skew** command has been obsoleted. The functionality has been replaced by a set of commands, which have capability beyond the set_clock_skew command had implemented.

The **set_clock_skew** command has been replaced by the following commands:

set_propagated_clock replaces the -propagated option of **set_clock_skew**

set_clock_latency replaces the -delay option of **set_clock_skew**

set_clock_uncertainty replaces the -uncertainty options of **set_clock_skew**

Example:

```
set_clock_skew -propagated -delay 1.0 -plus_uncertainty 2.1 clk
```

should be replaced as:

```
set_propagated_clock clk
 set_clock_latency 1.0 clk
 set_clock_uncertainty -hold 2.1 clk
```

WHAT NEXT

You should substitute the **set_clock_skew** command with the equivalent commands as suggested above. Please consult the man pages for **set_clock_latency** **set_clock_uncertainty** and **set_propagated_clock**.

SEE ALSO

set_propagated_clock (2), **set_clock_latency** (2), **set_clock_uncertainty** (2).

UID-296 (error) The option -cell is obsolete. Please use -lib_cell instead.

DESCRIPTION

The option **-cell** for the command **set_driving_cell** has been obsolete and will not be supported in XG mode. Please use the **-lib_cell** option instead.

WHAT NEXT

You should substitute the **-cell** option with **-lib_cell** option for all **set_driving_cell** commands. Plese refer to the **set_driving_cell** man page for detailed information on obsolete options for this command.

SEE ALSO

set_driving_cell (2).

UID-297 (error) The command set_wire_load is obsolete in XG mode.
It has been replaced by set_wire_load_model, set_wire_load_mode,

set_wire_load_selection_group, and set_wire_load_min_block_size commands.

DESCRIPTION

The **set_wire_load** command has been obsoleted in XG mode. The functionality has been replaced by a set of commands, which have capability beyond the set_wire_load command had implemented.

The **set_wire_load** command has been replaced by the following commands:

set_wire_load_model

set_wire_load_mode

set_wire_load_selection_group

set_wire_load_min_block_size

WHAT NEXT

You should substitute the **set_wire_load** command with the equivalent commands as suggested above. Please consult the man pages for **set_wire_load_model**, **set_wire_load_mode**, **set_wire_load_selection_group** and **set_wire_load_min_block_size**.

SEE ALSO

set_wire_load_model (2), **set_wire_load_mode** (2), **set_wire_load_selection_group(2), set_wire_load_min_block_size(2).**

UID-300 (error) Cannot use hdl options with the soft option.

DESCRIPTION

WHAT NEXT

UID-301 (error) 'get_attribute' can't get value for unknown

attribute type.

DESCRIPTION

WHAT NEXT

UID-302 (warning) Invalid value for link_force_case variable: default value check_reference will be used.

DESCRIPTION

WHAT NEXT

UID-303 (error) Cannot set initial value on pin %s from a non-scan cell.

DESCRIPTION

WHAT NEXT

UID-304 (error) Cannot set initial value on pin %s from an

unknown cell.

DESCRIPTION

WHAT NEXT

UID-305 (error) Period value unspecified.

DESCRIPTION

WHAT NEXT

UID-306 (error) Waveform set unspecified.

DESCRIPTION

WHAT NEXT

UID-307 (error) Waveform set must consist of two floating point values.

DESCRIPTION

WHAT NEXT

UID-308 (error) Period value cannot be zero.

DESCRIPTION

WHAT NEXT

UID-309 (error) Value for period is different from the default

value specified by test_default_period/custom test protocol.

DESCRIPTION

Period is the length of time required for each test vector cycle on a tester. Typically, only a single period is defined for a test set. Therefore, all the test clocks you created for a particular ATPG run should have same value for the period as the one specified by the test_default_period variable or in a custom test protocol.

WHAT NEXT

Omit the period specification, or specify the same value as the test_default_period variable.

UID-310 (error) Port '%s' is not an input port.

DESCRIPTION

The definition of the timing of a clock can only be applied to input ports.

WHAT NEXT

Use the **report_port** command to find the complete list of input ports. Select the correct port for applying the clock constraints. Reissue the command with the new port.

UID-311 (error) Cannot set testsim_input_delay on port '%s'. It is not an input or bidirectional port. Command ignored.

DESCRIPTION

WHAT NEXT

UID-312 (error) Cannot set testsim_output_strobe on port '%s'.

It is not an output or bidirectional port. Command ignored.

DESCRIPTION

WHAT NEXT

UID-313 (error) The specified input delay %5.2f is more than the period %5.2f. Command ignored.

DESCRIPTION

The input delay must be less than the clock period.

WHAT NEXT

The currently specified input delay has been ignored. Specify the input delay value again and ensure that the new value is less than the clock period.

UID-314 (error) The specified output strobe %5.2f is more than the period %5.2f. Command ignored.

DESCRIPTION

The output strobe must be less than the clock period.

WHAT NEXT

The currently specified output strobe value has been ignored. Specify the output strobe value again and ensure that the new value is less than the clock period.

UID-315 (error) The specified input delay %5.2f is negative. Command ignored.

DESCRIPTION

The input delay must be greater than or equal to zero.

WHAT NEXT

UID-316 (error) The specified output strobe %5.2f is negative. Command ignored.

DESCRIPTION

The output strobe must be greater than or equal to zero.

WHAT NEXT

The currently specified output strobe value has been ignored. Specify the output strobe value again and ensure that the new value is a non-negative real number.

UID-317 (error) Attribute '%s' has not been defined for %s.

DESCRIPTION

The **set_user_attribute** command requires that the attribute first be defined using either the **define_user_attribute** command or the **set_attribute** command.

WHAT NEXT

Check that the attribute name is correct and define the attribute using **define_user_attribute**, or else just use **set_attribute**.

UID-318 (error) Object class '%s' is not supported.

DESCRIPTION

The **-class** argument to the command requires a recognized object class such as design, cell, or net.

WHAT NEXT

Use the **-help** option of the command or see the command man page to find out what object classes are supported by the command.

UID-319 (error) Attribute '%s' is already defined as type %s for

object class %s.

DESCRIPTION

The attribute data type for a **define_user_attribute** or **set_attribute** command does not match the data type already defined for this attribute.

WHAT NEXT

Check the attribute name and data type against any previous attribute definitions, and correct the command.

UID-325 (warning) Option '%s' is ignored because '%s' is not specified.

DESCRIPTION

You receive this warning message because you have specified only one option with the **balance_buffer** command. You must specify both options or specify no options. The specified option is ignored.

WHAT NEXT

Reissue the **balance_buffer** command and specify both options or do not specify either option.

SEE ALSO

balance_buffer (2).

UID-326 (error) Can't find pin '%s' on cell '%s'.

DESCRIPTION

WHAT NEXT

UID-327 (warning) Arcs dont exist or have been disabled from

pin ’%s’ to pin ’%s’ on cell ’%s’.

DESCRIPTION

It is invalid to disable timing arcs between two pins where there are no arcs between the pins. Either the pins dont exist on the library cell or they have been disabled for some reason.

WHAT NEXT

UID-330 (error) ’%s’ in command get_design_parameter is not a valid parameter name for the current design. Valid parameter names are ’%s’.

DESCRIPTION

The specified parameter name in the *get_design_parameter* command is not one of the parameters for the current design.

WHAT NEXT

Check your spelling of the parameter name, or check the current design.

UID-331 (error) Parameter ’%s’ does not have a value.

DESCRIPTION

The specified parameter for the current design has not been assigned a value, and has no default value.

WHAT NEXT

Specify a default value for this parameter in the library, or *elaborate* the cell with a value for this parameter.

UID-332 (error) The -library option is only valid with the db

format.

DESCRIPTION

The *-library* option is used to write db designs into a design library.

WHAT NEXT

To store vhdl or verilog designs in a design library, use the *analyze* command. (Currently, only vhdl, verilog, and db designs can be stored in a design library.)

UID-333 (error) The -out flag cannot be used with the -library flag.

DESCRIPTION

When you write a db design into a library, the filename and path are determined from the db design name and the library name respectively. As a result, it is illegal to use the *-out* flag when the *-library* flag is specified.

WHAT NEXT

Re-issue the command, using only one of these flags.

UID-334 (error) Tried to write the root object ’%s’ into a design library.

DESCRIPTION

It is illegal to write root objects into a design library.

WHAT NEXT

On the command line, specify the individual designs that you would like to write, instead of the root object.

UID-335 (warning) The assignment operator "=" appears in the

filter string.

DESCRIPTION

The assignment operator is illegal in a filter string.

WHAT NEXT

You may have typed the assignment operator "=" in place of the comparison operator "==" (is equal to). Try the filter command again, but be sure to use "==" for comparison.

UID-336 (error) You cannot perform the command '%s' on design '%s' because it is a limited design.

DESCRIPTION

Access to a design can be limited for either of two reasons: (1) The design is fully licensed, but it has not yet been mapped. (2) The only licence that could be checked out for the design was a limited license. As a result, the internals of the design are hidden. You cannot write the design out, view a schematic, or execute any commands that would allow you to see the internals. There are also certain commands (such as group) that do not apply to limited designs.

WHAT NEXT

If the design is simply not mapped, then compiling the design will allow you access to it. If the design is limited because of licenses, then the only way to get access to the design is to check out a license that gives full access.

UID-337 (error) You cannot perform the command '%s' on design '%s' because it contains the limited design '%s'.

DESCRIPTION

Access to a design can be limited for either of two reasons: (1) The design is fully licensed, but it has not yet been mapped. (2) The only licence that could be checked out for the design was a limited license. As a result, the internals of the design are hidden. You cannot write the design out, view a schematic, or execute any

commands that would allow you to see the internals. There are also certain commands (such as group) that do not apply to limited designs.

WHAT NEXT

If the design is simply not mapped, then compiling the design will allow you access to it. If the design is limited because of licenses, then the only way to get access to the design is to check out a license that gives full access.

UID-338 (error) Cannot access design parameters on object '%s'.

Design parameter values are only valid on designs and references.

DESCRIPTION

By convention an attribute name beginning with a dollar sign ($) indicates a design parameter (i.e. VHDL generic or Verilog parameter). Design parameters only exist on design or reference objects.

WHAT NEXT

Either specify a valid design or reference, or don't use ``$'' in your attribute name. You may need to specify objects using the command *find(design, my_des)* or *find(reference, my_ref)* to insure that you are working on a design or reference.

UID-339 (warning) Can't remove attribute '%s' from object '%s'.

DESCRIPTION

You cannot remove a static or a derived attribute from this object.

WHAT NEXT

Don't try to remove a static or derived attribute.

UID-340 (error) The connection class attribute can be set only

on design ports.

DESCRIPTION

The *set_connection_class* command works only on ports that are connected to a design. You can't use this command to change the connection class attribute for ports in a library.

WHAT NEXT

To change the connection class for library ports, you need to change the text file description of the library (usually in a '.lib' file) and run Library Compiler on that library. If you intended to set the connection class for ports in a design, check that you have specified the port(s) correctly.

UID-341 (warning) Design '%s' has '%d' unresolved references. For more detailed information, use the "link" command.

DESCRIPTION

WHAT NEXT

UID-342 (error) The cell '%s' is not a synthetic library module, so set_implementation was not applied to it.

DESCRIPTION

Implementations can only be set on synthetic library modules. You cannot use set_implementation on non-synthetic library parts. You also cannot use set_implementation on synthetic library operators. It works for modules, not for operators. Use report_cell to see which cells are synthetic library modules.

This error can sometimes arise if the synthetic library in which this implementation resides has not been referred to in the link_library variable.

WHAT NEXT

Check the setting of the link_library variable to make sure it lists the synthetic library in which the module to which the cell refers resides. If not, update link_library and re-issue the set_implementation command.

If you want to set the implementation of a synthetic library operator, you can

include directives in your HDL source.

UID-343 (error) Invalid read_timing context. Valid contexts are vhdl, verilog.

DESCRIPTION

WHAT NEXT

UID-344 (warning) Can’t %s synthetic operator ’%s’.

DESCRIPTION

WHAT NEXT

UID-345 (error) The value for the ’max_levels’ argument should be
between 1 and %d for design ’%s’.

DESCRIPTION

WHAT NEXT

UID-346 (warning) The -max_levels argument is ignored when -hierarchy

option is not given.

DESCRIPTION

WHAT NEXT

UID-347 (warning) Can’t link reference ’%s’ to design ’%s’.

DESCRIPTION

WHAT NEXT

UID-348 (warning) Creating virtual clock named ’%s’ with no sources.

DESCRIPTION

This warning occurs when a virtual clock is created. A virtual clock has a name but no sources. This means it is not applied to any ports or pins in the design. A virtual clock may be used to specify input or output delay.

WHAT NEXT

The command **create_clock -period 10 -name CLK** does not apply the clock to any sources. If you want to apply the clock to a pin or port, you must specify the pin or port as in **create_clock -period 10 CLK** or **create_clock -period 10 -name CLK ff1/CP**.

UID-349 (warning) Could not read any link_library files. The

link_library setting %s may be invalid.

DESCRIPTION

WHAT NEXT

UID-350 (warning) Could not infer bus %s for design %s, because its index range does not match its width.

DESCRIPTION

WHAT NEXT

UID-351 (warning) The variable '%s' is obsolete. Use %s.

DESCRIPTION

This variable has been replaced and no longer has any effect.

WHAT NEXT

In your script, replace the setting of this variable with the new setting.

UID-352 (error) At least one argument must be specified with this command.

DESCRIPTION

This command requires at least one argument. Please refer to the man page for the command for more information.

WHAT NEXT

UID-353 (error) Arguments '%s' and '%s' are mutually exclusive.

DESCRIPTION

Some of the arguments specified in the command are mutually exclusive. Please refer to the man page for the command for more information.

WHAT NEXT

UID-354 (error) '%s' is a bad option. Please specify '%s'.

DESCRIPTION

The argument is not what is expected by the command. Please refer to the man page for the command for more information.

WHAT NEXT

UID-360 (error) Options -transparent and -user only valid when setting scan FALSE.

DESCRIPTION

WHAT NEXT

UID-361 (error) Options -transparent and -user can not both be

specified.

DESCRIPTION

WHAT NEXT

UID-362 (error) Option -transparent can not be specified with non-latch cell/design %s.

DESCRIPTION

WHAT NEXT

UID-363 (warning) Port information will be listed for the design of the current instance. This information is not used for analysis or optimization unless current_design is set to '%s'.

DESCRIPTION

Attributes on subdesign ports are not considered for timing or optimization. Only those attributes on ports at the top level (as specified by the **current_design** command) are used. The **report_port** command shows the attributes for the design of the **current_instance**, but these attributes will not have an effect unless **current_design** is used to change the top-level design.

WHAT NEXT

If you want information on the ports of the current design, use the **current_instance** command, with no arguments, before issuing the **report_port** command. If you want the information about ports for the design of the current instance, you can ignore this warning message.

UID-364 (error) The current_instance is not a unique instantiation

of design %s. Please rerun command %s after running uniquify.

DESCRIPTION

WHAT NEXT

UID-365 (error) Cell %s is not owned by the current_instance.
Only cells in the current_instance can be specified.

DESCRIPTION

WHAT NEXT

UID-366 (error) Cell %s is not owned by the current_design.
Only cells in the current_design can be specified.

DESCRIPTION

WHAT NEXT

UID-367 (error) Design %s is not referenced by any cell in current_design.
Only designs referenced in current_design can be specified.

DESCRIPTION

WHAT NEXT

UID-368 (error)
Only one design can be specified for top-down copying of

attributes.

DESCRIPTION

WHAT NEXT

UID-369 (warning)
The -all option to the link command is now obsolete.
Please add "*" at the head of your link_library variable to get this functionality.

DESCRIPTION

Make sure the astericks is in quotes when using the "*" option. A valid link_library setting is

```
link_library = {your_library.db, "*"}
```

WHAT NEXT

Use the "*" in your link_library variable instead of the -all option.

UID-370 (error) The design '%s' has clusters and cannot be modified by
the 'group' command. Use the remove_clusters command to remove the
clusters from the design first.

DESCRIPTION

The **group** command cannot be executed on a design with physical hierarchy because this would result in the hierarchical names of the design's cells changing. This situation would make it impossible for the tool that created the physical hierarchy to recognize the names.

WHAT NEXT

If appropriate, run the **remove_clusters** command to remove clusters from the design.

After the **group** command creates a new hierarchy, you may have to update your PDEF file so that the clusters in it correspond to the new logical hierarchy.

UID-371 (error) The '.' implementation can only be used with mapped synthetic modules.

DESCRIPTION

Using '.' as the implementation name locks a module to keep its current implementation. Since unmapped modules do not yet have their implementation chosen, it is impossible to know what implementation choice to lock.

WHAT NEXT

Use **compile** or **replace_synthetic** first to pick module implementations.

UID-372 (warning) No cells found to copy attributes from.

DESCRIPTION

WHAT NEXT

UID-373 (error) The specified range is different from the number of specified objects.

DESCRIPTION

WHAT NEXT

UID-374 (error)

No cells in design ’%s’ reference any of the specified designs.

DESCRIPTION

WHAT NEXT

UID-375 (error) Cannot use ’%s’ clock skew option on object ’%s’
because the ’%s’ attribute is already set on that object.

DESCRIPTION

The **rise_delay** and **fall_delay** clock skew attributes are incompatible with the **propagated_clock** attribute. In other words, the network delay to register clock pins is either determined by the delay attributes (ideal), or by evaluating the delays along the clock network (propagated). This error occurs in two situations. If there are already **rise_delay** or **fall_delay** attributes on an object, and **set_clock_skew -propagated** is used, it is an error. Also, it is an error if the **propagated_clock** attribute is present on an object when **set_clock_skew** is used with one of the following options: **-delay, -rise_delay, -fall_delay**.

WHAT NEXT

The **remove_attribute** command should be used to remove the conflicting attribute before applying the new information.

UID-376 (warning) It is dangerous to create a clock source on inout port ’%s’.

DESCRIPTION

A circuit in which a clock signal drives an inout port may be unpredictable. If the port is functioning as an output while the clock is driving, bus contention will occur. If the clock is three-stated, any registers in the clock’s fanout may lose state.

WHAT NEXT

Verify that the circuit is safe according to your design rules. DesignTime will assume that the clock is valid

UID-377 (error) Clock '%s' is not ideal. Cannot set clock transition.

DESCRIPTION

The indicated clock has a propagated clock skew. Clock transitions can only be specified for ideal clocks.

WHAT NEXT

To indicate ideal clocks, use set_clock_skew -ideal.

UID-378 (error) '%s' is not a valid format.

DESCRIPTION

The format option for the write_script command must be either dctcl or dcsh.

WHAT NEXT

Either specify a valid -format option for write_script or don't specify that option and the result will be in the same format that the shell is currently being run in.

UID-379 (error) Cannot perform %s on the instance %s because parent is not a unique instantiation of design %s. Please rerun the command after uniquifying the instance.

DESCRIPTION

You have issued the command when the parent design is not unique. This command expects the parent design to be unique to make sure that the reference of the design is consistent.

WHAT NEXT

If the instance was passed by mistake please rerun the command after fixing it. Otherwise call uniquify command with -cell option to uniquify the parent instance and rerun the command.

UID-380 (error) Invalid minimum porosity constraint, must be between 0 and 90.

DESCRIPTION

The **set_min_porosity** command sets the minimum porosity constraint on the design. The minimum porosity constraint value must be a number between 0 and 90. If set to 0, no porosity optimization will be done. The maximum porosity constraint is 90. For example, if set to 20, Design Compiler optimizes the design so that, on average, 20% of the total cell area is available for over-the-cell routing.

WHAT NEXT

Use **set_min_porosity** with a number between 0 and 90.

UID-381 (error) You are not licensed to run routability optimization.

DESCRIPTION

The **set_min_porosity** command sets the minimum porosity constraint on the design. That is, it constrains the design for a minimum over-the-cell routing area. The routing layers use the over-the-cell routing area to route the design. Design Compiler can improve the routability of designs by favoring cells with over-the-cell routing.

WHAT NEXT

To improve the routability of your design, contact your sales representative to acquire a license to run optimization.

UID-382 (warning) Setting a minimum porosity constraint to less than the default %g in link libraries.

DESCRIPTION

The **set_min_porosity** command sets the minimum porosity constraint on the design. That is, it constrains the design for a minimum over-the-cell routing area. The routing layers use the over-the-cell routing area to route the design. The porosity constraint given is less than the default minimum porosity set in the technologies libraries in the link path. **report_constraint** uses the default minimum porosity constraint specified in the link libraries.

WHAT NEXT

With **report_lib**, verify the *default_min_porosity* values in the link libraries. If necessary, set the porosity constraint to a value greater than the minimum default in the link libraries.

UID-383 (error) The porosity constraint value is less than the default %g in target libraries.

DESCRIPTION

The **set_min_porosity** command sets the minimum porosity constraint on the design. That is, it constrains the design for a minimum over-the-cell routing area. The routing layers use the over-the-cell routing area to route the design. The porosity constraint given is less than the default minimum porosity set in the technologies libraries in the target path. **compile -routability** and **reoptimize_design -routability** use the default porosity constraint from the target libraries by default.

WHAT NEXT

Verify with **report_lib** the *default_min_porosity* values in the target libraries. Set the porosity constraint to a value greater than the minimum default in the target libraries if necessary.

UID-384 (error) Invalid value specified for bus_naming_style : '%s'.

DESCRIPTION

WHAT NEXT

UID-385 (error) Invalid value specified for bus_range_separator_style %s.

DESCRIPTION

This error message occurs when you specify an invalid value for the **bus_range_separator_style** variable.

Invalid values are character strings that contain the following an odd number of % (percent symbols) followed by either the letter d or the letter s. All of the following are invalid values:

abc%%%d43
xv%ssx

WHAT NEXT

Provide a valid value for the **bus_range_separator_style** variable and reexecute the command.

SEE ALSO

create_bus(2)
bus_naming_style(3)

UID-386 (warning) The variable '%s' is now obsolete. The following, equivalent variable is being set: %s = "%s"

DESCRIPTION

This variable no longer has any effect. It has been replaced.

WHAT NEXT

Replace the setting of this variable in your script with the new setting.

UID-387 (warning) The variable '%s' is now obsolete. The following, equivalent variables are being set: %s = "%s", and, %s = "%s"

DESCRIPTION

These variables no longer have any effect. They have been replaced.

WHAT NEXT

Replace the settings of these variables in your script with the new settings.

UID-388 (error) Attribute '%s' does not exist on %s '%s'.

DESCRIPTION

The **set_attribute** command changes the value of existing attributes. If the attribute does not exist, then that attribute's value cannot be changed.

WHAT NEXT

The **set_attribute** command can be used to create a new attribute and set that attribute's value when **set_attribute** is used with the *-type* option. The *-type* option is used to specify the data type of the new attribute to be created. See the **set_attribute** manual page for more information on **set_attribute** and the *-type* option.

UID-389 (warning) Current operating conditions specify best_case_tree as the interconnect model. Annotated resistance will be ignored in this case.

DESCRIPTION

The best_case_tree model for interconnect assumes 0 interconnect delay. In this case, all annotated resistance values will be ignored.

WHAT NEXT

If best_case_tree is the desired interconnect model, then this message can be ignored. If the resistance values need to be accounted for during timing analysis, then choose a set of operating conditions which do not use the best_case_tree model to model the interconnect delay.

UID-390 (warning) All data in the names file '%s' is invalid.

DESCRIPTION

WHAT NEXT

UID-391 (error) The 'create_clock' command cannot be used on output port '%s'.

DESCRIPTION

Clock sources should be input ports or internal pins. In/out ports can be used, but they are not recommended because of bus contention issues.

WHAT NEXT

Identify a valid set of sources and reapply the **create_clock** command.

UID-392 (error) The object '%s' is a hierarchical object. You cannot set an IDDQ-invalid condition on a hierarchical object.

DESCRIPTION

Invalid IDDQ conditions must be specified in terms of logic values at ports of the design and at cell pins.

WHAT NEXT

UID-393 (error) No valid nodes specified for the set_iddq_invalid_state command.

DESCRIPTION

The 'set_iddq_invalid_state' was used without specifying a pin/port list for either the -logic_zero or -logic_one conditions. In this case the command does nothing.

WHAT NEXT

Specify a list of ports and/or leaf pins for either the -logic_one or -logic_zero conditions.

UID-394 (error) Error in command input : set_iddq_invalid_state command ignored.

DESCRIPTION

All of the pins specified for the -logic_zero or -logic_one conditions of the 'set_iddq_invalid_state' command were on hierarchical cells. Only leaf pins or ports are allowed for this command.

WHAT NEXT

Specify only leaf pins or ports for the -logic_zero and -logic_one conditions of the 'set_iddq_invalid_state' command.

UID-395 (warning) Could not link design '%s'. Therefore, the results of the filter command may be incorrect.

DESCRIPTION

The **filter** command automatically attempts to link the design before executing the filtering process. Therefore, this warning message is generated only if there were errors during the link.

If a design is not linked, some derived attributes will revert to their default values instead of having the values expected if the design were linked. Therefore, if the design cannot be linked, the **filter** command might not produce correct results.

For example, for a design that uses some sequential library cells that are not properly linked, the **is_sequential** attribute reverts to its default value of *false*, because there is no way to determine whether or not the design is sequential. This situation could occur if the design has not yet been linked, or if errors during the linking process prevent the sequential library cells from being linked properly.

Once the design is linked properly, however, then the **is_sequential** attribute maintains the correct value, and the **filter** command executes correctly.

WHAT NEXT

Resolve the link errors and then re-execute **filter**.

UID-396 (error) The cell '%s' does not reference a synthetic library operator DW03_mult_n_stage, so set_pipeline_stages was not applied to it.

DESCRIPTION

Cannot apply the 'set_pipeline_stages' command to the cell because it does not reference a synthetic library operator, DW03_mult_n_stage.

WHAT NEXT

Use report_cell to see which cells reference synthetic library operators DW03_mult_n_stage. Check the man page for the 'set_pipeline_stages' command.

UID-397 (error) You must chose one of {fixed min auto}.

DESCRIPTION

WHAT NEXT

UID-398 (warning) Pin '%s' does not belong to a cell in design '%s'.

DESCRIPTION

This warning occurs when calling cell_of command on an instance pin. The given pin belongs to a hierarchical cell of the current design.

WHAT NEXT

Set the current design to the design of that pin, then issue the cell_of command on the pin.

For example, if the message is

Warning: Pin 'U1/U2/U3/A' does not belong to a cell in design 'TOP'

cell_of can accept pins that belong to cells in the design TOP only. You are calling cell_of on an instance pin 'U1/U2/U3/A'. With this example, set current design to the design of instance 'U1/U2', then issue cell_of("U3/A");

UID-399 (error) Cannot perform %s on the instance %s because it is not unique. Please rerun the command after uniquifying the instance.

DESCRIPTION

You have issued the command when the instance is not unique. This command expects the instance to be unique to make sure that the reference of the design is consistent.

WHAT NEXT

If the instance was passed by mistake please rerun the command after fixing it. Otherwise call uniquify command with -cell option to uniquify the parent instance and rerun the command.

UID-400 (error) Design is already scan inserted, scan replaced or test ready.

DESCRIPTION

This error is generated when a design have been scan_replaced , is a test_ready or is scan_inserted. Since in all these cases the design have already been modified to have scan cells with an existing scan style, Hence it is not possible to change the scan style now.

WHAT NEXT

You can re read the design and set the new scan style and repeat the old flow to take into account the new scan_style.

UID-401 (warning) Design rule attributes from the driving cell will be set on the port.

DESCRIPTION

Design rule attributes from the driving cell will be set on the port when the set_driving_cell command is used. This is in addition to timing related parameters that are set on the port.

WHAT NEXT

Use the -no_design_rule option for set_driving_cell to avoid having design rules inferred.

UID-402 (warning) Specifying an input delay without an associated clock
can cause the port's timing to be analyzed incorrectly.

DESCRIPTION

If a port input delay is specified without reference to a clock, a default clocking waveform is inferred for the port's drivers, based on the flip-flops and latches in the port's transitive fanout. The input data will be assumed to be coming from an edge-triggered flip-flop clocked by the inferred waveform. The program attempts to figure out what the appropriate clock waveform should be, but there is no guarantee that the inferred clock will be appropriate for all cases. Therefore, it is safer to explicitly specify the clock whenever you set an input delay.

WHAT NEXT

To avoid having default clocks inferred, use the -clock option with set_input_delay. In some cases, the -level_sensitive and -clock_fall options might also be needed.

UID-403 (error) Can't read in the DB file '%s'.
File '%s' is created using program version '%s'
which is newer than '%s'.

DESCRIPTION

This error indicates that your db file is created using Synopsys program version which is newer than the current program.

WHAT NEXT

Check your db file, make sure it is created with Synopsys product whose version is not newer than the current program you are using.

UID-404 (error) No setup or hold margin was specified.

DESCRIPTION

Because no setup or hold margin was specified, no clock gating checks will be created.

WHAT NEXT

To specify margins for the clock gating checks, use the **-setup** or **-hold** options.

UID-405 (error) The set_auto_ideal_nets command is obsolete. Use set_auto_disable_drc_nets instead.

DESCRIPTION

Ideal nets are now defined as having ideal timing (zero latency and transition by default), no DRC checking, and **dont_touch** attributes set on them. The now-obsolete **set_auto_ideal_nets** command was not consistent with this definition of ideal, and has therefore been renamed to **set_auto_disable_drc_nets**. This command works in exactly the same way as **set_auto_ideal_nets**; it accepts the same arguments and by default disables DRC on clock and constant nets.

WHAT NEXT

Replace this command with the **set_auto_disable_drc_nets** command. Alternatively, if you want to set nets to be ideal, use **set_ideal_net** or **set_ideal_network** instead.

SEE ALSO

set_auto_disable_drc_nets (2), **set_ideal_net** (2), **set_ideal_network** (2).

UID-406 (information) set_ideal_net disables DRC, sets dont_touch on the net, and makes its timing ideal.

DESCRIPTION

This message informs you about the current behavior of the **set_ideal_net** command. Since release 2001.08, ideal nets are defined as having ideal timing (zero latency and transition by default), no DRC checking, and **dont_touch** attributes set on them. The previous behavior of the **set_ideal_net** command was only to switch off DRC checking for the net. To revert to the previous behavior, set the variable

use_old_ideal_net to true.

WHAT NEXT

This is an informational message only. No action on your part is required.

SEE ALSO

set_ideal_net (2), **set_ideal_network** (2); **use_old_ideal_net** (3).

UID-408 (warning) Current design named %s is hidden.

DESCRIPTION

This warning message occurs only in Incremental Mode.

You receive this warning message if the current design is hidden, either by a limited license or by a don’t show reference.

Access to a design can be limited for either of the following reasons:

• The design is fully licensed, but it has not yet been mapped.

• The only license that could be checked out for the design was a limited license.

The result of limited access is that the internals of the design are hidden. You are not permitted to write the design out, view a schematic, or execute any commands that would allow you to see the internals. Certain commands, such as the **group** command, do not apply to limited designs.

WHAT NEXT

This is a warning message only. No action is required.

However if the result is not what you intended, you can do one of the following:

• If the design is not mapped, compile the design.

• If the design is limited because of licenses, check out a license that allows full access.

After making your changes, you can reexecute the command that issued this warning message.

SEE ALSO

set_design_license(2)

UID-409 (error) Cannot group the cell %s because its parent is not %s.
Only cells whose parents are same can be grouped.

DESCRIPTION

You have issued the command when the cells passed to group command have different parents. This command expects all the cells to have the same parent.

WHAT NEXT

Please rerun the command after fixing the error.

UID-410 (error) Unable to find replacement gate '%s'.

DESCRIPTION

The replacement gate specified in the set_combinational_type command could not be found in the target library.

WHAT NEXT

Either change the target_library variable to include the library which contains the replacement gate or change the replacement gate.

UID-411 (error) Replacement design '%s' is not a combinational gate.

DESCRIPTION

The replacement_gate in the set_combinational_type command is not a combinational gate.

WHAT NEXT

Set_combinational_type must have a combinational gate as its replacement gate. Specify a new replacement gate.

UID-412 (warning) Overriding compile directives for cell %s.

DESCRIPTION

The compile directives set by the **set_compile_directives** command are ignored for this cell. The **set_combinational_type** command must override the compile directives to ensure that this cell is only translated into the given replacement cell.

WHAT NEXT

Do not use **set_combinational_type** and **set_compile_directives** on the same cell.

UID-413 (warning) Overriding previous replacement cell for cell %s.

DESCRIPTION

There was a previous **set_combinational_type** command issued for this cell. The old command is ignored.

WHAT NEXT

The **set_combinational_type** overrides any previous **set_combinational_type** commands issued for this cell.

UID-414 (error) Cannot set_compile_directives on cell %s because it already has set_combinational_type

DESCRIPTION

There was a previous **set_combinational_type** command issued for this cell. You cannot **set_compile_directives** for the same cell because the **set_combinational_type** command needs to ensure that this cell is only translated into the particular replacement cell.

WHAT NEXT

Remove the **set_combinational_type** information by doing a remove_attribute <cell_name> combinational_type_exact.

UID-415 (error) Cell list contains generic cell %s.

DESCRIPTION

The **set_compile_directives** command has been called on a list of cells containing generic cells .

WHAT NEXT

Use **set_compile_directives** only on list of technology specific cells.

UID-416 (warning) The compile directive given by option %s had already been %s on all specified cells.

DESCRIPTION

A **set_compile_directives** command option has no effect because the corresponding directive had already been set for the specified cells.

WHAT NEXT

Check if the options of **set_compile_directives** are set correctly. Note that the default is TRUE.

UID-417 (error) Cell list contains synthetic operator cell %s.

DESCRIPTION

The **set_compile_directives** command has been called on a list of cells containing synthetic operators.

WHAT NEXT

Use **set_compile_directives** only on list of technology specific cells.

UID-418 (error) Cell list contains cell %s which is control logic of

SELECT_OPs.

DESCRIPTION

The **set_compile_directives** command has been called on a list of cells containing control logic of SELECT_OPs.

WHAT NEXT

Use **set_compile_directives** only on list of technology specific cells.

UID-420 (error) %s cannot be used on port with clock specified.

DESCRIPTION

WHAT NEXT

UID-421 (error) bc_dont_ungroup cannot be applied after the current design is scheduled.

DESCRIPTION

You receive this message if you attempt to use **bc_dont_ungroup** after the current design is scheduled. Currently, you must use **bc_dont_ungroup** before scheduling the current design.

WHAT NEXT

Apply **bc_dont_ungroup** before scheduling your design.

SEE ALSO

bc_dont_ungroup (2), **schedule** (2).

UID-422 (error) get_timing_paths requires a mapped design.

DESCRIPTION

You receive this error message if you attempted to use **get_timing_paths** with an unmapped design. You cannot generate a timing report for an unmapped design because the correct timing arcs are not available.

WHAT NEXT

Compile your design using the **compile** command before executing **get_timing_paths**.

SEE ALSO

compile (2), **get_timing_paths** (2).

UID-423 (error) Invalid path group name %s supplied with -group option.

DESCRIPTION

This error message occurs if you specify a non-existent path group name when using the **-group** option with the **report_timing** command.

WHAT NEXT

Specify a valid (existing) path group name when using the **-group** option and then run the **report_timing** command again.

Path groups are created implicitly according to the clock of the destination register of a path. You can also define a path group with via the **group_path** command. To see a list of all valid path groups, issue the **report_path_group** command. Any of the path group names listed can be supplied with the **-group** option in the **report_timing** command.

SEE ALSO

group_path(2)
report_path_group(2)
report_timing(2)

UID-424 (warning) The min ideal latency is greater than the max ideal latency

for the object '%s'. Using the latest value for both min and max.

DESCRIPTION

You receive this message because you set the minimum ideal latency higher than the maximum ideal latency for the specified object. The max ideal latency must be greater than or equal to the min ideal latency for the same object. The message informs you that the latest value entered is being used for both minimum and maximum ideal latency.

WHAT NEXT

If it is acceptable to you for the latest value to be used for both minimum and maximum ideal latency, no action is required on your part. However, if you want different values for the minimum and maximum ideal latency, reset these values using the **set_ideal_latency** command, and ensure that the maximum value is greater than or equal to the minimum value.

SEE ALSO

set_ideal_latency (2).

UID-425 (warning) You cannot set ideal latency on object %s, f because it is not a pin of a leaf cell or a port of the current design.

DESCRIPTION

You receive this message if you attempt to set an ideal latency on an object that is not a pin of a leaf cell (a cell that does not contain other cells), or a port of the current design. You can set an ideal latency only on leaf cell pins or top-level ports.

WHAT NEXT

Reexecute the **set_ideal_latency** command with an *object_list* that contains only leaf cell pins and/or top-level ports.

SEE ALSO

set_ideal_latency (2).

UID-426 (warning) You cannot set ideal transition time on object %s,
because it is not a pin of a leaf cell or a port of the current design.

DESCRIPTION

You receive this message if you attempt to set an ideal transition time on an object that is not a pin of a leaf cell (a cell that does not contain other cells) or a port of the current design. You can set an ideal transition time only on leaf cell pins or top-level ports.

WHAT NEXT

Reexecute the **set_ideal_transition** command with an *object_list* that contains only leaf cell pins and/or top-level ports.

SEE ALSO

set_ideal_transition (2).

UID-427 (warning) The clock source '%s' has ideal timing specified,
but the clock was just created as an ideal clock.
Ignoring previously-specified ideal timing for this clock source.

DESCRIPTION

You receive this message from the **create_clock** command to warn you that the specified clock source has ideal timing previously specified. Clocks created by the **create_clock** command are ideal clocks, which ignore ideal timing. This message warns you that the previously-specified ideal timing is being ignored for the specified clock source.

An ideal clock uses latency and transition specified by **set_clock_latency** and **set_clock_transition** and ignores an ideal timing. Therefore, you cannot use the **set_ideal_latency** and **set_ideal_transition** commands on this ideal clock.

WHAT NEXT

If it is acceptable to you that the previously-specified ideal timing is ignored for this clock, no action is required on your part. Otherwise, verify that the specified

clock source was the one you intended to use for creating an ideal clock. If so, and if you want to set latency and transition time on the ideal clock, use the **set_clock_latency** and **set_clock_transition** commands.

SEE ALSO

create_clock (2), **set_clock_latency** (2), **set_clock_transition** (2), **set_ideal_latency** (2), **set_ideal_transition** (2).

UID-428 (warning) You cannot set an ideal latency on the clock source %s, because it is an ideal clock. Ignoring the specified ideal latency.

DESCRIPTION

You receive this message if you attempt to set an ideal latency on a clock source created using the **create_clock** command. Clocks created using **create_clock** are ideal clocks, and you cannot set an ideal latency on an ideal clock. Instead, to set its latency, use the **set_clock_latency** command.

WHAT NEXT

If it is acceptable to you that the ideal latency is ignored for the specified ideal clock, no action on your part is required. Otherwise, if you want to set latency on the clock, do so using the **set_clock_latency** command.

SEE ALSO

create_clock (2), **set_clock_latency** (2), **set_ideal_latency** (2).

UID-429 (warning) You cannot set an ideal transition time on the clock source %s, because it is an ideal clock. Ignoring the specified ideal transition time.

DESCRIPTION

You receive this message if you attempt to set an ideal transition time on a clock source created using the **create_clock** command. Clocks created using **create_clock** are

ideal clocks, and you cannot set an ideal transition time on an ideal clock. Instead, to set its transition time, use the **set_clock_transition** command.

WHAT NEXT

If it is acceptable to you that the ideal transition time is ignored for the specified ideal clock, no action on your part is required. Otherwise, if you want to set a transition time on the clock, do so using the **set_clock_transition** command.

SEE ALSO

create_clock (2), **set_clock_transition** (2), **set_ideal_transition** (2).

UID-430 (error) No object was specified for the **set_clock_uncertainty** comand.

DESCRIPTION

The clock uncertainty can be specified on a clock a clock or a clock pin. You can also specify inter-clock uncertainty by using the **-from** and **-to** to specify from which clock to which clock to apply this uncertainy. The **rise_delay** and **fall_delay** clock skew The source clock latency is the time it takes for a clock signal to propagate from its actual ideal waveform origin point to the clock definition point in the design. This attribute can be set on a clock source, or on the clock itself. In case it is set on the clock, it is applied to all the clock sources.

WHAT NEXT

Reapply the command with the relevant object(s).

UID-431 (error) -to clock_name is missing.

DESCRIPTION

This error message occurs when a required clock name is not specified. To set interclock uncertainty, specify a **-from** *from_clock* and **-to** *to_clock* pair. Use the **-from** and **-to** options only for interclock uncertainty.

To set uncertainty on a clock or a clock pin, specify the object name at the end of the command line.

WHAT NEXT

Run the command again using the correct options.

SEE ALSO

set_clock_uncertainty(2)

UID-432 (error) -from clock_name is missing.

DESCRIPTION

This error message occurs when the required clock name is missing. To set interclock uncertainty specify both the **-from** *from_clock* and **-to** *to_clock*>. The **-from** and **-to** option are used only for interclock uncertainty.

To set uncertainty on a clock or a clock pin, specify the object name at the end of the command line.

WHAT NEXT

Rerun the command using the correct options.

SEE ALSO

set_clock_uncertainty(2)

UID-433 (error) Too many objects for inter clock uncertainty.

DESCRIPTION

To set inter-clock uncertainty use **-from** <from_clock> and **-to** <to_clock> option. To set uncertainty on a clock or a clock pin, just specify the object name at the end of the command line. These 2 different types of clock uncertainty values cannot be set in one command line.

WHAT NEXT

Reapply the command(s) with the correct options.

UID-434 (error) '%s' is not a name of a clock.

DESCRIPTION

To specify inter-clock skew the **-from** and **-to** options should be followed by a clock name. To specify a skew to a register, the object should be specified without the **-from** and **-to** option.

WHAT NEXT

Reapply the command with the correct syntax.

UID-435 (error) Cannot set clock source latency on '%s' .This attribute can be set on a clock or a clock source pin.

DESCRIPTION

The source clock latency is the time it takes for a clock signal to propagate from its actual ideal waveform origin point to the clock definition point in the design. If you receive this message, you have attempted to set clock source latency on an object other than a clock or a clock source pin. This attribute can be set on a clock source, or on the clock itself. If it is set on the clock, the attribute is applied to all clock sources.

WHAT NEXT

If you want to set clock source latency, you need to identify the relevant clock or clock source where you want to set it. If you want to set actual latency on a clock pin, use the **set_clock_latency** command without the **-source** option.

UID-436 (error) '-rise' and '-fall' options are valid only for inter-clock uncertainty

DESCRIPTION

You receive this message if you attempt to specify **-rise** and **-fall** options for an endpoint uncertainty; you can specify only one value for the setup check and one value for the hold check. The value is applied to both the rise and the fall transition. The **-rise** and **-fall** options are valid only for inter-clock uncertainty.

WHAT NEXT

Reapply the command with the correct syntax.

UID-437 (warning) '%s' option is obsoleted. Although it will still function normally now, please use '%s' command to replace this

option in the future.

DESCRIPTION

The specified option is obsolete, although it is still functional in the current software version. In the future, please use the replacement command.

WHAT NEXT

Replace the obsolete option with the specified command.

UID-438 (warning) Attribute '%s' is removed from from object '%s'.

DESCRIPTION

The command executed caused the specified attribute to be removed from the specified object, either because the command must proceed without this attribute, or because the value of the attribute is invalid for this command.

WHAT NEXT

This message is for your information. No action is required on your part.

UID-439 (warning) '%s' command is obsoleted. Although it will still function normally now, please use '%s' command to replace this command in the future.

DESCRIPTION

DC is obsoleting this command. However, it is still functional in this version. In the future, please use the replacement command.

WHAT NEXT

Remove the obsolete commands, and replace it with the new command.

UID-440 (error) Can’t write constraints file ’%s’.

DESCRIPTION

Failed to open a script file in write mode. There can be several reasons for this. The most common reasons are: the user does not have write permissions in the directory, the disk is full or the user already has a file with the same name which can’t be deleted.

WHAT NEXT

Try to create a file with the same name from the C shell. Fix any problem that you might encounter. Delete the file and invoke the dc_shell command again.

UID-441 (warning) You cannot specify an input transition time for the %s ’%s’ using set_input_transition. Ignoring the transition time for this port.

DESCRIPTION

You receive this message if you specify an input transition for the specified ideal network port or ideal clock source, using **set_input_transition**. You cannot use **set_input_transition** for these objects; you must use **set_ideal_transition** for ideal network ports, and **set_clock_transition** for ideal clock sources. This message informs you that the input transition specified by **set_input_transition** is being ignored for the specified object.

WHAT NEXT

If it is acceptable to you that the input transition time is ignored, no action is required on your part. Otherwise, if you want to set an input transition time, use **set_ideal_transition** for an ideal network port and **set_clock_transition** for a clock source.

SEE ALSO

set_clock_transition (2), **set_ideal_transition** (2), **set_input_transition** (2).

UID-444 (error) ’%s’ is a PrimeTime option that is not supported

by Design Compiler.

DESCRIPTION

Although this option is supported by PrimeTime, Design Compiler does not currently support this option. You can check which option is supported by Design Compiler by executing "*command* -help" in **dc_shell**.

WHAT NEXT

Remove the option that is not supported.

UID-445 (warning) Ignoring %s objects in collection '%s' because they are not of type %s.

DESCRIPTION

You receive this error message when you specify a collection as an argument to a command, and some objects in the collection are not of a type accepted by the command. For example, you receive this error message if you execute the **report_net** command and not all of the objects in the specified collection are nets.

WHAT NEXT

Use the command **query_objects -verbose** to see the details of the objects in the collection and their types.

UID-446 (Error) For pattern '%s', %s.

DESCRIPTION

A problem has occured while trying to compile the regular expression pattern shown.

WHAT NEXT

Review the description in the man page for regexp to identify and correct the problem. Make sure that you intended the pattern to be a regular expression instead of a simple string match. A common mistake is to mix up the use of the wildcard '*' in string match with the corresponding regular expression '.*'. Also, remember that in regular expressions, the square brackets '[', ']' by default enclose a range of characters, and must be escaped with a backslash to be treated as regular characters.

UID-447 (warning) Your SDC output may contain ambiguous names because you have set the variable sdc_write_unambiguous_names to FALSE.

DESCRIPTION

Beginning with version 1.2, the Synopsys Design Constraints (SDC) format has features which ensure that the cell, net, pin, lib_cell, and lib_pin names written to the file are unambiguous. Some third party applications do no understand these features, and to suppress them, you set the variable **sdc_write_unambiguous_names** to FALSE. This warning reminds you that the setting of this variable may cause your SDC output to be ambiguous.

WHAT NEXT

Verify that you really want to disable the writing of unambiguous names. Review the man pages for **write_sdc** and **sdc_write_unambiguous_names**.

UID-448 (warning) The sdc version specified is not valid. Valid options are 1.2, 1.3, 1.4, 1.5, and latest.

DESCRIPTION

You receive this message if you specify an invalid version with the **-version** option of **write_sdc**. Valid values for **-version** are 1.2, 1.3, 1.4, 1.5, and latest (the default). Notice that in this case, specifying latest or 1.5 are equivalent, as is issuing **write_sdc** without the **-version** option.

WHAT NEXT

Reexecute **write_sdc** and either specify a valid version with the **-version** option, or omit the **-version** option and get the latest version.

SEE ALSO

write_sdc (2).

UID-449 (warning) The sdc version specified is not valid for db

mode. Valid options are 1.2, 1.3, 1.4, and latest.

DESCRIPTION

You receive this message if you specify an invalid version with the **-version** option of **write_sdc**. When in DB mode the valid values for **-version** are 1.2, 1.3, or 1.4. Notice that in this case, specifying 1.4 is equivalent to issuing **write_sdc** without the **-version** option.

WHAT NEXT

Reexecute **write_sdc** and either specify a valid version with the **-version** option, or omit the **-version** option and get the latest supported version.

SEE ALSO

write_sdc (2)

UID-450 (Warnning) Value for %s is negative.

DESCRIPTION

A negative value was given in the command line; the value was accepted.

WHAT NEXT

It is the user’s responsibility to verify that the negative value is a valid value to describe this property.

UID-451 (Warnning) ’%s’ option is ignored when ’%s’ argument is present.

DESCRIPTION

The given option is ignored to the current command when the specified argument is present. The command performs without the given option.

WHAT NEXT

UID-452 (Warning) Empty object list.

DESCRIPTION

You receive this message if you execute the **report_net_fanout** command with an empty pair of braces ({}) for the *net_list* argument, or with all members of *net_list* invalid. This condition could be caused by spelling errors or typos, or by listing nets for the wrong instance.

WHAT NEXT

If you want **report_net_fanout** to generate the report for all nets in the current instance, execute the command without the optional *net_list* argument. Otherwise, verify that the net list is correct for the current instance and that the names are spelled correctly. Then reexecute the **report_net_fanout** command.

SEE ALSO

report_net_fanout (2).

UID-453 (error) The argument of the -bound option must be larger than the argument of the -threshold option.

DESCRIPTION

You receive this message if you execute the **report_net_fanout** command and specify a value for the **-bound** option that is smaller than or equal to the value for the **-threshold** option. The **-bound** option represents the upper level of fanout for displaying nets, while the **-threshold** option represents the lower level. Therefore, the value of **-bound** must be larger than the value of **-threshold**.

WHAT NEXT

Reexecute the **report_net_fanout** command and specify a value for the **-bound** option that is larger than the value for the **-threshold** option.

SEE ALSO

report_net_fanout (2).

UID-455 (error) The value %s is not a legal option for the set_transform_for_retiming command.

DESCRIPTION

The **set_transform_for_retiming** command can only have the values **-multiclass**, **-decompose**, or **-dont_retime**.

WHAT NEXT

Check the spelling and choose either the **-multiclass**, **-decompose** or **-dont_retime** option for the **set_transform_for_retiming** command.

UID-456 (error) The value %s is not a legal option for the set_state_for_retiming command.

DESCRIPTION

The comand **set_state_for_retiming** can only have the values **-preserve** or **-dont_care**.

WHAT NEXT

Check the spelling and specify the **-preserve** or **-dont_care** option for the **set_state_for_retiming** command.

UID-457 (error) Cannot set size_only on cell '%s'.

DESCRIPTION

The **set_size_only** command works only on leaf cells.

WHAT NEXT

When you use **set_size_only**, make sure the cell you specify is a leaf cell.

UID-458 (warning) Cannot perform '%s' on object '%s' because

it is not a port.

DESCRIPTION

The specified object is not a port. The command cannot be applied.

WHAT NEXT

UID-459 (warning) Cannot perform '%s' on object '%s' because it is not a port.

DESCRIPTION

The specified object is not a port. The command can not be applied.

WHAT NEXT

Varify that the specified object is not a port.

UID-460 (error) Option '%s' is only available for dc_shell-t.

DESCRIPTION

The indicated option is only available in Tcl mode (dcshell-t).

WHAT NEXT

Start dc_shell as dc_shell-t or dc_shell -tcl_mode.

UID-461 (error) The -xg_mode option is not available.

DESCRIPTION

This error message occurs when the **-xg_mode** option is not available for the current release, or when there is a problem with accessing proper license features.

WHAT NEXT

Start dc_shell without using the **-xg_mode** option.

UID-462 (error) Invalid implementation '%s' for cell '%s'.

DESCRIPTION

The specified implementation for the synthetic cell does not exist in the specified synthetic libraries.

WHAT NEXT

Verify the existence of the specified implementation in the synthetic libraries. You can use the report_synlib command to list the contents of the synthetic library.

UID-463 (error) %s name is required to set implementation on operator '%s'.

DESCRIPTION

Either module name or implementation name is missing when setting implementation on operator.

WHAT NEXT

Reissue the **set_implementation** command with the implementation string that contains the module name and implementation name in the "<module_name>/<impl_name>" format.

UID-464 (error) Invalid module '%s' or implementation '%s' for cell '%s'.

DESCRIPTION

The specified module name or implementation name on operator cell does not exist in the synthetic libraries.

WHAT NEXT

Verify the existence of the specified implementation in the synthetic libraries. You

can use the report_synlib command to list the contents of the synthetic library.

UID-465 (error) Incorrect arguments to the set_retiming_bound command. Choose either the -forward or -backward option to specify the direction of the retiming_bound.

DESCRIPTION

This error message occurs because the **set_retiming_bound** command can only have the value of **-forward** or **-backward**.

WHAT NEXT

Check the spelling and rerun the **set_retiming_bound** command with either **-forward** or the **-backward**.

SEE ALSO

set_retiming_bound(2)

UID-466 (error) Missing arguments to command **set_retiming_bound**. Specify the direction of the retiming_bound using the -forward or -backward option.

DESCRIPTION

This error message occurs because the **set_retiming_bound** command requires either the **-forward** or **-backward** option to specify the direction that the registers move.

WHAT NEXT

Rerun the **set_retiming_bound** command with either **-forward** or **-backward**.

SEE ALSO

set_retiming_bound(2)

UID-467 (error) The '%s' option is not supported in Design

Compiler.

DESCRIPTION

This error message occurs when the specified option is not supported by Design Compiler.

WHAT NEXT

Rerun the command without the option.

SEE ALSO

report_qor(2)

UID-468 (warning) The ’%s’ option is not supported in Design Compiler and will be ignored.

DESCRIPTION

This warning message occurs when the specified option is not supported by Design Compiler.

WHAT NEXT

Rerun the command without the option.

SEE ALSO

UID-470 (warning) It is dangerous to create a generated clock on an inout port ’%s’.

DESCRIPTION

A circuit in which a generated clock drives an inout port may be unpredictable. If the port is functioning as an output while the generated clock is driving, bus contention will occur. If the generated clock is three-stated, any registers in the generated clock’s fanout may lose state.

WHAT NEXT

Verify that the circuit is safe according to your design rules. DesignTime will assume that the generated clock is valid.

UID-471 (error) The 'create_generated_clock' command cannot be used on output port '%s'.

DESCRIPTION

Generated clocks should be input ports or internal pins. In/out ports can be used, but they are not recommended because of bus contention issues.

WHAT NEXT

Identify a valid set of sources and reapply the **create_generated_clock** command.

UID-472 (error) You can specify only a single object for master clock source.

DESCRIPTION

The -source option takes only a single object as an argument.

WHAT NEXT

You can have a generated clock derived from a single clock. You cannot generate a clock from more than one master clock.

UID-473 (error) The number of edges specified '%d' is not an odd number > 3.

DESCRIPTION

The number of edges to make one period of the generated clock waveform has to be an odd number > 3.

WHAT NEXT

Carefully specify edges and ensure that you specify one full clock cycle using the edges.

UID-474 (Error) In the -edge specification of create_generated_clock ’%s’, the edge numbers must be greater than zero and in increasing order.

DESCRIPTION

In the -edge specification of a create_generated_clock command, the edge numbers specified must be in increasing order. The edge numbers should also be greater than zero, since it refers to the edge-number of the master clock.

WHAT NEXT

Check the -edge spec in create_generated_clock command and edge numbers increasing.

UID-475 (Error) The master source must be specified.

DESCRIPTION

For **create_generated_clock**, the -source option must be specified. This option specifies the source of the generated clock.

WHAT NEXT

Specify -source in the create_generated_clock command.

UID-476 (warning) Converting propagated clock at ’%s’ to ideal clock.

DESCRIPTION

You receive this message if you use **set_clock_latency** to set network latency on a propagated clock. Clocks processed by **set_clock_latency** are automatically converted to ideal clocks. The **set_propagated_clock** command is normally used to set propagated

clock network latency. This message warns you that the specified propagated clock is being converted to an ideal clock.

WHAT NEXT

This is a warning message only. If it is acceptable to you that the specified propagated clock is converted to an ideal clock, no action is required on your part. Otherwise, if you want the clock to be propagated, do not use **set_clock_latency** on the clock; use **set_propagated_clock** to specify a propagated clock latency.

SEE ALSO

set_clock_latency (2), **set_propagated_clock** (2).

UID-477 (warning) Converting ideal clock at '%s' to propagated clock.

DESCRIPTION

You receive this message if you use **set_propagated clock** to set the **propagated_clock** attribute on a clock on which you previously set latency or transition. Clocks for which latency or transition have been set are automatically considered to be ideal clocks. Setting the **propagated_clock** attribute on an ideal clock converts it to a propagated clock. This message warns you that the specified ideal clock is being converted to a propagated clock, and the previously-specified latency or transition will not be used.

WHAT NEXT

This is a warning message only. If it is acceptable to you that the specified ideal clock is converted to a propagated clock, no action is required on your part. Otherwise, if you want the clock to remain ideal, remove the **propagated_clock** attribute using the **remove_propagated_clock** command, and the previously-specified latency and transition values will be used.

SEE ALSO

remove_ideal_clock (2), **set_clock_latency** (2), **set_propagated_clock** (2).

UID-478 (Error) Virtual clock '%s' cannot be made propagated.

DESCRIPTION

You receive this message if you attempt to set a **propagated_clock** attribute on a

virtual clock. You cannot specify a virtual clock as a propagated clock, because virtual clocks do not have any source and cannot be made propagated.

WHAT NEXT

Review your design to verify your intended clock scheme.

SEE ALSO

set_propagated_clock (2).

UID-479 (Error) Clock transition cannot be specified for virtual clock ‘%s‘ .

DESCRIPTION

You receive this message if you attempt to use the **set_clock_transition** command on a virtual clock. You cannot specify clock transitions on virtual clocks, because they do not have any source.

WHAT NEXT

Review your design to verify your intended clock scheme.

SEE ALSO

set_clock_transition (2).

UID-480 (Warning) Clock transition specified for propagated clock ‘%s‘ will be ignored.

DESCRIPTION

You receive this message if you attempt to specify a clock transition on a propagated clock using **set_clock_transition**. You can specify clock transitions only for ideal clocks. This message warns you that the clock transition you specified is being ignored for the clock.

WHAT NEXT

If it is acceptable to you that the clock transition is ignored for this clock, no action is required on your part. Otherwise, if you want to specify a clock

transition for the clock, remove the **propagated_clock** attribute from it using **remove_propagated_clock**. Then reexecute **set_clock_transition**.

SEE ALSO

remove_propagated_clock (2), **set_clock_transition** (2).

UID-481 (error) White spaces are not allowed in the string '%s'.

DESCRIPTION

This error message occurs when white spaces appear in the input. This command does not allow any white space, such as tabs or spaces, in the string argument.

WHAT NEXT

Rerun the command without any white space in the string argument.

UID-482 (error) An empty string argument was found.

DESCRIPTION

This error message occurs when an empty string is entered as an argument. This command does not allow empty strings as arguments.

WHAT NEXT

Rerun the command with a non-empty string argument.

UID-483 (error) Not allowed to remove default power (or ground) net '%s'.

DESCRIPTION

This error occurs because the tool attempted to remove from the design the default power net stored in the **mw_logic1_net** variable (or the **mw_logic0_net** variable), which is not allowed. You are allowed to remove other power nets.

WHAT NEXT

Eliminate any command that attempts to remove the default power net.

UID-485 (error) Cannot specify %s without -source.

DESCRIPTION

This error message occurs when a specified command option requires another option, which is omitted.

WHAT NEXT

Refer to the manual page for this command for detailed information on valid options and rerun the command.

UID-486 (warning) The output of the propagate_constraints command is in DCSH mode. Use the UNIX utility dc-transcript to convert DCSH script to DC-Tcl script.

DESCRIPTION

You receive this message because you executed the **propagate_constraints** command from dc_shell-t; that is, in DC-Tcl mode. This message warns you that whether you execute the **propagate_constraints** command in DCSH-mode or in DC-Tcl mode, the output is always in DCSH mode. Thus, the script you generate is in DCSH mode.

WHAT NEXT

To convert the script from DCSH format to DC-Tcl format, use the UNIX dc-transcript utility.

SEE ALSO

propagate_constraints (2).

UID-487 (warning) The '%s' option is obsolete. It is ignored.

DESCRIPTION

WHAT NEXT

UID-488 (error) Control value '%s' already specified for '%s'.

DESCRIPTION

You receive this error message if you attempt to set the noncontrolling value for a particular object to high or low when you have already specified the opposite noncontrolling value for this object through a previous **set_clock_gating_check** command. This message informs you that you cannot specify both high and low noncontrolling values for the same object.

WHAT NEXT

If you want to reset or change the **-high** or **-low** option, first execute the **remove_clock_gating_check** command, then reexecute the **set_clock_gating_check** command with the desired option. Only use the **-high** or **-low** option when you are certain about the controlling value for a particular cell.

SEE ALSO

set_clock_gating_check (2).

UID-489 (error) Cannot specify %s option for '%s'. Can only specify on cells or pins.

DESCRIPTION

You receive this message if you execute the **set_clock_gating_check** command and specify both the **-hi** and **-low** options on objects that are neither cells nor pins.

WHAT NEXT

Use the **-high** or **-low** options only on cells or pins.

SEE ALSO

set_clock_gating_check (2).

UID-490 (error) Cannot specify both high and low for the same object.

DESCRIPTION

You receive this message if you executed the **set_clock_gating_check** command and specified both the **-high** and **-low** options for the same object. This message informs you that you can set the noncontrolling value of the clock for this particular clock gating check to be the high or the low interval of the clock, but not both.

WHAT NEXT

Reexecute the **set_clock_gating_check** command and specify either the **-high** or **-low** option. Use these options only when you are very certain about the controlling value of the clock for a particular cell.

SEE ALSO

set_clock_gating_check (2).

UID-491 (error) Only one clock can be specified.

DESCRIPTION

You receive this message if you executed the **set_input_delay**, **set_output_delay**, **remove_input_delay**, or **remove_output_delay** and specified multiple clocks in the -clocks option. You can only specify one clock for this option.

WHAT NEXT

Reexecute the command and only choose one clock.

SEE ALSO

set_input_delay (2), **set_output_delay** (2), **remove_input_delay** (2), **remove_output_delay** (2).

UID-492 (error) Object specified in -clock option must be a clock type.

DESCRIPTION

You receive this message if you executed the **set_input_delay**, **set_output_delay**, **remove_input_delay**, or **remove_output_delay** and specified a non-clock object in the -clocks option. You can only specify one clock object for this option.

WHAT NEXT

Reexecute the command and only choose one clock object.

SEE ALSO

set_input_delay (2), **set_output_delay** (2), **remove_input_delay** (2), **remove_output_delay** (2).

UID-493 (error) Timing derate value should be bigger than 0 and smaller than 2.0.

DESCRIPTION

This error message occurs when the timing value is not within the acceptable range. The timing derate value must be larger than 0 and smaller than 2.0.

WHAT NEXT

Specify a value within the range of 0 to 2.0 and run the command again.

SEE ALSO

set_timing_derate(2)

UID-494 (warning) No -early or -late option is specified.

DESCRIPTION

This warning message occurs when running the **set_timing_derate** command without specifying either the **-early** or the **-late** option. When neither option is specified, the default is that both are set to **true**, and the derate value is applied to both.

WHAT NEXT

This is only a warning message. No action is required on your part.

However, if you do not want the derate value to apply to both options, run the command again and specify either the **-early** or the **-late** option.

SEE ALSO

set_timing_derate(2)

UID-495 (error) Cannot specify %s option with object list.

DESCRIPTION

This error message occurs if you execute the **set_timing_derate** command and specify the **-net_delay** option on the object list.

WHAT NEXT

Execute the command again with the **-net_delay** option but without the object list.

SEE ALSO

set_timing_derate(2)

UID-496 (warning) SDC does not allow -min and -max deratings

DESCRIPTION

This warning occurs if you execute the **write_sdc** command and there is a difference between the -min and -max settings of a**set_timing_derate** . These switches are not found in SDC and as a result this information is lost when producing the SDC output. To be safe, the **write_sdc** command will produce the lesser of the two numbers for the early derating, and the greater of these two numbers for the late derating, although this may give overly pessimistic results further downstream.

WHAT NEXT

Examin the instances of **set_timing_derate** in the SDC output to determine whether the values are the most appropriate for tools that will make use of the SDC constraints.

SEE ALSO

set_timing_derate(2), write_sdc(2)

UID-499 (warning) The clock %s is not a generated clock. This command removes only generated clocks.

DESCRIPTION

One or more clock(s) specified in your command arguments is not a generated clock. The **remove_generated_clock** command can remove only generated clocks. This is not an error though.

WHAT NEXT

You can use remove_clock command to remove non-generated (or Master) clocks. To know more about this, see help for **create_clock, create_generated_clock, remove_clock, remove_generated_clcok**.

UID-500 (warning) Pin '%s' is hierarchical and not valid for case analysis.

DESCRIPTION

You receive this warning message because you specified hierarchical pins as objects for **set_case_analysis** and **remove_case_analysis**. Therefore, case analysis is not being set or removed on the specified pin. If there are multiple pins specified in the object_list, case analysis values will still be set or removed on nonhierarchical pins or ports.

WHAT NEXT

Do not specify hierarchical pins for **set_case_analysis** and **remove_case_analysis**.

SEE ALSO

remove_case_analysis (2), **set_case_analysis** (2).

UID-501 (error) There are no valid objects specified for case

analysis.

DESCRIPTION

You receive this error message because you did not provide a list of nonhierarchical pins or ports when you executed the **set_case_analysis** command or the **remove_case_analysis** command.

WHAT NEXT

Specify a valid set of non-hierarchical pins or ports.

SEE ALSO

remove_case_analysis (2), **set_case_analysis** (2).

UID-502 (error) Value '%s' is not a valid value.

DESCRIPTION

You receive this error message because you did not specify a valid value with the **set_case_analysis** command. Valid values are 0, 1, zero, and one.

WHAT NEXT

Specify a valid value for the **set_case_analysis** command.

SEE ALSO

set_case_analysis (2).

UID-503 (error) Rising and falling values are not currently supported.

DESCRIPTION

You receive this error message because you did not specify valid values with the **set_case_analysis** command. Valid values are 0, 1, zero, and one. Although PrimeTime supports rise, fall, rising, and falling, these options are not currently supported in DesignTime.

WHAT NEXT

Specify valid values for the **set_case_analysis** command.

SEE ALSO

set_case_analysis (2).

UID-504 (error) Must specify either -all or object_list.

DESCRIPTION

You receive this error message because you have not specified a value with the **remove_case_analysis** command. You must specify either an object list or the **-all** option with this command.

WHAT NEXT

Reexecute the **remove_case_analysis** command and specify either an object list or the **-all** option.

SEE ALSO

remove_case_analysis (2).

UID-505 (error) Cannot specify both -all and object_list.

DESCRIPTION

You receive this error message because you have executed the **remove_case_analysis** command and have specified the **-all** option and an object list. You can only specify one of these arguments with the **remove_case_analysis** command.

WHAT NEXT

Reexecute the **remove_case_analysis** command and specify either the **-all** option or an object list.

SEE ALSO

remove_case_analysis (2).

UID-506 (error) Cannot change link for instance cell '%s'.

DESCRIPTION

You receive this error message because you have executed the **change_link** command for an instance cell.

WHAT NEXT

Reexecute the **change_link** command without instance cells.

UID-510 (error) In Dcl mode, you can specify only one mode with the set_mode command.

DESCRIPTION

You receive this error message because you have executed the **set_mode** command and specified more than one mode. This is invalid and, as a result, no modes are set by this command.

WHAT NEXT

Reexecute the **set_mode** command and specify only one mode.

SEE ALSO

set_mode (2).

UID-511 (error) Specified instance %s not valid. Must be a cell.

DESCRIPTION

You receive this error message because you have issued the **set_mode** command on an instance that is not a cell. This is invalid and, as a result, no modes are set by this command.

WHAT NEXT

Reexecute the **set_mode** command and specify a mode on a cell or a cell instance.

SEE ALSO

set_mode (2).

UID-520 (error) Ungroup -start_level does not work when the variable disable_2001_ungroup is true.

DESCRIPTION

This message is issued when the variable disable_2001_ungroup is true and ungroup -start_level option is used. The -start_level option is not supported in the old version of ungroup and so this error message is issued. The same error message will be generated when trying to use ungroup -start_level for Behavioral compiler designs. A Behavioral Compiler design will have the attribute is_post_scheduled_design.

WHAT NEXT

Set the variable disable_2001_ungroup to false. If the error message still occurs, verify that the design is not a Behavioral Compilerdesign. If the design is a BC design, the -start_level option is not supported. To ungroup different levels of the design, use a combination of current_instance and ungroup. See the man page of ungroup for more details.

SEE ALSO

ungroup(2).

UID-521 (error) Ungroup -start_level cannot be used in conjunction with -small option.

DESCRIPTION

This message is issued when the -small and -start_level options are used together with the ungroup command. Both of these two options represent completly different strategies.

WHAT NEXT

Use either the -small option or the -start_level option.

SEE ALSO

ungroup(2).

UID-523 (Warning) Some valid instances of design '%s' are not ungrouped due to dont_touches or other MV-related constraints in other instances.

DESCRIPTION

This message is issued when ungroup -flatten, ungroup -small or ungroup -start_level is used where one or more instances of the design's multiply-instantiated sub-blocks has an instance-specific dont_touch attribute placed on one of its child cells, or has instance specific operating condition that is different from the owner block. Ungroup cannot be performed where it may change certain instances such that all instances of a sub-design can no longer point to the same reference. This problem does not occur if the dont_touches or Mv-related constraint are not instance specific.

WHAT NEXT

If it is not OK, remove the instance specific dont_touch or constraints and run ungroup again. Or use uniquify command to uniquify the design.

SEE ALSO

ungroup(2),uniquify(3).

UID-524 (Warning) Some valid instances of design '%s' are not ungrouped because of some instances outside the start_level"

DESCRIPTION

This message is issued when ungroup -start_level option is used in the case where one or more instances of the design's multiply-instantiated sub-block has a child cell which does not fall into the range of specified levels to be ungrouped. Ungroup cannot be performed where it may change certain instances such that all instances of a sub-design can no longer point to the same reference.

WHAT NEXT

Use ungroup -flatten option to flatten the design. Or, simply use the uniquify command to uniquify the design.

SEE ALSO

ungroup(2),uniquify(2).

UID-526 (error) No valid cells to ungroup within the level specified.

DESCRIPTION

This message is issued when there are simply no valid cells to be ungrouped from the specified -start_level downwards. In this case, nothing will be ungrouped.

WHAT NEXT

None.

SEE ALSO

ungroup(2).

UID-527 (error) Writing designs in DB format is no longer supported. Option xg_force_db is ignored.

DESCRIPTION

This message is issued when you are trying to write the design in XG mode in DB Format. Due to capacity reasons, it is recomended to write the netlist using DDC format instead of DB format.

WHAT NEXT

Please use a different format such as ddc to write out the netlist.

SEE ALSO

write(2).

UID-528 (warning) Writing designs in DB format is no longer

supported.

DESCRIPTION

This message is issued when you are trying to write the design in XG mode in DB Format. Due to capacity reasons, it is recommended to write the netlist using DDC format instead of DB format.

WHAT NEXT

Modify your scripts to write DDC format or ignore this error message if the usage was intentional.

SEE ALSO

write(2).

UID-529 (warning) A previous '%s' attribute on net '%s' will be overwritten.

DESCRIPTION

The **set_attribute** command can be used to specify the wired logic type of a net. This warning is given when a previous wire logic type exists and is different from the one being set.

WHAT NEXT

To avoid this warning message, use **remove_attribute** command to remove the existing wired logic attribute before setting the new wired logic attribute on the net.

UID-530 (Error) Writing designs in DB format is no longer supported.

DESCRIPTION

This message is issued when you are trying to write the design in XG mode in DB Format. Due to capacity reasons, it is recommended to write the netlist using DDC format instead of DB format.

WHAT NEXT

Modify your scripts to write DDC format or ignore this error message if the usage was intentional.

SEE ALSO

write(2).

UID-531 (Warning) Some valid instances of design '%s' passed as an argument to ungroup -all_instances option are not ungrouped due to dont_touches in other instances or other MV-related constraints in this instance or other instances.

DESCRIPTION

This message is issued when ungroup -all_instances is used where one or more instances of the design's multiply-instantiated sub-blocks has an instance-specific dont_touch attribute or datapath_optimization attribute placed on one of its child cells, or has instance specific operating condition/ power domains that is different from the owner block. Ungroup cannot be performed where it may change certain instances such that all instances of a sub-design can no longer point to the same reference. This problem does not occur if the dont_touches or Mv-related constraint are not instance specific.

WHAT NEXT

If it is not OK, remove the instance specific dont_touch or constraints and run ungroup again. Or use uniquify command to uniquify the design.

SEE ALSO

ungroup(2),uniquify(3), OPT-774.

UID-540 (error) -scenarios and -active_scenarios may only be used with ddc format

DESCRIPTION

The *-scenarios* and *-active_scenarios* options to the **read_file** command may only be used if *-format ddc* is specified.

WHAT NEXT

Verify that the correct format option has been supplied to the **read_file** command.

SEE ALSO

read_file(2)
read_ddc(2)

UID-541 (error) -active_scenarios may not be used without -scenarios

DESCRIPTION

The **read_file** command's *-active_scenarios* option may only be used if the *-scenarios* option is also specified.

WHAT NEXT

See **read_file**(2) for more information on controlling which scenarios' constraints are read from the ddc file.

SEE ALSO

read_file(2)
read_ddc(2)
set_active_scenarios(2)
all_scenarios(2)
all_active_scenarios(2)

UID-542 (error) All scenario names specified in -active_scenarios must also be specified in -scenarios

DESCRIPTION

The **read_file** command's *-active_scenarios* option may only contain scenario names that are also listed in the *-scenarios* option. The *-scenarios* option, however, may contain names that are not included in *-active_scenarios*.

WHAT NEXT

See **read_file**(2) for more information on controlling which scenarios' constraints

are read from the ddc file.

SEE ALSO

read_file(2)
read_ddc(2)
set_active_scenarios(2)
all_scenarios(2)
all_active_scenarios(2)

UID-550 (error) Unable to read the library '%s' from '%s'.

DESCRIPTION

This error message occurs when the library has been pruned to provide optimal performance of the tool. The library will be re-read from the disk on demand to restore the necessary information to memory.

The library has been removed or moved to a different location. This message occurs because the tool does not expect the library files to be removed within a session.

WHAT NEXT

Copy the library file to the appropriate location and rerun the command.

UID-600 (error) Illegal type '%s'. Must be either "buffer" or "inverter".

DESCRIPTION

You receive this message if you execute the **set_isolate_ports** command and use an invalid argument for the **-type** option. Valid arguments for **-type** are "buffer" and "inverter". To see a listing of options and arguments, from within dc_shell enter **set_isolate_ports -help**.

WHAT NEXT

Reexecute **set_isolate_ports** and use a valid argument for the **-type** option.

UID-601 (error) Cannot isolate port '%s' because it is an '%s'

port; only input or output ports can be isolated.

DESCRIPTION

You receive this message if you execute **set_isolate_ports** and specify a port that is an inout port. You can isolate only input or output ports.

WHAT NEXT

Reexecute the **set_output_ports** command and ensure that the list of ports contains only input or output ports.

UID-602 (error) Can’t specify <power_value> or <power_unit> when -delete_all is specified

DESCRIPTION

You receive this message if you specify <power_value> or <power_unit> along with ’-delete_all’ option to **set_cell_internal_power** command.

WHAT NEXT

Reexecute the **set_cell_internal_power** command and ensure that you specify either ’-delete_all’ option or <power_value> and/or <power_unit>.

UID-603 (error) There are no valid objects specified for set_cell_internal_power command.

DESCRIPTION

You receive this message if you do not specify <pin_objects> or ’-delete_all’ option to **set_cell_internal_power** command.

WHAT NEXT

Re-execute the **set_cell_internal_power** command and ensure that you specify either ’-delete_all’ option or list of pins where you want to annotate the power number.

UID-604 (information) It is recommended to use

set_ideal_network command instead of set_ideal_net.

DESCRIPTION

This information message occurs because the **set_ideal_net** and **set_ideal_network** commands are being combined. The **set_ideal_network** command is replacing **set_ideal_net**.

In the 2004.12 release, the **set_ideal_net** command is replaced by the following command, which is applied to the same objects:

set_ideal_network -no_propagate

WHAT NEXT

This is only an informational message. No action is required.

SEE ALSO

set_ideal_net(2)
set_ideal_network(2)
use_old_ideal_net(3)

UID-605 (warning) Replacing set_ideal_net command with set_ideal_network -no_propagate command.

DESCRIPTION

This warning message occurs because the **set_ideal_net** and **set_ideal_network** commands are being combined. The **set_ideal_network** command is replacing **set_ideal_net**.

The attributes are applied on the global driver pins of the specified nets, instead of applying the *ideal_net* attribute on the specified nets.

In the 2004.12 release, the **set_ideal_net** command is replaced by the following command, which is applied to the same objects:

set_ideal_network -no_propagate

WHAT NEXT

This is only an informational message. No action is required.

SEE ALSO

set_ideal_net(2)
set_ideal_network(2)
use_old_ideal_net(3)

UID-606 (warning) Transferring ideal_net attribute onto the driver pin %s of net %s.

DESCRIPTION

This warning message occurs because the **set_ideal_net** and **set_ideal_network** commands are being combined. The **set_ideal_network** command is replacing **set_ideal_net**.

In the 2004.12 release, the **set_ideal_net** command is replaced by the following command:

set_ideal_network -no_propagate

The attribute for *ideal_net* is transferred from the specified nets to the global driver pins of those nets, and is translated to the corresponding ideal network attributes.

WHAT NEXT

This is only a warning message. No action is required.

SEE ALSO

set_ideal_net(2)
set_ideal_network(2)
use_old_ideal_net(3)

UID-607 (error) The option -instance is obsolete in XG mode. Please use the complete path to the net instance with the %s command instead.

DESCRIPTION

You have used the option -instance which is obsolete in XG mode. In XG mode one can use the complete hierarcical net name to perform remove_net and create_net operations. Please check the man page of these commands for details and examples.

WHAT NEXT

Please re-issue the command with the new format.

UID-608 (information) Performing automatic 'set_ideal_net' on net '%s'.

DESCRIPTION

This message occurs because **set_ideal_net** is being automatically performed at the named net. This behavior can be controlled using the following variables:

icc_auto_ideal_nets (default is false) **icc_auto_ideal_fanout_threshold** (default is 500) **icc_auto_ideal_multi_driver_threshold** (default is 100)

This feature is meant to provide better default behavior during optimization for high-fanout nets that cannot be decomposed by buffering (for example, because they are dont_touch).

WHAT NEXT

No action is required.

SEE ALSO

set_ideal_net(2)
set_ideal_network(2)

UID-610 (error) '%s' is not a supported value for option '%s'.

DESCRIPTION

You have specified an illegal or unsupported value for a command option. You can check which options and values are supported by Design Compiler by executing "*command* -help" in **dc_shell**.

WHAT NEXT

Change the option value to one that is supported.

UID-611 (warning) Analysis type '%s' is not supported. Using

'%s' instead.

DESCRIPTION

The requested analysis type is not currently supported in Design Compiler. So we will use the closest available analysis type, which should be suitable in most cases. You can check which options are supported by Design Compiler by executing "*command* -help" in **dc_shell**.

WHAT NEXT

Verify that the substituted analysis type is acceptable for your purposes.

UID-620 (error) Number of pins on the cell being changed is not same as the number of pins on the new reference cell.

DESCRIPTION

You receive this error message because the number of pins on the cell or reference being changed with change_link, does not match the number of pins on the new reference.

WHAT NEXT

Please provide a compatible reference library cell for change_link to work correctly

UID-660 (error) Option%s is mutually exclusive to option%s.

DESCRIPTION

You receive this error message if you specify two or more options on one command line that have adverse effects and are therefore mutually exclusive.

WHAT NEXT

Refer to the man page for the command that you invoked for information about the options. Do not use options that cannot be specified together on one command line.

UID-661 (warning) Data missing for physically aware net delay

estimation.

DESCRIPTION

This warning message occurs when you start to use the physically aware net model without all of the essential data.

Any of the following causes the warning message:

• The physical library is not specified.

• The library is specified, but it could not be read in successfully.

• The library did not provide all of the necessary data, including the site’s row_height, average wire_width, capacitance, and resistance per unit length.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, you can do either of the following:

• Continue using the conventional wire load mode

• Make sure that you have specified a valid physical library.

UID-662 (warning) %s data missing in physical library.

DESCRIPTION

This warning message occurs when the physical library currently set does not define all of the values necessary to correctly activate the physically aware wire load estimation method.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, check that you are using the correct physical library.

UID-663 (warning) Physical library not specified.

DESCRIPTION

You receive this warning message when the **physical_library** variable is not set or the specified libraries cannot be loaded.

WHAT NEXT

This is only a warning message. No action is required.

However, you can check that you are using the correct physical library.

SEE ALSO

physical_library(3)

UID-665 (error) P/G net %s used in command %s.

DESCRIPTION

P/G nets can not be manipulated using connect_net or disconnect_net commands. connect_net and disconnect_net can only be used for signal nets.

WHAT NEXT

Use one of **connect_pg_nets** , **connect_logic_zero** or **connect_logic_one** commands to do the necessary netlist changes for P/G nets.

UID-666 (error) No Milkyway library is open.

DESCRIPTION

This error is generated when an ascii design is being read in without opening a Milkyway library first.

WHAT NEXT

Use **open_mw_lib** command to open an existing Milkyway library Use **create_mw_lib** command to create a Milkyway library if one does not exist. Run the read command again.

UID-667 (error) Some clocks have been specified in multiple groups.

DESCRIPTION

The messages prior to this show the clock that has been specified multiple times.

WHAT NEXT

A clock should be specified only once.

UID-668 (error) Can not specify -allow_paths with -logically_exclusive or -physically_exclusive.

DESCRIPTION

The allow_paths option is invalid for logically_exclusive or physically_exclusive option of set_clock_groups.

WHAT NEXT

Logically exclsuive relationship has no SI impact and only sets the false paths between the specified clocks. Hence -allow_paths does not make sense with -logically_exclusive option.

Physically exclusive clocks imply that clocks are not present at the same time and paths between the clocks can not exist.

UID-670 (error) Design CEL is already read-in and created. Please close current CEL before reading in another design.

DESCRIPTION

The design CEL design is already read and created, so can’t create another design.

WHAT NEXT

The command read_ddc will create the design CEL, so if you want to load more than one ddc files, make sure read them in at once.

UID-820 (error) Floorplan block '%s' is not defined.

DESCRIPTION

You have specified a command which works on an existing fp_block. The block you specified could not be found.

WHAT NEXT

Double check the names of defined blocks with write_fp_script.

UID-821 (error) Floorplan atom '%s' is not defined.

DESCRIPTION

You have specified a command which works on an existing fp_atom. The atom you specified could not be found.

WHAT NEXT

Double check the names of defined atoms with write_fp_script.

UID-822 (error) Atom '%s' is already defined.

DESCRIPTION

You are trying to redefine the binding of a floorplan atom which is already bound to another cell.

WHAT NEXT

Use a different atom name, or first undefine the atom name in question using "define_fp_atom -name atom_name -undef".

UID-823 (error) Atom '%s' is already defined for cell '%s'.

DESCRIPTION

You are attempting to redefine the the atom for a cell of the netlist.

WHAT NEXT

Define the new atom for a different cell, or first undefine the current atom using "define_fp_atom -name old_atom_name -undef".

UID-824 (error) Design '%s' (instance '%s') is multiply instantiated.
Floorplan atoms are only permitted within uniquified hierarchies.

DESCRIPTION

You have attempted to define an atom in a part of the hierarchy which is instantiated multiple times. The designs for atoms may only be instantiated once in your design.

WHAT NEXT

Use the "uniquify" command to force the multiple copies of the same design to be changed into multiple designs.

UID-825 (error) You must specify an atom name or cell name.

DESCRIPTION

You have used define_fp_atom without specifying -name flag or a cell name. This is not supported.

WHAT NEXT

Specify a -name flag.

UID-826 (error) The floorplan abstracts have not been created or are out of date.
Please (re)run create_fp_abstracts.

DESCRIPTION

This command requires create_fp_abstracts to be run before it can execute.

WHAT NEXT

Please re(run) create_fp_abstracts.

UID-827 (error) The floorplan abstract placement has not been created or is out of date.
Please (re)run place_fp_abstracts.

DESCRIPTION

This command requires place_fp_abstracts to be run before it can execute.

WHAT NEXT

Please re(run) place_fp_abstracts.

UID-828 (error) You can only select one of -select, -flyline, -expand, and -unexpand

DESCRIPTION

Only one of the given flags may be specified in a single command call.

WHAT NEXT

Specify only one of these flags per call.

UID-829 (error) You must specify a cell for -expand or -unexpand

DESCRIPTION

The -expand and -unexpand options require you to specify a cell to work on.

WHAT NEXT

Specify a cell name.

UID-830 (error) You must specify an abstract name for -select abstract

DESCRIPTION

The -select abstract option requires you to also specify the name of the abstract that you want to select.

WHAT NEXT

Specify the name of an abstract.

UID-831 (warning) Cell '%s' has been assigned an abstract area of zero

DESCRIPTION

You have either omitted the -area flag or explitly specified zero to the -area flag. This will cause the given cell to be ignored for area analysis of the floorplan.

WHAT NEXT

If you have assigned a zero area in error, you can either redefine the area by running "define_fp_abstract" again, or you can remove the abstract by using "define_fp_abstract -remove".

UID-832 (warning) You need to define floorplan atoms or trial atoms before running this command

DESCRIPTION

This command analyzes design statistics based on the currently defined floorplan atoms and trial atoms. Without these, there is nothing to report.

WHAT NEXT

Create floorplan atoms with define_fp_atom. Create trial atoms with define_trial_atoms.

UID-833 (error) Floorplan block '%s' has no bound logic

DESCRIPTION

The specified floorplan block is currently empty. So there is nothing to show.

WHAT NEXT

Select a different floorplan block as a connection source, or do not specify any connection source.

UID-834 (error) Cannot use '%s' as the clock reference. The clock reference used must be a clock object.

DESCRIPTION

The clock network latency is the time it takes a clock signal to propagate from the clock definition point to a register clock pin. In the case of multiple clocks pass through the same pin or port object, clock network latency can be specified on this object with respect to a specific clock. In this way, different values can be applied as clock network latency for different clocks. With the **-clock** option, a clock object must be provided to specify which clock the clock network latency is referring to. Note, the clock network latency is only applied on ideal clock network.

WHAT NEXT

Make sure to provide a clock object when using **-clock** option. Use **report_clock** to report all clocks in the current deign.

UID-835 (warning) Cannot use clock object '%s' in the object list when -clock option is provided. The -clock option will be ignored for '%s'.

DESCRIPTION

The clock network latency is the time it takes a clock signal to propagate from the clock definition point to a register clock pin. In the case of multiple clocks pass through the same pin or port object, clock network latency can be specified on this object with respect to a specific clock. In this way, different values can be applied as clock network latency for different clocks. With the **-clock** option, only non-clock object can be provided in the object list. Otherwise, the **-clock** option

will be ignored for these objects.

WHAT NEXT

Make sure to provide non-clock object in object list when using **-clock** option. Use **report_clock** to report all clocks in the current design.

UID-836 (error) Cannot use -clock option and any of the options -source, -early and -late at the same time.

DESCRIPTION

See **set_clock_latency** man page for the differernce between clock network latency and clock source latency.

WHAT NEXT

Only set clock network latency or clock soruce latency at one time.

UID-841 (error) Fail to rebuild timing design from database

DESCRIPTION

Failed to load the timing design from the database. This is usually caused by database corruption.

WHAT NEXT

Quit and restart the session. Save the database to a new name to avoid corrupting the previously valid database. If you are using CEL as input, check the CEL by opening in the new session.

UID-842 (warning) Command is not trace-mode compliant, and is ignored

DESCRIPTION

You are running a trace-mode session, and the command executed is not trace-mode compliant. The command will be ignored.

WHAT NEXT

If you want to execute this command, please end the trace-mode session.

UID-900 (error) The -type argument must provide at least one cell.

DESCRIPTION

You receive this error message if you issue **set_scan_register_type -type** without an argument for the required **-type** switch. The **set_scan_register_type** command requires that at least one example cell be given with **-type**.

WHAT NEXT

Reissue **set_scan_register_type -type** with at least one name of a valid example cell from the target library, as the argument to **-type**.

SEE ALSO

set_scan_register_type (2).

UID-901 (error) The %s cell already has the set_register_type attribute set.

DESCRIPTION

You can only use **set_scan_register_type** after removing the **set_register_type** attribute.

WHAT NEXT

Remove the **set_register_type** attribute and reissue the command.

UID-902 (error) The cell %s issued as an argument to set_scan_register_type -type or set_scan_replacement options

-lssd, -muxd, or -clocked_scan is a non-scan cell.

DESCRIPTION

You receive this error message when you issue the name of a non-scan cell as an argument to the **set_scan_register_type -type** command or the **set_scan_replacement** command with the **-lssd**, **-muxd**, or **-clocked_scan** option.

The **set_scan_register_type** command **-type** switch requires a scan cell as an argument. The **-type** switch must specify a list of scan cells for the **insert_scan** or the **compile -scan** command to use for scan replacement of non-scan sequential cells or designs.

The **set_scan_replacement** command with the **-lssd**, **-muxd**, or **-clocked_scan** switches requires a scan cell as an argument. These switches specify a scan replacement for each scan style for the set of non-scan cells specified through the **-nonscan** option.

WHAT NEXT

Reexecute the **set_scan_register_type** command and specify a scan cell as an argument.

SEE ALSO

compile(2)
insert_scan(2)
set_scan_register_type(2)
set_scan_replacement(2)

UID-903 (error) The %s cell is not valid for the methodology specified.

DESCRIPTION

You receive this error message when an example cell issued as an argument to the **set_scan_register_type -type** command or the **set_scan_replacement** command with the **-lssd**, **-muxd**, or **-clocked_scan** option is not valid for the methodology defined.

The methodology for the **set_scan_register_type** command is the one for the current design. The methodology for the **set_scan_replacement** command is specified by the option.

WHAT NEXT

Verify the defined methodology using the **report_test -methodology** command.

You can reexecute the **set_scan_register_type** command with the **-type** argument, specifying only cells that are valid for that methodology for the **-type** argument.

Find the valid cell for the methodology and then you can reissue the **set_scan_replacement** command.

SEE ALSO

report_test(2)
set_scan_register_type(2)
set_scan_replacement(2)

UID-904 (error) Unable to find example %s '%s'.

DESCRIPTION

You receive this error message if an example cell you issued as an argument to **set_scan_register_type -type** could not be found in the target library. All example cells given as arguments to **-type** must exist in the target library.

Possible causes for this error condition might be a typo or spelling error when you entered the example cell name; or the wrong target library specified in the **target_library** environment variable.

WHAT NEXT

To correct this error, proceed as follows:

1. Verify that the **target_library** environment variable is set with the target library that contains the specified example cell, by executing **list target_library** within **dc_shell**.

2. If necessary, reset **target_library** so that it contains the name of the appropriate target library.

3. Verify the correct capitalization and spelling of the example cell names, and reissue **set_scan_register_type**.

SEE ALSO

compile (2), **insert_scan** (2), **set_scan_register_type** (2); **target_library** (3).

UID-905 (error) The %s design named %s is of "unknown" sequential type.

DESCRIPTION

You receive this error message if the type specified to the **set_scan_register_type**

command or the **set_scan_replacement** command options cannot be recognized by the tool.

WHAT NEXT

Reissue the **set_scan_register_type** or the **set_scan_replacement** command with a recognizable sequential device.

SEE ALSO

set_scan_register_type(2)
set_scan_replacement(2)

UID-906 (error) There are no valid cells specified on which to assert set_scan_register_type.

DESCRIPTION

You receive this error message if you issue **set_scan_register_type** with the *cell_or_design_list* argument, but none of the cells on the list are valid. There is nothing for the command to operate on.

WHAT NEXT

Examine the list of cells you entered, verify the spelling and capitalization of the names, or otherwise determine the reason why the cells were invalid. Then reissue the **set_scan_register_type** command with a list of valid cells for *cell_or_design_list*.

SEE ALSO

compile (2), **insert_scan** (2), **set_scan_register_type** (2).

UID-907 (warning) Cell '%s' is not a sequential cell.

DESCRIPTION

You receive this message if you issue **set_scan_register_type** with a nonsequential cell in the *cell_or_design_list*. **set_scan_register_type** must specify only sequential cells for **insert_scan** or **compile -scan** to replace with their scan equivalents.

WHAT NEXT

Reissue **set_scan_register_type** using only sequential cells in the *cell_or_design_list*.

SEE ALSO

compile(2), insert_scan(2), set_scan_register_type(2).

UID-908 (warning) Cell '%s' has the dont touch attribute set on it; cannot scan-replace.

DESCRIPTION

You receive this message if **insert_scan** or **compile -scan** encounters a sequential cell that has the **dont_touch** attribute set to *true* on it. **insert_scan** and **compile -scan** attempt to perform scan replacement on your design by replacing each sequential cell with its scan equivalent. The **dont_touch** attribute is designed to protect cells from being modified or optimized, so cells that have this attribute cannot be scan replaced. This message informs you that the specified cell was not scan replaced.

WHAT NEXT

If you intended to protect the specified cell from scan replacement, no action is required on your part. However, if you want the specified cell to be scan replaced, first remove the **dont_touch** attribute, either with **remove_attribute** or by executing **set_dont_touch false**. Then reissue **insert_scan** or **compile -scan**.

SEE ALSO

compile (2), **insert_scan** (2), **remove_attribute** (2), **set_dont_touch** (2).

UID-909 (error) %s cannot be set on an input port %s.

DESCRIPTION

This error message occurs when you attempt to set a **model_load** attribute on an input port. This attribute can only be set on output or inout ports.

WHAT NEXT

Reexecute the **set_model_load** command and ensure that the *port_list* contains only output and inout ports.

SEE ALSO

set_model_load(2)

UID-910 (error) The argument of the -bound option must be larger than the argument of the -threshold option.

DESCRIPTION

You receive this error message when you execute the **compare_rc** or **estimate_rc** command and specify a value for the **-bound** option that is smaller than or equal to the value for the **-threshold** option. The **-bound** option represents the upper level of back-annotated capacitance, and the **-threshold** option represents the lower level. For this reason, the value of the **-bound** must be larger than the value of the **-threshold** option.

WHAT NEXT

Reexecute the **compare_rc** or the **estimate_rc** command and specify a value for the **-bound** option that is larger than the value for the **-threshold** option.

SEE ALSO

compare_rc(2)
estimate_rc(2)

UID-911 (error) The -nonscan option requires at least one cell when mapping is specified.

DESCRIPTION

You receive this error message if you do not specify at least one nonscan cell for the **-nonscan** option in the **set_scan_replacement** command for mapping.

WHAT NEXT

Reissue the **set_scan_replacement** command and specify a nonscan cell as an argument for the **-nonscan** option. The **-nonscan** argument is not needed when you use the **-remove** option alone.

SEE ALSO

compile(2)
insert_scan(2)

UID-912 (error) The replacement cell specified for the methodology %s is not a valid scan cell for the methodology.

DESCRIPTION

You receive this error message for the **set_scan_Replacement** command when the scannable cell you specified for a given scan style is not a valid scan cell. The scan cell might not be valid for the scan style (**-lssd**, **-muxd**, or **clocked_scan**) that you specified.

WHAT NEXT

Reissue the **set_scan_replacement** command and specify a valid scan cell as an argument for the scan style option.

SEE ALSO

compile(2)
insert_scan(2)
set_scan_replacement(2)

UID-913 (error) One of the -lssd, -muxd, and -clocked_scan options should have at least one cell when mapping is specified.

DESCRIPTION

You receive this error message when you do not specify at least one scannable cell for any of the **-lssd**, **-muxd**, or clocked_scan mapping options in the **set_scan_replacement** command.

WHAT NEXT

Reissue the **set_scan_replacement** command and specify a scannable cell as an argument for the **-lssd**, **-muxd**, or **clocked_scan** option. These arguments are not needed when you use the **-remove** option alone.

SEE ALSO

compile(2)
insert_scan(2)
set_scan_replacement(2)

UID-914 (error) Cannot find target_library.

DESCRIPTION

This error message occurs when you do not specify a target library.

WHAT NEXT

Set the **target_library** variable to the appropriate library and run the command again.

SEE ALSO

compile(2)
insert_scan(2)
set_scan_replacement(2)

UID-915 (error) Cannot find %s gate in the target_libray

DESCRIPTION

You receive this message if you do not specifiy a flop that exists in the target library in any of the options of set_scan_replacement.

WHAT NEXT

Reissue **set_scan_replacement** , and specify a valid scan cell as an argument for the options. These arguments are not needed for -remove alone.

SEE ALSO

compile(2), insert_scan(2), set_scan_replacement(2).

UID-916 (error) Non-scan cell %s has more functional pins than the scan cell %s.

DESCRIPTION

You receive this message if a non-scan flop specified for -nonscan option of set_scan_replacement has more no of pins than a scan flop specified in one of the options . For example the non-scan flop might have async pins while scan flop is a simple scan flop without async pins.This is an error, since if scan replacement

tries to use this to swap in a scan flop, it will result in bad logic.

WHAT NEXT

Re-issue **set_scan_replacement** , and specify a proper scan cell as an argument for the options.

SEE ALSO

compile(2), insert_scan(2), set_scan_replacement(2).

UID-917 (warning) Non-scan cell %s has less functional pins than the non-scan cell %s.

DESCRIPTION

You receive this message if a scan flop specified for any of the options of set_scan_replacement has more no of pins than the non-scan flop. For example the scan flop might have async pins while non-scan flop is a plain D flip-flop.

WHAT NEXT

Re-issue **set_scan_replacement** , and specify a proper scan cell as an argument for the options. If not scan replacement will tie these pins to their default values.

SEE ALSO

compile(2), insert_scan(2), set_scan_replacement(2).

UID-918 (information) The timing reported below is an estimate. Please run vendor P&R tool to find out the actual design performance.

DESCRIPTION

During timing analysis, DC FPGA uses cell delays and routing delays to calculate the path delays. Cell delays are provided by FPGA vendor and are thus accurate. The routing delays are estimates because DC FPGA does not have information on the cell placement and routing. Therefore, the timing reported by DC FPGA is an estimate. It is recommended that you always run vendor Place and Route tool to determine the actual design perfomance. Based on P&R timing result, you then decide whether and how you take the next step to improve timing.

WHAT NEXT

This is an informational message only. No action is required on your part.

UID-919 (Error) The -exact option has a list of cells to use for mapping.

DESCRIPTION

This is shown when the -exact option in set_scan_register_type has a list of cells provided for mapping. Only a single cell newm should be provided.

WHAT NEXT

Usea single cell for -exact option and re-execute the command.

UID-920 (error) The %s command is not allowed in an interface logic model (ILM). This %s is in an ILM: '%s'.

DESCRIPTION

This error occurs because the tool does not support netlist editing within an ILM. The restricted commands are the following:

create_cell
create_net
create_port
connect_net
define_bus
disconnect_net
connect_pin
connect_logic_zero
connect_logic_one
remove_port
remove_cell
remove_net
insert_buffer
remove_buffer
size_cell
undefine_bus

WHAT NEXT

Restrict the collection of objects that you are editing to exclude any objects

inside ILMs and reapply the netlist editing commands.

SEE ALSO

create_cell(2)
create_net(2)
create_port(2)
connect_net(2)
define_bus(2)
disconnect_net(2)
connect_pin(2)
connect_logic_zero(2)
connect_logic_one(2)
remove_port(2)
remove_cell(2)
remove_net(2)
insert_buffer(2)
remove_buffer(2)
size_cell(2)
undefine_bus(2)

UID-950 (error) Unsupported pin name '%s' or its synonym '%s'.

DESCRIPTION

This error message occurs when the pin name or its synonym has unsupported cg=haracters. Wildcards and regular expressions are not supported. Forward slash '/' is also not supported for simple pin name synonyms.

WHAT NEXT

Correct pin name or synonym string.

UID-951 (error) Pin name synonym '%s' exists already.

DESCRIPTION

This error message occurs when there is a conflict in pin name synonym. Multiple synonym definitions for a pin name synonym is not supported.

WHAT NEXT

Use '-force' switch to over-write the existing synonym. Use command report_pin_name_synonym to check the existing synonyms.

UID-952 (information) Synonym '%s' not found.

DESCRIPTION

This error message occurs when trying to delete a pin name synonym that does not exist.

WHAT NEXT

Use command report_pin_name_synonym to check the existing pin name synonyms.

UID-990 (error) Command '%s' is obsolete. Please use command '%s' instead.

DESCRIPTION

The command is obsolete. Please try the alternative command.

WHAT NEXT

Try the alternative command.

UID-991 (error) The driving cell %s has multiple inputs, and -from_pin is required when -input_transition_rise or -input_transition_fall is specified.

DESCRIPTION

This error message is displayed if only one of two options, which need to be specified together in case of multiple input cells, is specified.

WHAT NEXT

This error message is displayed if -input_transition_rise or -input_transition_fall is specified, without specifying -from_pin for driving cells with multiple input pins.

UID-992 (warning) Cannot find the top design for object %s.

DESCRIPTION

The top design for the given object could not be found. This may be caused either by a naming mismatch or an inconsistency in the hierarchy. As a result, the **setup** and **hold** attributes will not be propagated for this cell.

WHAT NEXT

Report this problem to Synopsys.

UID-993 (error) Cannot find the specified driving cell in memory.

DESCRIPTION

WHAT NEXT

Please use a driving cell from link library or from target library.

UID-995 (error) Cannot find the target library.

DESCRIPTION

The specified target library could not be found. This may be caused by incomplete search path. As a result, the **set_driving_cell** will not be performed.

WHAT NEXT

Please make sure the specified target library exists through search_path.

UID-996 (error) Cannot find the output pin '%s'.

DESCRIPTION

This error message is issued by the **set_driving_cell** command. You receive this message if the specified driving pin is not found or its type is not output. This could be caused by a spelling error or typo.

WHAT NEXT

Verify the correct name of the specified output pin, then reexecute **set_driving_cell** with the correct name.

SEE ALSO

set_driving_cell (2).

UID-997 (warning) The set_dont_touch_network command is used for clock %s, for which no sources are specified.

DESCRIPTION

This warning message occurs when the **set_dont_touch_network** command is used for a clock and the **dont_touch** attribute is assigned to the transitive fanout of the ports of the clock. The clock is created without specifying a list of ports, and the **set_dont_touch_network** command has no effect for this clock.

WHAT NEXT

This is only a warning message. No action is required.

Refer to the man pages for the **create_clock** command for more information.

SEE ALSO

create_clock(2)
set_dont_touch_network(2)

UID-998 (warning) Buffer tree at driver pin %s has cells or nets with dont_touch attribute.

DESCRIPTION

This warning message occurs when the **clean_buffer_tree** command is applied to a buffer tree that has buffers, inverters, or nets with the **dont_touch** attribute. The specified cells and the cells that follow will not be removed.

WHAT NEXT

This is only a warning message. No action is required.

Refer to the man page for the **clean_buffer_tree** command for more information.

SEE ALSO

clean_buffer_tree(2)
set_dont_touch(2)
set_dont_touch_network(2)

UID-999 (error) Must specify either %s or %s.

DESCRIPTION

This error message occurs when neither of the two mandatory options for a command are specified.

WHAT NEXT

Reissue the command and specify one of the two options in the error message.

UID-1000 (error) Invalid scenario name.

DESCRIPTION

This error is generated when providing and invalid scenario name.

WHAT NEXT

Use **all_scenarios** to see the names of the currently defined scenarios.

UID-1001 (error) Current scenario is not defined.

DESCRIPTION

This error is generated when current scenario is not defined.

WHAT NEXT

Use **all_scenarios** to see the names of the currently defined scenarios. Then invoke **current_scenario** to set the desired current_scenario.

UID-1002 (information) Cell %s is a special cell with always on pins and it is preserved with size_only attribute.

DESCRIPTION

The tool issues this message to inform that cells with always on pins are marked with size_only attribute. Preserving these cells during optimization ensures power management logic is synthesized correctly. Only cells that are in power down regions are considered. Also, cells that are marked dont_touch and cells that are already marked size_only are not considered. TCL variable mark_always_on_logic_size_only can be used to turn off size_only marking of such cells. The default value of this variable is true.

WHAT NEXT

If you want to turn off automatic marking of size_only attribute on such cells, set TCL variable mark_always_on_logic_size_only to false.

UID-1003 (warning) Driving cell was specified without the -library option. Using library_cell %s from library %s:%s.

DESCRIPTION

This warning message is displayed if the set_driving_cell command is issued without the -library option.

WHAT NEXT

Specify the library for the driving cell using the -library option. This is very important for multi voltage designs where library cell of a given name may be present in multiple libraries. It is important for user to check if the correct library cell was picked.

UID-1004 (error) Cannot use the '%s' option of save_mw_cel after ILM creation

DESCRIPTION

This error is seen when, after creating an ILM, you run **save_mw_cel** with an option that is not supported. Currently, this includes only the '-overwrite' options.

WHAT NEXT

The ’-overwrite’ option is not currently supported after **create_ilm** is run. A fresh version of the ILM view must be created.

SEE ALSO

create_ilm(2), save_mw_cel(2).

UID-1005 (error) Format ’%s’ is not a valid format.

DESCRIPTION

This error is generated when **write** command encounters an invalid write format. Please note that -power option works only for "verilog" format.

WHAT NEXT

Identify and correct format, then reinvoke the **write** command.

UID-1006 (information) Existing back annotation will be deleted.

DESCRIPTION

This message informs the user that the existing back annotation will be deleted.

WHAT NEXT

This is only an information message. No action is required.

UID-1007 (error) Static noise calculation requires ’ set_si_options -static_noise true ’ setting. Please set ’ set_si_options -static_noise true ’ and then run report_noise and report_noise_calculation.

DESCRIPTION

This error message occurs when the report_noise or report_noise_calculation is called without setting -static_noise option to true.

WHAT NEXT

Use 'set_si_options -static_noise true ' and then run report_noise and report_noise_calculation command.

UID-1008 (warning) Discarding all scenario specific information previously defined in this session.

DESCRIPTION

When issue the create_scenario command to create the first scenario, this warning will appear to remind you that any previously created scenario specific information will be discarded, and will not carry over into the context of the first scenario.

WHAT NEXT

No action is required, though you may want to review your script to ensure that scenario specific constraints are not erroneously created prior to the first create_scenario command.

SEE ALSO

create_scenario(2)

UID-1009 (warning) Current scenario changed to '%s'.

DESCRIPTION

This warning is generated when current scenario changes without explicit use of the **current_scenario** command.

WHAT NEXT

Confirm that the new current scenario is the correct scenario for your purposes.

UID-1010 (error) Invalid scenario '%s'.

DESCRIPTION

This error is generated when a non-existent scenario is specified.

WHAT NEXT

Use **all_scenarios** to see the names of the currently defined scenarios.

UID-1011 (error) Scenario is not active.

DESCRIPTION

This error is generated when a non active scenario is specified for current scenario. Only active scenarios can be set as the current scenario.

WHAT NEXT

Use **all_active_scenarios** to see the names of the currently active scenarios.

UID-1015 (warning) Resetting ’min_delta_delay’ to false when ’delta_delay’ is set to false.

DESCRIPTION

This warning message occurs when the **-delta_delay** option is being set to false while ’min_delta_delay’ option is set to true.

WHAT NEXT

This is only a warning message. No action is required.

UID-1016 (error) Cannot set ’min_delta_delay’ to true without having ’delta_delay’ option set to true.

DESCRIPTION

This error message is displayed if the option ’-min_delta_delay’ is specified to be true without having ’delta_delay’ set to true.

WHAT NEXT

Set both ’-min_delta_delay’ and ’-delat_delay’ options to true, and re-run the command.

UID-1017 (warning) Using the command-line option -nocase in fuzzy matching could cause a high runtime.

DESCRIPTION

This warning message occurs when using the **set_fuzzy_query_options** command with the **-nocase** option.

During fuzzy matching, switching the case-sensitivity mode using the command-line option **-nocase** forces fuzzy matching to reconfigure each time the mode is changed, which incurs a high runtime.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid incurring a high runtime do one of the following:

• Set the **find_ignore_case** variable to true so that fuzzy matching always works in case-insensitive mode.

• Set the **find_ignore_case** variable to false and do not use the **-nocase** option with any command, so that fuzzy matching always works in case-sensitive mode.

SEE ALSO

set_fuzzy_query_options(2)
find_ignore_case(3)

UID-1018 (error) Cannot set ’timing_window’ to true without having ’delta_delay’ or ’static_noise’ option set to true.

DESCRIPTION

This error message is displayed if the option ’-timing_window’ is specified to be true without having ’delta_delay’ or ’static_noise’ option set to true.

WHAT NEXT

Set ’-static_noise’ or ’-delat_delay’ option to true, and re-run the command.

UID-1019 (warning) Resetting ’timing_window’ to false when

’delta_delay’ and ’static_noise’ are both set to false.

DESCRIPTION

This warning message occurs when the **-delta_delay** option and **-static_noise** are being set to false while ’timing_window’ option is set to true.

WHAT NEXT

This is only a warning message. No action is required.

UID-1020 (error) the -all parameter can’t be used with other options.

DESCRIPTION

This error is generated when using the **set_active_scenarios** command, and both a list of scenarios and the **-all** parameter are specified.

WHAT NEXT

Either use **-all** or specify a list of scenario names.

UID-1021 (error) You must specify at least one active scenario.

DESCRIPTION

This error message occurs when using the **set_active_scenarios** command without specifying which scenarios to set active.

WHAT NEXT

Run the command again either using the **-all** option or specifying a list of scenario names.

SEE ALSO

set_active_scenarios(2)

UID-1022 (Information) Scenario %s is no longer active.

DESCRIPTION

This messages informs that a given scenario is now in the inactive state, and is not considered for optimization.

UID-1023 (Information) Scenario %s is now active.

DESCRIPTION

This messages informs that a given scenario is now in the active state, and is considered for optimization.

UID-1024 (Information) Removed Scenario %s .

DESCRIPTION

This messages informs that a given scenario was removed from memory. All its associated constraints are lost.

UID-1025 (Information) Mark scenario %s as CTS scenario.

DESCRIPTION

This messages informs that a given scenario was marked as CTS scenario, compile_clock_tree and optimize_clock_tree will work on CTS scenario if CTS scenario is marked.

UID-1026 (Information) Scenario %s is no longer a CTS scenario.

DESCRIPTION

This messages informs that a given scenario was no longer CTS scenario, it happened when another scenario is marked and CTS scenario or the CTS scenario is removed.

UID-1027 (information) CTS scenario %s is already the only active scenario.

DESCRIPTION

This messages issued during compile_clock_tree and optimize_clock_tree to informs that the CTS scenario is the only active scenario inthe flow.

UID-1028 (information) The current scenario has been switched to the CTS scenario %s.

DESCRIPTION

This messages is issued prior to clock tree optimization to inform you that the current scenario has been switched to the CTS scenario. Depending on the command, other scenarios may also be activated or deactivated. These are listed in the log file.

After this command is complete, the current and active scenarios will be restored.

UID-1029 (error) Can’t switch to CTS scenario %s, current scenario is %s

DESCRIPTION

This error is generated when compile_clock_tree and optimize_clock_tree trying to switch to CTS scenario but failed.

UID-1030 (error) Cannot restore current scenario to previous value %s, current value is %s

DESCRIPTION

This error is generated when compile_clock_tree and optimize_clock_tree trying to restore current scenario from CTS scenario but failed.

UID-1031 (information) Restore active scenarios, set current

scenario to previous value %s

DESCRIPTION

This message informs you that compile_clock_tree and optimize_clock_tree have successfully restored the active scenarios and current scenario.

UID-1032 (error) Can’t set both leakage-only and hold-only on current scenario!

DESCRIPTION

This error is issued by the **set_scenario_options** command when trying to set both leakage-only and hold-only options on current scenario. The command will return fail and the current setting will be unchanged.

WHAT NEXT

Use **report_scenarios** to check the current setting and fix the problem in script.

SEE ALSO

report_scenarios(2).

UID-1033 (information) Using default format ddc because -format was not specified.

DESCRIPTION

This information message occurs because the **-format** option of the **read_file** command was not specified. The file type cannot be inferred from the file name, so the default format of ddc is being used. It is good practice to always specify the format on the command line by using the **-format** option.

WHAT NEXT

This is an informational message. No action is required.

SEE ALSO

read_file(2)
UID-1034(n)

UID-1034 (information) Inferring file format %s based on file name extension(s).

DESCRIPTION

This information message occurs because the **-format** option of the **read_file** command was not specified. The command inferred the format based on the file name extension. It is good practice to always specify the format on the command line by using the **-format** option.

WHAT NEXT

This is an informational message. No action is required.

SEE ALSO

read_file(2)
UID-1033(n)

UID-1035 (error) Can’t set leakage-only or hold-only on scenario %s.

DESCRIPTION

This error is issued by the **set_scenario_options** command when trying to set leakage-only or hold-only options on an inactive scenario. The command will return fail and the current setting will be unchanged.

WHAT NEXT

Use **report_scenario_options** to check the current setting and fix the problem in script.

SEE ALSO

report_scenario_options(2). report_scenarios(2).

UID-1036 (warning) Can’t find scenario %s.

DESCRIPTION

This warning is issued by the **set_scenario_options** command when an invalid scenario

name is passed to the -scenarios option. The command will skip the entry and continue with other scenarios in the list.

WHAT NEXT

Use **all_scenarios** to check all valid scenario names and fix the problem in script.

SEE ALSO

all_scenarios(2). report_scenario_options(2).

UID-1037 (warning) Setting dynamic_power to false for scenario %s.

DESCRIPTION

This warning is issued by the **set_scenario_options** command when trying to set dynamic_power to true without setting setup to true or when setup is set to false with dynamic_power left to true. Dynamic power computation needs scenario options setup and dynamic_power both set to true, to work properly. The command will finish successfully but will force dynamic_power to false. Set dynamic_power and setup to true to avoid this warning and enable dynamic power.

WHAT NEXT

Use **report_scenario_options** to report the current settings and fix the problem in script.

SEE ALSO

report_scenario_options(2).

UID-1038 (error) Can’t set cts_mode to true for scenario %s.

DESCRIPTION

This error is issued by the **set_scenario_options** command when trying to set option cts_mode to true when either the scenario option setup or hold is set to false or option leakage_only or hold_only is set to true. The command will return fail and the current setting will be left unchanged.

WHAT NEXT

Use **report_scenario_options** to check the current settings and fix the problem in script.

SEE ALSO

report_scenario_options(2).

UID-1050 (error) Only %d character string is accepted as %s.

DESCRIPTION

The *-hierarchical_separators* option only accepts a list of single character strings; The *-bus_name_notations* option only accepts a list of two character strings.

WHAT NEXT

Fix the value of option *-hierarchical_separators* or *-bus_name_notations* and re-issue the command *set_query_options*.

UID-1051 (error) '%s' is not supported as %s.

DESCRIPTION

The *-hierarchical_separators* option does not accept the following characters: 0-9, a-z, A-Z, *, ?, \, +, (,), [,], ^. The *-bus_name_notations* option does not accept the following characters 0-9, a-z, A-Z, *, ?, \, +, ^. The *-bus_name_notations* option does not accept unpaired brackets such as "][", "(_".

WHAT NEXT

Fix the value of option *-hierarchical_separators* or *-bus_name_notations* and re-issue the command *set_query_options*.

UID-1052 (warning) %s is missing as %s. This may cause incorrect result and long runtime.

DESCRIPTION

'/' is often used as hierarchical separator for in-memory netlist; "[]" is often

used as bus name notation for in-memory netlist. Not including them in the fuzzy matching options may cause the program fail to find the object.

WHAT NEXT

Consider adding '/' in the **-hierarchical_separators** list, and "[]" in the **-bus_name_notations** list.

UID-1053 (error) Learning_effort must be one of: low, medium, high.

DESCRIPTION

WHAT NEXT

Fix the value of option *-learning_effort* and re-issue the command *set_query_options*.

UID-1054 (error) Only cell, pin, port and net are supported.

DESCRIPTION

WHAT NEXT

Fix the value of option *-class* and re-issue the command *set_query_options*.

UID-1055 (information) %d %s objects are matched according to fuzzy query options.

DESCRIPTION

This message is issued in verbose mode in case query had matched some object according to the options set by command *set_query_options*.

WHAT NEXT

UID-1056 (information) Fuzzy matching enabled. Please turn it

off once fuzzy matching is no longer needed.

DESCRIPTION

Fuzzy matching could slow down the program considerably, and use more memory. To avoid runtime and memory overhead, turn it off once it is no longer needed.

WHAT NEXT

UID-1057 (error) ’-reset’ option can not be used together with other options except for ’-show’.

DESCRIPTION

WHAT NEXT

UID-1058 (error) There must be at least 2 elements in %s list.

DESCRIPTION

WHAT NEXT

UID-1059 (information) Scenario %s either not exists or is inactive. %s will skip it.

DESCRIPTION

WHAT NEXT

UID-1060 (error) There must be at least 3 elements in %s list.

DESCRIPTION

This error is generated when there are not enough elements for -regsub option for

Design Compiler command ’set_fuzzy_query_options’.

WHAT NEXT

Check out the man page for Tcl Built-In regsub then reset the options for this.

UID-1061 (warning) ’-regsub’ option can not be used together with ’-exhaustive’ option, ’-regsub’ option will be ignored.

DESCRIPTION

When ’-exhaustive’ is specified, ’-regsub’ will not be supported for run time concern.

WHAT NEXT

Set one of the two options only and rerun the command.

UID-1062 (information) Object %s is found using matching pattern %s.

DESCRIPTION

The tool issues this message to inform that object is found with which pattern during fuzzy mathcing. This information can be used to double check the correctness of the SDC file sourcing.

WHAT NEXT

If you want to disable this message, turn off verbose mode by command set_fuzzy_query_options.

SEE ALSO

set_fuzzy_query_options (2).

UID-1063 (warning) Design %s doesn’t have scenario %s

DESCRIPTION

This warning is generated by **report_scenario** when a scenario exists in the session but the top level design doesn’t have that scenario. if the design is hierarchical, the scenario may exists in some hierarchical block. Or the scenario is create on other designs which has been closed. For hierarchical design, you may need to create the scenario for top-level design explicitly using **create_scenario**. Or, you may want to remove the scenario using **remove_scenario** to reduce memory.

UID-1064 (error) Save operation not allowed for ILM designs.

DESCRIPTION

This error occurred because the design being saved is an ILM design. ILM designs are not allowed to be saved with save_mw_cel.

WHAT NEXT

Use create_ilm to generate a new ILM view.

SEE ALSO

create_ilm(2).

UID-1065 (information) Overwrite is already the default. You do not need to specify this option.

DESCRIPTION

As of 2007.12, by default, save_mw_cel will overwrite a cell, so this option is no longer needed.

WHAT NEXT

You do not need to specify this option.

SEE ALSO

save_mw_cel(2).

UID-1072 (information) Object %s is found using matching pattern %s.

DESCRIPTION

The tool issues this message to inform that object is found with which pattern during fuzzy mathcing. This information can be used to double check the correctness of the SDC file sourcing.

WHAT NEXT

If you want to disable this message, turn off verbose mode by command set_fuzzy_query_options.

SEE ALSO

set_fuzzy_query_options (2).

UID-1098 (error) Need to specify one and only one port type.

DESCRIPTION

This error is generated when **set_output_clock_port_type** command without specifying correct port type.

WHAT NEXT

Please specify port type using one and only one option -clock or -data.

UID-1099 (error) Need to specify port_list or use -all option.

DESCRIPTION

This error is generated when **set_output_clock_port_type** command without correctly specifying port_list.

WHAT NEXT

Please specify port_list, or use -all option to apply the port type to all output ports.

UID-1100 (warning) Don’t apply this command on input port. Ignore it.

DESCRIPTION

This error is generated when user apply **set_output_clock_port_type** command on input port. Ignore this setting.

WHAT NEXT

UID-1101 (error) The design ’%s’ has physical/floorplan data and cannot be modified by the ’group’ command. Use the merge_fp_hierarchy command instead.

DESCRIPTION

The **group** command cannot be executed on a design with physical hierarchy.

WHAT NEXT

Please use merge_fp_hierarchy command instead.

SEE ALSO

merge_fp_hierarchy(2)

UID-1102 (information) This version of snapshot utility does not support MCMM design.

DESCRIPTION

This error message occurs when using the older version of snapshot utility on a MCMM design.

WHAT NEXT

Switch to using the newer version of snapshot utility by setting the variable enable_concise_qor_snapshot to TRUE (default).

SEE ALSO

create_qor_snapshot(2)
report_qor_snapshot(2)
remove_qor_snapshot(2)

UID-1103 (information) This newer version of snapshot utility does not support these options:

DESCRIPTION

This error message occurs when running the qor snapshot command with the above options

WHAT NEXT

User can ignore the message or re-run without the options.

SEE ALSO

create_qor_snapshot(2)
report_qor_snapshot(2)
remove_qor_snapshot(2)

UID-1104 (error) Not able to perform command due to read/write permission issue.

DESCRIPTION

Read/Write permission problem. There can be several reasons for this. The most common reasons are: the user does not have read/write permissions in the directory, the disk is full or the user already has a file with the same name which can’t be deleted.

WHAT NEXT

Try to create a file with the same name from the ICC shell. Fix any problem that you might encounter. Delete the file and invoke the icc_shell command again.

UID-1200 (error) cannot recognize the given value for option

'%s' in this SI command.

DESCRIPTION

check the command and give a valid value for the option.

UID-1201 (warning) Overriding result from previous set_ideal_network command on object %s.

DESCRIPTION

The previous setting of the ideal network on an object is being over-written.

WHAT NEXT

This is only a warning message. No action is required.

UID-1202 (warning) expecting %s objects of type %s.

DESCRIPTION

UID-1220 (error) Cannot find operating condition %s in library %s.

DESCRIPTION

This error message is displayed if the specified operating conditions can't be found in the library from -max_library or -min_library option of set_operating_conditions command.

WHAT NEXT

Specify correct operating condition which can be found in the library.

UID-1301 (error) The field '%s' has already been specified for

the current ’%s’

DESCRIPTION

This error occurs when a field is specified more than once for a given table. The error can also occur if the user does not include all fields during a table specification.

WHAT NEXT

Correct the AOCVM syntax by ensuring that each field is only specified once for a given table.

UID-1302 (error) The current table is missing one or more fields

DESCRIPTION

This error occurs when a table is found at the end of the aocvm file without the required number of fields.

WHAT NEXT

Correct the AOCVM syntax by adding the missing fields to the file.

UID-1303 (error) Expected to find a valid field name but found ’%s’.

DESCRIPTION

This error occurs when the parser cannot find a valid field name.

WHAT NEXT

Correct the AOCVM syntax by ensuring that each field is specified in the format
name: data
 where name is one of
version,table,distance,depth,object_spec,derate_type,delay_type,rf_type,object_type.

UID-1304 (error) Cannot specify '%s' for field '%s'.

DESCRIPTION

The data found in the AOCVM file is not valid for the given field.

WHAT NEXT

Check the AOCVM spec to see allowed values for the field and update the AOCVM file appropriately.

UID-1305 (warning) Cannot associate table with leaf cell '%s'.

DESCRIPTION

AOCVM does not support the association of AOCVM data with leaf cells.

WHAT NEXT

Associate AOCVM tables with hierarchical cells, library cells and designs only.

UID-1306 (warning) Cannot find any objects of type '%s' for specification '%s'.

DESCRIPTION

Could not find any objects for the given specification. The table is not annotated on any objects but parsing and annotation will not stop due to this warning.

WHAT NEXT

Check that the specification is correct.

UID-1307 (error) Expected table of size %d but found table of size %d.

DESCRIPTION

The size of the 2D AOCVM table must equal the number of depth indices by the number

of distance indices

WHAT NEXT

Correct the size of the table

UID-1308 (error) Cannot finish AOCVM file on a line continuation

DESCRIPTION

The AOCVM file ends with a line continuation. The parser expects more data but there is none.

WHAT NEXT

Remove the line continuation character

UID-1309 (error) Could not find the specified AOCVM file

DESCRIPTION

The AOCVM file could not be found

WHAT NEXT

Correct the name and path of the AOCVM file

UID-1310 (error) The field '%s' must be specified before '%s'

DESCRIPTION

While parsing an AOCVM 2D table a field cannot be set because another field has not been specified

WHAT NEXT

Change the order of the field specifications.

UID-1311 (error) The version '%s' is not valid. Allowable versions are '%s'

DESCRIPTION

An invalid version number has been specified

WHAT NEXT

UID-1312 (error) An aocvm file version must be specified.

DESCRIPTION

The version number is used for backward compatibility purposes if the AOCVM file format changes in the future. It does affect the results of the analysis.

The version of the aocvm file must be specified on the first line of the AOCVM file. e.g version:1.0

WHAT NEXT

Add the version information to the start of the AOCVM file.

UID-1313 (error) The %s array does not increase or decrease sequentially

DESCRIPTION

Sequential elements in the specified array must sequentially increase or decrease.

WHAT NEXT

Fix the array so that it sequentially increases or decreases.

UID-1314 (error) Negative values are not allowed

DESCRIPTION

Negative values are not allowed for the distance,depth arrays or in the 2D tables.

WHAT NEXT

Remove negative values from the AOCVM file.

UID-1315 (error) Cannot specify delay type %s with object type %s

DESCRIPTION

This combination of delay type and object types is not allowed as it makes no sense.

WHAT NEXT

Correct the AOCVM file to remove the invalid combination of delay type and object type.

UID-1316 (error) Cannot specify a non-monotonic derate table.

DESCRIPTION

This message is issued because the derate table specified in the message is incorrectly defined. The table has not been annotated.

The timing derates specified in each row and each column of the derate table must increase or decrease monotonically.

WHAT NEXT

Fix the specified table so that sequential elements in each row and each column of the table sequentially increase or decrease.

UID-1317 (error) Derate table variability is not decreasing with increasing depth.

DESCRIPTION

This message is issued because the derate table specified in the message is incorrectly defined. The table has not been annotated.

For a late derate table, the timing derates specified in each row of the derate table must decrease monotonically as depth increases. For an early derate table, the

timing derates specified in each row of the derate table must increase monotonically as depth increases.

No further restriction is placed on the table contents; however, typically, derate variability should be proportional to 1/sqrt(depth).

WHAT NEXT

Fix the specified table so that sequential elements in each row of the early (or late) table sequentially increase (or decrease) as depth increases.

UID-1318 (error) Derate table variability is not increasing with increasing distance.

DESCRIPTION

This message is issued because the derate table specified in the message is incorrectly defined. The table has not been annotated.

For a late derate table, the timing derates specified in each column of the derate table must increase monotonically as distance increases. For an early derate table, the timing derates specified in each row of the derate table must decrease monotonically as distance increases.

No further restriction is placed on the table contents; however, typically, derate variability should be proportional to distance.

WHAT NEXT

Fix the specified table so that sequential elements in each column of the early (or late) table sequentially decrease (or increase) as distance increases.

UID-1319 (information) Excluding ILMs from the list of designs to write.

DESCRIPTION

This message occurs when the **write_file** command detects one or more interface logic models (ILMs) in the requested set of designs to be written out. ILMs are not normally written with the **write_file** command and cannot be written out along with non-ILM designs.

However, you can write ILMs using the **write_file** command if all of the specified designs are ILMs.

WHAT NEXT

This is an information-only message. No action is required.

SEE ALSO

write_file(2)

UIDBG-1 (error) The attach ’%s’ does not exist.

DESCRIPTION

WHAT NEXT

UIDBG-2 (error) The object ’%s’ is not attached via the ’%s’ attach.

DESCRIPTION

WHAT NEXT

UIDBG-3 (error) More than one object is attached via the ’%s’

attach.

DESCRIPTION

WHAT NEXT

UIDBG-4 (error) No objects are attached via the ’%s’ attach.

DESCRIPTION

WHAT NEXT

UIDBG-5 (error) It’s illegal to specify both a library and a design.

DESCRIPTION

WHAT NEXT

UIDBG-6 (error) You must specify either a library or a design.

DESCRIPTION

WHAT NEXT

UIDBG-7 (error) You must invoke ’db_debug_start’ before issuing this command.

DESCRIPTION

WHAT NEXT

UIDPCM

UIDPCM-1 (error) ’%s’ is not a valid calc_mode.

DESCRIPTION

In DPCM, only "worst_case", "nominal" and "best_case" are valid calc_mode options.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

Error: "case" is not a valid calc_mode. (UIDPCM-1)

UIDPCM-2 (error) One or more rail voltage names or values are invalid in library ’%s’

DESCRIPTION

The set_dpcm_operating_condition requires that the command line arguments for -rail_voltages option assign voltage values to all rail voltages in the specified library. This message is issued when the following error condition is detected in the command line: - not enough entries for all rail voltages; - incorrect rail voltage name; - missing value for one or more rail voltages; - multiple values for one rail voltage;

WHAT NEXT

Use "report_dpcm_lib" command to get a list of valid rail voltage names in the library. And try the command again.

EXAMPLES

EXAMPLE MESSAGE

Error: One or more rail voltage names or values are invalid in library "test". (UID PCM-2)

UIDPCM-4 (warning) '%s' is not a valid level.Setting level to default level, performance. The valid levels are accurate and performance.

DESCRIPTION

In DPCM, only "performance" and "accurate" are valid level options.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

Error: "global" is not a valid level. Setting level to default level, performance. The valid levels are accurate and performance. (UIDPCM-4)

UIDPCM-5 (warning) '%s' is not a valid mode.Setting level to default mode,global. The valid modes are global and instance.

DESCRIPTION

In DPCM, only "global" and "instance" are valid mode options.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

Error: "performance" is not a valid mode. etting level to default mode,global. The valid modes are global and instance (UIDPCM-5)

UIDPCM-6 (error) DPCM Library '%s' not loaded.

DESCRIPTION

You receive this message if the **dpcm_libraries** variable contains the specified library but that library is not loaded. You can set the **dpcm_libraries** variable only

if a DPCM library is available for the specified library.

WHAT NEXT

Verify the correct spelling and path of the specified DPCM library in the **dpcm_libraries** variable. Set the **dpcm_rulepath** variable and others as specified by the dpcm vendor for the equivalent libraries specified in the **dpcm_libraries** variable.

SEE ALSO

dpcm_libraries (3), **dpcm_rulepath** (3), **dpcm_variables** (3).

UIDPCM-7 (error) '%s' is not a valid process factor.

DESCRIPTION

The process factor must be a non-negative floating point number no more than 100.0.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

Error: "-1" is not a valid process factor. (UIDPCM-7)

UIDPCM-8 (error) '%s' is not a valid voltage.

DESCRIPTION

The voltage must be a non-negative floating point number no more than 1000.0.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

Error: "-1" is not a valid voltage. (UIDPCM-8)

UIDPCM-9 (error) '%s' is not a valid tree_type.

DESCRIPTION

Only "worst_case_tree", "balanced" and "best_case_tree" are valid tree_type options.

WHAT NEXT

EXAMPLES

EXAMPLE MESSAGE

Error: "case" is not a valid tree_type. (UIDPCM-9)

UIDPCM-10 (warning) Invalid value '%s' for dpcm_slewlimit. The valid values are either FALSE or TRUE. Setting to default value, FALSE.

DESCRIPTION

You receive this message if the **dpcm_slewlimit** variable is set to some value other than *true* or *false*; these are the only allowed values. This message informs you that the variable is being set to *false*, its default value.

WHAT NEXT

If it is acceptable to you that the **dpcm_slewlimit** variable is set to *false*, no action is required on your part. Otherwise, set the variable to *true*.

SEE ALSO

dpcm_slewlimit (3), **dpcm_variables** (3).

UIDPCM-11 (warning) Invalid value '%d' for dpcm_debuglevel. The valid values are greater than or equal to zero. Setting to

default value, ’0’.

DESCRIPTION

You receive this message if the **dpcm_debuglevel** variable is set to a value that is not an integer of 0 or greater. This message informs you that the variable is being set to 0, its default value.

WHAT NEXT

If it is acceptable to you that the **dpcm_slewlimit** variable is set to to 0, no action is required on your part. Otherwise, set the variable to some value greater than 0.

SEE ALSO

dpcm_slewlimit (3), **dpcm_variables** (3).

UIDPCM-12 (warning) DPCM operating condition ’%s’ not found.

DESCRIPTION

You receive this warning message when the named operating condition was not found in the specified DPCM library.

WHAT NEXT

Use the **report_dpcm_operating_conditions** command to see the names of operating conditions available in the DPCM library.

UIDPCM-13 (error) The command requires the -temp option when the -default or -current options are not used.

DESCRIPTION

You receive this error message when the **-default** or **-current** option is not specified, and the **-temp** option is not specified.

WHAT NEXT

Re-execute the **create_operating_conditions** command with the **-temp** option, or specify the **-default** or **-current** option.

UIDPCM-14 (error) The command requires a rail voltage list when the options -default or -current are not used.

DESCRIPTION

You receive this error message when the **create_operating_conditions** command does not have the **-rail_voltages** option specified.

WHAT NEXT

Re-execute the **create_operating_conditions** command, and specify the **-rail_voltages** option.

UIDPCM-15 (warning) Invalid value '%s' for dpcm_arc_sense_mapping. The valid values are either FALSE or TRUE. Setting to default value, TRUE.

DESCRIPTION

You receive this message if the **dpcm_slewlimit** variable is set to some value other than *true* or *false*; these are the only allowed values. This message informs you that the variable is being set to *true*, its default value.

WHAT NEXT

If it is acceptable to you that the **dpcm_slewlimit** variable is set to *true*, no action is required on your part. Otherwise, set the variable to *false*.

SEE ALSO

dpcm_arc_sense_mapping(3), dpcm_variables (3).

UIED

UIED-1 (error) Bad file '%s' specified.

DESCRIPTION

WHAT NEXT

UIED-2 (error) Design '%s' already exists in file '%s'.

DESCRIPTION

WHAT NEXT

UIED-3 (error) Bad value specified for the -logic option.

DESCRIPTION

WHAT NEXT

UIED-4 (error) Must specify either reference name or -logic

option.

DESCRIPTION

WHAT NEXT

UIED-5 (error) Cell ’%s’ already exists in design ’%s’.

DESCRIPTION

WHAT NEXT

UIED-6 (error) Can’t find reference design or library cell ’%s’.

DESCRIPTION

WHAT NEXT

UIED-7 (error) Reference ’%s’ is not unique.

DESCRIPTION

WHAT NEXT

UIED-8 (error) Design ’%s’ can’t refer to itself.
This would cause recursive hierarchy.

DESCRIPTION

WHAT NEXT

UIED-9 (error) Can’t reference design ’%s’ in design ’%s’.

This would cause recursive hierarchy.

DESCRIPTION

WHAT NEXT

UIED-10 (error) A reference named ’%s’ already exists in design

’%s’.

DESCRIPTION

WHAT NEXT

UIED-11 (error) Must specify either cell list or -all option.

DESCRIPTION

WHAT NEXT

UIED-12 (error) Cell ’%s’ is not contained in design ’%s’.

DESCRIPTION

WHAT NEXT

UIED-13 (error) Net ’%s’ already exists in design ’%s’.

DESCRIPTION

WHAT NEXT

UIED-14 (error) Must specify either net list or -all option.

DESCRIPTION

WHAT NEXT

UIED-15 (error) Can’t remove net ’%s’; it’s part of a bus net.

DESCRIPTION

WHAT NEXT

UIED-16 (error) Net '%s' could not be found.

DESCRIPTION

WHAT NEXT

UIED-17 (error) Must specify only one net to connect.

DESCRIPTION

WHAT NEXT

UIED-18 (error) The first argument '%s' is not a net.

DESCRIPTION

WHAT NEXT

UIED-19 (error) Object '%s' is not a pin or port.

DESCRIPTION

WHAT NEXT

UIED-20 (error) Object '%s' is not contained in design '%s'.

DESCRIPTION

This error message occurs when you attempt to connect or disconnect a net to

specified pins that cannot be found.

WHAT NEXT

If you get this error message when executing the **connect_net** command, make sure that the pin-net pair is in the same logical hierarchy. Another option is to try to use the **connect_pin** command, which supports the connect operation if the pin-net pair is in a different logical hierarchy.

SEE ALSO

connect_pin(2)

UIED-21 (error) Object '%s' is already connected to net '%s'.

DESCRIPTION

WHAT NEXT

UIED-22 (error) Must specify either object list or -all option.

DESCRIPTION

WHAT NEXT

UIED-23 (error) Must specify only one net to disconnect.

DESCRIPTION

WHAT NEXT

UIED-24 (error) Object '%s' is not connected to net '%s'.

DESCRIPTION

This message is issued when either the object is not connected to the net or there are some constraints set on the object.

For ports, the object may have the attributes **driven_by_logic_one** or **driven_by_logic_zero** set on them. The ports can not be disconnected as long as these attributes are set on them.

The command **get_attribute** can be used to check if an attribute is set on an object. The command **remove_attribute** can be used to remove a specific attribute from an object.

WHAT NEXT

Please check to make sure the inputs are correct.

UIED-25 (error) Object '%s' is the wrong type.

Only nets, ports and pins are accepted.

DESCRIPTION

WHAT NEXT

UIED-26 (warning) Net ’%s’ is not connected to any objects.

DESCRIPTION

WHAT NEXT

UIED-27 (error) Port ’%s’ already exists in design ’%s’.

DESCRIPTION

WHAT NEXT

UIED-28 (error) Can’t remove port ’%s’; it’s part of a bus.

DESCRIPTION

WHAT NEXT

UIED-29 (error) Port ’%s’ could not be found.

DESCRIPTION

WHAT NEXT

UIED-30 (error) Must specify either port list or -all option.

DESCRIPTION

WHAT NEXT

UIED-31 (warning) The -logic option is ignored when explicit reference is given.

DESCRIPTION

WHAT NEXT

UIED-32 (error) Can’t %s for instance ’%s’ because design ’%s’ is instantiated %d times.

DESCRIPTION

This error indicates the current command can’t perform on this instance because it is instantiated more than once.

WHAT NEXT

Check your instance and reissue the command or you may continue.

UIED-33 (error) Can’t %s for instance ’%s’ which is a leaf cell.

DESCRIPTION

This error indicates the current command can’t perform on this instance which is a leaf cell.

WHAT NEXT

Check your instance and reissue the command or you may continue.

UIED-34 (error) Could not find parent cell ’%s’ for the creation of

’%s’.

DESCRIPTION

You receive this error message when you attempt to create either a cell, net or port in an instance which does not already. This command will not create any new hierarchy except the new leaf object which is specified in the command.

WHAT NEXT

Review the man page for the creation command being used, and try using current_instance to move to the instance within which you wish to create the new object. If you need to create levels of hierarchy, use the create_cell command to create each level one at a time.

UIED-35 (error) The instance ’%s’ is not a library cell.

DESCRIPTION

You receive this error message when you execute the **remove_cell** command and specify an instance to remove which is not a library cell.

WHAT NEXT

Use the **report_cell** command to examine the cells available for removal, and reissue the command with a library cell specified.

UIED-36 (error) Port ’%s’ is the last on a design, and may not be removed.

DESCRIPTION

This message is associated with the **remove_port** command and is issued upon an attempt to remove the last port on a design.

WHAT NEXT

Use the **report_port** command to examine the ports on a design.

UIED-37 (error) Objects ’%s’ and ’%s’ are at different levels in

the design hierarchy. Nets can be connected only to pins and ports at the same hierarchical level.

DESCRIPTION

You receive this message if you issue the **connect_net** command, and one or more pins or ports in the *object_list* is at a different hierarchical level from that of the specified net. **connect_net** can connect a net only to pins and ports within the same hierarchical level.

WHAT NEXT

Reexecute the **connect_net** command, and ensure that all pins and ports on the *object_list* are at the same hierarchical level as the net you specify. Or use the command connect_pin.

SEE ALSO

connect_net (2). **connect_pin** (2).

UIED-38 (error) Conflicting options '%s' and '%s' for size_cell.

DESCRIPTION

The two sets of options listed in the error message are conflicting. Options **-local**, **-fanin** and **-fanout** are for local sizing only, and cannot be mixed with any of the other options.

WHAT NEXT

Review the man page for **size_cell**, and change the options to remove the conflict.

UIED-39 (error) Pin %s is part of a library cell and cannot be removed.

DESCRIPTION

You receive this message if you issue the **remove_port** command and attempt to remove a port that belongs to a vendor library cell. You can remove ports only from non-vendor library designs. In xg mode, you specify the design or designs from which ports are to be removed by providing a path to the specific instance. The port or ports are removed from the design of the specified instance, after automatic

uniquification.

WHAT NEXT

If you want to remove a port from a design, reissue the **remove_port** command with a path to a hierarchical cell.

SEE ALSO

remove_port (2).

UIED-40 (error) All ports cannot be deleted from design %s.

DESCRIPTION

You receive this error message because you have attempted to remove all ports from the specified design. A design must contain at least one port. You can remove any port in any order until there is one remaining.

WHAT NEXT

Reexecute the command and specify the port or ports to be removed. Ensure that at least one port will remain in the design.

UIED-41 (error) Only one object is allowed when the -design argument is activated.

DESCRIPTION

You receive this error message because you have specified more than one object with the **-design** option. Only one object can be specified with this option.

WHAT NEXT

Reexecute the command with the **-design** argument and specify only one object.

UIED-42 (error) Design %s could not be found in the hierarchical

path to the specified object.

DESCRIPTION

You receive this error message if you have specified a design using the **-design** argument that could not be found in the path to the specified object.

WHAT NEXT

Verify that, in the hierarchical path to the specified object, there is a design specified using the **-design** switch. For example, in the command **remove_buffer T1/U1/G1/buf1 -design A**, one of the instances T1, U1, or G1 must be an instance of design A.

UIED-43 (error) Pin '%s' is an internal pin.

DESCRIPTION

This error message occurs when you attempt to connect or disconnect a net to specified pins which are internal pins.

WHAT NEXT

If you get this error message when executing the **connect_net** or **connect_pin** command, make sure that the pin specified is not an internal-pin. Internal pin is not supported in netlist editing, and should not be used for netlist connection.

SEE ALSO

UIED-44 (error) Must specify one supportd object.

DESCRIPTION

WHAT NEXT

Make sure specifies object is a net, leaf cell, or hierarchical pin/port

UIED-45 (error) %s is a SYNOPSYS reserved %s.

DESCRIPTION

WHAT NEXT

Please provide correct inputs to the command

UIED-46 (error) No object found for specified type.

DESCRIPTION

WHAT NEXT

Make sure the object specifies has the type matched to -type option

UIED-47 (error) Must specify only one object.

DESCRIPTION

WHAT NEXT

UIED-48 (error) Command %s does not support %s object %s.

DESCRIPTION

WHAT NEXT

See command man page for supported object types

UIED-49 (error) Bad value specified for the -range option.

DESCRIPTION

EXample: -range {0 3}

WHAT NEXT

UIED-50 (error) The %s '%s' is of direction inout. Ports/pins of direction inout is not allowed as an argument to connect_pin.

DESCRIPTION

The connect_pin command does not take a port/pin which has a direction inout.

WHAT NEXT

UIED-51 (error) The %s '%s' and %s '%s' of direction out cannot be connected.

DESCRIPTION

Either connect_pin command is issued with two pins/ports which has a direction out or both of them are connected to a net which already has a driver pin.

WHAT NEXT

UIED-52 (information) The pins/ports are already connected. Nothing to do.

DESCRIPTION

The connect_pin command has been issued and the pins/ports are already connected.

WHAT NEXT

UIED-53 (information) Removing %s from the input to

connect_pin since it is already connected to %s.

DESCRIPTION

Some of the pins/ports passed as an argument to connect_pin command are already connected to each other. Hence removing one of the pins/ports.

WHAT NEXT

UIED-54 (error)The port_name is not specified. Please re-issue the command with -port_name option.

DESCRIPTION

The command connect_pin has been issued without specifiying a port_name. The -port_name option is required when the connection has to be made between pins/ports from different sub designs.

WHAT NEXT

Re-issue the command with -port_name option.

UIED-55 (error)The %s '%s' is already connected to a net.

DESCRIPTION

The command connect_pin has been issued with a pin or port specified in the to_list which is already connected to a net.

WHAT NEXT

Re-issue the command after disconnecting the pin or port.

UIED-56 (error)The -only_physical option is not supported in IC Compiler.

DESCRIPTION

IC Compiler automatically examines the pins on the specified library cell, and if

all the pins are power/ground then that cell becomes physical only, that is, the cell is put in the Milkyway database, but is not part of the timing design used by optimization and, for instance, does not appear in Verilog outpout.

The user cannot determine that a cell will be physical only. The library analysis does that.

Please be aware that **connect_net** and **disconnect_net** cannot be used to attach physical only cells. **connect_logic_zero** and **connect_logic_one** may be used.

WHAT NEXT

UIED-57 (error) Must specify at least one tie cell.

DESCRIPTION

WHAT NEXT

UIED-58 (error) Pin %s is already disconnected

DESCRIPTION

Pin is not connected.

WHAT NEXT

Pin is not connected. There is no net on this pin to be edited.

UIED-61 (error) Failed to disconnect %s '%s'.

DESCRIPTION

Failed to disconnect pin or port properly.

WHAT NEXT

Check the inputs and try the command with correct inputs. If problems persist, report the problem to Synopsys

UIED-62 (error) Failed to reconnect %s '%s'.

DESCRIPTION

Failed to reconnect pin or port properly.

WHAT NEXT

Check the inputs and try the command with correct inputs. If problems persist, report the problem to Synopsys

UIED-63 (error) only PG nets are supported by this command.

DESCRIPTION

change_tie_connection can only be used to reconnect the existing connection to a new PG net.

WHAT NEXT

Please provide correct inputs to the command

UIED-64 (error) %s is not connected to a PG net.

DESCRIPTION

change_tie_connection can only be used to reconnect the existing connection of pins connected to a PG net to a new PG net.

WHAT NEXT

Please provide correct inputs to the command

UIED-65 (error) PG leaf pin is not supported by this command.

DESCRIPTION

change_tie_connection can only be used to reconnect the existing connection for signal pins connected to a PG net.

WHAT NEXT

Please provide correct inputs to the command

UIED-66 (error) Internal error - %s.

DESCRIPTION

Internal error.

WHAT NEXT

Report the problem to Synopsys

UIED-67 (error) Can not connect a PG net to leaf level output pin.

DESCRIPTION

Leaf level output pins are drivers and connecting them to a PG net would be considered a short. Therefore such connections are not allowed.

WHAT NEXT

Please provide correct inputs to the command

UIED-68 (error) Must specify only one net to reconnect.

DESCRIPTION

WHAT NEXT

UIED-69 (error) No net specified.

DESCRIPTION

change_tie_connection requires a valid net when -net option is used

WHAT NEXT

Please provide correct inputs to the command

UIED-70 (error) Must provide option '%s' or '%s'.

DESCRIPTION

The mentioned options are required in the command.

WHAT NEXT

Please re-issue the command with correct options.

UIED-71 (error) The argument '%s' of option -source is not a valid driver pin.

DESCRIPTION

The pin or port specified as the source of switch network is not of correct type.

WHAT NEXT

Please re-issue the command with valid pin or port as source.

UIED-72 (error) The required option -direction is not specified with -mode daisy.

DESCRIPTION

The option -direction is required in -mode daisy of the command connect_power_switch when using -voltage_area option without -object_list.

WHAT NEXT

Please re-issue the command with options.

UIED-73 (information) Connecting source '%s' to '%d' cells in

'%s' mode.

DESCRIPTION

The command connect_power_switch is performing the connections on the specified number of cells.

WHAT NEXT

UIED-74 (warning) Source has no location, the starting switch cell is choosen arbitrarily.

DESCRIPTION

The source port or pin has no location , thus the nearest switch from the source cannot be found.

WHAT NEXT

UIED-75 (error) %d out of %d cells are invalid for daisy-chain mode,missing switch/acknowledge pins.

DESCRIPTION

The arguments to -object_list contains switch cells that do not have either the switch pins or acknowledge pins for the daisy chain connections.

WHAT NEXT

Please re-issue the command with valid object list.

UIED-78 (warning) No %s matched the %s specification.

DESCRIPTION

No matching objects were found matching the input specification

WHAT NEXT

Please provide correct inputs to the command

UIED-79 (error) No pins or ports specified.

DESCRIPTION

change_tie_connection requires at least one pin or port to work on

WHAT NEXT

Please provide correct inputs to the command

UIED-80 (error) Other side of hierarchical pin is connected to incompatible net.

DESCRIPTION

This error would occur if the net provided as input to change_tie_connection is Power and the other side of the hierarchical pin is connected a Ground net or vice versa.

WHAT NEXT

Please provide correct inputs to the command

UIED-81 (error) Can not connect a PG net to a hierarchical %s, connected to a signal net on the other side

DESCRIPTION

This error would occur if change_tie_connection is used to connect a PG net in following cases - Connecting to a output hierarchical pin, which is connected to a signal net on the inside - Connecting to a input hierarchical pin, which is connected to a signal net on the outside Both the cases would result in two drivers being connected together, if the connection is allowed

WHAT NEXT

Please provide correct inputs to the command

UIED-82 (warning) Option *hier_cell_list* is ignored when option -top is given.

DESCRIPTION

WHAT NEXT

UIED-83 (error) Option *-type* has Invalid object type.

DESCRIPTION

WHAT NEXT

Please specify cell, net, or port for -type option

UIED-84 (error) Pins of library cells can not be renamed.

DESCRIPTION

WHAT NEXT

UIED-85 (error) Cannot change the name of a leaf cell pin.

DESCRIPTION

Leaf pin names are defined in libraries and cannot be changed in design by editing commands.

WHAT NEXT

Do not specify a leaf cell pin name that is defined in libraries.

UIED-86 (error) Cannot change the name of a hierarchical cell.

DESCRIPTION

Only leaf cell instance name can be changed.

WHAT NEXT

UIED-87 (error) No valid leaf cell specified.

DESCRIPTION

WHAT NEXT

UIED-88 (warning) Library cell used for cell %s, is from the library %s and not from library %s

DESCRIPTION

The library cell used for the cell, has been selected from the library which matches the MCMM and/or MV constraints, for the scope where the cell exists.

The library differs from the one you specified, as the library specified does not match the MCMM and/or MV constraints.

WHAT NEXT

This is more of a informational message and no action is required.

UIED-89 (warning) Library cell matching constraints can not be found. Library cell from the library %s is being used

DESCRIPTION

No library cell matching MV constraints could be found. Instead a library cell found in the link libraries is being used. Please run **check_mv_design** command and fix all reported issues.

WHAT NEXT

This is more of a informational message and no action is required, at this point but all MV errors should be fixed.

UIED-91 (error) Pin %s is on a hierarchical instance

DESCRIPTION

The commands connect_logic_zero or connect_logic_one can be used only for leaf cell pins.

WHAT NEXT

Use change_tie_connection for the appropriate operation on this pin

UIED-92 (error) Top level port %s can not be used with this command

DESCRIPTION

The commands connect_logic_zero or connect_logic_one can be used only for leaf cell pins.

WHAT NEXT

Use change_tie_connection for the appropriate operation on this port

UIED-93 (error) Must specify at least one hierarchy cell.

DESCRIPTION

WHAT NEXT

UIED-94 (error) %s ’%s’ already exists in cell ’%s’.

DESCRIPTION

WHAT NEXT

UIED-95 (error) The -create_net option requires either -power or

-ground, but not both.

DESCRIPTION

WHAT NEXT

UIED-96 (error) Must specify only one net.

DESCRIPTION

WHAT NEXT

UIED-97 (error) %s is not a hierarchical cell.

DESCRIPTION

WHAT NEXT

UIED-98 (error) %s %s does not exist in design.

WHAT NEXT

UIED-99 (error) Options %s and %s cannot be used simultaneously.

WHAT NEXT

UIED-100 (error) Net name '%s' for create_pg_network must ba

a base name and cannot contain '/'.

DESCRIPTION

Only base net name is needed. For example, if you want to create net 'M1/VDD' in hierarchical cell instance 'M1', you only need to specify 'VDD'. The command automatically creates the net in 'M1'.

WHAT NEXT

UIED-101 (error) Failed to connect %s '%s'.

DESCRIPTION

WHAT NEXT

UIED-102 (error) PG net can not connect to a tie hier pin.

DESCRIPTION

A Power net is always a driver and a Ground net is a sink. A Tie hier pin is also a driver. Connecting a power net to a tie hier pin is same as connecting two drivers while connecting the tie hier pin to ground would be a short. Therefore such connections are not allowed.

WHAT NEXT

UIED-103 (error) Tie net can be connected only to a signal hier pin.

DESCRIPTION

A tie net is a driver. A tie hier pin is also a driver. A power hier pin is a driver as well. Therefore a tie net can not be connected to either of those hier pins. Connecting a tie net to a ground hier pin would be a short, So a tie net can connect to signal leaf pins or signal hier pins only.

WHAT NEXT

UIED-104 (error) Can not connect a %s net to leaf level PG pin.

DESCRIPTION

Only PG nets can be connected to PG pins of leaf level instances

WHAT NEXT

UIED-105 (error) No objects specified to connect to.

DESCRIPTION

Valid pins or ports must be provided for connect_net to work.

WHAT NEXT

UIED-106 (error) Failed to disconnect %s '%s'.

DESCRIPTION

WHAT NEXT

UIED-107 (error) Reference of a standard cell can not be changed to a physical only cell.

DESCRIPTION

The reference of a standard cell can be changed to another standard lib cell only. It can not be changed to a physical only library cell.

WHAT NEXT

UIED-108 (error) Can not update reference for cell %s, in MW database.

DESCRIPTION

Internal error.

WHAT NEXT

UIED-109 (error) %s net can not connect to %s of a %s hier pin.

DESCRIPTION

A tie or PG net can only be a driver. So such a net can only be connected to either inside of a output hierarchical pin or outside of a input hierarchical pin.

WHAT NEXT

Please provide correct inputs to the command

UIED-110 (error) Reference of a physical only cell can not be changed to a standard cell.

DESCRIPTION

The reference of a physical only cell can be changed to another physical only lib cell only. It can not be changed to a logical library cell.

WHAT NEXT

UIED-111 (error) Can not connect a %s net to leaf level output

pin.

DESCRIPTION

A tie or PG net can only be a driver. So such a net can not be connected to a leaf level output pin.

WHAT NEXT

Please provide correct inputs to the command

UIED-112 (error) %s pin %s is a PG pin or a hierarchical pin connected to o a PG or tie net.

DESCRIPTION

connect_pin can only connect signal pins and unconnected hierarchical pins or hierarchical pins connected to signal nets.

WHAT NEXT

Please provide correct inputs to the command

UIED-113 (error) Port %s can not be connected to a PG net.

DESCRIPTION

Primary ports can not be connected to PG nets.

WHAT NEXT

Please provide correct inputs to the command

UIED-114 (error) No valid net specified.

DESCRIPTION

This command requires a valid net to work on.

WHAT NEXT

Please provide correct inputs to the command

UIED-115 (error) Default tie %s net can not connect to inside of a hier pin or a top level port.

DESCRIPTION

The default tie nets SNPS_LOGIC1 and SNPS_LOGIC0 are special nets inside ICC. They correspond to 1'b1 and 1'b0 in terms of verilog. There is no valid representaion in verilog for such connections. Only named tie nets can be connected in such manner.

WHAT NEXT

Please provide correct inputs to the command

UIED-116 (error) No PG net specified.

DESCRIPTION

recover_tie_connection requires valid PG nets when -net option is used.

WHAT NEXT

Please provide correct inputs to the command.

UIED-117 (error) Net '%s' is not a PG net.

DESCRIPTION

recover_tie_connection requires valid PG nets when -net option is used.

WHAT NEXT

Please provide correct inputs to the command.

UIED-118 (error) No hier cell instance specified.

DESCRIPTION

recover_tie_connection requires valid hier cell instances when -cell option is used.

WHAT NEXT

Please provide correct inputs to the command.

UIED-119 (error) '%s' is not a hier cell instance.

DESCRIPTION

recover_tie_connection requires valid hier cell instances when -cell option is used.

WHAT NEXT

Please provide correct inputs to the command.

UIED-120 (error) A %s net can not connect to a hierarchical pin connected to a %s net on the other side.

DESCRIPTION

A Power or Ground net can only connect to a hierarchical pin connected on the other side, if the net on the other side is of the same type - power or ground.

WHAT NEXT

Please provide correct inputs to the command

UIED-121 (error) Can not change link for hierarchical instance %s.

DESCRIPTION

The change_link command can only work on leaf level instances. The reference of hierrachical instances can not be changed using change_link.

WHAT NEXT

Please provide correct inputs to the command

UIED-122 (error) %s %s is not connected to a PG net.

DESCRIPTION

change_tie_connection can only be used to reconnect the existing connection of pins connected to a PG net to a new PG net.

WHAT NEXT

Please provide correct inputs to the command

UIED-123 (error) Cannot find the specified reference %s.

DESCRIPTION

The specified reference can not be found in any reference library path

WHAT NEXT

Please provide correct inputs to the command

UIED-124 (error) Unsupported view %s specified for "-view" option.

DESCRIPTION

The view specified is not supported. Only FRAM and CEL views are supported by this command.

WHAT NEXT

Please provide correct inputs to the command

UIED-125 (error) No library cell found for physical only library

cell ’%s’.

DESCRIPTION

No library cell matching the specified reference was found in the db library. The library cell exists in FRAM library.

WHAT NEXT

Please update the db library to have a reference cell matching this physical only cell.

UIED-126 (error) Pin %s is part of a library cell. Its bus property cannot be modified.

DESCRIPTION

You receive this message if you issue the **define_bus** command and attempt to manipilate a port that belongs to a vendor library cell. You can remove ports only from non-vendor library designs.

WHAT NEXT

If you want to define bus for a port from a design, reissue the **define_bus** command with a path to a hierarchical cell.

SEE ALSO

remove_port (2).

UIED-127 (error) Cannot define %s bus ’%s’; it already exists with %s.

DESCRIPTION

WHAT NEXT

Run undefine_bus and reissue define_bus.

UIED-128 (error) Can’t define %s bus ’%s’; %d is not within start index %d and end index %d.

DESCRIPTION

WHAT NEXT

Change start or end index.

UIED-129 (information) %s bus ’%s’ is already bit blasted.

DESCRIPTION

WHAT NEXT

UIED-130 (information) ’%s’ has no bus to be %s.

DESCRIPTION

WHAT NEXT

UIED-131 (error) Can’t define %s bus ’%s’; only %d bits between %d and %d exist in database.

DESCRIPTION

WHAT NEXT

Change start or end index. Or, create additional objects.

UIED-132 (error) Internal error in source file %s at line %d, error

code %d.

DESCRIPTION

This is an internal error.

WHAT NEXT

Report the problem to Synopsys

UIED-133 (error) cannot do the manual mapping because %s.

DESCRIPTION

This error occurs when manual spare cell mapping fails for the following reasons:

1. The cell eco_status is not eco_add
2. The target spare cell is not a real spare cell
3. The cell and spare cell do not have the same master name

WHAT NEXT

Please check if your cell and spare cell fulfill the mapping need.

SEE ALSO

map_freeze_silicon(2)

UIED-134 (error) Invalid map entry: %s.

DESCRIPTION

This error occurs when the mapping file has following errors:

1. extra field
2. missing field
3. the same cell appears more than once

WHAT NEXT

Please check your mapping file according to the line number and specific message.

Mapping File Format:

```
cell_1   spare_cell_1
cell_2   spare_cell_2
        ...      ...
```

SEE ALSO

map_freeze_silicon(2)

UIED-135 (information) Errors below occur at line %d.

DESCRIPTION

This information message specifies the line number where errors occur.

WHAT NEXT

UIED-136 (error) cannot remove hierarchical cells in freeze silicon mode.

DESCRIPTION

If specify the option -freeze_silicon, it could not remove hierarchical cells.

WHAT NEXT

Please check if the cells you specified contain hierarchical cells.

UIED-137 (error) the option -all and -freeze_silicon are mutually exclusive.

DESCRIPTION

It cannot specify the options -all and -freeze_silicon at the same time.

WHAT NEXT

UIED-138 (error) cannot replace the cell with gate array master

type with the spare cell without it, and vice versa.

DESCRIPTION

WHAT NEXT

UIED-139 (error) cannot replace the cell with the spare cell: They don’t have the same gate array master type id.

DESCRIPTION

The cell and spare cell must have the same gate array master type id.

WHAT NEXT

UIED-140 (error) cannot replace the gate array cell with the spare gate array cell: The width of cell is larger than the width of spare cell.

DESCRIPTION

The width of the cell must be less than or equal to the width of the spare cell.

WHAT NEXT

UIED-142 (error) Object ’%s’ is not a pin.

DESCRIPTION

WHAT NEXT

UIED-143 (error) Targeted pin: %s fails to find a net segment of

the input net network in the same hierar chical level.

DESCRIPTION

WHAT NEXT

UIG

UIG-1 (error) Unable to create %s property for setup data.

DESCRIPTION

This error message occurs when the **search_path** and **link_library** variables and related setup data for this run cannot be saved on the current CEL view.

WHAT NEXT

Make sure that you have write permission for the CEL view and then run the command again.

UIG-2 (error) Cannot get cellId for the current design.

DESCRIPTION

This error message occurs when there is an open CEL view, but the tool cannot obtain the CEL view’s identification.

WHAT NEXT

This is an internal error. Contact the Synopsys Customer Support Center by sending an email message to support_center@synopsys.com.

UIG-3 (error) Library is opened in read only mode.

DESCRIPTION

This error message occurs when the the design library is opened in read only mode. In this mode, the CEL view cannot be saved and new CEL views cannot be created.

WHAT NEXT

Close the library and reopen it without the read only option.

UIG-4 (error) Cell is opened in read only mode.

DESCRIPTION

This error message occurs when the the design CEL view is opened in read only mode. The design cannot be saved in this mode.

WHAT NEXT

Save the design as a new CEL view using the **-as** switch.

UIG-5 (information) Saved design named %s.

DESCRIPTION

This information message advises you that the design has been saved successfully.

WHAT NEXT

This is an informational message only. No action is required.

UIG-6 (error) Failed to save design %s.

DESCRIPTION

This error message occurs when the tool fails to save the specified design.

WHAT NEXT

Check any error messages issued before this one. Make the necessary corrections and then run the command again.

UIG-7 (error) No CEL view exists in memory. Use the -as option to specify the CEL view name.

DESCRIPTION

This error message occurs when the initial design was read from ASCII input (such as Verilog or .db), so a CEL view does not yet exist.

WHAT NEXT

Save the design as a new CEL view using the **-as** switch.

UIG-8 (error) A Milkyway design library must be specified.

DESCRIPTION

This error message occurs when the design library has not already been opened.

WHAT NEXT

Specify the design library using **-library** option to the **open_mw_cel** command.

You can also open the library with the **open_mw_lib** command before running **open_mw_cel**.

SEE ALSO

open_mw_cel(2)
open_mw_lib(2)

UIG-9 (error) Cannot get libId for current library.

DESCRIPTION

This error message occurs when the design library cannot be found. The library must be open for this command to run properly.

WHAT NEXT

Use the **open_mw_lib** command to open the library and rerun the command.

SEE ALSO

open_mw_lib(2)

UIG-10 (Information) AUTO-RESTORE: Setting variable %s to

%s.

DESCRIPTION

This message is issued when the library setup for the MW CEL is being restored from previously saved values, while opening the MW CEL. You can set the variable **auto_restore_mw_cel_lib_setup** to false if you do not want the setup to be restored from save values.

WHAT NEXT

This is for information only. Please set this variable to a different value if you want to override the current value.

UIG-11 (error) Invalid cell name specified.

DESCRIPTION

This error message occurs when the cell name being specified to save the CEL is not valid.

WHAT NEXT

Use a CEL name without any "." in the name. The only execption is if the name is specified with the extension ".CEL". For example, abc.CEL is valid name but abc.new is not.

UIG-12 (error) Cannot set scan type on pin %s.

DESCRIPTION

This error message occurs when the **set_scan_pin_type** command is not able to set the scan type on the pin or physical lib pin specified as input.

WHAT NEXT

Make sure that a valid pin is specified. If a physical lib pin is specified, then the corresponding physical lib cell must be instantiated in the design.

UIG-13 (Information) Scan type on pin %s, is being changed

from %s to %s.

DESCRIPTION

This message is issued when the input pin to the command fset_scan_pin_type has the scan pin type already set to a different value.

WHAT NEXT

This is for information only.

UIG-14 (error) Cannot remove scan type from pin %s.

DESCRIPTION

This error message occurs when the **remove_scan_pin_type** command is not able to remove the scan type from the pin or physical lib pin specified as input.

WHAT NEXT

Make sure that a valid pin is specified. If a physical lib pin is specified, then the corresponding physical lib cell must be instantiated in the design.

UIG-15 (Information) Scan type %s removed from pin %s.

DESCRIPTION

This message is issued when the scan pin type of the input pin to the command fremove_scan_pin_type is successfully removed.

WHAT NEXT

This is for information only.

UIG-16 (error) Type must be one of in or out.

DESCRIPTION

The value for type argument in the command **set_scan_pin_type** must be either in or out.

WHAT NEXT

Make sure that a correct value is specified.

UIG-17 (error) No CEL is open, please open a CEL first.

DESCRIPTION

A Milkyway CEL must be opened before running the command **set_scan_pin_type** or **remove_scan_pin_type**

WHAT NEXT

Open a Milkyway CEL and rerun the command

UIG-18 (error) No pin specified.

DESCRIPTION

This error message occurs when neither a pin nor a physical lib pin is specified, while running the **set_scan_pin_type** or **remove_scan_pin_type** command

WHAT NEXT

Make sure that a valid pin is specified.

UIG-19 (error) Specified reference cel %s is not instantiated in the design.

DESCRIPTION

This error message occurs when a physical lib pin is specified as input to the **set_scan_pin_type** command but the corresponding reference cel is not instantiated in the open Milkyway design.

WHAT NEXT

Make sure that the physical lib cell is instantiated in the design.

UIG-20 (warning) Specified reference cel %s is not instantiated in the design.

DESCRIPTION

This warning message occurs when a physical lib pin is specified as input to the **remove_scan_pin_type** command but the corresponding reference cel is not instantiated in the open Milkyway design. The pin does not have the scan_type property set so it can not be removed anyway

WHAT NEXT

Make sure that the physical lib cell is instantiated in the design.

UIG-21 (error) Cannot set the current instance to %s.

DESCRIPTION

This error message occurs when the owning cel-id of the new current_instance is not same as the current top cel. Current instance can only be set to a instance owned by the top cel.

WHAT NEXT

SEE ALSO

current_mw_cel

UIG-22 (error) Cannot open file %s for %s.

DESCRIPTION

This error message occurs when the options file can not be opened for read or write

WHAT NEXT

SEE ALSO

UIG-30 (error) Cannot find cell: %s.

DESCRIPTION

This error message occurs when dump out internal DataModel, but the tool cannot obtain the cell.

WHAT NEXT

This is an internal error. Contact the Synopsys Customer Support Center by sending an email message to support_center@synopsys.com.

UIG-31 (error) Cannot find net: %s.

DESCRIPTION

This error message occurs when dump out internal DataModel, but the tool cannot obtain the net.

WHAT NEXT

This is an internal error. Contact the Synopsys Customer Support Center by sending an email message to support_center@synopsys.com.

UIG-32 (error) Fail at file %s line %d.

DESCRIPTION

This error message occurs while handling the file at special line.

WHAT NEXT

SEE ALSO

UIL-0 (information) Note that the ".synopsys_lc.setup" init file of lc_shell is a subset of the dc_shell ".synopsys_dc.setup" init file. If a command other than an lc_shell command is encountered in the init file, an error message is issued and the processing might terminate. Refer to the Library Compiler manuals for supported commands.

DESCRIPTION

During the initialization phase, the Library Compiler command line tool **lc_shell and the graphical tool library_compiler** read in a setup file **.synopsys_lc.setup. Both tools perform a subset of the Design Compiler dc_shell commands. If a dc_shell command is encountered such as read_design command), Library Compiler tools issue an error. Depending on the semantics of the command read, it might terminate.**

WHAT NEXT

Refer to the Library Compiler User Guide and Reference Manuals for supported commands.

UIL-1 (warning) Overwriting an old symbol library '%s' file with a new one.

DESCRIPTION

The symbol library, specified in your **read_lib** command, already exists in the database. The old library is deleted from the database and replaced by the new one. This message is generated when

- Reading a symbol library directly or
- Reading an EDIF file with the "-symbol option" set to the same symbol filename

WHAT NEXT

Use **list -lib** to find all available libraries. No action is required if you decide to overwrite a library name reported by **list -lib**.

EXAMPLES

```
Reading a symbol library explicitly:

   lc_shell> read_lib uil1_symbol.slib
             Reading '/tmp/uil1_symbol.slib' ...
             Symbol library 'uil1' read successfully
   lc_shell> read_lib uil1_symbol.slib
             Reading '/tmp/uil1_symbol.slib' ...
             Warning: Overwriting an old symbol library '/tmp/
uil1.sdb' file with a  new one. (UIL-1)

Reading a symbol library though the EDIF file:

   lc_shell> read_lib -format edif uil1.edif -symbol uil1_symbol.slib
             Reading '/tmp/uil1_symbol.slib' ...
             Symbol library 'uil1' read successfully
   lc_shell> read_lib -format edif uil1.edif -symbol uil1_symbol.slib
             Reading '/tmp/uil1_symbol.slib' ...
             Warning: Overwriting an old symbol library '/tmp/
uil1.sdb' file with a new one. (UIL-1)
```

EXAMPLE MESSAGE

```
Warning: Overwriting an old symbol library '/tmp/
uil1.sdb' file with a new one. (UIL-1)
```

UIL-2 (warning) Overwriting an old technology library '%s' file with a new one.

DESCRIPTION

The technology library, specified in the **read_lib** command, already exists in the database. The old library is deleted from the database and is replaced by the new one.

WHAT NEXT

Use **list -lib** to find all available libraries. No action is required if you decide to overwrite a library name reported by **list -lib**.

EXAMPLES

```
lc_shell> read_lib uil2.lib
  Reading '/tmp/uil2.lib' ...
  Technology library 'uil2' read successfully
lc_shell> read_lib uil2.lib
  Reading '/tmp/uil2.lib' ...
  Warning: Overwriting an old technology library '/tmp/
```

uil2.db' file with a new one. (UIL-2)

EXAMPLE MESSAGE

```
Warning: Overwriting an old technology library '/tmp/
uil2.db' file with a new one. (UIL-2)
```

UIL-3 (warning) The '%s' library has not been read in yet.

DESCRIPTION

The command issued tries to access a library that does not exist in the database. A typo in the library name can also result in this problem. Any of the following commands might trigger the generation of this warning: **add_module, compare_lib, write_lib, report_lib and update_lib**.

WHAT NEXT

Use **list -lib** to find all available libraries. Make sure the library name is among the ones being reported by **list -lib**. Otherwise, load the library into the database using **read** for a db file, or **read_lib** for a library source file, then reissue the command.

EXAMPLE MESSAGE

```
Warning: The 'uil3' library has not been read in yet. (UIL-3)
```

UIL-4 (error) The '%s' library source file is not found.

DESCRIPTION

The library source file is not found either because

- The file is not in the search_path, assuming that the full path is not specified or,
- There is a typo in the filename.

WHAT NEXT

Issue the command with the correct file name and the full path. Alternatively, you can add the path to the current **dc_shell** or **lc_shell search_path**, and issue the command with the correct file name.

EXAMPLE MESSAGE

```
Error: The 'uil4.lib' library source file is not found. (UIL-4)
```

UIL-5 (error) The read_lib command does not support '%s' as the '-format' switch value. The only format allowed is 'edif'.

DESCRIPTION

Currently, **read_lib** accepts only **edif** as **-format** switch value for reading in symbol library in EDIF format. It is reported as an error if you specify any other **-format** switch value.

WHAT NEXT

If you want to read in an EDIF symbol library, make sure the **read_lib** switch **-format** has the value **edif**. Otherwise, do not specify the **-format** switch with the **read_lib** command. Reinvoke the **read_lib** with the correct switch value. For quick reference, invoking **read_lib** with -help switch, causes **read_lib** to print out its legal command syntax.

EXAMPLES

```
dc_shell> read_lib -help
Usage: read_lib
             -format      (EDIF symbol format; default is Synopsys format)
     -symbol      (with EDIF, name of Synopsys library file to create)
     <file_name>  (technology or symbol library file)
     -no_warnings (disable warning messages)
     -names_file  <file_list>  (one or more names files)
```

UIL-6 (warning) The Library Compiler is not enabled. The cell functionality is ignored.

DESCRIPTION

This site is not licensed for Library Compiler. The attempt to compile a technology library is restricted to timing information only. All cell functions are removed, so they become black-boxes.

WHAT NEXT

If you are compiling a technology library for timing analysis use only, ignore this

warning message. However, if you want to have full Library Compiler capability, contact your Synopsys system administrator to purchase Library Compiler.

EXAMPLE MESSAGE

```
Warning: The Library Compiler is not enabled. The cell
functionality will be ignored. (UIL-6)
```

UIL-7 (error) Cannot write the library to the '%s' file.

DESCRIPTION

An attempt to write out a database (db or sdb) file w with **write_lib** failed. The reasons you get this error could be because either

- You do not have write permission to the target directory or,
- There is not enough disk space for the file.

WHAT NEXT

Check disk space and permission of the target directory. Make sure you have enough disk space and write permission before using **write_lib**.

UIL-8 (error) The '%s' pin of the '%s' cell in the '%s' technology library is not found in the same cell of the '%s' symbol library.

DESCRIPTION

The Library Compiler detects unmatched pin names between a technology library and a symbol library using the **compare_lib** command.

WHAT NEXT

Correct the mismatch either in the technology library or the symbol library, and recompile the modified library.

EXAMPLE MESSAGE

```
Error: The 'D' pin of the 'uil8' cell in the 'techlib' technology library
is not found in the same cell of the 'symblib' symbol library. (UIL-8)
```

UIL-9 (error) The ’%s’ cell does not exist in the ’%s’ symbol library.

DESCRIPTION

A correspondent symbol cell cannot be found in the symbol library. This error is caused by a typo in a cell name in either the technology library file or the symbol library file, or a missing symbol cell. This error results in the use of a generic symbol library symbol or a black box symbol in a schematic containing the cell.

WHAT NEXT

If the error is due to a typo, correct the cell name typo. If the error is due to a missing symbol, add it to the symbol library. Recompile the modified library, and run compare_lib command.

EXAMPLE MESSAGE

Error: The ’uil9’ cell does not exist in the ’symblib’ symbol library. (UIL-9)

UIL-10 (error) Trying to compare a ’%s’ library with a ’%s’ library. compare_lib compares a technology library and a symbol library.

DESCRIPTION

The two libraries submitted to **compare_lib** are not a legitimate combination. **compare_lib** compares a technology library and a symbol library.

WHAT NEXT

Use **report_lib** to obtain the types of libraries. Make sure that you compare a symbol library and a technology library.

EXAMPLE MESSAGE

Error: Trying to compare a ’Technology’ library with a ’Technology’ library. compare_lib compares a technology library and a symbol library. (UIL-10)

UIL-12 (error) Trying to compare a library with itself. compare_lib

compares a technology library and a symbol library.

DESCRIPTION

The two libraries submitted to **compare_lib** are identical. The **compare_lib** command compares a technology library and a symbol library.

WHAT NEXT

Compare a symbol library and a technology library. If the technology library and symbol library share the same library name, specify the symbol library with its full name in **format file_path:library_name**. For example, the libraries are both named **uil12**. Issue the commands

```
dc_shell> list -library
        Library           File                    Path
        -------           ----                    ----
        uil12               uil12.db             /synopsys/libraries
        uil12               uil12.sdb            /synopsys/libraries
1

dc_shell> compare_lib uil12.db:uil12 uil12.sdb:uil12
```

EXAMPLES

```
dc_shell> compare_lib uil12 uil12
```

EXAMPLE MESSAGE

```
Error: Trying to compare a library with itself. compare_lib
        compares a technology library and a symbol library. (UIL-12)
```

UIL-13 (error) The specified '%s' library cannot be found in memory.

DESCRIPTION

You try to access a library that has not been read in yet. This error could result from typos in the library name.

WHAT NEXT

Use **list -lib** to find all available libraries. Make sure that you type in the correct library name with your command. If the library is not reported by the **list -lib** command, load the library with **read_lib** for a library source file, or **read** for a

db file, before reissuing the command.

UIL-15 (warning) No libraries in the '%s' library file.

DESCRIPTION

A file is read in, but no library is found in the file. It is most likely that the file is empty.

WHAT NEXT

Read in the correct file with a library.

UIL-16 (error) Cannot find the '%s' library or library file in memory.

DESCRIPTION

This error is obsoleted.

WHAT NEXT

UIL-17 (error) Could not open the '%s' file for reading.

DESCRIPTION

You do not have read permission of the specified EDIF file.

WHAT NEXT

Check the permissions for the file. Make sure you have read permissions for the file.

EXAMPLE MESSAGE

Error: Could not open the 'uil17.edif' file for reading. (UIL-17)

UIL-18 (error) Could not open the '%s' file for writing.

DESCRIPTION

An attempt to open an output file has failed. This problem might be caused by

1. Trying to write to a directory for which you do not have write permission.
2. Trying to write to an existing file for which you do not have write permission.
3. The output file name specifies a non-existing path.
4. The file system is full.

WHAT NEXT

Check the correctness of file name and path, and make sure you have write permission for the file. If the file system is full, provide more disk space.

UIL-19 (error) The '%s' cell does not exist in the '%s' technology library.

DESCRIPTION

This error message is issued by either **compare_lib** or **report_lib**. In the **compare_lib** case, if it cannot find a matched technology library cell for a symbol component, it reports this error with the message. In the **report_lib** case, if you specify a nonexistent cell in the cell list, this error message is displayed. This error usually is caused by a typo.

WHAT NEXT

Provide a correct name with each cell in a cell list. If you are not sure about cell names, do not specify a cell list.

UIL-20 (error) The '%s' symbol in the '%s' symbol library has an extra '%s' pin.

DESCRIPTION

This error message is issued by the **compare_lib** command. For each cell of a symbol library, Library Compiler checks for pin names in the same cell of the technology library and issues an error if the pin does not exist.

WHAT NEXT

Correct the symbol library by removing the pin name or adding it to the technology library. Use Library Compiler to recompile the modified library, and run the compare_lib command.

UIL-21 (error) The '%s' synthetic module does not exist in the '%s' library.

DESCRIPTION

This error message is issued by the **report_lib** command. You might have specified a nonexistent synthetic module in the module list. This error is usually caused by a typo.

WHAT NEXT

Provide a correct name with each module in a module list. If you are not sure about module names, do not specify a module list.

UIL-23 (error) Invalid output format '%s'.

DESCRIPTION

Currently, for dc_shell **write_lib** accepts only **db, edif**, and **vhdl** as **-format** switch value for writing libraries in the specifBed format. For lc_shell, only **db** and **vhdl** switch values are accepted. It is reported as an error if you specify any other **-format** switch value.

WHAT NEXT

If your want to write a db library, do not specify the **-format** switch with the **write_lib** command. Otherwise, make sure that the **write_lib** switch **-format** has the value edif or vhdl.

Reinvoke the **write_lib** with the correct switch value. For quick reference, invoking **write_lib** with the -help switch, causes **write_lib** to print out its correct command syntax.

EXAMPLES

```
dc_shell> write_lib -help
     Usage: write_lib
             <library_name> (a library already loaded into dc_shell)
             -format        db|edif|vhdl (write library in the specified format;
```

```
                default is db)
-output         <file_name>  (write library to the specified file)
-names_file     <file_list>  (one or more names files)
```

UIL-24 (error) Unacceptable VHDL library generation. You must read in the ‘%s‘ library from a technology library source file.

DESCRIPTION

This error is issued when the **write_lib -format vhdl** uses a library read as a db file using the **read** command.

WHAT NEXT

Read in the library from a technology library source file. Reissue the write_lib -format vhdl command.

EXAMPLE MESSAGE

```
Error: Unacceptable VHDL library generation.
You must read in the ‘uil24‘ library  from a technology library source file. (UIL-24)
```

UIL-25 (error) The ’-symbol’ option can only be used with the ’-format EDIF’ option.

DESCRIPTION

Currently, **read_lib** accepts the **-symbol** option only with **edif** as a **-format** switch value for reading in symbol library in EDIF format. It is reported as an error if you specify -symbol without the edif format.

WHAT NEXT

If your want to read in an EDIF library and select the Synopsys file to create a symbol library, make sure the **read_lib** switch **-format** has the value edif followed by the **-symbol filename** option. Otherwise, do not specify the **-symbol** switch with the **read_lib** command. Reinvoke the **read_lib** with the correct switch value. For quick reference, invoking **read_lib** with the -help switch, causes **read_lib** to print out its correct command syntax.

EXAMPLES

```
dc_shell> read_lib -help
Usage: read_lib
             -format      (EDIF symbol format; default is Synopsys format)
     -symbol      (with EDIF, name of Synopsys library file to create)
     <file_name>  (technology or symbol library file)
     -no_warnings (disable warning messages)
     -names_file  <file_list>  (one or more names files)
```

UIL-26 (error) Unacceptable list of cells for the '%s' library.

DESCRIPTION

This error message is issued by the **report_lib** command. You might have specified an empty or a corrupted cell list. This error usually is caused by a typo.

WHAT NEXT

Provide a correct name with each cell in a cell list. If you are not sure about cell name, do not specify a cell list.

UIL-27 (error) Invalid technology library timing report. You must read in the '%s' library from a technology library source file.

DESCRIPTION

This error message is issued by **report_lib -timing_arcs** or **-timing** command. The timing options are used only on a library that has been read from a ".lib" technology library source file by the **read_lib** command.

WHAT NEXT

To use the report_lib with the -timing option, read in the technology source library instead of the db file.

UIL-28 (warning) The '%s' vendor specific delay model is used in this library.

The library timing report might be incomplete.

DESCRIPTION

This message is issued during a **report_lib -timing** command. The **delay_model** attribute in the technology source file is set to a non-generic delay model, such as **generic_cmos** or **table_lookup**. In the case of a **cmos2**, **report_lib** does not display any information about the slope.

WHAT NEXT

You can choose to ignore the warning or to modify the delay model attribute in the technology source file if you want more timing information. Reread the library, and reissue the report_lib command.

EXAMPLE MESSAGE

```
Warning: The 'cmos2' vendor specific delay model is used in this library.
        The library timing report might be incomplete. (UIL-28)
```

UIL-29 (error) The '%s' library is a synthetic library. Use the report_synlib command.

DESCRIPTION

This error is issued when the **report_lib** command is used for reporting on a synthetic library. A dc_shell command **report_synlib** is used to report on synthetic libraries.

WHAT NEXT

Use **report_synlib** command to report on synthetic libraries.

UIL-30 (error) The '%s' library is not a synthetic library. Use report_lib command.

DESCRIPTION

This error is issued when the **report_synlib** command is used on reporting on a technology library. A Library Compiler command **report_lib** is used to report on technology libraries.

WHAT NEXT

Use **report_lib** command to report on technology libraries.

UIL-32 (warning) The '%s' model library is different from the current link library.

DESCRIPTION

The **model** command might generate this message whenever the model library is different from the current link library. This situation should not occur frequently, but whenever a **model** is used with a 'for' loop construct to get the model library, it is possible that the link library will be different from the model library.

WHAT NEXT

Redefine **link_library** to be the same as the model library.

UIL-33 (error) Invalid technology library state table report. You must read in library '%s' from a technology library source file.

DESCRIPTION

The report_lib options '-table' and '-full_table' require that the technology library source file is read in by read_lib. These options print out the state table information in the technology library.

WHAT NEXT

Read the technology library source file, then reissue the **report_lib** command with the **-table** or **-full_table** options.

UIL-34 (information) Updating technology library (please save) ...

DESCRIPTION

Every db technology library written out by a version of Library Compiler older than

4.0, is processed again every time that it is read in. To cut out this very significant amount of overhead, after reading in the db technology library, write the library back out and use the updated library.

The variables 'read_db_lib_warnings' and 'read_translate_msff' control options for this processing step. Please refer to their man pages for more details.

WHAT NEXT

Write the technology library back out by using the **write_lib** command.

UIL-35 (warning) operating conditions '%s' not overwritable in lib '%s'

DESCRIPTION

The command issued tries to overwrite an operating condition group that has been declared permanent before. create this operating condition with a different name.

WHAT NEXT

Use **report_lib** to find all available operating conditions for that lib. Choose a name which is not there and create a new one.

EXAMPLE MESSAGE

Warning: operating conditions 'WCCOM' not overwritable in lib 'my_lib' (UIL-35)

UIL-36 (warning) operating condition already defined in lib '%s'

DESCRIPTION

The command issued tries to overwrite an existing group with the same name.

WHAT NEXT

Use -overwrite option. If it is still not overwritable use **report_lib** to find all available operating conditions for that lib. Choose a name which is not there and create a new one.

EXAMPLE MESSAGE

operating condition already defined in lib 'mylib' (UIL-36)

UIL-37 (information) The DCM vendor specific delay model is used in this library.
The library report will not contain timing-related information.

DESCRIPTION

This message is issued during a **report_lib** command. The **delay_model** attribute in the technology source file is set to "dcm" delay model. The **report_lib** command does not display any timing information.

WHAT NEXT

EXAMPLE MESSAGE

```
Information: The DCM vendor specific delay model is used in this library.
        The library report will not contain timing-related information. (UIL-37)
```

UIL-39 (error) The psuedo techonlogy file %s not found.

DESCRIPTION

This message is issued during a **read_lib -format gdsii** command. The given pusedo library file doesn’t exist in the directory.

WHAT NEXT

1. Set the search_path variable correctly to point to the pusedo library directory.
2. Check to see if the file exists and has read permissions.

EXAMPLE MESSAGE

UIL-40 (warning) The library ’%s’ is not a physical library. Ignore -macro_only option.

DESCRIPTION

You receive this warning message because you have executed the **write_lib** command with the **-macro_only** option and specified a library that is not a physical library. The **-macro_only** option with the **write_lib** command applies only to the physical

library.

WHAT NEXT

Do not use the **-macro_only** option when writing a non-physical library. Or, ensure that the specified library is in the physical library before executing the **writ_lib -macro_only** argument.

SEE ALSO

write_lib (2).

UIL-41 (error) Invalid technology library noise report. You must read in the ‘%s‘ library from a technology library source file.

DESCRIPTION

This error message is issued by **report_lib -noise** command. The timing options are used only on a library that has been read from a ".lib" technology library source file by the **read_lib** command.

WHAT NEXT

To use the report_lib with the -noise option, read in the technology source library instead of the db file.

UIL-42 (error) %s ’%s’ is duplicated.

DESCRIPTION

This error message is issued by **merge_lib** command.

UIL-43 (error) Library ’%s’ is not a NLDM library and can’t be merged.

DESCRIPTION

This error message is issued by the **merge_lib** command.

WHAT NEXT

Only native nldm libraries can be merged.

UIL-44 (error) The '%s' of object '%s' and of object '%s' are different.

DESCRIPTION

This error message is issued by the **merge_lib** command.

WHAT NEXT

Some key properties of the two objects to merge should be the same.

UIL-45 (error) Can not open the Milkyway reference library '%s'.

DESCRIPTION

You receive this warning message because you have executed the **write_lib** command with the **-mw_ref_lib** option and specified a Milkyway reference library. However the Milkyway reference library can not be opened. The generated .db/.pdb file is not written into the Milkyway reference library

WHAT NEXT

Check if the Milkyway reference library specified exists and is not locked by other applications.

SEE ALSO

write_lib (2).

UIL-46 (warning) The operating condition '%s' is not valid. Use the default value of 'min'.

DESCRIPTION

You receive this warning message because you have executed the **write_lib** command with the **-mw_oc_type** option and specified an operating condition that is not valid.

The value of -fB-mw_oc_type can only be 'max', 'min', 'typical' or 'other'.

WHAT NEXT

SEE ALSO

write_lib (2).

UIL-47 (error) The option '-mw_ref_lib' is not specified while using the '-mw_oc_type' option.

DESCRIPTION

You receive this warning message because you have executed the **write_lib** command with the **-mw_oc_type** option and specified an operating condition without specifying a Milkyway reference library.

WHAT NEXT

Specify the '-mw_ref_lib' option along with the option '-mw_oc_type'

SEE ALSO

write_lib (2).

UIL-48 (error) the output format is not in db format while trying to write the output into a Milkyway reference library.

DESCRIPTION

You receive this warning message because you have executed the **write_lib** command with the **-mw_ref_lib** option and specified an output format which is not in db format. Only db format file can be written into an Milkyway reference library by **write_lib**

WHAT NEXT

Do not use the **-mw_ref_lib** option when writing a non-db format file.

SEE ALSO

write_lib (2).

UIL-49 (error) Invalid technology library user-defined data report.

The 'report_user_data' library_feature is not specified in the '%s' library.

You must read in the '%s' library from a technology library source file.

DESCRIPTION

This error message is issued by **report_lib -user_defined_data** command. The user-defined_data options are used only on a library that has been read from a ".lib" technology library source file by the **read_lib** command.

WHAT NEXT

To use the report_lib with the -user_defined_data option, read in the technology source library instead of the db file.

UIL-50 (error) The '%s' cell does not exist in the '%s' physical library.

DESCRIPTION

This error message is issued by **report_lib**. In the **report_lib** case, if you specify a nonexistent cell in the cell list, this error message is displayed. This error usually is caused by a typo.

WHAT NEXT

Provide a correct name with each cell in a cell list. If you are not sure about cell names, do not specify a cell list.

UIL-51 (error) The '%s' library is a symbol library.

It is not supported by the get_lib_attribute command.

DESCRIPTION

This error is issued when the **get_lib_attribute** command is used for a synthetic library. The gerht_lib_attribute command can only be used for technology libraries.

WHAT NEXT

Use **get_attribute** command for synthetic libraries.

UIL-52 (error) The '%s' library is a physical library. It is not supported by the get_lib_attribute command.

DESCRIPTION

This error is issued when the **get_lib_attribute** command is used for a physical library. The gerht_lib_attribute command can only be used for technology libraries.

WHAT NEXT

Use **get_attribute** command for physical libraries.

UIL-53 (error) Unacceptable list of library objects for the '%s' library.

DESCRIPTION

This error message is issued by the **get_lib_attribute** command. You might have specified an empty or a corrupted library object list. This error usually is caused by a typo.

WHAT NEXT

Provide a correct name with each object in a library object list. If you are not sure about library object name, do not specify a library object list.

UIL-54 (error) The '%s' object does not exist in the '%s'

technology library.

DESCRIPTION

This error message is issued by **get_lib_attribute**. If you specify a nonexistent object in the library object list, this error message is displayed. This error usually is caused by a typo.

WHAT NEXT

Provide a correct name with each object in a libray object list. If you are not sure about object names, do not specify a object list.

UIL-55 (error) The '%s' library_feature is not specified in the '%s' library.

DESCRIPTION

This error message is issued by **set_lib_attribute**. If you use set_lib_attribute command for a library which does not have 'allow_update_attribute' library feature, this error message is displayed.

WHAT NEXT

Set the 'allow_update_attribute' library_feature in the source library as follows:
library(sample) { ... library_features(report_delay_calculation); ... }

UIL-56 (error) The value '%s' is not valid for the attribute '%s', or the attribute '%s' is not modifiable.

DESCRIPTION

This error message is issued by **set_lib_attribute**.

WHAT NEXT

Correct the attribute value.

UIL-57 (error) Invalid technology library power report.

You must read in the ‘%s‘ library from a technology library source file.

DESCRIPTION

This error message is issued by the **report_lib -power** command when the library is read from a db file that is not enabled for reporting power information. In such cases, the **-power** option is enabled only if that library is read from a ".lib" technology library source file by the **read_lib** command.

A library db file can be enabled for reporting power information by compiling it from a ".lib" file that enables the library feature **report_power_calculation**.

WHAT NEXT

To use **report_lib** with the **-power** option, read in the technology source library instead of the db file.

UIL-58 (error) The format of the -%s option is incorrect.

DESCRIPTION

Command "merge_lib" requires that the -baseline option define a pair of baseline library name and calc_mode. Command "merge_lib" requires that the -library option define pairs of library name and calc_mode.

UIL-59 (error) Calc_mode ’%s’ is not valid.

DESCRIPTION

This error message is issued by the **merge_lib** command. 1.If the baseline defines the default_operating_conditions, then the name of that default operating condition can’t be used as a calc_mode for other libraries to be merged. 2.If the baseline does not defines the default_operating_conditions, then the name of the baseline library can’t be used as a calc_mode for other libraries to be merged. 3. The name of the baseline library plus "_CALC_MODE" can’t be used as a calc_mode for other libraries to be merged.

UIL-60 (error) Cannot attach test model to library cell '%s'.

DESCRIPTION

This error is generated because a test model in CTL format is successfully read in but cannot be associated with the named cell because it does not have a CTL interface or it does not exist.

WHAT NEXT

Make sure the named design exists and has the same CTL interface.

SEE ALSO

UIL-61 (warning) Override the test model attached to the library cell '%s'.

DESCRIPTION

The library cell already has a test model attached to it but a newly generated test model is going to override the old one and attach to the library cell.

WHAT NEXT

Make sure it is intended to override a previous attached test model to the library cell

SEE ALSO

UIL-62 (warning) Operating condition '%s' is not found in library '%s'.

DESCRIPTION

The command issued tries to access an operating condition that does not exist in the specified library. A typo in the operating condition name can also result in this problem. Any of the following commands might trigger the generation of this warning: **report_operating_conditions, delete_operating_conditions**.

WHAT NEXT

Use **report_operating_conditions -lib** to list all operating conditions. Make sure the operating condition name is among the ones being reported by **report_operating_conditions -lib**.

EXAMPLE MESSAGE

Warning: Operating condition 'OC1' is not found in library 'a_lib'. (UIL-62)

UIL-63 (warning) Operating condition '%s' can't be deleted since it is not created by users using command 'create_operating_conditions'.

DESCRIPTION

Only those operating conditions created by users using command **create_operating_conditionsfp and not being used by any design can be deleted from a library.**

EXAMPLE MESSAGE

Warning: Operating condition 'OC1' can't be deleted since it is not created by user
s using
command 'create_operating_conditions'. (UIL-63)

UIL-64 (warning) Operating condition '%s' can't be deleted since it's still used by design : %s.

DESCRIPTION

Only those operating conditions created by users using command **create_operating_conditionsfp and not being used by any design can be deleted from a library.**

EXAMPLE MESSAGE

Warning: Operating condition 'OC1' can't be deleted since it's still used by design
 : DESIGN1 DESIGN2. (UIL-64)

UIL-65 (error) The '%s' library_feature is not specified in the '%s'

library.

DESCRIPTION

This error message is issued by **report_lib -yield**. If you use 'report_lib -yield' command for a library which does not have 'report_yield' library feature, this error message is displayed.

WHAT NEXT

Set the 'report_yield' library_feature in the source library as follows:
library(sample) { ... library_features(report_yield); ... }

UIL-66 (error) Cannot write the library '%s'. The Composite Current Source information has been stripped while reading the library.

DESCRIPTION

This library was read into memory when db_load_ccs_data was set to false. Hence the Composite Current Source driver and receiver model from the library has been stripped while reading. To be able to write the library, the variable db_load_ccs_data has to be set to true before reading the library.

WHAT NEXT

Set the variable db_load_ccs_data to true in a new dc_shell session, read the library and then perform write_lib.

UIL-67 (error) Could not close the '%s' file.

DESCRIPTION

The file cannot be closed.

WHAT NEXT

Check to see if there are any error messages before this file closing operation.

EXAMPLE MESSAGE

Error: Could not close the 'a.lib' file. (UIL-67)

UIL-70 (warning) Cannot load the Composite Current Source information since you are not authorized for the license Galaxy-Beta.

DESCRIPTION

The license Galaxy-Beta is a requirement for using Composite Current Source (CCS) information. This message will be issued when the site is not authorized for Galaxy-Beta license and the user is trying to set the variable db_load_ccs_data to true. The same message will be repeated if he is not authorize for Galaxy-Beta license and he is reading a library with Composite Current Source driver and receiver model when the variable db_load_ccs_data is true.

SEE ALSO

db_load_ccs_data (3).

UIL-71 (error) Cannot write the library '%s'. Writing of the library which has Composite Current Source timing information is not supported inside '%s' in this release. Please use lc_shell.

DESCRIPTION

In this release, writing of the library which has CCS timing information is supported only in lc_shell. Hence issue the write_lib command inside lc_shell.

WHAT NEXT

UIL-72 (warning) The Composite Current Source information in the library '%s' is not reported. Reporting of CCS information is not supported inside '%s' in this release.

DESCRIPTION

In this release, report_lib -timing reports the CCS timing information only in lc_shell. If you want to view the CCS timing information, please use lc_shell.

WHAT NEXT

UIL-73 (error) Invalid technology library switch cell report. You must read in the ‘%s‘ library from a technology library source file.

DESCRIPTION

This error message is issued by **report_lib -switch** command. The switch option is used only on a library that has been read from a ".lib" technology library source file by the **read_lib** command.

WHAT NEXT

To use the report_lib with the -switch option, read in the technology source library instead of the db file.

UIL-74 (error) Invalid technology library pg pin report. You must read in the ‘%s‘ library from a technology library source file.

DESCRIPTION

This error message is issued by **report_lib -pg_pin** command. The pg_pin option is used only on a library that has been read from a ".lib" technology library source file by the **read_lib** command.

WHAT NEXT

To use the report_lib with the -pg_pin option, read in the technology source library instead of the db file.

UIL-75 (warning) The directory ’%s’ exists and the files with same name under it will be updated.

DESCRIPTION

This message is given if the directory exists. If so, the files with same name under it will be updated.

WHAT NEXT

If you want to keep the old files under this directory, just rename the output directory name by option **datasheet_output_dir** for Datasheet generator or **veriloglib_output_dir** for VERILOG generator.

EXAMPLES

```
datasheet_output_dir=test_datasheet
write_lib -format datasheet  dbvh13

OR

veriloglib_output_dir=test_verilog
write_lib -format verilog dbvh13
```

EXAMPLE MESSAGE

```
Warning: The directory already exists and the files with same name under it will be
 updated. (UIL-75)
```

UIL-76 (error) No/Invalid option value specified for '%s'.

DESCRIPTION

In calculate_caa_based_yield2db command, some options have dependency and requirement:

(1) Operating target should be a valid library name (already loaded in Library Compiler), or a valid db file (that can be read into LC successfully). (2) If the operating target is a db file, not a library name, The -output option with a valid db file name should be specified. And the output db file name should be different from input db file. (3) Currently, for '-data_kit_type' option, only 'tsmc' and 'tsmc_encr' are valid values. (4) When there are more than one routing layers defined in the library, The '-layer_dsd_alias' option must be provided. If there is only one routing layer in library, use default {0 0 0 0 0} as its value. (5) "-layer_dsd_alias" option value must contains 5 integer values, for the value of alias layers: Mx, My, Mz, Mr, Mt by order.

WHAT NEXT

Check the options to this command, specify all necessary and valid options.

EXAMPLES

```
calculate_caa_based_yield2db -data_kit_type tsmc
 -particle_distr_func_file tsmc.ddk a.db -output a.db

OR
```

```
calculate_caa_based_yield2db -data_kit_type tsmc
 -particle_distr_func_file tsmc.ddk -layer_dsd_alias {0 0} test

OR
calculate_caa_based_yield2db -data_kit_type tsmc
 -particle_distr_func_file tsmc.ddk nonexist.db
```

EXAMPLE MESSAGE

```
Error: No/Invalid option value specified for '-output'.(UIL-76)
Error: No/Invalid option value specified for '-layer_dsd_alias'.(UIL-76)
Error: No/Invalid option value specified for 'nonexist.db'.(UIL-76)
```

UIL-77 (error) The directory '%s' doesn't exist.

DESCRIPTION

This message is given if the directory doesn't exist. If so, the custom function file directory is wrong.

WHAT NEXT

If you want to define the directory for custom function files, define the correct directory name by option **veriloglib_custom_func_dir** for VERILOG generator.

EXAMPLES

```
veriloglib_custom_func_dir=test_dir
write_lib -format verilog dbvh13
```

EXAMPLE MESSAGE

```
Error: The directory 'test_dir' doesn't exit. (UIL-77)
```

UIL-78 (information) The mapping file "func.map" for custom udp flow doesn't exist.

DESCRIPTION

This message is given if the custom function directory is defined, but "func.map" file doesn't exit in the directory.

In custom UDP flow, verilog generator will check for mapping file "func.map" in the directory first. If the file doesn't exit or there is no mapping information for the

cell, verilog generator will search for file "[cell_name].func" as the single cell function part for the cell. If this file doesn’t exit, verilog generator will search for file "[library_name].func", and search the cell’s function part in this packet file. If this can’t be found either, verilog generator will not use custom UDP flow and comes to the general flow.

WHAT NEXT

Users can ignore this information if they have provided [cell_name].func, or [library_name].func for custom UDP flow, or they haven’t provided any kind of function files by don’t want to use custom UDP flow. If users want to use mapping file approach in custom UDP flow, you must provide the "func.map" file as in the description part.

UIL-79 (warning) Syntax error of mapping file "%s".

DESCRIPTION

This message is given if the mapping file has some syntax error.

Mapping file must be defined by the following syntax. Each line contains the mapping information of a specific file to multiple cells. Cell name is separate by blank. The bracket is needed here. No comment is applied here.

<file name> [<cell name1> <cell name2>]

WHAT NEXT

If user want to use mapping file approach in verilog and datasheet , user need to edit the mapping file and correct the syntax error.

EXAMPLES

Foo2.func [FDQ1X1 FDQ1X2]

UIL-80 (error) The %s format isn’t supported by datasheet generator.

DESCRIPTION

This error is given if the format is not "text" and "html".

WHAT NEXT

If user want to generate html format datasheet, set datasheet_enable to "html"; if user want to generate text format datasheet, set datasheet_enable to "text".

EXAMPLES

html format:
set datasheet_enable html

text format:
set datasheet_enable text

UIL-81 (error) The directory [%s] doesn’t exist.

DESCRIPTION

This error is given if the directory doesn’t exist or there is a typo in the directory name.

WHAT NEXT

check whether the directory exist or type the correct directory name.

EXAMPLES

Error: The directory [/slowfs/xxx] doesn’t exist. (UIL-81)

UIL-82 (error) The file [%s] can not be found

DESCRIPTION

This error is given if the file does not exist.

WHAT NEXT

check whether the file exist or type the correct file name.

EXAMPLES

```
Error: The file [/slowfs/xxx/yunz.txt] can’t be found. (UIL-82)
```

UIM-1 (error) State '%s' is not a state in the state machine.

DESCRIPTION

This error message is issued for fsm commands where a state needs to be specified and the state specified by the user doesn't exist in the design.

This message can be issued from commands set_fsm_order or set_fsm_encoding.

WHAT NEXT

To obtain the list of states in the design, invoke report_fsm command. Check the spelling state names or need to recheck your original state table or HDL design to make sure that the state is in the design. Then reinvoke the command.

UIM-2 (error) Illegal list of states.

DESCRIPTION

WHAT NEXT

UIM-3 (error) Design must be a state table inorder to set state

order.

DESCRIPTION

WHAT NEXT

UIM-4 (error) Design does not contain any states.

DESCRIPTION

WHAT NEXT

UIM-5 (error) Illegal state vector list.

DESCRIPTION

WHAT NEXT

UIM-6 (error) Non state table designs must have the complete

encoding specified.

DESCRIPTION

WHAT NEXT

UIM-7 (error) Illegal state encoding list.

DESCRIPTION

WHAT NEXT

UIM-8 (error) Invalid encoding style '%s'.

DESCRIPTION

WHAT NEXT

UIM-9 (error) Encoding '%s' used multiple times.

DESCRIPTION

WHAT NEXT

UIM-10 (error) Encodings have inconsistent length.

DESCRIPTION

WHAT NEXT

UIM-11 (error) Encoding '%s' has invalid characters.

DESCRIPTION

WHAT NEXT

UIM-12 (error) Invalid flatten minimize value '%s'.

DESCRIPTION

WHAT NEXT

UIM-13 (error) State '%s' used multiple times in encoding list.

DESCRIPTION

WHAT NEXT

UIM-14 (error) The '%s' command is obsolete in XG mode.

DESCRIPTION

The extract, reduce_fsm, minimize_fsm, and compare_fsm commands are obsolete in XG mode. The functionality that these commands perform is embedded in the ultra optimization flow. You can enable the ultra optimization with command 'set_ultra_optimization'.

WHAT NEXT

Do not use extract, reduce_fsm, minimize_fsm, or compare_fsm commands in XG mode.

SEE ALSO

set_ultra_optimization(2),

UIMG

UIMG-1 (error) Cannot %s design over existing design '%s'

DESCRIPTION

There is a conflict with an existing design or library object with the same name.

WHAT NEXT

Check if the destination design or library exists already.

UIMG-2 (error) Cannot %s a design to a file

DESCRIPTION

WHAT NEXT

UIMG-3 (error) Cannot %s design; no access to path '%s'

DESCRIPTION

WHAT NEXT

UIMG-4 (error) Cannot %s multiple designs to a single design

DESCRIPTION

WHAT NEXT

UIMG-5 (error) The 'uniquify_naming_style' variable must be

set to use this command.

DESCRIPTION

WHAT NEXT

UIMG-6 (error) ’%s’ is not a valid setting for the ’uniquify_naming_style’ variable.

DESCRIPTION

WHAT NEXT

UIMG-7 (error) The ’-force’ option cannot be used if the ’-cell’, ’-reference’ or ’-new_name’ options are used.

DESCRIPTION

WHAT NEXT

UIMG-8 (error) The ’-new_name’ option can only be used if one cell is specified.

DESCRIPTION

WHAT NEXT

UIMG-9 (error) The ’-reference’ option cannot be used if

the ’-cell’ or ’-new_name’ options are used.

DESCRIPTION

WHAT NEXT

UIMG-10 (error) Could not find the specified cell(s).

DESCRIPTION

This error message is issued by the uniquify command. The specified cells are invalid.

WHAT NEXT

Check the man page for the uniquify command.

UIMG-11 (error) Cannot find design named ’%s’.

DESCRIPTION

This error message is issued by the uniquify command. The specified design could not be found.

WHAT NEXT

Check the man page for the uniquify command.

UIMG-12 (error) Cell ’%s’ is linked to design ’%s’, which is a library design, so it cannot be uniquified.

DESCRIPTION

This error message is issued by the uniquify command. The specified cell could not be uniquified because it is linked to a library design.

WHAT NEXT

Check the man page for the uniquify command.

UIMG-13 (warning) No cells were uniquified.

DESCRIPTION

This error message is issued by the uniquify command.

WHAT NEXT

Check the man page for the uniquify command.

UIMG-14 (error) Rules '%s' are not defined.

DESCRIPTION

This error is issued either by change_names command or report_names command or define_name_rules command or report_name_rules command. The specified rules cannot be found.

WHAT NEXT

Check for the specified rules file.

UIMG-15 (error) Bad -type option '%s' specified.

DESCRIPTION

This message is issued by define_name_rules command. The type should be either net or port.

WHAT NEXT

Check man page for define_name_rules command.

UIMG-16 (error) Default rules '%s' are not defined.

DESCRIPTION

This message is issued by the report_names command or the change_names command. The specified default rules are not defined.

WHAT NEXT

Check that the variable default_name_rules is set correctly.

UIMG-17 (error) No name rules specified and no default. Use the -rules option or set the default_name_rules variable.

DESCRIPTION

WHAT NEXT

UIMG-18 (error) Can't open names file '%s'.

DESCRIPTION

WHAT NEXT

UIMG-19 (error) Too many errors in names file '%s'.

DESCRIPTION

WHAT NEXT

UIMG-20 (warning) No valid name changes found in names file

’%s’.

DESCRIPTION

WHAT NEXT

UIMG-21 (error) Invalid class string ’%s’.

DESCRIPTION

WHAT NEXT

UIMG-22 (warning) Can’t find %s ’%s’ in %s ’%s’.

DESCRIPTION

WHAT NEXT

UIMG-23 (information) Using name rules ’%s’.

DESCRIPTION

WHAT NEXT

UIMG-24 (information) No name changes to report in design ’%s’.

DESCRIPTION

WHAT NEXT

UIMG-25 (information) %d names changed using names file

’%s’.

DESCRIPTION

WHAT NEXT

UIMG-26 (warning) File %s,
line %d: unsupported class string ’%s’ in ’%s’.

DESCRIPTION

WHAT NEXT

UIMG-27 (warning) File %s,
line %d and
File %s,
line %d : duplicate change for %s ’%s’.
Previous change will be overwritten by the latest one.

DESCRIPTION

WHAT NEXT

UIMG-28 (warning) File %s,
line %d: Can’t find %s name ’%s’.

DESCRIPTION

WHAT NEXT

UIMG-29 (warning) File %s,

line %d and
File %s,
line %d : Unsupported multiple names files.
%s '%s' was the new name of %s '%s' in %s '%s'.

DESCRIPTION

WHAT NEXT

UIMG-30 (warning) File %s,
Line %d:A %s named '%s' already exists in design '%s'.

DESCRIPTION

WHAT NEXT

UIMG-31 (warning) File %s,
Line %d: Can't find %s '%s' in %s '%s'.

DESCRIPTION

WHAT NEXT

UIMG-32 (warning) File %s,
Line %d:ObjectType: %s
BusMemberName: '%s'BusPortName: '%s'
change_names can not be applied to individual BUS MEMBER.
Please specify the BUS PORT NAME instead.

DESCRIPTION

The "change_names" command does not allow bus members changed only. In 3.1a, it used to let users change bus members, and then it would automatically change bus port for

users. Now in 3.1b it does not allow users to change individual bus member. If users change bus, it will automatically change all its member at one time. UIMG-32 is used to warn users can not change bus member only.

WHAT NEXT

UIMG-33 (error) File %s,Line %d:

A DELIMITER '%s' is expected,which stops reading this names file. There are five fields separated by spaces in names_file formate.

<design_name> <object_type_string> <object_name> <new_name> <delimiter>

DESCRIPTION

WHAT NEXT

UIMG-34 (error) File %s,Line %d:

A DELIMITER '%s' is not expected, which stops reading this names file.

DESCRIPTION

WHAT NEXT

UIMG-35 (warning) The variable "%s" has set to "%s" from "".

DESCRIPTION

WHAT NEXT

UIMG-36 (warning) In design %s, %s bus member '%s' changed

to ’%s’.

DESCRIPTION

WHAT NEXT

UIMG-40 (information) Because you are in the simple compile mode, uniquifying the design will result in degradation of runtime.

DESCRIPTION

You receive this informational message if you attempt to manually uniquify your design while in the simple compile mode. This mode is intended to be used with non-uniquified designs. If you manually uniquify your design before using the **compile** command, you lose one of the benefits of the fast optimization mode and experience a longer runtime. For more information, see the man page for the **set_simple_compile_mode** command.

WHAT NEXT

To take full advantage of the fast optimization mode, remove **uniquify** from your script and rerun the script.

SEE ALSO

set_simple_compile_mode (2).

UIMG-41 (error) The variable ’change_names_use_alternative’

must be set to TRUE for xg mode.

DESCRIPTION

WHAT NEXT

UIMG-42 (error) File name cannot end with a slash (/).

DESCRIPTION

This error message occurs when you specify a file name that ends with a slash (/) character, which is illegal.

WHAT NEXT

Specify a legal file name.

The file name can be specified without a path (for the current directory), with a relative path, or with an absolute path.

All of the following file name specifications are legal:

```
adder.db

../adder.db

ALU_DESIGNS/adder.db

/designs/ALU_DESIGNS/adder.db
```

UIMG-43 (error) Cannot %s design %s:%s over existing design %s:%s.

DESCRIPTION

This error message occurs when the target design name is the same as the source design name. You cannot overwrite an existing design using the **copy_design** or the **rename_design** commands.

WHAT NEXT

If you do not specify the target file, you must specify a target design name that is

different than the source design name. If you want to copy or rename the source design to a different file while maintaining the same design name, you can specify both the file name and the design name of the target, such as new_file.db:mydesign.

If the target design already exists and you want to replace it, use the **remove_design** command before performing the copy or rename operation.

Carefully note the file names specified in the error message. Design names may exist in more than one file name.

SEE ALSO

copy_design(2)
remove_design(2)
rename_design(2)

UIMG-44 (error) Multiple designs named %s already exist.

DESCRIPTION

This error message occurs when the target design name already exists in multiple files. You cannot overwrite an existing design using the **copy_design** command or the **rename_design** command.

WHAT NEXT

If you want the target design to keep the same name as the source design, specify a file name in the destination, such as new_file.db:mydesign.

If a design of the same name already exists in the destination file, either delete it using the **remove_design** command, specify a different design name for the target, or specify a different file for the target.

In this case, you did not specify a target file name, and multiple designs with the target design name already exist. Use the **list_designs -show_file** command to see which designs exist in which files.

SEE ALSO

copy_design(2)
list_designs(2)
rename_design(2)

UIMG-45 (information) %s design %s:%s to %s:%s.

DESCRIPTION

This information message reports the file and design names of the design being copied or renamed, along with the file and the design names of the destination design.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

copy_design(2)
rename_design(2)

UIMG-46 (error) Target name must be specified.

DESCRIPTION

This error message occurs when you pass an empty target string to the **copy_design** or the **rename_design** command.

WHAT NEXT

Rerun the command and specify a valid string for the target name.

SEE ALSO

copy_design(2)
rename_design(2)

UIMG-47 (error) %s does not specify a unique design name.

DESCRIPTION

This error message occurs when **copy_design** or **rename_desing** fails to uniquely identify the design name, because there exists two or more designs across files that share the same name.

WHAT NEXT

Please specify unique design name(file_name:design_name) for **copy_design** or **rename_design** command to continue.

Use the **list_designs -show_file** command to see which designs exist in which files.

SEE ALSO

list_designs(2), copy_design(2), rename_design(2).

UIO-1 (error) Design Compiler is not enabled.

DESCRIPTION

You don’t have the Design-Compiler license available.

WHAT NEXT

Get the Design-Compiler license by invoke the **get_license Design-Compiler** command.

UIO-2 (error) %s must be ’low’, ’medium’ or ’high’.

DESCRIPTION

The defined command parameter was assigned an invalid value.

WHAT NEXT

Reexecute the command with a valid value for the defined parameter. Assign it to either *low*, *medium*, or *high*.

UIO-3 (error) Could not read the following target libraries:

DESCRIPTION

None.

WHAT NEXT

Check the listed target libraries in the error message.

UIO-4 (error) flatten_minimize strategy must be ’single_output’,

’multiple_output’ or ’none’.

DESCRIPTION

WHAT NEXT

UIO-5 (error) The library %s already contains a design %s.

DESCRIPTION

None.

WHAT NEXT

Check your design and library.

UIO-6 (error) Background directory %s exists.

DESCRIPTION

None.

WHAT NEXT

Check the listed directory.

UIO-7 (error) Could not create directory %s. Permission denied.

DESCRIPTION

None.

WHAT NEXT

Check ’write’ permission of the listed directory.

UIO-8 (error) Could not read the following synthetic library:

DESCRIPTION

A synthetic library is specified in your *synthetic_library* variable, but is not in the directories of your *search_path*. Optimization commands need a full set of synthetic libraries to run.

WHAT NEXT

Add the pathname of the library to your *search_path*, or specify a full path to the library in the command line (as in /usr/joe/my_lib.sldb), or remove the library from your *synthetic_library* variable.

UIO-9 (error) Cannot use '%s' option with the '%s' option.

DESCRIPTION

None.

WHAT NEXT

Please refer to the man page of your original command.

UIO-10 (warning) Overwriting the library '%s' with design '%s'. The library already contained this design and is now modified.

DESCRIPTION

None.

WHAT NEXT

Check the manual page of current command.

UIO-11 (error) None of the target libraries are enabled for

in_place optimization.

DESCRIPTION

The tool issues this error when target libraries are not enabled for in_place optimization.

WHAT NEXT

Check libraries specified in variable **target_library** to see if they are enabled for in_place optimization.

UIO-12 (information) Choosing a test methodology will restrict the optimization of sequential cells.

DESCRIPTION

None.

WHAT NEXT

Check the manual page of current command.

UIO-13 (error) The design '%s' already exists in library '%s' and cannot be overwritten by the 'model' command.

DESCRIPTION

None.

WHAT NEXT

Check the manual page of command **model**.

UIO-14 (error) Could not read generic technology library '%s'

DESCRIPTION

The generic technology library supplies simple combinational and sequential cells

that are useful for technology-independent component instantiation. Part descriptions, like those in synthetic libraries, use components from the generic technology library. This error only occurs if your installation of Synopsys has been corrupted.

WHAT NEXT

Contact your system administrator.

UIO-15 (warning) No target library specified.

DESCRIPTION

You must define a target library before you issue either the **compile** command or the **reoptimize_design** command.

WHAT NEXT

Use "target_library = ..." to indicate which library the design should be compiled into.

UIO-16 (error) Design '%s' contains cluster information; the compile cannot be run when clusters are present.

DESCRIPTION

The **compile** command does not accept designs that contain clusters. Please use **remove_cluster** to remove all the clusters before compile the desgin. Or, use physopt command to optimize the design containing the cluster (floorplan) information.

WHAT NEXT

Use the **remove_cluster** command to remove the clusters.

UIO-17 (error) Design does not meet the requirements of the reoptimize_design command.

DESCRIPTION

The following are the minimum requirements when using the **reoptimize_design** command:

1) Enable the *-post_layout_opto* option.

2) Enable the *-in_place* option.

3) Define a design that contains cluster information.

4) Enable the *-routability* option.

5) Specify a design that contains back-annotated capacitance values.

WHAT NEXT

Use one of the above-mentioned options, or modify the design appropriately. Or take a look at the **reoptimize_design** man page for the correct use of the command.

UIO-18 (error) The %s option can only be used in conjunction with the %s option(s).

DESCRIPTION

You have defined an invalid combination of options.

WHAT NEXT

To see the correct use of options, refer to the appropriate documentation.

UIO-19 (error) No routability constraint on design. Use set_min_porosity.

DESCRIPTION

The current design has no routability constraint, and the target libraries have no *default_min_porosity*. The design cannot be optimized for routability. Do not use the *-routability* option with the **compile** command or the **reoptimize_design** command.

WHAT NEXT

Use one **compile** or **reoptimize_design** without the *-routability* option. If you want to optimize the routability of the design, set the minimum porosity constraint on it with the **set_min_porosity** command.

UIO-20 (warning) Porosity constraint on design (%g) overwritten by default
porosity constraint in target libraries (%g). Using the default porosity constraint.

DESCRIPTION

The target libraries have a minimum porosity constraint higher than the porosity constraint set on the design. **compile -routability** and **reoptimize_design -routability** use the minimum porosity constraint from the target libraries.

The attribute *min_porosity* has been overwritten.

WHAT NEXT

To report the porosity of the design, use **report_routability**. To report the porosity constraint of the design, use **report_constraint**. If you want to increase the porosity constraint, use **set_min_porosity** with a value higher than the default porosity constraint in the target libraries. Then run **compile -routability** or **reoptimize_design -routability** again. Use **report_lib** to get the default minimum porosity constraint on a library.

UIO-21 (warning) No routability information in target library '%s'.

DESCRIPTION

The defined target library has no porosity information. It cannot be used to optimize the design for routability. The **compile -routability** command and the **reoptimize_design -routability** command optimize the design for routability. At least one target library defined with **target_library** must contain routability information.

WHAT NEXT

Make sure that at least one target library in the search path has routability information. To list all target libraries on the search path, use **list target_library**. To report library characteristics, including routability information, use **report_lib**.

UIO-22 (error) No target library has routability information.

Design was not optimized.

DESCRIPTION

No target library has routability information. The current design was not optimized because it cannot be optimized for routability with the current target libraries.

WHAT NEXT

To optimize the design, use **compile** or **reoptimize_design** without the *-routability* option.

If you want to compile the design for routability, define a target library with routability information. To report the characteristics of a library, use **report_lib**. To specify a target library, use **target_library**. With Library Compiler, add the routability information in the target library. Without Library Compiler, ask the vendor who owns the library to add routability information.

UIO-23 (error) Design '%s' contains cluster information; the %s command cannot be run when clusters are present.

DESCRIPTION

The **translate**, **balance_registers**, **balance_buffer**, and **replace_fpga** commands do not accept designs that contain clusters. To proceed, use **remove_clusters** to remove the clusters from the design.

WHAT NEXT

Use the **remove_clusters** command to remove the clusters from the current_design. Then reissue the command that failed.

UIO-24 (warning) Design '%s' does not contain back-annotated capacitance and/or resistance values.

DESCRIPTION

Generally, post-layout optimization should be executed on designs that contain back-annotated capacitance or resistance values.

The *post_layout_opto* capability can be run on designs that do not contain back-annotation, but the preferred methodology is to run the design through an incremental compile. If the design contains cluster information, the

reoptimize_design command can be used to incrementally optimize the design. These options give better results than post-layout optimization because they allow the most flexibility.

WHAT NEXT

This is only a warning. No special action is required.

UIO-25 (error) DC-Expert license is not enabled for '%s'.

DESCRIPTION

You need a DC-Expert license to use the **reoptimize_design** and **create_wire_load** commands. Your site might not have acquired a license, or other processes might be using all the available licenses.

WHAT NEXT

To get the DC-Expert license, invoke the **get_license DC-Expert** command, or contact your Synopsys representative.

UIO-26 (error) Floorplan-Management license is not enabled for '%s'.

DESCRIPTION

You need Floorplan-Management license to run **reoptimize_design**, **read_clusters**, **write_clusters**, **create_cluster** and **create_wire_load**. Your site might not have acquired a Floorplan-Management license, or other processes might be using all the licenses available.

WHAT NEXT

To get the Floorplan-Management license, invoke the **get_license Floorplan-Management** command, or call your Synopsys representative.

UIO-27 (warning) Must have a Behavioral Compiler license to

use ’%s’.

DESCRIPTION

None.

WHAT NEXT

Get a Behavioral Compiler license.

UIO-28 (error) Design scan style is not supported by the -scan option.

DESCRIPTION

The -scan option makes compile use scan cells. Before invoking the command, the user must associate a supported scan style with the design using the **set_scan_style** command or the **test_default_scan_style** environment variable. This message says that the specified scan style is not supported.

WHAT NEXT

Use the **set_scan_style** command to specify a supported scan style.

UIO-29 (error) You cannot specify polarity unless you use the async_reset option.

DESCRIPTION

None.

WHAT NEXT

Check the manual page of command **optimize_registers**.

UIO-30 (error) Cannot find reset_port %s on design %s.

DESCRIPTION

None.

WHAT NEXT

Check the manual page of command **optimize_registers**.

UIO-31 (error) You have to specify the polarity of the reset to be either active high or low.

DESCRIPTION

WHAT NEXT

UIO-32 (error) Unexpected value for polarity. Accepted values are high and low.

DESCRIPTION

WHAT NEXT

UIO-33 (warning) optimize_registers no longer flattens the design hierarchy by default. Unless you specify the flatten option, the hierarchy of the design will be preserved.

DESCRIPTION

None.

WHAT NEXT

Check the manual page of command **optimize_registers**.

UIO-35 (error) ECO-Compiler license is not enabled for '%s'.

DESCRIPTION

You need an ECO-Compiler license to use the **eco_analyze_design** and **eco_implement** commands. Your site might not have acquired a license, or other processes might be using all the available licenses.

WHAT NEXT

To get the ECO-Compiler license, invoke the **get_license ECO-Compiler** command, or contact your Synopsys representative.

UIO-37 (error) insert_pads accepts design objects as arguments

DESCRIPTION

The insert_pads commands accepts as its arguments designs on which I/O pads need to be inserted.

WHAT NEXT

Run the insert_pads command with design objects as arguments.

UIO-38 (error) The number of stages you have chosen is lower than two.

DESCRIPTION

For pipelining, at least one level of registers must be inserted into the design, which corresponds to two stages. In general the number of registers is one less than the number of stages.

WHAT NEXT

Choose two stages or more.

UIO-39 (error) You have specified both a synchronous and and

asynchronous reset port.

DESCRIPTION

The registers that are inserted for pipelining can only have one type of reset. Therefore you have to choose between synchronous or asynchronous reset.

WHAT NEXT

Select either ’-async_reset <port_name>’ or ’-sync_reset <port_name>’.

UIO-40 (error) You have specified a reset polarity but no reset port.

DESCRIPTION

It is only useful to have reset polarity if there is actually a reset port.

WHAT NEXT

Select either ’-async_reset <port_name>’ or ’-sync_reset <port_name>’ or remove the ’-reset_polarity high | low’ option from the command line.

UIO-41 (error) The number of stall ports that you have specified does
not match the number of stages.

DESCRIPTION

There can be either one stall port for all inserted registers or one stall port for each inserted row of registers (i.e. the number of stall ports must be either one or one less than the number of stages).

WHAT NEXT

Check the number of pins and the number of stages you have specified.

UIO-42 (error) Two stall ports have the same name (’%s’ and

’%s’).

DESCRIPTION

Names of stall ports must be unique for a valid design.

WHAT NEXT

Choose another name for one of the ports.

UIO-43 (error) A stall port (’%s’) has the same name as the clock port (’%s’).

DESCRIPTION

The names of all ports of the design must be unique.

WHAT NEXT

Choose another name for one of the ports.

UIO-44 (error) A stall port (’%s’) has the same name as the synchronous reset port (’%s’).

DESCRIPTION

The names of all ports of the design must be unique.

WHAT NEXT

Choose another name for one of the ports.

UIO-45 (error) A stall port (’%s’) has the same name as the asynchronous

reset port (’%s’).

DESCRIPTION

The names of all ports of the design must be unique.

WHAT NEXT

Choose another name for one of the ports.

UIO-46 (error) The clock port (’%s’) has the same name as the synchronous reset port (’%s’).

DESCRIPTION

The names of all ports of the design must be unique.

WHAT NEXT

Choose another name for one of the ports.

UIO-47 (error) The clock port (’%s’) has the same name as the asynchronous reset port (’%s’).

DESCRIPTION

The names of all ports of the design must be unique.

WHAT NEXT

Choose another name for one of the ports.

UIO-48 (error) The reset polarity must be either ’high’ or ’low’. ’%s’ has been specified.

DESCRIPTION

The reset can be either active high or active low.

WHAT NEXT

Choose a valid option.

UIO-49 (error) The stall polarity must be either ’high’ or ’low’. ’%s’ has been specified.

DESCRIPTION

The stall can be either active high or active low.

WHAT NEXT

Choose a valid option.

UIO-50 (error) ’%s’ has been specified as the clock port, but there is no such external port in design ’%s’.

DESCRIPTION

The name of the clock port specified must match the name of a port of the design.

WHAT NEXT

Check the name’s spelling or add an appropriate port to the design.

UIO-51 (error) ’%s’ has been specified as the reset port, but there is no such external port in design ’%s’.

DESCRIPTION

The name of the reset port specified must match the name of a port of the design.

WHAT NEXT

Check the name’s spelling or add an appropriate port to the design.

UIO-52 (error) ’%s’ has been specified as a stall port, but there is no
such external port in design ’%s’. If you have a port of the correct name,
it must be exactly one bit wide.

DESCRIPTION

The name of the stall ports specified must match the name of a port of the design, and it must be a one bit wide port of the design.

WHAT NEXT

Check the name’s spelling; add an appropriate port to the design or reduce the number of bits for the port to one.

UIO-53 (error) The stall port ’%s’ does not have direction ’in’.

DESCRIPTION

Stall ports must be inputs to the design.

WHAT NEXT

Change the direction to ’in’ or specify the direction ’in’ if you did not yet specify a direction.

UIO-54 (error) The reset port ’%s’ does not have direction ’in’.

DESCRIPTION

Reset ports must be inputs to the design.

WHAT NEXT

Change the direction to ’in’ or specify the direction ’in’ if you did not yet specify a direction.

UIO-55 (error) The clock port '%s' does not have direction 'in'.

DESCRIPTION

Clock ports must be inputs to the design.

WHAT NEXT

Change the direction to 'in' or specify the direction 'in' if you did not yet specify a direction.

UIO-56 (error) The name '%s' is not a legal HDL identifier for a (non-vector) single bit port.

DESCRIPTION

Port names must be simple legal HDL identfier containing only alphanumeric characters and underscores ('_').

WHAT NEXT

Change the name to a legal identifier name. This may mean that you have to split up vector stall ports into single stall ports.

UIO-57 (error) You have specified a stall polarity but no stall port.

DESCRIPTION

It is only useful to have a stall polarity if there is actually a stall port.

WHAT NEXT

Select either '-stall_port <port_list>' or remove the '-stall_polarity high | low' option from the command line.

UIO-58 (warning) As a result of -prioritize_min_path, min_delay

is made a higher priority than max_delay.

DESCRIPTION

None.

WHAT NEXT

None.

UIO-59 (warning) Setting attribute 'fix_multiple_port_nets' on design '%s'.

DESCRIPTION

The environment variable **compile_fix_multiple_port_nets** is replaced by the command **set_fix_multiple_port_nets**. For compatibility, if the variable is enabled during **compile** or **report_constraints** but no attribute exists on the design, the attribute is set as if the command **set_fix_multiple_port_nets -all** was used. Once the attribute is set it will not be removed even if the variable is set to FALSE.

WHAT NEXT

Update your compile script to use the **set_fix_multiple_port_nets** command instead of the **compile_fix_multiple_port_nets** variable.

UIO-60 (warning) Ignoring compile_fix_multiple_port_nets = %s.

DESCRIPTION

The command **set_fix_multiple_port_netsP replaces the environment variable compile_fix_multiple_port_nets**. When both the attribute and the variable are set, the attribute has priority and the variable setting is ignored.

WHAT NEXT

Update your compile scripts to use the **set_fix_multiple_port_nets** command instead of the **compile_fix_multiple_port_nets** variable.

UIO-61 (warning) Setting attribute ’critical_range’ on design ’%s’.

DESCRIPTION

The environment variable **compile_default_critical_range** is replaced by the command **set_critical_range**. For compatibility, if the variable is enabled during **compile** but no attribute exists on the design, the attribute is set to the current value of the variable. Once the attribute is set it will not be removed even if the environment variable is changed to another value, so that reports correctly show the value which was used during optimization.

WHAT NEXT

Update your script to use the **set_critical_range** command instead of the **compile_default_critical_range** variable.

UIO-62 (warning) Ignoring compile_default_critical_range = %g.

DESCRIPTION

The command **set_critical_range** replaces the environment variable **compile_default_critical_range**. When both the attribute and the variable are set, The attribute has priority and the variable setting is ignored. The warning is issued when the design attribute and the environment variable are set to different values. The attribute might have been set by a previous **compile** of the design. The **compile** command sets the attribute (and issues warning **UIO-61**) if there is no attribute and the environment variable is set, so that subsequent reports see the same value.

WHAT NEXT

Update your scripts to use the **set_critical_range** command instead of the **compile_default_critical_range** variable.

UIO-63 (warning) Setting attribute ’cost_priority’ on design ’%s’.

DESCRIPTION

The environment variables such as **compile_promote_delay_cost** for changing the optimization cost priority are obsolete, and are replaced by the command **set_cost_priority**. For compatibility, if the variable is set during **compile** but no **cost_priority** attribute exists on the design, the attribute is set to reflect the current value of the variable. Once the attribute is set it will not be removed even

if the environment variable is changed to another value, so that reports correctly show the value that was used during optimization. Once the attribute is set, the variable setting is ignored (indicated by warning **UIO-64**).

WHAT NEXT

Update your script to use the **set_cost_priority** command. Use **report_cost_priority** to see the current attribute setting of a design.

UIO-64 (warning) Attribute 'cost_priority' overrides '%s'.

DESCRIPTION

The command **set_cost_priority** replaces the given environment variable. When both the attribute and the variable are set, the attribute has priority and the variable setting is ignored. The attribute might have been set by a previous **compile** of the design. The **compile** command sets the attribute (and issues warning **UIO-63**) if there is no attribute and the environment variable is set, so that subsequent reports see the same value.

WHAT NEXT

Update your scripts to replace setting of the obsolete variable by the **set_critical_range** command. Use **report_compile_options** to see what cost priority is currently set on a design.

UIO-65 (error) DC ultra license is required to use feature '%s'.

DESCRIPTION

DC ultra license is required to use the features supported in the DC ultra package only. Please see the set_ultra_optimization command for a detailed set of these features.

If you are seeing this error message while invoking compile, there can be a couple of reasons. You could have used any of the commands supported only by the DC ultra package during the current session. Such commands normally acquire and retain the DC ultra license. However if you use **remove_license** command followed by compile, you might get this error if all the DC ultra licenses are in use by other users.

Secondly, you could have read in a db file which had been generated using the DC ultra features. An attribute is added to a db when compile is run using the DC ultra license. Hence, you can confirm that the db was generated using a DC ultra license by using the command:

get_attribute current_design compiled_with_ultra

WHAT NEXT

Use command **set_ultra_optimization [-force]**. This command will try to acquire the DC ultra license.

UIO-66 (error) Command '%s' unable to acquire DC ultra license.

DESCRIPTION

DC ultra license is not available or checked out.

WHAT NEXT

Use command **set_ultra_optimization [-force]**. This command will try to acquire the DC ultra license.

UIO-67 (information) %s mode successfully set.

DESCRIPTION

WHAT NEXT

UIO-68 (warning) %s mode not set.

DESCRIPTION

DC ultra license is not available or checked out.

WHAT NEXT

Use command **set_ultra_optimization [-force]**. This command will try to acquire the DC ultra license.

UIO-69 (error) The async_reset option has been discontinued

because of quality of results and correctness issues. If you need to retime registers with asynchronous clear or preset Please contact the Synopsys Support Center or your Synopsys AC for further support. If you do not want to retime registers with asynchronous clear or preset, please remove the async_reset and
the polarity option from the command.

DESCRIPTION

Retiming for flip-flops with asynchronous functionality using the async_reset option only handled flip-flops directly connected to a reset port. Only one set of registers connected to one port was retimed at an invocation of he command. The initial state of the circuit was not preserved. This caused usually bad quality of results or incorrect behavior of the circuit.

WHAT NEXT

Remove the async_reset and polarity options from the optimize_registers command. Review the manual page of the retiming command for alternative options or contact the Synopsys Support Center or your local Synopsys AC for alternatives.

UIO-70 (warning) The ’verbose’ option has been used without the
’check_design’ option and will be ignored.

DESCRIPTION

The ’verbose’ option indicates that the output of the ’check_design’ option should list individual cells names in the statistics part.

WHAT NEXT

Use ’check_design’ and ’verbose’ together or do not use ’verbose’ with your retiming command.

UIO-71 (information) %s mode successfully reset.

DESCRIPTION

WHAT NEXT

UIO-72 (error) Option '%s' not recognized.

DESCRIPTION

The option mentioned above is not a valid option.

WHAT NEXT

See the man page of the command for a list of valid options.

UIO-73 (information) %s optimization mode successfully set.

DESCRIPTION

WHAT NEXT

UIO-74 (information) %s optimization mode successfully reset.

DESCRIPTION

WHAT NEXT

UIO-75 (error) Instances of design '%s' have inconsistent **dont_touch** attributes.

DESCRIPTION

Running **compile -bottom_up** requires that instances of a design either all have or all do not have the **dont_touch** attribute. If you receive this message, **compile** has

detected that some, but not all, instances of the specified design have the **dont_touch** attribute.

WHAT NEXT

Ensure that all instances of the design either have or do not have the **dont_touch** attribute.

SEE ALSO

compile(2), **set_dont_touch(2)**.

UIO-76 (information) DC simple compile mode successfully set.

DESCRIPTION

WHAT NEXT

UIO-77 (information) DC simple compile mode successfully reset.

DESCRIPTION

WHAT NEXT

UIO-78 (warning) Ignoring '%s' option.

DESCRIPTION

You receive this message if you specify **compile -top** along with the **-no_map**, **-exact_map**, or **-scan** options. **compile -top** does not perform any mapping on the design, so the specified option is ignored.

WHAT NEXT

No action is required.

UIO-80 (error) The ’-quickturn’ option of compile cannot be used without a Quickturn supplied library.

DESCRIPTION

Your library does not have the required attributes that are placed on Quickturn libraries. You cannot use the -quickturn option of compile.

WHAT NEXT

Contact your Synopsys or Quickturn representative.

UIO-81 (information) Enabling special fast optimization for Quickturn libraries.

DESCRIPTION

A special optimization setting is enabled for Quickturn libraries. This setting is streamlined for shorter runtime.

WHAT NEXT

UIO-85 (warning) Ignoring design cell degradation information.

DESCRIPTION

The cell degradation information present on the design is being ignored. There can be two reasons for this. First reason is DC ultra license is not available or checked out. Secondly, the environment variable compile_fix_cell_degradation is set to "false".

WHAT NEXT

Use command **set_ultra_optimization [-force]**. This command will try to acquire the DC ultra license. Also check the environment variable compile_fix_cell_degradation.

UIO-86 (warning) Ignoring library cell degradation information.

DESCRIPTION

The cell degradation information present in the library is being ignored. There can be two reasons for this. First reason is DC ultra license is not available or checked out. Secondly, the environment variable compile_fix_cell_degradation is set to "false".

WHAT NEXT

Use command **set_ultra_optimization [-force]**. This command will try to acquire the DC ultra license. Also check the environment variable compile_fix_cell_degradation.

UIO-90 (warning) variable '%s' is obsolete; see the manual page.

DESCRIPTION

The variable being used is obsolete.

WHAT NEXT

See the manual for further details.

UIO-91 (warning) Multiple designs named '%s' occur in the link_library.
None of these designs will be used during link.
Design '%s' ignored.

DESCRIPTION

WHAT NEXT

UIO-92 (warning) Design '%s' comes before design '%s' in the

link_library; '%s' will be ignored.

DESCRIPTION

If the **link** command detects multiple designs with the same name in the **link_library**, **link** uses the first design found, ignores all others, and issues this warning message. **link** uses the first design found to resolve all design references with this name. Often, the design that appears first in the **link_library** was read into memory before other designs with the same name.

WHAT NEXT

Use the **list_designs** command to view a list of the designs that are in memory. If **link** has chosen the design you want to use, you do not need to take any action. Otherwise, keep the design you want and remove all other designs that have the same name, using the **remove_design** command. Then re-link using the **link** command.

To suppress this message and the informational message "UIO-93" in the future, add "UIO-92" to the **suppress_errors** variable in your **.synopsys_dc.setup** file.

SEE ALSO

link(2), **list_designs(2)**, **remove_design(2)**, **link_library(3)**, **suppress_errors(3)**, **.synopsys_dc.setup**, **UIO-93(n)**.

UIO-93 (information) Design '%s' is referenced in design '%s'.

DESCRIPTION

The **link** command has detected multiple designs with the same name in the **link_library**; the first design found was used to resolve all design references with this name. This message lists those designs in the design hierarchy that reference the first specified design.

WHAT NEXT

Check the designs that reference the first specified design to verify that the correct design is used in all cases. For more information, see the description for warning "UIO-92".

To suppress this message in the future, add "UIO-93" to the **suppress_errors** variable in your **.synopsys_dc.setup** file.

SEE ALSO

link(2), **link_library(3)**, **suppress_errors(3)**, **.synopsys_dc.setup**, **UIO-92(n)**.

UIO-94 (error) Current design is not defined.

DESCRIPTION

This error message is generated when the current design is not defined in **dc_shell**.

WHAT NEXT

Use the **list_designs** command to display designs in memory; or use **read** to read a design in. Then invoke the **current_design** command to set the current design.

SEE ALSO

current_design (2), **list_designs** (2), **read** (2).

UIO-95 (error) %s must be 'none', 'low', 'medium' or 'high'.

DESCRIPTION

The defined command parameter was assigned an invalid value.

WHAT NEXT

Reexecute the command with a valid value for the defined parameter. Assign it to either *none*, *low*, *medium*, or *high*.

UIO-96 (error) Doing reoptimize_design without back-annotation

DESCRIPTION

reoptimize_design should be used for post-layout optimization. This command needs back-annotation information to perform layout sensitive synthesis. You should provide SDF, net load as well as cell locations (for example, PDEF 2.0) which is required for Location-Based Optimization (LBO).

WHAT NEXT

Obtain back-annotation information. Please refer to the user manual for more information.

UIO-97 (error) Cannot estimate load or delay without RC coefficients

DESCRIPTION

You need to provided RC coefficients to reoptimize_design through the following four variables:

lbo_vertical_resistancelbo_vertical_capacitance lbo_horizontal_resistance lbo_horizontal_capacitance

WHAT NEXT

Please obtain the RC coefficients. You may also provide necessary

UIO-98 (error) Illegal combination of reoptimize_design options

DESCRIPTION

You can either specify -map_effort or those detailed controls like -sizing, -pin_swap, etc.; but not both.

WHAT NEXT

Please choose the proper combination of options

UIO-99 (warning) options '%s' is obsolete; see the manual page.

DESCRIPTION

The option being used is obsolete.

WHAT NEXT

See the manual for further details.

UIO-100 (warning) Doing compile -in_place without back-

annotation

DESCRIPTION

compile -in_place should be used for post-layout optimization. This command needs back-annotation information to perform layout sensitive synthesis. Ideally, you should provide both SDF and net load. Please also consider using reoptimize_design instead of compile -in_place, since the former does much better optimization and provides the Location-Based Optimization (LBO) capability which could achieve better timing convergence.

WHAT NEXT

Obtain back-annotation information. Please refer to the user manual for more information.

UIO-101 (error) Doing reoptimize_design without delay back-annotation

DESCRIPTION

reoptimize_design command needs back-annotation information to perform layout sensitive synthesis. You should provide the SDF file in addition to net load and cell locations (for example, PDEF 2.0).

WHAT NEXT

Obtain back-annotation information. Please refer to the user manual for more information.

UIO-102 (error) Doing reoptimize_design without load back-annotation

DESCRIPTION

reoptimize_design command needs back-annotation information to perform layout sensitive synthesis. You should provide net load information in addition to the SDF file and cell locations (for example, PDEF 2.0).

WHAT NEXT

Obtain back-annotation information. Please refer to the user manual for more

information.

UIO-109 (error) Doing reoptimize_design without delay back-annotation and cell locations

DESCRIPTION

reoptimize_design command needs back-annotation information to perform layout sensitive synthesis. You should provide the SDF file in addition to net load. You also need to provide cell location information (for example, PDEF 2.0) for Location-Based Optimization (LBO) which could achieve better timing convergence.

WHAT NEXT

Obtain back-annotation information. Please refer to the user manual for more information.

UIO-110 (error) Doing reoptimize_design without net load back-annotation and cell locations

DESCRIPTION

reoptimize_design command needs back-annotation information to perform layout sensitive synthesis. You should provide net load information in addition to the SDF file. You also need to provide cell location information (for example, PDEF 2.0) for Location-Based Optimization (LBO) which could achieve better timing convergence.

WHAT NEXT

Obtain back-annotation information. Please refer to the user manual for more information.

UIO-111 (warning) Doing reoptimize_design without cell location

DESCRIPTION

It is hightly recommended not to do reoptimize_design without cell locations, in which case wire load model will be used to estimate the capacitance for all new nets added. This could result in inaccurate timing estimation and thus make it harder to

achieve timing convergence.

You should provide cell location information (for example, PDEF 2.0) to perform Location-Based Optimization (LBO).

WHAT NEXT

Obtain back-annotation information. Please refer to the user manual for more information.

UIO-113 (error) Invalid argument for the -justification_effort option. Valid arguments are low, medium, or high.

DESCRIPTION

You receive this message if you issue **optimize_registers** or **set_optimize_registers** command with an invalid argument for the **-justification_effort** option. Valid arguments are low, medium, and high.

WHAT NEXT

Reissue the **optimize_registers** or the **set_optimize_registers** command with a valid argument for the **-justification_effort** option.

SEE ALSO

optimize_registers (2). **set_optimize_registers** (2).

UIO-127 (error) You cannot use the -post_route option without also using the -incremental option.

DESCRIPTION

You receive this message if you execute **physopt** with the **-post_route** option, and do not also use the **-incremental** option. You cannot use **-post_route** without **-incremental**. Optimization with post-route annotation requires that all cells have locations.

WHAT NEXT

Reexecute the **physopt** command, either with both the **-post_route** and **-incremental** options, or without **-post_route**.

SEE ALSO

physopt (2).

UIO-128 (error) At least one of the specified pins is of type INOUT.
Only input or output pins can be buffered.

DESCRIPTION

You receive this error message if you have attempted to insert a buffer and specified a pin in the input pin list which is of type INOUT. Only input or output pins can be buffered.

WHAT NEXT

Remove any pins with incorrect directions, and try the command again.

SEE ALSO

UIO-129 (error) Some but not all of the driver pins on a net were specified.
Must specify all or none.

DESCRIPTION

You receive this error message if you have attempted to insert a buffer and specified at least one, but not all of the driver pins of the net. When all driver pins are specified, the new inserted buffer will be driven by all the driver pins together, and the new buffer will in turn drive all of the loads of the original net.

WHAT NEXT

If a net is driven my multiple pins, include all of the driver pins in the pin list.

SEE ALSO

UIO-130 (error) A default buffer in the vendor library could not be

found.

DESCRIPTION

You receive this error message if you have attempted to insert a buffer, but a default buffer could not be found in the vendor library. Since a default buffer is instantiated by the command, it is necessary for a default buffer to be present. It is very unusual for this situation to occur, and suggests a more serious error of some kind, particularly with the vendor library.

WHAT NEXT

Check the correctness of the selected library and insure there is a default buffer in the library.

SEE ALSO

UIO-131 (error) Invalid argument for the -sync_transform option. Valid arguments are decompose, multiclass, or dont_retime.

DESCRIPTION

You receive this message if you issue **optimize_registers** or **set_optimize_registers** command with an invalid argument for the **-sync_transform** option. Valid arguments are decompose, multiclass, and dont_retime.

WHAT NEXT

Reissue the **optimize_registers** or the **set_optimize_registers** command with a valid argument for the **-sync_transform** option.

SEE ALSO

optimize_registers (2). **set_optimize_registers** (2).

UIO-132 (error) Invalid argument for the -async_transform option. Valid arguments are decompose, multiclass, or

dont_retime.

DESCRIPTION

You receive this message if you issue **optimize_registers** or **set_optimize_registers** command with an invalid argument for the **-async_transform** option. Valid arguments are decompose, multiclass, and dont_retime.

WHAT NEXT

Reissue the **optimize_registers** or the **set_optimize_registers** command with a valid argument for the **-async_transform** option.

SEE ALSO

optimize_registers (2). **set_optimize_registers** (2).

UIO-134 (error) Object %s does not have a connected net.

DESCRIPTION

When driver pins are used to specify the loads to be moved in the argument list of the move_load_pins command, they must have a connected net.

WHAT NEXT

SEE ALSO

UIO-135 (error) The specified destination object, %s, is not on a net equivalent to the source net.

DESCRIPTION

You receive this error message if you have specified an logically incorrect destination for the move_load_pins command, and you did not specify the -force option. By default, loads will only be moved to electrically equivalent nets.

WHAT NEXT

SEE ALSO

UIO-136 (error) Cell %s is not a library cell.

DESCRIPTION

You receive this error message if you have specified a cell that is not a library cell (for example, a hierarchical cell). Only library cells can be decomposed.

WHAT NEXT

Reexecute the command and specify only library cells.

UIO-137 (error) Cell %s is not a library cell.

DESCRIPTION

You receive this error message if you have specified a cell which is not a library cell. Only library buffers can be removed with this command.

WHAT NEXT

SEE ALSO

UIO-138 (error) Cell %s is neither a buffer nor an inverter.

DESCRIPTION

You receive this error message if you have specified a cell that is neither a buffer nor an inverter. Only buffers and inverters can be removed with this command. Inverters must be removed in pairs, and listed sequentially in the command argument.

WHAT NEXT

Reexecute the command, and specify only cells that are either buffers or inverters. Ensure that you list inverters in pairs, sequentially in the command argument.

UIO-139 (error) Unable to insert buffer for parallel devices.

DESCRIPTION

You receive this error message if you have attempted to insert a buffer by specifying an input pin on a cell which has an identical parallel cell.

WHAT NEXT

Either remove the specification from the object list, or insert a buffer into all of the parallel devices by specifying all the input pins of the parallel devices in the object list of the command.

SEE ALSO

UIO-140 (error) Could not make %d copies of cell %s.

DESCRIPTION

You receive this error message if you have specified an incorrect argument for the duplicate_cell command. Potential problems include an incorrect specification of the number of times to duplicate the cell, or and of the cell objects is incompatible with the command.

WHAT NEXT

SEE ALSO

UIO-141 (error) Object %s and destination object %s reside on different levels of hierarchy.

DESCRIPTION

You receive this error message if you issue the **move_load_pins** command and the source and destination of an object you specify to be moved are at different levels of hierarchy. You can move an object only to a destination that is at the same level of hierarchy as the source.

WHAT NEXT

Reissue the **move_load_pins** command and specify objects to be moved only to a

destination at the same level of hierarchy.

SEE ALSO

move_load_pins (2).

UIO-142 (error) At least one of the specified pins is not connected to a net.

DESCRIPTION

You receive this error message if you issue the **insert_buffer** command with a pin list that contains at least one unconnected pin. You cannot insert a buffer on an unconnected pin.

WHAT NEXT

Reissue the **insert_buffer** command and specify only pins that are connected to a net.

SEE ALSO

insert_buffer (2).

UIO-143 (error) The specified pin is not on a hierarchical cell

DESCRIPTION

You receive this error message if you have specified a pin which is not on a hierarchical cell. For example, if the pin is on a vendor library cell, or if a port in current_design is specified, this error will be issued.

WHAT NEXT

SEE ALSO

UIO-144 (error) Bidirectional pins cannot be duplicated

DESCRIPTION

You receive this error message if you have specified a pin which is marked as bidirectional. Reissue the command with a pin which has a direction specified as either 'in' or 'out'.

WHAT NEXT

SEE ALSO

UIO-145 (error) The number of copies requested is greater than the number of loads driven by the specified pin

DESCRIPTION

You receive this error message if you have specified the creation of too many copies of a pin. The number of copies must not be greater than the number of loads driven by the net of the specified pin.

WHAT NEXT

SEE ALSO

UIO-146 (error) Design %s could not be found in the hierarchical path to the specified object.

DESCRIPTION

You receive this error message if you have specified a design using the -design argument which could not be found in the path to the specified object. This message may be produced by several different commands.

WHAT NEXT

You must insure that somewhere in the hierarchical path to the object can be found the design specified using the -design switch. For example, using the command "remove_buffer T1/U1/G1/buf1 -design A", one of the instances T1, U1, or G1, must be an instance of design A.

SEE ALSO

UIO-147 (error) A single inverter, %s, was specified without a matching inverter. Inverters to be removed must be specified in sequential pairs.

DESCRIPTION

You receive this error message if you have specified the removal of an inverter without a matching inverter. This command removes either buffers or inverter pairs. If an inverter is specified, it must be directly followed in the command argument with its connected matching inverter.

WHAT NEXT

SEE ALSO

UIO-148 (error) Inverter %s does not have a matching inverter which is connected in series.

DESCRIPTION

You receive this error message if you have specified the removal of an inverter pair, but the inverters specified are not connected in series in the netlist. In order to remove inverter pairs, the inverters must be connected in series and specified sequentially in the command argument.

WHAT NEXT

SEE ALSO

UIO-149 (error) Inverter %s is not at the same hierarchical level as its connected matching inverter.

DESCRIPTION

You receive this error message if you have specified the removal of an inverter pair which is connected in series across a hierarchical boundary. Inverters must be connected in series, specified sequentially in the command arguments, and at the same level of hierarchy in order to be removed.

WHAT NEXT

SEE ALSO

UIO-150 (warning) You have chosen the no_compile option of the %s command. The resulting circuit may not show the best possible area and timing yet.

DESCRIPTION

This warning message occurs when you use the **no_compile** option of this command. The resulting circuit may not yet show the best possible area and timing. Run an incremental **compile** or **physopt** command to achieve the best results.

WHAT NEXT

This is only a warning message. No action is required.

However, you can compile the circuit with a command such as **compile -incr** or **physopt -incr**.

SEE ALSO

compile(2)
physopt(2)

UIO-151 (error) Only one object is allowed when the -design argument is activated

DESCRIPTION

Without the -design argument, many commands accept a list of objects on which to operate. With the -design argument, only one object is allowed, whether or not it is specified in list format.

WHAT NEXT

SEE ALSO

UIO-152 (error) Designs with %s are not supported in xg mode.

DESCRIPTION

You receive this message if you execute the **compile** command in xg mode, and the design requires operations that are not yet implemented in xg mode; for example, resource sharing algorithms. Currently, you can use the **compile** command in xg mode only on designs that have only gate-level and generic random logic, to perform simple operations (for example, incremental mapping optimizations or design rule fixing).

WHAT NEXT

If you did not expect the design to have DesignWare or FSMs, make sure that the intended design files were read. Otherwise, you must perform the specified operation in the normal dc_shell-t shell, not in xg mode.

SEE ALSO

compile (2).

UIO-153 (error) Option %s is not supported by the %s command.

DESCRIPTION

You received this message because the option you issued is invalid for the specified command.

WHAT NEXT

For a listing of command options, from within dc_shell execute *command_name* -help. Then reexecute the command using valid options.

UIO-154 (error) Either area or delay must be specified when using the -auto_ungroup argument for the compile command.

DESCRIPTION

This error message occurs when running the the **compile -auto_ungroup** command without specifying either the **area** or the **delay** argument. One of the two arguments must be specified, since different criteria are used for each case.

WHAT NEXT

Reexecute the **compile -auto_ungroup** command and specify either the **area** or the **delay** argument.

SEE ALSO

compile(2)

UIO-155 (error) The fpga_technology '%s' is not supported.

DESCRIPTION

The specified fpga technology is not supported by DCFPGA.

WHAT NEXT

Please see the set_fpga_defaults man pages for supported fpga technology.

SEE ALSO

set_fpga_defaults (2),

UIO-156 (error) fpga_technology is not specified.

DESCRIPTION

An "fpga_technology" argument is required to set the default values specific for that "fpga_technology".

WHAT NEXT

Please see the set_fpga_defaults man pages for supported fpga technology.

SEE ALSO

set_fpga_defaults (2),

UIO-157 (error) Target technology is not ’FPGA’. Using fpga_shell requires that all target technologies be FPGA.

DESCRIPTION

The tool issues this error when it finds that some of the target libraries do not have the target technology of FPGA, or if some of the FPGA based libraries have not been compiled for use with this tool.

WHAT NEXT

You need to add FPGA based libraries into the target_library and try again. If you add an FPGA library into the target_library field and still observe this error message, ask your vendor to provide an updated library for use with DC-FPGA.

UIO-160 (error) The -size_only switch must be used with the -incremental or -on_route switch option in physopt command.

DESCRIPTION

Optimization with -size_only restricts optimization changes to sizing changes only . It should be used only in -incremental or -on_route mode for physopt , since this is a limited optimization stage .

WHAT NEXT

See physopt manpage . For further restricting optimization to minimize eco placement changes , see -in_place_size_only option to physopt .

UIO-161 (warning) Can’t execute command ’%s’ in this context.

DESCRIPTION

This command can not be used as an embedded script in the HDL design. The command can be used as a shell script only. It is disabled as an embedded script.

WHAT NEXT

Remove this embedded command from the HDL design.

UIO-162 (error) Design ’%s’ has embedded script processing errors.

DESCRIPTION

This error message occurs when there are errors while executing the embedded script for the specified design. The errors may be due to the existence of action commands or syntax errors in the embedded script.

WHAT NEXT

Remove all action commands from the embedded script and fix any syntax errors, if present. Then remove the design from memory and read it back again.

UIO-163 (error) Design ’%s’ has embedded Tcl commands that are ignored in dcsh mode.

DESCRIPTION

This error message occurs when the specified design has embedded Tcl script that cannot be processed in dcsh mode.

WHAT NEXT

Use the Tcl mode of Design Compiler.

UIO-164 (error) Incomplete embedded Tcl script in design '%s'.

DESCRIPTION

This error message occurs when the specified design has embedded Tcl script which has unmatched braces.

WHAT NEXT

UIO-165 (error) A beta license is required to use the %s feature.

DESCRIPTION

You receive this error message when a beta license is required to use the features supported in the Design Compiler Star beta product. Refer to the set_dc_star_optimization command for a detailed set of these features.

This error message can occur while running the **compile** command if you use any of the commands supported only by the Design Compiler Star beta product during the current session. These commands normally acquire and retain the Design Compiler beta license. However, if you use the **remove_license** command followed by the **compile** command, this error occurs if all of the Design Compiler Star beta licenses are in use.

The error message can also occur when you read in a .db file that is generated using the Design Compiler Star product features. An attribute is added to the .db file when the **compile** command is run using the Design Compiler Star beta product. You can confirm that the .db file was generated using a Design Compiler beta license by executing the following command:

```
get_attribute current_design dc_star_enabled
```

WHAT NEXT

Use the **set_dc_star_optimization** command to attempt to acquire the beta license.

SEE ALSO

compile(2)
remove_license(2)
set_dc_star_optimization(2)

UIO-166 (information) %s optimization mode successfully set.

DESCRIPTION

This information message occurs when you set the optimization mode successfully.

WHAT NEXT

This is only an informational message. No action is required.

UIO-167 (information) %s optimization mode successfully reset.

DESCRIPTION

This information message occurs when you successfully reset the optimization mode.

WHAT NEXT

This is only an informational message. No action is required.

UIO-168 (error) DC Ultra cannot be disabled while DC star is active.

DESCRIPTION

DC Ultra is one of the features that gets automatically enabled if you use the set_dc_star_optimization command.

WHAT NEXT

Use command **set_dc_star_optimization false** to disable the DC star features.

UIO-170 (error) The -in_place_size_only switch must be used with the -incremental switch option in physopt command.

DESCRIPTION

Optimization with -in_place_size_only restricts optimization changes to sizing changes only . It disables optimization tricks that do new cell insertion or

existing cell deletion . The -in_place_size_only option , unlike -size_only option , is additionally contrained for minimal eco placement changes when it does sizing . With -in_place_size_only option , a cell will be sized only if the new sized cell can fit into any available space adjacent to the original cell location , to minimize eco changes . This constraint supercedes any timing or design rule cost improvement . This option should be used only in -incremental mode for physopt and preferably for post-route optimization , since this is a limited optimization stage .

WHAT NEXT

See user manual on post-route methodology.

UIO-171 (error) DC Ultra features requested, required license not available.

DESCRIPTION

You receive this error message when a DC Ultra license is required to use the features supported only in the DC Ultra package. Use the **set_ultra_optimization** command for a detailed set of these features.

This error message may occur when invoking the **compile** command if you use the **set_ultra_optimization** command to set the DC Ultra optimization mode and then cannot check out the DC Ultra license because all of the DC Ultra licenses are in use.

The message can also occur if you use the **remove_license** command to free the DC Ultra license(s) after acquiring them using the **set_ultra_optimization** command.

In either case, DC Ultra license(s) are not available after trying to acquire them using the **set_ultra_optimization** command.

WHAT NEXT

Ensure that a DC Ultra license is checked out when executing the **set_ultra_optimization** command. You can verify that the license is checked out by executing the **list** command. Check that the DC Ultra license is not freed by using the **remove_license** command between executing the **compile** command and the set_ultra_optimization command.

SEE ALSO

compile(2)
list(2)
remove_license(2)
set_ultra_optimization(2)

UIO-172 (error) Must have a Galaxy license to use '%s' option.

DESCRIPTION

You need a Galaxy license to use the options fyield_recovery and fonly_yield_recovery in physopt command. Your site might not have acquired a license.

WHAT NEXT

To get the Galaxy license, contact your Synopsys representative.

UIO-180 (error) The '%s' option is not supported in default high-effort physopt.
Please try rerunning this command with 'set physopt_disable_new_high_effort_flows true'.

DESCRIPTION

None.

WHAT NEXT

Please refer to the man page of your original command.

UIO-181 (error) The '%s' option is not supported in default high-effort physopt.
Please try running 'physopt -effort high -timing_driven_congestion'.

DESCRIPTION

None.

WHAT NEXT

Please refer to the man page of your original command.

UIO-182 (error) You have used the -edge option to optimize_registers or set_optimize_registers command without using the -clock option.

DESCRIPTION

This error message occurs because the **-edge** option must be used with the **-clock** option to the **optimize_registers** or **set_optimize_registers** command.

WHAT NEXT

Rerun the command and specify the name of the clock you want to retime using the **-clock** option. Only use the **-edge** option if you want to retime a single specific clock.

SEE ALSO

optimize_registers(2)
set_optimize_registers(2)

UIO-183 (error) %s is not a legal value for the -edge option to optimize_registers or set_optimize_registers command.

DESCRIPTION

This error message occurs when you specify an unacceptable value for the **-edge** option to the **optimize_registers** or **set_optimize_registers** command. The permitted values are **rise** and **fall**. No other values are allowed.

WHAT NEXT

Rerun the command and specify either **rise** or **fall** for the value for the **-edge** option.

SEE ALSO

optimize_registers(2)
set_optimize_registers(2)

UIO-185 (error) You cannot use the -wire_size option without the

-on_route option.

DESCRIPTION

You receive this message if you execute **physopt** with the **-wire_size** option, and do not use the **-on_route** option. You cannot use **-wire_size** without **-on_route**. Wire-based optimization requires the input design has routing.

WHAT NEXT

Reexecute the **physopt** command, either with both the **-wire_size** and **-on_route** options, or without **-wire_size**.

SEE ALSO

physopt (2).

UIO-186 (error) You cannot use the -wire_size_only option without the -on_route option.

DESCRIPTION

You receive this message if you execute **physopt** with the **-wire_size_only** option, and do not use the **-on_route** option. You cannot use **-wire_size_only** without **-on_route**. Wire-based optimization requires the input design has routing.

WHAT NEXT

Reexecute the **physopt** command, either with both the **-wire_size_only** and **-on_route** options, or without **-wire_size_only**.

SEE ALSO

physopt (2).

UIO-187 (error) The flag exclusive is not given.

DESCRIPTION

A single operation is provided on the list. You need to have either two or more operations listed or the flag exclusive on (meaning that the listed operation will not share a resource with other operations). The command

share_operations_on_one_resouce will be ignored.

WHAT NEXT

Add the flag exclusive **for that single operation, or add another operation (or both).**

UIO-188 (error) Listed operation %s is not found in the list of operations in the current design %s.

DESCRIPTION

This error message occurs because the **share_operations_on_one_resource** command requires that the listed cells all be operation cells. The command is ignored.

WHAT NEXT

Rerun the command, using the names of cells that are operation cells.

SEE ALSO

share_operations_on_one_resource(2)

UIO-189 (error) Current design %s does not contain cell %s.

DESCRIPTION

This error message occurs when the command requires that all of the listed operation cells belong to the current design.

WHAT NEXT

Rerun the command using the names of cells that belong to the current design.

SEE ALSO

share_operations_on_one_resource(2)

UIO-190 (error) The current design does not contain information

related to resource sharing.

DESCRIPTION

This error message occurs when running the **share_operations_on_one_resource** command either before elaboration or after compile.

The design does not contain information related to resource sharing until elaboration is performed. The command is ignored.

WHAT NEXT

Perform the elaboration step first, then run the **share_operations_on_one_resource** command, and then do the compile.

SEE ALSO

share_operations_on_one_resource(2)

UIO-191 (error) Listed operations belong to different processes.

DESCRIPTION

This error message occurs because the listed operations must belong to the same process, or they cannot be shared. The command is ignored.

WHAT NEXT

Check that the newly listed operations all belong to the same process and then run the command again.

SEE ALSO

share_operations_on_one_resource(2)

UIO-192 (error) An operation that was not listed was found and it was sharing with another listed operation.

DESCRIPTION

This error message occurs because it is required that if a listed operation is already sharing with another operation, then that operation must also be listed.

The operation was either not listed and was sharing with another operation, or it was listed but was sharing with an unlisted operation.

WHAT NEXT

Rerun the command and make sure that sure that any listed operation is accompanied by all of its already-sharing-with operations.

SEE ALSO

share_operations_on_one_resource(2)

UIO-193 (error) Some operations groups have conflicting manual or implementation directives (for example, %s and %s). The command is ignored.

DESCRIPTION

This error message occurs when manual and implementation directives conflict for sharing operations.

WHAT NEXT

Check that the manual or implementation directives of the listed operations do not conflict and run the command again.

SEE ALSO

share_operations_on_one_resource(2)

UIO-194 (error) Some operations groups have conflicting conflict vectors.

DESCRIPTION

This error message occurs because some operations to be shared have conflicting conflict vectors and some operation groups have conflicting vectors. The command is ignored.

WHAT NEXT

Use operations that can be shared and run the command again.

SEE ALSO

share_operations_on_one_resource(2)

UIO-196 (warning) You have specified a negative delay threshold. Using zero instead.

DESCRIPTION

This warning message occurs because the **-delay_threshold** option to the **optimize_registers** command must have a non-negative value.

WHAT NEXT

If zero it the correct value no action needs to be taken. If you want to specify a positive value run **optimize_registers** again with the correct **-delay_threshold** value.

SEE ALSO

optimize_registers(2)

UIO-197 (warning) You have specified a negative delay step. Using the computed default value instead.

DESCRIPTION

This warning message occurs because the **-delay_step** option to the **optimize_registers** command must have a non-negative value.

WHAT NEXT

If the default value works for you as desired no action needs to be taken. If you want to specify a positive value run **optimize_registers** again with the correct **-delay_step** value.

SEE ALSO

optimize_registers(2)

UIO-198 (error) You have specified delay step without a delay

threshold.

DESCRIPTION

This error message occurs because the **-delay_step** option to the **optimize_registers** command can only be specified if the **-delay_threshold** option is also specified.

WHAT NEXT

If you want to specify a delay threshold run **optimize_registers** with the **-delay_threshold** and **-delay_step** specified.

SEE ALSO

optimize_registers(2)

UIO-199 (error) %s must be ’none’, ’low’, ’medium’ or ’high’.

DESCRIPTION

The defined command parameter was assigned an invalid value.

WHAT NEXT

Reexecute the command with a valid value for the defined parameter. Assign it to either *none*, *low*, *medium*, or *high*.

UIO-200 (Error) Command ’%s’ is not supported for embedded script processing.

DESCRIPTION

This command can not be used in embedded scripts of HDL designs. Valid set of commands that can be used in HDL embedded scripts are listed below.

set_attribute
get_attribute
set_flatten
set_implementation
set_max_delay
set_model_load
set_model_drive
set_structure

```
set_design_license
set_local_link_library
set_max_area
current_design
set_ungroup
find
set_map_only
all_outputs
all_inputs
create_clock
set_optimize_registers
set_balance_registers
set_transform_for_retiming
set_boundary_optimization
set_size_only
set_dont_touch
set_dont_use
set_scan_element
set_model_map_effort
set_model_scale
set_wire_load_model
set_dont_touch_network
set_dont_retime
get_cells
get_nets
get_pins
get_ports
load_of
set_compile_directives
```

WHAT NEXT

Remove this embedded command from the HDL design.

UIO-201 (Error) Set of commands '%s' have one or more unsupported embedded script commands.

DESCRIPTION

Contains one or more commands which can not be used in embedded HDL scripts or one or more commands with syntax errors. Valid set of commands that can be used in HDL embedded scripts are listed below.

```
set_attribute
get_attribute
set_flatten
set_implementation
set_max_delay
```

set_model_load
set_model_drive
set_structure
set_design_license
set_local_link_library
set_max_area
current_design
set_ungroup
find
set_map_only
all_outputs
all_inputs
create_clock
set_optimize_registers
set_balance_registers
set_transform_for_retiming
set_boundary_optimization
set_size_only
set_dont_touch
set_dont_use
set_scan_element
set_model_map_effort
set_model_scale
set_wire_load_model
set_dont_touch_network
set_dont_retime
get_cells
get_nets
get_pins
get_ports
load_of
set_compile_directives

WHAT NEXT

Remove this embedded command from the HDL design.

UIO-202 (warning) Cannot use the ’-edge’ option with the ’-latch’ option.

DESCRIPTION

Using the -latch option and the -edge option of the optimize_registers or set_optimize_registers command does not make sense. When latches are retimed both phases of the latch system are retimed at the same time.

WHAT NEXT

You can ignore the warning for now. For the next run remove the ’edge’ option from

the optimize_registers or the set_optimize_registers command.

UIO-205 (warning) ’dont_retime’ has been selected as transformation for both synchronous and asynchronous sequential cells.

DESCRIPTION

The transformation option ’dont_retime’ has been selected for both synchronous and asynchronous sequential cells. No sequential cells will be moved during retiming unless you have the transform_for_retiming attribute set on specific cells.

WHAT NEXT

If you want to move registers during retiming, make sure you select ’multiclass’ or ’decompose’ for at least one of the ’-sync_trans’ or ’-async_trans’ options. Alternatively you should make sure at least some sequential cells have the transform for retiming attribute set to a value different from ’dont_retime’.

UIO-206 (error) The -layer -availability option is no longer supported under the enhanced router mode. Please use create_route_guide instead.

DESCRIPTION

This option is no longer supported.

WHAT NEXT

Use the create_route_guide command to specify layer availability.

SEE ALSO

create_route_guide(2) placer_enable_enhanced_router(3)

UIO-207 (error) %s option can be used only in conjunction with

%s option.

DESCRIPTION

None.

WHAT NEXT

Please refer to the man page of your original command.

UIO-208 (warning) Option '%s' is obsolete from 2007.03 release. This option will be ignored.

DESCRIPTION

None.

WHAT NEXT

Please refer to the man page of your original command.

UIO-210 (warning) Option %s is not supported by the %s command in DC Topographical mode. The option will be ignored.

DESCRIPTION

You received this message because the option you issued is not supported for the specified command when running dc_shell in Topographical mode.

WHAT NEXT

For a listing of supported command options, from within dc_shell execute man *command_name*. Then reexecute the command using supported options.

UIO-212 (warning) Ignoring retiming option.

DESCRIPTION

You receive this message if you specify **compile_ultra -retime** along with the **-top**, **-incremental**, or **-only_design_rule_fix** options. Retiming is not executed when these options are used and therefore the retiming parameter will be ignored.

WHAT NEXT

No action is required.

UIO-213 (Error) Some designs read from file %s are templates, and contain embedded scripts. To process these scripts, please use the "link" command after reading the file.

DESCRIPTION

This error indicates that the link command has to be run prior to execution of this command.

WHAT NEXT

run "link" command after reading the file.

SEE ALSO

UIO-214 (warning) Option ’-single_dir_option’ is not supported when the option ’-repartitioning_method’ is set as ’NONE’ or ’MULTI_DIRECTIONAL’. The option will be ignored.

DESCRIPTION

You received this message because the option you issued is not supported for the specified setting of option ’-repartitioning_method’ in ’set_optimize_dft_options’.

WHAT NEXT

Please refer to the man page of set_optimize_dft_options.

UIO-215 (warning) Cannot restore original license count of %d for feature %s.

DESCRIPTION

This warning message occurs when the tool encounters a problem checking out the required number of licenses for the parallel flow, and is unable to restore the same number of licenses that were held previously. This may be because there are an insufficient number of available licenses for the specified feature.

WHAT NEXT

Setting a lower level of parallelism with the **set_max_cores** command may reduce the number of licenses that are required.

SEE ALSO

compile_ultra(2)
set_max_cores(2)

UIO-250 (error) Invalid argument for the %s option. Valid arguments are %s .

DESCRIPTION

You receive this message because you issue a command with an invalid argument for the given opion.

WHAT NEXT

Reissue the command with one of the valid argments for the option.

UIP

UIP-1 (error) The module '%s' could not be found in the library '%s'.

DESCRIPTION

WHAT NEXT

UIP-2 (error) The design '%s' could not be found.

DESCRIPTION

WHAT NEXT

UIP-3 (error) The library '%s' could not be found.

DESCRIPTION

WHAT NEXT

UIP-4 (error) A design named '%s' has already been associated with module '%s'.

DESCRIPTION

WHAT NEXT

UIP-5 (warning) No designs in the library '%s' have been prebuilt

using the technology ’%s’.

DESCRIPTION

WHAT NEXT

UIP-6 (error) Could not build the synthetic design ’%s’.

DESCRIPTION

WHAT NEXT

UIP-7 (error) The library ’%s’ is not a valid synthetic library.

DESCRIPTION

WHAT NEXT

UIP-8 (error) The library ’%s’ is not a valid technology library.

DESCRIPTION

WHAT NEXT

UIP-9 (error) The cell ’%s’ cannot have its implementation set.

DESCRIPTION

WHAT NEXT

UIP-10 (error) The wire_load model ’%s’ could not be found in

library ’%s’.

DESCRIPTION

WHAT NEXT

UIP-11 (error) ’%s’ is not a valid argument for set_resource_allocation.
It should be one of ’none’, ’area_only’, or ’constraint_driven’.

DESCRIPTION

WHAT NEXT

UIP-12 (error) ’%s’ is not a valid argument for set_resource_implementation.
It shoule be either ’area_only’, or ’constraint_driven’.

DESCRIPTION

WHAT NEXT

UIP-101 (error) Cannot find "example" %s ’%s’.

DESCRIPTION

Command set_pad_type was invoked with the -example option, but the example pad indicated by the user does not exist in the target library. Therefore, the -example attribute was not set.

WHAT NEXT

Verify that the target library is the one intended. Check the validity of the search_path. Make sure the I/O pad cells were not marked as dont_touch or dont_use.

UIP-102 (error) Cannot find "exact" %s ’%s’

DESCRIPTION

Command set_pad_type was invoked with the -exact option, but the exact pad indicated by the user does not exist in the target library. Therefore, the -exact attribute was not set.

WHAT NEXT

Verify that the target library is the one intended. Check the validity of the search_path. Make sure the I/O pad cells were not marked as dont_touch or dont_use.

UIP-103 (error) "example" or "exact" cell ’%s’ is not an I/O pad.

DESCRIPTION

Command set_pad_type was invoked either with the -example or the -exact option, but the library cell indicated by the user is not an I/O pad. As a result, the -example (or -exact) attribute was not set.

Note that it in the case of Xilinx FPGA designs, it is illegal to use the Xilinx IOB as an example or exact candidate. This is because the IOB pads have all the pad attributes. So, using this device as an example or exact component is equivalent to asking for "all possible pads."

WHAT NEXT

Use command report_lib to have a list of library cells.

UIP-107 (error) No port ’%s’ in design.

DESCRIPTION

User tried to set I/O pads attributes on an element of the design that is not a port. Only ports can carry I/O pads requirements, which indicate the characteristics of the I/O pad to which the port should be connected.

WHAT NEXT

UIP-108 (error) Cannot set pad attributes on ’%s’.

DESCRIPTION

User invoked command set_pad_type on an object for which the pad-related attributes could not be set. Possible reasons for this include: inexistent object, don’t touch port, object that is not a port.

WHAT NEXT

UIP-109 (warning) Both "exact" and "example" options used. No attributes set.

DESCRIPTION

User invoked command set_pad_type with both the -exact and the -example options. Only one of the two can be set at a time, since specifying -exact indicates which I/O pad of the library HAS to be used. Using both options might involve conflicting requirements. Therefore, in that case, no attributes are set on the target port.

WHAT NEXT

UIPD-1 (error) Can’t open update file ’%s’.

DESCRIPTION

WHAT NEXT

UIPD-2 (error) Can’t write update output file ’%s’.

DESCRIPTION

WHAT NEXT

UIPD-3 (error) Output file has to be different than the script file ’%s’ being updated.

DESCRIPTION

WHAT NEXT

UIS_42 (warning) The value of variable ’gen_bus_%s_naming_style’

ends with the invalid ’%%’ (single percent sign).

DESCRIPTION

WHAT NEXT

UIS-1 (error) Create_schematic command is not available.

DESCRIPTION

WHAT NEXT

UIS-2 (error) Invalid output order.

DESCRIPTION

WHAT NEXT

UIS-3 (warning) Design ’%s’ isn’t mapped.

DESCRIPTION

WHAT NEXT

UIS-4 (error) Design ’%s’ could not be linked.

DESCRIPTION

This error is generated if the design could not be linked for highlighting the current design, but the highlight_path is invoked.

WHAT NEXT

Try to link the design by calling **link**, then reinvoke the **highlight_path**.

UIS-5 (error) Plot command is not available.

DESCRIPTION

WHAT NEXT

UIS-6 (error) Design %s has no schematic.

DESCRIPTION

WHAT NEXT

UIS-7 (error) Design Compiler is not enabled.

DESCRIPTION

You don’t have the Design-Compiler license available.

WHAT NEXT

Get the Design-Compiler license by invoke the **get_license Design-Compiler** command.

UIS-8 (error) Design ’%s’ could not be timed.

DESCRIPTION

WHAT NEXT

UIS-9 (error) Invalid pin list.

DESCRIPTION

WHAT NEXT

UIS-10 (error) No valid pins/ports specified.

DESCRIPTION

WHAT NEXT

UIS-11 (error) Bad sheet type ’%s’ specified.

DESCRIPTION

WHAT NEXT

UIS-12 (warning) Design ’%s’ has no cells!

DESCRIPTION

WHAT NEXT

UIS-13 (error) X Interface is not enabled.

DESCRIPTION

WHAT NEXT

UIS-14 (error) X has to be running to view a schematic.

DESCRIPTION

WHAT NEXT

UIS-15 (error) No minx device coordinate specified.

DESCRIPTION

WHAT NEXT

UIS-16 (error) No miny device coordinate specified.

DESCRIPTION

WHAT NEXT

UIS-17 (error) No maxx device coordinate specified.

DESCRIPTION

WHAT NEXT

UIS-18 (error) No maxy device coordinate specified.

DESCRIPTION

WHAT NEXT

UIS-19 (error) There is no sheet named ’%s’.

DESCRIPTION

WHAT NEXT

UIS-20 (error) No plot command is specified.

DESCRIPTION

WHAT NEXT

UIS-21 (error) The plot operation did not work. Is the plot_command variable set correctly?

DESCRIPTION

WHAT NEXT

UIS-22 (error) Invalid layer characteristic name.

DESCRIPTION

WHAT NEXT

UIS-23 (error) Wrong type value: ’%s’ for characteristic name: ’%s’.

Expecting an integer.

DESCRIPTION

WHAT NEXT

UIS-24 (error) Wrong type value: ’%s’ for characteristic name: ’%s’.
Expecting a floating point number.

DESCRIPTION

WHAT NEXT

UIS-25 (error) Wrong type value: ’%s’ for characteristic name: ’%s’.

Expecting ’true’ or ’false’.

DESCRIPTION

WHAT NEXT

UIS-26 (error) Generic schematic library not specified.

DESCRIPTION

WHAT NEXT

UIS-27 (error) Couldn’t read schematic library ’%s’.

DESCRIPTION

WHAT NEXT

UIS-28 (warning) Font library not specified.

DESCRIPTION

WHAT NEXT

UIS-29 (warning) Couldn’t read font library ’%s’.

DESCRIPTION

WHAT NEXT

UIS-30 (error) Can’t generate schematic - options are bad.

DESCRIPTION

WHAT NEXT

UIS-31 (error) Bad sheet fill ’%d’ specified.

DESCRIPTION

WHAT NEXT

UIS-32 (error) Couldn’t read generic symbol library ’%s’.

DESCRIPTION

WHAT NEXT

UIS-33 (warning) Couldn’t read symbol library ’%s’.

DESCRIPTION

WHAT NEXT

UIS-34 (error) ’gen_max_ports_on_symbol_side’ value must be positive.

DESCRIPTION

WHAT NEXT

UIS-35 (error) The -critical_path option must not be

specified if other options are specified.

DESCRIPTION

WHAT NEXT

UIS-36 (error) Either -critical_path or some ports and pins must be specified.

DESCRIPTION

WHAT NEXT

UIS-37 (error) No sheets were specified with the -sheet_list option.

DESCRIPTION

WHAT NEXT

UIS-38 (error) Couldn’t find a ripper for bussing in gen.

DESCRIPTION

WHAT NEXT

UIS-39 (warning) The value of variable ’gen_bus_%s_naming_style’

contains the invalid conversion string ’%%%c’.

DESCRIPTION

WHAT NEXT

UIS-40 (warning) The value of variable
’gen_bus_%s_naming_style’
contains no occurrences of ’%%%s’.

DESCRIPTION

WHAT NEXT

UIS-41 (warning) The value of variable
’gen_bus_%s_naming_style’
contains %d occurrences of ’%%%s’.

DESCRIPTION

WHAT NEXT

UIS-43 (warning) The value of variable ’%s’ isn’t valid--using

’%s’.

DESCRIPTION

WHAT NEXT

UIS-44 (warning) The variable ’%s’ isn’t defined--using ’%s’.

DESCRIPTION

WHAT NEXT

UIS-45 (warning) The order of ’%%d’ and ’%%s’ in the variable ’gen_bus_%s_naming_style’ is not correct.

DESCRIPTION

WHAT NEXT

UIS-46 (error) You cannot specify both the ’object_list’ and the ’object_type’ arguments.

DESCRIPTION

WHAT NEXT

UIS-47 (error) The ’%s’ argument must be a list of equations

(strings).

DESCRIPTION

WHAT NEXT

UIS-48 (warning) Schematic for proprietary design ’%s’ not generated.

DESCRIPTION

WHAT NEXT

UIS-49 (error) The format string must not have more than %d %%s specifications.

DESCRIPTION

WHAT NEXT

UIS-50 (error) The format string contains %d %%s specification(s),
but the value list has %d equation(s).

DESCRIPTION

WHAT NEXT

UIS-51 (error) Could not read either the generic symbol library: ’%s’,
or the default library: ’%s’.

Your software is probably installed incorrectly.

DESCRIPTION

WHAT NEXT

UIS-52 (warning) Could not read the specified generic symbol library: '%s'.

Had to read the default generic symbol library instead.
Your search_path is probably incorrect or pointing to
an older version of Synopsys software.

DESCRIPTION

WHAT NEXT

UIS-53 (error) Current design '%s' has no symbol view.

DESCRIPTION

This error is generated if there is no symbol view for the current design, but the **plot -symbol_view** is invoked.

WHAT NEXT

Create a symbol view for the current design by calling **create_schematic -symbol_view**, then reinvoke **plot -symbol_view**.

UIS-54 (error) Target system does not allow mixed bus ports.

DESCRIPTION

WHAT NEXT

UIS-55 (error) Target system does not allow compound names.

DESCRIPTION

WHAT NEXT

UIS-56 (error) Target system does not allow rippers.

DESCRIPTION

WHAT NEXT

UIS-57 (error) Unknown target system specified for schematics.

DESCRIPTION

WHAT NEXT

UIS-58 (error) More than one bussing style specified: using

default.

DESCRIPTION

WHAT NEXT

UIS-59 (warning) Net ’%s’ has no drivers.

DESCRIPTION

WHAT NEXT

UIS-60 (warning) Cell ’%s’ has no output or bidirect pins.

DESCRIPTION

WHAT NEXT

UIS-61 (error) You cannot use ’%s’ to highlight schematics.

DESCRIPTION

When using the highlight_path command, you must specify a layer_name that is NOT one of the built-in layer names. For instance, you cannot use the "cell_layer" to highlight schematics.

WHAT NEXT

Typically, you don’t need to specify a layer_name with the highlight_path command, it will choose a layer_name for you.

UIS-62 (error) current_highlight_layer is only defined if the

current_design is defined.

DESCRIPTION

The current_highlight_layer is a derived variable which depends on the current_design. If the current_design is not defined, then you cannot get or set the current_highlight_layer variable.

WHAT NEXT

Set the current_design before using the current_highlight_layer variable.

UIS-63 (error) There is no layer named "%s

DESCRIPTION

WHAT NEXT

UIS-64 (error) Highlight layer name "%s It should be of the form "highlight_layerN is a positive integer.

DESCRIPTION

The current_highlight_layer variable must be of the form "highlight_layerN", where N is a positive integer.

WHAT NEXT

When setting the current_highlight_layer, you must use a name of the form "highlight_layerN

UISN

UISN-1 (error) No valid synthetic library specified.

DESCRIPTION

WHAT NEXT

UISN-2 (error) Module '%s' not found.

DESCRIPTION

WHAT NEXT

UISN-3 (error) Verification implementation not found for module '%s'.

DESCRIPTION

WHAT NEXT

UISN-4 (warning) Implementation '%s' not found.

DESCRIPTION

WHAT NEXT

UISN-5 (error) No default check_parameters for module '%s'.

DESCRIPTION

You receive this error message because you have executed the **check_implementations** command, but no **check_parameters** attribute exists in the module group in your

synthetic library source file.

If you want to use default parameters, the module group in your synthetic library source file must contain a **check_parameters** attribute.

WHAT NEXT

Reexecute the **check_implementations** command and specify the **-parameters** option.

SEE ALSO

check_implementations (2).

UISN-6 (warning) Binding '%s' not found.

DESCRIPTION

WHAT NEXT

UISN-7 (error) Parameters may only be specified if all specified bindings

are for a single operator.

DESCRIPTION

WHAT NEXT

UISN-8 (error) No %s for operator ’%s’.

DESCRIPTION

WHAT NEXT

UISN-9 (error) Invalid parameter "%s

DESCRIPTION

WHAT NEXT

UISN-10 (error) Wrong number of pin_widths specified in ’%s’ for operator ’%s’.

DESCRIPTION

You must specify a pin width for each pin of the given operator. You have specified either too few or too many pins.

WHAT NEXT

UISN-11 (error) No such pin ’%s’ in pin_width ’%s’ for operator ’%s’.

DESCRIPTION

The pin you have specified is not on the operator. Be careful, pin names are case

sensitive.

WHAT NEXT

UISN-12 (error) Pin '%s' in pin_width '%s' for operator '%s' specified twice.

DESCRIPTION

The pin you have specified the given pin twice. In the process, you have omitted some other pin.

WHAT NEXT

UISN-13 (error) At least one option (-priority or -set_id) must be specified.

DESCRIPTION

You receive this error message because you executed the **set_impl_priority** command without specifying the **-priority** or **-set_id** option. You must specify either one or both of these options.

WHAT NEXT

Reexecute the **set_impl_priority** command and specify the **-priority** option, the **-set_id** option, or both.

SEE ALSO

set_impl_priority (2).

UISN-14 (error) set_id cannot be negative.

DESCRIPTION

WHAT NEXT

UISN-15 (error) You can set priority of implementations only.

DESCRIPTION

WHAT NEXT

UISN-16 (error) Environment variable '%s' is an unsupported type.

DESCRIPTION

Only environment variables of types integer, float, string, and list can be retrieved for synthetic library parts. The environment variable requested has a value whose type is not supported.

WHAT NEXT

Check to see that the correct environment variable name has been used. Check to see that the environment variable is set to the expected value.

UISN-17 (warning) Unable to access read cache directory '%s'. It will be ignored.

DESCRIPTION

One of the directory paths on the cache_read list was invalid or couldn't be read.

WHAT NEXT

Check the value of the cache_read environment variable and make sure that all cache filenames are correct.

UISN-18 (warning) Unrecognized key '%s' found in 'synlib_dont_get_license' variable.

DESCRIPTION

The key may either be typoed or not in the key file.

WHAT NEXT

UISN-19 (warning) Library '%s' in 'synlib_preferred_library' variable is not in the synthetic library list.
This library is deleted from the preferred library list.

DESCRIPTION

You receive this warning message because one of the specified names in the preferred library list is not in the synthetic library list.

WHAT NEXT

Reexecute the **synlib_preferred_library** variable and specify a library that is in the synthetic library list.

SEE ALSO

synlib_preferred_library (3).

UISN-20 (error) The dynamic module '%s' does not exist in the dynamic synthetic library.

DESCRIPTION

This error message is issued by the **report_dynamic_synlib** command. The dynamic module is created for HDL 'preserved_function'. You might have specified a nonexistent dynamic module in the module list.

WHAT NEXT

Provide a correct name with each module in the module list. If you are not sure

about module names, do not specify a module list.

UISN-21 (warning) The module '%s' is not a dynamic synthetic module. It is ignored.

DESCRIPTION

You receive this warning message because you have executed the **report_dynamic_synlib** command and specified a module in the module list that is not a dynamic synthetic module. Modules specified in the module list must be dynamic synthetic modules that are created for HDL 'preserved_function'. The nondynamic module is ignored while the rest of the list is reported.

WHAT NEXT

Verify that each module in the module list is a dynamic module. If you are not sure about dynamic module names, do not specify a module list. If you want to report on nondynamic modules, use the **report_synlib** command instead.

SEE ALSO

report_synlib (2).

UISN-22 (error) Unacceptable list of modules for dynamic synthetic library.

DESCRIPTION

This message is issued by the **report_dynamic_synlia** command. You might have specified an empty or a corrupted module list. This error usually is caused by a typo.

WHAT NEXT

Provide a correct name with each module in the module list. If you are not sure about the dynamic module names, do not specify a module list.

UISN-23 (error) Unknown synthetic library check '%s'.

Valid checks are '%s'.

DESCRIPTION

You receive this error message because you executed the **check_synlib** command with the **-group** option, but did not specify a valid group name. This command accepts an optional **-group list** argument that enumerates sets of checks. If you used this option, you might have included an invalid group name in the list of group names you specified. The following example will initiate all standard checks upon the current set of synthetic libraries:

```
dc_shell> check_synlib -group { "all" }
```

WHAT NEXT

Specify a list of valid checks for the *-group* option. If you are unsure about what checks to specify, use **all**, or remove the group argument from the **check_synlib** command.

SEE ALSO

check_synlib (2).

UISN-24 (warning) Skipping check of implementation '%s' for module '%s'.

DESCRIPTION

The **check_implementations** command ignores checks in which the verification implementations checks against itself. If a **check_implementations** command specifies a list of implementations and the list contains the verification implementation, this warning is issued and only non-verficication implementations are checked.

For example, the module "MyMod" contains two implementations, "Romulus" and "Remus". A check_implementation group flags the implementation "Romulus" to be the golden implementation for module "MyMod". The command **check_implementations -impl { Romulus Remus } MyMod** generates a warning for implementation "Romulus". The command, however, continues and verifies "Romulus" against "Remus".

WHAT NEXT

Remove any verification implementations specified in the **check_implementations** command. To learn what implememententations within a module are the verification implementation, use the **report_synlib** command.

UISN-25 (warning) No implementations to check for module '%s'.

DESCRIPTION

You receive this warning message because the **check_implementations** command found no implementations to check for the specified module. The **check_implementations** command will not verify an implementation marked as the verification implementation. You will also receive this warning message when an empty implementation list is specified for the **-implementations** option.

WHAT NEXT

For more information, see the *DesignWare Reference Manual* and the **check_implementations** manual page.

SEE ALSO

check_implementations (2).

UISN-26 (warning) The following synthetic libraries should be added to
the list of link libraries:
'%s'.

DESCRIPTION

You receive this warning message because you have executed the **synthetic_library** variable and have specified a library that was not specified with the **link_library** variable. All synthetic libraries specified with the **synthetic_library** variable must also be specified with the **link_library** variable.

For example, if the **synthetic_library** variable specified my_synlib.sldb, then the **link_library** variable should also specify my_synlib.sldb as shown below.

target_library = my_techlib.db synthetic_library = my_synlib.sldb link_library = {my_techlib.db my_synlib.sldb}

WHAT NEXT

See the *DesignWare User Guide* for more information.

SEE ALSO

link_library (3), **synthetic_library** (3).

UISN-27 (information) Evaluating DesignWare library utilization.

DESCRIPTION

This informational message indicates that libraries are being evaluated to determine whether or not synthetic libraries are available for use within a design. Although a library may be marked as available, the implementations contained within that library may or may not be used. Availability in the context of this message means that implementations within the library are candiates for use within the design.

In order for a synthetic library to be available, the following conditions must be satisfied:

-The .sldb file of the synthetic library must be specified using the **synthetic_library** list variable.

-The synthetic library must contain one or more implementations.

-Valid licenses for one or more licensed implementations within the synthetic library must be available for use. Alternatively, one or more single unlicensed implementations may be found within the synthetic library.

Note that, although a synthetic library may be marked as available for use, a case may exist where no implementations defined within the synthetic libary will be used. This occurs when the design hierarchy contains no synthetic parts, either inferred or instantiated. This may also be the by-product of module and implementation selection. An available synthetic library may contain implementations which are considered during an exploration phase of synthesis, but are not chosen to implement the final design.

WHAT NEXT

For more information, see the *DesignWare User Guide* and the *DesignWare Developer Guide*.

UISN-28 (error) %s key is required to enable this feature.

DESCRIPTION

This error message occurs when you attempt to use a feature for which you do not have a DC Ultra license and a DesignWare license.

WHAT NEXT

Contact the Synopsys Customer Support Center by sending an email message to support_center@synopsys.com.

UISN-30 (warning) Unrecognized key '%s' found in set_synlib_dont_get_license command.

DESCRIPTION

You receive this warning message when you execute the **set_synlib_dont_get_license** command and specify a key name that either contains a typo or is not listed in the key file.

WHAT NEXT

Verify that there is not a typo in the specified key name and that the key name is listed in the key file.

SEE ALSO

set_synlib_dont_get_license (2).

UISN-32 (information) new key '%s' is added to the '%s' list.

DESCRIPTION

At least one of the keys in the list is an old synlib license key. The old keys will be replaced with the new key. So the new key is added to the list.

The old synlib license keys are: "DesignWare-Foundation", "SynLib-ALU", "SynLib-AdvMath", "SynLib-Control", "SynLib-FltTol", "SynLib-Seq"

WHAT NEXT

The new key file will no longer contain some of the old keys. If there is error message says that the key is unrecognized key, remove it from the list.

UISN-33 (warning) Mixing UDPE & native MC generators is not

supported in the current release.

DESCRIPTION

UDPE datapath generators provide an alternative implementation for MC operators.

If this warning message is printed, UDPE generator usage will be turned off. Only default MC generators will be used.

WHAT NEXT

If you turn on any UDPE generator, turn on all of them.

UISN-34 (warning) license for feature '%s' has already been checked out. 'set_synlib_dont_get_license' on this license is ignored.

DESCRIPTION

You receive this warning message when you execute the **set_synlib_dont_get_license** command and specify a key name that has already been checked out. Or, you defined the list variable synlib_dont_get_license and added the name of a feature that has been checked out to the list.

WHAT NEXT

If you do not want the feature to be used, please remove the license from current process using remove_license command.

SEE ALSO

set_synlib_dont_get_license (2). **remove_license** (2). **synlib_dont_get_license** (3).

UISN-35 (warning) The target library doesn't have a usable full adder cell. Datapath QOR could be degraded.

DESCRIPTION

If the target library doesn't have a full adder cell, or if all full adder cells are marked as "dont_use", QOR of datapath blocks could be degraded.

WHAT NEXT

To prevent this warning message, use a target library with full adder cells.

UISN-36 (warning) The synthetic libraries in the synthetic_library list are from different versions.

DESCRIPTION

The synthetic libraries in the synthetic_library do not have the same version. You may have used the synthetic libraries from different directories.

WHAT NEXT

Make sure the synthetic libraries are from the same root.

UISN-38 (warning) The datapath optimization feature does not currently support the DPCM delay model. This feature is turned off (by setting the hlo_disable_datapath_optimization variable to true) for this command and subsequent commands.

DESCRIPTION

This warning message occurs because the datapath optimization flow does not support the DPCM delay model. If the DPCM delay model is used in the compile flow, then the **hlo_disable_datapath_optimization** variable is switched to true.

WHAT NEXT

This is a warning message only. No action is required.

However, the **hlo_disable_datapath_optimization** variable is switched to true. If you want to enable the datapath optimization flow, set the **dpcm_libraries** variable to an empty set, and reset the **hlo_disable_datapath_optimization** variable to false.

SEE ALSO

dpcm_libraries(3)
hlo_disable_datapath_optimization(3)

UISN-40 (Warning) DesignWare synthetic library dw_foundation.sldb is added to the synthetic_library in the current command.

DESCRIPTION

You are using the ultra optimization synthesis flow, but the DesignWare synthetic library is not listed in synthetic_library. This could result in sub-optimal synthesis quality.

For compile_ultra command, dw_foundation.sldb is automatically added to the synthetic_library in the current command. For set_ultra_optimization, if you do not specify the '-no_auto_dwlib' option, dw_foundation.sldb is automatically added to the synthetic_library in the subsequent compile command. Until you set set_ultra_optimization to be false or use '-no_auto_dwlib' option in the set_ultra_optimization command.

You get this message because the dw_foundation.sldb is automatically added to the synthetic_library in the current compile command.

WHAT NEXT

Add DesignWare synthetic library to your synthetic_library and link_library list.

SEE ALSO

set_ultra_optimization(2), compile_ultra(2)

UISN-41 (warning) The 'mc inside dc' datapath flow is obsolete in this release.

DESCRIPTION

The 'mc inside dc' datapath optimization flow has been obsoleted in this release. These datapath generators are now directly integrated into DC for better performance and reliability.

To use the new integrated datapath optimization flow, leave the variable **synlib_enable_dpgen** set at its default value. To use the old 'mc inside dc' flow, set **synlib_enable_dpgen** to false.

WHAT NEXT

Select the desired datapath optimization flow.

SEE ALSO

synlib_enable_dpgen(3).

UISN-42 (warning) Datapath smart generation must be set to true to use smart generation options.

DESCRIPTION

The values of the various datapath smart generation options have no meaning unless datapath smart generation is enabled.

To enable datapath smart generation, the variables **synlib_enable_dpgen** and **synlib_dwgen_smart_generation** must both be set to true.

WHAT NEXT

Select the desired datapath generation flow.

SEE ALSO

synlib_enable_dpgen(3), synlib_dwgen_smart_generation(3).

UISN-43 (warning) Unknown datapath smart generation option '%s'

DESCRIPTION

Datapath smart generation option take one of three values: **auto, true,** and **false.** The value given was not understood.

Unknown datapath smart generation option values are treated as **false;** meaning that the smart generation option is turned off.

WHAT NEXT

Select the correct datapath smart generation option value.

SEE ALSO

synlib_dwgen_smart_generation(3).

UISN-44 (Warning) Failed to read dw_foundation.sldb for the compile command.

DESCRIPTION

Compile ultra flow tried to read dw_foundation.sldb but failed to do so.

You are using the ultra optimization synthesis flow, but the DesignWare synthetic library is not listed in synthetic_library list. This could result in sub-optimal synthesis quality.

For compile_ultra command, dw_foundation.sldb is automatically added to the synthetic_library in the current command. For set_ultra_optimization, if you do not specify the '-no_auto_dwlib' option, then dw_foundation.sldb is automatically added to the synthetic_library in the subsequent compile command. Until you set set_ultra_optimization to be false or use '-no_auto_dwlib' option in the set_ultra_optimization command.

You get this message because the compile command tried to read the dw_foundation.sldb library but failed to do so.

WHAT NEXT

Add DesignWare synthetic library to your synthetic_library and link_library list and make sure the dw_foundation.sldb is in the search_path.

SEE ALSO

set_ultra_optimization(2), compile_ultra(2)

UISN-45 (Warning) Invalid dw naming style %s, the default naming style is used.

DESCRIPTION

The synlib_design_naming_style is set to an invalid value. The default value '%s_%s_%d' is used.

The variable must contain one or two %s, and one %d: If there is one %s, the naming style is <dw_component_name>_<index>; If there are two %s, the naming style is <parent_design_name>_<dw_component_name>_<index>;

If the variable contains less than one %s or more than two %s, or more than one %d, the default naming style will be followed. This variable will be ignored.

The naming style must end with %d, all %s must be in front of the %d.

WHAT NEXT

Set the synlib_design_naming_style variable to a valid naming style

SEE ALSO

UISN-46 (Warning) ’synlib_design_name_length’ is ignored for %s in %s.

DESCRIPTION

You have set the ’synlib_design_name_length’ to a value that is smaller than the required value. The dw name length limit is ignored.

There is a minimum length requirement for the dw design names: The minimum length is dw_component_name+user_characters+5. The 5 chars are used for for "<index>". If the limit set by ’synlib_design_name_length’ is smaller than the minimum length, the limit is ignored.

If there is one %s in the synlib_design_naming_style, the naming style is <dw_component_name>_<index>. In this case, if the dw name length exceeds the limit, the limit is ignored.

If there are two %s, the naming style is <parent_design_name>_<dw_component_name>_<index>. If the dw name length exceeds the limit, the parent_design_name will be cut short to meet the limit when the difference is shorter than the length of the parent_design_name. If the difference between the limit and the actural name is bigger than the length of the parent_design_name, the limit will be ignored.

WHAT NEXT

Change your ’synlib_design_naming_style’ setting or set the ’synlib_design_name_length" to a value that is bigger than the required length.

SEE ALSO

UISN-47 (Warning) The dw_prefer_mc_inside feature is obsolete.

DESCRIPTION

You set ’dw_prefer_mc_inside’ to be true. The dw_prefer_mc_inside is now obsolete. The dw_prefer_mc_inside feature is replaced by ’synlib_enable_dpgen’ feature. The

'dw_prefer_mc_inside' variable is removed.

If you specified dw_prefer_mc_inside to be true and synlib_enable_dpgen to be false, the synlib_enable_dpgen variable will be switched to true to enable the generator flow.

WHAT NEXT

This is a warning message only. No action is required.

SEE ALSO

synlib_enable_dpgen(3).

UISN-48 (Warning) The dw_prefer_mc_inside feature is replaced by the synlib_enable_dpgen feature. Setting 'synlib_enable_dpgen' to 'true'.

DESCRIPTION

You set 'dw_prefer_mc_inside' to be true; and set 'synlib_enable_dpgen' to be false. The dw_prefer_mc_inside feature is now obsolete and replaced by the synlib_enable_dpgen feature.

The 'dw_prefer_mc_inside' variable is removed. The 'synlib_enable_dpgen' variable is set to true.

WHAT NEXT

This is a warning message only. No action is required.

SEE ALSO

synlib_enable_dpgen(3).

UISN-49 (error) The internal rounding value should be equal or smaller than the external rounding value.

DESCRIPTION

You set internal rounding value to be bigger than the external rounding value. This will cause error in the generated netlist.

WHAT NEXT

Set the internal rounding value to be equal or smaller than the external rounding value.

SEE ALSO

set_dp_int_round(2).

UISN-50 (error) Internal rounding can not be set on %s.

DESCRIPTION

Internal rounding position can only be set on nets that are directly driven by the supported DesignWare cells. You try to set the internal rounding position on a net that is not driven by a supported DW cell.

The supported DesignWare cells are: Cells that infer DesignWare operator MULT_UNS_OP and MULT_TC_OP. Cells that instantiate the following DesignWare components: DW02_mult, DW_mult_uns, DW_mult_tc, DW_square, DW02_prod_sum, DW02_prod_sum1, DW_prod_sum_uns, DW_prod_sum_tc, DW02_mac, DW_mac_tc, DW_mac_uns.

WHAT NEXT

Only set internal rounding position on nets that are driven by supported DW cells.

SEE ALSO

set_dp_int_round(2).

UISN-51 (Warning) Internal rounding can not be performed on cell '%s' with forced static implementation '%s/%s'.

DESCRIPTION

You set dp internal rounding position on a DW OP cell. But also set the module and implementation of the cell. The internal rounding feature on a DW OP cell is not supported on cells with forced module and implementation.

WHAT NEXT

If you want to get better QoR by using the internal rounding feature, please remove the implementation set on the cell.

SEE ALSO

set_dp_int_round(2), remove_attribute(2).

UISN-52 (error) The internal rounding value should be equal or smaller than the bitwidth of net bus '%s'.

DESCRIPTION

You set internal rounding value to be bigger than the width of the net. The internal rounding value is invalid.

WHAT NEXT

Set the internal rounding value to be equal or smaller than the width of the nets.

SEE ALSO

set_dp_int_round(2).

will be obsoleted in the 08.09 release. You should use the super set dw_foundation.sldb synthetic library instead. (UISN-53)

UISN-53 (Warning) The DesignWare libraries '%s' will be obsoleted in the 08.09 release. You should use the super set dw_foundation.sldb synthetic library instead.

DESCRIPTION

You put the obsolete synthetic libraries in the synthetic_library list. The following synthetic libraries will be obsoleted in the 08.09 release: dw01.sldb, dw02.sldb, dw03.sldb, dw04.sldb, dw05.sldb, dw06.sldb, dw07.sldb, dw08.sldb. You should use the super set dw_foundation.sldb synthetic library instead.

WHAT NEXT

Replace the absolete synthetic libraries with dw_foundation.sldb in the synthetic library list.

UISN-55 (error) The low power synthetic library

dw_minpower.sldb is only supported in compile_ultra flow.

DESCRIPTION

This error message occurs when you add the low power synthetic library dw_minpower.sldb in the synthetic_library list. The low power DesignWare feature is only supported in the **compile_ultra** flow.

WHAT NEXT

If you intend to use the low power DesignWare feature, you must use the **compile_ultra** command. If you intend to use the compile expert flow, remove dw_minpower.sldb from the synthetic_library list.

SEE ALSO

compile_ultra(2)

UISN-56 (error) The DesignWare-LP license is not available.

DESCRIPTION

This error message occurs when you the DesignWare low power feature by adding the low power synthetic library dw_minpower.sldb in the synthetic_library or link_library list, but you do not have a DesignWare-LP license.

WHAT NEXT

If you intend to use the low power DesignWare feature, make sure you have the DesignWare-LP license. Otherwise, turn off the DesignWare low power feature by removing dw_minpower.sldb from the synthetic_library or link_library list.

UISN-57 (Warning) Your design does not have power constraint.

DESCRIPTION

You added the dw_minpower.sldb in your synthetic_library or link_library list. But you do not set power constraint on the design. You will get sub-optimial power QoR result.

WHAT NEXT

If you intend to use the low power DesignWare feature, make sure you set power constraint on the design, or enable datapath gating feature.

SEE ALSO

power_enable_datapath_gating (3), **set_max_leakage_power** (2), **set_max_dynamic_power** (2).

UISN-58 (Error) You do not have dw_minpower.sldb in your synthetic_library list.

DESCRIPTION

You set power_enable_datapath_gating to true. This feature require DW minPower components. You need to add dw_minpower.sldb in your synthetic_library or link_library list.

WHAT NEXT

Add dw_minpower.sldb in your synthetic_library or link_library list.

SEE ALSO

power_enable_datapath_gating (3),

UIT-2 (warning) Unrecognized compaction mode ignored.

DESCRIPTION

You receive this message because you have entered an incorrect value for the **-compaction_effort** option. Valid values for this option are *low*, *medium*, or *high*. Or, you can use the **-no_compaction** option.

The **create_test_patterns** command will continue to run with a default value of *low*.

WHAT NEXT

If you are willing to accept the results of low effort compaction, no action is required on your part. However, using low effort compaction typically results in a higher vector count than is a result of using medium or high effort compaction.

If you want to use **-compaction_effort medium** or **-compaction_effort high**, rerun the **create_test_patterns** command with the appropriate option.

SEE ALSO

create_test_patterns (2).

UIT-3 (error) Unrecognized test program format or missing license key.

DESCRIPTION

You receive this message if **write_test** does not recognize the format you specified with **write_test -format**, or if you do not have a required license key. **write_test** recognizes only formats that are contained in the variable **write_test_formats**; by default, **write_test_formats** contains the formats *synopsys*, *tds*, *wgl*, *verilog*, and *vhdl*. If you want to use a different format (for example, tdl91), you must enter it into **write_test_formats** so that **write_test** will recognize it. In addition, the tdl91 format requires a CTV key.

WHAT NEXT

If you receive this message, do the following:

1. Within **dc_shell**, list the **write_test_formats** variable to see whether it contains the format you want to use.

```
    dc_shell> list write_test_formats
    write_test_formats = {"synopsys", "tssi_ascii", "tds", "verilog", "vhdl", "wgl"}
```

2. If the required format (for example, tdl91) is not contained in the variable **write_test_formats**, add it, as follows.

```
    dc_shell> write_test_formats = write_test_formats + tdl91
```

3. Ensure that you have the correct key (in this case, the CTV key).

4. Re-issue the **write_test** command and specify the required format.

```
    dc_shell> write_test -format tdl91
```

SEE ALSO

write_test (2); **write_test_formats** (3).

UIT-4 (warning) You have asked for scan replacement, but attributes show that the design already has scan circuitry. Your request is ignored.

DESCRIPTION

This message tells you that you have asked DFT Compiler to replace non-scan cells with scan cells. Design attributes tell DFT Compiler that this process has already occurred. Your request is ignored.

WHAT NEXT

To eliminate the warning, change command options so that you do not ask scan insertion to do scan replacement.

UIT-5 (warning) No existing test circuitry to route, scan will be inserted.

DESCRIPTION

You receive this message if you run **insert_scan** on a design with scan replacement disabled and scan routing enabled, but where attributes on the design show that the design is not scan replaced. For example, you receive this mesasge if you enter the following sequence of commands:

1. **read rtl.v -format verilog**.

2. **compile**.

3. **set_scan_configuration -replace false -route true**.

4. **insert_scan**.

The message informs you that **insert_scan** is overriding your specification to not scan replace the design since **insert_scan** cannot route a design that is not scan replaced.

You receive this message if you read in a design from an ASCII format (Verilog, VHDL, or EDIF) that you have compiled with test-ready compile (**compile -scan**) and have run **insert_scan** with scan replacement disabled and scan routing enabled. Follwing is another example of a command sequence that will result in the return of this error message:

1. **read rtl.v -format verilog**

2. **current_design = top**

3. **compile -scan**

4. **write -hierarchy -format verilog -out design_tr.v**

5. **remove_design -designs**

6. **read -format verilog design_tr.v**

7. **current_design = top**

8. **set_scan_configuration -replace false -route true**

9. **insert_scan**

After invoking **insert_scan**, you receive the following message:

Warning: No existing test circuitry to route, scan will be inserted. Loading desing 'top' Using test design rule information from previous check_test run Architecting Scan Chains Inserting Scan Cells Routing Global Signals Mapping New Logic Transferring design 'top' to database 'top.db'

This is an invalid flow. You should only save and read the test-ready designs from db format. The scan configuration is correct for a test-ready design that you have saved in db format because the db format includes attributes to indicate to the **insert_scan** command that the design is scan replaced. However, these attributes are missing from the ASCII format.

WHAT NEXT

Correct your script to avoid running the **insert_scan** command with replacement disabled but routing enabled on a design that does not contain the attributes to indicate that the design is scan replaced.

If you intended to perform scan replacement on the design, no action is required on

your part and you can use the resulting design.

If your design was already scan replaced but did not have the necessary attributes, the **insert_scan** command has built valid scan chains (verify this with **check_test**). However, this is not an optimum flow for your design and your design may not be optimum for area and timing. If your design does not meet your area and timing constraints, correct your compile scripts to save the test-ready design in db format and rerun both compilation and scan insertion.

UIT-6 (error) Cannot load test vector database file.

DESCRIPTION

The test vector database file cannot be loaded, because of one or more of these errors:

wrong search path for the file
nonexistent test vector database file
misspelled test vector database filename
the file is write-protected
the file has wrong permissions set
the file contains no vectors

WHAT NEXT

Make sure that the file exists, has the correct search path, correct spelling, appropriate permissions, and contains test vectors.

UIT-8 (warning) Design has no scan path. Generated vectors will not be saved.

DESCRIPTION

You receive this message when attributes indicate that a design has no scan chain and the scan style is not set to combinational.

Under these circumstances, DFT Compiler performs a "what if" analysis to predict the coverage if you were to insert scan chains. Without scan chains, the vectors that are generated are meaningless and are not saved.

WHAT NEXT

If you wish only to check the coverage that DFT Compiler can achieve and do not wish to save the vectors, no action is required on your part. However, you can check what the achievable coverage is more quickly by using the **-dft** option of

create_test_patterns.

If your design has an existing scan path, establish attributes that indicate to DFT Compiler that the scan chain exists. To do this, annotate test ports using **set_signal_type**. Then declare the existing scan using the command **set_scan_configuration -existing_scan true** and run **check_test**. For example, for a circuit with an existing multiplexed flip-flop style scan chain and test ports TEST_SI_PORT, TEST_SE_PORT, and TEST_SO_PORT, do the following:

1. Issue the command **set_signal_type test_scan_in TEST_SI_PORT**.

2. Issue the command **set_signal_type test_scan_enable TEST_SE_PORT**.

3. Issue the command **set_signal_type test_scan_out TEST_SO_PORT**.

4. Issue the command **set_scan_configuration -style multiplexed_flip_flop**.

5. Issue the command **set_scan_onfiguration -existing_scan true**.

6. Run **check_test**.

7. Run **create_test_patterns**.

If you have a combinational design and wish to save the ATPG vectors, you must set the combinational scan style using the **set_scan_configuration -style combinational** command.

check_test (2), **create_test_patterns** (2), **set_scan_configuration** (2), **set_signal_type** (2).

UIT-9 (error) Test clock period of %.2f on port '%s' is inconsistent with period of %.2f specified in the test protocol.

DESCRIPTION

The test clock period on the port is inconsistent with the period you have specified in the test protocol.

WHAT NEXT

Check that your test clock period specification is consistent with your test protocol.

UIT-10 (error) internal failure, write_test vector formatter (stran)

failed.

DESCRIPTION

Attempt to format vector failed. This may be caused by improperly installed formatter executable, bin_path which points to the formatter is improperly specified, corrupted formatter executable, formatter executable has been tampered with, not enough disc space to write vectors, formatter run time execution error etc.

WHAT NEXT

Make sure that the formatter executable is properly installed, that your bin_path is properly set, and that there is sufficient disc space to generate vectors.

UIT-11 (error) internal failure, write_test vector formatter (stran) failed. (%d).

DESCRIPTION

Vector formatting process was abruptly terminated. Possible causes are: 1. Not enough disc space to continue writing vectors. 2. Formatter executable was accidentally deleted by another process. 3. Does not have write permission to either write to the directory, or to overwrite an existing vector file. 4. Temporary network problems.

WHAT NEXT

Make sure that sufficient disc space is available when generating vectors, all the right permissions are set, then reinvoke write_test.

UIT-13 (Information) The variable atpg_test_asynchronous_pins is obsolete. It has no effect.

DESCRIPTION

In release 1999.10, the variable atpg_test_asynchronous_pins was made obsolete. The create_test_pattern command now always generates tests for faults on asynchronous pins.

WHAT NEXT

No action required.

UIT-14 (error) internal error, key error for write_test formatter (stran).

DESCRIPTION

Intermediate (SIF) file used as input to the formatter executable contained illegal key. The intermediate file may be corrupted or have been manually tampered with.

WHAT NEXT

Reinvoke write_test command

UIT-15 (error) internal error, write_test formatter (stran) can not generate ’%s’ format.

DESCRIPTION

Unsupported test vector format indicated in the intermediate (SIF) input file for the write_test formatter executable. The file may be corrupted or may have been manually tampered with.

WHAT NEXT

Reinvoke write_test command

UIT-16 (error) No scan chains extracted for design - patterns cannot be formatted.

DESCRIPTION

Formatting scan test patterns into a set of manufacturing test vectors requires information about the scan chains within the design. This information includes the cells in each chain, the order in which they are connected, and scan chain inversions.

DFT Compiler automatically extracts scan chain information from a design when the

check_test or **create_test_patterns** commands are executed. Execution of these two commands stores a copy of the design in **db** format in memory. If the design is saved in **db** format, scan chain information is saved with the design.

If the design is not saved in **db** format, the scan chain information is not available and the **write_test** command in unable to format the patterns. Typically this happens when a design is read in as a netlist and an existing pattern database file is used as input to the **write_test** command.

WHAT NEXT

Run the **check_test** command to automatically extract the details of the design scan chains; use the **report_test -scan** command to verify that this information has been extracted. The extracted scan chain information is used by the **write_test** command to format test patterns.

UIT-19 (error) No test protocol exists for design '%s'.

DESCRIPTION

A test protocol is required for the successful completion of the current command. But no test protocol was found for the specified design.

WHAT NEXT

Install a test protocol.

Test protocols can be user-specified or automatically inferred. To specify a test protocol, use the commands read_test_protocol or read_init_protocol. To make DFT Compiler infer a test protocol, use the command check_test.

UIT-20 (error) Cannot open output test protocol file '%s'.

DESCRIPTION

You receive this message if you execute the **write_test_protocol** command and did not succeed.

WHAT NEXT

Check if the destination directory has write permission.

UIT-21 (warning) Unrecognized backtrack effort '%s' ignored.

DESCRIPTION

You receive this message when you have entered an incorrect value for the **-backtrack_effort** option of **create_test_patterns**. Valid values for this option are *low*, *medium*, and *high*.

The **create_test_patterns** command will continue to run with a default value of *low*.

WHAT NEXT

If you are willing to accept the results of low backtrack effort, no action is required on your part. However, some circuits running **create_test_patterns** with a low backtrack effort may encounter aborted faults when **create_test_patterns** is unable to generate patterns without exceeding the backtrack limit.

If the results of **create_test_patterns** do not meet your fault coverage requirements and there are many aborted faults, re-execute **create_test_patterns** with a backtrack effort of *medium* or *high*.

SEE ALSO

create_test_patterns (2).

UIT-22 (warning) Only %d%% of faults were considered in ATPG run.

DESCRIPTION

You receive this message if you use **restore_test** or **write_test** on a vdb file generated by **create_test_patterns -sample**.

This message reminds you that the vectors were generated only for a sample of faults in the design.

WHAT NEXT

If you wish to generate vectors for all faults, you need to either regenerate the vectors from scratch using **create_test_patterns**, or use the same vdb file again as a starting point for ATPG by using the **-input** option of **create_test_patterns**.

UIT-23 (error) No test protocol defined for design - patterns

cannot be formatted.

DESCRIPTION

Formatting scan test patterns into a set of manufacturing test vectors is controlled by the test protocol defined for a design. The protocol specifies the steps of the scan test sequence (scan-in, parallel measure/capture, and scan-out).

The **check_test** and **create_test_patterns** commands automatically infers a default protocol for a design. If the design is stored in **db** format, this protocol is saved with the design. Custom protocols may be necessary for designs that require preconditioning vectors or designs that employ nonstandard scan test sequences. A custom protocol can be defined for a design and specified using the **read_test_protocol** command.

In this case, this information is not available, and the **write_test** command in unable to format the patterns. Typically this happens when a design is read in as a netlist and an existing pattern database file is used as input to the **write_test** command.

WHAT NEXT

Run the **check_test** command to automatically infer a default protocol for the design. If a custom protocol is read in using the **read_test_protocol** command, execute **check_test** to extract detail's of the design's scan chains.

Note: If you create a protocol for a design, make sure that it is the same protocol used when existing pattern database files were created. If the protocols are different, the **write_test** command fails because the scan test patterns are inconsistent with the protocol. An example of an inconsistency is the use of different scan cells. Ideally, the design and its protocol should always be saved in **db** format after execution of the **create_test_patterns** command.

UIT-24 (warning) vhdlout_single_bit="%s" not supported; assuming vhdlout_single_bit="VECTOR".

DESCRIPTION

The **write_test** command issues this warning if you are writing out your vectors in VHDL format and the **vhdlout_single_bit** variable is not set to *VECTOR* or *BIT*. The warning message indicates which value the**vhdlout_single_bit** variable is set to.

The **vhdlout_single_bit** variable defines whether bussed ports are written as individual single bits in the test pattern. The **write_test** command only supports VECTOR or BIT values for this variable. However, the default value for this variable is *USER*. If you use the value *USER*, the **write_test** commmand will issue this message and automatically change the **vhdlout_single_bit** variable to *VECTOR*. Your vectors will be written out with the ports bussed.

WHAT NEXT

To avoid this violation, set the **vhdlout_single_bit** variable for *VECTOR* or *BIT* before issuing the **write_test** command.

If you have used the value *USER* and wish to write out your vectors in bit-blasted fashion, you will need to set the **vhdlout_single_bit** variable to *BIT* and re-execute the **write_test** command.

If you have used the value *USER* and wish to write out your vectors in bussed fashion, then no action is required on your part.

UIT-26 (error) Strobe value is required to be less than period value.

DESCRIPTION

Your strobe value has exceeded the period value.

WHAT NEXT

Change your strobe value.

UIT-27 (error) %s is a serial-only vector format.

DESCRIPTION

Invalid vectors are generated if you invoke **write_test** with the *-parallel* option for serial-only vector formats. When such an error occurs, this error message displays.

WHAT NEXT

for serial-only vector formats, invoke **write_test** without the *-parallel* option.

UIT-28 (error) Current test protocol cannot be used with a parallel load format.

DESCRIPTION

Currently the only protocols inferred by check_test can be used with a parallel load format. Therefore any custom test protocols cannot use this format due to the fact

that it is difficult to determine which bits correspond to which registers. This error message is displayed when such an error occurs. This error message will also be issued when it does not make sense to write out vectors in parallel load format, such as trying to write out parallel vectors for a combinational design or for a design which contains no scan element.

WHAT NEXT

Either let check_test infer a test protocol to use a parallel load format or do not use the parallel load format.

UIT-29 (error) No nets have global tracing enabled in design '%s'.

DESCRIPTION

BACKGROUND INFORMATION

Using the **check_test** command, DFT Compiler design rule checking (DRC) is performed by doing a symbolic simulation of the test protocol for a design.

If the data applied at the scan in ports is successfully and predictably loaded into the scan chain, the cells are scan controllable. If data can be captured into the scan cells during the parallel capture cycle, and successfully and predictably unloaded, the cells are scan observable. When sequential cells are neither fully scannable (both scan controllable and scan observable) nor valid nonscan cells (for partial scan designs), fault coverage suffers.

DFT Compiler provides a net tracing capability which allows you to view the results of the symbolic simulation to help in the identification and correction of test protocol problems. DFT Compiler displays the logic values of the nets as information messages. All output from the design rule checker, including information messages, is linked to the design schematic. You can debug your protocol by selecting nets with certain values, then viewing the corresponding section in the schematic through the Design Analyzer.

Net tracing is enabled in either of two fashions. If **trace_nets** *statements* are added to vector or stream groups within a custom test protocol supplied by the designer, they enable tracing within a *local* scope limited to that vector or stream group. Alternatively, by specifying nets using the **trace_nets** *command*, nets can be traced within the *global* scope of the entire current test protocol. The **untrace_nets** command only acts on nets specified by the **trace_nets** command.

MANIFESTATION

This error message is generated when the **untrace_nets** command has been invoked when there are *no* nets in the current design which have *global* tracing enabled as a result of a previous **trace_nets** command.

WHAT NEXT

This is a benign error message indicating that you have asked that tracing be disabled on nets for which *global* tracing is not enabled. If you are still seeing net tracing for any nets, it must be the result of *local* **trace_nets** *statements* in your custom protocol. Remove those statements from the custom protocol.

UIT-30 (error) Global tracing not enabled for net '%s' in design '%s'.

DESCRIPTION

BACKGROUND INFORMATION

Using the **check_test** command, DFT Compiler design rule checking (DRC) is performed by doing a symbolic simulation of the test protocol for a design.

If the data applied at the scan in ports is successfully and predictably loaded into the scan chain, the cells are scan controllable. If data can be captured into the scan cells during the parallel capture cycle, and successfully and predictably unloaded, the cells are scan observable. When sequential cells are neither fully scannable (both scan controllable and scan observable) nor valid nonscan cells (for partial scan designs), fault coverage suffers.

DFT Compiler provides a net tracing capability which allows you to view the results of the symbolic simulation to help in the identification and correction of test protocol problems. DFT Compiler displays the logic values of the nets as information messages. All output from the design rule checker, including information messages, is linked to the design schematic. You can debug your protocol by selecting nets with certain values, then viewing the corresponding section in the schematic through the Design Analyzer.

Net tracing is enabled in either of two fashions. If **trace_nets** *statements* are added to vector or stream groups within a custom test protocol supplied by the designer, they enable tracing within a *local* scope limited to that vector or stream group. Alternatively, by specifying nets using the **trace_nets** *command*, nets can be traced within the *global* scope of the entire current test protocol. The **untrace_nets** command only acts on nets specified by the **trace_nets** command.

MANIFESTATION

This error message is generated when a net specified by the **untrace_nets** command does not currently have *global* tracing enabled as a result of a previous **trace_nets** command.

If an asterisk (*) is encountered within a net name passed to **untrace_nets**, the set of all nets in the design containing the associated partial net name specified will be checked for tracing. If no net within the set was found to have tracing enabled, this error message is invoked for *all* the nets in the set.

WHAT NEXT

This is a benign error message indicating that you have asked that tracing be disabled on a net for which *global* tracing is not enabled. If you are still seeing net tracing for this net, it must be the result of a *local* **trace_nets** *statements* in your custom protocol. Remove that statement from the custom protocol.

If this error message is being produced multiple times it probably indicates that you have made imprecise use of a wildcard asterisk (*) when specifying your net. Check your use of asterisks within your list of net names passed to the **untrace_nets** command.

UIT-31 (error) Cannot find vector file '%s' written by TestSim.

DESCRIPTION

This error message will appear when you are trying to perform the **write_test** command on a test program created by a fault simulation run. During a fault simulation run, two **.vdb** files are created : **<test_program_name>.vdb** and **<test_program_name>.testsim.vdb**. The **write_test** command needs both of these files to write out the output vector file.

WHAT NEXT

Confirm that you have not accidentally deleted this file. If you have deleted this file, you will have to re-run fault simulation.

UIT-32 (error) Bad protocol format '%s'.

DESCRIPTION

You receive this message if you specify a test protocol format other than stil or tpf; these are the only formats allowed by **write_test_protocol**. By default, **write_test_protocol** uses tpf format.

WHAT NEXT

Re-execute **write_test_protocol** and specify either stil or tpf as the protocol format. Alternatively, if you want to use the default format (tpf), you can execute **write_test_protocol** with no format specification.

SEE ALSO

write_test_protocol(2).

UIT-33 (error) Bad test model format '%s'.

DESCRIPTION

You receive this message if you specify a test model format other than ctl; this is the only format allowed by **write_test_model**.

WHAT NEXT

Re-execute **write_test_model** and specify ctl as the test model format, or do not specify any format.

SEE ALSO

write_test_model(2).

UIT-34 (warning) Redundant TCK period specification '%f' ignored.
Existing TCK period '%f' (frequency '%e') retained.

DESCRIPTION

This warning message is generated when **insert_jtag -tck_period** is invoked on a design with an existing boundary scan Test Access Port (TAP) TCK port where a clock has been previously specified at this port. The period and resulting frequency of this clock is reported in the message. In this case, DFT Compiler ignores the new specification and retains the old specification.

WHAT NEXT

If the old specification (probably generated using the **create_clock** command) is unsatisfactory, either remove the clock attribute on the TAP TCK port and invoke **insert_jtag -tck_period** *<correct_period>*, or change the existing clock period specification and invoke **insert_jtag** without the **-tck_period** option.

UIT-35 (error) Physical dft preview doesn't support the shadow logic client.

DESCRIPTION

You receive this message if you've specifed the shadow logic DFT client to be

executed during DFT logic preview with the command: set_dft_configuration -order {wrapper} To perform physical dft preview, you have used the following commands: preview_dft -physcial Currently, physical dft preview doesn't support that client. This will prevent the completion of DFT logic previewing .

WHAT NEXT

Reset your DFT configuration: remove_dft_configuration Only set the Autofix client if you wish to use it as well as to perform physical dft preview. set_dft_configuration -order {autofix}. Proceed to DFT logic previewing.

SEE ALSO

preview_dft(2). insert_dft(2). set_dft_configuration(2).

UIT-36 (Error) Test protocol already exists for design '%s'.

DESCRIPTION

A valid test protocol already exists in memory. It was either created by using create_test_protocol command or read by using read_test_protocol command.

WHAT NEXT

You have to use remove_test_protocol command to avoid this message.

SEE ALSO

create_test_protocol, read_test_protocol, remove_test_protocol.

UIT-37 (Warning) Test protocol that already exists for design '%s' is invalid.

DESCRIPTION

An invalid test protocol exists in memory. It was either created by using create_test_protocol command or read by using read_test_protocol command. This invalid test protocol will be removed and a new one will be created.

WHAT NEXT

You can use remove_test_protocol command to avoid this message and read in a new protocol or create it from scratch.

SEE ALSO

create_test_protocol, read_test_protocol, remove_test_protocol.

UIT-39 (error) The test_require attribute cannot be set on the three-state driver ’%s’.

DESCRIPTION

DFT Compiler will not be able to account for the specified **test_require** on the three-state driver. The specification is ignored.

WHAT NEXT

There are multiple ways to specify required values around a three-state bus: up-stream from the driverds, after the bus, or on the enables. In order to obtain the effect of a require on a single three-state driver, do the following. Identify the driver’s input and enable pins. Manually insert buffers driving these pins. Set the desired test_require value on the driver of the data pin. Set a test_require value of 1 on the driver of the enable pin.

UIT-41 (error) No implementation for component "%s" supplied.

DESCRIPTION

You must specify an implementation for the passed component type.

The implementation must be available in the jtag.db library. It may be a default implementation supplied with DFT Compiler, or a user supplied implementation added to the jtag.db.

Refer to the DFT Compiler reference manual for details of how to add custom components to the jtag.db

WHAT NEXT

Re-execute the command, specifying an implementation type from those available in the jtag.db.

UIT-42 (error) ’%s’ is not a valid value for %s option of the

check_test command.

DESCRIPTION

This message tells you that you have given the **check_test** command invalid **-check_contention** or **-check_float** option arguments.

WHAT NEXT

Repeat the **check_test** command using valid option arguments.

UIT-43 (information) %s won’t force conditioned bidirectionals.

DESCRIPTION

The default protocol inferred by DFT Compiler assumes that all bidirectional ports are turned in the same direction during scan shift. They can be turned inwards or outwards.

This message tells you that scan insertion does not insert logic to reconfigure ports that are turned in the opposite direction during scan shift.

WHAT NEXT

Set "test_force_conditioned_bidir_pads" to "true" to change this behavior.

UIT-44 (information) Assuming %s for combinational methodology.

DESCRIPTION

This message tells you that DFT Compiler does not insert disabling logic when the test methodology is combinational.

WHAT NEXT

If you want to insert disabling logic, change the test methodology. To make the warning go away, ask for no disabling logic.

UIT-45 (information) %s won’t find the best scan-out pins.

DESCRIPTION

This message tells you that scan insertion does not look for the best scan-out pins when it routes scan chains.

WHAT NEXT

Set "test_disable_find_best_scan_out" to "false" to change this behavior.

UIT-46 (information) %s will create dedicated subdesign scan-out ports.

DESCRIPTION

You receive this message because DFT Compiler does not look for existing connections and creates dedicated subdesign scan-out ports if no port has a **test_scan_out signal_type** attribute.

When connecting scan chains from subdesigns to parent designs, DFT Compiler first looks for subdesign ports that have **test_scan_out signal_type** attributes. DFT Compiler then checks to see whether an existing connection can be used. If nothing is found, DFT Compiler creates a dedicated subdesign scan-out port.

WHAT NEXT

Set the **test_dedicated_subdesign_scan_outs** environment variable to **false** to change this behavior.

SEE ALSO

test_dedicated_subdesign_scan_outs (3).

UIT-47 (warning) Dedicated subdesign scan-out ports will be created for sub-designs when hierarchical isolation is specified. Ignoring hierarchical isolation if there are exsting dedicated

subdesign scan-out ports.

DESCRIPTION

You receive this message because DFT Compiler does not create dedicated subdesign scan-out ports when you also requested hierarchical isolation logic. The request for hierarchical isolation logic takes precedence. If the sub-designs already have dedicated scan-out ports hierarchical isolation request will not be valid.

When connecting scan chains from subdesigns to parent designs, DFT Compiler first looks for subdesign ports that have **test_scan_out signal_type** attributes. DFT Compiler then checks to see if an existing connection can be used. If it finds none, it creates a dedicated subdesign scan-out port.

You can set the **test_dedicated_subdesign_scan_outs** environment variable to **true** to direct DFT Compiler to ignore existing connections and create dedicated subdesign scan out ports.

WHAT NEXT

To obtain dedicated subdesign scan-outs, do not ask for hierarchical isolation logic. Set the **test_dedicated_subdesign_scan_outs** environment variable to **false** to eliminate the warning message.

SEE ALSO

test_dedicated_subdesign_scan_outs (3).

UIT-48 (warning) Scan insertion will not add clock gating logic.

DESCRIPTION

Sequential ATPG assumes that valid nonscan cells in designs using multiplexed flip-flop scan styles retain their states during scan shift. To insert clock gating logic into your design and falidate this assumption, use the **-clock_gating** option of **set_scan_configuration**.

This message tells you that you decided not to insert clock gating logic. **check_test** violates nonscan cells that do not retain their states during scan shift, and **create_test_patterns** cannot use them to control or observe test vectors.

WHAT NEXT

Confirm that you do not want scan insertion to add clock gating logic.

UIT-49 (warning) Scan style '%s' does not implement scan clock gating. Ignoring the set_scan_configuration -clock_gating command.

DESCRIPTION

Only the multiplexed_flip_flop scan style implements scan clock gating. This message tells you that you asked DFT Compiler to implement scan clock gating, but have specified a scan style that is not a multiplexed_flip_flop. DFT Compiler is telling you that it is ignoring your **-clock_gating** option.

WHAT NEXT

To get rid of the warning, remove the **-clock_gating** from the **set_scan_configuration** option list, or set the scan style to multiplexed_flip_flop.

UIT-50 (warning) Test methodology '%s' does not implement scan clock gating. Ignoring the set_scan_configuration -clock_gating command.

DESCRIPTION

Only the partial scan test methodology implements scan clock gating. This message tells you that you asked DFT Compiler to implement scan clock gating, but specified a test methodology that is not partial_scan. DFT Compiler is telling you that it is ignoring your **-clock_gating** option.

WHAT NEXT

To get rid of the warning, remove the **-clock_gating** from the **set_scan_configuration** option list, or set the test methodology to partial_scan.

UIT-51 (warning) Area-critical partial scan is not enabled. Ignoring the set_scan_configuration -area_critical true command.

DESCRIPTION

Ultimately, DFT Compiler covers the entire scan spectrum. By default, DFT Compiler selects scan cells to maximize fault coverage, subject to both area and timing

constraints. Tell DFT Compiler to ignore area constraints by setting a **set_scan_configuration -area_critical** option **false**, and tell it to ignore timing constraints by setting a **set_scan_configuration -timing_critical** option **false**. The user model sees timing-critical partial scan as the first step to scan spectrum coverage. Tell DFT Compiler to maximize fault coverage subject to timing constraints, and ignore area constraints. Give **set_scan_configuration** an **-area_critical** option, and ask for timing-critical partial scan by giving it a mandatory **false** argument.

WHAT NEXT

To get rid of the warning, remove the **-area_critical true** from the **set_scan_configuration** option list.

UIT-52 (warning) Test methodology '%s' cannot not scan cells on timing critical paths. Ignoring the set_scan_configuration -area_critical command.

DESCRIPTION

Only the partial scan test methodology cannot scan cells on timing critical paths. This message tells you that you asked DFT Compiler to implement not scan cells on timing critical paths, but specified a test methodology that is not partial_scan. DFT Compiler is telling you that it is ignoring your **-area_critical** option.

WHAT NEXT

To get rid of the warning, remove the **-area_critical** from the **set_scan_configuration** option list or set the test methodology to partial_scan.

UIT-53 (information) Enabling area critical partial scan.

DESCRIPTION

DFT Compiler can make scan cells non-scan to meet area constraints. Use this capability when you need to back off scan in a small percentage of cells to meet critical area constraints.

This message tells you that the capability is enabled.

WHAT NEXT

Confirm that you want to use the capability. To tell the DFT Compiler that you do not want to use the capability, use **set_scan_configuration -area_critical false**.

UIT-54 (Error) The format tpf is no longer supported.

DESCRIPTION

You receive this error message because you invoked one of the following commands: read_init_protocol or read_test_protocol or write_test_protocol with the -format option set to tpf. The tpf format has been obsoleted and the only valid format is the stil format.

WHAT NEXT

While writing the test protocol, replace the tpf format by the stil format and reissue the command. While reading an initialization protocol or a test protocol, ensure that the protocol has the stil format, replace the tpf format by the stil format and reissue the command.

SEE ALSO

read_init_protocol (2), **read_test_protocol** (2), **write_test_protocol** (2).

UIT-55 (Error) All the scan signals have to be routed in the compression flow.

DESCRIPTION

You receive this error message because the scan_signals option of the set_scan_configuration command has to be set to all for the scan compression feature.

WHAT NEXT

Set to all the scan signals for the set_scan_configuration command.

SEE ALSO

set_scan_configuration (2),

UIT-56 (Error) Scan methodology must be multipexed_flip_flop

and all the scan signals have to be routed in the logic BIST flow.

DESCRIPTION

You receive this error message related to the set_scan_configuration command because the methodology must be set to multiplexed_flip_flop, the scan_signals option must be set to all and the route option must be set to true for the logic BIST flow.

WHAT NEXT

Set to multiplexed_flip_flop the methodology, set to all the scan signalsand set to true the route for the set_scan_configuration command.

SEE ALSO

set_scan_configuration (2),

UIT-87 (warning) Assignment of %s-only BSR cells to port '%s' is not compliant with the IEEE 1149.1 JTAG standard.

DESCRIPTION

Unless the user requests a user-defined Boundary Scan Register (BSR) cell implementation using the **set_jtag_implementation** command, DFT Compiler selects default BSR cells from among the following 10 defined types:

TypeDefault NameBSR Cell Function

BSRINBOTHJTAG_BSRINBOTHset & observe data input cell
BSRINSETJTAG_BSRINSETset-only data input cell
BSRINOBSJTAG_BSRINOBSobserve-only data input cell
BSRINCLKBOTHJTAG_BSRINCLKBOTHset & observe clock input cell
BSRINCLKSETJTAG_BSRINCLKSETset-only clock input cell
BSRINCLKOBSJTAG_BSRINCLKOBSobserve-only clock input cell
BSROUTBOTHJTAG_BSROUTBOTHset & observe data output cell
BSROUTSETJTAG_BSROUTSETset-only data output cell
BSROUTOBSJTAG_BSROUTOBSobserve-only data output cell
BSRCTLJTAG_BSRCTLcontrol cell

IEEE 1149.1 Standard rule 10.1.1 specifies legal boundary scan register cell types. Several of the 10 types listed above are not compliant with the standard. Nonetheless, DFT Compiler supports them in order to allow designers the greatest possible flexibility when using Programmable JTAG.

10.1.1(b) "For a unidirectional system input pin (clock or nonclock), a

boundary-
scan register cell shall be connected between the system pin and the
on-
chip system logic to allow the state of the system pin to be observed and,
optionally, for the state of the system logic to be controlled."

Thus, legal data and clock input BSR cell types for unidirectional system input pins are observe-only and both control and observe. BSRINSET and BSRINCLKSET are non-compliant types.

10.1.1(c) "For 2-state and open-collector system output pins, a
boundary-
scan register cell shall be provided to allow the state of the system
pin to be controlled and the state of the on-
chip system logic output to be
observed."

Thus, the legal output BSR cell type for system 2-state and open-collector output pins is both control and observe. BSROUTSET and BSROUTOBS are non-compliant types.

10.1.1(d) "For 3-state system output pins, boundary-scan register cells shall be provided to allow both the data value and the output drive sta
te
(active or inactive) to be controlled and for the corresponding system
logic
outputs to be observed."

Thus, the legal output BSR cell type for system 3-state output pins is both control and observe. BSROUTSET and BSROUTOBS are non-compliant types.

10.1.1(e) "For a bidirectional system pin, boundary-scan register cells shall be provided to allow the value and direction of data at the syste
m pin to
be controlled *or* observed and, where appropriate, for the corresponding system logic inputs to be controlled."

This is somewhat ambiguous. Test Compiler interprets this rule to indicate that as applied to bidirectional signals BSRINSET, BSROUTSET and BSROUTOBS are non-compliant types.

The types '**BSR**xxx**BOTH**' (control and observe) '**BSR**xxx**SET**' (control-only) and '**BSR**xxx**OBS**' (observe-only) differ. They correspond respectively to the three modes 'both', 'control' and 'observe' specified with the **set_jtag_port_mode** command. When this command is invoked for one or more ports of the design, BSR cells for those ports will have BSR cells of the specified type associated with them.

If the specified type will result in a non-compliant BSR cell being synthesized for a port, this warning message is issued.

WHAT NEXT

Determine whether non-compliant BSR cells can be tolerated in your design. If not, modify the port mode settings for the offending ports.

UIT-88 (error) Data register ‘%s‘ pin of type ‘%s‘ not found.

DESCRIPTION

You receive this message because the specified data register pin is not recognized as a port at the top level of the core design.

As a designer customizing the JTAG chip interface, you may want the JTAG Test Access Port (TAP) to access core test structures that DFT Compiler cannot automatically recognize. For example, suppose you want to activate a RAM test using an embedded test data register. You must do the following:

1. Initiate the test. 2. Capture the result of the test in the data register. 3. Shift the test result out through **TDO**.

To perform this test using the JTAG TAP, you require:
• An activation signal enabled by the associated JTAG instruction. This signal enters the data register through its *enable_pin*.

• Connection of the data register’s serial input to **TDI**. This connection is optional, required only if data must be shifted *into* the data register to execute the test. This signal enters the data register through its *load_pin*.

• An input to the JTAG MUX (which selects between data registers) dedicated to this data register. This input is selected when the associated JTAG instruction is active. This signal leaves the data register through its *capture_pin*.

In order to retain the functional and structural identity of the core logic, the DFT Compiler’s JTAG logic synthesis interacts with the design’s core logic at the top level of the design’s hierarchy. This ensures that simulation of the core logic, before and after JTAG synthesis, remains identical. Thus, for DFT Compiler to automatically connect to the JTAG TAP the *capture_pin*, *load_pin*, and *enable_pin* of a user-specified core data register, these pins must exist as pseudo-ports at the top level of the original circuit. That is, it is the responsibility of the designer to ensure that the signals controlling and observing a core test register traverse the circuit hierarchy until they are visible at the top level of the design.

WHAT NEXT

Determine the reason that the pin has not been found. If it is appropriately named, check to ensure that the pin appears as a pseudo-port of the top level of the design core.

UIT-89 (error) An illegal implementation ‘%s‘ has been specified for JTAG component type ‘%s‘.

DESCRIPTION

Any alternate implementation for one of the JTAG component types

- the Test Access Port (TAP) Controller: **TAP**,
- the Bypass Register: **BR**
- the device Identification Register: **ID**
- the JTAG instruction register: **IR**, or
- one of the Boundary Scan Register cells: **BSRINBOTH**, **BSRINSET**, **BSRINOBS**, **BSROUTBOTH**, **BSROUTSET**, **BSROUTOBS**, **BSRCTL**, **BSRINCLKBOTH**, **BSRINCLKSET** or **BSRINCLKOBS**

must have all the I/O ports that exist on the default implementation.

WHAT NEXT

Compare the I/O of the user-specified implementation with that of the default component of the specified component type.

UIT-90 (error) set_jtag_implementation must be invoked with a legal component type. ‘%s‘ is not a recognized component type.

DESCRIPTION

set_jtag_implementation must be invoked with one of the JTAG component types

- the Test Access Port (TAP) Controller: **TAP**,
- the Bypass Register: **BR**
- the device Identification Register: **ID**
- the JTAG instruction register: **IR**, or
- one of the Boundary Scan Register cells: **BSRINBOTH**, **BSRINSET**, **BSRINOBS**, **BSROUTBOTH**, **BSROUTSET**, **BSROUTOBS**, **BSRCTL**, **BSRINCLKBOTH**, **BSRINCLKSET** or **BSRINCLKOBS**

These are the *only* legal JTAG component types.

WHAT NEXT

Invoke the dc_shell JTAG command with the **-help** option to review the correct command syntax and make sure a legal JTAG component type has been selected.

UIT-91 (warning) Illegal JTAG ground_bounce value ‘%d‘ replaced by ‘%d‘.

DESCRIPTION

The environmental variable **test_jtag_ground_bounce_limit** has been added to the .synopsys setup environment to provide the user with a mechanism to ensure that the ‘ground bounce’ problem does not occur for designs with JTAG synthesized by DFT Compiler.

This problem arises when the pins of a chip that does not normally support simultaneous switching or enabling of all outputs are controlled from the Boundary Scan Register (BSR), rather than from the on-chip system logic. For example, this situation arises when the EXTEST instruction is selected. It is possible that the tests supplied through the boundary-scan path will cause all outputs to change state and/or be active simultaneously. If precautions are not taken, the sum of the switching currents of all pins may produce VCC and VSS glitches that could exceed the tolerance level of the IC, and the core logic as well as the BSR cells and TAP would then be subject to interference. The power consumption could be increased beyond the capacity of the power pins for a prolonged period, perhaps resulting in incorrect operation of the chip.

Delays that only effect the signal path when the chip is in JTAG test mode can be added to prevent simultaneous switching of outputs when pins are driven from the BSR. The added delays should be small in comparison with the minimum period of TCK, but should be sufficient to ensure that the power-current demand arising from the change of state at one pin or group of pins does not overlap with that from another group producing the excessive power consumption.

However, if the process to optimize the number of BSR cells results in a single BSR cell (for example a bus three-state enable signal) driving too many enable signals, there is no way to introduce delays between the signals controlled by that BSR cell and ground bounce may not be prevented.

The environmental variable test_jtag_ground_bounce_limit puts a cap on the number of ouputs that can be driven by a single BSR cell. A default value is establised for this variable. The user can establish another positive non-zero limit, by changing the value of the variable in the .synopsys_dc.setup file.

The value of the ground-bounce limit for a particular JTAG design can be determined by executing **report_test -jtag**.

A detailed discussion of the Ground-Bounce problems is presented in Chapter 15, ‘Providing Boundary-Scan on Chips with Power or Output-Switching limitations’ of ‘The Test Access Port and Boundary-Scan Architecture’ by Colin M. Maunder and Rodham E. Tulloss, IEEE Computer Society Press Tutorial, 1990.

WHAT NEXT

Reset the value of the *test_jtag_ground_bounce_limit* to a legal value.

UIT-92 (information) User defined instruction '%s' not associated with
identifiable data register. Dangling signals will be synthesized.

DESCRIPTION

Each JTAG instruction activates a single target data register. By definition, the target register of any user defined instruction is not specified in the IEEE 1149.1 JTAG Standard; therefore, that target register cannot be inferred by DFT Compiler. The user must identify the target register by using either **-reg_name** *core_scan_chain_name* or **-reg_coordinates** *capture_pin* [*load_pin*] and **-reg-enable** *enable_pin*.

When invoking **set_jtag_instruction** *instruction_name* [**-code** *code*] if you do not specify **-reg_name** *core_scan_chain_name*, **-reg_coordinates** *capture_pin* [*load_pin*], or **-reg-enable** *enable_pin*, DFT Compiler will synthesize all the necessary instruction decode logic and create two new design ports: an input port called <*instruction_name*>**CAPTURE** and an output port called <*instruction_name*>**ENABLE**. The port <*instruction_name*>**ENABLE** is active **HIGH** when the instruction *instruction_name* is loaded into the IR. The designer can then manually edit the circuit to connect these two signals to the appropriate data register circuitry.

WHAT NEXT

Manually connect the two signals <*instruction_name*>**CAPTURE** and <*instruction_name*>**ENABLE** to the appropriate data register circuitry.

UIT-93 (warning) One or more ports have been excluded from the JTAG
Boundary Scan Register (BSR). JTAG logic synthesized based on this
configuration will not be compliant with the IEEE 1149.1 JTAG standard.

DESCRIPTION

The IEEE 1149.1 JTAG Standard specifies that *all* non-TAP I/O ports must be included in the BSR. Exclusion of one or more ports results in this warning message.

WHAT NEXT

If a non-compliant JTAG implementation is satisfactory, ignore this message.

Otherwise, compliance with this condition may be met by executing **set_jtag_port -default**.

UIT-94 (error) Erroneous JTAG data register '%s' associated with JTAG instruction '%s'.

DESCRIPTION

The IEEE 1149.1 JTAG Standard specifies and requires three mandatory JTAG instructions: BYPASS, SAMPLE/PRELOAD and EXTEST. If a JTAG device Identification Register (IDreg) exists, then a fourth JTAG instruction, IDCODE, is mandatory. The standard also defines three other instructions: INTEST, RUNBIST and USERCODE. The target register selected by each of these instructions is designated by the standard as follows:

Instruction**Target Data Register**

BYPASS**JTAG_BYPASS_REG**
SAMPLE/PRELOAD**JTAG_BSR**
EXTEST**JTAG_BSR**
INTEST**JTAG_BSR**
IDCODE**JTAG_ID_REG**
USERCODE**JTAG_ID_REG**
RUNBIST**JTAG_BIST_REG**

Because only one data register is associated with each of these instructions, it need never be specified by the designer. If the target data register *is* specified, using **set_jtag_instruction** *instruction_name* **-reg_name** *name*, a check is made that the legal data register has been specified. This error message appears if an illegal register is specified.

Note, however, that if you specify a particular core BIST register with RUNBIST, you need to include register coordinate information.

WHAT NEXT

Since specifying the data register with any of these seven JTAG instructions is redundant, avoid this error by simply removing the erroneous specification.

UIT-95 (error) JTAG logic already inserted into this design.

insert_jtag not invoked.

DESCRIPTION

Invoking JTAG synthesis on a design twice returns an error. The danger is that preexisting JTAG logic might be confused with core logic and result in duplicate JTAG logic synthesis.

When DFT Compiler successfully inserts JTAG into a design, it sets a design attribute flag. A call to **insert_jtag** is not executed if a check for the presence of this design attribute indicates pre-existing JTAG logic.

WHAT NEXT

If you want to reinvoke JTAG synthesis, make sure you begin with a clean design without JTAG.

UIT-96 (error) Port '%s' excluded from the JTAG Boundary Scan Register (BSR).
No BSR cells can be associated with it.

DESCRIPTION

BSR cells are only synthesized for ports that are included in the JTAG BSR. Thus it is an error to specify a routing order for BSR cells relative to ports that are excluded from the BSR.

WHAT NEXT

Either remove reference to those BSR cells associated to the excluded port or specify inclusion of the port in the BSR by executing **set_jtag_port** TRUE *port_name*.

UIT-97 (error) '%s' not an input or output port.
(You must specify '/out', '/in' or '/ctl'.)

DESCRIPTION

For bidirectional ports, the *port_name* is insufficient to differentiate between the Boundary Scan Register (BSR) input, output, and control cells.

WHAT NEXT

A trailing specifier **/in**, **/out** or **/ctl** must be appended to *port_name* to identify each bidirectional port BSR cell.

UIT-98 (error) '%s' not a port of the current design.

DESCRIPTION

JTAG Boundary Scan Register (BSR) cells can only be specified in **set_jtag_port_routing_order** relative to ports in the current design.

WHAT NEXT

Check the ports of the current design to verify the set of legal *port_name* candidates.

UIT-99 (error) Unrecognized BSR cell specifier '%s'. (Must be '/out', '/in' or '/ctl'.)

DESCRIPTION

The *ordered_list_of_annotated_BSR_port_names* contains members of four classes:

- <*input_or_output_port_name*> which, depending on the direction of the port, specifies a BSR input or output cell;
- <*bidirectional_port_name*>**/in** which specifies the BSR input cell associated with this bidirectional port;
- <*bidirectional_port_name*>**/out** which specifies the BSR output cell associated with this bidirectional port;
- <*tristate_or_bidirectional_port_name*>**/ctl** which specifies the BSR three-state control cell associated with this output or bidirectional port.

WHAT NEXT

Only three legal specifiers (**/in**, **/out** or **/ctl**) may be appended to a *port_name* to identify a BSR cell.

UIT-100 (error) Instruction Register (IR) too small.

This design requires an %d-bit register.

DESCRIPTION

The IEEE 1149.1 JTAG Standard mandates that the JTAG Instruction Register (IR) be at least two bits wide. DFT Compiler supports IRs of between 2 and 32 bits inclusively. The size of the IR is set in three ways:

- specifying the size using **insert_jtag -ir_size** *bit_width*;
- forcing the IR size by specifying an instruction code **set_jtag_instruction -code** "*code*";
- DFT Compiler will automatically infer the IR size from the set of specified and mandatory instructions selected.

WHAT NEXT

UIT-101 (error) JTAG Test Access Port (TAP) I/O port '%s' may not be included in the boundary scan register (BSR).

DESCRIPTION

The IEEE 1149.1 JTAG Standard specifies that the Boundary Scan Register (BSR) is a data register connected between TDI and TDO. The BSR may not include any of the JTAG Test Access Port (TAP) ports. An error will result if you include ports carrying the following signals:

- TDI: JTAG Test Data In
- TDO: JTAG Test Data Out
- TMS: JTAG Test Mode Select
- TCK: JTAG Test Clock
- TRST: JTAG Test Reset

WHAT NEXT

UIT-102 (error) Illegal JTAG boundary scan port mode '%s' specified.

DESCRIPTION

The JTAG circuitry associated with each port allows that port to be **controlled** only, **observed** only, or **both** controlled and observed. This is the JTAG operational mode of

a port.

The default mode can be initially set in the .synopsys file using **jtag_bsr_port_mode** = '<mode_string>' where allowable port modes are **control**, **observe**, or **both**.

WHAT NEXT

UIT-103 (error) Illegal JTAG boundary scan port signal type '%s' specified.

DESCRIPTION

The JTAG circuitry associated with a port can be optimized depending on the signal type, **clock**, **enable** or **data**, of that port.

The JTAG circuitry associated with an *input* port can be optimized based on the signal type (**clock** or **data**) of that port. Ports that drive clock trees can be associated with specialized JTAG circuitry. An input port can be explicitly identified as carrying one of the "clock" or "data" categories.

When the three-state elements driving three-state and bidirectional *outputs* are found in the core logic of the IC (i.e. not embedded in the pads themselves) DFT Compiler requires that these three-state elements be located at the top hierarchy of the core of the design so that Boundary Scan Register (BSR) cells can be placed on the **inside** of the three-state elements in order to control and observe the data and enable lines. In these cases, only a single three-state line exits the core logic.

However, in the cases where the three-state controller for output signals will be embedded in the three-state output or bidirectional input/ouput pad associated with these ports of a design two signals exit the core logic; a *data* line and a *enable* line. Unless, TC knows the distinction between these two types of exit lines, it will always assume that they are data lines and not insert the correct type of BSR cell on the enable lines. By specifying "enable" or "data" on a port the designer instructs TC on which type of BSR cell to place on these output ports.

Where possible, DFT Compiler will extract this information from the circuit design. A port may be explicitly identified as carrying one of these catagories of data.

WHAT NEXT

If you are defining the characteristics of input ports, choose between the "clock" and "data" options. If you are defining the characteristics of ouput ports, choose between the "enable" and "data" options.

UIT-104 (error) Requested Instruction Register size '%d' is less than

previously specified Instruction code size '%d'.

DESCRIPTION

The IEEE 1149.1 JTAG Standard mandates that the JTAG Instruction Register (IR) be at least two bits wide. DFT Compiler supports IRs of 2- to 32-bit widths inclusively. The size of the IR is set in three ways:

- specifying the size using **insert_jtag -ir_size** *bit_width*;
- forcing the IR size by specifying an instruction code **set_jtag_instruction -code** "*code*";
- DFT Compiler will automatically infer the IR size from the set of specified and mandatory instructions selected.

This error is generated if one or more JTAG instructions with specified codes of length *n* have been previously specified, but **insert_jtag -ir_size** *m* is invoked where *n* > *m*.

If *m* > *n* then DFT Compiler can pad the *m*-*n* high order bits of the previously specified instruction codes with 0s. But it cannot truncate previously specified codes when *m* > *n*.

WHAT NEXT

Either invoke **insert_jtag -ir_size** with a size greater or equal to the length of all previously specified codes, or, if a smaller IR is required, specify codes for all instructions with previously specifed codes, so that their code length is less than or equal to the desired IR size.

UIT-105 (error) Instruction '%s' has code fixed by the 1149.1 JTAG standard.
You cannot assign the code '%s' to this instruction.

DESCRIPTION

You receive this message because DFT Compiler generates it when an attempt is made to reset **BYPASS** and **EXTEST** JTAG code.

Each JTAG instruction requires the following triplet of information:

- Instruction name
- Target data register
- Instruction code

DFT Compiler can automatically generate some of this information.

The mandatory **BYPASS** and **EXTEST** JTAG instructions have mandatory codes. The **BYPASS** code is all *1*s (ones). The **EXTEST** code is all *0*s (zeros). All other mandatory and nonmandatory JTAG instructions support arbitrary codes.

Since the **BYPASS** and **EXTEST** instructions have mandatory codes, the designer never has to specify them. DFT Compiler automatically extracts all information relative to these two instructions.

UIT-106 (warning) The 1149.1 JTAG standard instruction '%s' does not support register coordinate specification. (Specifications ignored.)

DESCRIPTION

The IEEE 1149.1 JTAG Standard specifies and requires three mandatory JTAG instructions: BYPASS, SAMPLE/PRELOAD, and EXTEST. If a JTAG device Identification Register (IDreg) exists, then a fourth JTAG instruction, IDCODE, is mandatory. The standard also defines three other instructions: INTEST, RUNBIST, and USERCODE. The target register selected by each of these instructions is designated by the standard as follows:

Instruction**Target Data Register**

BYPASS**JTAG_BYPASS_REG**
SAMPLE/PRELOAD**JTAG_BSR**
EXTEST**JTAG_BSR**
INTEST**JTAG_BSR**
IDCODE**JTAG_ID_REG**
USERCODE**JTAG_ID_REG**
RUNBIST**JTAG_BIST_REG**

For the first six JTAG instructions above only one data register is associated with each of these instructions; the register does not need to be specified. In these six cases, if the target data register *is* specified, using **set_jtag_instruction** *instruction_name* **-reg_coordinates** *capture_pin* [*load_pin*] **-reg_enable** *enable_pin*, the register coordinate information is ignored and this warning message is generated.

If you specify a particular core BIST register with RUNBIST, you need to include register coordinate information.

WHAT NEXT

Since specifying the data register with any of these seven JTAG instructions is redundant, avoid this error by simply removing the redundant coordinate specification.

UIT-107 (error) Code length '%d' of instruction '%s' conflicts with a previously specified instruction code length '%d'.

DESCRIPTION

The IEEE 1149.1 JTAG Standard mandates that the JTAG Instruction Register (IR) be at least two bits wide. DFT Compiler supports IRs of 2- to 32- bit widths inclusively. The size of the IR is set in three ways:

- specifying the size using **insert_jtag -ir_size** *bit_width*;
- forcing the IR size by specifying an instruction code **set_jtag_instruction -code** "*code*";
- DFT Compiler will automatically infer the IR size from the set of specified and mandatory instructions selected.

If you specify codes to be assigned to specific instructions, the length of these codes must be consistent with any previously specified codes or the previously specified Instruction Register (IR) size.

WHAT NEXT

Modify the length of the offending codes to be equal that of previously specified instruction codes and/or IR size.

UIT-108 (error) Code '%s' for instruction '%s' conflicts with the code for instruction '%s'.

DESCRIPTION

You receive this message because the code for an instruction conflicts with the code specified for another instruction.

Each instruction must have a unique code that does not conflict with the code specified for another instruction. In the absence of a user-specified code for an instruction, DFT Compiler generates a unique code for that instruction.

Each JTAG instruction requires a triplet of information:

- Instruction name
- Target data register
- Instruction code

DFT Compiler can automatically generate some of this information. The mandatory **BYPASS** and **EXTEST** JTAG instructions have mandatory codes. The **BYPASS** code is all *1*s (ones). The **EXTEST** code is all *0*s (zeros). All other mandatory and nonmandatory JTAG

instructions support arbitrary codes.

WHAT NEXT

Eliminate the coding conflict by executing a legal change of code for one of the two conflicting instructions. (You cannot change the mandatory codes of the **BYPASS** and **EXTEST** instructions.)

Again execute the **set_jtag_instruction** command.

While changing the conflicting code, you must keep all other specifications relative to the instruction the same.

SEE ALSO

set_jtag_instruction (2).

UIT-109 (error) BSR cell '%s' has been assigned multiple routing positions.

DESCRIPTION

Each JTAG Boundary Scan Register (BSR) cell only appears once in the BSR. Therefore, when specifying its location in the BSR using the **set_jtag_port_routing_order** instruction, it is an error to specify more than one location for each BSR cell.

WHAT NEXT

Remove multiple specifications of the BSR cell reported in the error message, leaving at most one reference to it in the *ordered_list_of_annotated_BSR_port_names* when executing **set_jtag_port_routing_order**.

UIT-110 (warning) Compliance with the IEEE's 1149.1 JTAG Standard requires a BYPASS Register. This implementation is non-compliant.

DESCRIPTION

If you specify that a JTAG BYPASS register not be synthesized, the resulting JTAG architecture will *not* be IEEE 1149.1 compliant.

WHAT NEXT

If you want a compliant JTAG architecture, do not invoke **insert_jtag** with the **-no_bypass** option.

UIT-111 (warning) JTAG component implementation '%s' not found.
The default implementation will be used instead.

DESCRIPTION

The basic JTAG components (**BSRin**, **BSRout**, **BSRcontrol**, **TAP**, **BYPASS**, **ID**, and **IR**) must have functionality that conforms the the IEEE 1149.1 standard. Each can be implemented in a number of different architectures. There are several different functionality implementations (set-only, observe-only, or both set and observe) of the JTAG Boundary Scan Register (BSR) cells. DFT Compiler has a default implementation for each of the three types (input, output, and control) of BSR cells.

You can override the default implementation of all the JTAG components:

- one of the Boundary Scan Register (BSR) cells **BSRin**, **BSRout**, or **BSRcontrol**
- the Test Access Port (TAP) Controller **TAP**
- the Bypass Register **BYPASS**
- the device Identification Register **ID**
- the JTAG instruction register **IR**

by executing

set_jtag_implementation component_type *implementation*

where **component_type** is **BSRin**, **BSRout**, **BSRcontrol**, **TAP**, **BYPASS**, **ID**, or **IR**.

You can override the implementation of one or more of the BSR cells of the specified type in the BSR by executing the **set_jtag_implementation** instruction with the correct arguements:

- **set_jtag_implementation BSRin** *implementation* [*list_of_ports*]
- **set_jtag_implementation BSRout** *implementation* [*list_of_ports*]
- **set_jtag_implementation BSRcontrol** *implementation* [*list_of_ports*]

The *implementation* is the name of the desired JTAG component in the JTAG component library. If DFT Compiler cannot find this component in the library, it issues this message and uses the default implementation for this type of BSR cell.

WHAT NEXT

If you want to override the default implementation, make sure that the JTAG

component named *implementation* is in the JTAG library.

UIT-112 (error) Target core register '%s' not found.

DESCRIPTION

If you want to specify an instruction and, optionally, the code for a specific internal scan chain, execute **set_jtag_instruction** *instruction_name* **-reg_name** *name* [**-code** *code*].

The *name* of each internal scan chain is the name of its parallel scan-in port; that is, the port which has the **test_scan_in** attribute assigned to it. This guarantees the uniqueness of names for these scan chains and provides DFT Compiler with a mechanism to identify each target scan chain. If DFT Compiler cannot find this unique parallel scan-in port, this message is generated.

WHAT NEXT

Verify the names of the parallel scan-in ports of the design using **report_test -scan**.

UIT-113 (information) Creating user defined instruction '%s'. (not a 1149.1 JTAG standard instruction)

DESCRIPTION

DFT Compiler recognizes the seven standard instructions defined by the IEEE 1149.1 JTAG Standard:

Instruction**Target Data Register**

BYPASS**JTAG_BYPASS_REG**
SAMPLE/PRELOAD**JTAG_BSR**
EXTEST**JTAG_BSR**
INTEST**JTAG_BSR**
IDCODE**JTAG_ID_REG**
USERCODE**JTAG_ID_REG**
RUNBIST**JTAG_BIST_REG**

DFT Compiler also accepts user-defined JTAG instructions. These instructions may access core scan chains or invoke other test circuitry in the design. When a user-defined instruction has been successfully parsed, this information message is issued.

The existence of this message also provides a check for mispelled names of the seven

standard JTAG instructions. It verifies that you in fact want to create a user-defined instruction.

WHAT NEXT

UIT-114 (information) Creating 1149.1 JTAG standard instruction '%s'.

DESCRIPTION

DFT Compiler recognizes the seven standard instructions defined by the IEEE 1149.1 JTAG Standard:

Instruction**Target Data Register**

BYPASS**JTAG_BYPASS_REG**
SAMPLE/PRELOAD**JTAG_BSR**
EXTEST**JTAG_BSR**
INTEST**JTAG_BSR**
IDCODE**JTAG_ID_REG**
USERCODE**JTAG_ID_REG**
RUNBIST**JTAG_BIST_REG**

DFT Compiler also accepts user-defined JTAG instructions. This information message confirms that DFT Compiler has recognized and parsed one of the standard instructions.

The existence of this message also provides a check for user-defined instructions which have been mislabeled with standard instruction names.

WHAT NEXT

UIT-115 (error) Illegal joint specification of -no_internal scan and -daisy_chained internal scan. (Specify only one of these options.)

DESCRIPTION

By default DFT Compiler will attach core test structures that it recognizes (for example, internal scan chains) to the JTAG Test Access Port (TAP). Internal scan chains will not be connected to the TAP if you execute **insert_jtag -no_internal_scan**. If you want all of the recognized core scan chains accessible as a

single long register comprised of the individual scan chains serially daisy-chained together, execute **insert_jtag -daisy_chained** [*ordered_set_of_scan_chain_indexes*].

These two options are mutually exclusive. This error message is invoked if both options are specified at once.

WHAT NEXT

Determine which core scan chain option is desired and invoke **insert_jtag** with the appropriate argument.

UIT-116 (information) Instruction '%s' has been cancelled.

DESCRIPTION

Any non-mandatory instruction may be removed from the set of instructions "understood" by the synthesized JTAG instruction decode logic. This message confirms removal of the specified instruction. As a result, decode logic will not be synthesized to recognize this instruction.

WHAT NEXT

UIT-117 (error) Mandatory instruction '%s' may not be cancelled.

DESCRIPTION

The IEEE 1149.1 JTAG Standard requires the following mandatory instructions:

- BYPASS,
- SAMPLE/PRELOAD
- EXTEST.

If a Device Identification (ID) Register is part of the JTAG logic, then IDCODE is also mandatory.

The first three instructions will *always* be included in the set of instructions "understood" by the synthesized JTAG instruction decode logic. If you request an ID register, you must include the fourth instruction, IDCODE. An error message will appear if you attempt to cancel any one of these instructions.

WHAT NEXT

UIT-118 (error) JTAG insertion terminated abnormally.

DESCRIPTION

Anytime DFT Compiler encounters a fatal designer JTAG specification error after **insert_jtag** has been invoked, an error message identifying the problems appears and DFT Compiler executes a graceful abnormal termination of JTAG synthesis. Any changes to the design resulting from execution of **insert_jtag** are eliminated.

Fatal designer JTAG specification errors include encountering a three-state cell controlling a port which is not at the top level of the design (see **UIT-119**); and JTAG component library not found (see **TEST-234**).

WHAT NEXT

Identify and correct the cause of the abnormal termination and reinvoke **insert_jtag**.

UIT-119 (error) Three-state cell ‘%s‘ controlling port(s) in the JTAG Boundary Scan Register not at the top level of the design.

DESCRIPTION

Up to three Boundary Scan Register (BSR) cells can be associated with each port of the design. A simple input port has a single BSR input cell associated with it. If it is a two state output, an output port will have one BSR cell associated with it. If it is a three-state output, it will have two BSR cells associated with it. A bidirectional port can have three BSR cells associated with it (input, output and control BSR cells). When DFT Compiler inserts boundary scan cells for three-state ports into the design, it determines their location by locating the data and control inputs to generic three-state devices.

Whether or not you want to group all system logic into a level of (core) hierarchy, you must ensure that the three-state devices controlling the behavior of any ports are visible at the top level of the core hierarchy. This is necessary for pad optimization since three-states can be absorbed into a pad.

The following script fragment demonstrates this:

```
dc_shell> read -f lsi AMPM.NET

/* get the top level design */
dc_shell> current_design  = DESIGN
```

```
            /
* need to separate any top level port three_state control cells from the core.
               In this case they are buried in sub-modules U6 and U7 */
            dc_shell> ungroup  {U6 U7}

            /* group the core logic with the exception of the 6 three-state cells */
            dc_shell> group -design_name  CORE -except
            {U6/UU2 U6/UU3 U6/UU4 U7/UU4 U7/UU5 U7/UU6} -cell_name  AMPM

            /* need to set port_is_pad to do pad insertion */
            dc_shell> set_port_is_pad find  (port,"*")

            dc_shell> insert_jtag
```

This error message results when DFT Compiler encounters a three-state cell controlling a port which is not at the top level of the design. The complete hierarchical name of the offending cell is reported in the error message. DFT Compiler then gracefully aborts JTAG insertion.

WHAT NEXT

Bring the offending three-state cell to the top level as shown in the script fragment above to eliminate this error.

UIT-120 (warning) -no_asynchronous_reset option invoked but port '%s' with jtag_trst attribute found. Port '%s' will NOT be included in the JTAG Boundary Scan Register (BSR).

DESCRIPTION

The JTAG Test Access Port (TAP) provides the test interface in JTAG mode between the chip and the outside world. It includes the three mandatory input ports (test data in **TDI**, test mode select **TMS**, and test clock **TCK)** and one optional input (test reset **TRST***). It also includes a single output port (test data out **TDO**).

The active-LOW asynchronous reset signal, if present, provides asynchronous initialization of the TAP controller and other JTAG test logic in the circuit. In the absense of the **TRST*** signal, the TAP controller will synchronously enter the *Test-Logic-Reset* controller state following five rising edges of **TCK**, provided **TMS** is held high.

If none of the TAP I/O ports exist, the mandatory ports will be automatically generated. By default, the JTAG logic will be synthesized with an asynchronous reset. The optional **TRST*** port will not be generated if requested using **insert_jtag**

-no_asynchronous_reset. If however, the **TRST*** port already exists, and it has been identified using **set_signal_type** "*jtag_trst*" with **insert_jtag -no_asynchronous_reset** invoked, this warning message is generated to flag the apparent discrepancy in designer intent.

WHAT NEXT

Determine whether an asynchronous reset of the TAP controller is desired and act accordingly. If you want the port with the jtag_trst attribute included in the BSR, remove this attribute using **remove_attribute jtag_trst** *port_name*.

UIT-121 (error) Erroneous JTAG Manufacturer ID Number '%d'.

DESCRIPTION

The JTAG Device Identification Register (IDreg) is permanently loaded with a 32-bit number comprised of the JEDEC chip ID number, the design version number, and the manufacturer ID number.

Since the JTAG Device Identification register has a fixed size with four fixed-size fields, legal values for these fields must fall within the specified ranges. If DFT Compiler encounters an illegal value for the manufacturer ID field, this error message is generated along with error message UIT-124 specifying the erroneous value and the range of legal values.

WHAT NEXT

Enter a legal *integer* for *integer_in_range_0_to_2047* where **0** <= *integer* <= **2407** when executing **set_jtag_manufacturer_id** (see UIT-124).

UIT-122 (error) Erroneous JTAG Part Number '%d'.

DESCRIPTION

The JTAG Device Identification Register (IDreg) is permanently loaded with a 32-bit number comprised of the JEDEC chip ID number, the design version number, and the manufacturer ID number.

Since the JTAG Device Identification register has a fixed size with four fixed-size fields, legal values for these fields must fall within the specified ranges. If DFT Compiler encounters an illegal value for the part number field, this error message is generated along with error message UIT-124 specifying the erroneous value and the range of legal values.

WHAT NEXT

Enter a legal *integer* for *integer_in_range_0_to_65535* where **0** <= *integer* <= **65535** when executing **set_jtag_part_number** (see UIT-124).

UIT-123 (error) Erroneous JTAG Version Number '%d'.

DESCRIPTION

The JTAG Device Identification Register (IDreg) is permanently loaded with a 32-bit number comprised of the JEDEC chip ID number, the design version number, and the manufacturer ID number.

Since the JTAG Device Identification register has a fixed size with four fixed-size fields, legal values for these fields must fall within the specified ranges. If DFT Compiler encounters an illegal value for the design version field, this error message is generated along with error message UIT-124 specifying the erroneous value and the range of legal values.

WHAT NEXT

Enter a legal *integer* for *integer_in_range_0_to_15* where **0** <= *integer* <= **15** when executing **set_jtag_version_number** (see UIT-124).

UIT-124 (information) Number out of legal range. (Must be between %d and %d inclusively.)

DESCRIPTION

Since the JTAG Device Identification register has a fixed size with four fixed-size fields, legal values for these fields must fall within the specified ranges. Legal values for these ranges are specified as non-negative integers within the inclusive range specified in the error message.

WHAT NEXT

Enter a legal *integer* for *integer_in_range_X_to_Y* where **X** <= *integer* <= **Y** when executing **set_jtag_version_number**, **set_jtag_part_number** or **set_jtag_manufacturer_id**. The erroneous field is identified by the previous error message (see UIT-121, UIT-122 or UIT-123).

UIT-125 (warning) -cancel mode should be invoked with

instruction name only.
(Other arguments will be ignored.)

DESCRIPTION

Any non-mandatory instruction may be removed from the set of instructions "understood" by the synthesized JTAG instruction decode logic by executing **set_jtag_instruction** *instruction_name* [**-cancel**].

It is sufficient to supply *instruction_name* to identify which instruction to cancel, so the existence of other arguements to **set_jtag_instruction** is ignored when [**-cancel**] is included.

WHAT NEXT

To eliminate this warning, remove the superfluous arguments when executing [**-cancel**].

UIT-126 (error) ‘00001111111’ (127) is an illegal Manufacturer ID when
used in JTAG ID registers.

DESCRIPTION

The JTAG Device Identification Register (IDreg) is permanently loaded with a 32-bit number comprising the JEDEC chip ID number, the design version number, and the manufacturer ID number.

With respect to the manufacturer number, Rule 11.2.1(b) of the IEEE 1149.1 standard specifies that "00001111111 shall not be used in components that are otherwise compatible with this standard."

DFT Compiler generates this error message if this number is illegally defined using **set_jtag_manufacturer_id** *integer_in_range_0_to2047* [*list_of_designs*].

WHAT NEXT

Enter another manufacturer number using **set_jtag_manufacturer_id** *integer_in_range_0_to2047* [*list_of_designs*]. If you require (integer) 127 as the manufacturer ID number, enter (integer) 0 and manually rewire the code into the IDreg.

UIT-127 (error) Direction of pin '%s' is erroneous.

DESCRIPTION

You may want to control and access core test structures that DFT Compiler is unable to recognize automatically. For example, you may want to activate a RAM test, capture a response from that test structure, and shift it out through TDO.

To support such a scenario, two or three "hooks" are required:

enable_pin(input)- the existence of an activation signal enabled by the associated JTAG instruction
load_pin(input)- optional connection to TDI of the serial input of the core test structure data register
capture_pin(output)- a dedicated MUX input for selecting this data register as the source of TDO output.

You need to select this latter MUX input when the associated JTAG instruction is active. Specify the existence of these "hooks" with the command **set_jtag_instruction** *instruction_name* [**-code** *code*] **-reg_coordinates** *capture_pin* [*load_pin*] **reg_enable** *enable_pin*. If you specify *capture_pin*, *load_pin* and *enable_pin*, the inputs will be connected to the appropriate synthesized JTAG instruction control logic.

Note that if you specified **-reg_coordinates**, the *capture_pin* is mandatory and the *load_pin* is optional. Test compiler checks that the specified pins are of the correct direction, and issues this error message if a pin has an erroneous direction.

If you do not specify the *enable_pin* and *capture_pin*, the result is a synthesis of all the necessary JTAG instruction decode and control logic as well as the creation of two new (bogus) ports connected to the design; an input port named "<*instruction_name*>CAPTURE" and an output port named "<*instruction_name*>ENABLE". The port <*instruction_name*>ENABLE is active HIGH when *instruction_name* is loaded into the JTAG Instruction Register (IR). You can then manually edit the circuit to connect these two (bogus) ports to the appropriate input and output pins of the target core test structure (thus "removing" them as ports).

WHAT NEXT

If the specified pin direction is erroneous, then this is not the correct pin for this signal. Verify the design to identify to correct pin.

UIT-128 (error) Port '%s' must have pad attribute set.

DESCRIPTION

The JTAG Boundary Scan Register (BSR) associates a register with each pad of a device which can be used to either 'capture' (observe) the value at the pad and/or

'apply' (control) a value at the pad distinct from the value applied externally or internally. These registers are serially chained to form the BSR from which their values may be serially set and read.

Since the BSR only includes design ports which will eventually have pads associated with them (that is, *not* module ports internal to the final top level design), DFT Compiler only considers ports which have been designated as requiring pads as candidates for inclusion in the BSR. At least one port must be specified as requiring a pad, since the BSR must have at least one element.

DFT Compiler will generate this error if a port processed by **set_jtag_port** (or any other command processing ports to be included in the BSR) does not have its **port_is_pad** attribute set.

WHAT NEXT

Set the **port_is_pad** attribute using the **set_port_is_pad** command on each port to be considered for inclusion in the BSR. Note that this does not automatically mean that the port *will* be included in the BSR. For example, if a JTAG TAP port has the **port_is_pad** attribute set TRUE, it will nonetheless be excluded from the BSR.

One easy way to specify ports as pads is to execute **set_port_is_pad find (port,"*")** on the current_design.

UIT-129 (warning) -default should be invoked alone. (Other arguments will be ignored.)

DESCRIPTION

Many of the dc_shell JTAG commands include a **-default** argument which resets the specified JTAG settings to their default values. The **-default** argument overrides all other arguments so it should be invoked alone. This error message results from specification of **-default** with other arguments.

WHAT NEXT

Remove the conflicting arguments and reexecute the command.

UIT-130 (error) No options specified for the "%s" command. For available options, execute "%s -help".

DESCRIPTION

You must specify at least one optional argument with this command. This error message is generated when no options are specified with the command, and when the

command is invoked with the **-help** option.

WHAT NEXT

Invoke the command with the **-help** option to review the correct command syntax. Then, re-execute the command, using one of the optional arguments on the command line.

UIT-131 (error) JTAG Port '%s' is not an input or bidirectional port.

DESCRIPTION

Only input or bidirectional ports can take the */in* specifier. There are no input BSR cells associated with an output port. Thus, <*output_port_name*>*/in* is an illegal BSR cell identifier.

In *set_jtag_port_routing_order*, the *ordered_list_of_annotated_BSR_port_names* contains members of four classes:

- <*input_or_output_port_name*>, which specifies a BSR input or output cell (depending on the direction of the port),
- <*bidirectional_port_name*>*/in*, which specifies the BSR input cell associated with this bidirectional port,
- <*bidirectional_port_name*>*/out*, which specifies the BSR output cell associated with this bidirectional port, or
- <*tristate_or_bidirectional_port_name*>*/ctl*, which specifies the BSR three-state control cell associated with this output or bidirectional port.

Thus there are only three legal specifiers ('*/in*', '*/out*' or '*/ctl*') that can be appended to a *port_name* to identify a boundary scan register (BSR) cell. Each of these specifiers can only be associated with a subset of the port types (input, two-state output, three-state output and bidirectional ports) that can be included in the BSR.

DFT Compiler generates this message if you associate a non-existent boundary scan register (BSR) cell type ('*/in*', '*/out*' or '*/ctl*') with a port. DFT Compiler also generates UIT-138, which identifies the nature of the problem.

WHAT NEXT

An illegal specifier for *output_port_name* indicates that a port of that type does not have a BSR input cell associated with it. Therefore, either delete this reference to a non-existent BSR input cell or correct the reference to an existing BSR cell by correcting *output_port_name*.

(See UIT-138)

UIT-132 (error) JTAG Port '%s' is not an output or bidirectional port.

DESCRIPTION

Only output or bidirectional ports can take the */out* specifier. There are no output BSR cells associated with an input port. Thus, <*input_port_name*>*/out* is an illegal BSR cell identifier.

In *set_jtag_port_routing_order*, the *ordered_list_of_annotated_BSR_port_names* contains members of four classes:

- <*input_or_output_port_name*>, which specifies a BSR input or output cell (depending on the direction of the port),
- <*bidirectional_port_name*>*/in*, which specifies the BSR input cell associated with this bidirectional port,
- <*bidirectional_port_name*>*/out*, which specifies the BSR output cell associated with this bidirectional port, or
- <*tristate_or_bidirectional_port_name*>*/ctl*, which specifies the BSR three-state control cell associated with this output or bidirectional port.

Thus there are only three legal specifiers ('*/in*', '*/out*' or '*/ctl*') that can be appended to a *port_name* to identify a boundary scan register (BSR) cell. Each of these specifiers can only be associated with a subset of the port types (input, two-state output, three-state output and bidirectional ports) that can be included in the BSR.

DFT Compiler generates this message if you associate a non-existent boundary scan register (BSR) cell type ('*/in*', '*/out*' or '*/ctl*') with a port. DFT Compiler also generates UIT-138, which identifies the nature of the problem.

WHAT NEXT

An illegal specifier for *input_port_name* indicates that a port of that type does not have a BSR output cell associated with it. Therefore, either delete this reference to a non-existent BSR output cell or correct the reference to an existing BSR cell by correcting *input_port_name*.

(See UIT-138)

UIT-133 (error) JTAG Port '%s' is not three-stated.

DESCRIPTION

Only three-state ports can take the */ctl* specifier. There are no control BSR cells associated with an input or a two-state output port. Thus, <*two_state_input_or_output_port_name*>*/ctl* is an illegal BSR cell identifier.

In *set_jtag_port_routing_order*, the *ordered_list_of_annotated_BSR_port_names* contains members of four classes:

- <*input_or_output_port_name*>, which specifies a BSR input or output cell (depending on the direction of the port),
- <*bidirectional_port_name*>*/in*, which specifies the BSR input cell associated with this bidirectional port,
- <*bidirectional_port_name*>*/out*, which specifies the BSR output cell associated with this bidirectional port, or
- <*tristate_or_bidirectional_port_name*>*/ctl*, which specifies the BSR three-state control cell associated with this output or bidirectional port.

Thus there are only three legal specifiers ('*/in*', '*/out*' or '*/ctl*') that can be appended to a *port_name* to identify a boundary scan register (BSR) cell. Each of these specifiers can only be associated with a subset of the port types (input, two-state output, three-state output and bidirectional ports) that can be included in the BSR.

NOTE that even when a port is in fact three-stated, if the three-state is not visible at the top level of the core hierarchy, this error message may be generated and must be resolved. DFT Compiler determines whether a port is three-stated by checking for three-states at the top level of hierarchy. If it does not find them there, it assumes that the port is not three-stated and issues this error message when an operation requiring a three-stated port is invoked.

WHAT NEXT

An illegal specifier for *two_state_port_name* indicates that a port of that type does not have a BSR control cell associated with it. Therefore, either delete this reference to a non-existent BSR control cell or correct the reference to an existing BSR cell by attaching the **/ctl** specifier to the correct *three-state_or_bidirectional_port_name*.

If the offending port is in fact three-stated, you must regroup your core logic so that the three-state controlling this port is visible at the top level.

(See UIT-138)

UIT-134 (error) Insufficient information included with user-specified instruction '%s'. You must include either a register name or both reg_coordinate(s) and reg_enable specifications.

DESCRIPTION

Each JTAG instruction activates a single target data register. The target register of a user-defined instruction is (by definition) not specified in the IEEE 1149.1 JTAG Standard. Therefore that target register cannot be inferred by DFT Compiler, and you must identify it by using either *-reg_name core_scan_chain_name* or *-reg_coordinates capture_pin* [*load_pin*] and *-reg-enable enable_pin*.

This message is also generated if you only partially identify the data register by using only one of the two options *-reg_coordinates capture_pin* [*load_pin*] or *-reg-enable enable_pin*. For complete identification of the target data register, you must specify both.

WHAT NEXT

Determine what information is missing and supply it.

If you want to specify an instruction and (optionally) the code for a specific internal scan chain, execute *set_jtag_instruction instruction_name -reg_name name* [*-code code*].

The *name* of each internal scan chain is the name of its parallel scan-in port; that is, the port which has the *test_scan_in* attribute assigned to it. This guarantees the uniqueness of names for these scan chains and provides DFT Compiler with a mechanism to identify each target scan chain.

If you want to specify some other core test structure, identify it by using *-reg_coordinates capture_pin* [*load_pin*] and *-reg-enable enable_pin*.

[See UIT-92]

UIT-135 (error) Instruction '%s' has illegal JTAG instruction code string '%s'. (The code string must contain only '0's and '1's.)

DESCRIPTION

JTAG instruction codes are loaded 'as is' into the JTAG Instruction register. Therefore, they must be fully specified binary codes. Code cubes (which include 'dont care' X bits) are not allowed. The only characters permitted in these code

strings are ’0’s and ’1’s.

WHAT NEXT

Re-write the instruction code string using only ’0’s and ’1’s.

UIT-136 (error) Incompatible arguments. Specify either a register name or both register coordinate(s) and register enable.

DESCRIPTION

Each JTAG instruction activates a single target data register. The target register of a user-defined instruction is (by definition) not specified in the IEEE 1149.1 JTAG Standard. Therefore that target register cannot be inferred by DFT Compiler, and you must identify it by using either *-reg_name core_scan_chain_name* or *-reg_coordinates capture_pin* [*load_pin*] and *-reg-enable enable_pin*.

Specifying both *-reg_name core_scan_chain_name* and *-reg_coordinates capture_pin* [*load_pin*] or *-reg-enable enable_pin* is not supported and generates this error message.

WHAT NEXT

If you want to specify an instruction and (optionally) the code for a specific internal scan chain, execute *set_jtag_instruction instruction_name -reg_name name* [*-code code*].

The *name* of each internal scan chain is the name of its parallel scan-in port; that is, the port which has the *test_scan_in* attribute assigned to it. This guarantees the uniqueness of names for these scan chains and provides DFT Compiler with a mechanism to identify each target scan chain.

If you want to specify some other core test structure, identify it by using *-reg_coordinates capture_pin* [*load_pin*] and *-reg-enable enable_pin*.

UIT-137 (error) Instruction Register (IR) must be between 2 and 32 bits wide.

DESCRIPTION

The IEEE 1149.1 JTAG Standard mandates that the JTAG Instruction Register (IR) be at least two bits wide. DFT Compiler supports IRs of between 2 and 32 bits inclusively. There are three ways to set the size of the IR:

- You specify the size using *insert_jtag -ir_size bit_width*,
- You force the IR size by specifying an instruction code *set_jtag_instruction -code "code"*, or
- DFT Compiler automatically infers the IR size from the set of specified and mandatory instructions selected.

POSSIBLE CAUSES

This error occurs if you have *not* surrounded your specified code in quotes (" "). In the absence of quotes, the command line parser interprets the first character as an independent string and assumes that a 1-bit code has been specified, forcing a 1-bit IR.

WHAT NEXT

Specify an IR width between 2 and 32 bits. If you forgot the quotes in your *set_jtag_instruction* command, re-issue the command with quotes around the code.

UIT-138 (error) Non-existent BSR '%s' cell with routing position '%d' associated with port '%s'.

DESCRIPTION

In *set_jtag_port_routing_order*, the *ordered_list_of_annotated_BSR_port_names* contains members of four classes:

- *<input_or_output_port_name>*, which specifies a BSR input or output cell (depending on the direction of the port),
- *<bidirectional_port_name>/in*, which specifies the BSR input cell associated with this bidirectional port,
- *<bidirectional_port_name>/out*, which specifies the BSR output cell associated with this bidirectional port, or
- *<tristate_or_bidirectional_port_name>/ctl*, which specifies the BSR three-state control cell associated with this output or bidirectional port.

Thus there are only three legal specifiers ('*/in*', '*/out*' or '*/ctl*') that can be appended to a *port_name* to identify a boundary scan register (BSR) cell. Each of these specifiers can only be associated with a subset of the port types (input, two-state output, three-state output and bidirectional ports) that can be included in the BSR.

DFT Compiler generates this message if you associate a non-existent boundary scan register (BSR) cell type (‘*/in*’, ‘*/out*’ or ‘*/ctl*’) with a port. DFT Compiler also generates a message (UIT-131, UIT-132 or UIT-133) that tells you why the specifier you used is illegal.

WHAT NEXT

An illegal specifier for a port indicates that that type of port does not have that type of BSR cell associated with it. Therefore, either delete this reference to a non-existent BSR cell or correct the reference to an existing BSR cell by correcting the associated *port_name*.

(See UIT-131, UIT-132 or UIT-133)

UIT-139 (error) -no_internal_scan invoked but instruction ’%s’ specifies core scan chain ’%s’.

DESCRIPTION

If you want to specify an instruction and (optionally) the code for a specific internal scan chain, execute *set_jtag_instruction instruction_name -reg_name name* [*-code code*].

The *name* of each internal scan chain is the name of its parallel scan-in port; that is, the port which has the *test_scan_in* attribute assigned to it. This guarantees the uniqueness of names for these scan chains and provides DFT Compiler with a mechanism for identifying each target scan chain.

By default DFT Compiler will attach core test structures that it recognizes (e.g. internal scan chains) to the JTAG Test Access Port (TAP). Internal scan chains will *not* be connected to the TAP if you execute *insert_jtag -no_internal_scan*.

DFT Compiler generates this error message if *-no_internal_scan* has been invoked, but you have explicitly specified a JTAG instruction for one of the internal scan chains using *set_jtag_instruction instruction_name -reg_name name* [*-code code*].

WHAT NEXT

Resolve the conflict. If you want to cancel the scan chain instruction, execute *set_jtag_instruction instruction_name -cancel*. Otherwise invoke *insert_jtag* without *-no_internal_scan*.

UIT-140 (warning) The DFT Compiler specific JTAG instruction ’%s’ does not support register name or coordinate specification.

Specifications ignored.

DESCRIPTION

It is meaningless to specify *-reg_name*, *-reg_coordinates*, or *-reg_enable* with the *DAISY_CORE_SCAN* instruction. Doing so results in this error message.

The *DAISY_CORE_SCAN* instruction selects a single scan chain made up of all internal scan chains daisy-chained together. To assign a specific code to this instruction, issue the command *set_jtag_instruction DAISY_CORE_SCAN -code code*. This is equivalent to executing *insert_jtag -daisy_chained*, so you do not need to invoke *-daisy_chained* explicitly, UNLESS you want to specify the routing order of the serially daisy-chained scan chains.

WHAT NEXT

Re-invoke *set_jtag_instruction DAISY_CORE_SCAN -code code* without the *-reg_name*, *-reg_coordinates*, and/or *-reg_enable* specifications.

UIT-141 (error) Bad model scale factor, must be positive.

DESCRIPTION

For the command, set_model_scale, the scale value must be positive. You have entered a zero or negative number.

WHAT NEXT

Reenter the command with a positive scale factor.

UIT-142 (error) Bad model load value, should not be negative.

DESCRIPTION

For the command, set_model_load, the load value cannot be negative. You have entered a negative number.

WHAT NEXT

Reenter the command with a non-negative load value.

UIT-143 (error) Bad model drive value, should not be negative.

DESCRIPTION

For the command, set_model_drive, the drive value cannot be negative. You have entered a negative number.

WHAT NEXT

Reenter the command with a non-negative drive value.

UIT-144 (warning) Port '%s/%s' is not an input or inout port; model_drive not set.

DESCRIPTION

The *set_model_drive* command works only on input or inout ports.

WHAT NEXT

Examine the design to determine the correct ports for the command.

UIT-145 (error) Erroneous specification of a list of ports since set_jtag_implementation has not been invoked with a Boundary Scan Register (BSR) component.

DESCRIPTION

set_jtag_implementation only supports a **list_of_ports** when invoked with Boundary Scan Register (BSR) components (**BSRin**, **BSRout** or **BSRcontrol**), associating a JTAG component implementation of a BSR cell with specific ports in the BSR. A port list is meaningless with respect to the JTAG TAP controller, Bypass Register, Instruction Register or device Identification Register.

WHAT NEXT

Resolve the inconsistency either by removing the list_of_ports, or by specifying a BSR cell component.

UIT-146 (error) Three-state cell ‘%s‘ (technology library cell ‘%s‘) is dont_touch.

DESCRIPTION

For successful JTAG synthesis, DFT Compiler requires that all three-state devices associated with circuit I/O be at the top level of the design. When DFT Compiler inserts boundary scan cells for three-state ports into the design, it determines their location by locating the data and control inputs to the associated generic three-state devices. In order to translate a three-state device into its generic equivalent, the original three-state device must *not* have its **dont_touch** attribute set **TRUE**. If it is ‘ set **TRUE**, this error message is generated.

There are two ways that a device can have its **dont_touch** attribute set **TRUE**; the user can explicitly set the attribute, or the technology library cell with which the device is implemented may specify that the device should not be touched.

WHAT NEXT

Remove the **dont_touch** attribute associated with the offending three-state device.

UIT-147 (error) Invalid sample percentage value ’%d’.

DESCRIPTION

The **-sample** option of the command **create_test_patterns** specifies the percentage of faults to be considered for test generation.

WHAT NEXT

The value of this option should be in the 0-100 range.

UIT-149 (Information) The set_jtag_part_number command is overriding the environmental variable "jtag_part_number" value ‘%d’ by ‘%d’.

DESCRIPTION

It is possible to specify the value of the 16-bit binary part number field of the JTAG ID register in two ways: using the **set_jtag_part_number** command or using the

environmental variable *jtag_part_number*. This message indicates that the value set by *set_jtag_part_number* is overriding the default value set by **jtag_part_number**.

WHAT NEXT

Using environmental variables for those JTAG synthesis constraints that rarely change in your synthesis environment reduces the number of explicit JTAG synthesis commands you must invoke.

UIT-150 (Information) The set_jtag_manufacturer_id command is overriding the environmental variable "jtag_manufacturer_id_number" value ‘%d’ by ‘%d’.

DESCRIPTION

There are two ways to specify the value of the 11-bit binary manufacturer ID field of the JTAG ID register: by using the **set_jtag_manufacturer_id** command, or by using the environmental variable **jtag_manufacturer_id_number**. This message indicates that the default value set by the latter is being overridden by the value specified by the former.

WHAT NEXT

To reduce the number of explicit JTAG synthesis commands you must invoke, use environmental variables for those JTAG synthesis constraints that rarely change in your synthesis environment.

UIT-151 (Information) The set_jtag_version_number command is overriding the environmental variable "jtag_version_number" value ‘%d’ by ‘%d’.

DESCRIPTION

There are two ways to define the value of the 4-bit binary version number field of the JTAG ID register: by using the **set_jtag_version_number** command, or by using the environmental variable **jtag_version_number**. This message indicates that the default value set by the latter is being overridden by the value defined by the former.

WHAT NEXT

To reduce the number of explicit JTAG synthesis commands you must invoke, use environmental variables for those JTAG synthesis constraints that rarely change in your synthesis environment.

UIT-152a (warning) The '%s' command is ignored. Either a '%s' license or '%s' license is required for this command.

DESCRIPTION

You receive this warning message as a result of the **write_test** command. To run this command, you must have either the Test-Compiler license or the Test-IEEE-Std-1149-1 license.

WHAT NEXT

Verify that your installation is correct and that you are authorized for this license feature. If you are not authorized for this feature, contact Synopsys.

SEE ALSO

write_test (2).

UIT-152 (warning) The '%s' command is ignored. A '%s' license is required for this command.

DESCRIPTION

Some dc_shell commands require specific licenses. This error may occur when the required feature is not authorized.

WHAT NEXT

Make sure your installation is correct and that you are supposed to be authorized for this license feature.

UIT-153 (error) The sum of strobe time (%10.2f) and strobe width value (%10.2f) is required to be less than period value

(%10.2f).

DESCRIPTION

You have specified a strobe time and strobe width value such that the end of the strobe period stretches beyond the period.

WHAT NEXT

Check your strobe time specifications.

UIT-154 (error) Unable to fault-simulate vectors because %s.

DESCRIPTION

The current vectors could not be fault-simulated, either because the the test protocol is not parallel-loadable, or because the **vdb** file was not created by a v3.1 or later version of ATPG.

During fault simulation of **vdb** files, scan operations are performed in a parallel-load fashion. Thus, fault simulation of **vdb** files is restricted to parallel-loadable protocols only. Currently, custom test protocols are NOT parallel-loadable. Initialization protocols read with the **read_init_protocol** command are acceptable.

Only **vdb** files written by v3.1 (or later) ATPG can be directly fault- simulated by TestSim; **vdb** files written by TestSim itself cannot be directly fault-simulated by TestSim.

WHAT NEXT

If you have a **vdb** file with vectors that are not parallel-loadable, you can use the **write_test** command to write these vectors out into a *tds* or a *wgl* vector format and then fault-simulate that *tds* or *wgl* file. The *wgl* format is preferable because its vector file is usually smaller in size. Note, however, that if you simulate a scan vector set in a serial format such as *tds* or *wgl*, then fault simulation of scan operations will be serial and therefore considerably slower.

If you got this message because your **vdb** file was created by a previous release version of ATPG, then you will need to create a new **vdb** file or write out the vectors to *tds* or *wgl* as suggested above.

UIT-155 (error) write_test could not find the intermediate (SIF)

file to be formatted.

DESCRIPTION

Write_test formatter executable could not find the required input file (SIF file) to be formatted. The file may be deleted accidentally from the directory where this program is being run or it may not have been created due to errors such as not enough disc space to write vector file, occuring during write_test.

WHAT NEXT

Re-run write_test after ensuring that you have enough disk space

UIT-156 (error) write_test failed to open temporary file to be used during vector formatting.

DESCRIPTION

Write_test could not open temporary file(s) needed during the vector formatting process. This may be caused by lack of write permission to the directory, or failure due to insufficient disc space to write the file(s).

WHAT NEXT

Make sure that sure that there is sufficient disc space, and that all the right permissions are set.

UIT-157 (error) Insufficient memory, write_test failed to format vectors.

DESCRIPTION

Write_test ran out of run-time memory during vector formatting.

WHAT NEXT

Ensure that sufficient memory is available.

UIT-158 (error) internal error, write_test formatter executable

(stran) failed due to syntax error in input (SIF) file.

DESCRIPTION

The write_test formatter failed due to syntax error in the intermediate (SIF) file used as its input. The file may have been corrupted, incompletely generated (e.g. due to insufficient disc space) or have been manually tampered with

WHAT NEXT

Re-invoke write_test and notice any error and warning messages issued. Report any relevant messages to Synopsys.

UIT-159 (error) internal error, unexpected end-of-file found in input file to the write_test formatter executable (stran).

DESCRIPTION

The write_test formatter failed due to unexpected end-of-file found in the intermediate (SIF) file used as its input. The file may have been corrupted, incompletely generated (e.g. due to insufficient disc space) or have been manually tampered with

WHAT NEXT

Ensure that sufficient disc space is available, and that the write_test command does not issue any error messages.

UIT-160 (error) Unsupported vector format '%s' specified in the -format option.

DESCRIPTION

The vector format specified in the *-format* option of the **fault_simulate** command is not supported. Use one of the supported formats. The formats currently supported for the **fault_simulate** command are "sif", "tds", "vdb", "wgl", and "wif".

For the **prepare_testsim_vectors** command, all except the "vdb" format are supported. If you are using the "vdb" format, input this directly to the **fault_simulate** command without going through the **prepare_testsim_vectors** command.

WHAT NEXT

Use one of the supported vector formats.

UIT-163 (error) JTAG Port '%s' is not an input port.

DESCRIPTION

Only input ports can take the *clock* specifier. The JTAG circuitry associated with an *input* port can be optimized based on the signal type (**clock** or **data**) of that port. Ports that drive clock trees can be associated with specialized JTAG circuitry. An input port can be explicitly identified as carrying one of the "clock" or "data" categories.

DFT Compiler generates this message if you attempt to assign an output or bidirectional port the *clock* specifier.

The only legal output port specifiers are *enable* or *data*. (See error message UIT-164.)

WHAT NEXT

Remove all output ports from the list of ports receiving the *clock* specifier. If you are trying to specify the type of an output port, select between *enable* or *data*.

UIT-164 (error) JTAG Port '%s' is not a two-state output port.

DESCRIPTION

Only two-state output ports can take the *enable* specifier.

When the three-state elements driving three-state and bidirectional *outputs* are found in the core logic of the IC (i.e. not embedded in the pads themselves) DFT Compiler requires that these three-state elements be located at the top hierarchy of the core of the design so that Boundary Scan Register (BSR) cells can be placed on the **inside** of the three-state elements in order to control and observe the data and enable lines. In these cases, only a single three-state line exits the core logic.

However, in the cases where the three-state controller for output signals will be embedded in the three-state output or bidirectional input/ouput pad associated with these ports of a design a pair of two state signals exit the core logic; a *data* line and a *enable* line. (It does not make sense for one of these ports to be a bidirectional port.) Unless, TC knows the distinction between these two types of exit lines, it will always assume that they are data lines and not insert the correct type of BSR cell on the enable lines. By specifying "enable" or "data" on a port the designer instructs TC on which type of BSR cell to place on these output ports.

DFT Compiler generates this message if you attempt to assign an input or bidirectional port the *enable* specifier, or if you have assigned the *enable* specifier to a three-state output.

The only legal input port specifiers are *clock* or *data*. (See error message UIT-163.)

WHAT NEXT

Remove all input ports from the list of ports receiving the *enable* specifier. If you are trying to specify the type of an input port, select between *clock* or *data*.

UIT-165 (error) %s time (%10.2f) must be less than strobe time (%10.2f).

DESCRIPTION

Data application time/delay must happen before strobe time

WHAT NEXT

Change strobe time, and/or delay or bidirectional delay time such that data application time happens before strobe time, and rerun create_test_protocol. To set the strobe time use the test_default_strobe variable, and to set the bidirectional delay time use the test_default_bidir_delay variable.

UIT-167 (error) Test program '%s' does not match the design '%s'.

.

DESCRIPTION

This message indicates that the test program does not match the design. The design has probably been changed since the test program was written.

WHAT NEXT

If you need to use this test program, you must change the design back to what it was when the test program was written out. Otherwise, the test program cannot be used and a new one will have to be generated.

UIT-168 (error) Test program '%s' does not match the design

’%s’. Could not get value for port ’%s’ in test program. This port is present in the design.

DESCRIPTION

This message indicates that the test program does not match the design. The design has probably been changed since the test program was written.

WHAT NEXT

If you need to use this test program, you must change the design back to what it was when the test program was written out. Otherwise, the test program cannot be used and a new one will have to be generated.

UIT-169 (Error) No port has been specified.

DESCRIPTION

The set_dft_signal command allows design objects to specify ports. The port specicification is mandatory.

WHAT NEXT

Specify a port with the -port option and re-issue the command

UIT-170 (error) Value ’%s’ is not supported for the clock_gating option.
Use either ’entire_design’ or ’leaf_cell’ as values.

DESCRIPTION

The *clock_gating* option currently supports the options *entire_design* and *leaf_cell*.

The default behavior if the *clock_gating* option is not specified is to do entire design clock gating.

WHAT NEXT

Specify either *entire_design* and *leaf_cell* as values for the *clock_gating* option.

UIT-171 (error) The test program sequence contained in the test program '%s' does not match the expected test program sequence.

DESCRIPTION

The test program sequence information contained in the test program specified in this error message is incorrect. It does not match the test program sequence information that was expected. The expected test program sequence information was based on the information in the test program that was input to this 'write_test' command.

This will happen when the original vdb file for the test program specified in this error message was overwritten by a later fault processor run.

When you lose or corrupt a vdb file for a test program, all test programs which depended on this test program (i.e. all test programs which were after it in the same sequence) are also invalidated.

WHAT NEXT

Recreate the test program which is in error. You may have to also regenerate all test programs in the sequence following this test program.

UIT-172 (information) Formatting of test vectors was successful for test program '%s'.

DESCRIPTION

You receive this message when you use the **-cummulative** option in a multi-pass test (**multi_pass_test_generation** set to *true*) after **write_test** successfully formats each test program.

WHAT NEXT

No action is required on your part.

UIT-173 (warning) Formatting of test vectors failed for test

program '%s'.

DESCRIPTION

This message indicates that a serious error occured while **write_test** was processing your patterns. **write_test** has failed to save your patterns in the format you requested. Earlier messages will give you details of the specific problems encountered by **write_test**.

WHAT NEXT

Review previous error messages in the transcript and take the appropriate action based on those messages. See the man pages for the previous messages if you need more details on what action to take.

UIT-174 (warning) You cannot use the -output option with the -cumulative option.
The -output option will be ignored.

DESCRIPTION

You receive this message when you attempt to use both the **-cummulative** and **-output** options in a multi-pass test (**multi_pass_test_generation** set to *true*). You cannot set both options because when you use the **-cummulative** option, you are writing out more than one file. The **-output** option specifies only one filename.

The **write_test** command ignores the **-output** option and will write out more than one file.

WHAT NEXT

To avoid this violation, change your script so you do not use the **-cummulative** and **-output** options simultaneously.

If you wish to format your patterns into a single file, you must use single pass test generation.

SEE ALSO

create_test_patterns (2), **write_test** (2).

UIT-177 (warning) You cannot use the -all option as well as

specify the object list with the set_test_unmask_fault command. The -all option wins. All faults in the entire design will be unmasked.

DESCRIPTION

You receive this message if specify both an object list and the **-all** option for the **set_test_unmask_fault** command. For example:

```
dc_shell> set_test_unmask_fault U1 -all
```

Object list and the **-all** option are mutually exclusive. The message warns you that the **set_test_unmask_fault** command has honored the **-all** option and ignored object list.

WHAT NEXT

If you intend to unmask all faults, no action is required on your part. However, you can prevent future occurences of this error message by removing the object list.

If you intended to unmask only those faults specified by the object list, you need to re-establish fault masking on the faults you wish to mask. Use the **set_test_mask_fault** command to do this. Or, if you are using a script, you can correct and rerun the script.

UIT-178 (error) You must either use the -all option or specify the object list with the set_test_unmask_fault command.

DESCRIPTION

You receive this message if you do not specify either an object list or the **-all** option. The following command will result in this error message:

```
dc_shell> set_test_unmask_fault -sa1
```

You must specify either the **-all** option or an object list to identify which masked faults you wish to unmask.

WHAT NEXT

Issue the **set_test_unmask_fault** command with either an object list or the **-all** option specified.

UIT-184 (error) JTAG instruction '%s' not yet declared, so it cannot be cancelled.

DESCRIPTION

An instruction may not be deleted from the specification of the Boundary Scan Instruction Register instruction set, if it has not previously been added to that set.

In other words, *set_jtag_instruction <instruction_name> -cancel* may not be invoked if *set_jtag_instruction <instruction_name> has not been previously invoked.*

WHAT NEXT

Remove this call to cancel the instruction from your script as it is effects no useful operation.

UIT-186 (error) Illegal IDDQ fault model '%s'. Choose between 'shorts' and 'toggle'.

DESCRIPTION

The IDDQ fault model specified in the **-fault_model_iddq** option of the **fault_simulate** command is not supported. The IDDQ fault models currently supported are *shorts*, which targets transistor shorts and models 6 shorts per transistor; and *toggle*, which targets node toggle coverage.

WHAT NEXT

Reissue **fault_simulate** and specify either of the valid fault models *shorts* or *toggle* for the **-fault_model_iddq** option.

UIT-189 (error) Can't write output vdb file '%s'.

DESCRIPTION

This message indicates that the output **vdb** file cannot be written, because a file of the same name already exists and is protected from being overwritten.

WHAT NEXT

Use a different name for the output test program, or remove the write protection

from the existing **vdb** file so that it can be overwritten. Then re-execute.

UIT-191 (error) '%s' is not a known clock domain restriction.

DESCRIPTION

The set_scan_configuration command accepts a clock_domains option. This tells DFT Compiler how to define clock domains. Option arguments must be known restrictions.

WHAT NEXT

Replace the option argument with a known restriction, for example "no_mix", "mix_edges", or "mix_clocks".

UIT-192 (error) '%s' is not a known clock gating technique.

DESCRIPTION

The set_scan_configuration command accepts a clock_gating option. When a partial scan methodology and a multiplexed flip flop scan style is chosen, this tells DFT Compiler what technique to use to gate the clocks connected to non-scan cells. Option arguments must be known techniques.

WHAT NEXT

Replace the option argument with a known technique, for example "entire_design", "superbuffer", or "leaf_cell".

UIT-193 (error) Can not insert '%s' scan chains.

DESCRIPTION

The set_scan_configuration command accepts a chain_count option. This tells DFT Compiler the number of scan chains to implement in the testable design. Option arguments must be positive integers or "default" strings.

WHAT NEXT

Repeat the set_scan_configuration command using a positive integer or the string "default".

UIT-194 (error) '%s' is not a known bidirectional mode.

DESCRIPTION

The set_scan_configuration command accepts a dedicated_scan_ports option. This tells DFT Compiler whether to turn bidirectional ports inwards or outwards during scan. Arguments specified must be known bidirectional modes.

WHAT NEXT

Replace the option argument with a known bidirectional mode, for example "input" or "output".

UIT-195 (warning) Arguments override the default script file name, but do not ask for a script. None is generated.

DESCRIPTION

You receive this message because you are overriding a default script file name, but have not asked for a script file.

When you use **preview_scan** command with the **-script** option, DFT Compiler generates a script that completely specifies the scan design. If you do not specify the **-script** option, no script is generated.

The script file has a default name that you can override by specifying a script file name.

WHAT NEXT

Specify the **preview_scan** command with the **-script** option, if you want a script file. Otherwise, ignore the warning, or do request the script file name.

SEE ALSO

preview_scan (2).

UIT-196 (warning) '%s' is a %s and can not be used to specify a

scan signal port.

DESCRIPTION

The set_scan_signal command allows design objects to specify ports. These must be ports. Other kinds of design objects cannot be used to specify scan signal ports, and are rejected.

WHAT NEXT

Remove the object from the argument list to get rid of the warning. Use hierarchical instance names, with respect to the top-level design, to locate design objects.

UIT-197 (warning) '%s' is a %s and can not be used to specify a scan signal pin.

DESCRIPTION

The set_scan_signal command allows design objects to specify pins. These must be pins or pin instances. Other kinds of design objects cannot be used to specify scan signal ports, and are rejected.

WHAT NEXT

Remove the object from the argument list to get rid of the warning. Use hierarchical instance names, with respect to the top-level design, to locate design objects.

UIT-198 (error) '%s' is not a scan signal type.

DESCRIPTION

The **set_scan_signal** command lets you associate scan signal semantics with design ports. Specified signal types must be scan signal types in test_scan_enable, test_scan_enable_inverted, test_scan_clock, test_scan_clock_a, test_scan_clock_b, test_clock, test_scan_in, and test_scan_out. Other signal types do not have scan signal semantics and are rejected.

WHAT NEXT

Repeat the **set_scan_signal** command using a scan signal type.

UIT-199 (error) ’%s’ is not a signal type for the ’%s’ scan style.

DESCRIPTION

The set_scan_signal command lets you associate scan signal semantics with design ports. Specified signal types must be consistent with the specified scan style. Other signal types do not have scan signal semantics in the specified scan style and are rejected.

WHAT NEXT

Repeat the set_scan_signal command using a scan signal type that has meaning in the specified scan style.

UIT-200 (warning) %s port ’%s’ can not be a %s.

DESCRIPTION

You can use the **set_scan_signal** command to put associated scan semantics with design ports. This warning is generated when you try to set the signal type of a port to something that is inconsistent with its direction. For example, signal type test_scan_out is associated with scan chain outputs. It cannot be associated with an input port.

WHAT NEXT

Repeat the command using the correct port.

UIT-201 (warning) did not complete set_signal_type. ’%s’ is a %s, not a design port.

DESCRIPTION

You can use the set_signal_type command to put test-specific signal types on design ports. This warning is generated when you try to set the signal type of an object that is not a design port.

WHAT NEXT

Repeat the command using the correct port name.

UIT-202 (warning) did not complete set_signal_type. %s port '%s' can not be a %s.

DESCRIPTION

You can use the set_signal_type command to put test-specific signal types on design ports. This warning is generated when you try to set the signal type of a port to something that is inconsistent with its direction. For example, signal type test_scan_out is associated with scan chain outputs. It cannot be associated with an in port.

WHAT NEXT

Repeat the command using the correct port.

UIT-203 (warning) %s pin '%s' can not be a %s.

DESCRIPTION

You can use the set_scan_signal command to specify hookup pins for design ports that have scan semantics. This warning is generated when you try to set the hookup pin for a port to something that is inconsistent with its direction. For example, ports with signal type test_scan_out should be associated with output pins. They cannot be associated with input pins.

WHAT NEXT

Repeat the command using the correct hookup pin.

UIT-204 (error) There is no valid scan port.

DESCRIPTION

You use the set_scan_signal command to associate scan signal semantics with design ports. You see this error when nothing you specify is a valid design port.

WHAT NEXT

Study accompanying messages for the reasons why specified ports were not acceptable, and repeat the command using valid ports.

UIT-205 (error) No specified hookup pin is valid.

DESCRIPTION

You can use the set_scan_signal command to associate hookup pins with scan signal ports. You see this error when nothing you specify is a valid design pin.

WHAT NEXT

Study accompanying messages for the reasons why the specified access pins were not acceptable. Repeat the command using valid pin instances.

UIT-206 (warning) %d scan ports have been specified. Only the first will be processed.

DESCRIPTION

You use the set_scan_signal command to associate scan signal semantics with design ports. You see this error when you try to specify the signal type of multiple design ports using the same command. To simplify commands and eliminate ambiguity, separate commands must be used.

WHAT NEXT

Split outstanding scan port specifications among multiple commands.

UIT-207 (warning) %d hookup pins have been specified. Only the first will be processed.

DESCRIPTION

You can use the set_scan_signal command to associate hookup pins with scan signal ports. You see this warning when you try to associate more than one hookup pin with a design port. Only one can be specified.

WHAT NEXT

If you want another hookup pin to be used, repeat the command specifying only that pin.

UIT-208 (warning) There is no scan chain called '%s'. Specification is ignored.

DESCRIPTION

You can use the set_scan_signal command to associate scan chains with scan signals. You see this warning when you try to associate a non-existent chain with a scan signal. Chains must already have been specified using set_scan_path command.

WHAT NEXT

Correct the chain name, if you've made a mistake, or specify the chain using the set_scan_path command before repeating the specification.

UIT-209 (warning) %d scan ports have been specified, but access pins or scan chains have been specified also. Only the first scan port will be processed.

DESCRIPTION

You use the set_scan_signal command to associate scan signal semantics with design ports. You see this error when you try to specify the signal type of multiple design ports, and associate access pins of scan chains with them, using the same command. To simplify commands and eliminate ambiguity, separate commands should be used.

WHAT NEXT

Split outstanding scan port specifications among multiple commands.

UIT-210 (error) '%s' is not a known scan link type.

DESCRIPTION

Use the set_scan_link command to declare scan links for the current design. Known scan link types include "wire" and "scan_out_lockup". You see this error when you specify an unknown scan link type.

WHAT NEXT

Repeat the specification using a known scan link type.

UIT-211 (warning) '%s' is not a scan signal type. Discarding specified access point.

DESCRIPTION

The set_scan_segment command lets you specify access points with scan signal semantics. Specified signal types must be scan signal types in testdb_scan_enable, testdb_scan_enable_inverted, testdb_scan_clock, testdb_scan_clock_a, testdb_scan_clock_b, testdb_clock, testdb_scan_in, and testdb_scan_out. Other signal types do not have scan signal semantics and are rejected.

WHAT NEXT

Repeat the set_scan_segment command using a scan signal type.

UIT-212 (warning) '%s' does not identify a design pin. Discarding specified access point.

DESCRIPTION

The set_scan_segment command lets you specify access points with scan signal semantics. Specified access points must identify design pins. Other kinds of design objects cannot be used to specify access points, and are rejected.

WHAT NEXT

Remove the object from the argument list to get rid of the warning. Use hierarchical instance names, with respect to the top-level design, to locate design objects.

UIT-213 (warning) Access point specification is not paired. Last specification is incomplete and is discarded.

DESCRIPTION

The set_scan_segment command lets you specify access points with scan signal semantics. Specified access points must be pairs, where each pair includes a signal type and a design port or pin. Incomplete pairs cannot be used to specify access points, and are rejected.

WHAT NEXT

Remove the last object from the argument list to get rid of the warning.

UIT-214 (error) Link name '%s' identifies a design cell. Link specification creates ambiguity and is discarded.

DESCRIPTION

The set_scan_link command lets you define scan links. Specified link names cannot identify design cells. Otherwise future scan chain specifications would be ambiguous.

WHAT NEXT

Rename the scan link.

UIT-215 (error) Segment name '%s' identifies a design cell. Specification creates ambiguity and is discarded.

DESCRIPTION

The set_scan_segment command lets you define scan segments. Specified segment names cannot identify design cells. Otherwise future scan chain specifications would be ambiguous.

WHAT NEXT

Rename the scan segment.

UIT-216 (warning) %s pin '%s' can not be a %s.

DESCRIPTION

You can use the set_scan_segment command to specify access pins for scan segment using scan semantics. This warning is generated when you try to set the access point for a segment to something that is inconsistent with its direction. For example, ports with signal type test_scan_out should be associated with output pins. They cannot be associated with input pins.

WHAT NEXT

Repeat the command using the correct access pin or signal type.

UIT-217 (error) '%s' is not a signal type for the '%s' scan style.

DESCRIPTION

The set_scan_segment command lets you associate scan signal semantics with design ports and pins. Specified signal types must be consistent with the specified scan style. Other signal types do not have scan signal semantics in the specified scan style and are rejected.

WHAT NEXT

Repeat the set_scan_signal command using a scan signal type that has meaning in the specified scan style.

UIT-218 (warning) Segment access list has multiple hookup points for signal type '%s'. All but the first is discarded.

DESCRIPTION

The set_scan_segment command lets you associate scan signal semantics with design ports or pins. You can associate at most one hookup point with each signal type. This message tells you that you have tried to associate more than one hookup point with a signal type, and that DFT Compiler is discarding all but the first.

WHAT NEXT

Repeat the set_scan_segment command if you want to specify a different hookup point.

UIT-219 (warning) Segment access list has multiple signal types for hookup point '%s'. All but the first is discarded.

DESCRIPTION

The set_scan_segment command lets you associate scan signal semantics with design ports or pins. You can associate at most one signal type with each access point. This message tells you that you have tried to associate more than one signal type with an access point, and that DFT Compiler is discarding all but the first.

WHAT NEXT

Repeat the set_scan_segment command if you want to specify a different signal type.

UIT-220 (warning) Scan chain '%s' has scan style '%s' that differs from design scan style '%s'. Specification is ignored.

DESCRIPTION

You can use the set_scan_signal command to associate scan chains with scan signals. You see this warning when you try to associate a chain that you have specified under one scan style with a scan signal you specify under another. Chains must have been specified using the same scan style.

WHAT NEXT

Change the scan style and reapply the set_scan_signal command, or reapply your earlier set_scan_path command using the new scan style.

UIT-221 (warning) '%s' identifies multiple pins. Discarding specified access point.

DESCRIPTION

The **set_scan_segment** command lets you specify access points with scan signal semantics. Specified access points must identify one design pin. Wildcards cannot be used to specify access points, and are rejected.

WHAT NEXT

Remove the object from the argument list to get rid of the warning. Use hierarchical instance names, with respect to the top-level design, to locate design objects.

UIT-222 (warning) Segment '%s' does not have scan style '%s' and is not being added to the scan chain.

DESCRIPTION

The set_scan_path command accepts an ordered list of design objects. These must be cells, instances, links or segments. DFT Compiler does not support scan chains with

mixed scan styles. Segments must have the same scan style as the scan chain. You cannot add segments with other scan styles to a scan chain.

WHAT NEXT

If you really do want to add the segment to the chain, simply re-specify it using the same scan style as the chain.

UIT-223 (warning) '%s' is not a cell, instance, scan segment, or scan link, and is not being added to the scan chain.

DESCRIPTION

The set_scan_path command accepts an ordered list of design objects. These must be cells, instances, links or segments. Other kinds of design objects cannot be added to scan chains, and are rejected.

WHAT NEXT

Remove the object from the argument list to get rid of the warning. Use hierarchical instance names, with respect to the top-level design, to locate design objects.

UIT-224 (warning) write_test_max_scan_patterns value specified (%d) ignored.

DESCRIPTION

Illegal value specified for this variable: the value can not be a negative or a 1. The value specified is ignored.

WHAT NEXT

Use a value of greater than 1 for this variable

UIT-225 (warning) write_test_max_cycles value specified (%d)

ignored.

DESCRIPTION

Illegal value specified for this variable: the value can not be a negative. The value specified is ignored.

WHAT NEXT

Use a positive value for this variable

UIT-226 (warning) Scan chain element '%s' is a scan link and is not being added to the scan chain.

DESCRIPTION

The **set_scan_path** command accepts an ordered list of design objects. The first object in the list can not be a scan link because there is no preceding cell to associate it with.

WHAT NEXT

Remove the object from the argument list to get rid of the warning.

UIT-227 (warning) Scan style '%s' does not add lockup latches to the scan chain.
Ignoring the set_scan_configuration -add_lockup command.

DESCRIPTION

Only the multiplexed_flip_flop scan style adds lockup latches to the scan chain. This message tells you that you have asked DFT Compiler to add lockup latches to the scan chain, but have specified a scan style that is not multiplexed_flip_flop. DFT Compiler is telling you that it is ignoring your **-add_lockup** option.

WHAT NEXT

To get rid of the warning, remove the **-add_lockup true** from the **set_scan_configuration** option list, or set the scan style to multiplexed_flip_flop.

UIT-228 (warning) Ignoring preview_scan -show option argument '%s'.

DESCRIPTION

The **preview_scan** command has a **-show** option, that gives users the flexibility they need to customize what they see. The option takes a list argument, containing case-insensitive keywords in "cells", "scan", "segments", "scan_clocks", "scan_signals", and "all". This message says that you have used a **-show** option argument that is not a keyword. DFT Compiler ignores the specification.

WHAT NEXT

To get rid of the warning, remove the unknown keyword from the **preview_scan -show** option argument list.

UIT-229 (warning) Scan style '%s' does not need scan clock domain constraints. Ignoring the set_scan_configuration -clock_mixing command.

DESCRIPTION

Only the multiplexed_flip_flop scan style needs scan clock domain constraints. This message tells you that you have asked DFT Compiler to implement scan clock domain constraints, but have specified a scan style that is not multiplexed_flip_flop. DFT Compiler is telling you that it is ignoring your **-clock_mixing** option.

WHAT NEXT

To get rid of the warning, remove the **-clock_mixing** from the **set_scan_configuration** option list, or set the scan style to multiplexed_flip_flop.

UIT-230 (information) To support new scan insertion capabilities, this command is being replaced by the set_scan_path command, which is used with the insert_scan command. Please see the DFT Compiler Scan Synthesis User Guide for more information about set_scan_path and

insert_scan.

DESCRIPTION

To support new scan insertion capabilities, the **insert_test** command is being replaced by **insert_scan**.

The **set_scan_chain** command is not recognized by **insert_scan**. The **set_scan_path** command is used instead.

DFT Compiler continues to support **set_scan_chain** and **insert_test** for a transition period, so legacy **dc_shell** scripts continue to work.

We believe that **set_scan_path** and **insert_scan** supports all **set_scan_chain** and **insert_test** features, and ultimately intend obsoleting **set_scan_chain** and **insert_test**.

WHAT NEXT

See the DFT Compiler Scan Synthesis User Guide for more information about **set_scan_path**, **insert_scan**, and the hierarchical scan user interface. Let Synopsys know about any **set_scan_chain** or **insert_test** feature that you rely on, and is not supported by **set_scan_path** and **insert_scan**.

UIT-231 (Error) The options -chain and -cell cannot be specified at the same time.

DESCRIPTION

This message indicates that a report_scan_path command has been issued, but the two options -chain and -cell cannot be specified at the same time. You choose either to report the scan signal information for the scan chains with the -chain option or to report the cells of the scan chains with the -cell option.

WHAT NEXT

Remove one of the options (-chain or -cell) and reissue the command.

SEE ALSO

report_scan_path

UIT-232 (warning) Coverage threshold option ignored.

Coverage threshold must be greater than 0%%.

DESCRIPTION

The specified coverage threshold for fault_simulate was ignored because it was less than or equal to 0%.

WHAT NEXT

The coverage threshold must be greater than 0% and less than or equal to 100%.

UIT-233 (warning) Coverage threshold option ignored. Coverage threshold must be less than or equal to 100%%.

DESCRIPTION

The specified coverage threshold for fault_simulate was ignored because it was greater than 100%.

WHAT NEXT

The coverage threshold must be greater than 0% and less than or equal to 100%.

UIT-235 (error) cannot generate TSTL2 format, too many timing types.

DESCRIPTION

All the inputs with same delay are grouped into one input timing type. All the outputs with same delay (or strobe time) are grouped into one output timing type. TSTL2 format allows a maximum of seven (6 + 1 dedicated for DT waveform) types of input timing and two types of output timing. One TIMESET statement is generated for each timing type. Input to the write_test requires it to generate more than allowed TIMESET statements.

WHAT NEXT

To generate TSTL2 format, change the timing values on inputs and/or outputs to reduce the number of timing types. Read TIMESET statement section of TSTL2 specifications for detailed information.

UIT-236 (warning) You have invoked preview_dft with -script and one or more of the following options: -show, -test_points, -test_wrapper, -core_integration, -mbist, -bsd, -test_mode, -verbose. These options are ignored.

DESCRIPTION

The **preview_dft** command option **-script** is mutually exclusive to the following options **-show**, **-test_points**, **-test_wrapper**, **-core_integration**, **-mbist**, **-bsd**, **-test_mode**, and **-verbose**. This message says that you have asked for one or more of the options. DFT Compiler ignores the additional option(s) and generates a script.

WHAT NEXT

To get rid of the warning, invoke **preview_dft** with either the **-show** option and/or the following options: **-test_points**, **-test_wrapper**, **-core_integration**, **-mbist**, **-bsd**, **-test_mode**, **-verbose** OR just the **-script** option, but not both.

UIT-237 (information) You have invoked remove_scan_configuration with no options. The command is ignored.

DESCRIPTION

The **remove_scan_specification** command does nothing when it is invoked without options.

This, in itself, is not a problem. No scan specifications are removed. You might, however, have meant to use the "-all" option or one of the other more limited options.

WHAT NEXT

To get rid of the information message, invoke **remove_scan_configuration** with options.

UIT-238 (information) To support new scan insertion capabilities, this command is being replaced by the insert_scan command. Please see the DFT Compiler Scan Synthesis User

Guide for more information about insert_scan.

DESCRIPTION

To support new scan insertion capabilities, the **insert_test** command is being replaced by **insert_scan**.

DFT Compiler continues to support both commands for a transition period, so legacy **dc_shell** scripts continue to work.

insert_scan supports all **insert_test** features and ultimately intend obsoleting **insert_test**.

WHAT NEXT

See the DFT Compiler Scan Synthesis User Guide for more information about **insert_scan** and the hierarchical scan user interface. Let Synopsys know about any **insert_test** feature that you rely on, and is not supported by **insert_scan**.

UIT-239 (information) To support new scan insertion capabilities, this command is being replaced by the set_scan_path command, which is used with the insert_scan command. Please see the DFT Compiler Scan Synthesis User Guide for more information about set_scan_path and insert_scan.

DESCRIPTION

To support new scan insertion capabilities, the **insert_test** command is being replaced by **insert_scan**.

The **set_test_routing_order** command is not recognized by **insert_scan**. The **set_scan_path** command is used instead.

DFT Compiler continues to support **set_test_routing_order** and **insert_test** for a transition period, so legacy **dc_shell** scripts continue to work.

set_scan_path and **insert_scan** support all **set_test_routing_order** and **insert_test** features, and ultimately intend obsoleting **set_test_routing_order** and **insert_test**.

WHAT NEXT

See the DFT Compiler Scan Synthesis User Guide for more information about **set_scan_path**, **insert_scan**, and the hierarchical scan user interface. Let Synopsys

know about any **set_test_routing_order** or **insert_test** feature that you rely on, and is not supported by **set_scan_path** and **insert_scan**.

UIT-240 (information) Some design changes may have occurred after "create_test_patterns" or "create_test_patterns" was run in a different dc_shell session.

DESCRIPTION

write_test prints this message if it detects any design changes after "create_test_patterns" or if "create_test_patterns" was run in a different dc_shell session. Make sure that any changes made to the design after the test vectors were generated do not invalidate the patterns. This can cause simulation mismatches.

WHAT NEXT

If there are any design changes that invalidate the patterns, please rerun "create_test_patterns".

UIT-241 (warning) Ignoring the -complete true option because scan chain ’%s’ is empty.

DESCRIPTION

Specify scan chains using the **set_scan_path** command. Tell DFT Compiler to not add elements to your scan chain by setting the **-complete** option to **true**.

This message tells you that DFT Compiler ignores a **-complete true** option because it is applied to an empty scan chain.

WHAT NEXT

Remove the option from the command line or specify valid scan chain elements to get rid of the warning. If you did specify chain elements, study accompanying warning messages to see why they were discarded.

UIT-242 (information) The %s attribute on the library cell %s now has priority over this attribute on an instance, reference or

design.

DESCRIPTION

You receive this message when you perform **set_scan_element** or **set_scan_transparent** on a library cell. The message indicates that the command has been executed (and the specified attribute is now present on the library cell), but warns you that this attribute now has precedence and so cannot be overwritten by performing **set_scan_element** or **set_scan_transparent** on an instance, reference or design.

WHAT NEXT

If it is acceptable to you that the library cell attribute takes precedence over the attribute on an instance, reference or design, no action on your part is required. If this is not acceptable, remove the attribute from the library cell using **set_scan_element -false**, **set_scan_transparent -false**, or **remove_attribute**.

UIT-243 (warning) The design %s corresponding to the object %s has the %s attribute set to true. This specification will not have any effect.

DESCRIPTION

The value of the scan element or scan transparent attribute on a design has precedence over the the value of the scan element or scan transparent attribute on an instance or a reference. If the scan element or the scan transparent attribute is set on an instance or a reference, and the design corresponding to this instance or reference has the scan element or scan transparent attribute set, the specification does not have any effect because of the precedence rules.

WHAT NEXT

Remove the attribute on the design if you want to see the effect of the scan element or scan transparent attribute on an instance or reference.

UIT-244 (warning) The design %s corresponding to the object %s has the %s attribute set to true. This specification will not have any effect for the level-

sensitive elements inside %s.

DESCRIPTION

The value of the scan element or scan transparent attribute on a design has precedence over the the value of the scan element or scan transparent attribute on an instance or a reference. If the scan element or the scan transparent attribute is set on an instance or a reference, and the design corresponding to this instance or reference has the scan element or scan transparent attribute set, the specification does not have any effect because of the precedence rules.

WHAT NEXT

Remove the attribute on the design if you want to see the effect of the scan element or scan transparent attribute on an instance or reference.

UIT-245 (warning) Deleting the scan transparent attribute on object %s.

DESCRIPTION

If the value of the **scan_element** attribute on a design object is true, it implies that all flip-flops and all latches inside that design object, that do not have violations, must be made a part of the scan chain. Therefore, setting the **scan_element** attribute value on a design object that already has the scan transparent value set to true causes the scan transparent attribute to be deleted.

WHAT NEXT

If you do not want the scan transparent attribute deleted, use the **set_scan_element command to set the scan_element** attribute false. To reapply the scan transparent attribute, use the **set_scan_transparent** command.

UIT-246 (error) Compliance enable specification is not paired.

DESCRIPTION

The **set_bsd_compliance** command lets you specify a compliance enable pattern for a boundary scan design. Each compliance enable pattern consists of a set of port_name value pairs. Incomplete pairs cannot be used to specify a compliance enable pattern and are rejected.

WHAT NEXT

Make sure that the compliance enable pattern has port_name value pairs.

UIT-247 (error) '%s' is not a port of the design.

DESCRIPTION

The **set_bsd_compliance** command lets you specify a compliance enable pattern for a boundary scan design. Each compliance enable pattern consists of a set of port_name value pairs. One of the port names specified in the compliance enable pattern does not correspond to a design port.

WHAT NEXT

Change the compliance pattern specification such that all port names appearing in a compliance pattern are ports of the design.

UIT-248 (error) Multiple design objects found with name '%s'.

DESCRIPTION

The **set_bsd_compliance** command lets you specify a compliance enable pattern for a Boundary Scan Design. Each compliance enable pattern consists of a set of port_name-value pairs. One of the port names specified in the compliance enable pattern corresponds to multiple design objects.

WHAT NEXT

Re-issue the **set_bsd_compliance** command making sure that each port name in a compliance enable pattern corresponds to a unique design object.

UIT-249 (error) The value specified at a compliance enable port must be either a '0' or a '1'.

DESCRIPTION

The **set_bsd_compliance** command lets you specify a compliance enable pattern for a boundary scan design. Each compliance enable pattern consists of a set of port_name value pairs. The value at a compliance enable port must be either a logic zero or a logic one.

WHAT NEXT

Make sure that the value at each compliance enable port in a compliance enable pattern is either a logic zero or a logic one.

UIT-250 (error) The following compliance enable port is not an input port: %s.

DESCRIPTION

The **set_bsd_compliance** command lets you specify a compliance enable pattern for a boundary scan design. Each compliance enable pattern consists of a set of port_name value pairs. Each port name in a compliance enable specification must correspond to an input port of the design.

WHAT NEXT

Make sure that each port in the compliance enable pattern corresponds to an input port of the design.

UIT-251 (error) The following compliance enable port is a TAP port: %s.

DESCRIPTION

The **set_bsd_compliance** command lets you specify a compliance enable pattern for a boundary scan design. Each compliance enable pattern consists of a set of port_name value pairs. No compliance enable pattern may include a TAP port.

WHAT NEXT

Remove the TAP ports from the compliance pattern specification.

UIT-252 (warning) No TAP ports were found for the design.

DESCRIPTION

The **set_bsd_compliance** command issues an error if any compliance enable port is a TAP port. You get this warning if this check is not performed because no IEEE 1149.1 Test Access Ports were found for the design.

WHAT NEXT

No further action is necessary.

UIT-253 (error) The following port appears more than once in a compliance enable pattern: '%s'.

DESCRIPTION

The **set_bsd_compliance** command lets you specify a compliance enable pattern for a boundary scan design. Each compliance enable pattern consists of a set of port_name value pairs. No port can appear more than once in a compliance enable specification.

WHAT NEXT

Make sure that the compliance enable pattern has no duplicate ports.

UIT-254 (information) Writing '%s' package description.

DESCRIPTION

The **read_pin_map** command lets you read port-to-pin map files for Boundary Scan Designs. The **read_pin_map** command produces this information message when the user reads in a port-to-pin map file.

WHAT NEXT

No further action is necessary.

UIT-255 (information) Overwriting '%s' package description.

DESCRIPTION

The **read_pin_map** command lets you read port-to-pin map files for Boundary Scan Designs. If a port-to-pin map file with some package name has been read in and the user tries to read in another port-to-pin map file with the same package name, the **read_pin_map** command produces this information message.

WHAT NEXT

No further action is necessary.

UIT-256 (information) Deleting ’%s’ package description.

DESCRIPTION

The **remove_pin_map** command lets you delete a package description for a Boundary Scan Design. The **remove_pin_map** command produces this information message when the user tries to delete a package description.

WHAT NEXT

No further action is necessary.

UIT-257 (error) Could not find package ’%s’.

DESCRIPTION

The **remove_pin_map** command lets you delete a package description for a Boundary Scan Design. The **remove_pin_map** command produces this information message when the package name specified by the user has not been read in.

WHAT NEXT

Check the packages read in for the design using the **report_pin_map** command and reissue the **remove_pin_map** command with a valid package name.

UIT-258 (error) Naming check must be one of ’VHDL’, ’BSDL’ or ’none’.

DESCRIPTION

The only valid values for the naming_check argument to **write_bsdl** are "VHDL", "BSDL" or "none". This error message indicates that the naming_check argument has some value other than these.

WHAT NEXT

Make sure that the value of the naming check argument is valid.

UIT-259 (error) Unable to open output file '%s' for writing.

DESCRIPTION

This error message occurs when the output file cannot be opened for writing.

WHAT NEXT

Make sure that the output file and the directory have write permissions and run the command again.

UIT-260 (information) Opened BSDL file '%s' for writing.

DESCRIPTION

This information message indicates that the BSDL generation subsystem has successfully opened the output file for writing.

WHAT NEXT

No further action is necessary.

UIT-261 (error) Cannot read file '%s'.

DESCRIPTION

This error appears when you try to read a protected pin map file or the file does not exist.

WHAT NEXT

Check and correct search_path, then reinvoke the **read_pin_map** command.

UIT-262 (error) File '%s' is a directory name.

DESCRIPTION

You receive this message from the **read_pin_map** command if the argument you issued with that command is a directory name and not a filename. The argument of **read_pin_map** must be the full name of a file containing the port-to-pin mapping for

your design.

WHAT NEXT

Verify the full pathname of your port-to-pin mapping file, then reissue **read_pin_map** using the complete, correct filename as the argument.

SEE ALSO

read_pin_map(2).

UIT-263 (warning) %d ports have been specified. Only the first will be processed.

DESCRIPTION

You use the set_dft_signal command to associate test mode signal semantics with exactly one design port. You see this error when you try to specify the test mode of multiple design ports using the set_dft_signal command.

WHAT NEXT

Ensure that you want to associate test mode semantics with the first design port. Remove additional specifications to silence the warning.

UIT-264 (warning) %s port '%s' can not be a %s.

DESCRIPTION

You can use the set_dft_signal command to associate test mode signal semantics with exactly one design input port. This warning is generated when you apply the set_dft_signal command to a port that is not an input port.

WHAT NEXT

Repeat the command using the correct port.

UIT-265 (error) There is no valid test mode port.

DESCRIPTION

You use the set_dft_signal command to associate test mode signal semantics with exactly one design input port. You see this error when nothing you specify identifies a design input port.

WHAT NEXT

Study accompanying messages for the reasons why the port you specified was not acceptable, and repeat the command using a valid input port.

UIT-266 (error) '%s' is not a test mode signal type.

DESCRIPTION

The set_dft_signal command lets you associate test mode signal semantics with exactly one design input port. Specified signal types must be test mode signal types in test_hold_logic_zero and test_hold_logic_one. Other signal types do not have test mode signal semantics and are rejected.

WHAT NEXT

Repeat the set_dft_signal command using a test mode signal type.

UIT-267 (warning) Port '%s' has a '%s' signal_type attribute. This may conflict with '%s' signal semantics.

DESCRIPTION

The set_scan_signal and set_dft_signal commands let you associate signal semantics with design ports. This message tells you that a port has a signal_type attribute that may conflict with these semantics.

WHAT NEXT

Satisfy yourself that there is no conflict.

UIT-268 (warning) Port '%s' has a test_hold '%s' attribute. This

conflicts with ’%s’ signal semantics.

DESCRIPTION

The set_dft_signal command lets you associate signal semantics with exactly one design input port. This message tells you that the port has a test_hold attribute that conflicts with these semantics.

WHAT NEXT

Satisfy yourself that there is no conflict.

UIT-269 (error) The type of a Test Access Port must be one of %s, %s, %s, %s, or %s.

DESCRIPTION

You can use the **set_bsd_port** command to put test-specific signal types on design ports. The only valid signal types for 1149.1 TAP ports are tdi, tdo, tms, trst, or tck. This error message appears when you try set the signal type of a TAP port to a value other than tdi, tdo, tms, trst, or tck.

WHAT NEXT

Repeat the command using the correct TAP port type.

UIT-270 (error) More than one port specified with the set_1149.1_port command.

DESCRIPTION

You can use the **set_bsd_port** command to put test-specific signal types on a design port. This error occurs when you try to perform **set_bsd_port** on a set of ports.

WHAT NEXT

Specify exactly one port when using the **set_bsd_port** command.

UIT-271 (error) Did not complete set_bsd_port. ’%s’ is a %s, not

a design port.

DESCRIPTION

You can use the **set_bsd_port** command to put test-specific signal types on design ports. This error is generated when you try to set the signal type of an object that is not a design port.

WHAT NEXT

Repeat the command using the correct port name.

UIT-272 (error) Did not complete set_bsd_port. %s port '%s' can not be a %s.

DESCRIPTION

You can use the **set_bsd_port** command to put test-specific signal types on design ports. This error is generated when you try to set the signal type of a port to something that is inconsistent with its direction. For example, signal type tdo is associated with boundary scan test data output. It cannot be associated with an input port.

WHAT NEXT

Repeat the command using the correct port.

UIT-273 (error) A port, '%s', with a signal type of '%s' already exists in the design.

DESCRIPTION

You can use the **set_bsd_port** command to put test-specific signal types on a design port. This error message is produced if a port with the given signal type already exists in the design.

WHAT NEXT

Remove the signal_type attribute from the existing port and reissue the command.

UIT-274 (error) The '%s' port is a system clock.

DESCRIPTION

You can use the **set_bsd_port** command to put test-specific signal types on a design port. This error message is produced if you try to declare a system clock port as the TDI, TDO, TMS or TRST pin of the TAP.

WHAT NEXT

Reissue the **set_bsd_port** command specifying a non-clock port as the TDI, TDO, TMS or TRST pin of the TAP.

UIT-275 (error) The '%s' port is a test clock.

DESCRIPTION

You can use the **set_bsd_port** command to put test-specific signal types on a design port. This error message is produced if you try to declare a test clock port as the TDI, TDO, TMS or TRST pin of the TAP.

WHAT NEXT

Reissue the **set_bsd_port** command specifying a port that is not a test clock as the TDI, TDO, TMS or TRST pin of the TAP.

UIT-276 (Warning) Overwriting the signal type attribute for the port '%s'.

DESCRIPTION

You can use the **set_bsd_port** command to put test-specific signal types on a design port. This warning message is produced if you try to perform **set_bsd_port** on a port that already has a signal type attribute.

WHAT NEXT

No further action is necessary.

UIT-277 (error) The '<signal_port_bit_value_pairs>' list has no

members.

DESCRIPTION

The **set_bsd_compliance** command lets you specify a compliance enable pattern for a Boundary Scan design. The signal_port-bit_value list in a **set_bsd_compliance** cannot be empty.

WHAT NEXT

Reissue the command with a nonempty list of signal_port-bit_value pairs.

UIT-278 (information) You invoked remove_bsd_specification with no options. The command is ignored.

DESCRIPTION

The **remove_bsd_specification** command does nothing when it is invoked without options.

This, in itself, is not a problem. No IEEE 1149.1 specifications are removed. However, you might have meant to use the **-all** option or one of the other more limited options.

WHAT NEXT

To get rid of the information message, invoke **remove_bsd_specification** with options.

UIT-279 (warning) The sense value '%s' is ignored.

DESCRIPTION

In command **set_scan_signal**, the option **-sense** is applicable only if a hookup pin has been specified. If there is no hookup pin, the sense value is then ignored.

WHAT NEXT

If you want to specify a hookup pin, use the option **-hookup**.

UIT-280 (error) '%s' is not a correct hookup sense type.

DESCRIPTION

The **set_scan_signal** command lets you associate scan signal semantics with design ports. With respect to a specific design port, if a hookup pin also is specified, **insert_scan** connects wires to the hookup pin. The sense between the port and the hookup pin is specified by the option of **-sense**. The valid values are **non_inverted** and **inverted**, and the default value is **non_inverted**.

WHAT NEXT

Repeat the command using a correct hookup sense value.

UIT-281 (information) Setting the default package for the design '%s'.

DESCRIPTION

The **-default_package** switch of the **set_bsd_configuration** command lets you set the the default package for a Boundary Scan Design. You get this information message when you invoke the **set_bsd_configuration** command to set the default package for a Boundary Scan Design.

WHAT NEXT

No further action is necessary.

UIT-282 (information) Overwriting the default package for the design '%s'.

DESCRIPTION

The **-default_package** switch of the **set_bsd_configuration** command lets you set the the default package for a Boundary Scan Design. If the default package for a Boundary Scan Design has already been set, and you invoke the **set_bsd_configuration** command to set the default package for the Boundary Scan Design, you get this information message.

WHAT NEXT

No further action is needed.

UIT-283 (warning) Signature is not supported for '%s' instruction. Ignored the signature specification.

DESCRIPTION

This error message occurs when you specify a signature for another instruction. The **set_bsd_instruction** command allows you to set the signature for the RUNBIST instruction.

WHAT NEXT

The signature specification is ignored for this instruction. To avoid this warning, remove the signature specification.

SEE ALSO

set_bsd_instruction(2)

UIT-284 (error) The signature for the RUNBIST instruction is invalid.

DESCRIPTION

The **set_bsd_instruction** command allows you to set the parameters for the RUNBIST instructions. This error message indicates that you either ignored signature specification for RUNBIST or specified a RUNBIST signature that contains values other than a logic zero or a logic one.

WHAT NEXT

Make sure you specify signature if time or clock cycle is specified for RUNBIST instruction. Also make sure that the signature specified for the RUNBIST instruction is a stream of logic ones and zeros of a length equal to the length of the test data register selected by the RUNBIST instruction.

UIT-285 (error) The wait specification for the RUNBIST/INTEST instruction is missing.

DESCRIPTION

This error message occurs when you have not specified the duration required for the RUNBIST or INTEST instruction to complete. The **set_bsd_instruction** command allows

you to set the timing parameters for the RUNBIST or INTEST instructions.

WHAT NEXT

Specify the wait duration required for the RUNBIST or INTEST instructions to complete using either the **-time** or the **-clock_cycles** options.

SEE ALSO

set_bsd_instruction(2)

UIT-286 (error) The time specified for RUNBIST/INTEST to complete must be a positive real number.

DESCRIPTION

This error message occurs when you specify a nonpositive duration for the RUNBIST or INTEST instructions to complete. The **set_bsd_instruction** command allow you to set the parameters for the RUNBIST or INTEST instructions

WHAT NEXT

Specify a positive wait duration for the RUNBIST or INTEST execution and run the the command again.

SEE ALSO

set_bsd_instruction(2)

UIT-287 (error) The clock_port num_cycles list in the wait specification for the RUNBIST/INTEST instruction is empty.

DESCRIPTION

This error message occurs when the the argument passed using the **-clock_cycles** option contains no members. The **set_bsd_instruction** command allows you to set the parameters for the RUNBIST and INTEST instructions. One way to specify the RUNBIST or INTEST duration is to provide a list of clock_port integer pairs using the **-clock_cycles** option for these instructions.

WHAT NEXT

Make sure that the argument passed using the **-clock_cycles** option has a positive, even number of members and run the command again.

SEE ALSO

set_bsd_instruction(2)

UIT-288 (error) The RUNBIST/INTEST execution time specification is not paired.

DESCRIPTION

This error message occurs when the argument passed using the **-clock_cycles** option contains an odd number of members. The **set_bsd_instruction** command allows you to set the parameters for the RUNBIST and INTEST instructions. One way to specify the RUNBIST or INTEST duration is to provide a list of clock_port integer pairs using the **-clock_cycles** option for these instructions.

WHAT NEXT

Make sure that the argument specified with the **-clock_cycles** option contains an even number of members.

SEE ALSO

set_bsd_instruction(2)

UIT-289 (error) The number of clock cycles in the wait specification must be a positive integer.

DESCRIPTION

This error message occurs when you have specified a non-integer or a non-positive integer with the **-clock_cycles** option of the **set_bsd_instruction** command. The **set_bsd_instruction** command allows you to set the parameters for the EXTEST_PULSE, EXTEST_TRAIN, RUNBIST, and INTEST instructions. The number of clock cycles specified using the **-clock_cycles** option for this command must be a positive integer.

WHAT NEXT

Make sure that the number of clock cycles specified via the **-clock_cycles** option is a positive integer.

SEE ALSO

set_bsd_instruction(2)

UIT-290 (error) Could not find port '%s' in the design '%s'.

DESCRIPTION

This error message occurs when a port name specified using the **-clock_cycles** option of the previous commands is not a port of the design.

The **set_bsd_instruction** command allows you to set the parameters for the EXTEST_PULSE, EXTEST_TRAIN, RUNBIST, and INTEST instructions.

WHAT NEXT

Make sure that the port name specified with the **-clock_cycles** option is a port of the design.

SEE ALSO

set_bsd_instruction(2)

UIT-291 (error) The '%s' port in the wait specification is not an input/inout port.

DESCRIPTION

This error message occurs when a port specified using the **-clock_cycles** option of the prior commands is not an input or inout port.

The **set_bsd_instruction** command allows you to set the parameters for the RUNBIST and INTEST instructions.

WHAT NEXT

Make sure that all ports in the wait specification are input or inout ports.

SEE ALSO

set_bsd_instruction(2)

UIT-292 (error) The '%s' port in the RUNBIST/INTEST duration specification is not a system or test clock.

DESCRIPTION

The **set_bsd_runbist** and the **set_bsd_intest** commands allow you to set the parameters for the RUNBIST and INTEST instructions respectively. This error message indicates that a port specified using the **-clock_cycles** switch of the above commands is not a system or test clock.

WHAT NEXT

Make sure that all ports in the wait specification are either system clocks or test clocks.

UIT-293 (error) The '%s' port appears more than once in the RUNBIST/INTEST wait specification.

DESCRIPTION

The **set_bsd_runbist** and the **set_bsd_intest** commands allow you to set the parameters for the RUNBIST and INTEST instructions respectively. This error message indicates that a clock port appears more than once in the wait specification for the above commands.

WHAT NEXT

Make sure that no clock ports appear more than once in the RUNBIST/INTEST wait specification.

UIT-294 (information) Writing the parameters for the INTEST instruction.

DESCRIPTION

The **set_bsd_intest** command allows you to set the parameters for the INTEST instructions. This information message indicates that the parameters associated with the INTEST instruction are being written to the db design.

WHAT NEXT

No further action is needed.

UIT-295 (information) Overwriting the parameters for the INTEST instruction.

DESCRIPTION

The **set_bsd_intest** command allows you to set the parameters for the INTEST instructions. This command is not cumulative. This information message indicates that the existing parameters associated with the INTEST instruction are being overwritten by the new user specification for the INTEST parameters.

WHAT NEXT

No further action is needed.

UIT-296 (information) Writing the parameters for the RUNBIST instruction.

DESCRIPTION

The **set_bsd_runbist** command allows you to set the parameters for the RUNBIST instructions. This information message indicates that the parameters associated with the RUNBIST instruction are being written to the db design.

WHAT NEXT

No further action is needed.

UIT-297 (information) Overwriting the parameters for the RUNBIST instruction.

DESCRIPTION

The **set_bsd_runbist** command allows you to set the parameters for the RUNBIST instructions. This command is not cumulative. This information message indicates that the existing parameters associated with the RUNBIST instruction are being overwritten by the new user specification for the RUNBIST parameters.

WHAT NEXT

No further action is needed.

UIT-298 (error) The '%s' port is not an IEEE 1149.1 Test Access Port.

DESCRIPTION

The **remove_bsd_port** command allows you to remove the IEEE 1149.1 attributes from the test access ports. This error message indicates that the port you specified does not have the attributes associated with IEEE 1149.1 Test Access Ports.

WHAT NEXT

Run **report_test -port** to identify the IEEE 1149.1 test access ports and reissue the command.

UIT-299 (error) Could not remove the '%s' IEEE 1149.1 test access port.

DESCRIPTION

The **remove_bsd_port** command allows you to remove the IEEE 1149.1 attributes from the test access ports. This error message tells you that the **remove_bsd_port** cannot remove the IEEE 1149.1 test attibutes from the port.

WHAT NEXT

Make sure that the port is indeed an IEEE 1149.1 test access port.

UIT-300 (warning) The specified routing signals are ignored because the -route option is set to false.

DESCRIPTION

In command **set_scan_configuration**, the option **-route_signals** is not applicable when the option **-route** is set to false.

WHAT NEXT

Set the option **-route** to true, or just take the default value.

SEE ALSO

set_scan_configuration

UIT-301 (error) The specified routing signal type '%s' is incorrect.

DESCRIPTION

In command **set_scan_configuration", the correct routing scan signal types for the option -route_signals** are {**all**, **global**, **serial**, **scan_enables**, **clocks**}.

WHAT NEXT

Repeat the command using the correct routing scan signal types.

SEE ALSO

set_scan_configuration

UIT-302 (warning) The specified routing signal type '%s' is not valid for the scan style '%s'.

DESCRIPTION

In command **set_scan_configuration", the correct routing scan signal types for the option -route_signals** are {**all**, **global**, **serial**, **scan_enables**, **clocks**}.

However, some route signal types do not belong to certain scan styles. For example, the routing signal type **clocks** is not valid for **multiplexed-flip-flop** scan style, and **scan_enables** is not valid for **lssd** scan style.

WHAT NEXT

Check your set_scan_configuration -style and -route_signals specifications are consistent.

UIT-303 (warning) The -internal_clocks option will be ignored. It only applies to multiplexed-Flip-Flop scan style.

DESCRIPTION

You receive this message if you are using a scan style other than *multiplexed_flip_flop* and specified the **-internal_clocks** option with either the **set_scan_configuration** or **create_test_clock** command. You can use the **-internal_clocks** option only with the *multiplexed_flip_flop* scan style; the option is ignored for all other scan styles.

WHAT NEXT

If you want to use the **-internal_clocks** option, set the scan style to *multiplexed_flip_flop* using **set_scan_configuration**, and re-apply the **-internal_clocks** option. If you want to keep your current scan style, or if it is acceptable for the **-internal_clocks** option to be ignored, you do not need to take any action.

SEE ALSO

set_scan_configuration (2). **create_test_clock** (2).

UIT-304 (warning) Restoring Constrained value for port '%s'.

DESCRIPTION

In the STIL procedures, you can force a constrained port to a state other than the requested constrained value, but usually this is allowed only for a few tester cycles, and then the port must be returned to the constrained value. For example, you might want to hold a global reset port to an off state for general ATPG patterns but allow it to be asserted to initialize the design.

WHAT NEXT

This message is purely an informational message; no action is required.

UIT-305 (error) '%s' is not a DFT signal type.

DESCRIPTION

You receive this message if you execute the **set_dft_signal** command and use a signal type that is not a valid DFT signal type. Valid DFT signal types are

test_point_normal_data_source, test_point_normal_data_sink, test_point_clock and test_mode. Other signal types do not have DFT signal semantics and are rejected.

WHAT NEXT

Reexecute the **set_dft_signal** command using a valid DFT signal type.

SEE ALSO

set_dft_signal (2).

UIT-306 (warning) %d DFT ports have been specified, but access pins have been specified also. Only the first port will be processed.

DESCRIPTION

You receive this message if you execute the **set_dft_signal** command and specify both the **-hookup** *pin* and **-port** *port_list* options, where *port_list* contains more than one port. If you use the **-hookup** option, you can use only one design port for *port_list*.

WHAT NEXT

Re-execute the **set_dft_signal** command, and specify only one port if you are also specifying access pins with the **-hookup** option. If you want to specify multiple DFT ports, use a single command for each port.

SEE ALSO

set_dft_signal (2).

UIT-307 (warning) '%s' is a %s and cannot be used to specify a DFT signal port.

DESCRIPTION

The set_dft_signal command allows design objects to specify ports. These must be ports. Other kinds of design objects cannot be used to specify DFT signal ports, and are rejected.

WHAT NEXT

Remove the object from the argument list to get rid of the warning. Use hierarchical instance names, with respect to the top-level design, to locate design objects.

UIT-308 (warning) '%s' is a %s and cannot be used to specify a DFT signal pin.

DESCRIPTION

The set_dft_signal command allows design objects to specify pins. These must be pins or pin instances. Other kinds of design objects cannot be used to specify DFT signal ports, and are rejected.

WHAT NEXT

Remove the object from the argument list to get rid of the warning. Use hierarchical instance names, with respect to the top-level design, to locate design objects.

UIT-309 (warning) %s port '%s' cannot be a %s.

DESCRIPTION

You can use the **set_dft_signal** command to put associated DFT semantics with design ports. This warning is generated when you try to set the signal type of a port to something that is inconsistent with its direction. For example, signal type test_point_normal_data_source is associated with input ports. It cannot be associated with an output port.

WHAT NEXT

Repeat the command using the correct port.

UIT-310 (error) There is no valid DFT port.

DESCRIPTION

You receive this error message if you execute the **set_dft_signal** command and do not specify a valid design port.

WHAT NEXT

Study accompanying messages to determine why specified ports were not acceptable, and repeat the command using valid ports.

SEE ALSO

set_dft_signal (2).

UIT-311 (error) No specified hookup pin is valid.

DESCRIPTION

You receive this message if you execute the **set_dft_signal** command with the **-hookup** option, and its argument is not a valid design pin.

WHAT NEXT

Study accompanying messages to determine why the specified access pins were not acceptable. Repeat the command using valid pin instances.

SEE ALSO

set_dft_signal (2).

UIT-312 (warning) %s pin '%s' cannot be a %s.

DESCRIPTION

You can use the set_dft_signal command to specify hookup pins for design ports that have DFT semantics. This warning is generated when you try to set the hookup pin for a port to something that is inconsistent with its direction. For example, ports with signal type test_point_normal_data_source should be associated with output pins. They cannot be associated with input pins.

WHAT NEXT

Repeat the command using the correct hookup pin.

UIT-313 (warning) %d DFT ports have been specified. Only the

first will be processed.

DESCRIPTION

You use the **set_dft_signal** command to associate DFT signal semantics with design ports. You receive this error message when both of the following are true:

1. The **set_dft_signal** specification has multiple ports specified using the **-port** switch.

2. The **set_dft_signal** specification has a hookup pin specified using the **-hookup** switch.

WHAT NEXT

Execute the **set_dft_signal** command specifying a single port each time you wish to specify a hookup pin for the DFT signal.

UIT-314 (warning) %d hookup pins have been specified. Only the first will be processed.

DESCRIPTION

You receive this message if you execute **set_dft_signal -hookup** with more than one pin name as the argument to **-hookup**. You can specify only one pin name for the **-hookup** option. This message informs you that all pin names after the first one are ignored.

WHAT NEXT

Re-execute **set_dft_signal -hookup** with a single pin as the argument. If you want an additional hookup pin to be used, re-execute the command specifying that pin for the design port.

SEE ALSO

set_dft_signal (2).

UIT-315 (information) The list of ports from which the DFT

signals are to be removed is empty.

DESCRIPTION

You receive this message if you issue the **remove_dft_signal** command and the *object_list* argument is empty. The *object_list* argument is required; the command does nothing when it is invoked with an empty set of boundary scan ports to be removed.

WHAT NEXT

If you did not intend to remove DFT signals from any ports, no action is required on your part. Otherwise, re-issue the **remove_dft_signal** command with at least one port as argument.

SEE ALSO

remove_dft_signal (2).

UIT-316 (error) At present, the '%s' command only supports the full scan test methodology.

DESCRIPTION

You receive this error message if you execute **insert_dft** or **preview_dft** and have previously specified a scan test methodology of *partial_scan* or *none*. Currently the **insert_dft** and **preview_dft** commands support only the *full_scan* test methodology.

WHAT NEXT

Specify the *full_scan* test methodology by executing **set_scan_configuration -methodology full_scan**. Then reexecute **insert_dft** or **preview_dft**.

SEE ALSO

insert_dft (2), **preview_dft** (2), **set_scan_configuration** (2).

UIT-317 (error) At present, the '%s' command does not support

the '%s' scan style.

DESCRIPTION

You receive this error message if you execute **insert_dft** or **preview_dft** and have previously specified a scan style other than *multiplexed_flip_flop* or *lssd*. Currently the **insert_dft** and **preview_dft** commands support only the *multiplexed_flip_flop* scan style and the *lssd* scan style.

WHAT NEXT

Specify the *multiplexed_flip_flop* scan style or the *lssd* scan style by executing **set_scan_configuration -scan_style multiplexed_flip_flop** or **set_scan_configuration -scan_style lssd**. Then reexecute **insert_dft** or **preview_dft**.

SEE ALSO

insert_dft (2), **preview_dft** (2), **set_scan_configuration** (2).

UIT-318 (information) The '%s' command will become obsolete in the 2000.04 release. Please use '%s' instead.

DESCRIPTION

This message informs you that the **set_scan**, **set_scan_chain**, **set_test_routing_order** and **insert_test** commands will become obsolete in the 2000.04 release of DFT Compiler. You are advised to use the specified replacement commands instead.

WHAT NEXT

Use the **set_scan_element**, **set_scan_path** or **insert_scan** commands instead.

SEE ALSO

insert_scan (2), **set_scan_element** (2), **set_scan_path** (2).

UIT-319 (error) Cannot change the scan style for a '%s' design.

DESCRIPTION

You receive this error message if you attempt to use **set_scan_configuration -style** to change the scan style of a design whose scan state is test ready, scan replaced,

scan routed or existing scan. In all these cases, the design has already been modified to have scan cells according to the current scan style. Therefore, you cannot change the scan style for such designs.

WHAT NEXT

If you want to change the scan style for a design, you must start with a pre-scan design.

SEE ALSO

set_scan_configuration (2).

UIT-320 (warning) You have executed insert_dft with both the -dont_fix_constraint_violations and -map_effort options. Ignoring -map_effort.

DESCRIPTION

You receive this message if you invoke **insert_dft** with both the **-dont_fix_constraint_violations** and **-map_effort** options. If you use the **-dont_fix_constraint_violations** option, **insert_dft** does not fix constraint violations after scan synthesis. Therefore, the **-map_effort** option has no meaning and is ignored.

WHAT NEXT

If it is acceptable to you that the **-map_effort** option is ignored, no action is required on your part. Otherwise, reissue **insert_dft -map_effort** without the **-dont_fix_constraint_violations** option.

SEE ALSO

insert_dft (2).

UIT-321 (warning) The **model** command is obsolete as of release 2000.10. Use the PrimeTime STAMP functionality

instead.

DESCRIPTION

This message informs you that the **model** command is obsolete as of release 2000.10; it has been replaced by the PrimeTime STAMP functionality.

WHAT NEXT

If you have questions or issues, contact your local Synopsys representative.

UIT-322 (warning) Invalid argument for -chain_length: '%s'. Argument must be a postive integer or the string "default". If an invalid argument is provided the "default" value will be used.

DESCRIPTION

You receive this message if you execute the **set_scan_configuration** command and use an invalid argument for the **-chain_length** option. Valid arguments are positive integers or the string "default".

WHAT NEXT

Reexecute the **set_scan_configuration** command and use a valid argument for the **-chain_length** option.

SEE ALSO

set_scan_configuration (2).

UIT-323 (warning) You cannot use both the -longest_chain_length and -chain_count options in the same script. Ignoring -chain_count.

DESCRIPTION

You receive this message if your script contains the **set_scan_configuration** command and both the **-longest_chain_length** and **-chain_count** options are used. These two options are mutually exclusive; **-longest_chain_length** takes precedence. This message warns you that **-chain_count** is being ignored and that **-longest_chain_length** is in

effect.

This message is generated whether the two options are used on the same or on different command lines. For example, both of the following would generate the message:

set_scan_configuration -longest_chain_length 3 -chain_count 4
or
set_scan_configuration -chain_count 4
set_scan_configuration -longest_chain_length 3

In both cases, **-chain_count 4** is ignored and **-longest_chain_length 3** is used.

WHAT NEXT

If it is acceptable to you that the **-chain_count** option is ignored, no action is required on your part. However, if you want the **-chain_count** option to be effective, edit your script so that you do not also use the **-longest_chain_length** option. Then reexecute the command.

SEE ALSO

set_scan_configuration (2).

UIT-324 (error) Library cell %s not found in any of the libraries currently available in dc_shell.

DESCRIPTION

You get this error message when the library cell specified by the **set_bsd_pad_design** command, is not found in any of the libraries available in dc_shell.

WHAT NEXT

Insure that the library cell name is correct and the library it belongs to is available in the dc_shell. Check the **link_library** variable. Check the **search_path** variable.

SEE ALSO

set_bsd_pad_design (2).

UIT-325 (error) Pin named "%s" not found on the library cell

"%s".

DESCRIPTION

You get this error message when the library cell specified by the **set_bsd_pad_design** command does not have a pin as specified in the access list.

WHAT NEXT

Insure that correct library cell name and pin names are specified.

SEE ALSO

set_bsd_pad_design (2).

UIT-326 (information) The '%s' command will become obsolete in the '%s' release. Please use '%s' instead.

DESCRIPTION

This message informs you that the command specified in the error message will be obsolete in the release specified in the error message. You are advised to use the specified replacement command instead.

WHAT NEXT

Use the replacement command instead.

SEE ALSO

UIT-327 (Warning) Disable result '%s' is not valid for pad type '%s'. Ignoring the specified disable result and using the default value.

DESCRIPTION

You get this warning message when the disable result specified by the **-disable_res** option of the **set_bsd_pad_design** command, is not valid for the pad type.

Following are valid disable results for different pad types:

tristate_output - Z bidirectional - Z open_drain_output - WEAK0, PULL0 open_source_output - WEAK1, PULL1 open_drain_bidirectional - WEAK0, PULL0 open_source_bidirectional - WEAK1, PULL1

WHAT NEXT

Specify a valid disable result for the pad design and rerun.

SEE ALSO

set_bsd_pad_design (2).

UIT-328 (error) Signal types port and/or port_inverted not specified for differential pad design.

DESCRIPTION

You get this error message when the option **-differential** of the command **set_bsd_pad_design** is set to true and the **access_list** does not specify both **port** and **port_inverted** signal types. For differential pad designs both **port** and **port_inverted** signal types must be specified in the access list.

WHAT NEXT

Specify both **port** and **port_inverted** signal types for the pad design and rerun.

SEE ALSO

set_bsd_pad_design (2).

UIT-329 (Error) Instruction ’%s’ has illegal opcode "%s". (The opcode string must contain only binary values ’0’s and ’1’s.)

DESCRIPTION

BSD instruction opcodes must be binary codes. Code cubes (which include ‘dont care’ X bits) are not allowed. The only characters permitted in these code strings are ’0’s and ’1’s.

WHAT NEXT

Re-write the binary opcode for the instruction using only ’0’s and ’1’s.

UIT-330 (information) TPF protocol format will no longer be the default format from 2003.03 release. Please switch to STIL format in future releases.

DESCRIPTION

The tool shows this message to indicate that the default format of the test protocol will be changed in the future release. Please switch to the new test protocol format.

WHAT NEXT

SEE ALSO

read_test_protocol(2), write_test_protocol(2), read_init_protocol>(2).

UIT-331 (information) The '%s' command will become obsolete in the 2002.05 release. Please use TetraMAX ATPG tool instead.

DESCRIPTION

This message informs you that the **create_test_patterns** command will become obsolete in the 2002.05 release of DFT Compiler. You are advised to refer to TetraMAX ATPG tool for test pattern generation.

WHAT NEXT

Refer to the TetraMAX ATPG User Guide for more information about using TetraMAX ATPG tool.

UIT-332 (warning) Port '%s' has a driven_by_logic_%s attribute. This conflicts with '%s' signal semantics.

DESCRIPTION

The set_dft_signal command lets you associate signal semantics with exactly one design input port. This message tells you that the port has a driven_by_logic attribute that conflicts with these semantics.

WHAT NEXT

Satisfy yourself that there is no conflict.

UIT-333 (warning) Port '%s' has a dft_signal_type '%s' attribute. The signal semantics conflicts with the test_hold '%s' attribute.

DESCRIPTION

The set_test_hold command sets the test_hold attribute to a logic value to be assumed on specified input ports during testing. This message tells you that a port has a dft_signal_type attribute and the signal semantics conflicts with the value of the test_hold attribute.

WHAT NEXT

Satisfy yourself that there is no conflict.

UIT-334 (error) Incorrect value for the -async_fix option argument. Allowed values are mux and MUX; or gate and GATE.

DESCRIPTION

This error message informs you that you used the **set_autofix_configuration** command with an invalid argument for the **-async_fix** option. Allowed values for the **-async_fix** option argument are mux and MUX; or gate, GATE.

WHAT NEXT

Use the **set_autofix_configuration** command with the **-async_fix** option and specify one of the allowed values as the argument.

SEE ALSO

set_autofix_configuration (2).

UIT-335 (warning) You have specified the command '%s' for the port '%s' with a sense inout. Make sure you apply the correct test

constraints for test design rule checking.

DESCRIPTION

This warning message informs you that you used one of the following commands - **set_dft_signal**, **set_autofix_clock**, **set_autofix_async** - to specify a port with a direction inout.

WHAT NEXT

Make sure you apply the correct test constraints for test design rule checking.

SEE ALSO

set_dft_signal (2), **set_autofix_clock** (2), **set_autofix_async** (2).

UIT-336 (error) Boundary scan data register length should be a positive integer.

DESCRIPTION

You receive this message if you execute the **set_bsd_register** command and specify an invalid value for the *legth*.

WHAT NEXT

Specify a positive integer value for the boundary scan data register length.

SEE ALSO

insert_bsd (2), **set_bsd_register** (2).

UIT-337 (error) License feature '%s' required for the '%s' option of the '%s' command could not be found in the license file.

DESCRIPTION

Some dc_shell commands require specific licenses for some of their options. This error may occur when the required feature is not authorized.

WHAT NEXT

Make sure your installation is correct and that you are supposed to be authorized for this license feature.

UIT-338 (error) '%s'is not a valid value for the '%s' option of the '%s' command.

DESCRIPTION

You get this error when the value specified for the command option is invalid.

WHAT NEXT

Specifiy a valid value for the command option and rerun. See the command man page for a list of valid values for the option.

UIT-339 (error) Specified pin '%s' is not found in the design '%s'.

DESCRIPTION

You receive this message if the named pin is not found in the current design.

WHAT NEXT

Reexecute the command with the correct pin that exists in the current design.

SEE ALSO

set_power_up_reset (2).

UIT-349 (error) Register not specified for the instruction %s. The -register argument is required for user-defined and RUNBIST instructions.

DESCRIPTION

A standard data register or a user-defined register previously declared with the **set_bsd_register** command in DB mode or with **set_scan_path** command in XG mode, must

be specifed for user-defined and RUNBIST instruction by **-register** argument. For user-defined and RUNBIST instructions there is no default register to be connected for serial access between TDI and TDO when the instruction is active.

WHAT NEXT

Specify a standard data register or a user-defined register for the **-register** argument of the instrcution.

SEE ALSO

set_bsd_instruction (2), **set_bsd_register** (2), **set_scan_path** (2).

UIT-350 (error) '%s' is not a standard instruction.

DESCRIPTION

The **set_bsd_instruction** command is used to specify a standard boundary scan instruction as defined by IEEE Std 1149.1. You have used this command to specify a nonstandard boundary scan instruction.

WHAT NEXT

Issue the command with a standard boundary scan instruction.

UIT-351 (error) The '%s' instruction is not supported.

DESCRIPTION

The **set_bsd_instruction** command is used to specify a standard boundary-scan instruction as defined by IEEE Std 1149.1. At present, the **set_bsd_instruction** command only supports the following instructions: BYPASS, EXTEST, SAMPLE, HIGHZ, CLAMP and IDCODE. You have used this command to specify one of the following instructions: RUNBIST, INTEST or USERCODE.

WHAT NEXT

Reissue **set_bsd_instruction** command specifying a set of boundary scan instructions supported by BSD Compiler.

UIT-352 (information) Writing boundary-scan instruction '%s'.

DESCRIPTION

You receive this message from the **set_bsd_instruction** command to inform you that the specified instruction is being written to the database, to be implemented during the Boundary Scan logic insertion performed by **insert_bsd**.

WHAT NEXT

If you intend that the specified instruction be implemented, no action is required on your part. Otherwise, you can remove the instruction using **remove_bsd_instruction**.

SEE ALSO

insert_bsd (2), **remove_bsd_instruction** (2), **set_bsd_instruction** (2).

UIT-353 (warning) Overwriting boundary-scan instruction '%s'.

DESCRIPTION

You receive this message if you issue the **set_bsd_instruction** command and specify an instruction that is already on the list of instructions to be implemented by **insert_bsd**. This message informs you that the specified instruction is being overwritten in the list by the **set_bsd_instruction** command you just issued.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

insert_bsd (2), **set_bsd_instruction** (2).

UIT-354 (warning) %d boundary scan TAP ports have been specified. Only

the first boundary scan port will be processed.

DESCRIPTION

Use the **set_bsd_signal** command to associate boundary scan signal semantics with design ports. This error occurs when you try to specify the signal type of multiple design ports.

WHAT NEXT

Split outstanding boundary scan TAP port specifications among multiple commands.

UIT-355 (error) There is no valid boundary scan TAP port.

DESCRIPTION

Use the **set_bsd_signal** command to associate boundary scan signal semantics with design ports. This error occurs when nothing you specified is a valid design port.

WHAT NEXT

Study accompanying messages for the reasons why specified ports were not acceptable, and repeat the command using valid ports.

UIT-356 (warning) %d boundary scan ports are specified. Only the
first will be processed.

DESCRIPTION

Use the **set_bsd_signalf command to associate boundary scan signal semantics with design ports. This error occurs when you try to specify the signal type of multiple design ports using the same command. To simplify commands and eliminate ambiguity, use separate commands.**

WHAT NEXT

Split outstanding boundary scan port specifications among multiple commands.

UIT-357 (error) Instruction encoding must be one of ’default’ or

’one_hot’.

DESCRIPTION

You can use the **set_bsd_configuration** command to specify the instruction encoding for the boundary scan instructions synthesized by the **create_bsd** command. The only valid values for instruction encoding are **one_hot** or **default**. You have specified an instruction encoding other that **default** or **one_hot**.

WHAT NEXT

Specify the instruction encoding to be either **default** or **one_hot**.

UIT-358 (error) You must specify at least one option. For available options, input "set_bsd_configuration -help".

DESCRIPTION

The **set_bsd_configuration** command does nothing when it is invoked without options.

WHAT NEXT

To get rid of the information message, invoke **set_bsd_configuration** with at least one option.

UIT-359 (information) The set of boundary scan instructions to be removed is empty.

DESCRIPTION

The **remove_bsd_instruction** command does nothing when it is invoked with an empty set of instructions to be removed.

WHAT NEXT

To get rid of the information message, invoke **remove_bsd_instruction** with at least one instruction to be removed.

UIT-360 (information) Removing boundary scan instruction '%s'.

DESCRIPTION

The **remove_bsd_instruction** command is used to remove boundary scan instructions previously specified with the **set_bsd_instruction** command.

WHAT NEXT

Empty.

UIT-361 (warning) Could not remove boundary scan instruction '%s'.

DESCRIPTION

The **remove_bsd_instruction** command is used to remove boundary scan instructions previously specified with the **set_bsd_instruction** command. This warning message indicates that the boundary scan instruction specified by the user could not be removed.

WHAT NEXT

Check if the instruction was previously specified using the **set_bsd_instruction** command.

UIT-362 (warning) Could not find boundary scan instruction '%s'.

DESCRIPTION

The **remove_bsd_instruction** command is used to remove boundary scan instructions previously specified with the **set_bsd_instruction** command. This warning message indicates that the boundary scan instruction specified by the user could not be found.

WHAT NEXT

Check if the instruction was previously specified using the **set_bsd_instruction** command.

UIT-363 (information) The list of ports from which the boundary scan signals are to be removed is empty.

DESCRIPTION

The **remove_bsd_signal** command does nothing when it is invoked with an empty set of boundary scan ports to be removed.

WHAT NEXT

To get rid of the information message, invoke **remove_bsd_signal** with at least one boundary scan port to be removed.

UIT-365 (warning) The direction switch may only be used with bidirectional ports.

DESCRIPTION

The **-direction** switch of the **set_bsr_cell_type** command should only be used for bidirectional ports. You have used the **-direction** switch with some input or output ports. The **set_bsr_cell_type** command issued will only operate on bidirectional ports in the list of ports specified.

WHAT NEXT

None.

UIT-366 (warning) Ignoring the command for the %s ports.

DESCRIPTION

This warning message occurs when you invoke the **set_bsr_cell_type** command with the **-direction** switch and there are some input or output ports in the port list. This warning message also occurs when you specify a boundary scan cell type of **observe_only** for an output port or the output side of a bidirectional port.

WHAT NEXT

Correct your **set_bsr_cell_type** specification and re-issue the command.

UIT-367 (warning) Observe-only is not a valid boundary scan cell type for %s port.

DESCRIPTION

This warning message occurs when you specify a boundary scan cell type of **observe_only** for an output port or the output side of a bidirectional port.

WHAT NEXT

Correct your **set_bsr_cell_type** specification and re-issue the command.

UIT-368 (error) Invalid boundary scan cell type '%s'. Boundary scan cell type must be one of 'none', 'observe_only' or 'control_observe'.

DESCRIPTION

You have specified an invalid boundary scan cell type. Boundary scan cell type must be one of none, observe_only or control_observe.

WHAT NEXT

Specify one of the valid boundary scan cell types and re-issue the **set_bsr_cell_type** command.

UIT-369 (error) Invalid direction argument '%s'. The direction must be one of 'in' or 'out'.

DESCRIPTION

You have specified an invalid direction argument for a bidirectional port. The direction argument must be one of in or out, corresponding to the input and output sides of a bidirectional port.

WHAT NEXT

Re-issue the **set_bsr_cell_type** command with the correct direction.

UIT-370 (error) Scan specification on cell '%s' would make multibit '%s' in design '%s' non-homogeneous.

DESCRIPTION

Multibits have the property that each bit implements the same function. The scan specification is such that, if insert_scan implements it, the bits of this multibit no longer have the same function.

In order to avoid breaking the homogeneity property of multibits, DFT Compiler ignores this scan specification.

WHAT NEXT

If you still want the scan specification on this cell, you have two options:

1) Remove the multibit with the remove_multibit command. For this operation, you will need to set the current design to the design containing the multibit.

2) Issue the scan specification for the whole multibit.

UIT-371 (Warning) Multibit '%s' in design '%s' is not a scan segment.

DESCRIPTION

You have used a multibit in a context where a scan segment is expected. This particular multibit is not a segment. Either the global default (set using the set_scan_configuration) calls for multibits not to be segments, or you have marked this multibit as not a segment.

The multibit and its constituant cells are ignored.

WHAT NEXT

You can make a multibit into a scan segment using the set_scan_segment command. You can also list the individual bits of the multibit.

UIT-372 (Warning) The '%s' option of the set_scan_segment command does not apply to synthesizable segments; the option

is ignored.

DESCRIPTION

The command you have issued refers to a synthesizable segment. You can not specify access points or the contained cells of a synthesizable segment. These options are used for user segments.

The extra option is ignored.

WHAT NEXT

See the description of the set_scan_segment command for an explanation of the various options and their interrelations.

UIT-373 (Warning) The ’%s’ option of the set_scan_segment command does not apply to user segments; the option is ignored.

DESCRIPTION

The command you have issued refers to a user segment. In a user segment, the order of the cells are determined by the connectivity of the design. You cannot alter this through scan specifications.

The -reverse_order option has no effect, it is ignored.

WHAT NEXT

See the description of the set_scan_segment command for an explanation of the various options and their interrelations.

UIT-374 (warning) Multibit ’%s’ is already a synthesizable segment.

DESCRIPTION

The specification is redundant. It is ignored.

WHAT NEXT

No action required if you don’t mind the extra message.

UIT-375 (warning) ’%s’ is already a segment.

DESCRIPTION

The specification is redundant. It is ignored.

WHAT NEXT

No action required if you don’t mind the extra message.

UIT-376 (information) There is no explicit synthesizable segment specification for multibit ’%s’; it remains%s a synthesizable segment, as specified in the scan configuration.

DESCRIPTION

You have attempted to remove a segment specification which you have not given explicitely using the **set_scan_segment** command. The **remove_scan_configuration** command has effect only on explicit segments.

WHAT NEXT

If you want to override the default provided by the scan configuration, use the **set_scan_segment** command. To view the current default, use the **report_test -configuration** command. To specify a new default for multibits, use the **set_scan_configuration** command.

UIT-377 (information) The explicit synthesizable segment specification for multibit ’%s’ is removed; now, it is%s a synthesizable segment, as specified in the scan configuration.

DESCRIPTION

You have removed a segment specification which you previously set using the **set_scan_segment** command. This message informs you of the default specification this

segment inherits from the scan configuration. Note that it is possible to have non-segments become segments as a result of applying the **remove_scan_configuration** command.

WHAT NEXT

If you are happy with the current state of this segment, no action is required. Otherwise, you can issue an explicit scan configuration using the **set_scan_segment** command. To view the current default, use the **report_test -configuration** command. To specify a new default for multibits, use the **set_scan_configuration** command.

UIT-378 (error) Instance '%s' is not in the system.

DESCRIPTION

This error indicates that the current command cannot find the instance in the system.

WHAT NEXT

Use a different -instance option.

UIT-379 (error) Incorrect value of -clock option argument. Allowed values are true, TRUE, on, and ON; or false, FALSE, off, and OFF.

DESCRIPTION

You receive this message if you execute **set_autofix_configuration** or **set_autofix_element** with an incorrect argument for the **-clock** option. Allowed values of the **-clock** option argument are *true, TRUE, on*, and *ON*; or *false, FALSE, off*, and *OFF*.

WHAT NEXT

Re-issue the command with one of the allowed values for the **-clock** option argument.

SEE ALSO

set_autofix_configuration (2), **set_autofix_element** (2).

UIT-380 (error) Incorrect value of -async option argument. Allowed values are true, TRUE, on, and ON; or false, FALSE, off, and OFF.

DESCRIPTION

You receive this message if you execute **set_autofix_configuration** or **set_autofix_element** with an incorrect argument for the **-async** option. Allowed values of the **-async** option argument are *true, TRUE, on*, and *ON*; or *false, FALSE, off*, and *OFF*.

WHAT NEXT

Re-issue the command with one of the allowed values for the **-async** option argument.

SEE ALSO

set_autofix_configuration (2), **set_autofix_element** (2).

UIT-381 (error) Incorrect value of -fix_protocol option argument. Allowed values are true, TRUE, on, and ON; or false, FALSE, off, and OFF.

DESCRIPTION

You receive this message if you execute **set_autofix_configuration** or **set_autofix_element** with an incorrect argument for the **-fix_protocol** option. Allowed values of the **-fix_protocol** argument are *true, TRUE, on*, and *ON*; or *false, FALSE, off*, and *OFF*.

WHAT NEXT

Re-issue the command with one of the allowed values for the **-fix_protocol** option argument.

SEE ALSO

set_autofix_configuration (2), **set_autofix_element** (2).

UIT-382 (error) Incorrect value of -string option argument.

Allowed values are true, TRUE, false, or FALSE.

DESCRIPTION

You receive this message if you execute **set_autofix_element** with an incorrect argument for the **-string** option. Allowed values of the **-string** option argument are *true*, *TRUE*, *false*, or *FALSE*.

WHAT NEXT

Re-issue the command with one of the allowed values for the **-string** option argument.

SEE ALSO

set_autofix_element (2).

UIT-383 (error) No port of name %s was found in design %s.

DESCRIPTION

This is an error message. The port %s was not found in design %s.
Check the name and re-invoke the command.

WHAT NEXT

You may want to use find command to list all ports.

UIT-384 (error) Port %s is not a test clock.

DESCRIPTION

The port %s is not a test clock. Use **create_test_clock** to create a test clock associated with port %s.

WHAT NEXT

Use **report_test -port** to report all test clocks available on the current design.

UIT-385 (error) Port %s is not of type input.

DESCRIPTION

You receive this error message if the specified port, given with the **set_autofix_clock** command or the **set_autofix_async** command, is not an input port. This argument must be an input port.

WHAT NEXT

Re-issue the **set_autofix_clock** command or the **set_autofix_async** command and specify an input port.

SEE ALSO

set_autofix_clock (2), **set_autofix_async** (2).

UIT-386 (warning) Cannot find cell %s in design %s.

DESCRIPTION

You receive this message if the specified cell, which you gave as part of the *object_list* argument of the **set_autofix_clock** command or the **set_autofix_async** command, or the *cellNames* argument of the **set_dft_drc_rules** command, cannot be found. Often, typos or spelling errors cause messages of this type.

WHAT NEXT

Use the **find** command to list the cells in your design, and re-execute the command using the name of a valid cell.

SEE ALSO

set_autofix_clock (2), **set_autofix_async** (2), **set_dft_drc_rules** (2).

UIT-387 (warning) Cell %s is combinational; you must use a sequential cell or a hierarchical cell with sequential elements.

DESCRIPTION

This message warns you that the specified cell is combinational. **set_autofix_clock**, **set_autofix_async** and **set_autofix_element** require sequential cells or hierarchical

cells with sequential elements. You cannot use combinational cells.

WHAT NEXT

Re-issue the command and make sure that *object_list* does not contain any combinational cells.

SEE ALSO

set_autofix_clock (2), **set_autofix_async** (2), **set_autofix_element** (2).

UIT-388 (error) You cannot specify more than one clock.

DESCRIPTION

You receive this error message if you execute **set_autofix_clock** and specify more than one clock. You can specify only one clock.

WHAT NEXT

Re-execute **set_autofix_clock** and specify only one clock.

SEE ALSO

set_autofix_clock (2).

UIT-389 (error) You cannot specify more than one asynchronous port.

DESCRIPTION

This message informs you that you used the **set_autofix_async** command and specified more than one asynchronous port. You can specify only one asynchronous port with this command.

WHAT NEXT

Rerun **set_autofix_async** and specify only one asynchronous port.

SEE ALSO

set_autofix_async (2).

UIT-390 (error) Clock port %s has a hold value of %s. You cannot specify a clock port that has a hold value set on it.

DESCRIPTION

You receive this message from **set_autofix_clock** if the specified clock port has the specified hold value set on it. Clocks with hold values are not valid for **set_autofix_clock**. A hold value is set on a clock by using the **set_test_hold** command, which places the **test_hold** attribute on the clock. You can remove the **test_hold** attribute using the **remove_attribute** command; **reset_design** removes all attributes, including **test_hold**.

WHAT NEXT

Remove the **test_hold** attribute from the clock port using the **remove_attribute** command. Then reissue the **set_autofix_clock** command and respecify the clock port.

SEE ALSO

remove_attribute (2), **reset_design** (2), **set_autofix_clock** (2), **set_test_hold** (2).

UIT-391 (information) Performing set_autofix_clock of clock "%s" on cell/instance "%s".

DESCRIPTION

This message informs you that **set_autofix_clock** is being performed on the specified clock on the specified cell or instance.

WHAT NEXT

This is an informational message only; no action is required on your part.

SEE ALSO

set_autofix_clock (2).

UIT-392 (warning) The variable **disable_transition_degradation** is now obsolete. Use

disable_library_transition_degradation instead.

DESCRIPTION

This message informs you that the variable **disable_transition_degradation** is now obsolete, and has been replaced by **disable_library_transition_degradation**. However, **disable_transition_degradation** will continue to be supported for backward compatibility.

WHAT NEXT

Use **disable_library_transition_degradation** instead of **disable_transition_degradation** in future designs.

SEE ALSO

disable_library_transition_degradation (3).

UIT-393 (error) ’%s’ is not a valid compliance enable pattern name.

DESCRIPTION

The **remove_bsd_specification -compliance <all | pattern name>** command let you remove all compliance enable patterns, or one compliance enable pattern with given pattern name.

WHAT NEXT

You mush specify a valid pattern name, or "all". To view all existing compliance patterns, use command **report_test -bsd**.

SEE ALSO

set_bsd_compliance , **report_test** .

UIT-394 (error) Port %s is not a test asynch or a test asynch

inverted.

DESCRIPTION

The port %s is neither a test asynch nor a test asynch inverted. Use **set_signal_type** to create a test asynch or test asynch inverted associated with the port %s.

WHAT NEXT

Use **report_test -port** to report all test asynchs available on the current design.

UIT-395 (error) Port %s is already a test asynch or a test asynch inverted and can not be a test clock.

DESCRIPTION

The port %s is a test asynch or test asynch inverted and can not be a test clock. Use **remove_attribute** if you do not want the port %s to be a test asynch (or a test asynch inverted) and repeat **create_test_clock**.

WHAT NEXT

Use **report_test -port** to report all test clocks and test asynchs available on the current design.

UIT-396 (error) Port %s is already a test clock and can not be a test asynch or a test asynch inverted.

DESCRIPTION

The port %s is a test clock and can not be a test asynch or a test asynch inverted. Use **remove_attribute** if you do not want the port %s to be a test clock and repeat **set_signal_type**.

WHAT NEXT

Use **report_test -port** to report all test clocks and test asynchs available on the current design.

UIT-397 (error) You cannot specify more than two async ports.

DESCRIPTION

You receive this error message if you execute **set_autofix_async** and specify more than two asyncs. You can specify one or two asyncs.

WHAT NEXT

Re-execute **set_autofix_async** and specify one or two asyncs.

SEE ALSO

set_autofix_async (2).

UIT-398 (error) Options '-function' and '-direction' cannot be specified together.

DESCRIPTION

You receive this error message if you execute **set_bsd_data_cell** command and specified both the '-function' and '-direction' options. Currently **set_bsd_data_cell** command supports two alternate options to specify the BSR data cell function at a port. The '-function' option provides a direct way of specifying the BSR data cell function at a port. In the alternate way of specification the BSR data cell function is inferred from the '-direction' option and the port_direction. You should use exactly one of the '-function' and '-direction' options in your specification.

WHAT NEXT

Re-execute **set_bsd_data_cell** and specify exactly one of the '-function' and '-direction' option.

SEE ALSO

set_bsd_data_cell (2).

UIT-399 (error) Invalid value %s specified for the '-function'

option.

DESCRIPTION

You receive this error message if you execute **set_bsd_data_cell** command and specified an incorrect value for the '-function' option. The '-function' option provides a direct way of specifying the BSR data cell function at a port. The valid values for this option are: INPUT INPUT_INVERTED OUTPUT OUTPUT_INVERTED BIDIR BIDIR_INVERTED OBSERVE

WHAT NEXT

Re-execute **set_bsd_data_cell** and specify a valid value for the '-function' option.

SEE ALSO

set_bsd_data_cell (2).

UIT-400 (error) internal error, write_test vector formatter (stran) is unable to write out status.

DESCRIPTION

The **write_test** command invokes the vector formatter **stran** in order to translate .sif files to different vector formats. Once **stran** is run, it communicates back its result status to **write_test** through a file named '.stran.status'.

The error message above is issued by the **write_test** command when the '.stran.status' file is not writable. Two reasons for that to happen: either '.stran.status' has WRITE permission or no disk space left.

WHAT NEXT

Check for write permission on the .stran.status file or disk space.

UIT-401 (error) Unknown -command option argument '%s' for

preview_scan, assuming ’insert_scan’ (default).

DESCRIPTION

If you receive this message, you have probably used an invalid argument for the **-command** option of the **preview_scan** command. The valid arguments are **insert_scan** (the default) or **reoptimize_design**; this message informs you that the default, **insert_scan**, is being used.

When **-command** is set to **insert_scan**, **preview_scan** works only in logical domain. When **-command** is set to **reoptimize_design**, **preview_scan** takes the physical design information into account.

WHAT NEXT

If you do not want **preview_scan** to use the **insert_scan** argument to the **-command** option, reapply the **preview_scan** command with the **reoptimize_design** option. For details, see the **preview_scan** man page.

UIT-402 (error) BSD configuration style must be either synchronous or asynchronous.

DESCRIPTION

You receive this message if you issue **set_bsd_configuration -style** with an invalid argument for the **-style** option. Valid values are *synchronous* and *asynchronous*. The **set_bsd_configuration** command specifies the configuration style for the boundary scan design synthesized by the **insert_bsd** command.

WHAT NEXT

Reissue **set_bsd_configuration -style** with a valid argument for the **-style** option.

SEE ALSO

insert_bsd (2), **set_bsd_configuration** (2).

UIT-403 (error) BSD instruction width must be in the range of 2

to 31.

DESCRIPTION

You receive this message if you issue the **set_bsd_configuration** command with an invalid value for the **-ir_width** option argument. Valid values are 2 through 31 only. The **insert_bsd** command uses the **-ir_width** option value to specify the number of bits in the instruction register when synthesizing the boundary scan design.

WHAT NEXT

Reissue the **set_bsd_configuration** with a valid value for the **-ir_width** option argument.

SEE ALSO

insert_bsd (2), **set_bsd_configuration** (2).

UIT-404 (error) Invalid boundary scan register type for a bidirectional port.

DESCRIPTION

You receive this message if you issue the **set_bsd_data_cell** command and specify an invalid value for the boundary scan register cell type to be used for a bidirectional port. Valid values of boundary scan register cell types for input, output, and bidirectional ports are listed in the manual page and the online help for the **set_bsd_data_cell** command. The **insert_bsd** command uses the specified boundary scan register cell types when synthesizing the boundary scan design.

WHAT NEXT

Refer to the manual page or the online help for the **set_bsd_data_cell** command to determine the current valid boundary scan register cell types, and reissue the **set_bsd_data_cell** command with a valid type.

SEE ALSO

insert_bsd (2), **set_bsd_data_cell** (2).

UIT-405 (error) Invalid boundary scan register cell type for an

input port.

DESCRIPTION

You receive this message if you issue the **set_bsd_data_cell** command and specify an invalid value for the boundary scan register cell type to be used for an input port. Valid values of boundary scan register cell types for input, output, and bidirectional ports are listed in the manual page and the online help for the **set_bsd_data_cell** command. The **insert_bsd** command uses the specified boundary scan register cell types when synthesizing the boundary scan design.

WHAT NEXT

Refer to the manual page or the online help for the **set_bsd_data_cell** command to determine the current valid boundary scan register cell types, and reissue the **set_bsd_data_cell** command with a valid type.

SEE ALSO

insert_bsd (2), **set_bsd_data_cell** (2).

UIT-406 (error) Invalid boundary scan register cell type for an output port.

DESCRIPTION

You receive this message if you issue the **set_bsd_data_cell** command and specify an invalid value for the boundary scan register cell type to be used for an output port. Valid values of boundary scan register cell types for input, output, and bidirectional ports are listed in the manual page and the online help for the **set_bsd_data_cell** command. The **insert_bsd** command uses the specified boundary scan register cell types when synthesizing the boundary scan design.

WHAT NEXT

Refer to the manual page or the online help for the **set_bsd_data_cell** command to determine the current valid boundary scan register cell types, and reissue the **set_bsd_data_cell** command with a valid type.

SEE ALSO

insert_bsd (2), **set_bsd_data_cell** (2).

UIT-407 (error) Invalid port type '%s' specified for user-defined BSR, TAP, or BSD Register.

DESCRIPTION

You receive this message if you issue the **set_bsd_bsr_element**, **set_bsd_tap_element**, or **set_bsd_register** command and specify an invalid port type. Valid port types are found in the manual page or online help for each of the three commands. The **insert_bsd** command uses the user-defined registers when synthesizing the boundary-scan design.

WHAT NEXT

Refer to the manual pages or the online help for the **set_bsd_bsr_element**, **set_bsd_tap_element**, or **set_bsd_register** command to determine the current valid BSR, TAP, and BSD register port types, respectively. Then reissue the appropriate command with a valid port type.

SEE ALSO

insert_bsd (2), **set_bsd_bsr_element** (2), **set_bsd_register** (2), **set_bsd_tap_element** (2).

UIT-408 (error) Invalid port or control BSR name '%s'.

DESCRIPTION

You receive this message if you issue the **set_bsd_path** command and the *identifier_list* contains a name that is neither a valid design port nor a valid control BSR cell identifier; this could be caused by a typo or spelling error. The *identifier_list* must contain a list of names of valid ports and valid control BSR identifiers. The order of the names in the list determines the order that the **insert_bsd** command uses when it implements the boundary scan design.

WHAT NEXT

Verify the correct names of the ports and control BSR cell identifiers, then reissue the **set_bsd_path** command using the correct names and identifiers.

SEE ALSO

insert_bsd (2), **set_bsd_control_cell** (2), **set_bsd_path** (2).

UIT-409 (error) Port direction must be either "in" or "out".

DESCRIPTION

You receive this message if you execute **set_bsd_data_cell** or **set_bsd_path** and specify an invalid port direction. Valid port directions are "in" and "out". For **set_bsd_data_cell**, you specify the port direction using the **-direction** option. For **set_bsd_path**, you can specify the direction of a bidirectional port by attaching /in or /out to the port name in the *identifier_list*.

The **insert_bsd** command uses the port direction information when synthesizing the boundary scan design.

WHAT NEXT

Choose a valid port direction for the port, and reissue the appropriate command using the valid port direction.

SEE ALSO

insert_bsd (2), **set_bsd_data_cell** (2), **set_bsd_path** (2).

UIT-410 (error) You cannot specify the direction of a nonbidirectional port.

DESCRIPTION

You receive this message if you execute the **set_bsd_path** command and specify the direction of a port that is not a bidirectional port. You can specify the direction of a bidirectional port in the *identifier_list* as *port_name*/in or *port_name*/out; however, it is an error to attach /in or /out to the name of a nonbidirectional port. *insert_bsd* uses the *identifier_list* to determine the order in which the BSR cells are to be connected in the synthesized boundary scan design.

WHAT NEXT

Verify the port types in the *identifier_list*, and reexecute the **set_bsd_path** command specifying the direction for only the bidirectional ports.

SEE ALSO

insert_bsd (2), **set_bsd_path** (2).

UIT-411 (error) Cannot find the specified pin '%s'.

DESCRIPTION

You receive this message if you issue the **set_bsd_register** command and a pin specified in the *access_list* cannot be found on the user-specified boundary scan data register cell. This could be caused by a typo or spelling error. The **insert_bsd** command uses the user-specified boundary scan data register cell in synthesizing the boundary scan design. You may also get this message if you intend to specify a scan-through tap register, and issue the **set_bsd_register** command with the reserved words **SR_SI** or **SR_SO** in the access list, however the register name is not the reserved word **STT_REG**.

WHAT NEXT

Verify the correct name for the specified pin, and reissue the **set_bsd_register** command using the correct pin name. If you want to specify a scan-through-tap register use the reserved name **STT_REG** for the register and reissue the command.

SEE ALSO

insert_scan (2), **set_bsd_register** (2).

UIT-412 (error) You cannot specify a control BSR cell for a non-tristate port '%s'.

DESCRIPTION

You receive this message if you execute the **set_bsd_control_cell** command and the *port_list* contains a port that is not connected to a tristate pad. You specify a control BSR cell to control tristate port pads only. The **insert_bsd** command uses the control BSR cell when synthesizing the boundary scan design.

WHAT NEXT

Reexecute the **set_bsd_control_cell** command with a *port_list* that contains only names of ports that are connected to tristate pads.

SEE ALSO

insert_bsd (2), **set_bsd_control_cell** (2).

UIT-413 (error) Cannot find the specified port '%s' in the design

or instance.

DESCRIPTION

You receive this message if you execute the **set_bsd_bsr_element**, **set_bsd_tap_element**, or **set_bsd_register** command and a port you specify cannot be found in the design or instance. This could be caused by a typo or spelling error.

WHAT NEXT

Verify the name of the port. Then reissue the appropriate command using the correct port name for the design or instance.

SEE ALSO

insert_bsd (2), **set_bsd_bsr_element** (2), **set_bsd_register** (2), **set_bsd_tap_element** (2).

UIT-414 (error) Cannot find cell name '%s' in the current design.

DESCRIPTION

You receive this message if you issue the **set_bsd_register** command and the name you specify for the *hierarchical_cell* argument cannot be found in the current design. This could be caused by a typo, a spelling error, or an incorrect path.

The **insert_bsd** command uses the user-specified boundary scan data register cell in synthesizing the boundary scan design.

WHAT NEXT

Verify the correct name and hierarchical path of the cell you want to specify as a boundary scan data register, and reissue the **set_bsd_register** command using the correct name.

SEE ALSO

insert_bsd (2), **set_bsd_register** (2).

UIT-415 (error) Invalid cell type for boundary scan register

element.

DESCRIPTION

You receive this message if you issue the **set_bsd_bsr_element** command and specify an invalid value for the boundary scan register cell type. Valid values of boundary scan register cell types are listed in the manual page and the online help for the **set_bsd_bsr_element** command. The **insert_bsd** command uses the specified boundary scan register cell type when synthesizing the boundary scan design.

WHAT NEXT

Refer to the manual page or the online help for the **set_bsd_bsr_element** command to determine the current valid boundary scan register cell types, and reissue the **set_bsd_bsr_element** command with a valid cell type.

SEE ALSO

insert_bsd (2), **set_bsd_bsr_element** (2).

UIT-416 (error) Invalid cell type for boundary scan tristate control register.

DESCRIPTION

You receive this message if you issue the **set_bsd_control_cell** command and specify an invalid cell type for the boundary scan tristate control register. Valid values of cell types for a boundary scan tristate control register are listed in the manual page and the online help for the **set_bsd_control_cell** command. The **insert_bsd** command uses the specified boundary scan control register cell type when synthesizing the boundary scan design.

WHAT NEXT

Refer to the manual page or the online help for the **set_bsd_control_cell** command to determine the current valid cell types for the boundary scan tristate control register, and reissue the **set_bsd_control_cell** command with a valid cell type.

SEE ALSO

insert_bsd (2), **set_bsd_control_cell** (2).

UIT-417 (error) Invalid boundary scan register cell type for ports.

DESCRIPTION

You receive this message if you issue the **set_bsd_data_cell** command and specify an invalid value for the boundary scan register cell type to be used for specified ports. Valid values of boundary scan register cell types for input, output, and bidirectional ports are listed in the manual page and the online help for the **set_bsd_data_cell** command. The **insert_bsd** command uses the specified boundary scan register cell types when synthesizing the boundary scan design.

WHAT NEXT

Refer to the manual page or the online help for the **set_bsd_data_cell** command to determine the current valid boundary scan register cell types, and reissue the **set_bsd_data_cell** command with a valid cell type.

SEE ALSO

insert_bsd (2), **set_bsd_data_cell** (2).

UIT-418 (error) Cannot find the specified design in memory.

DESCRIPTION

You receive this message if you execute the **set_bsd_bsr_element** or **set_bsd_tap_element** command and the name you specify for the *design_name* argument cannot be found in memory. This could be caused by a typo or spelling error. The **insert_bsd** command uses the specified design as a boundary scan register or tap controller when synthesizing the boundary scan design.

WHAT NEXT

Verify that the design you want to use does exist in memory, and verify its spelling. Then re-execute the appropriate command using the correct design name.

SEE ALSO

insert_bsd (2), **set_bsd_bsr_element** (2), **set_bsd_tap_element** (2).

UIT-419 (error) You cannot use a reserved word as a user-

defined boundary scan data register name.

DESCRIPTION

You receive this message if you execute the **set_bsd_register** command in DB mode or **set_scan_path** comman in XG mode and specify a reserved word (for example, BOUNDARY, BYPASS, or DEVICE_ID) as the *register_identifier*. Reserved words are predefined names, reserved for boundary scan test data; you cannot use a reserved word to name a user-defined data register. Reserved words are listed in the manual page for the **set_bsd_register** command. The **insert_bsd** command in DB mode or **insert_dft** command in XG mode uses the user-defined data register when synthesizing the boundary scan design.

WHAT NEXT

Refer to the manual page of the **set_bsd_register** command for the list of reserved words, and specify a *register_identifier* that is not a reserved word.

SEE ALSO

insert_bsd (2), **set_bsd_register** (2), **insert_dft** (2), **set_scan_path** (2).

UIT-420 (error) Invalid bidirectional port is specified

DESCRIPTION

You can use the **set_bsd_path** command to specify the order in which the BSR cells need to hooked up in the boundary scan design synthesized by the **create_bsd** command. This command takes a list of design ports or control BSR names as input. For a bidirectional port the direction can be specified as <port_name>/in or <port_name>/out if the input BSR cell and output BSR cell for the port need to be routed in a particular order. Direction can’t be specified for a non bidirectional port. You have specified direction for a non bidirectional port.

WHAT NEXT

Don’t specify direction for a non bidirctional port.

UIT-421 (error) Invalid bidirectional port is specified

DESCRIPTION

You can use the **set_bsd_path** command to specify the order in which the BSR cells need to hooked up in the boundary scan design synthesized by the **create_bsd** command.

This command takes a list of design ports or control BSR names as input. For a bidirectional port the direction can be specified as <port_name>/in or <port_name>/out if the input BSR cell and output BSR cell for the port need to be routed in a particular order. Direction can’t be specified for a non bidirectional port. You have specified direction for a non bidirectional port.

WHAT NEXT

Don’t specify direction for a non bidirctional port.

UIT-422 (error) Invalid bidirectional port is specified

DESCRIPTION

You can use the **set_bsd_path** command to specify the order in which the BSR cells need to hooked up in the boundary scan design synthesized by the **create_bsd** command. This command takes a list of design ports or control BSR names as input. For a bidirectional port the direction can be specified as <port_name>/in or <port_name>/out if the input BSR cell and output BSR cell for the port need to be routed in a particular order. Direction can’t be specified for a non bidirectional port. You have specified direction for a non bidirectional port.

WHAT NEXT

Don’t specify direction for a non bidirctional port.

UIT-423 (error) Invalid bidirectional port is specified

DESCRIPTION

You can use the **set_bsd_path** command to specify the order in which the BSR cells need to hooked up in the boundary scan design synthesized by the **create_bsd** command. This command takes a list of design ports or control BSR names as input. For a bidirectional port the direction can be specified as <port_name>/in or <port_name>/out if the input BSR cell and output BSR cell for the port need to be routed in a particular order. Direction can’t be specified for a non bidirectional port. You have specified direction for a non bidirectional port.

WHAT NEXT

Don’t specify direction for a non bidirctional port.

UIT-424 (error) Specified BSD pad design "%s" does not exist.

DESCRIPTION

You receive this error message because you have executed the **set_bsd_pad_design** command and specified a design that does not exist in memory. You can use **set_bsd_pad_design** to specify and characterize a design as a pad design. Such a design is treated like a pad cell by the boundary-scan insertion.

WHAT NEXT

Use the **list_designs** command to see what designs are in memory, then use the **read** command to read in the design. Next, execute the **set_bsd_pad_design** command to set the desired design as a pad design.

SEE ALSO

list_designs (2), **read** (2), **set_bsd_pad_design** (2).

UIT-425 (error) Signal type "%s" specified in the access list of the pad design is invalid.

DESCRIPTION

You receive this error message because you have executed the **set_bsd_pad_design** command and have specified an invalid signal type as part of the access list for the pad design. You use the **set_bsd_pad_design** command to specify and characterize a design as a pad design. The access list for the pad design is specified as a list of pairs of signal types and pin names. Valid signal types are data_in, data_in_inverted, data_out, data_out_inverted, enable, and enable_inverted.

WHAT NEXT

Reexecute the **set_bsd_pad_design** command and specify a valid signal type in the access list for the **-access** option.

SEE ALSO

set_bsd_pad_design (2).

UIT-426 (error) Specified pad design "%s" does not have a pin

named "%s".

DESCRIPTION

You receive this error message when you execute the **set_bsd_pad_design** command and specify a pin name in the access list that does not exist in the pad design. The **set_bsd_pad_design** command is used to specify and characterize a design as a pad design. The access list for the pad design specifies a list of pairs of signal types and pin names.

WHAT NEXT

Reexecute the **set_bsd_pad_design** command and specify a valid pin name in the access list for the **-access** argument.

SEE ALSO

find (2), **set_bsd_pad_design** (2).

UIT-427 (error) "%s" is not a valid value for the "%s" option of the set_bsd_pad_design command.

DESCRIPTION

You receive this error message because you have specified an invalid argument for the **-type** option, the **-disable_res** option, or the **-differential** option of the **set_bsd_pad_design** command. Use the **set_bsd_pad_design** command to specify and characterize a design as a pad design. Valid arguments for the **-type** option are input, output, tristate_output, and bidirectional. Valid arguments for the **-disable_res** option are WEAK0, WEAK1, PULL0, and PULL1. Valid arguments for the **-differential** option are true and false.

WHAT NEXT

Reexecute the **set_bsd_pad_design** command and specify a valid option argument.

SEE ALSO

find (2), **set_bsd_pad_design** (2).

UIT-428 (error) Insufficient BSD instruction width ’%d’ specified.

Requires at least '%d'.

DESCRIPTION

This error message tells you that you used the **set_bsd_configuration** command and specified an invalid value for the **-ir_width** option. The specified width is not sufficient to hold all the instruction opcodes specified with the **set_bsd_instruction** command. The **insert_bsd** command uses the **-ir_width** option value to specify the number of bits in the instruction register when synthesizing the boundary scan design.

WHAT NEXT

Use the **set_bsd_configuration** command with the **-ir_width** option and specify a value sufficient to hold all the instruction opcodes.

SEE ALSO

insert_bsd (2), **set_bsd_configuration** (2). **set_bsd_instruction** (2).

UIT-429 (error) BSD instruction opcode width must be in the range of 2 to 31.

DESCRIPTION

This error message indicates that you ran the **set_bsd_instruction** command with the **-code** option and specified an invalid opcode width. Valid opcode widths are 2 through 31. The **insert_bsd** command uses the opcode width to specify the number of bits in the instruction register when synthesizing the boundary scan design.

WHAT NEXT

Rerun the **set_bsd_instruction** command and specify a valid opcode width for the **-code** option argument.

SEE ALSO

insert_bsd (2), **set_bsd_instruction** (2).

UIT-430 (error) Signal type '%s' specified twice or specified with

its inversion.

DESCRIPTION

This message informs you that you ran the **set_bsd_pad_design** command with an access list that specifies a signal type twice, or that specifies a signal type and its inversion. For example, an access list specifying both enable and enable_inverted signal types, or specifying two data_in signal types results in this error message.

WHAT NEXT

Rerun the **set_bsd_pad_design** command with a valid access list.

SEE ALSO

insert_bsd (2), **set_bsd_pad_design** (2).

UIT-431 (error) Signal type '%s' specified twice.

DESCRIPTION

You receive this message if you issue the **set_bsd_pad_design** command with an access list specifying a signal type or it's inverted type twice. For instance an access list specifying both enable and enable_inverted signal types, or an access list specifying two data_in signal types.

WHAT NEXT

Reissue the **set_bsd_pad_design** with a valid access list.

SEE ALSO

insert_bsd (2), **set_bsd_pad_design** (2).

UIT-432 (error) Incorrect %s field is specified for input/output ports.

DESCRIPTION

You receive this message if you execute **set_bsd_data_cell** command and specify an incorrect direction/function for an input or output port. The direction field in **set_bsd_data_cell** command for input/output ports should be unspecified(in which case

it is assumed to be the same as the port direction) or should be consistent with the port direction. The function field in **set_bsd_data_cell** command for input ports should be unspecified(in which case it is assumed to be INPUT) or should be either INPUT or INPUT_INVERTED or OBSERVE. The function field in **set_bsd_data_cell** command for output ports should be unspecified (in which case it is assumed to be OUTPUT) or should be either OUTPUT or OUTPUT_INVERTED. Please note that options direction and function are mutually exclusive.

WHAT NEXT

For input/output ports, leave the direction/function field blank or specifiy a direction/function consistent with the port direction. For bidirectional port, you should specify the direction/function, or leave it blank in case you specify the cell_type as "BC_7", or "none".

UIT-433 (error) The output format '%s' was not supported by new translation engine.

DESCRIPTION

You receive this message if you execute **write_test** command with **write_test_new_translation_engine** = true(default), but specify a test program format which is not currently supported by new translation engine.

WHAT NEXT

For valid test program formats currently supported by new translation engine, execute "write_test -help" for more information.

UIT-434 (error) The design does not have a BSD clock port.

DESCRIPTION

You receive this message if you execute **write_test** command to write out the BSD test program in or through STIL format, but the design does not have a BSD clock port.

WHAT NEXT

Please check if the jtag clock of the design was defined correctly.

SEE ALSO

set_bsd_signal (2), **set_bsd_port** (2), **set_signal_type** (2).

UIT-435 (error) The unix environment variable LTRAN_ROOT is not defined.

DESCRIPTION

You receive this message if you execute **write_test** command to write out test program with format tdl91, tstl2, or ftdl, with environment variable **write_test_new_translation_engine" set to true(default). In this case, the environment variable LTRAN_ROOT** must be correctly set to invoke Ltran executable.

WHAT NEXT

You should set it as,

setenv LTRAN_ROOT $SYNOPSYS/$TARGET_ARCH/syn/tran

UIT-436 (warning) Assigning name "%s" to the bsr element.

DESCRIPTION

You get this warning when the (optional) name parameter for the bsr element is not specified. When unspecified, a name identical to the bsr element type("BC_1", "BC_2", "BC_4" or "BC_7") is assigned to the bsr element. As BSD compiler recognizes the bsr elements named as "BC_1", "BC_2", "BC_4" and "BC_7" as the default bsr elements of types BC_1, BC_2, BC_4 and BC_7 respectively, this bsr element will become the default bsr element for the type. If a bsr element named so(explicitly or implicitly) is not defined, then Design Ware bsr element remains the default bsr element for the type. A default bsr element is the one chosen from different implementations for bsr cells not having a "set_bsd_data_cell" or "set_bsd_control_cell" specification.

WHAT NEXT

Specify a valid name other than "BC_1", "BC_2", "BC_4" and "BC_7" for the bsr element if you do not intend to use this bsr element as the default for the type, and rerun the command.

SEE ALSO

set_bsd_bsr_element (2), **set_bsd_data_cell** (2), **set_bsd_control_cell** (2).

UIT-437 (error) Reserved name %s cannot be used as bsr

element name for type %s.

DESCRIPTION

You get this warning when the name specified for the bsr element is one of the reserved names "BC_1", "BC_2", "BC_4" or "BC_7" and it does not match with the specified type of the bsr element. Reserved bsr elements names "BC_1", "BC_2", "BC_4" and "BC_7" are used to explictly define the default bsr elements of types BC_1, BC_2, BC_4 and BC_7 respectively (else Design Ware bsr elements are used as default), and must match with the type. A default bsr element is the one chosen from different implementations for bsr cells not having a "set_bsd_data_cell" or "set_bsd_control_cell" specification.

WHAT NEXT

Correct the name or the type of the bsr element. Specify a unique name other than "BC_1", "BC_2", "BC_4" and "BC_7" for the bsr element if you do not intend to use this bsr element as the default for the type.

SEE ALSO

set_bsd_bsr_element (2), **set_bsd_data_cell** (2), **set_bsd_control_cell** (2).

UIT-438 (error) Reserved name "%s" cannot be used as bsr element name.

DESCRIPTION

You get this warning when the name specified for the bsr element is one of the reserved names "DW_BC_1", "DW_BC_2", "DW_BC_4", "DW_BC_7" or "NONE". These reserved bsr elements names are used to convey the following meaning when used as the bsr element idenetifier in the "set_bsd_data_cell" and "set_bsd_control_cell" commands:

DW_BC_1 - Insert a Design Ware BSR cell of type BC_1 DW_BC_2 - Insert a Design Ware BSR cell of type BC_2 DW_BC_4 - Insert a Design Ware BSR cell of type BC_4 DW_BC_7 - Insert a Design Ware BSR cell of type BC_7 NONE - Do not insert a BSR cell

WHAT NEXT

Specify a valid name for the bsr element other than "DW_BC_1", "DW_BC_2", "DW_BC_4", "DW_BC_7" or "NONE".

SEE ALSO

set_bsd_bsr_element (2), **set_bsd_data_cell** (2), **set_bsd_control_cell** (2).

UIT-439 (error) BSR element named %s has already been defined.

DESCRIPTION

You get this warning when the name specified for the bsr element has already been used to define a bsr element by an earlier "set_bsd_bsr_element" command.

WHAT NEXT

Specify a unique and valid name for the bsr element, and rerun the command.

SEE ALSO

set_bsd_bsr_element (2), **set_bsd_data_cell** (2), **set_bsd_control_cell** (2).

UIT-440 (warning) This bsr cell becomes the default bsr element for type %s.

DESCRIPTION

BSD compiler recognizes the bsr elements named as "BC_1", "BC_2", "BC_4" and "BC_7" as the default bsr elements of types BC_1, BC_2, BC_4 and BC_7 respectively. If a bsr element named so is not defined, then Design Ware bsr element remains the default bsr element for the type. Note that if the name is not specified for a bsr element then BSD compiler assigns a name identical to the bsr element type("BC_1", "BC_2", "BC_4" or "BC_7") for the bsr element. A default bsr element is the one chosen from different implementations for bsr cells not having a "set_bsd_data_cell" or "set_bsd_control_cell" specification.

WHAT NEXT

Specify a valid name other than "BC_1", "BC_2", "BC_4" and "BC_7" for the bsr element if you do not intend to use this bsr element as the default for the type, and rerun the command.

SEE ALSO

set_bsd_bsr_element (2), **set_bsd_data_cell** (2), **set_bsd_control_cell** (2).

UIT-441 (error) Ilegal width %d for port '%s'. Port width for signal

type ’%s’ must be %d.

DESCRIPTION

You get this error when you specify a custom tap design port signal type and the actual width of the port is not found valid. The bus port widths must be as follows for different access types:

instructions = 32-bit tap_state = 16-bit user_code_val = 32-bit ver = 4-bit part_num = 16-bit mnfr_id = 11-bit

Rest of the access types are scalar with expected port width of 1.

WHAT NEXT

Provide a correct interface for the tap design.

SEE ALSO

set_bsd_tap_element (2)

UIT-442 (error) Usercode value is not specified for the %s instruction.

DESCRIPTION

You get this error when you specify the USERCODE instruction, but don’t provide a usercode value. USERCODE instruction must have the usercode value specified using the "-user_code_val" option of the "set_bsd_instruction" command.

WHAT NEXT

Correct the specification by specifying the usercode value. The 32-bit usercode value can be specified as design pin(s) and/or sized binary constant and/or sized hex constant. Design pins must be specified as full hierarchical full pin names. Binary and hex constants must be specified using the verilog syntax.

Example: -------

Following is an incomplete and hence invalid USERCODE specification:
set_bsd_instruction USERCODE -code {0110}

The above USERCODE specification should be corrected by specifying the usercode value. For instance following is a valid USERCODE specification:

set_bsd_instruction USERCODE -code {0110} -user_code_val {version_reg/v3,

version_reg/v2, version_reg/v1, version_reg/v0, 16'b1111111110000000, 12'h2ab}

SEE ALSO

set_bsd_instruction (2)

UIT-443 (error) Usercode value cannot be specified for %s instruction. Usercode value can only be specified for the USERCDOE instruction.

DESCRIPTION

You get this error when you specify the usercode value for a non USERCODE instruction. An instruction is treated as the USERCODE instruction when the instruction name is spelt as u-s-e-r-c-o-d-e (case insensitive).

WHAT NEXT

Correct the specification. If you have USERCODE specification mixed with other instructions, you will get this error for other instructions in the list. If this is the case, separate the USERCODE specification.

If you intend to implement the USERCODE instruction and get this message make sure that the instruction name is spelt correctly(it must be spelt as case insensitive u-s-e-r-c-o-d-e).

SEE ALSO

set_bsd_instruction (2)

UIT-444 (error) '%s' is a PrimeTime command that is not supported by Design Compiler.

DESCRIPTION

Although this command is supported by PrimeTime, it is not currently supported by Design Compiler. You can check which commands are supported by Design Compiler by executing **list -commands** or **help** in dc_shell.

WHAT NEXT

Remove the command that is not supported.

UIT-445 (warning) Invalid value '%s' for spdm_mode. The valid values are either false or true.Setting default value as false.

DESCRIPTION

WHAT NEXT

Set it to one of the valid values.

EXAMPLES

EXAMPLE MESSAGE

```
Error: Invalid value 'false' for spdm_mode. The valid values are either false or tr
ue. Setting default value as false.(UIT-445)
```

UIT-446 (error) Invalid argument in the usercode value list. '%s' is not a valid design pin, sized binary or a sized hex constant.

DESCRIPTION

You get this error when you specify an invalid value in the usercode value argument list for the USERCODE instruction. The 32-bit usercode value can be specified as any combination of design pin(s) and/or sized binary constant and/or sized hex constant.

WHAT NEXT

Check and correct the usercode value argument syntax. Design pins must be specified as full hierarchical full pin names. Binary and hex constants must be specified using the following verilog syntax:

<size>'[b|B|h|H]<binary or hexadecimal value>

Example: ------- Following is a valid USERCODE specification:

```
set_bsd_instruction USERCODE -code {0110} -user_code_val {version_reg/v3,
version_reg/v2, version_reg/v1, version_reg/v0, 16'b1111111110000000, 12'h2ab}
```

SEE ALSO

set_bsd_instruction (2)

UIT-447 (error) Invalid size %d of the usercode value argument '%s'. Usercode value argument's size should be in the range of 1 to 32-bits.

DESCRIPTION

You get this error when you specify a binary or hexadecimal constant value in the usercode value argument list and the size of the argument is not in the valid range of 1 to 32-bits.

Binary and hex constants are specified using the following verilog syntax:

<size>'[b|B|h|H]<binary or hexadecimal value>

Example: ------- Following is a valid USERCODE specification:

set_bsd_instruction USERCODE -code {0110} -user_code_val {version_reg/v3, version_reg/v2, version_reg/v1, version_reg/v0, 16'b1111111110000000, 12'h2ab}

WHAT NEXT

Check and correct the usercode value argument's size.

SEE ALSO

set_bsd_instruction (2)

UIT-448 (error) %s usercode value '%s' cannot be represented in the specified %d bits.

DESCRIPTION

You get this error when you specify a binary or hexadecimal constant value in the usercode value argument list and the specified size of the argument is not sufficient enough to represent the value you have specified.

Binary and hex constants are specified using the following verilog syntax:

<size>'[b|B|h|H]<binary or hexadecimal value>

WHAT NEXT

Check and correct the usercode value argument's size.

Example: ------- Following is a wrong USERCODE specification, leading to the above

error as the hex value 5'h2ab cannot be represented in 5 bits:

```
set_bsd_instruction USERCODE -code {0110} -user_code_val {version_reg/v3,
version_reg/v2, version_reg/v1, version_reg/v0, 16'b1111111110000000, 5'h2ab}
```

Following would be a corrected specification:

```
set_bsd_instruction USERCODE -code {0110} -user_code_val {version_reg/v3,
version_reg/v2, version_reg/v1, version_reg/v0, 16'b1111111110000000, 12'h2ab}
```

SEE ALSO

set_bsd_instruction (2)

UIT-449 (error) A %s value is specified as the usercode value. Usercode value must be a 32-bits value.

DESCRIPTION

You get this error when the cumulative bit width of the arguments specified in the '-user_code_val' option of the set_bsd_instruction command is not 32-bits.The 32-bit usercode value can be specified as any combination of design pin(s) and/or sized binary constant and/or sized hex constant.

Binary and hex constants are specified using the following verilog syntax:
<size>'[b|B|h|H]<binary or hexadecimal value>

WHAT NEXT

Check and correct the usercode value argument's size.

Example: ------- Following is a wrong USERCODE specification, leading to the above error as the cumulative bit width of the usercode value here is 31:

```
set_bsd_instruction USERCODE -code {0110} -user_code_val {version_reg/v3,
version_reg/v2, version_reg/v1, version_reg/v0, 16'b1111111110000000, 11'h2ab}
```

Following would be a corrected specification:

```
set_bsd_instruction USERCODE -code {0110} -user_code_val {version_reg/v3,
version_reg/v2, version_reg/v1, version_reg/v0, 16'b1111111110000000, 12'h2ab}
```

SEE ALSO

set_bsd_instruction (2)

UIT-450 (error) Cannot read test model file '%s'.

DESCRIPTION

This error occurs when you try to read a test model file that is protected or does not exist.

WHAT NEXT

Check that the file exists, check the search_path, and check what protections are set on the file. Then, rerun the **read_test_model** command.

SEE ALSO

read_test_model (2).

UIT-451 (error) Cannot write test model file '%s'.

DESCRIPTION

This error is generated when you run the **write_test_model** command and attempt to write the test model file to a nonexistent or protected directory, or over a file that is protected.

WHAT NEXT

Check the existence and the write protection of the directory.

Check the protection of the existing file with the same name. Make the necessary change to the file or directory, and rerun the **write_test_model** command.

SEE ALSO

write_test_model (2).

UIT-452 (error) Cannot attach test model to design '%s'.

DESCRIPTION

This error is generated because a test model in CTL format is successfully read in but cannot be associated with the named design because it does not have a CTL interface.

WHAT NEXT

Make sure the named design exists and has a CTL interface. Then, rerun the **read_test_model** command.

SEE ALSO

read_test_model (2).

UIT-453 (error) Design '%s' has no test model.

DESCRIPTION

This error is generated when you request a test model operation on a design that has no test model.

WHAT NEXT

Make sure you specified the design you intended. To see a list of designs that have test models, use the **list_test_models** command. You may try to read a test model with the **read_test_modelP command or infer one with the check_dftP command.**

SEE ALSO

check_dft (2), **create_test_schedule** (2), **list_test_models** (2), **read_test_model** (2), **remove_test_models** (2), **report_test_models** (2), **write_test_model** (2).

UIT-454 (error) Format '%s' is not a valid test model format.

DESCRIPTION

This error message indicates that you specified an invalid format with the **read_test_model** command. Valid formats are db (the default) and ctl.

WHAT NEXT

Rerun the **read_test_model** command and specify a valid format.

SEE ALSO

read_test_model (2).

UIT-455 (error) The CTL model in '%s' is not accepted.

DESCRIPTION

This error occurs when you run the **read_test_model** command and specify a CTL file that has errors that prevent the correct interpretation of the file. The exact errors are reported as CTL-* messages immediately preceding this message.

WHAT NEXT

Fix the reported errors and reissue the command.

SEE ALSO

list_test_models (2), **remove_test_model** (2), **report_test_model** (2), **write_test_model** (2).

UIT-456 (error) The CTL model on design '%s' is not accepted.

DESCRIPTION

This error occurs when the test model stored on the specified design contains errors that prevent its correct interpretation. The errors are reported as CTL-* messages immediately preceding this message.

WHAT NEXT

This error is most likely due to a corrupted db file. Verify that the file is not corrupted by reading it using the **read** command and using the design in a context other than test models. If the file is not corrupted, report the problem to Synopsys immediately.

SEE ALSO

list_test_models (2), **read** (2), **remove_test_model** (2), **report_test_model** (2).

UIT-457 (information) The name of the design is included in the model file; the -design option is ignored.

DESCRIPTION

This message informs you that the **-design** option does not need to be specified with

the **read_test_model** command. For test models in db format, the model file contains the design name.

WHAT NEXT

To avoid receiving this message, use the **read_test_model** command without the **-design** option.

SEE ALSO

read_test_model (2).

UIT-458 (error) Asynchronous port %s has a hold value of %s. You cannot specify an asynchronous port that has a hold value set on it.

DESCRIPTION

This error message tells you that the asynchronous port given to the **set_autofix_async** command has the specified hold value set on it. Asynchronous ports with hold values are not valid for **set_autofix_async**. A hold value is set on an asynchronous port using the **set_test_hold** command, which places the **test_hold** attribute on the asynchronous port. You can remove the **test_hold** attribute by using the **remove_attribute** command; **reset_design** removes all attributes, including **test_hold**.

WHAT NEXT

Remove the **test_hold** attribute from the asynchronous port using the **remove_attribute** command. Then, run the **set_autofix_async** command and specify the asynchronous port.

SEE ALSO

remove_attribute (2), **reset_design** (2), **set_autofix_async** (2), **set_test_hold** (2).

UIT-459 (information) Running set_autofix_async on asynchronous port(s) "%s" to autofix the asynchronous

signal(s) on the cell or instance "%s".

DESCRIPTION

This message informs you that **set_autofix_async** is being run on the specified asynchronous port to autofix the asynchronous signal(s) of the specified cell or instance.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

set_autofix_async (2).

UIT-460 (error) Mode decoding style must be one of ’default’ or ’one_hot’.

DESCRIPTION

This error message tells you that you have specified a decoding style other than default or one_hot for the **-mode_decoding_style** option to the **set_core_integration_configuration** command. You use **set_core_integration_configuration** to specify the decoding style for the test mode ports used during core integration by the **insert_dft** command.

WHAT NEXT

Specify default or one_hot as the mode decoding style.

SEE ALSO

insert_dft (2), **set_core_integration_configuration** (2).

UIT-461 (information) You must specify the -mode_decoding_style option and the default or one_hot switch.

DESCRIPTION

This informational message tells you that you did not specify any options with the

set_core_integration_configuration command.

WHAT NEXT

Use the **set_core_integration_configuration** command and specify an option.

SEE ALSO

set_core_integration_configuration (2).

UIT-462 (information) You must specify at least one of the following switches: -all.

DESCRIPTION

This message informs you that you did not specify an option when you used the **remove_core_integration_configuration** command. The **remove_core_integration_configuration** command does nothing when it is used without options.

WHAT NEXT

Use the **remove_core_integration_configuration** command with at least one option.

SEE ALSO

remove_core_integration_configuration (2).

UIT-463 (error) Design '%s' already has a wrapper.

DESCRIPTION

This error message indicates that you attempted to insert a wrapper around a design using the **insert_wrapper -core_wrapper** command, but the design is already wrapped.

WHAT NEXT

Run the **insert_dft** command, but do not specify the **-core_wrapper** option.

SEE ALSO

insert_dft (2), **set_dft_configuration** (2).

UIT-464 (warning) Resolution of tristate port '%s' failed.

DESCRIPTION

This warning message tells you that the core wrapper architect only supports simple tristate drivers; for example, single-cell drivers at the top-level. Complex drivers are not supported.

WHAT NEXT

Use simple tristate drivers in the design. Alternatively, the port can be excluded from wrapping.

SEE ALSO

set_dft_configuration (2). **set_core_wrapper_cell** (2). **set_core_wrapper_configuration** (2).

UIT-465 (warning) Resolution of bidirectional port '%s' failed.

DESCRIPTION

This warning message tells you that the core wrapper architect only supports simple bidirectional drivers, which are single cell drivers at the top level. Complex drivers are not supported.

WHAT NEXT

Use simple bidirectional drivers in the design. Alternately, exclude the port from wrapping.

SEE ALSO

set_dft_configuration (2), **set_core_wrapper_cell(2), set_core_wrapper_configuration** (2).

UIT-466 (warning) Degenerate bidirectional port : %s.

DESCRIPTION

This warning messages means that the core wrapper architect excludes the specified port from wrapping because it is a degenerate bidirectional port.

WHAT NEXT

Rerun the command and specify a port that is not a degenerate bidirectional port.

SEE ALSO

set_dft_configuration (2). **set_core_wrapper_cell** (2).

UIT-467 (warning) Degenerate tristate port : %s.

DESCRIPTION

This warning message informs you that the core wrapper architect excludes the specified port from wrapping because it is a degenerate tristate port.

WHAT NEXT

Rerun the command and specify a port that is not a degenerate tristate port.

SEE ALSO

set_dft_configuration (2), **set_core_wrapper_cell** (2).

UIT-468 (error) You must specify at least one of the following switches: -default_wrapper_cell, -default_safe_state.

DESCRIPTION

This error occurs because you used the **set_core_wrapper_configuration** command but did not specify any options.

WHAT NEXT

Run the **set_core_wrapper_configuration** with at least one option.

SEE ALSO

remove_core_wrapper_configuration (2).

UIT-469 (warning) Bad type for wrapper cell.

DESCRIPTION

This warning message informs you that the specified wrapper cell type is invalid. The default specification is used.

WHAT NEXT

Rerun the command and specify a valid wrapper cell type.

SEE ALSO

set_core_wrapper_configuration (2). **set_core_wrapper_cell** (2).

UIT-470 (error) You must specify at least one of the following switches: -cell_type, -safe_value, or -port_list.

DESCRIPTION

This error occurs because you used the **set_core_wrapper_cell** command and did not specify and option.

WHAT NEXT

Run the **set_core_wrapper_cell** command with at least one option.

SEE ALSO

set_core_wrapper_configuration (2).

UIT-471 (warning) Bad port: '%s'.

DESCRIPTION

This warning message informs you that you specified a port that is not in the design.

WHAT NEXT

Run the command and specify a port that is in the design.

SEE ALSO

set_core_wrapper_cell (2), **set_core_wrapper_configuration** (2).

UIT-472 (error) Error when running Core Wrapper.

DESCRIPTION

This message informs you that the Core Wrapper client could not be run successfully. This indicates an error in the design or in the specifications for core wrapping. Causes might be one of the following:

1. Trying to directly wrap a CTL model
2. Trying to wrap a design without any connected ports
3. An error while instantiating wrapper cells due to incorrect libraries
4. Unsupported scan methodology

WHAT NEXT

Check the design. Make sure you are not directly trying to wrap a test model. Check the specifications.

SEE ALSO

insert_dft (2), **preview_dft** (2), **remove_core_wrapper_configuration** (2), **set_core_wrapper_cell** (2), **set_core_wrapper_configuration** (2), **set_dft_configuration** (2), **set_dft_signal** (2).

UIT-473 (error) ’%s’ identifies multiple pins.

DESCRIPTION

This error occurs if you use the **set_bsd_register** command and specify a pin in the access list that contains a wildcard that identifies multiple pins on the register cell. Each signal type and pin name pair must identify only one pin. If you want to identify multiple pins of the same type, you must specify multiple signal types and pin name pairs.

WHAT NEXT

Reissue the **set_bsd_register** command and specify multiple pin name pairs, or use a more specific wildcard.

SEE ALSO

set_bsd_register (2).

UIT-474 (error) The test model for design ’%s’ is stored in version %s of CTL. It cannot be retrieved.

DESCRIPTION

The version of CTL in which the test model is expressed is incompatible with the tool’s capabilities.

CTL is an evolving standard (P1450.6) which is not under the control of the Synopsys developers. Since the Beta version, some incompatible changes were introduced into the language.

Note that the CTL version is not an official denomination of P1450.6. It is an arbitrary number assigned to Synopsys’ implementation of a snapshot of the evolving standard. The first production release supports version 1.00.

WHAT NEXT

There are two options. If the model is on a design for which full implementation is available, then you can run check_scan to regenerate the model in the current version of CTL. If the design implementation is not readily available, then the process by which the model was created, most likely insert_scan, needs to be repeated using the current version of the tool.

SEE ALSO

read_test_model(), write_test_model(), check_scan()

UIT-475 (information) The test model on design '%s' is updated to the current CTL version. Writing out the design to disk will make this update permanent.

DESCRIPTION

The version of CTL in which the stored test model is expressed is not compliant with the current state of the proposed standard. The model was retrieved and automatically translated to the newer version of the CTL syntax.

CTL is an evolving standard (P1450.6) which is not under the control of the Synopsys developers. Since the previous version of DFT Compiler, some incompatible changes were introduced into the language.

Note that the CTL version is not an official denomination of P1450.6. It is an arbitrary number assigned to Synopsys' implementation of a snapshot of the evolving standard. DFT Compiler currently supports version 1.70.

WHAT NEXT

There are two options. 1- Do nothing, in which case the same message will be reissued each time this test model is used in this version of DFT Compiler. 2- Save the db file containing this test model back to disk.

SEE ALSO

read_test_model(), write_test_model()

UIT-476 (error) The test model for design '%s' cannot be retrieved.

DESCRIPTION

The version of CTL in which the test model is expressed is compatible with the tool's capabilities, but the information cannot be retrieved. This may be due to data corruption on the db file, or incomplete compatibility between tool versions.

CTL is an evolving standard (P1450.6) which is not under the control of the Synopsys developers. Since the previous release of DFT Compiler, some incompatible changes were introduced into the language.

Note that the CTL version is not an official denomination of P1450.6. It is an arbitrary number assigned to Synopsys' implementation of a snapshot of the evolving standard. This release supports version 1.70.

WHAT NEXT

There are multiple options. If the db file containing the model is very old, reading it into a previous version of DFT Compiler and writing it back to disk will automatically update the text of the model to the DFT Compiler version. The current version of DFT Compiler will most likely be able to read the newly updated model. Otherwise, the model can be regenerated from the current text, from the current netlist, or from the pre-dft netlist. To update the model from the current text, edit the ascii version of the model contained in file <design_name>_obsolete_model.ctl, in the current directory. It can then be read back in and re-attached to the design using the read_test_model command. If the model is on a design for which full implementation is available, then the model may be regenerated from the netlist: you can run DRC to regenerate the model in the current version of CTL. If the design implementation is not readily available, then the process by which the model was created, most likely insert_scan, needs to be repeated using the current version of the tool.

SEE ALSO

read_test_model(), write_test_model(), check_scan()

UIT-477 (information) The '%s' command is obsoleted in the 2003.03 release. Please use '%s' instead.

DESCRIPTION

This message informs you that the **set_test_signal** command is obsoleted in the 2003.03 release of DFT Compiler. You are advised to use the specified replacement commands instead.

WHAT NEXT

Use the **set_dft_signal** command instead.

SEE ALSO

insert_dft (2), **set_dft_signal** (2).

UIT-478 (Error) Valid index required for scan-in and scan-out

ports

DESCRIPTION

This message indicates that you are attempting to describe the scan-in and scan-out ports in the design without associated indices. In order to to correctly extract scan chains using descriptive specifications, the test design rule checker needs information associating scan access pins to their respective scan chains.

WHAT NEXT

Specify the appropriate indices.

SEE ALSO

test_drc (2),

UIT-479 (information) The option -order '{%s}' is obsolete in the 2003.12 release. Please use the options -autofix and/or -shadow_wrapper.

DESCRIPTION

This message informs you that the **-order** option of the **set_dft_configuration** command is obsolete in the 2003.12 release of DFT Compiler. You are advised to use the specified replacement options instead.

WHAT NEXT

Use the the **-autofix** and/or **-shadow_wrapper** options instead.

SEE ALSO

insert_dft (2), **set_dft_configuration** (2).

UIT-480 (error) The -order option cannot not be used with the -

autofix and/or -shadow_wrapper options.

DESCRIPTION

The **-order** option will become obsolete in the 2003.12 release. You are advised to use the **-autofix** and/or the **-shadow_wrapper** options instead.

WHAT NEXT

Modify the options accordingly to the recommendations and repeat the command.

SEE ALSO

insert_dft (2) **set_dft_configuration** (2)

UIT-481 (warning) Resolution of tristate port '%s' connected to pin '%s' of cell '%s' failed. The port will be excluded from wrapping.

DESCRIPTION

This warning message tells you that the core wrapper architect didn't find any tristate driver for the specified port connected to a tristate pin of a cell with test model.

WHAT NEXT

Use simple tristate drivers in the design for the speciied port. Alternatively, the port can be excluded from wrapping.

SEE ALSO

set_dft_configuration (2). **set_core_wrapper_cell** (2). **set_core_wrapper_configuration** (2).

UIT-482 (warning) Resolution of bidirectional port '%s' connected to pin '%s' of cell '%s' failed. The port will be excluded from wrapping.

DESCRIPTION

This warning message tells you that the core wrapper architect didn’t find any bidirectional driver for the specified port connected to a bidir pin of a cell with test model.

WHAT NEXT

Use simple bidirectional drivers in the design. Alternately, exclude the port from wrapping.

SEE ALSO

set_dft_configuration (2), **set_core_wrapper_cell(2), set_core_wrapper_configuration** (2).

UIT-483 (warning) Mapping Wrapper Cell Designs is not successfull, turning off wrapper insertion.

DESCRIPTION

This warning message tells you that the core wrapper insertion couldn’t map wrapper cell designs successfully. Wrapper insertion can’t proceed without mapped wrapper cells. Wrapper insertion will be turned off.

WHAT NEXT

Check if link library is setup properly to include the libraries used in mapping wrapper cells. Check if there is a license available to map wrapper cells.

SEE ALSO

set_dft_configuration (2), **set_core_wrapper_cell(2), set_core_wrapper_configuration** (2).

UIT-484 (error) Instance '%s' of design '%s' has no test model.

DESCRIPTION

This error is generated when there is no test model for the design corresponding to the cell instance you specified in a **set_test_target** command.

WHAT NEXT

Make sure you specified the instance you intended. To see a list of designs that have test models, use the **list_test_models** command. You may need to use the read_test_model command to attach a test model to the design specified in the error message.

SEE ALSO

set_test_target (2), **list_test_models** (2), **read_test_model** (2), **report_test_models** (2).

UIT-485 (error) Test mode '%s' does not exist.

DESCRIPTION

This error is generated when the **-test_mode** argument to the current command is invalid.

WHAT NEXT

Use the **list_test_modes** command to see the valid **-test_mode** arguments. If the desired test mode is not listed, you can create a new test mode with the **define_test_mode** command.

SEE ALSO

define_test_mode (2), **list_test_modes** (2), **set_test_target** (2).

UIT-486 (error) Cell '%s' is repeated.

DESCRIPTION

This error is generated when a cell in the **-cores** argument of the **set_test_target** command is repeated. Each cell may only have one mode.

WHAT NEXT

Choose only one mode for each cell and repeat the command. You can use the **report_test_model** command to see the availble test modes for a given design.

SEE ALSO

report_test_model (2), **set_test_target** (2).

UIT-487 (error) Cell '%s' can not be in wrapped mode '%s' when -purpose is top_internal_test.

DESCRIPTION

This error is generated when you try to put a core into a wrapped internal test mode (i.e. wrp_if mode) when you have specified the purpose of the mode as a top-level scan test. These are incompatible, because the top-level scan test implies that you will apply a set of patterns to the top level and the wrapped internal test mode implies that you will apply the patterns that were generated for the core. There is no way to apply both patterns at once.

WHAT NEXT

You should use the **define_test_mode** command to create two test modes. Use **set_test_target -purpose top_internal_test** without cores for one mode, and **set_test_target -purpose core_internal_test** with the desired cores for the other mode.

SEE ALSO

set_test_target (2).

UIT-488 (error) Test mode '%s' does not exist for instance '%s' of design '%s'.

DESCRIPTION

This error is generated when the **-cores** argument to the **set_test_target** command specifies an invalid mode.

WHAT NEXT

Use the **report_test_model** command to see the valid test modes for the design

indicated in the error message. Retry the **set_test_target** command using a valid mode.

SEE ALSO

report_test_model (2), **set_test_target** (2).

UIT-489 (error) No mode specified for instance %s.

DESCRIPTION

This error is generated when the **-cores** argument to the **set_test_target** command specifies an instance without a mode.

WHAT NEXT

Make sure that the **-cores** argument contains complete instance/mode pairs when you retry the **set_test_target** command.

SEE ALSO

set_test_target (2).

UIT-490 (error) Bad -purpose '%s'.

DESCRIPTION

This error is generated when you you specify an unrecognized **-purpose** for the **set_test_target** command.

WHAT NEXT

Retry the command with a valid **-purpose**.

SEE ALSO

set_test_target (2).

UIT-491 (error) You must specify -cores when -purpose is

core_internal_test.

DESCRIPTION

This error is generated when you specify **-purpose core_internal_test** without the **-cores** argument for the **set_test_target** command.

WHAT NEXT

Retry the command with a the **-cores** argument, or change **-purpose** to **top_internal_test**.

SEE ALSO

set_test_target (2).

UIT-492 (error) Current test mode is not defined.

DESCRIPTION

This error is generated when the **-test_mode** argument is omitted from the current command, and the current test mode has not been set.

WHAT NEXT

Use the **current_test_mode** command to define the current test mode, or specify a test mode directly with the **-test_mode** argument when you retry the command.

SEE ALSO

current_test_mode (2), **list_test_modes** (2), **set_test_target** (2).

UIT-493 (error) Test mode '%s' must be type InternalTest.

DESCRIPTION

This error is generated when the test mode for the **set_test_target** command does not have type InternalTest. Since the **set_test_target** command only specifies internal tests (either at the top level or core level) it doesn't make sense for the test mode to be anything other than InternalTest.

WHAT NEXT

Use the **define_test_mode** command to create a test mode with **-type InternalTest**, and specify that test mode with either the **current_test_mode** command, or the **-test_mode** argument when you retry the **set_test_target** command.

SEE ALSO

current_test_mode (2), **define_test_mode** (2), **set_test_target** (2).

UIT-494 (error) Cannot write CTL model with exec name '%s' to file '%s'.

DESCRIPTION

This error is generated when you run the **write_test** command and failed to write out the CTL model with the specified pattern exec name to the given file.

WHAT NEXT

Check the existence and the write protection of the directory.

Check the protection of the existing file with the same name.

Check the CTL model if the specified PatternExec exists. Be sure not to have quoted pattern exec name in the command line.

SEE ALSO

write_test_model (2).

UIT-495 (error) There is no valid pattern info in file '%s'.

DESCRIPTION

This error occurs when you run the **read_pattern_info** command and there is no valid pattern information block in the input file although it is a valid CTL file.

WHAT NEXT

Check the input file to add pattern info block.

UIT-496 (error) The patinfo for Pattern '%s' already existed.

DESCRIPTION

This error occurs when you run the **read_pattern_info** command and the patinfo blocks in the input file already exist in the CTL model. Unless '-overwrite' switch is added, it is an error to re- define the existing patinfo.

WHAT NEXT

Add switch '-overwrite' if you want to redefine the existing patinfo.

UIT-497 (error) Cannot find pattern matching name '%s' in existing CTL model.

DESCRIPTION

This error occurs when you run the **read_pattern_info** command and the pattern name in the patinfo file does not have a match in the existing CTL model.

WHAT NEXT

The user should change the pattern block name in the test program and patinfo file to match the pattern name in the CTL model.

UIT-498 (Warning) The following ports of design '%s' have no corresponding Signals in its test model:%s.

DESCRIPTION

The error occurs when you run the **read_test_model** command, if some ports of the design don't have corresponding Signals in the read test model. This means that there is no test information for these ports. This will make the test model unusable.

WHAT NEXT

The user should check the validity of the test model and whether it realy is the test model of the design it is being attached to.

UIT-499 (Warning) The following test model Signals have no corresponding ports in design '%s':%s.

DESCRIPTION

The error occurs when you run the **read_test_model** command, if some Signals of the model don't have corresponding ports in the design it is being associated with. This means that the model provides information about non-existing port. This will make the test model unusable.

WHAT NEXT

The user should check the validity of the test model and whether it realy is the test model of the design it is being attached to.

UIT-500 (Warning) The following ports of sub-design '%s' have no corresponding Signals in its test core:%s.

DESCRIPTION

The error occurs when some ports of a sub-design don't have corresponding Signals in its test core referenced by the test model of current design. This will make the CoreType unusable.

WHAT NEXT

The user should check the validity of the test core defined in the test model of current design.

UIT-501 (Warning) The following test core Signals have no corresponding ports in sub-design '%s':%s.

DESCRIPTION

The error occurs when some Signals of a core referenced by the model of current design don't have corresponding ports in the sub-design it is being associated with. This means that the CoreType provides information about non-existing port. This will make the CoreType unusable.

WHAT NEXT

The user should check the validity of the CoreType in the test model of current design.

UIT-502 (error) Mode decoding style must be one of ’binary’ or ’one_hot’.

DESCRIPTION

This error message tells you that you have specified a decoding style other than binary or one_hot for the **-mode_decoding_style** option to the **set_dft_configuration** command. You use **set_dft_configuration** to specify the decoding style for the test mode ports used during multi-mode DFT insertion by the **insert_dft** command.

WHAT NEXT

Specify binary or one_hot as the mode decoding style.

SEE ALSO

insert_dft (2), **set_dft_configuration** (2).

UIT-503 (Error) The signal ’%s’ must be predefined as an Oscillator signal.

DESCRIPTION

This error tells you that one of the specified PLL clocks has not been predefined as an Oscillator signal and hence the clock controller specification cannot be accepted. The **set_dft_clock_controller** command specification is ignored due to the error.

WHAT NEXT

To correct this error, specify the PLL clocks signals as having the Oscillator signal type.

In DB mode, a PLL clock pll/out is defined using either
dc_shell-t> **set_dft_signal Oscillator -hookup_pin pll/out**
or
dc_shell-t> **set_dft_signal Oscillator_inverted -hookup_pin pll/out**
depending on the PLL clock active state.

In XG mode, a PLL clock pll/out is defined using
dc_shell-xg-t> **set_dft_signal -view existing_dft -type Oscillator -hookup_pin pll_out -active_state < 0 | 1 >**

SEE ALSO

set_dft_signal (2)

UIT-504 (Warning) The port '%s' has not predefined as an Oscillator signal.

DESCRIPTION

This warning tells you that one of the specified ATE clocks has not been predefined as an Oscillator signal. If the ATE clock is a reference clock, it has to be predefined as an Oscillator signal; otherwise, this warning can be ignored. The **set_dft_clock_controller** command specification is not ignored due to this warning.

WHAT NEXT

You can ignore this warning if the ATE clock is not a reference clock. If the ATE clock is a reference clock, specify the ATE clock signal as having the Oscillator signal type and reissue the set_dft_clock_controller command.

In DB mode, a reference and ATE clock ate_clk is defined using either
dc_shell-t> **set_dft_signal Oscillator -port ate_clk**
or
dc_shell-t> **set_dft_signal Oscillator_inverted -port ate_clk**
depending on the ATE clock active state.

In XG mode, an ATE clock ate_clk is defined using
dc_shell-xg-t> **set_dft_signal -view existing_dft -type Oscillator -port ate_clk -active_state < 0 | 1 >**

SEE ALSO

set_dft_signal (2)

UIT-505 (Error) An ATE clock must be a port of the design; '%s'

is not a valid port name.

DESCRIPTION

This error tells you that one of the specified ATE clock names is not a valid port name. The **set_dft_clock_controller** command specification is discarded due to this error.

WHAT NEXT

If you want to specify a hookup pin for an ATE clock, you should specify the hookup pin with the **set_dft_signal** command and reissue the **set_dft_clock_controller** command.

SEE ALSO

set_dft_signal (2)

UIT-506 (Warning) The port '%s' has not predefined as a clock signal.

DESCRIPTION

This error tells you that the specified port has not been predefined as a clock signal and that the Oscillator signal specification cannot be accepted. If the port is a reference clock it has to be first defined as a clock and then defined as a reference clock. The **set_dft_signal** command specification is ignored due to this error.

WHAT NEXT

If the port is a reference clock, specify the ATE clock signal as having the a clock signal type and reissue the **set_dft_signal** command.

In DB mode, a reference clock ref_clk is defined using
dc_shell-t> **create_test_clock ref_clk -waveform [list 45 55]** dc_shell-t>
set_dft_signal Oscillator -port ref_clk

In XG mode, an ATE clock ate_clk is defined using
dc_shell-xg-t> **set_dft_signal -view existing_dft -type MasterClock -port ref_clk -timing [list 45 55]** dc_shell-xg-t> **set_dft_signal -view existing_dft -type Oscillator -port ref_clk**

SEE ALSO

set_dft_signal (2)

UIT-510 (Error) Test Model of core instance '%s' is not valid for integration.

DESCRIPTION

SoC BIST does not allow integration of unencapsulated cores during core integration. This error tells you that the specified core instance is not encapsulated and hence a test mode of the core instance can't be used with **set_test_target** command. The **set_test_tagret** command specification is ignored due to the error.

WHAT NEXT

To avoid the error, specify only encapsulated core test modes with **set_test_target** command.

SEE ALSO

set_test_target (2)

UIT-511 (Error) More than one bist test modes are specified, bist test modes can't be tested in parallel.

DESCRIPTION

SoC BIST does not allow bisted cores to be tested in parallel currently. This error tells you that the **set_test_target** specification includes more than one bist test modes. The **set_test_target** command specification is ignored due to the error.

WHAT NEXT

To avoid the error, specify only one encapsulated bist test mode with **set_test_target** command.

SEE ALSO

set_test_target (2)

UIT-512 (Error) Bist test modes are specified along with scan test modes, bist test modes can’t be tested in parallel.

DESCRIPTION

SoC BIST does not allow bisted cores to be tested in parallel currently. This error tells you that the **set_test_target** specification includes one or more bist test modes and one or more scan test modes. The **set_test_target** command specification is ignored due to the error.

WHAT NEXT

To avoid the error, don’t mix bist test modes with scan test modes with **set_test_target** command.

SEE ALSO

set_test_target (2)

UIT-520 (error) Specified dft design "%s" does not exist.

DESCRIPTION

You receive this error message because you have executed the **define_dft_design** command and specified a design that does not exist in memory. You can use **define_dft_design** to specify and characterize a design as a dft design. Such a design is treated like a user dft design of the specified type for dft insertion.

WHAT NEXT

Use the **list_designs** command to see what designs are in memory, then use the **read** command to read in the design. Next, execute the **define_dft_design** command to set the desired design as a pad design.

SEE ALSO

list_designs (2), **read** (2), **define_dft_design** (2).

UIT-521 (error) Specified dft design "%s" does not have a pin

named "%s".

DESCRIPTION

You receive this error message when you execute the **define_dft_design** command and specify a pin name in the interface list that does not exist in the specified dft design. The **define_dft_design** command is used to specify and characterize a design as a dft design of a type. The interface list for the dft design specifies a list of triplets of signal type, pin name and pin polarity.

WHAT NEXT

Reexecute the **define_dft_design** command and specify a valid pin name in the interface list for the **-interface** argument.

SEE ALSO

find (2), **define_dft_design** (2).

UIT-522 (error) Syntax error with the list specified with -interface option, expects a list of triplets <signal_type> <pin_name> <pin_polarity> .

DESCRIPTION

You receive this error message when you execute the **define_dft_design** command and specify an incorrect interface list. The **define_dft_design** command is used to specify and characterize a design as a dft design of a type. The interface list for the dft design specifies a list of triplets : signal type, design pin name and design pin polarity.

WHAT NEXT

Reexecute the **define_dft_design** command and specify a valid list for the **-interface** argument.

SEE ALSO

find (2), **define_dft_design** (2).

UIT-523 (error) Invalid design name '%s' - this design name is

reserved.

DESCRIPTION

You receive this error message when you execute the **define_dft_design** command and specify a design name that is reserved. The **define_dft_design** command is used to specify and characterize a design as a dft design of a type. The design name specified with this command can not be one of the following names as the name conflicts with our designware implementation of the dft component.

DW01_decode DW_control_force DW_Z_control_force DW_observ_dgen DW03_shftreg DW_bc_1 DW_bc_2 DW_bc_3 DW_bc_4 DW_bc_5 DW_bc_7 DW_bc_8 DW_bc_9 DW_bc_10 DW_wc_d1_s DW_wc_s1_s DW_INSTRREG DW_tap DW_tap_uc DFT_bistc DFT_codec DFT_xbistc DFT_xcodec DFT_clk_mux DFT_clk_chain DW_mbist_ctrl DW_mbist_wrapper

WHAT NEXT

Reexecute the **define_dft_design** command and specify a valid design name for the **-design_name** argument.

SEE ALSO

find (2), **define_dft_design** (2).

UIT-524 (error) Illegal width %d for pin '%s' of signal type '%s', legal width must be %d.

DESCRIPTION

You receive this error message when you execute the **define_dft_design** command and specify a design pin of invalid width. The **define_dft_design** command is used to specify and characterize a design as a dft design of a type. The dft design pins are checked for legal width according to the specified dft design type.

The legal widths of bus pins for different interface pin types as as follows.

DFT Design Type : TAP

instructions = 32-bit tap_state = 16-bit

DFT Design Type : TAP_UC

instructions = 32-bit tap_state = 16-bit user_code_val = 32-bit ver = 4-bit part_num = 16-bit mnfr_id = 11-bit

WHAT NEXT

Reexecute the **define_dft_design** command and specify a valid design with bus pins of legal width.

SEE ALSO

find (2), **define_dft_design** (2).

UIT-525 (error) Incorrect syntax specified for list param, list param should be terminated with end_list

DESCRIPTION

You receive this error message when you execute the **define_dft_design** command and specify a list parameter with no list terminator. The syntax of a list paramter is as follws.

<parameter name> <parameter type> <param value1> <param value2> ... end_list

where <parameter type> is string .

WHAT NEXT

Reexecute the **define_dft_design** command and specify the correct syntax for list parameters.

SEE ALSO

define_dft_design (2).

UIT-530 (error) Specified pin '%s' is not found in the current design.

DESCRIPTION

You receive this error message when you execute the **set_bsd_instruction** command and specify a pin name that does not exist in the current design.

WHAT NEXT

Reexecute the **set_bsd_instruction** command and specify a valid pin name.

SEE ALSO

find (2), **set_bsd_instruction** (2).

UIT-531 (error) Register '%s' can't be used with standard instruction(s) : %s .

DESCRIPTION

You receive this error message when you execute the **set_bsd_instruction** command and specify an incorrect register name for a standard instruction.

Here are the standard instructions and the corresponding register names.

EXTEST BOUNDARY EXTEST_PULSE BOUNDARY EXTEST_TRAIN BOUNDARY SAMPLE BOUNDARY PRELOAD BOUNDARY INTEST BOUNDARY

BYPASS BYPASS HIGHZ BYPASS CLAMP BYPASS

IDCODE DEVICE_ID USERCODE DEVICE_ID

This error message is issued when a non standard register is specified for a standard instruction.

WHAT NEXT

Reexecute the **set_bsd_instruction** command and specify thye correct register name.

SEE ALSO

find (2), **set_bsd_instruction** (2).

UIT-532 (error) Invalid Input Clock Conditioning '%s' specified.

DESCRIPTION

You receive this error message when you execute the **set_bsd_instruction** command and specify an incorrect input clock conditioning value.

Here are the allowed values for input clock conditioning.

PI

TCK

WHAT NEXT

Reexecute the **set_bsd_instruction** command and specify thye correct input clock conditioning value with option -input_clock_condition.

SEE ALSO

find (2), **set_bsd_instruction** (2).

UIT-533 (error) Invalid Output Conditioning '%s' specified.

DESCRIPTION

You receive this error message when you execute the **set_bsd_instruction** command and specify an incorrect out conditioning value.

Here are the allowed values for output conditioning.

BSR

HIGHZ

NONE

WHAT NEXT

Reexecute the **set_bsd_instruction** command and specify thye correct output conditioning value with option -output_condition.

SEE ALSO

find (2), **set_bsd_instruction** (2).

UIT-534 (error) Input Clock Conditioning can't be specified for a short BSR chain instruction.

DESCRIPTION

You receive this error message when you execute the **set_bsd_instruction** command and specify input clock conditioning for an instruction that selects a short BSR chain.

WHAT NEXT

Reexecute the **set_bsd_instruction** command with out input clock conditioning.

SEE ALSO

find (2), **set_bsd_instruction** (2).

UIT-535 (error) Output Conditioning can’t be specified for a short BSR chain instruction.

DESCRIPTION

You receive this error message when you execute the **set_bsd_instruction** command and specify output conditioning for an instruction that selects a short BSR chain.

WHAT NEXT

Reexecute the **set_bsd_instruction** command with out output conditioning.

SEE ALSO

find (2), **set_bsd_instruction** (2).

UIT-536 (error) Invalid Excluded BSR Conditioning ’%s’ specified.

DESCRIPTION

You receive this error message when you execute the **set_bsd_instruction** command and specify an incorrect excluded bsr cell onditioning value.

Here are the allowed conditioning values for BSR cells excluded from the current instruction.

CLAMP

NONE

WHAT NEXT

Reexecute the **set_bsd_instruction** command and specify thye correct excluded bsr conditioning value with option -excluded_bsr_condition.

SEE ALSO

find (2), **set_bsd_instruction** (2).

UIT-537 (error) Excluded BSR Conditioning can’t be specified for a non short BSR chain instruction.

DESCRIPTION

You receive this error message when you execute the **set_bsd_instruction** command and specify excluded bsr conditioning for an instruction that doesn’t select a short BSR chain.

WHAT NEXT

Reexecute the **set_bsd_instruction** command with out excluded bsr conditioning.

SEE ALSO

find (2), **set_bsd_instruction** (2).

UIT-538 (error) Invalid BSR chain name ’%s’.

DESCRIPTION

You receive this error message when you execute the **set_bsd_path** command in DB mode or **set_scan_path** command in XG mode and specify a reserved name as the BSR chain(path) name.

Here are the reseved names that are not allowed for BSR chains.

BYPASS DEVICE_ID BOUNDARY (allowed in XG mode) STT_REG

WHAT NEXT

Reexecute the command and specifiy a different name for BSR chain name.

SEE ALSO

find (2), **set_bsd_path** (2), **set_scan_path** (2).

UIT-539 (error) Conflicting BSD register name ’%s’.

DESCRIPTION

You receive this error message when you execute the **set_bsd_register** command in DB

mode or **set_scan_path** command in XG mode and specify a conflicting name as the BSD register name. The name is also used to describe a short BSR chain.

WHAT NEXT

Reexecute the command and specifiy a different name for BSD register name.

SEE ALSO

find (2), **set_bsd_register** (2), **set_scan_path** (2).

UIT-540 (error) Conflicting BSR chain name '%s'.

DESCRIPTION

You receive this error message when you execute the **set_bsd_path** command in DB mode or **set_scan_path** command in XG mode and specify a conflicting name as the BSR chain name. The name is also used to describe a short BSD register.

WHAT NEXT

Reexecute the command and specifiy a different name for BSR chain name.

SEE ALSO

find (2), **set_bsd_path** (2), **set_scan_path** (2).

UIT-541 (warning) Unable to find the bsr cell for '%s', ignoring the member.

DESCRIPTION

You receive this error message when you execute the **set_bsd_path** command in DB mode or **set_scan_path** command in XG mode and specify a short BSR chain and a member of the short chain doesn't point to a valid BSR cell.

Please note that input/output/control BSR cells of a tristate/bidir ports can included seprately in a short BSR chain only if they are defined.

EX:-

set_bsd_data_cell -function input -port out set_bsd_data_cell -function output -port out set_bsd_control_cell CTRL1 -type BC_1 -port out

set_bsd_path -name SHORT_BSR1 { out/in out1 out/out out3 CTRL1 }

Individual BSR cells of BSR embedded pads can’t be included in a short BSR chain, either alll of embedded BSR cells can be included in a short BSR chain or none.

WHAT NEXT

Reexecute the command and specifiy a valid BSR cell name.

SEE ALSO

find (2), **set_bsd_path** (2), **set_scan_path** (2).

UIT-542 (error) Invalid or missing %s Condition specified for standard instructions : %s .

DESCRIPTION

You receive this error message when you execute the **set_bsd_instruction** command and specify **-input_clock_condition** or f-output_condition options. These options are not allowed for the following standard instructions.

EXTEST EXTEST_PULSE EXTEST_TRAIN SAMPLE PRELOAD BYPASS HIGHZ CLAMP IDCODE USERCODE

The standard predefines condition if any required for these instuctions and user is not allowed to change that.

You also see this error message for INTEST or RUNBIST instructions if **-input_clock_condition** or f-output_condition options are not specified or incorrect value specified for the option f-output_condition.

The standard allows only BSR or HIGHZ output condition for these instructions.

There are no restrictions on output condition for user defined instructions.

WHAT NEXT

Reexecute the command with the correct options.

SEE ALSO

set_bsd_instruction (2).

UIT-543 (error) Invalid bit '%c' specified in capture value.

DESCRIPTION

You receive this error message when you execute the **set_bsd_instruction** command and specify **-capture_value** option and specify an invalid capture value string.

The format of capture value string is as follows.

nn'bXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

where nn is between 1 and 32 and X can be 0 or 1, -

nn'hXXXXXXXX

where nn is betweeen 1 and 32 and X can be 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, a, A, b, B, c, C, d, D, e, E, f, F, -

WHAT NEXT

Reexecute the command with correct capture value.

SEE ALSO

set_bsd_instruction (2).

UIT-544 (error) Invalid capture value length '%d'.

DESCRIPTION

You receive this error message when you execute the **set_bsd_instruction** command and specify **-capture_value** option and specify an invalid capture value string.

The format of capture value string is as follows.

nn'bXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

where nn is between 1 and 32 and X can be 0 or 1, -

nn'hXXXXXXXX

where nn is between 1 and 32 and X can be 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, a, A, b, B, c, C, d, D, e, E, f, F, -

The bit stream length in binary form can't exceed 32.

WHAT NEXT

Reexecute the command with correct capture value.

SEE ALSO

set_bsd_instruction (2).

UIT-545 (error) Invalid LSB for IDCODE capture value.

DESCRIPTION

You receive this error message when you execute the **set_bsd_instruction** command and specify **-capture_value** option and specify an invalid capture value string. The LSB bit of the capture value string for IDCODE instruction should be ’1’.

WHAT NEXT

Reexecute the command with correct capture value.

SEE ALSO

set_bsd_instruction (2).

UIT-546 (error) BSD Test Data Register length is mandatory, specify the length with -exact_length option.

DESCRIPTION

You receive this error message when you execute the **set_scan_path** command in XG mode to specify a Test Data Register(TDR) and don’t specify the length of the Test Data Register.

WHAT NEXT

Reexecute the command and specifiy the length of the TDR using -exact_length option.

SEE ALSO

set_scan_path (2).

UIT-547 (error) One of the options -ordered_elements or -hookup_elements is mandatory for BSD.

DESCRIPTION

You receive this error message when you execute the **set_scan_path** command in XG mode to specify a BSR chain or Test Data Register(TDR) and don’t specify either of the required options.

In view spec, option -ordered_elements is used to specify a BSR chain.

In view spec/existing_dft, option -hookup_elements is used to specify a TDR.

WHAT NEXT

Reexecute the command and specifiy either of the options as required.

SEE ALSO

set_scan_path (2).

UIT-548 (error) Options -ordered_elements, -hookup_elements are mutually exclusive for BSD.

DESCRIPTION

You receive this error message when you execute the **set_scan_path** command in XG mode to specify a BSR chain or Test Data Register(TDR) and specify both of the above options. These options are mutually exclusive, specify only one of the options.

In view spec, option -ordered_elements is used to specify a BSR chain.

In view spec/existing_dft, option -hookup_elements is used to specify a TDR.

WHAT NEXT

Reexecute the command and specifiy only one of the above options as required.

SEE ALSO

set_scan_path (2).

UIT-549 (error) BSR chains can not be specified in view existing_dft.

DESCRIPTION

You receive this error message when you execute the **set_scan_path** command in XG mode in view existing_dft to specify a BSR chain. BSR chains can not be specified in view existing_dft.

BSR chains can be specified in view spec using the option -ordered_elements in conjunction with the option -class bsd.

WHAT NEXT

Fix the error and reexecute the command.

SEE ALSO

set_scan_path (2).

UIT-550 (error) Invalid argument in the capture value list. '%s' is not a valid design pin, sized binary or a sized hexadecimal constant.

DESCRIPTION

This error message occurs when an invalid value is specified in the capture value argument list for the USERCODE instruction. The 32-bit capture value can be specified as any combination of design pin(s), sized binary constant(s), and/or sized hexadecimal constant(s).

Specify binary and hexadecimal constants using the following Verilog syntax:

```
<size>'[b|B|h|H]<binary or hexadecimal value>
```

For example, the following is a valid USERCODE specification:

```
set_bsd_instruction USERCODE -code {0110}
   -capture_value {version_reg/v3, version_reg/v2, version_reg/v1, \
   version_reg/v0, 16'b1111111110000000, 12'h2ab}
```

WHAT NEXT

Check and correct the capture value argument syntax. Specify design pins as full hierarchical pin names.

SEE ALSO

set_bsd_instruction(2)

UIT-551 (error) Invalid size %d of the capture value argument '%s'. Capture value argument's size should be in the range of 1 to 32 bits.

DESCRIPTION

This error message occurs when you specify a binary or hexadecimal constant value in the capture value argument list, and the size of the argument is not in the valid range of 1 to 32 bits.

Specify binary and hexadecimal constants using the following Verilog syntax:

```
<size>'[b|B|h|H]<binary or hexadecimal value>
```

For example, the following is a valid USERCODE specification:

```
set_bsd_instruction USERCODE -code {0110}
   -capture_value {version_reg/v3, version_reg/v2, version_reg/v1, \
   version_reg/v0, 16'b1111111110000000, 12'h2ab}
```

WHAT NEXT

Check and correct the size of the capture value argument, and run the command again.

SEE ALSO

set_bsd_instruction(2)

UIT-552 (error) %s capture value '%s' cannot be represented in the specified %d bits.

DESCRIPTION

This error message occurs when you specify a binary or hexadecimal constant value in the capture value argument list and the specified size of the argument is not sufficient to represent the specified value.

Specify binary and hexadecimal constants using the following Verilog syntax:

```
<size>'[b|B|h|H]<binary or hexadecimal value>
```

For example, the following is a valid USERCODE specification:

```
set_bsd_instruction USERCODE -code {0110}
   -capture_value {version_reg/v3, version_reg/v2, version_reg/v1, \
   version_reg/v0, 16'b1111111110000000, 12'h2ab}
```

WHAT NEXT

Check and correct the size of the capture value argument, and run the command again.

SEE ALSO

set_bsd_instruction(2)

UIT-553 (error) A %s value is specified as the capture value. Capture value must be a 32-bit value.

DESCRIPTION

This error message occurs when the cumulative bit width of the arguments specified in the **-capture_value** option of the **set_bsd_instruction** command is not 32 bits. The 32-bit capture value can be specified as any combination of design pin(s), sized binary constant(s), and/or sized hexadecimal constant(s).

Specify binary and hexadecimal constants using the following Verilog syntax:

```
<size>'[b|B|h|H]<binary or hexadecimal value>
```

For example, the following is a valid USERCODE specification:

```
set_bsd_instruction USERCODE -code {0110}
   -capture_value {version_reg/v3, version_reg/v2, version_reg/v1, \
   version_reg/v0, 16'b1111111110000000, 12'h2ab}
```

WHAT NEXT

Check and correct the size of the capture value argument, and run the command again.

SEE ALSO

set_bsd_instruction(2)

UIT-554 (error) '%s' cell does not exist in the design.

DESCRIPTION

This error message occurs when the cell that was specified as part of of the *state_cells* argument of the **set_tap_elements** command, cannot be found.

Typographical or spelling errors often cause this type of error message.

WHAT NEXT

Use the **find** command to list the cells in your design, and rerun the **set_tap_elements** command using the name of a valid cell.

SEE ALSO

set_tap_elements(2)

UIT-555 (error) Invalid data. Recheck the file format or type.

DESCRIPTION

This error message indicates that an invalid data is read with the **read_bsdl** command. This might happen when a BSDL file read is not in proper unix format. You might observe this for files transferred from different platforms or operating systems.

WHAT NEXT

Check the file type using unix **file** command. Recheck the BSDL file data.

SEE ALSO

read_bsdl (2).

UIT-580 (error) The test_modes value, %s, specified is not a valid value.

DESCRIPTION

The -test_modes option requires a valid integer number of modes required in the design.

WHAT NEXT

UIT-581 (error) The client %s specified is not a valid dft client.

DESCRIPTION

You receive this message if you issue **set_dft_configuration -order** and specify an invalid value for the **-order** option argument. Valid values are *autofix*, to specify the Autofix utility as dft client; or *wrapper*, to specify the Shadow LogicDFT utility as dft client. For more information, see the manual page for the **set_dft_configuration** command.

WHAT NEXT

Reissue **set_dft_configuration -order** with a valid value for the **-order** option argument.

SEE ALSO

set_dft_configuration (2).

UIT-582 (error) Core Integration of cores is mutually exclusive with options : -shadow_wrapper | -core_wrapper | -testability | -mbist | -scan_compression .

DESCRIPTION

You receive this message if you issue **set_dft_configuration -core_integration** and also specify one of the following options. *-shadow_wrapper -core_wrapper -testability -mbist -scan_compression* UI option *-core_integration* is mutually exclusive with the above options. For more information, see the manual page for the **set_dft_configuration** command.

WHAT NEXT

Reissue **set_dft_configuration** command with valid options.

SEE ALSO

set_dft_configuration (2).

UIT-583 (error) Core Integration of MBIST cores doesn’t support the options : -clock_controller | -bist .

DESCRIPTION

You receive this message if you issue **set_dft_configuration -core_integration** and also specify one of the following options. *-bist -clock_controller* UI option *-core_integration* is mutually exclusive with the above options when the design contains MBIST(Tech2) cores. UI option *-core_integration* is mutually exclusive with the option *-clock_controller* when the design contains MBIST(Tech1) cores. For more information, see the manual page for the **set_dft_configuration** command.

WHAT NEXT

Reissue **set_dft_configuration** command with valid options.

SEE ALSO

set_dft_configuration (2).

UIT-584 (error) Object ’%s’ is not valid, it’s either not found or not a cell of current design, ’%s’.

DESCRIPTION

Object specified in the command has to be present as a cell under the current design.

WHAT NEXT

Check whether the name of the object is correct and current design is specified correctly.

UIT-587 (error) Cell ’%s’ doesn’t have a test model.

DESCRIPTION

Cell specified in the command should have a test model. The specification can’t be executed if there is no test model for the specified cell.

WHAT NEXT

Check whether the name of the cell is correct and it has a test model. Correct the specification and reexecute the command. Note that test model can be attached to a cell using read_test_model command.

SEE ALSO

set_core_integration_configuration (2), **read_test_model** (2).

UIT-588 (error) MBIST(Tech2) encapsulated core modes can't be used with set_test_target command.

DESCRIPTION

You receive this message if you issue **set_test_target** command and also specify an encapsulated MBIST(Tech2) core mode with *-cores* option. DFT architect creates a single top level mode to target all MBIST(Tech2) encapsulated core modes of the same type and user can't change this behavior with set_test_target command. The name of such a test mode can be controlled with *define_test_mode* and *set_dft_logic_usage* commands.

WHAT NEXT

Don't specify **set_test_target** command with MBIST(Tech2) core modes.

SEE ALSO

set_test_target (2), **define_test_mode** (2), **set_dft_logic_usage** (2).

UIT-590 (error) A configuration for port %s already exits.

DESCRIPTION

The **set_port_configuration** command has previously been specified for this port.

WHAT NEXT

Check to see if the **set_port_configuration** command has previously been specified for this port.

UIT-591 (error) Duplicate control specification for %s data port of %s.

DESCRIPTION

The **set_port_configuration** command has previously been specified for this port.

WHAT NEXT

Verify that the **set_port_configuration** command has previously been specified for this port.

UIT-592 (error) %s has a clock port specified for it that is different from the port specified in the command.

DESCRIPTION

A previous **set_port_configuration** command has specified a different clock port for this port.

WHAT NEXT

Check if the **set_port_configuration** command has previously been used to specify a clock for this port.

UIT-593 (error) %s specified as clock port in the command does not exist on the cell

DESCRIPTION

You receive this message if you issue the **set_port_configuration** command and the clock port you specified was not found on the specified cell. This could be caused by a spelling error or typo.

WHAT NEXT

Verify that the port exists on the cell, and verify the correct spelling. Then reexecute **set_port_configuration**.

SEE ALSO

set_port_configuration (2).

UIT-594 (error) Multiple ports named %s on Object %s

DESCRIPTION

You receive this message if you execute **set_port_configuration** and specify a port name that occurs more than once on the specified object. There can be only one port associated with a given port name.

WHAT NEXT

Examine the library description of the cell to determine why there are two ports with the same name. Ensure that there is only one port associated with each port name. Then reexecute **set_port_configuration**.

SEE ALSO

set_port_configuration (2).

UIT-595 (error) The read control pattern is not paired (port value)

DESCRIPTION

You receive this message if you issue the **set_port_configuration** command with the **-read** option, and a *signal_value_pin_pairs* argument to **-read** does not contain two values. Each **-read** argument must be a pair that includes both a signal value and the name of the input pin associated with that value. One of those values is missing.

WHAT NEXT

Examine your execution of **set_port_configuration** for an unpaired pin name or signal value. Reexecute **set_port_configuration -read** and ensure that all arguments to **-read** are signal_value/pin_name pairs.

SEE ALSO

set_port_configuration (2).

UIT-596 (error) port %s not found on %s

DESCRIPTION

You receive this message if you issue **set_port_configuration** and the *port_name* cannot be found on the specified object. This could be caused by a spelling error or typo.

WHAT NEXT

Verify that the port exists on the object, and verify the correct spelling. Then reexecute **set_port_configuration**.

SEE ALSO

set_port_configuration (2).

UIT-597 (error) Illegal value %s speicified in the read control for port %s

DESCRIPTION

You receive this message if you issue the **set_port_configuration** command with the **-read** option and specify an illegal value for the *signal_value* part of the *signal_value_pin_pairs* argument pair. *signal_value* can have values of only 0 or 1.

WHAT NEXT

Reexecute **set_port_configuration -read** with a valid value for *signal_value*.

SEE ALSO

set_port_configuration (2).

UIT-598 (error) Illegal direction for port %s

DESCRIPTION

You receive this message if you issue the **set_port_configuration** command with the **-read** option and specify a non-input port as the control port of the *signal_value_pin_pairs* argument. You can specify only input ports.

WHAT NEXT

Reexecute **set_port_configuration -read** using the name of an input port as the control port for the *signal_value_pin_pairs* argument.

SEE ALSO

set_port_configuration (2).

UIT-599 (error) port %s has already been specified in the read control pattern

DESCRIPTION

You receive this message if you issue the **set_port_configuration** command with the **-read** option and the specified port name appears more than once in the list of *signal_value_pin_pairs*. Each port name can be used only once.

WHAT NEXT

Reexecute **set_port_configuration -read** without duplicating any port names in the *signal_value_pin_pairs* arguments.

SEE ALSO

set_port_configuration (2).

UIT-600 (error) %s, %s specification conflicts with previous value specified on %s

DESCRIPTION

You receive this message if you issue the **set_port_configuration** command with the **-read** option and a signal value assigned to a pin as one of the *signal_value_pin_pairs* conflicts with the value already assigned to that pin through a previous execution of **set_port_configuration**. Each pin can have only one value assigned to it.

WHAT NEXT

Remove the ealier specification using remove_port_configuration command if the previous specification was incorrect and then issue both correct set_port_configuration commands. If the current specification is wrong then reissue

only the current command with correct specification.

UIT-601 (error) cound not find object named %s

DESCRIPTION

You receive this message if you issue **set_port_configuration** or **remove_port_configuration** and the specified object cannot be found in the design. This could be caused by the wrong current design setting, or by a spelling error or typo.

WHAT NEXT

Verify that the current design is set as intended. Verify that the object exists in the design, and verify the correct spelling. Then reexecute the command.

SEE ALSO

remove_port_configuration (2), **set_port_configuration** (2).

UIT-602 (error) %s is an output port. It can’t have an write control.

DESCRIPTION

You receive this message if you issue the **set_port_configuration** command with the **-write** option and specify an output port as a control port for the *signal_value_pin_pairs* argument. You can specify only input ports as control ports.

WHAT NEXT

Reexecute **set_port_configuration -write** using the name of an input port as part of the *signal_value_pin_pairs* argument.

SEE ALSO

set_port_configuration (2).

UIT-603 (error) The read control pattern is missing or empty

DESCRIPTION

You receive this message if you issue the **set_port_configuration** command with the **-tristate** option and do not specify a read control using the **-read** option. A tristate port must have a read control.

WHAT NEXT

Reexecute **set_port_configuration** and use the **-read** option to specify a read control for the tristate port.

SEE ALSO

set_port_configuration (2).

UIT-604 (error) The current design does not exist

DESCRIPTION

You receive this message if you issue the **set_port_configuration** command and the specified current design cannot be found in memory. This could be caused by a spelling error or typo.

WHAT NEXT

Verify that the current design exists in memory, and verify the correct spelling. If necessary, load the design into memory or respecify using **current_design**. Then reexecute **set_port_configuration**.

SEE ALSO

current_design (2), **set_port_configuration(2).**

UIT-605 (error) The direction of port %s is missing

DESCRIPTION

You receive this message if you issue the **set_wrapper_element** command and do not supply a direction for the specified port. Each port must have a specified direction.

WHAT NEXT

Check the model for the cell, and find out the port direction. Then reexecute **set_wrapper_element** and specify the direction of the port.

SEE ALSO

set_wrapper_element (2).

UIT-606 (error) The port configuration information is missing for %s

DESCRIPTION

You receive this message if you issue **set_wrapper_element** and the specified port does not have port configuration information. Each port must either be modeled using Library Compiler's memory syntax, or the port interface must be described using **set_port_configuration** for each output or bidirectional port.

WHAT NEXT

Either modify the module description in the library or provide the interface information using the **set_port_configuration** command. Then reexecute **set_wrapper_element**.

SEE ALSO

set_wrapper_element (2), **set_port_configuration** (2).

UIT-607 (error) No objects specified in the command

DESCRIPTION

You receive this message if you issue **set_wrapper_element** and do not specify an object. You must specify at least one object.

WHAT NEXT

Reexecute **set_wrapper_element** and specify at least one object.

SEE ALSO

set_wrapper_element (2).

UIT-608 Wrapper attribute not found on %s

DESCRIPTION

You receive this message if you issue the **remove_wrapper_element** command and the **wrapper_element** attribute was not found on the specified object. You can remove the **wrapper_element** attribute from an object only if the attribute has been set on that object using the **set_wrapper_element** command.

You might not have been aware that the specified object did not have the attribute; or you might have inadvertently specified the wrong object when you executed the **remove_wrapper_element** command.

WHAT NEXT

Determine whether the object specified in this warning message is the object from which you intended to remove the **wrapper_element** attribute. If necessary, reexecute the **remove_wrapper_element** command and specify only objects on which the **wrapper_element** attribute has been set.

SEE ALSO

remove_wrapper_element (2), **set_wrapper_element** (2).

UIT-609 (error) %s is an output port; can’t have a write control

DESCRIPTION

You receive this message if you issue the **set_port_configuration** command with the **-write** option and specify an output port as part of the *signal_value_pin_list* argument. Only input ports can have write control.

WHAT NEXT

Verify the correct spelling of the input ports you want to use as control ports. Then reexecute **set_port_configuration** and specify only input ports as part of the **-write** *signal_value_pin_list* argument.

SEE ALSO

set_port_configuration (2).

UIT-610 (error) Illegal object type. Need reference or design

DESCRIPTION

Only reference of design can be specified in the command. You receive this message if you issue **set_port_configuration** or **remove_port_configuration** with an illegal object type as part of the *cell_design_ref_list* argument. Objects can be only cells, designs, or references.

WHAT NEXT

Reexecute the command and specify only cells, designs, or references for the *cell_design_ref_list* argument.

SEE ALSO

remove_port_configuration (2), **set_port_configuration** (2).

UIT-611 (error) Black_boxes are not supported.

DESCRIPTION

Only modules with descriptions or empty boxes are supported by the command.

WHAT NEXT

create an empty box i.e. an interface description for the module in the design.

UIT-612 (error) Port %s not found on %s

DESCRIPTION

Port specified in the command should be there on the cell specified for command to be successful.

WHAT NEXT

check whether cell name and port name are correct.

UIT-613 (error) Object %s not found in %s

DESCRIPTION

Object specified in the command has to be present under the current design.

WHAT NEXT

Check whether the name of the object is correct and current design is specified correctly.

UIT-614 (error) Wrapping a constant is not supported

DESCRIPTION

The module to be wrapped has to be a non-constant.

WHAT NEXT

Check whether name of the object is correct.

UIT-615 (warning) %s has already been specified for wrapping

DESCRIPTION

An Object can be specified for wrapping only once. You receive this message if you issue the **set_wrapper_element** command and the **wrapper_element** attribute is already set on the specified object. You can set the **wrapper_element** attribute only once on a given object.

You might not have been aware that the specified object already had the attribute, or you might have inadvertently specified the wrong object, when you executed the **set_wrapper_element** command.

WHAT NEXT

Determine whether the object specified in this warning message is the object on which you intended to set the **wrapper_element** attribute. If necessary, reexecute the **set_wrapper_element** command and specify only objects on which the **wrapper_element** attribute has not already been set.

SEE ALSO

set_wrapper_element (2).

UIT-616 (warning) %s has already been wrapped

DESCRIPTION

An object can be wrapped only once.

WHAT NEXT

Check whether the object name is correct.

UIT-617 (warning) %s has already been specified as clock port for %s port

DESCRIPTION

Duplicate specification is detected.

WHAT NEXT

Check the names of clock port and data port.

UIT-618 (error) '%d' is not a valid value for %s option of the rtldrc command.

DESCRIPTION

You receive this message when you have assigned an invalid value to the **-max_detail_lines** option for the **rtldrc** command. The value must be greater than or equal to 0.

WHAT NEXT

Reexecute the **rtldrc** command using a valid value.

UIT-619 (error) '%s' is not a valid disabling option for a tristate net.

DESCRIPTION

You receive this message if you issue **set_scan_configuration** or **set_scan_tristate** with an invalid value for the scan shift tristate disabling option for internal or external tristate nets. Valid values for the tristate disabling option in scan shift are *enable_one*, disable_all, or *no_disabling*.

WHAT NEXT

Reissue the **set_scan_tristate** or **set_scan_configuration** command and specify a valid scan shift disabling option for tristate nets in the design.

SEE ALSO

insert_scan (2), **set_scan_configuration** (2), **set_scan_tristate** (2).

UIT-620 (information) Writing the disable option for the tristate net '%s'.

DESCRIPTION

You receive this message to inform you that the **set_scan_tristate** command is writing to the persistent database the scan shift disabling option you specified for this tristate net.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

insert_scan (2), **set_scan_configuration** (2), **set_scan_tristate.**

UIT-621 (warning) Overwriting the disable option for the tristate

net ’%s’.

DESCRIPTION

You receive this message to inform you that there was already a scan shift disabling option set for this tristate net, and that setting is being overwritten by the scan shift disabling option you just specified using the **set_scan_tristate** command.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_scan (2), **remove_scan_specification** (2), **set_scan_configuration** (2), **set_scan_tristate** (2).

UIT-622 (error) The ’%s’ object is a ’%s’.

DESCRIPTION

You receive this message if you issue the **set_scan_tristate** command and the *net_list* argument includes the name of an object that is not a net. You can specify only net names with the **set_scan_tristate** command.

WHAT NEXT

Reissue the **set_scan_tristate** command and specify a *net_list* argument that lists only net names.

SEE ALSO

set_scan_tristate (2).

UIT-623 (error) ’%s’ is not a bidirectional port.

DESCRIPTION

You receive this message if you issue the **set_scan_bidi** command and the *port_list* argument includes the name of an object that is not a bidirectional port. You can specify only bidirectional ports with the **set_scan_bidi** command.

WHAT NEXT

Reissue the **set_scan_bidi** command and specify a *port_list* argument that lists only bidirectional port names.

SEE ALSO

set_scan_bidi (2).

UIT-624 (information) Writing the mode in scan shift for the bidirectional port '%s'.

DESCRIPTION

You receive this message to inform you that the **set_scan_bidi** command is writing to the persistent database the scan shift mode you specified for this bidirectional port.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

insert_scan (2), **set_scan_configuration** (2), **set_scan_bidi** (2).

UIT-625 (warning) Overwriting the mode in scan shift for the bidirectional port '%s'.

DESCRIPTION

You receive this message to inform you that there was already a scan shift mode set for this bidirectional port, and that setting is being overwritten by the scan shift mode you just specified using the **set_scan_bidi** command.

WHAT NEXT

No action is required on your part.

SEE ALSO

insert_scan (2), **remove_scan_specification** (2), **set_scan_bidi** (2),

set_scan_configuration (2).

UIT-626 (error) '%s' is not a valid disabling option for internal tristate nets.

DESCRIPTION

You receive this message if you issue **set_scan_configuration** with an invalid value of the scan shift tristate disabling option for internal tristate nets. Valid values are *disable_all*, *enable_one* (the default) or *no_disabling*.

WHAT NEXT

Reissue the **set_scan_configuration** command and specify a valid scan shift tristate disabling option for internal tristate nets in the design.

SEE ALSO

insert_scan (2), **set_scan_configuration** (2).

UIT-627 (error) '%s' is not a valid value for the **-prtool** option argument.

DESCRIPTION

You receive this message if you execute **set_scan_configuration** with an incorrect argument for the **-prtool** option. Currently allowed values are *cadence* and *avant*.

WHAT NEXT

Reissue the **set_scan_configuration** command with one of the allowed values for the **-prtool** option argument.

SEE ALSO

set_scan_configuration (2).

UIT-628 (warning) The design '%s' is not scan completed and

cannot be represented with a test model.

DESCRIPTION

Only a scan completed design may be represented using a test model. You have specified a design that is not scan completed as a scan core.

WHAT NEXT

Make sure that your design is scan completed and re-issue the **set_scan_core** command.

UIT-630 (error) Pin '%s' is not sticky.

DESCRIPTION

You receive this message if you issue the **set_rtl_load** command and specify a pin that is not sticky. A sticky pin is a pin or port that is guaranteed to be persistent throughout the early stages of optimization, so that annotated capacitance and resistance can "stick" to those pins and not be lost. You can perform **set_rtl_load** only on sticky pins, or on nets connected to sticky pins.

For a complete explanation of sticky pins, see the manual page for the **set_rtl_load** command.

WHAT NEXT

If you want to set an RTL load value on the specified pin, you must make it sticky; you can do so by using **set_dont_touch** or set_size_only on the pin. Then reissue the **set_rtl_load** command.

If you do not need to set an RTL load on the specified pin, remove it from the *pin_net_list* and reissue the **set_rtl_load** command.

SEE ALSO

set_dont_touch (2), **set_rtl_load** (2), **set_size_only** (2).

UIT-631 (error) Net '%s' has no sticky pins.

DESCRIPTION

You receive this message if you issue the **set_rtl_load** command and specify a net that has no sticky pins. A sticky pin is a pin or port that is guaranteed to be persistent throughout the early stages of optimization, so that annotated

capacitance and resistance can "stick" to those pins and not be lost. You can perform **set_rtl_load** only on sticky pins, or on nets connected to sticky pins.

For a complete explanation of sticky pins, see the manual page for the **set_rtl_load** command.

WHAT NEXT

If you want to set an RTL load value on the specified net, you must make one or more pins of the net sticky. You can make pins sticky by using **set_dont_touch** or set_size_only; alternatively, you can make the net sticky by using **set_dont_touch** on the net. Then reissue the **set_rtl_load** command.

If you do not need to set an RTL load on the specified net, remove it from the *pin_net_list* and reissue the **set_rtl_load** command.

SEE ALSO

set_dont_touch (2), **set_rtl_load** (2), **set_size_only** (2).

UIT-632 (error) You must specify at least a capacitance or resistance value.

DESCRIPTION

You receive this message if you issue the **set_rtl_load** command and do not specify a capacitance or a resistance value on the pin or net. You must specify at least one; otherwise, the command has no effect. For more information, see the manual page for the **set_rtl_load** command.

WHAT NEXT

Reissue the **set_rtl_load** command and specify a capacitance or resistance value, or both, using the **-cap** *cvalue* or **-res** *rvalue* arguments.

SEE ALSO

set_rtl_load (2).

UIT-633 (error) You must specify a net or pin object or -all.

DESCRIPTION

You receive this message if you issue the **remove_rtl_load** command and do not specify

either **-all** or *pin_net_list*. You must specify one or more target objects on which the **remove_rtl_load** command is to operate.

WHAT NEXT

Reissue the **remove_rtl_load** command and specify either **-all** or *pin_net_list*.

SEE ALSO

remove_rtl_load (2), **set_rtl_load** (2).

UIT-634 (error) You must specify either or both of the **-capacitance** and **-delay** options.

DESCRIPTION

You receive this message if you issue the **calculate_rtl_load** command without either the **-capacitance** or **-delay** option. At least one of these options is required, and you can specify both.

WHAT NEXT

Reissue the **calculate_rtl_load** command and specify at least one of the **-capacitance** and **-delay** options.

SEE ALSO

calculate_rtl_load.2

UIT-635 (error) Net '%s' must have a set_load value.

DESCRIPTION

You receive this message if you issue **calculate_rtl_load -capacitance** and the specified net does not have a **set_load** value on it. In order for the **-capacitance** option to be processed, you must have previously placed a **set_load** value on the specified net, or on the net that is connected to the specified pin.

WHAT NEXT

Set a load on the specified net using **set_load**. Then reissue the **calculate_rtl_load** command.

SEE ALSO

calculate_rtl_load (2), **set_load** (2).

UIT-650 (warning) A set_test_point_element command has already been specified for the pin %s and for the type %s. The previous set_test_point specification will be deleted and replaced with the current one.

DESCRIPTION

You have used set_test_point_element to set a new test point on pin %s
A user-defined test point specification already exists on that pin. This is a warning message
The previous user-defined test point specification will be deleted.

WHAT NEXT

If you do not want to remove a test point which already exists on the specified pin, do not specify this pin with the set_test_point_element command.

UIT-651 (Information) The previous user-defined test point specification in location %s of type %s is being deleted.

DESCRIPTION

This is an information message. The previous user-defined test point specification in location %s of type %s
is being deleted.

WHAT NEXT

You can specify another test point location with the set_test_point_element command.

UIT-652 (warning) Cell %s has a dont_touch attribute. The asynchronous violation associated with it will not be

autofixed.

DESCRIPTION

You receive this warning message because the asynchronous violation associated with cell %s will not be autofixed because of a **dont_touch** attribute on this cell.

WHAT NEXT

If you are satisfied with this result, no action is required on your part. If you want the asynchronous violation associated with the specified cell to be autofixed, remove the **dont_touch** attribute from the specified cell and rerun autofix.

SEE ALSO

insert_dft (2).

UIT-653 (warning) Cell %s has a dont_touch attribute. The clock violation associated with it will not be autofixed.

DESCRIPTION

You receive this warning message because the clock violation associated with cell %s will not be
autofixed because of a **dont_touch** attribute on this cell.

WHAT NEXT

If you are satisfied with this result, no action is required on your part. If you want the clock violation associated with the specified cell to be autofixed, remove the **dont_touch** attribute from the specified cell.

SEE ALSO

insert_dft (2).

UIT-654 (information) There are %d other cells with the same

violation.

DESCRIPTION

This message summarizes the total number of violations identified in UIT-652 and UIT-653.

WHAT NEXT

This is an informational message. No action is required on your part. For more information, see the manual page for UIT-652 and UIT-653.

SEE ALSO

insert_dft (2).

UIT-655 (warning) Scan style '%s' does not add lockup latches to the scan chain.
Ignoring the set_scan_configuration -insert_end_of_chain_lockup_latch command.

DESCRIPTION

This warning message tells you that you have asked DFT Compiler to add lockup latches to the scan chain but have specified a scan style that is not multiplexed_flip_flop. The compiler is ignoring the **-insert_end_of_chain_lockup_latch** option. Only the multiplexed_flip_flop scan style adds lockup latches to the scan chain.

WHAT NEXT

To avoid receiving this warning message, remove **-insert_end_of_chain_lockup_latch true** from the **set_scan_configuration** option list, or set the scan style to multiplexed_flip_flop.

SEE ALSO

set_scan_configuration (2).

UIT-656 (warning) port '%s' is the wrong direction to be a %s.

DESCRIPTION

This warning message informs you that you tried to set the access point for a register port to something that is inconsistent with its direction. The **set_bsd_register** command lets you specify access points for a user-defined register using boundary scan signal semantics. Ports with signal type "tdo" must be associated with output ports. Ports with all other signal types should not be associated with output ports or tristate ports.

WHAT NEXT

Issue the **set_bsd_register** command and specify a valid access port or signal type.

SEE ALSO

set_bsd_register (2).

UIT-657 (error) Register port list has multiple signal types for hookup point '%s'.

DESCRIPTION

This error message informs that you tried to associate more than one signal type with a port. The **set_bsd_register** command lets you specify ports for user-defined registers using boundary-scan signal semantics. However, you can associate only one signal type with each port.

WHAT NEXT

Use the **set_bsd_register** command and specify only one signal type per port.

SEE ALSO

set_bsd_register (2).

UIT-658 (warning) Port specification is not paired. Last

specification is incomplete and is discarded.

DESCRIPTION

This warning message informs you that you specified an incomplete port with the **set_bsd_register** command. The **set_bsd_register** command lets you specify ports for user-defined registers using boundary-scan signal semantics. Specified ports must be pairs, and each pair must include a signal type and a design port or pin. Incomplete pairs cannot be used to specify ports and are discarded.

WHAT NEXT

To avoid receiving this warning message, remove the last object from the argument list.

SEE ALSO

set_bsd_register (2).

UIT-659 (error) Port type '%s' is repeated.

DESCRIPTION

This error message informs you that multiple ports have been specified for the same signal type in the access list. The **set_bsd_register** command lets you specify ports for user-defined registers using boundary-scan signal semantics. Port signal types "tdi" and "tdo" can be specified multiple times only for register named as **STT_REG**. For all other registers signal types "tdi" and "tdo" can be specified only once. All other signal types can always be repeated.

WHAT NEXT

Run the **set_bsd_register** command and specify only one "tdi" and one "tdo" port if the register is not **STT_REG**. If you want to specify a scan-through-tap register use the reserved name **STT_REG** for the register and reissue the command.

SEE ALSO

set_bsd_register (2).

UIT-660 (error) Access point specification is missing signal type

’%s’.

DESCRIPTION

The **set_bsd_register** command lets you specify access points for a user-defined register with boundary-scan signal semantics. This error is generated because the register cannot be wired correctly without a signal of the designated type.

WHAT NEXT

Rerun the **set_bsd_register** command and include ports for the required signal type using the **-access** option.

SEE ALSO

set_bsd_register (2).

UIT-661 (Error) Missing ports for user-defined BSR or TAP elements.

DESCRIPTION

This error is generated because some of the required access ports for the BSR and TAP elements are missing from the specification. The **set_bsd_bsr_element** or **set_bsd_tap_element** command lets you specify user-defined BSR or TAP elements.

WHAT NEXT

Rerun one of the commands and specify all required access ports using the **-access** option. For a list of required access ports, see the man page for the **set_bsd_bsr_element** or **set_bsd_tap_element** commands.

If you are getting this error on set_bsd_tap_element, it might be due to the reason that you are using an old custom tap imlementation and signal type ’instructions’ is missing in the access list. In this case you might want to set the variable ’bsd_use_old_tap’ to true and rerun the command.

SEE ALSO

set_bsd_bsr_element (2), **set_bsd_tap_element** (2).

UIT-662 (error) Mismatched signal types ’tdi’ and ’tdo’.

DESCRIPTION

The **set_bsd_register** command lets you specify access points ’tdi’ and ’tdo’ multiple times for the scan-through-tap register **STT_REG**. This error is generated either because access points ’tdi’ and ’tdo’ do not match in number or because they are not specified in alternate order.

WHAT NEXT

Correct the access points ’tdi’ and ’tdo’ specified in the **-access** option and rerun the **set_bsd_register** command.

SEE ALSO

set_bsd_register (2).

UIT-663 (error) Multiple signal types cannot be specified for hookup port ’%s’.

DESCRIPTION

This error message informs that you tried to associate more than one signal type with a hookup port. The **set_dft_signal** command lets you specify hookup ports for diffrent types. However, you can associate only one signal type with each port.

WHAT NEXT

Use the **set_dft_signal** command and specify only one signal type per hookup port.

SEE ALSO

set_dft_signal (2).

UIT-664 (error) -bsd_style can only be specified with -view spec.

DESCRIPTION

You receive this error message when you execute the **set_scan_path** command in XG mode with view existing_dft and -bsd_style options . -bsd_style can not be specified with view existing_dft.

WHAT NEXT

Fix the error and re-execute the command.

SEE ALSO

set_scan_path (2).

UIT-665 (error) -bsd_style can only be specified for user defined test data registers.

DESCRIPTION

You receive this error message when you execute the **set_scan_path** command with -bsd_style option for Boundary or Short BSR Chains. -bsd_style can be specified for User Defined Test Data Registers only.

WHAT NEXT

Use -bsd_style for User Defined Test Data Registers only.

SEE ALSO

set_scan_path (2).

UIT-666 (warning) Scan-in and scan-out ports for compression mode %s should be specified only in the base mode.

DESCRIPTION

This warning message occurs when scan-in and scan-out ports are specified in the compression mode.

The compression mode specifications are specifically used to guide the tool to build scan chains outside compressor/decompressor in the compression mode. These chains can be specified in the compression mode by using the **set_scan_path command** and assigning the flops to be routed between the external scan-in and scan-out ports.

If you do not intend to build any chains outside compressor/decompressor, specify scan-in and scan-out specifications only in the all_dft mode or the base scan mode.

For example, the following commands instruct the tool to build scan chains outside compressor/decompressor in compression mode:

```
set_dft_signal -type ScanDataIn -port my_si \
  -view spec -test_mode ScanCompression_mode

set_dft_signal -type ScanDataOut -port my_so \
  -view spec -test_mode ScanCompression_mode

set_scan_path my_ext_chain -view spec -scan_data_in my_si \
  -scan_data_out my_so -include_elements {Flop1 Flop2 Flop3} \
  -complete true -test_mode ScanCompression_mode
```

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, use the commands shown above for correct specifications, or remove the scan-in and scan-out specifications from the compression mode and specify them in the all_dft or the base scan mode.

SEE ALSO

set_dft_signal(2)
set_scan_compression_configuration(2)
set_scan_path(2)

UIT-667 (error) Pin name '%s' specified more than once.

DESCRIPTION

This message informs you that you ran the **define_dft_design** command with an access list that specifies a pin name more than once.

WHAT NEXT

Rerun the **define_dft_design** command with a valid access list.

SEE ALSO

insert_bsd (2), **set_bsd_pad_design** (2).

UIT-668 (error) Signal type '%s' specified more than once.

DESCRIPTION

This message informs you that you ran the **define_dft_design** command with an access list that specifies any of the following signal types more than once: data_in,

data_out or enable.

WHAT NEXT

Rerun the **define_dft_design** command after making sure that the signal types viz. data_in, data_out and enable are specified only once.

SEE ALSO

insert_bsd (2), **set_bsd_pad_design** (2).

UIT-669 (error) Polarity high(H) specified more than once for signal type '%s'.

DESCRIPTION

This message informs you that you ran the **define_dft_design** command with an access list that specifies polarity "high" more than once for any of the following signal types: data_in, data_out and port.

WHAT NEXT

Rerun the **define_dft_design** command after making sure that the polarity "high" is specified exactly once if the signal type is data_in, data_out or port.

SEE ALSO

insert_bsd (2), **set_bsd_pad_design** (2).

UIT-670 (error) Polarity low(L) specified more than once for signal type '%s'.

DESCRIPTION

This message informs you that you ran the **define_dft_design** command with an access list that specifies polarity "low" more than once for any of the following signal types: data_in, data_out and port.

WHAT NEXT

Rerun the **define_dft_design** command after making sure that the polarity "low" is specified exactly once if the signal type is data_in, data_out or port.

SEE ALSO

insert_bsd (2), **set_bsd_pad_design** (2).

UIT-671 (warning) Signal type '%s' should not be specified for 'hybrid' PAD. Ignored the specification.

DESCRIPTION

This message informs you that you ran the **define_dft_design** command for a hybrid PAD with an interface list that specifies any of the following signal types: port, data_in, data_out, or enable. These signal types are not used for a hybrid PAD. For a hybrid PAD this information is collected from the **$bsr_segment$** specification of the **-params** option of the **define_dft_design** command.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended you can make sure that the port, data_in, data_out, and enable signal types are not specified for the hybrid PAD, and then run the **define_dft_design** command again.

SEE ALSO

define_dft_design(2)
insert_dft(2)

UIT-700 (warning) Invalid scan state.

DESCRIPTION

This warning message informs you that you have specified an invalid scan state with the **set_scan_state** command.

WHAT NEXT

Rerun the **set_scan_state** command and specify a valid scan state.

SEE ALSO

set_scan_state (2).

UIT-701 (error) Incorrect value of -power_saving_on option argument. Allowed values are true, TRUE; or false, FALSE.

DESCRIPTION

You receive this message if you execute **set_testability_configuration** with an incorrect argument for the **-power_saving_on** option. Allowed values of the **-power_saving_on** option are *true, TRUE; or false, FALSE.*

WHAT NEXT

Re-issue the command with one of the allowed values for the **-power_saving_on** option argument.

SEE ALSO

set_testability_configuration (2).

UIT-702 (warning) '%s' is not an external port and cannot be used to specify a port.

DESCRIPTION

This warning informs you that you used an object other than an external port to specify a port. The **set_test_hold** command allows only external ports to specify ports. Other kinds of objects cannot be used to specify ports and are rejected.

WHAT NEXT

Remove the offending object from the argument list. Use hierarchical instance names, with respect to the top-level design, to locate external ports. Then, rerun the command with a valid external port.

SEE ALSO

set_test_hold (2).

UIT-703 (warning) The test point '%s' is not inserted, because the instance location '%s' does not exist due to insert_dft

optimization.

DESCRIPTION

You receive this warning message if you execute **insert_dft** after the **set_test_point_element** command. The set_test_point_element command allows design objects to specify pin instances on which test points need to be inserted. Some test points might be rejected if their corresponding pin instances do not exist after the optimization.

WHAT NEXT

If the test point is required then use the **set_dont_touch** command to prevent the cell from being modified or replaced during optimization. Another way consists in using **insert_dft** with optimization switched off. Use **-dont_fix_constraints** and **-ignore_compile_design_rules** options to switch off optimization.

UIT-703 (warning) The test point '%s' is not inserted because the instance location '%s' does not exist due to insert_dft optimization.

DESCRIPTION

This messages informs you that the specified test point is rejected because corresponding pin instances do not exist after optimization. You receive this warning message if you use the **insert_dft** command after the **set_test_point_element** command. The **set_test_point_element** command allows design objects to specify pin instances on which test points must be inserted.

WHAT NEXT

Use the **set_dont_touch** command to prevent the cell from being modified or replaced during optimization; or, use **insert_dft** with optimization switched off. Use the **-dont_fix_constraints** and **-ignore_compile_design_rules** options with the **insert_dft** command to switch off optimization.

SEE ALSO

insert_dft (2), **set_dont_touch** (2), **set_test_point_element** (2).

UIT-704 (warning) Cell '%s' has a dont_touch attribute.

The violation(s) associated with it will not be autofixed.

DESCRIPTION

This message informs you that the **dont_touch** attribute exists on the specified cell and prevents violations associated with this cell from being autofixed. You receive this warning message when you use the **preview_dft** command. The full list of instances with the **dont_touch** attribute is reported using the **preview_dft -verbose** command. Without the **-verbose** switch, the **preview_dft** command reports the first violation and the total number occurrences of the **dont_touch** attribute.

WHAT NEXT

If you are satisfied with this result, no action is required on your part. If you want the violation(s) associated with the specified cell to be autofixed, remove the **dont_touch** attribute from the specified cell and rerun AutoFix.

SEE ALSO

preview_dft (2).

UIT-705 (information) There are %d other cells with the same violation.

DESCRIPTION

This message summarizes the total number of violations identified in UIT-704. Specifically, this message reports the first violation and the total number of occurrences of the **dont_touch** attribute in the design.

WHAT NEXT

This is an informational message. No action is required on your part. For more information, see the manual page for UIT-704.

SEE ALSO

preview_dft (2); **UIT-704** (n).

UIT-706 (information) The port %s is used as a test mode signal to AutoFix asynchronous sets and resets and as a test scan

enable signal.

DESCRIPTION

This message informs you that the port %s is shared between the test mode signal and the test scan enable signal to Autofix asynchronous sets and resets. You have used the **set_autofix_configuration** command with the **-fix_async_with_se true** option to use the test scan enable signal to Autofix asynchronous sets and resets.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

set_autofix_configuration (2).

UIT-707 (error) Incorrect value for -fix_async_with_scan_en option argument. Allowed values are true, TRUE, on, and ON; or false, FALSE, off, and OFF.

DESCRIPTION

This error message informs you that you used the **set_autofix_configuration** command with an invalid argument for the **-fix_async_with_scan_en** option. Allowed values for the **-fix_async_with_scan_en** option argument are true, TRUE, on, and ON; or false, FALSE, off, and OFF.

WHAT NEXT

Use the **set_autofix_configuration** command with the **-fix_async_with_scan_en** option and specify one of the allowed values as the argument.

SEE ALSO

set_autofix_configuration (2).

UIT-708 (Warning) Overwriting the async port specification '%s'

to autofix the cell/instance ’%s’.

DESCRIPTION

You can use the **set_autofix_async** command to put a specific async port to autofix a cell/instance. This warning message is produced if you try to perform **set_autofix_async** on a cell/instance that already has a specified async port.

WHAT NEXT

No further action is necessary.

UIT-709 (information) One asynchronous pin of the cell %s has already been autofixed. As a consequence, another handler %s will be used to autofix the second asynchronous pin %s.

DESCRIPTION

You receive this information message because one of the asynchronous signals of the cell has been autofixed. The same handler cannot be used to autofix the asynchronous pins of the same register. Therefore, two different handlers will be used to autofix the two asynchronous pins of the same register.

WHAT NEXT

Use the set_autofix_async command to specify existing ports to be used to fix asynchronous signals of cells.

SEE ALSO

insert_dft (2), **set_autofix_async(2), set_dft_signal** (2).

UIT-710 (error) Invalid cell type for core wrapper insertion.

DESCRIPTION

You receive this message if you issue the **set_core_wrapper_design** command and specify an invalid value for the wrapper cell type. Valid values of wrapper cell types are listed in the manual page and the online help for the **set_core_wrapper_design** command. The **insert_dft** command uses the specified wrapper cell type when synthesizing wrapper into the design.

WHAT NEXT

Refer to the manual page or the online help for the **set_core_wrapper_design** command to determine the current valid wrapper cell types, and reissue the **set_core_wrapper_design** command with a valid wrapper cell type.

SEE ALSO

insert_dft (2), **set_core_wrapper_design** (2).

UIT-711 (error) Cannot find the specified design in memory.

DESCRIPTION

You receive this message if you execute the **set_core_wrapper_design** command and the name you specify for the *design_name* argument cannot be found in memory. This could be caused by a typo or spelling error. The **insert_dft** command uses the specified design as a wrapper cell design when synthesizing wrapper into the design.

WHAT NEXT

Verify that the design you want to use does exist in memory, and verify its spelling. Then re-execute the appropriate command using the correct design name.

SEE ALSO

insert_dft (2), **set_core_wrapper_design** (2).

UIT-712 (error) Invalid port type '%s' specified for user-defined wrapper cell design.

DESCRIPTION

You receive this message if you issue the **set_core_wrapper_design** command and specify an invalid port type. Valid port types are found in the manual page or online help for the above command. The **insert_dft** command uses the user-defined wrapper cell design when synthesizing wrapper into the design.

WHAT NEXT

Refer to the manual pages or the online help for the **set_core_wrapper_design**, command to determine the current valid wrapper cell design port types, respectively. Then reissue the appropriate command with a valid port type.

SEE ALSO

insert_dft (2), **set_core_wrapper_design** (2).

UIT-713 (Error) Missing ports for user-defined wrapper cell design : %s.

DESCRIPTION

This error is generated because some of the required access ports for the wrapper cell design are missing from the specification. The **set_core_wrapper_design** command lets you specify user-defined wrapper cell design.

WHAT NEXT

Rerun one of the commands and specify all required access ports using the **-access** option. For a list of required access ports, see the man page for the **set_core_wrapper_design** command.

SEE ALSO

set_core_wrapper_design (2).

UIT-714 (error) Cannot find the specified port '%s' in the design.

DESCRIPTION

You receive this message if you execute the **set_core_wrapper_design** command and a port you specify cannot be found in the design. This could be caused by a typo or spelling error. The **insert_dft** command uses the specified wrapper cell type when synthesizing wrapper into the design.

WHAT NEXT

Verify the name of the port. Then reissue the appropriate command using the correct port name for the design or instance.

SEE ALSO

insert_dft (2), **set_core_wrapper_design** (2).

UIT-715 (error) Scan chain '%s' exists in another mode.

DESCRIPTION

DFT Compiler does not allow same scan chains to be specified using multiple **set_scan_path** commands. This warning tells you that an earlier specification for the same scan chain exists for another mode. Scan chain names should be unique for the whole design.

WHAT NEXT

Establish whether you want the specification to be overwritten. If not, combine the two specifications into one **set_scan_path** command for the same mode.

UIT-717 (error) The option **test_use_test_models** is not supported by **write_layout_scan**.

DESCRIPTION

You receive this message if you set the env variable **test_use_test_models** to TRUE before the command write_layout_scan. This flow is not supported for write_layout_scan.

WHAT NEXT

Reset the env variable **test_use_tes_models** before the command **write_layout_scan**

SEE ALSO

test_use_test_models (3). **write_layout_scan** (2).

UIT-718 (error) The -power_saving_on option is only available when the -method option has the tdvr argument.

DESCRIPTION

You receive this message if you execute **set_testability_configuration** with the **-power_saving_on** option and without tdvr as an argument for the **-method** option.

WHAT NEXT

Re-issue the command with tdvr for the **-method** option argument or re-issue the command without the fB-power_saving_on option.

SEE ALSO

set_testability_configuration (2).

UIT-719 (Error) The type %s is not a valid type for the set_test_point_element command.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but the type is not a valid type for the command.

WHAT NEXT

Check the valid types in the manpage of the set_test_point_element, modify the type and re-issue the command.

SEE ALSO

set_test_point_element

UIT-720 (Error) The parameter for the %s option has to be enable or disable.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but the parameter for the option is not a valid one. The valid parameters are enable or disable.

WHAT NEXT

Change the parameter for the option and re-issue the command.

SEE ALSO

set_test_point_element

UIT-721 (Error) Port %s is not a test mode.

DESCRIPTION

The port %s is not a test mode. Use **set_dft_signal** to create a test mode associated with port %s.

WHAT NEXT

After the dft signal specification, re-issue the command.

UIT-722 (Warning) The -scan_test_point_enable option is ignored for the type %s.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but the -scan_test_point_enable option is not an option that can be specified for the type and the option is ignored. The -scan_test_point_enable option is a valid option for the control types.

WHAT NEXT

Remove the -scan_test_point_enable option.

SEE ALSO

set_test_point_element

UIT-723 (Warning) The -test_points_per_test_point_enable option is ignored for the type %s.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but the -test_points_per_test_point_enable option is not an option that can be specified for the type and the option is ignored. The -test_points_per_test_point_enable option is a valid option for the control types.

WHAT NEXT

Remove the -test_points_per_test_point_enable option.

SEE ALSO

set_test_point_element

UIT-724 (Warning) The -test_point_enable option is ignored for the type %s.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but the -test_point_enable option is not an option that can be specified for the type and the option is ignored. The -test_point_enable option is a valid option for the control types.

WHAT NEXT

Remove the -test_point_enable option.

SEE ALSO

set_test_point_element

UIT-725 (Error) The port or the pin %s does not have the correct direction.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but the port or the pin does not have the correct direction according to the option in which the port or the pin has been specified.

WHAT NEXT

Specify another port or another pin with the correct direction and re-issue the command.

SEE ALSO

set_test_point_element

UIT-726 (Error) The pin %s does not have the correct direction for a test point location.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but a pin from the list does not have the correct direction. A test point location has to be an output pin.

WHAT NEXT

Specify another pin with the correct direction for the test point location and re-issue the command.

SEE ALSO

set_test_point_element

UIT-727 (Error) The port %s cannot be specified for a test point location.

DESCRIPTION

This message indicates that a set_test_point_element command has been issued, but a port cannot be the location of a test point. A test point location has to be an output internal pin.

WHAT NEXT

Specify an internal output pin and re-issue the command.

SEE ALSO

set_test_point_element

UIT-728 (warning) Cell ’%s’ has no function specification.

The asynchronous pin violation(s) associated with it will not be autofixed.

DESCRIPTION

This message informs you that the specified cell has no function specification and this prevents the asynchronous pin violations associated with this cell from being autofixed. You receive this warning message when you use the **preview_dft** and **insert_dft** commands.

WHAT NEXT

If you are satisfied with this result, no action is required on your part. If you want the violation(s) associated with the specified cell to be autofixed, provide the library for the cell; the test_simulation_library does not provide enough information to autofix the asynchronous pins of the specified cell.

SEE ALSO

preview_dft (2), **insert_dft** (2).

UIT-730 (Error) Unsupported client '%s' for RTL Insertion.

DESCRIPTION

This message informs you that RTL insertion is incompatible with any other DFT clients.

WHAT NEXT

Remove DFT clients from set_dft_configuaration and insert_dft UI commands.

SEE ALSO

set_dft_configuaration (2), **insert_dft** (2).

UIT-731 (Error) Unrecognized HDL format '%s'.

DESCRIPTION

This message informs you that the specified HDL format for RTL insertion is not valid. Only 'verilog' and 'VHDL' are valid values.

WHAT NEXT

Change the HDL format to 'verilog' or 'VHDL'.

SEE ALSO

set_dft_rtl_configuration (2),

UIT-732 (error) '%s' is not a directory.

DESCRIPTION

You have specified an invalid directory; or, the directory or one or more of its parents are read or search protected.

WHAT NEXT

Check your project file to ensure that variables specifying directories are correctly set.

Change your permissions to enable reading and searching of the appropriate directory and all of its parents. For example,

```
chmod a+rx <dir_name>
```

UIT-733 (error) Cannot perform RTL insertion because the variable hdlin_enable_rtldrc_info is set to FALSE

DESCRIPTION

The variable hdlin_enable_rtldrc_info must be set to TRUE to perform RTL insertion. FALSE is the hdlin_enable_rtldrc_info variable default value.

WHAT NEXT

Set the variable hdlin_enable_rtldrc_info to TRUE For example,

```
set hdlin_enable_rtldrc_info TRUE
```

UIT-770 (Warning) The option -identify_shift_register will be

ignored in 2007.03 SP4. Shift register identification will be moved fully to DC Ultra in Z2007.03 SP4.

DESCRIPTION

This options is ignored in 2007.03 release. Added back in 2007.03 SP1. This option will again be ignored from 2007.03 SP4. The functionality is incorporated into **compile_ultra -scan**. The variable compile_seqmap_identify_shift_registers can be used to enable/disable the identification in compile_ultra -scan

WHAT NEXT

Execute **compile_ultra -scan**

UIT-800 (warning) Bad value for the number of test points per observe flop option. Eight test points per observe flop will be considered during test point insertion.

DESCRIPTION

In order to provide balanced xor tree, the only accepted values for **-test_points_per_observe_flop** option are 1, 2, 4 and 8. If a different value is set, then the default value (8) will be considered.

WHAT NEXT

Set number of test points per observe clock with a correct value.

UIT-801 (warning) No observe test point will be inserted.

DESCRIPTION

This warning message appears when **-max_observe_points** and/or **-max_observe_logic_area** are set to zero. In this case, no observe test point will be inserted in the design.

WHAT NEXT

Set **-observe_points_per_scan_cell** and/or **-max_observe_logic_area** options with the correct value.

UIT-802 (Error) Unable to read the TRC file %s given.

DESCRIPTION

This is issued from the command **read_trc_file** . The command is not able to read the file specified due to errors given before.

WHAT NEXT

Check the file syntax as well is as per the standard supported.

UIT-803 (information) reverting value of environment variable '%s' to its default value '%s'.

DESCRIPTION

DFT Compiler validates the values of environment variables it uses. You see this message when an environment variable value is invalid. DFT Compiler supplies a default.

WHAT NEXT

Confirm that the environment variable is invalid. Modify the environment variable value to remove the warning.

UIT-804 (Warning) '%s' is not a valid scan style.

DESCRIPTION

DFT Compiler validates the values of environment variables it uses. You see this message when an environment variable that needs to specify a scan style specifies an invalid one. DFT Compiler will use a default scan style.

WHAT NEXT

Confirm that the environment variable is invalid. Modify the environment variable value to remove the warning.

UIT-805 (Warning) ’%s’ is not ’true’ or ’false’.

DESCRIPTION

DFT Compiler validates the values of environment variables it uses. You see this message when an environment variable that needs to specify either ’true’ or ’false’ specifies something else. DFT Compiler will use a default value.

WHAT NEXT

Confirm that the environment variable is invalid. Modify the environment variable value to remove the warning.

UIT-806 (warning) Cannot associate a ’%s’ signal with chain ’%s’.

DESCRIPTION

DFT Compiler uses one scan enable signal to enable scan mode. This message warns that you used the **set_scan_signal** command to associate a scan enable with a specific scan chain. Because the scan enable is associated with all scan chains, the specific association is ignored.

WHAT NEXT

Remove the association to suppress the warning.

UIT-807 (information) reverting value of environment variable ’%d’ to its default value ’%d’.

DESCRIPTION

DFT Compiler validates the values of environment variables it uses. You see this message when an environment variable value is invalid. DFT Compiler supplies a default.

WHAT NEXT

Confirm that the environment variable is invalid. Modify the environment variable value to remove the warning.

UIT-808 (Warning) ’%s’ does not include the substring ’%%s’.

DESCRIPTION

DFT Compiler validates the values of environment variables it uses. You see this message when an environment variable that needs include the substring "%s" does not. DFT Compiler will use a default value.

WHAT NEXT

Confirm that the environment variable is invalid. Modify the environment variable value to remove the warning.

UIT-809 (warning) Hookup sense value ’%s’ conflicts with the old value ’%s’.

DESCRIPTION

DFT Compiler only associates exactly one hookup sense between a design port and an internal hookup pin. This message warns that you have used the **set_scan_signal** command to associate a second hookup sense, and that the second specification has overwritten the first.

WHAT NEXT

Check that you do want to overwrite the specification. Repeat the correct specification if the overwrite was mistaken.

UIT-810 (error) Argument -memory_cells should be specified for a single controller.

DESCRIPTION

This error occurs because you used the **set_mbist_controller** command to assign a list of memory cells to two or more controllers.

WHAT NEXT

Run the **set_mbist_controller** command spcifying one controller with -controller_names and a list of memory cells using -memory_cells.

SEE ALSO

set_mbist_element (2).

UIT-811 (error) Memory '%s' has already been assigned to a controller. Cannot change notouch value to TRUE.

DESCRIPTION

This error occurs because you either used the **set_mbist_controller** command to assign a memory cell, which has already been assigned to a controller, to a new controller or you used **set_mbist_element** command to set notouch value to TRUE for that memory cell.

WHAT NEXT

Run the **remove_mbist_configuration** command to remove the current MBIST configuration. Assign the memory cell to the new controller using **set_mbist_controller** command spcifying one controller with -controller_names and the memory cell using -memory_cells.

SEE ALSO

remove_mbist_configuration (2).

UIT-812 (error) -notouch and -ip_parameters are mutually exclusive.

DESCRIPTION

This error occurs because you used the **set_mbist_element** command to simultaneously set the -notouch value and assign the -ip_parameters for the memory cells.

WHAT NEXT

Run the **set_mbist_element** command with either -notouch or the -ip_parameter switch.

SEE ALSO

remove_mbist_configuration (2).

UIT-813 (error) Odd number of items in the -ip_parameters list.

DESCRIPTION

This error occurs because you used the **set_mbist_element** or **set_mbist_controller** command to pass odd number of items in the -ip_parameters list.

WHAT NEXT

Run the **set_mbist_element** or **set_mbist_controller** command with even number of items in the -ip_parameter list.

SEE ALSO

remove_mbist_configuration (2).

UIT-814 (error) -notouch value can be either TRUE or FALSE.

DESCRIPTION

This error occurs because you used the **set_mbist_element** command to set -notouch to a value other than TRUE or FALSE.

WHAT NEXT

Run the **set_mbist_element** command with -notouch value as TRUE or FALSE

SEE ALSO

remove_mbist_configuration (2).

UIT-815 (error) Memory '%s' has notouch value set to TRUE and cannot be assigned ip parameters or to a controller .

DESCRIPTION

This error occurs because you either used the **set_mbist_controller** command to assign a memory cell, which has already been excluded from MBIST consideration, to controller or tried to assign ip parameters using /fBset_mbist_element/fP.

WHAT NEXT

Run the **remove_mbist_configuration** command to remove the current MBIST configuration. Assign the memory cell to the new controller using **set_mbist_controller** command spcifying one controller with -controller_names and the memory cell using -memory_cells.

SEE ALSO

remove_mbist_configuration (2).

UIT-816 (error) Invalid value for the -mbist parameter

DESCRIPTION

This error occurs because you specified an invalid value for the -mbist parameter.

WHAT NEXT

See the list of available values

SEE ALSO

preview_dft (2).

UIT-817 (error) "%s" is not a valid command line option for set_mbist_run command.

DESCRIPTION

You receive this message because the parameter(s) name or value specified in the set_mbist_run command are not valid.

WHAT NEXT

Please enter valid parameter name and values in the command line.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

UIT-818 (error) Parameter "fail_limit" can be defined only for debug mode.

DESCRIPTION

You receive this message because the parameter "fail_limit" was specified for a test_mode other than debug mode.

WHAT NEXT

Please change the test_mode to debug mode or remove the "fail_limit" parameter from the command line.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

UIT-819 (error) Memory instance %s does not exist in the top level model.

DESCRIPTION

You receive this message because either the memory instance is missing from the top model or the corresponding reference object is missing.

WHAT NEXT

Please add the memory instance to the netlist. If the instance does not exist in the design, remove the instance name from the list of memories in the command line. If the memory instance is in the design, read the library cell or the design object corresponding to the reported memory instance in the dc_shell.

SEE ALSO

insert_dft (2), **preview_dft** (2), **read_test_model** (2), **set_dft_configuration** (2).

UIT-820 (error) Odd number of items in the -parameters list.

DESCRIPTION

This error occurs because you used the **set_mbist_wrapper**, **set_mbist_controller** or

set_mbist_configuration command to pass an odd number of items in the **-parameters** list.

WHAT NEXT

Run the respective command with an even number of items in the -parameter list.

SEE ALSO

set_mbist_configuration (2) **set_mbist_wrapper** (2) **(XG** mode) **set_mbist_controller** (2) **reset_mbist_configuration** (2) **(XG** mode) **remove_mbist_configuration** (2)

UIT-821 (error) Controller '%s' has no memories assigned to it, and can not have -complete TRUE.

DESCRIPTION

This error occurs because you used the **set_mbist_controller** command to set a controller as complete (no more memories can be assigned), but you never assigned any memories. This means you tried to specify a controller that controls nothing.

WHAT NEXT

Try the same **set_mbist_controller** command again, while including some -memory_cells.

SEE ALSO

set_mbist_controller (2).

UIT-822 (error) 'memory_cells' (alias 'target' in XG mode) parameter is required when view is set to SPEC

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode) because the 'memory_cells' (alias 'target' in XG mode) parameter is missing. This is required when view is set to SPEC.

WHAT NEXT

Look at **set_mbist_element** (or **set_mbist_wrapper** in XG mode) man page

SEE ALSO

preview_dft (2). **set_mbist_element** (2). **set_mbist_wrapper** (2).

UIT-823 (warning) '-mem_id' is ignored when 'view' option is set to EXISTING

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode) because the 'mem_id' option is specified in the case of 'view' option set to SPEC. The 'mem_id' option is required only when 'view' is set to EXISTING.

WHAT NEXT

Look at **set_mbist_element** (or **set_mbist_wrapper** in XG mode) man page

SEE ALSO

preview_dft (2). **set_mbist_element** (2). **set_mbist_wrapper** (2).

UIT-824 (warning) '-no_touch', '-memory_cells' (alias '-target' in XG mode) and '-ip_parameters' (alias '-parameters' in XG mode) options are ignored when 'view' option is set to EXISTING

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode) because the '-no_touch', '-memory_cells' (alias '-target' in XG mode) and '-ip_parameters' (alias '-parameters' in XG mode) options are used when 'view' option is set to SPEC and are ignored when 'view' option is set to EXISTING.

WHAT NEXT

Look at **set_mbist_element** (or **set_mbist_wrapper** in XG mode) man page

SEE ALSO

preview_dft (2). **set_mbist_element** (2). **set_mbist_wrapper** (2).

UIT-825 (error) the test model has not been generated by MBISTC Tech 2

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode) because the test model of the current design has not been generated by MBISTC Tech 2 and so it can not be modified.

WHAT NEXT

Read the correct test model and set the correct current design

SEE ALSO

preview_dft (2). **set_mbist_element** (2). **set_mbist_wrapper** (2).

UIT-826 (error) 'content_file' option supports only one file name in the case of 'view' option set to EXISTING

DESCRIPTION

This is issued from the command **set_mbist_element** (or **set_mbist_wrapper** in XG mode) because the 'content_file' option value is a list of file names. The 'content_file' value can be a file name list in the case of 'view' option set to SPEC; only one file name is supported for 'content_file' option in the case of 'view' option set to EXISTING.

WHAT NEXT

Look at the **set_mbist_element** (or **set_mbist_wrapper** in XG mode) man page

SEE ALSO

preview_dft (2). **set_mbist_element** (2). **set_mbist_wrapper** (2).

UIT-827 (error) At least one of the trace_file parameters must be

specified

DESCRIPTION

This is issued from the command **report_mbist_trace** as no trace file was specified. You must specify at least one of the following parameters: **-trace_file**, **-repair_trace_file**

WHAT NEXT

Specify a trace file parameter

SEE ALSO

report_mbist_trace (2).

UIT-900 (warning) '%s' is not a cell, instance, scan segment, or scan link, and is not being added to the scan group.

DESCRIPTION

The set_scan_group command accepts an unordered list of design objects. These must be cells, instances, links or segments. Other kinds of design objects cannot be added to scan groups, and are rejected.

WHAT NEXT

Remove the object from the argument list to get rid of the warning. Use hierarchical instance names, with respect to the top-level design, to locate design objects.

UIT-901 (warning) Scan group element '%s' is a scan link and is not being added to the scan group.

DESCRIPTION

The **set_scan_group** command accepts an unordered list of design objects. The first object in the list can not be a scan link because there is no preceding cell to associate it with.

WHAT NEXT

Remove the object from the argument list to get rid of the warning.

UIT-902 (Error) Ignoring the scan group specification as the scan group '%s' is empty.

DESCRIPTION

Specify scan groups using the **set_scan_group** command.

This message tells you that DFT Compiler ignores a **set_scan_group** command because the scan group is empty .

WHAT NEXT

Specify valid scan group elements to get rid of the error. If you did specify group elements, study accompanying warning messages to see why they were discarded.

UIT-903 (error) Scan %s '%s' element '%s' has internal and wrapper segments.

DESCRIPTION

This error message is generated when you try to include a core cell into a scan group or scan segment. A core cell is a cell with a test model and has both internal scan and wrapper segments. As internal scan segments and wrapper segments can't be mixed during core integration, you can't include such a cell with other elements of a scan group or a scan segment.

WHAT NEXT

Check if you have specified core_integration flag of dft configuration. If you are not integrating cores, remove such a specification and reinvoke the current command.

SEE ALSO

set_scan_group (2). **set_scan_segment** (2). **set_dft_configuration** (2). **remove_dft_configuration** (2).

UIT-904 (error) Scan Group '%s' has %s segments.

DESCRIPTION

This error message is generated when you try to include a wrapper or an internal scan segment with other segments in a scan group during core integration. Wrapper or internal scan segments can not be mixed with other segments during core integration.

WHAT NEXT

Check if you have specified core_integration flag of dft configuration. If you are not integrating cores, remove such a specification and reinvoke the current command.

SEE ALSO

set_scan_group (2). **set_dft_configuration** (2). **remove_dft_configuration** (2).

UIT-905 (warning) Scan group '%s' overwrites an earlier specification.

DESCRIPTION

DFT Compiler does not allow scan groups to be specified using multiple **set_scan_group** commands. This warning tells you that an earlier specification of scan group is being overwritten.

WHAT NEXT

Establish whether you want the specification to be overwritten. If not, combine the two specifications into one **set_scan_group** command.

UIT-906 (error) Scan group '%s' exists in another mode.

DESCRIPTION

DFT Compiler does not allow same scan group to be specified using multiple **set_scan_group** commands. This warning tells you that an earlier specification for the same scan group exists for another mode. Scan group names should be unique for the whole design.

WHAT NEXT

Establish whether you want the specification to be overwritten. If not, combine the two specifications into one **set_scan_group** command for the same mode.

UIT-907 (error) Scan groups '%s' and '%s' have common elements.

DESCRIPTION

DFT Compiler does not let scan groups share scan elements (cells or design instances). This error tells you that some elements belong to more than one group.

WHAT NEXT

If the common elements can be removed from the scan group you're specifying, remove them and reapply the **set_scan_group** command. Otherwise, apply the **remove_scan_group** command and start again specifying without common elements between groups.

UIT-908 (error) Signal of data type '%s' is not valid for internal pins flow.

DESCRIPTION

The signal data types that are valid for internal pins flow are MasterClock, ScanMasterClock, Reset, Constant, ScanDataIn, ScanDataOut, ScanEnable, and TestMode.

WHAT NEXT

Please specify a valid data type using the **set_dft_signal** command and turn on the internal pins flow using the **set_dft_drc_configuration**.

UIT-909 (error) Internal pin '%s' of type '%s' direction is not valid for internal pins flow.

DESCRIPTION

If the internal pin specified is not a hierarchical pin and is of data type MasterClock, ScanMasterClock, Reset, Constant, ScanDataIn, ScanEnable, and TestMode, the pin should be of direction Out and if the data type is ScanDataOut, the pin

should be of direction In. For the hierarchical pins, pins with both In and Out directions are valid.

WHAT NEXT

Please specify a pin with valid direction using the **set_dft_signal** command and turn on the internal pins flow using the **set_dft_drc_configuration**.

UIT-910 (error) The hookup pin '%s' of type '%s' direction is not a valid hookup pin.

DESCRIPTION

The valid hookup pins specified for set_dft_signal are either driven by a proper combinational/sequential logic or they are outputs of a black box. The hookup pins specified by the user that have no driver or pins that are connected to a logic zero or one internally are not valid.

WHAT NEXT

Please change the netlist to either add driver for the hookup pin or specify another pin with valid driver using the **set_dft_signal** command.

UIT-911 (error) Numbers of pipeline head and tail registers do not match the respective numbers in previously specified scan paths

DESCRIPTION

You have specified several scan paths with their corresponding head and tail registers. But the number of head pipeline registers specified for the current chain is different from the one specified in previous chains or the number of tail pipeline stages specified for the current chain is different from the one specified in previous chains. The number of head pipeline registers should be the same across all chains. The number of tail pipeline registers should be the same across all chains.

WHAT NEXT

Correct the list of register name for **set_scan_path -pipeline_head** or **-pipeline_tail** command

UIT-912 (error) The pin '%s' is not a valid hookup pin.

DESCRIPTION

The valid hookup pins specified for set_scan_path are either driven by a proper combinational/sequential logic or they are outputs of a black box. For a hierarchical box that has some pins with proper drivers, or pins that are connected to a logic zero or one internally, the hookup pins specified by the user that have no driver are not valid. The hookup pin must be associated with a pin using set_dft_signal, prior to be used in set_scan_path for scan path specification.

WHAT NEXT

Please change the netlist to either add driver for the hookup pin or specify another pin with valid driver using the **set_dft_signal** and **set_scan_path** commands.

UIT-913 (warning) Same hookup pin specified more than once. Duplicate hookup pins will be removed.

DESCRIPTION

The hookup pins specified for set_scan_path are expected to be unique. Multiple use of a hookup pin gives this warning. The duplicate hookup pin specification is ignored.

WHAT NEXT

Use unique hookup pins with **-hookup** option of **set_scan_path** command. Use **report_scan_path** command to observe the scan path set.

UIT-914 (warning) Specification of a signal of type Oscillator in spec view is ignored.

DESCRIPTION

You receive this message because you have specified a signal of type Oscillator with -view spec or without the -view option. In this case, the command will be ignored because a signal of type Oscillator must be specified in view existing_dft.

WHAT NEXT

Please specify the signal in existing view using the **set_dft_signal** command.

UIT-915 (error) Hookup pin is not allowed for the '%s' boundary scan port.

DESCRIPTION

This error message occurs when a hookup pin is specified while using the **set_dft_signal** command with the **-type TAP** ports option. A hookup pin cannot be specified for the TCK, TDI, TDO, TMS and TRST boundary scan TAP ports.

WHAT NEXT

Remove the **-hookup_pin** option for BSD TAP ports. See the **set_dft_signal** man page for more information.

SEE ALSO

set_dft_signal(2)

UIT-916 (error) Only one port is allowed for the '%s' boundary scan signal type.

DESCRIPTION

This error message occurs when multiple ports for a BSD signal type are specified with the **-port** option of the **set_dft_signal** command. Only one port should be used as a boundary scan TAP port.

WHAT NEXT

Use only one port with the **-port** option of the **set_dft_signal** command for boundary scan TAP ports.

SEE ALSO

set_dft_signal(2)

UIT-917 (warning) BSD Test Data Register hookup pins are going to be obsoleted in existing_dft view for synthesis, specify

them in spec view.

DESCRIPTION

Considering that BSD Test Data Registers can be useful only at spec view, it is decided to remove the -existing_dft option of **set_scan_path** and **set_dft_signal** commands for BSD Test Data Registers.

WHAT NEXT

Use -hookup_pins option with option -view spec for Test Data Registers in BSD, while using **set_dft_signal** or **set_scan_path** commands.

UIT-918 (warning) BSD Test Data Register hookup pin of type reset is obsoleted, specify the pin type as bsd_reset, changing the pin type to bsd_reset.

DESCRIPTION

The hookup pin type **reset** is obsoleted in BSDC, instead it is suggested to use the new option **bsd_reset** for the same functionality. You get this message if -type reset is used while specifying hookup pin for Test Data Register using **set_dft_signal** command.

WHAT NEXT

You can ignore this warning as hookup pin type **reset** is read as **bsd_reset** by BSDC. Instead hookup pin type **bsd_reset** can be used to not get this warning.

UIT-919 (warning) Incorrect active state '%d' specified for TRST port, resetting the active state of the port to 0.

DESCRIPTION

This warning message occurs when the **set_dft_signal -active_state** option is not set to 0 (zero) for the TRST port type. If the TRST port **-active_state** is not set to 0, BSDC forces the active state to 0.

WHAT NEXT

This is only a warning message. No action is required.

You can ignore this warning as BSDC sets the active state to 0 internally. To avoid this message, use 0 with the **-active_state** option for a TRST port while using **set_dft_signal** command.

SEE ALSO

set_dft_signal

UIT-920 (error) The option -include_elements of set_scan_path command does not accept a collection as an input.

DESCRIPTION

You have specified a collection as an input parameter for the -include_elements option of the set_scan_path command. This option accepts only a list of elements.

WHAT NEXT

Use a list of elements as an input parameter

UIT-921 (warning) Incorrect active state '%d' specified for TAP port, resetting the active state of the port to 1.

DESCRIPTION

This warning message occurs when the **set_dft_signal -active_state** option is not set to 1 (one) for the TAP port type (TCK/ TMS/ TDI / TDO). If the TAP port **-active_state** is not set to 1, BSDC forces the active state to 1.

WHAT NEXT

This is only a warning message. No action is required.

You can ignore this warning as BSDC sets the active state to 1 internally. To avoid this message, use 1 with the **-active_state** option for a TAP port while using **set_dft_signal** command.

SEE ALSO

set_dft_signal

UIT-930 (error) Signal of data type '%s' is not valid for -connect_to option.

DESCRIPTION

The signal data types that are valid with **-connect_to** option are MasterClock, ScanMasterClock, ScanClock and Oscillator.

WHAT NEXT

Please specify a valid data type using the **set_dft_signal** command.

UIT-931 (error) Pin '%s' direction is not valid for -connect_to option.

DESCRIPTION

You receive this message because you specified a wrong pin direction for **-connect_to** option. In this case, the pin should be of direction In.

WHAT NEXT

Please specify a pin with a valid direction using the **set_dft_signal** command.

UIT-935 (error) Invalid clock controller specification due to inconsistent pll clock sources.

DESCRIPTION

This error message occurs when a single clock controller is specififed for pllclocks sources that come from different hierarchical blocks.

WHAT NEXT

Specify a clock controller for each group of pllclocks that belong to the same hierarchy using the **set_dft_clock_controller** command.

SEE ALSO

set_dft_clock_controller(2)

UIT-999 (Error) The scan state is invalid for running this command. The scan state should be scan existing.

DESCRIPTION

You receive this error message because the scan state should be either **scan_existing** (scan routed) for the **disconnect_scan_chains** command to run. If the current state of the design is not scan existing, this error message prevents disconnect_scan_chains command from proceeding.

WHAT NEXT

Set the scan state using the **set_scan_state** command before using the **disconnect_scan_chains** command.

SEE ALSO

set_dft_optimization_configuration (2), **disconnect_scan_chains** (2), **insert_dft** (2),

UIT-1000 (error) Invalid argument for -use_register_io: '%s'. Argument must be either true or false.

DESCRIPTION

You receive this message if you execute either **set_core_wrapper_configuration** or **set_core_wrapper_cell** command and use an invalid argument for the **-use_register_io** option. Valid arguments are true or false.

WHAT NEXT

Reexecute the command and use a valid argument for the **-use_register_io** option.

SEE ALSO

set_core_wrapper_configuration (2). **set_core_wrapper_cell** (2).

UIT-1001 (error) Invalid argument for -longest_chain_length:

’%s’. Argument must be a postive integer or the string "default".

DESCRIPTION

You receive this message if you execute the **set_core_wrapper_configuration** command and use an invalid argument for the **-longest_chain_length** option. Valid arguments are positive integers or the string "default".

WHAT NEXT

Reexecute the **set_core_wrapper_configuration** command and use a valid argument for the **-longest_chain_length** option.

SEE ALSO

set_core_wrapper_configuration (2).

UIT-1002 (error) Can not insert ’%s’ scan chains.

DESCRIPTION

The set_core_wrapper_configuration command accepts a chain_count option. This tells DFT Compiler the number of scan chains to implement in the testable design. Option arguments must be positive integers or "default" strings.

WHAT NEXT

Repeat the set_core_wrapper_configuration command using a positive integer or the string "default".

SEE ALSO

set_core_wrapper_configuration (2).

UIT-1003 (error) Cannot find the specified port ’%s’ in the current design.

DESCRIPTION

You receive this message if you execute the **set_core_wrapper_path** command and a port you specify cannot be found in the current design. This could be caused by a typo or spelling error or an invalid name being used as a port name.

WHAT NEXT

Verify the name of the port. Then reissue the command **set_core_wrapper_path** using the correct port name of the current design.

SEE ALSO

set_core_wrapper_path (2)

UIT-1004 (error) Wrapper Cell type must be either "in" , "out" or "en".

DESCRIPTION

You receive this message if you execute **set_core_wrapper_path** and specify an invalid wrapper cell type. Valid cell types are "in", "out" or "en". For **set_core_wrapper_path**, you can specify the type of a wrapper cell by attaching /in , /out or /en to the port name in the *identifier_list*. The cell types /in, /out, /en can be used to identify wrapper cells attached to a bidirectional port. The cell types /out, /en can be used to identify wrapper cells attached to a tr-state port. No cell type can be used to identify wrapper cells attached to input ports.

WHAT NEXT

Choose a valid cell type for the Wrapper cell, and reissue the command **set_core_wrapper_path** using the valid wrapper cell type.

SEE ALSO

set_core_wrapper_path (2).

UIT-1005 (warning) Ignoring the -complete true option because wrapper chain '%s' is empty.

DESCRIPTION

The **set_core_wrapper_path** command accepts a list of ports and **-complete** option. This tells DFT Compiler the order of wrapper cells in a wrapper chain to implement in the testable design. This error occurred as user didn't specify any valid ports and **-complete** option is set to TRUE for the command.

WHAT NEXT

Repeat the **set_core_wrapper_path** command using either a set of valid ports or setting the **-complete** option to false.

SEE ALSO

set_core_wrapper_path (2).

UIT-1006 (information) You have invoked remove_core_wrapper_specification with no options. The command is ignored.

DESCRIPTION

The **remove_core_wrapper_specification** command does nothing when it is invoked without options.

This, in itself, is not a problem. No core wrapper specifications are removed. You might, however, have meant to use the "-all" option or one of the other more limited options.

WHAT NEXT

To get rid of the information message, invoke **remove_core_wrapper_specification** with options.

SEE ALSO

remove_core_wrapper_specification(2) set_core_wrapper_path(2) set_core_wrapper_design(2)

UIT-1007 (error) Pipelining is only supported with the "no_mix" scan clock domain constraints.

DESCRIPTION

You get this message when you have selected something else than **no_mix** after the option **-clock_mixing** and you have enabled scan enable pipelining. Pipelining scan enable supports only the no_mix scan clock domain constraints.

WHAT NEXT

Modify the scan clock domain constraint to **no_mix**, using the set_scan_configuration command

SEE ALSO

set_scan_configuration(2)

UIT-1008 (error) Invalid argument for -register_io_implementation: '%s'. Argument must be either swap or in_place.

DESCRIPTION

You receive this message if you execute either **set_core_wrapper_configuration** or **set_core_wrapper_cell** command and use an invalid argument for the **-register_io_implementation** option. Valid arguments are swap or in_place.

WHAT NEXT

Reexecute the command and use a valid argument for the **-register_io_implementation** option.

SEE ALSO

set_core_wrapper_configuration (2). **set_core_wrapper_cell** (2).

UIT-1009 (error) Invalid argument for -one_wrapper_clock: '%s'. Argument must be either true or false.

DESCRIPTION

You receive this message if you execute either **set_core_wrapper_configuration** or **set_core_wrapper_cell** command and use an invalid argument for the **-one_wrapper_clock** option. Valid arguments are swap or in_place.

WHAT NEXT

Reexecute the command and use a valid argument for the **-one_wrapper_clock** option.

SEE ALSO

set_core_wrapper_configuration (2). **set_core_wrapper_cell** (2).

UIT-1010 (error) Scan %s '%s' element '%s' has internal and wrapper segments.

DESCRIPTION

This error message is generated when you try to include a core cell into a scan path or scan segment. A core cell is a cell with a test model and has both internal scan and wrapper segments. As internal scan segments and wrapper segments can't be mixed during core integration, you can't include such a cell with other elements of a scan path or a scan segment.

WHAT NEXT

Check if you have specified core_integration flag of dft configuration. If you are not integrating cores, remove such a specification and reinvoke the current command.

SEE ALSO

set_scan_path (2). **set_scan_segment** (2). **set_dft_configuration** (2). **remove_dft_configuration** (2).

UIT-1011 (error) Scan Chain '%s' has %s segments.

DESCRIPTION

This error message is generated when you try to include a wrapper or an internal scan segment with other segments in a scan path during core integration. Wrapper or internal scan segments can not be mixed with other segments during core integration.

WHAT NEXT

Check if you have specified core_integration flag of dft configuration. If you are not integrating cores, remove such a specification and reinvoke the current command.

SEE ALSO

set_scan_path (2). **set_dft_configuration** (2). **remove_dft_configuration** (2).

UIT-1012 (Error) Incorrect lockup element type specified.

DESCRIPTION

This is issued from the command **set_scan_configuration** or **set_scan_path**, when the user intends to specify the type of lockup element to be used (-lockup_type). Values for the lockup type are restricted to either "latch" or "flip_flop". By default, the lockup type is set to "latch"

WHAT NEXT

Check the value entered after the option -lockup_type.

UIT-1013 (Error) The period %f must evenly divide the default period %f.

DESCRIPTION

This error occurs when you use the -mbist_clock argument and the specified period does not evenly divide the default period. This relation is required to create the MBIST protocols.

WHAT NEXT

Specify a different clock period with the **create_test_clock** command, or change the default period with the **test_default_period** command.

SEE ALSO

create_test_clock (2) **test_default_period** (3)

UIT-1014 (Error) The parameter for the -write_ip_rtl option has to be enable, generate_only or disable.

DESCRIPTION

This message indicates that a set_dft_insertionj_configuration command has been issued, but the parameter for the option is not a valid one. The valid parameters are enable, generate_only or disable.

WHAT NEXT

Change the parameter for the option and re-issue the command.

SEE ALSO

set_dft_insertion_configuration, reset_dft_insertion_configuration, report_dft_insertion_configuration.

UIT-1015 (Error) The parameter for the -ip_rtl_format option has to be verilog or vhdl.

DESCRIPTION

This message indicates that a set_dft_insertionj_configuration command has been issued, but the parameter for the option is not a valid one. The valid parameters are verilog or vhdl.

WHAT NEXT

Change the parameter for the option and re-issue the command.

SEE ALSO

set_dft_insertion_configuration, reset_dft_insertion_configuration, report_dft_insertion_configuration.

UIT-1016 (error) %s.

DESCRIPTION

This error is generated when the **-design** or **-memory_ref** arguments of the **create_mbist_standalone** command specify a wrong design name.

WHAT NEXT

Make sure that the **-design** or **-memory_ref** arguments specify a valid design name then retry the **create_mbist_standalone** command.

SEE ALSO

create_mbist_standalone (2).

UIT-1020 (error) : Component signal type '%s' is not specified in user design interface signals.

DESCRIPTION

This error message is generated when you try to define a dft design with command define_dft_design. The error message is issued when a pin of the specified signal type is not included in the interface of the dft design.

WHAT NEXT

Reexecute the **define_dft_design** command and specify a dft design pin of the signal type with the **-interface** argument.

SEE ALSO

define_dft_design (2). **insert_dft** (2).

UIT-1021 (error) Unknown signal type '%s' is specified in user design interface signals.

DESCRIPTION

This error message occurs when attempting to define a DFT design with the **define_dft_design** command. The error message indicates that an unknown signal type is specified with the interface of the DFT design.

WHAT NEXT

If the port of the specified signal type is used in DFT insertion, add the correct signal type for the port and rerun the **define_dft_design** command.

SEE ALSO

define_dft_design(2)
insert_dft(2)

UIT-1022 (error) : Unable to find the specified design type '%s',

make sure that proper dw libs are included in link_library.

DESCRIPTION

This error message is generated when you try to define a dft design with command define_dft_design. The error message is issued when the specified design type is not a known design type. This can happen if all dw libraries are not specified with the link_library variable.

WHAT NEXT

Specify all dw libraries with link_library variable and rerun the define_dft_design command.

SEE ALSO

define_dft_design (2). **insert_dft** (2).

UIT-1023 (error) : One of the options '-design_name' or '-type' or '-all' is mandatory.

DESCRIPTION

This error message is generated when you try to remove a dft design with command remove_dft_design. The error message is issued when the command is run with insufficient options.

WHAT NEXT

Specify one of the options '-design_name' or '-type' or -all' with the remove_dft_design command.

SEE ALSO

define_dft_design (2). **insert_dft** (2).

UIT-1024 (error) : Options '-design_name', '-type', '-all' are

mutually exclusive, specify only one of them.

DESCRIPTION

This error message is generated when you try to remove/report a dft design with command remove_dft_design/report_dft_design. The error message is issued when the command is run with invalid combination of options. Please note that options '-design_name', '-type', '-all' of the command remove_dft_design/report_dft_design are mutually exclusive.

WHAT NEXT

Specify only one of the options '-design_name' or '-type' or -all' with the remove_dft_design/ report_dft-design commands.

SEE ALSO

define_dft_design (2). **insert_dft** (2).

UIT-1025 (error) : Design '%s' is not specified with define_dft_design command.

DESCRIPTION

This error message is generated when you try to remove/report a dft design with command remove_dft_design/report_dft_design. The error message is issued when the command is run with the '-design_name' option and the specified design is not defined using define_dft_design command.

WHAT NEXT

Check if the specified design is defined using define_dft_design command. You can use report_dft_design command to see all the user dft designs.

SEE ALSO

define_dft_design (2). **insert_dft** (2).

UIT-1026 (information) Memory-driven specification mode is enabled. You can not specify any Tests with the

set_mbist_controller command.

DESCRIPTION

You just enabled the MBIST configuration, and memory-driven specification mode is enabled, because you set the test_mbc_memory_driven_spec environment variable to true.

WHAT NEXT

All memory models should contain complete Test specifications. You can not specify any Tests with the **set_mbist_controller** command. This means all Test parameters (ie Test0, Test1, ...) are invalid.

SEE ALSO

set_mbist_configuration (2), **set_mbist_controller** (2), **test_mbc_memory_driven_spec** (3), **test_varbiables** (3).

UIT-1027 (warning) Memory-driven specification mode is enabled. The test you just defined will not be synthesized.

DESCRIPTION

The memory-driven specification mode is enabled, because you set the test_mbc_memory_driven_spec environment variable to true. This means that all synthesized tests are specified in the memory models. Any tests you define with the **define_mbist_program** command can only be used at run-time by the **set_mbist_run** command.

WHAT NEXT

Do not attempt to specify any Tests with the **set_mbist_controller** command. This means all Test parameters (ie Test0, Test1, ...) are invalid.

SEE ALSO

set_mbist_configuration (2), **set_mbist_controller** (2), **define_mbist_program** (2), **test_mbc_memory_driven_spec** (3), **test_varbiables** (3).

UIT-1028 (warning) Invalid option(s) specified to the

set_optimize_registers command.

DESCRIPTION

You receive this message if you execute the **set_optimize_registers** command with options that are not supported in non-XG mode.

WHAT NEXT

Please see the man page of the **set_optimize_registers** command for a list of options that are supported in XG/non-XG modes.

SEE ALSO

set_optimize_registers (2). **optimize_registers** (2).

UIT-1030 (error) Option -time, -clock_cycles and -signature can not be specified for instruction '%s'.

DESCRIPTION

You receive this error message when you execute the **set_bsd_instruction** command and specify time constant or signature for an invalid instruction. Time constants are supported only for the following instructions.

INTEST RUNBIST EXTEST_PULSE EXEST_TRAIN

Signature is supported only for RUNBIST instruction.

For EXTEST_PULSE instruction, options -time specifies minimum wait duration in real time and option -clock_cycles specifies minimum wait duration in TCK pulses. These two option are mutually exclusive for this instruction.

For EXTEST_TRAIN instruction minimum number of TCK pulses should be specified with -clock_cycles option in addition to maximum time with -time option.

WHAT NEXT

Reexecute the **set_bsd_instruction** command with out time constant and signature specifications.

SH SEE ALSO **find** (2), **set_bsd_instruction** (2).

UIT-1031 (error) Invalid IEEE1149 Std. version '%s', valid

values are : ieee1149.1_2001 | ieee1149.1_1993, ieee1149.6_2003 .

DESCRIPTION

You receive this error message when you execute the **set_bsd_configuration** command and specify an incorrect std. version. The following std. versions are leagl.

"ieee1149.1_1993" "ieee1149.1_2001" "ieee1149.1_2001 ieee1149.6_2003" "ieee1149.1_1993 ieee1149.6_2003" "ieee1149.6_2003"

Std. version "ieee1149.6_2003" is same as "ieee1149.1_2001 ieee1149.6_2003" .

The default valud for the Std. option is "ieee1149.1_2001" .

WHAT NEXT

Reexecute the **set_bsd_configuration** command with the correct std. version name(s).

SH SEE ALSO **find** (2), **set_bsd_configuration** (2).

UIT-1032 (Warning) IEEE1149 Std. versions ieee1149.1_2001, ieee1149.1_1993 are mutually exclusive, ignoring std. version ieee1149.1_1993 .

DESCRIPTION

You receive this error message when you execute the **set_bsd_configuration** command and specify an incorrect std. version. The following std. versions are leagl.

"ieee1149.1_1993" "ieee1149.1_2001" "ieee1149.1_2001 ieee1149.6_2003" "ieee1149.1_1993 ieee1149.6_2003" "ieee1149.6_2003"

Std. version "ieee1149.6_2003" is same as "ieee1149.1_2001 ieee1149.6_2003" .

The default valud for the Std. option is "ieee1149.1_2001" .

WHAT NEXT

Reexecute the **set_bsd_configuration** command with the correct std. version name(s).

SH SEE ALSO **find** (2), **set_bsd_configuration** (2).

UIT-1033 (error) Incorrect port '%s' with direction '%s' specified, only ports with direction 'out' or 'inout' are allowed.

DESCRIPTION

You receive this error message when you execute the **set_bsd_ac_port** command and specify an incorrect port. Only ports of type 'out' or 'inout' are allowed as ac ports.

WHAT NEXT

Reexecute the **set_bsd_ac_port** command with the correct ports.

SH SEE ALSO **find** (2), **set_bsd_ac_port** (2).

UIT-1034 (error) Insufficient number of options, specify either of options : -port_list | -all

DESCRIPTION

You receive this error message when you execute the **remove_bsd_ac_port** command and doesn't specify the required options. Either of the options -all or -port_list are required for this command.

WHAT NEXT

Reexecute the **remove_bsd_ac_port** command with the required options.

SH SEE ALSO **find** (2), **remove_bsd_ac_port** (2).

UIT-1035 (error) Options -port_list and -all are mutually exclusive, specify only one of them.

DESCRIPTION

You receive this error message when you execute the **remove_bsd_ac_port** command and specified conflicting options. Options -all and -port_list are mutually exclusive.

WHAT NEXT

Reexecute the **remove_bsd_ac_port** command with the either of -all or -port_list

options.

SH SEE ALSO **find** (2), **remove_bsd_ac_port** (2).

UIT-1036 (Warning) Port '%s' is not an ac port, not removing the port.

DESCRIPTION

You receive this error message when you execute the **remove_bsd_ac_port** command and specified a port which is not an AC port. You can only remove AC ports with this command.

WHAT NEXT

Reexecute the **remove_bsd_ac_port** command with the AC ports.

SH SEE ALSO **find** (2), **remove_bsd_ac_port** (2).

UIT-1037 (error) No Ac Ports found on the current design.

DESCRIPTION

You receive this error message when you execute the **remove_bsd_ac_port** command and there are no AC ports to be removed. Check if the current design is correct.

WHAT NEXT

If the current design is correct, the **remove_bsd_ac_port** command is not required as there are no AC ports to be removed.

SH SEE ALSO **find** (2), **remove_bsd_ac_port** (2).

UIT-1038 (error) Capture value not specified for the IDCODE or USERCODE instructions.

DESCRIPTION

You receive this error message when you execute the **set_bsd_instruction** command and doesn't specify capture value. Capture value is mandatory for these instructions.

WHAT NEXT

If the current design is correct, the **set_bsd_instruction** command with capture value.

SH SEE ALSO **find** (2), **set_bsd_instruction** (2).

UIT-1039 (Warning) Instruction '%s' does not exist, could not remove the instruction.

DESCRIPTION

You receive this error message when you execute the **remove_bsd_instruction** command and specify an unexisting instruction.

WHAT NEXT

Check for instruction name and reexecute the **remove_bsd_instruction** command with the correct instruction names.

SH SEE ALSO **find** (2), **remove_bsd_instruction** (2).

UIT-1040 (error) No instructions exist, cannot remove instructions.

DESCRIPTION

You receive this error message when you execute the **remove_bsd_instruction** command and there are no instructions specified for the current design.

WHAT NEXT

If the current design is correct, the **remove_bsd_instruction** command is unnecessary as there are instructions to be removed.

SH SEE ALSO **find** (2), **remove_bsd_instruction** (2).

UIT-1041 (error) Boundary Cell Types AC_1, AC_2, AC_7, AC_SELU, AC_SELX can't be used for ports which are not AC

ports.

DESCRIPTION

You receive this error message when you execute the **set_boundary_cell** command on specify AC BSR cells on a set of ports that are not AC ports. AC BSR cells can be used only on AC ports.

WHAT NEXT

Fix the problem and Reexecute the **set_boundary_cell** command with the correct specification.

SH SEE ALSO **find** (2), **set_boundary_cell** (2).

UIT-1042 (error) Invalid cell type '%s' specified with function '%s' for boundary scan.

DESCRIPTION

You receive this error message when you execute the **set_boundary_cell** command on specify a BSR cell type that is not supported with the specified function.

Here is the list of cell types allowed for different functions.

FUNCTION BSR Cell Types ========== input BC_1 | BC_2 | BC_4 | none input_inverted BC_1 | BC_2 | BC_4 | none output BC_1 | BC_2 | AC_1 | AC_2 | none output_inverted BC_1 | BC_2 | AC_1 | AC_2 | none bidir BC_7 | AC_7 | none bidir_inverted BC_7 | AC_7 | none control BC_1 | BC_2 | none observe BC_4 | none receiver_p BC_4 | BC_1 | BC_2 | none receiver_n BC_4 | BC_1 | BC_2 | none ac_select AC_SELU | AC_SELX | none
==========

WHAT NEXT

Fix the problem and Reexecute the **set_boundary_cell** command with the correct specification.

SH SEE ALSO **find** (2), **set_boundary_cell** (2).

UIT-1043 (error) Specified design '%s' is not a user dft design,

allowed design types : %s

DESCRIPTION

You receive this error message when you execute the **set_boundary_cell** command on specify a design name which is not of a standard dft design type.

Here is the list of allowed dft design types.

WC_D1 WC_D1_S WC_S1 WC_S1_S BC1 BC2 BC4 BC7 AC1 AC2 AC7 AC_SELU AC_SELX

WHAT NEXT

Fix the problem and Reexecute the **set_boundary_cell** command with the correct specification.

SH SEE ALSO **find** (2), **set_boundary_cell** (2).

UIT-1044 (Warning) Option '-share' is applicable only for Control/Ac Select Boundary Cells, ignoring the option.

DESCRIPTION

You receive this error message when you execute the **set_boundary_cell** command and specify option -share with an unspported function. This option can can be specified only with option -function values : control | ac_select .

WHAT NEXT

Fix the problem and Reexecute the **set_boundary_cell** command with the correct specification.

SH SEE ALSO **find** (2), **set_boundary_cell** (2).

UIT-1045 (error) Boundary Cell Name is mandatory for Control/ Ac Select boundary cells.

DESCRIPTION

You receive this error message when you execute the **set_boundary_cell** command and specify option -function with value control or ac_select and doesn't specify a name for the boundary cell. Option -name is mandatory for these function values.

WHAT NEXT

Fix the problem and Reexecute the **set_boundary_cell** command with the correct specification.

SH SEE ALSO **find** (2), **set_boundary_cell** (2).

UIT-1046 (error) Option '-ports' is mandatory with options '-class core_wrapper', '-class bsd'.

DESCRIPTION

You receive this error message when you execute the **set_boundary_cell** command and doesn't specify a list of ports with option -class values core_wrapper or bsd. Port list is mandatory for these class values.

WHAT NEXT

Fix the problem and Reexecute the **set_boundary_cell** command with the correct specification.

SH SEE ALSO **find** (2), **set_boundary_cell** (2).

UIT-1047 (error) Option '-cells' is not allowed with options '-class core_wrapper', '-class bsd'.

DESCRIPTION

You receive this error message when you execute the **set_boundary_cell** command and specified a list of cells with option -class values core_wrapper or bsd. Cell list is not allowed for these class values.

WHAT NEXT

Fix the problem and Reexecute the **set_boundary_cell** command with the correct specification.

SH SEE ALSO **find** (2), **set_boundary_cell** (2).

UIT-1048 (error) Options '-type' and 'design' are mutually

exclusive.

DESCRIPTION

You receive this error message when you execute the **set_boundary_cell** command and specified options -type and -design. These options are mutually exclusive.

WHAT NEXT

Fix the problem and Reexecute the **set_boundary_cell** command with the correct specification.

SH SEE ALSO **find** (2), **set_boundary_cell** (2).

UIT-1049 (error) Invalid boundary cell type with '-class core_wrapper', allowed values : WC_D1 | WC_D1_S | WC_S1 | WC_S1_S .

DESCRIPTION

You receive this error message when you execute the **set_boundary_cell** command and specified a cell tyep not suitable for option -class value core_wrapper. Only the following cell types are allowed for this class value.

WC_D1 WC_D1_S WC_S1 WC_S1_S

WHAT NEXT

Fix the problem and Reexecute the **set_boundary_cell** command with the correct specification.

SH SEE ALSO **find** (2), **set_boundary_cell** (2).

UIT-1050 (error) Invalid functin value with '-class core_wrapper', allowed values : input | output | control | bidir .

DESCRIPTION

You receive this error message when you execute the **set_boundary_cell** command and specified a function tyep not suitable for option -class value core_wrapper. Only the following function types are allowed for this class value.

input output control bidir

WHAT NEXT

Fix the problem and Reexecute the **set_boundary_cell** command with the correct specification.

SH SEE ALSO **find** (2), **set_boundary_cell** (2).

UIT-1051 (error) Ports '%s' can't be specified with function '%s' .

DESCRIPTION

You receive this error message when you execute the **set_boundary_cell** command and specified a function tyep not suitable for the specifed ports.

Here is a list of functions and allowed port types.

Function Name Port Direction ========== input input | bidir input_inverted input | bidir output output | bidir output_inverted output | bidir bidir bidir bidir_inverted bidir control output | bidir observe input | output | bidir receiver_p input | bidir receiver_n input | bidir ac_select output | bidir ==========

WHAT NEXT

Fix the problem and Reexecute the **set_boundary_cell** command with the correct specification.

SH SEE ALSO **find** (2), **set_boundary_cell** (2).

UIT-1052 (Warning) Boundary Cell '%s' overwrites an earlier specification.

DESCRIPTION

You receive this error message when you execute the **set_boundary_cell** command and the specification overwrites an earlier specification.

Here are situations where earlier specification is overwritten.

1. Option -name value is already specified for a previous Boundary Cell. Previous Boundary Cell is overwritten.

2. Option -function value is already specified for a previous Boundary Cell with common ports. Common ports are removed from the previous Boundary Cell.

3. A Boundary Cell with common ports and unspecified -function value is found. Common ports are removed from the previous Boundary Cell.

4. Option -function value is not specified and a Boundary Cell with common ports is found. Common ports are removed from the previous Boundary Cell.

WHAT NEXT

No action is required if overwriting earlier specification is ok with you.

SH SEE ALSO **find** (2), **set_boundary_cell** (2).

UIT-1053 (error) %s delay time (%10.2f) is required to be less than rise time value (%10.2f) for port '%s'.

DESCRIPTION

Input/Bidirectional delay time is greater than specified rise time of the port.

WHAT NEXT

Check your test_default_delay/test_default_bidir_delay and timing specification for the specified port.

UIT-1054 (error) Rise time (%10.2f) of port '%s' is required to be less than strobe time value (%10.2f).

DESCRIPTION

You have specified rise time of the specified port greater than the strobe time.

WHAT NEXT

Check your test_default_strobe and timing specification for the specified port.

UIT-1055 (warning) Bidir delay (%10.2f) must be less than

strobe time (%10.2f), setting bidir delay to input delay (%10.2f) .

DESCRIPTION

You have specified bidirectional delay time greater than the strobe time. Bidurectional delay time is reset to input delay time.

WHAT NEXT

Check your test_default_strobe and test_default_bidir_delay variables.

SH SEE ALSO **create_bsd_patterns** (2), **test_default_bidir_delay** (3).

UIT-1056 (warning) Bidir delay (%10.2f) must be less than period (%10.2f), setting bidir delay to input delay (%10.2f) .

DESCRIPTION

You have specified bidirectional delay time greater than the period. Bidurectional delay time is reset to input delay time.

WHAT NEXT

Check your test_default_period and test_default_bidir_delay variables.

SH SEE ALSO **create_bsd_patterns** (2), **test_default_bidir_delay** (3).

UIT-1057 (warning) Bidir delay (%10.2f) must be less than TCK rise time (%10.2f), setting bidir delay to input delay (%10.2f) .

DESCRIPTION

You have specified bidirectional delay time greater than the TCK rise time. Bidurectional delay time is reset to input delay time.

WHAT NEXT

Check your test_default_bidir_delay variable and rise time of TCK.

SH SEE ALSO **create_bsd_patterns** (2), **test_default_bidir_delay** (3).

UIT-1058 (error) Invalid Paramter Type '%s' specified for parameter '%s' .

DESCRIPTION

You have specified an unsupported paramater type with **define_dft_design** command. Only the following parameter types are supported.

string

boolean

float

list string

WHAT NEXT

Correct the specification and reissue the **define_dft_design** command.

SH SEE ALSO **define_dft_design** (2).

UIT-1059 (error) Invalid Paramter value '%s' specified for parameter '%s', expected value of type '%s' .

DESCRIPTION

You have specified an unsupported paramater value with **define_dft_design** command. Only the following parameter values are supported.

Parameter Type Parameter Value ============================== string string

boolean true | false

float floating point number

list string list of strings ==============================

WHAT NEXT

Correct the specification and reissue the **define_dft_design** command.

SH SEE ALSO **define_dft_design** (2).

UIT-1060 (error) Invalid List Paramter member type '%s' specified for parameter '%s' .

DESCRIPTION

You have specified an unsupported list paramater member type with **define_dft_design** command. Only the following parameter types are supported.

list string

WHAT NEXT

Correct the specification and reissue the **define_dft_design** command.

SH SEE ALSO **define_dft_design** (2).

UIT-1061 (error) Incorrect Pin Polarity '%s' specified for pin '%s', expected polarity : high | low .

DESCRIPTION

You have specified an unsupported pin polarity value with **define_dft_design** command. Only the following polarity values are supported.

high | h

low | l

WHAT NEXT

Correct the specification and reissue the **define_dft_design** command.

SH SEE ALSO **define_dft_design** (2).

UIT-1062 (error) Option '-params' is only allowed for dft designs of type 'PAD'.

DESCRIPTION

You have specified option '-params' for a dft design that is not of type 'PAD' with **define_dft_design** command. This option is supported only for dft designs of type 'PAD'.

WHAT NEXT

Correct the specification and reissue the **define_dft_design** command.

SH SEE ALSO **define_dft_design** (2).

UIT-1063 (error) Invalid Pad Access Pin Type '%s' specified for the PAD design '%s'.

DESCRIPTION

You have specified an unsupported pad access pin type for a pad design with **define_dft_design** command. Only the following pad access pin types are supported.

Pad Type	Allowed Access Pin Types			
any pad	capture_clk port ac_mode	capture_en shift_dr	update_clk low si	update_en high so
input	data_out mode_in	receiver_p ac_init_clk	receiver_n ac_init_data_n	ac_init_data_p observe
output	data_in	mode_out	ac_test	
tristate_output	data_in highz	mode_out	ac_test	enable
bidirectional	data_out data_in highz mode1_inout	receiver_p mode_out mode_in mode2_inout	receiver_n ac_test ac_init_clk observe	ac_init_data_p enable ac_init_data_n
open_drain_output	enable	mode_out	ac_test	highz
open_drain_bidirectional	enable data_out highz mode1_inout	receiver_p mode_out mode_in mode2_inout	receiver_n ac_test ac_init_clk observe	ac_init_data_p ac_init_data_n
open_source_output	enable	mode_out	ac_test	highz
open_source_bidirectional	enable data_out highz mode1_inout	receiver_p mode_out mode_in mode2_inout	receiver_n ac_test ac_init_clk observe	ac_init_data_p ac_init_data_n

WHAT NEXT

Correct the specification and reissue the **define_dft_design** command.

SH SEE ALSO **define_dft_design** (2).

UIT-1064 (error) Invalid Pad type '%s' specified for the PAD design '%s'.

DESCRIPTION

You have specified an unsupported pad type for a pad design with **pad_type** parameter of **define_dft_design** command. Only the following pad types are supported.

input

output

tristate_output

bidirectional

open_drain_output

open_drain_bidirectional

open_source_output

open_source_bidirectional

Note that the pad types need to be specified in the following format.

define_dft_design ... -params { pad_type string <pad_type> ... }

where <pad_type> is one of the pad types mentioned above.

WHAT NEXT

Correct the specification and reissue the **define_dft_design** command.

SH SEE ALSO **define_dft_design** (2).

UIT-1064a (error) No pad type found for the PAD design '%s'.

DESCRIPTION

This error message occurs because the pad type was not specified with the **-param {pad_type}** option of the **define_dft_design** command.

WHAT NEXT

Rerun the **define_dft_design** command with the **-param {pad_type}** option specifying a valid pad type.

SEE ALSO

define_dft_design(2)

UIT-1065 (error) Invalid Parameter '%s' of type '%s' specified, expected type '%s' .

DESCRIPTION

You have specified an unsupported parameter or unsupported parameter type for a pad design with **define_dft_design** command. Only the following parameters are supported.

Parameter Name Parameter Type ================================ pad_type string $disable_res$ string | boolean $differential$ string | boolean $bsr_segment$ list string lib_cell string | boolean lp_time string hp_time string on_chip string | boolean ================================

WHAT NEXT

Correct the specification and reissue the **define_dft_design** command.

SH SEE ALSO **define_dft_design** (2).

UIT-1066 (error) Invalid active_state value %s specified.

DESCRIPTION

You have specified an unsupported active_state value with **set_bsd_power_up_reset** command. Only the following active_state values are supported.

high low

WHAT NEXT

Correct the specification and reissue the **set_bsd_power_up_reset** command.

SH SEE ALSO **set_bsd_power_up_reset** (2).

UIT-1067 (error) Incorrect number of ports/values specified with option '-pattern'.

DESCRIPTION

You have specified an insufficient number of port/value pairs with option **-pattern** of **set_bsd_compliance** command. The syntax of the compliance pattern is as follows.

{ [<port_name> <port_value>]+ }

where <port_name> is the name of the port of the current design and <port_value> can be 0 or 1.

WHAT NEXT

Correct the specification and reissue the **set_bsd_compliance** command.

SH SEE ALSO **set_bsd_compliance** (2).

UIT-1068 (error) Specified IR width %d is not within 2-32 inclusive, ir_width specification discarded.

DESCRIPTION

You have specified an unsupported Instruction Register(IR) Width with **set_bsd_configuration** command. The IR width should be a positive number between 2 and 32.

WHAT NEXT

Correct the specification and reissue the **set_bsd_configuration** command.

SH SEE ALSO **set_bsd_configuration** (2).

UIT-1069 (error) Invalid value %s specified for option -

asynchronous_reset.

DESCRIPTION

You have specified an invalid value for option **-asynchronous_reset** of **set_bsd_configuration** command. The allowed values for this option are : true | false

WHAT NEXT

Correct the specification and reissue the **set_bsd_configuration** command.

SH SEE ALSO **set_bsd_configuration** (2).

UIT-1070 (error) Invalid value %s specified for option -instruction_encoding.

DESCRIPTION

You have specified an invalid value for option **-instruction_encoding** of **set_bsd_configuration** command. The allowed values for this option are : binary | one_hot

WHAT NEXT

Correct the specification and reissue the **set_bsd_configuration** command.

SH SEE ALSO **set_bsd_configuration** (2).

UIT-1071 (error) Invalid value %s specified for option -style.

DESCRIPTION

You have specified an invalid value for option **-style** of **set_bsd_configuration** command. The allowed values for this option are : synchronous | asynchronous

WHAT NEXT

Correct the specification and reissue the **set_bsd_configuration** command.

SH SEE ALSO **set_bsd_configuration** (2).

UIT-1072 (warning) UI option -ieee1149.1_1993 will be obsolete, please use option -std to specify the std. version.

DESCRIPTION

You have specified option -ieee1149.1_1993 with **set_bsd_configuration** command. This option is obsolete, use the new option **-std ieee1149.1_1993** to enable IEEE1149.1_1993 standard.

WHAT NEXT

Correct the specification and reissue the **set_bsd_configuration** command.

SH SEE ALSO **set_bsd_configuration** (2).

UIT-1073 (warning) Ignoring %s constant of pad design '%s'.

DESCRIPTION

You have specified LP_time or HP_time constants for a pad design and the value of this time constant is not valid.

The time is not valid if the time constant is less than 0.0

LP_time constant is also invalid if HP_time contant is not specified.

The time constant should be a positive real number in units of nano seconds.

WHAT NEXT

Correct the specification and reissue the **define_dft_design** and **preview_dft**, **insert_dft** commands.

SH SEE ALSO **define_dft_design** (2), **preview_dft** (2), **insert_dft** (2).

UIT-1074 (error) Std. Instruction '%s' is not allowed if support for ieee1149.6_2003 is not enabled.

DESCRIPTION

You have specified EXTEST_PULSE or EXTEST_TRAIN instruction with **set_bsd_instruction** command, but didn't enable IEEE1149.6_2003 standard. These two instructions are supported only if IEEE1149.6_2003 standard support is enabled with option **-std**

ieee1149.6_2003 of **set_bsd_configuration** command.

WHAT NEXT

Correct the specification and reissue the **set_bsd_configuration** and **preview_dft**, **insert_dft** commands.

SH SEE ALSO **set_bsd_configuration** (2), **preview_dft** (2), **insert_dft** (2).

UIT-1075 (warning) Port '%s' doesn't need an AC/DC Selector cell, not adding the selector cell for the port.

DESCRIPTION

You have specified that AC/DC selector cell should be added for the specified port and the tool determined that the port doesn't need such a BSR cell. AC/DC selector cells are added to control the AC mode pin of AC BSR cells. If an AC BSR cell(AC_1, AC_2, AC_7) doesn't drive a port, no AC/DC slection BSR cell is needed for the port.

WHAT NEXT

Correct the specification and reissue the **set_boundary_cell** and **preview_dft**, **insert_dft** commands.

SH SEE ALSO **set_boundary_cell** (2), **preview_dft** (2), **insert_dft** (2).

UIT-1076 (error) Invalid cell type '%s' for boundary scan tristate control register of port '%s', adding default control BSR cell to the port.

DESCRIPTION

You have specified an invalid BSR cell as a control BSR cell for a port with **set_oundary_cell** command. Valid control BSR cells are : BC_1 | BC_2 | none. A default BSR cell will be added as a control cell for the port. The default control BSR cell is BC_1 cell if INTEST instruction is specified, otherwise the default control cell is BC_2 BSR cell.

WHAT NEXT

Correct the specification and reissue the **set_boundary_cell** and **preview_dft**, **insert_dft** commands.

SH SEE ALSO **set_boundary_cell** (2), **preview_dft** (2), **insert_dft** (2).

UIT-1077 (error) Invalid cell type '%s' for boundary scan ac/dc select register of port '%s', not adding any ac/dc selector BSR cell to the port.

DESCRIPTION

You have specified an invalid BSR cell as a ac/dc selector BSR cell for a port with **set_oundary_cell** command. Valid ac/dc selector BSR cells are : AC_SELU | AC_SELX | none. No AC/DC selector BSR cell is added to the specified port.

WHAT NEXT

Correct the specification and reissue the **set_boundary_cell** and **preview_dft**, **insert_dft** commands.

SH SEE ALSO **set_boundary_cell** (2), **preview_dft** (2), **insert_dft** (2).

UIT-1078 (warning) BC_1 cell should be used for output control pins when INTEST is specified, using BC_1 cell for control pin of port '%s'.

DESCRIPTION

You have specified BC_2 BSR cell as the control cell for a port and also specified INTEST instruction. When INTEST instruction is specified, BC_2 BSR cell can't be used as a control BSR cell, adding BC_1 BSR cell as the control cell for the specified port.

WHAT NEXT

Correct the specification and reissue the **set_boundary_cell** and **preview_dft**, **insert_dft** commands.

SH SEE ALSO **set_boundary_cell** (2), **preview_dft** (2), **insert_dft** (2).

UIT-1079 (error) Polarity '%s' is not allowed of pad access pins

of type '%s'.

DESCRIPTION

You have specified an incorrect polarity for a pad access pin. Here is a list of pad access pins and the allowed polaritiues for each of them.

Padd Acces Pin Type Allowed Polarites ========== port high low ac_mode high low shift_dr high low capture_clk high low capture_en high low update_clk high low update_en high low data_out high low ac_init_data_p high low ac_init_data_n high low ac_init_clk high low mode_in high low data_in high low mode_out high low ac_test high low mode1_inout high low mode2_inout high low enable high low highz high low

observe high low high high high si high so high receiver_p high receiver_n high ==========

WHAT NEXT

Correct the specification and reissue the **define_dft_design** command.

SH SEE ALSO **define_dft_design** (2).

UIT-1080 (Warning) Port '%s' is not a linkage port, not removing the port.

DESCRIPTION

You receive this warning message when you execute the **remove_bsd_linkage_port** command and specified a port which is not a Linkage port. You can only remove Linkage ports with this command.

WHAT NEXT

Reexecute the **remove_bsd_linkage_port** command with Linkage ports.

SH SEE ALSO **remove_bsd_linkage_port** (2). **set_bsd_linkage_port** (2).

UIT-1081 (Error) No Linkage Ports found on the current design.

DESCRIPTION

You receive this error message when you execute the **remove_bsd_linkage_port** command and no linkage ports found on the current design. You can only remove Linkage ports

with this command.

WHAT NEXT

Reexecute the **remove_bsd_linkage_port** command with Linkage ports.

SH SEE ALSO **remove_bsd_linkage_port** (2). **set_bsd_linkage_port** (2).

UIT-1082 (Error) No Power Up Reset Ports found on the current design.

DESCRIPTION

You receive this error message when you execute the **remove_bsd_power_up_reset** command and no power up reset ports found on the current design. You can only remove Power Up Reset ports with this command.

WHAT NEXT

Reexecute the **remove_bsd_power_up_reset** command with Power Up Reset ports.

SH SEE ALSO **find** (2), **remove_bsd_power_up_reset** (2). **set_bsd_power_up_reset(2).**

UIT-1083 (Warning) Pattern-name '%s' is not in bsd compliance, not removing pattern-name.

DESCRIPTION

You receive this warning message when you execute the **remove_bsd_compliance** command and specified a pattern-name which is not set using set_bsd_compliance. You can only remove compliance pins with this command.

WHAT NEXT

Reexecute the **remove_bsd_compliance** command with compliance pins.

SH SEE ALSO **find** (2), **remove_bsd_compliance(2). set_bsd_compliance(2).**

UIT-1084 (Error) No Compliance Ports found on the current

design.

DESCRIPTION

You receive this error message when you execute the **remove_bsd_compliance** command and no compliance pins found on the current design. You can only remove Compliance pins with this command.

WHAT NEXT

Reexecute the **remove_bsd_compliance** command with Compliance pins.

SH SEE ALSO **find** (2), **remove_bsd_compliance** (2). **set_bsd_compliance** (2).

UIT-1085 (Warning) Cell '%s' is not a boundary cell IO, not removing the cell.

DESCRIPTION

You receive this warning message when you execute the **remove_boundary_cell_io** command and specified a cell which is not a Boundary Cell IO. You can only remove Boundary Cell IOs with this command.

WHAT NEXT

Reexecute the **remove_boundary_cell_io** command with Boundary cell IOs.

SH SEE ALSO **remove_boundary_cell_io** (2). **set_boundary_cell_io** (2).

UIT-1086 (Error) No Boundary Cell IOs found on the current design.

DESCRIPTION

You receive this error message when you execute the **remove_boundary_cell_io** command and no boundary cell IOs found on the current design. You can only remove Boundary IO cells with this command.

WHAT NEXT

Reexecute the **remove_boundary_cell_io** command with Boundary cell IOs.

SH SEE ALSO **remove_boundary_cell_io** (2). **set_boundary_cell_io** (2).

UIT-1087 (Error) Insufficient number of options, specify either of options : -cell | -all.

DESCRIPTION

You receive this error message when you execute the **remove_boundary_cell_io** command and doesn't specify the required options. Either of the options -all or -cell are required for this command.

WHAT NEXT

Reexecute the **remove_boundary_cell_io** command with the required options.

SH SEE ALSO **find** (2), **remove_boundary_cell_io** (2). **set_boundary_cell_io** (2).

UIT-1088 (Error) Options -cell and -all are mutually exclusive, specify only one of them.

DESCRIPTION

You receive this error message when you execute the **remove_boundary_cell_io** command and specified conflicting options. Options -all and -port_list are mutually exclusive.

WHAT NEXT

Reexecute the **remove_boundary_cell_io** command with the either of -all or -port_list options.

SH SEE ALSO **find** (2), **remove_boundary_cell_io** (2). **set_boundary_cell_io** (2).

UIT-1089 (error) Insufficient number of options, specify either of options : -name | -all

DESCRIPTION

You receive this error message when you execute the **remove_bsd_compliance** command and doesn't specify the required options. Either of the options -name or -all are

required for this command.

WHAT NEXT

Reexecute the **remove_bsd_compliance** command with the required options.

SH SEE ALSO **remove_bsd_compliance(2). set_bsd_compliance(2).**

UIT-1090 (Warning) Option '-name' is applicable only for Control/Ac Select Boundary Cells, ignoring the option.

DESCRIPTION

You receive this warning message when you execute the **set_boundary_cell** command and specify option -name with an unspported function. This option can can be specified only with option values : control | ac_select .

WHAT NEXT

Fix the problem and Re-execute the **set_boundary_cell** command with the correct specification.

SH SEE ALSO **find** (2), **set_boundary_cell** (2).

UIT-1091 (Warning) Option '-share' is applicable only for multiple Control/Ac Select Boundary Cells, ignoring the option.

DESCRIPTION

You receive this warning message when you execute the **set_boundary_cell** command and specify option -share with a single port in -ports option. The option -share is applicable only when used with multiple Control/Ac Select Boundary Cells.

WHAT NEXT

Fix the problem and Re-execute the **set_boundary_cell** command with the correct specification.

SH SEE ALSO **set_boundary_cell** (2). **set_scan_path** (2).

UIT-1093 (error) Invalid value %s specified for the -rtl option.

DESCRIPTION

This error message occurs when an invalid value is specified for the **-rtl** option of the **set_bsd_configuration** command. The allowed values for this option are **enable** or **disable**.

WHAT NEXT

Reissue the **set_bsd_configuration** command with either the **-rtl enable** or the **-rtl disable** option.

SEE ALSO

set_bsd_configuration(2)

UIT-1094 (warning) The -output option must be used with the -rtl enable option. Discarded the option.

DESCRIPTION

This warning message occurs when the **-output** option of the **set_bsd_configuration** command is specified, but the **-rtl** option is not set to **enable**. The **-output** option must be used with the **-rtl enable** option of the **set_bsd_configuration** command.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, reissue the **set_bsd_configuration** command with **-rtl enable** and **-output** options.

SEE ALSO

set_bsd_configuration(2)

UIT-1095 (error) The -rtl enable option must be used with the -

output option.

DESCRIPTION

This error message occurs when the the **-rtl enable** option of **set_bsd_configuration** command is specified without using the **-output** option. The **-rtl enable** option must be used with the **-output** option of the **set_bsd_configuration** command.

WHAT NEXT

Reissue the **set_bsd_configuration** command using both the **-rtl enable** option and the **-output** option.

SEE ALSO

set_bsd_configuration(2)

UIT-1096 (error) Test model does not exist for the design '%s'.

DESCRIPTION

This error message occurs when there is no test model for the design corresponding to the design you specified in the **use_test_model** command.

WHAT NEXT

Make sure you specified the design you intended, and that the design has an attached CTL model. To see a list of designs that have test models, use the **list_test_models** command. You may need to use the **read_test_model** command to attach a test model to the design specified in the error message.

SEE ALSO

list_test_models(2)
read_test_model(2)
report_test_models(2)
use_test_model(2)

UIT-1100 (Error) Invalid option value '%s'

DESCRIPTION

The value specified for the option is invalid

WHAT NEXT

Check the value

SEE ALSO

UIT-1101 (Error) Could not find valid link/reference for %s.

DESCRIPTION

You receive this error message in set_bsd_register command when the cell specified in the '-cell' option of the command does not have a valid reference. This might happen when the specified cell does not have a reference or when it has failed to link.

WHAT NEXT

Run the link command and fix the LINK-3 or LINK-5 errors reported on the cell.

SEE ALSO

link (2), **set_bsd_register** (2),

UIT-1102 (Error) Could not find valid link/reference for %s.

DESCRIPTION

You receive this error message in set_dft_signal command when the cell specified in the '-hookup_pin' option of the command does not have a valid reference. This might happen when the specified cell does not have a reference or when it has failed to link.

WHAT NEXT

Run the link command and fix the LINK-3 or LINK-5 errors reported on the cell.

SEE ALSO

link (2), **set_dft_signal** (2),

UIT-1110 (warning) DFT Hierarchy Location specification is not

honored when %s is enabled.

DESCRIPTION

You receive this warning message when you execute the **set_dft_location** command and also enable the following DFT clients for DFT insertion.

Wrapper Boundary Scan Logic Bist

When these clients are specified, user specified DFT Hierarchy location is not used in DFT insertion.

WHAT NEXT

Dft logic not added to user specified DFT Hierarchy during DFT insertion.

SH SEE ALSO **set_dft_location** (2), **set_dft_configuration** (2)

UIT-1111 (warning) DFT Hierarchy Location specification is ignored for Test Point, PLL or pipeline scan insertion.

DESCRIPTION

You receive this warning message when you execute the **set_dft_location** command and also enable the Test Point, PLL or pipeline scan insertion during DFT insertion.

When Test Point insertion, PLL or pipeline scan is enabled, Test Point, PLL or pipeline scan dft logic is not added to the user specified DFT Hierarchy location.

WHAT NEXT

Test Point, PLL or pipeline scan Dft logic not added to the user specified DFT Hierarchy during DFT insertion.

SH SEE ALSO **set_dft_location** (2), **set_dft_configuration** (2)

UIT-1112 (warning) Specified hierarchy name ’%s’ doesn’t exists in the current design ’%s’.

DESCRIPTION

You receive this warning message when you execute the **set_dft_location** command and specify an instance name with the command that doesn’t exists in the current design.

WHAT NEXT

DFT insertion creates the specified instance.

SH SEE ALSO **set_dft_location** (2), **insert_dft** (2)

UIT-1113 (error) Specified hierarchy name '%s' is not valid.

DESCRIPTION

You receive this warning message when you execute the **set_dft_location** command and specify an invalid instance name with the command.

WHAT NEXT

Check if the specified instance name is valid and reissue the command with the correct instance name.

SH SEE ALSO **set_dft_location** (2)

UIT-1114 (error) Specified name '%s' is not an instance of hierarchical design.

DESCRIPTION

You receive this warning message when you execute the **set_dft_location** command and specify a leaf level instance with the command.

The specified name should be an instance of a hierarchical design. Instances of black box modules, unresolved modules or library cells are not allowed as valid instance names for this command.

WHAT NEXT

Reissue the command with a valid hierarchical instance name.

SH SEE ALSO **set_dft_location** (2)

UIT-1115 (error) Specified instance '%s' %s.

DESCRIPTION

This error message occurs when an invalid instance is specified with the **set_dft_location** command.

Instances with dont_touch or test model or ILMs are not valid instances for the command. Instances inside a test model or ILM are not valid instances for the command.

WHAT NEXT

Reissue the command with a valid instance name.

SEE ALSO

set_dft_location(2)

UIT-1200 (error) The -none option cannot not be used with the -all option.

DESCRIPTION

You are advised to use the **-none** option to turn off optimizations during scan insertion and use **-all** option for performing all the optimizations during scan insertion.

WHAT NEXT

Modify the options accordingly to the recommendations and repeat the command.

SEE ALSO

insert_dft (2) **set_dft_optimization_configuration** (2)

UIT-1300 (Warning) Resetting wire load mode to '%s'.

DESCRIPTION

The wire load mode is set to a default value.

WHAT NEXT

Use the **set_wire_load_mode** command to adjust.

UIT-1310 (error) Core Integration of cores requires the option : -scan .

DESCRIPTION

You receive this message if you issue **set_dft_configuration -integration enable** and also specify the following option. *-scan disable* UI option *-integration* of command *set_dft_configuration* requires the option *-scan enable*. For more information, see the manual page for the **set_dft_configuration** command.

WHAT NEXT

Reissue **set_dft_configuration** command with valid options.

SEE ALSO

set_dft_configuration (2).

UIT-1311 (error) Core Integration of cores is mutually exclusive with options : -fix_set | -fix_reset | -fix_bus | -fix_bidirectional | -fix_clock | -fix_xpropagation | -control_points | -observe_points | -logicbist | -mbist | -wrapper | -scan_compression .

DESCRIPTION

You receive this message if you issue **set_dft_configuration -integration enable** and also specify one of the following options. *-fix_set enable -fix_reset enable -fix_bus enable -fix_bidirectional enable -fix_clock enable -fix_xpropagation enable -control_points enable -observe_points enable -logicbist enable -mbist enable -wrapper enable -scan_compression enable*

UI option *-integration* of command *set_dft_configuration* is mutually exclusive with the above options. For more information, see the manual page for the **set_dft_configuration** command.

WHAT NEXT

Reissue **set_dft_configuration** command with valid options.

SEE ALSO

set_dft_configuration (2).

UIT-1312 (error) Core Integration of cores doesn’t support the options : -clock_controller .

DESCRIPTION

You receive this message if you issue **set_dft_configuration -integration enable** and also specify one of the following options. *-clock_controller enable* UI option *-integration* of command *set_dft_configuration* is mutually exclusive with the option *-clock_controller enable* when the design doesn’t contain MBIST(Tech2) cores. For more information, see the manual page for the **set_dft_configuration** command.

WHAT NEXT

Reissue **set_dft_configuration** command with valid options.

SEE ALSO

set_dft_configuration (2).

UIT-1313 (error) Boundary Scan Synthesis is mutually exclusive with options : -scan | -fix_set | -fix_reset | -fix_bus | -fix_bidirectional | -fix_clock | -fix_xpropagation | -control_points | -observe_points | -wrapper | -scan_compression .

DESCRIPTION

You receive this message if you issue **set_dft_configuration -bsd enable** and also specify one of the following options. *-scan enable -fix_set enable -fix_reset enable -fix_clock enable -fix_xpropagation enable -control_points enable -observe_points enable -wrapper enable -scan_compression enable*

UI option *-bsd* of command *set_dft_configuration* is mutually exclusive with the above options. For more information, see the manual page for the **set_dft_configuration** command.

WHAT NEXT

Reissue **set_dft_configuration** command with valid options.

SEE ALSO

set_dft_configuration (2).

UIT-1314 (error) Boundary Scan Synthesis doesn't support the options : -mbist | -logicbist | -clock_controller .

DESCRIPTION

You receive this message if you issue **set_dft_configuration -bsd enable** and also specify one of the following options. *-logicbist enable -mbist enable -clock_controller enable* UI option *-bsd* of command *set_dft_configuration* is mutually exclusive with the option *-logicbist enable*. UI option *-bsd* of command *set_dft_configuration* is mutually exclusive with the option *-mbist enable* when not synthesizing MBIST(Tech1) logic. UI option *-bsd* of command *set_dft_configuration* is mutually exclusive with the option *-clock_controller enable* when not synthesizing MBIST(Tech2) logic. For more information, see the manual page for the **set_dft_configuration** command.

WHAT NEXT

Reissue **set_dft_configuration** command with valid options.

SEE ALSO

set_dft_configuration (2).

UIT-1315 (error) Boundary Scan Integration of MBIST/LBIST logic requires the option : -scan .

DESCRIPTION

You receive this message if you issue **set_dft_configuration -bsd enable** and also specify the following option. *-scan disable -mbist enable* OR *-logicbist enable* UI option *-integration* of command *set_dft_configuration* requires the option *-scan*

enable when *-mbist enable* OR *-logicbist enable* is also set. For more information, see the manual page for the **set_dft_configuration** command.

WHAT NEXT

Reissue **set_dft_configuration** command with valid options.

SEE ALSO

set_dft_configuration (2).

UIT-1316 (warning) The option -integration is not recommended and will be obsoleted in the 2007.03 release.

DESCRIPTION

You receive this message if you issue **set_dft_configuration -integration enable** command in XG mode or **set_dft_configuration -core_integration** command in DB mode.

It is not receommended to use Core Integration functionality, the functionality is going to be obsoleted in 2007.03 release.

In DB mode, core integration functionality is still supported only with **-bist** option.

WHAT NEXT

Reissue **set_dft_configuration** command with valid options.

SEE ALSO

set_dft_configuration (2).

UIT-1800 (error) '%s' is not defined as a TestMode port.

DESCRIPTION

The port defined in the **-encoding** option of the **define_test_mode** command is not defined as a **TestMode port**. The type of the port is defined by using the **set_dft_signal** command.

UIT-1801 (error) The value '%s' for the TestMode port is not correct.

DESCRIPTION

The value defined for the port in the **-encoding** option must be either equal to 0 or 1.

UIT-1802 (warning) The current mode already contains encoding.

DESCRIPTION

The current mode already contains encoding. The previous encoding specification will be overwritten.

UIT-1803 (error) The following compliance enable port is not an input or inout port: %s.

DESCRIPTION

The **set_bsd_compliance** command lets you specify a compliance enable pattern for a boundary scan design. Each compliance enable pattern consists of a set of port_name value pairs. Each port name in a compliance enable specification must correspond to an input or inout port of the design.

WHAT NEXT

Make sure that each port in the compliance enable pattern corresponds to an input or inout port of the design.

UIT-1804 (error) No patterns found to write native Verilog test bench file.

DESCRIPTION

This error is generated when the create_bsd_patterns does not generate any patterns that could be written to the native Verilog test bench.

WHAT NEXT

Check what caused no test bench patterns to be generated.

SEE ALSO

create_bsd_patterns (1). **write_test** (1).

UIT-1805 (Error) Specification of hookup sense without port sepecification is invalid.

DESCRIPTION

You receive this message because you have specified a hookup sense for a hookup pin without specifying the port name corresponding to this hookup pin. In the particular case of an internal pin specification, you should drop both the hookup sense and the port name.

WHAT NEXT

If you are in an internal pin flow, please drop the hookup sense specification. If you are not in an internal pin flow please specify the port name corresponding to your hookup pin. **set_dft_signal** command.

UIT-1806 (error) '%s' is defined several times in the encoding definition .

DESCRIPTION

The port defined in the **-encoding** option must be defined once.

UITCL-100 (error) Can’t get object name of multiple objects; Only a single object collection accepted.

DESCRIPTION

This command only accepts a collection that contains only one object.

WHAT NEXT

Try the command again with one object collection.

UITCL-101 (error) Cannot split list elements of value ’%s’ for variable ’%s’.

DESCRIPTION

The variable value is not a valid list. Therefore, its value cannot be processed correctly.

WHAT NEXT

Check the value of the given variable that is printed out by the error message.

UITCL-102 (warning) The update_script command is not supported in Tcl mode; Update_script is available in dcsh only. To translate dcsh to tcl format, use the dc-transcript program.

DESCRIPTION

This command is not supported in dc_shell Tcl mode.

WHAT NEXT

UITE

UITE-100 (error) Design mode configuration '%s' is not defined.

DESCRIPTION

The given design mode configuration is not defined.

WHAT NEXT

Design mode might be misspelled. Try report_design_modes to find out. To make a new design_mode_configuration, use create_design_mode.

UITE-101 (error) Design mode '%s' is not defined in mode configuration '%s'.

DESCRIPTION

The given design mode configuration does not contain the given mode. If no design modes configuration is specified, the first one is assumed.

WHAT NEXT

The design mode might be misspelled. Try report_design_mode to find out. The wrong design mode configuration might be assumed.

UITE-102 (error) No design modes have been defined.

DESCRIPTION

No design modes have been defined for the current design.

WHAT NEXT

To make a design_mode_configuration, use create_design_modes.

UITE-103 (error) Design mode group '%s' is already defined.

DESCRIPTION

There is already a design mode group of the specified name.

WHAT NEXT

To define a different design mode group, choose another name and enter the command again. Once a design mode group is defined, you cannot change it. You must reset all of the design modes and start again.

UITE-104 (error) Input port '%s' not found.

DESCRIPTION

Synchronize_inputs only works on top-level input or inout ports of the current design.

WHAT NEXT

To find the names of the existing input ports, use report_port.

UITE-105 (error) Port '%s' must be an input or inout port.

DESCRIPTION

Synchronize_inputs only works on the top-level input or inout ports of the current design.

WHAT NEXT

To find the names of the existing input and inout ports, use report_port.

UITE-106 (warning) The %s command will be discontinued in

future releases. This command has been replaced by %s

DESCRIPTION

A command has been renamed. The old command name is being supported temporarily but will cause syntax errors in future releases

WHAT NEXT

Use the new command instead of the discontinued command.

SEE ALSO

UITE-107 (error) Cannot set timing derates on a design that is not the current design.

DESCRIPTION

This message is issued if the user has called the set_timing_derate command with a design, which is not the current design, as an argument.

WHAT NEXT

If the user has intended to operate on the specified design, then set the current design using the current_design command.

SEE ALSO

set_timing_derate (2). **current_design** (2).

UITE-115 (error) Reference '%s' '%s' must be a leaf pin or port.

DESCRIPTION

-reference_pin should specify a leaf pin or port on some clock network, i.e. direct or transistive fanout of some clock source given by -clock.

WHAT NEXT

UITE-116 (Error) Edge value of clock '%s' is greater than its subsequent edge values.

DESCRIPTION

The value of each edge must be less or equal than its subsequent edge values. There must be an even number of edges and they are assumed to be alternating rise and fall.

WHAT NEXT

Use **report_clock** to check for clock information.

UITE-119 (Warning) Clock does not have waveform values monotonically increasing, so waveform has been adjusted.

DESCRIPTION

There must be an even number of edges, which are interpreted as alternating rising and falling edges. The edges must be monotonically increasing, except for a special case with two edges specified. When only two edge values are specified and the first value is greater than the second value, it is interpreted as a return-to-one waveform instead of the normal return-to-zero waveform if the falling edge adding one period is still larger than rising edge.

WHAT NEXT

UITE-120 (error) Invalid waveform. Edges must be an even number of
monotonically increasing values less than one period in duration.

DESCRIPTION

The specified clock waveform is not valid.

WHAT NEXT

UITE-121 (warning) Creating virtual clock named '%s' with no sources.

DESCRIPTION

This warning occurs when a virtual clock is created. A virtual clock has a name but no sources. This means it is not applied to any ports or pins in the design. A virtual clock can be used to specify input or output delay.

WHAT NEXT

The command **create_clock -period 10 -name CLK** does not apply the clock to any sources. If you want to apply the clock to a pin or port, you must specify the pin or port as in **create_clock -period 10 CLK** or **create_clock -period 10 -name CLK ff1/CP**.

UITE-122 (error) The 'create_clock' command cannot be used on output port '%s'.

DESCRIPTION

Clock sources must be input ports or internal pins. Inout ports can be used, but they are not recommended because of bus contention issues.

WHAT NEXT

Identify a valid set of sources and reapply the **create_clock** command.

UITE-123 (warning) Creating a clock source on inout port '%s'.

DESCRIPTION

A circuit, where a clock signal drives an inout port, can be unpredictable. If the port is functioning as an output while the clock is driving, bus contention occurs. If the clock is three-stated, any registers in the fanout of the clock can lose state.

WHAT NEXT

Verify that the circuit is safe according to your design rules. The PrimeTime product assumes that the clock is valid.

UITE-124 (error) Cannot remove internal path group '%s'.

DESCRIPTION

You cannot use **remove_path_group** to remove internal path groups (such as the default group).

WHAT NEXT

Reenter the command without the internal path group name.

UITE-125 (warning) Invalid delay direction for port '%s'.

DESCRIPTION

The entered port direction does not match the specifier used. For example, an input port is used with a -to specifier.

WHAT NEXT

Re-enter the command with valid port directions.

UITE-126 (error) Unable to %s on path from '%s' to '%s'.

DESCRIPTION

A timing exception command failed to apply or remove information on the specified path.

WHAT NEXT

UITE-127 (information) Found a design with sdf backannotation: (design '%s', file '%s').

Performance will be better by reading the db with -netlist_only and
then reading the sdf file with read_sdf.

DESCRIPTION

A design with sdf backannotation was read in from a db file. The performance of PrimeTime will be improved if the design db is read in order to obtain only the netlist (read_db -netlist_only), and the sdf data is read from an sdf file using read_sdf.

WHAT NEXT

UITE-128 (error) Unable to set %s on '%s'.

DESCRIPTION

Failed to execute the given set operation on the specified clock.

WHAT NEXT

UITE-129 (error) Unable to remove %s on '%s'.

DESCRIPTION

Failed to execute the given remove operation on the specified clock.

WHAT NEXT

UITE-130 (warning) Creating a clock on internal pin '%s'.

DESCRIPTION

Clock sources must be input ports. Internal pins can be used, but they are not recommended because they segment your path and prevent slew propagation. PrimeTime restarts slew propagation from the internal clock source pins and reset its value to zero as if the user issued a set_annotated_transition command with a value of zero on the internal clock source pin. You can use the set_annotated_transition command on the clock source pin to set a slew value different than zero.

WHAT NEXT

Identify a valid set of sources and reapply the **create_clock** command.

SEE ALSO

create_clock (2), **set_annotated_transition** (2).

UITE-131 (error) Design mode '%s' is already defined.

DESCRIPTION

There is already a design mode of the specified name.

WHAT NEXT

Choose a different design mode name and enter the command again, or remove the old design mode with the remove_design_mode command.

UITE-132 (warning) Mode '%s' does not exist on cell '%s'.

DESCRIPTION

There is no mode of the specified name on the cell.

WHAT NEXT

Use report_mode to determine the valid modes for the cell.

UITE-133 (error) Pin '%s' is not a valid %s.

DESCRIPTION

The specified pin is not a valid timing startpoint or endpoint. Some commands such as set_mode require that the from objects be valid timing startpoints, and the to objects be valid endpoints.

WHAT NEXT

Use input ports or register clock pins for the from objects, and output ports or register data pins for the to objects.

UITE-134 (warning) Creating a %s on multi-driven net '%s', only driver
pin '%s' is used as the source.

DESCRIPTION

It is recommended that you use only ports/pins as clock or generated clock sources. Net can be used as clock source, but the effective source used by PrimeTime is the driver pin of the net. If the net is multi-driven, only one of the driver pins is used as the source of the clock.

WHAT NEXT

Identify a valid set of sources and reapply the **create_clock** or **create_generated_clock** command.

SEE ALSO

create_clock (2), **create_generated_clock** (2).

UITE-135 (error) Creating a %s on net '%s' which does not have a driver pin as real source.

DESCRIPTION

It is recommended that you use only ports/pins as clock or generated clock sources. Net can be used as clock source, but the effective source used by PrimeTime is the driver pin of the net. If the net is multi-driven, only one of the driver pins is used as the source of the clock. If the net does not have a driver pin, the clock will not be correctly created.

WHAT NEXT

Identify a valid set of sources and reapply the **create_clock** or **create_generated_clock** command.

SEE ALSO

create_clock (2), **create_generated_clock** (2).

UITE-136 (warning) Creating a generated clock on hierarchical

pin '%s'.

DESCRIPTION

It is recommended that you do not specify a generated clock on a hierarchical design pin. PrimeTime may support generated clocks on hierarchical pins in the future.

WHAT NEXT

Move the generated clock to a leaf driver or load pin on the same net.

SEE ALSO

create_clock (2), **create_generated_clock** (2).

UITE-137 (warning) Creating '%s' on a hierarchical pin '%s'.

DESCRIPTION

Defining a constraint at a hierarchical pin causes the timing arcs (net arcs) from leaf pins driving this pin to leaf pins driven by this pin to be broken. This gives rise to two distinct limitations. First, the hierarchical boundary is a virtual designation and, generally, does not map to a specific physical location. Hence, PrimeTime cannot make any assumptions as to distributing the interconnect delay to the left and right of the bidirectional boundary. Second, breaking the original timing arcs may introduce a loss of timing information. For example, if the hierarchical pin were driven by three leaf pins and drives three other leaf pins, then breaking at the hierarchical boundary would reduce nine timing arcs to six, or worse, three considering the first limitation.

WHAT NEXT

Move the constraint to a leaf driver or load pin on the same net.

SEE ALSO

create_clock (2), **set_clock_sense** (2), **set_input_delay** (2), **set_output_delay** (2).

UITE-150 (warning) Negative clock latency specified: %g

DESCRIPTION

You specified a negative value to **set_clock_latency**. Although this is legal, it is

not typical.

WHAT NEXT

Ensure that you really wanted a negative value.

UITE-200 (error) Must specify %s option along with %s option.

DESCRIPTION

The two options must be together; if one of them is not specified, it is an error.

WHAT NEXT

Specify both the options together.

UITE-201 (warning) Option '%s' is valid only with option '%s'.

DESCRIPTION

The option specified is valid only if specified along with the other option.

WHAT NEXT

This option will be ignored, so you can remove this option from the command.

UITE-202 (error) The factor for -MULTIPLY_BY/-DIVIDE_BY '%d' is not a power of two.

DESCRIPTION

The -MULTIPLY_BY or -DIVIDE_BY factor should be a power of two, if not, it is an error.

WHAT NEXT

If the multiplication factor or division factor is not a power of two, model the clock derivation with -EDGES option.

UITE-203 (error) The number of edges specified '%d' is not an odd number larger than or equal to 3.

DESCRIPTION

The number of edges to make one period of the generated clock waveform has to be an odd number larger than or equal to 3.

WHAT NEXT

Carefully specify edges and ensure that you specify one full clock cycle using the edges.

UITE-204 (error) The number of edge_shifts specified '%d' using '-EDGE_SHIFT' option is not equal to the number of edges specifed '%d' using '-EDGES' option.

DESCRIPTION

The number of edge_shifts specified using the '-EDGE_SHIFTS' option must be equal to the number of edges specified using the '-EDGES' option.

WHAT NEXT

Make the number of edge_shifts equal to the number of edges.

UITE-205 (error) Expected to find, at most, two numbers along with the option '%s', but found %d.

DESCRIPTION

The options '-MAX_EDGE_DELAY/-MIN_EDGE_DELAY' can have, at the most, two numbers along with each, one for rise and one for fall edge.

WHAT NEXT

Specify only the rise and fall edge delays.

UITE-206 (error) The clock %s is a generated clock.

DESCRIPTION

A generated clock cannot be removed using 'remove_clock' command.

WHAT NEXT

To remove the generated clocks, use the **remove_generated_clock** command.

UITE-207 (error) A generated clock has already been defined with the name %s.

DESCRIPTION

A generated clock has already been defined with the name you specified.

WHAT NEXT

Either delete the generated clock and change the name, or change the name of the clock you are defining.

UITE-208 (error) You can specify only a single object for master clock source.

DESCRIPTION

The -source option takes only a single object as an argument.

WHAT NEXT

You can have a generated clock derived from a single clock. You cannot generate a clock from more than one master clock.

UITE-209 (error) You cannot specify an output port '%s' to be a

generated clock master source.

DESCRIPTION

Generated clock master can be an input or inout port or a pin.

WHAT NEXT

An output port cannot be a generated clock master.

UITE-210 (warning) Creating a generated clock on input or inout port ’%s’.

DESCRIPTION

When creating a generated clock on an input or inout port, please note that the generated clock would only derive its waveform characteristics from the master clock. Delay, on the other hand, is derived from delay information at the port itself. Additionally, creating a generated clock to drive an inout port can cause unpredictable circuit behavior. If the port is functioning as an output while the clock is driving, bus contention occurs. If the clock is three-stated, any registers in the fanout of the clock can lose state.

WHAT NEXT

Verify that the circuit is safe according to your design rules. The PrimeTime product assumes the generated clock is valid.

UITE-211 (Error) The -edges spec of generated clock ’%s’ has edge number
less than 1, the edge number should be from 1 up.

DESCRIPTION

The -edge specification in creat_generated_clock command should use edge number of the master clock which should be from 1 up. Zero or negative number are not allowed.

WHAT NEXT

Change your -edge spec in create_generated_clock coommand.

UITE-212 (Error) In the -edge specification of create_generated_clock
 '%s', the edge numbers must be in increasing order.

DESCRIPTION

In the -edge specification of a create_generated_clock command, the edge numbers specified must be in increasing order.

WHAT NEXT

Check the -edge spec in create_generated_clock command and edge numbers increasing.

UITE-213 (Warning) clock port '%s' cannot be assigned input delay relative to clock '%s'. Ignoring the value.

DESCRIPTION

When setting an input delay on clock port, it must be specified relative to the same clock. If a different clock is specified, this setting is ignored.

WHAT NEXT

Remove the unneeded input delay value using the **remove_input_delay** command.

UITE-214 (Information) Updating %-35s

DESCRIPTION

Shows the progress of update timing. The update timing can happen explicitly by calling update_timing or implicitly by calling one of the commands that need update timing.

UITE-215 (warning) Ignoring -significant_digits option with -

connections.

DESCRIPTION

Since the output of report_net with the -connections option formats the output according to the number of significant digits necessary, the -significant_digits option is ignored.

UITE-216 (warning) Object '%s' is not a valid %s.

DESCRIPTION

The specified object is neither a valid timing startpoint nor endpoint. Commands such as **set_false_path**, **set_multicycle_path**, and **group_path** require the **-from** option *from_list* objects to be valid timing startpoints and the **-to** option *to_list* objects to be valid timing endpoints.

One important limitation to note is that the call to **update_timing** command may cause the creation of path endpoints at combinational pins. One major example is clock gating checks if the pin connects to the signal gating the clock signal. In that case, entering an exception before an **update_timing** would emit this message, whereas doing so after an **update_timing** would not.

WHAT NEXT

Use input ports or register clock pins for the *from_list* objects. Use output ports or register data pins for the *to_list* objects.

SEE ALSO

group_path (2), **set_false_path** (2), **set_multicycle_path** (2), **update_timing** (2).

UITE-217 (warning) Forcing pin '%s' to be a timing %s.

DESCRIPTION

The specified pin is neither a valid timing startpoint nor endpoint. The **set_max_delay** and **set_min_delay** commands are point-to-point timing exception commands. In this case, these commands override the default single-cycle timing relationship for affected timing paths, so the matched component of each path has a new startpoint (if you specify the **-from** option) and a new endpoint (if you specify the **-to** option). The remaining portions of the path are left unconstrained at the specified pin.

WHAT NEXT

PrimeTime assumes the behavior described above is intended. If not, use input ports or register clock pins for the **from** *from_list* objects, and output ports or register data pins for the **-to** *to_list* objects.

SEE ALSO

set_max_delay (2), **set_min_delay** (2).

UITE-218 (Warning) set_clock_groups overwrote existing false paths.

DESCRIPTION

The **set_clock_groups** command won't analyze the paths between exclusive and asynchronous clocks. Previous manually defined false paths between these exclusive and asynchronous clocks will be removed by **set_clock_groups** command.

WHAT NEXT

Use the **report_exceptions** command to see the existing false paths. To undo the **set_clock_groups**, use the **remove_clock_groups** command.

SEE ALSO

set_false_path(2), set_clock_groups(2), remove_clock_groups (2), **report_exceptions(2).**

UITE-219 (warning) Exception overwrites a previous exception of the same type.

DESCRIPTION

The entered exception overwrites a previously entered exception that is of the same type: false path, multicycle path, min or max delay. The overwritten exception uses the same design objects in the specification. Part or all of the former exception will be discarded.

WHAT NEXT

Make sure that the appropriate exceptions are set to the desired design paths. Note that discarded exceptions will not appear as ignored in report_exceptions.

SEE ALSO

set_false_path (2), **set_multicycle_path** (2), **set_max_delay** (2), **set_min_delay** (2), **report_exceptions** (2).

UITE-220 (information) Design exceptions have been modified.

DESCRIPTION

Some user-entered false paths, multi-cycle paths, min or max delays, were cleaned up by the **transform_exceptions** command. While this clean up removed ignored path specifiers from the original specifications, the design paths utilization of the exceptions is unchanged.

WHAT NEXT

Refer to the man page for **transform_exceptions(2)** for more details.

UITE-221 (error) Transformation options %s are mutually exclusive.

DESCRIPTION

The **transform_exceptions** command options **-remove_ignored**, **-flatten**, **-use_to_for_endpoints** cannot be specified for the same command invocation. Since these are different transformations with different requirements that can be order dependent, the user cannot intermix these transformations.

WHAT NEXT

Separate the indicated transformation options into separate calls to the **transform_exceptions** command.

SEE ALSO

transform_exceptions (2).

UITE-222 (error) The feedback pin '%s' , and the output pin '%s'

do not belong to the same PLL.

DESCRIPTION

The feedback pin specified using the **-pll_feedback** and the output pin specified using the **-pll_output** option of **create_generated_clock** command do no belong to the same PLL. Since these pins belong to different cells, there is no valid feedback path for the PLL.

WHAT NEXT

Define a valid configuration for the PLL, where the feedback pin is connected to an output clock pin on the PLL.

UITE-223 (error) The source pin '%s' does not belong to the PLL cell '%s'.

DESCRIPTION

The master pin specified using the **-source** does not belong to the same PLL to which the feedback pin specified by the **-pll_feedback** belongs. During the defining of a PLL and its feedback path, the master pin specified using the **-source** option should be the reference clock pin of the PLL.

WHAT NEXT

Define a valid configuration for the PLL, where the master pin is the reference clock pin of the PLL.

UITE-300 (Error) %s '%s' in when expression: '%s' for libcell '%s'.

DESCRIPTION

There was an error while parsing the when expression for the specified library cell. Therefore, the when expression will be ignored.

WHAT NEXT

The library DB file has not been properly generated.

UITE-301 (Warning) Conflict in specifying '%s' with '%s'. Option '%s' will be used.

DESCRIPTION

The listed command options cause a conflict. The more specific option will be chosen.

WHAT NEXT

Look at the manpage for this command for more information on command options.

UITE-302 (Warning) Negative clock uncertainty specified: %g

DESCRIPTION

You specified a negative value to set_clock_uncertainty.

Typically, clock uncertainty should be positive. Negative uncertainty values are supported for constraining designs with complex clock relationships. Setting the uncertainty value to a negative number may lead to optimistic timing analysis and should be used with extreme care.

WHAT NEXT

Ensure that you really wanted a negative value.

UITE-303 (warning) Setting input delay on clock port '%s'. This will not be supported in future releases.

DESCRIPTION

The setting of an input delay on a clock port that does not fanout to a latch D pin is interpreted as clock source latency. However, this feature will not be supported in future releases.

WHAT NEXT

Use the **set_clock_latency** command with the **-source** option to specifically set clock source latency.

SEE ALSO

remove_clock_latency (2), **set_clock_latency** (2).

UITE-304 (warning) Setting input delay on clock port '%s', which also has a source latency. Input delay will be ignored.

DESCRIPTION

The setting of an input delay on a clock port that does not fanout to a latch D pin is interpreted as clock source latency. However, the clock also has a defined source latency, so the input delay is ignored.

SEE ALSO

remove_clock_latency (2), **set_clock_latency** (2).

UITE-305 (warning) Converting a propagated clock '%s' to an ideal clock.

DESCRIPTION

The direct setting of a clock network latency on a propagated clock converts it to a ideal clock.

WHAT NEXT

Verify that this is the intended behavior.

SEE ALSO

remove_clock_latency (2), **set_clock_latency** (2).

UITE-306 (Error) The %s command requires all clocks are active.

DESCRIPTION

You receive this error message because there is inactive clocks in the design. The

characterize_context require all clocks in the design are active.

WHAT NEXT

To active all clocks in the design, use the **set_active_clocks [all_clocks]** command. To report clock status, use the **report_clock** command.

SEE ALSO

set_active_clocks (2), **report_clock** (2).

UITE-307 (error) Clock %s exists in more than one group.

DESCRIPTION

The **set_clock_groups** command allows each clock can be defined in only one clock group.

WHAT NEXT

To define multiple groups related to the same clock, use multiple **set_clock_groups** commands.

SEE ALSO

set_clock_groups(2).

UITE-308 (Error) Clock group %s does not exist.

DESCRIPTION

All names must be predefined by the **set_clock_groups**.

WHAT NEXT

Use the **set_clock_groups** command to define clock groups. Use the **report_clock** command with -groups option to see existing clock groups.

SEE ALSO

remove_clock_groups(2), set_clock_groups(2), report_clock(2).

UITE-309 (warning) Exclusive or asynchronous clock groups specification supercedes set_false_path between clocks.

DESCRIPTION

A preceding **set_clock_groups** command already dictates that paths between some or all of the clocks specified in the current **set_false_path** exception will not be analyzed. Therefore, the exception will not be entered into PrimeTime and would not show in the output of the **report_exceptions** command. Note that if the exception specifies more clocks than present in the asynchronous or exclusive groups, then a reduced exception is entered such that this reduced exception is a subset of the original that only specifies clock to clock pairs not in the asynchronous or exclusive groups.

WHAT NEXT

Use **report_clock -groups** to view the current asynchronous or exclusive clock groups. Use the **remove_clock_groups** command to remove existing clock groups, if desired.

SEE ALSO

report_clock(2), set_clock_groups(2), remove_clock_groups(2), set_false_path(2).

UITE-310 (warning) CRPR command options will be discontinued in future releases.

DESCRIPTION

The user interface to clock reconvergence pessimism removal (CRPR) has changed. The following discontinued options:

-remove_clock_reconvergent_pessimism
-report_clock_reconvergent_pessimism

of the **report_timing**, **report_constraint**, and **get_timing_paths** commands are replaced with the following Boolean variable:

timing_remove_clock_reconvergence_pessimism

In future releases, use of the discontinued options will cause a syntax error.

WHAT NEXT

Use the new **timing_remove_clock_reconvergence_pessimism** variable instead of the

discontinued options. For details on backward compatibility, see the **timing_remove_clock_reconvergence_pessimism** man page.

SEE ALSO

get_timing_paths (2), **report_constraint** (2), **report_timing** (2), **timing_remove_clock_reconvergence_pessimism.** (3).

UITE-311 (error) CRPR command options cannot be used if the design is up to date.

DESCRIPTION

Until the following discontinued options:

-remove_clock_reconvergent_pessimism and
-report_clock_reconvergent_pessimism

of the **report_timing**, **report_constraint**, and **get_timing_paths** commands are completely removed, limited backward-compatibility support is provided: If the design is not up to date, then the following Boolean variable:

timing_remove_clock_reconvergence_pessimism

is automatically set to **TRUE**. If the design is up to date, then the command fails.

WHAT NEXT

Use the new **timing_remove_clock_reconvergence_pessimism** variable instead of the discontinued options. For more detail on backward compatibility, see the **timing_remove_clock_reconvergence_pessimism** variable man page.

SEE ALSO

get_timing_paths (2), **report_constraint** (2), **report_timing** (2), **update_timing** (2), **timing_remove_clock_reconvergence_pessimism.** (3).

UITE-312 (information) Variable timing_remove_clock_reconvergence_pessimism was set to

TRUE.

DESCRIPTION

Until the following discontinued options:

-remove_clock_reconvergent_pessimism
-report_clock_reconvergent_pessimism

of the **report_timing**, **report_constraint**, and **get_timing_paths** commands are completely removed, limited backward-compatibility support is provided. If the design is not up to date, then the following Boolean variable:

timing_remove_clock_reconvergence_pessimism

is automatically set to **TRUE**. If the design is up to date, then the command fails.

WHAT NEXT

Update your scripts to use the new **timing_remove_clock_reconvergence_pessimism** variable instead of the discontinued command options.

SEE ALSO

get_timing_paths (2), **report_constraint** (2), **report_timing** (2), **timing_remove_clock_reconvergence_pessimism.** (3).

UITE-313 (Information) '%s' has been renamed to '%s'.

DESCRIPTION

You receive this message because the *-exclusive* option has been renamed to *-logically_exclusive* since *-physically_exclusive* is added.

WHAT NEXT

Use the **report_clock** with -groups option to check what clock groups have been set.To remove the existing clock groups, use the **remove_clock_groups** command.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

UITE-314 (warning) Converting pin '%s' from propagated to ideal.

DESCRIPTION

Setting a clock network latency on a pin or port directly will convert all the latches in the transitive fanout to ideal if they were marked propagated before.

WHAT NEXT

Please verify that this is the intended behaviour.

UITE-315 (warning) Converting %s object '%s' from ideal to propagated.

DESCRIPTION

The direct setting of a propagated_clock attribute on a clock, pin, or port can convert all latches in the transitive fanout to propagated. This occurs if they were already marked ideal and had some network latencies set. The user-specified network latencies are removed and can not be recovered. This message is generated if you use the **set_propagated_clock** command on the objects (pin, port or clock) after setting network latencies by using the **set_clock_latency** command on the same objects.

WHAT NEXT

Verify that this is the intended behavior.

SEE ALSO

remove_clock_latency (2), **set_clock_latency** (2), **set_propagated_clock** (2).

UITE-316 (warning) Virtual clock '%s' cannot be made propagated.

DESCRIPTION

A virtual clock cannot be made propagated as it has no source and does not affect any register in the design.

WHAT NEXT

Remove the virtual clock from the clock list.

SEE ALSO

remove_clock (2).

UITE-317 (error) Exception is not set because no through objects could be found.

DESCRIPTION

The object list of the exception path is empty at the from, to, or through position. This might happen if the specified object in the command line is a net that does not have any global driver or is a cell with no output pins.

WHAT NEXT

Verify that this is the intended behavior.

UITE-318 (Warning) Clock groups with same clocks are already set.

DESCRIPTION

You receive this warning message because the clock groups you specified are already set by previous command.

WHAT NEXT

Use the **report_clock** with -groups option to check what clock groups have been set.To remove the existing clock groups, use the **remove_clock_groups** command.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

UITE-319 (warning) Setting clock latency on a non-clock pin or

port.

DESCRIPTION

The direct setting of a clock network latency on a non-clock pin or a port converts all latches in the transitive fanout to an ideal clock.

WHAT NEXT

Verify that this is the intended behavior.

SEE ALSO

remove_clock_latency (2), **set_clock_latency** (2).

UITE-400 (Error) No sequential clock pins in '%s' or its transitive fanout.

DESCRIPTION

You receive this message if you execute **report_clock_timing** with an input pin list (either *from_list* or *to_list*) that does not contain any sequential clock pins, nor any in the pins' transitive fanout. All pins in the *from_list* and *to_list* lists must be sequential clock pins, or must contain them in their transitive fanout.

WHAT NEXT

Reexecute the **report_clock_timing** command and ensure that all pins in the *from_list* or *to_list* are sequential clock pins, or that they have sequential clock pins in their transitive fanout.

SEE ALSO

report_clock_timing (2).

UITE-401 (Warning) Pins that are not sequential clock pins and contain no sequential clock pins in their transitive fanout have

been dropped from '%s'.

DESCRIPTION

You receive this message if the list of input pins submitted to **report_clock_timing** in the *to_list* or *from_list* contains pins that are not sequential clock pins, and do not have sequential clock pins in their transitive fanout. Such pins are not valid inputs to **report_clock_timing**. This message warns you that the offending pins are being omitted from the report.

WHAT NEXT

If it is acceptable to you for these pins to be excluded from the report, no action on your part is required. Otherwise, investigate why these were included in the lists of input pins, and make corrections accordingly. Then reexecute the **report_clock_timing** command, and ensure that all pins on the *from_list* and *to_list* are sequential clock pins, or that they have sequential clock pins in their transitive fanout.

SEE ALSO

report_clock_timing (2).

UITE-402 (Error) No pins specified by the given '%s' belong to the specified clock domains.

DESCRIPTION

You receive this message if you execute **report_clock_timing** and none of the pins on the input pin list (either *from_list* or *to_list*) belong to any of the clock domains specified by *clock_list*. All pins in the *from_list* and *to_list* must be clocked by one of the specified clocks.

WHAT NEXT

Reexecute the **report_clock_timing** command and ensure that all pins on the *from_list* and *to_list* are clocked by one of the clocks on the *clock_list*.

SEE ALSO

report_clock_timing (2).

UITE-403 (Warning) Pins specified by the given '%s' that do not belong to the specified clock domains have been dropped from the current %s report.

DESCRIPTION

You receive this message if you execute **report_clock_timing** with an input pin list (either *from_list* or *to_list*), and some of the pins do not belong to any of the clock domains specified by *clock_list*. All pins in the *from_list* and *to_list* must be clocked by one of the specified clocks. This message warns you that the offending pins are being omitted from the report.

WHAT NEXT

If it is acceptable to you for these pins to be excluded from the report, no action on your part is required. Otherwise, investigate why these were included in the lists of input pins, and make corrections accordingly. Then reexecute the **report_clock_timing** command, and ensure that all pins on the *from_list* and *to_list* are clocked by at least one of the clocks in *clock_list*.

SEE ALSO

report_clock_timing (2).

UITE-404 (Error) 'from_list' and 'to_list' contain no pins that are clocked by the same clock; therefore, the skew cannot be reported.

DESCRIPTION

You receive this message if you execute **report_clock_timing** and specify a skew report, but the *from_list* and *to_list*) do not contain any pins clocked by the same clock. Skew reports are produced by **report_clock_timing** only on a per-clock-domain basis. If both *from_list* and *to_list* are specified and *clock_list* is not, the set of clock domains clocking any pin in the *from_list* is intersected with the set of clock domains clocking any pin in the *to_list*. If this intersection is null, the skew report cannot continue.

WHAT NEXT

Reexecute the **report_clock_timing** command, and ensure that the *from_list* and *to_list* contain pins clocked by the same clock. If you do not specify the *clock_list*, ensure

that pins on the *from_list* and *to_list* belong to the same clock domain or set of domains.

SEE ALSO

report_clock_timing (2).

UITE-405 (Warning) Pins have been dropped from '%s', because they are not contained in the clock intersection with '%s'.

DESCRIPTION

You receive this message if you execute **report_clock_timing** and specify a skew report, but the *from_list* and *to_list* contain some pins that are not clocked by the same clock. Skew reports are produced by **report_clock_timing** only on a per-clock-domain basis. If both *from_list* and *to_list* are specified and *clock_list* is not, the set of clock domains clocking any pin in *from_list* is intersected with the set of clock domains clocking any pin in *to_list*. This message warns you that pins in either input list that are not part of any of these derived domains are being removed from the list of pins to report.

WHAT NEXT

This is a warning message only; no action is required on your part. In general, you can ignore this warning, because the **report_clock_network** command makes it easy to specify a superset of the clock pins of interest; the pruning referred to in this message is helpful to narrow down the superset of clock pins. However, if you have specified pins that you believe are part of a shared clock domain or set of domains, you should investigate why a sink pin in *to_list* is not included in ANY domain implied by *from_list*, or vice versa.

SEE ALSO

report_clock_timing (2).

UITE-406 (Error) No clock pins of '%s' sequential devices found.

DESCRIPTION

A skew report requires a set of clock pins capable of launching data and a set of clock pins capable of capturing data. The combination of *from_list*, *to_list*, and *clock_list* values specified in the **report_clock_timing** command failed to produce these two sets of pins.

WHAT NEXT

If you specify the *from_list* value, ensure that it contains clock pins of launching sequential devices, either explicitly or in its transitive fanout. If you specify the *to_list* value, ensure that it contains clock pins of capturing sequential devices, either explicitly or in its transitive fanout. If you specify the *clock_list* value, ensure that the clocks have associated networks (that they are not virtual clocks).

SEE ALSO

report_clock (2), **report_clock_timing** (2).

UITE-407 (Error) No clock pins of launching or capturing sequential devices are found.

DESCRIPTION

A latency or transition time report requires a set of clock pins capable of either launching or capturing data. The combination of *from_list*, *to_list*, and *clock_list* values specified in the **report_clock_timing** command failed to produce these pins.

WHAT NEXT

If you specify the *from_list* or *to_list* value, ensure that they contain clock pins of launching or capturing sequential devices, either explicitly or in their transitive fanout. If you specify the *clock_list* value, ensure that the clocks have associated networks (that they are not virtual clocks).

SEE ALSO

report_clock (2), **report_clock_timing** (2).

UITE-408 (Error) No sequential clock pins in '%s' or its transitive fanout are clocked.

DESCRIPTION

The specified list contains sequential device clock pins, but none of them are clocked.

WHAT NEXT

The specified input pin list (either the *from_list* or *to_list* value) must be part of the clock network of a defined clock. Check the clock definitions and the scope of their networks and determine if this is true.

SEE ALSO

all_clocks (2), **create_clock** (2), **report_clock** (2), **report_clock_network** (2), **report_clock_timing** (2).

UITE-409 (Error) No pins specified by the given '%s' belong to the specified '%s'.

DESCRIPTION

You receive this message if you execute an inter-clock skew report using **report_clock_timing** and none of the pins on the input pin list, either *from_list* or *to_list*, belong to the clock domains specified by *from_clock_list* or *to_clock_list* respectively. At least one pin in both *from_list* and *to_list* must be clocked by one of the specified clocks.

WHAT NEXT

Reexecute the **report_clock_timing** command and ensure that all pins on the *from_list* and *to_list* are clocked by one of the clocks on the *from_clock_list* and *to_clock_list* respectively.

SEE ALSO

report_clock_timing (2).

UITE-410 (Warning) Pins specified by the given '%s' that do not belong to the specified '%s' have been dropped from the current inter-clock skew report.

DESCRIPTION

You receive this message if you execute an inter-clock skew report using **report_clock_timing** and some of the pins on the input pin list, either *from_list* or *to_list*, do not belong to any of the clock domains specified by *from_clock_list* or

to_clock_list respectively. All pins in the *from_list* and *to_list* should be clocked by one of the specified clocks. This message warns you that the offending pins are being omitted from the report.

WHAT NEXT

If it is acceptable to you for these pins to be excluded from the report, no action on your part is required. Otherwise, investigate why these were included in the lists of input pins, and make corrections accordingly. Then reexecute the **report_clock_timing** command, and ensure that all pins on the *from_list* and *to_list* are clocked by one of the clocks on the *from_clock_list* and *to_clock_list* respectively.

SEE ALSO

report_clock_timing (2).

UITE-411 (Error) No clock pins of '%s' sequential devices found.

DESCRIPTION

An intre-clock skew report requires a set of clock pins capable of launching data and a set of clock pins capable of capturing data. The combination of *from_list*, *to_list*, *from_clock_list* and *to_clock_list* values specified in the **report_clock_timing** command failed to produce these two sets of pins.

WHAT NEXT

If you specify the *from_list* value, ensure that it contains clock pins of launching sequential devices, either explicitly or in its transitive fanout. If you specify the *to_list* value, ensure that it contains clock pins of capturing sequential devices, either explicitly or in its transitive fanout. If you specify *from_clock_list* or *to_clock_list*, ensure that the clocks have associated networks (that they are not virtual clocks).

SEE ALSO

report_clock (2), **report_clock_timing** (2).

UITE-412 (Error) Pin '%s' is not the clock pin of a sequential

device.

DESCRIPTION

You receive this message if you execute **report_crpr** with an input pin (either *from_pin* or *to_pin*) that is not a sequential clock pin. Both the *from_pin* and *to_pin* must be sequential clock pins.

WHAT NEXT

Reexecute the **report_crpr** command and ensure that the *from_pin* and *to_pin* are sequential clock pins.

SEE ALSO

report_crpr (2). **timing_remove_clock_reconvergence_pessimism.** (3).

UITE-413 (Warning) Searching unconstrained paths will take longer run-time than expected.

DESCRIPTION

The tool will search for unconstrained paths when constrained paths can not be found, which will involve partial update timing, and takes longer time than searching constrained paths.

WHAT NEXT

It is suggested that all paths in the design get constrained. The potential unconstrained paths may be caused by black boxes, no launching or capturing clocks, empty hierarchy, cells from IP instead of from library, etc. To check constraints in the design, please use the **check_timing** command. Specifing the to_pin_list can also reduce the number of endpoints to search and speed up the report timing process.

SEE ALSO

check_timing (2), **timing_report_status_level** (3), **report_timing** (2), **report_constraint** (2).

UITE-414 (Error) CRPR is currently switched off.

DESCRIPTION

This error message is being issued because the user has attempted to use some functionality related to Clock Reconvergence Pessimism Removal (CRPR) when it is not turned on (see the **report_crpr** man page).

WHAT NEXT

Set the variable, **timing_remove_clock_reconvergence_pessimism** to TRUE and carry out a full update_timing in order to have CRPR included in the timing analysis.

SEE ALSO

report_crpr (2), **timing_remove_clock_reconvergence_pessimism** (3).

UITE-416 (Warning) There %s %d invalid %s.

DESCRIPTION

When report_timing is specified with "*" or a cell name, there is possibility that many invalid startpoints or endpoints are gotten, such as **-from [get_pins FF/*]** includes input, output and asynchronous pins. The current behavior for PrimeTime will consider these invalid startpoints or endpoints as through points and continues the path searching. Even though it is convenient to use, it is not suggested since it usually takes longer run time.

WHAT NEXT

You can use filter to filter redundant or invalid objects, such as **-from [get_pins "FF/* -filter "is_clock_pin == true"]**. You also can use variable **timing_report_always_use_valid_start_end_points** to report using valid startpoints and endpoints only.

SEE ALSO

report_timing (2), **timing_report_always_use_valid_start_end_points** (3).

UITE-418 (Error) Could not find latch for pin '%s'.

DESCRIPTION

You receive this error message because the input clock pin (either *from_pin* or *to_pin*) you specified with the **report_crpr** command does not correspond to a sequential device or constrained port. Both the *from_pin* and *to_pin* must be sequential clock pins or constrained ports.

WHAT NEXT

Reexecute **report_crpr** and ensure that the *from_pin* and *to_pin* are sequential clock pins or constrained ports.

SEE ALSO

report_crpr (2); **timing_remove_clock_reconvergence_pessimism** (3).

UITE-421 (warning) Using the %s option to specify both launching and capturing clocks has been discontinued and will not be supported in future releases.

DESCRIPTION

The command **report_crpr** has been enhanced to account for cases where multiple clocks fan out to the clock pins of sequential devices. In order to account for this new behavior optional command arguments have been added to allow the user to specify the clocks incident on both the launching and capturing devices. See the man page for report_crpr for more detiails.

WHAT NEXT

After examining the man page repeat the command with the relevant arguments.

SEE ALSO

UITE-422 (warning) -leaf cannot be specified for pins/ports.

Ignoring -leaf.

DESCRIPTION

The all_connected command allows -leaf option to be specified for net objects. You are seeing this message because you specified -leaf for pins/ports.

WHAT NEXT

The command will proceed by ignoring the -leaf. So, you need not do anything.

UITE-423 (error) path_collection cannot be used with any other path search option.

DESCRIPTION

The path_collection is intended to be directly printed according to formatting options specified. No option that need path search, like -nworst, -from, -to etc. can be used with this option.

WHAT NEXT

Try use only print formatting options with path_collection.

UITE-424 (error) Regular path-based analysis works only when design is in on_chip_variation mode.

DESCRIPTION

Regular path-based analysis only recomputes paths when the analysis type of the design is set to *on_chip_variation*. When the analysis type is set to *single*, no recomputed paths are returned.

WHAT NEXT

Use **set_operating_conditions** to set the design to the *on_chip_variation* analysis mode.

UITE-425 (error) Cannot activate modes %s and %s on cell %s

as they are in the same mode group %s, no mode has been activated.

DESCRIPTION

It is not possible to activate more than one cell mode in a cell mode group at any one time.

WHAT NEXT

Select only one cell mode per cell mode group

UITE-426 (error) Cannot perform regular PBA on unconstrained paths.

DESCRIPTION

Regular PBA only recomputes constrained paths and ignores unconstrained paths, regardless of the value of the variable timing_report_unconstrained_paths. Also, the unconstrained paths will not be returned in the resulting collection.

WHAT NEXT

Only perform path-based analysis on constrained paths.

UITE-427 (warning) Setting a %s derate on hierarchical net '%s', all other portions of this net will also use this derate factor.

DESCRIPTION

This message is issued if the user has set a net-specific derate factor on a hierarchical portion of a global net. A global net is a net that spans a number of hierarchies.

Since PrimeTime will calculate only one delay for the entire global net the derate factor will be set for every net segment (hierarchical portion) in this global net.

WHAT NEXT

No user action required.

SEE ALSO

set_timing_derate (2), **report_timing_derate** (2).

UITE-428 (warning) Maximum of %d paths can be recalculated together.

DESCRIPTION

Regular path-based analysis is intended to remove pessimism from critical paths. Recalculating a huge number of paths can lead to significant runtime. If path-based analysis is performed on more paths than the limit, then only the worst paths up to the path limit will be recomputed and returned. This path limit does not include unconstrained paths that are skipped by regular path-based analysis.

WHAT NEXT

Please perform path-based analysis on small paths sets below the path limit. Alternatively, the **pba_disable_path_recalculation_limit** variable can be used to disable the path limit; however, please note that the runtime can be significant when recalculating large numbers of paths.

UITE-429 (warning) The timing path due to a data check constraint at pin '%s' has not been recalculated.

DESCRIPTION

PrimeTime does not support the path-based recalculation of paths due to data check constraints. These paths are returned directly without recalculation.

SEE ALSO

get_timing_paths (2), **report_timing** (2), **set_data_check** (2).

UITE-430 (warning) Variable timing_report_maxpaths_nworst_reached is suggested to use

with timing_report_always_use_valid_start_end_points.

DESCRIPTION

Variable timing_report_maxpaths_nworst_reached message may count more endpoints and less max paths if invalid start/through/end points are specified.

UITE-432 (warning) The %s variable is obsolete as of the %s release.

Do not use this variable as it is no longer supported.

DESCRIPTION

You received this message because you have set the indicated variable to a value other than the default value of the variable.

As of the indicated release of PrimeTime, this variable is obsolete and will no longer be supported in this or subsequent releases. In the indicated release, PrimeTime will honor the setting of this variable and issue this warning message. In subsequent releases, the behavior with default value of this variable will be supported only, and the variable will be removed from PrimeTime.

WHAT NEXT

Please remove the settings of this variable.

UITE-433 (warning) The %s option is obsolete as of the %s release.

Do not use this option as it is no longer supported.

DESCRIPTION

You received this message because you have used the indicated option of the command you are running.

As of the indicated release of PrimeTime, this option is obsolete and will no longer be supported in this or subsequent releases. In the indicated release, PrimeTime will honor the usage of this option and issue this warning message. In subsequent releases, the option will be removed from the command that you are running and you will receive an error message when you use the option.

WHAT NEXT

Please do not use this obsolete option of the command that you are running.

UITE-434 (warning) The %s option is obsolete as of the %s release.
Do not use this option as it is no longer supported.

DESCRIPTION

You received this message because you have used the indicated option of the report_timing or get_timing_paths command.

As of the indicated release of PrimeTime, this option is obsolete and will no longer be supported in this or subsequent releases. In the indicated release, PrimeTime will honor the usage of this option and issue this warning message. In subsequent releases, the option will be removed from the command that you are running and you will receive an error message when you use the option.

This variable is obsolete and replaced with the usage of the variable timing_enable_preset_clear_arcs. By setting the value of this variable to the non-default value, you can obtain the same effect as with this obsoleted option. You will, however, incur the CPU cost of a full update when the value of the variable is changed. In order to minimize the CPU cost, please do not change the value of the variable frequently.

WHAT NEXT

Please set timing_enable_preset_clear_arcs variable to true instead.

UITE-435 (Information) %s

DESCRIPTION

Display messages when variable **timing_report_maxpaths_nworst_reached** sets to TRUE.

WHAT NEXT

SEE ALSO

UITE-436 (warning) Resetting a %s derate on hierarchical net

'%s', all other portions of this net will also use this derate factor.

DESCRIPTION

This message is issued if the user has reset a net-specific derate factor on a hierarchical portion of a global net. A global net is a net that spans a number of hierarchies.

Since PrimeTime will calculate only one delay for the entire global net the derate factor will be reset for every net segment (hierarchical portion) in this global net.

WHAT NEXT

No user action required.

SEE ALSO

reset_timing_derate (2).

UITE-437 (warning) Implicitly setting the '%s' option for the set_timing_derate command.

DESCRIPTION

This message is issued if the user has called the set_timing_derate command with an object_list and has not explicitly set one of the net_delay, cell_delay or cell_check options.

WHAT NEXT

Explicitly specify one of the net_delay, cell_delay or cell_check options. The net_delay and cell_delay options may be specified together.

SEE ALSO

set_timing_derate (2).

UITE-438 (error) Ambiguous command. One of the net_delay,

cell_delay or cell_check options must be specified.

DESCRIPTION

This message is issued if the user has called the set_timing_derate command with an object_list and has not explicity set one of the net_delay, cell_delay or cell_check options and the object_list contains hierarchical cells.

WHAT NEXT

Explicitly specify one of the net_delay, cell_delay or cell_check options. The net_delay and cell_delay options may be specified together.

SEE ALSO

set_timing_derate (2).

UITE-445 (Information) %s

DESCRIPTION

Display messages when variable **timing_report_maxpaths_nworst_reached** sets to TRUE.

WHAT NEXT

SEE ALSO

UITE-446 (Warning) Enabling Clock Reconvergence Pessimism Removal (CRPR).

DESCRIPTION

This message is being issued because the user has enabled the adaptive CRPR engine (turned on by setting **timing_crpr_enable_adaptive_engine** to TRUE) when CRPR is turned off. The adaptive engine will only function when CRPR is turned on, hence CRPR has been enabled automatically.

See the man page for **timing_crpr_enable_adaptive_engine** for more details.

WHAT NEXT

Update scripts to set the variable **timing_remove_clock_reconvergence_pessimism** to TRUE.

SEE ALSO

timing_crpr_enable_adaptive_engine (2), **timing_remove_clock_reconvergence_pessimism** (3).

UITE-447 (Warning) Derate summary report may not match the output of report_timing without timing derates applied.

DESCRIPTION

This warning message is issued when the **report_timing** command has been called with the '-derate' option when the design has derate and signal integrity data and signal integrity analysis is enabled.

The derate summary report may not match the output of report_timing when there are no timing derates applied. Application of derates to aggressor nets will widen arrival windows thus making crosstalk interaction more likely. These additional crosstalk effects appear in the output of report_timing with derates applied. A full analysis with no derating applied would be required to remove these additional crosstalk effects.

If CRPR is on, then the clock reconvergence pessimism (due to derating) in the derate summary report shows the amount of CRP removed due to the static effect of derating. It is not possible to remove the additional crosstalk effects arising from derating.

WHAT NEXT

Reset the timing derates using the **reset_timing_derate** command and use report_timing to determine the effect of removing timing derates.

SEE ALSO

report_timing (2), **reset_timing_derate** (2), **si_enable_analysis** (2), **timing_remove_clock_reconvergence_pessimism** (3).

UITE-448 (Warning) Unrealistically large derate value specified:

%g

DESCRIPTION

This warning message is issued when the **set_timing_derate** command has been called with a derate value greater than 2.

A derate factor greater than 2.0 is unrealistically large. As a consequence, the values shown in the Derate Summary Report in the **report_timing** output may not be accurate.

WHAT NEXT

It is likely that the specified derate value is incorrect, because of a user input error. Please specify a more realistic derate factor within the range [0 to 2].

SEE ALSO

report_timing (2), **set_timing_derate** (2).

UITE-450 (Warning) Transferring ideal net attribute onto driver pin '%s' of net '%s'.

DESCRIPTION

This warning message occurs when the set_ideal_network command is called with nets specified in the object_list.

If a net is ideal then all it's driver pins must be ideal. The ideal network attribute is transferred from the specified net to the global driver pins of that net.

WHAT NEXT

No action is required.

SEE ALSO

set_ideal_network (2).

UITE-451 (Warning) Ignoring hierarchical pin '%s'. Object must

be a port, net or pin of a leaf cell.

DESCRIPTION

This warning message occurs when the set_ideal_network command is called with a hierarchical pin in the object_list. You cannot specify a hierarchical pin as an ideal network start point.

PrimeTime ignores the hierarchical pin specified in the warning message, but continues to set ideal networks on any remaining valid objects in the object_list.

WHAT NEXT

Specify only ports, nets or pins of leaf cells in the object_list. A leaf cell is a cell that does not contain other cells.

SEE ALSO

set_ideal_network (2).

UITE-452 (Warning) Ignoring net '%s' because the 'no_propagate' option is not specified.

DESCRIPTION

This warning message occurs when the set_ideal_network command is called with nets specified in the object_list and the 'no_propagate' option has not been specified.

WHAT NEXT

To set a net ideal use the 'no_propagate' option.

SEE ALSO

set_ideal_network (2).

UITE-453 (Warning) Overwritting previous ideal network that

was set on pin '%s'.

DESCRIPTION

This warning message occurs when the user sets an ideal network on a pin, which already has an ideal network set on it. The previous ideal network that was set on the pin is overwritten with this ideal network set on the pin.

WHAT NEXT

No action is required.

SEE ALSO

set_ideal_network (2).

UITE-454 (Warning) Ignoring hierarchical pin '%s'. Object must be a port or pin of a leaf cell.

DESCRIPTION

This warning message occurs when the set_ideal_latency command or set_ideal_transition command is called with a hierarchical pin in the object_list. You cannot annotate ideal timing values on a hierarchical pin.

PrimeTime ignores the hierarchical pin specified in the warning message, but continues to set ideal values on any remaining valid objects in the object_list.

WHAT NEXT

Specify only ports or pins of leaf cells in the object_list. A leaf cell is a cell that does not contain other cells.

SEE ALSO

set_ideal_network (2), **set_ideal_latency** (2), **set_ideal_transition** (2).

UITE-455 (Warning) Removing ideal attribute from driver pin

’%s’ of net ’%s’.

DESCRIPTION

This warning message occurs when the remove_ideal_network command is called with nets specified in the object_list.

If a net is ideal then all it’s driver pins must be ideal. The ideal network attribute is transferred from the specified net to the global driver pins of that net.

WHAT NEXT

No action is required.

SEE ALSO

remove_ideal_network (2).

UITE-456 (Warning) Ideal timing is specified on the non-ideal %s.

DESCRIPTION

This warning message occurs if the user has annotated ideal latency and/or ideal transition values on a pin or port that is not part of an ideal network. The annotated ideal timing values will only take effect if the object is part of an ideal network.

WHAT NEXT

If you intend to apply the annotated ideal timing values, then set an an network on the pin or port using the set_ideal_network command.

If you do not intend to apply annotated ideal timing values on the object, then remove the annotated ideal timing values using the remove_ideal_latency command and/or the remove_ideal_transition command.

SEE ALSO

set_ideal_network (2), **set_ideal_latency** (2), **set_ideal_transition** (2), **remove_ideal_latency** (2), **remove_ideal_transition** (2).

UITE-457 (Error) '%s' and '%s' are already defined as '%s' not allowing paths.

DESCRIPTION

You receive this error message because the *-allow_paths* defined by asynchronous clock groups is conflict with false path set by either the asynchronous, physically exclusive or logically exclusive clock groups for the same clock pair.

WHAT NEXT

Use the **report_clock** with -groups option to check what clock groups have been set.To remove the existing clock groups, use the **remove_clock_groups** command.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

UITE-458 (Error) '%s' and '%s' are already defined as -allow_paths in asynchronous clock groups.

DESCRIPTION

You receive this error message because the clock pair is already defined as asynchronous clock relationships which allow paths between these two clocks.

WHAT NEXT

Use the **report_clock** with -groups option to check what clock groups have been set.To remove the existing clock groups, use the **remove_clock_groups** command.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

UITE-459 (Error) Reference pin '%s' is not reached by any clock.

DESCRIPTION

You receive this error message because the input or output delay you defined on a pin or port with respect to a reference pin, which is not a fanout of any clock network. In case of no clock propagates to reference pin, the defined input/output delay will be ignored.

WHAT NEXT

It is suggested that reference pin for input/output delay constraints should be in the fanout of clock network. Please verify the connection of reference pin and modified the reference pin if needed.

SEE ALSO

set_input_delay (2), **remove_input_delay** (2), **set_output_delay** (2), **remove_output_delay** (2).

UITE-460 (Warning) Overwriting previously defined AOCVM value: %s.

DESCRIPTION

You received this warning message because the AOCVM value you have specified has overwritten a previously defined AOCVM value of the same type.

WHAT NEXT

No action is required. Use the **report_aocvm** command to show the AOCVM information that been defined.

SEE ALSO

set_aocvm_coefficient (2), **report_aocvm** (2).

UITE-461 (Error) Generated clock '%s' '%s' is not satisfiable%s

DESCRIPTION

This is an error message whenever the clock network traversal can not find a path

which satisfies the sense relationship defined by create_generated_clock command.

WHAT NEXT

Check for the generated clock definition to see if the generated clock is correctly defined. One example is that a divided_by 2 generated clock is driven by a inverter only. In this case, generated clock should be redefined with -invert with -divided_by 1. Another example is a divided_by 2 generated clock with preinverting. If master clock source pin is used as generated clock source pin, PrimeTime will issue the warning message. In this case, generated clock source pin should be redefined to clock pin of divider.

UITE-462 (Error) No constant bounding derates have been defined.

DESCRIPTION

You have received this message because you have attempted to perform a path-based AOCVM analysis using either the **report_timing** command or the **get_timing_paths** command, but no constant timing derates have been defined.

Constant derates are required to pessimistically bound derates calculated during a path-based AOCVM analysis. PrimeTime aborted the AOCVM analysis, because there are no constant derates and so there is no OCV pessimism for AOCVM to remove.

WHAT NEXT

Define constant bounding derates using the **set_timing_derate** command. Alternatively, consider using the graph-based AOCVM analysis, which *automatically* determines tight non-optimistic bounding derates for the path-based AOCVM analysis.

SEE ALSO

report_timing (2),
get_timing_paths (2),
set_timing_derate (2),
report_timing_derate (2),
timing_aocvm_enable_analysis (3).

UITE-463 (Error) No AOCVM derate factors have been defined.

PrimeTime cannot continue with AOCVM analysis.

DESCRIPTION

You have received this message because you have attempted to perform an AOCVM analysis, but no AOCVM derate factors have been defined. An AOCVM analysis requires AOCVM derate factors.

AOCVM derate factors are specified using the **read_aocvm** command.

WHAT NEXT

Either define AOCVM derate factors using the **read_aocvm** command.

SEE ALSO

read_aocvm (2), **report_aocvm** (2).

UITE-464 (Warning) No coordinates locations have been defined; AOCVM analysis may be inaccurate.

DESCRIPTION

You have received this message because you have attempted to perform an AOCVM analysis, but no coordinates locations have been defined.

Coordinates locations are used to calculate the systematic component of an AOCVM derate factor. The coordinates of various nodes of nets, pins, and ports are imported into PrimeTime from parasitic files using the **read_parasitics** command.

PrimeTime will continue with the AOCVM analysis and assume the most pessimistic coordinates locations possible.

WHAT NEXT

Set the **read_parasitics_load_locations** variable to **true** and read parasitics using the **read_parasitics** command.

SEE ALSO

report_timing (2), **get_timing_paths** (2), **read_parasitics** (2), **read_parasitics_load_locations** (3).

UITE-465 (Warning) No clock paths found. AOCVM requires a 'full_clock_expanded' path for an accurate analysis.

DESCRIPTION

You have received this message because you have attempted to perform an AOCVM analysis on a path, but the clock path has not been included.

PrimeTime will continue with the AOCVM analysis, however the analysis may be inaccurate due to the lack of information.

WHAT NEXT

Use the **get_timing_paths** command with the **-path_type** option to obtain a path with it's associated clock path.

SEE ALSO

get_timing_paths (2), **report_timing** (2).

UITE-466 (Warning) Ignoring hierarchical cell '%s'. Object must be a leaf cell or a library cell.

DESCRIPTION

This warning message occurs when the set_aocvm_coefficient command is called with a hierarchical cell in the object_list. You cannot annotate AOCVM coefficients on a hierarchical cell.

PrimeTime ignores the hierarchical cell specified in the warning message, but continues to set AOCVM coefficient values on any remaining valid objects in the *object_list*.

WHAT NEXT

Specify only leaf cells or library cells in the *object_list*. A leaf cell is a cell that does not contain other cells.

SEE ALSO

set_aocvm_coefficient (2), **report_aocvm** (2).

UITE-467 (Error) AOCVM and Variation-Aware analyses are mutually exclusive; PrimeTime will disable the AOCVM analysis.

DESCRIPTION

You have received this message because you have attemtped to perform an AOCVM analysis and a Variation-Aware analysis together. The analyses cannot be performed together.

WHAT NEXT

If you intend to perform a Variation-Aware analysis only, then no action is required.

If you intend to perform an AOCVM analysis, then you must disable Variation-Aware analysis, which is controlled using the PrimeTime variable **variation_enable_analysis**.

SEE ALSO

get_timing_paths (2), **report_timing** (2), **timing_aocvm_enable_analysis** (3), **variation_enable_analysis** (3).

UITE-468 (Information) The CRP value reported by report_timing and report_clock_timing will be %s.

DESCRIPTION

You are receiving this message because the report_crpr command has detected that its corresponding report_timing (or report_clock_timing) command is using a smaller CRP value. The report_crpr command reports the exact CRP value whereas report_timing (and report_clock_timing) use values calculated considering the CRPR threshold. This difference is a product of performance optimizations that are outlined in the next paragraph.

In order to prevent performance degradation during update_timing, CRPR groups sequential devices with similar CRP values (i.e. the difference between the CRP values is within the value of the crpr threshold). This can lead to some paths using a CRP value that will be smaller than the exact CRP. The difference between the two will be bounded by the value of the CRPR threshold.

WHAT NEXT

In order to align the CRP values used by report_timing, report_clock_timing and report_crpr the crpr threshold may be set to a smaller value. It should be noted that this can cause significant performance degradation during subsequent timing

updates.

SEE ALSO

timing_crpr_threshold_ps (3),

UITE-469 (error) Unable to set %s on '%s'.

DESCRIPTION

Failed to execute the given set operation on the specified object.

WHAT NEXT

UITE-470 (Warning) Ignoring systematic AOCVM coefficients in the derate table based flow.

DESCRIPTION

You have received this message because systematic AOCVM coefficients have been defined in a derate table based AOCVM flow.

Systematic AOCVM coefficients, specified using the **set_aocvm_ceofficient -systematic** command, are used only in the component based AOCVM flow; they will be ignored by PrimeTime in the derate table based flow.

WHAT NEXT

No action is required.

SEE ALSO

read_aocvm (2), **set_aocvm_coefficient** (2).

UITE-471 (Warning) Ignoring AOCVM components in the derate

table based flow.

DESCRIPTION

You have received this message because AOCVM components have been defined in a derate table based AOCVM flow.

AOCVM components, specified using the **set_aocvm_component** command, are used only in the component based AOCVM flow; they will be ignored by PrimeTime in the derate table based flow.

WHAT NEXT

No action is required.

SEE ALSO

read_aocvm (2), **set_aocvm_component** (2).

UITE-472 (Error) You cannot specify the -aocvm_guardband option of set_timing_derate in the derate_list of the timing_aocvm_derate_list variable.

DESCRIPTION

You have received this message because you have attempted set guardband derate factors using the **-aocvm_guardband** option of the **set_timing_derate** command in the *derate_list* of the **timing_aocvm_derate_list** variable.

WHAT NEXT

Remove the **-aocvm_guardband** option.

SEE ALSO

set_timing_derate (2), **timing_aocvm_derate_list** (3).

UITE-473 (Error) You cannot specify the -aocvm_guardband

option of set_timing_derate in the pba_derate_list variable.

DESCRIPTION

You have received this message because you have attempted set AOCVM guardband derate factors using the **-aocvm_guardband** option of the **set_timing_derate** command in the **pba_derate_list** variable. This usage is not permitted.

WHAT NEXT

Remove the **-aocvm_guardband** option.

SEE ALSO

set_timing_derate (2), **pba_derate_list** (3).

UITE-474 (Warning) The option '%s' is now the default and will be removed from the UI in a later release. You can use '%s' to get the old default behavior.

DESCRIPTION

You have received this message because you have issued an option that is now the default option on the command and will be removed from the UI in a later release.

WHAT NEXT

Remove the option for future.

SEE ALSO

UITE-475 (Warning) Usage of the timing_aocvm_derate_list variable is deprecated and will be obsoleted in the 2008.12 release of PrimeTime. Use 'set_timing_derate -aocvm_guardband' instead.

DESCRIPTION

You have received this message because you have attempted set AOCVM guard-band

derate components using the **timing_aocvm_derate_list** variable. This variable has been deprecated, and it will be obsoleted entirely in the 2008.12 release of PrimeTime.

WHAT NEXT

Use the **-aocvm_guardband** option on the **set_timing_derate** command to specify AOCVM guard-band derates instead. This option is only applicable in an AOCVM context. In a AOCVM context the derate factor that is applied to an arc is a product of the guard-band derate factor and the AOCVM derate factor.

SEE ALSO

set_timing_derate (2).

UITE-476 (Error) Graph-based AOCVM analysis must be performed in 'on_chip_variation' mode.

DESCRIPTION

You have received this message because you have attempted to perform graph-based AOCVM analysis in the 'single' or 'bc_wc' analysis mode, which is not supported.

WHAT NEXT

Use the **set_operating_conditions** command to set the design into 'on_chip_variation' mode.

SEE ALSO

report_design (2), **set_operating_conditions** (2), **timing_aocvm_enable_analysis** (3).

UITE-477 (Error) Graph-based delay-weighted AOCVM analysis cannnot be performed in worst_arrival mode.

DESCRIPTION

You have received this message because you have attempted to perform graph-based AOCVM analysis in the delay-weighted analysis mode, but the design is in worst_arrival mode.

WHAT NEXT

Set the **timing_slew_propagation_mode** variable to "worst_slew" and set the **si_xtalk_delay_analysis_mode** variable to "all_paths" if you want to perform graph-based AOCVM analysis in the delay-weighted analysis mode.

SEE ALSO

si_xtalk_delay_analysis_mode (3), **timing_slew_propagation_mode** (3), **timing_aocvm_analysis_mode** (3), **timing_aocvm_enable_analysis** (3).

UITE-478 (Error) Graph-based delay-weighted AOCVM analysis cannnot be used when the si_use_driving_cell_derate_for_delta_delay variable is set to true.

DESCRIPTION

You have received this message because you have attempted to perform graph-based AOCVM analysis in the delay-weighted analysis mode, but the **si_use_driving_cell_derate_for_delta_delay** variable is set to *true*.

WHAT NEXT

Set the **si_use_driving_cell_derate_for_delta_delay** variable to *false* if you want to perform graph-based AOCVM analysis in the delay-weighted analysis mode. Otherwise, if you need to use the **si_use_driving_cell_derate_for_delta_delay** variable, turn off graph-based AOCVM using the **timing_aocvm_enable_analysis** variable.

SEE ALSO

si_use_driving_cell_derate_for_delta_delay (3), **timing_aocvm_analysis_mode** (3), **timing_aocvm_enable_analysis** (3).

UITE-479 (Warning) Exhaustive path-based analysis may take a long time using the current PrimeTime settings. Try using the following settings, which may reduce the runtime of the

analysis:%s

DESCRIPTION

You have received this message because you have attempted to perform an exhaustive path-based analysis using settings that may considerably degrade the runtime of the analysis.

WHAT NEXT

The warning message suggests settings that should be changed to improve the runtime of the analysis.

SEE ALSO

report_timing (2),
get_timing_paths (2),
pba_aocvm_only_mode (3),
timing_aocvm_analysis_mode (3),
timing_aocvm_enable_analysis (3),
timing_remove_clock_reconvergence_pessimism (3),
timing_report_use_worst_parallel_cell_arc (3).

UITE-480 (Warning) The exhaustive path-based recalculation limit of %d has been exceeded at endpoint '%s' and group '%s'. The worst PBA slack found at this endpoint was %g. It is known that no PBA paths with slack worse than %g exist at this endpoint for this group.

DESCRIPTION

You have received this message because the user specified path-based endpoint recalculation limit has been met during an exhaustive search for worst paths at this endpoint. This message gives details on the endpoint that has not been exhaustively searched.

WHAT NEXT

Exhaustive path recalculation is a last mile analysis technique and as a result it should only be used when the design is close to signoff. Try to recalculate the endpoint using conservative values for slack_lesser_than, nworst and max_paths.

Increasing the user specified path-based endpoint recalculation limit may allow the endpoint to be exhaustively searched, however this will increase the runtime of the

analysis.

SEE ALSO

report_timing (2),
get_timing_paths (2),
pba_exhaustive_endpoint_path_limit (3),
timing_aocvm_analysis_mode (3).

UITE-481 (Warning) Usage of the 'set_aocvm_component' command is deprecated and will be obsoleted in the 2008.12 release of PrimeTime. Use the 'read_aocvm' command instead.

DESCRIPTION

You have received this message because you have attempted to set random or systematic AOCVM components using the **set_aocvm_component** command. The component-based AOCVM flow has been deprecated, and it will be obsoleted entirely in the 2008.12 release of PrimeTime.

WHAT NEXT

Use the **read_aocvm** command to specify AOCVM derates instead.

SEE ALSO

set_aocvm_component (2), **read_aocvm** (2).

UITE-482 (Error) Cannot specify a value for nworst (%d) greater than the exhaustive path-based recalculation limit (%d). Setting nworst to %d.

DESCRIPTION

You have received this message during a exhaustive path-based recalculation. An exhaustive path-based limit applies during this analysis and the user specified nworst value cannot exceed this limit.

WHAT NEXT

Set a conservative value for nworst. If necessary increase the path-based endpoint recalculation limit, however this will increase the runtime of the analysis.

SEE ALSO

report_timing (2),
get_timing_paths (2),
pba_exhaustive_endpoint_path_limit (3),
timing_aocvm_analysis_mode (3).

UITE-483 (Error) Usage of the 'delay_based_random_variation_model' analysis mode has been obsoleted.

DESCRIPTION

You have received this message because you have attempted to perform the 'delay_based_random_variation_model' AOCVM analysis mode. This AOCVM analysis mode was obsoleted 2008.06 release of PrimeTime.

WHAT NEXT

There is no action that can be taken to perform this type of analysis.

SEE ALSO

timing_aocvm_analysis_mode (3).

UITE-484 (warning) Timing path with -true is not recalculated.

DESCRIPTION

The command get_recalculated_timing_paths does not support recalculation of paths from -true option. Also these paths are not returned as part of the resulting collection.

UITE-485 (Error) Setting input delay on a clock port (%s) that does not fanout to any data sink.

DESCRIPTION

A set_input_delay was set on this clock input port. However, this input port has no data sinks, so the input delay has no effect. To specify clock latency instead of data input delays, the set_clock_latency command should be used.

WHAT NEXT

Be sure to use set_clock_latency with the -source option to specifically set clock latency. If a data sink is expected in the fanout of this input port, check the design.

SEE ALSO

remove_clock_latency (2), **set_clock_latency** (2).

UITE-486 (Error) Cannot specify a value for the pba_derate_list variable in an AOCVM context.

DESCRIPTION

You have received this message because you attempted to perform a path-based AOCVM analysis and you specified a value for the **pba_derate_list** variable.

WHAT NEXT

To perform a path-based AOCVM analysis, set the **pba_derate_list** variable to "". Otherwise, to use the derates specified in the **pba_derate_list** variable, you must remove all AOCVM information using the **remove_aocvm** command.

SEE ALSO

get_timing_paths (2), **report_timing** (2), **remove_aocvm** (2), **pba_derate_list** (3).

UITE-487 (Warning) AOCVM path-based analysis can take a long time if path-specific slew propagation is also performed.

DESCRIPTION

The **-pba_mode** option on **report_timing** (and **get_timing_paths**) instructs PrimeTime to perform both AOCVM PBA and regular PBA (path-specific slew propagation). The analysis runtime is significantly improved if only AOCVM path-based analysis is performed.

This message is only displayed once per session.

WHAT NEXT

If you intended to perform AOCVM and regular path-based analyses, then no action is

required.

If you intended to perform only AOCVM path-based analysis, then set the **pba_aocvm_only_mode** variable to true.

SEE ALSO

report_timing (2),
get_timing_paths (2),
pba_aocvm_only_mode (3),

UITE-488 (warning) Setting input delay on clock port ('%s') that has data sink(s). The behavior will change in future releases.

DESCRIPTION

The setting of an input delay on a clock port that has data sink(s) is also interpreted as clock source latency. However, this feature will not be supported in future releases.

WHAT NEXT

Use the **set_clock_latency** command with the **-source** option to specifically set clock source latency.

SEE ALSO

remove_clock_latency (2), **set_clock_latency** (2).

UITE-489 (Error) Setting input delay on clock port ('%s') relative to a clock (%s) defined at the same port. Command is ignored.

DESCRIPTION

The setting of an input delay on a clock port relative to a clock defined at the same port is ignored. The same signal at the port cannot be delayed relatif to itself.

WHAT NEXT

Please make review the constrainst. Input delay can be set at the clock port, but relative to a clock defined at another port.

SEE ALSO

remove_clock_latency (2), **set_clock_latency** (2).

UIV-1 (error) Specify one of the following: -list, -resize, -scroll, -enter,
-motion, -button, -key.

DESCRIPTION

WHAT NEXT

UIV-2 (error) If -scroll is specified, -value must also be specified.

DESCRIPTION

WHAT NEXT

UIV-3 (error) If -list, -resize and -scroll are not specified, -type

must be specified.

DESCRIPTION

WHAT NEXT

UIV-4 (error) ’%s’ is not a valid selection for ’%s’.

DESCRIPTION

WHAT NEXT

UIV-5 (error) View object ’%s’ does not exist.

DESCRIPTION

WHAT NEXT

UIV-6 (error) If -resize is not specified, widget_name must be specified.

DESCRIPTION

WHAT NEXT

UIV-7 (error) If resize is specified, the width and height must be

specified.

DESCRIPTION

WHAT NEXT

UIV-8 (error) If -list is specified, -value must also be specified.

DESCRIPTION

WHAT NEXT

UIV-9 (error) Window number '%d' does not exist.

DESCRIPTION

WHAT NEXT

UIV-10 (error) One of the -settings, -value arguments must be used.

DESCRIPTION

WHAT NEXT

UIV-11 (error) Parameters to the -settings argument must be strings.

DESCRIPTION

WHAT NEXT

UPF-001 (error) The %s command is not supported in non-UPF mode.

DESCRIPTION

This error message occurs when the specified command is supported only in UPF mode.

WHAT NEXT

Either start the tool in UPF mode or remove the unsupported command.

UPF-002 (error) The %s command is not supported in UPF mode.

DESCRIPTION

This error message occurs when the specified command is supported only in non-UPF mode.

WHAT NEXT

Either start the tool in non-UPF mode or remove the unsupported command.

UPF-003 (error) The %s option is not supported in non-UPF mode.

DESCRIPTION

This error message occurs when the specified option is supported only in UPF mode.

WHAT NEXT

Either start the tool in UPF mode or remove the unsupported option.

UPF-004 (error) The %s option is not supported in UPF mode.

DESCRIPTION

This error message occurs when the specified option is supported only in non-UPF mode.

WHAT NEXT

Either start the tool in non-UPF mode or remove the unsupported option.

UPF-005 (error) %s %s already exists.

DESCRIPTION

This error message occurs when the specified power domain already exists. Either the power domain name is already being used or you are trying to create a design-level power domain that covers the design top and one already exists.

WHAT NEXT

Specify a unique name for the power domain you are creating.

UPF-006 (error) Supply net %s already exists.

DESCRIPTION

This error message occurs when the specified supply net already exists. Supply net names must be unique.

WHAT NEXT

Specify a unique name for the supply net. Use the **get_supply_nets** command with the **-hierarchical** option to see all supply nets that have been defined.

SEE ALSO

get_supply_nets(2)

UPF-007 (error) Supply port %s already exists.

DESCRIPTION

This error message occurs when the specified supply port already exists. Supply port names must be unique.

WHAT NEXT

Specify a unique name for the supply port. Use the **get_supply_ports** command with the **-hierarchical** option to see all supply ports that have been defined.

SEE ALSO

get_supply_ports(2)

UPF-008 (error) Design element %s does not reside beneath the scope instance %s.

DESCRIPTION

This error message occurs when a design element specified in the element list of the power domain does not reside beneath the scope of the power domain.

WHAT NEXT

Make sure that all design elements specified in the **-elements** list are within the current scope or within the scope of the **-scope** instance, if specified.

SEE ALSO

create_power_domain(2)

UPF-009 (error) Power domain %s does not exist.

DESCRIPTION

This error message occurs when the specified power domain does not exist.

WHAT NEXT

Make sure that the power domain has been specified in the current scope and rerun

the command.

UPF-010 (error) Supply net %s does not exist.

DESCRIPTION

This error message occurs when the specified supply net does not exist.

WHAT NEXT

Specify the supply net in the current scope.

UPF-011 (error) Supply port %s does not exist.

DESCRIPTION

This error message occurs when the specified supply port does not exist.

WHAT NEXT

Specify the supply port with respect to the current scope.

UPF-012 (error) A leaf cell instance %s has been specified as the scope.

DESCRIPTION

This error message occurs when the specified leaf cell instance is named as the scope.

A leaf cell instance cannot be specified as the scope of any objects or as the current scope. Only a hierarchical instance can be specified as the scope.

WHAT NEXT

Make sure that the specified scope is not a leaf instance and rerun the command.

UPF-013 (error) Supply net %s is already connected to supply

port %s.

DESCRIPTION

This error message occurs when a connection from the specified supply net to the specified supply port already exists. The supply net cannot be connected to the supply port more than once.

WHAT NEXT

Review your script for the **connect_supply_net** command and make sure that the specified supply net and ports are named correctly in the current scope.

Use the **save_upf** command to check existing connections.

SEE ALSO

connect_supply_net(2)
save_upf(2)

UPF-014 (error) Inside/outside connection of supply port %s is already established to supply net %s.

DESCRIPTION

This error message occurs when the specified supply port already has inside/outside connections to the specified supply net.

A supply port can be connected by only one supply net on each side (inside/outside).

WHAT NEXT

Use the **save_upf** command to check existing connections.

SEE ALSO

save_upf(2)

UPF-015 (error) Invalid connection from supply net %s to supply

port %s.

DESCRIPTION

This error message occurs when attempting to make a connection from a supply net that is below the scope of the supply port. A supply port can be connected only by a supply net that is at or above the scope of the supply port.

WHAT NEXT

Specify a supply net that is at or above the scope of the supply port. Use the **save_upf** command to check existing connections.

SEE ALSO

save_upf(2)

UPF-016 (warning) Supply net %s is being replaced by %s as a %s connection for power domain %s.

DESCRIPTION

This warning message occurs when the primary power and ground nets of the power domain are already defined. This command supersedes the previous connections.

WHAT NEXT

This is only a warning message. No action is required.

SEE ALSO

set_domain_supply_net(2)

UPF-017 (warning) Attempting to read a UPF mode specific constraint '%s' in non-UPF mode. The constraint will be lost.

DESCRIPTION

This warning message occurs when attempting to read a .ddc file containing UPF mode specific constraints from a Design Compiler or IC Compiler shell running in non-UPF mode. The UPF mode specific constraints are not preserved in non-UPF mode and will be lost.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, you can either reapply the lost constraints using the equivalent non-UPF commands or start the shell in UPF mode and run the UPF commands again.

UPF-018 (warning) Attempting to read a non-UPF mode specific constraint '%s' in UPF mode. The constraint will be lost.

DESCRIPTION

This warning message occurs when you are attempting to read a .ddc file containing non-UPF mode specific constraints from a Design Compiler or IC Compiler shell running in UPF mode. The non-UPF mode specific constraints cannot be preserved in UPF mode and will be lost.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, you can either reapply the lost constraints using the equivalent UPF commands or start the shell in non-UPF mode and run the non-UPF commands again.

UPF-019 (error) At least one of the options %s or %s must be specified.

DESCRIPTION

This error message occurs when no options are specified. The tool requires that at least one of the two options shown in the message be specified.

WHAT NEXT

Use one or both of the options and rerun the command.

UPF-020 (error) Supply net %s is already created for power

domain %s.

DESCRIPTION

This error message occurs when the specified supply net already exists and is associated with the given power domain.

WHAT NEXT

Specify a different power domain and rerun the command.

UPF-021 (error) Supply port %s cannot be created at the logical instance %s.

DESCRIPTION

This error message occurs when a hierarchical name is specified as a supply port, but the logical instance path is invalid for the scope instance.

A scope instance must already exist and cannot be a leaf cell.

WHAT NEXT

Use the **get_cells** command to verify that the scope instance exists. Make sure that the scope instance is not a leaf cell.

SEE ALSO

get_cells(2)

UPF-022 (error) Hierarchical name %s cannot be specified for create_supply_port command when -domain is specified.

DESCRIPTION

This error message occurs when running the **create_supply_port** command with the **-domain** option specified. Because **create_supply_port** creates the supply port in the scope of the power domain, a hierarchical name cannot be specified for the supply port.

WHAT NEXT

Specify a simple name for the supply port if you run **create_supply_port** with the **-domain** option. Specify a hierarchical name for the supply port if you run **create_supply_port** without the **-domain** option.

See the **create_supply_port** man page for complete syntax information.

SEE ALSO

create_supply_port(2)

UPF-023 (error) Strategy %s already exists on power domain %s.

DESCRIPTION

This error message occurs when attempting to define a specified strategy that already exists.

WHAT NEXT

Use a unique strategy name and rerun the command.

UPF-024 (error) The UPF value conversion table '%s' already exists.

DESCRIPTION

This error message occurs when the specified value conversion table you are trying to define already exists.

WHAT NEXT

Specify a unique name for the value conversion table you are defining and rerun the command.

UPF-025 (error) The UPF value conversion table '%s' cannot be

found.

DESCRIPTION

This error message occurs when the specified value conversion table does not exist.

WHAT NEXT

Create the required value conversion table using the **create_hdl2upf_vct** or **create_upf2hdl_vct** command.

SEE ALSO

create_hdl2upf_vct(2)
create_upf2hdl_vct(2)

UPF-026 (error) Strategy %s does not exist on power domain %s.

DESCRIPTION

This error message occurs when using the **set_retention_control** command to specify a retention strategy that has not been defined for the given power domain.

WHAT NEXT

Check that the retention strategy name is correct and that **set_retention** has been defined for the specified retention strategy and the specified power domain.

SEE ALSO

set_retention(2)
set_retention_control(2)

UPF-027 (error) Options %s and %s are mutually exclusive.

DESCRIPTION

This error message occurs when attempting to use two command options that cannot be used together.

WHAT NEXT

The specified options are mutually exclusive and cannot be used together. Use only one of the options and rerun the command.

UPF-028 (error) Bind checker has already been defined on %s.

DESCRIPTION

This error message occurs when attempting to bind a checker to a cell that already has the checker defined.

WHAT NEXT

Remove the existing checker on the cell and then bind a new checker on the cell.

UPF-029 (error) The top-level design instance has been defined.

DESCRIPTION

This error message occurs when setting the top-level design instance on a design that already has a top-level design instance defined.

WHAT NEXT

Make sure that the **set_design_top** command is run only once for the design.

SEE ALSO

set_design_top(2)

UPF-030 (error) The connection is abandoned because it invalidates the power state table.

DESCRIPTION

This error message occurs when attempting to connect a supply net or port to another supply net or port when the power state table does not allow the connection. The connection operation is abandoned because it would invalidate the power state table.

WHAT NEXT

Remove the power state table and rerun the command.

UPF-031 (error) Port state format is not acceptable: %s.

DESCRIPTION

This error message occurs when the supply port state specified in the **add_port_state** command does not follow the UPF standard:

```
add_port_state port_name
   -state {name <nom | <min nom max> | off> }
```

WHAT NEXT

Use the syntax shown above and rerun the command.

SEE ALSO

add_port_state(2)

UPF-032 (error) Port state ’%s’ has been defined.

DESCRIPTION

This error message occurs when the specified input port state name was previously defined. The input port state name has already been used on the port.

WHAT NEXT

Specify a unique name for the port state and rerun the command.

UPF-033 (error) Same or connected supply net or port of ’%s’ is already in the supply list.

DESCRIPTION

This error message occurs when the specified supply net or port either already exists in the power state table supply list, or is connected to another port or net in the supply list.

A supply net or port can appear only once in the supply list of the power state table. If a port or net is connected to another port or net, they cannot be in the supply list simultaneously.

WHAT NEXT

The supply list keeps only one supply net or port for each supply net or port group. Remove the redundant supply net or port from the supply list.

UPF-034 (error) Can not find power state table '%s'.

DESCRIPTION

This error message occurs when the specified power state table name in the command does not match the previously defined name of the power state table.

WHAT NEXT

Use the previously defined name of the power state table and rerun the command.

UPF-035 (error) Cannot find port state '%s'.

DESCRIPTION

This error message occurs when the tool cannot find the specified port state.

In each power state table, each supply net or port can accept only a state that has been defined on a connected port or itself.

WHAT NEXT

Use the **write_script** or **save_upf** command to view the states that have been defined for a supply port. Specify a defined port state name and rerun the command.

SEE ALSO

save_upf(2)
write_script(2)

UPF-036 (error) The connection is abandoned because it

causes conflicting port states.

DESCRIPTION

This error message occurs when attempting to connect two ports that have the same state name but have different contents.

WHAT NEXT

Remove the conflicting port states and rerun the command.

UPF-037 (error) Level shifter strategy '%s' has been defined.

DESCRIPTION

This error message occurs when attempting to define a level shifter strategy that is already defined. A level shifter strategy can be defined only once.

WHAT NEXT

Make sure that level shifter strategies are defined only once on a domain. Use the **save_upf** command to view the defined level shifter strategies.

SEE ALSO

save_upf(2)

UPF-038 (error) A level shifter strategy has been defined on '%s'.

DESCRIPTION

This error message occurs when a level shifter strategy is already defined on the specified design element. A design element can have only one level shifter strategy.

WHAT NEXT

Make sure that level shifter strategies are defined only once on an element.

UPF-039 (error) Power switch %s already exists.

DESCRIPTION

This error message occurs when a power switch with the specified name already exists and cannot be created again.

WHAT NEXT

Use a unique name for the new power switch and rerun the command.

UPF-040 (information) Setting upf_version outside of a UPF file has no effect.

DESCRIPTION

This information message occurs when the **upf_version** variable is set outside of the context of a UPF file. In this situation, changing the **upf_version** variable has no effect.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

upf_version(3)

UPF-041 (warning) The UPF version in file %s does not match the version you requested from load_upf (%s). Some constraints and options may not function.

DESCRIPTION

This warning message occurs when you specify with the **load_upf -version** command a UPF version that is different from that specified with the **upf_version** command in the UPF file.

WHAT NEXT

Ensure that the commands in your UPF file conform to the UPF version you specified

with the **load_upf** command.

However, if the result is not what you intended, specify the correct UPF version and rerun the **load_upf** command.

SEE ALSO

load_upf(2)

UPF-042 (warning) The UPF command '%s' is not supported by %s.

DESCRIPTION

This warning message occurs when the current application does not support the specified UPF command, so the command is ignored. Some applications do not support all of the UPF commands.

Each instance of an ignored UPF command generates one UPF-042 warning message. Then, after the **load_upf** command completes, a UPF-043 summary message informs you of how many of each type of UPF command was ignored.

WHAT NEXT

If the result is not what you intended, check the UPF file for unsupported commands.

For a complete list of supported commands, see the **load_upf** command man page.

SEE ALSO

load_upf(2)

UPF-043 (information) Ignored %d unsupported '%s' command %s.

DESCRIPTION

This is a summary message indicating how many instances of a particular UPF command were ignored by the **load_upf** command because the command is not supported.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

load_upf(2)

UPF-044 (error) Errors reading UPF file: %s. Use error_info for more information.

DESCRIPTION

This error message is generated by the **load_upf** command when a syntax error occurs during the reading of a UPF file. The text of the message shows the specific error.

WHAT NEXT

Use the **error_info** command to show the file and line number of the syntax error.

SEE ALSO

error_info(2)

UPF-045 (error) Detected circular references to file %s while loading UPF file %s.

DESCRIPTION

This error message occurs when you attempt to load a UPF file that references itself; this results in a circular reference, which is illegal. The following is an example of a circular reference:

```
File 1.upf:
load_upf 2.upf

File 2.upf:
load_upf 1.upf
```

WHAT NEXT

Remove the **load_upf** command that causes the circular reference.

UPF-046 (warning) Removed control signal from '%s' strategy.

DESCRIPTION

This warning message occurs because when objects used as reference for a UPF control signal are removed, the related UPF constraint is also removed. Design objects like ports and pins can be removed by direct commands such as **remove_design**.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this warning message, apply UPF constraints after all design manipulations, the design object can be found when loading the UPF constraints.

SEE ALSO

remove_design(2)

UPF-047 (error) Could not set the scope to %s. load_upf failed.

DESCRIPTION

This error message occurs when the scope specified with the **load_upf -scope** command does not exist.

WHAT NEXT

Ensure that the design contains a cell instance name that matches the string supplied to the **-scope** option. After making any changes, rerun the command.

SEE ALSO

load_upf(2)

UPF-048 (error) RTL port %s cannot be made a supply port because it is already connected by a signal net.

DESCRIPTION

This error message occurs when the specified RTL port is already being used as a signal port.

An RTL port can only be set as a supply port (using the **add_port_state** or **connect_supply_net** command) if the port is not connected to a signal net.

WHAT NEXT

Make sure that the **add_port_state** or **connect_supply_net** syntax is correct, or disconnect the RTL port from the signal net. After making your changes, rerun the command.

SEE ALSO

add_port_state(2)
connect_supply_net(2)

UPF-049 (error) Name space conflict while trying to create object %s.

DESCRIPTION

This error message occurs when a UPF command attempts to create

- An object with the same name as an existing design object
- A power domain with the same name as an instance or a port in the same scope

WHAT NEXT

Ensure that objects specified in your UPF file are not the same as existing objects in the same name space.

UPF-050 (error) Supply net %s cannot be connected as ground and also have a nonzero operating voltage or a nonzero on state%s.

DESCRIPTION

This error message occurs when a supply net that has been connected as ground has a nonzero operating voltage or a nonzero "on" state in the power state table.

A supply net that has already been specified as a ground net cannot have an operating voltage or a nonzero "on" state. Conversely, a supply net that has an operating voltage or a nonzero "on" state cannot be used as a ground net.

WHAT NEXT

Check that all supply nets connected as ground are specified to operate at zero volts and do not have nonzero "on" supply states.

UPF-051 (error) The power network and ground network cannot be connected together.

DESCRIPTION

This error message occurs when attempting to connect the power supply network and the ground supply network. The power and ground supply networks cannot be connected to each other.

WHAT NEXT

Use the **write_script** or **save_upf** command to review all of the UPF commands, and disconnect the power network from the ground network.

SEE ALSO

save_upf(2)
write_script(2)

UPF-052 (error) Supply net %s cannot have different operating voltages from other supply nets (e.g. %s) connected to it as a single metal through supply ports.

DESCRIPTION

This error message occurs when attempting to specify an operating voltage different from other supply nets connected to it as a single metal through supply ports.

All supply nets connected together as a single metal through supply ports must share common operating voltages. Supply nets having different operating voltages cannot be connected together through supply ports.

WHAT NEXT

If you have previously applied the **set_voltage** command on several supply nets connected together, apply **set_voltage** on these supply nets simultaneously to change their operating voltages. To do this, specify multiple supply nets in the **-object_list**. Connecting supply nets that have different operating voltages is

illegal.

SEE ALSO

set_voltage(2)

UPF-053 (error) Option %s in the given UPF command is not supported.

DESCRIPTION

This error message occurs when attempting to run a UPF command with an option that is not supported by UPF.

WHAT NEXT

Omit the unsupported option and rerun the command.

UPF-054 (warning) The power state table can only be created in the top-level scope.

DESCRIPTION

This warning message occurs when attempting to create a power state table that is not in the top-level scope.

Creating a power state table is not allowed if the current scope is not on the top level of the design.

WHAT NEXT

Change the scope to the top level of the design using the **set_scope** command, and rerun the **create_pst** command.

SEE ALSO

create_pst(2)
set_scope(2)

UPF-055 (error) Top-level power domain is not yet defined.

DESCRIPTION

This error message occurs when attempting to run the **compile** or **check_mv_design** command without defining the top-level power domain. The top-level power domain must be defined in order for synthesis to proceed.

WHAT NEXT

Create the top-level power domain using the **create_power_domain** command.

SEE ALSO

create_power_domain(2)

UPF-056 (error) No primary supply nets (power and ground) have been defined for power domain %s.

DESCRIPTION

This error message occurs because the primary power and ground nets are not defined for the specified power domain. Primary supply nets must be defined for all power domains in the design.

WHAT NEXT

Define the primary power and ground nets for the specified power domain using the **set_domain_supply_net** command.

SEE ALSO

set_domain_supply_net(2)

UPF-057 (error) Supply net %s does not have a defined operating voltage%s.

DESCRIPTION

This error message occurs because the specified supply net is defined in the design but does not have an defined operating voltage.

All supply nets defined in the design must have a defined operating voltage in order for synthesis to proceed.

WHAT NEXT

Apply the operating voltages using the **set_voltage** command.

SEE ALSO

set_voltage(2)

UPF-058 (error) Supply net %s cannot be used in domain %s.

DESCRIPTION

This error message occurs because the specified supply net is not defined for the given domain. A supply net can only be used in the domains for which it has been defined.

WHAT NEXT

Define an existing supply net for a new domain using the **create_supply_net -reuse** command.

SH "SEE ALSO"

create_supply_net(2)

UPF-059 (error) Isolation name %s already used.

DESCRIPTION

This error message occurs when the specified isolation name is already in use. The **set_isolation** command cannot define an isolation strategy with a name that has already been used to define another isolation strategy in the same power domain.

WHAT NEXT

Use a unique name to define the isolation strategy and rerun the command.

SEE ALSO

set_isolation(2)

UPF-060 (error) %s default isolation already exists for this domain.

DESCRIPTION

This error message occurs when attempting to define default isolation strategies that are already defined.

The **set_isolation** command allows you to define default isolation strategies for input, output, or both kinds of ports of the power domain. Once defined, these default strategies cannot be redefined.

For example, if you first define an isolation strategy that applies to input ports, then you can later define another default isolation strategy that applies to both kinds of ports or just input ports.

WHAT NEXT

Define only one default isolation strategy for a given port type.

SEE ALSO

set_isolation(2)

UPF-061 (error) Isolation strategy %s does not exist or it does not belong to power domain %s.

DESCRIPTION

This error message occurs when using the **set_isolation_control** or **map_isolation_cell** command when specifying an isolation strategy that does not exist or that not belong to the power domain in -domain option.

The **set_isolation_control** command and **map_isolation_cell** command are effective only when you specify an isolation strategy that already exists in the given power domain.

WHAT NEXT

Look for typos in isolation strategy name. Make sure the isolation strategy was created using set_isolation command for the power domain specified in -domain option

SEE ALSO

set_isolation(2)

set_isolation_control(2)
map_isolation_cell

UPF-062 (information) Converting isolation signal %s to its driver pin %s.

DESCRIPTION

This information message occurs after specifying a net or hierarchical pin as the isolation signal with the **set_isolation_control** command. The tool then uses the driver pin of the net as the isolation signal.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

set_isolation_control(2)

UPF-063 (warning) set_isolation_control for isolation strategy %s is not defined. Skipping this strategy.

DESCRIPTION

This warning message occurs when the specified isolation strategy has not been defined with the **set_isolation_control** command. The strategy is skipped.

The **set_isolation_control** command specifies crucial parts of the isolation strategy. The tool cannot add isolation cells if **set_isolation_control** is not defined for an isolation strategy.

WHAT NEXT

Define **set_isolation_control** for the isolation strategy and rerun the command.

SEE ALSO

set_isolation_control(2)

UPF-064 (error) Error encountered while processing option %s

of create_power_switch command. No switch is created.

DESCRIPTION

This error message occurs when the tool detects an error during the processing of the specified option used in the **create_power_switch** command.

This error might be caused by incorrectly specified supply nets, signal nets, or Boolean functions.

WHAT NEXT

Check the syntax and make sure that all names are referenced with respect to the current scope.

SEE ALSO

create_power_switch(2)

UPF-065 (error) Hierarchical name %s cannot be directly specified for the object created by this command.

DESCRIPTION

This error message occurs when a hierarchical name is specified for the object created by this command.

Only simple names, without a slash (/), are permitted for the object created by this command. The created object automatically has its hierarchical name based on the scope instance in which it is created. For example, an object with the simple name of 'A' created in scope U1/U2/U3 (relative to the top) will have a hierarchical name of U1/U2/U3/A.

WHAT NEXT

Use a simple name for the object and rerun the command.

UPF-066 (error) In UPF mode (default for dc_shell), the -object_list option for set_operating_conditions is not allowed on

cells that are not macro nor pad.

DESCRIPTION

This error message occurs when attempting to use the **-object_list** option with the **set_operating_conditions** command in UPF mode. The **-object_list** option is deprecated for **set_operating_conditions** in UPF mode, except when the objects are macro or pad cells.

WHAT NEXT

Use the **set_voltage** command to constrain the design for multivoltage on power nets.

SEE ALSO

set_operating_conditions(2)
set_voltage(2)

UPF-067 (error) Supply net connection cannot be determined for power_pin %s on cell %s.

DESCRIPTION

This error message occurs when preexisting technology cells in the design have backup power or ground pins. These cells, including macro cells, retention cells, isolation cells, and dual-rail always-on cells, require proper UPF constraining so that their backup connections can be determined by the tool.

For macro cells, exception connections may be needed. For others, relevant **set_retention** and **set_isolation** commands are needed.

WHAT NEXT

Set up the design using the **connect_supply_net**, **set_retention**, and **set_isolation** commands.

"SEE ALSO

connect_supply_net(2)
set_isolation(2)
set_retention(2)

UPF-068 (error) Incorrect -hdl_type or -table specification in

create_hdl2upf_vct or create_upf2hdl_vct commands.

DESCRIPTION

This error message occurs when the tool encounters an illegal specification for the **-hdl_type** or **-table** option.

The **-hdl_type** option uses the following format:

```
-hdl_type { <vhdl | vlog | SV> [typename] }
```

The **-hdl_type** option supports the following case-sensitive values:

- vhdl
- verilog
- SV

The value conversion table included in the **-table** option cannot be empty.

WHAT NEXT

If the **-hdl_type** option was used, verify that you specified the correct format and value. If the **-table** option was used, verify that you specified a value conversion table that is not empty.

SEE ALSO

create_hdl2upf_vct(2)
create_up2hdl_vct(2)

UPF-069 (error) Incorrect syntax on retention %s control signal or its sense value.

DESCRIPTION

This error message occurs when attempting to run the UPF **set_retention_control** command using an incorrect syntax.

The **set_retention_control** command requires that you specify the control signal together with the control signal sense in the format of {*signal_net signal_sense*}.

The error message indicates that either *signal_net* or *signal_sense* was not specified, or an incorrect syntax was used for specifying the retention control signal and its sense value.

WHAT NEXT

Check the command syntax and ensure that it follows the syntax shown in the **set_retention_control** man page.

SEE ALSO

set_retention_control(2)

UPF-070 (error) %s isolation cell has a mismatch between the UPF pragma and UPF.

DESCRIPTION

This error message occurs when the UPF isolation strategy name stored on the cell does not match the UPF isolation name strategy for the power domain port that is being isolated by this cell.

During compile, the tool checks each isolation cell to ensure it is consistent with the **set_isolation** UPF command specified for the power domain port that connects to the isolation cell. A mismatch might occur if the UPF file is modified after compile or if changes are made to the UPF isolation pragmas or attributes on the isolation cells.

The pragmas are placed in the Verilog/VHDL output of the tool for internal tracking purposes.

WHAT NEXT

Change the pragma in the Verilog/VHDL file back to its original value if it has been modified since being written out by the tool.

SEE ALSO

set_isolation(2)

UPF-071 (error) %s isolation cell’s location is inconsistent with its UPF strategy %s.

DESCRIPTION

This error message occurs when the UPF isolation location stored on the cell does not match the actual location of the cell, either in the same design as where **set_isolation** is specified, or in the parent design.

During compile, the tool checks each isolation cell to ensure it is consistent with the **set_isolation** UPF command specified for the power domain port that connects to the isolation cell. A mismatch might occur if the UPF file is modified after compile or if changes are made to the UPF isolation pragmas or attributes on the isolation cells.

The pragmas are placed in the Verilog/VHDL output of the tool for internal tracking purposes.

WHAT NEXT

Change the pragma in the Verilog/VHDL file back to its original value, if it has been modified since being written out by the tool.

SEE ALSO

set_isolation(2)

UPF-072 (error) The %s isolation cell's clamp value is inconsistent with its UPF strategy %s.

DESCRIPTION

This error message occurs when the UPF isolation clamp value stored on the cell does not match the actual clamp value of this isolation cell.

During compile, the tool checks each isolation cell to ensure it is consistent with the **set_isolation** UPF command specified for the power domain port that connects to the isolation cell. A mismatch may occur if the UPF file is modified after compile or if changes are made to the UPF isolation pragmas or attributes on the isolation cells.

The pragmas are placed in the Verilog/VHDL output of the tool for internal tracking purposes.

WHAT NEXT

Change the pragma in the Verilog/VHDL file back to its original value if it has been modified since being written out by the tool.

SEE ALSO

set_isolation(2)

UPF-073 (information) Isolation strategy %s applied on isolation

cell %s.

DESCRIPTION

This information message advises you that the specified isolation strategy has been applied to an existing isolation cell and no new cell needs to be created.

If an isolation strategy is specified for a port that already has an isolation cell, the tool verifies that the existing isolation cell satisfies all of the parameters of the isolation strategy, except for power and ground nets. If these parameters are satisfied, the tool uses the existing cell and does not create another isolation cell for the port. The cell gets its isolation power and ground nets as specified in the isolation strategy.

WHAT NEXT

This is only an information message. No action is required.

UPF-074 (error) Cannot apply UPF retention strategy %s on existing retention cell %s because the lib_cell_type %s in this UPF retention strategy is different than the existing retention cell's lib_cell_type %s.

DESCRIPTION

This error message occurs when the specified retention strategy cannot be applied because the given *lib_cell_type* does not match the existing *lib_cell_type*.

If you run the **map_retention_cell** UPF command with the **-lib_cell_type** option on an existing retention cell in the netlist and specify a library type that does not match the retention type on the existing library cell, the command is ignored. The existing retention cell type takes priority.

WHAT NEXT

Check the **map_retention_cell** command man page for information about the **-lib_cell_type** option.

SEE ALSO

map_retention_cell(2)

UPF-075 (error) Cannot apply UPF retention strategy %s on

existing retention cell %s because there is a conflict between library cells that are specified in this UPF retention strategy and the library cell %s of the existing retention cell.

DESCRIPTION

This error message occurs when the UPF retention strategy cannot be applied because there is a conflict between the library cells specified in this retention strategy and the library cell of the existing retention cell.

If the UPF **map_retention_cell** command specifies an existing retention cell in the netlist and the **-lib_cells** option specifies a set of library cells that does not contain the library cell of the existing preinstantiated retention cell, the **map_retention_cell** command on the existing retention cell is ignored. The existing retention cell takes priority over this command.

WHAT NEXT

Check the **map_retention_cell** man page for the correct input.

SEE ALSO

map_retention_cell(2)

UPF-076 (error) Cannot find the real driver of isolation_signal %s.

DESCRIPTION

This error message occurs when the specified isolation signal is either driven by an unlinked cell or not driven by a real driver.

The **-isolation_signal** option of the **set_isolation_control** command requires that the signal the option specifies be driven by a real driver. Real drivers include output pins of leaf level cells and the top-level design ports. If a cell is unlinked, the tool cannot determine if the port of the cell driving an isolation signal is an output port.

"WHAT NEXT

Modify the **set_isolation_control** command so that it specifies an isolation signal that is being driven by a real driver, and fix any linking issues.

SEE ALSO

set_isolation_control(2)

UPF-077 (warning) Design has %d retention cells that cannot be hooked up based on the UPF retention constraints due to retention library issues.

DESCRIPTION

This warning message occurs when attempting to use a retention cell syntax that is no longer valid. Use the retention cell syntax provided in release 2007.03 or later.

In UPF mode, UPF retention control signals are save signals or restore signals that correspond to the retention save or retention restore pin in the retention library cell. This can only be modeled using the retention cell syntax introduced in the 2007.03 release. If you attempt to use a retention cell syntax from a release prior to 2007.03, the retention pins do not have any save or restore meaning. The tool cannot determine which retention pin is the save pin, which pin is the restore pin, and so cannot do the hookup using UPF retention constraints.

WHAT NEXT

If the result is not what you intended, you can do either of the following (although the first method is considered best practice):

• Update your .lib file to use the retention cell syntax from release 2007.03 or later and recompile your .lib file to get the library. This is the cleanest method.

• Use the **set_retention_control_pins** command to convert your library to a library that has the retention cell syntax from release 2007.03 or later.

SEE ALSO

set_retention_control_pins(2)

UPF-078 (error) Isolation cell voltage mismatch for For pin %s. Nominal voltage of Isolation power net (%s) is different from the nominal volatge of the primary power net (%s) of the power

domain where the isolation cell will be created.

DESCRIPTION

In UPF user specifies isolation intent using set_isolation and set_isolation_control command. DC requires that the nominal volatge of the power net specifed in the set_isolation command matches the nominal volatge of the primary power of the location specifed in the set_isolation command. This error will occur whenever these two volatges do not match. Note that both min and max values of tthe nominal volatges should match.

WHAT NEXT

Change the nominal volatges of the isolation power net or the primary power net of the location specified in set_isolation so that they match. Nominal voltages are specifed using set_voltage command.

UPF-079 (error) Nominal voltage of retention power net (%s) is different from the nominal volatge of the primary power net (%s) of the power domain (%s) where the retention cell will be created.

DESCRIPTION

If UPF user specifies retention intent using set_retention command, DC currently requires that the nominal volatge of the retention power net specifed in the set_retention command matches the nominal volatge of the primary power of the power domain where the retention cells will be created under this retention strategy. This error will occur whenever these two volatges do not match. Note that both min and max values of the nominal volatges should match.

WHAT NEXT

Change the nominal volatges of the retention power net or the primary power net of the power domain where the retention cells will be created under this retention strategy. Nominal voltages are specified using set_voltage command.

UPF-080 (error) Nominal voltage of retention ground net (%s) is different from the nominal voltage of the primary ground net (%s) of the power domain (%s) where the retention cell will be

created.

DESCRIPTION

This error message occurs when the nominal voltage of the specified ground net does not match the nominal voltage of the specified primary ground net.

The tool requires that the nominal voltage of the retention ground net specified in the **set_retention** command matches the nominal voltage of the primary ground net of the power domain where the retention cells will be created under this retention strategy.

WHAT NEXT

Change the nominal voltages of the retention ground net or the primary ground net of the power domain where the retention cells will be created based on this retention strategy. Specify nominal voltages using the **set_voltage** command.

SEE ALSO

set_retention(2)
set_voltage(2)

UPF-081 (warning) Retention strategy %s does not have an associated map_retention_cell constraint.

DESCRIPTION

This warning message occurs because the tool cannot map sequential cells under the specified retention strategy when the strategy does not have an associated **map_retention_cell** command.

In each UPF retention strategy, the associated **map_retention_cell** command specifies how the retention cell mapping will be done. If a retention strategy does not have an associated **map_retention_cell** command, the tool cannot map any sequential cells that are under this retention strategy to the retention cell.

WHAT NEXT

To map specific sequential cells under a retention strategy to a retention cell during compile, make sure that there is a corresponding **map_retention_cell** command associated with the retention strategy.

SEE ALSO

map_retention_cell(2)

UPF-082 (Error) The specified power switch %s has not been created for power domain %s.

DESCRIPTION

This error message occurs because you are refering to a power switch that either (1) has yet been created, or, (2) has been created, but not for the power domain.

WHAT NEXT

Use [get_power_switches <domain_scope>/<switch_name>] command to look for the power switch, to see if it exists at all.

Also make sure that the power switch was indeed defined for the power domain.

UPF-083 (error) The argument %s cannot be used with the argument %s.

DESCRIPTION

This error occurs if you have entered a combination of arguments that is invalid.

WHAT NEXT

Please refer to the man page of the command used to see the valid option of arguments.

UPF-084 (error) The power domain "%s" does not have any isolation strategies defined.

DESCRIPTION

This error occurs when the single power domain specified with the isolation strategies has no isolation strategies defined.

WHAT NEXT

Please make sure that there are isolation strategies defined for the given power domain and try again.

UPF-085 (error) The argument %s cannot be used without the argument %s.

DESCRIPTION

This error occurs if you have entered a combination of arguments that is invalid.

WHAT NEXT

Please refer to the man page of the command used to see the valid option of arguments.

UPF-086 (warning) Argument -applies_to to set_isolation is ignored because -elements arguments is also specified

DESCRIPTION

The -elements option to set_isolation command has priority over -applies_to option. This means that set_isolation will applies to all members of -elements argument regardless of the direction specified in -applies_to option. This is to keep set_isolation command in compliance with UPF specification.

WHAT NEXT

Please remove -applies_to option from this set_isolation command.

UPF-087 (error) Cannot set_voltage on an empty list of supply net(s).

DESCRIPTION

This error message occurs attempting to set voltage an empty list of supply nets, or the specified supply nets are invalid.

The cause could the invalid supply net name specified by user, or the design contains invalid supply net data.

WHAT NEXT

Check and make sure the specified supply nets exist.

UPF-088 (warning) set_isolation_control -location self is specified for non-hierarchical pin %s. No isolation will be inserted for this pin.

DESCRIPTION

set_isolation_control -location self is specified for a non-hierarchical pin, such as a pin on a macro cell. The tool will not be able to honor this strategy, since nothing can be inserted within a macro.

WHAT NEXT

Use -location parent for such a pin.

UPF-089 (error) set_retention_control has already been defined for strategy %s.

DESCRIPTION

The error occurs when applying **set_retention_control** to a retention strategy that already has control defined.

WHAT NEXT

Please make sure that there is only one **set_retention_control** for a retention strategy.

UPF-090 (error) Pin %s is not on boundary of domain %s.

DESCRIPTION

This error message occurs when attempting to specify a pin in -elements option of set_isolation or set_level_shifter command that is not on the power domain boundary for which the isolation or level shifter strategy is being defined.

WHAT NEXT

Look at the pin in the error message, verify that it is not a pin on the power domain boundary and change it to the one on the power domain boundary to which the isolation or level shifter strategy applies.

SEE ALSO

set_isolation(2)
set_level_shifter(2)

UPF-091 (warning) Unable to find a match for some of the library cells specified.

DESCRIPTION

This warning message occurs when the tool is unable to find a match for some of the library cells specified in the **-lib_cells** option of either the **map_isolation_cell** or the **map_level_shifter_cell** command in any of the technology libraries.

WHAT NEXT

This is only a warning message. No action is necessary.

However, if the result is not what you intended, verify that there are no typographical errors in the library cell names of the **-lib_cells** option.

Make sure you have specified just the cell_name of the library cell and not used the library_name/cell_name format.

For the **map_isolation_cell** command, make sure the library cell’s clamp value does not contradict the isolation strategy clamp value.

SEE ALSO

map_isolation_cell(2)
map_level_shifter_cell(2)

UPF-092 (error) Isolation strategy %s is defined with -no_isolation option

DESCRIPTION

This error message occurs when map_isolation_cell or set_isolation_control command is specified on an isolation strategy defined with -no_isolation option.

WHAT NEXT

Please verify that the isolation strategy on which map_isolation_cell or set_isolation_control is specified is not defined with -no_isolation option.

SEE ALSO

map_isolation_cell

UPF-093 (error) UPF commands are supported only with the compile_ultra command.

DESCRIPTION

This error message occurs when the **compile** command is issued on a design with UPF constraints. UPF is only supported by DC Ultra. Use the **compile_ultra** command instead.

WHAT NEXT

Verify if there are any UPF constraints on the design. You can check for UPF commands using either the **save_upf** *file_name* command or the **write_script** command. If the UPF constraints are intentional use **compile_ultra** to compile the design.

SEE ALSO

save_upf(2)
write_script(2)

UPF-094 (error) Level shifter strategy %s is not found

DESCRIPTION

This error message occurs when map_level_shifter_cell command is issued for a not existent level shifter strategy or the strategy does not belong to the power domain specified with -domain option

WHAT NEXT

Please verify that the level shifter strategy on which map_level_shifter_cell is being defined is present and it exists on the power domain specified with -domain optiion

SEE ALSO

set_level_shifter

UPF-095 (Warning) Supply net %s has an out of domain connection to cell %s in domain %s that is not consistent with UPF semantics.

DESCRIPTION

A supply net can only be connected to power pins that lie within the extent of the power domain(s) in which the supply net is defined.

WHAT NEXT

Ensure that the supply net is defined in the power domain to which the cell belongs. This can be done using **create_supply_net -reuse**. Fix the connection before reading this UPF into any tools.

SEE ALSO

create_supply_net(2)
connect_supply_net(2)

UPF-096 (error) UPF resolution type %s not supported on net %s.

DESCRIPTION

This error message occurs when the resolution type is valid according to the UPF definition but is not supported by the shell.

WHAT NEXT

This message applies to the **create_supply_net** command **-resolve** option, for which the shell currently only supports the **unresolved** and **parallel** values. The value of **one_hot** is not supported.

SEE ALSO

create_supply_net(2)

UPF-097 (error) Invalid UPF resolution type %s on net %s.

DESCRIPTION

This error message occurs when the resolution type does not comply with the IEEE 1801 (UPF) standard.

WHAT NEXT

This message applies to the **create_supply_net -resolve** option. The shell currently supports only the values of **unresolved and parallel** for this option.

SEE ALSO

create_supply_net(2)

UPF-098 (warning) Default resolution forced to %s for net %s.

DESCRIPTION

This warning message occurs when the **create_supply_net** command is specified with the **-reuse** option, but **-resolve parallel** is omitted on a supply net that supports multiple drivers.

WHAT NEXT

According to the IEEE 1801 (UPF) standard, the default resolution for a supply net is **unresolved** when the **-resolve** option is omitted. However, when a supply net is connected to multiple domains, the definition must be consistent across instantiations. If the first instantiation was of type **parallel** and **-resolve** is omitted for subsequent connections, the shell will enforce the consistency.

SEE ALSO

create_supply_net(2)

UPF-099 (error) Inconsistent resolution type on net %s.

DESCRIPTION

This error message occurs when the **create_supply_net** command with the **-reuse** option is specified and the **-resolve** option is inconsistent with the previous definition.

WHAT NEXT

According to the IEEE 1801 (UPF) standard, the definitions of resolution types may not be mixed on a single supply net.

SEE ALSO

create_supply_net(2)

UPF-100 (error) Multiple drivers on unresolved supply net %s.

DESCRIPTION

This error message occurs when multiple power sources are connected to a net specified as **unresolved** with the **create_supply_net** command **-resolvefp option.**

WHAT NEXT

Supply nets specified as **unresolved** may receive only 1 driver. Either disconnect other sources or specify the supply net as **parallel**.

SEE ALSO

create_supply_net(2)

UPF-101 (Error) Supply net %s cannot be connected to the cell %s in domain %s. This connection is not consistent with UPF semantics.

DESCRIPTION

A supply net can only be connected to power pins that lie within the extent of the power domain(s) in which the supply net is defined.

WHAT NEXT

Define the supply net in the power domain which contains the cell before its connection. This can be done using the **create_supply_net -reuse** command.

SEE ALSO

create_supply_net(2)
connect_supply_net(2)

UPF-102 (error) Supply net %s cannot be specified for retention strategy %s since it is not defined in the power domain %s.

DESCRIPTION

Using supply net(s) for a retention strategy, which are not defined in the domain of the strategy, is not consistent with UPF semantics.

WHAT NEXT

Ensure that the supply nets being used are defined in the power domain in which strategy is defined. This can be done using **create_supply_net -reuse**.

SEE ALSO

set_retention(2)
create_supply_net(2)

UPF-103 (error) Supply net %s cannot be specified for isolation strategy %s since it is not defined in the power domain %s in which the isolation cells will be inserted.

DESCRIPTION

Supply net(s) specified for an isolation strategy, must be available in the domain in which the isolation cells inserted by the strategy would lie, for the UPF design to be consistent with UPF semantics.

WHAT NEXT

Ensure that the supply nets being used are defined in the power domain(s) in which the isolation cells inserted by the strategy would lie. This can be done using **create_supply_net -reuse**.

SEE ALSO

set_isolation(2)
set_isolation_control(2)
create_supply_net(2)

UPF-104 (error) Supply net %s cannot be used as the %s net for

power switch %s as it is not defined in the power domain %s.

DESCRIPTION

Supply net(s) being used as input supply nets and output supply nets for a power switch, must be defined in the power domain in which the power switch is being created, for the UPF design to be consistent with UPF semantics.

WHAT NEXT

Ensure that the supply nets being specified as the input and output supply nets are defined in the power domain(s) in which the power switch is being created. This can be done using **create_supply_net -reuse**.

SEE ALSO

create_power_switch(2)
create_supply_net(2)

UPF-105 (error) Cannot apply UPF retention strategy %s on existing retention cell %s because there is a conflict between retention cell type '%s' that are specified in this UPF retention strategy and the library cell %s of the existing retention cell.

DESCRIPTION

This error message occurs when the UPF retention strategy cannot be applied because there is a conflict between the retention cell type specified in this retention strategy and the library cell of the existing retention cell.

If the UPF **map_retention_cell** command specifies an existing retention cell in the netlist and the **-lib_cell_type** option specifies a set of library cells that does not contain the library cell of the existing preinstantiated retention cell, the **map_retention_cell** command on the existing retention cell is ignored. The existing retention cell takes priority over this command.

WHAT NEXT

Check the **map_retention_cell** man page for the correct input.

SEE ALSO

map_retention_cell(2)

UPF-106 (warning) Supply net %s cannot be used for the isolation strategy %s since it is not defined in the power domain %s in which the isolation cells will be inserted.

DESCRIPTION

Supply net(s) specified for an isolation strategy, must be available in the domain in which the isolation cells inserted by the strategy would lie, for the UPF design to be consistent with UPF semantics.

WHAT NEXT

Ensure that the supply nets being used are defined in the power domain(s) in which the isolation cells inserted by the strategy would lie. This can be done using **create_supply_net -reuse**. Fix the issue before reading the UPF into any tool.

SEE ALSO

set_isolation(2)
set_isolation_control(2)
create_supply_net(2)

UPF-107 (error) Duplicate port name %s in instance %s

DESCRIPTION

Port names must be unique within and instance.

WHAT NEXT

Ensure that all ports of the instance have a unique name.

UPF-108 (error) Invalid boolean expression '%s' in argument %s.

DESCRIPTION

The expected boolean expression must comply with the SystemVerilog requirements.

WHAT NEXT

The boolean expression must be a combination of instance control port names and logical or bitwise operators (!, |, ||, &, &&, ^ and ==). SystemVerilog keywords are not acceptable port names.

UPF-109 (error) Invalid portname %s in -ack_delay option.

DESCRIPTION

The argument of -ack_delay must match a -ack_port option.

WHAT NEXT

Ensure the option -ack_delay has a -ack_port counterpart.

UPF-110 (error) Nonexistent input port '%s' in -on_state option.

DESCRIPTION

This error message occurs when the specified input port does not match the argument of the **-on_state** option. The argument of the **-on_state** option must match an **-input_supply_port** argument.

WHAT NEXT

Ensure that the argument of the **-on_state** option matches an **-input_supply_port** counterpart and run the command again.

UPF-111 (error) Invalid state name specification for instance %s.

DESCRIPTION

This error message occurs when the specified instance refers to an invalid state name specification. All arguments and options that rely on a state specification must refer to the same state, the actual operation being defined by the Boolean expression.

WHAT NEXT

Ensure that all arguments and options refer to the same state within an instance.

UPF-112 (error) Pin or port %s was already assigned the isolation strategy %s before %s.

DESCRIPTION

This error message occurs when a pin or port is listed in the elements list of one isolation strategy. You may not explicitly include the same pin or port in more than one isolation strategy.

WHAT NEXT

Ensure that all pins are assigned in only one isolation strategy.

SEE ALSO

set_isolation(2)

UPF-113 (warning) Inout %s, %s is ignored.

DESCRIPTION

This warning message appears if an inout Pin/Port is specified in the **-elements** option of the **set_isolation** or **set_level_shifter** command. You cannot specify an isolation or level shifter strategy on an inout Pin/Port.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid receiving this message, verify if the Pin/Port for which the warning appears is an inout pin. Since isolation and level shifter strategies cannot be specified on an inout Pin/Port, remove this from the list in the **-elements** option and run the command again.

SEE ALSO

set_isolation(2)
set_level_shifter(2)

UPF-114 (warning) Power switch %s does not have a match in the target libraries.

DESCRIPTION

This warning message occurs when the model names specified for the power switch do not match any entry in the target libraries.

WHAT NEXT

Check the available models in the target libraries and specify a valid name. At least one valid name must exist.

SEE ALSO

map_power_switch(2)

UPF-115 (warning) Library cell for instance %s is not a power switch.

DESCRIPTION

This warning message occurs when the library cell specified for the **map_power_switch** command does not appear to be a valid power switch. While the library cell specified is found in the target libraries, the function of the library cell does not match that of a power switch.

WHAT NEXT

Check the available library cells in the target libraries and specify a valid name. At least one valid name must exist in the list provided with the **map_power_switch** command.

SEE ALSO

map_power_switch(2)

UPF-116 (error) The set_retention command was invoked with

an empty list of elements for strategy %s.

DESCRIPTION

This error message occurs because the **set_retention** command takes an optional **-elements** argument that defines the pins and ports affected by the strategy. If this argument is specified, the list of elements must contain at least 1 valid port or pin.

WHAT NEXT

Check that the list of ports is not empty and contains existing ports or pins in the design, and run the command again.

SEE ALSO

set_retention(2)

UPF-119 (error) Cannot find supply pin %s in cell %s.

DESCRIPTION

This error message occurs when the **connect_supply_net** attempts to connect a specific supply pin of a given library cell to a supply net. In this case, the pin must exist in the interface.

WHAT NEXT

Check the interface of the library cell and correct the pin name.

SEE ALSO

connect_supply_net(2)

UPF-120 (error) The specified net control or ack net ’%s’ cannot be found.

DESCRIPTION

This error message occurs when the specified control or ack net for a UPF power switch does not exist.

WHAT NEXT

Check that the name is correct and run the command again.

SEE ALSO

create_power_switch(2)

UPF-121 (information) A total of %d power switches found that are not mapped to a valid library cell; %d of them have been reported.

DESCRIPTION

This information message provides a a summary of the total number of power switches that are not mapped to an existing library cell, or are mapped to a library cell other than a power switch.

WHAT NEXT

All of these violations can be viewed using the **check_mv_design -max_messages** command. Use a larger value with **-max_messages** if you are already seeing this message with the **check_mv_design** command.

SEE ALSO

check_mv_design(2)
map_power_switch(2)

UPF-122 (information) Selecting supply net %s for isolation strategy %s:%s in scope %s for characterization.

DESCRIPTION

This information message occurs when the supply net specified for the isolation strategy is not available in the hierarchy that is being characterized. A supply net connected to the specified supply net in the instance being characterized is used.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

characterize(2)

UPF-123 (error) Unable to find a supply net connected to the supply net %s, in the scope %s.

DESCRIPTION

This error message occurs when the **propagate_constraints** command cannot find a supply net in the scope that is connected to the supply net specified for the isolation strategy with the location defined as the parent in the scope of the characterized instance.

WHAT NEXT

Connect the supply nets at the scope in which the isolation cells will be inserted to supply nets associated with the isolation strategy through supply ports.

Compiling the design without correcting the connections will generate a **UPF-103** error message.

SEE ALSO

connect_supply_net(2)
create_supply_net(2)
create_supply_port(2)
UPF-103(n)

UPF-124 (error) Control signal specified for strategy %s not supported because %s.

DESCRIPTION

This error message occurs when the control signal specified for the isolation or retention strategy is invalid.

WHAT NEXT

Determine the reason for the control signal rejection and correct the isolation or retention control signal. After making your changes, run the command again.

SEE ALSO

set_isolation_control(2)
set_retention_control(2)

UPF-125 (warning) Cell %s, previously an isolation cell, is now being treated as a normal cell.

DESCRIPTION

This warning message occurs when a cell with the attributes of an isolation cell is linked to a normal cell. The tool removes the isolation cell attributes and treats the cell as a normal cell.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, you can make sure the libraries have not changed. If standard cells are used as isolation cells, remember to set the **ok_for_isolation** and **isolation_cell_enable_pin** attributes again, if the libraries are reloaded. These attributes are not written to the libraries.

UPF-126 (warning) Library cell %s not found and is ignored.

DESCRIPTION

This warning message occurs when the specified library cell cannot be found.

WHAT NEXT

This only a warning message. No action is required.

However, if the result is not what you intended, check that the specified library cell exists.

UPF-127 (error) Invalid direction '%s' is specified.

DESCRIPTION

This error message occurs when an invalid direction string is specified for the **create_supply_port** command. The tool only supports the **-direction** option values of

in or **out**.

WHAT NEXT

Run the **create_supply_port** command again, with the direction specified as either **-direction in** or **-direction out**.

SEE ALSO

create_supply_port(2)

UPF-128 (warning) Retention cell %s has only a single save-restore pin %s, but its retentions strategy %s specifies two distinct save and restore signals. Only the save signal will be used for this cell.

DESCRIPTION

A retention cell with a single pin for both save and restore functionality is used for a retention strategy that has both a save and a restore signal (different from the save signal) specified. The hook-up of the retention cell will be to the save signal.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, check whether the **set_retention_control** and **map_retention_cell** commands used for the strategy really reflect your intentions. For example, check whether you accidentally specified 2 different control signals or chose the wrong retention cell type for the strategy.

SEE ALSO

map_retention_cell(2)
set_retention_control(2)

UPF-130 (warning) Cannot apply UPF retention strategy %s on existing retention cell %s because there is a conflict between the

cell’s save/restore hook-up and the strategy’s specification.

DESCRIPTION

This error message occurs when the UPF retention strategy cannot be applied because there is a conflict between the cell’s save/restore hook-up and the strategy’s specification. For example, the save and restore connections could be swapped or have the wrong polarity.

If the UPF **set_retention_control** command specifies save and restore signals that do not match the connection to the existing retention cell to which the strategy is to be applied, the existing cell is assumed not to belong to the strategy.

WHAT NEXT

Check the **set_retention_control** command for the correct **-restore_signal** and **-save_signal** options or check the cell’s save and restore pin connections.

SEE ALSO

set_retention_control(2)

UPF-131 (error) Only pad cells or macros were found in domain %s; set_isolation_control may not use location "self".

DESCRIPTION

This error message occurs because the isolation control of a power domain may not be defined with the location "self" if the domain contains only pad cells or macros.

WHAT NEXT

Define the location as "parent" or add relevant hierarchical modules to the power domain and run the command again.

SEE ALSO

set_isolation_control(2)

UPF-132 (warning) Pad cells or macros were found in domain

%s with location ’self’.

DESCRIPTION

This warning message occurs because pad cells and macros are not hierarchical and, therefore, cannot use location "self" in **set_isolation_control**. The location "parent" will be assumed for these cells.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this warning, define the location as "parent".

SEE ALSO

set_isolation_control(2)

UPF-133 (warning) Power switch %s in domain %s cannot be created because the domain contains only pads.

DESCRIPTION

This warning message occurs when attempting to apply a power switch on a domain that contains only pad cells. Pad cells are passive and are not affected by power switches. Therefore, applying a power switch to a domain that contains only pads has no effect. The switch will not be created.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this warning message, define a power switch in a domain that does not contain only pad cells.

SEE ALSO

create_power_switch

UPF-134 (error) Retentions cannot be applied to pads in domain

%s.

DESCRIPTION

This error message occurs when attempting to set a retention strategy on a domain that contains only pad cells. Pad cells are passive and do not support retention.

WHAT NEXT

Set the retention strategy only on a domain that does not contain only pad cells.

SEE ALSO

set_retention(2)

UPF-135 (error) Only pad cells or macros were found in domain %s; set_level_shifter may not use the location "self".

DESCRIPTION

This error message occurs because the level shifter strategy of a power domain may not be defined with the location "self" if the domain contains only pad cells or macros.

WHAT NEXT

Define the location as "parent" or add relevant hierarchical modules to the power domain.

SEE ALSO

set_level_shifter(2)

UPF-136 (information) A total of %d isolation strategies were applied to power domains that include pad cells as root cells, on which the strategy cannot be applied; %d of them have been

reported.

DESCRIPTION

This information message provides a summary of the total number of isolation strategies that may be ignored.

WHAT NEXT

This is informational message only. No action is required.

All of these violations can be viewed using the **check_mv_design -max_messages** command. Use a larger value with the **-max_messages** option if you are already seeing this message with the **check_mv_design** command.

SEE ALSO

check_mv_design(2)
set_isolation(2)
set_isolation_control(2)

UPF-137 (information) A total of %d retention strategies were defined for pad cells, on which the strategy cannot be applied; %d of them have been reported.

DESCRIPTION

This information message provides a summary of the total number of retention strategies that may be ignored.

WHAT NEXT

This is an information-only message. No action is required.

However, all of these violations can be viewed using the **check_mv_design -max_messages** command. Use a larger value with the **-max_messages** option if you are already seeing this message with the **check_mv_design** command.

SEE ALSO

check_mv_design(2)
set_retention(2)

UPF-138 (information) A total of %d power switches were created in domains composed only of pad cells as root cells; %d of them have been reported.

DESCRIPTION

This information message provides a summary of the total number of power switches that may be ignored.

WHAT NEXT

This an information-only message. No action is required.

However, all of these violations can be viewed using the **check_mv_design -max_messages** command. Use a larger value with the **-max_messages** if you are already seeing this message with the **check_mv_design** command.

SEE ALSO

check_mv_design(2)
create_power_switch(2)

UPF-139 (information) A total of %d level-shifter strategies were applied to pad cells; %d of them have been reported.

DESCRIPTION

This information message provides a summary of the total number of level-shifters strategies that may be ignored.

WHAT NEXT

This is an information-only message. No action is required.

However, all of these violations can be viewed using the **check_mv_design -max_messages** command. Use a larger value with the **-max_messages** option if you are already seeing this message with the **check_mv_design** command.

SEE ALSO

check_mv_design(2)
set_level_shifter(2)
set_level_shifter_strategy(2)

UPF-140 (warning) Removed isolation strategy %s as its signal/ element is removed.

DESCRIPTION

This warning message occurs because when objects used as reference for a UPF control signal are removed, the related UPF constraint is also removed. Design objects like ports and pins can be removed by direct commands such as **remove_design**.

WHAT NEXT

This is only a warning message. No action is required.

However, to avoid this warning message, apply UPF constraints after all design manipulations, so the design object can be found when loading the UPF constraints.

SEE ALSO

remove_design(2)
set_isolation(2)

UPF-141 (warning) Always on inverter characterized for "%s" operating condition was marked dont_use or it is not defined in target library.

DESCRIPTION

The target library does not contain an always on inverter which optimization tool can use on isolation control signal line, or the retention control signal line.

During isolation insertion or retention hookup, always on inverter may be needed based on the signal control sense value and the library cell control pin’s sense/ disable value. For example, if retention library cell save pin’s disable value is 0, but the retention control signal sense is specified as "low or 0", then an inverter will be inserted between the retention save control signal and the retention save pin. This inverter might need to be always on inverter based on the supply net relationship. If always on inverter does not exist, this inverter will lead to always on warning MV-076 later after compile.

WHAT NEXT

Add always on buffer to the target library. If always on buffer exists, then make sure it is not marked with dont_use attribute.

UPF-142 (error) Power and ground net or -clamp_value cannot be specified by the %s strategy with -no_isolation.

DESCRIPTION

This error message occurs when attempting to specify isolation power, isolation ground, or **-clamp_value** for an isolation strategy with the **-no_isolation** option.

WHAT NEXT

If you want to have isolation cells inserted, remove **-no_isolation**. If no isolation is intended, remove the power and ground net or the **-clamp_value** specification.

SEE ALSO

set_isolation(2)

UPF-143 (warning) Power domain %s contains pad cells or macros, which cannot be assigned a level shifter strategy with location "self".

DESCRIPTION

This warning message occurs because pad cells and macros will be defined as location "parent".

WHAT NEXT

Define the location as "parent" to avoid this message.

SEE ALSO

set_level_shifter(2)

UPF-200 (error) Symbol ’%s’ violates the UPF naming conventions.

DESCRIPTION

This error message occurs when an argument violates the identifier naming

conventions of UPF.

WHAT NEXT

Identifiers used with UPF constructs must start with a letter. All other characters of the idetifier must be either an alphanumeric character, "A-Z a-z 0-9", or the underscore character, "_". UPF names are case sensitive.

UPF-300 (error) Cannot apply UPF map_retention_cell -elements on retention strategy %s because map_retention_cell is already defined on this strategy.

DESCRIPTION

This error message occurs when map_retention_cell -elements is issued, while another map_retention_cell is already defined for this retention strategy.

WHAT NEXT

Check the **map_retention_cell** constraint. If -elements has to be used for map_retention_cell, then you better split the retention strategy to two retention strategies.

SEE ALSO

map_retention_cell(2)

UPF-500 (warning) Power or ground net creation is skipped for supply net %s because it is not connected to any power domain or domain element.

DESCRIPTION

This warning message occurs when the tool cannot create a power or ground net because the specified supply net is not connected to a power domain or domain element. The tool cannot determine if the net being created will be used as a power net or a ground net.

A supply net and its connected supply nets should be used for one of the following connections:

- Primary power or ground net of power domain(s)

- Explicit connections on power or ground pins of cell(s)
- Isolation power or ground supply
- Retention power or ground supply

WHAT NEXT

Check the UPF constraints and make sure the supply net or its connected supply nets are connected to a domain or domain element.

SEE ALSO

check_mv_design(2)
derive_pg_connection(2)

UPF-501 (error) Failed to get matching power or ground net for supply net %s.

DESCRIPTION

This error message occurs when the specified supply net does not have a matching power or ground net.

The specified supply net belongs to a supply net group, which includes all connected supply nets. All nets in a supply net group must have the same power or ground net. The matching power or ground net has the same name as the supply net within the highest logic hierarchy among all nets in the supply net group.

WHAT NEXT

Use the **derive_pg_connection -create_net** command to create power or ground nets if they are missing. Ensure that all supply nets and ports are properly defined and connected.

SEE ALSO

check_mv_design(2)
derive_pg_connection(2)

UPF-502 (warning) Supply net %s is not connected to any

domain element.

DESCRIPTION

This warning message occurs when the specified supply net is not connected to a power domain or domain element. The tool cannot determine if the supply net will be used as a power net or a ground net.

A supply net and its connected supply nets should be used for one of the following connections:

- Primary power or ground net of power domain(s)
- Explicit connections on power or ground pins of cell(s)
- Isolation power or ground supply
- Retention power or ground supply

WHAT NEXT

Check the UPF constraints and make sure the supply net or its connected supply nets are connected to a domain or domain elements.

SEE ALSO

check_mv_design(2)
derive_pg_connection(2)

UPF-503 (error) Supply net %s is connected to power or ground pin %s outside the net's domain scope.

DESCRIPTION

This error message occurs when an explicit connection is made between the power or ground pin in one domain scope and the supply net in another domain scope.

WHAT NEXT

Make the supply net available to the domain of the power or ground pin. If the pin's domain and the supply net's domain share the same hierarchical scope, introduce the supply net to the pin's domain using the **create_supply_net -reuse** command. Otherwise, create additional supply ports and supply nets and connect them to the supply net to make it available to the pin's domain.

SEE ALSO

check_mv_design(2)
connect_supply_net(2)
create_supply_net(2)
create_supply_port(2)

UPF-504 (error) Top-level power states %s is not fully included in the power state table of scope %s.

DESCRIPTION

This error message occurs when a power state defined at the top-level is not included in the power state table of a lower-level scope.

WHAT NEXT

Add the top-level power state to the power state table of the lower-level scope.

SEE ALSO

check_mv_design(2)

UPF-505 (warning) Power state '%s' in scope '%s' is ignored or partially ignored by implementation.

DESCRIPTION

This error message occurs when a power state defined in a lower-level scope is not included by the top-level power state table and therefore is ignored by implementation.

WHAT NEXT

Please investigate if the power state tables are defined as intended.

SEE ALSO

check_mv_design(2)

UPF-506 (warning) No port state has been defined on any

supply port connected to supply net %s.

DESCRIPTION

This error message occurs when there is no port state defined on any supply port that is connected to the supply net.

Level shifter violations appear between two signal pins if one of them is powered by a supply power with port states and the other one without.

WHAT NEXT

Please check the connectivity of supply net with port, or add appropriate port states to supply port connected to the supply net.

SEE ALSO

check_mv_design(2)

UPF-507 (Error) Supply %s must belong to the scope of PST.

DESCRIPTION

This error message occurs when the supply list contains certain objects with scopes not belonging to the scope of the PST to be created.

WHAT NEXT

Use supply objects within the scope of the PST in the supply list.

SEE ALSO

create_pst(2)

UPF-508 (warning) Skipping the following %d netgroups since they do not have valid states:%s.

DESCRIPTION

This error message occurs when there is no port state defined on any supply port that is connected to the supply net. Nets of the netgroups that do not have any state can not have any PST entries. Without a PST entry, features such as LS inserter are unable to process the nets.

WHAT NEXT

Please check the connectivity of supply net with port, or add appropriate port states to supply port connected to the supply net.

SEE ALSO

UPF-506
add_pst_state
connect_supply_net

UPF-509 (warning) The netgroups in the following scenarios do not have a corresponding PST entry:%s.

DESCRIPTION

This error message occurs when voltages have been assigned to a netgroup without creating a corresponding PST entry. Without a PST entry, features such as LS inserter are unable to insert all the required level-shifters.

WHAT NEXT

Create a PST, if one is not there already and add a state to it corresponding to the missing values.

SEE ALSO

create_pst
add_pst_state

UPF-510 (warning) Non-existing supply '%s' is ignored in PST '%s'.

DESCRIPTION

This warning message occurs when a supply in PST is found non-existing in the design. The corresponding column of the supply in the PST is ignored. This could be caused by removing a sub-design that contains a supply used in a higher-level PST.

WHAT NEXT

Reload the sub-design with UPF and the corresponding column of the supply in the PST will be used again.

SEE ALSO

`create_pst`
`add_pst_state`

VAL-1 (error) Parsing error in the association list '%s'.

DESCRIPTION

The association list is a sequence of comma separated clauses where each clause has the form: parameter => value For example: a=>123, b => "this is a string", c=>enum_literal is a valid association list. Only named associations are supported; positional associations are not supported.

WHAT NEXT

Check that your association list is in the right format including all associations having a parameter name and a parameter value.

VAL-2 (warning) The value '%s' from parameter '%s' is being omitted.

DESCRIPTION

Legal parameter values for design names are integers, strings, and enumeration literals. Integers are <digits> or verilog format 'd<digits> or <width>'h<hex number>. Strings are "<string>" or verilog format 's<string>. Enumerations are <enumeration_literal>; character literals for enumerations are not included in the design name.

WHAT NEXT

Re-enter your parameter/generic value. Avoid this warning by putting the parameter/generic in the generics_not_in_name attribute in the VHDL source.

VAL-3 (warning) The parameter/generic value '%s' in design '%s' exceeds the threshold length %d. Excluding the parameter from the design name.

DESCRIPTION

This message indicates that the specified parameter value is longer than the maximum length specified in the **dc_shell** environment variable **hdl_naming_threshold**. The

parameter value is excluded from the design name.

WHAT NEXT

To prevent this warning from appearing, change the value of the **hdl_naming_threshold** variable to increase the threshold; or, specify that this parameter is not to be used in the design name by adding the parameter to the VHDL attribute **generics_not_in_name**.

VAL-4 (error) Internal parameter parser error, unrecognized token "%s".

DESCRIPTION

This is an internal error caused by something in your parameter specification that the parser doesn’t recognize.

WHAT NEXT

Examine your parameter specification closely for correct syntax. Please file a Star and include this testcase.

VAL-5 (error) Array members must be of the same type. %s

DESCRIPTION

The elements of a VHDL array must be of the same type. In your parameter specification string, you have included an aggregate with members that are of different types.

WHAT NEXT

Examine your parameter specification string closely to see if there is an aggregrate with incompatible member types and correct the problem. Examples include: -p # p1 => (’1’, 2, ’3’) # -p # p2 => ("a", ’b’, "c") #

VAL-6 (error) Illegal value for aggregrate member "%s".

DESCRIPTION

Your parameter specification includes a VHDL aggregrate. One of the elements of this aggregate is not recognized as a legal value. The only supported types are: integer character string array

WHAT NEXT

Examine your parameter specification string closely to see if one of the elements of an aggregrate has a typo.

VAL-7 (error) Aggregrate elements must be separated by commas:
%s

DESCRIPTION

You have included a VHDL aggregrate in your parameter specification string. Elements of an aggregrate must be delimited by commas, some other character was found.

WHAT NEXT

VAL-8 (error) Arrays can only be concatenated with arrays:
%s

DESCRIPTION

Your parameter specification includes a VHDL aggregrate, followed by a ’&’ followed by something that is not an aggregrate. This not a supported syntax for parameter specifications.

WHAT NEXT

Examine your parameter specification to see if there is a typo. in one of your parameter values.

VAL-9 (error) Strings can only be concatenated with strings:

%s

DESCRIPTION

Your parameter specification includes a VHDL concatenation operator, ’&’. The values being concatenated must both be strings.

WHAT NEXT

VAL-10 (error) Parameter name must be followed by a legal value:
%s

DESCRIPTION

Your parameter specification included a value that could not be recognized. Only integer, string, character, and array type values are supported.

WHAT NEXT

VAL-11 (error) Illegal parameter name "%s".

DESCRIPTION

Your parameter specification contains a parameter name that contains illegal characters. Parameter names can only contain [a-z0-9_].

WHAT NEXT

VAL-12 (error) Unexpected end of parameter specification:
%s

DESCRIPTION

Your parameter specification includes a parameter name with no corresponding value.

WHAT NEXT

VAL-13 (error) "%s" is not a valid parameter value.

DESCRIPTION

Your parameter specification includes a parameter value that is not recognized. The only supported types of parameter values are integer, character, string and array.

WHAT NEXT

VAL-14 (error) Parameter specifications must be separated by commas:
%s

DESCRIPTION

Commas are required to separate individual parameter specifications.

WHAT NEXT

VAL-15 (error) Negative integers with radix not supported: "%s".

DESCRIPTION

Verilog supports specifying the width and radix of integer constants. These values can also be negative. This syntax is not supported for parameter specification strings.

WHAT NEXT

Specify the value as a negative integer like "-24" or invert the value manually and specify it as an unsigned value.

VAL-16 (error) This form of Verilog integer syntax not supported:

"%s".

DESCRIPTION

Only a limited subset of the Verilog integer syntax is supported. An integer width must be specified and the only radix allowed is hexadecimal.

EXAMPLES

```
'h23    // not supported
8'hAF   // supported
-8'h3   // not supported
3'o3    // not supported
-3      // supported
```

WHAT NEXT

If you need to specify the width of a value, use radix hexadecimal.

VAL-17 (error) Parameter value, '%s', must have 32 bits or fewer.

DESCRIPTION

EXAMPLES

WHAT NEXT

Either the width or the value must be changed to be less than or equal to a 32 bit number.

VE-0 (error) %s

DESCRIPTION

A syntax or internal error has surfaced during verilog parsing. The message specifies where the error appeared and why it was issued.

WHAT NEXT

Internal errors indicate a problem which should be reported to your Synopsys representitive.

VE-1 (error) Unable to open file ’%s’

DESCRIPTION

The specified file cannot be opened, which is most likely caused by the file being outside the search_path. This error is also triggered if the file permissions prohibit read access.

WHAT NEXT

If the file exists in the current directory, ensure "." is present in the search_path.

For files in other directories, add the directory to your search_path.

Permissions problems can be ruled out by trying to view the file in an editor. Errors of this variety are not specific to Verilog.

VE-2 (warning) Unsized number %s is too big. It will be

truncated to 32 bits %s

DESCRIPTION

WHAT NEXT

VE-3 (error) Undefined variable ’%s’ used %s

DESCRIPTION

WHAT NEXT

VE-4 (error) Variable ’%s’ defined more than once %s

DESCRIPTION

WHAT NEXT

VE-5 (error) Cannot assign to constant ’%s’ %s

DESCRIPTION

WHAT NEXT

VE-6 (error) Illegal assignment to reg ’%s’ %s

DESCRIPTION

WHAT NEXT

VE-7 (error) Illegal assignment to wire ’%s’ %s.

DESCRIPTION

Only continuous assignment is allowed for wire types. Most likely, a wire type was assigned inside an always block.

WHAT NEXT

The assignment to a wire type should be moved outside the always block, or the assignment's target should be changed to a register type.

EXAMPLE

The following example will trigger error VE-7:

```
wire  tmp;

always @(inp)
begin
  tmp = inp;

  ...
end
```

If continuous assignment is desired, move the assignment outside the always block.

```
wire  tmp;

assign tmp = inp;

always @(inp)
begin

  ...
end
```

If the assignment inside an always block is appropriate, the target of the assignment should be changed into a register type.

```
reg  tmp;

always @(inp)
begin
  tmp = inp;

  ...
end
```

VE-8 (error) Module/Function name '%s' defined more than

once
%s

DESCRIPTION

WHAT NEXT

VE-9 (error) Component '%s' instantiated more than once %s

DESCRIPTION

WHAT NEXT

VE-10 (error) Ambiguous direction declaration for port '%s' %s

DESCRIPTION

The same port has been declared with differing directions.

WHAT NEXT

If the port needs to be used as both input and output, declare the port to be of type "inout".

EXAMPLE

The declarations below seek to declare 'result' as both input and output:

```
input [3:0] result; output [3:0] result;
```

To resolve the conflict, declare the port as inout:

```
inout [3:0] result;
```

The port will allow input and output operations, and the VE-10 error message will no longer be triggered.

VE-11 (error) Port ’%s’ defined more than once %s

DESCRIPTION

WHAT NEXT

VE-12 (error) Port ’%s’ used before being assigned a direction %s

DESCRIPTION

WHAT NEXT

VE-13 (error) Port ’%s’ not defined in module terminal list but defined
in an input/output/inout statement %s

DESCRIPTION

WHAT NEXT

VE-14 (error) Port ’%s’ has no defined direction (input/output/inout)
%s

DESCRIPTION

WHAT NEXT

VE-15 (error) Attempt to disable block/function ’%s’ which is not active

%s

DESCRIPTION

WHAT NEXT

VE-17 (error) Continuous Assignment made to reg ’%s’ %s.

DESCRIPTION

WHAT NEXT

VE-18 (warning) Wand and Wor declarations treated as Wire declaration

%s

DESCRIPTION

WHAT NEXT

VE-19 (error) Initial statement not supported %s

DESCRIPTION

WHAT NEXT

VE-20 (error) Task statement not supported %s

DESCRIPTION

WHAT NEXT

VE-21 (error) Depending on edge and non-edge expression not supported %s.

DESCRIPTION

The sensitivity list contains both level-sensitive and edge-sensitive registers. Edge-sensitive registers are indicated by the use of either posedge or negedge in the sensitivity list.

All registers in an always block must either be edge-sensitive or level-sensitive.

WHAT NEXT

A mix of level- and edge-sensitive registers requires separate always blocks. Move the level-sensitive registers into their own always block.

VE-22 (error) Depending on 2 edges of same variable ’%s’ not

supported
%s

DESCRIPTION

WHAT NEXT

VE-23 (error) All asynchronous conditions must be tested in an "if" statement

%s

DESCRIPTION

WHAT NEXT

VE-24 (error) You must specify an "else" clause for the clocked logic

%s

DESCRIPTION

WHAT NEXT

VE-25 (error) Can’t test variable ’%s’ because it wasn’t in the event expression

%s

DESCRIPTION

This error occurs if a reg or wire that is not specified in the timing control of an ’always’ block is tested inside an ’if’ statement in the always block. In the example below, reset2 is tested in the ’if’ statement but does not occur in the timing block (reset1 appear instead).

EXAMPLES

```
module err (d, reset1, reset2, clk, q);
input d, clk;
input reset1, reset2;
output q;


always @ (posedge clk or negedge reset1)
   if (! reset2 )
     q = d;
end

endmodule
```

WHAT NEXT

Introduce the offending reg or wire in the timing control of the ’always’ block.

VE-26 (error) Testing wrong polarity of variable ’%s’ %s

DESCRIPTION

WHAT NEXT

VE-27 (error) Delay/Event control not allowed in continuous assignment statement

%s

DESCRIPTION

WHAT NEXT

VE-28 (error) Resource ’%s’ defined more than once %s

DESCRIPTION

WHAT NEXT

VE-29 (error) Resource ’%s’ not defined %s

DESCRIPTION

WHAT NEXT

VE-30 (error) Expected semicolon (;) at end of statement %s

DESCRIPTION

WHAT NEXT

VE-31 (warning) Resource declaration legal only in functions and blocks

%s

DESCRIPTION

WHAT NEXT

VE-32 (warning) Attributes for resources can be assigned only in functions
and blocks %s

DESCRIPTION

WHAT NEXT

VE-33 (warning) Directive ’%s’ must be scoped inside a function %s

DESCRIPTION

WHAT NEXT

VE-34 (warning) Illegal directive ’%s’ ignored %s

DESCRIPTION

WHAT NEXT

VE-35 (warning) Directive ’%s’ must be scoped inside a module

%s

DESCRIPTION

WHAT NEXT

VE-36 (warning) Directive ’%s’ declared more than once %s

DESCRIPTION

WHAT NEXT

VE-37 (error) Unknown enumerated type ’%s’ %s

DESCRIPTION

WHAT NEXT

VE-38 (error) Declaration of enumeration type requires range specification

%s

DESCRIPTION

WHAT NEXT

VE-39 (error) Enumerated type ’%s’ declared more than once

%s

DESCRIPTION

WHAT NEXT

VE-40 (warning) Value assignment to parameters of instantiated modules is not supported. It is ignored %s

DESCRIPTION

WHAT NEXT

VE-41 (warning) Port number %d of module '%s' was renamed to '%s'.

DESCRIPTION

Typically this warning occurs when unusual characters are used to form a port name. The use of brackets in a port name is an example of when this warning can be triggered. HDL Compiler renames the original port so that it can process the design.

WHAT NEXT

For port names containing brackets, change the name so it no longer uses brackets.

VE-42 (warning) TIME declarations are not supported %s

DESCRIPTION

WHAT NEXT

VE-43 (warning) EVENT declarations are not supported %s

DESCRIPTION

WHAT NEXT

VE-44 (warning) DEFPARAM is not supported %s

DESCRIPTION

WHAT NEXT

VE-45 (error) Resource declarations are not allowed in unnamed blocks
%s

DESCRIPTION

WHAT NEXT

VE-46 (error) Attribute declarations are not allowed in unnamed blocks

%s

DESCRIPTION

WHAT NEXT

VE-47 (warning) Width specified for number %s is too small. Higher order bits will be truncated %s

DESCRIPTION

WHAT NEXT

VE-48 (error) Incorrect number of terminals for bufif/notif %s

DESCRIPTION

WHAT NEXT

VE-49 (error) Expected identifier to label resource %s

DESCRIPTION

WHAT NEXT

VE-50 (error) End of file seen before %s block begun at line %d was ended

DESCRIPTION

A comment, directive or dc_script crossed the end of file boundry, indicating it wasn't terminated appropriately. This problem likely involves an unbalanced "/*", which will need a terminating "*/".

WHAT NEXT

For run-on comments or dc_script_begin, examine the lines immediately after the one specified in the error. Mark the boundry between code and comment with a terminating "*/".

For (preprocessor) directives, its very likely an ‘ifdef or ‘else was not completed with an ‘endif. Determine what code should fit within the ‘ifdef, and end it with an ‘endif.

VE-51 (error) Illegal use of array of register ’%s’ %s

DESCRIPTION

WHAT NEXT

VE-52 (error) ’include’ directive requires a filename enclosed in double quotes
%s

DESCRIPTION

A missing or misformed include filename can trigger this error. Here is an example usage of ‘include:

```
‘include "myfile.v"
```

WHAT NEXT

Provide the filename, if missing.

Preface the filename with a double-quote ("), and place another double-quote after the last character in the filename.

VE-53 (error) Recursive file inclusion detected for file "%s"

DESCRIPTION

A circular dependency was found in the use of an ‘include directive. This error is issued to prevent a file from including itself in an endless loop. Breaking the need for an ‘include loop will avoid triggering this error.

A file that directly includes itself most likely meant to include another file with a similiar name.

WHAT NEXT

Examine the need for the nested `include. Most likely, several files all depend on each other. The dependencies should be split up so that one file does not depend on any of the others. This can be achieved by moving needed code or `defines to one central file. When one file no longer depends on the others, the corresponding `include(s) can be removed from that file. This should break the `include loop and avoid the VE-53 error.

VE-54 (error) RTL assignments are allowed only when no blocking delays are used
%s

DESCRIPTION

This error occurs when RTL assignments and blocking delays are specified in the same module. RTL assignments are assignments made using the "<=" operator. Blocking delays are delays specified using the "#" construct (as in foo = #5 bar; or as in #7 foo = bar;).

WHAT NEXT

If you need to use RTL assignments, remove the blocking delays from your description. (Delays are ignored by the synthesis tool.)

VE-55 (error) Blocking delays are allowed only when no RTL assignments are used
%s

DESCRIPTION

WHAT NEXT

VE-56 (error) RTL assignments are not allowed for wires

%s

DESCRIPTION

WHAT NEXT

VE-57 (error) A reg can only be assigned with all RTL assignments or all procedural assignments %s.

DESCRIPTION

The two different methods of assignment are incompatible. Procedural assignments provide access to assigned values in the current clock cycle. A value passed along from variable A to variable B to variable C through a procedural assignment winds up with all three having the same value in every clock cycle. In the netlist, procedural assignments are indicated when the input net of one flip-flop is also connected to the input net of another. Both flip-flops will input the same value in the same clock cycle.

Values generated by RTL assignment are passed on in the next clock cycle. An assignment from variable A to variable B takes place after one clock cycle, provided that variable A has previously been the target of an RTL assignment. An assignment from variable B to variable C will always take place after one clock cycle, since B was the target of an RTL assignment of variable A’s value. Variable A will transmit its current value to variable C in two clock cycles. In the netlist, this method of assignment shows up as flip-flop B getting its input from the output net of flip-flop A. The value held by flip-flop A will take one clock cycle to propagate to flip-flop B.

A given register can only follow one of the assignment methods. The VE-57 error message indicates a single register is assigned with both procedural and RTL assignment methods. This usage does not clearly specify if the register’s value should be available in the current cycle or the next cycle.

WHAT NEXT

Decide if a register’s value, when passed on, should be that of the current clock cycle or the next clock cycle. If only one method of assignment was intended, fix the unintended use of the other method of assignment.

If both styles of assignment are needed, two variables are required in place of the original. One variable will be the target of procedural assignments and uses, while the other is used in RTL assignments.

EXAMPLE

The following example illegally mixes RTL and procedural assignment.

```
always @(posedge clk) begin
  tmp1 = input1 + input2;
  output1 = tmp1;

  tmp1 <= input1 + input2;
  output2 <= tmp1;
end
```

The intent appears to be providing the value of (input1 + input2) on output1, and the same value should be delayed one clock cycle before appearing on output2. Since tmp1 is the target of both methods of assignment, a VE-57 error is triggered by the aforementioned HDL. To retain the same intent, a second variable is introduced which interacts with the RTL assignments:

```
always @(posedge clk) begin
  tmp1 = input1 + input2;
  output1 = tmp1;

  tmp2 <= tmp1;
  output2 <= tmp2;
end
```

The previous example avoids targeting the same variable with RTL and procedural assignments. Register tmp1 is targeted by the procedural assignment, while new variable tmp2 is targeted by the RTL assignment.

VE-58 (error) Identifier '%s' previously declared %s

DESCRIPTION

WHAT NEXT

VE-60 (error) Unable to open file '%s' included by the 'include' directive %s

DESCRIPTION

The specified file cannot be opened, which is most likely caused by the file being

outside the search_path. This error is also triggered if the file permissions prohibit read access.

WHAT NEXT

If the file exists in the current directory, ensure "." is present in the search_path.

For files in other directories, add the directory to your search_path.

Permissions problems can be ruled out by trying to view the file in an editor. Errors of this variety are not specific to Verilog.

VE-61 (warning) Assignments to supply nets are ignored %s

DESCRIPTION

WHAT NEXT

VE-62 (warning) ’use_mux’ directive is not supported %s

DESCRIPTION

WHAT NEXT

VE-70 (error) Access to variables external to a module is not allowed from
inside functions and tasks %s

DESCRIPTION

WHAT NEXT

VE-71 (error) Assignment to external variables is not supported

’%s’

DESCRIPTION

WHAT NEXT

VE-72 (error) %s is not a construct in up or down path of module ’%s’

DESCRIPTION

WHAT NEXT

VE-73 (error) Component %s has not been instantiated in module ’%s’

DESCRIPTION

WHAT NEXT

VE-74 (error) Module %s not defined

DESCRIPTION

WHAT NEXT

VE-75 (error) Intra module hierarchical name (%s) not

supported in module ’%s’

DESCRIPTION

WHAT NEXT

VE-76 (error) Cannot find symbol ’%s’ in module ’%s’

DESCRIPTION

WHAT NEXT

VE-77 (error) Nested module names and intra-module hierarchical names not supported

in module ’%s’

DESCRIPTION

WHAT NEXT

VE-78 (error) Cannot find variable %s in module ’%s’

DESCRIPTION

WHAT NEXT

VE-79 (error) Module %s defined more than once

DESCRIPTION

WHAT NEXT

VE-80 (error) (Internal error) Unable to add extra port to contained design

DESCRIPTION

WHAT NEXT

VE-81 (error) (Internal error) Unable to create connection for

new port

DESCRIPTION

WHAT NEXT

VE-91 (error) In an event expression with ’posedge’ and ’negedge’ qualifiers, only
simple identifiers are allowed %s

DESCRIPTION

WHAT NEXT

VE-92 (error) The expression in the reset condition of the ’if’ statement in this
’always’ block can only be a simple identifer or its negation (%s)

DESCRIPTION

WHAT NEXT

VE-93 (error) The statements in this ’always’ block are outside the scope of the
synthesis policy (%s).
Only an ’if’ statement is allowed at the top level in this ’always’ block. Please refer to the HDL Compiler reference manual for ways

to infer flip-flops and latches from ’always’ blocks.

DESCRIPTION

WHAT NEXT

VE-94 (error) Asynchronous conditions for an ’always’ block can only be compared to 0 or 1 %s

DESCRIPTION

WHAT NEXT

VE-95 (error) Unsupported global reference %s

DESCRIPTION

In a previous release, the HDL Compiler provided limited support for global references. This is no longer true.

WHAT NEXT

Please rewrite your description without using globals. Normally, this can be done by passing signals through module inputs and/or outputs.

VE-96 (error) Redefinition of Object %s %s

DESCRIPTION

Object redefined when it is not allowed

WHAT NEXT

Change the name in the second definition

VE-97 (error) Mismatched directive %s

DESCRIPTION

Compiler directive used with wrong coupling. For example, an "‘endif" is used without a corresponding "‘ifdef" before it.

WHAT NEXT

Delete the mismatched directive or add the missed one.

VE-98 (warning) Macro %s is redefined %s

DESCRIPTION

The same macro name is provided two different definitions, leading to a single macro name having different meanings in separate parts of the HDL. Although not an error, this is a potentially hard to find and confusing problem.

WHAT NEXT

If the duplicate macro definition was accidental, provide a different name for one of the usages.

If the duplicate usage is intentional, this warning can be avoided by performing an ‘undef of the macro name before each duplicate definition.

VE-100 (warning) No arguments specified for pragma ’%s’ %s

DESCRIPTION

WHAT NEXT

VE-101 (warning) Pragma ’%s’ requires two arguments. The

second argument must be a string enclosed in double quotes %s

DESCRIPTION

WHAT NEXT

VE-102 (warning) Pragma '%s' accepts only one argument %s

DESCRIPTION

WHAT NEXT

VE-103 (warning) More than one %s pragma specified for %s %s

DESCRIPTION

A set/reset or multibit pragma was specified on the same signal more than once. For set/reset pragmas, a pragma may have been specified on the same block more than once. This warning is issued at the point where the duplicate pragma usage was detected.

WHAT NEXT

Find the first usage of the pragma, then determine which use of the set/reset or multibit pragma can be removed.

VE-104 (warning) The pragma '%s' for object %s will be ignored because the object could not be accessed.

DESCRIPTION

When a pragma is defined for an object, an attribute is placed on the object. If the object cannot be found, this pragma has no effect.

WHAT NEXT

Check HDL source to make sure that the object—usually a port, wire, or variable—is

specified before the pragma is defined.

VE-105 (error) %s has already been specified as a master process for a slave process %s

DESCRIPTION

WHAT NEXT

VE-106 (error) %s has already been specified as a slave process for a master process %s

DESCRIPTION

WHAT NEXT

VE-107 (warning) The "master_process_is/slave_process_is" pragma has been ignored because the %s process’%s’ could not be found.

DESCRIPTION

WHAT NEXT

VE-108 (error) For loop termination condition does not match index direction %s

DESCRIPTION

This error occurs when you use a "<" or "<=" with a decrementing loop, or a ">" or ">=" with an incrementing loop.

WHAT NEXT

Change the loop termination comparison to match the direction of the loop index.

EXAMPLE

The follow example demonstrates all eight possible combinations of loop bounds, termination conditions, and index directions. The loops labeled "Zero Iterations" are legal, but they have no effect since the loop initialization already violates the termination condition.

```
module test(a);
output [0:1] a;
reg    [0:1] a;

integer i;

    always @( a ) begin
      for(i=0; i<=1; i=i+1) a[i] = 1'b1; /* OK */
      for(i=0; i<=1; i=i-1) a[i] = 1'b1; /* Error */
      for(i=0; i>=1; i=i+1) a[i] = 1'b1; /* Error */
      for(i=0; i>=1; i=i-1) a[i] = 1'b1; /* Zero Iterations */

      for(i=1; i<=0; i=i+1) a[i] = 1'b1; /* Zero Iterations */
      for(i=1; i<=0; i=i-1) a[i] = 1'b1; /* Error */
      for(i=1; i>=0; i=i+1) a[i] = 1'b1; /* Error */
      for(i=1; i>=0; i=i-1) a[i] = 1'b1; /* OK */
    end

endmodule
```

VE-109 (information) Make sure there is an assertion block in the design
for directive '%s' %s.

DESCRIPTION

Directive 'one_hot' indicates at most one object in its group can have a *Logic1* value at any instance of time, all other objects must have a *Logic0* value. Directive 'one_cold' indicates at most one object in its group can have a *Logic0* value at any instance of time, all other objects must have a *Logic1* value. This information is used when inferring sequential logic.

WHAT NEXT

For a directive *//synopsys one_hot "set, reset"*, add a block in the design like the following example.

```
// synopsys translate_off
always @(set or reset)
begin
  if (set + reset > 1)
    $write("ONE-HOT violation for set, reset");
end
// synopsys translate_on
```

For a directive *//synopsys one_cold "set, reset"*, add a block in the design like the following example.

```
// synopsys translate_off
always @(set or reset)
begin
  if ({~set} + {~reset}  > 1)
    $write("ONE-COLD violation for set, reset");
end
// synopsys translate_on
```

VE-110 (warning) The directive '%s' for the group containing object '%s' is ignored because the object is not defined %s.

DESCRIPTION

WHAT NEXT

VE-111 (warning) The directive '%s' requires an argument containing more than one object %s.

DESCRIPTION

WHAT NEXT

VE-112 (error) The directive '%s' must be scoped inside a

named block %s.

DESCRIPTION

WHAT NEXT

Create a *label* for the 'always' block in which you want to apply this directive. Use the directive after 'begin:*label*'.

VE-120 (warning) This design contains multiple nets of type 'wired_and' or 'wired_or'. Please see the extended message for this warning for more information.

DESCRIPTION

The circuit synthesized by the (V)HDL Compiler can have a potential mismatch with simulation if a wire (signal in VHDL) or reg (variable) drives (through the use of the 'assign' construct in Verilog, '<=' construct in VHDL) more than one wire(signal) whose resolution is of type 'wired_and' or 'wired_or'.

In the following example, 'a' drives two wires(signals) 'e' and 'f' which are of resolution 'wired_or'.

EXAMPLES

Verilog

```
wor e,f;

assign f = a;
assign f = b & d;

assign e = a;
assign e = c & d;
```

WHAT NEXT

Instantiate explicit buffers to do the assignment to the wor or wand net. Do not use the Verilog 'buf' construct. Use a GTECH BUF gate or a buffer from your target

library

EXAMPLES

Verilog

```
wor e,f;

GTECH_BUF U1 (.A(a), .Z(f));
// assign f = a;
assign f = b & d;

GTECH_BUF U2 (.A(a), .Z(e));
//assign e = a;
assign e = c & d;
```

VE-121 (warning) This design contains event in verilog assignment. Please see the extended message for this warning for more information.

DESCRIPTION

The circuit synthesized by the (V)HDL Compiler can have a potential mismatch with simulation if an assignment in verilog contains event.

EXAMPLES

Verilog

```
q = @ (posedge ck) d;
```

Only one reg will be inferred if above assignment is used.

WHAT NEXT

Use the following assignments to replace above assignment if you want to have two regs inferred.

```
reg temp;

temp = d; @ (posedge ck); q = temp;
```

VE-122 (warning) Parameter range specification is only meaningful to synthesis. Different result may exist from simulations %s.

DESCRIPTION

Some simulators may ignore the range specification and expand the parameter to 32 bits. The circuit synthesized by the (V)HDL Compiler can have a potential mismatch with simulation if range specification is used in parameter declaration. For the following example, the value of "out" from simulator may be 0, while (V)HDL Compiler gives the value 16.

EXAMPLE1

Verilog

```
output [4:0] out;
parameter [3:0] a = 0;

assign out = {1'b1, a};
```

For the following example, the value of "a" from simulator may be 10, while (V)HDL Compiler gives the value 2. The leftmost bit is chopped out.

EXAMPLE2

Verilog

```
parameter [2:0] a = 4'b1010;
```

WHAT NEXT

Accordance between synthesis and simulation must be checked by the user where the bit width of the parameter is referred.

VE-123 (warning) This design contains assignment from wire to reg. Please see the extended message for this warning for more information.

DESCRIPTION

The circuit synthesized by the (V)HDL Compiler can have a potential mismatch with simulation if an expression containing wire is assigned to a reg.

EXAMPLES

Verilog

```
input a;
reg p;
reg q;

wire x = p;

always @(posedge CLK)
  p = a;
  q = x;
end
```

Two regs will be inferred for synthesis. While for certain simulation tools, it may simulate only as one reg. (e.g. VCS will simulate the above code as one reg)

VE-124 (error) Constant at RHS can not fit into LHS %s.

DESCRIPTION

The value of the right-hand side is outside the range of the left-hand side.

EXAMPLE

Verilog

```
parameter [2:0] a = 14;
```

```
parameter [2:0] b = 4'b1110;
```

WHAT NEXT

Declare a proper range for the left-hand side. Or check the value on the right-hand side to ensure that the range of the left-hand side covers that of the right-hand side.

VE-125 (warning) The '%s' '%s' is not a legal verilog identifier. It has been renamed to '%s'.

DESCRIPTION

This warning is generated when the identifier contains illegal Verilog character.

WHAT NEXT

Please refer to Verilog reference manual and change it to legal Verilog character if you do not want it to be renamed.

VE-126 (warning) Port %s has been declared previously with a different type %s

DESCRIPTION

The port warned has been declared previously with a different type.

Verilog

```
module test ( ..., dataout);
output dataout;
reg [2:0] dataout;
```

Here dataout has been previously declared as one-bit, and later on declared as [2:0]. This may cause simulation, synthesis and formal verification mismatch due to the different interpretation in different tools as what's type of dataout.

WHAT NEXT

Change your Verilog source code to remove the inconsistent declaration for the port.

VE-127 (error) Ascending range in enum declaration is not supported with hdlin_enable_presto = false

DESCRIPTION

Ascending range in enum declaration is not supported with hdlin_enable_presto = false.

WHAT NEXT

Please either change the ascending range into descending range or restore hdlin_enable_presto to its default value TRUE.

VE-128 (error) Bussed clock is not longer supported in HDLC. Use Presto Verilog instead.

DESCRIPTION

Bussed clock is no longer supported in HDLC.

WHAT NEXT

Please either recode the Verilog source code, or use Presto Verilog instead.

VER-1 (warning) %s Redundant digits given in number %s.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-2 (warning) %s Unknown debug option %s

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-4 (warning) %s Incompatible port connection, port %d of instance %s in module %s.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-5 (warning) %s Mismatch in number of ports for instance

%s

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-8 (warning) %s Hierarchical component name %s is a macromodule and not expandable.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-9 (warning) %s Illegal synopsys label pragma, it will be ignored.

DESCRIPTION

When synopsys label pragma is put wrong place, this warnning message will be dumped. Presto ignores this label pragma.

WHAT NEXT

Put the label pragma into right place.

VER-12 (error) %s Hierarchical component name %s is not a

module, task, function, or block

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-15 (error) %s The call to ’$display’ does not have enough arguments to satisfy all format specifiers.

DESCRIPTION

This error message occurs if you supply a format string when using the ’$display’ system function, and there are not enough subsequent parameters to supply each token in the specifier.

In the following example, the format specifier "%s%s%d" contains three tokens and requires at least three values, which are a, b, and c.

```
   $display ("%s%s%d", a, b, c);
```

WHAT NEXT

Correct any occurrences of insufficient parameters for the specified format string in the Verilog code.

SEE ALSO

analyze(2)
read(2)

VER-16 (error) %s First parameter of $dumpvars must be an integer

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-17 (error) %s Incompatible number of arguments, usage versus declaration.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-18 (error) %s Bounds %s for vector %s must be integer.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-19 (error) %s +liborder and +librescan conflict; only one can be specified.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-20 (error) %s Package %s does not export the name '%s'.

DESCRIPTION

This message issues when the System Verilog scope operator (::) tries to extract content from the specified package, but the name was either not found in the global scope of that package, or its package-level definition is marked as not exportable.

WHAT NEXT

Check that the package name is correct and that the source code with the desired definition has been analyzed without errors more recently than any other package with the same name. If the supplying package is at fault, re-analyze it and also the present file. If the consuming reference is not correct, adjust the RTL and re-analyze. The setting of hdlin_sv_packages can also affect whether names imported into a package can be re-exported.

SEE ALSO

analyze (2), **read** (2), **hdlin_sv_packages** (3), **VER-26** (n), **VER-934** (n).

VER-21 (error) %s Multiple conflicting definitions of '%s' are available via wildcard imports.

DESCRIPTION

This message issues when you use a name which you have not previously declared that has more than one distinct definition supplied through several wildcard import routes (import pkg_A::*, pkg_B::*;) into the same surrounding scope.

When all imported packages are analyzed with hdlin_sv_packages set to *dont_chain*, this error corresponds to the prohibition in section 19.2.1 of IEEE-1800-2005: a name may come from at most one wildcarded package. Packages analyzed with hdlin_sv_packages set to *chain* or *enable*, may also export names that they imported from elsewhere. Thus a single common definition for name might arrive via several paths, VER-21 issues only when multiple source definitions are import candidates, and no import is more local than the others at the point of use.

WHAT NEXT

There are many RTL source code adjustments of the import statements and/or the name reference that could clear this condition: You could place the wildcard imports at different levels in the scope stack so that the prefered supplier shadows the unwanted supplier. You could add an explicit "import desired_supplier::name;" you could prefix the package scope extraction operator "desired_supplier::" to the name reference to indicate the desired package. You might delete the import of an unused

package that causes the conflict. You could correct a spelling to avoid the collision. You could supply a missing local declaration of the name in the overloaded scope to override the wildcard imports. You could explicitly declare the name with a local meaning.

If you believe the RTL as written is correct, check that the current search_path reaches .pvk files that were produced by successfully analyzing the current versions of these packages' source files. The setting of *hdlin_sv_packages* ***at the time those packages were analyzed can also affect whether names imported into them will be re-exported, which might be either producing or exposing the observed name conflict.***

SEE ALSO

analyze (2), **read** (2), **hdlin_sv_packages** (3), **ELAB-106** (n).

VER-22 (error) %s Too many parameters found on task %s.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-23 (error) %s The %s parameter is not completely writable and it is being passed to an OUTPUT or INOUT formal parameter.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-25 (error) %s Module ’%s’ is redefined.

DESCRIPTION

You receive this message to inform you that during execution of the **analyze** or **read** command the compiler has encountered in your design a module declaration that has the same name as a previously defined module. Each module name must be unique.

WHAT NEXT

Rename one of the modules so that all modules have unique names.

SEE ALSO

analyze (2), **read** (2).

VER-26 (warning) %s The package %s has already been analyzed. It is being replaced.

DESCRIPTION

You receive this warning message if a package with the same name was analyzed by a previous read or analyze command, possibly during a different DC shell session. This can occur in three possible ways:

• The file currently being analyzed has already been analyzed.

• A package with the same name is declared in another file analyzed in the current work directory.

• You have modified the package’s source file and are reanalyzing it.

The previous package contents are removed, and possibly overwritten by the declaration currently being analyzed.

WHAT NEXT

This is only a warning message.

However, you can check the overwritten file. If the result is not what you intended, change the package name and run the command again.

All references to a revised package should be re-analyzed to insure that they are coherent. Failure to do this is one source of ELAB-106 warnings, VER-20, and various

type-mismatch errors.

SEE ALSO

analyze (2), **read** (2), **ELAB-106** (n), **VER-20** (n), **VER-930** (n).

VER-27 (error) %s Package %s has already been used or declared during this command.

DESCRIPTION

This error issues if a package is used before being (re)declared within the same analyze or read command. There are many ways this condition can arise. In addition to use-before-declaration within a single file: the file currently being analyzed, a copy of that file, or another file declaring or using a package with the same name may have appeared earlier in the file list of this command, been ‘include’d there, or been indirectly imported by earlier package reference(s).

WHAT NEXT

Arrange your command line(s) so that every package is analyzed or read exactly once before its first use.

Use a separate analyze command to update or change a package’s definition. All references to a re-analyzed package should also be re-analyzed to insure that they are coherent. Failure to do this is one source of ELAB-106 ("homograph") warnings and type-mismatch errors.

SEE ALSO

VER-26 VER-227 ELAB-106 analyze (2), **read** (2).

VER-28 (error) %s %s is a function and not a task

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-30 (error) %s Stack overflow. %s

DESCRIPTION

This error message occurs when RTL compilation cannot complete because the internal stack overflowed. All applications and tools need an internal stack to execute. This stack can grow up to a limit set by the "limit" command on csh interpreters, or the "ulimit" command on sh interpreters.

The following conditions may cause the internal stack to overflow:

• Your design has an infinite or very long iterative loop and you set a high value for the **hdlin_while_loop_iterations** variable.

• Your design has a deeply nested construct, such as a deeply parenthesized expression. This occurs with code generated by other tools, but not with hand coded sources.

Note that this message may be shown for loops that finish in simulation, but are infinite in synthesis. One example of an infinite loop, and so is unsupported, is this design:

```
module sum (input [3:0] in, output reg [7:0] out);
reg [3:0] i;
always @* begin
  i = in;
  out = 0 ;
  while (i>0) begin
    out = out + i;
    i = i - 1;
  end
end
endmodule
```

This example will not finish in synthesis because the terminating condition depends on a port and so is never a proper constant.

WHAT NEXT

Review your code and ensure that the terminating condition of an iterative loop will eventually be constant true. It is always difficult to determine if an iterative loop will eventually finish, but this message is usually shown when it is infinite.

In very unusual cases, the VER-30 message is shown because the stack size limit is not big enough. Check the current stack size limit with the "limit stacksize" command on csh interpreters, or the "ulimit -s" command on sh interpreters. Increase the stack size significantly, for example with the "limit stacksize 100m" command on csh interpreters, or the "ulimit -S -s 104857600" command on sh interpreters. Restart Design Compiler. Analyze and elaborate your design again. If the message persists or the current stack size is unlimited, re-evaluate the possibility of an infinite loop.

Note that if your design has an infinite loop and the stack size limit is increased, Design Compiler will also take more time to show the stack overflow message.

If your design has been generated by another tool, this error message may be due to a deeply nested construct. In this case increase the stack size limit as described above, restart Design Compiler, and analyze and elaborate your design again.

SEE ALSO

analyze(2)
elaborate(2)
ELAB-900(n)
ELAB-901(n)

VER-35 (warning) %s Register (%s) is the target of both blocking and nonblocking assignments in the same process.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-36 (error) %s Internal error: %s, in %s at line %d

DESCRIPTION

This message issues when RTL compilation cannot complete because the compiler reached some detectably invalid internal state. Internal cross-checks are used extensively in the Presto RTL compilers to prevent software bugs from producing erroneous results - often called "bad logic". RTL code which conforms closely to the IEEE standards (1364, 1800, or 1076) and lies within the synthesizable subsets of those languages should, of course, not encounter internal compiler errors.

WHAT NEXT

Contact Synopsys support who can help you further diagnose this problem and can often help you find a coding workaround, or a compiler release where the bug has been fixed.

If you encounter an internal error when using the most recent release from Synopsys, submit a testcase that reproduces the problem to the Synopsys Support Center by using Enter A Call at http://solvnet.synopsys.com/EnterACall.

For information about the latest software releases, go to the Synopsys SolvNet Release Library at http://solvnet.synopsys.com/ReleaseLibrary.

For information about creating, packaging, and sending a testcase, go to http://www.synopsys.com/testcase.

SEE ALSO

read (2), **analyze** (2), **elaborate** (2), **ELAB-255** (n), **VER-37** (n).

VER-37 (error) %s Internal error.

DESCRIPTION

This error message occurs if the HDL Compiler encounters an internal error and cannot proceed. The command shell is not affected by this failure, so your work session can continue without loss of data. Internal errors in the HDL Compiler are usually related to one or two constructs that can be recoded to work around the problem until Synopsys releases a new compiler free of this defect.

The Presto HDL Compiler contains thousands of internal checks on its operation designed to catch miscompilation problems as close as possible to their source. Internal errors prevent the production of incorrect results.

WHAT NEXT

If you encounter an internal error when using the most recent release from Synopsys, submit a testcase that reproduces the problem to the Synopsys Support Center by using Enter A Call at http://solvnet.synopsys.com/EnterACall.

For information about the latest software releases, go to the Synopsys SolvNet Release Library at http://solvnet.synopsys.com/ReleaseLibrary.

For information about creating, packaging, and sending a testcase, go to http://www.synopsys.com/testcase.

VER-38 (error) %s Internal error: %s

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-40 (error) %s Too many errors; can’t continue.

DESCRIPTION

The Presto HDL Compiler issues this error from the read, analyze, or elaborate commands when it has encountered too many errors to continue the compilation.

WHAT NEXT

Correct all of the errors reported before this one, and repeat the command.

VER-41 (error) %s Unable to open file ‘%s’: %s.

DESCRIPTION

This error message occurs when you issue a **read** or **analyze** command on a file that cannot be opened for reading or writing.

WHAT NEXT

To write to a file, make sure that the directory named by the **hdlin_output_dir** variable is writable, or change **hdlin_output_dir** to point to a writable directory. To read a file, make sure the file exists.

SEE ALSO

analyze(2)
read(2)

VER-43 (error) %s Out of memory.

DESCRIPTION

This may indicate syntax errors.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-44 (warning) %s Little argument or return value checking

implemented for system task or function %s.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-51 (error) %s internal error: %s

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-55 (error) %s Illegal character in module, interface, or package name.

DESCRIPTION

You receive this error message when the name you specified for a module, interface, or package cannot be directly used to name a file in the host file system. This is usually due to some reserved characters, such as '/' or ':'. Names in the standard *definitions name space* exist as file system objects and must conform to host or network naming conventions in addition to Verilog lexical rules.

For example, a/b/c is an invalid module name.

WHAT NEXT

Change the module name in the relevant code to conform to the rules for file names in the host file system and run the command again.

VER-59 (error) %s Array index out of bounds %s.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-60 (error) %s Array index out of bounds %s.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-61 (warning) %s Statement unreachable %s.

DESCRIPTION

This warning is issued when statements inside of conditional branches can’t be reached, because the condition is always false or a previous condition is always true.

WHAT NEXT

Check the conditions of conditional statements like: if, case, when, ?, ...

VER-65 (error) %s Option ’hdlin_decoder_min_use_percentage’ must be in the range 0..100 (currently %d).

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-66 (warning) %s Won’t infer decoders with input width > %d; option ’%s’ set too large.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-86 (warning) %s Comparison against ’x’ values not inside a casex is always false.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-97 (error) %s No input files specified.

DESCRIPTION

You receive this error message because no input files were specified with the **analyze** or **read** command for the Presto HDL Compiler. These commands require that one or more input files be specified.

WHAT NEXT

Execute the **analyze** or **read** command and specify one or more input files.

SEE ALSO

analyze (2), **read** (2).

VER-98 (error) %s Relative placement group '%s' is defined multiple times.

DESCRIPTION

This error message occurs when a relative placement group is defined multiple times.

WHAT NEXT

Remove the duplicate relative placement group and run the command again.

SEE ALSO

elaborate(2)
read(2)

VER-102 (warning) %s Variable '%s' does not accept the value '%d'. The value has been reset to a compatible value.

DESCRIPTION

This warning message occurs when a variable uses a value that is not supported by the current flow. The variable is reset to a compatible value as documented in the man page of the variable.

WHAT NEXT

Verify that the value for the variable is within the allowed range, and that the value matches your design requirement.

SEE ALSO

analyze(2)
elaborate(2)
read (2)

VER-103 (warning) %s Pragma is obsolete or not implemented.

It will be ignored.

DESCRIPTION

A pragma is a compiler directive in the source code. The Presto HDL compiler does not implement certain pragmas that the Synopsys HDL Compiler does. This warning, which has occurred during **analyze** or **read** command activity, notifies you that the pragma in the design will not have the same effect it would have if you were to compile the design using the Synopsys HDL Compiler.

The Presto HDL compiler implements most of the commonly used compiler directives, but not some of the less frequently used ones.

WHAT NEXT

If your design requires the use of the pragma the message refers to, use the Synopsys HDL Compiler to analyze and elaborate your design.

SEE ALSO

analyze (2), **elaborate** (2), **read** (2).

VER-104 (warning) %s The '%s' construct is not supported. It will be ignored.

DESCRIPTION

This warning message occurs during an **analyze** or **read** command activity, and notifies you that the given construct in your design is not supported for synthesis.

WHAT NEXT

Check your design to verify that it still functions correctly, even though the construct the message refers to is ignored.

To avoid this warning, surround the construct with the following compiler directives:

```
`ifndef SYNTHESIS

    <construct>

`endif
```

When the Presto HDL Compiler sees these compiler directives, it does not interpret

the construct.

SEE ALSO

analyze(2)
read (2)

VER-105 (warning) %s Call to function '%s' with no parameters is not standard Verilog.

DESCRIPTION

You receive this message because, during a **read** or **analyze** command activity, the compiler encountered a call to a function or functions that used parentheses to indicate an empty parameter list.

IEEE standard Verilog requires that a function have at least one input argument. The Presto HDL compiler accepts functions with no arguments; however, many Verilog tools do not.

```
...
  x = f();  // non-standard call to zero-argument function
...
```

WHAT NEXT

Consider adding at least one input argument to the function in question to conform to IEEE standards.

SEE ALSO

analyze (2), **read** (2), **VER-175** (n).

VER-106 (error) %s Function declaration redeclares symbol '%s'.

DESCRIPTION

You see this message because you have assigned a function declaration to a symbol that has already been defined.

In the following example, which demonstrates such a situation, the symbol *f* is declared twice: first as a register and then as a function:

```
reg f;          // initial declaration of 'f'

function f;     // illegal redeclaration of 'f'
...
endfunction
```

The example elicits the VER-106 message.

WHAT NEXT

Rename either the function declaration or the other declaration and all corresponding uses of the symbol.

SEE ALSO

analyze (2), **read** (2).

VER-107 (error) %s Functions cannot contain blocking delays.

DESCRIPTION

You are seeing this message because, during the execution of the **read** or **analyze** command, the compiler has encountered blocking delays in your design. The Verilog standard states that functions execute in one (simulation) time unit and cannot contain time-controlling statements, such as blocking delays.

The following example demonstrates the incorrect use of blocking delays in a function body:

```
...
function f;
 input a;
 begin
  #10;       // illegal use of blocking delay inside a function
  f = a;
 end
endfunction
...
```

WHAT NEXT

For synthesis, remove the the blocking delays because the compiler does not accept them and terminates with this error.

SEE ALSO

analyze (2), **read** (2).

VER-108 (error) %s Functions cannot contain event control statements.

DESCRIPTION

You receive this error message because you have attempted to use an event control statement inside of a function. According to the Verilog standard, functions shall execute in one simulation time unit, and are not allowed to contain time-controlling statements. Therefore, event control statements are not allowed inside functions.

The following example demonstrates the illegal use of an event control statement in a function body:

```
...
function f;
 input a;
 begin
  @(posedge clk);   // illegal use of an event control statement in a function.
  f = a;
 end
endfunction
...
```

WHAT NEXT

Rewrite the source code so that the functions do not contain any time-controlling statements.

SEE ALSO

analyze (2), **read** (2).

VER-109 (error) %s Function arguments cannot be declared as ’inout’.

DESCRIPTION

You receive this error message because you have declared a function argument as ’inout’. According to the Verilog standard, functions can have arguments declared as ’input’ only. Declaring a function argument as ’inout’, as illustrated in the following example, results in this error message.

```
...
function f;
 inout a;    // illegal declaration of a function argument as ’inout’.
 ...
```

```
endfunction
...
```

WHAT NEXT

Rewrite the code so that the function has 'input' arguments only. If you cannot avoid using 'inout' arguments, consider using a task instead of a function.

SEE ALSO

analyze (2), **read** (2).

VER-110 (error) %s Function '%s' not defined.

DESCRIPTION

You receive this error message because no function with the given name has been defined.

WHAT NEXT

Check to see if the specified function name was misspelled. If not, add a function declaration to define the missing function.

SEE ALSO

analyze (2), **read** (2).

VER-111 (error) %s Function arguments cannot be declared as 'output'.

DESCRIPTION

You receive this error message because, according to IEEE Std 1364, functions can only have arguments declared as 'input'. Declaring a function argument as 'output', as illustrated in the following example, results in this error message.

```
...
function f;
 output a;    // illegal declaration of a function argument as 'output'.
 ...
endfunction
...
```

WHAT NEXT

Rewrite the code so that the function only has 'input' arguments. If you cannot avoid using 'output' arguments, consider using a task instead of a function.

SEE ALSO

analyze (2), **read** (2).

VER-112 (error) %s Illegal function declaration using empty parameter list.

DESCRIPTION

You receive this error message because the function declaration was written with an empty parameter list.

The following example shows a function declaration that would generate this error.

```
function foo();
...
endfunction
```

The correct function declaration:

```
function foo;
...
endfunction
```

WHAT NEXT

Rewrite the function declaration as shown in the example.

SEE ALSO

analyze (2), **read** (2).

VER-113 (error) %s Functions cannot enable tasks.

DESCRIPTION

You receive this error message because you attempted to enable a task from a function. According to the IEEE Std 1364, tasks cannot be enabled from functions. The following is an example of this situation.

```
task t;
  ...
endtask


function f;
  ...
  t;          // error: tasks cannot be enabled from functions.
endfunction
```

WHAT NEXT

Rewrite the source code so that tasks are enabled only from processes or other tasks.

SEE ALSO

analyze (2), **read** (2).

VER-114 (error) %s Functions cannot contain 'wait' statements.

DESCRIPTION

You receive this error message when you attempt to use a 'wait' statement inside of a function. According to the IEEE Verilog Standard 1364, functions shall execute in one simulation time unit and are not allowed to contain time-controlling statements. Therefore, 'wait' statements are not allowed inside functions.

The following example demonstrates the illegal use of a 'wait' statement in a function body.

```
...
function f;
  input a;
  begin
    wait (!a) f = a;   // 'wait' not allowed inside a function.
  end
endfunction
...
```

WHAT NEXT

Rewrite the Verilog source code so that functions do not contain any time-controlling statements.

SEE ALSO

analyze (2), **read** (2).

VER-115 (error) %s Redefinition of compiler directive '%s' not supported.

DESCRIPTION

Redefining compiler directives using 'define' is not allowed. The following example is the illegal attempt to redefine the compiler directive 'define' itself:

```
   `define define 2      // error: illegal redefinition of a
                         // compiler directive
```

WHAT NEXT

If a redefinition of the the original directive was not intended, just rename the symbol such that it does not collide with a compiler directive.

VER-116 (error) %s Redeclaration of symbol '%s' as parameter.

DESCRIPTION

You receive this message if a symbol in a parameter declaration has already been declared, either as a parameter or as something else. In the following example, "in" is first declared as an input, then erroneously redeclared as a parameter.

```
 input in;
 ...
 parameter in = 1'b0;    // erroneous redeclaration of input 'in'
                         // as a parameter.
```

WHAT NEXT

Decide which of the declarations is the intended one and remove or change the name in the other declaration. If you change the name in a declaration, ensure that you change all occurrences of that name.

SEE ALSO

analyze (2), **read** (2).

VER-117 (error) %s Read-only expression '%s' passed to 'output' or 'inout' argument of a task or function.

DESCRIPTION

Task (or SV function) arguments declared with direction 'output' or 'inout' must receive an actual register, selection within a register, or other legal target of an assignment statement.

For example, the following two task calls are incorrect because neither an input nor a wire are registers, so they are not valid arguments to task output or inout parameters.

```
input a;
wire b;

task t;
  output x;
  begin
    x = 1'b0;
  end
endtask

always @(posedge clk)
  begin
    t(a);      // error: input is not a register
    t(b);      // error: wire is not a register
  end
```

WHAT NEXT

Check the argument name or its positional order. If the task or function definition does not assign to the formal argument, restrict its direction to 'input'. Otherwise change the calling RTL to receive the task's (or function's) assignment into a register variable.

SEE ALSO

analyze(2)
read(2)
VER-118(n)

VER-118 (error) %s Constant passed to an 'output' or 'inout'

argument of a task or function.

DESCRIPTION

Task (or SV function) arguments declared with direction 'output' or 'inout' must receive an actual register, selection within a register, or other legal target of an assignment statement.

The following task call is illegal because 1b0 is a constant value and not a valid argument to a task output or inout parameter.

```
task t;
 output x;
 ...
endtask

...

t(1'b0);    // error: passing a constant value to an
            // 'output' parameter
```

WHAT NEXT

Check the argument name or its positional order. If the task or function definition does not assign to the formal argument, restrict its direction to 'input'. Otherwise change the calling RTL to receive the task's (or function's) assignment into a register variable.

SEE ALSO

analyze(2)
read(2)
VER-117(n)

VER-119 (error) %s Wrong number of arguments in call to function or task '%s'.

DESCRIPTION

You receive this error message because the actual number of arguments in the function or task call does not match the number of formal arguments expected by the corresponding function or task.

WHAT NEXT

Specify the correct number of arguments. Refer to the function or task declaration

to determine the number and order of the expected arguments.

SEE ALSO

analyze (2), **read** (2).

VER-120 (error) %s Port '%s' not declared as 'input', 'output' or 'inout'.

DESCRIPTION

The IEEE Verilog Standard 1364 requires that each port listed in a module port list be declared as input, output, or inout.

You receive this error because a port listed in the module port list is not declared subsequently as input, output, or inout.

The following example shows a correct port declaration:

```
module m (i, o);
 input i;      // omitting this input declaration is an error.
 output o;
 reg o;

 always ...

endmodule
```

If the input declaration of port *i* is not present, an error is issued.

WHAT NEXT

Add the missing port declaration, as either input, output, or inout.

SEE ALSO

analyze (2), **read** (2).

VER-121 (error) %s Redeclaration of port '%s' is not allowed.

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the Presto HDL Compiler has detected that the same port is declared twice inside the same function, task, or module. Following is an example that illustrates this type

of error:

```
  function f;
   input a;
   input a;      // redeclaration of already declared port
    ...
  endfunction;
```

WHAT NEXT

Remove or rename as appropriate one of these ports.

SEE ALSO

analyze (2), **read** (2).

VER-122 (error) %s Redeclaration of symbol '%s' as a real number is not allowed.

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the Presto HDL Compiler has detected a symbol declared twice, which is not valid.

In the following example, "r" is declared both as an integer and as a real number.

```
   integer r;
   real r;   // error: invalid redeclaration of "r" as a real number
```

WHAT NEXT

Remove or rename as appropriate one of the declarations.

SEE ALSO

analyze (2), **read** (2).

VER-123 (error) %s Redeclaration of symbol '%s' not allowed.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-124 (error) %s Task or function argument must be specified.

DESCRIPTION

This message issues when the Presto HDL Compiler parses an incomplete parameter list, or one with empty comma-delimited positions. It is an error to omit a parameter (argument) in the list used to enable (invoke) a task or function (unless, in SystemVerilog, the corresponding formal argument was declared with a default value initializer). Default initializers are not yet supported by Presto HDL.

The following example demonstrates a correct and an incorrect task call:

```
task not;
 input a;
 output y;
 ...
endtask

...
not(,o);       // error: incomplete parameter list: first argument missing
not(a,b);      // correct task call
...
```

WHAT NEXT

Check the location of commas in this argument list. Specify any missing arguments.

SEE ALSO

analyze (2), **read** (2).

VER-125 (error) %s called function (or task) '%s' not defined as a function (or task).

DESCRIPTION

This error message occurs during **analyze** or **read** command activity when the Presto HDL Compiler detects a function (or task) that is not properly defined.

The specified function or task is either not defined at all, defined as something

other than a function (or task), or using a task as a function, or using a function as a task.

In Verilog-2005 and SystemVerilog standards, functions (or tasks) defined within anonymously scoped generate blocks are not accessible outside that block. For example:

```
module m #(parameter P=32) (output o);
  generate
    if (P>16)
      function f (input i);
         f = 1'b0 ;
      endfunction
    else
      function f (input i);
         f = 1'b1 ;
      endfunction
  endgenerate

  assign o = f(1'b0);          /* Function 'f' is not visible  */
                               /* outside the generate block */
endmodule
```

WHAT NEXT

Check that the name of the function (or task) is spelled correctly, and that the name is a valid definition of the function (or task).

SEE ALSO

analyze(2)
read(2)

VER-126 (error) %s Called task '%s' not defined as a task.

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the Presto HDL Compiler has detected a task that is not properly defined.

The task, which a task call refers to, is not defined at all or it is defined as something other than a task.

WHAT NEXT

Check to verify that the name of the task is spelled correctly. If it is, then you

need to supply a different (correct) definition of the task.

SEE ALSO

analyze (2), **read** (2).

VER-127 (error) %s Called task '%s' not defined as a task.

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the Presto HDL Compiler has detected a task that is not properly defined.

The task, which a task call refers to, is not defined at all or it is defined as something other than a task.

WHAT NEXT

Check to verify that the name of the task is spelled correctly. If it is, then you need to supply a different (correct) definition of the task.

SEE ALSO

analyze (2), **read** (2).

VER-128 (error) %s Parameterless task call to task '%s' should not have parentheses.

DESCRIPTION

Task calls that do not pass any parameters should not use parentheses to indicate an empty parameter list.

The following example demonstrates the right and the wrong way to call a task without parameters:

```
task t;
 ...
endtask

...
 t();         // error: incorrect syntax for empty parameter list
 t;           // correct syntax without parentheses
...
```

WHAT NEXT

Rewrite the task call as shown in the example above.

VER-129 (warning) %s Intraassignment delays for blocking assignments are ignored.

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the Presto HDL Compiler has detected an intraassignment delay specified for a blocking assignment. Such delays have no meaning in synthesis, and the compiler ignores them.

Following is an example of an intraassignment delay.

```
y = #10 a;
```

WHAT NEXT

Synthesis ignores intraassignment delays for blocking assignments, so it is acceptable to remove them in instances such as this.

SEE ALSO

analyze (2), **read** (2).

VER-130 (warning) %s Intraassignment delays for nonblocking assignments are ignored.

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the Presto HDL Compiler has detected an intraassignment delay specified for a nonblocking assignment. Such delays have no meaning in synthesis, and the compiler ignores them.

Following is an example of an intraassignment delay.

```
y = #10 a;
```

WHAT NEXT

Synthesis ignores intraassignment delays for nonblocking assignments, so it is acceptable to remove them in instances such as this.

SEE ALSO

analyze (2), **read** (2).

VER-131 (error) %s Intra-assignment events for blocking assignments are unsupported in synthesis.

DESCRIPTION

This error message occurs because intra-assignment events in blocking assignments are not supported for synthesis. For example:

```
y = @(posedge clk) a;
```

WHAT NEXT

Rewrite the block so it does not use an intra-assignment event.

VER-132 (error) %s Intra-assignment events for non-blocking assignments are not supported.

DESCRIPTION

Intraassignment events for non-blocking assignments are not supported during synthesis. For example:

```
y <= @(posedge clk) a;
```

The correct synthesizable version is:

```
y <= a;
```

WHAT NEXT

Remove the intraassignment event as shown above.

VER-133 (warning) %s Intra-assignment repeat-event controls

for blocking assignments are ignored.

DESCRIPTION

Intra-assignment repeat-event for blocking assignments do not have a meaning for synthesis and are ignored. For example:

```
   y = repeat(3) @(posedge clk) a;
```

The correct synthesizable version is:

```
   y = a;
```

WHAT NEXT

Take out the repeat event specification as shown above.

VER-134 (error) %s Variable '%s' is the target of both blocking and nonblocking assignments in the same always block.

DESCRIPTION

Mixing of blocking and nonblocking assignments to the same variable in the same always block is not supported in synthesis. For example:

```
  always @(...) begin
    y <= a;
    y = a;
  end
```

Verilog simulator performance is not improved by the mixing of blocking and nonblocking assignments in the same always block.

WHAT NEXT

If the always block represents combinational logic, rewrite the always block to use only blocking assignments. If the always block represents sequential logic, rewrite the always block to use only nonblocking assignments.

VER-135 (warning) %s Intra-assignment repeat-event controls

for non-blocking assignment are ignored.

DESCRIPTION

Intra-assignment repeat-event for non-blocking assignments do not have a meaning for synthesis and are ignored. For example:

```
y <= repeat(3) @(posedge clk) a;
```

The correct synthesizable version is:

```
y <= a;
```

WHAT NEXT

Take out the repeat event specification as shown above.

VER-136 (warning) %s Function '%s' with non-empty body is mapped to '%s'; body will be ignored.

DESCRIPTION

By mapping a function to a module, the module (instead of the function body) determines the implementation of the function. This warning is given to remind you the body of the function will be ignored.

The following example contains a function for which this warning message will be issued:

```
function f;     // synopsys map_to_module add
 input a;
 input b;
 begin
  f = a+b;      // function body will be ignored.
 end
endfunction
```

WHAT NEXT

Make sure that the body of the function is indeed intended to be ignored in favor of the module the function is mapped to.

VER-137 (error) %s Return port name '%s' conflicts with names

of function input parameters.

DESCRIPTION

The return port name specified by the 'return_port_name' pragma must be different from all formal parameters of the function the pragma is attached to. This error indicates that there is a conflict with one of the formal parameter names.

In the following example such a conflict is demonstrated: The return port name is specified to be "a", but a function parameter with the same name exists.

```
  function f;
// synopsys map_to_module down
// synopsys return_port_name a
   input a;
   ...
  endfunction
```

To resolve this error, the name of the function parameter is changed to "b" in the following example:

```
  function f;
// synopsys map_to_module down
// synopsys return_port_name a
   input b;
   ...
  endfunction
```

WHAT NEXT

Change the name of the conflicting function parameter or the port name of the module the function is mapped to so that they don't conflict.

VER-138 (warning) %s Extraneous argument for system function or task '%s' ignored.

DESCRIPTION

The system function has been passed an unexpected additional argument. This argument will be ignored.

WHAT NEXT

Remove the extra argument from the call. Refer to the function/task declaration to find out which arguments are actually required.

VER-139 (warning) %s Parameterless call to function '%s' should not have parentheses.

DESCRIPTION

In Verilog, calls to functions without parameters should not use parentheses to indicate an empty parameter list; only the function identifier is used to call the function.

The following example indicates the correct and incorrect way to write a parameterless Verilog function call:

```
...
  x = f();    // incorrect syntax: using parentheses
  x = f;      // correct syntax: using the function identifier only
...
```

WHAT NEXT

Remove the parentheses as shown in the example above.

SEE ALSO

analyze (2), **read** (2).

VER-140 (warning) %s Nonblocking assignments and blocking delays in the same process; potential simulation or synthesis mismatch.

DESCRIPTION

This warning message occurs during **analyze** or **read** command activity, when the Presto HDL Compiler detects a nonblocking assignment and a blocking delay in the same process. This can cause simulation or synthesis mismatches.

The following is an example that causes the warning message:

```
always @(posedge clk) begin
  #10;              // blocking delay is ignored
  out <= in;        // nonblocking assignment
end
```

WHAT NEXT

Review the code carefully to explore the potential for a simulation or synthesis mismatch.

SEE ALSO

analyze(2)
read(2)

VER-141 (error) %s Blocking delays and nonblocking assignments are not allowed in the same process.

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the Presto HDL Compiler has detected a nonblocking assignment and a blocking delay in the same process, which is invalid for synthesis.

Even though synthesis ignores blocking delays, it is important to recognize them in the two forms in which they occur. Blocking delays can stand alone or as part of an intra-assignment delay. The following example shows an instance of each form:

```
always @(posedge clk) begin
  a <= x;         // nonblocking assignment
  #10;            // blocking delay, not allowed with nonblocking assignment
  b = #10 y;    // intraassignment delay, not allowed with nonblocking assignment
end
```

WHAT NEXT

Synthesis ignores blocking delays, so it is acceptable to remove them in instances such as this.

SEE ALSO

analyze (2), **read** (2).

VER-142 (error) %s Nonblocking assignments and blocking delays are not allowed in the same process.

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the

Presto HDL Compiler has detected a nonblocking assignment and a blocking delay in the same process.

The following example demonstrates this invalid description:

```
always @(posedge clk) begin
  #10;            // blocking delay
  out <= in;      // nonblocking assignment, not allowed with blocking delay
end
```

WHAT NEXT

Synthesis ignores blocking delays, so it is acceptable to remove them in instances such as this.

SEE ALSO

analyze (2), **read** (2).

VER-143 (error) %s Blocking delays and nonblocking assignments are not allowed in the same process.

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the Presto HDL Compiler has detected a nonblocking assignment and a blocking delay in the same process, which is invalid for synthesis.

Even though synthesis ignores blocking delays, it is important to recognize them in the two forms in which they occur. Blocking delays can stand alone or as part of an intra-assignment delay. The following example shows an instance of each form:

```
always @(posedge clk) begin
  a <= x;         // nonblocking assignment
  #10;            // blocking delay, not allowed with nonblocking assignment
  b = #10 y;   // intraassignment delay, not allowed with nonblocking assignment
end
```

WHAT NEXT

Synthesis ignores blocking delays, so it is acceptable to remove them in instances such as this.

SEE ALSO

analyze (2), **read** (2).

VER-144 (error) %s Incorrect naming of port found.

DESCRIPTION

You receive this message because the **read** or **analyze** command has detected an incorrect port name. A missing port name after '.' can cause the problem, as shown in the following example:

```
module test(a, . (b), c);
  input a, b;
  output c;

endmodule
```

WHAT NEXT

Make sure the port name is complete.

SEE ALSO

analyze (2), **read** (2).

VER-145 (error) %s Declarations are supported in named blocks only

DESCRIPTION

This error message occurs because declarations are allowed only in named blocks.

WHAT NEXT

Correct the code by either removing the declarations inside the block, or giving the block a name.

SEE ALSO

analyze(2)
read(2)

VER-146 (warning) %s Time precision is less precise than the

time unit.

DESCRIPTION

This warning message advises you that time precision is usually more precise than the time unit.

WHAT NEXT

This is a warning message only. No action is required on your part.

However, it is best practice to check the code and change the time precision to be more precise than the time unit where necessary.

SEE ALSO

analyze(2)
read(2)

VER-147 (error) %s Instantiation %s has mixed ordered and named port connections

DESCRIPTION

This error message occurs because instantiation is using both ordered port connections and named port connections. Mixed ordered and port connections are not supported.

WHAT NEXT

Change the code to use only ordered or only port connections.

SEE ALSO

analyze(2)
read(2)

VER-148 (error) %s Gate output %s must be a net

DESCRIPTION

This error message occurs when the variable type for gate output is not set to net.

WHAT NEXT

Change the variable type to net in the code.

SEE ALSO

analyze(2)
read(2)

VER-149 (error) %s Symbol %s not included in portlist

DESCRIPTION

This error message occurs when the symbol declared in input and output lists is not included in the port list.

WHAT NEXT

Add the missing input and output lists in the port list to the code.

SEE ALSO

analyze(2)
read(2)

VER-150 (error) %s Net assignment %s found in net declaration list.

DESCRIPTION

You receive this message because the **read** or **analyze** command has detected a net assignment in a net declaration, a construct that the Presto HDL Compiler does not support.

The following is one example that can cause the problem:

```
module test( a, b, c);
  input a, b;
  output c;
  wire d, e=a;

endmodule
```

WHAT NEXT

Check your design for invalid constructs like this and correct them.

SEE ALSO

analyze (2), **read** (2).

VER-151 (warning) %s port %s have inconsistent declarations.

DESCRIPTION

You receive this message because the **read** or **analyze** command has detected inconsistency of the port type.

The following is one example that can cause the problem:

```
   `define N 4

   module m1 (a,b) ;
   input [`N-1:0] a, b ;
   parameter P = `N ;
   wire [`N-1:0] a ;
   wire [P-1:0] b ;
   endmodule
```

This a mismatch for b, because the parameter P could be overridden, so it cannot be assumed to have its default value.

Another example that can cause the problem is:

```
   module m2 (a,b);

   parameter A=2;
   parameter B=A;

   input [A:0] a;
   input [B:0] b;

   wire [B:0] a;
   wire [A:0] b;

   endmodule
```

Even though B has the same default value as A, that value can be overridden.

WHAT NEXT

Use identical expressions in corresponding pairs of port and signal declarations.

analyze (2), **read** (2).

VER-152 (error) %s Vector or memory size mismatch on port %s using last declaration.

DESCRIPTION

You receive this message because the **read** or **analyze** command has detected vector or memory size mismatches.

The following is one example that can cause the problem:

```
   ‘define N 4

   module m1 (a,b) ;
   input [‘N-1:0] a, b ;
   parameter P = ‘N+1 ;
   wire [‘N-1:0] a ;
   wire [P-1:0] b ;
   endmodule
```

This a mismatch for b, because the parameter P’s default value is not the same as ‘N. As a result, the width of array can not be determined.

Another example that can cause the problem is:

```
   module m2 (a,b);

   parameter A=2;
   parameter B=A;

   input [A:0] a;
   input [B:0] b;

   wire [B:0] a;
   wire [A:0] b;

   endmodule

   module top(a, b);
   input [2:0] a;
   output [3:0] b;

   m2 #(.B(3)) inst2(a, b);
   emdmodule
```

Even though B has the same default value as A, that value is overridden
in the module instantiation when design top is evaluated.
As a result, the port a and b in module m2
has mismatched sizes in their declarations.

WHAT NEXT

Use identical expressions in corresponding pairs of port and signal declarations.

analyze (2), **read** (2).

VER-153 (error) %s Port %s occurs more than once in instance %s of module %s.

DESCRIPTION

You see this message because during **read** or **analyze** command activity, the compiler has detected that you have used the same port name more than once in an instantiation, which is not valid.

The following is one example that can cause the problem:

```
module test( a, b, c);
input a, b;
output c;

my_test c1(.p1(a), .p1(b), .p2(c));

endmodule
```

WHAT NEXT

Check your design for duplicate port names and correct them.

SEE ALSO

analyze (2), **read** (2).

VER-154 (error) %s Gate instance with too few ports

DESCRIPTION

This error message occurs when there are not enough ports in the gate instance.

WHAT NEXT

Change the code to use the correct number of ports for the gate instance.

SEE ALSO

analyze(2)
read(2)

VER-155 (warning) %s non constant assignment to specparam %s.

DESCRIPTION

This warning message occurs when a non constant is assigned to the **specparam** variable and may not be accepted by other simulators.

WHAT NEXT

This is a warning message only. No action is required on your part.

However, it is best practice to assign a constant expression to the **specparam** variable.

SEE ALSO

analyze(2)
read(2)

VER-156 (error) %s UDP initialization value %s is not 0, 1, or X.

DESCRIPTION

This error message occurs when the user-defined primitive (UDP) initialization value is not assigned as 0, 1, or X.

WHAT NEXT

Assign 0, 1, or X to the UDP initialization value and run the command again.

SEE ALSO

analyze(2)
read (2)

VER-157 (error) %s UDP initialization variable %s must be

output.

DESCRIPTION

This error message occurs when the user-defined primitive (UDP) initialization variable is not output.

WHAT NEXT

The UDP initialization statement specifies the value of the output port when simulation begins. Use output port as the UDP initialization variable and run the command again.

SEE ALSO

analyze(2)
read(2)

VER-158 (error) %s too few input entries in table specification.

DESCRIPTION

This error message occurs when there are not enough input entries in the table specification. The number of input entries must be equal to the number of input variables.

WHAT NEXT

Modify the table specification, ensuring that the number of input entries is equal to the number of input variables, and then run the command again.

SEE ALSO

analyze(2)
read(2)

VER-159 (error) %s too many input entries in the table specification.

DESCRIPTION

This error message occurs when there are too many input entries in the table specification. The number of input entries must be equal to the number of input

variables.

WHAT NEXT

Modify the table specification, ensuring that the number of input entries is equal to the number of input variables, and then run the command again.

SEE ALSO

analyze(2)
read(2)

VER-160 (error) %s vector declaration %s not supported in UDPs.

DESCRIPTION

This error message occurs because vector declaration is not supported in user-defined primitives (UDPs).

WHAT NEXT

Do not use vector declaration in UDPs, or use the Synopsys compiler directives **translate_off** and **translate_on** to comment it out as shown in the following example.

```
/* synopsys translate_off */
Vector declaration
/* synopsys translate_on */
```

After making corrections, run the command again.

SEE ALSO

analyze(2)
read(2)

VER-161 (error) %s path element %s should be wire.

DESCRIPTION

This error message occurs if the path element is not wire.

WHAT NEXT

Change the specified path element to wire and run the command again.

SEE ALSO

analyze(2)
read(2)

VER-162 (error) %s module path source %s not port.

DESCRIPTION

This error message occurs if the module path source is not port.

WHAT NEXT

Change the module path source to port and run the command again.

SEE ALSO

analyze(2)
read(2)

VER-163 (error) %s module path destination %s not port.

DESCRIPTION

This error message occurs if the module path destination is not port.

WHAT NEXT

Change the module path destination to port and run the command again.

SEE ALSO

analyze(2)
read(2)

VER-164 (error) %s path pulse source %s not defined.

DESCRIPTION

This error message occurs if the path pulse source is not defined.

WHAT NEXT

Define the specified path pulse source and run the command again.

SEE ALSO

analyze(2)
read(2)

VER-165 (error) %s path pulse destination %s is not defined.

DESCRIPTION

This error message occurs if the specified path pulse destination is not defined.

WHAT NEXT

Define a valid path pulse destination and rerun the command.

SEE ALSO

analyze(2)
read(2)

VER-166 (error) %s path pulse source %s is not a port.

DESCRIPTION

This error message occurs when the path pulse source should be a port.

WHAT NEXT

Change the specified path pulse source to an input port and rerun the command.

SEE ALSO

analyze(2)
read(2)

VER-167 (error) %s path pulse destination %s is not a port.

DESCRIPTION

This error message occurs when the path pulse destination should be a port.

WHAT NEXT

Change the specified path pulse destination to an output port and rerun the command.

SEE ALSO

analyze(2)
read(2)

VER-168 (error) %s timing notifier malformed.

DESCRIPTION

This error message occurs when an expression (instead of an identifier) is used as a timing modifier.

WHAT NEXT

Change the timing notifier to use an identifier and rerun the command.

SEE ALSO

analyze(2)
read(2)

VER-169 (error) %s illegal reference event: expressions are not

allowed.

DESCRIPTION

This error message occurs when an expression is used as a reference event. An expression cannot be used as a reference event.

WHAT NEXT

Use a legal reference event and rerun the command.

SEE ALSO

analyze(2)
read(2)

VER-170 (error) %s timing notifier %s should be a reg.

DESCRIPTION

This error message occurs because the timing notifier should be a **reg**.

WHAT NEXT

Correct the timing notifier to use a **reg** and rerun the command.

SEE ALSO

analyze(2)
read(2)

VER-171 (error) %s timing function %s has an incorrect number of parameters.

DESCRIPTION

This error message occurs when the timing function has an incorrect number of parameters.

WHAT NEXT

Modify the timing function so that it has the correct number of parameters and rerun

the command.

SEE ALSO

analyze(2)
read(2)

VER-172 (error) %s wire (%s) is connected to both the input and output of a built-in gate.

DESCRIPTION

This error message occurs when the same wire is connected to both the input and the output of a built-in gate, resulting in combinational feedback.

WHAT NEXT

Modify the design so that the same wire is not connected to both the input and output of the built-in gate, and then run the command again.

SEE ALSO

analyze(2)
read(2)

VER-173 (warning) %s delays for continuous assignment are ignored.

DESCRIPTION

This warning message advises that delays for continuous assignment are ignored in synthesis.

WHAT NEXT

This is a warning message only. No action is required on your part.

However, it is best practice to ensure that the ignored delay is not integral to the functionality of the design.

SEE ALSO

analyze(2)

read(2)

VER-174 (error) %s '%s' is listed more than once in port list.

DESCRIPTION

This error message occurs when the specified port name is used more than once in a port list.

WHAT NEXT

Correct the code to use a port name only once in each port list and then rerun the command.

SEE ALSO

analyze(2)
read(2)

VER-175 (warning) %s Function '%s' should have at least one input argument.

DESCRIPTION

You receive this message because, during **read** or **analyze** command activity, the compiler encountered a function that has no input arguments. The IEEE standard for Verilog (1364-1995) requires that a function have at least one input argument.

For example, the following function would trigger this warning:

```
     function [0:2] f;
       begin
 f = 3'b101;
       end
     endfunction
```

The Presto HDL compiler accepts functions with no arguments; however, many tools do not.

WHAT NEXT

Consider adding at least one input argument to the function in question to conform to IEEE standards.

SEE ALSO

analyze (2), **read** (2), **VER-105** (n).

VER-176 (warning) %s delay controls are ignored for synthesis.

DESCRIPTION

This warning message occurs because your RTL description contains a delay control. Delay controls are ignored for synthesis.

The following is an example of a delay control.

```
module foo;
  ...
  always
  #(5)   // delay control, will be ignored.
     b = a;
endmodule
```

WHAT NEXT

This is a warning message only. No action is required on your part. You can leave the delay controls in your description, but be aware that the delay controls have no meaning for synthesis.

SEE ALSO

analyze(2)
read(2)

VER-177 (error) %s real declarations are not supported by synthesis.

DESCRIPTION

This error message occurs because the real data type is not supported by synthesis.

The following example shows a real declaration.

```
module foo;
  real r;         // data type real not supported by synthesis
endmodule
```

WHAT NEXT

Rewrite your RTL code so that it does not contain real data types. Depending on your specific design, you may need to use integer types instead of real types. Rerun the command after making the changes.

SEE ALSO

analyze(2)
read (2)

VER-178 (error) %s realtime declarations are not supported by synthesis.

DESCRIPTION

This error message occurs because the realtime data type is not supported by synthesis.

The following example shows a realtime declaration.

```
module foo;
  realtime r;       // data type realtime not supported by synthesis
endmodule
```

WHAT NEXT

Realtime variables do not have a meaning in synthesis. Rewrite your RTL code so that it does not use realtime data types. Rerun the command after making the changes.

SEE ALSO

analyze(2)
read(2)

VER-179 (error) %s triand declarations are not supported by synthesis.

DESCRIPTION

This error message occurs because your RTL description contains triand declarations, which are not supported by synthesis.

The following example shows a triand declaration.

```
module foo;
  triand d;
endmodule
```

WHAT NEXT

Rewrite your design so that it does not use triand declarations. Since triand nets imply an and logic function, one solution is to explicitly describe the logic in your RTL code. Rerun the command after making your changes.

SEE ALSO

analyze(2)
read(2)

VER-180 (error) %s trior declarations are not supported by synthesis.

DESCRIPTION

This error message occurs because your RTL description contains trior declarations, which are not supported by synthesis.

The following example shows a trior declaration.

```
module foo;
  trior d;
endmodule
```

WHAT NEXT

Rewrite your design so that it does not use trior declarations. Since trior nets imply an or logic function, one solution is to explicitly describe the logic in the RTL code. Rerun the command after making the changes.

SEE ALSO

analyze(2)
read(2)

VER-181 (error) %s tri0 declarations are not supported by

synthesis.

DESCRIPTION

This error message occurs because your RTL description contains tri0 declarations, which are not supported by synthesis.

The following example shows a tri0 declaration:

```
module foo;
  tri0 d;
endmodule
```

WHAT NEXT

Rewrite your design such that it does not use tri0 declarations and then rerun the command.

SEE ALSO

analyze(2)
read(2)

VER-182 (error) %s tri1 declarations are not supported by synthesis.

DESCRIPTION

This error message occurs because your RTL description contains tri1 declarations, which are not supported by synthesis.

The following example shows a tri1 declaration:

```
module foo;
  tri1 d;
endmodule
```

WHAT NEXT

Rewrite your design so that it does not use tri1 declarations and run the command again.

SEE ALSO

analyze(2)
read(2)

VER-183 (error) %s trireg declarations are not supported by synthesis.

DESCRIPTION

This error message occurs because your RTL description contains trireg declarations, which are not supported by synthesis.

The following example shows a trireg declaration.

```
module foo;
  trireg d;
endmodule
```

WHAT NEXT

Rewrite your design so that it does not use trireg declarations and run the command again.

SEE ALSO

analyze(2)
read(2)

VER-184 (error) %s pulldown declarations are not supported by synthesis.

DESCRIPTION

This error message occurs because your RTL description contains pulldown declarations, which are not supported by synthesis.

The following example shows a pulldown declaration.

```
module foo (c);
  output c;
  ..
  pulldown c1(c);
```

```
endmodule
```

WHAT NEXT

Rewrite your design so that it does not use pulldown declarations and then run the command again.

SEE ALSO

analyze(2)
read(2)

VER-185 (error) %s pullup declarations are not supported by synthesis.

DESCRIPTION

This error message occurs because your RTL description contains pullup declarations, which are not supported by synthesis.

The following example shows a pullup declaration.

```
module foo (c);
  output c;
  ..
  pullup c1(c);
endmodule
```

WHAT NEXT

Rewrite your design so that it does not use pullup declarations and then run the command again.

SEE ALSO

analyze(2)
read(2)

VER-186 (error) %s user-defined primitives (UDPs) are not

supported by synthesis.

DESCRIPTION

This error message occurs because user-defined primitives (UDPs) are not supported by synthesis.

WHAT NEXT

Enclose the UDPs in the following statement and run the command again.

```
‘ifndef SYNTHESIS
  ...
‘endif
```

SEE ALSO

analyze(2)
read(2)

VER-187 (error) %s fork and join constructs are not supported by synthesis.

DESCRIPTION

This error message occurs because fork and join constructs are not supported by synthesis.

WHAT NEXT

Enclose the fork-join construct as follows and rerun the command.

```
‘ifndef SYNTHESIS
 ...
‘endif
```

SEE ALSO

analyze(2)
read(2)

VER-188 (error) %s wait statements are not supported by synthesis.

DESCRIPTION

This error message occurs because wait statements are not supported by synthesis.

WHAT NEXT

Enclose the wait statements as follows and run the command again.

```
`ifndef SYNTHESIS
 ...
`endif
```

SEE ALSO

analyze(2)
read(2)

VER-189 (error) %s case equality (===) is not supported by synthesis.

DESCRIPTION

This error message occurs because case equality (===) is not supported by synthesis.

WHAT NEXT

If the statement containing === is for synthesis, try replacing === with ==, if it does not change the semantics.

If the statement containing === is not for synthesis, enclose the statement as follows.

```
`ifndef SYNTHESIS
 ...
`endif
```

After making your changes, run the command again.

SEE ALSO

analyze(2)
read(2)

VER-190 (error) %s case inequality (!==) is not supported by synthesis.

DESCRIPTION

This error message occurs because case inequality (!==) is not supported by synthesis.

WHAT NEXT

If the statement containing !== is for synthesis, try replacing !== with !=, if it does not change the semantics.

If the statement containing !== is not for synthesis, enclose the statement with the following.

```
‘ifndef SYNTHESIS
 ...
‘endif
```

After making the changes, run the command again.

SEE ALSO

analyze(2)
read(2)

VER-191 (error) %s time declarations are not supported by synthesis.

DESCRIPTION

This error message occurs because time declarations are not supported by synthesis.

WHAT NEXT

Enclose the time declarations with the following and then run the command again.

```
`ifndef SYNTHESIS
 ...
`endif
```

SEE ALSO

analyze(2)
read(2)

VER-192 (warning) %s In initial block, only $power and $retain are supported, other statements are ignored.

DESCRIPTION

This warning message advises you that in initial block, only $power and $retain calls are supported in synthesis. All other statements are not supported in synthesis.

WHAT NEXT

This is a warning message only. No action is required on your part.

However, to avoid receiving this warning message, you can suppress the message, or enclose the initial block with the following.

```
`ifndef SYNTHESIS
 ...
`endif
```

SEE ALSO

analyze(2)
read(2)

VER-193 (error) %s event triggers are not supported.

DESCRIPTION

This error message occurs because event triggers are not supported.

WHAT NEXT

Enclose the event trigger with the following and then rerun the command.

```
`ifndef SYNTHESIS
 ...
`endif
```

SEE ALSO

analyze(2)
read(2)

VER-194 (error) %s Base of subscript operator %s must be a vector.

DESCRIPTION

You receive this message because during **read** or **analyze** command activity, the compiler has detected a subscript operator whose base is not a vector, which is invalid.

The following is one example that can cause the problem:

```
module test(a, b);
input a;
output b;
reg b;

always
  b = a[0];

endmodule
```

WHAT NEXT

Check your design for invalid constructs like this and correct them.

SEE ALSO

analyze (2), **read** (2).

VER-195 (error) %s Illegal digit %c in based number.

DESCRIPTION

You see this message because during **read** or **analyze** activity, the compiler has

detected an invalid digit in a based number.

WHAT NEXT

Check your design for invalid digits in based numbers and correct them.

SEE ALSO

analyze (2), **read** (2).

VER-196 (error) %s Unable to open modfile %s for writing: %s

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-197 (information) %s writing module %s to file %s.

DESCRIPTION

This information message advises you that the tool is writing the specified module to an analyzed file format (.pvl) file.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

analyze(2)
read(2)

VER-198 (error) %s mixed direction ports %s must be nets.

DESCRIPTION

This error message occurs because the code contains mixed direction ports that

should be net-types.

WHAT NEXT

Rewrite code so that the ports with mixed direction are net-types and then rerun the command.

SEE ALSO

analyze(2)
read(2)

VER-199 (error) %s UDP table has invalid edge specification.

DESCRIPTION

This error message occurs when the UDP table has an invalid edge specification, such as (0 0), (1 1) or (X X). The two level symbols in the edge indicator should be different. So (0 0), (1 1) and (X X) are invalid, while (1 0) is valid.

WHAT NEXT

Change the invalid edge indicator to a valid one and run the command again.

VER-200 (error) %s port %s must be declared as input.

DESCRIPTION

This error message occurs because the port must be declared as an input port.

WHAT NEXT

Correct the RTL code to declare the port as input port and then run the command again.

VER-201 (error) %s port %s must be declared as output.

DESCRIPTION

This error message occurs when the port must be declared as an output port.

WHAT NEXT

Correct the RTL code to declare the port as an output port and then run the command again.

VER-202 (error) %s path element %s should be reg or wire.

DESCRIPTION

This error message occurs because the path element should be either reg or wire.

WHAT NEXT

Correct the code to declare the path element as either reg or wire and run the command again.

VER-203 (error) %s pulse limit for path not defined.

DESCRIPTION

This error message occurs because the pulse limit for path is not defined. The valid **specparam** assignment format is one of the following.

```
specparam_identifier = constant_mintypmax_expression

specparam_identifier = pulse_control_specparam
```

The **pulse_control_specparam** format is as follows.

```
$PATHPULSE$... = (reject_limit_value, [, error_limit_value]).
```

You receive this error message when the required **reject_limit_value** is missing.

WHAT NEXT

Add the **reject_limit_value** to the code and then run the command again.

VER-204 (error) %s timing reference event %s not port.

DESCRIPTION

This error message occurs because the timing reference event specified is not port.

WHAT NEXT

Change the timing reference event to port and run the command again.

VER-205 (error) %s timing reference event %s should have edge identifier.

DESCRIPTION

This error message occurs because the timing reference event requires an edge identifier.

WHAT NEXT

Add an edge identifier to the timing reference event and run the command again.

VER-206 (error) %s Too many parameters passed to system task '%s'.

DESCRIPTION

The given system task is passed more arguments than expected.

WHAT NEXT

Find out how which arguments the system task expects. Remove the extraneous arguments from the task call.

VER-207 (error) %s The %s systask parameter must be

writable.

DESCRIPTION

Actual parameters passed to 'output' or 'inout' formal task parameters must be writable (because they are conceptually used as left-hand-side values of assignments). In the following example a constant is passed as an argument to the system function '$random', which indeed expects the argument to be writable:

```
...
r = $random(3);      // error: constant "3" is not writable.
...
```

WHAT NEXT

Make sure the actual argument in question is writable, eg. a 'register'.

VER-208 (warning) %s Register '%s' is the target of both blocking and non-blocking assignments in the same process.

DESCRIPTION

Presto does allow mixing blocking and non-blocking assignments in the same process. However, this coding style can lead to unexpected results and the code may be hard to comprehend.

This warning is informational only. It tells you that targets assigned by both kinds of assignments actually exist.

WHAT NEXT

Make sure the mixture of blocking and non-blocking assignments is really what you intended.

VER-209 (warning) %s Little argument or return value checking implemented for system task or function '%s'.

DESCRIPTION

Argument and return value checking for system tasks and functions is limited. This is a warning message indicating that some errors potentially remain uncaught because of incomplete checking.

WHAT NEXT

The user should check system task or function all carefully to make sure the argument and return value are correct.

VER-210 (error) %s timing reference event %s has wrong edge.

DESCRIPTION

This error message occurs when the wrong edge is specified in the timing reference event.

WHAT NEXT

Specify the edge as either posedge or negedge and then run the command again.

VER-211 (error) %s timing limit malformed.

DESCRIPTION

This error message occurs when the timing limit is malformed because both the event and the normal condition exist in the timing limit. Only one of these conditions is allowed.

WHAT NEXT

Remove either the event or the normal condition and then run the command again.

VER-212 (error) %s timing limit should be positive.

DESCRIPTION

This error message occurs when the timing check limit should be positive.

WHAT NEXT

Specify blocks are not supported in synthesis. Prevent the block from being read by enclosing it in the following compiler directives.

```
‘ifndef SYNTHESIS
 ...
```

```
   `endif
```

After making the changes, run the command again.

SEE ALSO

analyze(2)
read(2)

VER-213 (error) %s timing event malformed.

DESCRIPTION

This error message occurs when the timing check event is malformed.

WHAT NEXT

Specify blocks are not supported in synthesis. Prevent the specify block from being read by enclosing it in the following compiler directives.

```
   `ifndef SYNTHESIS
    ...
   `endif
```

After making the changes, run the command again.

SEE ALSO

analyze(2)
read(2)

VER-214 (error) %s timing notifier %s malformed.

DESCRIPTION

This error message occurs when the optional notifier on the timing check is malformed.

WHAT NEXT

Specify blocks are not supported in synthesis. Prevent the specify block from being read by enclosing it in the following compiler directives.

```
   `ifndef SYNTHESIS
    ...
   `endif
```

After making the changes, run the command again.

SEE ALSO

analyze(2)
read(2)

VER-215 (error) %s timing reference event %s is not input or inout port.

DESCRIPTION

This error message occurs because the reference event for a timing check must be an input or inout port.

WHAT NEXT

Specify blocks are not supported in synthesis. Prevent the specify block from being read by enclosing the block in the following compiler directives.

```
   `ifndef SYNTHESIS
    ...
   `endif
```

After making the changes, run the command again.

SEE ALSO

analyze(2)
read(2)

VER-216 (error) %s %s is not a parameter in module %s

DESCRIPTION

You receive this error message because the name used in module instantiation (component instantiation in VHDL) or DEFPARAM is not a parameter in the specified module.

WHAT NEXT

Change the name in the instantiation to a supported parameter.

SEE ALSO

elaborate (2), **read** (2).

VER-217 (error) %s wrong number of ports in UDP instantiation, not the same as declaration.

DESCRIPTION

This error message occurs when the number of ports in the UDP instantiation is different than the number of ports in the UDP declaration.

WHAT NEXT

UDPs are not supported in synthesis. Modify the code so it does not use UDPs and then rerun the command.

SEE ALSO

analyze(2)
read(2)

VER-219 (error) %s Non-standard replication constant is not supported.

DESCRIPTION

This message is a follow-up to the ELAB-364 warning message, but is issued with "Error" severity, so that violations of the prevailing language standard halt compilation.

WHAT NEXT

Change the relevant code to conform to the level of IEEE Std 1364 selected by hdlin_vrlg_std, or choose a different value for hdlin_repeat_count_0.

VER-220 (error) %s Unresolved hierarchical name %s in

module %s.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-221 (error) %s Module %s to be elaborated is not defined in analyzed source files.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-222 (warning) %s Assignment output %s should be a register.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-223 (warning) %s Task %s is not implemented; statement skipped.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-224 (error) %s Package '%s' has not been analyzed for import or content extraction.

DESCRIPTION

This syntax error issues when a reference to the given package is analyzed before its declaration has been analyzed. Successfully analyzed packages leave a <identifier>.pvk file in DC shell's working directory. This file must be found and read when the package is later referenced for import or to extract its contents. Note that packages may never refer to each other in a cycle of dependence.

WHAT NEXT

Compare the spelling of the package identifier in the reference to its intended declaration. Remove cycles of package reference for which no analyze ordering is possible. Insure that the source file containing the package declaration is analyzed before the the source files that refer to it, or that the package declaration precedes all uses within the same source file. Check DC shell's search paths to insure that packages analyzed by other DC shell sessions can be found by this session. Inspect file and directory search permissions to be certain you can access the package. Check whether an intervening read or analyze command reported a syntax error within a package of the same name, thereby removing the good package's .pvk file.

SEE ALSO

VER-227
analyze(2)
read(2)

VER-225 (warning) %s Recommend parentheses when a reduction-or follows bitwise-or.

DESCRIPTION

A reduction-or operator follows a bitwise-or operator in the Verilog source. This is often a typographical error, when a space is inserted between the two characters in '||' (logical-or), resulting in '| |' (bitwise-or followed by reduction-or). Furthermore, some Verilog tools do not accept this syntax.

WHAT NEXT

If you intended to use a reduction-or, surround it with parentheses to inhibit this warning.

VER-226 (warning) %s Single element concatenation has unsized number.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-227 (error) %s Package '%s' directly or indirectly refers to the current package '%s'.

DESCRIPTION

This syntax error issues within a package if a cyclic reference is made (by scope-extraction operator) to a package whose definition appears to depend upon the package currently being analyzed. This error is reported aggressively, based upon any mention of the current package in the source of the target package or recursively in the packages to which it may refer, regardless of whether an actual cycle of definitional dependence is being formed. Aggressive enforcement prevents VER-224 errors when all the packages are re-analyzed in an empty work directory; i.e. it prevents incremental closure of package reference cycles which would make it impossible to analyze them in an acyclic order.

WHAT NEXT

You might not be extracting from the right package. See the VER-224 help page for suggestions related to this contingency.

Perhaps you chose a name for your package that matches another package name deeper in the supply-chain of the package libraries you are using. Choose a unique package name.

If you are analyzing a older library package that used to work, perhaps the tree of packages upon which it depends has grown to include a package name which collides with this one. Since VER-227 is reported for any name collision in the transitive closure of scope extractions, it could take a while to track down by trial and error. Use 'strings *.pvk | fgrep my-package' or similar search tools to locate uses

of the current package name in the *.pvk (or the package source files) of your project. Once located, the remedy may involve renaming one or the other package, or splitting either one so that the supply trees are disjoint (have no name collisions).

SEE ALSO

VER-224
analyze(2)
read(2)

VER-228 (error) %s Import symbol %s has already been defined.

DESCRIPTION

This error message issues when you attempt to import a name that is already declared in the immediately surrounding scope.

WHAT NEXT

Edit the RTL source to remove or rename whatever has been declared or imported with the same name, or to enclose the import statement and all references to the name in a more local sequential block. Rerun the command.

SEE ALSO

analyze(2)
read(2)

VER-229 (error) %s Value '%s' for enumerated type '%s' should be an integer or sized constant.

DESCRIPTION

You receive this error message when a parameter declaration with an attached 'synopsys enum' pragma declares a parameter whose value is not an integer or sized constant. For example:

```
    parameter [2:0] /* synopsys enum colors */ red = 3'b001,
 green = 3'b010,
 yellow = "YELLOW";
```

The third value in this example would result in this error message.

WHAT NEXT

Modify the design so that all parameters declared as members of an enumerated type are given an integer value or sized constant value.

SEE ALSO

analyze (2), **read** (2).

VER-230 (warning) %s Recommend parentheses when a reduction-and follows bitwise-and.

DESCRIPTION

A reduction-and operator follows a bitwise-and operator in the Verilog source. This is often a typographical error, when a space is inserted between the two ampersands in '&&' (logical-and), resulting in '& &' (bitwise-and followed by reduction-and). Furthermore, some Verilog tools do not accept this syntax.

WHAT NEXT

If you intended to use a reduction-and, surround it with parentheses to inhibit this warning.

VER-231 (warning) %s Range ignored for integer variables.

DESCRIPTION

This is a syntax error. The range will be ignored. In future releases this usage may be disallowed.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-232 (warning) %s Specifying strengths with the 'strength'

keyword is archaic.

DESCRIPTION

This message notifies you that during **read** or **analyze** command activity, the compiler has detected use of 'strength' as a keyword. This word is archaic and may not be supported by some Verilog tools. Synthesis ignores all drive strengths, including one specified in this way.

WHAT NEXT

Avoid the use of the 'strength' keyword.

SEE ALSO

analyze (2), **read** (2).

VER-233 (error) %s Symbol '%s' cannot be used as an argument to the 'disable' statement because it is not a task or named block identifier.

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the compiler has detected an invalid argument to a disable statement. The invalid argument is a symbol that does not refer to a task or named block. In the following example, the symbol *x* does not refer to a named block and will trigger this error.

```
    module test(in1);
       input in1;
       reg x;

       always begin : block
  if(in1)
     disable x;
       end
    endmodule
```

WHAT NEXT

Correct the **disable** statement to refer to a named block or task.

SEE ALSO

analyze (2), **read** (2).

VER-234 (error) %s Strengths highz0 and highz1 cannot be paired together in a strength specification.

DESCRIPTION

You receive this error message because, during **read** or **analyze** command activity, the compiler has detected a strength specification that uses both highz0 and highz1 strengths, which is invalid. Furthermore, all strength specifications are ignored for synthesis.

WHAT NEXT

Correct the strength specification so that it does not use both highz1 and highz0.

SEE ALSO

analyze (2), **read** (2).

VER-235 (error) %s Strength %s for pullup/pulldown must be a strength0.

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the Presto HDL Compiler has detected an invalid strength value in a position that requires a *strength0* value.

Synthesis ignores all strength specifications and does not support pullup and pulldown gates.

WHAT NEXT

Replace the invalid value with a *strength0* value. Acceptable are *supply0*, *strong0*, *pull0*, *weak0*, and *highz0*.

SEE ALSO

analyze (2), **read** (2).

VER-236 (error) %s Strength %s for pullup/pulldown must be a

strength1.

DESCRIPTION

You receive this message because the **read** or **analyze** command has detected an invalid strength value in a position that requires a strength1 value. Synthesis ignores all strength specifications, and does not support pullup and pulldown gates.

WHAT NEXT

Replace the strength value with a strength1 value. Acceptable values are *supply1*, *strong1*, *pull1*, *weak1*, and *highz1*.

SEE ALSO

analyze (2), **read** (2).

VER-237 (error) %s Strength specifications must have strength0 and strength1 components.

DESCRIPTION

You receive this error message because you have specified a strength that does not have one strength0 and one strength1 component. With the exception of 'pullup' and 'pulldown' gates, a strength must have one strength0 and one strength1 component.

Note that all strength specifications are ignored for synthesis.

In the example below, both strengths are from the strength1 category, resulting in this error message.

```
wire x, y, z;
and (weak1,strong1) a1 (x, y, z);
```

WHAT NEXT

Specify a strength from the strength0 category and a strength from the strength1 category.

SEE ALSO

analyze (2), **read** (2).

VER-238 (error) %s Strength declaration in incorrect place.

DESCRIPTION

There is a syntax error in the Verilog source because a strength declaration appears at an incorrect place. Often, this indicates a second strength specification in a gate instantiation.

For example, in the following code segment, the second strength specification will trigger this error because it is not valid Verilog.

```
wire a, b, c, x, y, z;
and (weak1,weak0) a1(a, b, c), (weak1,weak0) a2(x, y, z);
```

WHAT NEXT

Examine the given file and line to determine which strength specification needs to be moved or deleted.

VER-239 (error) %s A wire declaration cannot have a drive strength, at symbol '%s'.

DESCRIPTION

A wire declaration contained a drive strength. A drive strength can only be specified in a net assignment.

WHAT NEXT

Remove the drive strength from the declaration.

VER-240 (warning) %s Strength %s for pullup is redundant.

DESCRIPTION

A 'pullup' gate has only a strength0 specified, and no strength1. This is likely an error, because strength0 specifications are ignored for 'pullup' gates.

Note, however, that 'pullup' gates are not supported for synthesis, and drive strengths are ignored for synthesis.

WHAT NEXT

Check if you intended to specify a strength1 for the pullup gate instead of a strength0. If not, ignore the warning.

VER-241 (warning) %s Strength %s for pulldown is redundant. 0-strength defaulting to strong0.

DESCRIPTION

A 'pulldown' gate has only a strength1 specified, and no strength0. This is likely an error, because strength1 specifications are ignored for 'pulldown' gates.

Note, however, that 'pulldown' gates are not supported for synthesis, and drive strengths are ignored for synthesis.

WHAT NEXT

Check if you intended to specify a strength0 for the pulldown gate instead of a strength1. If not, ignore the warning.

VER-242 (error) %s Enumerated type '%s' needs a size specification.

DESCRIPTION

You receive this error message because a parameter declaration that is being used to declare an enumerated type using the 'synopsys enum' pragma is missing a size specification. The following declaration results in this error message.

```
    parameter /* synopsys enum colors */ red = 3'b001,
 green = 3'b010,
 yellow = 3'b100;
```

WHAT NEXT

Add a size specification to the declaration. The above example can be corrected as follows:

```
    parameter [0:2] /* synopsys enum colors */ red = 3'b001,
       green = 3'b010,
       yellow = 3'b100;
```

SEE ALSO

analyze (2), **read** (2).

VER-244 (error) %s Enumerated type '%s' has not been declared.

DESCRIPTION

You receive this error message because the design has declared a symbol as a member of an enumerated type using the 'synopsys enum' pragma, but the enumerated type has not been declared.

WHAT NEXT

Declare each enumerated type before using it. If you have declared the enumerated type, verify that no errors occurred while processing it.

SEE ALSO

analyze (2), **read** (2).

VER-245 (warning) %s Enumerated type '%s' is not compatible with this declaration.

DESCRIPTION

The design declares a symbol as a member of an enumerated type using the 'synopsys enum' pragma, but the enumerated type has a different underlying type than the symbol. In the following example, the declaration of 'current_state' would trigger this error because its type is not '[0:2]'.

```
parameter [0:2] /* synopsys enum colors */ red = 3'b001,
   green = 3'b010,
   yellow = 3'b100;

reg [0:3] /* synopsys enum colors */ y;
```

WHAT NEXT

If it is typo, correct the type of either the enumerated type declaration or the symbol declaration so that they match. A corrected declaration for 'y' in the above example would change its bounds to '[0:2]':

```
    reg [0:2] /* synopsys enum colors */ y;
```

If user intends to let the symbol and the enumerated type have different type, the user have to make sure that the synthesis behavior is what the user wants.

VER-246 (error) %s Port %s declared as being two different enums.

DESCRIPTION

This error occurs when port has both a port declaration determining its direction, and a register declaration, and has a different enumerated type attached to the two declarations, using the 'synopsys enum' pragma. In the following example, the two declarations of 'y' would cause this error to be issued:

```
    parameter [0:2] /* synopsys enum colors */ red = 3'b001,
       green = 3'b010,
       yellow = 3'b100;
    parameter [0:2] /* synopsys enum numbers */ one = 3'b001,
two = 3'b010;


    output [0:2] /* synopsys enum colors */ y;
    reg [0:2] /* synopsys enum numbers */ y;
```

WHAT NEXT

Choose one enumerated type for the port in question, and correct the declaration.

VER-247 (error) %s Enumerated type '%s' has multiple declarations.

DESCRIPTION

You receive this error message because the same enumerated type is declared twice. The following example illustrates this situation.

```
parameter [0:2] /* synopsys enum colors */ red = 3'b001,
                                           green = 3'b010,
                                           yellow = 3'b100;

parameter [0:4] /* synopsys enum colors */ brown = 5'b001,
                                           black = 5'b010,
                                           gray = 5'b100;
```

WHAT NEXT

Specify a new name for one of the enumerated types.

SEE ALSO

analyze (2), **read** (2).

VER-248 (error) %s Encoding '%s' for '%s' is the wrong size for this enumerated type.

DESCRIPTION

You receive this error message because a value given for an enumerated type has a different size than the enumerated type itself.

In the following example, the state values given are 8 bits, while the enumerated type is declared as 12 bits. This difference will result in this error message.

```
   parameter [11:0] /* synopsys enum states */ state1 = 8'b00000001,
                                                 state2 = 8'b00000010;
```

WHAT NEXT

Modify the values or the type declaration so that they are the same size.

SEE ALSO

analyze (2), **read** (2).

VER-249 (error) %s force output %s must be a register or a net.

DESCRIPTION

This error message occurs because a force statement can only be used to assign to a variable or a net.

WHAT NEXT

Force statements are not supported in synthesis. Enclose the force statement in the following compiler directives to prevent the statement from being read.

```
`ifndef SYNTHESIS
 ...
`endif
```

SEE ALSO

analyze(2)
read(2)

VER-251 (error) %s Expecting a pair of bounds [msb:lsb].

DESCRIPTION

This error message occurs when an array dimension has not specified exactly two bounds. Verilog bit vectors, Verilog memories, and all packed dimensions of SystemVerilog array types must be declared using the subscript values for both the most and the least significant bits as shown in the following example:

```
reg [ most_significant_bit_index : least_significant_bit_index ] packed_vector;
```

WHAT NEXT

Adjust the bounds syntax. Or, in SystemVerilog, move the dimension brackets to the right of the array or type identifier to specify that this dimension should be treated as unpacked.

SEE ALSO

analyze(2)
read(2)

VER-252 (error) %s illegal use of identifier %s.

DESCRIPTION

This error message occurs when an identifier that is defined as a function is being used as a task.

WHAT NEXT

Modify the source code to change the call to a function call and then run the command again.

SEE ALSO

analyze(2)
read(2)

VER-253 (error) %s Illegal reference to memory %s.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-254 (error) %s invalid symbol %s found in activation expression.

DESCRIPTION

This error message occurs when there is an invalid symbol in an activation expression. The symbol in an activation expression should be a net, variable or event.

WHAT NEXT

Change the symbol in the activation expression to a net, variable or event, and then rerun the command.

SEE ALSO

analyze(2)
read(2)

VER-255 (error) %s invalid symbol %s found in expression.

DESCRIPTION

This error message occurs when there is an invalid symbol in an expression. The symbol in an expression should be a net or variable.

WHAT NEXT

Change the symbol in the activation expression to a net or variable and then rerun the command.

SEE ALSO

analyze(2)
read(2)

VER-256 (error) %s illegal part selection has been found.

DESCRIPTION

This error message occurs when an illegal part selection is found. The index of a vector in part selection should be constant valued, and its sign bit cannot be Z or X value.

WHAT NEXT

Check the indexes of vectors in the part selection and correct the offending index. Run the command again.

SEE ALSO

analyze(2)
read(2)

VER-257 (error) %s invalid symbol %s found as system task argument.

DESCRIPTION

This error message occurs when there is an invalid symbol in a system task argument list. The symbol used as a system task argument should be a net, variable, instance, module, event, or function.

WHAT NEXT

Change the symbol in the system task argument list to a net, variable, instance, module, event, or function.

SEE ALSO

analyze(2)
read(2)

VER-258 (error) %s no semicolon at end of module name.

DESCRIPTION

This error message occurs when the semicolon is missing from the end of a module name.

WHAT NEXT

Add a semicolon to the end of the module name and run the command again.

SEE ALSO

analyze(2)
read(2)

VER-259 (error) %s multiple delays found.

DESCRIPTION

This error message occurs when the tool finds multiple delays. Only one delay is allowed.

WHAT NEXT

Correct the code to ensure that there is only one delay, and then run the command again.

SEE ALSO

analyze(2)
read(2)

VER-260 (error) %s symbol %s must be a constant or

parameter.

DESCRIPTION

This error message occurs because the symbol indicated in the error message must be a constant or a parameter, as required by the language.

In the example below, the expression in the generate case statement is required to evaluate to a constant value at elaboration time. The use of an input port in that expression violates this requirement.

```
module m (a);
  input a;

  generate
    case (a)        // error: not constant
    ...
  endgenerate
endmodule
```

WHAT NEXT

Change the specified symbol to a constant or a parameter and then run the command again.

SEE ALSO

analyze(2)
read(2)

VER-261 (error) %s continuous assignment output %s must be a net.

DESCRIPTION

This error message occurs because the output of a continuous assignment must be a net.

WHAT NEXT

Change the output of the continuous assignment to net and then run the command again.

SEE ALSO

analyze(2)

read(2)

VER-262 (error) %s net symbol %s has already been defined.

DESCRIPTION

This error message occurs when the redeclaration of a net symbol is detected. A net can only be declared once.

WHAT NEXT

Remove or rename the nets declared with the same name and then run the command again.

SEE ALSO

analyze(2)
read(2)

VER-263 (error) %s bit- or part-selected destination of a force %s must be a net.

DESCRIPTION

This error message occurs because the bit-selected or part-selected destination of a force statement must be a net and not a variable.

WHAT NEXT

Change the destination of the force statement from a variable to a net and run the command again.

SEE ALSO

analyze(2)
read(2)

VER-264 (error) %s bad hierarchical name (%s).

DESCRIPTION

For Verilog, hierarchical references are not supported for synthesis.

For SystemVerilog, the preceding expression does not evaluate to a struct or union.

WHAT NEXT

For Verilog, exclude the code from synthesis by enclosing the hierarchical reference in the conditional compilation directives shown below.

```
‘ifndef SYNTHESIS
 ...
‘endif
```

For SystemVerilog, if the name is a struct or union member, make sure the preceding expression evaluates to a struct or union. If the name is not a struct or union, follow the instructions in the previous paragraph, and enclose the code in the conditional compilation directives.

VER-265 (error) %s RCMOS switches are not supported.

DESCRIPTION

This error message occurs because RCMOS switches are not supported for synthesis.

WHAT NEXT

Exclude the code from synthesis by enclosing the code in the conditional compilation directives shown below.

```
‘ifndef SYNTHESIS
 ...
‘endif
```

VER-266 (error) %s RNMOS switches are not supported.

DESCRIPTION

This error message occurs because RNMOS switches are not supported for synthesis.

WHAT NEXT

Exclude the code from synthesis by enclosing the code in the conditional compilation directives shown below.

```
‘ifndef SYNTHESIS
 ...
‘endif
```

VER-267 (error) %s RPMOS switches are not supported.

DESCRIPTION

This error message occurs because RPMOS switches are not supported for synthesis.

WHAT NEXT

Exclude the code from synthesis bvy enclosing the code in the conditional compilation directives shown below.

```
‘ifndef SYNTHESIS
 ...
‘endif
```

VER-268 (error) %s RTRAN switches are not supported.

DESCRIPTION

This error message occurs because RTRAN switches are not supported for synthesis.

WHAT NEXT

Exclude the code from synthesis by enclosing the code in the conditional compilation directives shown below.

```
‘ifndef SYNTHESIS
 ...
‘endif
```

VER-269 (error) %s RTRANIF0 switches are not supported.

DESCRIPTION

This error message occurs because RTRANIF0 switches are not supported for synthesis.

WHAT NEXT

Exclude the code from synthesis by enclosing the code in the conditional compilation directives shown below.

```
`ifndef SYNTHESIS
 ...
`endif
```

VER-270 (error) %s RTRANIF1 switches are not supported.

DESCRIPTION

This error message occurs because RTRANIF1 switches are not supported for synthesis.

WHAT NEXT

Exclude the code from synthesis by enclosing the code in the conditional compilation directives shown below.

```
`ifndef SYNTHESIS
 ...
`endif
```

VER-271 (error) %s TRAN switches are not supported.

DESCRIPTION

This error message occurs because TRAN switches are not supported for synthesis.

WHAT NEXT

Exclude the code from synthesis by enclosing the code in the following conditional compilation directives.

```
‘ifndef SYNTHESIS
 ...
‘endif
```

SEE ALSO

analyze(2)

VER-272 (error) %s TRANIF0 switches are not supported.

DESCRIPTION

This error message occurs because TRANIF0 switches are not supported for synthesis.

WHAT NEXT

Exclude the code from synthesis by enclosing the code in the following conditional compilation directives

```
‘ifndef SYNTHESIS
 ...
‘endif
```

SEE ALSO

analyze(2)

VER-273 (error) %s TRANIF1 switches are not supported.

DESCRIPTION

This error message occurs because TRANIF1 switches are not supported for synthesis.

WHAT NEXT

Exclude the code from synthesis by enclosing the code in the following conditional compilation directives

```
‘ifndef SYNTHESIS
 ...
‘endif
```

SEE ALSO

analyze(2)

VER-274 (warning) %s Unsupported system task '%s' will be ignored for synthesis.

DESCRIPTION

Many system tasks are used only for simulation or testbench purposes; they are not supported for synthesis, and are ignored. This warning alerts you that your design contains an unsupported system task (or unsupported system function whose result is discarded).

WHAT NEXT

If your design functions correctly without the system task, then no action is needed.

SEE ALSO

analyze (2), **read** (2).

VER-275 (error) %s User-defined primitives (UDP's) are not supported.

DESCRIPTION

User-defined primitives (UDP's) are not supported.

WHAT NEXT

Change your source file to remove UDPs or enclose them with translate on and translate off, or enclose them with `ifndef SYNTHESIS ... `endif.

SEE ALSO

analyze (2), **read** (2).

VER-276 (error) %s Specify blocks are not supported.

DESCRIPTION

This error message occurs because specify blocks are not supported for synthesis.

WHAT NEXT

Exclude the specify blocks from the synthesis source code by enclosing the blocks in conditional compilation directives as shown below.

```
‘ifndef SYNTHESIS
   specify
      ...      /* specparams that interfere with synthesis */
   endspecify
‘endif
```

VER-277 (warning) %s Charge strengths are ignored.

DESCRIPTION

Charge strengths are ignored for synthesis.

WHAT NEXT

No further action required.

VER-278 (error) %s Array bounds must be of integer type.

DESCRIPTION

You receive this error message because you have not provided the correct value for array bounds. For synthesis, array bounds must be of integer type.

EXAMPLE

The following erroneous example tries to declare an array with a float value as an array bound:

```
...
reg [3.0:0] r;   /* ERROR: ’3.0’ is not an integer bound */
...
```

WHAT NEXT

Correct the values of the array bounds in your design so that they are expressed as integers.

VER-279 (error) %s Syntax error in parameter value list at or near token '%s' (string position %d).

DESCRIPTION

This error message occurs when there is a syntax error in a parameter value list given by the **elaborate** command **-parameters** argument.

WHAT NEXT

Correct the syntax error in the parameter value list and then run the **elaborate** command again.

See the man page for the **elaborate** command for information on the accepted parameter list syntax.

SEE ALSO

elaborate(2)

VER-280 (warning) %s In UPF shell mode, the RTL power construct $isolate, $power and $retain are ignored.

DESCRIPTION

This warning message advises you that in UPF mode, the $isolate, $power and $retain statements are ignored.

WHAT NEXT

This is a only a warning message. No action is required.

However, to prevent this warning message, remove the $isolate, $power and $retain power constructs from the RTL code.

VER-281 (warning) %s The statements in initial blocks are

ignored.

DESCRIPTION

This warning message advises you that initial blocks are not supported in synthesis.

WHAT NEXT

This is a warning message only. No action is required on your part.

However, to avoid receiving this warning message, you can enclose the initial block with the following:

```
‘ifndef SYNTHESIS
 ...
‘endif
```

SEE ALSO

analyze(2)
read(2)

VER-282 (warning) All isolation_upf and retention_upf pragmas are ignored.

DESCRIPTION

This warning message advises you that all isolation_upf and retention_upf pragmas are ignored.

WHAT NEXT

This is only a warning message. No action is required.

However, to prevent this warning message, remove the isolation_upf and retention_upf pragmas from input Verilog.

SEE ALSO

read(2)

VER-286 (warning) %s ’event’ declarations are not supported by

synthesis.

DESCRIPTION

The Verilog ’event’ declaration is not supported for synthesis.

WHAT NEXT

Rewrite your design so that it does not use the ’event’ declaration.

VER-287 (error) %s In UPF shell mode, the RTL power construct $isolate, $power and $retain are not supported.

DESCRIPTION

This error message advises you that in UPF shell mode, the $isolate, $power and $retain statements are not supported.

WHAT NEXT

Remove the specified line of code which contains the $isolate, $power or $retain constructs, and correct the design correspondingly. Or, you may set hdlin_upf_allow_legacy_construct to true to let the tool strip off the logic for you.

VER-288 (error) %s Block name symbol %s already defined.

DESCRIPTION

This error message occurs when the name used for the block label has been previously used as an object name or a block label.

For example:

```
module test (input in, output reg out1, out2);
always @(in) begin:BLK
  out1 = in;
end
always @(in) begin:BLK
  out2 = in;
end
endmodule
```

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-289 (error) %s Instance name symbol %s already defined.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-290 (error) %s Error in edge control specifier.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-291 (error) %s Event symbol %s already defined.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE std 1364.

VER-292 (error) %s Unable to open file ‘%s’: %s.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-293 (error) %s ‘%s’ is not a regular file.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-294 (error) %s Syntax error at or near token ’%s’%s.

DESCRIPTION

You receive this error message because your code contains a syntax error or there’s a syntax error in a /* Synopsys */ comment.

WHAT NEXT

Review your code and make appropriate corrections.

VER-295 (error) %s CMOS switches are not supported.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-296 (error) %s NMOS switches are not supported.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-297 (error) %s PMOS switches are not supported.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-298 (warning) %s Keyword vectored is ignored.

DESCRIPTION

This warning message advises you that **vectored** is an optional advisory keyword. Presto warns about IEEE-1364 conforming uses of this net accessibility specification, but it is otherwise ignored for synthesis.

The following example shows the declaration of a vectored net. Since Presto ignores the keyword **vectored**, the effect is the same as if the keyword had been omitted.

```
...
wire vectored [1:0] x;
...
```

WHAT NEXT

This is a warning message only. No action is required on your part.

VER-299 (error) %s Illegal use of event '%s' as module connection.

DESCRIPTION

You receive this message because the **read** or **elaborate** command detects an event in a module connection list. Events cannot be module connections in a module instantiation statement.

The IEEE 1364 Standard defines the term "module connection" as an element connected to a port of the instantiated module. Expressions in a parenthesized list in a module instantiation statement are valid module connections.

The following example shows an invalid attempt to use an event as a module connection:

```
event e;
...
SUBMODULE my_submodule(e);  /* error: event used as module connection */
```

WHAT NEXT

Determine the original intent of the module connection and replace the event with an element that correctly connects to a module.

analyze (2), **read** (2).

VER-300 (error) %s Illegal attempt to declare hierarchical reference '%s'.

DESCRIPTION

Hierarchical names are illegal in contexts where they would introduce or declare a new name in the current scope.

For example it is illegal to do a cross module declaration, as shown in the following code fragment:

```
reg a.b; /* illegal to declare a register in another scope */
```

WHAT NEXT

Check if this is a typo, where a period should be a comma. Check that the names in the hierarchical reference are properly declared and accessible in the current scope. Reduce cross-module references by adding explicit ports to carry signals between modules.

VER-301 (error) %s Specparam symbol '%s' already defined.

DESCRIPTION

You receive this error message if you attempt to redefine an already defined symbol as a specification parameter.

EXAMPLE

The following example demonstrates a case that results in this error message.

```
reg x;                    /* declaration of 'x' as a register */
...
specify
  specparam x = 1;      /* illegal attempt to redeclare 'x' */
  ...
endspecify
```

WHAT NEXT

Rename the original symbol or the specification parameter and all corresponding uses so that there is no conflict.

SEE ALSO

analyze (2), **read** (2).

VER-302 (warning) %s Pragma '%s' for object '%s' will be ignored because the object could not be found.

DESCRIPTION

A pragma is a compiler directive in the source code. This warning appears because, during **read** or **analyze** command activity, the symbol used in an *infer_multibit* pragma is not declared in the source code.

WHAT NEXT

Possibly you misspelled the name of the symbol or the symbol you used exists only in an old version of the source code and is no longer valid. Correct the symbol name or consider removing the pragma.

SEE ALSO

analyze (2), **read** (2).

VER-305 (warning) %s Drive strength specifications for gate instantiations are ignored.

DESCRIPTION

You receive this warning message because a drive strength specification has been found in a gate instantiation statement. Drive strength specifications have no meaning for synthesis and are ignored.

EXAMPLE

The following example shows a gate instantiation statement containing a drive strength specification, which results in this warning message.

```
not (highz1, strong0) n1 (a,y);  /* highz1 and strong0 are drive strengths */
```

WHAT NEXT

The drive strength specification is ignored during synthesis. If the code is intended for synthesis purposes only, consider removing the drive strength specification.

SEE ALSO

analyze (2), **read** (2).

VER-306 (warning) %s Drive strength specification for tri-state gate instantiation is ignored.

DESCRIPTION

You receive this warning message because a drive strength specification has been found in a tristate gate instantiation statement. Drive strength specifications have

no meaning for synthesis and are ignored.

EXAMPLE

The following example shows a gate instantiation statement containing a drive strength specification that results in this warning message.

```
  bufif (highz1, strong0) b1 (y,a,c);  /* highz1 and strong0 are drive strengths */
```

WHAT NEXT

If the code is intended for synthesis purposes only, consider removing the drive strength specification.

SEE ALSO

analyze (2), **read** (2).

VER-307 (warning) %s Drive strength specification for pull gate instantiation is ignored.

DESCRIPTION

You receive this warning message because a drive strength specification has been found in a pull gate instantiation statement. Be aware that drive strength specifications have no meaning for synthesis and are ignored.

EXAMPLE

The following example shows a gate instantiation statement containing a drive strength specification that results in this warning message.

```
 pullup (strong1) p1 (y);    /* highz1 and strong0 are drive strengths */
```

WHAT NEXT

If the code is intended for synthesis purposes only, consider removing the drive strength specification.

SEE ALSO

analyze (2), **read** (2).

VER-308 (warning) %s Drive strength specification for module instantiation is ignored.

DESCRIPTION

You receive this warning message because a drive strength specification has been found in a module instantiation statement. Drive strength specifications have no meaning for synthesis and are ignored.

EXAMPLE

The following example shows a module instantiation statement containing a drive strength specification that results in this warning message.

```
...
down (strong1, strong0) d (a,y);  /* module instantiation with drive strengths */
...
```

WHAT NEXT

If the code is intended for synthesis purposes only, consider removing the drive strength specification.

SEE ALSO

analyze (2), **read** (2).

VER-309 (warning) %s Drive strength specification for continuous assignment is ignored.

DESCRIPTION

You receive this warning message because a drive strength specification has been found in a continuous assignment statement. Be aware that the drive strength specifications have no meaning for synthesis and are ignored.

EXAMPLE

The following example shows a continuous assignment statement containing a drive strength specification that results in this warning message.

```
...
assign (strong1, strong0) y = a; /* containing assignment with drive strengths */
...
```

WHAT NEXT

If the code is intended for synthesis purposes only, consider removing the drive strength specification.

SEE ALSO

analyze (2), **read** (2).

VER-310 (warning) %s Keyword scalared is ignored.

DESCRIPTION

This warning message advises you that **scalared** is an optional advisory keyword. Presto warns about IEEE-1364 conforming uses of this net accessibility specification, but it is otherwise ignored for synthesis.

The following example shows the declaration of a scalared net. Since Presto ignores the keyword **scalared**, the effect is the same as if the keyword had been omitted.

```
...
wire scalared [1:0] x;
...
```

WHAT NEXT

This is a warning message only. No action is required on your part.

VER-311 (warning) %s Parameter range specification is new feature of Verilog 2001. Synthesis and non-Verilog 2001 compatible simulation may have different results.

DESCRIPTION

This warning appears during **read** or **analyze** command activity to let you know that some simulators might ignore the range specification in the parameter declaration of your design and expand the parameter to 32 bits. It is thus possible that the circuit synthesized by the Presto HDL Compiler and the non-Verilog 2001 compatible simulation results will not match.

In the following example, the value of *out* from the simulator might be 0, but Presto HDL Compiler gives the value 16.

Verilog

```
output [4:0] out;
parameter [3:0] a = 0;

assign out = {1'b1, a};
```

In the following example, the value of *a* from the simulator might be 10, but the Presto HDL Compiler gives the value 2. The bit on the left is ignored.

Verilog

```
parameter [2:0] a = 4'b1010;
```

WHAT NEXT

Check accordance between synthesis and simulation at the location in the source code that refers to the bit width of the parameter.

SEE ALSO

analyze (2), **read** (2).

VER-312 (error) %s Cannot write architecture file %s: %s.

DESCRIPTION

You receive this error when, during a **read** or **analyze** command, the Presto HDL compiler cannot open or write a file describing the source language (and for VHDL, the architecture) of the module or entity being analyzed.

WHAT NEXT

Make sure that the output directory is writable.

SEE ALSO

analyze (2), **read** (2).

VER-313 (warning) %s Verilog 'signed' data types are present; Verilog 'integer' data types become signed as well.

DESCRIPTION

You receive this warning when you use the Verilog 2000 'signed' keyword to declare signed data types, using the Presto HDL Compiler in release 2000.11-1 and subsequent

releases. Using signed types causes signed logic for 'integer' types to be generated, as well (that is, any arithmetic using the variable of type integer will generate signed GTECH components in your netlist.)

Ordinarily the interpretation of integers as signed or unsigned data types in generated logic is controlled by the variable hdlin_unsigned_integers. However, when any variables in your design are declared using the 'signed' keyword, the variable is ignored, and integers are always interpreted as signed quantities.

This is a departure from releases of Presto prior to 2000.11-1, and from the default HDL Compiler in all previous releases. In earlier releases, the integer data type was not considered a hardware data type, but instead was intended only for compile-time calculations, such as counting loop iterations. As such, the integer data type generated unsigned logic.

This change reflects a reclassification of the integer data type under the Synopsys synthesis subset and conforms more closely to the IEEE Standard 1364-1995.

If you use integer data types to produce logic in your design, you might see a difference between designs compiled with earlier Presto HDL Compiler or HDL Compiler versions, as compared to Presto HDL Compiler version 2000.11-1 and subsequent versions. Make sure that expressions involving integer data types that produce logic are correctly computed when using signed arithmetic.

WHAT NEXT

Ensure that your use of the integer data type is consistent with signed arithmetic.

SEE ALSO

hdlin_unsigned_integers (3), **analyze** (2), **read** (2).

VER-314 (warning) %s Starting with the 2000.11-1 release, the Presto Verilog reader treats Verilog 'integer' types as signed; synthesized result may not match earlier versions of HDL Compiler.

DESCRIPTION

You receive this warning when you use the Verilog 'integer' data type, when compiling your design with the Presto HDL Compiler, in release 2000.11-1 and subsequent releases.

By default, when expressions involving integer variables produce logic in the netlist, signed logic for will be generated (that is, any arithmetic using the variable of type integer will generate signed GTECH components in your netlist.)

This is a departure from Presto HDL Compiler in releases before 2000.11-1 and from the default HDL Compiler in all releases before 2001.08. In those earlier releases, the integer data type was not considered a hardware data type, but instead was intended only for compile-time calculations, such as counting loop iterations. As such, the integer data type generated unsigned logic.

This change reflects a reclassification of the integer data type under the Synopsys synthesis subset and conforms more closely to the IEEE Standard 1364-2001.

If you use integer data types to produce logic in your design, make sure that expressions involving integer data types that produce logic are correctly computed when using signed arithmetic.

The interpretation of integers as signed or unsigned data types in generated logic is controlled by the variable hdlin_unsigned_integers. However, when any variables in your design are declared using the 'signed' keyword, the variable is ignored, and integers are always interpreted as signed quantities.

WHAT NEXT

Ensure that your use of the integer data type is consistent with signed arithmetic. If your design requires unsigned arithmetic generated by integer datatypes, and your design does not use Verilog 2000 'signed' types, consider setting hdlin_unsigned_integers to true.

SEE ALSO

hdlin_unsigned_integers (3), **analyze** (2), **read** (2).

VER-315 (warning) %s Module '%s' was renamed to '%s' with architecture '%s'.

DESCRIPTION

You receive this warning because the named module contains the special separator string "__" and was thus renamed to include the module and architecture. This warning informs you of the situation and this man page instructs you what to do if you did *not* intend the renaming.

When a Verilog module name contains the special separator string "__" (two underscores), and the **hdlin_module_arch_name_splitting** variable is set to *true*, Presto HDL Compiler interprets the module name as specifying both a module and a specific architecture or implementation for that module. The portion of the original module name before the separator string becomes the new module name, and the portion after becomes the architecture.

For example, a module named "mod__impl" would be renamed to "mod" and marked as having architecture "impl".

If the variable **hdlin_module_arch_name_splitting** is set to *false*, this renaming never occurs and modules always retain their original names. If it is set to *true*, the "__" is used to divide the module name into module and architecture, as described above.

This capability exists primarily to allow the creation of synthetic libraries using Verilog, with multiple architectures per module.

WHAT NEXT

If you did not intend to specify a module and architecture pair separated by "__", either set **hdlin_module_arch_name_splitting** to *false* or rename your module so that it doesn't contain the separator string.

If you intended to imply a specific architecture, no further action on your part is required.

SEE ALSO

analyze (2), **read** (2); **hdlin_module_arch_name_splitting** (3).

VER-316 (error) %s The aggregated port expression in the declaration for port '%s' has a mixed direction.

DESCRIPTION

This error indicates that the compiler has found a port declaration with an aggregated port expression that has a mixed direction.

Modules with mixed-direction port declarations are not supported in synthesis.

In Verilog, port directions are not declared directly, but are instead implied by the directions declared for port identifiers within port expressions.

When the port expression is a concatenation and the port identifiers within it are declared with different directions, the port has a mixed direction.

```
module mixed_direction (.p({a,e})) ;
input a;
output e;
not(e,a);
endmodule
```

WHAT NEXT

If you did not intend to specify a port with a mixed direction, change the expression in the port declaration or change the directions of some the identifiers it uses. If you intended to specify a port expression with mixed direction, split

the port into smaller ports that do not have mixed directions.

SEE ALSO

analyze (2), **read** (2).

VER-318 (warning) %s %s to %s %s occurs.

DESCRIPTION

You receive this warning message when the Presto HDL Compiler performs one of the following conversions or assignments:

- Implicitly converts an unsigned expression to a signed expression
- Implicitly converts a signed expression to an unsigned expression
- Assigns an unsigned right side to a signed left side
- Assigns a signed right side to an unsigned left side.

The following is an example of implicit signed/unsigned conversion:

```
reg signed [3:0] a;
   reg [7:0] c;

   a = 4'sb1010;
   c = a+7'b0101011;
```

According to Verilog standard 2001, the tool converts the signed operand *a* to an unsigned value in the second assignment. The *a* operand is not sign-extended and the Presto HDL Compiler issues the following warning message:

```
   signed to unsigned conversion occurs
```

However, if the operand being converted is a constant with leading zeros (in this case, converting between signed and unsigned does not change logic), the Presto HDL Compiler does not issue a warning. For example:

```
   c = 5'sb01101+7'b0101011;
```

The first operand on the right side is implicitly converted to an unsigned value, but no warning is issued since the msb of the operand is 0.

Explicit type casting might also disable warnings about conversions. In the example

above, Presto HDL Compiler does not issue any warnings if *a* is coerced to be unsigned; for example, by assigning *c* as follows:

```
c = $unsigned(a)+7'b0101011;
```

The following is an example of a signed/unsigned assignment:

```
reg [7:0] a;

a = 4'sb1010;
```

The Presto HDL Compiler issues the following warning message:

```
signed to unsigned assignment occurs
```

Although the left side is unsigned, the right side is still sign-extended, so after the assignment, *a* equals 8'b11111010.

WHAT NEXT

This is a warning message only. No action is required on your part if you want to have signed/unsigned conversions or assignments. However, you can avoid implicit conversion or signed/unsigned assignments by changing your Verilog code.

SEE ALSO

elaborate(2)
read(2)

VER-319 (error) %s defparam to local parameter '%s' inside generate block not supported.

DESCRIPTION

You receive this error message because parameter overwrites inside *generate* blocks to local parameters are not supported by synthesis.

```
module m ();
  parameter p = 1;
  generate
    defparam p = 2;     // not allowed
  endgenerate
endmodule
```

WHAT NEXT

Rewrite your source file, removing the parameter overwrites inside the generate blocks to local parameters, and then run the command again.

SEE ALSO

elaborate (2), **read** (2).

VER-320 (warning) %s right hand side of defparam statement should only contain constants or references to parameters.

DESCRIPTION

You receive this warning message because according to the Verilog standard, the right side of a defparam statement should be a constant expression involving only numbers and references to parameters.

```
module m ();
  genvar i;

  generate
    for (i=0; i<10; i=i+1) begin : B1
      defparam p = i;   // warning: genvar is not allowed on the RHS
    end;
  endgenerate
endmodule
```

WHAT NEXT

No action is required on your part.

However, to strictly comply with the language standard, you should rewrite your code to use only constants or references to parameters on the right side of defparam statements.

You can avoid the warning message by changing the source file so that the defparam statements conform to the Verilog standard.

SEE ALSO

elaborate (2), **read** (2).

VER-321 (error) %s genvar '%s' used outside generate loop.

DESCRIPTION

You receive this error message because a genvar can only be used inside the generate loop that uses the genvar as a loop index variable. Using the genvar outside of this loop is not permitted.

```
module m ();
  genvar i;

  generate
    for (i=0; i<10; i=i+1) begin : B1
    ...
    end;
    assign y = i;   // use pf genvar outside generate loop.
  endgenerate
endmodule
```

WHAT NEXT

Change your source file so that all genvars are only used inside the generate loop that uses the genvar as a loop index variable, and then run the command again.

SEE ALSO

elaborate (2), **read** (2).

VER-322 (error) %s A packed object cannot contain unpacked data: %s.

DESCRIPTION

This error message occurs because a structure or union declared as packed cannot contain an unpacked member; an array with packed dimensions cannot have elements whose type is unpacked; or a Verilog-style concatenation cannot include unpacked ingredients.

```
struct packed {
  struct {
  } a;       // error: unpacked structure inside packed structure
} b;
struct { byte car, cdr } cons;       // This unpacked type cannot be:
cons [12] register_file;             // on a packed dimension, or
register_file = {12{ cons'{0,0} }};  // in a packed concatenation.
```

WHAT NEXT

Change your source file so that either the element (and all of its subelements) are declared as packed, or else declare all outer structs and/or unions as unpacked, and write outer array dimensions to the right of their variable name (which connotes an unpacked data arrangement).

In concatenations, you can rewrite the code to treat unpacked data in a separate structure. If this is not possible, then cast the concatenation to the appropriate unpacked type. As a final option, you can cast the offending element to a packed type of the correct width.

SEE ALSO

elaborate(2)
read(2)

VER-323 (error) %s Trying to redeclare typename '%s'.

DESCRIPTION

You receive this error message because an identifier declared as a typename can't be redeclared later.

```
typedef logic SPOCK;
...
reg SPOCK     // error: 'SPOCK' already declared as a typename
```

WHAT NEXT

Change your source file by renaming either the typename or the identifier causing the name clash to a new name.

SEE ALSO

elaborate (2), **read** (2).

VER-324 (error) %s Illegal slice name.

DESCRIPTION

You receive this error message because you are applying more than one slice to an array or the slice is not the last element in the select chain.

The example below demonstrates legal and illegal situations.

```
  reg [0:3] [4:7] [8:11] a;

  ... = a[1:2];      // legal: only one slice at the end of the select chain
  ... = a[2][5:6];   // legal: only one slice at the end of the select chain

  ... = a[1:2][4];   // illegal: slice not last element of select chain
  ... = a[1:2]5:6];  // illegal: more than one slice in select chain
```

WHAT NEXT

Change your source file to use select chains with only one slice per select chain and make sure the slice is always the last element in the select chain.

SEE ALSO

elaborate (2), **read** (2).

VER-325 (error) %s This structure constructor is missing a value for member '%s'.

DESCRIPTION

This error message occurs because structure construction expressions must specify a value for every member of the structure. The cited member was not mentioned in the list of member:value specifications, and none of the type:value or default:value specifications could be applied successfully.

WHAT NEXT

Check the nesting of curly braces around this source line. Check the declaration of the structure type(s) and typedef names involved. After making the necessary changes, run the command again.

VER-326 (error) %s conditionally generated declaration of port '%s'.

DESCRIPTION

You receive this error message because the declaration of a port is conditionally generated. All 3 port declarations in the following example are illegal because they are either fully or partly contained in a conditional generate region.

```
module m (a, b, c);
 reg c;
```

```
 output b;

 generate
  if (...)
   output a;
   reg a;
   reg b;
   output c;
 endgenerate
endmodule
```

WHAT NEXT

Check the nesting of curly braces around this source line. Check the declaration of the structure type(s) and typedef names involved.

VER-327 (error) %s Non-constant index expression on left hand side of continuous assignment '%s'.

DESCRIPTION

You receive this error message because the left hand side of a continuous assignment contains a non-constant index expression. This is not legal Verilog.

```
module m (a, b);
 reg [0:7] a;
 integer b;

 assign a[b] = 1'b0;    // error, 'b' is non-constant

endmodule
```

WHAT NEXT

Rewrite the design such that all left hand sides of continuous assignments contain only constant index expressions. Depending on the context one way of achieving this is to turn the continuous assignment into a nonblocking assignment inside a combinational always block.

VER-328 (error) %s Syntax error on apparent Verilog 2001 construct.

DESCRIPTION

You receive this error message because hdlin_vrlg_std has been set to 1995, but the

Verilog code apparently contains a Verilog 2001 construct.

WHAT NEXT

Either rewrite the code so that it does not use Verilog 2001 constructs or do not override the default value of hdlin_vrlg_std.

VER-329 (warning) %s Parameter keyword used in local parameter declaration.

DESCRIPTION

You receive this warning message because the ’parameter’ keyword has been used in a local parameter declaration.

According to the 2nd paragraph of 3.11.1 in the Verilog-2001 LRM, "If any param_assignments appear in a module_parameter_port_list, then any param_assignments that appear in the module become local parameters and shall not be overridden by any method." For example, because p2 in the following is a local parameter:

```
module bottom #(parameter p1 = 13) (output [31:0] o) ;
parameter p2 = 17 ;
assign o = p1 + p2 ;
endmodule
```

an instantiation that attempted to override it would be disallowed:

```
module top (output [31:0] o) ;
bottom #(.p2(29)) bot ( o ) ;
endmodule
```

In SystemVerilog there are several additional scope contexts in which the parameter keyword is a synonym for the localparam keyword. According to 6.3.2 in the IEEE SystemVerilog LRM, "Unlike nonlocal parameters, local parameters can be declared in a generate block, in a package, or in a compilation-unit scope. In these contexts, the parameter keyword can be used as a synonym for the localparam keyword."

WHAT NEXT

If there is no need to override the parameters in a module or interface declaration either do nothing or use the ’localparam’ keyword instead. If there is a need to override the parameter in this declaration, declare them in the list_of_parameter_declarations instead.

The parameters in a package, compilation-unit scope or generate block are always local parameters and cannot be overridden.

VER-330 (warning) %s No operator for pragma label %s

DESCRIPTION

In the statement, there is no operator to which the label could be applied.

Verilog

```
a = b ; // synopsys label my_oper
```

A label can be associated only with an infix operator, such as +, or with a task or function call.

WHAT NEXT

Modify the Verilog source code to remove the pragma or to introduce an operator for the label.

SEE ALSO

analyze (2), **read** (2).

VER-331 (warning) %s Redeclaration of port '%s'.

DESCRIPTION

You receive this message because, during **analyze** or **read** command activity, the Presto HDL Compiler has detected that a port previously declared using an ANSI-style port declaration (12.3.4 in the Verilog 2001 LRM) has been redeclared in the body of the module.

Following is an example that illustrates this type of problem:

```
module m ( input a, output b);
 wire a; // redeclaration of input port
 reg b; // redeclaration of ouput port
endmodule
```

WHAT NEXT

Remove the redeclaration and move any additional information it contains into the ANSI-style port declaration.

SEE ALSO

analyze (2), **read** (2).

VER-332 (warning) %s The ’%s’ pragma is ignored when applied to ’if’ statements.

DESCRIPTION

This warning message occurs during **analyze** or **read** command activity when the compiler finds a full_case or parallel_case pragma applied to an "if" statement.

The full_case or parallel_case pragmas are only effective when applied to case statements.

The infer_mux pragma is meaningful when applied to "if" statements.

WHAT NEXT

Remove any full_case or parallel_case pragmas from "if" statements in your design.

SEE ALSO

analyze(2)
read(2)

VER-333 (error) %s Widths of ports on ’tran’ instantiation are inconsistent.

DESCRIPTION

This error message occurs when a Verilog "tran" instance has an input and output port that have different widths.

The following module produces this error message because the widths of "a" and "b" are not equal.

```
module E (a, b);

  input [2:0] a;
  output [3:0] b;

  tran (a, b);
```

```
endmodule
```

WHAT NEXT

Correct the widths of the ports so that they are consistent and then invoke the compiler again.

SEE ALSO

elaborate(2)

VER-334 (error) %s Width of interface port is not consistent with width of expression.

DESCRIPTION

This error message occurs when the design being compiled contains an interface instantiation in which the declared width of the interface’s modport does not match the width of the connection in the interface instantiation.

WHAT NEXT

Correct the width of the ports so that they are consistent and then invoke the compiler again.

SEE ALSO

elaborate(2)

VER-335 (error) %s ’defparam’ is not supported inside generate blocks

DESCRIPTION

You receive this error message when running the **read** or the **elaborate** command if your design contains a **defparam** statement within a **generate** block.

Presto HDL Compiler does not support **defparam** parameter value override assignments within **generate** blocks.

The following example demonstrates a supported coding style for parameter value override assignments.

```
module sub (...);
```

```
   PARAMETER P1 = 10;
   ...
endmodule


module top (...);

  ...
  generate if(1) begin: blk
    sub u1 (...) ;           //error: defparams not supported
    defparam u1.P1 = 20;     //       inside generate blocks.
  end

  ...

  generate if(1) begin: blk2
    sub #(20) u1 (...) ;    //supported method to assign parameter
  end                       //value overrides

  ...
endmodule
```

WHAT NEXT

Rewrite the parameter value assignment as shown in the example above.

SEE ALSO

elaborate(2)
read(2)

VER-336 (warning) %s 'defparam' that accesses a hierarchical name may be ignored.

DESCRIPTION

The **read** or the **analyze** command issues this message when your design contains a **defparam** statement that modifies a parameter through hierarchical reference.

Presto HDL Compiler ignores **defparam** overrides of parameters inside functions, tasks or named blocks. Since the actual target is not known at the point where the defparam statement is analyzed, this message is just a warning and may be a false negative indication.

WHAT NEXT

You may ignore this message if the defparam overrides a parameter which will later be declared in the top level of a module instantiated from within the current design. Otherwise, recode the design and try again.

SEE ALSO

elaborate(2)
read(2)

VER-337 (error) %s PARAMETER assignment statement has same LHS and RHS '%s'.

DESCRIPTION

This error message occurs when the PARAMETER assignment statement has the same LHS and RHS. For example: parameter P0 = P0.

WHAT NEXT

Correct the PARAMETER assignment statement and make sure RHS is constant.

SEE ALSO

elaborate(2)
read(2)

VER-400 (error) %s Bad format character in template_naming_style or template_parameter_style.

DESCRIPTION

Bad format character in template_naming_style or template_parameter_style.

WHAT NEXT

Change the relevant code to conform to the IEEE Std.

VER-401 (warning) %s Formality does not support %s .

DESCRIPTION

Formality does not support this feature now, please do not use it, otherwise, mismatch will happen.

WHAT NEXT

VER-402 (error) %s Improper usage of internally defined macros: %s

DESCRIPTION

Following are Presto Verilog Compiler specific macros, DC, PRESTO, VERILOG_1995, VERILOG_2000, VERILOG_2001 and SYSTEMVERILOG. SYNTHESIS is a reserved macro in IEEE Verilog synthesizable subset. All of the above have a pre-defined value of "". They should only be used with `ifdef, `ifndef and `elsif.

WHAT NEXT

VER-403 (warning) %s Improper usage of internally defined macros: %s

DESCRIPTION

Following are Presto Verilog Compiler specific macros, DC, PRESTO, VERILOG_1995, VERILOG_2000, VERILOG_2001, VERILOG_2005 and SYSTEMVERILOG. SYNTHESIS is a reserved macro in IEEE Verilog synthesizable subset. All of the above have a pre-defined value of "". They should only be used with `ifdef, `ifndef and `elsif.

WHAT NEXT

VER-404 (error) %s Incorrect value for hdlin_vrlg_std. Valid values are 1995, 2001, or 2005.

DESCRIPTION

This error message occurs when a nonexistent version of the Verilog standard is requested.

WHAT NEXT

Set the value of **hdlin_vrlg_std** to the intended version and run the command again.

SEE ALSO

hdlin_sverilog_std(3)
hdlin_vrlg_std(3)

VER-405 (error) %s A non-locally static choice must be the single choice, file support call for workaround.

DESCRIPTION

A non-locally static choice must be the single choice, file support call for workaround.

WHAT NEXT

VER-406 (warning) %s A non-locally static choice has more than one choice may not be supported correctly, you need to make sure the generated design is correct.

DESCRIPTION

A non-locally static choice has more than one choice may not be supported correctly, you need to make sure the generated design is correct.

WHAT NEXT

VER-407 (error) %s Return port name of type function must be '%s'.

DESCRIPTION

You receive this error message because the return port name of the type function is not as required .

WHAT NEXT

Correct the return port name for the type function by using -- pragma **return_port_name**.

SEE ALSO

elaborate (2).

VER-408 (error) %s Bad clock expression: ’%s’.

DESCRIPTION

This error message occurs when the clock expression is unacceptable due to the specified issue.

When the specified problem is an unsupported clock expression, be aware that in VHDL only simple constants are supported; for example:

```
generic ( CLK_EDGE: std_logic := ’1’ );
if (clk’event and clk = CLK_EDGE)
```

However, the following valid code is not simple enough to be supported:

```
generic( CLK_EDGE: std_logic := 1 );
constant CLK_EDGE2 : std_logic := CLK_EDGE;
if (clk’event and clk = CLK_EDGE2)  -- not simple enough
```

Complicated constant clock expressions will be supported in a future release.

WHAT NEXT

Use only simple constants in clock expressions.

VER-409 (error) %s Attributes with non-locally static values on integer/constants are not supported.

DESCRIPTION

Attributes with non-locally static values on integer/constants are not supported.

WHAT NEXT

Change the relevant code to conform to the IEEE Std.

VER-410 (warning) %s Expecting explicit event control

immediately after always_ff.

DESCRIPTION

Expecting explicit event control immediately after always_ff.

WHAT NEXT

VER-411 (error) %s Interface instance is expected here : %s

DESCRIPTION

Failed to get the expected interface instance.

The most likely cause of this error message is that an interface has been instantiated before declaration. In synthesis, interfaces, unlike modules, must be declared before they are instantiated.

WHAT NEXT

Please check your RTL for typographical errors, or that you have declared the interface before instantiating it and try again.

VER-412 (error) %s Illegal digit %c in unbased number.

DESCRIPTION

The digit should be one of the four basic values (0, 1, x, z).

WHAT NEXT

Check your design for invalid digits in unbased numbers and correct them.

VER-413 (error) %s Invalid argument for system task or function : %s

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std.

VER-414 (warning) %s Unsupported hdlin_field_naming_style : %s.

DESCRIPTION

Unsupported hdlin_field_naming_style encountered when analyzing/reading SystemVerilog RTL with Presto HDL Compiler.

The hdlin_field_naming_stle variable defines the parts of the net names that Presto HDL Compiler generates corresponding to the fields in VHDL records and SystemVerilog structs.

By default, the hdlin_field_naming_style is derived from the bus_naming_style and bus_dimension_separator_style. But when these are "%s[%d]" and "][" or are "%s<%d>" and "><", then it is possible to specify an independent hdlin_field_naming_style, such as "%s<%s>", "%s[%s]", or "%s.%s", in which the first %s stands for the name up to the field and the second %s stands for the field. The hdlin_field_naming_style must be of the form "%sX%s" or "%sX%sY", where X and Y are (possibly identical) non-whitespace characters.

WHAT NEXT

Modify the bus_naming_style, bus_dimension_separator_style, and/or hdlin_field_naming_style.

SEE ALSO

hdl_variables (3), **bus_naming_style** (3). **bus_dimension_separator_style** (3). **hdlin_field_naming_style** (3).

VER-415 (error) %s POLICY WARNING: missing constant expression in clk event.

DESCRIPTION

POLICY WARNING: missing constant expression in clk event.

WHAT NEXT

VER-416 (warning) %s The -preserve command-line option contains the %s hierarchical name.

DESCRIPTION

This warning message occurs when the **-preserve** option specifies a hierarchical name. Only simple names are allowed when the **-preserve** option is used with the **analyze**, **read_file**, **read_verilog**, or **read_vhdl** command.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, change the hierarchical name to a simple name in the relevant script.

SEE ALSO

analyze(2)
read_file(2)
read_verilog(2)
read_vhdl(2)

VER-418 (error) %s Empty string used as bus_dimension_separator_style.

DESCRIPTION

An empty bus_dimension_separator_style string ("") was encountered when elaborating a multidimensional bus.

WHAT NEXT

Do not override the bus_dimension_separator_style to the empty string ("").

SEE ALSO

hdl_variables (3), **bus_naming_style** (3). **bus_dimension_separator_style** (3).

VER-419 (warning) %s Empty string used as bus_dimension_separator_style.

DESCRIPTION

An empty bus_dimension_separator_style string ("") was encountered when elaborating a multidimensional bus.

WHAT NEXT

Do not override the bus_dimension_separator_style to the empty string ("").

SEE ALSO

hdl_variables (3), **bus_naming_style** (3). **bus_dimension_separator_style** (3).

VER-441 (warning) %s Port number %d of '%s' was named '%s'.

DESCRIPTION

You receive this warning when a complex port such as the third port in

```
module m(clk, out, .P({a,b}));
```

is declared without an explicit port name, as in

```
module m(clk, out, {a,b});
```

WHAT NEXT

If you want to control the naming of the port, add an explicit name to the port declaration.

VER-444 (error) %s Incorrect value for hdlin_sverilog_std. Valid values are 2005 or 2009.

DESCRIPTION

You receive this error message when a nonexistent version of the SystemVerilog standard is requested.

WHAT NEXT

Set the value of **hdlin_sverilog_std** to the intended version.

SEE ALSO

hdlin_sverilog_std(3)
hdlin_vrlg_std(3)

VER-500 (error) %s %s

DESCRIPTION

A syntax or internal error has surfaced during verilog traversering. The message specifies where the error appeared and why it was issued.

WHAT NEXT

Internal errors indicate a problem which should be reported to your Synopsys representitive.

VER-501 (error) %s Redundant %s directives on a chain of if-else-if statements.

DESCRIPTION

You receive this error message when running the **read** or the **elaborate** command if your SystemVerilog design contains a chain of if-else-if statements with redundant **unique** or **priority** keywords. For example:

```
unique if ( x == 0 )
  y = 1;
else unique if ( x == 1 )
  y = 2;
```

The second **unique** keyword is not permitted. Only the top if statement should be labeled.

WHAT NEXT

Verify that you intend to use a unique or priority chain of if statements, and remove the redundant directive.

SEE ALSO

elaborate(2)
read(2)

VER-502 (error) %s Conflicting directives on a chain of if-else-if statements; outer statements are labeled '%s', inner statement '%s'.

DESCRIPTION

You receive this error message when running the **read** or the **elaborate** command when your SystemVerilog design contains a chain of if-else-if statements with conflicting **unique** or **priority** keywords. For example:

```
unique if ( x == 0 )
  y = 1;
else if (x == 1)
  y = 2;
else priority if ( z == 0 )
  y = 2;
else if ( z == 0 )
  y = 3;
```

The inner if statement is labeled with a conflicting directive, which is not permitted. Use a directive only on the top if statement.

WHAT NEXT

If you want to start a new, separate chain of if-else-if statements inside the final else branch of the outer chain, use a block around the inner chain as shown below.

```
unique if ( x == 0 )
  y = 1;
else if (x == 1)
  y = 2;
else
  begin
    priority if ( z == 1 )
      y = 2;
    else if ( z == 0 )
 y = 3;
  end
```

Otherwise, decide whether you intend to use a **unique** or **priority** chain of if statements, and label only the top level if statement, removing all other directives in the chain of if-else-if statements.

SEE ALSO

elaborate(2)
read(2)

VER-503 (warning) %s Case statement marked unique has overlapping conditions.

DESCRIPTION

You receive this warning message when running the **read** or the **elaborate** command if your SystemVerilog design contains a **unique** case statement with overlapping branches. This means that more than one condition can be true at the same time, which contradicts the definition of unique case.

For example, the following case is not unique because the third branch matches any value of c, including the values matched by the first two branches. Therefore, the case requires priority encoding for correct execution.

```
unique casex ( c )
  2'bx1: y = 2;
  2'b1x: y = 1;
  2'bxx: y = 3;
endcase
```

The synthesis tool may make optimizations based on the **unique** keyword so that the priority encoding logic is simplified. However, this may bring simulation/synthesis mismatch.

If you are unsure whether or not a case is **unique**, do not mark it **unique**.

WHAT NEXT

Check the case statement conditions. Make sure that the case labels are intended to overlap. Otherwise, either correct the conditions so that they do not overlap, or remove the **unique** keyword.

SEE ALSO

elaborate(2)
read(2)

VER-504 (warning) %s Case statement marked %s does not

cover all possible conditions.

DESCRIPTION

You receive this warning message when running the **read** or the **elaborate** command if your SystemVerilog design contains a **unique** or **priority** case statement, where it is possible that no branch condition will evaluate to true. This means the case statement may execute, but no branch is taken, which contradicts the definition of **unique** and **priority** case statements.

For example, the following case is not a **unique** or **priority** case, because when c is 3'b011, 3'b010, or 3'b001, no branch is executed.

```
unique casex ( c )
  3'b111: y = 5;
  3'b11x: y = 4;
  3'b1xx: y = 3;
  3'b000: y = 2;
endcase
```

However, based on your knowledge of the design, you may know that only the listed values will occur. In this case, you can ignore this warning.

The synthesis tool cannot check all **unique** and **priority** case statements for this condition. If a case is marked **unique** or **priority**, but the case statement may execute without having any branch taken, your design may produce unexpected results.

If you are unsure whether or not a case statement is a **unique** or **priority** case statement, do not mark it unique.

WHAT NEXT

Check the case statement conditions. Based on your knowledge of the design, if you know that any values that are omitted from the case conditions cannot occur, you may ignore the warning. Otherwise, either add branches to cover the missing values, add a default branch, or remove the **unique** or **priority** keyword.

SEE ALSO

elaborate(2)
read(2)

VER-505 (warning) %s If statement marked unique has

overlapping conditions.

DESCRIPTION

You receive this warning message when running the **read** or the **elaborate** command if your SystemVerilog design contains a **unique** if statement whose branches overlap. This means that more than one condition can be true at the same time, which contradicts the definition of a **unique** statement.

For example, the following if statement is not **unique** because the third branch overlaps with the first. Therefore, the if statement requires **priority** encoding for correct execution.

```
unique if ( c == 2'b01 )
  y = 2;
else if ( c == 2'b10 )
  y = 1;
else if ( c == 2'b11 || c == 2'b01 )
   y = 3;
```

The synthesis tool may make optimizations based on the **unique** keyword so that the priority encoding logic is simplified. However, this may bring simulation/synthesis mismatch.

If you are unsure whether or not an if statement is **unique**, do not mark it **unique**.

WHAT NEXT

Check the if statement conditions. Make sure that the case labels are intended to overlap. Otherwise, either correct the conditions so that they do not overlap, or remove the **unique** keyword.

SEE ALSO

elaborate(2)
read(2)

VER-506 (warning) %s If statement marked %s does not cover all possible conditions.

DESCRIPTION

You receive this warning message when running the **read** or the **elaborate** command if your SystemVerilog design contains a **unique** or **priority** if statement where it is possible that no branch condition will evaluate to true. This means that the if statement may execute, but no branch is taken, which contradicts the definition of **unique** and **priority** if statements.

For example, the following if chain is not a **unique** or **priority** if statement because only two of the eight possible values of c are checked.

```
priority if ( c == 3'b111 )
  y = 5;
else if ( c == 3'b110 )
  y = 4;
```

However, based on your knowledge, you may know that only those two values will occur. In this case, you may ignore this warning.

The synthesis tool cannot check all **unique** and **priority** if statements for this error. If an if statement is marked **unique** or **priority**, but the statement may execute without having any branch taken, your design may produce unexpected results.

If you are unsure whether or not an if statement is a **unique** or **priority** if statement, do not mark it as **unique** or **priority**.

WHAT NEXT

Check the if statement conditions. Based on your knowledge of the design, if you know that any values that are omitted from the if conditions cannot occur, you may ignore the warning. Otherwise, either add branches to cover the missing values, add a final else branch, or remove the **unique** or **priority** keyword.

SEE ALSO

elaborate(2)
read(2)

VER-507 (error) %s Enumerated type member %s does not match size of type; (size %d, expecting %d).

DESCRIPTION

You receive this error message when running the **read** or **elaborate** command if your SystemVerilog design contains an enumerated type declaration, and a member of the enumerated type is the wrong size.

A value can be the wrong size because it will not fit into an explicitly declared data type, or because it does not match the size of a previous enum member that has a sized value.

```
enum short { red = 600000, blue = 2, green = 1} e; // red is too large to fit

enum { red = 5'd4, blue = 4'd3, green } e; // blue's size does not match red's
```

Consult the SystemVerilog language reference manual for more information on how values are assigned to members of enumerated types.

WHAT NEXT

Examine the members of the enumerated type, and make the changes needed to ensure that each member has the same size.

SEE ALSO

elaborate(2)
read(2)

VER-508 (error) %s Enumerated type member %s duplicates a previously seen value %s.

DESCRIPTION

You receive this error message when running the **read** or **elaborate** command if your SystemVerilog design contains an enumerated type declaration, and two members of the enumerated type are assigned to the same value.

The error is issued either for members that have an explicit value assigned to them, or for members whose value is determined automatically from the values of the preceding members.

Values of SystemVerilog enumerated type members are determined as follows.

• If an explicit value is given, then that value is used.

• If no explicit value is given, and the member is the first in the enumerated type, it is assigned to 0.

• If no explicit value is given, and the member is not the first in the enumerated type, then it is given a value 1 greater than that of the previous member.

In the following example red and green are explicitly assigned the same value.

```
 enum { red = 1, blue = 2, green = 1} e;
```

In the next example, red is assigned explicitly to 2, while green is given the value 2 because the previous member is given the value 1.

```
   enum { red = 2, blue = 1, green } e;
```

Consult the SystemVerilog language reference manual for more information on how values are assigned to members of enumerated types.

WHAT NEXT

Examine the members of the enumerated type, and make the changes needed to ensure that each member has a unique value.

SEE ALSO

elaborate(2)
read(2)

VER-509 (error) %s Enumerated type member %s cannot be assigned a four-state value (%s).

DESCRIPTION

You receive this error message when running the **read** or **elaborate** command if your SystemVerilog design contains an enumerated type declaration, the data type of the enumerated type is a two-state type, and a member of the enumerated type is assigned to a four-state value.

In the first example below, the int type is a two-state type and cannot represent x or z values, so red cannot be assigned to 3'bxxx. If no data type is specified for the enumerated type, then it defaults to int, which is a two-state type.

```
enum int { red = 3'bxxx, blue = 2, green = 1} e;   // error

enum { red1 = 3'bxxx, blue1 = 2, green1 = 1} e;   // error since default is int
```

To use four-state values in enumerated types, choose a data type as shown below.

```
enum integer { red = 3'bxxx, blue = 2, green = 1} e;   // OK with integer
```

Consult the SystemVerilog language reference manual for more information on how values are assigned to members of enumerated types.

WHAT NEXT

Either use a four-state data type, or remove any four-state values from the list of enumerated type members.

SEE ALSO

elaborate(2)

VER-510 (error) %s Value of enumerated type member %s cannot be determined since previous value was four-state.

DESCRIPTION

You receive this error message when running the **read** or **elaborate** command if your SystemVerilog design contains an enumerated type declaration, the specified member of the type is not explicitly assigned a value, and the previous member of the enumerated type is assigned to a four-state value.

Values of SystemVerilog enumerated type members are determined as follows.

• If an explicit value is given, then that value is used.

• If no explicit value is given, and the member is the first in the enumerated type, it is assigned to 0.

• If no explicit value is given, and the member is not the first in the enumerated type, then it is given a value 1 greater than that of the previous member.

When the value of a member of the enumerated type contains x or z, then it is an error not to specify an explicit value for the following member.

In the following example, red contains x, so blue must be explicitly assigned a value.

```
 enum int { red = 3'bxxx, blue, green = 1} e;   // error
```

WHAT NEXT

Supply an explicit value for any enumerated type member that follows a member with a four-state value.

SEE ALSO

elaborate(2)
read(2)

VER-511 (error) %s Subscript or range expression of the enum

member %s is not a literal constant.

DESCRIPTION

You receive this error message when running the **read** or **elaborate** command if your SystemVerilog design contains an enumerated type declaration that uses a subscript or range expression to produce a series of values in the type, and the subscript or range expression does not consist solely of constants.

The Presto HDL Compiler supports only a literal constant in such subscript or range expressions. For example, the following design fragment generates an error, because a parameter is used in a subscript expression for an enumerated type member.

```
parameter n = 8;
typedef enum { state[n] } states;
```

The following example showns an acceptable declaration.

```
typedef enum { state[8] } states;
```

WHAT NEXT

Supply a constant value for all subscript or range expressions in enumerated type declarations.

SEE ALSO

elaborate(2)
read(2)

VER-512 (error) %s Only integer types or one dimensional packed arrays are permitted as the underlying type of an enumeration.

DESCRIPTION

You receive this error message when running the **read** or **elaborate** command if your SystemVerilog design contains an enumerated type declaration that specifies an underlying data type, and the underlying data type is not permitted.

Only integer types or one dimensional packed arrays are permitted as the underlying type of an enumeration. The following is an example of an unacceptable declaration.

```
/* Not acceptable */
```

```
    typedef enum logic signed [0:0][0:0] { state1, state2, state3, state4 } states;
```

This example shows an acceptable declaration.

```
    typedef enum logic signed [1:0] { state1, state2, state3, state4 } states;
```

WHAT NEXT

Correct the design to use an integer type or one dimensional packed array as the underlying type of the enumeration.

SEE ALSO

elaborate(2)
read(2)

VER-513 (error) %s redeclaration of symbol %s as constant.

DESCRIPTION

You receive this error message if a symbol in a constant declaration has already been declared, either as a constant or as something else. In the following example, in is first declared as an input, then erroneously redeclared as a constant.

```
    input in;
    ...
    const in = 1'b0;      // erroneous redeclaration of input 'in'
                          // as a constant
```

WHAT NEXT

Decide which of the declarations is the intended one and remove or change the name in the other declaration, and then run the command again.

SEE ALSO

analyze(2)
read(2)

VER-514 (error) %s Return statement in non-void function %s

requires an expression as return value.

DESCRIPTION

You receive this error message when running the **read** or **elaborate** command if your SystemVerilog contains a function with a non-void return type, and a return statement occurs without an expression to use as the return type.

When a function is declared with a return type, all return statements must be accompanied by an expression.

WHAT NEXT

Supply a return value in the return statement and run the command again.

SEE ALSO

elaborate(2)
read(2)

VER-515 (warning) %s Discarding return value of function %s.

DESCRIPTION

You receive this warning message when running the **read** or **elaborate** command if your SystemVerilog design contains a call to a function, and the function's return value is not used.

The warning is not issued if the return type of the function is void.

WHAT NEXT

This is a warning message only. No action is required on your part if you intended to ignore the return value of the function.

However, if you do not want the return value of the function ignored, change the return type to void and run the command again.

SEE ALSO

elaborate(2)
read(2)

VER-516 (error) %s the name %s after the end construct does

not match the name %s of the construct.

DESCRIPTION

You receive this error message when the name after the end construct (module, interface, block, function, or task) does not match the construct name.

The following is an example of mismatched names after endmodule.

```
module name1(input i, output o);
assign o = i;
endmodule :name2  //name2 is not the same as name1
```

The following shows another example of mismatched names for sequential block.

```
module name1(input i, output reg o);
always begin
  o = i;
end : name2  //the name of the sequential block is not specified.
endmodule : name1
```

WHAT NEXT

Correct the names so that they match and run the command again.

SEE ALSO

analyze(2)
read(2)

VER-517 (error) %s A case statement is marked with both a unique or priority keyword, and a full_case or parallel_case directive.

DESCRIPTION

You receive this error message from the **read** or **elaborate** commands when your SystemVerilog design contains a case, casex, or casez statement marked with the 'priority' or 'unique' keyword that is also marked with the '//synopsys parallel_case' or '//synopsys full_case' pragma.

In Verilog, pragmas were the only means of communicating information about a case statement's properties to the compiler. In SystemVerilog, the 'unique' and 'priority' keywords convey that information. The Presto HDL Compiler accepts either

style, but does not accept a mixture of the two styles on the same case statement.

WHAT NEXT

If knowledge of the design guarantees that :

  1. At least one case condition will evaluate to true
BUT NOT:
  2. No more than one case condition will evaluate to true

then use the 'priority' keyword on the case.

If knowledge of the design guarantees that :

  1. At least one case condition will evaluate to true
AND:
  2. No more than one case condition will evaluate to true

then use the 'unique' keyword on the case.

If knowledge of the design guarantees that :

  1. No more than one case condition will evaluate to true
BUT NOT:
  2. At least one case condition will evaluate to true
AND:

then use the '//synopsys parallel_case' pragma for the case statement.

If neither of these conditions is known to be true, then use no keyword or pragma.

VER-518 (error) %s Cannot recover from previous errors.

DESCRIPTION

This error message occurs when the errors reported so far have left the compiler in a state where further error reports would be inaccurate, misleading, or omitted. The **analyze** or **read** command stops even if some of the source text has not yet been processed. For example, if the $unit scope of a SystemVerilog compilation issues any errors, compilation of modules or interfaces with visibility into that $unit may not proceed.

WHAT NEXT

Resolve the previously reported error message(s), and rerun the **analyze** or **read** command.

SEE ALSO

analyze(2)
read(2)

VER-519 (warning) %s Return value of function '%s' is not set.

DESCRIPTION

This warning message occurs during a **read** or **elaborate** command, when your SystemVerilog design contains an automatic function with a non-void return value that does not set the return value inside the function body. The return value of the function is not specified by the language standard. Change the your code to clearly specify the result.

The warning is not issued if the return type of the function is *void*.

```
function automatic f;
  input a;
  reg r;
  r = 2 * a;
endfunction

always begin
 y = f (a);
end
```

WHAT NEXT

If you intended to ignore the return value of the function you can disregard the warning message.

If the result is not what you intended, change the code to clearly specify the result.

SEE ALSO

elaborate(2)
read(2)

VER-520 (warning) %s Task enable in always_comb block.

DESCRIPTION

This warning message occurs during a **read** or **analyze** command when your SystemVerilog design contains a task enable within an always_comb block. This is a possible

simulation-synthesis mismatch, because the language standard does not require simulators to be sensitive to the contents of a task.

WHAT NEXT

Modify your code to use calls to void functions instead of task enables within always_comb blocks and then run the command again.

SEE ALSO

analyze(2)
read(2)

VER-521 (error) %s Using nonexistent return value of void function '%s'.

DESCRIPTION

You receive this error message from the **read** or **analyze** commands when your SystemVerilog design uses a call to a void function as an expression instead of like a task enable.

```
function automatic void f ( a , output [1:0] b ) ;
reg r;
   b = 2 * a;
endfunction

always begin
   y = f (a , b);
end
```

WHAT NEXT

Modify the void function to one that returns a value or to pass back the result through an output port.

VER-522 (error) %s The 'inout' port '%s' is not of net type.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it encounters an inout port declared with a non-net type, such as 'struct', 'bit', 'reg' or 'logic'. According to IEEE Std 1800-2005, section 19.12.1, a variable data type is not permitted on either side of an inout port.

WHAT NEXT

Rewrite the SystemVerilog code to use a net type on this port or to use two ports instead of just one. (In simulation, a 'ref' port could also be used, but 'ref' ports are not synthesizable.)

SEE ALSO

analyze (2), **read** (2).

VER-523 (error) %s Static %s '%s' is not synthesizable in %s, expecting 'automatic' keyword.

DESCRIPTION

This error message occurs when a function or task that is not automatic is encountered in $unit (formerly known as $root), in a package declaration, or in an interface declaration. The synthesizable SystemVerilog subset requires that each task and function in $unit, in a package declaration, or in an interface declaration be declared **automatic**.

WHAT NEXT

Add the **automatic** keyword after the **task** or **function** keyword.

VER-524 (error) %s Multiple implicit port connection tokens in instantiation.

DESCRIPTION

This syntax error message occurs when the .* implicit port connection token is used more than once in a single module or interface instantiation:

```
 xtend xtend(.* , .dout(dataout[7:0]), .*, din(alu_out[7]));
```

WHAT NEXT

Remove all but one of the .* tokens from the instantiation. Run the **analyze** or **read** command again.

SEE ALSO

analyze(2)
read(2)

VER-525 (error) %s Invalid interface access %s.

DESCRIPTION

This error message occurs when the Presto HDL Compiler finds an error when accessing the interface instance or the interface port.

For example:

```
   I inst();   // I is an interface definition, with modport mp
               // assign a = inst.mp.b;
```

WHAT NEXT

Correct the access to the interface and then run the compiler again.

SEE ALSO

analyze(2)
elaborate(2)
read(2)

VER-526 (error) %s Invalid name %s in the modport %s of the interface %s.

DESCRIPTION

This error message occurs when the Presto HDL Compiler finds an invalid name in the modport definition. This error may be caused by one of the following:

• There is no valid symbol declared in the interface.

• The symbols declared are inconsistent with the usage in the modport declaration. In the following example, the function *foo* is used as a port and signal *s* is used as a function or task:

```
  interface I();
      function foo ... endfunction
      logic s;
      modport MP (input foo, import function s());
      endinterface
```

• The name has been used in the modport declaration. In the following example, there are two ports named *s*:

```
interface I();
    function foo ... endfunction
    logic s;
    modport MP (input s, input s, import foo());
    endinterface
```

WHAT NEXT

Correct the name in the modport definition and then run the compiler again.

SEE ALSO

analyze(2)
elaborate(2)
read(2)

VER-527 (error) %s The input port %s is not writable.

DESCRIPTION

This error message occurs when the input port expanded from modport is not writable.

In the following example, *a* is an input port expanded from modport port *i* in module *M*. The assignment to *i.a* causes the error message.

```
interface I ();
logic a;
modport MP(input a);
endinterface

module M(I.MP i);
assign i.a = 1'b1;
endmodule
```

WHAT NEXT

Correct any errors in the code and run the command again.

SEE ALSO

analyze(2)
read(2)

VER-528 (warning) %s Invalid symbol name '%s' in the pragma signal name list. It is being ignored.

DESCRIPTION

This warning message occurs because the Presto HDL Compiler found an invalid symbol name in the pragma signal name list. This problem may be caused by one of the following:

• There is no valid symbol declared in the module.

• The usage of the symbol in the pragma signal name list is not consistent with the symbol declaration in the module.

• The type of the symbol (such as constant or function name) is not allowed to appear in the pragma signal name list.

WHAT NEXT

This is only a warning message. You can eliminate this warning by following the instructions below.

If you do not want the symbol to be ignored from the pragma signal name list, correct the symbol name in the pragma signal name list and then run the compiler again.

SEE ALSO

analyze(2)
elaborate(2)
read(2)

VER-530 (warning) %s Treating %s '%s' as automatic in %s; possible simulation-synthesis mismatch.

DESCRIPTION

This warning message occurs when a function or task that is not declared **automatic** is encountered in $unit (formerly known as $root), in a package declaration, or in an interface declaration. The synthesizable SystemVerilog subset requires that each task and function in $unit, in a package declaration, or in an interface declaration be declared **automatic**.

WHAT NEXT

Add the **automatic** keyword after the **task** or **function** keyword and run the command

again.

VER-531 (information) %s Variable '%s' is being read, but is not initialized. The subprogram default value will be used.

DESCRIPTION

You receive this message from the Presto HDL Compiler when your design contains a variable which is read, but has not been initialized yet. The subprogram default value will be used.

The subprogram default value can be 0's (as default) or tick-LEFT, which is controlled by the switch:

hdlin_subprogram_default_values

WHAT NEXT

Verify that you intended to use the subprogram default value as the initial value of the uninitialized variable.

SEE ALSO

hdlin_subprogram_default_values.

VER-532 (warning) %s If statement with %s directive but no else clause.

DESCRIPTION

You receive this warning message when running the **read** or the **elaborate** command if your SystemVerilog design contains a unique or priority if that has no has no else clause. For example:

```
unique if ( x == 0 )
  y = x;
```

According to the language standard, the unique or priotity keyword on an if with no else clause, is an assertion that the condition is always true. Hence, the example is equivalent to an assertion that x is always 0, followed by the assignment. It could be optimized to

```
y = 0;
```

WHAT NEXT

Verify that you intend to assert that the condition is always true. If so, consider using a formal assertion. If not, remove the unique or priority keyword.

SEE ALSO

elaborate(2)
read(2)

VER-533 (warning) %s Using default enum base size of 32.

DESCRIPTION

You receive this warning from the **read** or **analyze** commands when your SystemVerilog design contains an enum declaration without an explicit size declaration after the enum keyword. According to the language standard, the default size of an enum is 32. For example, in

```
typedef enum { RED, BLUE, GREEN, YELLOW } Color ;
Color current, next ;
```

current and next will be 32 bits wide, not 2 bits wide, as in

```
typedef enum [1:0] { RED, BLUE, GREEN, YELLOW } Color ;
Color current, next ;
```

WHAT NEXT

Modify your code to use an explict size declaration for the enum.

VER-537 (error) %s Inout direction for variable %s in modport.

DESCRIPTION

This error message occurs when the Presto HDL Compiler finds a variable listed in a modport definition with direction **inout**. A variable port cannot have direction **inout**.

WHAT NEXT

Correct the direction for the variable in the modport definition from **inout** to **input** or **output**, or correct the the declaration of the data object from a variable kind to a net kind.

SEE ALSO

analyze(2)
elaborate(2)
read(2)

VER-538 (warning) %s Inout direction for variable %s in modport.

DESCRIPTION

This warning message occurs when the Presto HDL Compiler finds a variable listed in a modport definition with direction **inout**. A variable port cannot have direction **inout**.

WHAT NEXT

Correct the direction for the variable in the modport definition from **inout** to **input** or **output**, or correct the the declaration of the data object from a variable kind to a net kind.

SEE ALSO

analyze(2)
elaborate(2)
read(2)

VER-540 (warning) %s Redefining macro '%s' with value '%s' to

’%s’.

DESCRIPTION

A macro is being defined at least twice with different values in the RTL code. If this is not really intented by customer, it may produce unexpected syntesys results.

The macro redefinition may happend if it is defined several times in different files or when macros are defined in files included by other include files.

WHAT NEXT

If a redefinition of the macro was not intended, just rename the macro such that it does not collide with the other macro definition, or keep files using one set of macro definitions separate when reading in the designs, to avoid macro names clashes.

VER-541 (warning) %s Parameters of macro ’%s’ have been redefined.

DESCRIPTION

A macro is being defined at least twice with a different list of parameters in the RTL code. If this is not really intented by customer, it may produce unexpected synthesis results.

The macro redefinition may happen if it is defined several times in different files or when macros are defined in files included by other include files.

The redefinition checks for literal parameter definition. If in one file exists this definition:

‘define SUM(x,y) x+y

and in another verilog file exists another definition of SUM:

‘define SUM(a,b) a+b

and if both files are used while compiling the same unit scope, VER-541 warning message will be issued, even if the macros are semantically equal.

When a macro is being redefined, usually the definition of macro will change too, so an additional VER-540 warning message may be issued.

WHAT NEXT

If a redefinition of the macro was not intended, just rename the macro so that it

does not collide with the other macro definition, or keep files using one set of macro definitions separate when reading in the designs, to avoid macro names clashes.

VER-553 (error) %s Pack operation using streaming operator requires that width of destination be greater than or equal to target.

DESCRIPTION

The Presto HDL Compiler issues this error message when the right-hand side of an assignment is a streaming operation that streams more bits than the left-hand side can use.

WHAT NEXT

Correct any errors like this in your code.

SEE ALSO

analyze (2), **read** (2).

VER-554 (error) %s Unpack operation using streaming operator requires that width of source bit stream be greater than or equal to target.

DESCRIPTION

The Presto HDL Compiler issues this error message when the left-hand side of an assignment is a streaming operation that consumes more bits than the right-hand side can provide.

WHAT NEXT

Correct any errors like this in your code.

SEE ALSO

analyze (2), **read** (2).

VER-555 (warning) %s Truncation discards bits.

DESCRIPTION

The Presto HDL Compiler issues this warning message when the left-hand side of an assignment discards some of the bits provided by the right-hand side.

WHAT NEXT

Correct any errors like this in your code.

SEE ALSO

analyze (2), **read** (2).

VER-561 (error) %s Subscript expression of the enum member %s is not a positive literal constant.

DESCRIPTION

You receive this error message when running the **read** or **elaborate** command if your SystemVerilog design contains an enumerated type declaration that uses [N] to produce a series of members in the type, but the N is not positive.

Only a positive literal constant is legal in that context.

For example, the following design fragment generates an error, because [0] is used to produces a series of members.

```
typedef enum { state[0] } states;
```

WHAT NEXT

Supply a positive literal value for expressions in enumerated type declarations.

SEE ALSO

elaborate(2)
read(2)

VER-700 (error) %s The construct ’%s’ is not supported in

synthesis.

DESCRIPTION

This error message occurs when the syntactic construct cited is not supported for synthesis.

WHAT NEXT

Exclude non-synthesizable constructs by enclosing the code with the conditional compilation directives shown below.

```
module mt( a );
`ifndef SYNTHESIS
   localparam realtime bus_stop=42;
`endif
```

VER-701 (error) %s Variable ’%s’ index not supported.

DESCRIPTION

You receive this error from the **read -f verilog -netlist** command, which invokes the Verilog netlist reader, because your code contains constructs the Verilog netlist reader does not support. To read a limited set of constructs more efficiently, the Verilog netlist reader supports only those Verilog constructs that commonly occur in netlists.

The Verilog netlist reader does not support the use of variables within subscripts or array declarations.

WHAT NEXT

If your code contains any of these constructs, use HDL Compiler to read your Verilog design. Invoke HDL Compiler by omitting the "-netlist" option from the **read** command, or by using the **analyze** and **elaborate** commands.

SEE ALSO

analyze (2), **elaborate** (2), **read** (2).

VER-702 (error) %s Unknown wire type '%s'.

DESCRIPTION

You receive this error from the **read -f verilog -netlist** command, which invokes the Verilog netlist reader, because your code contains constructs the Verilog netlist reader does not support. To read a limited set of constructs more efficiently, the Verilog netlist reader supports only those Verilog constructs that commonly occur in netlists, in order to read a limited set of constructs more efficiently.

The Verilog netlist reader does not support the use of some Verilog variable declarations, such as the "reg" datatype.

WHAT NEXT

If your code contains these constructs, use HDL Compiler to read your Verilog design. Invoke HDL Compiler by omitting the "-netlist" option of the **read** command, or by using the **analyze** and **elaborate** commands.

SEE ALSO

analyze (2), **elaborate** (2), **read** (2).

VER-703 (error) %s Unknown constant value '%d'

DESCRIPTION

You receive this message because The Verilog netlist reader was unable to read the design; the reader could not determine a constant value for the variable named in the message.

WHAT NEXT

Use HDL Compiler to read your Verilog design. Invoke HDL Compiler by omitting the "-netlist" option from the **read command**, or by using the **analyze** and **elaborate** commands.

SEE ALSO

analyze (2), **elaborate** (2), **read** (2).

VER-704 (error) %s Constant width not matched '%d' vs '%d'.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-705 (error) %s Constant signal '%s' cannot be at the left side.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-706 (error) %s Verilog netlist reader encountered trouble to build the named port in this design.

DESCRIPTION

Verilog netlist reader has limited support for named port handling. The following examples demonstrate the typical cases netlister reader now has trouble handling.

```
    module inouta (.a(i),.b(i));
inout i;
    endmodule

    module bit_select ( .a(i), .b1(j[1]), .b2(j[0]) );
input        i;
output [1:0] j;
    endmodule
```

WHAT NEXT

Please use read command without the -netlist option.

VER-710 (error) %s The construct '%s' is not supported when %s = %s.

DESCRIPTION

This error message occurs because the syntactic construct cited is not supported by the current configuration of the HDL Compiler or optimizer cited in the message.

WHAT NEXT

Adjust the global option named in the message. Note that not all option combinations are possible. After making your changes, run the command again.

VER-720 (error) %s The construct '%s' is not supported in this language.

DESCRIPTION

This error message occurs when the syntactic construct cited is not supported for the language specified by the **-format**, **-rtl**, or **-netlist** option of your **read** or **analyze** command.

Verilog (**-format verilog**) reports this error for syntax where SystemVerilog (**-format sverilog**) has extended the language beyond IEEE Std 1364.

This error may also be reported in rare situations where SystemVerilog does not implement syntax that is only available in older editions of Verilog.

The **-netlist** reader reports this error message about features that are not supported in gate-level netlists.

WHAT NEXT

Adjust your use of the **-format** option or Tcl commands with the **read_** prefix to parse the intended source language.

Switching from **-netlist** to **-rtl** may not be a practical solution for a large design. Use the **-rtl** reader on a small sample of the cited syntax, write the equivalent gate-level output, and then recode your **-netlist** input in the pattern suggested by the **-rtl** compiler.

SEE ALSO

analyze(2)
read(2)

VER-721 (error) %s The construct '%s' is not supported.

DESCRIPTION

This error message occurs when the syntactic construct cited is not supported in this compiler release.

WHAT NEXT

Check whether or not you are running a current version of the synthesis tool.

If you are interested in more information about this feature, contact the Synopsys Support Center by using Enter A Call at http://solvnet.synopsys.com/EnterACall.

For information about the latest software releases, go to the Synopsys SolvNet Release Library at http://solvnet.synopsys.com/ReleaseLibrary.

For information about creating, packaging, and sending a test case, go to http://www.synopsys.com/testcase.

VER-722 (error) %s The relative placement directive '%s' has a syntax error.

DESCRIPTION

This error message occurs when the relative placement directive has a syntax error.

For example, the orientation in may be **rp_orient** incorrect. The orientation should be N|W|S|E|FN|FW|FS|FE.

Another example is that the alignment default is not **sw** in **rp_align**.

WHAT NEXT

Correct the relative placement syntax error.

VER-730 (warning) %s The '%s' syntax is non-standard. %s

DESCRIPTION

This is a generic warning message which issues at every use of certain non-standard language features. The report includes a sentence to clarify what semantics are provided in lieu of the standard-prescribed error.

The setting of hdlin_vrlg_std at the time the (System)Verilog source is analyzed can influence which syntax gets this citation and what semantics are supplied.

WHAT NEXT

Make sure you agree that the non-standard meaning is the intended behavior for this RTL. Check the setting of hdlin_vrlg_std if you believe that this construct is meant to invoke a standard definition. If you need more choices of behavior when migrating legacy codes to current standards, contact Synopsys.

SEE ALSO

analyze (2), **read** (2).

VER-731 (warning) %s The '%s' syntax is non-standard. %s Only the first use of this construct will be cited.

DESCRIPTION

This is a generic warning message which issues on the first use of oft-repeated, but non-standard, language features. The report includes a sentence to clarify what semantics are provided in lieu of the standard-prescribed error. Other uses of the construct will be handled similarly, but silently.

The setting of hdlin_vrlg_std at the time the (System)Verilog source is analyzed can influence which syntax gets this citation and what semantics are supplied.

WHAT NEXT

Make sure you agree that the non-standard meaning is the intended behavior for this RTL. Check all uses of the non-standard construct. Check the setting of hdlin_vrlg_std if you believe that this construct is meant to invoke a standard definition. If you need more choices of behavior when migrating legacy codes to current standards, contact Synopsys.

SEE ALSO

analyze (2), **read** (2).

VER-733 (warning) %s Forward references to '%s' are non-standard. %s

DESCRIPTION

This message warns about violations of the SystemVerilog standard requirement that data variables be declared before use. Only the first reference to each name is cited. The references have been tolerated without this warning because the selection syntax you used could also be a legal form of hierarchical reference, but the explicit local declaration for this name became available before a hierarchical reference was located.

This is an unsound language extension, since forward references to variables cannot be resolved in all possible contexts. To aid the migration of legacy codes that may have relied upon forward reference, this message has warning level severity; it will rise to an error level severity in a future release of Presto SystemVerilog.

The setting of the **hdlin_sverilog_std** variable at the time the SystemVerilog source is analyzed can influence which syntax gets this citation and what semantics are supplied.

WHAT NEXT

Make sure you agree that the non-standard meaning is the intended behavior for this RTL. Check the setting of the **hdlin_sverilog_std** variable if you believe that this construct is meant to invoke a standard definition. If you need more choices of behavior when migrating legacy codes to current standards, contact Synopsys.

SEE ALSO

analyze(2)
read(2)
hdlin_vrlg_std(3)

VER-734 (warning) %s Nonstandard package access '%s::'; this name has a more local definition.

DESCRIPTION

This message warns about your use of a nonstandard language extension which might not be available in other SystemVerilog implementations. The SystemVerilog standard

prescribes that the identifier left operand to the scope operator (::) can resolve to a local data object, function, block label, or a wildcard import candidate for such an object, even though doing so inevitably leads to an error for misuse of the scope extraction syntax. Your access to a package with the same name as this more local definition will not be supported on a minimally conforming language processor. Notwithstanding this language extension, the scope operator always resolves the name of a local type even if this leads to an error, despite the existence of a package of the same name.

WHAT NEXT

No action is required. The scope operator found a package with the given name. To make this use conform to the IEEE standard, rename either the package or its local homograph.

SEE ALSO

analyze(2)
read(2)
suppress_message(2)

VER-736 (warning) %s Task '%s' with non-empty body is mapped to '%s'; body will be ignored.

DESCRIPTION

This warning message occurs when you map a task to a module because the module (instead of the task body) determines the implementation of the task. The body of the task is ignored.

The following example contains a task for which this warning message is issued:

```
task so_msff_t(output so, input si);  // synopsys map_to_module r00foobar
begin
   if(si === 1'b1) // task body will be ignored
     so <= si;
end
endtask
```

WHAT NEXT

This only a warning message.

Make sure that you intended the body of the task to be ignored in favor of the module that the task is mapped to.

VER-737 (warning) %s No module instance name.

DESCRIPTION

The Presto HDL Compiler issues this warning message when a module instantiation without an instance name is detected during the **analyze** or **read** command.

According to the Verilog language standard, module instantiations must include an explicit name. For backward compatibility reasons, the Presto HDL Compiler issues a warning instead of an error on such usage and invents an instance name.

WHAT NEXT

Add an explicit instance name so that the instantiation conforms with the language standard.

SEE ALSO

analyze (2), **read** (2).

VER-738 (error) %s No structure of instances name.

DESCRIPTION

The Presto HDL Compiler issues this error message when a structure of instances without a name is detected during the **analyze** or **read** command. This syntactic restriction is consistent with the syntactic restrictions the Verilog langauage standard imposes on arrays of instances.

WHAT NEXT

Add an explicit name for the structure of instances.

SEE ALSO

analyze (2), **read** (2).

VER-739 (error) %s No array of instances name.

DESCRIPTION

The Presto HDL Compiler issues this error message when an array of instances without a name is detected during the **analyze** or **read** command. According to the Verilog

language standard, every array of instances, even of gate instances, must have an explicit name specified.

WHAT NEXT

Add an explicit name for the array of instances.

SEE ALSO

analyze (2), **read** (2).

VER-791 (warning) %s An end_keywords directive without a matching begin_keywords directive.

DESCRIPTION

The Presto HDL Compiler issues this warning when excess end_keywords directives are encountered. For example,

```
‘begin_keywords "1364-1995"
   module test (in, generate);
   input in;
   output generate;
   assign generate = in;
   endmodule
‘end_keywords
‘end_keywords
```

WHAT NEXT

Determine whether there is a missing begin_keywords directive or too many end_keywords directives.

SEE ALSO

analyze (2), **read** (2).

VER-792 (warning) %s A begin_keywords directive without a matching end_keywords directive.

DESCRIPTION

The Presto HDL Compiler issues this warning when insufficient end_keywords

directives are encountered. For example,

```
‘begin_keywords "1364-1995"
‘begin_keywords "1364-1995"
   module test (in, generate);
   input in;
   output generate;
   assign generate = in;
   endmodule
‘end_keywords
```

WHAT NEXT

Determine whether there are too many begin_keywords directives or not enough end_keywords directives to match them.

SEE ALSO

analyze (2), **read** (2).

VER-793 (error) %s Unknown begin_keywords directive version specifier ’%s’.

DESCRIPTION

The Presto HDL Compiler issues this error when the begin_keywords directives is used with an unknown version specifier. For example,

```
‘begin_keywords "1364-1999"
   module test (in, generate);
   input in;
   output generate;
   assign generate = in;
   endmodule
‘end_keywords
```

WHAT NEXT

Determine if there is typo in the version specifier, which must be one of "1364-1995", "1364-2001", "1364-2001-noconfig", "1364-2005", or "1800-2005".

SEE ALSO

analyze (2), **read** (2).

VER-794 (error) %s Missing or unknown version specifier in begin_keywords directive.

DESCRIPTION

The Presto HDL Compiler issues this error when the begin_keywords directives is used alone, instead of with a version specifier, or when the double quotes in the version specifier are omitted. For example,

```
   `begin_keywords
      module test (in, generate);
      input in;
      output generate;
      assign generate = in;
      endmodule
   `end_keywords
```

or

```
   `begin_keywords 1364-1995
      module test (in, generate);
      input in;
      output generate;
      assign generate = in;
      endmodule
    `end_keywords
```

WHAT NEXT

Determine if there is a version specifier, which must be one of "1364-1995", "1364-2001", "1364-2001-noconfig", "1364-2005", or "1800-2005". If so, then check if the double quotes have been forgot.

SEE ALSO

analyze (2), **read** (2).

VER-795 (error) %s The begin_keywords directive is only supported in SystemVerilog format.

DESCRIPTION

The Presto HDL Compiler issues this error when the begin_keywords directives is used with the Verilog format instead of with the SystemVerilog format.

WHAT NEXT

Read the design as SystemVerilog.

SEE ALSO

analyze (2), **read** (2).

VER-796 (error) %s A begin_keywords directive within a design element.

DESCRIPTION

The Presto HDL Compiler issues this error when

WHAT NEXT

Do something wonderful.

SEE ALSO

analyze (2), **read** (2).

VER-797 (error) %s An end_keywords directive within a design element.

DESCRIPTION

The Presto HDL Compiler issues this error when

WHAT NEXT

Do something wonderful.

SEE ALSO

analyze (2), **read** (2).

VER-900 (error) %s The ’defparam’ construct is not supported.

DESCRIPTION

Presto HDL Compiler does not support the use of defparam statements. The following is an example of a defparam statement.

```
module top;
  defparam b.parm = 0;
  bottom b ();
endmodule

module bottom;
  parameter parm = 1;
  . . .
endmodule
```

WHAT NEXT

Replace defparam statements with module instance parameter overrides as shown in the following example.

```
module top;
  bottom #(.parm(0)) b ();
endmodule
```

VER-901 (error) %s The ’‘define’ directive requires that commas separate formal arguments.

DESCRIPTION

The ’‘define’ directive allows you to parameterize macros. An example is:

```
‘define ADD(A,B) ((A)+(B))
```

This error message is generated whenever two formal arguments to the macro are not separated by a comma.

```
‘define ADD(A B) ((A)+(B))
             ^  The missing comma will result in an error message.
```

WHAT NEXT

Delete whitespace or add a comma to form the identifier(s) needed by the macro’s definition.

VER-902 (error) %s The ‘‘define’ directive requires a non-empty argument list if parentheses are present.

DESCRIPTION

The following macro definition is rejected because no identifiers were found inside the parentheses.

```
‘define MACRO() 10
```

WHAT NEXT

When a macro does not need arguments, omit the parentheses.

```
‘define MACRO 10
```

VER-903 (error) %s the ‘default_nettype directive cannot occur inside a module, interface, or package.

DESCRIPTION

This error message occurs because when using the ‘default_nettype directive, it must be placed outside the scope of a module declaration as shown in the following example.

```
‘default_nettype wand

module top;
endmodule
```

The following example shows an invalid use of the ‘default_nettype directive.

```
module top;
‘default_nettype wand
endmodule
```

WHAT NEXT

Remove any ‘default_nettype directives from within module bodies. Ensure that the desired default net type is in effect from a directive outside the module body.

VER-904 (error) %s The ‘ifdef directive must have an identifier

name after it.

DESCRIPTION

This error message occurs when the token following an ‘ifdef directive is not an identifier name. A common mistake is to use a literal constant after the ‘ifdef.

The following is a example of the valid use of an ‘ifdef directive.

```
‘ifdef SYNTHESIS
‘endif
```

This is an example of an invalid use of the ‘ifdef directive, which generates this error message.

```
‘ifdef 5
‘endif
```

WHAT NEXT

Correct your design so that the ‘ifdef directive is used with a valid identifier, and then run the command again.

VER-905 (error) %s The ‘else directive was found without a corresponding ‘ifdef directive.

DESCRIPTION

This error message occurs when an ‘else directive is found without a corresponding ‘ifdef directive. Two common causes of this error message are that the corresponding ‘ifdef either does not exist, or that the ‘ifdef is not followed by an identifier name.

The following is an example of an ‘else directive without a corresponding ‘ifdef directive.

```
‘else
‘endif

// the ‘ifdef is missing
```

This is an example of an ‘ifdef directive without the following identifier name.

```
‘ifdef
```

```
   `else
   `endif

   // the `ifdef exists, but no identifier name follows it
```

This is an example of the correct use of an `else directive.

```
   `ifdef SYNTHESIS
   // ...

   `else
   // ...

   `endif
```

WHAT NEXT

Correct the design so that the `ifdef, `else, and `endif directives are matched, and then run the command again.

VER-906 (error) %s The ‘endif directive was found without a corresponding ‘ifdef directive.

DESCRIPTION

This error message occurs when the `endif directive is found without a corresponding `ifdef directive. Two common causes of this error message are that the corresponding `ifdef either does not exist, or that the `ifdef is not followed by an identifier name.

The following is an example of an `endif directive without a corresponding `ifdef directive.

```
   `endif

   // the `ifdef is missing
```

This is an example of an `ifdef directive without the following identifier name.

```
   `ifdef
   `endif

   // the `ifdef exists, but no identifier name follows it
```

This is an example of the correct use of an `endif directive.

```
‘ifdef SYNTHESIS
// ...

‘endif
```

WHAT NEXT

Correct the design so that the ‘ifdef and ‘endif directives match, and then run the command again.

VER-907 (error) %s The ‘timescale directive was used incorrectly.

DESCRIPTION

This error message occurs when the syntax of the ‘timescale directive is incorrect.

The correct syntax of the ‘timescale directive is shown below.

```
‘timescale time_unit / time_precision
```

The following is example of the correct use of the ‘timescale directive.

```
‘timescale 1 ns / 1 ps
```

The ‘timescale directive has no effect on synthesis.

WHAT NEXT

Correct the directive to use a valid timescale. Consult the IEEE 1364 standard for valid values. After making your changes, run the command again.

VER-908 (error) %s The ‘unconnected_drive directive requires pull1 or pull0 to be used.

DESCRIPTION

This error message occurs when either the ‘unconnected_drive directive is used without either pull1 or pull0.

The following example shows the correct use of the ‘unconnected_drive directive.

```
   `unconnected_drive pull1
```

This directive has no effect for synthesis.

WHAT NEXT

Correct the `unconnected_drive directive to use either use pull0 or pull1 and then run the command again.

VER-909 (error) %s The `default_nettype directive requires a valid wire type or ’none’.

DESCRIPTION

This error message occur when using the `default_nettype directive, without specifying a valid wire type or ’none’. The following list shows the valid wire types.

```
   wire      tri         tri0
   wand      triand      tri1
   wor       trior      trireg
```

This example shows a valid use of the `default_nettype directive with the wand wire type.

```
   `default_nettype wand
```

When the `default_nettype is set to ’none’, all nets must be explicitly declared.

WHAT NEXT

Correct the `default_nettype directive to use a valid wire type or ’none’ and then run the command again.

VER-910 (error) %s macro calls are nested too deeply.

DESCRIPTION

This error message occurs when there are too many nested macro calls. There is a limit to the amount of nesting that can occur in macro calls. The following is an example of a nested macro call.

```
   `a( `b( `c( ... ) ) )
```

The Verilog standard sets the nesting limit to 50 levels, although the compiler may support more levels.

WHAT NEXT

Recode your design to reduce the nesting of macro calls and then run the command again.

VER-911 (error) %s The ‘‘define’ directive must have an identifier name after it.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it finds that the token following an ‘define directive is not an identifier name. A common mistake is to use a literal constant, which the following example shows:

```
‘define 0 5
‘endif
```

The following example shows a valid use of ‘define.

```
‘define ZERO 0
‘endif
```

WHAT NEXT

Correct any errors like this in your code.

SEE ALSO

analyze (2), **read** (2).

VER-912 (error) %s The macro specified with the ‘‘define’ directive has a bad parameter list.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it encounters a ‘define directive that specifies a macro that in turn takes parameters, and the parameters are not a list of identifier names.

The following example generates this error message.

```
‘define NOT(0) ~X
```

WHAT NEXT

Be sure that any macro you specify with a ‘define directive has a valid parameter list of identifier names.

SEE ALSO

analyze (2), **read** (2).

VER-913 (error) %s The macro ’%s’ has not been defined.

DESCRIPTION

This message occurs when an attempt is made to use a macro that has not been previously defined. An example of this error is:

```
module top (out);
   output out;

   assign out = ‘UNDEFINED_MACRO;
endmodule
```

WHAT NEXT

Either define the macro, correct the macro reference to refer to a defined macro, or remove the macro invocation. After making your changes, rerun the command.

SEE ALSO

analyze(2)
read(2)

VER-914 (error) %s End-of-file found before ‘endif found.

DESCRIPTION

This message occurs when an ‘ifdef or ‘ifndef compiler directive is not closed with a corresponding ‘endif compiler directive.

WHAT NEXT

Insert an ‘endif to close the ‘ifdef or ‘ifndef.

SEE ALSO

analyze (2), **read** (2).

VER-915 (error) %s Syntax error in system timing check at token ’%s’.

DESCRIPTION

Standard Verilog system timing checks can be grouped into those ($setup, $hold, $setuphold, $recovery, $removal, $recrem) that use a stability window and those ($skew, $timeskew, $fullskew, $period, $width, $nochange) that are for clock and control signals.

Although the syntax looks like system task enables, the Verilog standard makes clear that these timing checks are not actual system task enables.

This error is issued when an actual system task enable is encountered where a system timing check is expected.

WHAT NEXT

Modify the code to use standard system timing check syntax.

SEE ALSO

analyze (2), **read** (2).

VER-916 (error) %s ’%s’ is a system function and not a system task.

DESCRIPTION

You receive this error when a system function call is used as a statement instead of as an expression. Often this is an indication that the value of the system function call is being inadvertently thrown away.

```
module m ;
 always
   $random() ;
```

```
endmodule
```

WHAT NEXT

If you really do not wish to use the return value, you could assign it to a dummy variable that will not be used or wrap the system function call in a dummy if statement.

```
module m ;
 always
   if ($random()) ;
endmodule
```

SEE ALSO

analyze (2), **read** (2).

VER-917 (error) %s The ’inout’ port ’%s’ is incompatibly declared as ’real’.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it encounters an inout port declared a real type, which is invalid.

WHAT NEXT

Correct any errors like this in your code.

SEE ALSO

analyze (2), **read** (2).

VER-918 (error) %s The ’inout’ port ’%s’ is incompatibly declared as ’reg’.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it encounters an inout port declared a register type (reg), which is invalid.

WHAT NEXT

Correct any errors like this in your code.

SEE ALSO

analyze (2), **read** (2).

VER-919 (error) %s The 'input' port '%s' is incompatibly declared as 'real'.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it encounters an input port declared a real type, which is invalid.

WHAT NEXT

Correct any errors like this in your code.

SEE ALSO

analyze (2), **read** (2).

VER-920 (error) %s The 'input' port '%s' is incompatibly declared as 'reg'.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it encounters an input port declared a register type (reg), which is invalid.

WHAT NEXT

Correct any errors like this in your code.

SEE ALSO

analyze (2), **read** (2).

VER-921 (warning) %s The macro '%s' you are attempting to undefine with the ''undef' directive is not defined.

DESCRIPTION

When using the ''undef' directive to undefine a macro, it must be defined. For example, the following examples would result in error messages:

```
'define CAT
'undef KAT

'define MY_MACRO
'undef MY_MACRO
'undef MY_MACRO
```

WHAT NEXT

Examine the code to see if perhaps the name of the macro has been misspelled, the 'undef occurs twice, or the macro never got defined.

SEE ALSO

analyze (2), **read** (2).

VER-923 (error) %s A valid identifier must follow the ''undef' directive.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it finds that the 'undef directive lacks the required identifier.

The following example shows an instance of an invalid statement (0 is not a valid identifier):

```
'undef 0
```

WHAT NEXT

Correct any instances of this type by replacing an invalid identifier with a valid one.

SEE ALSO

analyze (2), **read** (2).

VER-924 (error) %s Newline in argument list of ‘define %s.

DESCRIPTION

This error message occurs when the ‘define directive’s argument list contains a new line. All parameters of a macro and its definition must occur on the same line.

WHAT NEXT

Remove the newline, or if the newline is part of a formal argument’s default text, use a backslash character (\) immediately before the newline as an escape.

VER-925 (error) %s Input files nested too deep ’%s’.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it finds that input source files are nested too deeply, using the ‘include directive in Verilog.

When this happens, the message is generated.

WHAT NEXT

Reduce the number of nested input files to a workable amount.

SEE ALSO

analyze (2), **read** (2).

VER-926 (error) %s The ’‘include’ directive requires a filename enclosed in double quotes.

DESCRIPTION

When using the ‘include directive to input another file, you must provide the filename enclosed in double quotation marks, as shown in the following example:

```
‘include "my_include.h"
```

WHAT NEXT

Be sure to use double quotation marks when using the ‘include directive in this way.

SEE ALSO

analyze (2), **read** (2).

VER-927 (error) %s The number of parameters for the ’%s’ macro doesn’t match its definition.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it finds that the number of parameters you pass to a macro does not match the number of parameters specified by the macro definition.

The following example shows such an error:

```
‘define ADD(A,B) A+B

module top (IN, OUT);
input IN;
output OUT;

assign OUT = ‘ADD(IN);
endmodule
```

WHAT NEXT

Correct any errors like this in your code.

SEE ALSO

analyze (2), **read** (2).

VER-929 (error) %s The input file %s specified by the ’‘include’ directive cannot be recursive.

DESCRIPTION

This message occurs when the file specified by an ’‘include’ directive contains an ’‘include’ directive to the current file or to another file that has one or so on. The Verilog language standard expresses it as: "A file included in the source using

the ‘include compiler directive may contain other ‘include compiler directives. The number of nesting levels for include files shall be finite."

WHAT NEXT

Remove one of more of the ‘include directives from the files, or wrap the contents of the included file in an ‘ifndef. For example,

```
‘ifndef SEEN_HEADER_VH
‘define SEEN_HEADER_VH
    < the original contents of file >
‘endif
```

SEE ALSO

analyze (2), **read** (2).

VER-930 (error) %s System function %s has been defined.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-931 (error) %s System task %s has been defined.

DESCRIPTION

This may be a syntax error.

WHAT NEXT

This message is no longer issued.

SEE ALSO

analyze (2), **read** (2).

VER-932 (error) %s '%s' is a system task and not a system function.

DESCRIPTION

This message is issued when a system task enable is used as an expression, that is, when it used as if were a system function call and had a return value. For example,

```
module m ( output reg o ) ;
   always o = $display("Hello, world") ;
endmodule
```

WHAT NEXT

Modify code as appropriate.

SEE ALSO

analyze (2), **read** (2).

VER-933 (error) %s The '%s' system call should not have parentheses unless it has at least one parameter.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it encounters invalid parentheses. In Verilog, when calling a system task or system function, if the task or function does not take parameters, you cannot have empty parentheses in the code.

The following example illustrates an invalid use of parentheses:

```
assign Q = $time();
```

Because $time takes 0 parameters, you must omit the parentheses, as shown here:

```
assign Q = $time;
```

WHAT NEXT

Correct any invalid instances like this in your code.

SEE ALSO

analyze (2), **read** (2).

VER-934 (information) %s The imported name '%s' is %svisible to clients of this package.

DESCRIPTION

This information message issues for every name imported into the most global scope of a package declaration. It indicates whether or not the prevailing SystemVerilog dialect makes this name visible to the package's clients.

WHAT NEXT

Because early SV implementations differ on this aspect of the *import* statement, you may need to adjust the setting of *hdlin_sv_packages* to bring the set of exported names into agreement with other tools in the flow which use your package. The reported visibility is final; settings of hdlin_sv_packages at the time that clients refer to this package will have no effect on which of its names will be (in)visible.

SEE ALSO

analyze (2), **read** (2), **hdlin_sv_packages** (3), **VER-20** (n).

VER-935 (error) %s Identifier name '%s' has not been declared.

DESCRIPTION

This error is issued when the name of a variable is used before it has been declared.

WHAT NEXT

This error is no longer issued.

SEE ALSO

analyze (2), **read** (2).

VER-936 (warning) %s the undeclared symbol '%s' assumed to

have the default net type, which is '%s'.

DESCRIPTION

The Verilog standard says that if no explicit declaration is given for an identifier and the identifier is not in the scope of a ''`default_nettype none' compiler directive, then it shall be assumed to be implicitly declared as a net of the default net type, which is 'wire' unless overridden with the `default_nettype compiler directive. Specifically, this is assumed for undeclared identifiers used in a port expression declaration, for undeclared identifiers used in the terminal list of a primitive instance or a module instance, and, in Verilog 2001, for undeclared identifiers that appear on the left-hand side of a continuous assignment statement.

WHAT NEXT

Check your design to make sure that you intended an implicit declaration for this symbol. If not, add an explicit declaration.

SEE ALSO

analyze (2), **read** (2).

VER-937 (warning) %s Invalid argument for system function or task %s ignored.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-938 (warning) %s Missing expected argument for system function or task %s.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-939 (warning) %s The '%s' directive is not supported and will be ignored.

DESCRIPTION

This message is issued when a compiler directive is encountered that is not currently supported. The result is that the directive is just ignored. For example,

```
`delay_mode_unit
```

WHAT NEXT

No action is necessary.

SEE ALSO

analyze (2), **read** (2).

VER-941 (warning) %s Invalid escape sequence '\%c' in call to '$display'.

DESCRIPTION

When using '$display' this message is issued when the format specifier contains an invalid escape sequence for printing special characters.

```
$display("Hello, \zWorld.") ;
```

WHAT NEXT

Rewrite the format specifier to use a valid escape sequence.

SEE ALSO

analyze (2), **read** (2).

VER-942 (warning) %s Unescaped Verilog-2001 keyword '%s' used as identifier.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when you use one of the identifiers 'design', 'instance' or 'cell', which are reserved keywords in Verilog-2001, without escaping it. In future releases, this restriction will be enforced as a syntax error.

WHAT NEXT

Either modify the code, so that it doesn't use a keyword without escaping it, or disable Verilog 2001 features by setting hdlin_vrlg_std to 1995.

SEE ALSO

analyze (2), **read** (2).

VER-943 (error) %s Implicit net declaration for '%s' prohibited by ''default_nettype none' compiler directive.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when a net is implicitly declared within the scope of a ''default_nettype none' compiler directive.

WHAT NEXT

Modify the code, so that either the net is explicitly declared or its implicit declaration is not in the scope of a ''default_nettype none' compiler directive.

SEE ALSO

analyze (2), **read** (2).

VER-951 (error) %s The destination of a procedural continuous assignment must not be an array reference, bit select, or part

select.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it encounters an invalid destination for a procedural continuous assignment. The destination must not be an array reference, bit select, or part select.

Eiher of the procedural continuous assignments in the following example causes this error.

```
module foo (A, B);
        output [1:0] A;
        input B;
        reg [1:0]A;
   reg C[1:0];

always
begin
        assign  A[1] = B;       // This is an error.
        assign  C[1] = B;       // This is an error.
end

endmodule
```

WHAT NEXT

Correct any similar invalid instances in your code and then run the command again.

SEE ALSO

analyze(2)
read (2)

VER-952 (error) %s Assigment to '%s' requires that it be a register.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it encounters assignments that are not registers but should be.

In the following example, *a* and *c* should be registers.

```
always
begin
```

```
a = b;
c = d;
end
```

WHAT NEXT

Redefine the assignments as registers.

SEE ALSO

analyze (2), **read** (2).

VER-953 (error) %s Deassigning argument '%s' requires that '%s' be a register.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it encounters a value for a deassignment that is not a register.

The code in the following example causes the error because *B* is not a register type:

```
module foo (A, B);
        input A;
        output B;

always
        deassign B;
endmodule
```

WHAT NEXT

Change the value of the deassignment to a register.

SEE ALSO

analyze (2), **read** (2).

VER-954 (error) %s The register symbol '%s' has already been

defined.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it encounters a register defined twice in the code. It is illegal to define a register twice.

The code in the following example generates this error:

```
module foo;
        reg C;
        reg C;
endmodule
```

WHAT NEXT

Correct the code so that it defines a register once only.

SEE ALSO

analyze (2), **read** (2).

VER-955 (error) %s Assigning to output '%s' requires that it be a register.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it encounters assignments that should be registers.

In the following example, *a* and *c* should be registers:

```
always
begin
assign a = b;
assign c = d;
end
```

WHAT NEXT

Redefine the assignments as registers.

SEE ALSO

analyze (2), **read** (2).

VER-956 (error) %s The symbol '%s' is not defined.

DESCRIPTION

The Presto HDL Compiler issues this error message during execution of the **analyze** or **read** command when it encounters the use of a symbol or variable that has not been defined.

For example, the code in the following example generates the error:

```
module foo (A);
        input A;

always
        undefined = A;
endmodule
```

WHAT NEXT

Define the symbol or variable.

SEE ALSO

analyze (2), **read** (2).

VER-957 (error) %s Too many delay values supplied in the delay list.

DESCRIPTION

When specifying the delay of gates, you cannot supply more delay values than the gate supports.

For example, the following code attempts to instantiate a buffer:

```
module foo (A, B);
        input A;
        output B;

        buf # (0, 1, 2, 3, 4, 5) (B,A);
endmodule
```

The buf gate uses only 2 delay values, so providing 6 delay values is an error.

WHAT NEXT

To correct the above example, the code should read as follows:

```
module foo (A, B);
        input A;
        output B;

        buf # (0, 1) (B,A);
endmodule
```

SEE ALSO

analyze (2), **read** (2).

VER-958 (error) %s The triggered named event ’%s’ has not been declared.

DESCRIPTION

This error is issued whenever the named event to be triggered on has not been declared. (NOTE: Event triggers are not supported by synthesis.)

For example,

```
   module m;
     always
       begin
                -> nonexistent ;
       end
   endmodule
```

generates an error because the event ’nonexistent’ has not been defined.

WHAT NEXT

Add an ’event’ declaration to declare the named event, and wrap the event trigger with "‘ifndef SYNTHESIS ... ‘endif" to avoid a VER-193 error.

For example,

```
   module m;
     event nonexistent ;
     always
       begin
       ‘ifndef SYNTHESIS
```

```
                -> nonexistent ;
       `endif
       end
   endmodule
```

SEE ALSO

analyze (2), **read** (2).

VER-959 (error) %s The triggered event '%s' not declared as an event.

DESCRIPTION

This error is issued when the event name to be triggered was declared as some type other than 'event'. (NOTE: Event triggers are not supported by synthesis.)

For example,

```
   module foo;
     reg nonevent;
     always
        begin
               -> nonevent ;
        end
     endmodule
```

generates an error because the name 'nonevent' has been declared as a 'reg' instead of an event.

WHAT NEXT

Modify the declaration be an 'event' declaration, and wrap the event trigger with "`ifndef SYNTHESIS ... `endif" to avoid a VER-193 error.

For example,

```
   module m;
     event nonevent ;
     always
       begin
       `ifndef SYNTHESIS
                -> nonevent ;
       `endif
       end
   endmodule
```

SEE ALSO

analyze (2), **read** (2).

VER-960 (error) %s Lack of register declaration requires combinational primitive.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-961 (error) %s Register declaration ’%s’ supported only for output.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-962 (error) %s Existence of register declaration requires sequential primitive.

DESCRIPTION

This is a syntax error.

WHAT NEXT

Change the relevant code to conform to the IEEE Std 1364.

VER-963 (error) %s Illegal part select of memory '%s'.

DESCRIPTION

In Verilog, it is illegal to index a slice of a memory using a part select. The following example illustrates a part select of a memory that results in this error message.

```
module foo;
  reg [10:0] mem [10:0];
  reg [10:0] temp [3:0];

  always
     temp[3:0] = mem[3:0];
endmodule
```

WHAT NEXT

Rewrite this part of your design with a looping construct. Or, if available, read the file as SystemVerilog, in which it is legal to index a slice of a memory with a part select.

SEE ALSO

analyze (2), **read** (2).

VER-964 (error) %s Port '%s' incompatibly declared as scalar and vector.

DESCRIPTION

You get this message when the width declarations for a port are inconsistent. For example,

```
module m(dataout);
output dataout;
reg [2:0] dataout;
endmodule
```

WHAT NEXT

Modify the declarations to be consistent with each other. Usually, but not necessarily, this entails adding vector range information to the scalar declaration.

VER-965 (error) %s Premature end-of-file encountered in a '%s' block begun at line %d.

DESCRIPTION

This message, issued during execution of the **analyze** or **read** command, indicates that the Presto HDL Compiler has encountered a block of code that does not have its terminating token. For example, a *module* that has no *endmodule* or a comment that begins with '/*' but has no '*/' to terminate it.

WHAT NEXT

Review your code to locate such missing tokens and insert them.

SEE ALSO

analyze (2), **read** (2).

VER-966 (error) %s Procedural-continuous assignments are not supported by synthesis.

DESCRIPTION

This message, issued during execution of the **analyze** or **read** command, indicates that the Presto HDL Compiler has encountered a procedural-continuous assignment. Synthesis ignores such assignments.

The following example illustrates a procedural-continuous assignment, assign B = A, that synthesis ignores:

```
module foo (A, B);
        input A;
        output B;
        reg B;

always
        assign B = A;      //  this is a procedural-continuous assignment.

endmodule
```

WHAT NEXT

Because synthesis ignores procedural-continuous assignments, consider removing them if the code is intended for synthesis only.

SEE ALSO

analyze (2), **read** (2).

VER-967 (error) %s The ’force’ construct is not supported by synthesis.

DESCRIPTION

This message, issued during execution of the **analyze** or **read** command, indicates that the Presto HDL Compiler has encountered a force construct. Synthesis ignores such constructs.

The following example illustrates a force construct, force B, that synthesis ignores:

```
module foo (B);
        output B;
        reg B;

always
        force B = 1’b1;           // force is not supported

endmodule
```

WHAT NEXT

Because synthesis ignores force constructs, consider removing the force construct if the code is intended for synthesis only.

SEE ALSO

analyze (2), **read** (2).

VER-968 (error) %s The ’release’ construct is not supported by synthesis.

DESCRIPTION

This warning, issued during execution of the **analyze** or **read** command, indicates that the Presto HDL Compiler has encountered a release construct. Synthesis ignores such constructs.

The following example illustrates a release construct, release B, that synthesis ignores:

```
module foo (B);
   output B;
   reg B;

always
        release B;        // release is not supported

endmodule
```

WHAT NEXT

Because synthesis ignores release constructs, consider removing the release construct if the code is intended for synthesis only.

SEE ALSO

analyze (2), **read** (2).

VER-969 (error) %s The 'deassign' construct is not supported by synthesis.

DESCRIPTION

This warning, issued during execution of the **analyze** or **read** command, indicates that the Presto HDL Compiler has encountered a deassign construct. Synthesis ignores such constructs.

The following example illustrates a deassign construct, deassign B, that synthesis ignores:

```
module foo (B);
   output B;
   reg B;

always
   deassign B;          // deassign is not supported

endmodule
```

WHAT NEXT

Because synthesis ignores deassign constructs, consider removing the deassign construct if the code is intended for synthesis only.

SEE ALSO

analyze (2), **read** (2).

VER-970 (warning) %s The delay specification for gate instantiation is ignored.

DESCRIPTION

This warning, issued during execution of the **analyze** or **read** command, indicates that the Presto HDL Compiler has encountered a delay information for gate instantiation. Synthesis ignores such a delay specification.

The following example illustrates delay information, #(1,2), that synthesis ignores:

```
module foo (A,B,C);
   input A,B;
   output C;
   and #(1,2) (C,A,B);
endmodule
```

WHAT NEXT

Because synthesis ignores delay information on gate instantiation, consider removing the delay information if the code is intended for synthesis only.

SEE ALSO

analyze (2), **read** (2).

VER-971 (warning) %s The delay specification for tri-state gate instantiation is ignored.

DESCRIPTION

This warning, issued during execution of the **analyze** or **read** command, indicates that the Presto HDL Compiler has encountered delay information for a tri-state gate instantiation. Synthesis ignores such delay information.

The following example illustrates delay information, #(1,2), that synthesis ignores:

```
module foo (A,B,C);
   input A,B;
   output C;
   bufif0 #(1,2) (C,A,B);
endmodule
```

WHAT NEXT

Because synthesis ignores delay information on tri-state gate instantiation,

consider removing the delay information if the code is intended for synthesis only.

SEE ALSO

analyze (2), **read** (2).

VER-972 (warning) %s The delay specification for mos switch instantiation is ignored.

DESCRIPTION

This warning, issued during execution of the **analyze** or **read** command, indicates that the Presto HDL Compiler has encountered delay information for a mos switch instantiation. Synthesis ignores such delay information.

The following example illustrates delay information, #(1,2), that synthesis ignores:

```
module foo (A,B,C);
   input A,B;
   output C;
   nmos #(1,2) (C,A,B);
endmodule
```

WHAT NEXT

Because synthesis ignores delay information for mos switch instantiation, consider removing the delay information if the code is intended for synthesis only.

SEE ALSO

analyze (2), **read** (2).

VER-973 (warning) %s The delay specification for cmos switch instantiation is ignored.

DESCRIPTION

This warning, issued during execution of the **analyze** or **read** command, indicates that the Presto compiler has encountered delay information for a cmos switch instantiation. Synthesis ignores such delay information.

The following examples illustrates delay information, #(1,2), that synthesis ignores:

```
module foo (A,B,C,D);
   input A,B,C;
   output D;
   cmos #(1,2) (D,A,B,C);
endmodule
```

WHAT NEXT

Because synthesis ignores delay information on a cmos switch instantiation, consider removing the delay information if the code is intended for synthesis only.

SEE ALSO

analyze (2), **read** (2).

VER-974 (warning) %s The delay specification for bi-directional switch instantiation is ignored.

DESCRIPTION

This warning, issued during execution of the **analyze** or **read** command, indicates that the Presto compiler has found delay information for a bidirectional switch instantiation. Synthesis ignores such delay information.

The following example illustrates delay information, #(1,2), that synthesis ignores:

```
module foo (A,B,C);
   input C;
   inout A,B;
   tranif0 #(1,2) (A,B,C);
endmodule
```

WHAT NEXT

Because synthesis ignores delay information on bidirectional switch instantiation, consider removing the delay information if the code is intended for synthesis only.

SEE ALSO

analyze (2), **read** (2).

VER-975 (warning) %s The delay specification for pull gate

instantiation is ignored.

DESCRIPTION

This warning, issued during execution of the **analyze** or **read** command, indicates that the compiler has found a delay specification for a pull gate instantiation.

The following example illustrates a delay specification, #(1), that synthesis ignores:

```
module foo (A);
        output A;
        pullup #(1) (A);
endmodule
```

WHAT NEXT

Because synthesis ignores delay specifications on pull gate instantiations, consider removing the delay specification if the code is intended for synthesis only.

SEE ALSO

analyze (2), **read** (2).

VER-976 (warning) %s The delay specification for net declaration is ignored.

DESCRIPTION

This warning, issued during execution of the **analyze** or **read** command, indicates that the compiler has found a delay specification in a net declaration.

The following example illustrates a delay specification, #(1), that synthesis ignores:

```
module foo;
        wire #(1) w;
endmodule
```

WHAT NEXT

Be aware that synthesis ignores delay specifications on nets. If the code is intended for synthesis only, consider removing the delay specification.

SEE ALSO

analyze (2), **read** (2).

VER-977 (warning) %s The strength specification for a net declaration is ignored by synthesis.

DESCRIPTION

This warning, issued during execution of the **analyze** or **read** command, indicates that the compiler has found a strength specification in a net declaration.

WHAT NEXT

Be aware that synthesis ignores strength specifications on nets. If the code is intended for synthesis purposes only, consider removing the strength specification.

SEE ALSO

analyze (2), **read** (2).

VER-978 (error) %s Ambiguous genvar (’%s’) used in generate loop statement.

DESCRIPTION

You receive this error message because the two genvar assignments used in a generate loop specification must have the same genvar on the left hand sides. For example:

```
generate
  for (i=0; i<5; j=i+1)      // 2 different genvars "i" and "j" used
  ....
endgenerate
```

WHAT NEXT

Change the generate loop so that the same genvar is used on the left side of both assignments, and then run the command again.

SEE ALSO

analyze (2), **read** (2).

VER-979 (error) %s Two nested generate loops using the same genvar '%s'.

DESCRIPTION

You receive this error message because the same genvar is used as loop index by two nested generate loops. According to the language standard, using the same genvar by two nested generate loops is not allowed. The situation is demonstrated by the following example:

```
generate
  for (i=0; i<5; i=i+1) // genvar 'i' as index
    for (i=1; i<4; i=i+1) //ERROR: nested loop using the same genvar 'i' as index
  ....
endgenerate
```

WHAT NEXT

Rewrite one of the generate loops to use a different genvar as index.

SEE ALSO

analyze (2), **read** (2).

VER-980 (error) %s Illegal assignment to genvar '%s'.

DESCRIPTION

You receive this error message because the design contains an assignment to a genvar outside of a generate loop header. The value of genvars can only be defined by assignments inside generate loop headers. For example:

```
   generate
     for (i=0; i<5; i=i+1) // only valid assignments to genvar 'i'
     ...
     i = 5;  // ERROR: invalid assignment to genvar 'i'
     ...
   endgenerate
```

WHAT NEXT

Rewrite the RTL description so that genvars are only assigned values inside the generate loop headers.

SEE ALSO

analyze (2), **read** (2).

VER-981 (error) %s Macro definition is recursive '%s'.

DESCRIPTION

The Presto HDL Compiler issues this error message when a recursively defined macro is called while executing the **analyze** or **read** command.

Macros are defined using the define directive in Verilog.

WHAT NEXT

Redefine the macro to eliminate all self-references, including indirect self-references occurring in the definitions of other macros.

SEE ALSO

analyze (2), **read** (2).

VER-982 (error) %s The ''elsif' directive was found without a corresponding ''ifdef' directive.

DESCRIPTION

You receive this error message when the `elsif directive is found with no corresponding `ifdef. The `ifdef might not exist, or the `ifdef might not be followed by an identifier name.

The following is an example of a missing `ifdef:

```
`elsif SYNOPSIS_SYNTHESIS
`else
`endif

// the `ifdef is missing
```

The following shows an example of an `ifdef without an identifier name:

```
`ifdef
`elsif SYNOPSYS_SYNTHESIS
`else
`endif
```

```
// the ‘ifdef exists, but no identifier name follows it
```

WHAT NEXT

Correct the ‘elseif directive so it includes the ‘ifdef directive as shown in the example:

```
‘ifdef SOMETHING_ELSE
// ...

‘elsif SYNOPSYS_SYNTHESIS
// ...

‘else
// ...

‘endif
```

SEE ALSO

analyze (2), **read** (2).

VER-983 (error) %s The ’‘ifndef’ directive must have an identifier name after it.

DESCRIPTION

The tool issues this error message when the token following an ‘ifndef directive is not an identifier name. A common mistake is using a literal constant.

The following example shows an invalid identifier name, resulting in this error message.

```
‘ifndef 5
‘endif
```

WHAT NEXT

Correct the identifier name after the ‘ifndef directive, as shown in the following example:

```
‘ifndef SYNOPSYS_SYNTHESIS
‘endif
```

SEE ALSO

analyze (2), **read** (2).

VER-984 (error) %s The ‘‘elsif’ directive must have an identifier name after it.

DESCRIPTION

The tool issues this error message because the token following an ‘elsif directive is not an identifier name. A common mistake is using a literal constant.

The following example shows an invalid identifier name, resulting in this error message.

```
‘elsif 5
```

WHAT NEXT

Correct the identifier name after the ‘elsif directive, as shown in the example of a valid ‘elsif:

```
‘elsif SYNOPSYS_SYNTHESIS
```

SEE ALSO

analyze (2), **read** (2).

VER-985 (warning) %s The ‘‘line’ directive requires a %s.

DESCRIPTION

You receive this warning message because the Verilog ‘line compiler directive cannot find the expected arguments.

The expected arguments are a nonnegative decimal number, a double-quoted string, and a level of 0, 1, or 2.

WHAT NEXT

No action is required on your part.

SEE ALSO

analyze (2), **read** (2).

VER-986 (warning) %s Empty port in module declaration.

DESCRIPTION

You receive this warning message when the port list of a module declaration has an unconnected port.

EXAMPLE

The following legal Verilog statement indicates a module with four ports, the last of which is unconnected.

```
...
module m( a,b,c,);   /* Legal, but perhaps not intended */
...
```

WHAT NEXT

This is a warning message only. No action is required on your part.

However, if the unconnected port is not your intention, remove a comma and then run the command again.

SEE ALSO

analyze(2)
read(2)

VER-987 (warning) %s Port %s is implicitly typed

DESCRIPTION

The port warned has been declared previously with a different type.

Verilog

```
module test ( ..., dataout);
output dataout;
```

```
        reg [2:0] dataout;
```

Here dataout has been previously declared as one-bit, and later on declared as [2:0]. This may cause simulation, synthesis and formal verification mismatch due to the different interpretation in different tools as what's type of dataout.

WHAT NEXT

Change your Verilog source code to remove the inconsistent declaration for the port.

SEE ALSO

analyze (2), **read** (2).

VER-999 (error) %s Only simple identifiers are allowed in pragma signal list.

DESCRIPTION

You receive this error message when the pragma signal list contains expression list or non-simple identifiers.

EXAMPLE

The following verilog code won't work as identifier associated with pragam is not an simple identifier.

```
// synopsys sync_set_reset "reset[0]"

reg y ;
always @ (posedge clk)
begin : synchronous_reset
if (reset[0])
y = 1'b0;
else
y = d1;
end
```

WHAT NEXT

Use a wire and replace non-simple identifier.

SEE ALSO

analyze (2), **read** (2)

VER-1000 (warning) The hdlin_enable_presto variable will be ignored in a future release.

DESCRIPTION

The HDL Compiler (Presto Verilog) tool was introduced as the default Verilog reader in the 2001.08 release. In a future release, you will no longer be able to disable it using the **hdlin_enable_presto** variable.

WHAT NEXT

Remove the **hdlin_enable_presto** variable from your scripts.

SEE ALSO

hdlin_enable_presto (3).

VER-1005 (warning) %s Port %s of type input is being assigned.

DESCRIPTION

The port of type input is being assigned.

Verilog

```
module test ( ..., datain);
input datain;
assign datain = ...;
```

The port of type input has been assigned. This may cause simulation, synthesis and formal verification mismatch due to the different interpretation in different tools as what’s type of dataout.

WHAT NEXT

Change your Verilog source code to remove the inconsistent declaration for the port.

SEE ALSO

analyze (2), **read** (2).

VER-1006 (error) %s Entity of architecture '%s' cannot be found.

DESCRIPTION

This error message occurs during an **analyze** or **read** command activity if the entity of an architecture cannot be found.

WHAT NEXT

Ensure the desired entity exists and has been specified correctly. Check if there are any unsupported embedded configurations inside the architecture.

SEE ALSO

analyze(2)
read (2)

VER-1007 (error) %s Only one event control allowed on always_ff block.

DESCRIPTION

You receive this error message because SystemVerilog does not support multiple event statements on an always_ff block.

WHAT NEXT

Change the source code to remove the use of multiple events in the always_ff block.

SEE ALSO

elaborate (2), **read** (2).

VER-1008 (error) %s Incompatible DW encrypted file %s, the encrypted file is version %s, only version lower than or equal to

%s can be read by the current DC.

DESCRIPTION

This error message occurs when the tool detects that there is an incompatible version of an encrypted DW file.

WHAT NEXT

You need another version of DC to read the file.

SEE ALSO

analyze (2), **read** (2).

VER-1009 (error) %s No delays are allowed on an always_ff, always_comb or always_latch block.

DESCRIPTION

You receive this error message because SystemVerilog does not support delays on an always_ff, always_comb or always_latch block.

WHAT NEXT

Change the source code to remove the use of delays in the always_ff, always_comb or always_latch block.

SEE ALSO

elaborate (2), **read** (2).

VER-1010 (error) %s Port ’%s’ of type input is being assigned

DESCRIPTION

SystemVerilog has two kinds of input ports: variable input ports and net input ports. (SEE LRM 6.7) It is legal to assign to net input ports, but not legal to assign to variable input ports.

Sverilog

```
module test ( ..., datain);
input datain;
assign datain = ...;
```

WHAT NEXT

Change your source code to remove the inconsistent declaration for the port.

SEE ALSO

analyze (2), **read** (2).

VER-1011 (error) %s Tasks cannot contain event control statements.

DESCRIPTION

You receive this error message because you have attempted to use an event control statement inside of a task. This is not supported by Presto.

WHAT NEXT

Rewrite the source code so that tasks don’t contain events.

SEE ALSO

analyze (2), **read** (2).

VERIL

VERIL-0 (warning) %s

DESCRIPTION

WHAT NEXT

VERIL-1 (error) %s

DESCRIPTION

WHAT NEXT

VERIL-2 (fatal) %s

DESCRIPTION

WHAT NEXT

VERIL-3 (fatal) %s

DESCRIPTION

WHAT NEXT

VFM

VFM-1 (warning) Variable '%s' has been set to '%s', which conflicts
with the verification friendly mode.

DESCRIPTION

You turned on an optimization that may reduce the likelihood that the design can be formally verified.

WHAT NEXT

In case you run into problems during formal verification, you should consider turning off this optimization.

VFM-2 (error) Options '%s' and '%s' are incompatible.

DESCRIPTION

You selected two incompatible options.

WHAT NEXT

Re-issue the command command.

VFM-3 (information) Enabled verification friendly mode with dp_optimization_effort level '%s'.

DESCRIPTION

You successfully enabled the verification friendly mode.

WHAT NEXT

NA

VFM-4 (error) Failed to enable verification friendly mode.

DESCRIPTION

DC was unable to enable the verification friendly mode.

WHAT NEXT

Please address the problems highlighted by previous messages and re-issue the command.

VFM-5 (error) You need to provide a filename for the svf information.

DESCRIPTION

set_verification_friendly_mode will enable generation of setup information for Formality. You need to provide the name of a file to write this information to.

WHAT NEXT

Re-issue the command command with the 'filename' option.

VFM-6 (information) Disabled verification friendly mode. All optimizations have been turned to their default settings.

DESCRIPTION

You successfully disabled the verification friendly mode.

WHAT NEXT

NA

VFM-7 (warning) You need to perform set_svf to enable

generation of setup information for formality.

DESCRIPTION

Use set_svf to generate a Formality setup information file to ensure efficient compare point matching in Formality. For set_verification_friendly_mode to enable generation of setup information for Formality, you will need to create the file using set_svf.

WHAT NEXT

To avoid receiving this message, perform a set_svf prior to issuing set_verification_friendly_mode

SEE ALSO

set_svf(2).

VFP-001 (error) Failed to create placement netlist.

DESCRIPTION

This error message occurs during the loading of the virtual flat placement netlist. It indicates that the loading was not successful, and thus placement did not run. The most common reason for this error is that you have voltage areas in the design, but the voltage area information is not consistent.

WHAT NEXT

Check that your voltage area and operating condition information is consistent. Check the log file to see what errors occurred before this error and address those errors. Do not proceed ahead in the flow with this result as placement did not run.

SEE ALSO

set_operating_conditions(2)

VFP-002 (error) Missing the required license, %s.

DESCRIPTION

This error message occurs because you have accessed a command or feature that requires a license which is not available.

WHAT NEXT

Check if there are any licenses available or if there is any problem with the license server.

VFP-003 (error) No design is loaded.

DESCRIPTION

This error message occurs if there is no design loaded and a loaded design is needed.

WHAT NEXT

Load your design.

SEE ALSO

open_mw_cel(2)
open_mw_lib(2)

VFP-004 (error) The options %s and %s are mutually exclusive.

DESCRIPTION

This error message occurs when you use two options which are mutually exclusive.

WHAT NEXT

Check the man page of the command to determine why these options are mutually exclusive. Do not use one of the two options.

VFP-005 (error) Pad scaling error -- %s.

DESCRIPTION

This error message occurs during MinChip IO placement scaling. Depending on the detail of the message, it could be a design data issue or it could be that the IO placement of the design is too complicated for the command to handle or there is simply not enough space for shrinking.

WHAT NEXT

Check that the design is opened properly, and it has peripharal IO pad cell or bump cell. You may also seek to use core sizing only for MinChip.

SEE ALSO

estimate_fp_area(2)

VFP-006 (error) Failed to get MW lib id.

DESCRIPTION

This error message occurs while the command is reading the design. It is probably because the design library is not loaded to the tool or the design database is corrupted.

WHAT NEXT

Check if the design library is loaded to the tool.

SEE ALSO

open_mw_cel(2)

VFP-007 (error) Failed to open file %s for %s.

DESCRIPTION

This error message occurs when the command trys to open a file to read or write but fails.

WHAT NEXT

Check the permission of the directory and the file with the name indicated in the message.

SEE ALSO

VFP-008 (error) %s.

DESCRIPTION

This error message occurs when the objects specified with option -align_pins is not one design port and one macro cell pin.

WHAT NEXT

Check the objects specified in the command with the option -align_pins. Make sure to give one design port and one macro cell pin.

SEE ALSO

set_fp_macro_options (2)

VFP-009 (error) %s.

DESCRIPTION

This error message occurs when one or more macro cells specified with the -elements option is already defined in an existing macro array constraint.

WHAT NEXT

This error indicates conflicting macro array constraints being defined. The later constraint is accepted by the tool. It is user’s call to either remove the previously defined array constraint and set the new one, or keep the existing macro array constraint and ignore the new one.

SEE ALSO

set_fp_macro_array (2)

VFP-010 (error) %s.

DESCRIPTION

This error message occurs when the array name specified with the option -name is the same as the name of an existing macro array constraint.

WHAT NEXT

This error indicates conflicting macro array constraints being defined. The later constraint is accepted by the tool. It is user’s call to either remove the previously defined array constraint and set the new one, or keep the existing macro array constraint and ignore the new one, or change the new array constraint to use another name.

SEE ALSO

set_fp_macro_array (2)

VFP-011 (error) %s.

DESCRIPTION

This error message occurs when the tool couldn’t find any macro cell instance in the collection specified with the option -elements.

WHAT NEXT

Check the values passed to option -elements in the command line. Make sure there are proper numbers of macro cells in the collection.

SEE ALSO

set_fp_macro_array (2)

VFP-012 (error) %s.

DESCRIPTION

This error message occurs when each collection in the list of collections specified with option -elements contain different numbers of macro cells for a 2D rectangular array constraint.

WHAT NEXT

Check whether the array constraint is supposed to be a rectilinear one. If the array is supposed to be a rectilinear shape array, please specify option -rectilinear. Otherwise, check the values passed to option -elements in the command lineand make sure that all the collections in the list contain the same number of macro cells.

SEE ALSO

set_fp_macro_array (2)

VFP-013 (error) %s.

DESCRIPTION

This error message occurs when the macro cells specified with the option -elements belong to different plan groups.

WHAT NEXT

Plan groups are exclusive. Macro cells defined in one array constraint are going to be packed together. All the cells within an array constraint has to be in one plan group. Please check the specified array element cells. You may want to break this array constraint into two or more arrays for different plan groups.

SEE ALSO

set_fp_macro_array (2)

VFP-014 (error) The command %s is obsolete. Please use command %s instead.

DESCRIPTION

This error message occurs when you use an obsolete command. Use the suggested replacement command instead.

WHAT NEXT

Check the man page of the replacement command to make sure that it will meet your requirements. Change scripts to use the replacement command.

VFP-015 (error) Invalid value for option %s.

DESCRIPTION

This error message occurs when you give an invalid value to an option.

WHAT NEXT

Check the man page of the command to determine what are the valid values for the option.

VFP-016 (error) No plan groups are specified.

DESCRIPTION

This error message occurs when incremental placement on plan groups was requested, but no plan groups were given.

WHAT NEXT

Use -plan_groups option to specify the plan groups. Check the man page for more details on the command and its options.

VFP-017 (error) No voltage areas are specified.

DESCRIPTION

This error message occurs when incremental placement on voltage areas was requested, but no voltage areas were given.

WHAT NEXT

Use -voltage_areas option to specify the voltage areas. Check the man page for more details on the command and its options.

VFP-018 (error) The options %s and %s must be used together.

DESCRIPTION

This error message occurs when certain options are related and need to be used together or not at all.

WHAT NEXT

Use both related options, or do not use them at all. Check command man page for more details.

VFP-019 (error) All IO cells must be on the same edge of the design.

DESCRIPTION

This error message occurs when you have specified IO cells on more than one edge of the design. This command requires that all IO cells be on the same edge of the design.

WHAT NEXT

Check the specified IO cells, remove the ones not on the correct edge. Check command

man page for more details.

VFP-020 (error) Failed to get chip boundary.

DESCRIPTION

This error message occurs when there is no chip/cell boundary created in the design.

WHAT NEXT

Use initialize_floorplan to create the cell and core before running this command.

SEE ALSO

initialize_floorplan(2)

VFP-021 (error) Failed to find any IO cells in design.

DESCRIPTION

This error message occurs when there are no IO cells in the design. This command requires that there be IO cells to execute.

WHAT NEXT

If there appears to be IO cells in design, check the type of those cells. They may be marked as macros instead of IOs.

VFP-022 (error) No IO cell instances are specified.

DESCRIPTION

This error message occurs when there are no IO cells specified for the command. This command requires that there be IO cells specified to execute.

WHAT NEXT

Determine what IO cells you want the command to operate on, then give them as input to command. Check the type of the IO cells to make sure they are really marked as IOs.

VFP-023 (error) Failed to load %s information.

DESCRIPTION

This error message occurs when there is is a problem with loading certain fundamental information from database. This is likely because something is not set up correctly in database.

WHAT NEXT

Check for issues related to the information that was not found. Try recreating the database.

VFP-024 (error) Failed to find any nets in design.

DESCRIPTION

This error message occurs when there were no nets found in design. Placement requires that there be nets in the design.

WHAT NEXT

Check if there are nets in design. If there are nets, it is possible that those nets were filtered out because they had more pins than -max_fanout option specifies, or that they had a net weight of 0.

SEE ALSO

create_fp_placement(2)

VFP-025 (error) Internal error: %s

DESCRIPTION

This error message occurs when there is a serious internal error. It is possible that the database is corrupt or some other unexpected situation has happened.

WHAT NEXT

Regenerate the data base. Report this issue.

VFP-026 (error) Unable to remove constraint.

DESCRIPTION

This error message occurs when there is some error in removing macro constraint.

WHAT NEXT

There is probably another error issued prior to this error that should give move detail about the reason of failure.

VFP-027 (error) Cannot find %s with name %s.

DESCRIPTION

This error message occurs when the command cannot find the object with the specified name.

WHAT NEXT

Check any name specified in the command line and check the design to see whether the name is correct.

VFP-028 (error) Anchor object %s is not fixed or implied fixed.

DESCRIPTION

This error message occurs when the specified anchor object is not fixed or implied fixed by existing relative location constraints.

WHAT NEXT

User need to decide whether to fix the anchor object, to set another relative location constraint to imply this anchor object is fixed, or to discard this relative location constraint.

VFP-029 (error) Constraint %s already exist.

DESCRIPTION

This error message occurs when the given name of the constraint is the same as another constraint previously set.

WHAT NEXT

User can decide whether to delete the old constraint and set the new one, or discard the new constraint.

VFP-030 (error) Failed to get boundary of %s %s.

DESCRIPTION

This error message occurs when the command trys to get the boundary or bounding box of the object with the given name but failed.

WHAT NEXT

Check the design and see whether the name is correct.

VFP-031 (error) %s has a utilization of %.2f.

DESCRIPTION

This error message occurs the specified utilization exceeds 100%.

WHAT NEXT

Check the size of the design to make sure utilization is reasonable for placement.

VFP-032 (error) Error in getting design for timing analysis.

DESCRIPTION

This error message occurs when the command tries to access data for timing analysis purposes and failed.

WHAT NEXT

Check if the design and its environment are set up properly for running timing analysis in the tool.

VFP-033 (error) Failed in updating timer.

DESCRIPTION

This error message occurs when the command tries to update timer and failed.

WHAT NEXT

Check if the design and its environment are set up properly for running timing analysis in the tool, and if timing report can run through successfully.

VFP-034 (error) Failed preplacement check.

DESCRIPTION

This error message occurs when the preplacement check fails.

WHAT NEXT

There should be some other messages before this one that tells more detail about the failure.

VFP-035 (error) Failed returning placement to Milkyway.

DESCRIPTION

This error message occurs when the tool tries to send placement result to Milkyway DB but failed.

WHAT NEXT

There might be disk problem or DB corruption problem with the design. Try to do some editing operations like moving cells, see if that can be completed successfully.

VFP-036 (error) Failed in placement.

DESCRIPTION

This error message occurs when certain step in the placement failed.

WHAT NEXT

There should be some other error message about the detail of the failure before this message. Look in the log file for any prior error message and decide what to do next.

VFP-037 (error) Problem detected with cell padding. Congestion driven will not be run..

DESCRIPTION

This error message occurs when error occurs in calculating congestion-driven cell padding. When this error occurs, the placement will run without congestion-driven even though congestion-driven option is on.

WHAT NEXT

There is probably other more detailed message before this message that would point out the reason of failure. Look in the log file for the details.

VFP-038 (error) Failed during increment congestion/timing driven placement.

DESCRIPTION

This error message occurs when error occurs in congestion-driven or/and timing-driven incremental placement.

WHAT NEXT

There should be other more detailed messages before this message that would point out the reason of failure. Look in the log file for the details.

VFP-039 (error) %s %s is beyond core area.

DESCRIPTION

This error message occurs when the placement detects the specified object is beyond core area while placement only handles the object being completely inside core area.

WHAT NEXT

When this error is issued, if the placement continues, the tool must be taking only the object’s inside core area portion into consideration for placement. Whether the placement stops or not, it is advised that user check the specified object and fix the object being outside core area (partially or completely) problem.

VFP-040 (error) %s with multiple instantiated plan groups not supported.

DESCRIPTION

This error message occurs when the design has multiple instantiated plan groups (MIPG) and user is trying to run a function that doesn’t support MIPG.

WHAT NEXT

User need to decide whether to uniquefy the MIPGs or simply not to run the specified function.

VFP-041 (error) Incremental placement with multiple instantiated plan groups outside the core not supported.

DESCRIPTION

This error message occurs when incremental placement is called on a design with multiple instantiated plan groups outside the core.

WHAT NEXT

User need to decide whether to uniquefy the MIPGs or simply not to run the specified function.

VFP-042 (error) Pad file not found for multi-vdd design placement.

DESCRIPTION

This error message occurs when the tool couldn’t find the pad file.

WHAT NEXT

Check the command line and see whether the file exists and if the file name is spelled correctly with the pad file option.

VFP-043 (error) Pre-legalization check failed because of above issues.

DESCRIPTION

This error message occurs when the pre-legalization check failed.

WHAT NEXT

The messages before this one should provide more detail about the failure. Please read the log file and fix the indicated problem, then call legalization again.

VFP-044 (error) Failed to get %s.

DESCRIPTION

This error message occurs when the tool tries to get the specified information from database but failed.

WHAT NEXT

Check the design database or any technology setup for the design.

VFP-045 (error) Less than 3 movable cells found. Placement will

not be run in this case.

DESCRIPTION

Too few placeable instances for the placement algorithm to run.

WHAT NEXT

Check whether cells are mistakenly marked as fixed.

VFP-046 (error) %s. Placement will not be run.

DESCRIPTION

Placeable cells all have no area.

WHAT NEXT

Check design.

VFP-047 (error) %s area available for placement. Placement will not be run.

DESCRIPTION

The region being placed is overutilized.

WHAT NEXT

There are several reasons why this message could occur. First, this can occur due to hard macro or plan group padding. Try removing padding and placement blockages. If the error occurs on a movebound, plangroup or voltage area check whether cells from other areas are occupying the region. Secondly, this error could be due to sliver size. As channels get changed due to macro placement, they may become smaller than sliver_size and get blocked out. If channels around fixed macros are smaller than sliver size they will not be available for placement. In the default flow sliver size is 20 microns. Try setting it to -1 if this error comes up.

A more rare reason this message could occur is because you have floating (not fixed) rectilinear macro in the design. Float rectlinear macros are approximated as their bounding box during the first part of placement. This is an overestimation of the size of the rectilinear macro and could lead to a false utilization issue. If you have this situation, try fixing the rectilinear macros because fixed rectilinear

macros are seen by placement in their correct size.

A final rare reason this message could occur is because there is an inconsistency between your plan groups and the logical hierarchy. To fix this, you should remove the plan groups and recreate them to make sure they are consistent with the logical hierarchy.

SEE ALSO

set_fp_placement_strategy(2)
remove_plan_groups(2)
create_plan_groups(2)

VFP-048 (error) Conflicting cell constraints found.

DESCRIPTION

Constraints on macro cells are conflicting. Some constraints might not be satisfied.

WHAT NEXT

Check macro constraints. Sometimes move bound constraints conflict with other macro constraints such as anchor bound or edge constraints.

VFP-049 (error) Some cells do not fit into plan group or core boundary

DESCRIPTION

There are cells in the design that cannot fit into their respective plan group, movebound or voltage area constraint. Alternatively there are cells that are too large to fit within the core boundary.

WHAT NEXT

Check the orientation constraints on your macros. Possibly the cell could fit with a different orientation. If the large size of the cell is desired then the cell should be placed and fixed before running placement.

VFP-050 (error) Fixed macro %s is outside its plan group.

DESCRIPTION

Some fixed macros are violating their plangroup or movebound constraint.

WHAT NEXT

Move the macro into its plangroup.

VFP-051 (error) Failure during simultaneous placement and pin assignment.

DESCRIPTION

This error message occurs when there was a serious error during one phase of the simultaneous placement and pin assignment. It is likely that the resulting design does not have a good placement and/or pin assignment, and thus should be discarded.

WHAT NEXT

Check in the log file before this message and see what error(s) have occurred.

VFP-052 (error) Unable to load user grid from MW.

DESCRIPTION

This error message occurs when tool tries to get the user grid from the MW database, but fails to find the user grid.

WHAT NEXT

Recreate the user grid with set_user_grid command and try again.

VFP-053 (error) Command expects only 1 plan group.

DESCRIPTION

This error message occurs when you have passed a collection with more than 1 plan

group to the command or a collection with no plan groups. This command is intended to take a collection of only 1 plan group.

WHAT NEXT

Look at man page to understand why only 1 plan group is allowed. Only pass 1 plan group to command.

VFP-054 (error) Different number of cells in MIM group.

DESCRIPTION

This error message occurs when you have 2 multiply instantiated modules (MIM) plan groups that have a different number of cells. MIM plan groups in the same MIM group are supposed to have the same number of cells.

WHAT NEXT

When MIMs are created, they will have the same number of cells. It is possible that something happened after creation that changed the cells in the MIMs. Look to see if there was any optimization done, or any manual change to the netlist to cause that the MIM plan groups are no longer identical.

VFP-055 (error) Cannot restore placement because %s.

DESCRIPTION

This error message occurs if the restore placement has failed. There are a number of possibilities why this would happen. One is that the shape of the plan groups was changed after the original copy. If this happens, restore will not work. Another possibility is if the database got corrupted and the original placement data got lost.

WHAT NEXT

Unfortunately, there is nothing to do to fix this.

VFP-056 (error) Plan group %s is not an MIM plan group.

DESCRIPTION

This error message because the command is expecting a multiply instantiated module

(MIM) plan group, but the plan group is not an MIM plan group.

WHAT NEXT

Use report_mim to confirm that the plan group is not MIM. Determine if this plan group is supposed to be MIM and make it MIM if needed.

VFP-057 (error) Plan groups %s and %s are not the same shape/size.

DESCRIPTION

This error message occurs if the named plan groups are not the same shape or size. This is necessary for multiply instantiated modules (MIM) plan groups.

WHAT NEXT

Use update_mim_boundary to make the plan group shapes the same.

VFP-058 (error) Plan group %s has an illegal orientation.

DESCRIPTION

This error message occurs if the specified plan group has an illegal orientation. The specified plan group should be a multiply instantiated module (MIM) plan group as those are the only ones that can have a non ROT0 orientation. MIM plan groups are only allowed to be flipped. They are not allowed to be rotated by 90 degrees.

WHAT NEXT

Change orientation of plan group to ROT0 orientation which is always a legal orientation.

VFP-401 (warning) The command %s is obsolete. Use %s instead.

DESCRIPTION

This warning message occurs when you use an obsolete command. An obsolete command may still run, but it is unsupported and may be removed at any time. It is

recommanded to switch to the replacement command given in the warning message.

WHAT NEXT

Change your scripts to use the replacement command given in the warning message.

VFP-402 (warning) Pad scaling warning -- %s.

DESCRIPTION

This warning message occurs during MinChip IO scaling. Depends on the detail of the message, it warns user of potential problems in IO scaling that might cause the output to be incorrect.

WHAT NEXT

Check the output of the command to make sure that IO pad and bump cells are placed ok.

VFP-403 (warning) %s.

DESCRIPTION

This warning message occurs when -use_keepout_margin option is specified together with -x_offset and/or -y_offset.

WHAT NEXT

The option -use_keepout_margin overrules the options -x_offset and -y_offset. When it is specified together with one or both of the options, options -x_offset and -y_offset are ignored by the tool.

VFP-404 (warning) Option %s can only be used with option %s. Option %s ignored.

DESCRIPTION

This error message occurs when you use a secondary option that can only be used in conjunction with a primary option. In this case, the secondary option is ignored.

WHAT NEXT

Determine if you need the secondary option. If so, then you must also use the primary option. Check the command man page for more details.

VFP-405 (warning) Ref lib cel %s has too many overlap layer shapes (%d), overlap layer ignored.

DESCRIPTION

This error message occurs when you have a ref lib cel that has an overlap layer, and that overlap layer is very complex, i.e., it has many shapes in it. In this case, placement will ignore the overlap layer and use the cel boundary instead. This is because having a lot of shapes will create runtime issues.

WHAT NEXT

If you want to use overlap layer on this cel, then you need to simplify the overlap layer to have less than 1000 shapes.

VFP-406 (warning) %s cell %s overlaps %s cell %s.

DESCRIPTION

This error message occurs when overlap between cells are detected.

WHAT NEXT

Check the overlap and decide whether manual editing is needed to remove the overlap. It is possible that setting or changing certain parameters of the command can help resolve the overlaps.

VFP-407 (warning) Failed to get hierarchy information.

DESCRIPTION

This error message occurs when the tool tries to access certain information in hierarchy preservation and fails.

WHAT NEXT

Check if the design has hierarchy preservation information.

VFP-408 (warning) Problem detaching cell from plan group during legalization.

DESCRIPTION

This error message occurs when the tool is preprocessing the design for legalize placement.

WHAT NEXT

This could potentially be caused by data corruption in plan group related information in the design, and it will lead to placement result violating plan group/voltage area/region constraints. One way to fix the problem is to try deleting the plan groups and re-create them.

VFP-409 (warning) Problem attaching cell to plan group, hierarchy may be compromised.

DESCRIPTION

This error message occurs when the tool is post-process the design after legalize placement.

WHAT NEXT

This could potentially be caused by data corruption in plan group related information in the design, and it will lead to incorrect physical hierarchy. One way to fix the problem is to try deleting the plan groups and re-create them.

VFP-410 (warning) Less than 3 movable cells found. Placement will not be run in this case.

DESCRIPTION

Too few placeable instances for the placement algorithm to run.

WHAT NEXT

Check whether cells are mistakenly marked as fixed.

VFP-411 (warning) Cannot find hard or exclusive plan group, movebound or voltage area %s

DESCRIPTION

No plangroup, voltage area or movrbound could be found with the specified name.

WHAT NEXT

Check the spelling of the plangroup name.

VFP-412 (warning) Fixed macros are overlapping

DESCRIPTION

Overlapping fixed objects have been found.

WHAT NEXT

If the overlap is unintentional then either unfix the macros or manually remove overlap.

VFP-413 (warning) Cannot find a legal location for cell %s

DESCRIPTION

The overlap removal algorithm was unable to find a legal location for one of the macros.

WHAT NEXT

If possible try relaxing the constraints on this macro. If this is not possible the macro may need to be placed manually.

VFP-414 (warning) Legal locations were not found for all

macros. %s

DESCRIPTION

The overlap removal algorithm was unable to find a legal location for some of the macros.

WHAT NEXT

If possible try relaxing the constraints on these macro. If this is not possible the macro may need to be placed manually.

VFP-415 (warning) No hierarchy information in design. Hierarchy gravity turned off.

DESCRIPTION

This error message occurs when you have a design that has no logical hierarchy, and you have used the -hierarchy_gravity option for placement. In this case, the -hierarchy_gravity option is not useful, so it is turned off automatically.

WHAT NEXT

There is nothing to be done.

VFP-416 (warning) Option -vertical is not applicable to rectangular 2D array. Option -vertical is ignored.

DESCRIPTION

This error message occurs when a rectangular 2D macro array is defined with the option -vertical.

WHAT NEXT

Option -vertical means arranging the element cells in the array vertically instead of horizontally. It is accepted for 2D rectilinear arrays defined by specifying option -rectilinear. For 2D rectangular array, you can re-arrange the cells' orders in the -element option to achieve the effect of rotating a macro array.

VFP-417 (warning) Failure in auto hierarchy gravity detection.

DESCRIPTION

This error message occurs when placement is analyzing hierarchy preservation data of the design in order to find the proper hierarchy nodes as guidance to placement of a physically flat design.

WHAT NEXT

The failure indicates problem in hierarchy gravity, and would cause placement to automatically turn off hierarchy gravity option to continue with flat placement. If you want create_fp_placement to run with some hierarchy guidance, please create the desired plan groups. You can leave the plan groups outside the chip area. create_fp_placement will use these plan groups for hierarchy gravity.

VFP-418 (warning) Unable to open cell %s.%s for OVERLAP layer information.

DESCRIPTION

This error message occurs when placement tries to open a macro cell’s reference to get OVERLAP layer information but fails.

WHAT NEXT

When placement fails to get a macro cell’s OVERLAP layer information, it will continue with the cell boundary information in the design’s CEL view. The failure could be and is most likely because the reference library for the macro cell is missing. If you know that the macro cell has no OVERLAP layer shapes, you can ignore this warning. If you know that the macro cell has OVERLAP layer, please find the reference library and setup the correct reference library path for the design.

VFP-419 (error) The placer detected conflicting constraints on the following cells:
%s

DESCRIPTION

You receive this message because, by default, the placer errors out if it detects conflicting constraints on one or more cells. These constraints can be movebounds, array constraints, or simple (non-disjunctive) spatial constraints that are

impossible to meet. This can occur due to cells being fixed, the requirement for cells to fit on the chip, or constraints directly conflicting with each other.

WHAT NEXT

Please remove or change the conflicting constraints and rerun the placer.

SEE_ALSO

VFP-420 (warning) The placer detected conflicting constraints on the following cells: %s

DESCRIPTION

You receive this warning because the placer detected conflicting constraints on one or more cells. These constraints can be movebounds, array constraints, simple (non-disjunctive) spatial constraints that are impossible to meet. This can occur due to cells being fixed, the requirement for cells to fit on the chip, or constraints directly conflicting with each other.

WHAT NEXT

No action is required on your part.

However, you can avoid receiving this warning, if you are satisfied with your macro placement, by removing or changing the conflicting constraints and rerunning the placer. If you want the placer to error out when it detects conflicting constraints, set the **physopt_error_out_on_conflicting_macro_constraints** variable to **true**.

SEE_ALSO

set_mpc_macro_options(2)
set_mpc_options(2)
physopt_error_out_on_conflicting_macro_constraints(3)

VFP-421 (warning) The following bounds conflict:%s Treating groupbounds as soft constraints.

DESCRIPTION

You receive this message because the placer detected conflicting movebounds and

groupbounds on two or more cells. The placer will still honor the movebounds but it will treat all conflicting groupbounds as soft constraints. This means that the placer will attempt to honor the groupbounds, but they will be given the same priority as wirelength.

A conflict is defined as a physical impossibility. For example, suppose cell A is in a movebound with coordinates ((0 0)(10 10)), cell B is in a movebound with coordinates ((1000 1000)(1010 1010)) and cells A and B are both in a groupbound with dimension (20 20). There is no way for all three of those bounds to be satisfied. Alternatively, if cell B were fixed at location (1000 1000) we would have a similar problem. This kind of situation causes the placer to perform poorly, so the tool will weaken the groupbounds.

WHAT NEXT

No action is required on your part.

However, you can avoid receiving this warning by reviewing your movebounds and groupbounds and removing all conflicts.

SEE_ALSO

create_bounds(2)

VFP-422 (error) The following bounds conflict:%s

DESCRIPTION

You receive this message because, by default, the placer errors out if it detects conflicting movebounds and groupbounds on two or more cells. These bounds can be user-specified bounds or bounds generated by the tool (designated as "auto_bound").

A conflict is defined as a physical impossibility. For example, suppose cell A is in a movebound with coordinates ((0 0)(10 10)), cell B is in a movebound with coordinates ((1000 1000)(1010 1010)) and cells A and B are both in a groupbound with dimension (20 20). There is no way for all three of those bounds to be satisfied. Alternatively, if cell B were fixed at location (1000 1000) we would have a similar problem. This kind of situation causes the placer to perform poorly, so the tool will error out.

WHAT NEXT

You should review your movebounds and groupbounds and remove all conflicts. Alternatively, you can set the variable **placer_dont_error_out_on_conflicting_bounds** to **true**. This will cause the tool to automatically weaken the conflicting groupbounds and continue. If one or more of the conflicting bounds were generated by the tool ("auto_bound") then you can either remove the bounds that you have set or use the variable described above.

SEE_ALSO

create_bounds(2)
create_placement(2)
place_opt(2)
placer_dont_error_out_on_conflicting_bounds(3)

VFP-423 (warning) Save original placement failed.

DESCRIPTION

This warning message occurs when there was a problem with saving the current (ie original) placement. Saving the placement is necessary for the -restore_placement option to work. If this warning has occured, then it is likely that you will not be able to restore the original placement.

WHAT NEXT

Possible reasons for this warning include a corrupted database or no available disk space.

VFP-424 (warning) Flipping plan group %s may result in a nonlegal placement.

DESCRIPTION

This warning message occurs when there may be a legality problem with flipping the placement in a plan group. Due to the need for standard cells to fit in a row structure, it is necessary for a plan group to correctly align with the row structure to be able to flip the placement of standard cells in the plan group.

WHAT NEXT

Determine if you expect the result of flipping to be legal, or if that is not important to you right now. If you expect the result to be legal, then examine result to see if it is legal or not. If not, then adjust the plan group shapes so that a flipped plan group will also be legal. For example, if you have a double back design where there are no row gaps, then one possible legal plan group shape has a height which is even multiple of row height and the lower left corner of the plan group is on a row boundary.

VFP-425 (warning) No scan chain found.

DESCRIPTION

This warning message occurs when you use the -ignore_scan option, but no scan chain was detected in design. Since there is no scan chain, this option will have no affect on placement.

WHAT NEXT

Determine if there is a scan chain in the design. If there is no scan chain, then create the scan chain. If there is a scan chain in the design, please report this issue.

SEE ALSO

report_scan_chain(2)
get_scan_chain(2)

VFP-426 (warning) %d macros are overlapping.

DESCRIPTION

Overlapping macros have been found.

WHAT NEXT

If the overlap is unintentional then run create_fp_placement to remove the overlaps or manually remove the overlaps.

SEE ALSO

create_fp_placement(2)

VFP-427 (warning) %d plan group cells not inside their plan group.

DESCRIPTION

Cells which belong to a plan group are not inside their plan group. Because a plan group is an exclusive constraint, that could mean there is a problem with the placment.

WHAT NEXT

If this is unintentional then run create_fp_placement to correct the placement.

SEE ALSO

create_fp_placement(2)

VFP-428 (warning) Cell %s is not inside its %s %s.

DESCRIPTION

This warning means that there is a cell which is constrained to be placed in a certain area, but is not placed in that area. Typically, this is a plan group cell which is not placed inside its plan group.

WHAT NEXT

If this issue is unintentional then run create_fp_placement or create_placement to place the cell in the appropriate area.

SEE ALSO

create_fp_placement(2)
create_placement(2)

VFP-429 (warning) Unsupported region(s) detected in design.

DESCRIPTION

This warning means that there are one or more regions in the design. Regions are a placement constraint that was used in JupiterXT/Astro, but they are not supported in ICC. In ICC, regions have been replaced by movebounds.

WHAT NEXT

If you dont care about the region placement constraint, then you can ignore this warning. If you care about the constraint, then recreate the constraint using movebounds.

SEE ALSO

create_bounds(2)

VFP-430 (warning) Top level cell %s is overlapping %s %s %s.

DESCRIPTION

This warning indicate that a top level cell is overlapping an exclusive placement constraint such as a plan group or a voltage area. This could indicate that there is a problem with the placment of the top level cell as exclusive placement constraints do not allow top level cells to overlap.

WHAT NEXT

Look at the top level cell that is overlapping. If it is fixed, then that is likely the reason it is overlapping. You can unfix the cell and then run create_fp_placement to correct the placement. If the cell is not fixed and you have already run create_fp_placement then manually remove the overlap.

SEE ALSO

create_fp_placement(2)

VFP-431 (warning) %s is not a module name. Ignored.

DESCRIPTION

This warning indicate that a given cell is not a logical hierarchy cell, while the command is expecting the input to be logical hierarchy cell(s). So the given cell with the specified name is ignored by the command.

WHAT NEXT

Check the name of the cell in the command line to see if the name is correct for a logical hierarchy cell.

SEE ALSO

VFP-432 (warning) High fanout net synthesis has not performed on the design yet.

DESCRIPTION

This warning indicates that timing-driven placement is run on the design before high fanout net synthesis. The timing analysis inside the timing-driven placement is

affected by the unsynthesized high fanout nets. Although Virtual Flat placement does not consider the wire length of high fanout nets in its placement engine, these high fanout nets would still affect the timing on other nets and so to affect the timing-driven placement.

WHAT NEXT

User can set these high fanout nets to be ideal nets to reduce their impact on timing-driven placement.

SEE ALSO

set_ideal_net
set_ideal_network

VFP-433 (warning) %s %s is beyond core area.

DESCRIPTION

This message occurs when the placement detects the specified object is partally beyond core area.

WHAT NEXT

Tthe tool will only take the object’s inside core area portion into consideration for placement. Whether the placement stops or not, It is advised that user check the specified object and verify that the object’s location is intentional.

VFP-801 (info) %s

DESCRIPTION

This message occurs during set_fp_placement_strategy. There are some placement strategy options that have corresponding tcl variable controlling the same thing. When one of these options are set or reset, this message is issued to inform the user that the corresponding tcl variable is set to new value.

WHAT NEXT

SEE ALSO

set_fp_placement_strategy(2)

VH-005 (Error) Cannot create signature file under working directory

DESCRIPTION

This error message is generated if the master cannot generate a signature file under the working directory. The signature file is used by slaves to check that the work directory seen by master is also visible by slaves.

WHAT NEXT

Check the permission of the current directory from where the master is launched.The permission must be writebale, readable and executable.

VH-014 (error) Check your tool environment on machine <name>.

DESCRIPTION

This error occurs because the master process cannot invoke a slave using the ./.dps script in the current working directory.

WHAT NEXT

Run the ./.dps script from the UNIX shell where the master shell was invoked. Determine if the **SYNOPSYS_ROOT** variable is a valid path where the shell executable is available. Also ensure that you have at least one extra license that is required to run the script.

Also you can issue the following prompt:

rsh <machine_name> -login <login_name> `$path/.dps`

where $path is the full path to the working directory. If the command fails, you might have a problem in the environment setting. For example, the "rsh is not in the user path" problem can cause this error.

VH-018 (error) The shell executable on machine

<machine_name> has a different label.

DESCRIPTION

This error occurs because the master and the slave executables are not from the same installation. Both master and slave should have the same synopsys root. Check the csh file generated by the setup stage, and ensure that the value of synopsys_root is the same as that in the master.

The tool can also generate this error message if it is impossible for you to perform an rsh to the slave machine. Run **rsh <machine_name>** from the master shell, and determine if there is any problem accessing the specified machine name.

WHAT NEXT

Fix the rsh problem. Also ensure that the master and slave run using the same synopsys root. Open the ./.dps csh script in the current working directory, and verify that the value of the **SYNOPSYS_ROOT** variable is the same as the synopsys_root for the master shell.

VHD-1 (error) %s The library '%s' is not mapped to a directory.

DESCRIPTION

This message indicates that you attempted to access a library which does not have a valid directory path associated with it.

WHAT NEXT

For information on mapping between design libraries and paths, refer to the **define_design_lib** command manual page. Mapping can also be done via the .synopsys_vss.setup file.

VHD-3 (error) %s You have declared more than one architectures with the same name '%s'.

DESCRIPTION

You receive this error message if you have declared more than one architectures with the same name.

The last declared implementation of the architecture will overwrite its previous declared implementations.

WHAT NEXT

Verify that each of the architecture has been assigned a different name.

VHD-4 (warning) %s The architecture %s has already been analyzed. It is being replaced.

DESCRIPTION

You receive this warning message if an architecture with the same name has already been analyzed, which occurs if either of the following are true:

- The current analyzed file has already been analyzed.

• An architecture with the same name is declared in another file and has already been analyzed.

The implementation of the architecture is overwritten by the latest declared implementation.

WHAT NEXT

This is only a warning message.

However, you can check the overwritten file. If the result is not what you intended, change the architecture name and then run the command again.

VHD-5 (warning) %s the architecture %s has already been analyzed by a compiler other than Presto HDL. It is being replaced.

DESCRIPTION

You receive this warning message if an architecture with the same name has already been analyzed by a compiler other than Presto HDL.

The implementation of the architecture is overwritten by the latest declared implementation.

WHAT NEXT

This is a warning message only. No action is required on your part.

However, you can check the overwritten file. If the result is not what you intended, change the architecture name and then run the command again.

VHD-6 (warning) %s The entity '%s' has multiple architectures defined. The last defined architecture '%s' will be used to build the design by default.

DESCRIPTION

You receive this warning message if there are multiple architectures associated with the same entity. Just one architecture will be chosen to build the design. In PRESTO-VHDL, the last defined architecture will be chosen by default.

WHAT NEXT

Verify if the last defined architecture is what you want to use to build the design.

VHD-7 (warning) %s Initial values for signals/variables are not supported for synthesis by default. They are ignored.

DESCRIPTION

You receive this warning message if the signals/variables have initial values when they are declared. Presto VHDL ignores the initial values and uses the subprogram default value instead. This may cause simulation mismatch.

If variables are declared in a function, you can enable the variable initial value support by setting the following switch to true (the default is false):

hdlin_support_subprogram_var_init

WHAT NEXT

This is only a warning message.

If the subprogram default value is the same as the declared initial value or is acceptable, no action is required.

Otherwise, you can do either of the following:

- Use the **hdlin_support_subprogram_var_init** switch to solve the problem.
- Instead of the initial value, use an explicit assignment to set the initial value.

SEE ALSO

hdlin_subprogram_default_values(3)
hdlin_support_subprogram_var_init(3)

VHD-8 (information) %s Variable '%s' is being read, but is not initialized. The subprogram default value will be used.

DESCRIPTION

You receive this information message from the Presto HDL Compiler when your design contains a variable which is read, but is not yet initialized. The subprogram default value is used.

The subprogram default value can be 0s (as default) or ` (grave accent), which is controlled by the following switch:

hdlin_subprogram_default_values

WHAT NEXT

This is only an information message. No action is required.

However, it is best practice to verify that you intended to use the subprogram default value as the initial value of the uninitialized variable.

SEE ALSO

hdlin_subprogram_default_values(3)

VHD-100 (error) %s Elements of aggregate or string literal are out of bound, overlap or do not cover all cases.

DESCRIPTION

This error occurs when the values specified for an aggregate do not cover all the possible elements or if more than one value is specified for the same element or if the values specified are for elements that are not part of this aggregate.

WHAT NEXT

Modify your HDL description to ensure that there is one to one correspondence between elements of the aggregate and the values specified for it.

VHD-101 (error) %s Invalid return value for function.

DESCRIPTION

The output of the subprogram doesn’t exist or is not valid

WHAT NEXT

Look at the subprogram body and see if all return paths exist and are valid

SEE ALSO

VHD-200 (error) Unexpected %s %s. Analysis Failed.

DESCRIPTION

This message indicates an internal problem in the VHDL analysis for synthesis.

WHAT NEXT

Contact your Synopsys application engineer or the Synopsys hotline staff. Document beforehand the test case that produced the error to assist Synopsys personnel in analyzing your problem. In the meantime, do not use the construct that caused the error.

VHDL_217 (error) Multiple definition of '%s' %s

DESCRIPTION

WHAT NEXT

VHDL-1 (warning) Can't find types for all ports on design '%s'. It will be written out with its ports bit-blasted.

DESCRIPTION

This error is generated when vhdlout_single_bit is not set to BIT and if there are no bus information, then the design probably came from a format that doesn't put bus information on, and the user will expect the ports to be bit-blasted anyways.

WHAT NEXT

Try to read in a different format of netlist which can represent buses. They can be EDIF,Verilog, VHDL, etc. Or change vhdlout_single_bit to BIT.

VHDL-2 (warning) '%s' is both a %s and a %s. The %s is being renamed to '%s'.

DESCRIPTION

There was a name clash between these two objects. Please refer to the IEEE Standard VHDL Language Reference Manual (normally referred to as the VHDL LRM) for details on scoping rules for identifiers.

There is a limitation in the intelligence of VHDLout when issuing this warning. If there is a port with a name that clashes with a type-name, where the type is used as a sub-type of another type in a design being written out, and this sub-type is defined in STD.STANDARD (a predefined package that is part of the language definition), then this warning is issued even though no type declaration for the sub-type is written out. In other words this warning may be issued for a type name that is actually not written out. With the current version of the VHDL LRM, IEEE Std 1076-1987, this will only happen for the following example:

```
entity e is
```

```
  port ( bit: out bit_vector(1 downto 0));
end e;

architecture a of e is
begin
...
end a;
```

WHAT NEXT

You can change the port names so it will not be clashed with type-name.

VHDL-3 (warning) Design '%s' has invalid vhdl types. It will be written out with its ports bit-blasted.

DESCRIPTION

This error is generated when vhdlout_single_bit is not set to BIT, and type information is not supported.

WHAT NEXT

Change the types to the supported types. one of the following: Bit,Array,Enumeration and Record

VHDL-4 (error) Design '%s' is not linked. Use the link command on the design if you would like to write out vhdl for it.

DESCRIPTION

The design needs to be linked first in order for the VHDL writer to write out the design.

WHAT NEXT

Run the link command in dc_shell.

VHDL-5 (error) Could not process the types for the design.

DESCRIPTION

WHAT NEXT

VHDL-6 (error) Could not process the types in the design. Try setting vhdlout_dont_write_types to TRUE.

DESCRIPTION

WHAT NEXT

VHDL-7 (error) You must change ’vhdlout_bit_type’ to a bit type that includes a three-state value when writing out %s.

DESCRIPTION

vhdlout_bit_type determines what VHDL type to use when writing out ports, single-bit-wide ports, or ports that were buses in the original source but are written out bit-blasted.

This error can occur if, for instance, a generic three-state device is written out and *vhdlout_bit_type* is set to type "BIT," which does not contain a three-state value. Such a description cannnot simulate the high-impedance value, so VHDLout issues this error.

Note that VHDLout, apart from the type "BIT," does not recognize possible values of a type. So, if you use a type other than "BIT," but it does not contain a three-state value, this error will go undetected.

WHAT NEXT

Set *vhdlout_bit_type* to a type that contains a three-state value. For example *std_logic*.

EXAMPLE

This example will cause the error if read in and then written out with

vhdlout_bit_type = BIT.

```
library IEEE;
use     IEEE.std_logic_1164.all;

entity TRI_VHDL is
  port ( cond : in boolean; a : in std_logic; r : out std_logic);
end TRI_VHDL;

architecture test of TRI_VHDL is
begin
  process ( cond, a) begin
    if( cond) then
      r <= a;
    else
      r <= 'Z';
    end if;
  end process;
end test;
```

EXAMPLE MESSAGE

```
Error: You must change 'vhdlout_bit_type' to a bit type that includes a
        three-state value when writing out generic three-state devices. (VHDL-7)
```

VHDL-8 (error) This pre-v2.0 db file contains inconsistent type information.

DESCRIPTION

The current version of Design Compiler is not able to read the db generated before version 2.0.

WHAT NEXT

Please re-read in the original VHDL file.

VHDL-9 (error) You tried to write out two designs ('%s' and '%s') that contained different types with the same name ('%s').

DESCRIPTION

VHDL writer is not able to write out two designs (object) of the same names but of different types.

WHAT NEXT

Please write out the designs separately.

VHDL-10 (warning) The type '%s' in design '%s' was renamed to '%s'.

DESCRIPTION

This warning is generated when the type needs to be renamed because of the illegal VHDL character. It is generated internally for the returned types of subprograms.

WHAT NEXT

Check the returned type defined for the subprograms; if it is an anonymous type, try to change it to be a real type.

VHDL-11 (warning) The bits in port '%s' in design '%s' have inconsistent '%s' constraints.
Some constraint information is being lost.

DESCRIPTION

This warning is generated when there is more than one constraint set for the same port. It takes the first constraint you set.

WHAT NEXT

Make sure the constraints are setting once, or the first constraint is the one you want.

VHDL-12 (warning) EQUAL and OPPOSITE attributes on multi-

bit ports are being ignored.

DESCRIPTION

This warning is generated when EQUAL and OPPOSITE attributes exist on multi-bit ports.

WHAT NEXT

Make sure the attributes are consistently set for multi-bit ports.

VHDL-13 (warning) The '%s' '%s' is not a legal vhdl identifier. It has been renamed to '%s'.

DESCRIPTION

This warning is generated when the identifier contains illegal VHDL character.

WHAT NEXT

Please refer to VHDL reference manual and change it to legal VHDL character if you do not it to be renamed.

VHDL-14 (error) Record '%s' has duplicate field names '%s'

DESCRIPTION

WHAT NEXT

VHDL-15 (error) The variable '%s' should be a list of lists with each sub-list having exactly three strings in it.

DESCRIPTION

The variable vhdlout_conversion_functions should contains list of list which contains exactly three strings in it. They are "from_type", "to_type" and "function_name".

WHAT NEXT

Type "help vhdlout_conversion_functions" for more details.

VHDL-16 (error) Unable to model inout ports '%s' and '%s', which are wired together.

DESCRIPTION

The **write -f vhdl** command is intended primarily for the creation of a simulation model of the contents of the **dc_shell** database. This error occurs if there is more than one bidirectional port (port mode "inout") in the same net. Note that a bidirectional port driving a bidirectional pin will not cause this error.

This connectivity cannot be correctly modeled for simulation in VHDL, because it would require one assign statement for port A driving port B and one for port B driving port A. This circular assignment does not work.

WHAT NEXT

The preferred remedy is to change the HDL source so that it does not contain more than one bidirectional port per net.

The least preferred remedy is to use the **dc_shell disconnect_net** command to disconnect all but one of the bidirectional ports in the same net. Then re-write the design. If necessary, these ports can be reconnected manually in the resulting VHDL text file.

VHDL-17 (error) Unable to write a conversion function for the inout %s port '%s'.

DESCRIPTION

VHDLout encountered a bidirectional port when it was creating type conversion functions. Because information about the current direction of the signal is not available at any given time, it is not possible to create a working type conversion function for bidirectional signals. Hence, one does not know whether to convert for a source or a sink signal.

Beyond looking at the port's mode, VHDLout also analyzes the net to see if the port is used both as a sink and a source. If it is used only as a unidirectional signal, VHDLout treats it as such and creates a type conversion for it. Of course, this error does not occur in that case.

WHAT NEXT

Note that type conversion functions are created in two situations:

vhdlout_single_bit = VECTOR and *vhdlout_write_top_configuration = TRUE*.

To write a VHDL description for the design in this situation, change the setting of *vhdlout_single_bit* to "not equal VECTOR" or set *vhdlout_write_top_configuration = FALSE*.

vhdlout_single_bit = USER and *vhdlout_preserve_hierarchical_types = VECTOR* and

The suggested remedy for this situation is to set
vhdlout_preserve_hierarchical_types = USER

To see the possible settings and their meanings, refer to the man page for the *vhdlout_single_bit* variable. With either of these two changes, no type conversions are created.

If the above setting does not work, then it could be this port connects to an component pin that is buffer.

VHDL-18 (warning) '%s' is not a legal simulator. Variable '%s' is being ignored.

DESCRIPTION

This warning is generated when vhdlout_target_simulator is set to an unknown simulater.

WHAT NEXT

Reset vhdlout_traget_simulator to a valid simulator.

VHDL-19 (warning) Target simulator '%s' is not supported when %s is set to "TRUE".

DESCRIPTION

The warning is generated when vhdlout_target_simulator is set to a "xp" or "xp100" simulator and vhdlout_equations is set to TRUE.

WHAT NEXT

Change vhdlout_equations to FALSE or change vhdlout_target_simulator.

VHDL-20 (warning) There are inout ports of type '%s' that are multiply driven. The type '%s' must be a resolved type or the vhdl will not simulate.

DESCRIPTION

VHDLout cannot determine whether the port is of a resolved type. This warning is issued whenever a multiply driven inout port is found.

WHAT NEXT

Check that the type reported in the message is a resolved type. If it is, ignore this warning. If the type is not resolved, two remedies exist.

Modify the setting of **vhdlout_single_bit** or **vhdlout_preserve_hierarchical_types** as appropriate. Change the variable setting to "BIT" or "VECTOR." When necessary, VHDLout creates a resolved type. For more information on the use of these variables, see the appropriate man pages.

Alternately modify your VHDL source to use a resolved type for the inout ports, recreate the design, and write again. Note that the warning is issued only once for each type. In a hierarchical design, multiple entities with the same problem may exist.

EXAMPLES

Example of warning that is safe to ignore. "std_logic" is a resolved type.

```
library IEEE;
use     IEEE.std_logic_1164.all;

entity M_VHDL is
  port ( a, b : in std_logic; r : inout std_logic);
end M_VHDL;

architecture test of M_VHDL is
begin
  process ( a) begin
    r <= a;
  end process;

  process ( b) begin
    r <= b;
  end process;
end test;
```

Example where warning is correct. "BIT" is not a resolved type. This will cause problems in simulation.

```
entity M_VHDL is
```

```
  port ( a, b : in bit; r : inout bit);
end M_VHDL;

architecture test of M_VHDL is
begin
  process ( a) begin
    r <= a;
  end process;

  process ( b) begin
    r <= b;
  end process;
end test;
```

EXAMPLE MESSAGE

```
Warning: There are inout ports of type 'std_logic' that are
        multiply driven. The type 'std_logic' must be a resolved type or
        the vhdl will not simulate. (VHDL-20)
```

VHDL-21 (warning) STD.TEXTIO package used by design '%s' in file '%s' is not supported for synthesis.

DESCRIPTION

STD.TEXTIO package is not supported for synthesis.

WHAT NEXT

Remove the use of this package from the use clause

VHDL-22 (error) Stop processing due to a corrupted db file (%s).

DESCRIPTION

Somehow the db file contains incomplete type information. Please find out which command caused this problem and report it to the Support Center or CAE.

WHAT NEXT

Please regenerate the db file.

VHDL-23 (error) Write command failed due to system error.

DESCRIPTION

It could be the file system is full.

WHAT NEXT

VHDL-24 (error) Can not write out the assignment statement for this inout port %s.

DESCRIPTION

This ocurrs probably due to the renaming on the inout port signals.

WHAT NEXT

Check your design and the port assignment.

VHDL-25 (error) Can not write out this design '%s' with memory operations in it using non-levelized writer.

DESCRIPTION

The design needs to be flatten before writting out.

WHAT NEXT

Please set vhdlout_levelize to TRUE.

VHDL-100 (error) Parameter ’%s’ multiply defined %s

DESCRIPTION

WHAT NEXT

VHDL-101 (error) Variable or signal ’%s’ defined more than once %s

DESCRIPTION

WHAT NEXT

VHDL-102 (error) Port ’%s’ defined more than once %s

DESCRIPTION

WHAT NEXT

VHDL-103 (error) Entity ’%s’ defined more than once %s

DESCRIPTION

WHAT NEXT

VHDL-104 (warning) ’SIGNAL’ declaration for subprogram input

port ignored %s

DESCRIPTION

WHAT NEXT

VHDL-105 (error) Unknown type ’%s’ used %s

DESCRIPTION

WHAT NEXT

VHDL-106 (error) Undefined function, variable or type ’%s’ %s

DESCRIPTION

WHAT NEXT

VHDL-107 (error) Undefined variable ’%s’ %s

DESCRIPTION

WHAT NEXT

VHDL-108 (warning) ’Transport’ construct is not supported. It is ignored %s

DESCRIPTION

WHAT NEXT

VHDL-109 (warning) Signal assignment delays are not

supported. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-110 (error) Invalid based integer %s %s

DESCRIPTION

WHAT NEXT

VHDL-111 (warning) GUARDED is not supported. It is ignored %s

DESCRIPTION

WHAT NEXT

VHDL-112 (warning) TRANSPORT is not supported. It is ignored %s

DESCRIPTION

WHAT NEXT

VHDL-113 (warning) GUARDED and TRANSPORT are not

supported. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-114 (warning) Beginning designator '%s' does not match end designator '%s'
for construct %s

DESCRIPTION

WHAT NEXT

VHDL-115 (warning) Access types are not supported. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-116 (warning) File types are not supported. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-117 (warning) Record types are not supported. They are

ignored %s

DESCRIPTION

WHAT NEXT

VHDL-118 (warning) Physical types are not supported. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-119 (warning) Library clauses are not supported. They're

ignored %s

DESCRIPTION

WHAT NEXT

VHDL-120 (warning) Bus-resolution function ’%s’ ignored %s

DESCRIPTION

WHAT NEXT

VHDL-121 (error) Allocators are not supported %s

DESCRIPTION

WHAT NEXT

VHDL-122 (error) Cannot index into scalar variable ’%s’ %s

DESCRIPTION

WHAT NEXT

VHDL-123 (error) Cannot evaluate to expression or range %s

DESCRIPTION

WHAT NEXT

VHDL-124 (error) Cannot evaluate to range %s

DESCRIPTION

WHAT NEXT

VHDL-125 (error) Cannot cast expression to type ’%s’ %s

DESCRIPTION

WHAT NEXT

VHDL-126 (error) Multiple ’others’ clause in aggregate %s

DESCRIPTION

WHAT NEXT

VHDL-127 (error) Cannot mix named and positional elements in

same aggregate %s

DESCRIPTION

WHAT NEXT

VHDL-128 (error) Expected named element in aggregate %s

DESCRIPTION

WHAT NEXT

VHDL-129 (error) Illegal attribute or cast for ’%s’ %s

DESCRIPTION

WHAT NEXT

VHDL-130 (error) Cannot open file ’%s’

DESCRIPTION

WHAT NEXT

VHDL-131 (error) Syntax error %s

DESCRIPTION

WHAT NEXT

VHDL-132 (error) Can only assign to signals using ’<=’ %s

DESCRIPTION

WHAT NEXT

VHDL-133 (error) Multiple waveform elements are not supported %s

DESCRIPTION

WHAT NEXT

VHDL-134 (error) Cannot read from output port %s

DESCRIPTION

WHAT NEXT

VHDL-135 (error) Cannot assign to input port %s

DESCRIPTION

WHAT NEXT

VHDL-136 (error) Function parameters can only be of mode ’in’ %s

DESCRIPTION

WHAT NEXT

VHDL-137 (error) Procedure parameters cannot be of mode

’buf’ or ’linkage’

DESCRIPTION

WHAT NEXT

VHDL-138 (error) Cannot assign to signals using ’:=’ %s

DESCRIPTION

WHAT NEXT

VHDL-139 (warning) Label declarations are not valid VHDL %s

DESCRIPTION

WHAT NEXT

VHDL-140 (error) Unexpected unconstrained range

specification %s

DESCRIPTION

WHAT NEXT

VHDL-141 (error) Unexpected paranthesised list %s

DESCRIPTION

WHAT NEXT

VHDL-142 (error) Undefined variable %s %s

DESCRIPTION

WHAT NEXT

VHDL-143 (error) Unexpected range specification %s

DESCRIPTION

WHAT NEXT

VHDL-144 (error) Cannot constrain type %s

DESCRIPTION

WHAT NEXT

VHDL-145 (error) Syntax error: identifier expected

DESCRIPTION

WHAT NEXT

VHDL-146 (error) Syntax error: Illegal constraint %s

DESCRIPTION

WHAT NEXT

VHDL-147 (error) Syntax error: Empty paranthesised list %s

DESCRIPTION

WHAT NEXT

VHDL-148 (error) Cannot evaluate to expression %s

DESCRIPTION

WHAT NEXT

VHDL-149 (error) Cannot use type ’%s’ as variable %s

DESCRIPTION

WHAT NEXT

VHDL-150 (error) Port and generic names can only be simple

identifiers %s

DESCRIPTION

WHAT NEXT

VHDL-151 (error) Predefined attributes not supported for enumerated value ’%s’ %s

DESCRIPTION

WHAT NEXT

VHDL-152 (error) Predefined attributes supported only for arrays and ranges %s

DESCRIPTION

WHAT NEXT

VHDL-153 (error) Cannot evaluate expression to type %s

DESCRIPTION

WHAT NEXT

VHDL-154 (error) Return statement attempts to return

expression in a procedure

DESCRIPTION

WHAT NEXT

VHDL-155 (error) Type ’%s’ multiply defined %s

DESCRIPTION

WHAT NEXT

VHDL-156 (error) Package ’%s’ defined more than once %s

DESCRIPTION

More than one package body has been analyzed for a given package header. There are two ways this can happen: there are two bodies for a package in the file that was analyzed, or the package header and body are in separate files and the body was analyzed a second time.

WHAT NEXT

A package can have only one body. If a package has more than one body, remove all but one of them.

If the package header and body are in separate files and you need to reanalyze the package body (if it has changed, for example), you must reanalyze the package header before analyzing the new package body.

VHDL-157 (error) Package ’%s’ not found %s

DESCRIPTION

WHAT NEXT

VHDL-158 (error) Entity class must be ’type’ for enumeration

encoding %s

DESCRIPTION

WHAT NEXT

VHDL-159 (error) Attributes not supported for operator symbols %s

DESCRIPTION

WHAT NEXT

VHDL-160 (error) ’OTHERS’ and ’ALL’ not supported for attribute specification %s

DESCRIPTION

WHAT NEXT

VHDL-161 (error) Encoding for multiple types not supported in same specification %s

DESCRIPTION

WHAT NEXT

VHDL-162 (error) Type ’%s’ has already been assigned default

encoding %s

DESCRIPTION

WHAT NEXT

VHDL-163 (error) Number of enumerations specified is not equal to the number of
enumerations specified in the type %s

DESCRIPTION

WHAT NEXT

VHDL-164 (error) All encodings must be of equal length in

enumeration %s

DESCRIPTION

WHAT NEXT

VHDL-165 (error) ’while’ statement not supported %s

DESCRIPTION

WHAT NEXT

VHDL-166 (error) ’NEXT’ statement is not in loop %s

DESCRIPTION

WHAT NEXT

VHDL-167 (error) ’EXIT’ statement is not in loop %s

DESCRIPTION

WHAT NEXT

VHDL-168 (error) Cannot use OTHERS along with other

choices in a choice expression %s

DESCRIPTION

WHAT NEXT

VHDL-169 (error) Process name ’%s’ is not unique %s

DESCRIPTION

WHAT NEXT

VHDL-170 (error) Constant ’%s’ defined more than once %s

DESCRIPTION

WHAT NEXT

VHDL-171 (error) Cannot assign to constants %s

DESCRIPTION

WHAT NEXT

VHDL-172 (error) Component ’%s’ defined more than once %s

DESCRIPTION

WHAT NEXT

VHDL-173 (error) Attribute ’%s’ not supported %s

DESCRIPTION

WHAT NEXT

VHDL-174 (error) Incorrect form of ’wait’ statement %s

DESCRIPTION

WHAT NEXT

VHDL-175 (error) Wait statements not allowed in processes with sensitivity lists %s

DESCRIPTION

WHAT NEXT

VHDL-176 (error) Resource ’%s’ defined more than once %s

DESCRIPTION

WHAT NEXT

VHDL-177 (error) Synthesis attribute ’%s’ must be scoped

inside a design %s

DESCRIPTION

WHAT NEXT

VHDL-178 (error) Undefined resource '%s' %s

DESCRIPTION

WHAT NEXT

VHDL-179 (error) Iteration scheme required %s

DESCRIPTION

WHAT NEXT

VHDL-180 (warning) Configurations are not supported. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-181 (warning) Disconnection specifications are not

supported. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-182 (warning) Aliases are not supported. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-183 (warning) The REGISTER keyword is not supported. It is ignored %s

DESCRIPTION

WHAT NEXT

VHDL-184 (warning) The BUS keyword is not supported. It is ignored %s

DESCRIPTION

WHAT NEXT

VHDL-185 (warning) Files are not supported. They are ignored

%s

DESCRIPTION

WHAT NEXT

VHDL-186 (warning) Incomplete type declarations are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-187 (warning) Directive '%s' must be scoped inside a

subprogram %s

DESCRIPTION

WHAT NEXT

VHDL-188 (error) Error in manual resource binding syntax %s

DESCRIPTION

WHAT NEXT

VHDL-189 (warning) Attribute ’%s’ not supported %s

DESCRIPTION

WHAT NEXT

VHDL-190 (warning) Guard expression not supported for blocks %s

DESCRIPTION

WHAT NEXT

VHDL-191 (warning) Ports and generics not supported in block

statements %s

DESCRIPTION

WHAT NEXT

VHDL-192 (warning) Entity statement parts are not supported. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-193 (warning) Assertion statements are not supported. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-194 (warning) Generics are not supported. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-195 (warning) Timeout clause not supported in wait

statement %s

DESCRIPTION

WHAT NEXT

VHDL-196 (warning) Sensitivity list not supported in wait statement %s

DESCRIPTION

WHAT NEXT

VHDL-197 (warning) %s assumed to be of type ’integer’ %s

DESCRIPTION

WHAT NEXT

VHDL-198 (error) Entity class must be ’type’ for data_class attribute %s

DESCRIPTION

WHAT NEXT

VHDL-199 (error) Type ’%s’ has already been assigned a data

class %s

DESCRIPTION

WHAT NEXT

VHDL-200 (warning) Resource sharing attributes are effective only in processes and subprograms %s

DESCRIPTION

WHAT NEXT

VHDL-201 (warning) Sensitivity list for process not supported. It is ignored %s

DESCRIPTION

WHAT NEXT

VHDL-202 (error) Enumeration literal '%s' defined more than once in same enumeration type %s

DESCRIPTION

WHAT NEXT

VHDL-203 (warning) Expected semicolon (;) at end of statement

%s

DESCRIPTION

WHAT NEXT

VHDL-204 (warning) Expected "%s" %s

DESCRIPTION

WHAT NEXT

VHDL-205 (warning) ’THEN’ expected after condition following ’IF’ keyword %s

DESCRIPTION

WHAT NEXT

VHDL-206 (warning) ’SELECT’ expected after expression following ’WITH’ keyword %s

DESCRIPTION

WHAT NEXT

VHDL-207 (warning) ’IS’ expected after the expression following

’CASE’ keyword %s

DESCRIPTION

WHAT NEXT

VHDL-208 (warning) Initial values for signals not supported %s

DESCRIPTION

WHAT NEXT

VHDL-210 (error) ’%s’ declaration is not legal in a %s %s

DESCRIPTION

WHAT NEXT

VHDL-211 (error) An ’if’ statement is not a concurrent statement %s

DESCRIPTION

WHAT NEXT

VHDL-212 (error) A loop statement is not a concurrent

statement %s

DESCRIPTION

WHAT NEXT

VHDL-213 (warning) Dc script in %s '%s' ignored

DESCRIPTION

WHAT NEXT

VHDL-214 (error) Signal '%s' illegally redefined %s

DESCRIPTION

WHAT NEXT

VHDL-215 (error) End of file seen before %s block begun at line

%d was ended

DESCRIPTION

WHAT NEXT

VHDL-216 (error) Illegal reuse of ’%s’ %s

DESCRIPTION

WHAT NEXT

VHDL-218 (error) Variable %s is not defined as a record %s

DESCRIPTION

WHAT NEXT

VHDL-219 (error) Suffix of record is not a simple name %s

DESCRIPTION

WHAT NEXT

VHDL-220 (warning) Port ’%s’ does not exist %s "multiple_port" attribute ignored.

DESCRIPTION

WHAT NEXT

VHDL-221 (error) Architecture ’%s’ defined more than once for

same entity %s

DESCRIPTION

WHAT NEXT

VHDL-222 (error) Constant records are not supported %s

DESCRIPTION

WHAT NEXT

VHDL-223 (error) %s is supported only when it is of type ’integer’

%s

DESCRIPTION

WHAT NEXT

VHDL-224 (error) Cannot find declaration for component %s

DESCRIPTION

WHAT NEXT

VHDL-225 (error) %s is not a formal port of component %s

DESCRIPTION

WHAT NEXT

VHDL-226 (error) ’others’ is not legal as a formal name in a port map statement %s

DESCRIPTION

WHAT NEXT

VHDL-227 (error) In a port map statement, formals that are not simple names

or simple subelements are not supported %s

DESCRIPTION

WHAT NEXT

VHDL-228 (warning) Initial values are not supported for variables %s

DESCRIPTION

WHAT NEXT

VHDL-229 (error) ’%s’ must be a procedure %s

DESCRIPTION

WHAT NEXT

VHDL-230 (error) Compilation aborted. Too many errors.

DESCRIPTION

WHAT NEXT

VHDL-231 (error) Identifier %s is reserved for internal use. Please use a different

name for this entity %s

DESCRIPTION

WHAT NEXT

VHDL-232 (error) Cannot find entity %s

DESCRIPTION

The entity for the current architecture could not be found in the library.

WHAT NEXT

Provide the entity for the architecture.

VHDL-233 (warning) Port ’%s’ of component ’%s’ includes a default value, which is not supported for synthesis.

DESCRIPTION

Default values for ports of a component are not supported for synthesis. For example:

```
entity e is
  port (a: in bit;
        z: out bit);
end;

architecture a of e is
  component c
    port (p: in bit;
          q: in bit := ’1’;
          x: out bit);
  end component;

begin
  u1: c port map (p => a, x => z);
end;
```

WHAT NEXT

Remove the default value for the component port and add an equivalent association in

```
the port map of the component instantiation. For example:

architecture a of e is
  component c
    port (p: in bit;
          q: in bit;
          x: out bit);
  end component;

  constant c1: bit := '1';
begin
  u1: c port map (p => a, q => c1, x => z);
end;
```

VHDL-240 (warning) Dc_shell variable 'bin_path' has incorrect value.

DESCRIPTION

WHAT NEXT

VHDL-241 (warning) Cannot execute vhdl parser. Execution will continue with less error checking for the VHDL source.

DESCRIPTION

WHAT NEXT

VHDL-250 (error) Cannot create work directory for VHDL parser

DESCRIPTION

WHAT NEXT

VHDL-251 (error) Unable to initialize workspace for VHDL

parser

DESCRIPTION

WHAT NEXT

VHDL-252 (error) Abnormal exit of child process

DESCRIPTION

WHAT NEXT

VHDL-261 (error) Component name is not a simple name %s

DESCRIPTION

WHAT NEXT

VHDL-262 (warning) Only simple configurations (specification of architecture for a top
level entity) are supported. Nested block specifications and component

configurations are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-263 (error) Expected simple name for architecture %s

DESCRIPTION

WHAT NEXT

VHDL-264 (warning) Configuration specifications are not supported. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-265 (warning) The value ’%s’ of ’vhdlout_preserve_hierarchical_types’ is greater than that of ’vhdlout_single_bit’. ’vhdlout_preserve_hierarchical_types’ is changed to be equal to ’vhdlout_single_bit’.

DESCRIPTION

This error occurs when *vhdlout_preserve_hierarchical_types* is set to a higher value than *vhdlout_single_bit*.

The variables *vhdlout_single_bit* and *vhdlout_preserve_hierarchical_types* control how VHDLout handles types on ports and pins. See the manual pages on these variables for information on possible settings.

WHAT NEXT

Change the value of *vhdlout_single_bit* and/or *vhdlout_preserve_hierarchical_types* and retry the *write* command.

EXAMPLE MESSAGE

Error: The value 'ENUM' of *vhdlout_preserve_hierarchical_types* is greater than that of *vhdlout_single_bit*. *vhdlout_preserve_hierarchical_types* is changed to be equal to *vhdlout_single_bit*.

VHDL-266 (error) '%s' contains the invalid string '%s'.

DESCRIPTION

This error occurs when *vhdlout_single_bit* or *vhdlout_preserve_hierarchical_types* is set to an invalid value.

The variables *vhdlout_single_bit* and *vhdlout_preserve_hierarchical_types* control how VHDLout handles types on ports and pins. See the manual pages on these variables for information on possible settings.

WHAT NEXT

Correct the setting of the variable and retry the *write* command.

EXAMPLE MESSAGE

Error: 'vhdlout_preserve_hierarchical_types' contains the invalid string 'RNUM'.

VHDL-267 (error) The current setting, '%s', of 'vhdlout_package_naming_style' does not produce a valid VHDL identifier.

DESCRIPTION

VHDLout infers the name of the type-conversion package (if it is needed) from the variable *vhdlout_package_naming_style*. The setting of this variable must result in a legal VHDL identifier. See the manual page for *vhdlout_package_naming_style* for more details.

This error occurs when vhdlout_package_naming_style is set to a value that results in an illegal name for the type conversion package.

WHAT NEXT

Correct the setting of the variable and retry the *write* command.

EXAMPLE MESSAGE

Error: The current setting, '%s', of *vhdlout_package_naming_style* does not produce a valid VHDL identifier.

VHDL-268 (error) '%s' is not valid for 'vhdlout_package_naming_style'.

DESCRIPTION

VHDLout infers the name of the type-conversion package (if it is needed) from the variable *vhdlout_package_naming_style*. The setting of this variable must result in a legal VHDL identifier. See the manual page for *vhdlout_package_naming_style* for more details.

This error occurs when *vhdlout_package_naming_style* is set to a string that cannot be understood by VHDLout. The string (or substring) begins with a '%' followed by an unexpected character.

WHAT NEXT

Correct the setting of the variable and retry the *write* command.

EXAMPLE MESSAGE

Error: '%' is not valid for *vhdlout_package_naming_style*.

VHDL-269 (warning) The dc_script '%s' will be applied to all subsequent entities in this file.

DESCRIPTION

This use of dc_scripts is discouraged because it does not have the same scope as *library* and *use* clauses.

WHAT NEXT

To apply a dc_script to a single design unit, the script must be declared in the declarative region of that design unit.

You can suppress this message by setting the *suppress_errors* variable.

VHDL-270 (warning) Configurations are written out only when the 'vhdlout_single_bit' mode is 'vector'.

DESCRIPTION

Configurations between the test bench and your top-level design are written out only when the variable *vhdlout_single_bit* is set to type *vector*.

The purpose of the configuration is to map between the original and new types. If *vhdlout_single_bit* is set to *user*, the original types are used, and a configuration is unnecessary. If *vhdlout_single_bit* is set to *bit*, the new ports do not map well to the original types. In this case, a configuration is impractical.

WHAT NEXT

If you are using the original types (*vhdlout_single_bit* is set to *user*), you can ignore this message, or, to disable the writing of configurations, you can set *vhdlout_write_top_configuration* to "FALSE."

If you want to write out a configuration with your design, set *vhdlout_single_bit* to *vector*, and rewrite the design.

NOTE: Setting *vhdlout_single_bit* to *vector* does not affect the acceleration of your design.

VHDL-271 (error) Design %s contains a type with name matching the current setting of 'vhdlout_bit_type' (%s), that is more than one bit wide. Cannot write a VHDL description including this design.

DESCRIPTION

The 'vhdlout_bit_type' must be a one-bit wide type for VHDLout to be able to produce a legal description.

WHAT NEXT

Check your type definition and ensure it is one bit wide. If the type definition is an enumerated type with more than two possible values, it may be missing the ENUM_ENCODING attribute.

VHDL-272 (warning) You must change 'vhdlout_bit_type' to a bit type that includes a three-state value when writing out three-state resolution functions. If left as is, this description may or may not simulate.

DESCRIPTION

Vhdlout found a possible clash between two connected objects. An object A, that may drive a three-state value. An object B, being driven by object A and that is of a type not including a three-state value.

For example: a signal of type 'bit' may drive a port in mode 'inout'. This is legal and works as long as that port is never driven by the outside world. This may also happen if the source description language was less rigorous on types than VHDL.

Note that such a clash is cought by simulation during run-time.

WHAT NEXT

The alternatives are:

A - locate the clash and correct the HDL description, re-analyze, re-synthesize and re-write vhdl. In the example above, one can either use a resolved type for the signal or change the port's mode to 'out'.

B - leave as is and simulate to find out if this was a true error.

VHDL-273 (error) There is a latch in this un-compiled design. Unfortunately, this release cannot write VHDL for latches pre-compile.

DESCRIPTION

This will be fixed in a future release.

WHAT NEXT

Work around, compile design before writing out VHDL.

VHDL-274 (warning) Library cell %s has a pin of unsupported three-state driver type. It will be treated as a regular three-state driver type. The description may not simulate correctly.

DESCRIPTION

Driver type may be specified for three-state cell pins in Synopsys' Library format, which is used to describe technology libraries. This warning is issued when VHDLout is writing a behavioral description and don't recognize the driver type at hand. The resulting description may have problems simulating weak signal values properly.

Please inform Synopsys when this happens.

WHAT NEXT

This warning is issued only when vhdlout_equations = TRUE. The warning can be avoided by setting the variable to FALSE in which case a structural description is written. For such a description, the driver type isn't relevant to VHDLout.

An alternate approach is to use the dont_use attribute on the library cell in question, prior to compiling the design. Please refer to man-page for the dc_shell command set_dont_use for details.

VHDL-275 (warning) Library cell %s have three-state pins of different driver types, VHDLout cannot handle more than one type on same cell. All pins on this cell will be treated as regular three-state driver type. The description may not simulate correctly.

DESCRIPTION

Driver type may be specified for three-state cell pins in Synopsys' Library format, which is used to describe technology libraries. This warning is issued when VHDLout is writing a behavioral description and encounters different pin driver types on the same library cell. VHDLout is not capable of handling more than one driver type per cell.

The resulting description may have problems simulating weak signal values properly.

Please inform Synopsys when this happens.

WHAT NEXT

This warning is issued only when vhdlout_equations = TRUE. The warning can be avoided by setting the variable to FALSE in which case a structural description is written. For such a description, the driver type isn't relevant to VHDLout.

An alternate approach is to use the dont_use attribute on the library cell in question, prior to compiling the design. Please refer to man-page for the dc_shell command set_dont_use for details.

VHDL-276 (warning) The acceleratable VHDL description that you requested could not be written, because your design, '%s', cannot be described using the XP-supported VHDL subset. The VHDL description is being written without setting the BACKPLANE attribute.

DESCRIPTION

The XP accelerator accepts as input only a limited subset of VHDL constructs. A design that cannot be described using this subset is not acceleratable by the XP accelerator.

By setting the variable **vhdlout_target_simulator** to *XP*, you requested a VHDL output that is targeted at the XP accelerator. If **vhdlout_target_simulator** is set to *XP*, **write -f vhdl** attempts to describe the design using the XP-supported VHDL subset. If this is successful, then **write -f vhdl** adds the BACKPLANE attribute to the output VHDL file, indicating that the design is to be simulated using the XP Accelerator.

If, however, **vhdlout_target_simulator** is set to *XP* and the design cannot be described using the XP-supported VHDL subset, then **write -f vhdl** does not add the BACKPLANE attribute to the generated VHDL description, and issues this warning message.

The XP-supported VHDL subset cannot describe type conversions or user-defined types. (For more information on allowed types, refer to the ZyCad XP manuals.) If you receive this warning message, your design might require type conversions and/or might contain user-defined types.

WHAT NEXT

If your design contains user-defined types or requires type conversions, check the setting of the variable **vhdlout_single_bit** and, if it is set to USER, change it to VECTOR or BIT. Then re-execute **write -f vhdl**.

VHDL-277 (error) The VHDL PROCESS on line %d must be labelled.

DESCRIPTION

The process statement contains an attributed object in its scope and, as a result, must be labelled.

WHAT NEXT

Label the process statement.

VHDL-278 (error) The port '%s' in design '%s' has unknown direction.

DESCRIPTION

The VHDL writer does not know the port direction, so it cannot write it out. This is probably caused by some modules that are missing when reading Verilog files.

WHAT NEXT

Read in the complete design that has specified the port direction and try again.

VHDL-279 (warning) STD.TEXTIO package is not supported for synthesis.

DESCRIPTION

STD.TEXTIO package is not supported for synthesis.

WHAT NEXT

Remove the use of this package from the use clause

VHDL-280 (error) Only global constants are supported as the

index constraint for aliasing.

DESCRIPTION

Only global constants are supported as the index constraint for aliasing. Generics are also not supported in this position.

WHAT NEXT

Modify the alias declaration so that index constraint is a global constant.

VHDL-281 (error) You cannot take an index or slice of a non-vector alias %s.

DESCRIPTION

You received this message because you attempted to apply indexing or slicing to an alias that was not declared as a vector type.

Note that this error can occur even if the VHDL language permits indexing or slicing to be applied to the alias. For example, consider the following:

```
subtype T is bit_vector(0 to 2);
alias b: T is a(1 to 3);
```

In the alias declaration, HDL Compiler does not recognize 'T' as a vector type. Thus, this error will occur if any attempt is made to apply slicing or indexing to 'b'; for example, "b(0)" or "b(0 to 1)".

WHAT NEXT

Modify the alias declaration so that the type of the alias is an array type; for example, std_logic_vector. The example shown above could be rewritten as follows:

```
alias b: bit_vector(0 to 2) is a(1 to 3);
```

VHDL-283 (error) Aliased objects may only be a simple name, an index of a simple name, or a slice of a simple name.

DESCRIPTION

An attempt was made to declare an alias to a non-simple name. Aliases may be declared only for simple names, simple names with indexes, or simple names with

slices. For example, the following aliases are acceptible:

```
alias a: bit is foo;
alias a: bit is foo(0);
alias a: bit_vector(0 to 1) is foo(2 to 3);
```

WHAT NEXT

Modify the alias declaration so that the aliased object is either a simple name, an index of a simple name, or a slice of a simple name.

VHDL-284 (error) Arbitrary expression for bussed clock index is not supported.

DESCRIPTION

Arbitrary expression for a bussed clock index is not supported. Only single variable index or integer expressions are supported.

WHAT NEXT

Use supported expressions for a bussed clock index.

VHDL-285 (warning) "BAD CONNECTION - primary in/out port %s of %s is driven or read by an internal node. Using intermediate signal to generate a syntactically correct VHDL description. Consequently, this will violate the definition of structural VHDL description syntax."

DESCRIPTION

VHDL syntax rule does not allow primary port of "in" mode be updated by an internal node, or a primary port of "out" mode be read by an internal node. VHDL writer is generating an intermediate signal of the form portName_port to handle this bad connection, so it can write out a syntatically correct VHDL file. The intermediate signal will be assigned a value in the body of the architecture, and this signal assignment will violate the rule for structural VHDL description.

WHAT NEXT

Fix this bad connection in your design.

VHDL-286 (warning) There is a data discrepancy between synopsys database and the output file.

DESCRIPTION

VHDL/verilog writer detects that the names of the netlist objects have changed to fit syntax and semantic requirement for VHDL/verilog. The change might cause a back-annotation problem in the flow. For example, if the VHDL/verilog output file is used to generate sdf or saif file. The netlist object names in the sdf or sail might not able to back-annotate to synopsys database.

WHAT NEXT

Run the **change_names** command with the **-rule vhdl/verilog** and then rewrite the netlist.

SEE ALSO

change_names (2).

VHDL-287 (error) "BAD CONNECTION - port %s of mode other than out is unconnected. Consequently, this will violate the definition of structural VHDL description syntax."

DESCRIPTION

VHDL syntax rule does not allow port of mode other than "out" be unconnected.

WHAT NEXT

Run change_names to create a dummy net to connect the port.

VHDL-288 (error) "BAD CONNECTION - bussed port %s is partially connected."

DESCRIPTION

VHDL syntax rule does not allow bussed port to be partially connected.

WHAT NEXT

Run change_names to create a dummy net to connect each bit of the port.

VHDL-289 (error) Bussed clock is not longer supported in VHDLC. Use Presto VHDL instead.

DESCRIPTION

Bussed clock is no longer supported in VHDLC.

WHAT NEXT

Please either recode the VHDL source code, or use Presto VHDL instead.

VHDL-290 (warning) A dummy net '%s' is created to connect open pin '%s'.

DESCRIPTION

VHDL writer detects that a pin is not connected. The writer creates a dummy net connected to the pin to satisfy syntax requirement for VHDL. You may use variable vhdlout_unconnected_pin_prefix to control the prefix of the dummy nets. The dummy net appears in the output VHDL file only. It does not exist in the db file. To let db file contain dummy nets, change_names needs to be executed before VHDL writer.

WHAT NEXT

SEE ALSO

change_names (2). **vhdlout_unconnected_pin_prefix** (3).

VHDL-291 (warning) You are using an older version of the VHDL netlist reader/writer, which will be obsoleted in the X-

2005.06 release.

DESCRIPTION

You are using an older version of the VHDL netlist reader/writer, which will be obsoleted in the X-2005.06 release. To use the current VHDL reader/writer, please make sure these variables are set as follows:

VHDL netlist reader: enable_2003.03_vhdl_reader true VHDL netlist writer: enable_2003.03_vhdl_writer true

WHAT NEXT

SEE ALSO

VHDL-292 (error) Verilog In Error, %d modules are possible top modules.

DESCRIPTION

Unsupport more then one top modules.

WHAT NEXT

Please check the design file, and make sure there is only one top module.

VHDL-2001 (warning) Statements in an entity declaration are not supported for synthesis. They are ignored in entity %s %s

DESCRIPTION

WHAT NEXT

VHDL-2021 (warning) ’BUS’ and ’REGISTER’ signal kinds are

not supported for synthesis. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-2022 (warning) Initial values for signals are not supported for synthesis. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-2023 (warning) Type of the generic is assumed to be ’Integer’ in synthesis %s

DESCRIPTION

WHAT NEXT

VHDL-2024 (error) Only generics of type INTEGER are supported for synthesis. - %s

DESCRIPTION

The synthesis VHDL subset only includes generics of type integer.

WHAT NEXT

VHDL-2035 (warning) Type %s has already been assigned

default encoding %s

DESCRIPTION

WHAT NEXT

VHDL-2040 (warning) Attribute %s not supported for synthesis %s

DESCRIPTION

WHAT NEXT

VHDL-2041 (warning) Alias declarations are not supported for synthesis. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-2042 (warning) File declarations are not supported for synthesis. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-2043 (warning) Disconnection specifications are not

supported for synthesis. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-2045 (warning) Guard conditions for blocks are not supported %s

DESCRIPTION

WHAT NEXT

VHDL-2046 (warning) Declaration and use of generics and ports in a block header is not supported %s

DESCRIPTION

WHAT NEXT

VHDL-2047 (error) The attribute '%s' defined on line %d is not contained within an architecture. Attribute '%s' only applies to processes, and it must be defined inside of the architecture that contains the process.

DESCRIPTION

Attributes that need to be applied to processes must occur inside of the architecture that contains them.

WHAT NEXT

Move the attribute to inside of the architecture.

VHDL-2048 (error) Could not find process '%s' inside of the architecture%s
at line %d. The process is referred to by the attribute '%s' defined on line %d.

DESCRIPTION

The attribute '%s' is meant to apply to processes only, and the process defined could not be found.

WHAT NEXT

Check the names of the processes and the definition of the attribute for errors.

VHDL-2049 (Warning) The attribute '%s' is only valid when applied to
one of the following:
%s.
On line %d, the attribute is applied to a(n) %s.
The attribute will be ignored.

DESCRIPTION

The name attribute is only allowed to attribute certain classes.

WHAT NEXT

Check to make sure that the attribute is applied to the correct object.

VHDL-2050 (warning) Timeout clause not supported for

synthesis in wait statement %s

DESCRIPTION

WHAT NEXT

VHDL-2060 (error) The translate_on/translate_off pragma has been incorrectly used here
inside a construct %s.

DESCRIPTION

Only use the translate_on and translate_off pragmas on complete constructs, not on parts of constructs. For example, do not use these pragmas to comment out one of more branches of a "case" statement or the "if" construct as shown in the following examples.

Example 1

```
. . .
-- pragma translate_off
if (Is_X(svec))  then
  assert (now < 20 ns)
    report "logic vector contains U, X, Z or W"
    severity error;
else
-- pragma translate_on
  if ( t > 20) then  -- synthesize this RTL
    . . .
-- pragma translate_off
end if;
-- pragma translate_on
. . .
```

Example 2

```
. . .
case (expr_1) is
  -- pragma translate_off
  when value_1 =>  -- incomplete case statement missing this branch
    . . .
  -- pragma translate_on
  when value_2 =>
```

```
    . . .
  when . . .
    . . .
end case;
```

WHAT NEXT

Modify the placement of translate_on and translate_off pragmas. When you use the translate_on and translate_off pragmas, use them around the entire "if"/"case" statement. When this isn't possible, then "translate_off" parts of a construct that aren't part of VHDL syntax. In the modified example below, the "if", "then" and "else" constructs are all "translated", the "else" clause is interpreted to synthesis as a "null".

Example 1

```
. . .
temp := (others => "X");
if (svec /= temp)  then
  if ( t > 20) then  -- synthesize this RTL
    . . .
else
-- pragma translate_off
  assert (now < 20 ns)
    report "logic vector contains U, X, Z or W"
    severity error;
-- pragma translate_on
end if;
. . .
```

Example 2

```
. . .
case (expr_1) is
  when value_1 =>
  -- pragma translate_off
    . . .
  -- pragma translate_on
  when value_2 =>
    . . .
  when . . .
    . . .
end case;
```

VHDL-2090 (warning) Declarations in a configuration declaration statement are not supported for synthesis. They are

ignored %s

DESCRIPTION

WHAT NEXT

VHDL-2091 (warning) Configuration specifications are not supported for synthesis %s

DESCRIPTION

WHAT NEXT

VHDL-2092 (warning) Only simple configurations (specification of architecture for a top
level entity) are supported for synthesis. Nested block specifications and component
configurations are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-2093 (error) Access types are not supported for synthesis %s

DESCRIPTION

WHAT NEXT

VHDL-2094 (warning) File types are not supported for

synthesis. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-2095 (warning) Physical types are not supported for synthesis. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-2096 (warning) Incomplete type declarations are not supported for synthesis. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-2097 (warning) Signal assignment delays are not supported for synthesis. They are ignored %s

DESCRIPTION

WHAT NEXT

VHDL-2098 (warning) 'Transport' construct is not supported for

synthesis. It is ignored %s

DESCRIPTION

WHAT NEXT

VHDL-2099 (warning) Assert and report statements are not supported for synthesis. They are ignored %s

DESCRIPTION

The VHDL "assert" and "report" statements have no meaning for synthesis. These statements are ignored by HDL Compiler.

WHAT NEXT

VHDL-2100 (error) Allocators are not supported for synthesis %s

DESCRIPTION

WHAT NEXT

VHDL-2103 (error) %s

DESCRIPTION

Slang functions cannot have a return data-type that is unconstrained. The return-type cannot be a record or multi-dimensional array.

The legal data types allowed are:

Scalar types: enumeration, integer, physical, floating-point Composite types: single dimensional array only Access Types File Types

Slang procedures and functions cannot have parameters whose data-type is a record or multi-dimensional array.

The legal data types allowed are:

Scalar types: enumeration, integer, physical, floating-point Composite types: single dimensional array only Access Types File Types

WHAT NEXT

VHDL-2104 (error) indexing of access-type line is not supported %s

DESCRIPTION

WHAT NEXT

VHDL-2105 (error) The suffix all is not supported %s

DESCRIPTION

WHAT NEXT

VHDL-2106 (error) generalized Wait statements are supported only in architectures that are attributed as TESTBENCH %s

DESCRIPTION

WHAT NEXT

VHDL-2107 (error) generalized Wait statements are not supported in architectures whose TESTBENCH attribute is not

set TRUE %s

DESCRIPTION

WHAT NEXT

VHDL-2108 (error) Wait statements are not supported in subprograms %s

DESCRIPTION

WHAT NEXT

VHDL-2109 (error) Event and Stable attributes are not supported in subprograms %s

DESCRIPTION

WHAT NEXT

VHDL-2110 (error) An expression of this kind is supported for synthesis, when only one variable is used. This expression has two variables %s and %s %s

DESCRIPTION

WHAT NEXT

VHDL-2111 (error) Aggregate assignment by name is not

supported for the field names of a record.

DESCRIPTION

The fields of a record were assigned using named aggregate assignment, which is not supported for synthesis. The following is an example of this style of assignment:

```
  type myrec_type is record
    vecpart : bit_vector(0 to 4);
    count   : integer range 0 to 4;
  end record;

  signal myrec : myrec_type;

    ...

  myrec <= (vecpart => input_vecpart, count => input_count);
```

In the above example, "vecpart" and "count" are fields of a record. For records, aggregate assignment using named notation is not supported.

WHAT NEXT

Assign each field of the record individually, or use positional notation. The following example shows both positional notation and assignment of each field individually.

```
  type myrec_type is record
    vecpart : bit_vector(0 to 4);
    count   : integer range 0 to 4;
  end record;

  signal myrec_positional : myrec_type;
  signal myrec_eachfield  : myrec_type;

   ...

  myrec_eachfield.vecpart <= input_vecpart;
  myrec_eachfield.count   <= input_count;

  myrec_positional <= (input_vecpart, input_count);
```

VHDL-2112 (error) %s

DESCRIPTION

File names in the file declaration should be constants, generics or constant string literals. Use of expression or argument of the subprogram parameter is not supported by Cyclone.

WHAT NEXT

VHDL-2120 (error) In a port map statement, formals that are not simple names or simple subelements are not supported for synthesis %s

DESCRIPTION

WHAT NEXT

VHDL-2121 (error) Type conversion on formal associations is not supported for synthesis %s

DESCRIPTION

WHAT NEXT

VHDL-2130 (error) Only simple configurations are supported for synthesis. This configuration declaration is not supported %s

DESCRIPTION

WHAT NEXT

VHDL-2131 (error) Configurations are not supported for direct instantiation during synthesis %s.

DESCRIPTION

```
The following usage is not supported in VHDL Compiler.

LABEL: configuration library_name.configuration_name
            generic map (...)
port map (...);
```

WHAT NEXT

VHDL-2132 (warning) Explicit architecture specification is not supported for direct instantiation during synthesis %s.

DESCRIPTION

```
The following usage is not correct in VHDL Compiler.

LABEL: library_name.entity_name(architecture_name)
            generic map (...)
port map (...);

VHDL Compiler reads the architecture to be used from the .mra file. Therefore, only
the most recently analyzed one is meaningful to synthesis.
```

WHAT NEXT

```
Remove the architecture specification from the statement and analyze the
architecture you want to use first.
```

VHDL-2140 (error) Multi-dimensional arrays are not supported for synthesis %s

DESCRIPTION

WHAT NEXT

VHDL-2141 (error) Multiple waveform elements are not supported for synthesis %s

DESCRIPTION

WHAT NEXT

VHDL-2142 (error) Attribute ‘RANGE or ‘REVERSE_RANGE

can’t have index with it %s.

DESCRIPTION

Multiple-dimensional array is not supported for synthesis. So ‘RANGE(i) or ‘REVERSE_RANGE(i) is meaningless for synthesis.

WHAT NEXT

VHDL-2150 (error) This form of wait statement is not supported for synthesis %s

DESCRIPTION

WHAT NEXT

VHDL-2151 (error) Attribute %s%s is not supported for synthesis %s

DESCRIPTION

WHAT NEXT

VHDL-2152 (error) Literal ’%s’ is not supported for synthesis %s

DESCRIPTION

WHAT NEXT

VHDL-2153 (error) Physical types are not supported for

synthesis %s

DESCRIPTION

WHAT NEXT

VHDL-2154 (error) Cannot mix named and positional elements in same aggregate for synthesis %s

DESCRIPTION

WHAT NEXT

VHDL-2155 (error) Deferred constants are not supported for synthesis %s

DESCRIPTION

WHAT NEXT

VHDL-2156 (error) Floating point types are not supported for synthesis %s

DESCRIPTION

The VHDL predefined type "REAL" is an example of a floating point type.

WHAT NEXT

Remove any floating point types from the VHDL source.

VHDL-2157 (error) Type %s not found %s

DESCRIPTION

This error occurs if a type is used but not declared. It is likely to happen if the type declaration is enclosed in *translate_off* or *synthesis_off* comments.

WHAT NEXT

Declare the type before you use it.

VHDL-2158 (error) Record types (%s) are not supported in generic declarations for synthesis %s

DESCRIPTION

Record types are not support in generics, only in ports, signals variables, and constants.

WHAT NEXT

Use multiple smaller generics.

VHDL-2159 (error) Empty string constants are not supported for synthesis %s.

DESCRIPTION

A string with no characters or spaces is not supported by VHDL Compiler. For example, the following is not supported:

```
entity test is
  generic(str : string := "");  -- This is not supported
  port(data_in  : in std_logic;
       data2_in : in std_logic;
       data_out : out std_logic);
end test;
architecture one of test is
constant c1 : string := "";  -- This is not supported
begin
end test;
```

WHAT NEXT

Use a blank string (i.e. " ") instead of an empty string (i.e. ""). The above code should be modified to:

```
entity test is
  generic(str : string := " ");  -- Add a space.  This is allowed.
  port(data_in  : in std_logic;
       data2_in : in std_logic;
       data_out : out std_logic);
end test;
architecture one of test is
constant c1 : string := " ";  -- Add a space.  This is allowed.
begin
end test;
```

VHDL-2160 (error) The ’event or ’stable attribute (%s) is supported only when the attribute is used in conformance with the style described in the Synopsys manual for the VHDL compiler.

DESCRIPTION

An example of the use of the *’event* attribute is:

```
if (clk’event and clk = ’1’) then ...
```

or

```
wait until clk’event and clk = ’1’;
```

An example for the use of the ’stable attribute is:

```
if (not clk’stable and clk = ’1’) then ...
```

or

```
wait until not clk’stable and clk = ’1’;
```

This error will occur in cases such as the following:

```
if(clock’event and clock = ’1’ and enable = ’1’) then ...
```

or

```
wait until clk’stable and clk = ’1’;
```

WHAT NEXT

Modify the statement containing the *'stable* or *'event* attribute so that it is in conformance with the suggested style.

VHDL-2161 (warning) Synopsys attribute %s's value is not set to TRUE, the attribute is ignored %s

DESCRIPTION

This is a Boolean attribute. To have any effect, it must be set to "TRUE."

WHAT NEXT

Check that the attribute specification assigns the value "TRUE." Case doesn't matter.

VHDL-2162 (error) Usage of parameters or variables declared in parent subprogram is not supported %s

DESCRIPTION

VHDL Compiler doesn't allow parameters or variables declared in parent subprogram to be used in nested child subprograms. For Example, the following usage of "j" and "v" are prone to bad logic:

```
library ieee ;
use ieee.std_logic_1164.all ;
entity my_test is
port( d                : in std_logic ;
       q                : out std_logic
    );
end  my_test ;
architecture synthesize of my_test is
begin
    process(d)
        procedure outer_procedure(signal j : out std_logic) is
        variable v : std_logic;
            procedure inner_procedure is
            begin
                j <= v;
            end ;
        begin
            v := '1';
            inner_procedure(j);
```

```
        end ;
    begin
        outer_procedure(q);
    end process;
end  synthesize ;
```

WHAT NEXT

Change the usage of parameters or variables in your VHDL code.

VHDL-2163 (error) The rising_edge or falling_edge function (%s) is supported only when used in conformance with the style described in the VHDL Compiler Reference Manual.

DESCRIPTION

You receive this error message if you use the *rising_edge* or *falling_edge* function in a way that does not conform to the style described in the *VHDL Compiler Reference Manual*.

The following are examples of uses that would generate this error message.

```
if rising_edge( ck ) and enable = '1' then ...
```

or

```
if falling_edge( ck ) and ck = '0' then ...
```

The following is an example of a supported use of the *rising_edge* function.

```
if rising_edge( ck ) then ...
```

or

```
wait until rising_edge( ck );
```

Similarly, the following is an example of a supported use of the *falling_edge* function.

```
if falling_edge( ck ) then ...
```

or

```
wait until falling_edge( ck );
```

WHAT NEXT

Refer to the *VHDL Compiler Reference Manual* and modify the statement containing the

rising_edge or *falling_edge* function so that it conforms to the suggested style. Then, re-execute the command.

VHDL-2201 (error) An entity named '%s' already exists in this library. (It may be an internal Synopsys design). Please use a different name for your entity.

DESCRIPTION

WHAT NEXT

VHDL-2202 (error) %s is the name of an internal Synopsys design. Please use a different name for your entity.

DESCRIPTION

WHAT NEXT

VHDL-2203 (error) Cannot find entity %s %s

DESCRIPTION

WHAT NEXT

VHDL-2204 (error) Could not find object %s %s. This error can occur if a
package (%s) that exists in memory also exists in another library referred to
in a Library statement. This error can also occur if the package uses

synthesis_off/synthesis_on directives around the object.

DESCRIPTION

This error occurs because the synthesis tool searches for packages in memory before it searches the libraries.

A package exists in memory if it has been analyzed in the current session of the tool. The error can also occur if two or more libraries have packages of the same name and if the packages are used in the same design.

If the object contains synopsys synthesis_off/on or translate_off/on directives around it, the object is not synthesized. As a result, the object cannot be found when it is referenced in the design. The problem can also occur if the directives are placed incorrectly around part of the object. For example, consider the following procedure declaration:

```
procedure my_proc (variable data_in: in std_logic;
                   variable clk: in std_logic;
                   variable data_out: out std_logic;
-- synopsys synthesis_off
                   variable delay: in time);
-- synopsys synthesis_on
```

In this case, the directives have not been inserted properly, so the procedure is not synthesized. To make the code usable for both synthesis and simulation, this procedure declaration should be:

```
procedure my_proc (variable data_in: in std_logic;
                   variable clk: in std_logic;
                   variable data_out: out std_logic
-- synopsys synthesis_off
                   ;
                   variable delay: in time
-- synopsys synthesis_on
   );
```

WHAT NEXT

To get around this problem, if you have more than one package of the same name (even if they are in different libraries), rename one of the packages. If you do not have more than one package of the same name, analyze the package and the design that uses the package in separate sessions of **dc_shell** or **design_analyzer.**

If the problem has to do with the synthesis_off/on or translate_off/on directives, modify the code to use the directives appropriately. Please see the DESCRIPTION section above for additional information on this.

VHDL-2205 (warning) Package '%s' defined more than once %s

DESCRIPTION

This warning occurs if the same package is multiply declared in same HDL source file.

It also occurs if multiple HDL source files are read by the same **read** or **analyze** command *and* if the same package is defined in more than one of the files.

WHAT NEXT

Be sure to read or analyze a package only once.

VHDL-2206 (error) You have declared two architectures with the same name %s %s

DESCRIPTION

You are using two (or more) architectures with the same name, belonging to the same entity.

WHAT NEXT

Rename the architecture(s) so that they have unique names.

VHDL-2207 (error) You have declared a component inside a for generate loop.

DESCRIPTION

VHDL-compiler does not allow component declaration inside a for generate loop.

WHAT NEXT

Move the component declaration outside the for loop.

VHDL-2221 (error) Type %s is not defined %s

DESCRIPTION

WHAT NEXT

VHDL-2230 (error) ’%s’ used more than once as the label for an instance.

DESCRIPTION

This error occurs if two or more instances in the same scope are labelled with the same name using the "label" pragma.

WHAT NEXT

Change the names of one instances to make them distinct. You can do this by changing the label pragma for each instance.

VHDL-2231 (error) Undefined resource %s %s

DESCRIPTION

WHAT NEXT

VHDL-2232 (error) Entity class must be ’type’ for data_class attribute %s

DESCRIPTION

WHAT NEXT

VHDL-2233 (error) Type %s has already been assigned a data

class %s

DESCRIPTION

WHAT NEXT

VHDL-2234 (error) Object %s not found %s

DESCRIPTION

An object was referenced but not declared. This can happen if a pragma *synthesis_off* hides the declaration.

WHAT NEXT

Change the HDL description so that the declaration is visible for the HDL Compiler.

VHDL-2235 (warning) Type %s not found %s

DESCRIPTION

WHAT NEXT

VHDL-2236 (warning) Pragma "out_port_type" must have exactly two arguments %s

DESCRIPTION

WHAT NEXT

VHDL-2237 (warning) The pragma ’%s’ on line %d is not a supported pragma

It will be ignored.

DESCRIPTION

This error is given when the user has a comment of the form

-- pragma <pragma_name>

And the pragma_name is not one of the pragmas that is supported.

WHAT NEXT

This is just a warning, so no action is required. However, the user may want to check the pragma_name to see if it has been mis-typed.

VHDL-2241 (error) Cannot encode multiple types in same attribute specification %s

DESCRIPTION

WHAT NEXT

VHDL-2242 (error) All encodings must be of equal length in enumeration %s

DESCRIPTION

WHAT NEXT

VHDL-2243 (error) The value of Synopsys attribute %s is expected to be name of port, signal or variable %s

DESCRIPTION

The attribute value does not match the name of an object of the class of port, signal, or variable.

WHAT NEXT

Change the attribute value.

VHDL-2244 (error) Synopsys attribute %s's value is expected to be name of a process label %s

DESCRIPTION

The attribute value does not match name of a process label.

WHAT NEXT

Change the attribute value.

VHDL-2245 (error) Label %s already has a Synopsys set_reset attribute %s

DESCRIPTION

The process label has more than one Synopsys *set_reset* attribute, which is illegal.

WHAT NEXT

Change source code to put only one *set_reset* attribute on the process.

VHDL-2246 (error) More than one Synopsys attribute master_process_is and/or slave_process_is specified for same process label %s

DESCRIPTION

A process label can have only one *master_process_is/slave_process_is* attribute.

WHAT NEXT

Change source code to put only one attribute on the process.

VHDL-2247 (error) Pragma translate_off inside an expression is not supported %s

DESCRIPTION

Inside an expression, the VHDL Analyzer cannot deal with pragma *translate_off* or *translate_on*.

WHAT NEXT

In the case of an after-clause, like the example below, take out the pragmas. After-clauses are ignored for synthesis. A warning is issued in that case.

To suppress warnings, refer to the man page for the *suppress_errors* variable.

EXAMPLE

The following example will cause error VHDL-2247:

```
    entity pragma is
        port ( iput : in bit; oput : out bit);
    end pragma;

    architecture test of pragma is
    begin
oput <= iput
        -- synopsys translate_off
        AFTER 7 ns
        -- synopsys translate_on
        ;

    end test;
```

VHDL-2248 (error) Body of package %s seen before or without its declaration %s

DESCRIPTION

The package declaration must be analyzed before the corresponding package body. There was probably a problem with the declaration part related to the synthesis subset, causing the analysis of the declaration to terminate. Since the analysis of the package declaration was terminated, the body cannot be analyzed.

WHAT NEXT

Correct the problem in the package declaration, and this error will go away.

EXAMPLE

This example will cause error VHDL-2248:

```
package P is
  constant    C : bit; -- deferred constant, not supported by synthesis.
end P;

package body P is
  constant    C : bit := '0';
end P;
```

VHDL-2249 (warning) The attribute '%s' requires a list of more than one signal %s.

DESCRIPTION

WHAT NEXT

VHDL-2250 (warning) Incorrect computation may result because range of the left hand side does not cover range of the right hand side for assignment %s.

DESCRIPTION

When the value of the right-hand side is outside the range of the left-hand side, a run-time error occurs in simulation. However, no logic is built by the VHDL Compiler to detect this kind of run-time error.

WHAT NEXT

Declare a proper range for the left-hand side. Or type-convert the right-hand side to ensure that the range of the left-hand side covers that of the right-hand side.

VHDL-2251 (error) Enabling expression not permitted outside

wait statements %s

DESCRIPTION

This error occurs with statements of the form: if(clk'event and clock = '1' and enable = '1') then .. Such expressions are only permitted in: wait until clk'event and clock = '1' and enable = '1' ... at present

WHAT NEXT

Modify the if statement with the enabling condition to conform to suggested style.

VHDL-2252 (information) Make sure there is an assertion statement in the design for attribute '%s' %s.

DESCRIPTION

Attribute 'one_hot' indicates at most one object in its group can have a *Logic1* value at any instance of time, all other objects must have a *Logic0* value. Attribute 'one_cold' indicates at most one object in its group can have a *Logic0* value at any instance of time, all other objects must have a *Logic1* value.

WHAT NEXT

For *"attribute one_hot of c1, c2, c3 : signal is "true"*, add a process in the design like the following exmaple.

```
-- synopsys synthesis_off
process (c1, c2, c3)
begin
  assert not ((c1='1' and c2='1') or
              (c1='1' and c3='1') or
              (c2='1' and c3='1'))
    report "One-hot violation"
      severity Error;
end process
-- synopsys synthesis_on
```

For *"attribute one_cold of c1, c2, c3 : signal is "true"*, add a process in the design like the following exmaple.

```
-- synopsys synthesis_off
process (c1, c2, c3)
begin
  assert not ((c1='0' and c2='0') or
```

```
              (c1='0' and c3='0') or
              (c2='0' and c3='0'))
    report "One-cold violation"
      severity Error;
end process
-- synopsys synthesis_on
```

VHDL-2253 (error) Unsupported type of value in attribute specification - %s.

DESCRIPTION

Synthesis VHDL subset does not include this type of a value in a attribute specification. Value could be of concatenation type.

WHAT NEXT

Rewrite the attribute specification using the VHDL synthesis subset.

VHDL-2254 (error) "Time" is an unsupported type - %s

DESCRIPTION

Synthesis VHDL subset does not include the VHDL type TIME. Your HDL should not depend on simulation-specific delays for its proper behavior.

WHAT NEXT

You can prevent synthesis from using simulation-specific HDL by enclosing it within the synthesis_off / synthesis_on pragmas.

EXAMPLE

The following is a sample usage of the TIME type used in a declaration:

```
GENERIC( DelayAmount : TIME );
```

To prevent the TIME type from going through synthesis, change the above HDL to:

```
GENERIC( --synopsys synthesis_off DelayAmount : TIME --synopsys synthesis_on );
```

This will ensure the HDL is present for simulation, but is ignored during synthesis.

VHDL-2255 (error) Generics of type string are not supported - %s

DESCRIPTION

Synthesis VHDL subset does not include generics of type string.

WHAT NEXT

Rewrite the attribute specification using the VHDL synthesis subset.

VHDL-2256 (error) Range of enum types is not supported %s.

DESCRIPTION

Ranges of enumerated types using the *TO* construct are not supported in VHDL Compiler. The following *CASE* statement using the *TO* construct is not supported.

```
type STATE_TYPE is (STATE0, STATE1, STATE2, STATE3);
signal STATE, NEXT_STATE : STATE_TYPE;

process
begin
  case STATE is
  when STATE0 =>
       DOUT <= '0';
  when STATE1 to STATE3  =>
       DOUT <= '1';
  end case;
end process;
```

WHAT NEXT

The workaround is to use the "|" construct which performs an *OR* operation.

```
type STATE_TYPE is (STATE0, STATE1, STATE2, STATE3);
signal STATE, NEXT_STATE : STATE_TYPE;

process
begin
```

```
    case STATE is
    when STATE0 =>
         DOUT <= '0';
    when STATE1 | STATE2 | STATE3 =>
         DOUT <= '1';
    end case;
  end process;
```

VHDL-2257 (error) unsupported function call %s

DESCRIPTION

Some remote functions can not be called.

WHAT NEXT

Move to a local package.

VHDL-2260 (error) Bit-slice is not supported in generic for '%s', %s.

DESCRIPTION

Bit slices in the generic map of a component instantiation are not supported. For example:

```
U1: GATE1  generic map ( INIT(0) => '0', INIT(1 to 7 ) => init_val)
           port map ( DINPUT(0) => d0, DINPUT(1) => d1, DOUTPUT => dout );
```

WHAT NEXT

Concatenate the values assigned to slices in the generic map or port map. Assign this concatenation to an intermediate signal or variable, and use this signal or variable in the component instantiation. For example:

```
aggr1 <= ('0' & init_val);
U1: GATE1  generic map ( INIT => aggr1 )
           port map ( DINPUT(0) => d0, DINPUT(1) => d1, DOUTPUT => dout );
```

VHDL-2262 (error) Enumeration values may not be used as for

or for-generate loop bounds

DESCRIPTION

Enumeration values may not be used to define the bounds of a for or for-generate loop in Synopsys' synthesizable subset of VHDL. These bounds must be integer values that can be computed at compile time.

VHDL-2263 (error) Number of enumeration encoding values does not match the number of enumeration values, line %d.

DESCRIPTION

The number of enumeration encoding values defined via the ENUM_ENCODING attribute must match the number of enumeration values for the type.

WHAT NEXT

Modify the number of enumeration or enumeration attribute values.

VHDL-2264 (error) Incorrect way to use '%s attribute .

DESCRIPTION

WHAT NEXT

event and 'stable attributes are allowed to be used only when inferring a clock edge . For example

```
(clock'event and clock = '1')

and

((not clock'stable) and clock = '1')
```

following are not allowed

```
((not clock'event and clock = '1')

and

(clock'stable and clock = '1')
```

VHDL-2270 (error) The alias declaration%sis invalid because object %s is an alias. Aliases to existing aliases are not supported for synthesis .

DESCRIPTION

HDL Compiler supports aliases to signals, variables and constants only. HDL Compiler does not support aliases that refer to existing aliases.

WHAT NEXT

Either remove the alias to an alias and replace references to the first alias with references to the second, or replace the second alias with an alias to the original object. For example, given:

```
signal B : std_logic_vector(0 to 31); alias MSB : std_logic_vector(0 to 7) of B(24 to 31); alias MSN : std_logic_vector(0 to 3) of MSB(4 to 7);

...

MSN <= "0000";
```

You could remove the definition of MSN and replace its use with:

```
MSB(4 to 7) <= "0000";
```

Or, you could transform the declaration of MSN and leave its use intact:

```
alias MSN : std_logic_vector(o to 3) of B(28 to 31);

...

MSN <= "0000";
```

VHDL-2271 (error) Cannot use predefined attributes with alias %s%s, as the alias’s range is not locally static.

DESCRIPTION

HDL Compiler does not support the use of predefined attributes (such as ’LEFT, ’HIGH, ’RANGE, and so on) with aliases when the alias range is not locally static.

WHAT NEXT

Replace the predefined attribute with the corresponding components of the alias’s range. For example, given

```
procedure foo(B : inout std_logic_vector) is begin constant b_left : integer :=
B'length-1; alias b_alias : std_logic_vector(b_left downto 0) of B;

...

for I in b_alias'RANGE loop ... end loop;

... end foo;

replace the loop with

for I in 0 to b_left loop ... end loop;
```

VHDL-2280 (error) 'IMAGE is used outside of an attribute statement in a for-generate loop.

DESCRIPTION

HDL Compiler supports the 'IMAGE attribute only as part of an attribute specification of the following type:

```
attribute RELATIVE_LOCATION of <object> : label is <string_literal> &
INTEGER'IMAGE(<indexvar>) & <string_literal>
```

Where <indexvar> is the index variable of a for-generate loop.

WHAT NEXT

The following is an example of the situation in which 'IMAGE might be used.

```
G : FOR d IN 0 TO 7 GENERATE B : BLOCK ATTRIBUTE RELATIVE_LOCATION OF flop : LABEL
IS "R" & INTEGER'IMAGE(d) & "C0"; BEGIN flop : dff PORT MAP (D => INP(d),
Q=>OUTP(d), CK=>CLK); END BLOCK; END GENERATE G;
```

In this case, you're instantiating a set of eight DFFs that will be used to latch the value of an eight-bit bus. Note that 'IMAGE can be used only

+ Within a block within a for-generate loop.
+ As part of an attribute statement, where the attribute name is "RELATIVE_LOCATION" and the value is a concatination of three strings: a prefix, the 'IMAGE expression, and a suffix. In the previous example, "R" is the prefix and "C0" is the suffix. The prefix and suffix must be literals.
+ With the index variable for the for-generate loop.

Note that choices for the following are left to you:

+ The label for the for-generate loop and the block.
+ The number and contents of the instantiation statements within the block.

You can also specify more than one entity name in the attribute statement. For example, you can use

ATTRIBUTE RELATIVE_LOCATION OF flop,rflop : LABEL IS "R" & INTEGER'IMAGE(d) & "C0";

if you were instantiating two series of entities:

flop : dff PORT MAP (D => INP(d), Q=>OUTP(d), CK=>CLK); rflop : dff PORT MAP (D => INP(d), Q=>R_OUTP(8-d), CK=>CLK);

You can also have more than one such attribute statement if you want to specify a different prefix or suffix.

VHDL-2281 (error) The attribute RELATIVE_LOCATION does not have a value of the form <string_literal> & INTEGER'IMAGE(<indexvar>) & <string_literal>

DESCRIPTION

HDL Compiler supports the use of the RELATIVE_LOCATION attribute only with a very specific value. The attribute statement must be of the form:

attribute RELATIVE_LOCATION of <object> : label is <string_literal> & INTEGER'IMAGE(<indexvar>) & <string_literal>

Where <indexvar> is the index variable of a for-generate loop.

WHAT NEXT

The following is an example of the situation in which you may use the attribute RELATIVE_LOCATION:

G : FOR d IN 0 TO 7 GENERATE B : BLOCK ATTRIBUTE RELATIVE_LOCATION OF flop : LABEL IS "R" & INTEGER'IMAGE(d) & "C0"; BEGIN flop : dff PORT MAP (D => INP(d), Q=>OUTP(d), CK=>CLK); END BLOCK; END GENERATE G;

In this case, we're instantiating a set of eight DFFs that will be used to latch the value of an eight-bit bus. Note that 'IMAGE can be used only: + Within a block within a for-generate loop. + As part of an attribute statement, where the attribute name is "RELATIVE_LOCATION" and the value is a concatination of three strings: a prefix, the 'IMAGE expression, and a suffix. In the above example, "R" is the prefix and "C0" is the suffix. The prefix and suffix must be literals. + With the index variable for the for-generate loop.

Note that choices for the following are left to you: + The label for the for-generate loop and the block. + The number and contents of the instantiation statements within the block.

You may also specify more than one entity name in the attribute statement. For

example, you could use

```
ATTRIBUTE RELATIVE_LOCATION OF flop,rflop : LABEL IS "R" & INTEGER'IMAGE(d) & "C0";
```

if you were instantiating two series of entities:

```
flop : dff PORT MAP (D => INP(d), Q=>OUTP(d), CK=>CLK); rflop : dff PORT MAP (D =>
INP(d), Q=>R_OUTP(8-d), CK=>CLK);
```

You may also have more than one such attribute statement, if you want to specify a different prefix and/or suffix.

VHDL-2282 (error) The argument to 'IMAGE is not a for-generate loop index variable.

DESCRIPTION

HDL Compiler supports the 'IMAGE attribute only as part of an attribute specification of the following type:

```
attribute RELATIVE_LOCATION of <object> : label is <string_literal> &
INTEGER'IMAGE(<indexvar>) & <string_literal>
```

Where <indexvar> is the index variable of a for-generate loop.

WHAT NEXT

The following is an example of the situation in which 'IMAGE might be used.

```
G : FOR d IN 0 TO 7 GENERATE B : BLOCK ATTRIBUTE RELATIVE_LOCATION OF flop : LABEL
IS "R" & INTEGER'IMAGE(d) & "C0"; BEGIN flop : dff PORT MAP (D => INP(d),
Q=>OUTP(d), CK=>CLK); END BLOCK; END GENERATE G;
```

In this case, you're instantiating a set of eight DFFs that will be used to latch the value of an eight-bit bus. Note that 'IMAGE can be used only

+ Within a block within a for-generate loop.
+ As part of an attribute statement, where the attribute name is "RELATIVE_LOCATION" and the value is a concatination of three strings: a prefix, the 'IMAGE expression, and a suffix. In the previous example, "R" is the prefix and "C0" is the suffix. The prefix and suffix must be literals.
+ With the index variable for the for-generate loop.

Note that choices for the following are left to you:

+ The label for the for-generate loop and the block.
+ The number and contents of the instantiation statements within the block.

You can also specify more than one entity name in the attribute statement. For

example, you can use

ATTRIBUTE RELATIVE_LOCATION OF flop,rflop : LABEL IS "R" & INTEGER'IMAGE(d) & "C0";

if you were instantiating two series of entities:

flop : dff PORT MAP (D => INP(d), Q=>OUTP(d), CK=>CLK); rflop : dff PORT MAP (D => INP(d), Q=>R_OUTP(8-d), CK=>CLK);

You can also have more than one such attribute statement if you want to specify a different prefix or suffix.

VHDL-2283 (error) Only the type INTEGER is supported for the prefix of the attribute 'IMAGE %s

DESCRIPTION

Presently 'IMAGE attribute has a limited support in HDL compiler. Only Integer may appear as a prefix to it

WHAT NEXT

Please rewrite the use of 'image attribute so that it has integer as its prefix

VHDL-2284 (error) Declarative regions of generate statements is not supported %s

DESCRIPTION

This version of VHDL Compiler doesn't support declarative regions of generate statements.

WHAT NEXT

Use block statement inside the generate statement.

Example:

You replace the following VHDL codes

---------- build_blks: FOR i IN 1 TO 4 GENERATE

SIGNAL int_connect: unsigned(3 DOWNTO 0); BEGIN blk1: blk_in PORT MAP(a_in(i - 1), int_connect(i - 1)); blk2: blk_out PORT MAP(int_connect(i - 1), b_out(i - 1)); END

```
GENERATE build_blks; ------------------------------------------------------------
-------

by

------------------------------------------------------------------- build_blks:
FOR i IN 1 TO 4 GENERATE

THE_BLOCK : block SIGNAL int_connect: unsigned(3 DOWNTO 0); BEGIN blk1: blk_in PORT
MAP(a_in(i - 1), int_connect(i - 1)); blk2: blk_out PORT MAP(int_connect(i - 1),
b_out(i - 1)); end block;

END GENERATE build_blks; --------------------------------------------------------
-----------
```

VHDL-2285 (warning) VHDL-93 generates different concatenation results from VHDL-87 %s.

DESCRIPTION

You receive this message if **read** or **elaborate** detects that the concatenation result generated by VHDL-93 for your design differs from the result that would have been generated by VHDL-87. This message is to warn you to expect different results from those you might have become accustomed to with VHDL-87.

By default, currently VHDL Compiler uses VHDL-93 concatenation, which generates a different left bound and/or direction from VHDL-87. (For details of the concatenation definition, see the IEEE *VHDL-93 Language Reference Manual*.) You can override the default behavior by setting the **hdlin_vhdl93_concat** environment variable to *false*.

WHAT NEXT

If you receive this message, proceed as follows:

1. Read the *VHDL-93 Language Reference Manual* to understand the concatenation results generated by VHDL-93.

2. If this is acceptable for your design, you need take no further action.

3. If you want to revert to VHDL-87 behavior, set **hdlin_vhdl93_concat** to *false*.

SEE ALSO

hdlin_vhdl93_concat (3); *VHDL-93 Language Reference Manual*.

VO-1 (warning) Changed instance name %s to %s in module %s. Please use the change_names command to make the correct changes before invoking the verilog writer.

DESCRIPTION

This warning is generated when the instance name has the same name as the port net name. In Verilog, both port and module have its own name space, which include instance names and net names. Implicit nets are used for those nets connected to ports: meaning the port net is using the same name as its port. Because instance names and net names are sharing the same space, they can not use the same names.

WHAT NEXT

If you do not want it to be renamed by the writer, use the **change_name** command to make sure the instance name is correctly changed.

VO-2 (warning) Changed wire name %s to %s in module %s. Please use the change_names command to make the correct changes before invoking the verilog writer.

DESCRIPTION

This warning is generated when the net, which does not connect to port, has the same name as the port. Because the net does not connected to port, under the implicit net declaration, this net has to be renamed.

WHAT NEXT

If you do not want it to be renamed by the writer, use the **change_name** command to make sure the net name is correctly changed.

VO-3 (warning) Net(s) of type ’tri’ are written out.

DESCRIPTION

This description may not be acceleratable for simulation.

WHAT NEXT

Change the value of the variable *verilogout_no_tri*. For instructions about how to use the variable, see the man page. Then, rewrite the Verilog description.

VO-4 (warning) Verilog ’assign’ or ’tran’ statements are written out.

DESCRIPTION

In this design, ports are attached to other ports, which forces Verilogout to use *assign* or *tran* statements to write out a correct description.

The description may not be acceleratable for simulation.

WHAT NEXT

If the problem exists, it can be solved by the **compile** command with proper setting of the variable *set_fix_multiple_port_nets*. For instructions about how to use the variable, see the man page. Then, compile and rewrite the Verilog description.

VO-5 (error) The db file contains inconsistent information about the bussed port ’%s’. Its width is %d, but the actually elements only have %d.

DESCRIPTION

In this design, ports are maybe previously processed without updated the bussed information correctly.

WHAT NEXT

If the problem exists, Please use the bit-blast verilog.

VO-6 (error) Can not write out this design ’%s’ with memory

operations in it using non-levelized writer.

DESCRIPTION

This error happened when verilogout_levelize is set to FALSE, there is a memory component in the design.

WHAT NEXT

Please set verilogout_levelize to TRUE.

VO-7 (warning) In design '%s', port '%s' has negative indeces [%d:%d] which will be converted into [%d:%d].

DESCRIPTION

This warning is generated when there is a negative indeces in the type, because Verilog does not like negative indeces.

WHAT NEXT

If the resulting indeces are not wanted, recreate design with positive indeces.

VO-8 (warning) Unknown direction port '%s' is assumed to be inout in module '%s'.

DESCRIPTION

This warning is generated when the port name has no specific direction. It will be assumed that the port is inout.

WHAT NEXT

Make sure the port direction is defined.

VO-9 (warning) The output verilog file contains power/ground

information, and is not supported by the verilog reader.

DESCRIPTION

This warning is generated when the variable verilogout_show_power_pins is set to true. With this option turned on, the verilog writer writes out power/ground information as specified in the library.

WHAT NEXT

This verilog file will need to be modified before it can be read by verilog reader.

VO-10 (warning) no rail connection specified for (%s)

.

DESCRIPTION

This warning is generated when there is a power rail is specified and no rail connection specified in the library.

WHAT NEXT

Either specify the rail connection in the library or the verilog writer will try to inherit the rail connection from the reference.

VO-11 (warning) Verilog writer has added %d nets to module %s using %s as prefix. Please use the change_names command to make the correct changes before invoking the verilog writer.

DESCRIPTION

This warning is generated when the verilog writer adds extra nets to designs to make the verilog output legal. Verilog syntax does not allow a partially connected bus. For the unconected bus bits of the partially connected bused, verilog writer generates dummy nets.

WHAT NEXT

If you do not want dummy nets to be generated by the writer, use the **change_name** command to make sure the net name is correctly changed.

VO-12 (warning) Module %s contains unmapped components. The output netlist might not be read back into the system.

DESCRIPTION

This warning is generated when the verilog writer detects that there are references of SELECT_OP or GTECH components in the module. When the design is not mapped, Formality, DC, and PC might not able to process netlist with unmapped components.

WHAT NEXT

VO-13 (warning) Bus naming style currently specified as %s, verilog syntax requires bus naming style to be "[]".

DESCRIPTION

This warning is generated when the verilog writer detects that the specified bus naming style is different from what verilog syntax is required. Please check design busses to conform to verilog bus pattern (%s[%d]). If the db bus pattern does not match the verilog bus pattern, the verilog writer will bit blast the bus.

WHAT NEXT

If you do not want busses to be bit blasted by the writer, use the **change_name** command to make sure the busses name is correctly changed.

VO-14 (warning) Verilog writer will obsolete the variable verilogout_levelize in 2005.06.

DESCRIPTION

This warning is generated when the user is trying to write a flat verilog netlist from a hierarchical design by setting the variable verilogout_levelize to TRUE. This feature will no longer be supported and the variable will become obsolete starting from 2005.06 release.

WHAT NEXT

Please change your script so that it will not use the variable starting from 2005.06 release.

VO-15 (warning) The design cannot be written out as levelized, reverting to writing out hierarchical netlist.

DESCRIPTION

This warning is generated when the user is trying to write a flat verilog netlist from a hierarchical design by setting the variable verilogout_levelize to TRUE. However, the writer is detecting that this design cannot be written out as a levelized netlist and it is reverting to the non-levelized mode.

WHAT NEXT

VO-16 (warning) XG mode verilog writer does not support the variable verilogout_levelize. The design will be written in hierarchical style.

DESCRIPTION

This warning is generated when the user is trying to write a flat verilog netlist from a hierarchical design by setting the variable verilogout_levelize to TRUE in XG mode. However, the verilog writer in XG mode does not support this variable, and it is reverting to the non-levelized mode.

WHAT NEXT

VO-17 (warning) You are using an older version of the Verilog netlist reader/writer, which will be obsoleted in the X-2005.06 release.

DESCRIPTION

You are using an older version of the Verilog netlist reader/writer, which will be obsoleted in the X-2005.06 release. To use the current Verilog reader/writer, please make sure these variables are set as follows:

Verilog netlist reader: enable_2003.03_verilog_reader true Verilog netlist writer: enable_2003.03_verilog_writer true

WHAT NEXT

SEE ALSO

VO-18 (warning) You are using an older version of the Verilog netlist reader/writer, which will be obsoleted in the X-2005.06 release.

DESCRIPTION

You are using an older version of the Verilog netlist reader/writer, which will be obsoleted in the X-2005.06 release. To use the current Verilog reader/writer, please make sure these variables are set as follows:

Verilog netlist reader: enable_2003.03_verilog_reader true Verilog netlist writer: enable_2003.03_verilog_writer true

WHAT NEXT

SEE ALSO

VO-19 (error) Cannot write out this design '%s' in SystemVerilog format.

DESCRIPTION

This format is not supported if any of this is true, (a) Multiple designs have be specified to the write command. (b) RTL for this design is not in SystemVerilog format. (c) Design ports in the RTL follow non-ANSI styled port declaration.

WHAT NEXT

If multiple designs have to be specified in the write command, specify either a single design or no design list. Current design is written, if no design is specified.

VO-20 (error) Clock name is not defined.

DESCRIPTION

This error message occur when running the **write** command without defining a clock name.

WHAT NEXT

Name each clock and run the command again.

SEE ALSO

write(2)

VO-21 (warning) Carry-outs are not currently supported while writing functional synthesizeable RTLout.

DESCRIPTION

This warning message occurs because carry-outs are not currently supported while writing functional, synthesizeable RTL output.

WHAT NEXT

This is only a warning message. No action is required.

However, if possible, you might want to remove carry-outs in order to write out functional, synthesizeable RTL out.

SEE ALSO

write(2)

VO-22 (warning) Two’s complement multiplier cannot be written functionally in Verilog.

DESCRIPTION

This warning message is generated because the two’s complement multiplier cannot be written functionally in Verilog.

WHAT NEXT

This is only a warning message. No action is required.

However, if possible, you might want to remove the two’s complement multiplier in order to write out functional Verilog.

SEE ALSO

write(2)

VO-23 (warning) Unable to determine direction of port ’%s’ of cell ’%s’. Cannot write functional model.

DESCRIPTION

This warning message occurs when the direction of port cannot be determined and the functional model cannot be written.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, set port direction and run the command again.

SEE ALSO

write(2)

VO-24 (error) Bus bag is missing for the port ’%s’.

DESCRIPTION

This error message occurs when bus bag is missing for the port. This database is corrupted.

WHAT NEXT

Fix the database with the bus bag for the port and run the command again.

SEE ALSO

write(2)

VTC-1 (error) Port '%s' in design '%s' does not have a type.

DESCRIPTION

This error should only result from corrupt data being generated by a Synopsys tool.

WHAT NEXT

Either try to re-generate the design, or write out the design in single-bit or vector format.

VTC-2 (error) Type '%s' is duplicated in design '%s' and design '%s' but the types are not equivalent.

DESCRIPTION

You tried to write out multiple designs that have types with the same name, but the types are not equivalent. Since all of the necessary type conversion functions are written out into a single package, this cannot be done without generating incorrect VHDL.

WHAT NEXT

If the designs are in the same hierarchy, turning the lower levels of hierarchy into "vector" mode will solve the problem. If the designs are not in the same hierarchy, then the problem will go away if they are written out separately.

VTC-3 (error) A conversion function for inout port '%s' in design '%s' cannot be written out.

DESCRIPTION

When conversion functions are written out inside of a design, it is not possible in VHDL to convert a port to a set of signals bidirectionally using conversion functions. The only way that this can be done is by using a configuration.

WHAT NEXT

Either write out the mode in single_bit or vector mode, or else write out a configuration.

VTC-4 (error) Port '%s' in design '%s' has unknown direction.

DESCRIPTION

This error should only occur when an unlinked verilog reference is trying to be written out. Until the verilog reference is linked, the direction of the ports are not known.

WHAT NEXT

Get the design to link successfully.

VTC-5 (error) In order to write out type conversions in configuration
the setting of the variable %s must be 'VECTOR'.

DESCRIPTION

When writing out vhdl with type conversions being done in the configuration (set by setting vhdlout_write_top_configuration to TRUE), the value of vhdlout_single_bit must be set to 'VECTOR'.

WHAT NEXT

Either set vhdlout_write_top_configuration to FALSE, or set vhdlout_single_bit to VECTOR.

WC-1 (error) '%s' is an invalid write_constraints format. Valid formats are '%s'.

DESCRIPTION

The **write_constraints** command has three valid formats: **synopsys**, **sdf** and **sdf-v2.1**. By default the constraints file is generated in synopsys format.

WHAT NEXT

Use **write_constraints -format synopsys** or **write_constraints -format sdf** or **write_constraints -format sdf-v2.1**. Read the **write_constraints** man page for more information on writing a constraint file for layout tools.

WC-2 (warning) nworst_value must be an integer greater than 0. Using -nworst 1.

DESCRIPTION

The *-nworst* option of the **write_constraints** command requires an integer greater than 0. *nworst_value* specifies the maximum number of paths ending at each end point considered by **write_constraints**. By default, one (worst) timing path per end point is considered. Set *nworst* to the number of paths that must be considered for each end point.

WHAT NEXT

Reenter the **write_constraints** command with *-nworst <nworst_value>*, where *<nworst_value>* is an integer greater than 0.

WC-3 (warning) Both -by_input_pin_name and -by_output_pin_name can't be selected. Using '%s'.

DESCRIPTION

Those two options are contradictory, both cannot be used with **write_constraints**.

Read the **write_constraints** man page for more information on the **write_constraints** options.

WHAT NEXT

Re-enter the **write_constraints** command with either **-by_input_pin_name** or **-by_output_pin_name**.

WC-4 (warning) max_path_value must be an integer greater than 0.
Using -max_paths 1.

DESCRIPTION

The **-max_paths** option of the **write_constraints** command requires an integer greater than 0. max_path_value specifies the maximum number of timing paths selected for writing constraints. By default, one timing path is selected, it is the most critical paths (the paths with the smallest timing slack).

WHAT NEXT

Re-enter the **write_constraints** command with **-max_paths** <max_path_value>, where <max_path_value> is an integer greater than 0.

WC-5 (warning) The -max_nets value is a percentage, it must be greater than 0.0 and less or equal to 1.0. Using '%s'.

DESCRIPTION

The **write_constraints** command has the option *-max_nets <max_net_number* to specify the maximum number of nets written to the constraints file. *<max_net_number>* is a percentage of the total number of nets in the current design.

The default value for *<max_net_number>* is 0.05 (5% of all nets are written to the constraints file). *<max_net_number>* must be a real number between 0 and 1. If you want to write all nets on the selected paths in the constraints file, use *<max_net_number> = 1* (for 100%). For more information about the options of this command, read the **write_constraints** man page.

WHAT NEXT

Reenter the **write_constraints** command with *-max_nets <max_path_value>*, where *<max_path_value>* is a percentage greater than 0.0 and less or equal to 1.0.

WC-6 (warning) The -min_net_priority value must be greater or equal to 0. Using '%s'.

DESCRIPTION

The **write_constraints** option **-min_net_priority** specifies the minimum net priority number. This number must be an integer greater or equal to 0. The default is 0. The minimum net priority number used was invalid, the minimum net priority used is the one specified in this warning message. Refer to **write_constraints** man page for more information on net priority numbers.

WHAT NEXT

If the minimum net priority number is acceptable, keep the constraint file generated, otherwise use the **write_constraints** again with a valid minimum net priority number.

WC-7 (warning) The maximum net priority must be greater than the minimum net priority.
Using max_net_priority = '%s'.

DESCRIPTION

The **write_constraints** option **-min_net_priority** specifies the maximum net priority number. This number must be an integer greater than the minimum net priority number. The default is 100. The maximum net priority number used was invalid, the maximum net priority used is the one specified in this warning message. Refer to **write_constraints** man page for more information on net priority numbers.

WHAT NEXT

If the maximum net priority number used is acceptable, keep the constraint file generated, otherwise use the **write_constraints** again with a valid maximum net priority number.

WC-8 (information) Writing constraints to file '%s'.

DESCRIPTION

The command **write_constraints** is writing a constraints file to disk. Check the **write_constraints** man page for information on how to use the command. Use the **write** command to write a netlist for the current design before using the **write_constraints**

command. This is because **write** can change names and the new names should appear in the constraints file as well. This message indicates the disk location of the constraints file created with **write_constraints**.

WHAT NEXT

The constraints file can be used in layout tools or other tools reading **write_constraints** file formats.

WC-9 (warning) A path starting at '%s' and ending at '%s' has a violated constraint.

DESCRIPTION

The design constraints violated constraints on the selected paths for **write_constraints**. One of the paths starting and ending at the specified pins in this message has a timing constraint which is not met in Design Compiler. This means that this path constraint migh be violated after layout as well. The violated constraints are still written in the constraint file unless the constraints are invalid. A constraint is invalid if it can never be met.

WHAT NEXT

Use **report_constraint -all_violators** to see if the violation is severe enough to hold going into layout. Compile the design until all constraints are met or slightly violated such that the layout tool can fix the violations and create a new constraint file.

WC-10 (warning) No more net constraints can be written; the maximum number (%.2f percent of all nets in the design) has been reached.

DESCRIPTION

Design Compiler writes net constraints for up to a specified percentage of the number of nets in the design. (The default value is 5%.)

This message is issued when there are more nets on constrained paths than can be written into the constraint file.

WHAT NEXT

To write more net constraints, use the option *-max_nets* of the command

write_constraints to specify the maximum percentage of nets that can be written. For example, to allow 50 percent of all nets in the design to be written as constraints, use *-max_nets 0.5*.

Take care when you set the maximum number of constraints, however: layout tools are usually limited in the number of constraints they can accept.

WC-11 (warning) '%s' is not supported with the SDF format.

DESCRIPTION

With the SDF format, the only options available for **write_constraints** are [-output file] [-max_paths number] [-max_path_timing] [-from pin_list] [-to pin_list] and [-through pin_list]

WHAT NEXT

Re-enter the **write_constraints** command with the valid options.

WC-12 (error) No valid constraint selected with the SDF format. Valid selections are '%s'.

DESCRIPTION

With the SDF format, the only constraint type available for **write_constraints** is **-max_path_timing**.

WHAT NEXT

Re-enter the **write_constraints** command with the valid constraint type.

WC-13 (information) Design '%s' has %g paths.

DESCRIPTION

This message indicates the total number of timing paths in the design.

WHAT NEXT

The information can be used to constrain a certain percentage of paths in the design.

WC-14 (information) The constraint file has ’%d’ path constraints.

DESCRIPTION

The **write_constraints** command has generated path constraints for all the paths selected. There will never be more path constraints generated than paths selected. There can be less path constraints than paths selected if some paths selected have no constraints or if the constraints are impossible: for example if the arrival to a path staring point is 10 and the required arrival time at the end of the path is 5, the constraint will never be met, the constraint will not be written in the constraint file for that path.

WHAT NEXT

Verify that all paths selected have valid constraints.

WC-15 (warning) The path : ’%s’-’%s’ has a non-positive constraint,
constraint value changed to %g.

DESCRIPTION

The required arrival time at a path endpoint is smaller than, or equal to, the actual arrival time at the path startpoint. There is no way that this constraint can ever be met. In addition, many tools don’t support negative or zero values in an SDF. Because the variable environment variable sdfout_allow_non_positive_constraints is ’false’, the value was changed to prevent a problem in a downstream application.

WHAT NEXT

Verify that all paths selected have valid constraints. If you want the non-positive constraints to appear in the SDF file, set the sdfout_allow_non_positive_constraints variable to the value ’true’.

WC-17 (warning) ’%s’ is not supported when using any of the design covering

options (-cover_design or -cover_nets).

DESCRIPTION

The specified option can not be used in conjuction with and of the covering options to write_constraints. It will be ignored.

WHAT NEXT

If you want the option to take effect, don’t use a covering option. If you just want to eliminate the warning message, then remove the offending option from the write_constraints command line.

WC-18 (error) no other constraint types are supported when using -environment.

DESCRIPTION

The **-environment** option cannot be used in conjunction with any other constraint types.

WHAT NEXT

Generate constraints using only the **-environment option**, or without the **-environment** option, depending on your needs.

WC-19 (error) You cannot specify both -cover_design and -cover_nets.

DESCRIPTION

Only one of the path coverage options can be specified on a call to **write_constraints.** You can specify either **-cover_design** or **-cover_nets**, but not both.

WHAT NEXT

Re-execute **write_constraints** using one or the other of **-cover_design** or **-cover_nets**.

WC-20 (error) '%s' is not supported with the Synopsys format.

DESCRIPTION

The -environment option is only supported when using the SDF format.

WHAT NEXT

Try again with the format specified as SDF (-format SDF).

WC-21 (warning) Can't use the %s option with the -environment option.

DESCRIPTION

The specified option can not be used with the -environment option. It will be ignored.

WHAT NEXT

WC-30 (warning) -max_path_slack is only supported when using -cover_design.

DESCRIPTION

The -max_path_slack option is only supported when used in conjunction with the -cover_design option when using the write_constraints command. The generated constraints are valid but the -max_path_slack option was ignored.

WHAT NEXT

In general, use of the -cover_design option will result in a set of paths which are more unique than a like number of paths generated without this option. Therefore, the best course of action is to add the -cover_design option to the write_constraints command line and run the command again.

WINSEL

WINSEL-001.n

WINSEL-001 (Warning) Invalid object class %s. Supported objects are : %s

DESCRIPTION

The specified object class does not exist.

WHAT NEXT

Verify that the object class exists and the spelling is correct.

WINSEL-002 (ERROR) Bad syntax for rectangle: %s

DESCRIPTION

The syntax specified for the rectangle was not acceptable. Correct syntax is, a rectangle must be of the form

{ <lower_left_point> <upper_right_point> }

and the point is

{ <x_dist > <y_dist> }

Note that distances are fixed point numbers, like 17.25 or 13000.1 or 2500.

WHAT NEXT

Please fix the syntax and try again.

WINSEL-003.n

WINSEL-003 (error) Nothing matched for search constraints.

DESCRIPTION

No objects satisfied the constraints you specified.

WHAT NEXT

Check the command arguments you gave, and see if the constraints can be changed or relaxed to make a match.

WL-1 (Warning) Overwriting library file '%s'.

DESCRIPTION

The library file specified with **create_wire_load -output** already existed. It has been overwritten with a new library file.

WHAT NEXT

If it's not necessary to keep the old library file, nothing needs to be done. If it's necessary to keep the old library file, to avoid losing it, look for a backup copy and rename it.

WL-2 (Error) File '%s' cannot be opened for writing.

DESCRIPTION

The library file cannot be opened for writing.

WHAT NEXT

Check the user-writing privileges in the current directory and in the directory specified by the path. Check to see if a file with the same location and name already exists and cannot be overwritten by the user.

WL-3 (Warning) Smoothing is unused, creating possibly unrealistic models.

DESCRIPTION

The **create_wire_load** command created models without "smoothing" the wire load model curve. Which means that the models might not be realistic. Using linear approximations, the smoothing operations ensure that the model curve is gradually increasing with the fanout. Smoothing also adds pessimism to high fanouts.

WHAT NEXT

The models are created from basic averages of the back-annotation data. Use **report_wire_load** to check the validity of the models created. The models may be

inaccurate if the average capacitance is not increasing with the fanout, or if the number of points used to calculate the average capacitance is small (less than 50) and the standard deviation is high.

If the model is invalid, use the *output* option to write the model to a text file. Then edit the text file before updating the model into a library using **update_lib**. To smooth the model's curve, use **create_wire_load** without the *dont_smooth* option.

WL-4 (Information) Writing wire load model(s) to library file '%s'.

DESCRIPTION

The **create_wire_load** command generated wire load models in the specified file. The models were not set on the current design.

WHAT NEXT

Using **report_wire_load**, verify the accuracy of the wire load created. To set wire load models on the design, use **create_wire_load** without the *output* option. Use **update_lib** to save the wire load models in a library file.

WL-5 (Information) Creating wire load model(s) for design '%s'.

DESCRIPTION

The **create_wire_load** command generated wire load models for the identified design. The wire load models created are set on the design, and when *hierarchy* is set, its subdesigns. If the *update_lib* option is used, they are also stored in a library file.

WHAT NEXT

Verify the validity of the wire load models created and set on the design. To check the wire loads set on designs/clusters, and to verify the accuracy of the designs/clusters, use **report_wire_load**, **report_design**, and **report_clusters**.

WL-6 (Error) Current design is not uniquified.

DESCRIPTION

The design has multiple instances of the same subdesign.

WHAT NEXT

Uniquify the design before creating wire load models. Use the **uniquify** command to eliminate multiple instances. This command creates a unique copy of the design for each instance and names the new designs according to the *uniquify_naming_style* variable. You can also manually uniquify by using the **copy_design** and **change_link** commands.

WL-7 (Error) Could not find cluster '%s' in design '%s'.

DESCRIPTION

The **create_wire_load** command could not find the cluster identified with the *cluster* option.

WHAT NEXT

Using the **report_clusters** command, verify the name of the clusters on the current design. Add cluster information to the design with the **read_clusters** command.

WL-8 (Information) Setting wire load model mode from '%s' to '%s' for design '%s'.

DESCRIPTION

The **create_wire_load** command is setting the wire load model mode to "enclosed" if the *hierarchy* or *top* options are used, or to the mode specified by fmode otherwise.

With "top" mode, all nets in the design are estimated with the wire load model set at the top level of the design. This mode is not recommended if the design is hierarchical or if subdesigns have different wire load models than the top design has. This mode is recommended if the design has no hierarchy.

With "enclosed" mode, nets in the design are estimated with the wire load model set at the lowest level of hierarchy containing all segments of the net. This mode is recommended for hierarchical designs.

With "segmented" mode, each net segment in the design is estimated with the wire load model set at the level of hierarchy containing the net segment. This mode is recommended for hierarchical designs, but it is not as accurate as the "enclosed" mode is.

WHAT NEXT

Verify that the wire load model set on the specified design is acceptable.

WL-9 (Information) Changing wire load model from '%s' to '%s' for %s '%s'.

DESCRIPTION

The **create_wire_load** command overwrites wire load models previously created and set on the design or its clusters.

WHAT NEXT

Use **create_wire_load** with the *-output* option to save the model into a file. Before running the timing verifier or compiling the design, verify with the **report_wire_load** command that the expected wire load model is set on the design or its clusters.

WL-10 (Error) The wire model name '%s' is already used in %s '%s'.

DESCRIPTION

There is already a wire load model with the same name in the specified design/ cluster.

WHAT NEXT

Use another name with **create_wire_load -name**, or remove the wire load model set on the design/cluster with **set_wire_load_model**.

WL-11 (Warning) Wire load model '%s' unused because design '%s' has clusters.

DESCRIPTION

Because the current design contains clusters or because the *-hierarchy* option was used, the **create_wire_load** command did not use the model name defined with the *name* option. Because only one name is defined with the *name* option, it is ambiguous as to

which cluster or design the defined wire load model name should apply to.

WHAT NEXT

Use the options *cluster* and *name* to define the wire load model name for a specific cluster. Do not use the *-hierarchy* option with the *-name* option. Verify the wire load names on the clusters with **report_clusters**.

WL-12 (Information) Creating wire load models for clusters of design '%s'.

DESCRIPTION

The current design has cluster information. Because the cluster information is useful for creating more accurate wire load models, wire load models are created for the clusters by default.

WHAT NEXT

Use **remove_clusters** to remove the cluster information from the current design if you wish to create wire load models for the logical hierarchy.

WL-13 (Warning) The wire model name '%s' is already used in %s '%s'.

DESCRIPTION

There is already a wire load model with the same name in the specified library. The wire load model has been created.

WHAT NEXT

The wire load model created should not be updated in the specified library unless you intend to overwrite the wire load in the library.

WL-14 (Error) Bad percentile value, must be between 0 and 100.

DESCRIPTION

The **create_wire_load** command failed because the *percentile* option was used with an

invalid value. Valid values are numbers between 0 and 100.

The "average" of net capacitance for a fanout is chosen so that there is a a certain percentage of data points below the "average" value. For example, with 10 capacitances—1, 2, 3, 4, 6, 7, 9, 10, 12, 17—and a percentile of 75, the "average" capacitance for this fanout is such that 75% of the capacitances are below the "average," which in this case is 10. The default value is 0. In this case, standard averages are calculated. In the previous example, the average is 7.1. This option allows the creation of more pessimistic wire load models.

WHAT NEXT

Use **create_wire_load** with a valid percentile value.

WL-15 (Error) Bad trim value. Must be 0 <= trim_value < 50.

DESCRIPTION

The **create_wire_load** command failed because the *trim* option was used with an invalid value. Valid values are numbers greater than or equal to zero (0) and less than 50. Each fanout has a capacitance range, which is bound by the minimum capacitance and the maximum capacitance annotated on nets.

The trim value is the percentage of data points removed from each end of the capacitance range. The trim operation assures that data points at the extremes of the capacitance range are not used for calculating the average capacitance. The trim increases the accuracy of the model created. The trim does not occur if there is less than 10 data points.

WHAT NEXT

Use **create_wire_load** with a valid trim value. The default value is 10; that is, 20% of data points are not used.

WL-16 (Warning) There is no default_wire_load_resistance in library '%s'. Using 0!
The models created will estimate 0 interconnect delays.

DESCRIPTION

The defined library has no *default_wire_load_resistance* value. The **create_wire_load** command created models that estimate net resistances to zero (0), and thus interconnect delays to zero (0).

WHAT NEXT

If you have a Library Compiler license, add a *default_wire_load_resistance* in the technology library. The *default_wire_load_resistance* can either be the worst of all routing layers' resistance per unit length or their average.

If you do not have a Library Compiler license, but know the routing layers resistance per unit length, use **create_wire_load -output** to write models into a file. Then update the "resistance" field in the models in the file. Then update the file into a technology library on the link path, with **update_lib**.

The resistance per unit length should be the same as the one for other wire load models of the same technology. Use **report_lib** to check the resistance per unit length of wire load models in the technology library.

WL-17 (Warning) There is no default_wire_load_capacitance in library '%s'. Using 1.

DESCRIPTION

The defined library has no *default_wire_load_capacitance* value. The **create_wire_load** command created models that assume a net capacitance per unit length of 1.

WHAT NEXT

If you have a Library Compiler license, add a *default_wire_load_capacitance* in the technology library. The *default_wire_load_capacitance* can either be the worst of all routing layers' capacitance per unit length or their average.

If you do not have a Library Compiler license, keep the created models. The net length is not exact, but the capacitance calculated from the net length is correct.

Because the net length is incorrect, the net resistance and net area will not be estimated accurately unless you modify the "resistance" and "area" per unit length of the models created. To do so, identify with **report_lib** the resistance per unit length and area per unit length of wire load models in the technology library. Then, use **create_wire_load -output** to write models into a file. Then update the "resistance" and "area" fields in the models in the file. Finally, with **update_lib**, update the file into a technology library on the link path.

WL-18 (Warning) The default_wire_load_capacitance in library '%s' is invalid.

Using 1.

DESCRIPTION

The defined library has no valid *default_wire_load_capacitance* value. Valid *default_wire_load_capacitance* values are numbers greater than zero (0). The **create_wire_load** command created models that assume a net capacitance per unit length of 1.

WHAT NEXT

If you have a Library Compiler license, add a valid *default_wire_load_capacitance* in the technology library. The *default_wire_load_capacitance* can either be the worst of all routing layers' capacitance per unit length or their average.

If you do not have a Library Compiler license, keep the created models. The net length is not exact, but the capacitance calculated from the net length is correct.

Because the net length is incorrect, the net resistance and net area will not be estimated accurately unless you modify the "resistance" and "area" per unit length of the models created. To do so, identify with **report_lib** the resistance per unit length and area per unit length of wire load models in the technology library. Then, use **create_wire_load -output** to write models into a file. Then update the "resistance" and "area" fields in the models in the file. Finally, with **update_lib**, update the file into a technology library on the link path.

WL-19 (Error) can't use -mode top for -cluster or -hierarchy

DESCRIPTION

We do not support *mode* on a cluster. It is always assumed to be **enclosed**.

Also, mode **top** for *hierarchy* does not make sense. In **top** mode, any wire load model on a lower level hierarchy will be overwritten, therefore those wire load models created by *hierarchy* on lower level hierarchy have no effect at all.

WHAT NEXT

Remove unwanted options.

WL-20 (Warning) this combination of options does not usually

make sense.

DESCRIPTION

We recommend use all enclosed nets (including child hierarchy) for mode **top**; and only nets in this level of hierarchy for mode **enclosed**. If you do need other combinations, it is still legal to do so, but you must take extra precaution.

WHAT NEXT

Change the options according to the methodology.

WL-21 (Warning) Design '%s' is flat.

DESCRIPTION

You should specify *hierarchy* only if your design does have physical or logical hierarchy. Because the design is flat, *hierarchy* will be ignored.

WHAT NEXT

Remove this option if it is a typo.

WL-22 (Error) The mode '%s' is not supported.

DESCRIPTION

Only **top** and **enclosed** are supported.

WHAT NEXT

Please use **top** or **enclosed** mode.

WL-23 (Error) Library '%s' is not in memory.

DESCRIPTION

The -update_lib option only works on a library which already resides in memory.

WHAT NEXT

If you want to update a library after create_wire_load, do not remove it from the memory with the **remove_lib** command. You should not update a library which is not linked with the current design, either. Also check whether there is any typo in the library name given.

WL-24 (Information) Creating wire load model(s) for cluster '%s'.

DESCRIPTION

The **create_wire_load** command generated wire load models for the identified cluster. The wire load models created are set on the cluster, and when *hierarchy* is set, its subclusters. If the *update_lib* option is used, they are also stored in a library file.

WHAT NEXT

Verify the validity of the wire load models created and set on the cluster. To check the wire loads set on designs/clusters, and to verify the accuracy of the designs/clusters, use **report_wire_load**, **report_design**, and **report_clusters**.

WL-25 (Error) Design '%s' has no net capacitance annotated.

DESCRIPTION

The **create_wire_load** command generates wire load models from net capacitance annotated on the current design. There is no net capacitance annotated on the current design, so no wire load model can be created.

WHAT NEXT

Use the **set_load** command to annotate net capacitance on the current design. The net capacitances are given from the net reports of the layout tools.

WL-26 (Information) %d wire load model(s) written to file '%s'.

DESCRIPTION

The **create_wire_load** command generated wire load models in the specified file. The wire load models were not set on the design.

WHAT NEXT

Use **create_wire_load** without the *output* option to create and set wire load models on the current design. To save the wire load model created, update the wire load models in the specified file into a library file with the command **update_lib**.

WL-27 (Information) Creating wire load model '%s' for cluster '%s'.

DESCRIPTION

The **create_wire_load** command generated a wire load model for the given cluster. Note that the wire load model is set on the cluster if the *output* option was not used. If the *output* option was used, the wire load model is stored in the library text file.

WHAT NEXT

For more information about creating wire load models, see the **create_wire_load** man page.

WL-28 (Warning) Model '%s' had a slope of %.2g, changing to slope = 1.

DESCRIPTION

The **create_wire_load** command generated a wire load model with a negative slope. Negative slopes do not represent reality. A negative slope implies that high fanout nets can be driven faster than low fanout nets. The slope has been changed to 1.

WHAT NEXT

The wire load model you created is not accurate because all nets annotated have the same fanout number. Edit the model to set the slope.

To edit the wire load, use the *output* option of the **create_wire_load** command to write the wire load in a text file. Then, if necessary, edit this text file to change the slope value. With the **update_lib** command, the edited wire load model can be stored in a library and, with **set_wire_load_model**, set on a design.

WL-29 (Warning) No wire load model created for the design/

cluster ’%s’.

DESCRIPTION

The **create_wire_load** command could not find any enclosed nets on the specified design/cluster, or those nets have no net capacitance annotated, So, no wire load model could be created. Capacitances annotated on nets connected to top level ports are not used for creating wire load models.

WHAT NEXT

Annotate net capacitances on the design/cluster, with the **set_load** command. Use values from the net reports of the layout tools. Make sure the design/cluster does have nets which are not connected to top level ports.

WL-30 (Warning) Not all nets had capacitance annotated.

DESCRIPTION

The **create_wire_load** command generated a wire load model. Not all nets in the design or cluster had a net capacitance annotated. Which means that the wire load model may not be accurate. Nets without annotated capacitance are not taken into account for creating the wire load models.

WHAT NEXT

You can identify the nets with missing back-annotation using command "check_design -post_layout" and annotate capacitances on those nets. Otherwise, you can verify the accuracy of the wire load model created with **report_wire_load**. The standard deviation is rating the accuracy of the net length for each fanout.

WL-31 (Information) Creating wire load model ’%s’ for design ’%s’.

DESCRIPTION

The **create_wire_load** command generated a wire load model for the given design. Note that the wire load model is set on the design if the *output* option was not used. If the *output* option was used, the wire load model is stored in the library text file.

WHAT NEXT

For more information about creating wire load models, see the **create_wire_load** man

page.

WL-32 (warning) Total area (%g) not greater than cell area (%g) for %s.
The -total_area option will be ignored as a result.

DESCRIPTION

The total area specified for the named design/cluster is not greater than the cell area. This implies a negative area for the wires. Area coefficients will not be calculated for any created wire load models. Note that wire load models may still end up with area coeffiecients if there is a default area value in the library.

WHAT NEXT

Remove the -total_area option from the create_wire_load command line or increase the area value such that it is greater than the cell are of the design or cluster.

WL-33 (warning) Area coefficients will not be calculated because the
variable create_wl_dont_set_wire_load has been set to true.

DESCRIPTION

The variable create_wl_dont_set_wire_load has been set to true, which means that wire loads generated by create_wire_load are not to be set on the design or clusters. Area coefficients can not be calculated unless the wire load models are set on the design or cluster, so they will not be calculated.

WHAT NEXT

Remove the -total_area option from the create_wire_load command line or change the value of the variable create_wl_dont_set_wire_load to false.

WL-34 (Information) %d wire load model(s) written to library

’%s’.

DESCRIPTION

Wire load models generated by the **create_wire_load** command are saved into the library. The library must already reside in memory, and will not be write back to disk after being updated.

WHAT NEXT

Use the **write_lib** to write the library back to disk.

WL-35 (Information) set_wire_load_model command written to script file ’%s’.

DESCRIPTION

A set_wire_load_model command corresponding to the wire load model generated by the **create_wire_load** command is written into the script file. The new command is appended to any existing content of the file.

WHAT NEXT

Use the script to set wire load models in another run.

WL-37 (Warning) Cannot set wire load on ’%s’.

DESCRIPTION

For instances, you can only set wire load models or selection groups on hierarchical cell instances.

WHAT NEXT

Respecify the command.

WL-40 (error) Could not find user specified selection group: %s.

DESCRIPTION

The user specified selection group could not be found. If the selection group was specified using set_wire_load_selection_group with the -library switches, then the selection group was not found in the user specified library (must be in the link path). Otherwise the selection group was not found in the first used target library or in the first library of the link path.

WHAT NEXT

Either change the current selection group name to something which can be found in the link library or target library variables, or update the link library or target library variables such that the current selection group name can be found.

WL-50 (Error) The -cell option does not work for physical hierarchy.

DESCRIPTION

It is an error to specify both *cell* and *cluster*, because *cell* specifies a logical hierarchy, but logical hierarchy and physical hierarchy are not corresponding to each other at all.

It is also an error to specify both *cell* and *hierarchy* with cluster information. Again this is because *cell* specifies logical hierarchy.

WHAT NEXT

Remove unwanted options.

WL-51 (Error) Empty list given with the -cell option.

DESCRIPTION

The *cell* option expects a list of hierarchical cells.

WHAT NEXT

Check whether it is the option you want.

WL-52 (Warning) Cell '%s' is not a hierarchial cell.

DESCRIPTION

We do not create wire load model for leaf cells.

WHAT NEXT

Check if it is a typo.

WL-53 (Warning) Variable '%s' is set true. Wire resistance is ignored. Using this variable can invalidate the DesignWare cache. Refer to the 'compile_ignore_wire_resistance' man page for more details.

DESCRIPTION

If you receive this message, **compile** has detected that the variable **compile_ignore_wire_resistance** is set to *true*, indicating that **compile** is to ignore wire resistance when performing wire delay calculations.

Changing the value of either **compile_ignore_wire_resistance** or **compile_ignore_wire_area** invalidates the contents of the DesignWare cache.

WHAT NEXT

If you want **compile** to use wire resistance in wire delay calculations, set **compile_ignore_wire_resistance** to *false*.

After you change either **compile_ignore_wire_resistance** or **compile_ignore_wire_area**, you must regenerate the DesignWare cache. For instructions, see the man page for the **compile_ignore_wire_resistance** variable.

SEE ALSO

compile (2), **compile_ignore_wire_area** (3), **compile_ignore_wire_resistance(3).**

WL-54 (Warning) Variable '%s' is set true. Wire area is ignored. Using this variable can invalidate the DesignWare cache. Refer

to the ’compile_ignore_wire_area’ man page for more details.

DESCRIPTION

If you receive this message, **compile** has detected that the variable **compile_ignore_wire_area** is set to *true*, indicating that **compile** is to ignore wire area when performing wire delay calculations.

Changing the value of either **compile_ignore_wire_area** or **compile_ignore_wire_resistance** invalidates the contents of the DesignWare cache.

WHAT NEXT

If you want **compile** to use wire area in wire delay calculations, set **compile_ignore_wire_area** to *false*.

After you change either **compile_ignore_wire_area** or **compile_ignore_wire_resistance**, you must regenerate the DesignWare cache. For instructions, see the man page for the **compile_ignore_wire_area** variable.

SEE ALSO

compile (2), **compile_ignore_wire_area** (3), **compile_ignore_wire_resistance(3).**

WL-55 (Warning) Wire load table size must be greater than 15.

DESCRIPTION

Wire load table size must be greater than 15, otherwise the value will be ignored and the default value of 20 will be used.

WHAT NEXT

Decide on a value greater than 15.

WMDB-1 (error) Internal error in creating mdb object for design %s.

DESCRIPTION

WHAT NEXT

WMDB-2 (error) Layer information not converted to mdb in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-3 (error) Via information not converted to mdb in design

’%s’.

DESCRIPTION

WHAT NEXT

WMDB-4 (error) Ports not converted to mdb in design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-5 (error) Cell rows not converted to mdb in design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-6 (error) Track information not converted to mdb in design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-7 (error) Obstructions not converted to mdb in design

’%s’.

DESCRIPTION

WHAT NEXT

WMDB-8 (error) Routing information not converted to mdb in design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-9 (error) Movebounds not converted to mdb in design

’%s’.

DESCRIPTION

WHAT NEXT

WMDB-10 (error) No library information present for design.

DESCRIPTION

WHAT NEXT

WMDB-11 (error) No library information present for design .

DESCRIPTION

WHAT NEXT

WMDB-12 (error) Entry already in the hash table for site object%s.

DESCRIPTION

WHAT NEXT

WMDB-13 (error) Entry already in the hash table for wirecode object %s.

DESCRIPTION

This error message occurs when routes in the Milkyway database contain wires with duplicate IDs.

WHAT NEXT

Check the routes by reviewing the PDEF file for duplicate layers. Remove the duplicate layers and rerun the command.

WMDB-14 (error) Entry already in the hash table for via object '%s'.

DESCRIPTION

This error message occurs when the routes in the Milkyway database contain vias that have duplicate IDs.

WHAT NEXT

Check the routes by reviewing the PDEF file for duplicate layers. Remove the duplicate layers and rerun the command.

WMDB-15 (warning) Rectilinear shape for core area are not supported .

DESCRIPTION

The rectilinear core shapes on the floorplan are not supported by write_mdb. No floor plan data will be translated correctly by write_mdb.

WHAT NEXT

Dumpout PDEF and update the rectilinear shape to a rectangular shape until this feature is supported.

WMDB-16 (error) Die size of the chip not set correctly for design

’%s’.

DESCRIPTION

WHAT NEXT

WMDB-17 (information) The tool detected and pre-existing cell instance group "%s

DESCRIPTION

This message advises you that the cell group that existed in the CEL has been deleted and updated with an instance group from the tool.

WHAT NEXT

This is only an informational message. No action is required.

WMDB-18 (warning) Creation of MDB to set the cell boundary failed for design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-19 (information) The tool detected the pre-existing cell plan group "%s

DESCRIPTION

This message advises you that the plan group that existed in the CEL has been deleted and updated with bounds from the tool.

WHAT NEXT

This is only an informational message. No action is required.

However, if the existing plangroup was a exclusive plangroup, you might have to re-apply the properties again, since the tool does not support the exclusive plangroup and the property might have been lost during a read or write operation.

WMDB-20 (error) creation of milkway DB for baseArray failed for design '%s' .

DESCRIPTION

WHAT NEXT

WMDB-21 (error) License expired, Please check the LM_LICENSE_FILE .

DESCRIPTION

WHAT NEXT

WMDB-22 (warning) Scheme generation for site failed for design '%s' .

DESCRIPTION

WHAT NEXT

WMDB-23 (warning) Creation of MDB site failed for design '%s' .

DESCRIPTION

WHAT NEXT

WMDB-24 (warning) Non default rule '%s' are incorrect, missing

via ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-25 (warning) Scheme generation for non default rule ’%s’ failed .

DESCRIPTION

WHAT NEXT

WMDB-26 (warning) Creation of MDB for non default rule ’%s’ failed .

DESCRIPTION

WHAT NEXT

WMDB-27 (warning) Failed to get the region coordinates..

DESCRIPTION

WHAT NEXT

WMDB-28 (warning) Scheme generation for cellgroups failed for

design ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-29 (warning) creation of milkyway db for cellgroups failed for design ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-30 (warning) Scheme generation failed for routing obstruction in design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-31 (warning) Creation of MDB failed for routing obstruction in design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-32 (warning) Scheme generation failed for placement

obstruction in design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-33 (warning) Creation of MDB failed for placement obstruction in design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-34 (warning) Scheme generation failed for placement obstruction in design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-35 (warning) Creation of MDB failed for placement

obstruction in design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-36 (error) Internal Error for routing keepouts.

DESCRIPTION

WHAT NEXT

WMDB-37 (error) Failed to create obstruction ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-38 (warning) Rectilinear obstructions are not supported

’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-39 (error) Internal Error for routing obstructions ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-40 (error) Failed to create obstruction ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-41 (warning) Pin type COVER not supported.

DESCRIPTION

WHAT NEXT

WMDB-42 (warning) direction not set correctly for pin ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-43 (warning) Failed to create physical information for

Pin ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-44 (warning) Scheme generation for pins failed for design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-45 (warning) Master cell ’%s’ not found in Milkyway, using pdb information.

DESCRIPTION

WHAT NEXT

WMDB-46 (error) Creation of physical only cell ’%s’ failed for reference ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-47 (warning) Scheme generation failed to create

placement for design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-48 (warning) Creation of MDB Instance failed to create placement information for instance ’%s’ in design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-49 (warning) scheme generation failed to create a cell instance ’%s’ in design ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-50 (warning) scheme generation failed to create a cell instance ’%s’ in design ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-51 (warning) link the design prior to running write_mdb

command .

DESCRIPTION

WHAT NEXT

WMDB-52 (error) Failed to get boundary info for ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-53 (warning) Route type not defined in milkyway db .

DESCRIPTION

WHAT NEXT

WMDB-54 (warning) Route type not defined in milkyway db .

DESCRIPTION

WHAT NEXT

WMDB-55 (warning) Assuming detail route type .

DESCRIPTION

WHAT NEXT

WMDB-56 (warning) Route type for Fill wire not supported.

DESCRIPTION

WHAT NEXT

WMDB-57 (error) Route attributes not mapped correctly.

DESCRIPTION

WHAT NEXT

WMDB-58 (warning) Ignoring net '%s',with length=0 for design .

DESCRIPTION

WHAT NEXT

WMDB-59 (warning) Internal (error) , layer_name not found for id %d .

DESCRIPTION

WHAT NEXT

WMDB-60 (warning) Internal (error) , ignoring route data for net '%s', with width 0 for layer name '%s'.

DESCRIPTION

WHAT NEXT

WMDB-61 (warning) Internal (error) , ignoring route data with

width 0 for layer name .

DESCRIPTION

WHAT NEXT

WMDB-62 (error) Cannot find via_name for ’%d’ .

DESCRIPTION

WHAT NEXT

WMDB-63 (warning) Route Via ignored ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-64 (warning) Marking Net type as Shield for net ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-65 (error) in accesing route data.

DESCRIPTION

WHAT NEXT

WMDB-66 (warning) This net ’%s’ does not have a pin

connection..

DESCRIPTION

WHAT NEXT

WMDB-67 (warning) Nondefault rule ’%s’ for net ’%s’ not set correctly .

DESCRIPTION

WHAT NEXT

WMDB-68 (warning) Clock net ’%s’ not set correctly .

DESCRIPTION

WHAT NEXT

WMDB-69 (warning) port ’%s’ not connected in scheme for cell instance ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-70 (warning) port ’%s’ not connected in milkyway db for

cell instance ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-71 (warning) creation of MDB for simple via failed for design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-72 (warning) Scheme generation for simple via failed for design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-73 (warning) Scheme generation for routing wires failed for design ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-74 (warning) Creation of MDB for routing wires failed for

design ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-75 (warning) Tracks cannot be converted without outline of the chip.

DESCRIPTION

WHAT NEXT

WMDB-76 (warning) Track direction not set correctly .

DESCRIPTION

WHAT NEXT

WMDB-77 (warning) Scheme generation for wire tracks failed for design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-78 (warning) Creation of MDB wire tracks failed for

design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-79 (warning) Scheme generation for wire direction failed for design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-80 (warning) Creation of MDB for wire direction failed for

design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-81 (warning) Creation of base array failed for site ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-82 (error) Layer Name not found for tracks ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-83 (error) Layer name ’%s’ not found in Milkway DB .

DESCRIPTION

WHAT NEXT

WMDB-84 (warning) Net name ’%s’, not found in design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-85 (error) Layer name ’%s’ not found in Milkway DB .

DESCRIPTION

WHAT NEXT

WMDB-86 (error) Layer name ’%s’ not found in Milkway DB .

DESCRIPTION

WHAT NEXT

WMDB-87 (error) Failed to Create wire master for layer name ’%s’ in design ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-88 (error) Creation of Horizontal wire failed for net ’%s’ in design %s.

DESCRIPTION

WHAT NEXT

WMDB-89 (error) Setting of route_type failed for design %s.

DESCRIPTION

WHAT NEXT

WMDB-90 (error) Creation of Vertical wire failed for net ’%s’ in

design %s.

DESCRIPTION

WHAT NEXT

WMDB-91 (error) Setting of route_type failed for design %s.

DESCRIPTION

WHAT NEXT

WMDB-92 (error) Un connected routing data for net '%s' in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-93 (error) Creation of Wire Master failed for layer No '%d' with width '%d' .

DESCRIPTION

WHAT NEXT

WMDB-94 (error) Failed to create contact for via '%s' in design

’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-95 (error) Failed to create cell group for group name ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-96 (error) Failed to add cell instance ’%s’ to group ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-97 (error) Failed to create region for group name ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-98 (error) Failed to store hard/soft data as property for

group name ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-99 (error) Failed to open cell ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-100 (error) Failed to the cell boundary for cell ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-101 (error) Failed to map library via ’%s’ to contact/ contactarray .

DESCRIPTION

WHAT NEXT

WMDB-102 (warning) Failed to map the via ’%s’ to contact/ contactarray .

DESCRIPTION

This message indicates that the routing segment has a via, which violates the rules that are defined in the technology file.

The most common reasons, where a via violates the rule. 1. cut_min_spacing 2. Upper

and lower enclosure width.

WHAT NEXT

1. Check your technology file, to make that the design uses the right technology. 2. Rerun the routing for the nets, which violates this rule.

WMDB-103 (error) No library information present for design

’%s’.

DESCRIPTION

WHAT NEXT

WMDB-104 (error) Vias with no geometry not supported .

DESCRIPTION

WHAT NEXT

WMDB-105 (error) Routing via not translated .

DESCRIPTION

WHAT NEXT

WMDB-106 (error) Failed to Initialize MWX Api’s code ’%d’ .

DESCRIPTION

WHAT NEXT

WMDB-107 (error) current design not linked .

DESCRIPTION

WHAT NEXT

WMDB-108 (error) File open error ’%s’.

DESCRIPTION

WHAT NEXT

WMDB-109 (warning) Failed to get mdbout design context!.

DESCRIPTION

WHAT NEXT

WMDB-110 (warning) Failed to get cell (%s) hierarchy preservation data from hash table!.

DESCRIPTION

WHAT NEXT

WMDB-111 (warning) Failed to put design (%s) hierarchy preservation data into hash table!.

DESCRIPTION

WHAT NEXT

WMDB-112 (warning) Failed to query cell instance (%s) by name during hierarchy preservation.

DESCRIPTION

WHAT NEXT

WMDB-113 (warning) Failed to get hierarchy preservation data

for parent %s of cell %s.

DESCRIPTION

WHAT NEXT

WMDB-114 (warning) Failed to attach hierarchical port instance to hierarchical net!.

DESCRIPTION

WHAT NEXT

WMDB-115 (warning) Failed to attach hierarchical port instance to cell instance!.

DESCRIPTION

WHAT NEXT

WMDB-116 (warning) Could not to get cell hierarchy preservation data from hash table!.

DESCRIPTION

WHAT NEXT

WMDB-117 (warning) Failed to create hierarchical high-connect

net (%s)!.

DESCRIPTION

WHAT NEXT

WMDB-118 (warning) Failed to create hierarchical high-connect net (%s)!.

DESCRIPTION

WHAT NEXT

WMDB-119 (warning) Failed to create hierarchical low-connect net (%s)!.

DESCRIPTION

WHAT NEXT

WMDB-120 (warning) Failed to create hierarchical low-connect net (%s)!.

DESCRIPTION

WHAT NEXT

WMDB-121 (warning) Failed to create hierarchical low-connect

net (%s)!.

DESCRIPTION

WHAT NEXT

WMDB-122 (error) Failed to create hierarchical low-connect net (%s)!.

DESCRIPTION

WHAT NEXT

WMDB-123 (warning) Failed to create hierarchical port instance (%s)!.

DESCRIPTION

WHAT NEXT

WMDB-124 (warning) Failed to get port master data from hash table (%s)..

DESCRIPTION

WHAT NEXT

WMDB-125 (warning) Failed to attach hierarchical port instance

hi-connect net!.

DESCRIPTION

WHAT NEXT

WMDB-126 (warning) Failed to attach hierarchical port instance hi-connect net!.

DESCRIPTION

WHAT NEXT

WMDB-127 (warning) Failed to attach hierarchical port instance low-connect net!.

DESCRIPTION

WHAT NEXT

WMDB-128 (warning) Failed to attach hierarchical port instance un-connect net!.

DESCRIPTION

WHAT NEXT

WMDB-129 (warning) Failed to attach hierarchical port instance

to cell instance!.

DESCRIPTION

WHAT NEXT

WMDB-130 (warning) Failed to query cell instance (%s) by name during hierarchy preservation.

DESCRIPTION

This warning message occurs when the Milkyway libraries are corrupted and the flat instance does not match the database file.

WHAT NEXT

This is only a warning message.

However, you can eliminate this warning message by writing to a new cell.

WMDB-131 (error) Failed to attach the reference library '%s'.

DESCRIPTION

This error message occurs when the specified reference libraries cannot be set for the design library.

WHAT NEXT

Check that the reference library path is valid. Check that the libraries have the necessary permissions. Ensure that the reference libraries are relative to the design library (and not the current directory).

WMDB-132 (warning) Failed to create instance '%s', for master '%s'.

DESCRIPTION

This warning message occurs when the FRAM libraries are missing. Some cells are

treated as a black box and are not recognized by the Astro router.

WHAT NEXT

Check the reference libraries added to the design libraries and verify that the master name exists in the corresponding reference library.

WMDB-133 (error) Failed to create net '%s'.

DESCRIPTION

This error message occurs when the creation of the specified net fails. This failure may be caused by corrupted Milkyway libraries.

WHAT NEXT

Rerun the design from a clean directory. Make sure that the permissions are correct and the is enough disk space.

WMDB-134 (error) Failed to bind the design with '%s'.

DESCRIPTION

This error message occurs when the FRAM libraries do not exist for all of the leaf cells.

WHAT NEXT

Check the reference libraries that are added for the design libraries and ensure that the necessary STD cells are present in the reference libraries.

WMDB-135 (error) Failed to create port '%s' for net '%s'.

DESCRIPTION

This error message occurs when the tool fails to create the specified port because of a mismatch in FRAM libraries and the hierarchy cells.

WHAT NEXT

Make sure that the library preparation is performed using the **gePrepLibs** command.

For the reported reference name, make sure that the FRAM libraries are consistent with the .lib file.

SEE ALSO

gePrepLibs(2)

WMDB-136 (error) Failed to connect port instance '%s' in cell '%s' with net '%s'.

DESCRIPTION

This error message occurs when the specified port instance is not connected with the specified net. This may be due to inconsistent FRAM libraries and .lib files.

WHAT NEXT

Make sure that your libraries are consistent and run the command again.

WMDB-137 (error) Top design is not set correctly.

DESCRIPTION

This error message occurs when the current design is not set correctly.

WHAT NEXT

Run the **current_design** command and set the top design for the **write_mdb** command to work correctly.

SEE ALSO

current_design(2)
write_mdb(2)

WMDB-138 (warning) Link the design prior to running the

write_mdb command.

DESCRIPTION

This warning message occurs to advise you to run the **link** and the **link_physical** commands before running the **write_mdb** command.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the steps below.

Run the **link** command, and then run the **link_physical** command, making sure each command completes successfully. Then run the **write_mdb** command.

SEE ALSO

link(2)
link_physical(2)
write_mdb(2)

WMDB-139 (warning) Failed to create port '%s', for ref_name '%s'.

DESCRIPTION

This warning message occurs when the specified port cannot be createed for the specified reference name. The port is not created because of a mismatch in the FRAM libraries and the hierarchy cells.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the steps below.

Make sure that the library preparation is done using the **gePrepLibs**. Also, make sure that the FRAM libraries are consistent with the

SEE ALSO

gePrepLibs(2)

WMDB-140 (warning) Unable to save cell master '%s'.

DESCRIPTION

This warning message occurs when the specified cell cannot be stored to the Milkyway NETL view.

WHAT NEXT

This is only a warning message.

You can safely ignore this warning message if you are using Astro and you are not dependent on the NETL view.

If you want to use the NETL view, use the ASCII flow and the **auVerilogIn** Astro command.

SEE ALSO

The **auVerilogIn** Astro command in Physical Implementation Online Help.

WMDB-141 (warning) Unable to save cell master '%s'.

DESCRIPTION

This warning message occurs when the specified cell cannot be stored to the Milkyway NETL view.

WHAT NEXT

This is only a warning message.

You can safely ignore this message if you are using Astro and you are not dependent on the NETL view.

If you want to use the NETL view, use the ASCII flow and **auVerilogIn** Astro command.

SEE ALSO

The **auVerilogIn** Astro command in Physical Implementation Online Help.

WMDB-142 (warning) Instance doesn’t exist ’%s’ .

DESCRIPTION

WHAT NEXT

WMDB-143 (error) Directory not writable ’%s’.

DESCRIPTION

This error message occurs when the directory pointed by the **mw_design_library** variable is not writable.

WHAT NEXT

Verify that the directory pointed by **mw_design_library** is a valid directory and that you have the correct file permissions.

SEE ALSO

mw_design_library(3)

WMDB-144 (warning) Logical design data exists in ’%s’.

DESCRIPTION

This warning message occurs when the LOGIC view design data already exists. This may be due to a previous **write_mdb** command. This may also be due to very low memory available on the system.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Run the command again on a new mw_design_library directory or use a machine with more swap space.

SEE ALSO

write_mdb(2)

WMDB-146 (error) Failed to create netlist view for design '%s'.

DESCRIPTION

This error message occurs when the netlist view is not created for the specified design. This NETL view does not exist.

WHAT NEXT

Check that the permissions are correct for the value pointed to by the **mw_design_library** variable and verify that the directory is writable.

Also, check that the values pointed to by the **mw_reference_library** variable exist.

If you are using Astro, you can use the CEL view to do routing without any issues and the NETL view can be ignored.

SEE ALSO

mw_design_library(3)
mw_reference_library(3)

WMDB-147 (info) Starting to Expand the netlist for design '%s' .

DESCRIPTION

WHAT NEXT

WMDB-148 (error) Failed to create expand view for cell '%s'.

DESCRIPTION

WHAT NEXT

WMDB-149 (warning) Flat instance does not exist '%s'.

DESCRIPTION

This warning message occurs when the flat instances that are added for multi-voltage do not exist in Milkyway. The region object in the tool may not be translated

correctly to Milkyway.

WHAT NEXT

This is only a warning message.

However, if the result is not what you intended, you can check the flat object where the multi-voltage property is set and determine if it exists in Milkyway.

Create the voltage area in Astro after performing the **write_mdb**. Also, make sure that the hierarchies are consistent in Milkway by running the **astRepairHierPreservation** Astro command.

SEE ALSO

write_mdb(2)
astRepairHierPreservation

WMDB-150 (error) Top design is not set correctly.

DESCRIPTION

This error message occurs when the current design is not set correctly.

WHAT NEXT

Run the **current_design** command and set the current design correctly.

SEE ALSO

current_design(2)

WMDB-151 (information) Applications of Milkyway do not accept a port name the same as the net name for design '%s', and are not connected.

DESCRIPTION

This error message occurs because the design has the same name on a net and on a port, but they are not connected in the specified design and are not accepted by the Milkyway database.

WHAT NEXT

Define the name rules and change the names on the design before running the write_mdb command.

The following example shows one method you can use to change the names on the design:

```
prompt> define_name_rules snps_milkyway -equal_ports_nets
prompt> define_name_rules snps_milkyway -check_internal_net_name
prompt> change_names -rule snps_milkyway -hier
```

The second way to change the names on the design is by running the following command:

```
prompt> change_names -rule verilog -hier
```

SEE ALSO

change_names(2)
define_name_rules(2)

WMDB-152 (information) Cannot perform incremental operation; using non-incremental mode to save cell '%s'.

DESCRIPTION

This information message occurs when performing an incremental update using the **write_mdb** command, if either of the following conditions exist:

• The cell with the same name already exists in the Milkyway design library.

• The **write_mdb** follows a **read_mdb** command, such as if the database is created or updated using **read_mdb**.
The routing data and all of the floorplan data that exists in the LOGIC database is saved in the Milkyway database.

In incremental mode, the route information that is changed in the tool is only transferred to Milkyway. The change of route information is normally detected by changes in nets or changes to cell locations in the design w.r.t to the Milkyway database.

WHAT NEXT

This is an information message only. No action is required.

However, if you want the routing data to be transferred to Milkyway from the LOGIC database, make sure that there are no versions of cells with the same name in the Milkyway design library.

You can create a new design library using the **create_mw_design** command and use **write_mdb** to save the CEL from which to transfer the routes.

SEE ALSO

create_mw_design(2)
read_mdb(2)
write_mdb(2)

WMDB-153 (warning) Failed to get the master name for cell instance '%s'.

DESCRIPTION

This warning message occurs when the **write_mdb** command cannot get the master name for the given cell instance, possibly due to a corrupted Milkway database.

WHAT NEXT

Check that the **mw_reference_library** variable is set correctly and verify that the reference libraries are added to the design library.

SEE ALSO

create_mw_design(2)
set_mw_design(2)
mw_reference_library(3)

WMDB-154 (error) Failed to initiate a iterator.

DESCRIPTION

write_mdb can not initiate an iterator to iterate through mdb objects.

WHAT NEXT

Please verify your data and try again in need.

SEE ALSO

WMDB-155 (error) Failed to iterate through expanded cell instances.

DESCRIPTION

write_mdb failed to iterate through mdb expanded cell instances. The mdb may be corrupted.

WHAT NEXT

Please verify your data and try again in need.

SEE ALSO

WMDB-156 (warning) Failed to delete cell instance '%s'.

DESCRIPTION

write_mdb failed to delete a mdb cell instances. This cell instance may not exist or the mdb has been corrupted.

WHAT NEXT

Please verify your data and try again in need.

SEE ALSO

WMDB-157 (warning) Failed to get port type. (port id: %d)

DESCRIPTION

write_mdb can not get the port type attribute of a certain port. Port may not exist or mdb has been corrupted.

WHAT NEXT

Please verify your data and try again in need.

SEE ALSO

WMDB-158 (error) Fail to create port '%s'.

DESCRIPTION

write_mdb can not create a port specified by name '%s' in mdb.

WHAT NEXT

Please verify your data and try again.

SEE ALSO

WMDB-159 (error) Failed to connect net '%s' to port '%s'.

DESCRIPTION

This error message occurs when the **write_mdb** command cannot connect the specified net to the specified port. Refer to the log file for details.

WHAT NEXT

Check that the reference libraries are correct, and that the specified ports exist in the reference libraries.

Also, you can try writing into a new design library by creating it with the **create_mw_design** command.

SEE ALSO

create_mw_design(2)
write_mdb(2)

WMDB-160 (error) Failed to connect pin '%s/%s' to net '%s'.

DESCRIPTION

This error message occurs when the **write_mdb** command fails to connect the pin with the specified net. This error indicates the Milkyway database may be corrupted.

WHAT NEXT

Create the design_library by changing the value of the **mw_design_library** variable in a new directory.

Make sure that the value of the **mw_reference_library** variable is set correctly and that all of the FRAM libraries exist.

Check that the reference libraries are correct and that the specified ports exist in the reference libraries.

You can try writing into a new design library by creating it using the **create_mw_design** command.

SEE ALSO

create_mw_design(2)
write_mdb(2)
mw_design_library(3)

WMDB-161 (error) Failed to delete the global route for net '%s'.

DESCRIPTION

write_mdb failed to delete the global route for a net. The global route data for the specified net does exist in the Milkyway database.

WHAT NEXT

Manually delete the global route data for the specified net.

SEE ALSO

Astro

WMDB-162 (warning) Failed to delete net '%s'.

DESCRIPTION

This warning message occurs the **write_mdb** command fails to delete a net. The Milkyway database may be corrupted.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following

the instructions below.

Create the design_library by changing the value of the **mw_design_library** variable in a new directory.

Make sure that the value of the **mw_reference_library** variable is set correctly and that all of the FRAM libraries exist.

Check that the reference libraries are correct and that the specified ports exist in the reference libraries.

You can try writing into a new design library by creating it using the **create_mw_design** command.C

SEE ALSO

create_mw_design(2)
write_mdb(2)
mw_design_library(3)

WMDB-163 (warning) Failed to delete all pins for port '%s'.

DESCRIPTION

This warning message occurs when the **write_mdb** fails to delete all pins for specified port. The Milkyway database may be corrupted.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Create the design_library by changing the value of the **mw_design_library** variable in a new directory.

Make sure that the value of the **mw_reference_library** variable is set correctly and that all of the FRAM libraries exist.

Check that the reference libraries are correct and that the specified ports exist in the reference libraries.

You can try writing into a new design library by creating it using the **create_mw_design** command.

SEE ALSO

create_mw_design(2)
write_mdb(2)
mw_design_library(3)

WMDB-164 (warning) Failed to delete a port '%s'.

DESCRIPTION

This warning message occurs when the **write_mdb** command fails to delete the specified port. The Milkyway database may be corrupted.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Create the design_library by changing the value of the **mw_design_library** variable in a new directory.

Make sure that the value of the **mw_reference_library** variable is set correctly and that all of the FRAM libraries exist.

Check that the reference libraries are correct and that the specified ports exist in the reference libraries.

You can try writing into a new design library by creating it using the **create_mw_design** command.

SEE ALSO

create_mw_design(2)
write_mdb(2)
mw_design_library(3)

WMDB-165 (warning) Failed to create port vector info object.

DESCRIPTION

This warning message occurs when the **write_mdb** command fails to create a vector info object for a hierarchical port. This could cause an inconsistent bus port for the design.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Verify your data and run the command again.

SEE ALSO

write_mdb(2)

WMDB-166 (warning) Failed to set port vector info object.

DESCRIPTION

This warning message occurs when the **write_mdb** command fails to build the relationship between a vector info object and a hierarchical port. This causes an inconsistent bus in the design. The bus information for ports may be lost during **read_mdb** or **write_mdb** command activity.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Check your design for RAMS, which may result from BUSES in the RAMS. If you are writing out a NETL view, there should not be any problems in the flow, since Astro can use the information from NETL. This is also true for **read_mdb**.

SEE ALSO

read_mdb(2)
write_mdb(2)

WMDB-167 (error) Failed to create hierarchical cell instance master '%s'.

DESCRIPTION

This error message occurs when the the hierarchical cell instance with the specified name for the design cannot be created in Milkyway. The result may cause inconsistent hierarchy data.

WHAT NEXT

Run the **write_mdb** command on a new Milkyway design library and save it to a new CEL.

If the design is a flat design and if it is a one way flow, you may be able to ignore this message.

SEE ALSO

write_mdb(2)

WMDB-168 (error) Failed to create hierarchical port instance master '%s'.

DESCRIPTION

This error message occurs when the hierarchical port instance with the specified name for the design cannot be created in Milkyway. The result may be inconsistent hierarchy data. There is an internal error with the hierarchy preservation of Milkyway.

WHAT NEXT

Run the **write_mdb** command on a new Milkyway design library and save it to a new CEL.

If the design is a flat design and if it is a one way flow, you may be able to ignore this message.

See the **astRepairHierPreservation** Astro command in Physical Implementation Online Help.

SEE ALSO

write_mdb(2)

WMDB-169 (error) Hashing error during write_mdb.

DESCRIPTION

This error message occurs during **write_mdb** command activity and indicates an internal error with the hierarchy preservation of Milkyway.

WHAT NEXT

Run the **write_mdb** command on a new Milkyway design library and save it to a new CEL.

If the design is a flat design and if it is a one way flow, you may be able to ignore this message.

SEE ALSO

write_mdb(2)

WMDB-170 (error) Failed to attach hier port inst master '%s' to hier cell inst master '%s'.

DESCRIPTION

This indicates an internal error, during hierarchy preservation.

WHAT NEXT

File a star, and if the design is FLAT, maybe you can ignore this warning message.
Try running change_names -rule verilog and save the design.

SEE ALSO

WMDB-171 (error) Failed to create cell instance '%s'.

DESCRIPTION

This indicates an internal error, during hierarchy preservation.

WHAT NEXT

File a star, and if the design is FLAT, maybe you can ignore this warning message.
Try running change_names -rule verilog and save the design.

SEE ALSO

WMDB-172 (error) Failed to attach vcell instance '%s' to its parent '%s'.

DESCRIPTION

This indicates an internal error, during hierarchy preservation.

WHAT NEXT

File a star, and if the design is FLAT, maybe you can ignore this warning message.
Try running change_names -rule verilog and save the design.

SEE ALSO

WMDB-173 (warning) Failed to get cell instance data from hash table (%s)..

DESCRIPTION

This indicates an internal error, during hierarchy preservation.

WHAT NEXT

File a star, and if the design is FLAT, maybe you can ignore this warning message. Try running change_names -rule verilog and save the design.

SEE ALSO

WMDB-174 (information) Initializing hierarchy preservation...

DESCRIPTION

This indicates the hierarchy perservation is getting initialized by write_mdb.

The old hierarchy data, if any will be deleted, and the new hierarchy preservation data will be created in the CEL.

WHAT NEXT

SEE ALSO

WMDB-175 (warning) Failed to delete hierarchy preservation records.

DESCRIPTION

The hierarchy preservation data that exists in the CEL specified by mw_cell_name or -cell option cannot be deleted. If you see this error, it is likely that the hierarchy information is not correct, and needs to be fixed for hierarchy designs.

WHAT NEXT

The could indiciate the data is already corrupted. The user cannot delete the hierarchy preservation manually using Astro and do write_mdb again.

SEE ALSO

WMDB-176 (error) Failed to create new Milkyway library '%s'.

DESCRIPTION

This error message occurs when the Milkyway design library is not created as specified by the **mw_design_library** variable.

WHAT NEXT

Check that the technology file is correct and that there are no errors when parsing the technology file.

Verify that the value specified in **mw_design_library** is correct and the file has the necessary permissions.

Make sure there is enough disk space available to create a new design library.

SEE ALSO

mw_design_library(3)

WMDB-177 (error) Technology file is NULL or invalid.

DESCRIPTION

This error message occurs when the technology file is not provided or the file information is invalid.

WHAT NEXT

The technology file is required to run the **create_mw_design** command. The file provides the technology information for the Milkyway database library to be created.

Make sure that the information in the technology file does not contain any conflicts, since conflicts may cause the tf checker to fail.

Also, make sure that the required permissions specified in the **mw_design_library** variable are correct.

SEE ALSO

create_mw_design(2)
set_mw_design(2)
mw_design_library(3)

WMDB-178 (information) Please run ’change_names’ command to make sure that the names are consistent across db.

DESCRIPTION

This message indicates that the port names and the net names does not have the same name and are not connected.

The flow may have some problems due to the above mentioned reasons, and it may be corrected by running change_name before saving the CEL.

WHAT NEXT

Run change_names -rules verilog -hier before running write_mdb.

SEE ALSO

change_names

WMDB-179 (error) Failed to load technology file ’%s’.

DESCRIPTION

The technology file specified cannot be loaded to the memory.

WHAT NEXT

Please check if the technology file exists, and the permissions are set correctly.

SEE ALSO

mw_design_library variable

WMDB-180 (warning) Failed to set reference library ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-181 (error) Failed to open library ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-182 (warning) Failed to get milkyway library distance

unit converting factor.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-183 (information) Cell ’%s’ already exists in view ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-184 (error) Failed to create cell ’%s’ in view ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-185 (error) Failed to set layout view for cell ’%s’ in view

’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-186 (error) Failed to close cell.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-187 (error) Failed to copy cell ’%s’ to ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-188 (error) Failed to open cell ’%s’, view ’%s’.

DESCRIPTION

The specified leaf cell cannot be open during write_mdb. This error will affect translating the physical information for the design.

WHAT NEXT

Please if the reference libraries are specified correctly before write_mdb.

SEE ALSO

mw_reference_library(2), create_mw_design(2)

WMDB-189 (warning) Maximum var route rule crossed above limit.

DESCRIPTION

The number of default route rules has reached its limit of 256.

WHAT NEXT

Try deleting the number of var route rules available in the design, or merge the rules with the exisiting rules.

SEE ALSO

dbDefineVarRoute rule in Astro.

WMDB-190 (warning) Failed to get contact from technology file.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-191 (error) Failed to create master cell ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-192 (error) Failed to set the port type for port ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-193 (error) Failed to create pin ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-194 (warning) Failed to set var route rule ’%s’ for net

’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-195 (error) Failed to get the net ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-196 (error) Failed to get the cell instance ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-197 (error) Failed to get the port ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-198 (error) Failed to connect port ’%s’ with net ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-199 (error) Failed to connect a port with net ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-200 (information) Failed to update capacitance mode to

TLU+.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-201 (error) Invalid number of Milkyway boundary points.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-202 (error) Failed to get Milkyway cell boundary.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-203 (error) Failed to convert Milkyway boundary.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-204 (error) Failed to calculate standard cell area in

current cell.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-205 (error) Failed to calculate standard cell area for cell

’%s.%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-206 (error) Failed to calculate area for current cell.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-207 (error) Failed to calculate area for cell ’%s.%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-208 (error) Failed to create wire direction on layer ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-209 (information) Searching for any single pin nets.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-210 (warning) Failed to mark the db sync flag in milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-211 (warning) Failed to mark the SDC sync flag in milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-212 (warning) Failed to mark the Hierarchy preservation

flag in Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-213 (warning) Failed to mark the write_mdb flag in

Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-214 (error) Failed to close cell ’%s’ view ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-215 (warning) Failed to get data for cell instance ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-216 (warning) Failed to set status for cell instance ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-217 (error) Failed to get tile(site) info, name ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-218 (error) Failed to create tile pattern for site ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-219 (warning) Failed to update base array Bbox, name

’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-220 (error) Failed to create cell row, name ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-221 (error) Failed to set cell row tile.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-222 (error) Failed to set cell row pattern.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-223 (error) Failed to get tile pattern number, parttern

’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-224 (error) Failed to set cell row tile pattern record to parttern ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-225 (error) Failed to set cell row starting tile, site ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-226 (error) Layer id ’%d’ exceeds Milkyway Layer id limit

’%d’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-227 (error) Failed to find layer ’%s’ in Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-228 (error) Failed to create wire track.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-229 (error) Failed to compute wire track boundary BBox.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-230 (error) Failed to set wire track boundary BBox.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-231 (error) Failed to purge existing wire tracks in Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-232 (error) Failed to purge existing wire directions in

Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-233 (error) Eeq class number exceeds Milkyway limit.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-234 (error) Failed to create a pin for port '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-235 (error) Failed to create wire master for net.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-236 (error) Failed to create wire for net.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-237 (error) Failed to connect route segment with wire.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-238 (error) Failed to set net Max/Min layer.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-239 (error) Failed to create via ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-240 (error) Failed to read vias from design.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-241 (warning) Via ’%s’ cut dimensions do not match.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-242 (warning) Via ’%s’ cut spacing do not match.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-243 (warning) Via ’%s’ enclosure dimensions are too short.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-244 (warning) Ignore via ’%s’ which violates the Min

Area rule in tech file.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-245 (error) Internal error for via ’%s’ rule.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-246 (information) Stack vias not supported ’%s:%d’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-247 (error) Failed to create global route for net.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-248 (error) Failed to connect global route to net.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-249 (error) Number of nets does not match number of

ports or cell masters or cell instances.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-250 (error) PGConnect failed.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-251 (error) Failed to create placement blockage.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-252 (error) Internal error for routing obstr in layer ’%d’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-253 (error) Failed to create routing blockage.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-254 (information) Reassign group %s from region %d to

region %d.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-255 (error) Failed to get object type.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-256 (error) Region ’%d’ is not a soft block.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-257 (error) Failed to find group ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-258 (error) No any groups specified.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-259 (error) Failed to create cell region.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-260 (error) Failed to get group by name ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-261 (error) Failed to get group size.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-262 (error) No cell instance in group ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-263 (warning) Group ’%s’ has been bounded to region ’%d’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-264 (warning) Failed to set group parent, group ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-265 (error) Failed to assign group to region.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-266 (error) Failed to update region group name

property.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-267 (error) Failed to delete group ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-268 (error) Failed to create group ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-269 (error) Failed to create property for group ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-270 (error) Failed to get group property.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-271 (error) Failed to get expanded cell instance.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-272 (error) Cell boundary for cell instance ’%s’ is null.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-273 (error) Failed to update group ’groupLength’ property, group ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-274 (error) Failed to update group ’groupSize’ property,

group ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-275 (error) Failed to purge existing tile patterns in Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-276 (error) Failed to purge existing cell rows in Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-277 (error) Failed to purge existing base arrays in

Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-278 (information) Update port shape ... port ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-279 (error) Failed to get port data, port ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-280 (error) Cell ’%s’ doesn’t exist in view ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-281 (error) Version ’%d" of cell ’%s’ doesn’t exist in view

’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-282 (error) Failed to get the place group ’%s’.

DESCRIPTION

While creating a floor plan group, write_mdb detects that no place group with the given name existed. However, a plan group is usually based on a place group.

WHAT NEXT

Please create a place group using the given name first.

SEE ALSO

WMDB-283 (error) Failed to create plan group ’%s".

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-284 (error) Failed to create/update ’%s’ property, value

’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-285 (warning) Bus information was not correctly set for port ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-286 (warning) Bus information was not correctly set for

net ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-287 (warning) Failed to set net name ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-288 (warning) Failed to set net type.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-289 (error) Failed to createa ports for design ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-290 (error) Failed to createa connections for design

’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-291 (error) Failed to lock library;

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-292 (error) Internal error, ignore non-default rule for

layer ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-293 (error) Internal error for via ’%s’ rule.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-294 (warning) Failed to set the boundary for design.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-295 (warning) Physical information will not be translated. Set the chip boundary to translate physical

information.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-296 (error) Internal error, failed to map layer ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-297 (error) Failed to create port instance for net ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-298 (warning) Pin ’%s’ doesn’t have complete physical

information, created in default location.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-299 (error) Failed to set port shape for pin '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-300 (error) Failed to set the Non default rule '%s' on net '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-301 (error) Failed to get the Non default rule width for

net ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-302 (warning) Wire extension doesn’t comply with

milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-303 (error) Failed to create a route segment for net ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-304 (warning) Placement blockage type not supported.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-305 (error) Failed to create a logical view for cell ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-306 (warning) Wire direction may be incorrect.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-307 (information) Design not uniquified, only logic view will be created.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-308 (error) Failed to create LOGIC view for library '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-309 (warning) Failed to preserve the Hierarchy

information.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-310 (information) Updating SDC information...

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-311 (information) Done updating SDC information.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-312 (error) Failed to get net name.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-313 (error) Failed to get library id from cell id('%d').

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-314 (error) Failed to get cell instance master(id: ’%d’).

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-315 (error) Failed to get port instance master(id: ’%d’).

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-316 (error) Failed to set port net id.(port id: ’%d’)

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-317 (information) Connected %d ports to net ’%s’

through pattern ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-318 (information) Disconnected %d ports from net ’%s’

through pattern '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-319 (information) Connected %d ports to child net.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-320 (information) Disconnected %d ports from child net.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-321 (error) Iteration error.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-322 (error) Failed to get cell name.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-323 (information) On cell ’%s’:

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-324 (error) Failed to get cell instance count in cell ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-325 (information) Net ’%s’ does not exist, create it now …

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-326 (information) Can not find matched port for inputing

port pattern.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-327 (error) Failed to get net type for net '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-328 (information) Net '%s' in cell '%s' has type '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-329 (information) Net '%s' in cell '%s' has different

subtype than that currently specified.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-330 (error) Failed to create port by net ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-331 (error) Failed to create cell "PG connected port" property, net ’%s’, cell ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-332 (error) Failed to remove PGConnect created port,

by net ’%s’, in cell ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-333 (error) Must choose Disconnect mode when

deleting top cell port.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-334 (error) Failed to connect/disconnect PG.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-335 (error) Milkyway host initialization failed.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-336 (error) Milkyway DB initialization failed.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-337 (error) Milkyway ax initialization failed.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-338 (error) Library path is NULL.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-339 (error) Can not purge technology information.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-340 (error) Failed to initialize technology main table.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-341 (error) Failed to build technology main table.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-342 (error) Failed to set port name for port ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-343 (warning) Cannot get tile table for tile ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-344 (error) Failed to update the property for tile ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-345 (error) Failed to create tile table ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-346 (error) Failed to create tile in paramset ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-347 (error) Tile pattern with name ’%s’ has existed in

DB, creation failed.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-348 (error) Failed to create tile pattern ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-349 (error) The tiles are not set correctly.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-350 (warning) Failed to get a Bounding box for the

design.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-351 (error) Failed to get the default contact by layer ’%d’

and ’%d’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-352 (error) Failed to get library contact table.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-353 (error) Failed to attach the TLUPlus file.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-354 (error) No Milkyway design specified.

DESCRIPTION

WHAT NEXT

```
You need to specify a Milkyway library either from the command line or through
setting the ’mw_design_library’ var previous to ’read_mdb/write_mdb’ command. e.g.,
to set the var, please follow, set mw_design_library design_lib_name write_mdb

view man page to see how to specify from command line.
```

SEE ALSO

WMDB-355 (warning) No reference libraries set for Milkyway design.

DESCRIPTION

This warning message occurs when a reference library is not specified to the main Milkyway database library (the design library). Link errors may occur if the reference libraries are not specified for the design.

WHAT NEXT

This is only a warning message. A reference library is required for resolving cell instances.

You can specify a reference library by setting the **mw_reference_library** variable, as shown in the example below, before using the the **create_mw_design** command:

```
psyn_shell-t> set mw_reference_library "ref_lib_name1 ref_lib_name2"
```

You can also specify the reference library by running the **set_mw_design** command as shown in the following example:

```
psyn_shell-t> set_mw_design
```

SEE ALSO

create_mw_design(2)
set_mw_design(2)

WMDB-356 (error) Failed to save the milkyway db for design

’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-357 (information) write_mdb done successfully.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-358 (error) Failed to set ’%s’ variable.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-359 (error) No Milkyway cell specified.

DESCRIPTION

WHAT NEXT

```
You need to specify a Milkyway cell either from the command line or through setting
the ’mw_cell_name’ var previous to ’read_mdb’ command. e.g., to set the var, please
follow, set mw_design_library mdb_design_name set mw_cell_name mdb_cell_name
read_mdb

Please view man page to see how to specify from command line.
```

SEE ALSO

WMDB-360 (error) Failed to link the design.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-361 (information) read_mdb will read only the logic db.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-362 (error) Failed to update the physical information for cell '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-363 (error) Failed to update the changed netlist

information for cell '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-364 (information) read_mdb done successfully.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-365 (error) Failed to open reference library '%s'.

DESCRIPTION

This error message occurs when the tool fails to open the specified reference library.

A reference library is required for resolving cell instances.

WHAT NEXT

Make sure you specified the correct reference libraries and that all of the libraries are accessible.

SEE ALSO

create_mw_design(2)
set_mw_design(2)

WMDB-366 (warning) No pdb library present for the reference

library ’%s’.

DESCRIPTION

This warning message occurs when the **create_mw_design** command cannot find the physical library database for the specified reference library.

Physical library databases that provide physical information are required by the **link_physical_library** command. The **create_mw_design** command automatically adds the physical library databases from reference libraries to the **physical_library** variable.

WHAT NEXT

This is only a warning message. No action is required.

However, if you want the physical information from the reference Milkyway database library, make sure that sure that the physical database library exists for it.

SEE ALSO

create_mw_design(2)
link_physical_library(2)

WMDB-367 (information) Dumping plib from milkyway technology file...

DESCRIPTION

This information message occurs when the **create_mw_design** command is in the process of dumping the physical library from the Milkyway technology file.

WHAT NEXT

This is only an informational message. No action is required.

SEE ALSO

create_mw_design(2)

WMDB-368 (error) Failed to dump physical library from

Milkyway design library '%s'.

DESCRIPTION

This error message occurs when the **create_mw_design** command fails to dump the physical library based on the specified technology file.

WHAT NEXT

Check that your technology file is correct and run the command again.

SEE ALSO

create_mw_design(2)

WMDB-369 (information) Replacing reference libary for design library '%s'.

DESCRIPTION

This information message occurs when the **set_mw_design** command is replacing the old reference libraries in current **mw_design_library** with the new libraries.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

set_mw_design(2)
mw_design_library(3)
mw_reference_library(3)

WMDB-370 (error) Failed to get reference library for design library '%s'.

DESCRIPTION

This error message occurs when the tool cannot obtain the reference libraries for a specific Milkyway design library.

WHAT NEXT

Make sure that the **mw_reference_library** is properly set for the current **mw_design_library** variable.

SEE ALSO

create_mw_design(2)
set_mw_design(2)
mw_design_library(3)
mw_reference_library(3)

WMDB-371 (error) Failed to create Milkyway design library '%s'.

DESCRIPTION

This error message occurs when the tool fails to to create a Milkyway design library.

WHAT NEXT

Make sure you run the flow correctly. For a detailed description of how to run the flow, refer to the **create_mw_design** command man page.

SEE ALSO

create_mw_design(2)

WMDB-372 (error) Failed to import the physical library '%s'.

DESCRIPTION

This error message occurs when the **create_mw_design** command fails to import the specified physical library database.

WHAT NEXT

Verify that you provided the correct physical library database by checking the value of the **physical_library** variable.

SEE ALSO

create_mw_design(2)
physical_library(3)

WMDB-373 (error) Failed to create TLUPlus model for Library '%s'.

DESCRIPTION

This error message occurs when the **create_mw_design** command fails to create the TLUPlus model for the current **mw_design_library** variable.

WHAT NEXT

Verify that both the TLU table file and the layer map file are correct and then run the command again.

SEE ALSO

create_mw_design(2)
mw_design_library(3)

WMDB-374 (error) Failed to get TLUPlus attach file '%s'.

DESCRIPTION

This error message occurs when the **create_mw_design** command fails to get the TLUPlus attach file for the current **mw_design_library** variable.

WHAT NEXT

Verify that the TLUPlus file is created correctly.

SEE ALSO

create_mw_design(2)
mw_design_library(3)

WMDB-375 (error) Failed to remove reference libraries for design library '%s'.

DESCRIPTION

This error message occurs when the **create_mw_design** command fails to remove old reference libraries from the current design library while attempting to replace them with the new libraries.

WHAT NEXT

Verify that you are using the correct design library and run the command again.

SEE ALSO

create_mw_design(2)

WMDB-376 (warning) Failed to add reference library '%s' for design library.

DESCRIPTION

This warning message occurs when the **create_mw_design** command fails to add the specified reference library to the design library.

WHAT NEXT

Verify that the reference libraries you specify meet the following criteria:
 1. The reference library does exist.
 2. The reference library is not the same as the design library.
 3. The reference library is accessible.
 4. The reference library is consistent with the main library in the technology file.
 5. The reference library does not exist in the main library reference list.

SEE ALSO

create_mw_design(2)

WMDB-377 (information) Unable to get direction for port,

assuming INPUT.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-378 (information) Unable to get direction for leaf port.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-379 (warning) Failed to get port type.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-380 (warning) Failed to get hierarchical net name.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-381 (warning) Failed to set routing segment width on a

layer for net ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-382 (warning) Failed to read the GCEL grid from milkway design library.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-383 (information) ’stop at any level’ functionality is disabled by variable ’disable_mdb_stop_points’.

DESCRIPTION

This information message occurs when the **disable_mdb_stop_points** is set to **true**, which disables the "stop at any level" function for the current command.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

disable_mdb_stop_points(3)

WMDB-384 (information) Cell '%s' is a stop_point (module %s).

DESCRIPTION

This information message occurs when the current cell is a stop point module. The **write_mdb** command will not explore the submodules of the current cell. The **write_mdb** command will annotate the nonleaf macro modules as the stop points.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

write_mdb(2)
disable_mdb_stop_points(3)

WMDB-385 (error) region %s is disjointed, which is not allowed in Milkyway.

DESCRIPTION

Current region contains disjointed areas, which is not supported by Milkyway. write_mdb will not save this region to Milkyway.

WHAT NEXT

Change the disjointed region into different regions and do write_mdb again.

SEE ALSO

create_region (3) remove_region (3)

WMDB-386 (error) Failed to create/update property %s for %s.

DESCRIPTION

write_mdb failed to create or update the property for the given object. This will lead to the property missing in the design.

WHAT NEXT

Please make sure the disk space is enough for milkyway. Also verify your data and try again.

SEE ALSO

WMDB-387 (error) Failed to add hierarchical cell %s to the voltage area %s.

DESCRIPTION

write_mdb failed to add a hierarchical cell (and its sub-cells) into the voltage area. This is usually caused by a corrupted hierarchy on the db side.

WHAT NEXT

Verify your data and try again.

SEE ALSO

create_region (3)

WMDB-388 (Warning) Unit conversion needed, this could lead to precision loss.

DESCRIPTION

Current design has different "distance unit" value than the one in target mdb library (specified in the tf file). Therefore write_mdb needs to do the unit conversion.

WHAT NEXT

SEE ALSO

write_mdb (2)

WMDB-389 (error) Unit conversion could lead to precision loss

due to roundoff errors. To proceed regardless of precision loss, use the -enforce_scaling option.

DESCRIPTION

This error occurs because the tool defines the distance unit based on the unit described in the first physical input (for example, in DEF). The error is caused because the current design has a higher distance unit value than the one in the target mdb library (specified in the tf file). Writing does not continue due to the possible data loss caused by roundoff errors during unit conversion.

WHAT NEXT

Use the **-enforce_scaling** option to enforce this unit conversion regardless of potential precision loss due to roundoff errors.

WMDB-390 (Info) Unit conversion between pdb and mdb. This could lead to precision loss.

DESCRIPTION

The specified pdb file(s) have different "distance unit" value as the one in target mdb library (specified in the tf file). Therefore the unit conversion could have precision loss. This usually happens when you specify your own pdb file instead of the one generated by write_mdb.

WHAT NEXT

Adjust the unit per micro value in pdb files before write_mdb.

SEE ALSO

write_mdb (2)

WP-1 (error) '%s' is an invalid write_parasitics format. Valid formats are '%s'.

DESCRIPTION

The **write_parasitics** command has two valid formats: **reduced** and **actual**. By default the parasitics file is generated in reduced format.

WHAT NEXT

Use **write_parasitics -format reduced** or **write_parasitics -format actual**. Read the **write_parasitics** man page for more information on writing a parasitics file.

WP-2 (error) '%.2f' is an invalid write_parasitics ratio. It will be ignored. Valid ratio is in the range 0.0-1.0.

DESCRIPTION

The **write_parasitics** command ratio has to be in the range 0.0 - 1.0. By default the nets in the reduced format are generated with ratio equal to 0.5. The capacitor closest to the driver is 0.5 times the total net capacitance.

WHAT NEXT

Read the **write_parasitics** man page for more information on writing a parasitics file.

WP-3 (information) Writing parasitics to file '%s'.

DESCRIPTION

The command **write_parasitics** is writing a parasitics file to disk. Check the **write_parasitics** man page for information on how to use the command. Use the **write** command to write a netlist for the current design before using the **write_parasitics** command. This is because **write** can change names and the new names should appear in the parasitics file as well. This message indicates the disk location of the parasitics file created with **write_parasiticspp**.

WHAT NEXT

The parasitics file can be used in layout tools or other tools reading **write_parasitics** file formats.

WP-4 (warning) Can’t use the ’%s’ option with the -format "actual" option.

DESCRIPTION

The specified option cannot be used with the -format "actual" option. It will be ignored.

WHAT NEXT

Read the **write_parasitics** man page for more information on writing a parasitics file.

WP-5 (warning) The -format ’%s’ option is currently unsupported. The reduced format will be used to generate the parasitics file.

DESCRIPTION

The nets in the parasitics file will be in the reduced SPEF format.

WHAT NEXT

Read the **write_parasitics** man page for more information on writing a parasitics file.

WP-6 (error) The design does not have routed information.

DESCRIPTION

You receive this message because using the **write_parasitics** command with the **-distributed** option requires routed information in psyn_shell. In icc_shell you need to run extract_rc before you can write parasitics.

WHAT NEXT

In psyn_shell before running this command, you must run the **compile_physical**, **legalize_placement**, **physopt**, or **run_router** command. In icc_shell you must run extract_rc.

SEE ALSO

compile_physical (2), **legalize_placement** (2), **run_router** (2), **write_parasitics** (2). **extract_rc** (2).

WP-7 (warning) Net %s has more than max number of fanouts. Not putting net information in SPEF.

DESCRIPTION

You receive this message because the **write_parasitics** command with the **-distributed** option writes out only information for nets with less than the maximum number of fanouts. The **high_fanout_net_threshold** variable defines the maximum number of fanouts.

WHAT NEXT

You must use the **set_load** and **set_resistance** commands for any net with greater than the maximum number of fanouts.

SEE ALSO

set_load (2), **set_resistance** (2), **write_parasitics** (2), **steiner_route_fanout_limit** (3).

WP-8 (warning) Header information is missing: %s.

DESCRIPTION

You receive this warning message because you issued the **extract_rc** command but did not specify all header information. The SPEF writer continues to print out the file even though it is missing the indicated field. This missing field might cause problems for the SPEF reader.

WHAT NEXT

Ensure that you provide all header information and reexecute the command.

SEE ALSO

extract_rc (2).

WP-9 (warning) Unsupported direction. Using default direction (BIDIRECTION).

DESCRIPTION

You receive this warning message because the specified direction of a port is not supported by the SPEF file format. The default direction is used.

The SPEF file format supports three directions: INPUT, OUTPUT, and BIDIRECTION.

WHAT NEXT

Specify a supported direction for the port and reexecute the **extract_rc** command.

SEE ALSO

extract_rc (2).

WP-10 (error) Only supports the writing out of the net type.

DESCRIPTION

You receive this error message because you executed the **write_sdc** command and specified a file type to be written out that is not supported. The SPEF writer can only write out the net type.

WHAT NEXT

Reexecute the **write_sdc** command and specify a net type.

SEE ALSO

write_sdc (2).

WP-12 (error) Not able to write out the %s of net %s.

DESCRIPTION

The writer has problem writing out the indicated section due to an internal error.

WHAT NEXT

Please call the application support center and report the problem.

WSCR-001 (error) Cannot open the output file %s

DESCRIPTION

The output file for write_script cannot be opened.

WHAT NEXT

Verify that the path for the file name exists. If the path does exist, make sure you have access permission.

WSCR-002 (information) SDC supports a subset of the contraints supported by Primetime. Some constraints may not be preserved by write_sdc.

DESCRIPTION

The Synopsys Design Constraints (SDC) format is a subset of the constraints supported by PrimeTime. Some of the constraints which you applied to the design may not be written to SDC. Others may only be partially written.

The following is a complete list of the constraints which are written to SDC with limitations:

- For **set_driving_cell**, the -min and -max options are not supported.

- For **set_port_fanout_number**, the -min and -max options are not supported.

WHAT NEXT

WSCR-003 (information) The design has rise/fall qualified exceptions which will not be written out.

DESCRIPTION

Rise/Fall qualified exceptions are only supported by Primetime. So write_script will

not write out these exceptions for dcsh or dctcl mode. write_sdc also will not write these exceptions.

WHAT NEXT

WSCR-004 (warning) Your SDC output may contain ambiguous names because you have set the variable sdc_write_unambiguous_names to FALSE.

DESCRIPTION

Beginning with version 1.2, the Synopsys Design Constraints (SDC) format has features ensuring that the cell, net, pin, lib_cell, and lib_pin names written to the file are unambiguous. Some third party applications do no understand these features.

You can set the **sdc_write_unambiguous_names** variable to **false** to suppress these features. This warning reminds you that the setting of this variable may cause your SDC output to be ambiguous.

WHAT NEXT

Verify that you really want to disable the writing of unambiguous names. Review the man pages for the **write_sdc** command and the **sdc_write_unambiguous_names** variable.

SEE ALSO

write_sdc (2), **sdc_write_unambiguous_names** (3).

WSCR-005 (warning) Clock '%s' created with -add option will not be written out.

DESCRIPTION

Multiple clock defination on same pin/port is only supported by PrimeTime. So write_script will not write out these clocks for dcsh or dctcl mode. write_sdc also will not write these clocks.

WHAT NEXT

WSCR-006 (warning) Cannot disable %s objects from %s to %s.

DESCRIPTION

The write_script command has found multiple arcs between the pins noted in the message, such that a non-zero subset of the arcs is disabled and at least one arc is not disabled. Moreover, the write_script command is unable to generate a **filter expression** based on the attributes of the arc objects that can completely distinguish the subset of disabled arcs from the non-disabled ones. If it is the case that some, but not all, of the disabled arcs can be distinguished, then the write_script command will cause that subset only to be disabled.

WHAT NEXT

To match the set of disable arcs between the pins, you need to replicate the methodology by which the arcs were disable in the first place and append the necessary commands to the script file generated by the write_script command.

WT-3 (information) Writing timing information to file '%s'.

DESCRIPTION

The command **write_timing** is writing a timing file to disk. Check the **write_timing** man page for information on how to use the command. Use the **write** command to write a netlist for the current design before using the **write_timing** command. This message indicates the disk location of the timing file created with **write_timing**.

WHAT NEXT

The timing file can be used in simulation tools or other tools reading **write_timing** file formats.

WT-4 (warning) Invalid time scale specified. Assuming '1'.

DESCRIPTION

The time scale is set with the variables **vhdlout_time_scale** and **sdfout_time_scale** for the sdf and synopsys_vhdl timing formats. The time scale must be an integer value greater than zero.

In the synopsys_vhdl format, timing information is written in 1ns, 1ps or 1us only. The time unit choosen is the time unit specified in the technology library. For example, if the time unit is specified in nanoseconds, the timing data will be written in nanoseconds. If the library time unit is "10ns", the scaling is 10 and the unit is nanoseconds, the timing data is multiplied by 10 and is written in nanoseconds. If there is no time unit in the library, the unit is assumed to be nanoseconds, and the scale is the value of the environment variable **vhdlout_time_scale**. For example, if the library has no time unit specified but is in 0.1 ns, set **vhdlout_time_scale** to 0.10 in order to scale the data to nanoseconds. If **vhdlout_time_scale** is not specified, 1 is the default.

In the sdf format, timing information can be written in 1 10 and 100 multiples of ns ps and us. The time unit in the sdf file is the time unit specified in the technology library and will be written in the timing file under TIMESCALE. If there is no time unit in the library, the unit is assumed to be a multiple of nanoseconds, and the multiple is the value of the environment variable **sdfout_time_scale**. For example, if the library has no time unit specified but is in 10 ns, set **sdfout_time_scale** to 10 in order to specify the time unit as 10ns and write a timing file in 10ns. If **sdfout_time_scale** is not specified, 1 is the default.

WHAT NEXT

The timing file was written with a default time scale of 1. If the library was not in 1ns, 1ps or 1us, you need to re-write the timing file after setting the value of **vhdlout_time_scale** or **sdfout_time_scale**. To avoid this warning message, set the value of **vhdlout_time_scale** or **sdfout_time_scale** to 1 if the library is already in 1ns, 1ps or 1us, or to the scale unit of the library. The value of **sdfout_time_scale** can only be 1, 10 or 100.

WT-5 (error) Invalid write_timing format specified. Valid formats are synopsys_vhdl, sdf, sdf-v2.1.

DESCRIPTION

An invalid format was requested for the **write_timing** command. The **write_timing** command valid formats are synopsys_vhdl, sdf-v2.1 and sdf.

WHAT NEXT

Re-write the timing file using either **write_timing -format synopsys_vhdl** or **write_timing -format sdf** or **write_timing -format sdf-v2.1**.

WT-6 (warning) Using '%s' vhdl time scale of '%f %s'.

DESCRIPTION

The technology library has timing for cells but no timing unit explicitly specified. This warning indicates the time scale used when writing a timing file in synopsys_vhdl format.

WHAT NEXT

The timing unit of the timing in the technology library should be the same as the time scale specified in this message. If it is different, set **vhdlout_time_scale** to the timing unit of the library. For example, if the technology library is in 10ns, use: **vhdlout_time_scale = 10**.

To determine the current value of **vhdlout_time_scale**, use: **list vhdlout_time_scale**.

WT-7 (warning) Design contains black-box components. These

cells will have no timing information.

DESCRIPTION

A timing file is written for the current design but the design contains cells with no timing. Those cells have no timing because they were not found in the technology libraries in the search path.

WHAT NEXT

Use the **link -all** command to list which cells are black-box components. Modfify the **search_path** if necessary to solve the link errors before writing the timing file again.

WT-9 (warning) Using '%s' sdf time scale of '%f %s'.

DESCRIPTION

The technology library has timing for cells but no timing unit explicitly specified. This warning indicates the time scale used when writing a timing file in sdf format.

WHAT NEXT

The timing unit of the timing in the technology library should be the same as the time scale specified in this message. If it is different, set **sdfout_time_scale** to the timing unit of the library. For example, if the technology library is in 10 ns, use: **sdfout_time_scale = 10**.

The valid values for **sdfout_time_scale** are 1, 10 and 100. To determine the current value of **sdfout_time_scale**, use: **list sdfout_time_scale**.

WT-12 (error) Invalid write_timing context. Valid contexts are vhdl, verilog.

DESCRIPTION

The **-context** option of **write_timing** indicates if the sdf timing file will be used with a verilog or a vhdl netlist. The context name must be one of "vhdl" or "verilog". "vhdl" is the default. With the synopsys_vhdl format, the context is implicitly "vhdl". With the vhdl context, when library cell names have invalid vhdl names, cell names are modified to follow vhdl naming conventions before being written in the timing file. With the verilog context, the library cell names are written to the timing file without modifications.

WHAT NEXT

Use **write_timing** with **-context vhdl** or **-context verilog**.

WT-13 (warning) The timing file might contain invalid vhdl names if the library '%s' has invalid vhdl cell names.

DESCRIPTION

The library used for timing the design is older than v2.2. Libraries created before v2.2 can have cell reference names invalid under the VHDL naming conventions. With invalid vhdl names in the library, the timing file might contain invalid vhdl names if the design refers to cells with invalid names.

WHAT NEXT

If the cell reference names in the library are invalid, the timing file will contain invalid vhdl names. The library needs to be recompiled with Library Compiler of v2.2 or later release.

XDC-1 (error) Can’t open an X Window.

DESCRIPTION

WHAT NEXT

XG-100 (error) The command '%s' is not yet supported in XG mode.

DESCRIPTION

This version of XG mode does not support the requested command. This will be supported in a future release.

WHAT NEXT

SEE ALSO

XG-101 (error) The option '%s' for command '%s' is not yet supported in XG mode.

DESCRIPTION

This version of XG mode does not support the requested option of the command. This will be supported in a future version.

WHAT NEXT

SEE ALSO

XG-102 (error) The command '%s' will not be supported in XG mode.

DESCRIPTION

XG mode does not support the requested command.

WHAT NEXT

SEE ALSO

XG-103 (error) The option '%s' for command '%s' will not be supported in XG mode.

DESCRIPTION

XG mode does not support the requested option for this command.

WHAT NEXT

SEE ALSO

XG-104 (error) EDIF format support is disabled in XG mode.

DESCRIPTION

This error message occurs when you are trying to read or write EDIF format which is not supported in XG mode.

WHAT NEXT

Use supported standard formats.

SEE ALSO

XNFI-1 (error) %s

DESCRIPTION

An error message from the XNF reader.

WHAT NEXT

Correct the problem in your XNF file and reread.

XNFI-2 (warning) %s

DESCRIPTION

A warning message from the XNF reader.

WHAT NEXT

Verify the cause of the warning, correct your XNF file, and reread the file if necessary.

XNFI-3 (info) %s

DESCRIPTION

An informational message from the XNF reader.

WHAT NEXT

XNFI-4 (error) Cannot open file '%s'.

DESCRIPTION

The XNF reader was unable to open a particular file.

WHAT NEXT

Be sure that the file you have identified in the **read** command actually exists.

XNFI-5 (error) Cannot create design '%s'.

DESCRIPTION

The XNF reader was unable to create the named design.

WHAT NEXT

XNFI-6 (warning) Xilinx family '%s' is currently not supported by the XNF reader.
The following format(s) are currently supported: %s.

DESCRIPTION

The components that can be specified in XNF are different for different Xilinx families. This message indicates that, according to the Xilinx reader, the family for this particular XNF file is not currently supported.

WHAT NEXT

Convert your XNF design to a family that is supported.

XNFI-7 (warning) Assuming Xilinx family '%s' for the reading of these XNF file(s).

DESCRIPTION

The XNF reader is making an assumption regarding the family for these XNF files.

WHAT NEXT

XNFI-8 (info) Reading submodule '%s' in file '%s'

DESCRIPTION

The XNF parser is reading a hierarchical submodule of the XNF design, which is contained in the given file.

WHAT NEXT

XNFI-9 (warning) No ports were created in design '%s' because the XNF file had no EXT records.

DESCRIPTION

Design Compiler requires that a design's interface be completely defined when it is read in. The "external interface" for an XNF design is defined by the EXT records in the XNF file. The XNF reader defines a port on your design for each EXT record the XNF file contains. This message warns that your XNF file has no EXT records and, as a result, the design just created has no ports.

Unfortunately, XNF is not rigorous about defining the external interface to a hierarchical element of a design. In fact, any signal inside a hierarchical design can be used as an "interface" to the outside world. Which means that the interface for a design depends on the particular instantiation, because it is legal for different instantiations of the same design to use different signals as "interfaces." Although this situation probably brings joy to the hearts of hackers, imagine as an analogy a function written in C that could have ANY of its internal variables available to the calling routine.

This "feature" of XNF causes problems for Synopsys tools and leads us to "uniquify" a design "on the fly" as it is being read in, creating a unique design reference for each instance of a hierarchical design.

This works just fine for every design in the hierarchy *except* the top level, where we are forced either to require a definition for the interface to the design, or to create a port for every net that exists in the design. We've opted for the former, so that means you need to do one of the following:

• Add EXT records to your XNF so that we can build an interface for your design when reading in the XNF.

• Use the **create_port**, **create_net**, and **connect_net** commands to do this from inside

dc_shell.

Good luck.

WHAT NEXT

Add EXT records to your XNF file, defining the external interface for your design. Or use the **create_port**, **create_net**, and **connect_net** commands to do this from inside **dc_shell**.

XNFO-1 (warning) %s '%s' is renamed to '%s' in design '%s' because it isn't a legal name.

DESCRIPTION

The Xilinx Netlist Format (XNF) language has a restricted character set for naming component symbols and signals. This message indicates that the XNF writer has renamed a component in your design so that it will be syntactically legal in the XNF language.

WHAT NEXT

You may want to alter your design description to use names that are legal in XNF. For more information about legal names in XNF, see the specification for the language, available from Xilinx.

XNFO-2 (warning) %s '%s' is renamed to '%s' in design '%s' because of %s of the same name.

DESCRIPTION

This message indicates that the XNF writer has renamed a component or net in your design to remove a name clash between the component or net and another component or net.

WHAT NEXT

You may want to alter your design description to use names that do not conflict.

XNFO-3 (warning) Pin '%s' on cell '%s' has no direction. Not written.

DESCRIPTION

The Xilinx Netlist Format (XNF) language assumes that all pins on components must have a direction attribute. This message indicates that the XNF writer has encountered a pin in your design without a direction attribute.

WHAT NEXT

Check your design description to see if you specified the correct pin. Also, make sure your design is correctly linked (via the **link** command).

XNFO-6 (error) Unable to open XNF output file '%s'.

DESCRIPTION

This error message occurs when the XNF writer is unable to open a file where XNF output will be placed. Remember that the XNF language specifies hierarchy in a design through the use of separate files, and that an XNF file will be written out for each level of the hierarchy.

WHAT NEXT

Find out why the named file cannot be opened, fix the problem, and try writing out your design again.

XNFO-7 (information) Writing XNF output file '%s' for submodule '%s'.

DESCRIPTION

This informational message tells you that the XNF writer is writing a separate file for a submodule in your hierarchical design. Remember that the XNF language specifies hierarchy in a design through the use of separate files, and that an XNF file will be written out for each level of the hierarchy.

WHAT NEXT

You do not need to take any action regarding this message. If you do not want your design to be written out flat instead of hierarchically, you need to flatten the design inside the dc_shell. First, use the *ungroup* command to remove the hierarchy. Second, generate gates for the XNF writer, using the *replace_fpga* command. Then use the *write* command to write out the XNF for the design.

XNFO-8 (error) Cell instance '%s' in design '%s' is a CLB. Xilinx does not allow CLB symbols in XNF for their 4000 family FPGAs.

Please run the command ’replace_fpga’ to convert the CLBs in this
design to gates.

DESCRIPTION

Xilinx does not currently (as of March 1992) support a representation for programming 4000 family CLB components directly in XNF, even though previous Xilinx families have in the past supported this capability. This error message is issued whenever the XNF writer detects a CLB component in your design.

WHAT NEXT

Use the **replace_fpga** command to convert all CLBs into primitive gates. During the conversion, the **replace_fpga** command notates the internal design representation with information that describes the boundaries of F, G and H logic generators in each CLB. [This programming information for the F, G and H blocks is the only kind of CLB programming currently allowed by Xilinx for the 4000 family.] The netlist writer uses the annotated boundary information to "program" the logic generator blocks in each CLB.

After the **replace_fpga** command converts all CLBs, call the **write** command.

XNFO-9 (warning) Design ’%s’ was modified after it was converted to gates
using the command ’replace_fpga’, and the ’write’ command cannot insure
that the FMAP and HMAP information on the design is still valid.
Therefore, no FMAP or HMAP information will be written for this design.

DESCRIPTION

Xilinx does not currently (as of March 1992) support a representation for programming 4000 family CLB components directly in XNF, even though previous Xilinx families have in the past supported this capability.

This warning message indicates that the design has been modified between the time that **replace_fpga** and **write** were run. Therefore, the XNF writer can not guarantee that the mapping information on the design for FMAP and HMAP constructs is still correct.

WHAT NEXT

Use the **replace_fpga** command to convert all CLBs into primitive gates. During the conversion, the **replace_fpga** command notates the internal design representation with information that describes the boundaries of F, G and H logic generators in each CLB. [This programming information for the F, G and H blocks is the only kind of CLB programming currently allowed by Xilinx for the 4000 family.] The netlist writer uses the annotated boundary information to "program" the logic generator blocks in each CLB.

After the **replace_fpga** command converts all CLBs, call the **write** command. Do not call any commands that could change the design representation between the calls to **replace_fpga** and **write**.

XNFO-10 (error) Map information contained in map_bag '%s' on design '%s' is not valid. This mapping information will not be written out as FMAP or HMAP constructs in XNF.

DESCRIPTION

Xilinx does not currently (as of March 1992) support a representation for programming 4000 family CLB components directly in XNF, even though previous Xilinx families have in the past supported this capability. Therefore you must the **replace_fpga** command to convert all CLBs into primitive gates. During the conversion, the **replace_fpga** command will notate the internal design representation with information that describes the boundaries of F, G and H logic generators in each CLB. [This programming information for the F, G and H blocks is the only kind of CLB programming that is currently allowed by Xilinx for the 4000 family.] The netlist writer will use the annotated boundary information to "program" the logic generator blocks in each CLB. This mapping information is stored in a set of "map_bag"s on the design. If the design is somehow modified between the time that the map bags are created and the time that XNF is written out, this message will occur, to indicate that the FMAP and HMAP mapping information contained in the bag is invalid, and that this information will not be written to XNF. This can result in a lower quality of results for Xilinx designs.

WHAT NEXT

Run the **replace_fpga** command to remove the CLB(s) from your design, and then call the **write** command. Do not call any commands that could change the design representation between the calls to **replace_fpga** and **write**.

XNFO-11 (error) Cell instance '%s' in design '%s' is an IOB. Xilinx does not allow IOB symbols in XNF for their 4000 family FPGAs.

Please run the command ’replace_fpga’ to convert the IOBs in this
design to gates.

DESCRIPTION

Xilinx does not currently (as of March 1992) support a representation for programming 4000 family IOB components directly in XNF, even though previous Xilinx families have in the past supported this capability. Therefore you must the **replace_fpga** command to convert all IOBs into primitive gates.

This error message is issued whenever the XNF writer detects an IOB component in your design. To fix the error, you need to run the **replace_fpga** command to remove the IOB(s) from your design, and then call the **write** command.

WHAT NEXT

Run the **replace_fpga** command to remove the IOB(s) from your design, and then call the **write** command.

XNFO-12 (warning) At least one GSR pin in this design is being driven by a signal other than logic zero. This presents a potential problem, because we do not write out any connection information about GSRs to XNF.

DESCRIPTION

The XNF (Xilinx Netlist Format) language does not support a GSR pin on a CLB. Therefore, we must assume that all GSR pins in the design are grounded. As a result, any logic in your design that drives a GSR pin will be removed from the actual design written out to XNF. This is serious, because it will certainly result in a design that has a different GSR behavior than the one you’ve described.

WHAT NEXT

Modify your design, removing the GSR logic.

XNFO-13 (information) %d XNF Timing Constraints Written.

DESCRIPTION

This message indicates the number of XNF timing constraints written in the XNF format. A timing constraint is written for each combinational path in the design.

The information provides feedback on the number of constraints generated so as to inform the user of the impact on the size of the XNF file and the potential runtime increase of placement and routing.

To modify this number, set to zero (0) the io_variable *xnfout_constraints_per_endpoint*.

WHAT NEXT

Run placement and routing. Then, either analyze timing within place and route environment, or back-annotate wire delays. Determine whether final wire delays meet the generated timing constraints.

XNFO-14 (information) Generating XNF Timing Constraints

DESCRIPTION

This information indicates that XNF timing constraints are being generated for output to the XNF format.

The variable value *xnfout_constraints_per_endpoint* is used to control the number of constraints written per sequential endpoint. In addition, the **dc_shell** variable *xnfout_default_time_constraints* value controls whether default time constraints will be written.

The information is provided for the user to recognize that timing constraints will be written into the XNF netlist format.

To disable generation of timing constraints, set to zero (0) the **dc_shell** variable *xnfout_constraints_per_endpoint*.

WHAT NEXT

XNFO-15 (warning) Multi-clock design, this design has %d clocks,
XNF time constraints may not be accurate between sequential

elements driven by different clock types.

DESCRIPTION

This message informs that the design has multiple clocks defined.

The XNF timing constraints format does not support more than one **Clock_To_Setup** constraint per flip-flop. Therefore, only a single C2P constraint is written per flip-flop. Which means that a flip-flop with incident paths driven by flip-flops with different clocks will have a "worst case" constraint of the two paths written out. This situation may cause timing constraints that are more constraining than necessary. This in turn can cause the Xilinx PPR program to complain about failing to meet timing constraints. When in fact the timing may be within the actual design requirements.

WHAT NEXT

Proceed with caution. Or consider disabling generation of XNF timing constraints by setting *xnfout_constraints_per_endpoint* to zero (see io_variables).

XNFO-16 (Error) Port %s does not have a pad inserted.

DESCRIPTION

This error indicates that a port in the design, which has been marked as a pad cell using set_port_is_pad, does not have a pad cell connecting to it. This is an illegal XNF netlist. Most likely there was an error during insert_pads or replace_fpga which prevented I/O pad insertion.

WHAT NEXT

Determine what failed in the insert_pads, or replace_fpga commands. Most likely there is a dont_touch on library pad cell preventing pad insertion.

XSCHDB-1 (error) ’%s’ is not a valid color. Cannot color the cursor.

DESCRIPTION

WHAT NEXT

XUI-1 (error) ’%s’ is not a valid color. Cannot color the cursor.

DESCRIPTION

WHAT NEXT

XUI-2 (warning) Can’t find font ’%s’

DESCRIPTION

WHAT NEXT

XUI-3 (warning) Using the default font

DESCRIPTION

WHAT NEXT

XUI-4 (fatal) Can’t find the default font ’%s’.

DESCRIPTION

WHAT NEXT

ZRT

ZRT-001 (error) Failed to save CEL.

DESCRIPTION

This error message indicates that the design CEL could not be saved into the Milkyway library. The reasons for this could be one of the following.

- No write permission for the Library/CEL.
- No disk space is available.

WHAT NEXT

Please check that the Milkyway design library and CEL are writeable and that there is sufficient disk space available.

ZRT-002 (error) Failed to load CEL.

DESCRIPTION

This error message indicates that the router failed to read in all the required information from the data base. The reason for this could be one of the following:

- There is some inconsistency issue in the design.
- There is some problem in the technology file.
- Certain information that is needed for the router is missing.

WHAT NEXT

Please check the Milkyway design or/and the technology file.

ZRT-003 (warn) Fail to create eco route attach file.

DESCRIPTION

This message indicates that the router failed to create or update an attachment file that describes the nets that have been changed by the eco route command. Without this file, the signoff flow may be broken. The reasons for this could be one of the following:

- No write permission for the Library/CEL.
- No disk space is available.

WHAT NEXT

Please check that the Milkyway design library and CEL are writeable and that there is sufficient disk space available.

ZRT-004 (error) Number of routing layers has to be greater than 1.

DESCRIPTION

The design only has one routing layer and the router can only route design with two or more routing layers.

WHAT NEXT

Please add more routing layer to the design.

ZRT-005 (error) Unable to support design with more than %d routing layers.

DESCRIPTION

The router currently only supports maximum of 15 routing layers.

WHAT NEXT

Please reduce the number of routing layers.

ZRT-006 (warn) Both adjacent cut rule and enclosed cut rule are specified, supporting only enclosed cut rule.

DESCRIPTION

Enclosed cut rule is a super set of adjacent cut rule which is an older rule the router supports for backward compatibility. So if both rules are specified, only enclosed cut rule is honored.

WHAT NEXT

Please remove adjacent cut rule and use enclosed cut rule to specify adjacent cut rule.

ZRT-007 (warn) Ignore fat rule on layer %s.

DESCRIPTION

The reason for receiving this warning could be one of the following:

- Fat threshold table is not in ascending order.
- Fat spacing table is not symmetric.

WHAT NEXT

Please check the technology file and make sure the fat rule is specified correctly.

ZRT-008 (warn) Ignore protrusion rule on layer %s.

DESCRIPTION

The reason for receiving this warning could be one of the following:

• Protrusion threshold table is not in ascending order.

WHAT NEXT

Please check the technology file and make sure the protrusion rule is specified correctly.

ZRT-009 (warn) Ignore %s rule on layer %s.

DESCRIPTION

This warning is issued because the spacing for this rule is not specified in increasing order.

WHAT NEXT

Please check the technology file and make sure the rule is defined correctly.

ZRT-010 (warning) Cannot find a fat contact for layer '%s'.

DESCRIPTION

This error message indicates that a suitable fat contact cannot be found for the given layer. This is most likely due to missing fat contact definition in the technology, and it will restrict the router's ability to resolve fat contact violations.

WHAT NEXT

Please check that the Milkyway technology file and add fat contact definition.

ZRT-011 (warning) Found more than one fat contacts for layer '%s'.

DESCRIPTION

This warning message indicates that more than one fat contact was found for the

given layer. This is most likely due to multiple fat contact definitions in the technology. The router will arbitrarily use one of the fat contacts to fix fat contact violations.

WHAT NEXT

Please check that the Milkyway technology file and remove duplicate fat contact definitions.

ZRT-012 (error) illegal fat contact '%s' for layer '%s'.

DESCRIPTION

This error message indicates that an illegal fat contact rule was found in the technology file. This will restrict the router's ability to fix fat contact violations.

WHAT NEXT

Please check that the Milkyway technology file and fix the fat contact specification.

ZRT-013 (error) illegal extension fat contact '%s' for layer '%s'.

DESCRIPTION

This error message indicates that an illegal extension fat contact rule was found in the technology file. This will restrict the router's ability to fix extension fat contact violations.

WHAT NEXT

Please check that the Milkyway technology file and fix the extension fat contact specification.

ZRT-014 (warn) Ignore stub spacing definition on layer %s.

DESCRIPTION

The reason for this warning message is most likely because the stub spacing value is less or equal to 0

WHAT NEXT

Please check the technology file and make sure the stub spacing is defined correctly.

ZRT-015 (warn) Ignore contact %s.

DESCRIPTION

The reason for receiving this warning could be one of the following:

- Lower, upper, or cut layer of the contact is not a valid routing layer.
- The contact has the same lower and upper layer.

WHAT NEXT

Please check the technology file and make sure the contact is defined correctly.

ZRT-016 (warn) Inconsistent %s design rule found between %s and %s.

DESCRIPTION

This warning message indicates that inconsistent design rule values are found. This is most likely due to the design rule being defined multiple times with the same two layers but with different values. Only the first definition read by the router is honored.

WHAT NEXT

Please check the technology file and make sure the design rule is only defined once for the same two layers.

ZRT-017 (warn) No diode ratio set for %s, turning off antenna

rule mode %d.

DESCRIPTION

When an antenna rule of diode mode 5 or greater is defined, diode ratio also needs to be specified for every routing layer. In this case, one or more layers are found without diode ratio and so the antenna rule is ignored.

WHAT NEXT

Please use define_antenna_layer_rule to specify diode ratio for every routing layer.

ZRT-018 (warn) No scale factor set for %s, turning off antenna rule mode %d.

DESCRIPTION

When an antenna rule of diode mode 11 or 12 is defined, scale factor also needs to be specified for every routing layer. In this case, one or more layers are found without scale factor and so the antenna rule is ignored.

WHAT NEXT

Please use define_antenna_layer_rule to specify scale factor for every routing layer.

ZRT-019 (warn) Illegal min/max layer constraint on net %s.

DESCRIPTION

This warning occurs when the min layer constraint is on a higher layer than the max layer constraint. This constraint is ignored for the net.

WHAT NEXT

Please use set_net_routing_layer_constraints to redefine the min/max layer constraint or use remove_net_routing_layer_constraints to remove the constraint on the net.

ZRT-020 (warn) Illegal cell min/max layer constraint.

DESCRIPTION

This warning occurs when the min layer constraint is on a higher layer than the max layer constraint. This cell constraint is ignored.

WHAT NEXT

Please redefine or reset this cell layer constraint.

ZRT-021 (info) Multiple default contact %s found for layer %s.

DESCRIPTION

This message indicates that more than one default contact was found for the given layer. This is most likely due to multiple default contact definitions in the technology. The router will arbitrarily use one of the default contacts depending on the available routing resource.

WHAT NEXT

No action necessary unless allowing multiple default contacts is not the correct intention. In that case, please remove duplicate default contact definition from the technology file.

ZRT-022 (warn) Cannot find a default contact for layer %s.

DESCRIPTION

This warning message indicates that no default contact was found for the given layer. This is most likely due to missing default contact definition in the technology.

WHAT NEXT

Please add default contact definition to the technology file.

ZRT-023 (warn) BPV on %d macros were done with "treat

blockage as thin".

DESCRIPTION

"Treat blockage as thin" flag was on during the BPV process and thus blockages inside these macros will be treated as thin by the router.

WHAT NEXT

If treating the blockages as thin is not the desired behavior, please re-run extract_blockage_pin_via.

ZRT-024 (error) %s has no corresponding % layer.

DESCRIPTION

The given layer does not have a corresponding wire/via layer. This limits the router’s ability to move from one layer to another.

WHAT NEXT

Please define the corresponding wire/via layer in the technology file.

ZRT-025 (warn) Layer %s does not have a preferred direction, assigning to %s.

DESCRIPTION

This message indicates that the layer does not have a preferred direction assigned to it. If the adjacent layer has a preferred direction, the opposite direction is set for the layer. Otherwise, metal 1 is assigned to horizontal, metal 2 to vertical, and so forth.

WHAT NEXT

Please use set_preferred_routing_direction to assign preferred direction.

ZRT-026 (warn) Layer %s pitch %.3f may be too small: wire/via-

down %.3f, wire/via-up %.3f.

DESCRIPTION

The pitch defined for the layer may be too small due to a larger up via and/or down via requirement. The router will use the larger spacing when placing those via.

WHAT NEXT

This is only a warning message.

ZRT-027 (warn) Ignore %d top cell ports with no pins.

DESCRIPTION

This warning message indicates that the design’s top cell has logical ports which have no physical shapes attached to them. The router will ignore such ports.

WHAT NEXT

Please check the top cell and create physical shapes for those ports if needed.

ZRT-028 (error) Failed to open child cell %s.%s.

DESCRIPTION

This warning message indicates that the router was not able to open the child cell for read. This could be because the reference library where the child cell resides does not have read permission or is missing.

WHAT NEXT

Please make sure the reference library is linked and readable to the current design.

ZRT-029 (error) Cell %s has inconsistent number of logical ports

in the library and in the top cell.

DESCRIPTION

This warning message indicates that the counts for the logical ports are different between the child library cell’s record and the top cell’s record. This could happen if the library cell got modified after the top cell was created.

WHAT NEXT

Please check and update the design hierarchy.

ZRT-030 (warn) Ignore pin (cell %s, port %s) on layer %d.

DESCRIPTION

This warning message occurs because physical pin shape on non-routing layer was found. The router will ignore such pin.

WHAT NEXT

Please check to see if the pin shape is on the correct layer.

ZRT-031 (warn) Invalid routing layer ’%s’ on wire

DESCRIPTION

This warning message indicates that a wire from the database is on an invalid routing later. The wire will be ignored by the router.

WHAT NEXT

Please check the database and fix the wire to be on valid routing layer.

ZRT-032 (warn) Invalid routing layer ’%s’ on path

DESCRIPTION

This warning message indicates that a path from the database is on an invalid routing later. The path will be ignored by the router.

WHAT NEXT

Please check the database and fix the path to be on valid routing layer.

ZRT-033 (warn) Invalid contact array %d.

DESCRIPTION

This warning message indicates that an invalid contact array is in the database. The router was unable to find a master via corresponding to the specified contact code from database.

WHAT NEXT

Please check the database and specify the correct contact code for the contact array

ZRT-034 (warn) Invalid contact %d.

DESCRIPTION

This warning message indicates that an invalid contact is in the database. The router was unable to find a master via corresponding to the specified contact code from database.

WHAT NEXT

Please check the database and specify the correct contact code for the contact.

ZRT-035 (warn) Invalid routing layer ’%s’ on global route

DESCRIPTION

This warning message indicates that a global route from database in on an invalid routing layer. The router will ignore the global route.

WHAT NEXT

Please check the database and fix the global route to be on valid routing layer.

ZRT-036 (warn) Ignore polygon pin (cell %s, port %s) on layer %d.

DESCRIPTION

This warning message occurs because polygon pin shape was found. The router currently does not handle polygon pin and thus this pin will be ignored.

WHAT NEXT

Please modify the polygon into rectangles.

ZRT-037 (warn) Ignore polygon via-region in cell %s.

DESCRIPTION

This warning message occurs because polygon via-region was found. The router currently does not handle polygon via-region and thus this via region will be ignored.

WHAT NEXT

Please re-run extract_blockage_pin_via.

ZRT-038 (warn) Cannot find contact %d for via-region in cell %s.

DESCRIPTION

This warning message indicates that contact cannot be found for the contact code stored with the via-region. This via-region will be ignored by the router.

WHAT NEXT

Please use a correct contact code for the via-region and re-run extract_blockage_pin_via.

ZRT-039 (warn) Contact %s for via-region in cell %s cannot be

rotated.

DESCRIPTION

This warning message indicates that non-rotatable contact was found for a rotated via-region. The via-region is ignored in this case.

WHAT NEXT

Please re-run extract_blockage_pin_via.

ZRT-040 (warn) Cell %s's boundary has exceeded the limit.

DESCRIPTION

This warning message occurs because the cell boundary size is larger than the system's limit. The cell boundary has been adjusted to fit the limit.

WHAT NEXT

Please re-size the cell boundary to be smaller.

ZRT-041 (error) Cannot find port %s in cell %s.

DESCRIPTION

This warning message occurs when master port cannot be found during the instance port processing. This could happen if the library cell got modified after the top cell was created and the hierarchical information is out of date.

WHAT NEXT

Please check and update the design hierarchy.

ZRT-042 (warn) Contact %s's %s layer enclosure %s does not

satisfy end of line enclosure design rule.

DESCRIPTION

The router depends on correct construction of contacts to avoid the end of line enclosure rule. In this case, the contact’s metal enclosure does not satisfy the requirement and there may be end of line enclosure design rule violation at the end of routing stage.

WHAT NEXT

Please modify the contact to satisfy the end of line enclosure requirement or remove the design rule from the technology file.

ZRT-043 (warn) Found must join pins on port %s without any net.

DESCRIPTION

Must join pins without net information were found. The router won’t be able to connect them unless net is assigned to them.

WHAT NEXT

Please create net for those pins.

ZRT-044 (warn) Standard cell pin %s/%s has no via regions.

DESCRIPTION

Via regions are useful in avoiding DRCs in accessing pins and in accessing pins off the routing grid.

WHAT NEXT

Please check for DRCs in accessing this pin and generate the via regions if necessary.

ZRT-045 (warn) Via regions for port %s/%s may block other

ports completely.

DESCRIPTION

Via regions are useful in avoiding DRCs in accessing pins and in accessing pins off the routing grid.

WHAT NEXT

Please check for DRCs in accessing this pin and generate the via regions if necessary.

ZRT-046 (warn) Conflicting voltage-areas for instance %s.

DESCRIPTION

This warning message indicates that the instance belongs to two conflicting voltage-areas. In the case of a conflict, the voltage-area of the smallest enclosing instance will take precedence. The reasons for this could be one of the following.

• The leaf-level instance has been assigned a voltage-area that conflicts with the enclosing hierarchical voltage-area.

WHAT NEXT

Please make sure that each instance belongs to only one voltage-area.

ZRT-047 (error) Ignoring voltage-area %s because maximum number of voltage-areas allowed is %d.

DESCRIPTION

This error message indicates that the number of voltage-areas in this design exceeds the maximum allowed. The reasons for this could be one of the following.

• Too many voltage-areas are being used in this design.

WHAT NEXT

Please make sure that the number of voltage-areas is within the limit.

ZRT-048 (error) Failed to write cel %s.

DESCRIPTION

Failed to save back to the database.

WHAT NEXT

Check preceding error messages for specific failure reasons.

ZRT-049 (error) Failed to load cel %s.

DESCRIPTION

Failed to read design from the database.

WHAT NEXT

Check preceding error messages for specific failure reasons.

ZRT-050 (warn) Invalid rotated polygon in master cell '%s'

DESCRIPTION

This warning message indicates that a rotated polygon in the master cell has invalid dimensions. This rotated polygon will be ignored by the router.

WHAT NEXT

Please check the database and fix the rotated polygon dimensions.

ZRT-051 (warn) Illegal Jog wire end of line rule (%s, %s).

DESCRIPTION

This warning message indicates that end of line rule is specified between two inconsistent layers.

WHAT NEXT

Please check the technology file and make sure the end of line rule is specified between a cut and metal layer.

ZRT-052 (warn) Illegal Jog wire end of line rule (%s, %s), (%d %d).

DESCRIPTION

This warning message indicates that end of line rule is specified between two inconsistent layers.

WHAT NEXT

Please check the technology file and make sure the end of line rule is specified between adjacent cut and metal layer.

ZRT-053 (warn) Illegal Special end of line enclosure rule (%s, %s).

DESCRIPTION

This warning message indicates that end of line rule is specified between two inconsistent layers.

WHAT NEXT

Please check the technology file and make sure the end of line rule is specified between a cut and metal layer.

ZRT-054 (warn) Illegal Special end of line enclosure rule (%s,

%s), (%d %d).

DESCRIPTION

This warning message indicates that end of line rule is specified between two inconsistent layers.

WHAT NEXT

Please check the technology file and make sure the end of line rule is specified between adjacent cut and metal layer.

ZRT-055 (warn) Illegal T-shape end of line enclosure rule (%s, %s).

DESCRIPTION

This warning message indicates that end of line rule is specified between two inconsistent layers.

WHAT NEXT

Please check the technology file and make sure the end of line rule is specified between a cut and metal layer.

ZRT-056 (warn) Illegal T-shape end of line enclosure rule (%s, %s), (%d %d).

DESCRIPTION

This warning message indicates that end of line rule is specified between two inconsistent layers.

WHAT NEXT

Please check the technology file and make sure the end of line rule is specified between adjacent cut and metal layer.

ZRT-057 (warn) Illegal Jog wire off limits rule (%s, %s).

DESCRIPTION

This warning message indicates that end of line rule is specified between two inconsistent layers.

WHAT NEXT

Please check the technology file and make sure the end of line rule is specified between a cut and metal layer.

ZRT-058 (warn) Illegal Jog wire off limits rule (%s, %s), (%d %d).

DESCRIPTION

This warning message indicates that end of line rule is specified between two inconsistent layers.

WHAT NEXT

Please check the technology file and make sure the end of line rule is specified between adjacent cut and metal layer.

ZRT-059 (warn) Illegal Fat wire off limits rule (%s, %s).

DESCRIPTION

This warning message indicates that end of line rule is specified between two inconsistent layers.

WHAT NEXT

Please check the technology file and make sure the end of line rule is specified between a cut and metal layer.

ZRT-060 (warn) Illegal Fat wire off limits rule (%s, %s), (%d %d).

DESCRIPTION

This warning message indicates that end of line rule is specified between two inconsistent layers.

WHAT NEXT

Please check the technology file and make sure the end of line rule is specified between adjacent cut and metal layer.

ZRT-061 (warn) Port %s (cell %s) of net %s has no pin.

DESCRIPTION

This warning message indicates that the port has no physical shape attached to it. The router will ignore such port and the net will be left open at the end of the routing stage.

WHAT NEXT

Please check the cell and create pin shape for the port.

ZRT-062 (warn) Value %s is not one among the predefined values for option %s. Assigning the default value.

DESCRIPTION

This warning message indicates that the value specified for the string token option is not among the list of predefined values. This can happen if the set of predefined values change and an old value which no longer exists is read from a saved cell. In this case, the option is assigned the default value.

WHAT NEXT

Please set the right value for the option, if the default value is not correct.

ZRT-063 (warn) Cover cell ’%s’ contains a non PG port ’%s’.

Ignoring it.

DESCRIPTION

This warning message indicates that the cover cell contains a port which is connected to non PG net. This is not handled currently based on our methodology.

WHAT NEXT

Please make sure that the cover cell does not contain non PG port.

ZRT-064 (error) Cell %s is not placed.

DESCRIPTION

This error message indicates that the cell has not been legally placed and it will be ignored by the router.

WHAT NEXT

Please make sure all the cells are placed before running the router.

ZRT-065 (warn) Ignore net %s's connection to port %s (cell %s).

DESCRIPTION

This warning message indicates that the port will be ignored by the router, and the reason is most likely due to some data error with the cell.

WHAT NEXT

Please check the port's cell and fix any problem associated with it.

ZRT-066 (error) Net %s not found.

DESCRIPTION

Failed to find the net in the current design.

WHAT NEXT

Check the spelling of the net name. Make sure net of that name exists.

ZRT-067 (error) Net %s is not a power/ground net.

DESCRIPTION

Found net is not a power/ground net.

WHAT NEXT

Make sure net is a power or a ground net.

SEE ALSO

connect_pg_nets(2)

ZRT-068 (error) Ground net not found.

DESCRIPTION

Failed to find the ground net in the current design.

WHAT NEXT

Add a ground net to the current design.

SEE ALSO

connect_pg_nets(2)

ZRT-069 (error) Too many ground nets, please specify one.

DESCRIPTION

This command found more than one ground net in the current design.

WHAT NEXT

Specify a ground net as an argument to a command.

ZRT-070 (error) Could not find any nets in the design that match the specification.

DESCRIPTION

The command expects the list of nets to be specified. Either the specification is incorrect, or there are no nets in the design that match the specification.

WHAT NEXT

Please check to make sure that the syntax for specifying the nets is correct.

ZRT-071 (error) Could not set a zroute option.

DESCRIPTION

The tool was not able to set a zroute option. This is caused by a bug in the tool.

WHAT NEXT

Please file a star.

ZRT-072 (error) Top cell not open.

DESCRIPTION

The top cell is not open.

WHAT NEXT

Open the top cell to run the current command.

ZRT-073 (error) The -from_file option specifies: %s but that file is not found .

DESCRIPTION

This warning message occurs because route_zrt_group cannot find a file by the name specified.

WHAT NEXT

Please ensure that the file exits and has been generated correctly.

ZRT-074 (error) The file: %s does not contain any valid net names.

DESCRIPTION

This warning message occurs because route_zrt_group cannot find any valid net names in the file specified by the -from_file option.

WHAT NEXT

Please ensure that the file was generated correctly and contains some valid net names.

ZRT-075 (warn) The the file: %s specifies a net: %s which does not exist.

DESCRIPTION

This warning message occurs because the -from_file option for the route_zrt_group command has encountered a putative net name which does not specify a net.

WHAT NEXT

Please ensure that the file was generated correctly and contains some valid net names.

ZRT-076 (warn) Invalid contact array pitch (contact code %d) (location %d %d).

DESCRIPTION

The contact array at the specified location has pitch smaller than the pitch required by the router. The router will continue, using the larger pitch. DRC’s reported against the via arrays will be conservative.

WHAT NEXT

Please check the database and verify that contact array pitch is even multiple of min grid.

ZRT-077 (warn) %s has different horizontal and vertical net weight.

DESCRIPTION

The net has different horizontal weight and vertical weight specified. The router currently only supports one net criticality value per net, and the larger of the two values will be used. This message is only printed once for the first net found with the issue.

WHAT NEXT

Please check the setup for the net and make sure it is correct.

ZRT-078 (warn) Illegal enclosed via metal minLength rule (%s, %s).

DESCRIPTION

This warning message indicates that enclosed via metal minLength rule is defined between inconsisten layers. It should be defined between a cut layer and the metal layer just above it.

WHAT NEXT

Please check the technology file and make sure the enclosed via metal minLength rule is specified between a cut layer and metal layer.

ZRT-079 (warn) Illegal enclosed via metal minLength rule (%s, %s), (%d %d).

DESCRIPTION

This warning message indicates that enclosed via metal minLength rule is defined between inconsisten layers. It should be defined between a cut layer and the metal

layer just above it.

WHAT NEXT

Please check the technology file and make sure the enclosed via metal minLength rule is specified between a cut layer and the metal layer jus above it.

ZRT-080 (error) Layer %s has no routing tracks.

DESCRIPTION

The given layer does not have any routing tracks. This prevents the router from assigning wires and vias on the layer.

WHAT NEXT

Please check if the routing tracks have been correctly defined on the layer. If the intent is to have the router automatically generate routing tracks then please make sure that the value of the zroute common option "-track_auto_fill" is set to true (the default value).

ZRT-081 (warn) NDR width is smaller than default width (%s, %s).

DESCRIPTION

This warning message indicates that the NDR width defined on one routing layer is smaller than the default width of the same layer.

WHAT NEXT

Please check the NDR rule definition in tcl command to make sure that the NDR width is no less than the default width on each routing layer.

ZRT-082 (warn) Turning off legal width checking on layer %s as the rule is not specified correctly.

DESCRIPTION

The number of legal widths specified cannot exceed 16. They must be in increasing

order and must contain the default width on the layer.

WHAT NEXT

Please check the technology file and make sure the legal width rules are correctly specified.

ZRT-083 (warn) Contact %s's %s layer enclosure does not satisfy legal width requirement.

DESCRIPTION

The router depends on correct construction of contacts that satisfy the legal width rule. In this case, the contact's metal enclosure does not satisfy the legal width requirement and it may result in long routing run time.

WHAT NEXT

Please modify the contact to satisfy the legal width requirement or remove the design rule from the technology file.

ZRT-084 (warn) Turning off viaOnGrid rule checking on cut layer %s as the lower and the upper routing layers have the same preferred direction, and viaOnGrid rule is not well-defined.

DESCRIPTION

If the upper and the lower routing layers of a cut layer have the same preferred direction, then the following conditions have to be satisfied in order to correctly check viaOnGrid rule on the cut layer.

• All routing tracks on both layers must be completely aligned.

• There must be a perpendicular direction layer, only one side of either below the lower layer or above the upper layer.

WHAT NEXT

Please check the technology file and make sure the viaOnGrid rule and routing tracks on adjacent layers are correctly specified.

ZRT-085 (error) Cannot run timing based detail route command with the timing driven option set to false.

DESCRIPTION

This error indicates that a timing based detail route command is being run without turning on the detail route timing driven option.

WHAT NEXT

Please set the detail route timing driven option to true before running the command (set_route_zrt_detail_options -timing_driven true).

ZRT-086 (warn) NDR via surround is smaller than the NDR width defined on the metal layer (%s, %s, %s). "NDR width or contact code mismatch" DRCs will be flagged on those vias.

DESCRIPTION

This warning message indicates that the width of a NDR via surround on one metal layer is smaller than the NDR width defined on the same layer. The users may see "NDR width or contact code mismatch" DRCs flagged on the NDR via surround if it is not covered by sufficiently wide wires.

WHAT NEXT

It is expected to see "NDR width or contact code mismatch" DRCs flagged on these via surrounds in this case.

ZRT-087 (warn) The design contains a huge X-oriented obstruction.

DESCRIPTION

This warning message indicates that the current design contains an unusually large X-oriented (45 or 135 degree) obstruction. Large X-oriented obstructions may cause inefficiency in the router and result in slow runtime.

WHAT NEXT

Check the design to see if the large X-oriented obstruction is indeed intended. The user may need to break it into smaller ones if possible.

ZRT-088 (error) NDR rule %s has illegal widths on layer %s.

DESCRIPTION

This error message indicates that either the wire width, shield width or the via width on the metal layer is illegal or larger than the signal route max width defined on that layer. Zroute will ignore this NDR rule on the associated nets in the design.

WHAT NEXT

Please make sure that the NDR rule widths are legal and are less than or equal to the signal route max width defined in the tech file.

ZRT-089 (warn) Value %s for layer %s is very big.

DESCRIPTION

This warning is issued because the value for a spacing is very big. Check if it is intentional.

WHAT NEXT

If the large value was set by accident, correct it and rerun the routing command.

ZRT-100 (warning) Pin %s of net %s has no valid shapes to connect.

DESCRIPTION

This message indicates that pin has no shapes inside design boundary.

WHAT NEXT

Please make sure that the pin has valid shapes to connect.

ZRT-101 (warning) Power net %s has no power preroutes, skip tie-off.

DESCRIPTION

Power net has no power preroutes. Tie-off will be turned off for this net.

WHAT NEXT

Please add power preroutes.

ZRT-102 (info) %d of the existing global routes are deleted.

DESCRIPTION

All existing global routes are deleted at the beginning of global routing stage, unless incremental option is set to true. In route_zrt_group flow, only nets not specified in the net group will be deleted if incremental option is true.

WHAT NEXT

No action necessary.

ZRT-103 (info) Global Routing terminated early: %s

DESCRIPTION

Global routing terminated early because either the congestion has been minimized or it does not seem like the congestion can be improved further.

WHAT NEXT

No action necessary.

ZRT-200 (error) Skipping track assignment because this design

has no global routes.

DESCRIPTION

This message indicates that there are no global routes in this design, so the router cannot perform track assignment. This happens because either global routing is not correctly finished, or track assignment is already done.

WHAT NEXT

First check whether track assignment was already completed. Then check whether global routing was completed before running track assignment.

ZRT-300 (warn) Antenna diodes cannot protect any pin.

DESCRIPTION

Under certain antenna calculation modes, diode cells do not offer any protection to violating pins.

WHAT NEXT

Please check the antenna calculation mode. If diode cells are desired, set the antenna diode calculation mode appropriately.

ZRT-301 (warn) Antenna diode insertion will be off.

DESCRIPTION

Antenna diode insertion is set on by the input options, but will be off in this run because diode insertion could not be initialized.

WHAT NEXT

Please preceding warnings for specific problems in initializing diode insertion.

ZRT-302 (warn) No antenna diodes found, or could not link

them.

DESCRIPTION

Antenna diode insertion is set on by the input options, but no diode cells were found in the linked library.

WHAT NEXT

Check the library to find diode cells.

ZRT-303 (warn) Failed to initialize legalizer for antenna diode insertion.

DESCRIPTION

Antenna diode insertion is set on by the input options, but the router could not initialize the legalizer for diode insertion.

WHAT NEXT

Check the preceding messages from the legalizer for specific problems.

ZRT-304 (info) Skip final DRC merging, too many DRCs.

DESCRIPTION

DRC merging reduces redundant DRCs by merging aligned and coincident DRCs. However, DRC merging is skipped if there are too many DRCs, as it might take too log.

WHAT NEXT

No action necessary.

ZRT-305 (info) Merged away %d aligned/redundant DRCs.

DESCRIPTION

DRCs can be merged if at least two opposing edges are aligned and they are of the

same type, layer, and nets. For example, if two overlapping different-net-metal-spacing DRCs are between shapes of the same layer, from the same two nets, and have top and bottom edges aligned, then they will be merged to one DRC. Merging is done to give the user a more realistic number of DRCs, and to minimize the effect of the router's internal representation of the shapes on the DRC count.

WHAT NEXT

No action necessary.

ZRT-306 (info) Discarded %d drcs of internal-only type.

DESCRIPTION

DRCs of internal-only type are not violations of technology rules and may be discarded.

WHAT NEXT

No action necessary.

ZRT-307 (info) Skip DR iteration %d for new DRC type to start.

DESCRIPTION

Some DRC analysis may be deferred until later global iterations. In that case, the router may skip iterations while the number of DRCs is zero, until all DRC analysis is on.

WHAT NEXT

No action necessary.

ZRT-308 (error) Design has global route wires. Please run track assignment before detailed route.

DESCRIPTION

Track assignment is required before detailed routing.

WHAT NEXT

Run track assignment.

ZRT-309 (warn) No antenna rules defined, Skip antenna analysis.

DESCRIPTION

Antenna rules must be defined in the library in order to do antenna analysis.

WHAT NEXT

Define antenna rules in the library.

ZRT-310 (error) Failed to store hierarchical antenna property.

DESCRIPTION

Attempt to store hierarchical antenna property in top level pins failed.

WHAT NEXT

It is a bug.Please report it.

ZRT-311 (warning) Skipping antenna analysis for net %s. The pin %s on cell %s does not enough gate area information.

DESCRIPTION

One or more input pins of this net do not have the correct gate area values. So antenna analysis will not be done for this net.

WHAT NEXT

Check and set correct gate area for all the input pins of the net and also for all the metal & cut layers.

ZRT-312 (info) Detail Routing terminated early because DRCs were not converging: %s

DESCRIPTION

Detail Routing terminated early because DRCs were not converging.

WHAT NEXT

No action necessary.

ZRT-400 (error) Cannot open timing file '%s'.

DESCRIPTION

The reasons for this could be one of the following.

- The file does not exist.
- You do not have the required permissions to read it.

WHAT NEXT

Please make sure the timing file exists and that you have the required permissions to read it.

ZRT-401 (error) Corrupted or incomplete timing file.

DESCRIPTION

The reasons for this could be one of the following.

- There was not enough disk space when the timing file was saved.

• The timing file was saved using a different executable from the one that is being used to read it.

WHAT NEXT

Please re-run after making sure that there is enough disk space available.

ZRT-402 (error) Cannot find the user specified timing file '%s'.

DESCRIPTION

The reasons for this could be one of the following.

• The file does not exist or the full path to the file was not specified.

• You do not have the required permissions to read it.

WHAT NEXT

Please make sure the full path to the file is specified and that you have the required permissions to read it.

ZRT-403 (warn) Hidden %s parameter %s of %s is obsolete in Zroute.

DESCRIPTION

This debug/hidden parameter has been set or has a different value than the default value, but the parameter to option translator does not support translation of this parameter.

WHAT NEXT

If possible, please remove this parameter from the script or reset the value if it's coming from the cell parameter setting.

ZRT-404 (warn) Unable to translate %s of %s because %s -%s

does not support value %d.

DESCRIPTION

The parameter is set to a value that is not supported by the option and thus can not be translated.

WHAT NEXT

Please do not use the unsupported value with the parameter.

ZRT-405 (warn) Unable to translate %s -%s because %s of %s does not support mode %s.

DESCRIPTION

The option is set to an additional mode that is not supported by the parameter and thus can not be translated.

WHAT NEXT

Please do not set the option to this mode if the translation of this option to parameter is required.

ZRT-406 (warn) Unable to translate %s to %s because %s.

DESCRIPTION

The translator cannot perform the translation because there is no exact correspondence between the option and the parameter.

WHAT NEXT

Please review the setting of the option or the parameter.

ZRT-407 (error) Failed in separate process.

DESCRIPTION

This error message indicates that the command failed in the separate process. The reasons for this could be one of the following.

- Crash in separate process flow.
- No disk space is available.

WHAT NEXT

Please check that there is sufficient disk space available. If disk space is not the issue, please contact customer service. This is a bug.

ZRT-408 (error) Using -nets option without -antenna, -open_net, or -voltage_area.

DESCRIPTION

This error message indicates that the command verify_zrt_route failed. The option "-nets" is specified without any accompanying options. The reason could be one of the following:

- Check open nets option is not specified.
- Check antennas is not specified.
- Check voltage areas is not specified.

WHAT NEXT

1) Specify one or more of these three options in this Tcl command. or 2) Remove the "-nets" option and rerun the command.

ZRT-409 (warn) %s parameter %s is not supported by Zroute.

DESCRIPTION

The translator cannot perform the translation because the parameter is currently not supported by Zroute.

WHAT NEXT

Please review the setting of the parameter.

ZRT-410 (info) %s parameter %s is obsolete in Zroute.

DESCRIPTION

The translator cannot perform the translation because the parameter is obsolete in Zroute. Most likely Zroute is already handling the parameter automatically and there is no need for an user option, or the parameter is useless in Zroute.

WHAT NEXT

ZRT-411 (warn) %s parameter %s is supported by Zroute only in MW technology file.

DESCRIPTION

The parameter is not supported as an option in Zroute and needs to be defined in Milkyway technology file.

WHAT NEXT

Please define the design rule criteria in the technology file.

ZRT-412 (warn) %s parameter %s cannot be translated exactly to corresponding Zroute option.

DESCRIPTION

Zroute has a similar option, but the approach it takes is different and does not

match the parameter with one to one correspondence.

WHAT NEXT

Please set the option manually and refer to the application notes for more details.

ZRT-413 (error) Invalid coordinates for area routing.

DESCRIPTION

The router cannot perform area routing because the specified coordinates are invalid.

WHAT NEXT

Please use the correct format to specify the coordinates.

ZRT-414 (error) Abnormal exit of child process

DESCRIPTION

Child process crashed.

WHAT NEXT

This is a bug.Please report it.

ZRT-415 (warn) The number of threads for this run is reduced to %d.

DESCRIPTION

Based on the maximum number of threads set,an attempt is made to checkout the required number of license keys of each type.However all the required keys are not available.Based on available number of keys of each type,a reduced number of threads is calculated and used for this run.

WHAT NEXT

Please check if license keys of each type are available for this run.

ZRT-416 (warning) %d %s cell PG pins connected to net NULL and not PG.

DESCRIPTION

This warning message indicates that the filler cell removal command detects PG pins of some cells in the design connected to NULL net. Short violations between the PG pins connected to NULL net and PG pins connected to valid PG nets will be detected during the command, and filler cells with such violations will be removed.

WHAT NEXT

Please run the connect_pg_nets command to ensure valid PG connecttions to PG pins.

ZRT-417 (warning) Deleted instance %s is not a standard filler cell

DESCRIPTION

This warning message indicates that the filler cell removal command detects a violation on a cell which name matches a given name pattern, but is not classified as a standard filler cell. Filler cells are standard cells without any connections to signal nets. Filler cells that were inserted with insert_stdcell_filler command have a prefix of "xofiller".

WHAT NEXT

Please check the given name pattern if it is indeed intended for filler cell deletion. You may use a default name pattern if only filler cells with a prefix of "xofiller" were intended for deletion.

ZRT-418 (warning) Instance %s which is connected to signal nets is not deleted.

DESCRIPTION

This warning message indicates that the filler cell removal command detects a violation on a cell which name matches a given name pattern, but has connections to signal nets. Such cells can not be removed.

WHAT NEXT

Please check the given name pattern if it is indeed intended for filler cell deletion.

ZRT-419 (warning) Cell %s has internal violations

DESCRIPTION

This warning message indicates that the filler cell removal command detects a cell which has violation on objects inside the cell. Such violation is ignored for cell removal purpose.

WHAT NEXT

Please check the filler library cell for violations.

ZRT-420 (error) It is not recommended to use classic router commands after Zroute commands.

DESCRIPTION

Routing was done with Zroute on the current design. Now an attempt is made to run commands of classic router. This is not recommended because the DRC analysis and routing graph interpretations are different between the two routers.

WHAT NEXT

Continue to run all the routing commands in Zroute. If the intention to use the classic router for the flow, delete all the existing routes and start the flow with classic router.

ZRT-421 (error) Cannot open file '%s' for '%s'.

DESCRIPTION

The file cannot be opened.

WHAT NEXT

Please make sure you have the required permissions on the directory.

ZRT-422 (warn) %s option "%s" will be obsolete in %s release. %s.

DESCRIPTION

The option specified will be obsoleted in future release.

WHAT NEXT

Please define the design rule in the technology file.

ZRT-423 (warn) %s parameter %s is supported by Zroute by command line option.

DESCRIPTION

The parameter is supported in Zroute as command line option.

WHAT NEXT

Please use command line option instead.

ZRT-424 (warning) max_number_of_threads option is deprecated

DESCRIPTION

The -max_number_of_threads option is being phased out, in favor of using the -max_cores option for the set_host_options command.

WHAT NEXT

Please update scripts to use ’set_host_options -max_cores’ instead of using ’set_route_zrt_common_options -max_number_of_threads’.

ZRT-425 (warning) The deprecated option ’set_route_zrt_common_options -

max_number_of_threads’specified a contradictory number of threads than what is specified using the recommended ’set_host_options -max_cores’ option. Both the recommended command ’set_host_options -max_cores %d’ and the deprecated ’set_route_zrt_common_options -max_number_of_threads %d’ have been specified. Zroute will use %d as the maximum number of threads.

DESCRIPTION

The -max_number_of_threads option is being phased out, in favor of using the -max_cores option for the set_host_options command.

WHAT NEXT

Please update scripts to use ’set_host_options -max_cores’ instead of using ’set_route_zrt_common_options -max_number_of_threads’.

ZRT-426 (error) This error message indicates that invalid route type is specified.

DESCRIPTION

The valid values for the route type are fixed_route and nonfixed_route.

WHAT NEXT

Check the command syntax from the man page and use the correct value.

ZRT-427 (warning) Net %s was modified, will be reshielded.

DESCRIPTION

The indicated shielded net was modified outside of Zroute environment. It will be automatically reshielded at the end of signal routing.

WHAT NEXT

This is just an informational message, and no action is required from the user.