Power Compiler™ Quick Reference

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SYNOPSYS®

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Getting Help

Power Compiler provides various forms of online help.

- The help command provides you with quick help for one or more commands or procedures.
- The man command displays the man page.

You can use a wildcard pattern as the argument for the help command. The wildcard characters are

*	Matches n characters.
?	Matches exactly one character.

Accessing Brief Help

Use this command to list all commands by function group:

```
dc_shell> help
```

Use this command to display all commands that end with the word clock:

```
dc_shell> help *clock
```

Use this command to get syntax help for one or more commands:

```
dc_shell> help -verbose cmd_name_pattern
```

Use this command to get syntax help for a specific command:

```
dc_shell> command_name -help
```

Man Page Viewing Instructions

The following sections describe how to set up your environment and the syntax to use to view man pages.

Setting Up the UNIX Environment

Edit your .cshrc file to contain these lines:

```
setenv SYN_MAN_DIR synopsys_root/doc/syn/man
setenv MANPATH ${MANPATH}:${SYN_MAN_DIR}
```

SYN_MAN_DIR is a variable that contains the path to the man page directories, and *synopsys_root* represents the specific path to the Synopsys software directory at your site.

Viewing Man Pages From UNIX

Command

```
% man command_name
```

Variable

```
% man variable_name
```

Error, warning, or information message

```
% man message_id
```

Viewing Man Pages From dc_shell

Command

```
dc_shell> man command_name
```

Variable

```
dc_shell> man variable_name
```

Error, warning, or information message

```
dc_shell> man message_id
```

Power Compiler Commands

Invoke these commands from within the Power Compiler tool.

all_clock_gates

Returns a collection of clock gating cells or pins in the current design.

```
collection all_clock_gates
[-no_hierarchy]
[-clock clock_name]
[-cells]
[-enable_pins]
[-clock_pins]
[-output_pins]
[-test_pins]
[-observation_pins]
```

apply_clock_gate_latency

Annotates the clock latencies on the existing clock gating cells based on the settings previously specified using the set_clock_gate_latency command.

```
status apply_clock_gate_latency
```

characterize

Captures information about the environment of specific cell instances, and assigns the information as attributes on the design to which the cells are linked.

```
int characterize
cell_list
[-no_timing] [-constraints]
[-connections] [-power]
[-verbose]
```

check_isolation_cells

Reports the existing isolation cells in the current design. It also reports if any isolation cell is redundant or might be required.

```
status check_isolation_cells
[-input]
[-output]
[-inside]
[-outside]
[objects]
```

check_level_shifters

Checks the design for all existing level shifters and nets against the specified level shifter strategy and threshold.

```
status check_level_shifters
[-verbose]
```

compile

Performs logic-level and gate-level synthesis and optimization on the current design.

```
status compile
[-no_map]
[-map_effort medium | high]
[-area_effort none | low | medium | high]
[-incremental_mapping]
[-exact_map]
[-ungroup_all]
[-boundary_optimization]
[-auto_ungroup area | delay]
[-no_design_rule | -only_design_rule |
-only_hold_time]
[-scan]
[-top]
[-power_effort none | low | medium | high]
[-gate_clock]
```

connect_power_domain

Connects power net information for the specified power domains. This command is supported only in non-UPF mode.

```
status connect_power_domain
power_domains
[-primary_power_net power_net]
[-primary_ground_net ground_net]
[-backup_power_net power_net]
[-backup_ground_net ground_net]
[-internal_power_net internal_power_net]
[-internal_ground_net internal_ground_net]
```

connect_power_net_info

Connects the specified power net information to the specified power pins. This command is supported only in non-UPF mode.

```
status connect_power_net_info
object_list
-power_pin_name power_pin_name
-power_net_name power_net_name
```

connect_supply_net

Connects the supply net to the specified supply ports and pins. This command is supported only in UPF mode.

```
status connect_supply_net
supply_net_name
-ports list
```

create_nominal_power_state

Creates a new power state according to the format of the current power state template. This command is supported only in non-UPF mode.

```
status create_nominal_power_state
voltage_list
[-name power_state_name]
```

create_power_domain

Creates a power domain, which provides a power supply distribution network.

Syntax for UPF Mode

```
status create_power_domain
domain_name
[-elements list]
[-include_scope]
[-scope instance_name]
```

Syntax for Non-UPF Mode

```
string create_power_domain
domain_name
[-power_down]
[-power_down_ctrl object_list]
[-power_down_ack object_list]
[-object_list object_list]
```

create_power_net_info

Creates a power net. This command is supported only in non-UPF mode.

```
status create_power_net_info
power_net_name
-power | -gnd
[-switchable]
[-nominal_voltages nominal_voltage_list]
[-voltage_ranges voltage_range_list]
```

create_power_switch

Creates a power switch at the specified power domain. This command is supported only in UPF mode.

```
string create_power_switch
switch_name
-domain domain_name
-output_supply_port {port_name
supply_net_name}
-input_supply_port {port_name
supply_net_name}
-control_port {port_name net_name}
[-ack_port {port_name net_name
[{boolean_function}]}]
[-ack_delay {port_name delay}]
-on_state {state_name input_supply_port
{boolean_function}}
[-off_state {state_name {boolean_function}}]
```

create_supply_net

Creates a supply net for the specified power domain. The supply net is created in the logic hierarchy at the same scope as the specified power domain. This command is supported only in UPF mode.

```
string create_supply_net
supply_net_name
-domain domain_name
[-reuse]
[-resolve unresolved | parallel]
```

create_supply_port

Creates a supply port in the specified power domain or in the current scope if no power domain is specified. This command is supported only in UPF mode.

```
string create_supply_port
supply_port_name
[-domain domain_name]
[-direction in | out]
```

disconnect_power_net_info

Removes the exceptional power net information hookups with the power pin.

```
status disconnect_power_net_info
object_list
-power_pin_name power_pin_name
```

get_power_domains

Creates a collection of power domains that meet the specified criteria.

UPF Mode:

```
collection get_power_domains
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[[patterns] [-hierarchical] | -of_objects
objects]
```

Non-UPF Mode:

```
collection get_power_domains
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[patterns | -of_objects objects]
```

get_power_switches

Creates a collection of power switches that meet the specified criteria. This command is supported only in UPF mode.

```
collection get_power_switches
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[patterns]
[-hierarchical]
```

get_supply_nets

Creates a collection of supply nets that meet the specified criteria. This command is supported only in UPF mode.

```
collection get_supply_nets
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[patterns]
[-hierarchical]
```

get_supply_ports

Creates a collection of supply ports that meet the specified criteria. This command is supported only in UPF mode.

```
collection get_supply_ports
[-filter expression]
[-quiet]
[-regexp [-nocase]]
[patterns]
[-hierarchical]
```

hookup_power_gating_ports

Connects the control pins of retention registers through the design hierarchy based on the specification. This command is supported only in non-UPF mode.

```
status hookup_power_gating_ports
[-type style]
[-default_port_naming_style naming_style]
[-port_naming_styles
list_of_port_naming_styles]
```

hookup_retention_register

Hooks up the save and restore pins of the retention registers to the save signal and the restore signal. This command is supported only in UPF mode.

```
status hookup_retention_register
```

identify_clock_gating

Identifies Power Compiler inserted clock-gating circuitry in a structural netlist.

```
integer identify_clock_gating
[-reset]
[-reset_only cell_or_pin_list]
[-gating_element gating_cell]
[-gated_element gated_cell_or_pin_list]
[-ungated_element ungated_cell_list]
```

infer_power_domains

Infers power domains from the $power specification. This command is supported only in non-UPF mode.

```
status infer_power_domains
[-verbose]
```

insert_clock_gating

Performs clock gating on an appropriately-prepared GTECH netlist.

```
status insert_clock_gating
[-regular_only]
[-global]
[-no_hier]
```

insert_isolation_cell

Inserts isolation cells on the specified nets, pins or ports. Isolation cell is a general term that applies to isolation (ISO) cells and enabled level-shifter (ELS) cells.

```
status insert_isolation_cell
[-force]
[-verbose]
-enable enable_signal
-object_list objects
-reference lib_cell_name
```

insert_level_shifters

Inserts appropriate level shifters in the current design.

```
status insert_level_shifters
[-preserve]
[-all_clock_nets]
[-clock_net clock_name]
[-verbose]
```

lib2saif

Creates a forward-annotation SAIF file for a specified technology library.

```
int lib2saif
[-output file_name]
library
[-lib_pathname lib_path_name]
```

map_isolation_cell

Specifies how to map or remap the isolations and enable level-shifter cells belonging to the specified isolation strategy. This command is supported only in UPF mode.

```
status map_isolation_cell
isolation_strategy
-domain power_domain
-lib_cells lib_cells
```

map_level_shifter_cell

Specifies that the level-shifter cells belonging to the specified strategy can only be mapped to a subset of the library cells. This command is supported only in UPF mode.

```
status map_level_shifter_cell
level_shifter_strategy
-domain power_domain
-lib_cells lib_cells
```

map_power_switch

Defines which power switch library cells to use for the mapping of the given UPF power switch. This command is supported only in UPF mode.

```
status map_power_switch
switch_name
-domain domain_name
-lib_cells name_list
```

map_retention_cell

Defines how to map the unmapped sequential cells to retention cells for the specified UPF retention strategy of the power domain. This command is supported only in UPF mode.

```
status map_retention_cell
retention_strategy
-domain power_domain
[-lib_cells lib_cells]
[-lib_cell_type lib_cell_type]
[-elements objects]
```

merge_saif

Reads a list of SAIF files with their corresponding weights, computes the merged toggle rate and static probability, and annotates the switching activity for nets, pins,and ports in the current design. The command then generates a merged output SAIF file.

```
integer merge_saif
-input_list saif_file_and_weight_list
-instance_name inst_name
[-output merged_saif_name]
[-simple_merge]
[-ignore ignore_name]
[-ignore_absolute ig_absolute_name]
[-exclude exclude_file_name]
[-exclude_absolute ex_absolute_file_name]
[-unit_base unit_value]
[-scale scale_value]
[-khrate khrate_value]
[-map_names]
[-rtl_direct]
[-strip_module annotated_instance_name]
```

propagate_constraints

Propagates timing constraints from lower levels of the design hierarchy to the current design.

```
status propagate_constraints
[-design design_list]
[-all]
[-clocks]
[-disable_timing]
[-dont_apply]
[-false_path]
[-gate_clock]
[-ideal_network]
[-ignore_from_or_to_port_exceptions]
[-ignore_through_port_exceptions]
[-max_delay]
[-min_delay]
[-multicycle_path]
[-operating_conditions]
[-power_supply_data]
[-output file_name]
[-port_isolation]
[-verbose]
[-case_analysis]
[-target_library_subset]
```

propagate_switching_activity

Forces a propagation of the power switching activity information.

```
int propagate_switching_activity
[-effort low | medium | high]
[-verbose]
[-infer_related_clocks]
```

read_saif

Reads a SAIF file and annotates switching activity information on nets, pins, ports, and cells in the current design.

```
status read_saif
-input file_name
-instance_name name
[-target_instance instance]
[-ignore ignore_name]
[-ignore_absolute ig_absolute_name]
[-exclude exclude_file_name]
[-exclude_absolute ex_absolute_file_name]
[-names_file name_changes_log_file]
[-scale scale_value]
[-unit_base unit_value]
[-khrate khrate_value]
[-map_names]
[-auto_map_names]
[-rtl_direct]
[-verbose]
```

remove_clock_gating

Directs the compile -incremental, and compile_ultra -incremental commands to remove clock gating from objects clock-gated by Power Compiler.

```
integer remove_clock_gating
[-gated_registers gated_register_list]
[-min_bitwidth minsize_value]
[-gating_cells clock_gating_cells_list]
[-all]
[-no_hier]
[-verbose]
[-undo]
```

remove_isolation_cell

Removes specified isolation cell or cells from design.

```
int remove_isolation_cell
[-force]
-object_list cells
```

remove_level_shifters

Removes all of the level shifters from the design.

```
integer remove_level_shifters
[-force]
```

remove_nominal_power_state

Removes a list of power states. This command is supported only in non-UPF mode.

```
status remove_nominal_power_state
[power_state_name_list]
```

remove_operand_isolation

Removes the isolation logic inserted by Power Compiler during the operand isolation step.

```
status remove_operand_isolation
[-from from_list]
[-to to_list]
```

remove_power_domain

Removes the specified power domains.

```
status remove_power_domain
domain_name | -all
```

remove_power_net_info

Deletes power net info. This command is supported only in non-UPF mode.

```
int remove_power_net_info
name
-all
```

replace_clock_gates

Replaces manually inserted clock gates with Power Compiler clock gates.

```
int replace_clock_gates
[-global]
[-no_hier]
```

report_clock_gating

Reports information about clock gating performed by Power Compiler.

```
status report_clock_gating
[-no_hier]
[-verbose]
[-gated]
[-ungated]
[-gating_elements]
[-only cell_list]
[-nosplit]
[-physical]
[-multi_stage]
[-style]
[-structure]
[-scenario scenario_list]
```

report_isolation_cell

Displays information about isolation cells in the current scope. This command is supported only in UPF mode.

```
status report_isolation_cell
[isolation_cells]
[-domain power_domains]
[-isolation_strategy
isolation_strategy_names]
[-ports pins_ports]
[-verbose]
[-nosplit]
```

report_level_shifter

Displays information about level shifter cells in the current scope. This command is supported only in UPF mode.

```
status report_level_shifter
[level_shifter_cells]
[-domain power_domains]
[-verbose]
[-nosplit]
```

report_lib

Displays information about technology, symbol libraries, or physical libraries.

```
int report_lib
[-all]
[-ccs_recv]
[-em]
[-fpga]
[-full_table]
[-k_factors]
[-power]
[-power_label]
[-routing_rule]
[-rwm]
[-table]
[-timing]
[-timing_arcs]
[-timing_label]
[-user_defined_data]
[-vhdl_name]
[-yield]
[-switch]
[-pg_pin]
[-char]
[-operating_condition]
[-op_cond_name op_cond_name]
[cell_list]
library_name
```

report_nominal_power_state_template

Reports the current power state template. This command is supported only in non-UPF mode.

```
integer report_nominal_power_state_template
```

report_operand_isolation

Reports the status of operand isolation cells in the current design.

```
status report_operand_isolation
[-instances]
[-isolated_objects]
[-unisolated_objects]
[-all_objects]
[-verbose]
[-no_hier]
[-nosplit]
[object_list]
```

report_power

Calculates and reports dynamic and static power for a design or instance.

```
int report_power
[-net]
[-cell]
[-only cell_or_net_list]
[-hier]
[-hier_level level_value]
[-verbose]
[-cumulative]
[-flat]
[-exclude_boundary_nets]
[-include_input_nets]
[-analysis_effort low | medium | high]
[-nworst number]
[-sort_mode mode]
[-histogram [-exclude_leq le_val
 | -exclude_geq ge_val]]
[-nosplit]
[-scenario scenario_list]
```

report_power_calculation

Displays the calculation of the internal power for a pin, the leakage power for a cell, or the switching power for a net.

```
int report_power_calculation
pin_cell_or_net_list
[-state_condition boolean_eq_of_pins |
default | all]
[-path_source pin_name | default | all]
[-rise]
[-fall]
[-verbose]
[-nosplit]
```

report_power_domain

Reports information about the specified power domain.

```
status report_power_domain
[power_domains]
```

report_power_gating

Reports the power gating style of retention registers in the design.

```
int report_power_gating
[cell_or_design_list]
[-missing]
[-unconnected]
```

report_power_net_info

Reports the power net information for the current design. This command is supported only in non-UPF mode.

```
integer report_power_net_info
```

report_power_pin_info

Reports the power pin information for technology library cells or leaf cells. In UPF mode, the command reports power pin information only for instantiated cells and not the library cells.

```
status report_power_pin_info
object_list
```

report_power_state_table

Reports the legal power states in the current design. This command is supported only in non-UPF mode.

```
integer report_power_state_table
[-power_nets power_net_list]
[-compress]
[-trace_name]
[-significant_digits digit]
[-width]
[-column_space column_space]
```

report_power_switch

Reports all of the specified power switches. This command is supported only in UPF mode.

```
status report_power_switch
[power_switch_name]
[-verbose]
```

report_retention_cell

Displays information about retention cells in the current scope. This command is supported only in UPF mode.

```
status report_retention_cell
[retention_cells]
[-domain power_domains]
[-retention_strategy
retention_strategy_names]
[-verbose]
```

report_saif

Reports statistics on the switching activity annotation on the current design or instance.

```
int report_saif
[-hier]
[-flat]
[-type rtl | gate]
[-rtl_saif]
[-missing]
[-only cell_or_net_list]
[-annotated_flag]
```

report_supply_net

Reports all the supply nets in the current scope. This command is supported only in UPF mode.

```
status report_supply_net
[supply_net_name]
[-include_exception]
```

report_supply_port

Reports information about the supply ports in the current scope. This command is supported only in UPF mode.

```
status report_supply_port
[supply_port_name]
```

reset_clock_gate_latency

Resets all clock latency values previously specified for or applied to clock gating cells.

```
int reset_clock_gate_latency
[-clock clock_list]
```

reset_nominal_power_state_template

Resets the current power state template. This command is supported only in non-UPF mode.

```
integer reset_nominal_power_state_template
```

reset_switching_activity

Removes the toggle rate and static probability attributes, or the maximum toggle rate attribute, from nets, pins, cells, and ports of the current design.

```
integer reset_switching_activity
-switching_activity | -max_toggle_rate |
-all
[-verbose]
[object_list]
```

rewire_clock_gating

Changes the clock-gating cell implemented by the tool for a particular gated cell.

```
status rewire_clock_gating
[-gating_cell new_clock_gating_cell]
[-gated_objects gated_objects_list]
[-balance_fanout]
[-undo]
[-verbose]
```

rtl2saif

Creates a SAIF forward-annotation file starting from the top level of the design.

The rtl2saif command will be obsolete in a future release as RTL forward SAIF is now obsolete.

```
int rtl2saif
[-output file_name]
[-design design_name]
```

saif_map

Manages the SAIF name mapping mechanism for reading SAIF files.

```
string saif_map
[-start]
[-end]
[-reset]
[-report]
[-get_name]
[-set_name names]
[-add_name names]
[-remove_name names]
[-clear_name]
[-get_object_names name]
[-create_map]
[-write_map filename]
[-read_map filename]
[-type type]
[-inverted]
[-instances objects]
[-hierarchical]
[-no_hierarchical]
[-columns columns]
[-sort columns]
[-rtl_summary]
[-missing_rtl]
[-input SAIF_file]
[-source_instance SAIF_instance_name]
[-target_instance target_instance_name]
[-review]
[-preview]
[-hsep character]
[object_list]
[-verbose]
[-non_verbose]
[-nosplit]
```

set_cell_internal_power

Sets or removes the power_value attribute on the specified pins. The value represents the power consumption for a single toggle of each pin.

```
int set_cell_internal_power
[-delete_all]
pin_list
[power_value [unit]]
```

set_clock_gate_latency

Specifies clock network latency values to be used for clock gating cells, as a function of clock domain, clock gating stage, and fanout.

```
status set_clock_gate_latency
[-clock clock_list]
[-overwrite]
-stage cg_stage
-fanout_latency cg_fanout_list
```

set_clock_gating_registers

Forces the enabling or disabling of clock gating for specified registers in the current design, overriding all conditions necessary for automatic RTL clock gating by the compile_ultra -gate_clock command.

```
status set_clock_gating_registers
[-include_instances register_list]
[-exclude_instances register_list]
[-undo register_list]
```

set_clock_gating_style

Sets the clock-gating style for the clock-gate insertion and replacement.

```
status set_clock_gating_style
[-sequential_cell none | latch]
[-minimum_bitwidth minsize_value]
[-setup setup_value]
[-hold hold_value]
[-positive_edge_logic {cell_list |
integrated [active_low_enable]
[invert_gclk]}
[-negative_edge_logic {cell_list |
integrated [active_low_enable]
[invert_gclk]}
[-control_point none | before | after]
[-control_signal scan_enable | test_mode]
[-observation_point true | false]
[-observation_logic_depth depth_value]
[-max_fanout max_fanout_count]
[-num_stages num_stages_count]
[-no_sharing]
[-gicg_pos_cell {[cell_library/]cell_name}]
[-gicg_neg_cell {[cell_library/]cell_name}]
[-gicg_pos_auto {[cell_library/]cell_name}]
[-gicg_neg_auto {[cell_library/]cell_name}]
```

set_cost_priority

Sets the cost_priority attribute to a specified value on the current design.

```
int set_cost_priority
[-default]
[-delay]
cost_list
[-design_rules]
[-min_delay]
```

set_dft_signal

Specifies the DFT signal types for DRC and DFT insertion.

```
status set_dft_signal
[-view existing_dft | spec]
[-test_mode mode_name]
-type signal_type
[-port port_list]
[-active_state active_state]
[-timing timing]
[-period period]
[-hookup_pin hookup_pin]
[-hookup_sense inverted | non_inverted]
[-internal_clocks none | single | multi]
[-ctrl_bits ctrl_bits_list]
[-pll_clock pll_clock]
[-ate_clock ate_clock]
[-differential_clock clock_port]
[-connect_to pin_list]
[-usage use_type]
[-associated_clock associated_clock]
[-associated_internal_clocks pin_names]
```

set_domain_supply_net

Set the primary power net and primary ground net of an already existing power_domain. This command is supported only in UPF mode.

```
int set_domain_supply_net
domain_name
-primary_power_net supply_net_name
-primary_ground_net supply_net_name
```

set_dont_use

Sets the dont_use attribute on library cells to exclude them from the target library during optimization.

```
int set_dont_use
[-power] object_list
```

set_isolation

Defines the UPF isolation strategy for the power domains in the design. This command is supported only in UPF mode.

```
status set_isolation
isolation_strategy
-domain power_domain
-isolation_power_net isolation_power_net
-isolation_ground_net isolation_ground_net
[-clamp_value 0 | 1 | z | latch]
[-applies_to inputs | outputs | both]
[-elements objects]
[-no_isolation]
```

set_isolation_control

Provides additional options needed for creating isolation cells. This command is needed with most set_isolation commands. This command is supported only in UPF mode.

```
status set_isolation_control
isolation_strategy
-domain power_domain
-isolation_signal isolation_signal
[-isolation_sense low | high]
[-location self | parent]
```

set_leakage_power_model

Specifies the model that will be optimized by leakage optimizations.

```
status set_leakage_power_model
[-type leakage | channel_width]
[-mvth_weights weights]
[-reset]
```

set_level_shifter

Sets a strategy for level shifting during implementation. This command is supported only in UPF mode.

```
status set_level_shifter
level_shifter_name
-domain domain_name
[-elements list]
[-applies_to inputs | outputs | both]
[-threshold value]
[-rule low_to_high | high_to_low | both]
[-location self | parent | fanout |
automatic]
[-no_shift]
```

set_level_shifter_strategy

Sets the type of strategy to use for adjusting the voltage levels in the design.

```
int set_level_shifter_strategy
-rule all | low_to_high | high_to_low
[-location inside | outside | source | sink]
```

set_level_shifter_threshold

Sets the minimum threshold beyond which the voltage adjustment is required.

```
int set_level_shifter_threshold
-voltage volt
-percent diff
```

set_max_dynamic_power

Sets the target dynamic power for the current design by setting the max_dynamic_power attribute to a specified value.

```
int set_max_dynamic_power
dynamic_power
[GW | MW | KW | W | mW | uW | nW | pW | fW |
aW]
```

set_max_leakage_power

Sets the target leakage power for the current design by setting the max_leakage_power attribute to a specified value.

```
int set_max_leakage_power
leakage_power
[GW | MW | KW | W | mW | uW | nW | pW | fW |
aW]
```

set_max_total_power

Sets the target total power for the current design by setting the max_total_power attribute to a specified value.

The set_max_total_power constraint will be obsolete in a future release. Use set_max_leakage_power and set_max_dynamic_power constraints as a replacement.

```
int set_max_total_power
total_power
[GW | MW | KW | W | mW | uW | nW | pW | fW |
aW]
```

set_nominal_power_state_template

Specifies a list of power nets as the template to define power states. This command is supported only in non-UPF mode.

```
integer set_nominal_power_state_template
[power_net_list]
```

set_operand_isolation_cell

Specifies a list of operators or hierarchical combinational cells to be included or excluded as operand isolation candidates.

```
status set_operand_isolation_cell
object_list
[true | false]
```

set_operand_isolation_scope

Specifies whether a design or instance should be included or excluded for operand isolation processing.

```
status set_operand_isolation_scope
object_list
[true | false]
```

set_operand_isolation_slack

Sets the timing threshold to a value below which the automatic isolation roll back operation is not triggered.

```
status set_operand_isolation_slack
[slack_value]
[-weight weight_value]
```

set_operand_isolation_style

Sets the operand isolation style used by Power Compiler.

```
int set_operand_isolation_style
[-logic AND | OR | adaptive]
[-user_directives]
[-verbose]
```

set_power_gating_signal

Sets the attributes on the ports or pins in the design to indicate the power gating pins and the type of retention registers that will use the ports or pins to connect to or through the corresponding design hierarchy. This command is supported only in non-UPF mode.

```
integer set_power_gating_signal
[-power_pin_index index]
[-library_pin library_pin_name]
[-type style]
ports_or_pins
```

set_power_gating_style

Sets the power_gating_style attributes on designs, cell instances, or HDL blocks, to specify the type of retention register cells from the target library used by the compile command. This command is supported only in non-UPF mode.

```
int set_power_gating_style
-type style
[-hdl_blocks hdl_blocks]
[-hierarchy]
[cell_or_design_list]
```

set_power_prediction

Sets the power prediction mode for compile_ultra or compile_ultra -incremental. This command is supported only in topographical mode.

```
int set_power_prediction
[true | false]
[-ct_references lib_cell_list]
```

set_related_supply_net

Associates an external supply net to the port of the design.

```
status set_related_supply_net
[supply_net_name]
[-object_list objects]
[-reset]
[-ground ground_net_name]
[-power power_net_name]
```

set_replace_clock_gates

Set directives for clock gate replacement. Forces the enabling or disabling of clock gate replacement for specified combinational cells in the current design. Also sets the edge type for modules or black-box cells that otherwise could not be replaced. The cells are replaced by executing the replace_clock_gates command.

```
int set_replace_clock_gates
[-include_cells cell_list]
[-exclude_cells cell_list]
[-rising_edge_clock pin_list]
[-falling_edge_clock pin_list]
[-undo object_list]
```

set_retention

Defines the UPF retention strategy for the power domains in the design. This command is supported only in UPF mode.

```
status set_retention
retention_strategy
-domain power_domain
-retention_power_net retention_power_net
-retention_ground_net retention_ground_net
[-elements objects]
```

set_retention_control

Defines the UPF retention control signals for the defined UPF retention strategy. This command is supported only in UPF mode.

```
status set_retention_control
retention_strategy
-domain power_domain
-save_signal {save_signal save_sense}
-restore_signal {restore_signal
restore_sense}
```

set_retention_control_pins

Converts the retention register library cell attributes in the old library format to the ones that can be used in $retain flow. The $retain flow requires retention register library cells to have new retention cell attributes, which is different from the original power gating flow.

```
status set_retention_control_pins
[-type style]
[-power_pin_index power_pin
 | -library_pin library_pin_name]
[-is_save_pin | -is_restore_pin |
-is_save_restore_pin]
lib_or_lib_cell_list
```

set_switching_activity

Sets switching activity annotation on nets, pins, ports and cells of the current design.

```
int set_switching_activity
[-static_probability sp_value]
[-toggle_rate tr_value]
[-state_dep state_condition]
[-path_dep path_sources]
[-rise_ratio ratio_value]
[-period period_value | -clock clock_name]
[-select select_types]
[-hier]
[-instances instances]
[object_list]
[-verbose]
```

write_saif

Writes a backward Switching Activity Interchange Format (SAIF) file.

```
int write_saif
-output file_name
[-instances instances]
[-no_hier]
[-rtl]
[-propagated]
[-exclude_sdpd]
```

write_script

Writes shell commands to save the current settings.

```
int write_script
[-hierarchy]
[-no_annotated_check] [-no_annotated_delay]
[-no_cg]
[-full_path_lib_names] [-nosplit]
[-format dctcl | dcsh]
[-include loop_breaking]
[-output file_name]
```

Power Compiler Variables

Power Compiler defines a set of variables that are used to control its behavior.

compile_power_domain_boundary_optimization

Sets the variable to false to disable boundary optimization across power domain boundaries.

Default value for this variable is true.

do_operand_isolation

Enables or disables operand isolation as a dynamic power optimization technique for a design.

Default value for this variable is false.

ilm_enable_power_calculation

Perform power calculation on design which is to be used as ILM block.

Default value for this variable is true.

physopt_power_critical_range

Specifies a margin of slack for cells during leakage power optimization. If a cell has a slack less than the power critical range, power optimization will not be done for the cell.

Default value for this variable is -1.04858e+06.

power_cg_all_registers

Specifies to the insert_clock_gating command whether to clock gate all registers, including those that do not meet the necessary requirements.

Default value for this variable is false.

power_cg_auto_identify

Activates automatic identification of Power Compiler inserted clock gating circuitry from a structural netlist.

Default value for this variable is false.

power_cg_balance_stages

Controls clock gate stage balancing is on or off during compile [-incremental_mapping] -gate_clock or compile_ultra [-incremental_mapping] -gate_clock.

Default value for this variable is false.

power_cg_cell_naming_style

Specifies the naming style for clock gating cells created during insert_clock_gating.

Default value for this variable is "".

power_cg_derive_related_clock

When *true*, clock domain relationship between registers will be derived from the hierarchical context.

Default value for this variable is false.

power_cg_designware

Performs clock gating on DesignWare sequential components in the design.

The use of power_cg_designware variable will be obsolete in a future release. Clock gating insertion with compile_ultra -gate_clock automatically inserts clock gates in DesignWare modules.

Default value for this variable is false.

power_cg_enable_alternative_algorithm

Specifies to the insert_clock_gating, compile-gate_clock and compile_ultra -gate_clock commands whether to use an alternative algorithm to find gatable registers.

Default value for this variable is false.

power_cg_flatten

Specifies to different ungroup commands whether to flatten Synopsys clock-gating cells.

Default value for this variable is false.

power_cg_gated_clock_net_naming_style

Specifies the naming style for gated clock nets created during insert_clock_gating.

Default value for this variable is "".

power_cg_ignore_setup_condition

When *true*, the setup condition will be ignored for latch-free clock gating.

Default value for this variable is false.

power_cg_inherit_timing_exceptions

Specifies that during compile -gate_clock or compile_ultra [-incr] -gate_clock, timing exceptions defined on registers have to be automatically inferred on to the enable pin of the clock gate that is gating these registers.

Default value for this variable is false.

power_cg_module_naming_style

Specifies the naming style for clock gating modules created during insert_clock_gating.

Default value for this variable is "".

power_cg_print_enable_conditions

When *true*, the enable conditions of registers and clock gates will be reported during clock gate insertion.

Default value for this variable is false.

power_cg_print_enable_conditions_max_terms

Specifies the maximum number of product terms to be reported in the sum of product expansion of the enable condition.

Default value for this variable is 10.

power_cg_reconfig_stages

Controls the reconfiguration of multistage clock gates during compile [-incremental_mapping] -gate_clock or compile_ultra [-incremental_mapping] -gate_clock.

Default value for this variable is false.

power_default_static_probability

Specifies the default static probability value.

Default value for this variable is 0.5.

power_default_toggle_rate

Specifies the default toggle rate value.

Default value for this variable is 0.1.

power_default_toggle_rate_type

Specifies the default toggle rate type.

Default value for this variable is fastest_clock.

power_do_not_size_icg_cells

Controls whether compile does not size the integrated clock-gating cells in a design to correct DRC violations because doing so may result in lower area and power.

Default value for this variable is true.

power_driven_clock_gating

Controls whether switching activity and dynamic power of the register banks should be considered when optimizing the clock gating of the design.

Default value for this variable is false.

power_enable_one_pass_power_gating

When *true*, one-pass flow power gating will be enabled.

Default value for this variable is false.

power_enable_power_gating

When set to true compile will enable the power gating flow which allows the selected retention registers from target library to be used to map sequential elements.

Default value for this variable is false.

power_fix_sdpd_annotation

Specifies whether user-annotated SDPD switching activity annotation is corrected before it is used.

Default value for this variable is true.

power_fix_sdpd_annotation_verbose

Specifies whether verbose messages are reported during fixing of user-annotated SDPD switching activity.

Default value for this variable is false.

power_hdlc_do_not_split_cg_cells

When *true*, nsert_clock_gating does not split clock-gating cells to limit their fanout.

Default value for this variable is false.

power_keep_license_after_power_commands

Affects the amount of time a Power Compiler license is checked out during a dc_shell (Design Compiler) session.

Default value for this variable is false.

power_lib2saif_rise_fall_pd

Specifies whether lib2saif generates forward SAIF files with directives to generate rise/fall dependent path-dependent toggle counts.

Default value for this variable is false.

power_min_internal_power_threshold

Specifies the minimum cell internal power value that can be used in power calculations.

Default value for this variable is "".

power_model_preference

Specifies the preference between the CCS power and the NLPM models in library cells that have power specified in both models.

Default value for this variable is nlpm.

power_opto_extra_high_dynamic_power_effort

This variable makes the compile command invoke more dyanmic power optimization algorithms.

Default value for this variable is false.

power_preserve_rtl_hier_names

Preserves the hierarchy information of the RTL objects in the RTL design.

Default value for this variable is false.

power_rclock_inputs_use_clocks_fanout

Specifies whether clock network objects in an input port fanout are used to infer the input port's related clock.

Default value for this variable is true.

power_rclock_unrelated_use_fastest

Specifies whether the fastest clock is set as the related clock of a design object when a related clock is not inferred by the related clock inference mechanism.

Default value for this variable is true.

power_rclock_use_asynch_inputs

Specifies whether the inferred related clock on an asynchronous pin of a flip-flop is used to determine the nferred related clock on the cell's outputs.

Default value for this variable is false.

power_remove_redundant_clock_gates

Specifies to the compile -incremental and physopt -incremental commands whether to remove redundant Synopsys clock gating cells.

Default value for this variable is true.

power_rtl_saif_file

Defines for the rtl2saif command where to store the forward-annotation SAIF file, if you do not specify the -output option.

Default value for this variable is power_rtl.saif.

power_sa_propagation_effort

Specifies the default effort level used when propagating switching activity.

Default value for this variable is low.

power_sa_propagation_verbose

Specifies the default verbose mode used when propagating switching activity.

Default value for this variable is false.

power_same_switching_activity_on_connected_objects

Forces the tool to use the last user-annotated switching activity data on all connected tool objects.

Default value for this variable is false.

power_sdpd_message_tolerance

Specifies the tolerance value for issuing warnings and information messages during fixing of user-annotated SDPD switching activity.

Default value for this variable is 0.00001.

power_sdpd_saif_file

Defines for the lib2saif command where to store the forward-annotation SAIF file, if you do not specify the -output option.

Default value for this variable is power_sdpd.saif.