EE382M: VLSI-2 EXAMPLE Questions that may be on Exam #1

Early Design Planning

What are five key activities of the early design planning process? Explain in detail to receive full credit?

Constant Field Scaling vs. Constant Voltage Scaling

a) Explain what are the main differences between these two scaling theories.

b) List 3 or more device and/or circuit parameters that scale differently between these two scaling theories.

c) Explain one limitation of Constant Field Scaling.

d) Explain one limitation of Constant Voltage Scaling.

Power equation

Derive the **Power = ½ CV²F** equation

Gate Delay Derivation

Using an inverter driving a total load C = C- + C+, derive the average delay equation below (for both transitions). Show all of your work.

$$\tau = \frac{C * Vdd}{4}\left[\frac{1}{Wn * Idsatn} + \frac{1}{Wp * Idsatp}\right]$$

Variability

a) What is the difference between Static timing analysis and statistical timing analysis?

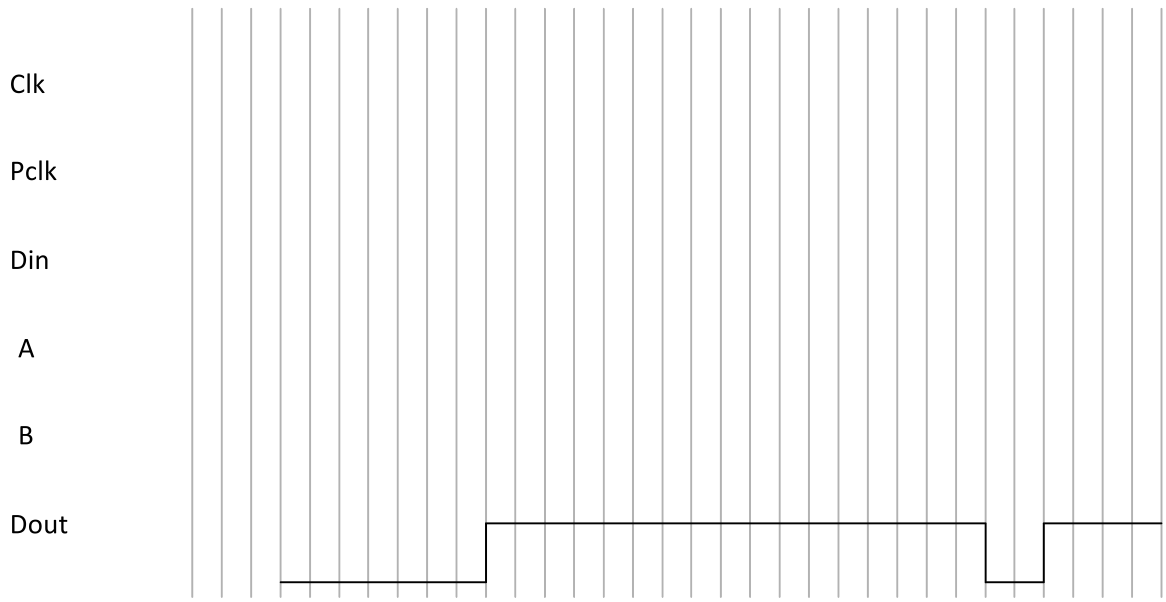
b) How does chemical mechanical polishing of the metal layers impact timing? Why can we model it with statistical variations?

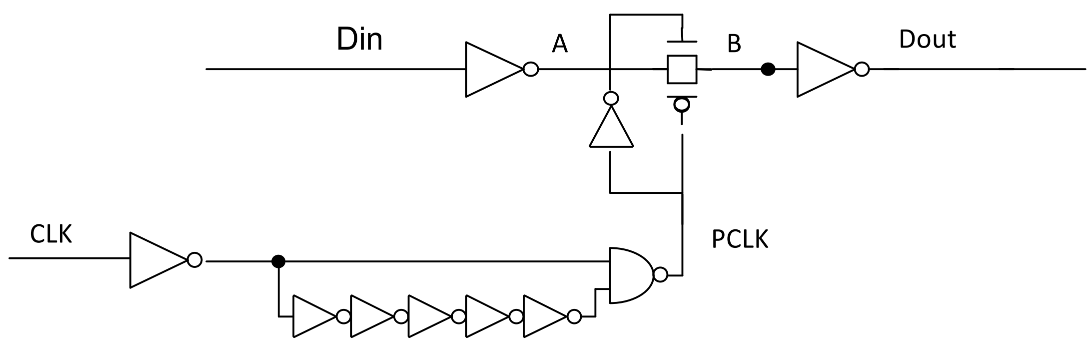
c) Why does modeling cause statistical variations?

Pulsed Latch Timing

- **UNIT** delays on all INVERTERS, NAND gates, and transmission gates. Both transistors on the transmission gate must be on before it transmits a signal.
- Assume perfect rise/fall times on all signals.

a) Given Dout in the timing diagram below, draw CLK, Din, PCLK, A, & B waveforms. Each “tick” on the graph represents one gate delay.





b) Why does this latch not work at very high frequencies? How would you fix it?

c) What limits the maximum frequency of this type of flip-flop?

d) What is the approximate hold time for this flop?

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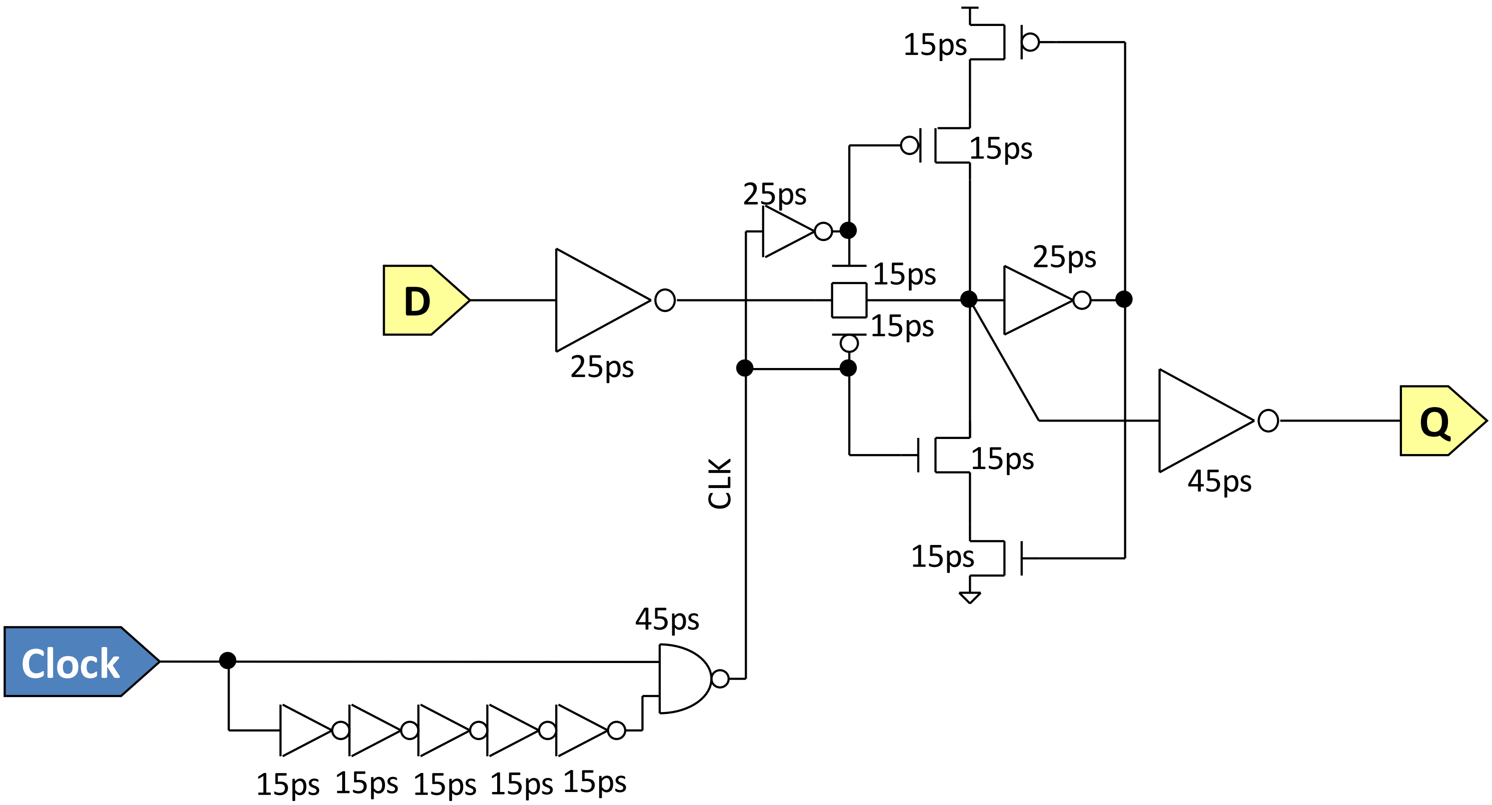
Sequential Elements (20 Points)



a) What is the T_{setup} time

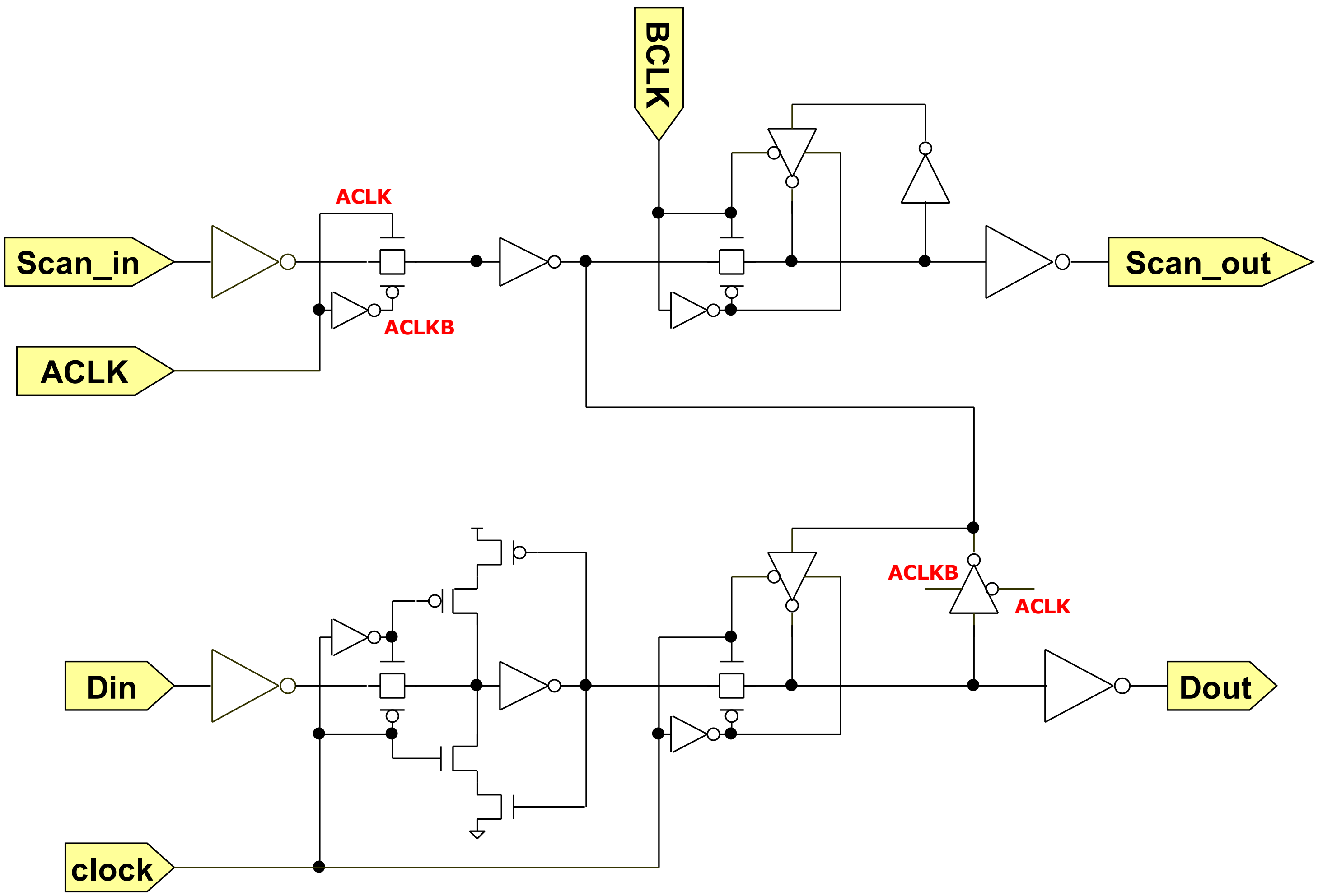
b) What is the T_{hold} time?

c) What is the $T_{clock\text{-}q}$ time?

d) What is the pulse width of the CLK signal?

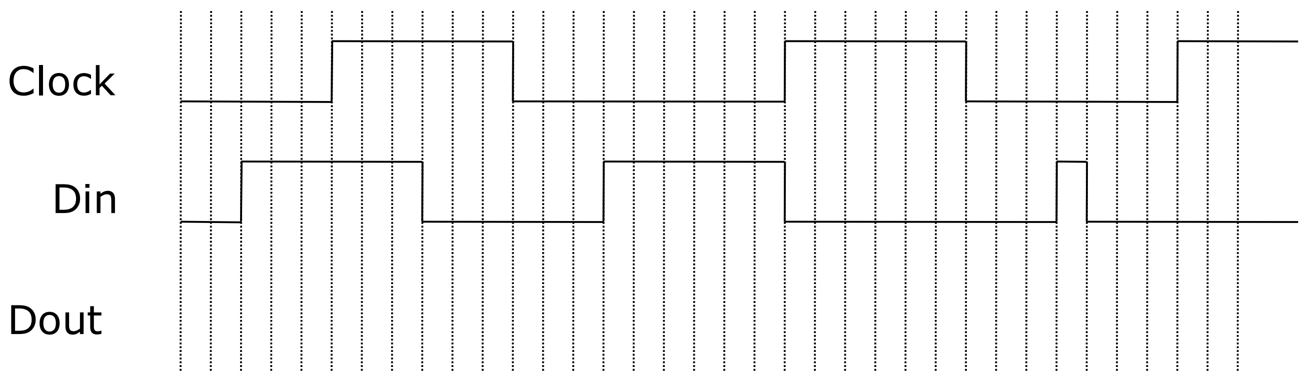
Sequential Elements

a) There is something wrong with this Scan Flip-Flop. Annotate the schematic to fix the problem



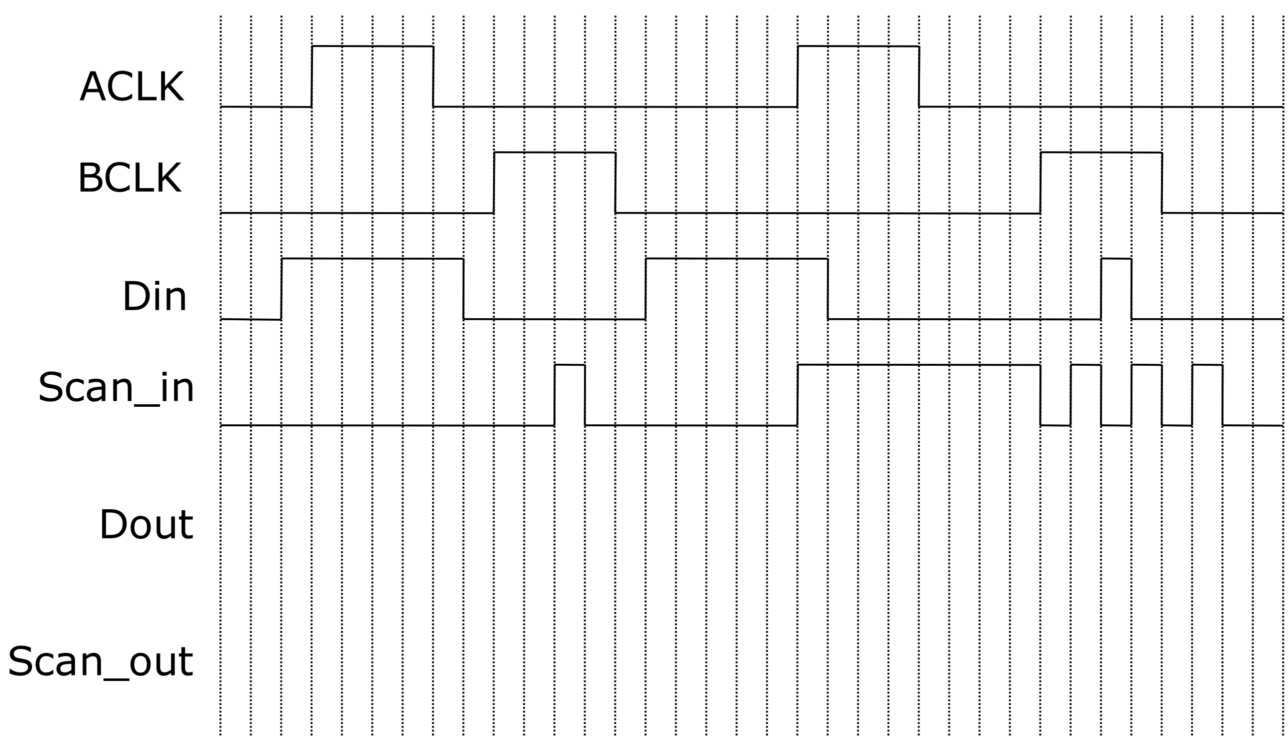
b) Assuming you fixed the Scan Flip Flop correctly; annotate the following timing diagram for signal Dout. **Assume ACLK and BLCK are low (0.0V)**

Assume **UNIT** delays for the Inverters, N-CH & P-CH devices



c) Again assuming you fixed the Scan Flip Flop correctly, annotate the following timing diagram for signal Dout and Scan_out. **Assume Clock is low (0.0V)**

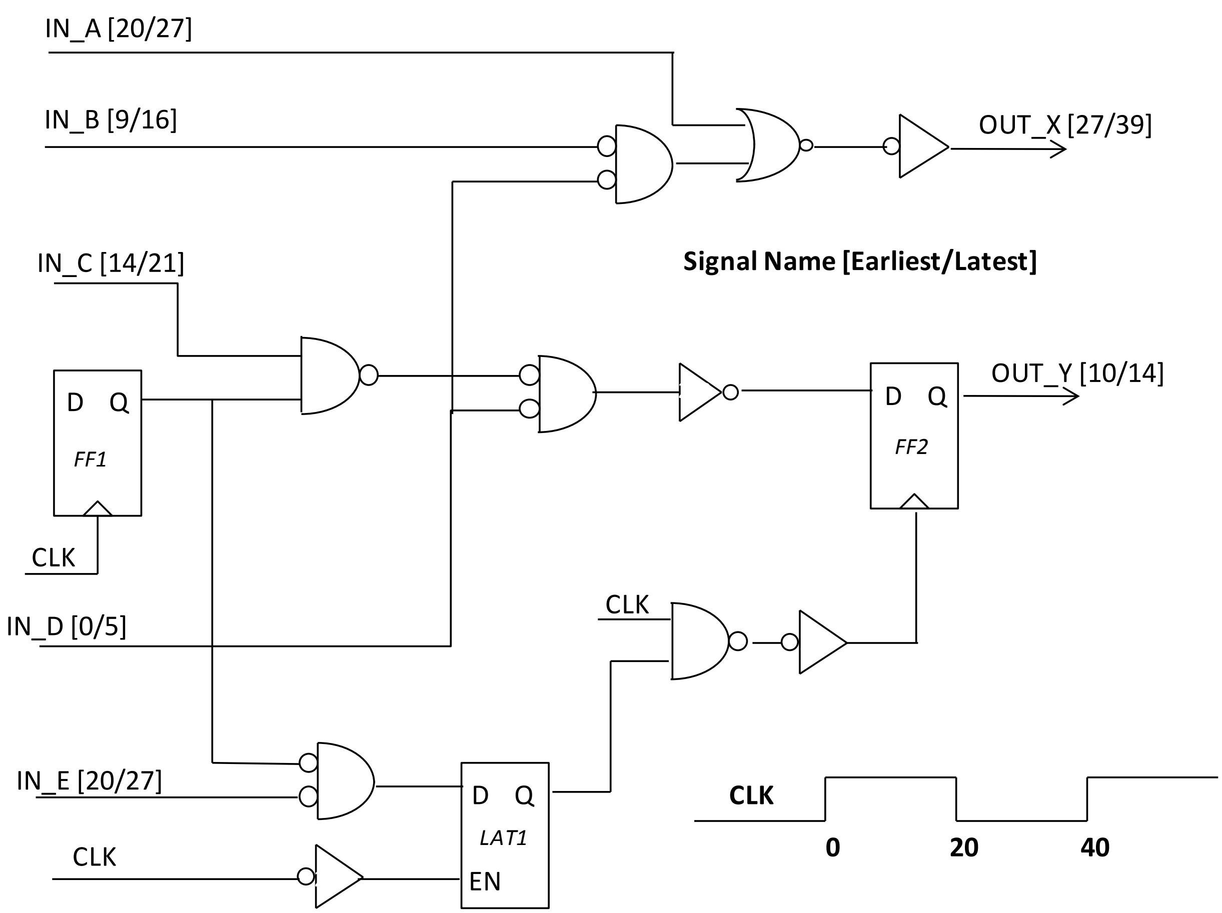
Assume **UNIT** delays for the Inverters, N-CH & P-CH devices



Timing

The I/O timing constraints for this circuit are annotated on the schematic below. The first number is for “MIN Mode” timing and the second number is for “MAX Mode” timing. Your task is to a) identify the critical min and max paths to the primary outputs OUT_X and OUT_Y and b) to find the MIN and MAX slack for this circuit.

Note that the timing delays for each combinational logic gate type are given below. The clock period is 40 units. For robustness the integration team has determined that there is a restriction that the setup time to a clock-gating element will be [1/1] i.e., 1 unit for “MIN-Mode and 1 unit for “MAX-Mode”.



GATE Type [Fastest/Slowest]

2-NAND [3/5]	**DFF Setup [8/12]**	**Latch D-Q [5/7]**
2-NOR [4/6]	**DFF Hold [8/12]**	**Latch C-Q [6/8]**
INV [2/3]	**DFF C-Q [5/7]**	**Latch Hold [0/1]**

HINT: Don’t forget about cycle-adjust requirements for some paths.

a) What are the critical "Max" paths in this circuit?

b) What are the critical "MIN" paths in this circuit?

c) What are the Max-Mode slacks for LAT1 & FF2?

d) What are the Min-Mode slacks for LAT1 & FF2?

Flip-Flop Design

a) What is time borrowing? Give an example on how it could be implemented on a Flip-Flop. What impact does it have on timing analysis?

b) Describe input setup, input hold, and clock to Q delay for a Flip-Flop. Why are these important? Use timing diagrams to describe these.

c) What is a frequency independent failure? Will raising or lowering VDD help alleviate the problem? How do you prevent the problem?

Constant Field Scaling

For this problem we are assuming constant field scaling and the scaling factor 'K' is > 1   i.e. √ 2

a) Explain why gate capacitance scales by **1/K** from one technology generation to the next?

b) Explain why resistance of metal wires scale proportionally to $\mathbf{K^2}$

c) Explain why metal wire RC delay scales proportionally to **K/K (i.e. 1)**.

d) Explain why transistor density (trans/mm^2) scales proportionally to $\mathbf{K^2}$

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EDP Timing

1. Which of the following statements is true for considering timing in the early design planning (EDP) phase of a large chip design project (e.g., "system on a chip" or microprocessor)? Select the **best** answer.
   a. The successful culmination of the EDP timing closure process yields an architectural specification and a floorplan that achieves area and timing goals.
   b. During the EDP phase the design team must define the final cluster sizes before any full chip timing closure can be considered.
   c. Timing closure in the EDP phase is a process of exploring whether the micro-architectural mechanisms can meet timing and to rapidly converge on final cluster sizes and positions prior to embarking on the implementation phase of the design.
   d. All of the above.
   e. Only a and b.
   f. Only a and c.

2. Which of the following practices/analyses is recommended during the EDP timing closure process? Select the **best** answer.
   a. Perform register to register hold time checks
   b. Analyze EDP timing assertions on fully combinatorial input-to-output paths through clusters
   c. Usage of Elmore delay model for critically identified top level chip wires
   d. All of the above.
   e. Only a and b.
   f. Only a and c.

3. Which of the following activities occurs during the EDP timing closure process? Select the **best** answer.
   a. Cluster size estimation
   b. Iterative refinement of data via improved data quality as the implementation progresses
   c. Changes to the architectural specification as timing problems affiliated with architectural mechanisms are corrected
   d. All of the above.
   e. Only a and b.
   f. Only a and c.

4. Which of the following is true of the timing closure process? Select the **best** answer.
   a. Cluster teams attach *required arrival times* (RATs) and *arrival times* (ATs) to their block's input and output pins, respectively, to enable slacks to be calculated at the full chip level. With the RATs the cluster team is indicating when their block requires a signal and with the ATs they are informing the rest of the chip when a launched signal is available.
   b. A contract is established for a path launched from one cluster and captured in another when the top chip slack for that path is not negative. Subsequent cluster timing analyses will then employ an arrival time on inputs derived from the RATs used in the full chip's slack calculation. Likewise the cluster's ATs that were used to find full chip slacks will become the cluster's output pin required arrival times.
   c. If the clock path delay is to be ignored for ease of analysis, it then follows that both the setup time of the capture register and the launch delay should also be ignored.
   d. Only a and b.
   e. Only a and c.
   f. All of the above.

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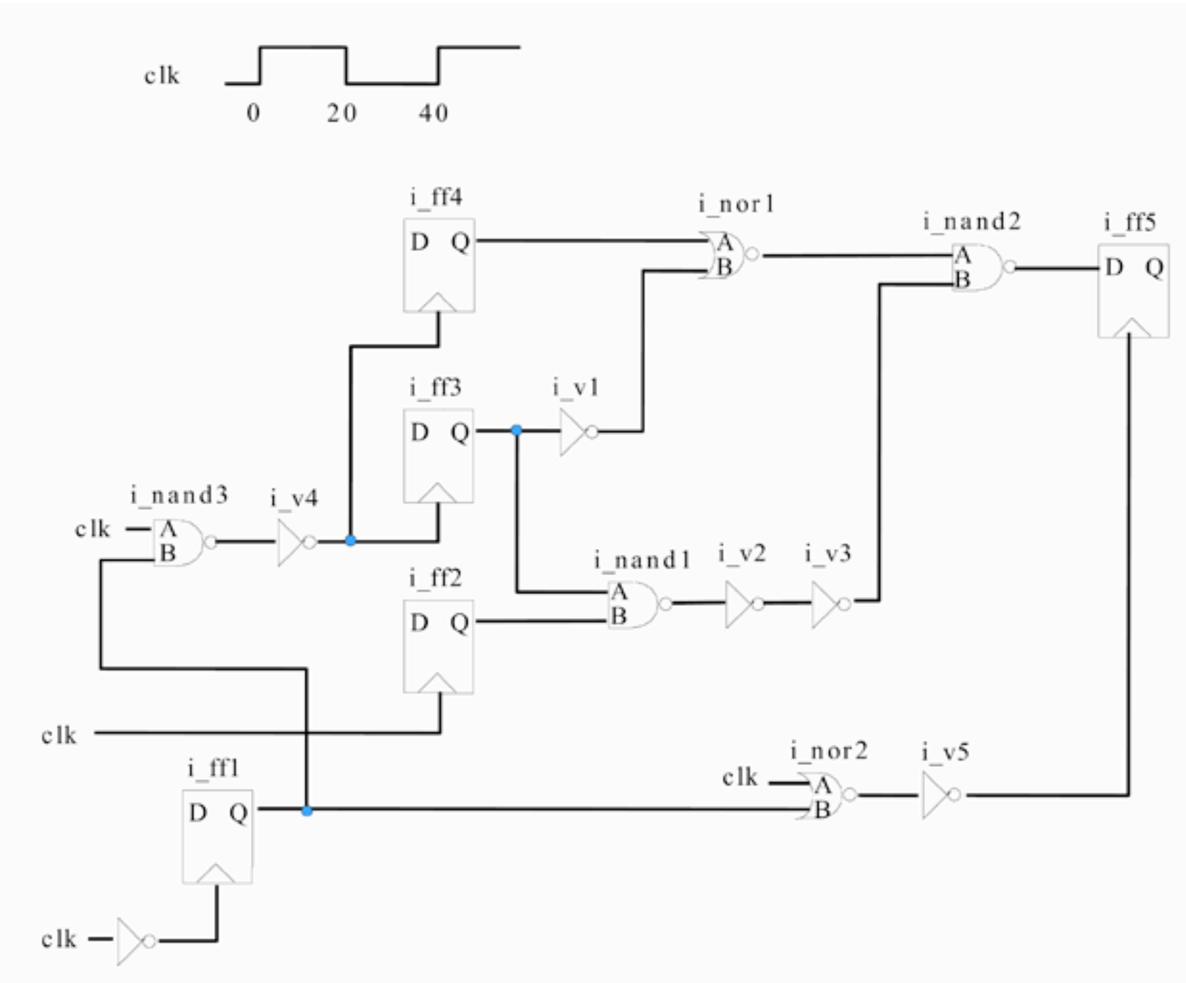
Timing (25 Points)

The arrival times (ATs) below apply to the circuit below. Your task is to **A**) identify the critical min and max paths to instance pin i_ff5/D and **B**) to also find the min and max slack at the following three instance pins using arrival times and the fact that a timing check must be performed at instances where clock and data signals meet: i_ff5/D, i_nand3/B, i_nor2/B. Notice from the table that min and max ATs for clock pins are the same, and non-clock trace pins have same rise and fall ATs for simplicity.



For the critical path identification, list the instances of the data launch in order from path start (clk) to end at i_ff5 (where capture clock converges with launched data).

Assume that clk skew is 0 and that the required setup and hold time for all sequential instances is also 0. Your slacks don't need to match what a STA tool would report for part B, but explain your slack answers where necessary especially pertaining to which edge of the clock is reference for the test.

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For your consideration of part B, the STA timer would attempt to maintain that all events occur within one cycle of clk and perform “cycle accounting adjustments” to accommodate that notion. This adjustment is based on the STA assumption that races, where launch and capture events are triggered from a common causal event, exist only for hold checks such that for setup checks, if a launch and capture event occurs from the same STA edge of the clock, the capture will be adjusted into the next cycle for the slack calculation.

A1) What is Max critical path from clk to i_ff5:

clk -> ?? -> ?? -> ?? -> ?? -> ?? -> ?? -> ?? -> ?? -> i_ff5

A2) What is the Min critical path from clk to i_ff5:

clk ->?? -> ?? -> ?? -> ?? -> ?? -> ?? -> ?? -> ?? -> i_ff5

B. Find the slacks for the “?” in this table:

PIN	**Clock**	**ATmin (r/f)**	**ATmax (r/f)**	**Min Slack**	**Max Slack**
Clk	Yes	0/20	0/20	Don’t care	Don’t care
i_ff1/clk	Yes	22/3	22/3	Don’t care	Don’t care
i_ff2/clk	Yes	0/20	0/20	Don’t care	Don’t care
i_ff3/clk	Yes	6/26	6/26	Don’t care	Don’t care
i_ff4/clk	Yes	6/26	6/26	Don’t care	Don’t care
i_ff5/clk	Yes	7/25	7/25	Don’t care	Don’t care
i_ff5/D	No	8/8	23/23	**?**	**?**
i_nand1/A	No	8/8	10/10	Don’t care	Don’t care
i_nand1/B	No	2/2	4/4	Don’t care	Don’t care
i_nand2/A	No	12/12	16/16	Don’t care	Don’t care
i_nand2/B	No	7/7	19/19	Don’t care	Don’t care
i_nand3/A	Yes	0/20	0/20	Don’t care	Don’t care
i_nand3/B	No	26/26	29/29	**?**	**?**
i_nor1/A	No	8/8	10/10	Don’t care	Don’t care
i_nor1/B	No	10/10	12/12	Don’t care	Don’t care
i_nor2/A	Yes	0/20	0/20	Don’t care	Don’t care
i_nor2/B	No	26/26	29/29	**?**	**?**

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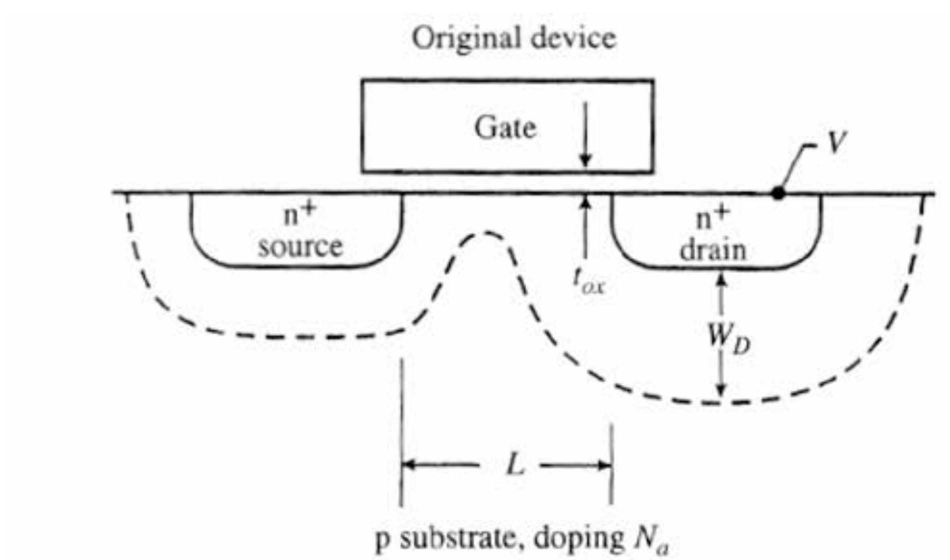
Transistor Scaling **(25 Points)**

Fill out the following table for Constant **FIELD** Scaling.

NOTE: the scaling factor K is > 1 where **K is typically √ 2**

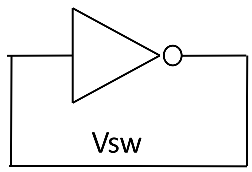
MOSFET device and Circuit Parameters	**Scaling factor K > 1**
Device dimensions (t_{ox}, L, W, x_j)	**1/K**
Doping Concentration (N_a, N_d)	
Voltage (V)	
Depletion Layer Width (W_d)	
Electric Field (ε)	**1**
Capacitance (C=εA/t)	
Power Density (P/A)	
Circuit Density (proportional to 1/A)	
Circuit Delay Time (τ ~ CV/I)	
Channel Resistance (R)	



Device Operation **(20 Points)**

Derive the analytic expression for Vsw where Vout=Vin=Vsw (switch point) for region C for the inverter transfer function shown to the right.

Assume that | Vtp | = Vtn and βn = βp



Recall that the currents through each transistor are equal in the switch point

$$\frac{\beta_n}{2}(V_{in} - V_{tn})^2$$