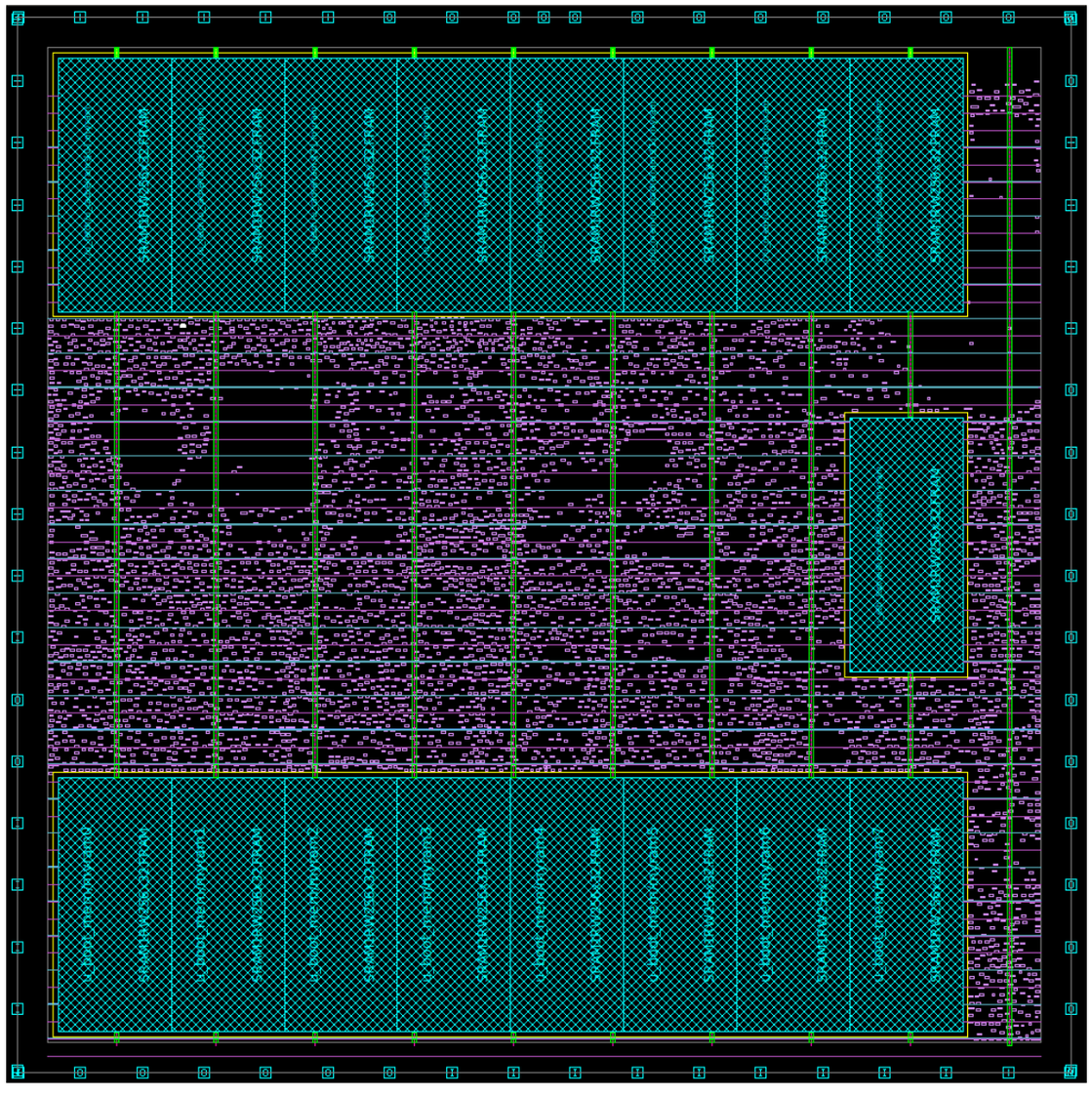
EE382M VLSI-II Project Details

Outline

- Project Objective
- Tentative Targets
- Amber25 Architecture
- 32/28nm EDK
- Design Flow
  - Design Compiler
  - IC Compiler
  - PrimeTime/PTPX
  - Formality

Project Objective

- Design a physical layout of Amber25 SoC that satisfies certain area, power, and timing constraints
  - Input: verilog(RTL), cell/block/tech libraries
  - Output: physical layout

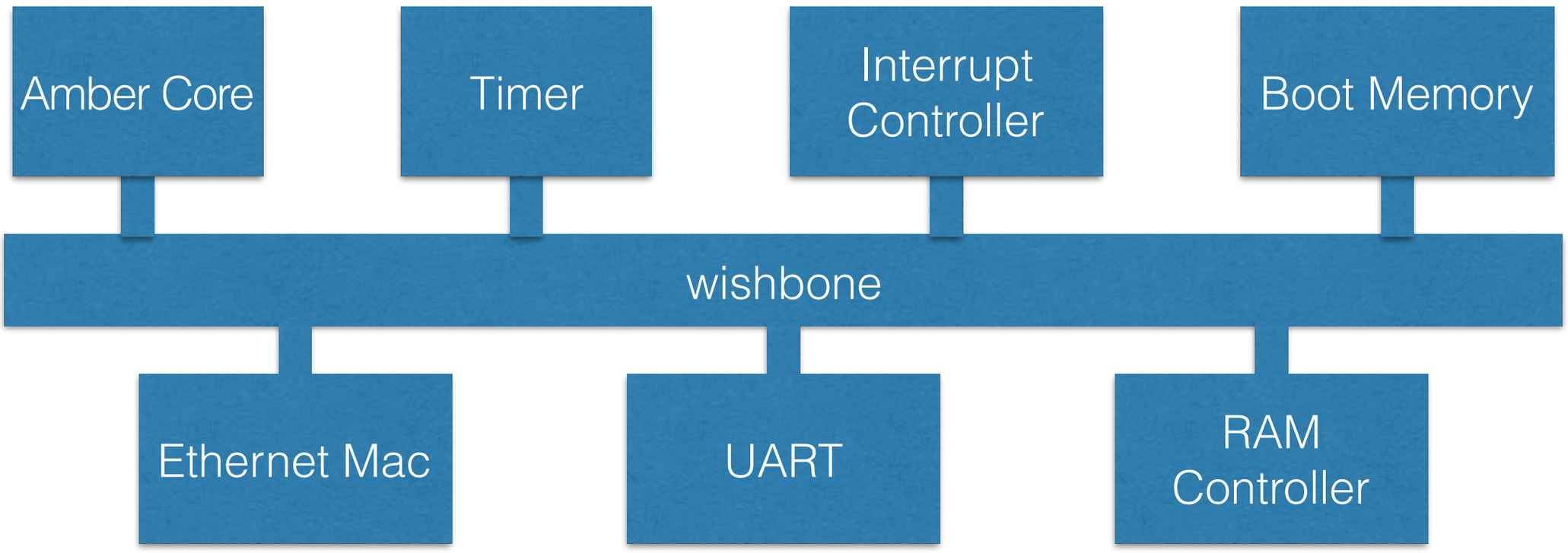


Design Targets

Targets	High Performance	Low Power
cycle time (ns)	2.3	8
total power (mW)	130	15
die area (mm^2)	0.8	0.7
utilization (%)	65	85

PVT Corners	Process	Voltage	Temperature	Checking …
ff1p16v125c	Fast	1.16V	125c	Hold timing
tt1p05v25c	Typical	1.05V	25c	Power
ss0p95n40c	Slow	0.95V	-40c	Setup timing

Amber25 Architecture



Standard Cell Details

- 32/28nm EDK
- Logic Cells (200+ cells)
  - Simple: X0, X1, X2, X4
  - Complex: X0, X1, X2
- Flip-Flops (80+ cells)
  - X0, X1, X2
  - set, reset, active high, active low
- Inverters
  - X0, X1, X2, X4, X8, X16, X32
- Buffers
  - X2, X4, X8, X16, X32
- Misc. Cells
  - Isolation cells, tie cells, …

Vt Flavors

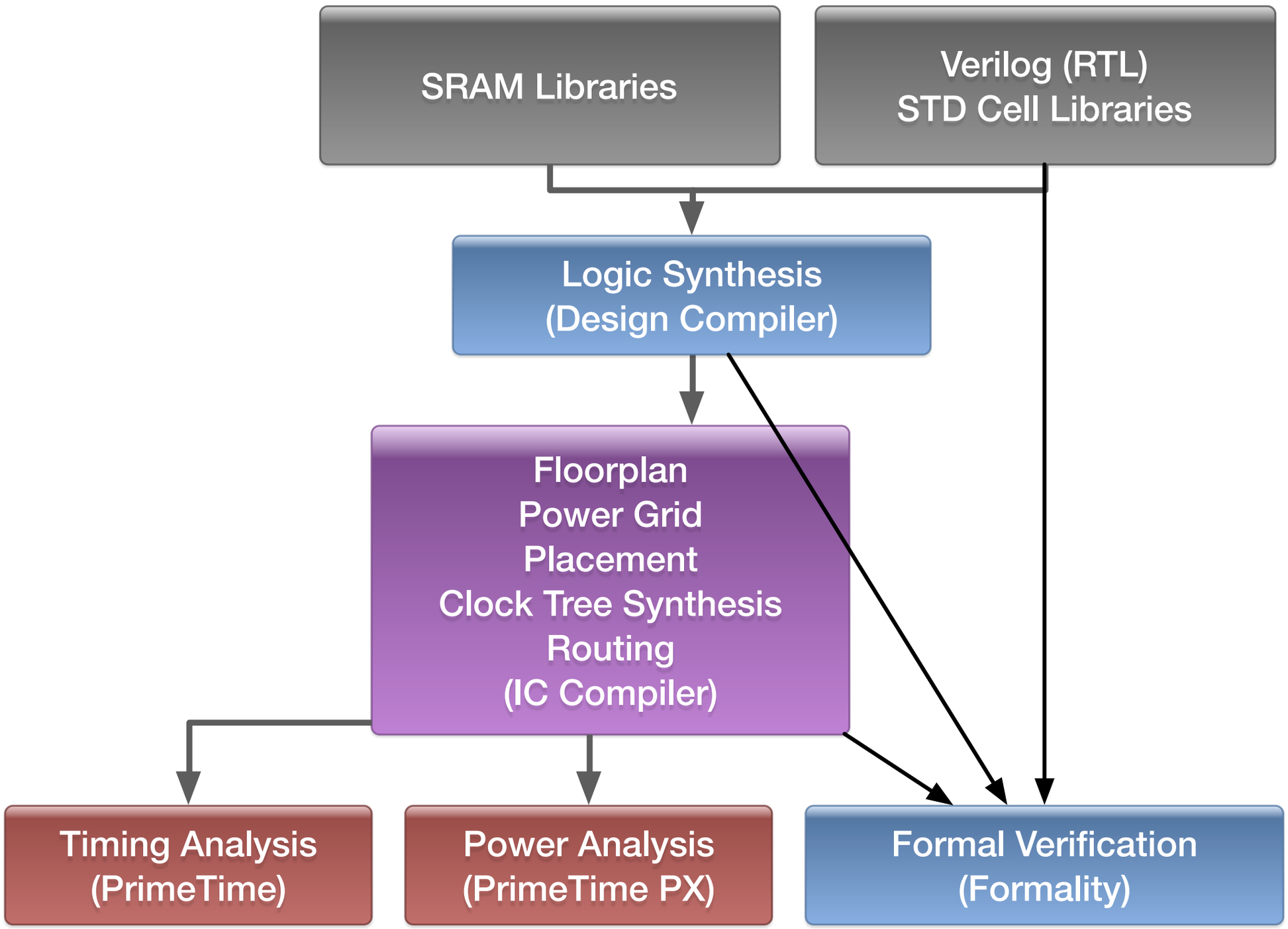
- 3 Vt flavors
  - HVT — High Vt, Low Leakage, Slow Device
  - RVT — Regular Vt, Medium Leakage
  - LVT — Low Vt, High Leakage, Fast Device

INVX1 Vt Comparison

(input slew = 32ps, output load = 0.25fF, corner = tt1p05v25c)

	HVT	RVT	LVT
Area	1	1	1
Leakage Power	1	7.2	33.7
Delay	1	0.78	0.64

Design Flow

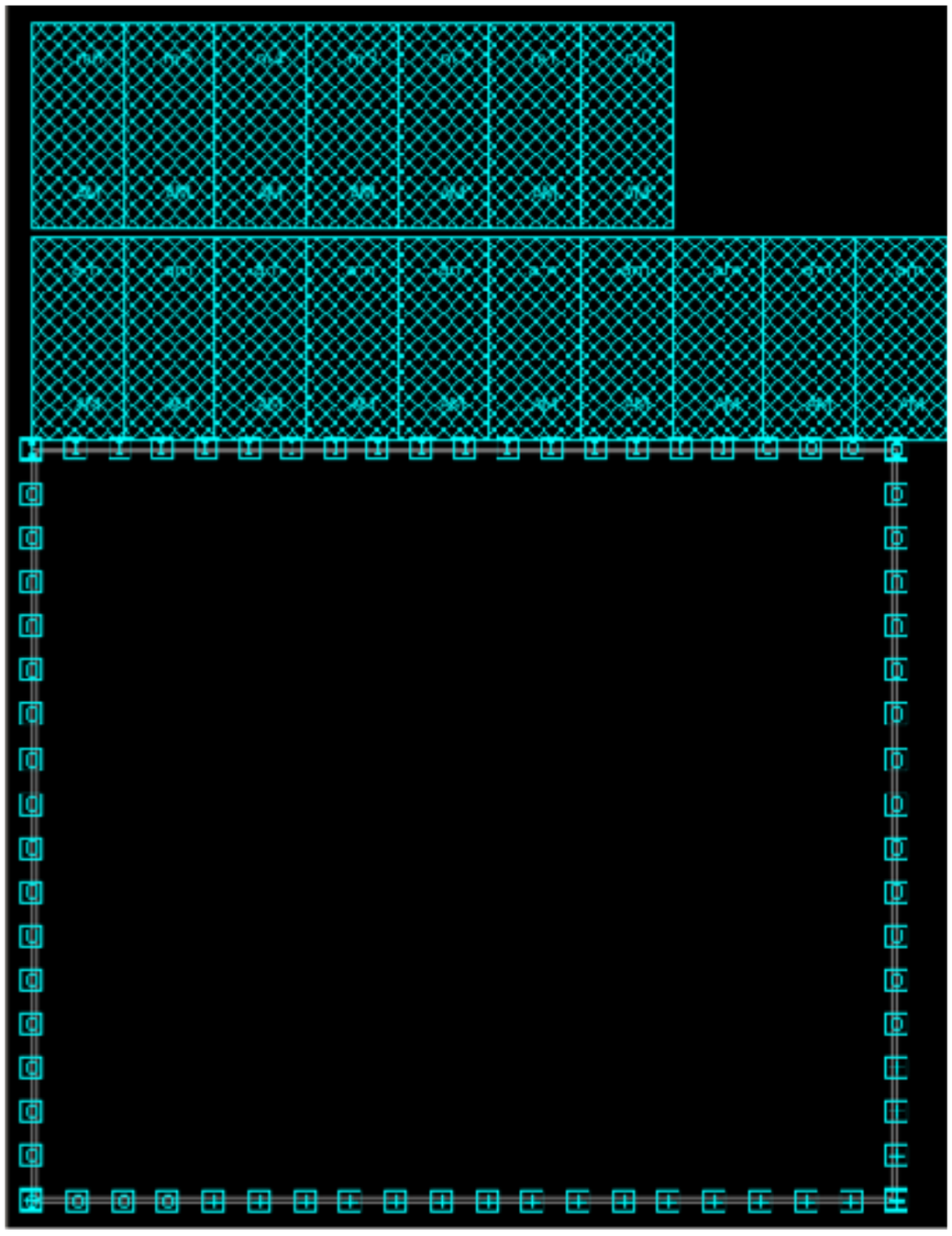

SRAM Libraries
Verilog (RTL)
STD Cell Libraries
Logic Synthesis
(Design Compiler)
Floorplan
Power Grid
Placement
Clock Tree Synthesis
Routing
(IC Compiler)
Timing Analysis
(PrimeTime)
Power Analysis
(PrimeTime PX)
Formal Verification
(Formality)

Design Compiler (DC)

- Logic Synthesis: Convert behavioral-level verilog (RTL) to gate-level verilog (netlist)
- Clock Scheme
  - u_clocks_resets module generates clocks
    - **o_sys_clk** drives Amber Cores
      - cycle time: 2.3 / 8 ns
    - **o_sys_clk_slow** drives the wishbone bus and other peripheral blocks
      - cycle time: 4 times slower than o_sys_clk
  - **mtx_clk_pad_i** & **mrx_clk_pad_i** are used by the Ethernet Mac block
      - cycle time: 20ns
- Timing
  - All paths are assumed to be single cycle
  - Each path is synchronous with only one clock domain
  - A few paths with lot of stages (>30) are timing critical

Create Die Area (ICC)

Determining die size based on utilization target and cell area

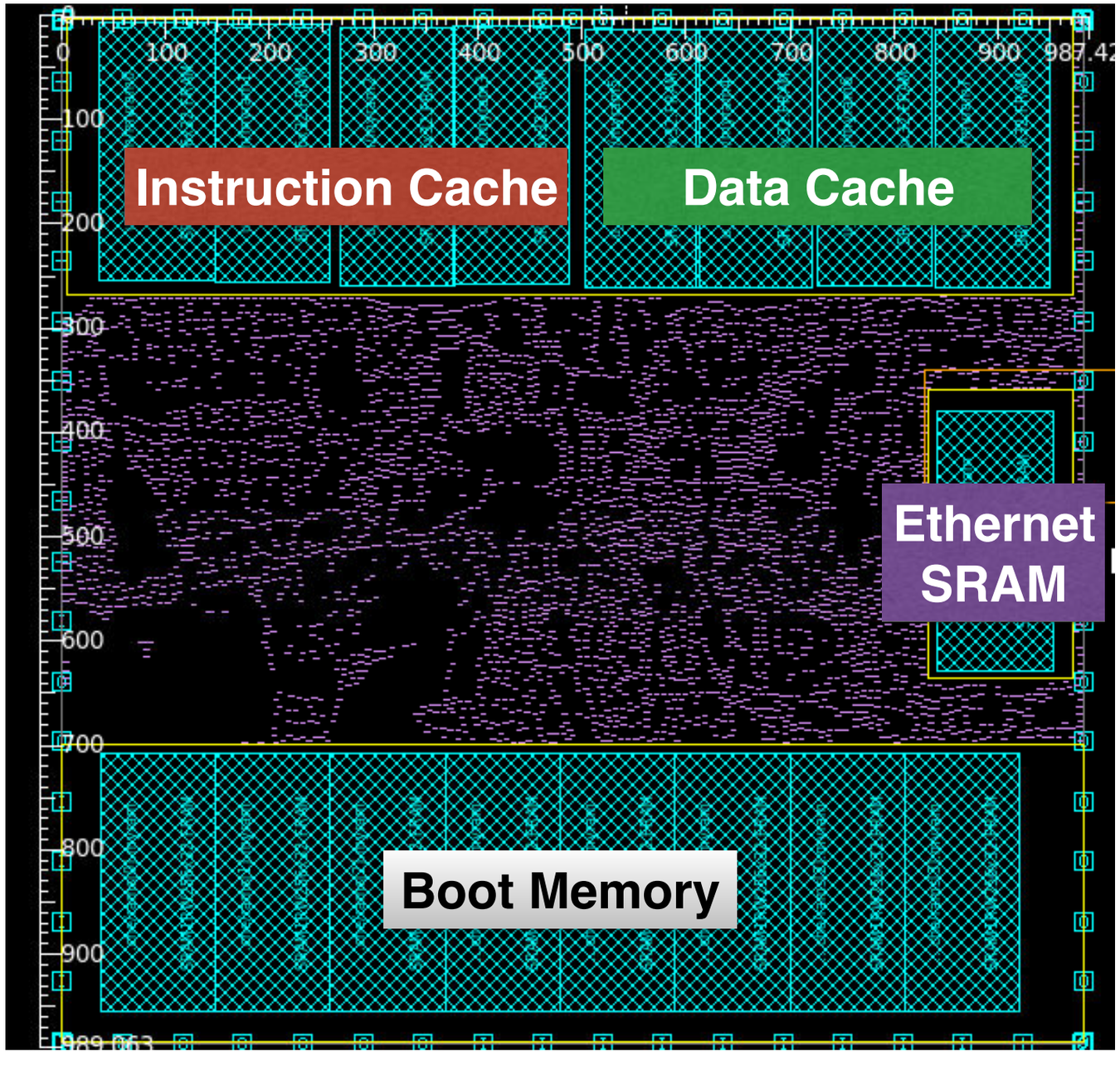


Floorplan (ICC)

Determining SRAMs' positions in die area.

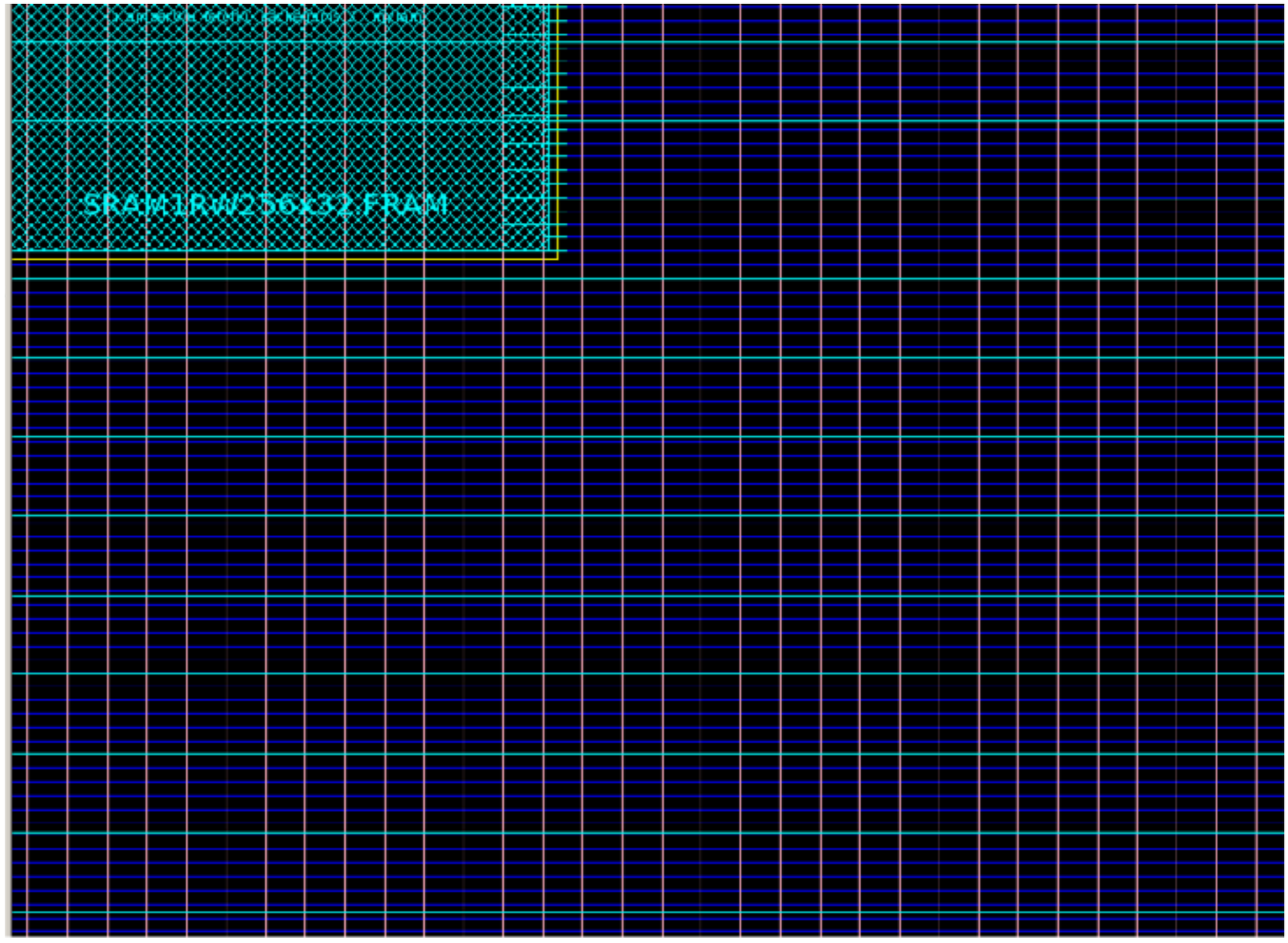
- 17 SRAM blocks in total
  - 4 for core Icache
  - 4 for core Dcache
  - 8 for boot memory
  - 1 for ethernet block

- Each SRAM is of size 256x32



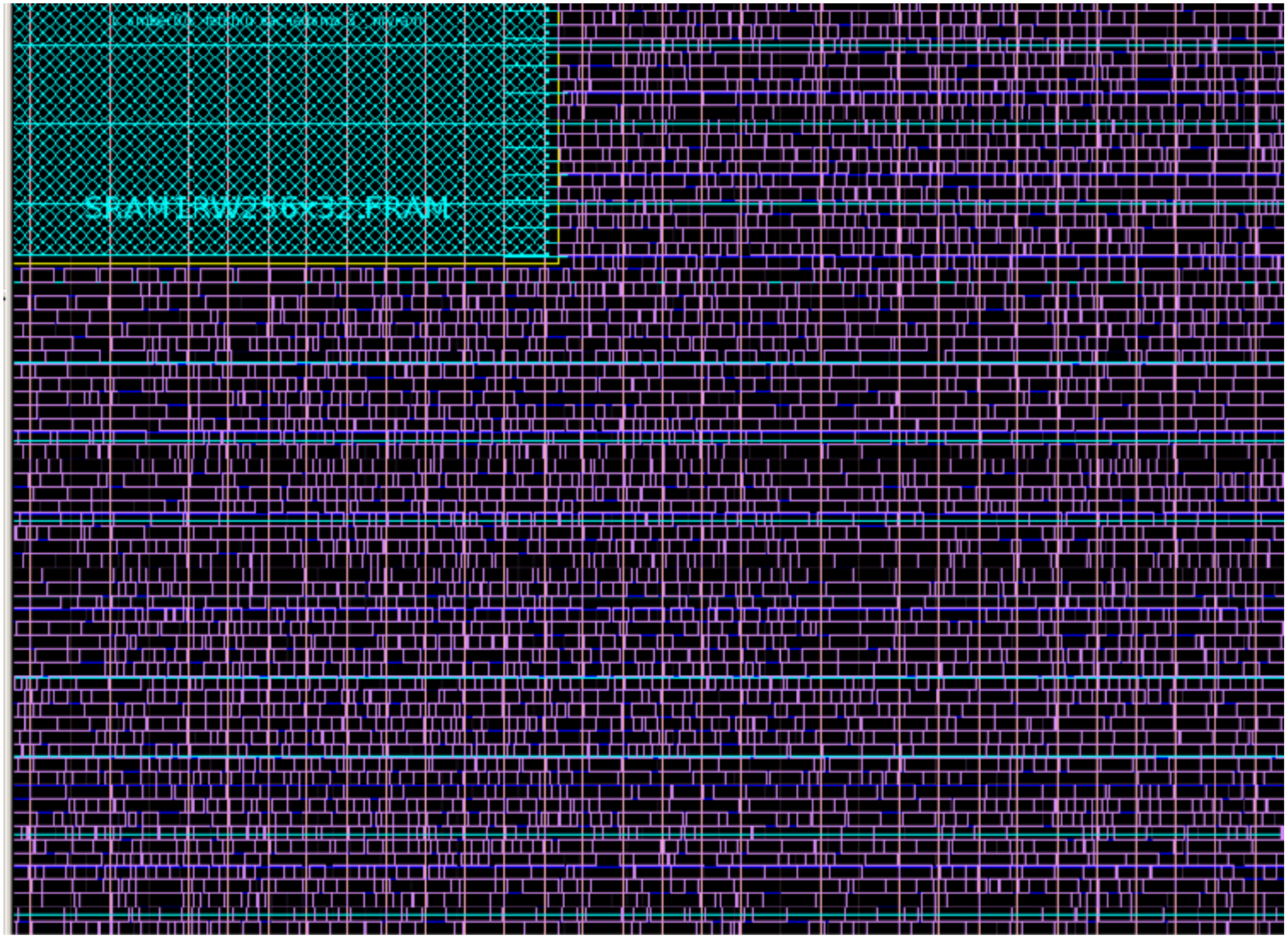
Power Grid (ICC)

Planning power/ground nets

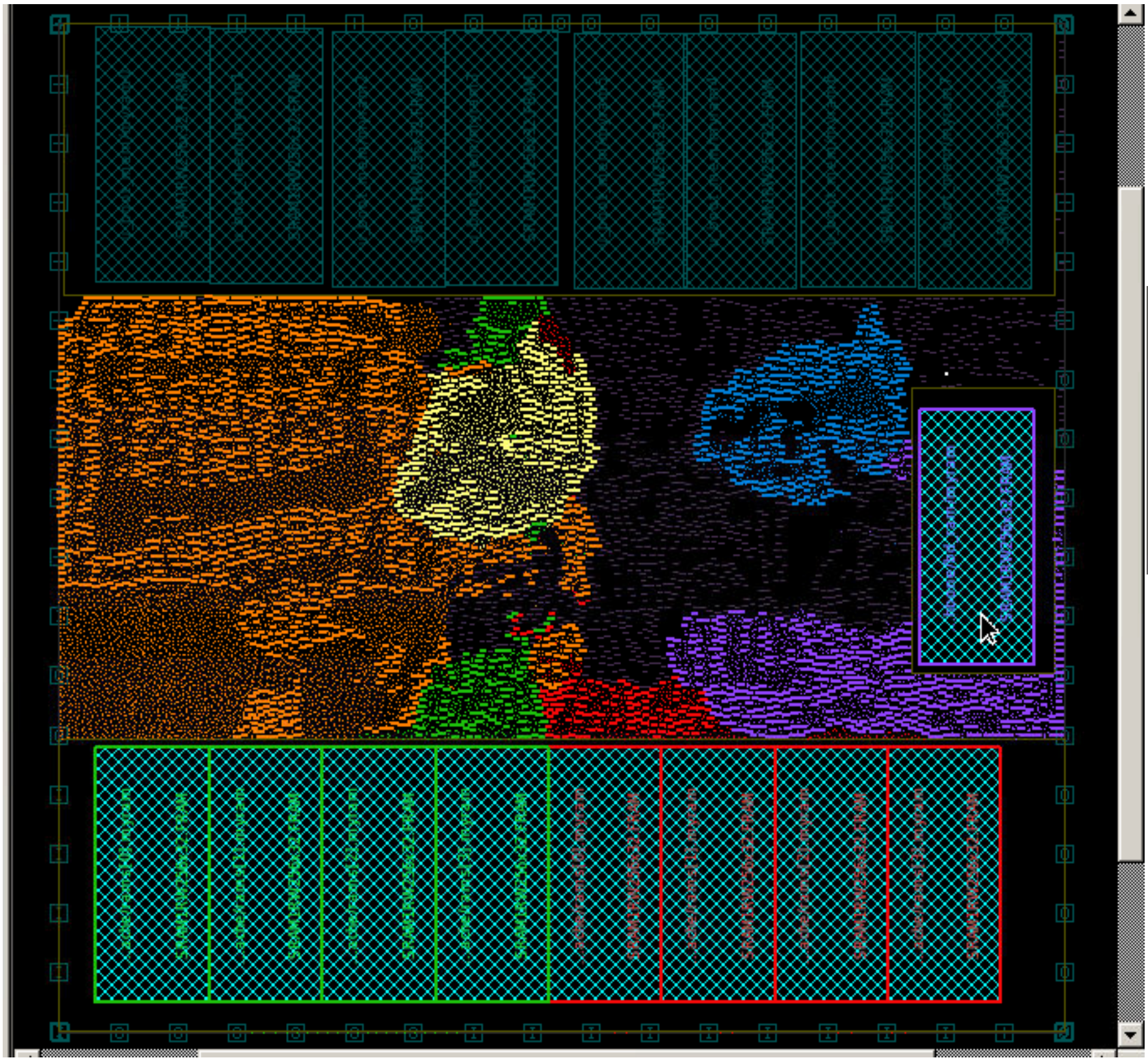


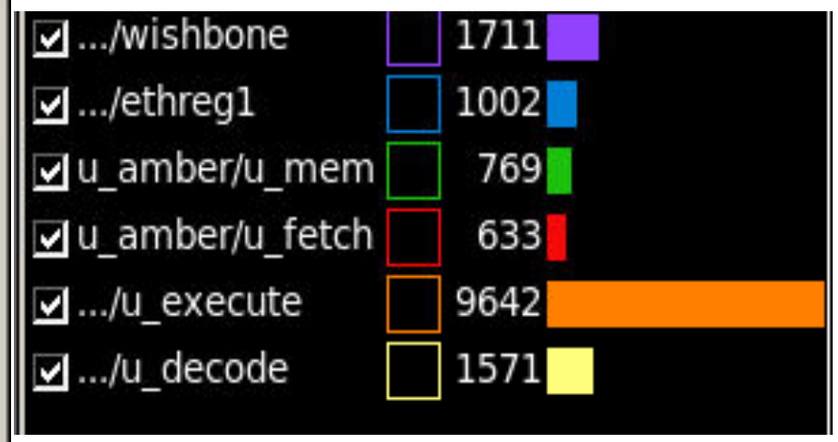
Placement (ICC)

Placing standard cells



Placement (2)

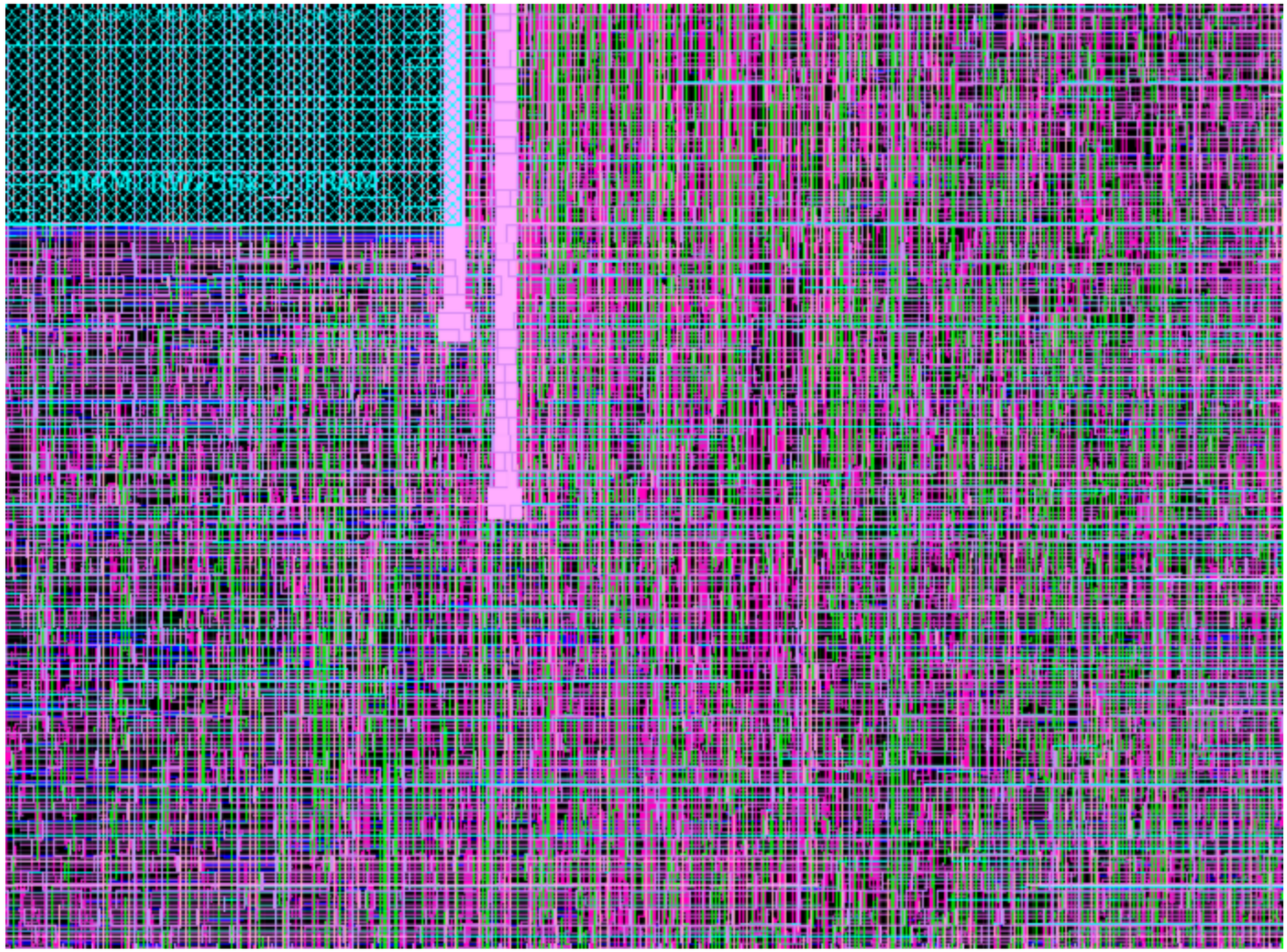



.../wishbone
1711
.../ethreg1
1002
u_amber/u_mem
769
u_amber/u_fetch
633
.../u_execute
9642
.../u_decode
1571

CTS & Routing (ICC)

Clock Tree Synthesis (CTS): Generating clock networks

Routing: Connecting inter-cell networks

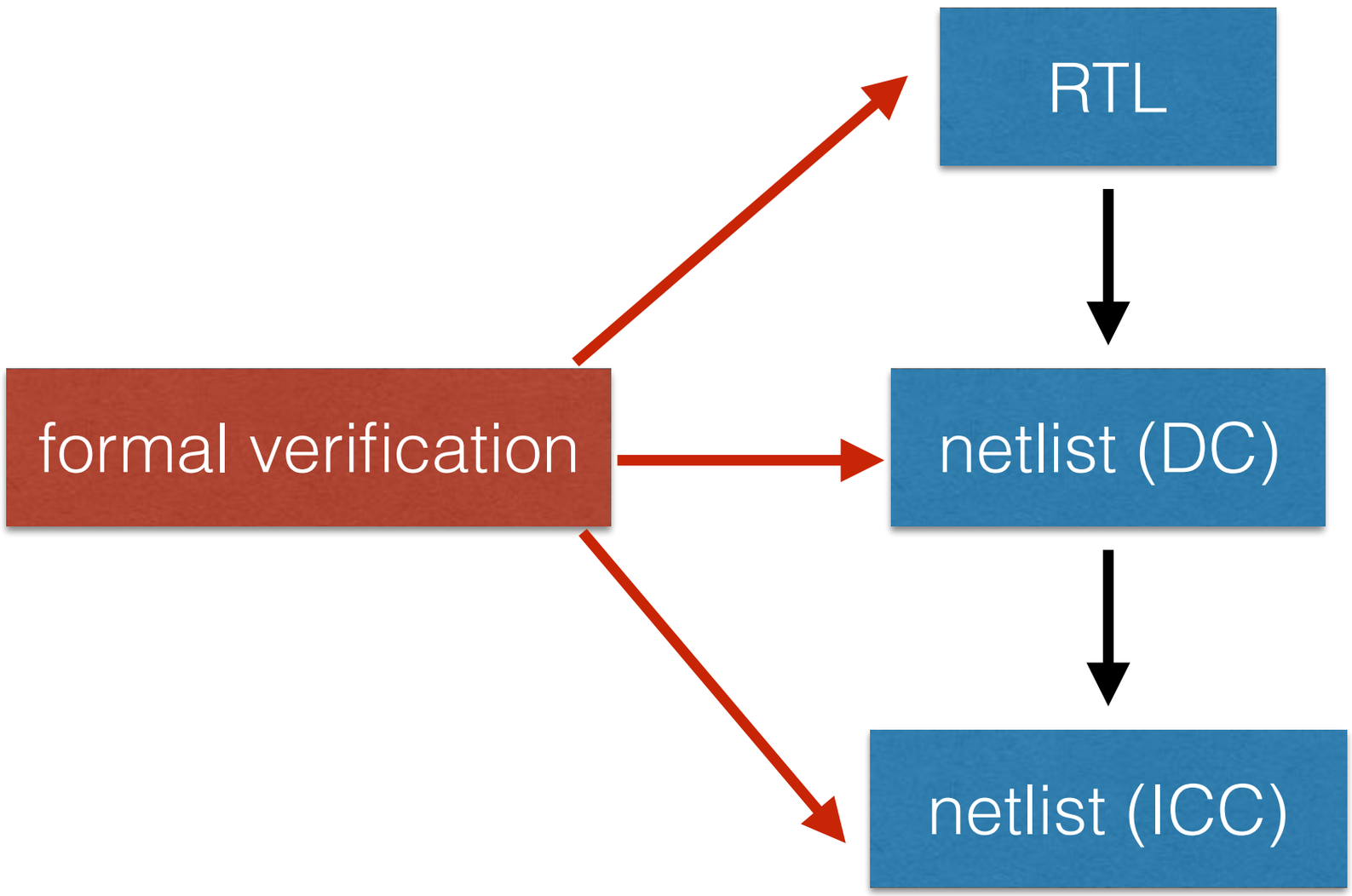


Timing/Power Analysis (PrimeTime/PTPX)

- Timing Analysis:
  - Detecting setup/hold critical paths
  - Detecting bottleneck cells
  - ECO flow helps fix timing
- Power Analysis:
  - Activity factor based timing analysis

Formal Verification (Formality)

Checking if two versions of a design are functionally equivalent



To Get started

- Flow framework is provided
  - /home/projects/courses/spring_17/ee382m-16810/project_spring_17/get_started
  - Don’t trust my framework/code blindly
- Read through “tcl_tutorial.pdf” before you start
- Don't try to understand everything before you start
- Try to understand what information is contained in each type of library/file
  - Liberty File (*.lib / *.db)
  - SPEF (*.spef)
  - DEF (*.def)
  - LEF (*.lef)
  - ……