EE-382M
VLSI–II
CMOS LEVEL SHIFTERS
SPRING 2017

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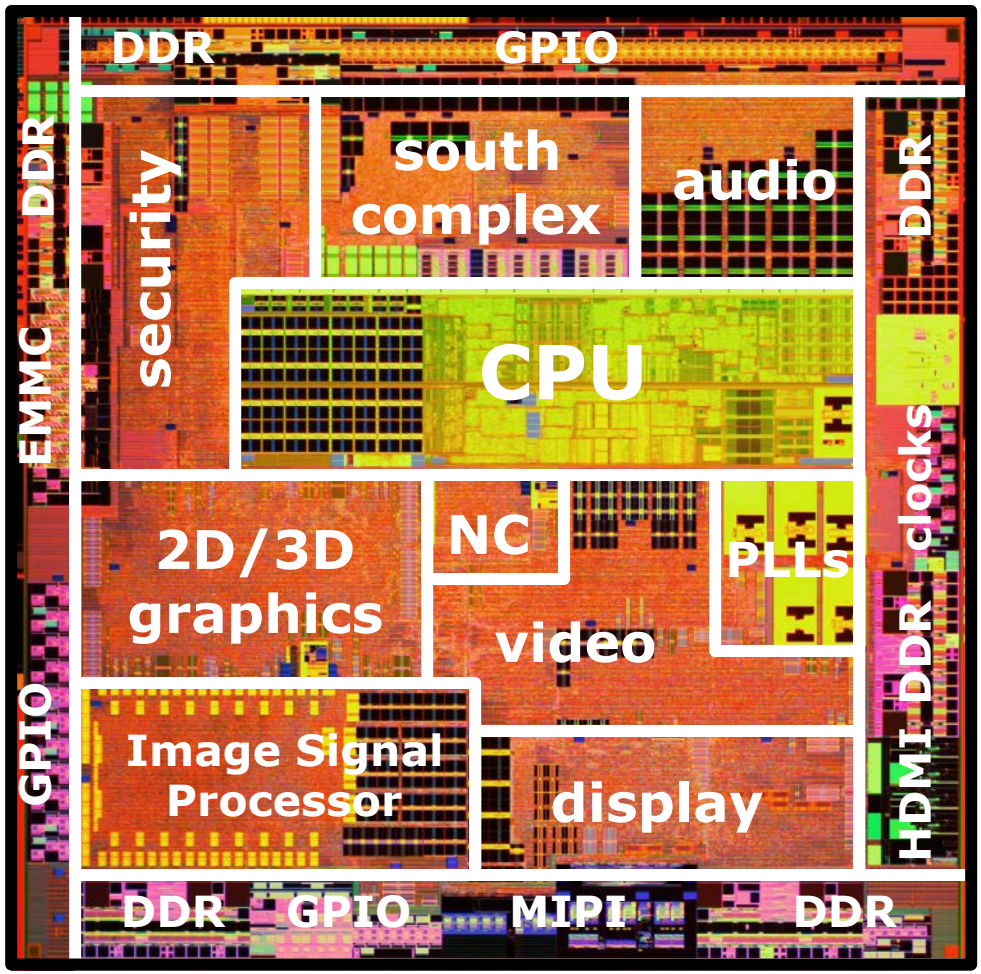
OUTLINE

- Motivation
- Basic Operation
- Design Evolution
- Designing for Collapsible Power Grids with FIREWALLs
- Multi-stage Design for High Voltage
- Conclusion

MOTIVATION

SoC integration of many unrelated functions in their own power 'islands'.

Intel Z2460 ATOM SoC

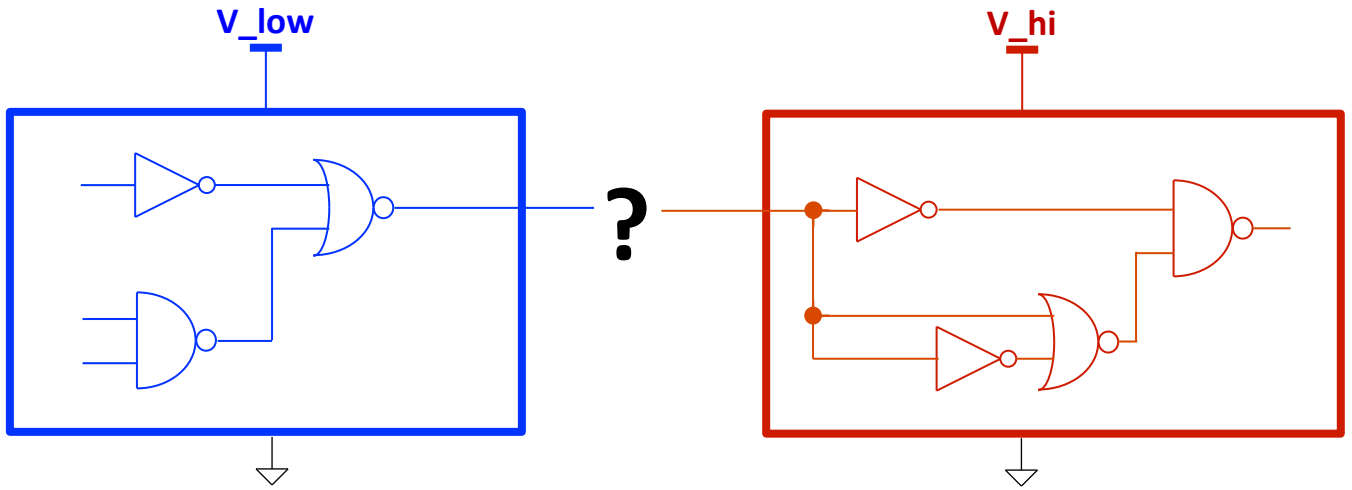


Rumi Zahir, HOT CHIPs #24, Aug. 2012

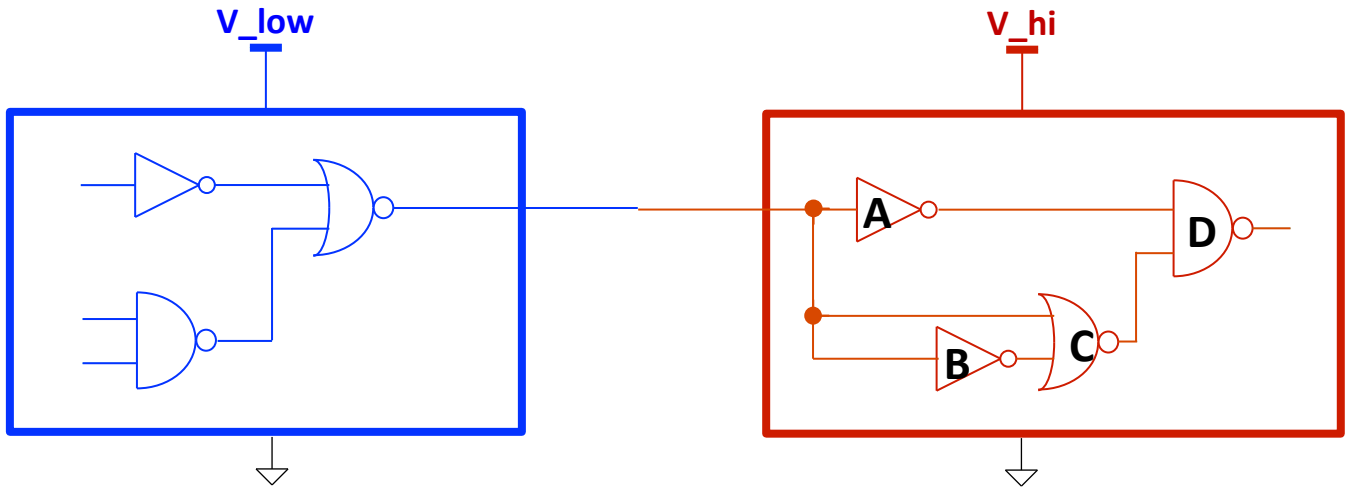
MOTIVATION – cnt'd

- On-die voltage regulation leading to power 'islands' that can have different voltage levels.
- Power management that shuts functional units off.
- Voltage-Frequency pairs; CPU's can be run in several operating points where its power supply is adjusted to reduce power:
  - lowest frequency: 100 - 600MHz
  - medium frequency: 700 - 1500MHz
  - burst frequency: 1600 – 3000MHz
- OFF chip drivers have to support various voltage levels whereas the controller logic is powered by a lower voltage :
  - LPDDR: 1.25V
  - MIPI-display: 1.25V regulated to 0.4V differential
  - HDMI-display 3.3V
  - SD cards: 2.85V
  - GPIO: 1.25V and 1.80V

BASIC OPERATION #1



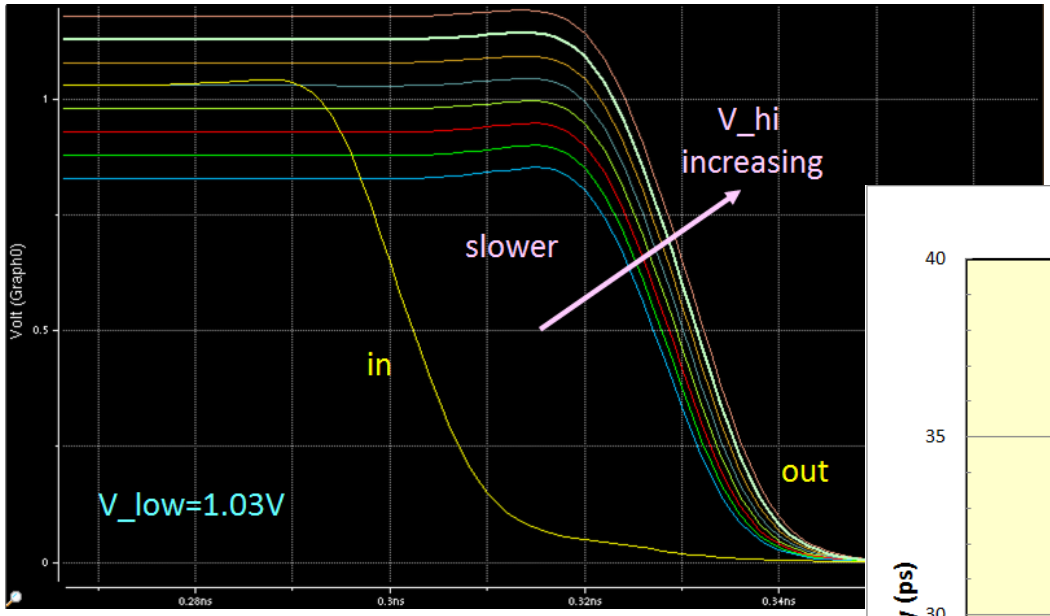
BASIC OPERATION #2

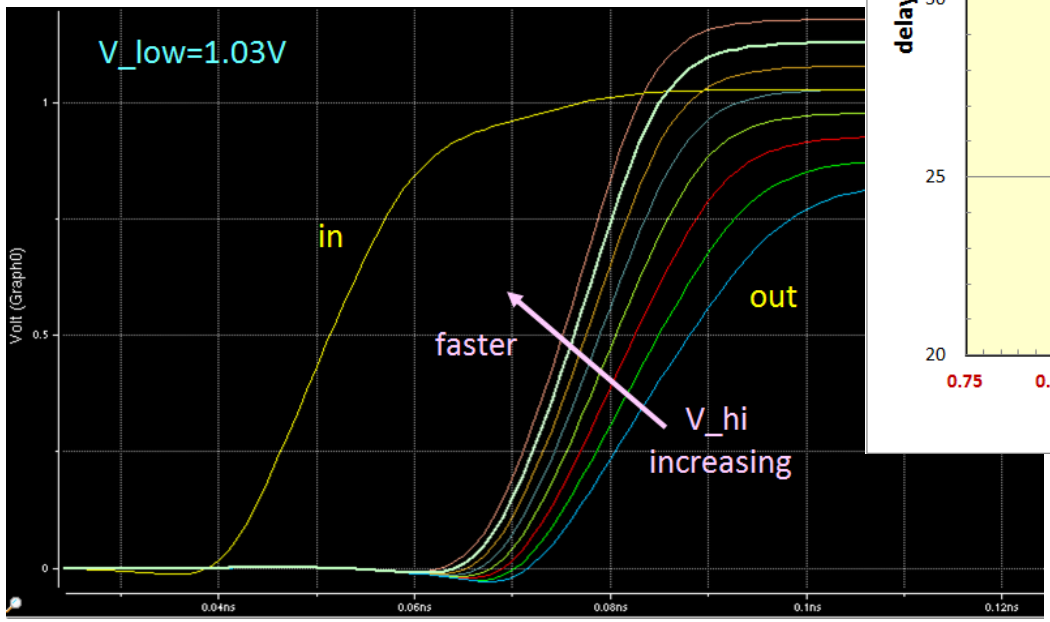


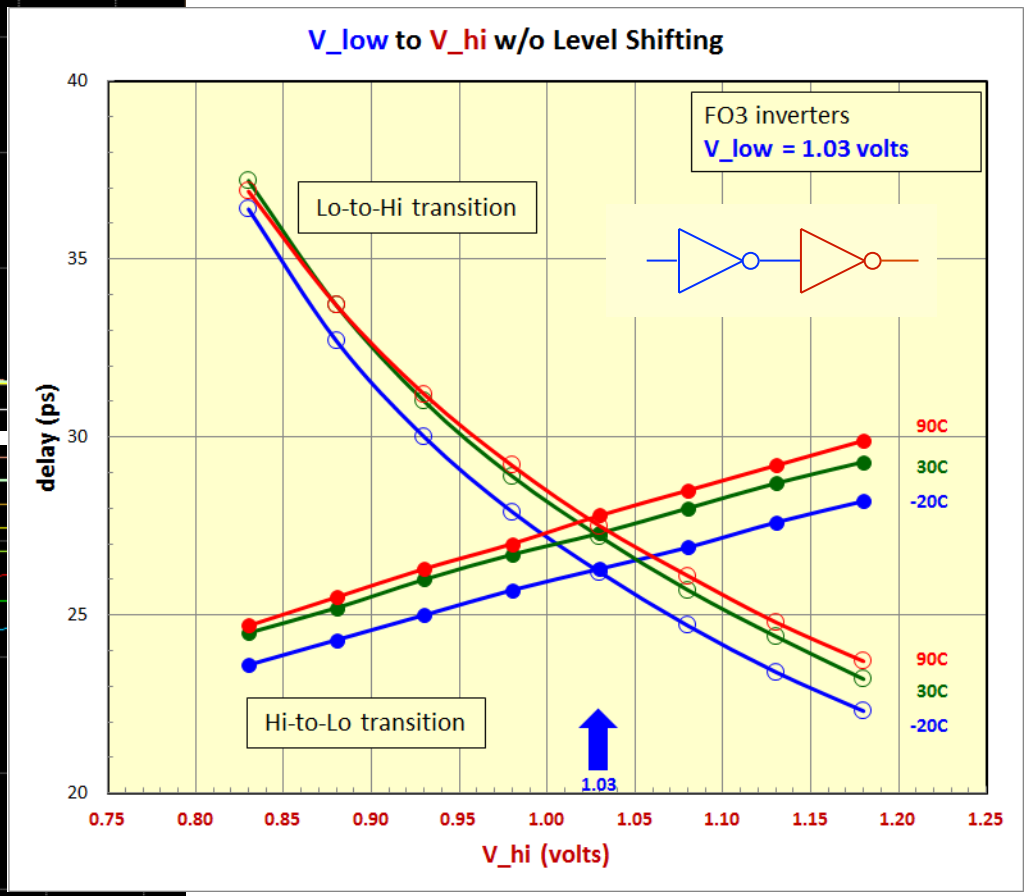
- Will this work? Assume ***V_low = 0.8V*** and ***V_hi = 1.2V***.
- What can you say about inverters A and B, nor-gate C, nand-gate D?
- Even if you can size the gates to work correctly, what can you say about ***V_hi*** power?
- What if ***V_low=1.2V*** and ***V_hi=0.8V***? Is this ok?

NO LEVEL SHIFTER

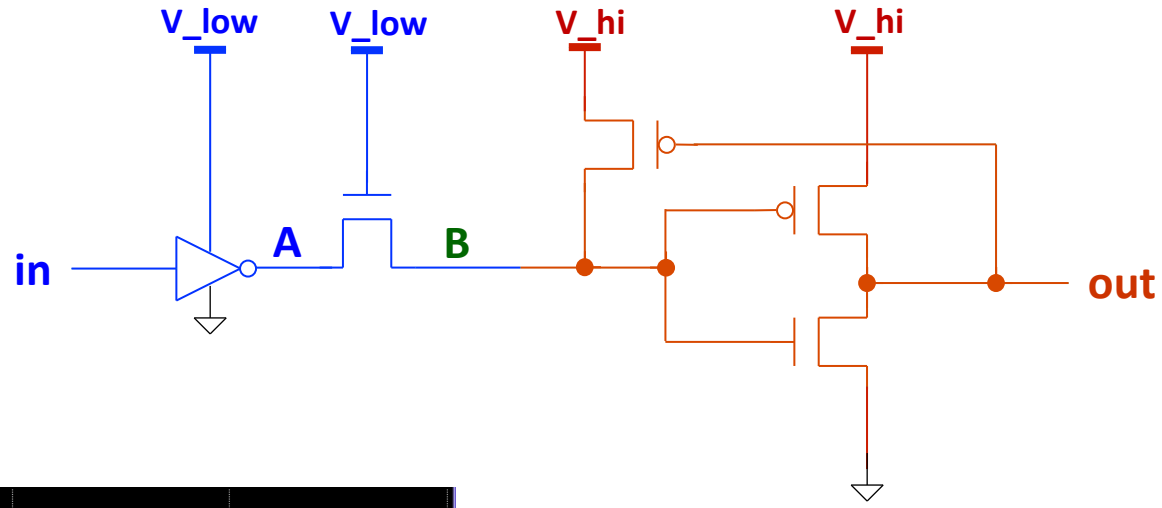
between 2 inverters

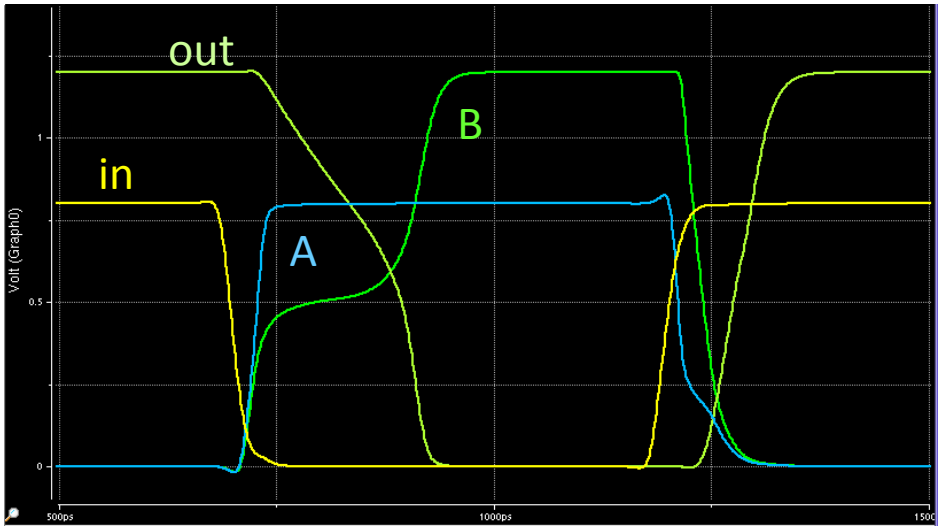






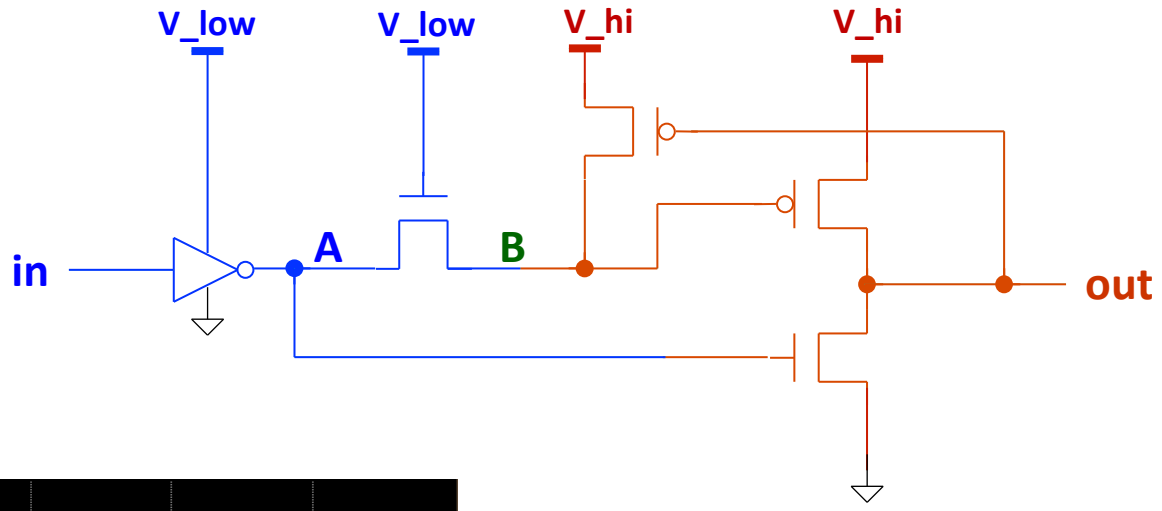
DESIGN #1a

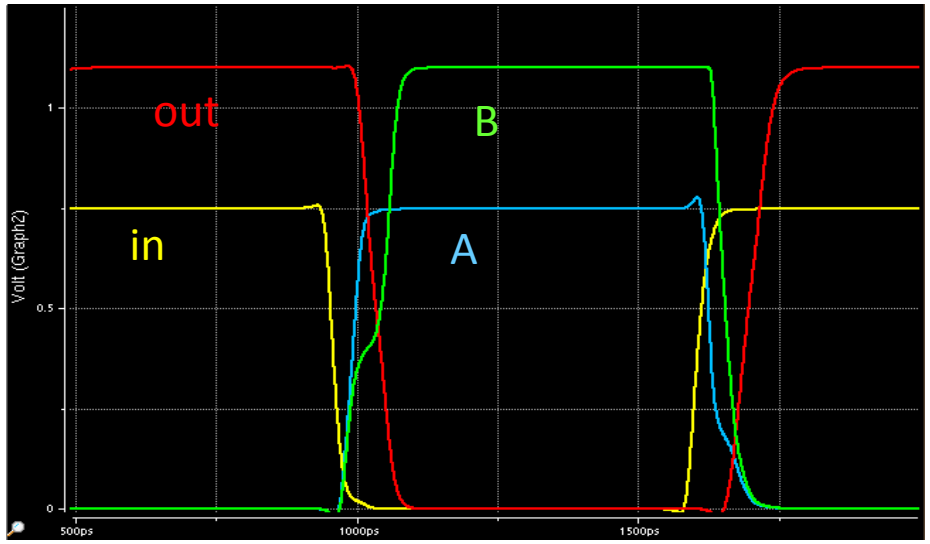




ASSYMETRICAL LATENCY:
Note that the high-to-low delay is higher.

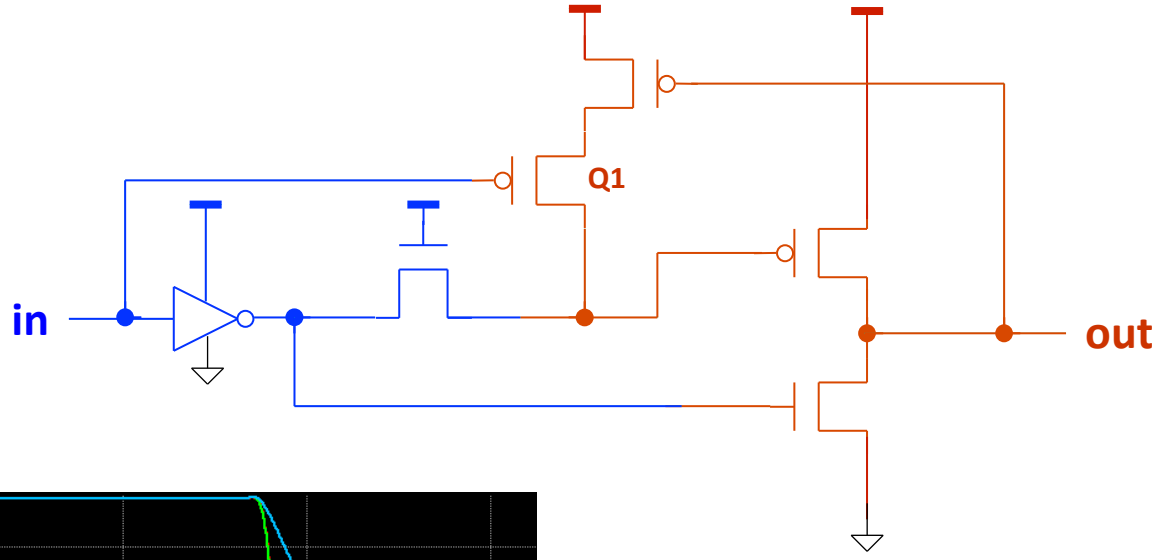
DESIGN #1b

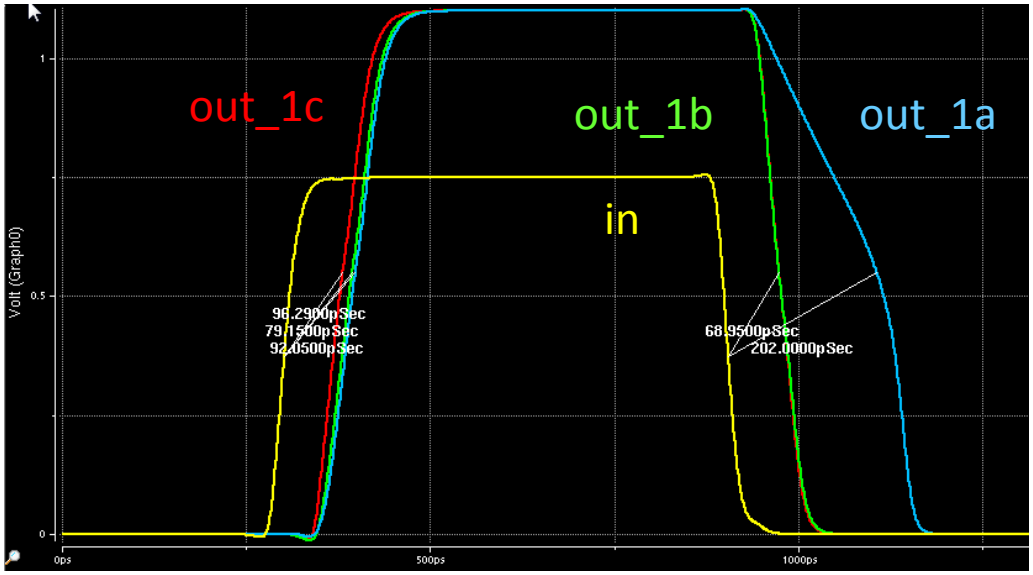




Asymmetrical delay is solved while keeping the delay to 2 inversions.

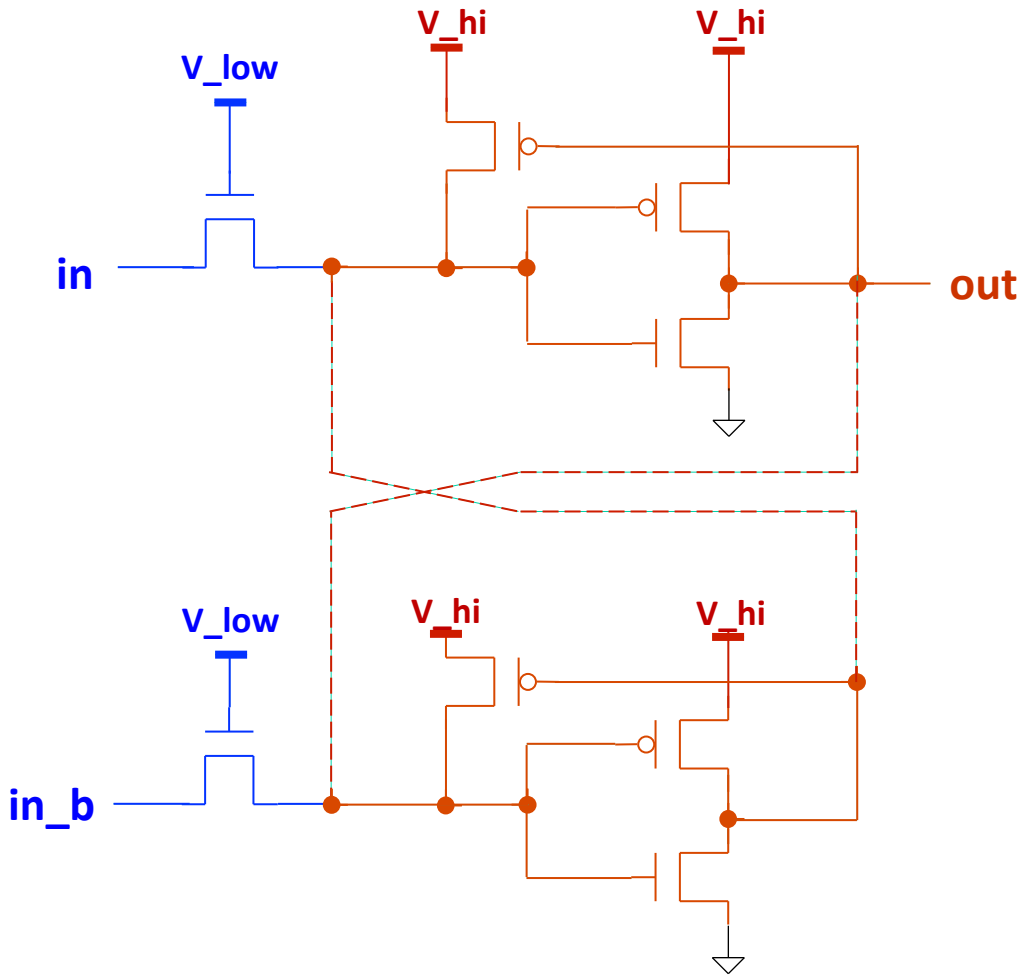
DESIGN #1c



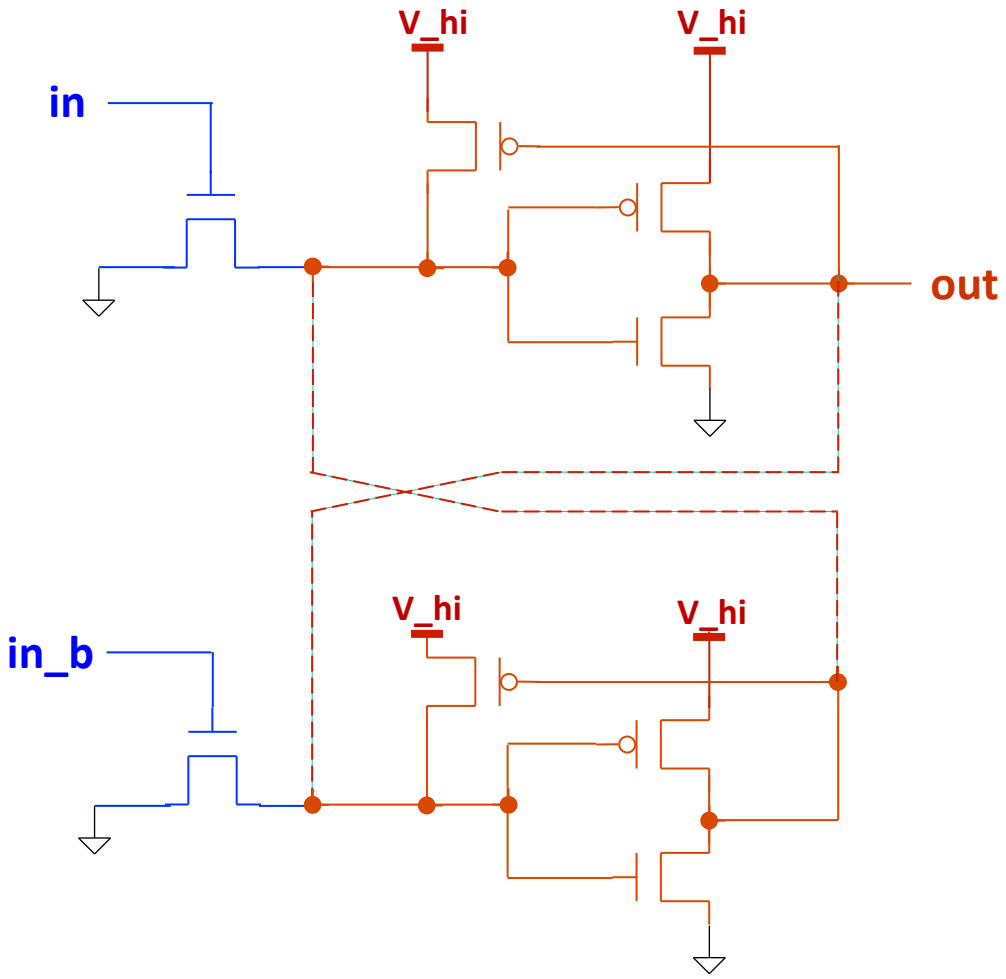


Improves the low-to-high transition by partially turning off Q1.

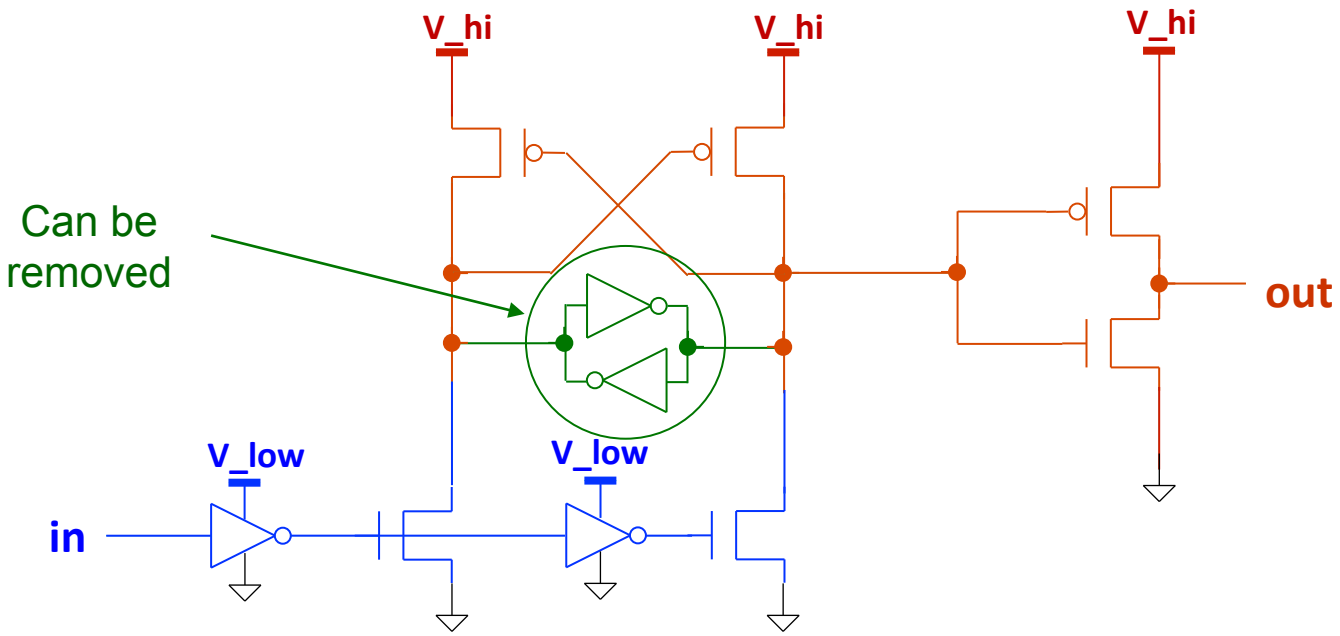
DIFFERENTIAL DESIGNS –part 1-



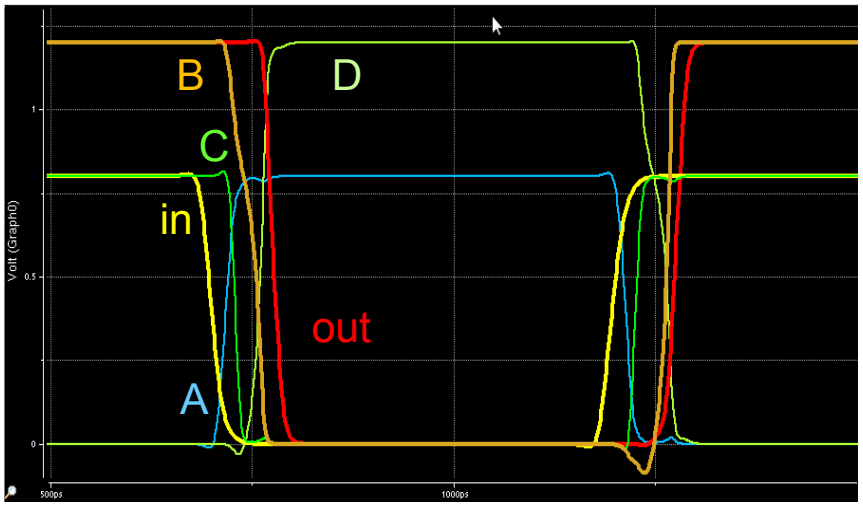
DIFFERENTIAL DESIGN –part 2-

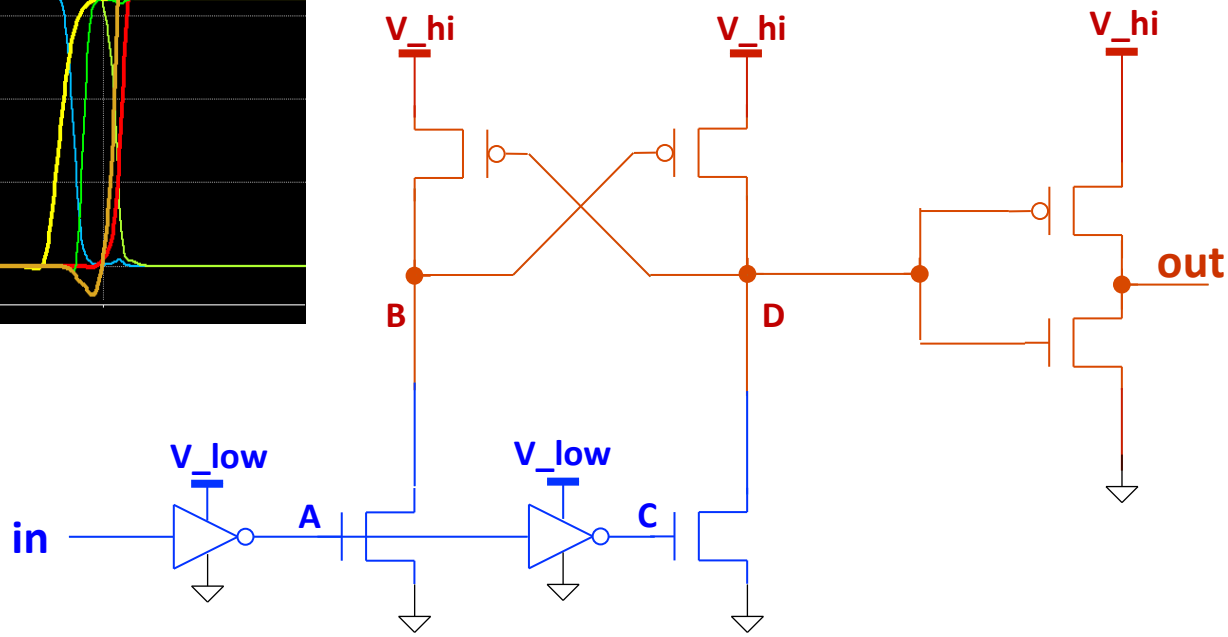


RE-ARRANGING leads to DESIGN #2



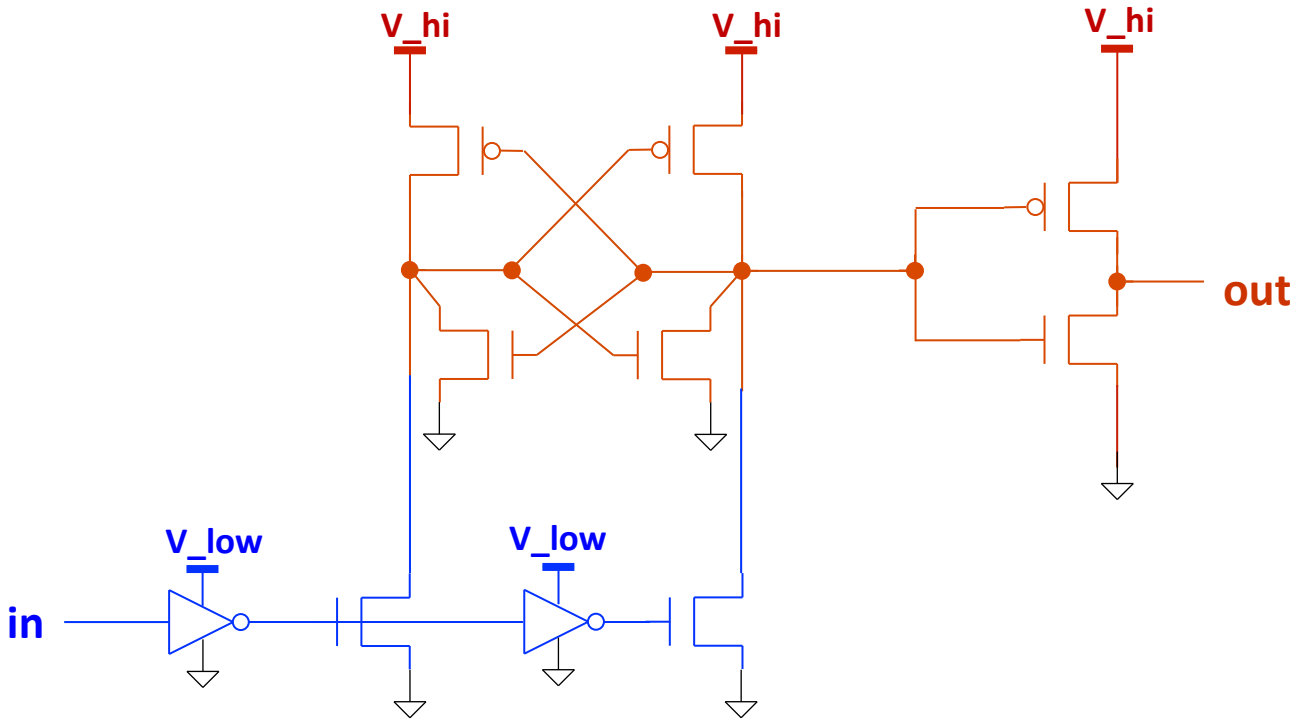
DESIGN #2


B
D
C
in
out
A
Volt (Graph0)
500ps
1000ps

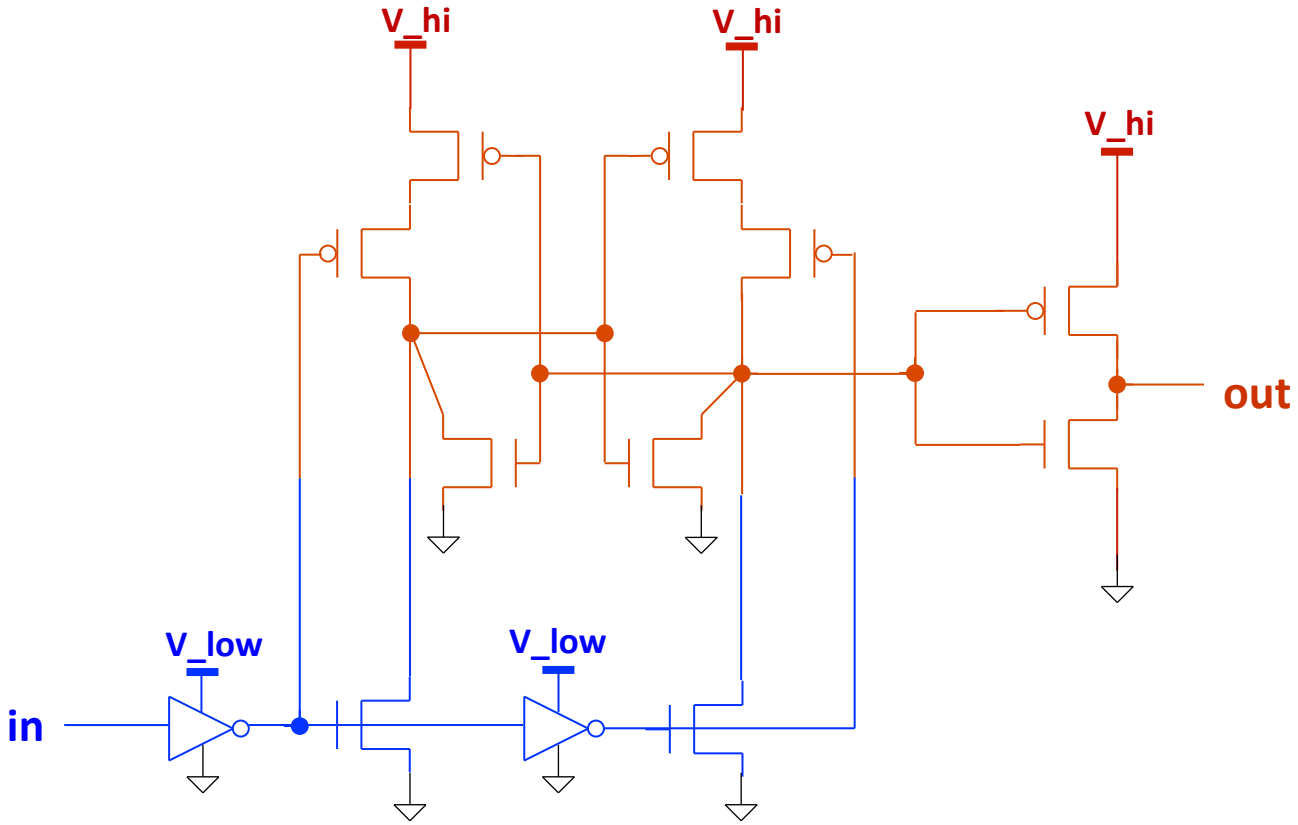

V_hi
V_hi
V_hi
out
B
D
V_low
V_low
in
A
C

DESIGN #3: state is preserved in V_hi

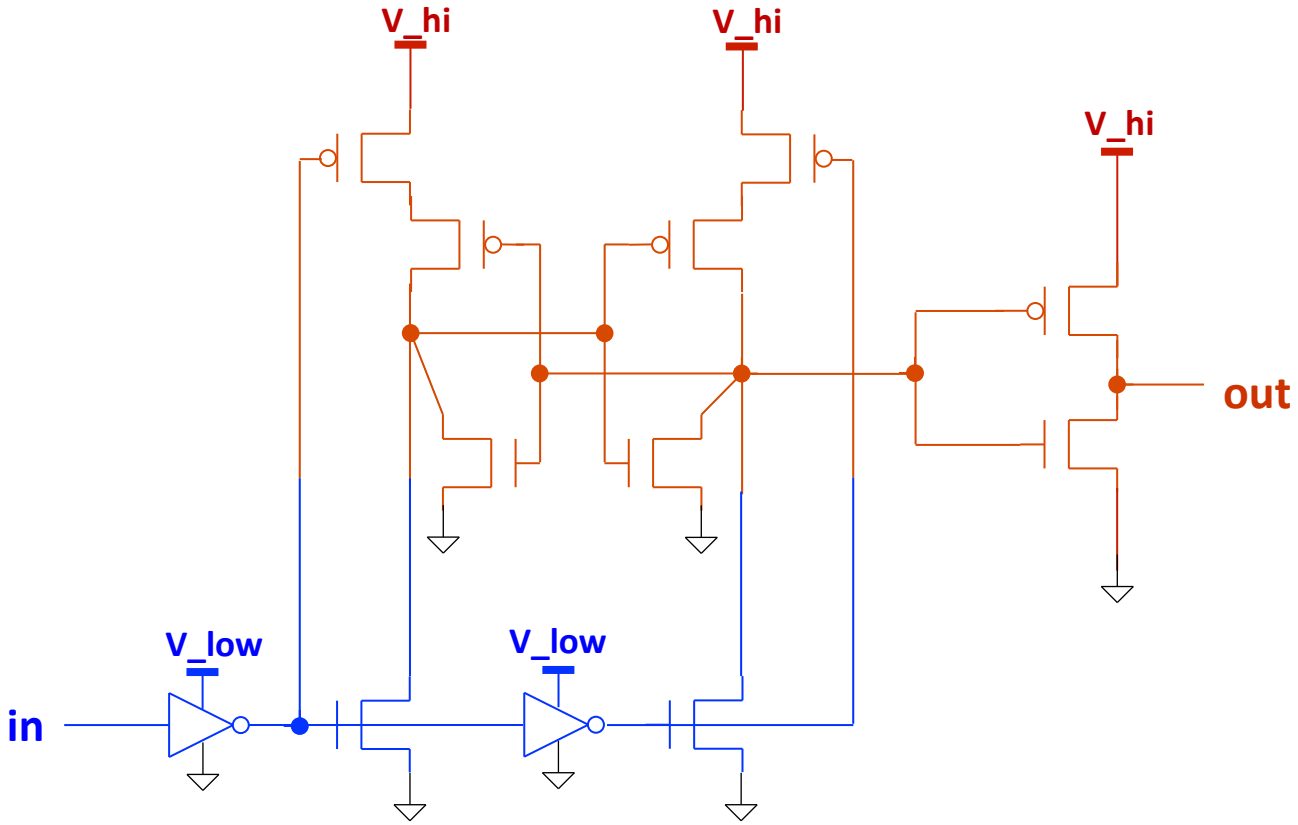
Add full back-to-back inverters for highest NOISE immunity at the expense of increased write-current and time to flip the latch. In addition, if the V-low power is removed, the state is preserved by the V_hi powered latch.



DESIGN #4a: Improving write speed

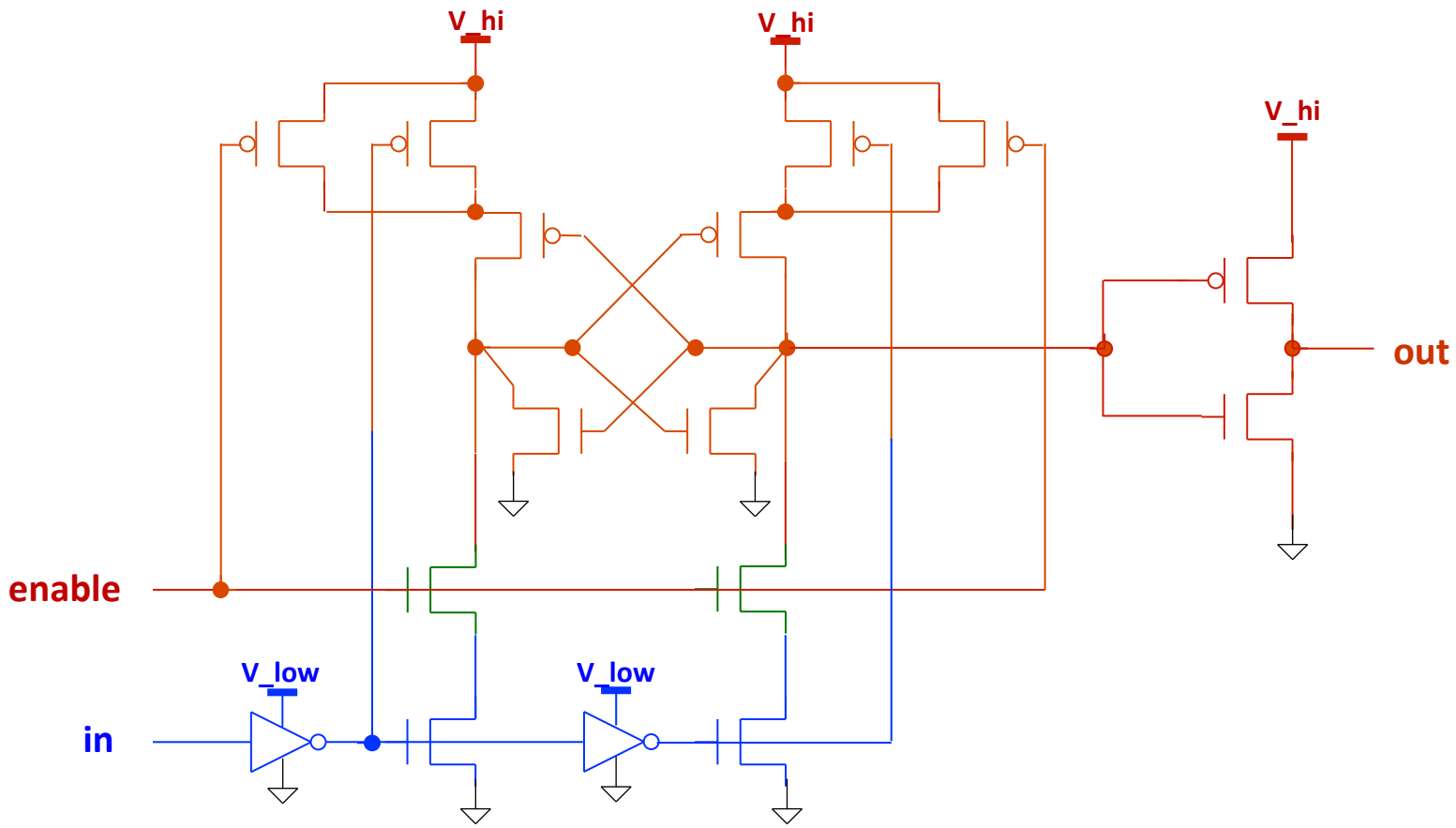


DESIGN #4b: Improving write speed



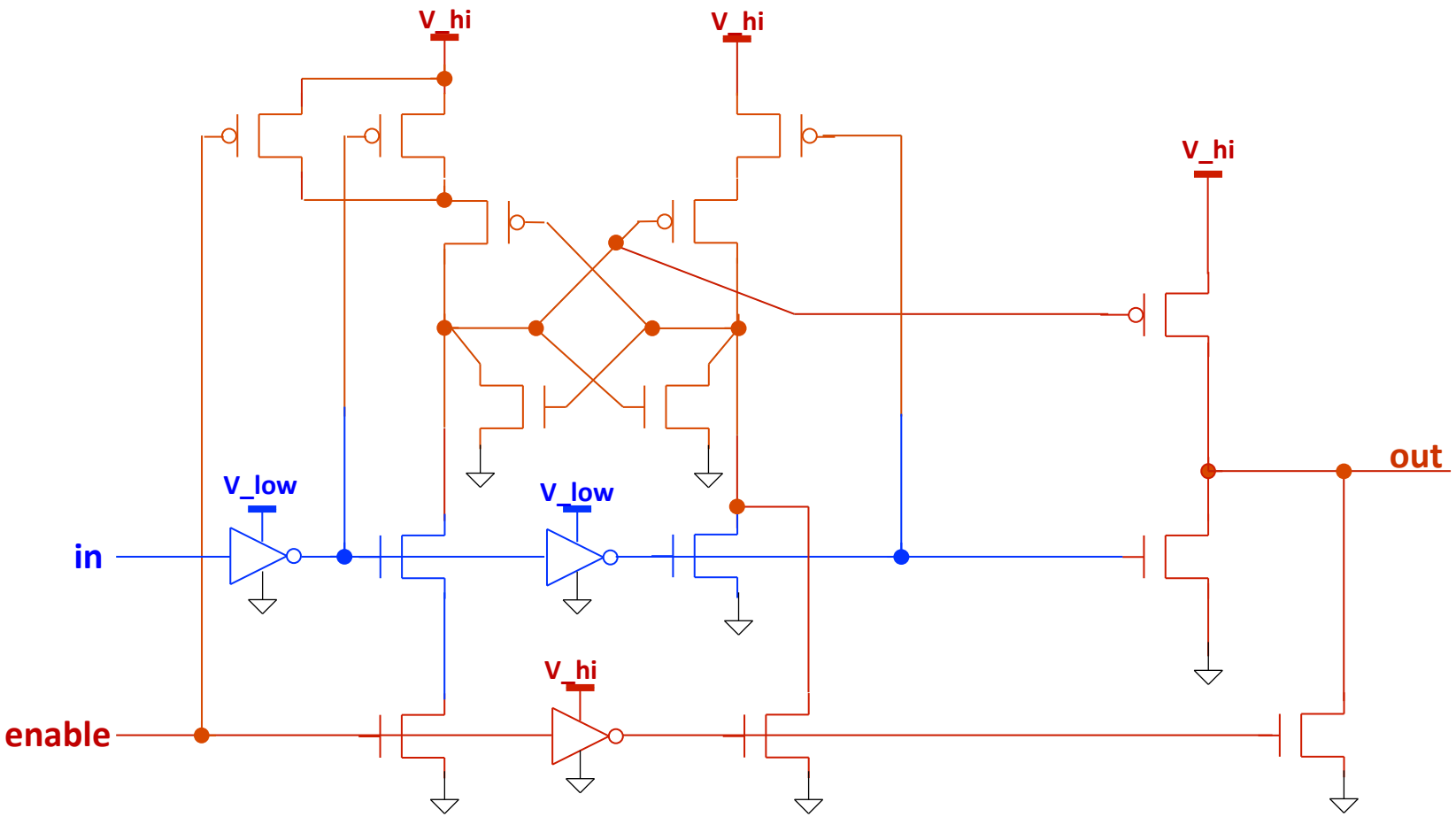
- Is the state stored in the **V_hi** JAM latch preserved if **V_low** is removed?
- Is this a better design compared to #4a?

DESIGN #5: Preserving State



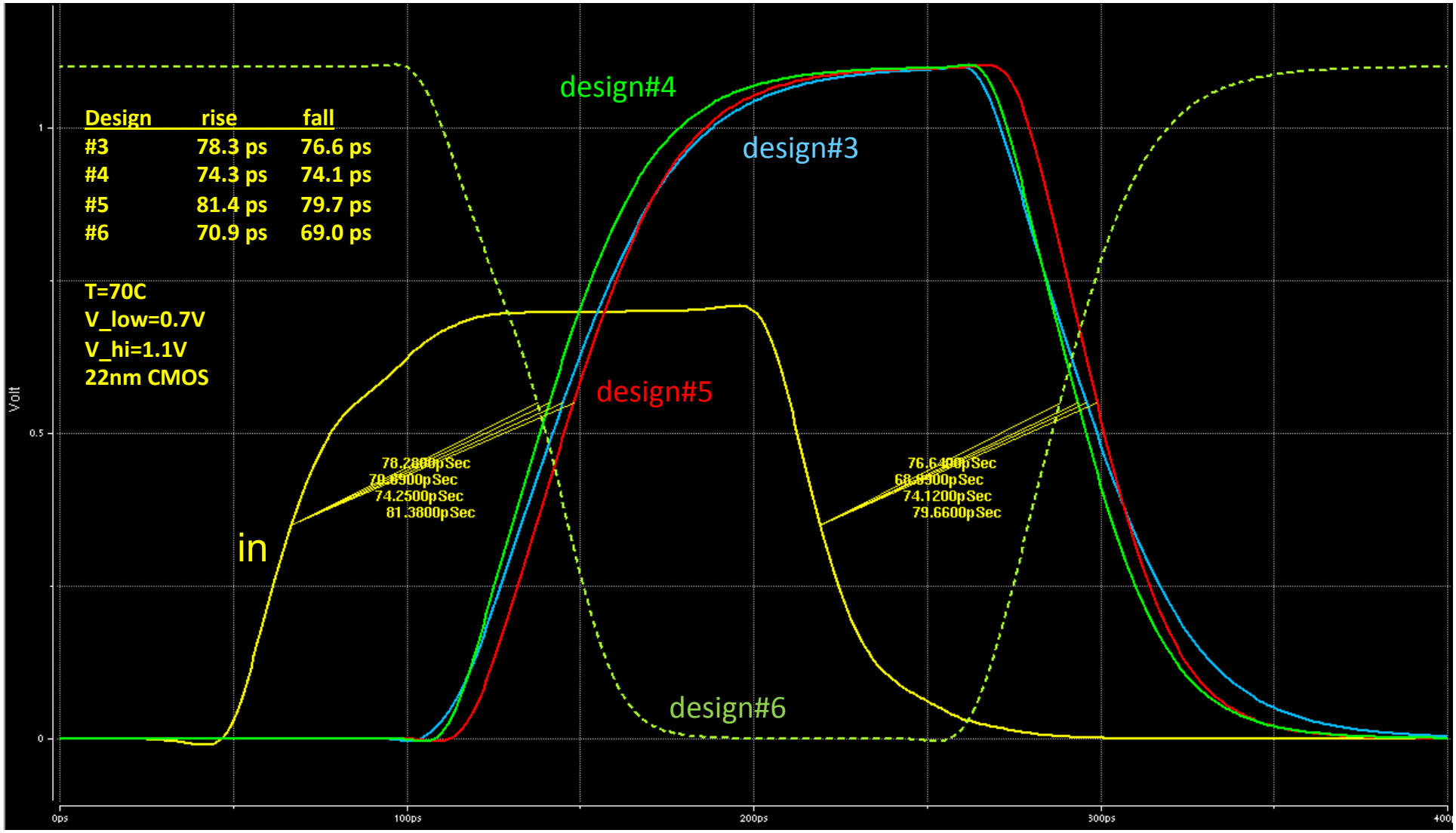
Expect this design to slow down, why?
How can you make this design faster?

DESIGN #6: Preserving State



Guarantees that the output is always a '0' when Level-Shifter is disabled.

Performance Comparison

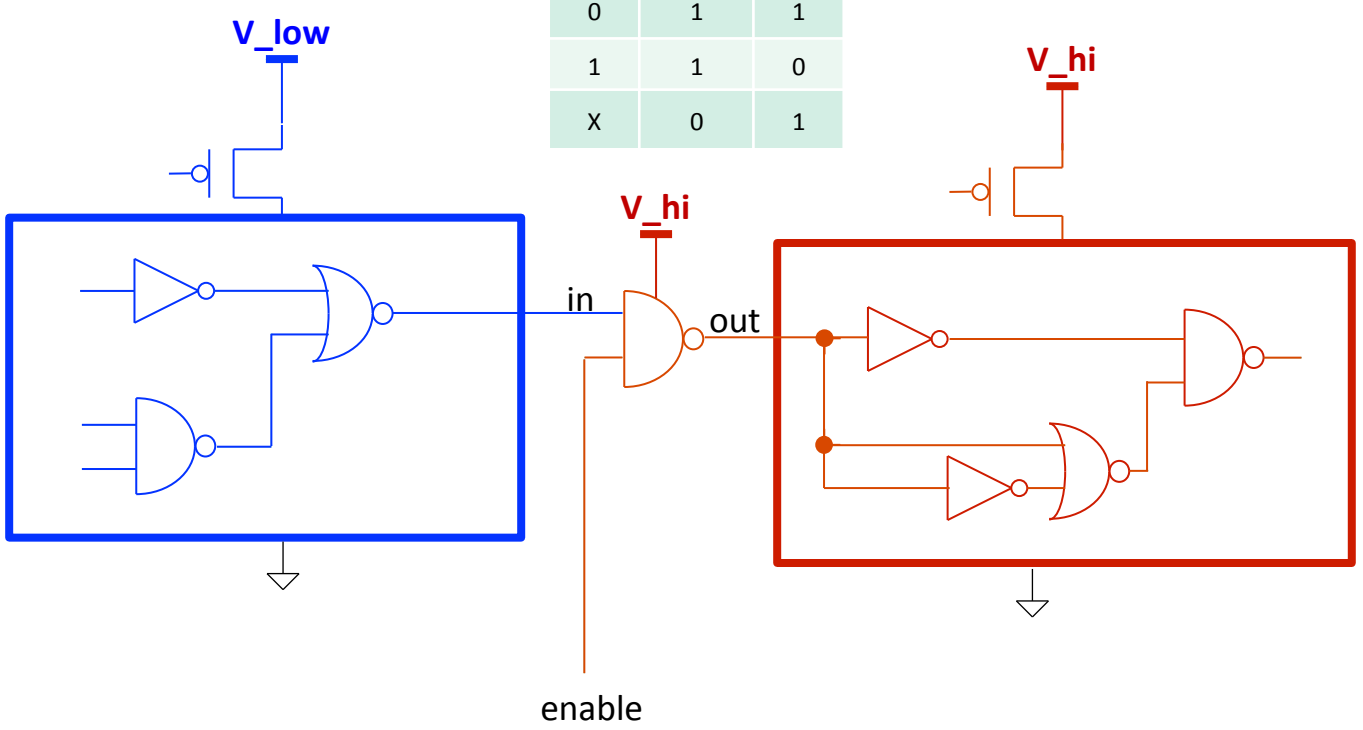


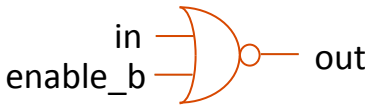
ADDING a FIREWALL

- All prior designs assumed that neither ***V_low*** nor ***V_hi*** are powered down.
- What if ***V_low*** is power-gated and ***V_hi*** remains powered up?
- What happens to the outputs of the ***V_low*** powered (blue) logic?
- Will the state of the ***V_hi*** logic be preserved (even if it remains powered up)?

ADDING a FIREWALL

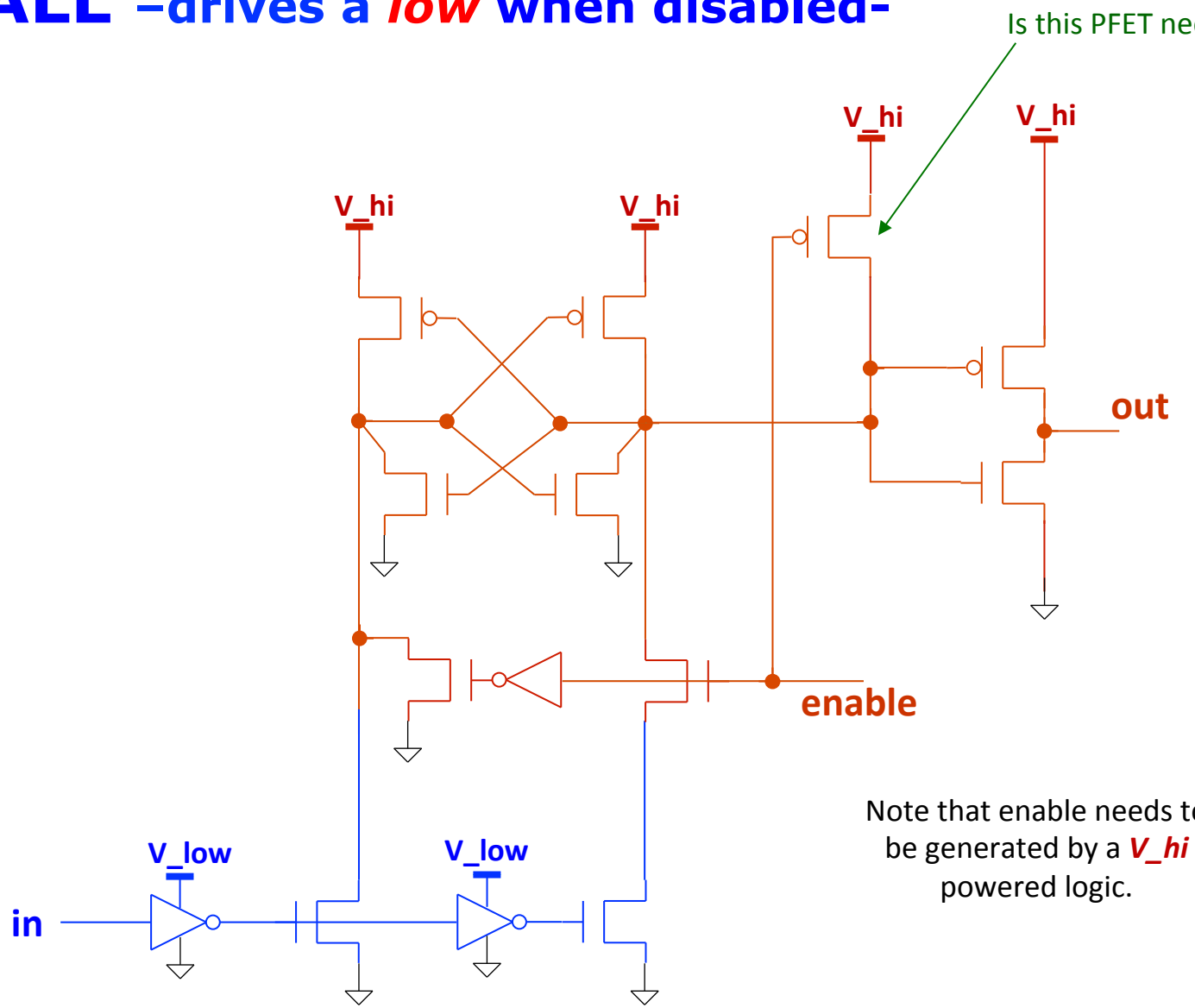
in	enable	out
0	1	1
1	1	0
X	0	1





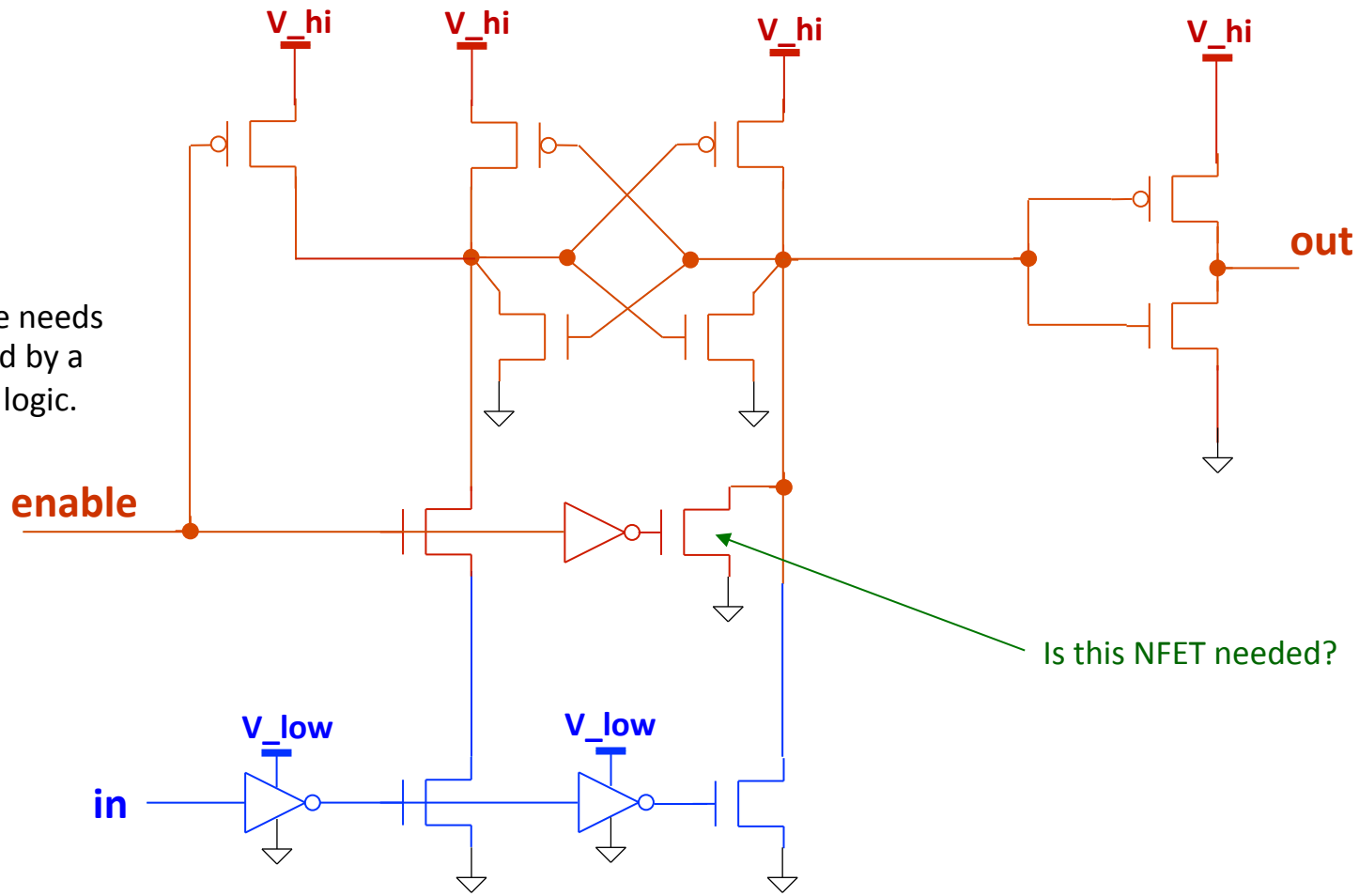
in	enable_b	out
0	0	1
1	0	0
X	1	0

FIREWALL –drives a *low* when disabled-



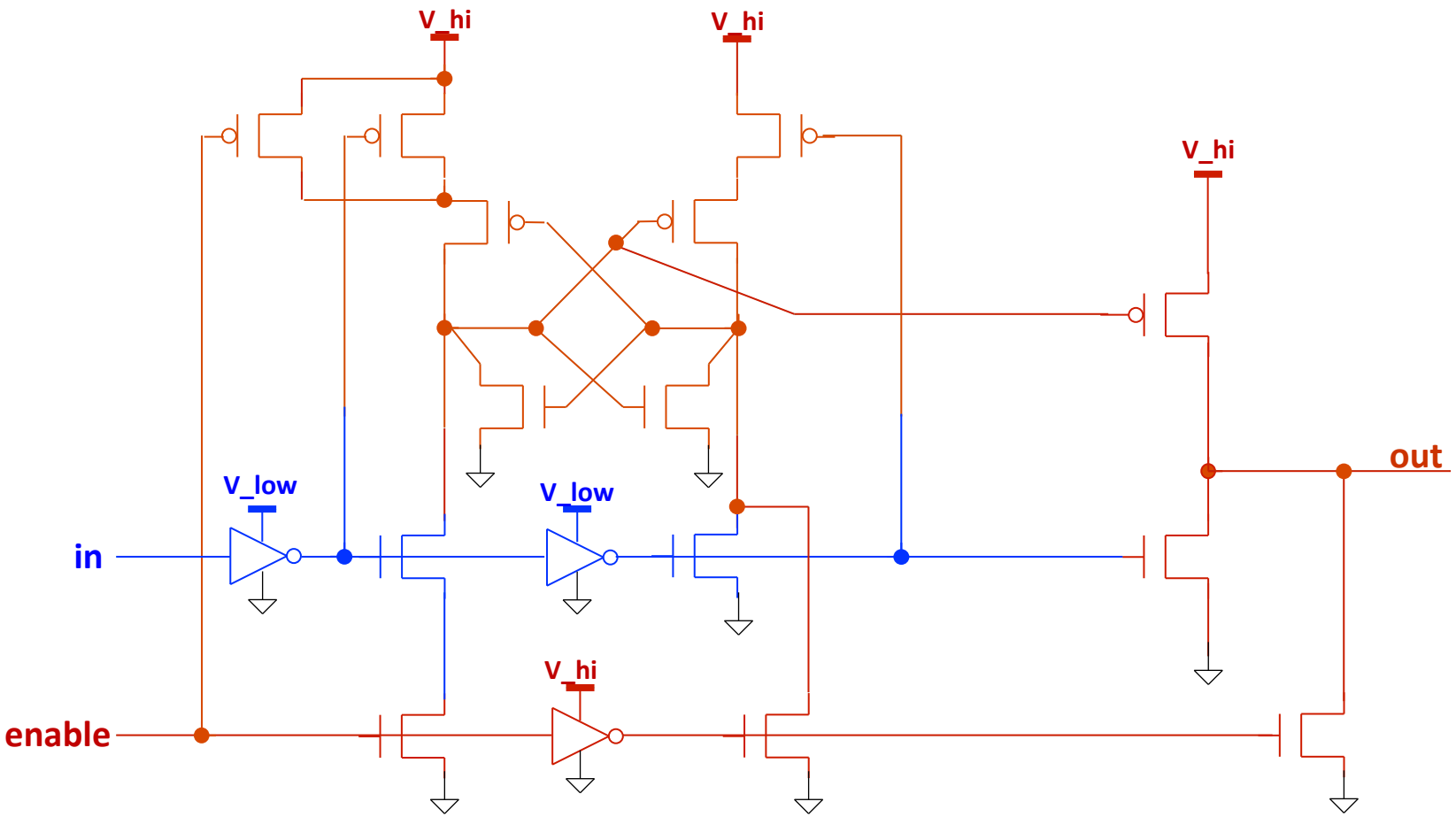
Note that enable needs to be generated by a ***V_hi*** powered logic.

FIREWALL –drives a *high* when disabled-



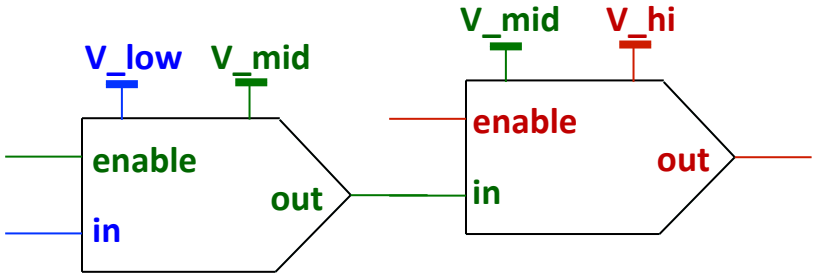
Note that enable needs to be generated by a ***V_hi*** powered logic.

FIREWALL –drives a *low* when disabled-

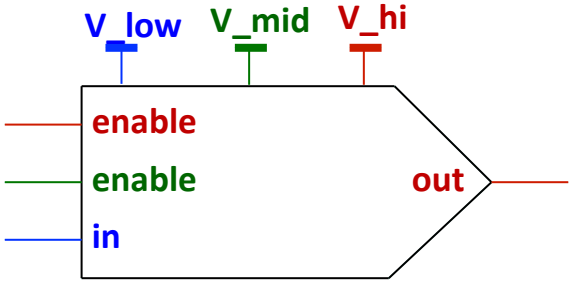


WHAT ABOUT MUCH HIGHER *V_hi* ?

rail	volts
V_low	0.75
V_mid	1.20
V_hi	1.80

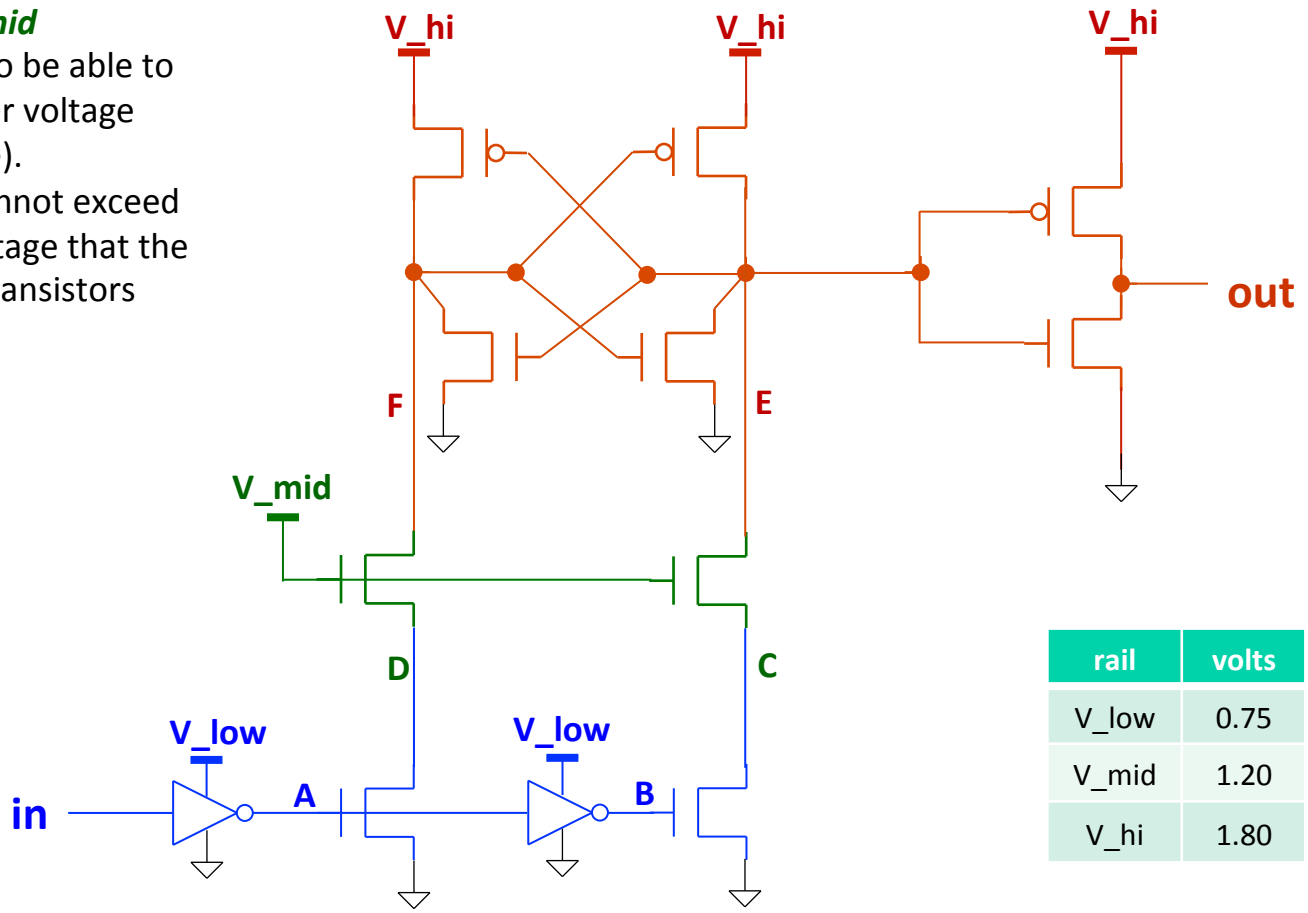


rail	volts
V_low	0.75
V_mid	1.20
V_hi	1.80



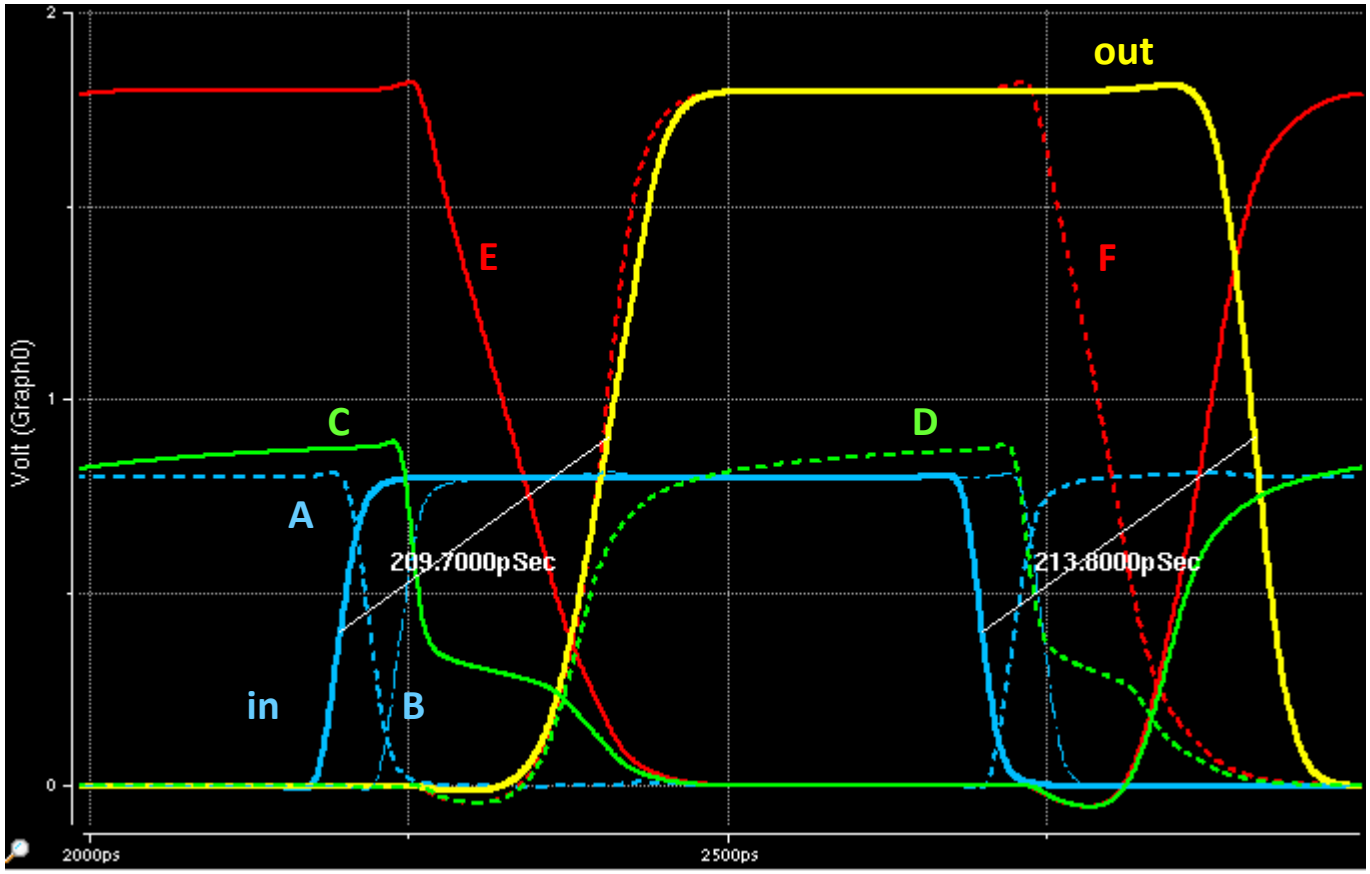
Multi-Stage Design

- The ***V_hi*** and ***V_mid*** transistors need to be able to 'handle' the higher voltage (1.80V in this case).
- Nodes D and C cannot exceed the maximum voltage that the V_low powered transistors can tolerate.

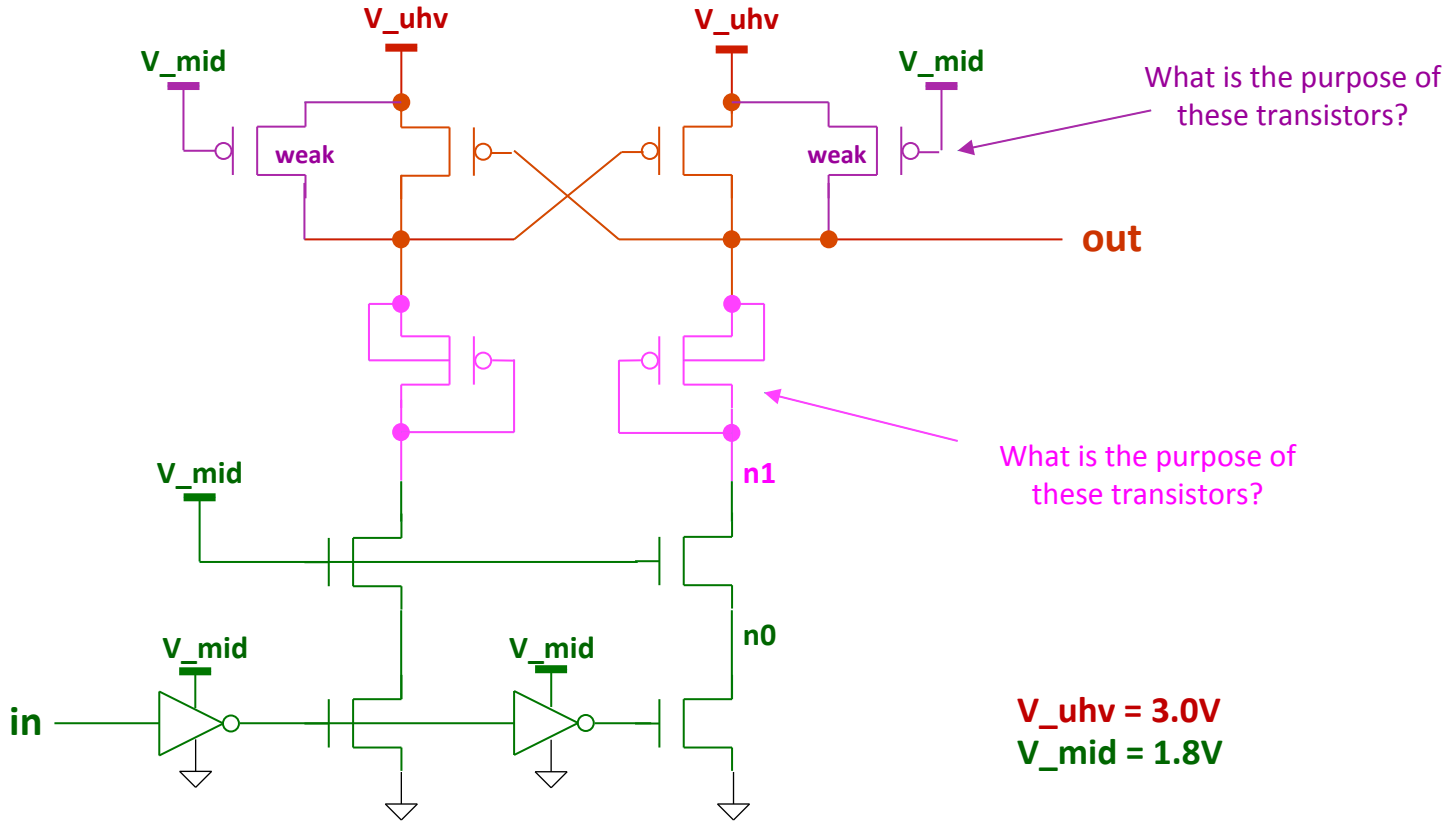


rail	volts
V_low	0.75
V_mid	1.20
V_hi	1.80

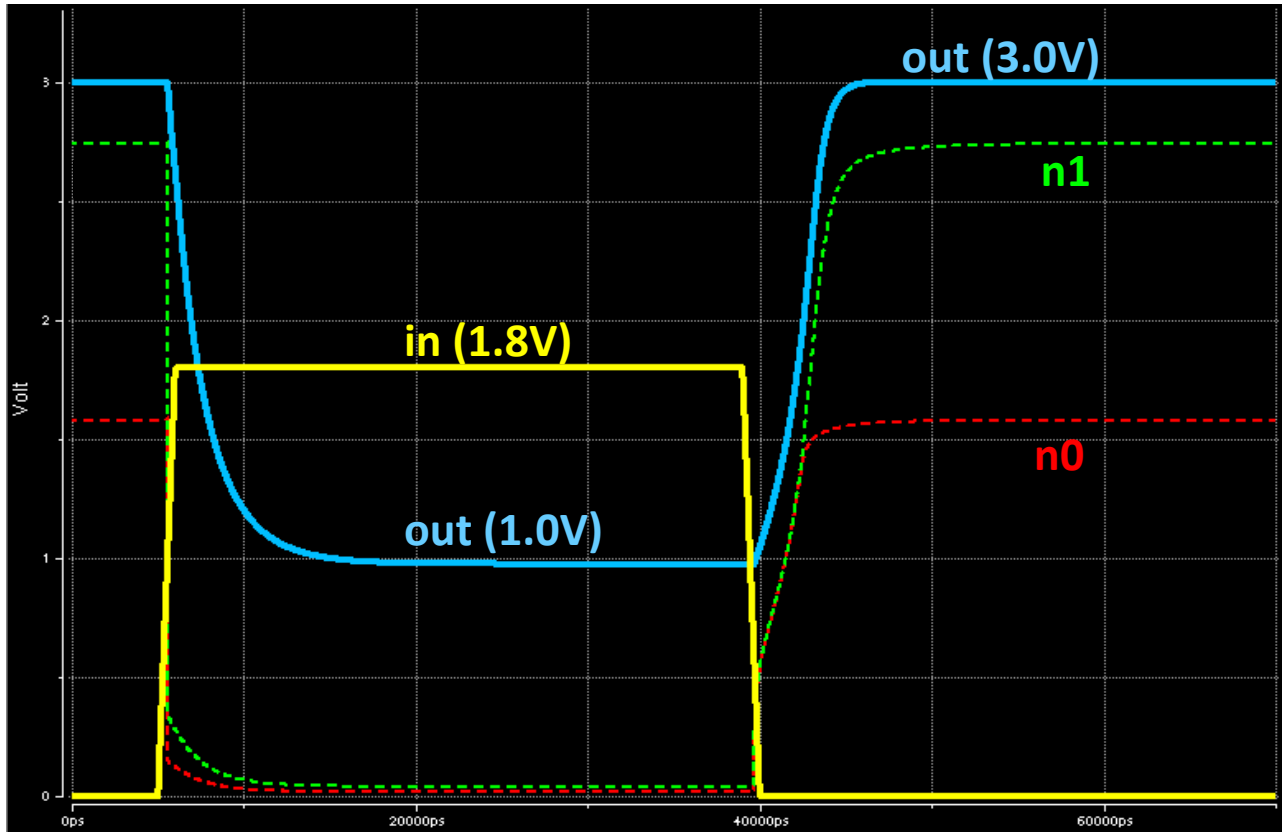
Multi-Stage Level Shifter Performance



What About Supplies Higher Than Vmax?



What About Supplies Higher Than Vmax?



SUMMARY

- Modern day mobile SoC designs contain many functions (CPU, Graphics, Memory controllers, DDR IO, Display controllers, HDMI, MIPI, Video Processing, standard voltage off-chip transceivers, etc.) which are powered by different voltages and may be power-gated to globally optimize battery life.
- Voltage level shifters are used at the IO interfaces of these functional blocks powered by different voltage levels.
- Fire-Walling is required to preserve state of those functional blocks that remain powered-up; short-circuit current reduction needs it as well (blocks X-propagation).
- Reducing level shifter latency is critical for high performance circuits.

REFERENCES

1. Rumi Zahir, 'Medfield Smartphone SoC Intel Atom Z2460 Processor', HOT CHIPS #24, August 2012.
2. Kerry Bernstein et. al., 'High Speed CMOS Design Styles', Kluwer Academic Publishers, 1999, pp. 230-233.
3. Chandrakasan, Bowhill, Fox, 'Design of High Performance Microprocessor Circuits', IEEE Press. P. 384.
4. S.H. Kulkarni and D. Sylvester, 'Fast and Energy-Efficient Asynchronous Level Converters for Multi-VDD Design', IEEE SoC Conference, 2003, pp. 169-172.
5. S. Hsu, A. Agarwal, M. Anders, S. Mathew, H. Kaul, F. Sheikh, R. Krishnamurthy, "A 280mV-to-1.1V 256b reconfigurable SIMD vector permutation engine with 2-dimensional shuffle in 22nm CMOS," 2012 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), pp.178-180, 19-23 Feb. 2012.