EE 382M
VLSI–II: Advanced Circuit Design
Noise Analysis

2017

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Outline

- General Remarks
  - Timing Failures vs. Noise Failures
  - Fixing Noise Failures
  - Noise Analysis
- Circuit Sensitivity
- Cross Talk Noise
- Power Supply Noise
- Summary

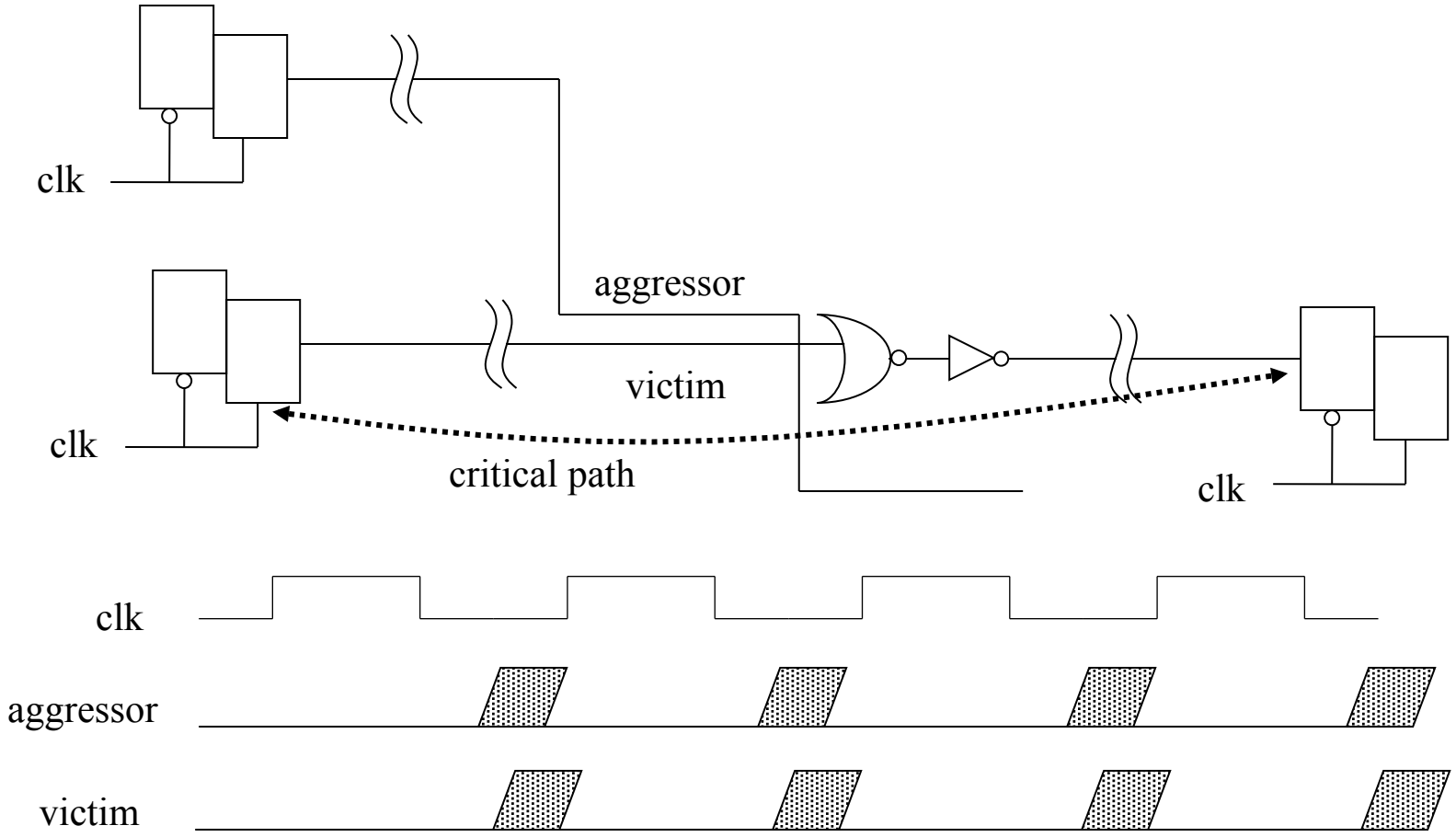
Timing & Noise Failures

- **Timing Failures**
  - Occur when noise impacts a long path delay
    - Noise is injected on switching nets & circuits
  - Hardware functions correctly with a slower clock
  - Design changes required to achieve highest clock rates, but chip will operate at slower frequency

- **Noise failures**
  - Occur when noise disrupts a quiet logic state
    - Injected noise arrives at latch when latch is sampled
    - Some failures resolve with slower clock
    - Some failures are independent of clock rate
    - Some failures brought on at slower clock rates
    - Some failures change with voltage & temperature
  - Design changes are required to achieve any functionality

Timing Failure Example

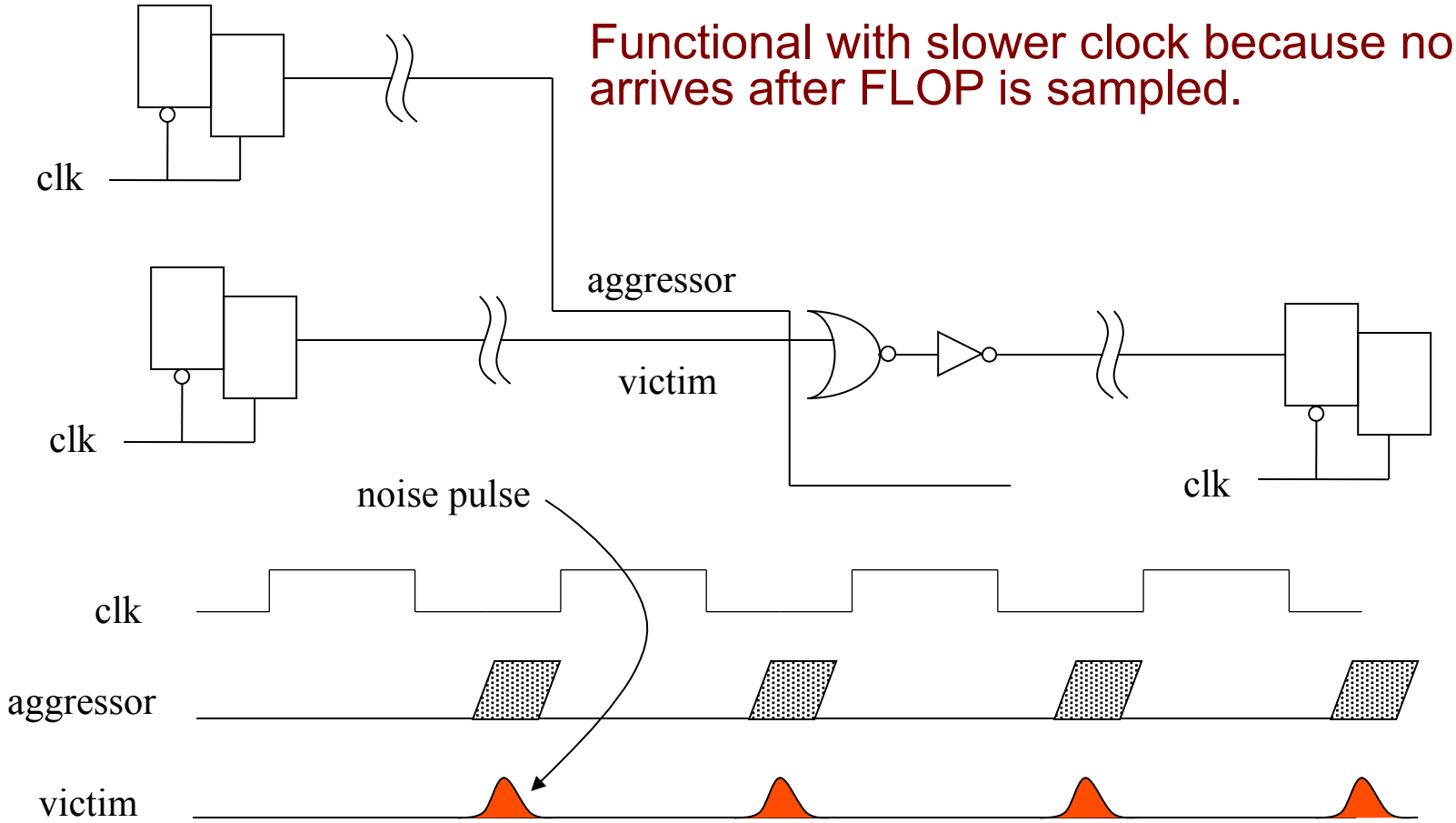
Aggressor & victim switch simultaneously (in opposite directions) & victim net can be a critical path!



Noise Failure Example I

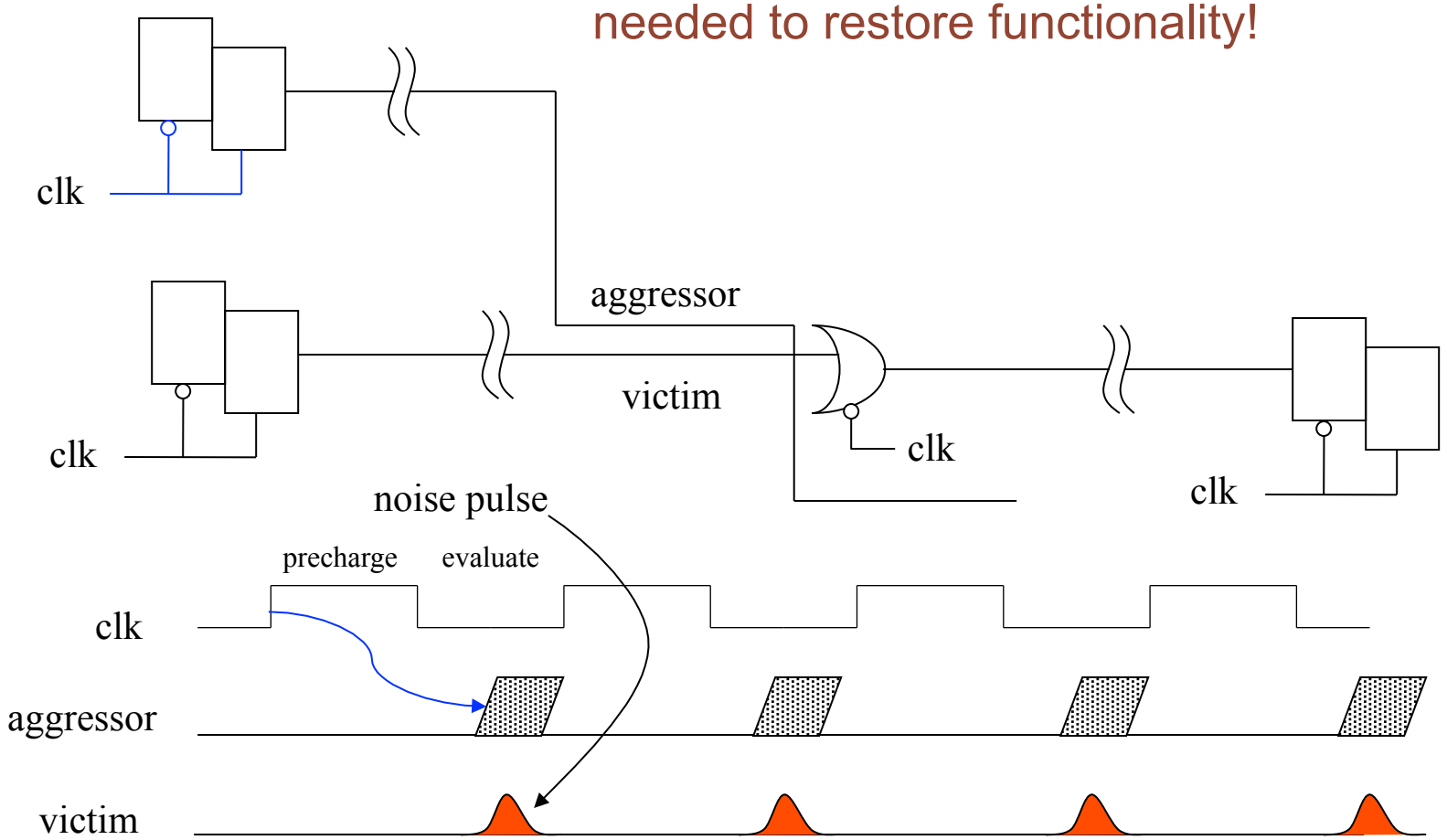
Victim net is not in critical path but late aggressor noise pulse propagates down the victim net & arrives at FLOP at sampling time.

Functional with slower clock because noise arrives after FLOP is sampled.



Noise Failure Example II

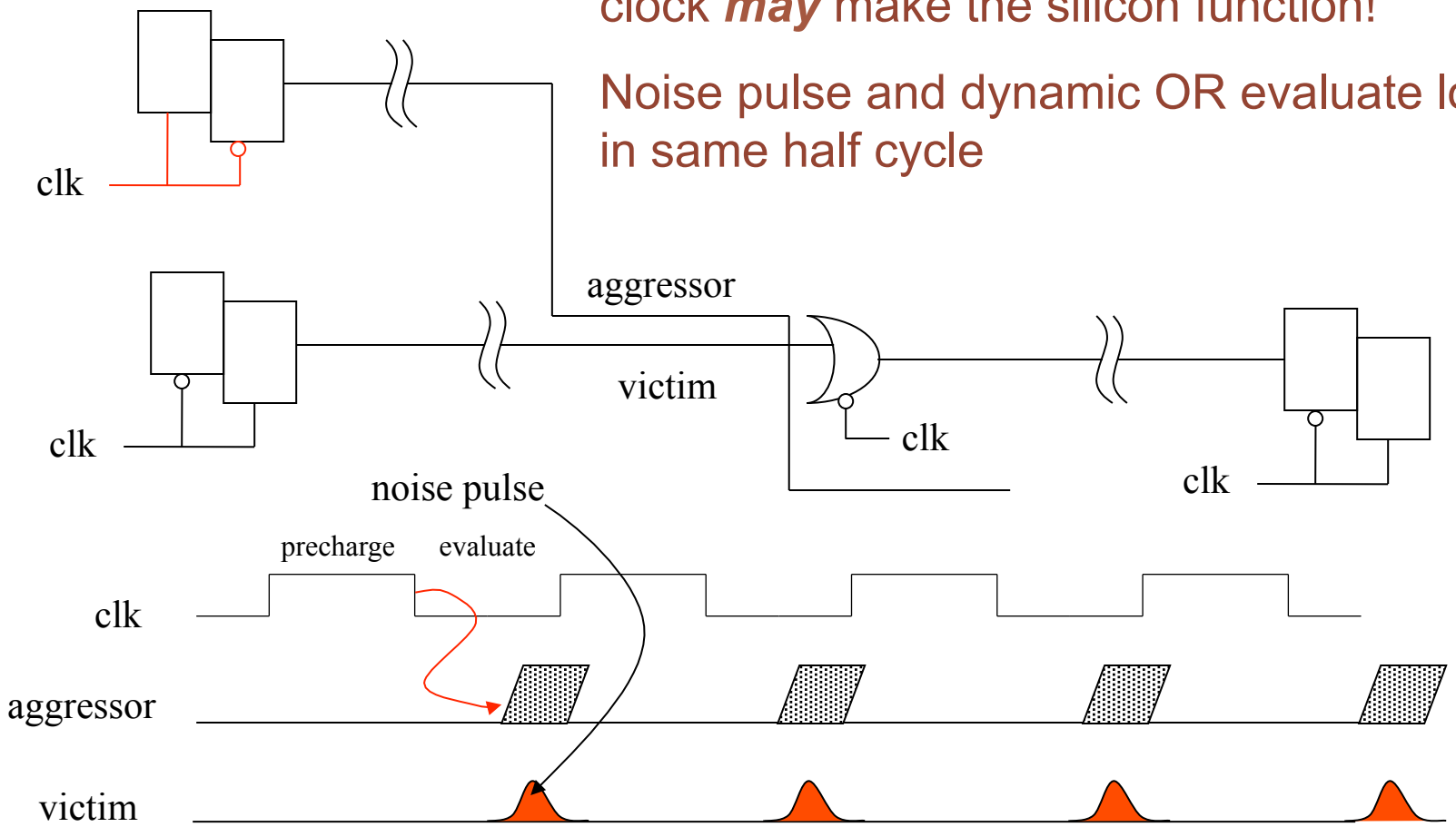
If OR gate is a dynamic circuit that evaluates when clk=0, then a much slower clock is needed to restore functionality!



Noise Failure Example III

If dynamic OR gate evaluates and aggressor launches on same clock phase, a much slower clock ***may*** make the silicon function!

Noise pulse and dynamic OR evaluate locked in same half cycle



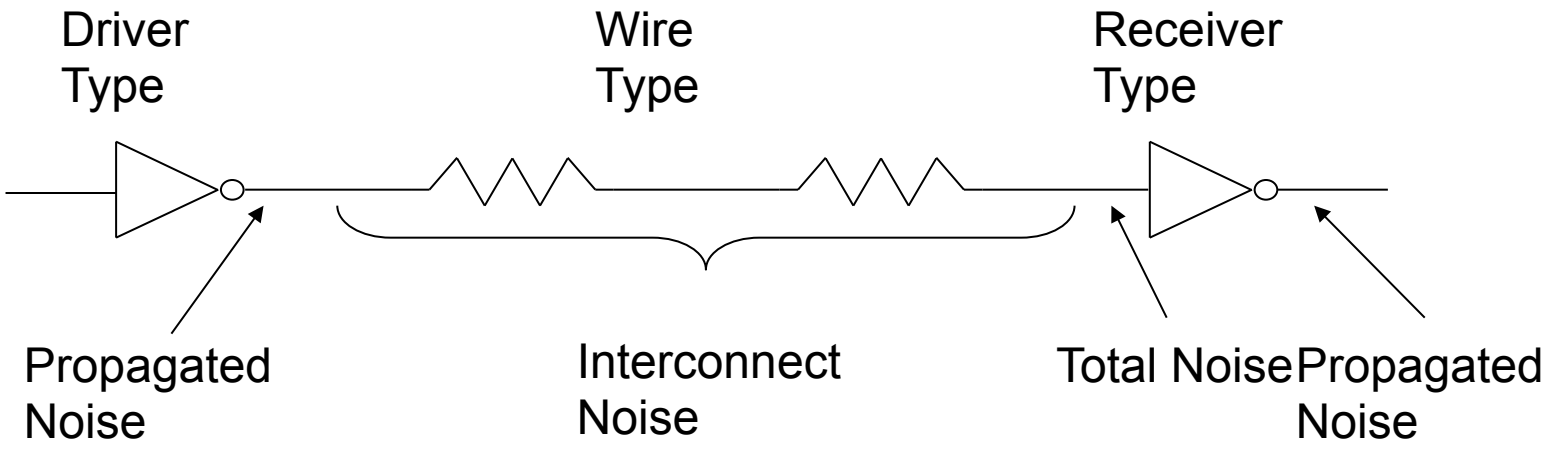
Fixing Noise Failures

- **Reduce noise level below circuit noise sensitivity**
  - Changes might include:
    - Wiring changes
    - Power distribution changes
    - Clock or Power gating settings
    - Aggressor circuit or keeper circuit changes
    - Clock or timing changes
  - Invariably costs additional design resource
- **Decrease circuit noise susceptibility**
  - Involves some type of circuit change
    - Dynamic to static
    - Different p/n ratio
    - Hysteresis feedback loops
    - Larger keeper devices on domino gates
  - Invariably trades speed for increased noise immunity

Noise Analysis

Noise is typically analyzed as individual driver-receiver pairs.

Accounts for both noise generation and noise reception!

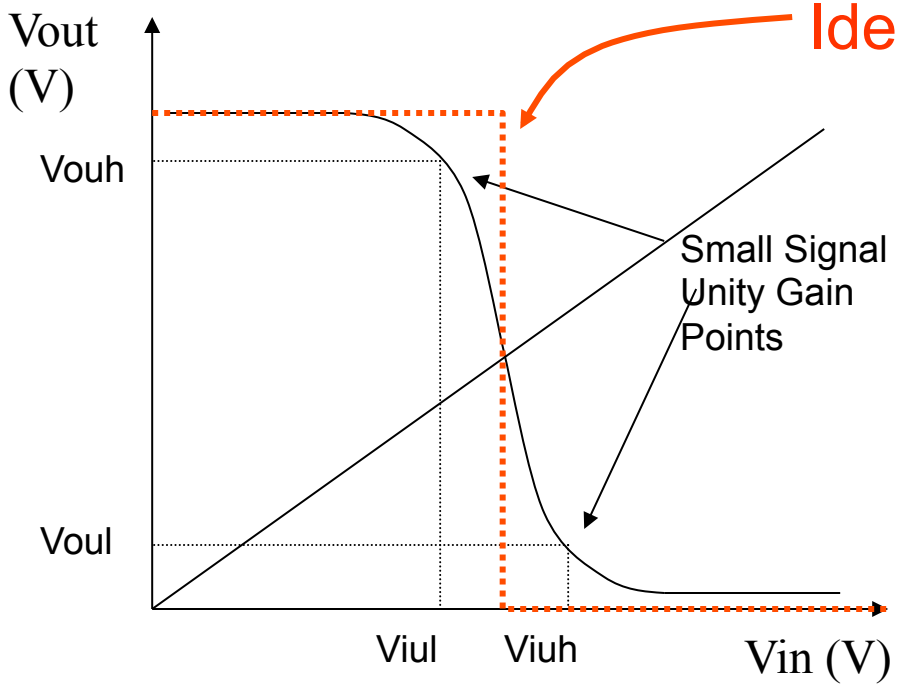


A budget for total noise prevents failure at this receiver.

A budget for propagated noise prevents failure at the next receiver.

Circuit Sensitivity

Circuit Noise Margins



A gate's noise margins are formally defined by the unity gain points of its transfer curve.

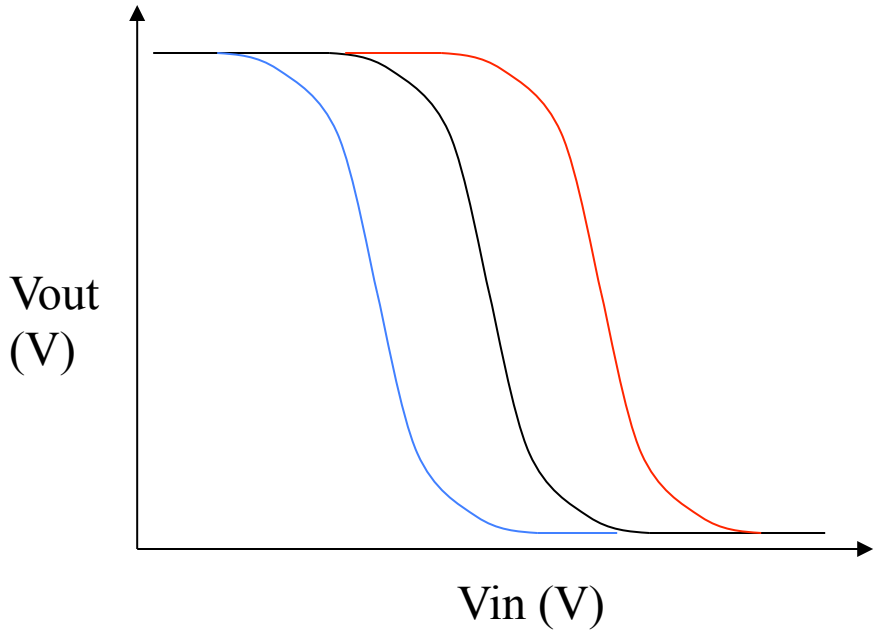
UNM(h) = Vouh - Viuh

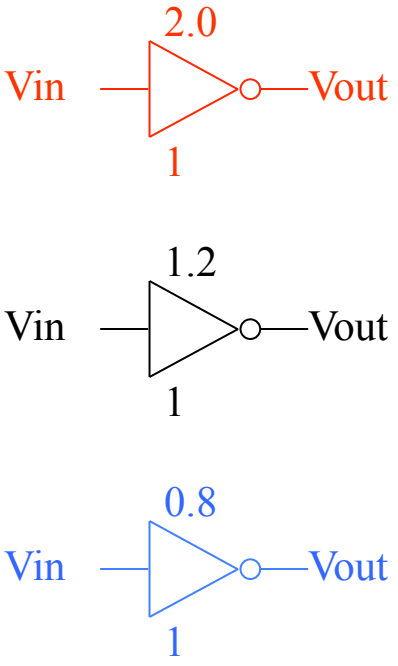
UNM(l) = Viul - Voul

The unity gain noise margins are the maximum amounts of DC noise which can be added to every node.

DC measurements of noise and noise margins tend to be overly conservative.

Adjust P/N Ratio of Receiver

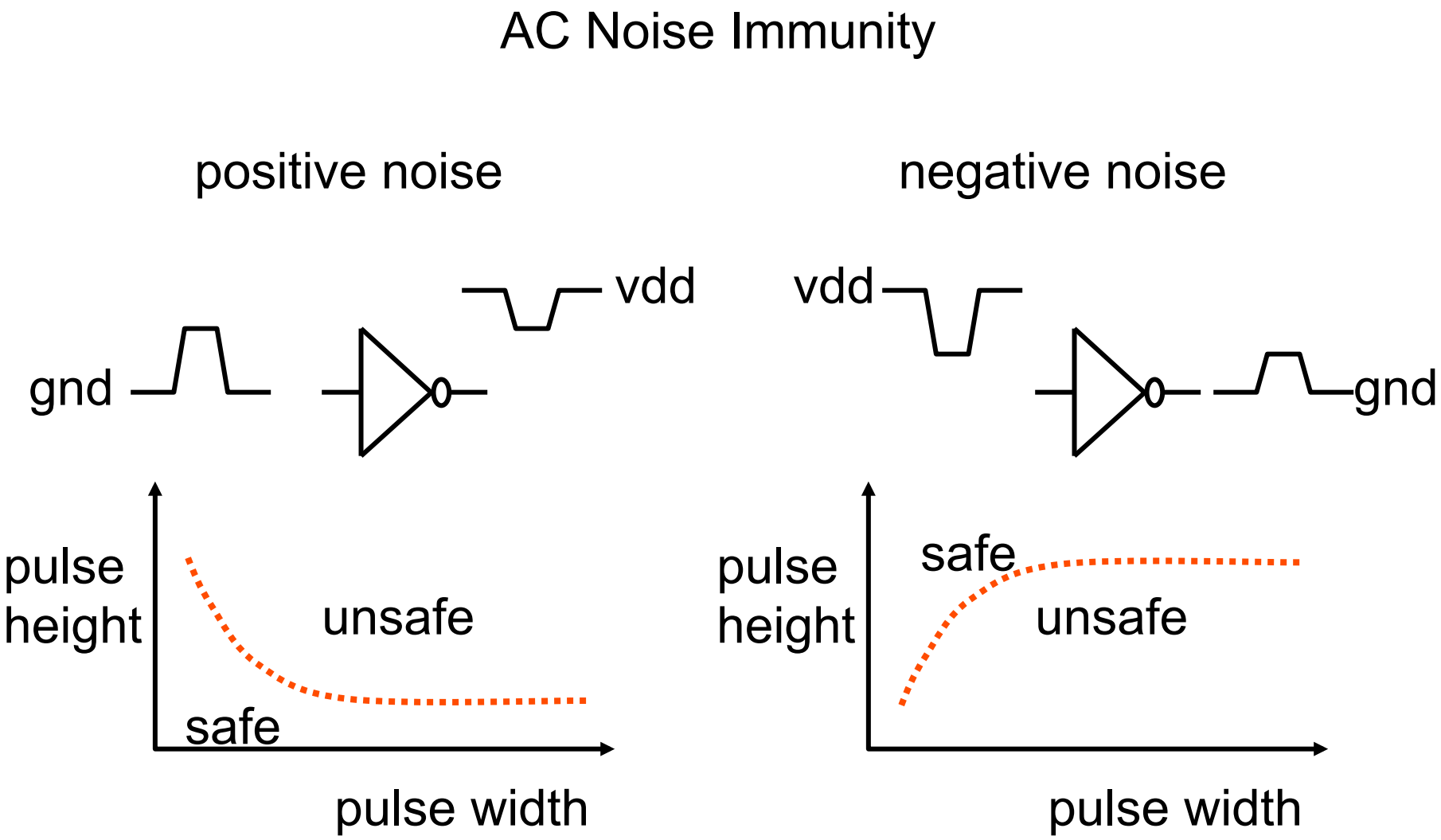




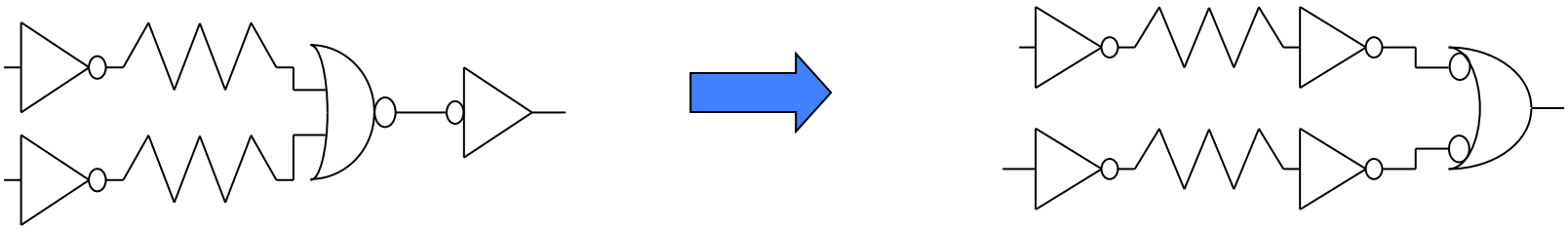
Changing the P/N ratio of a receiver can greatly affect its sensitivity to noise.

Con: May slow critical transition

Circuit Noise Margins



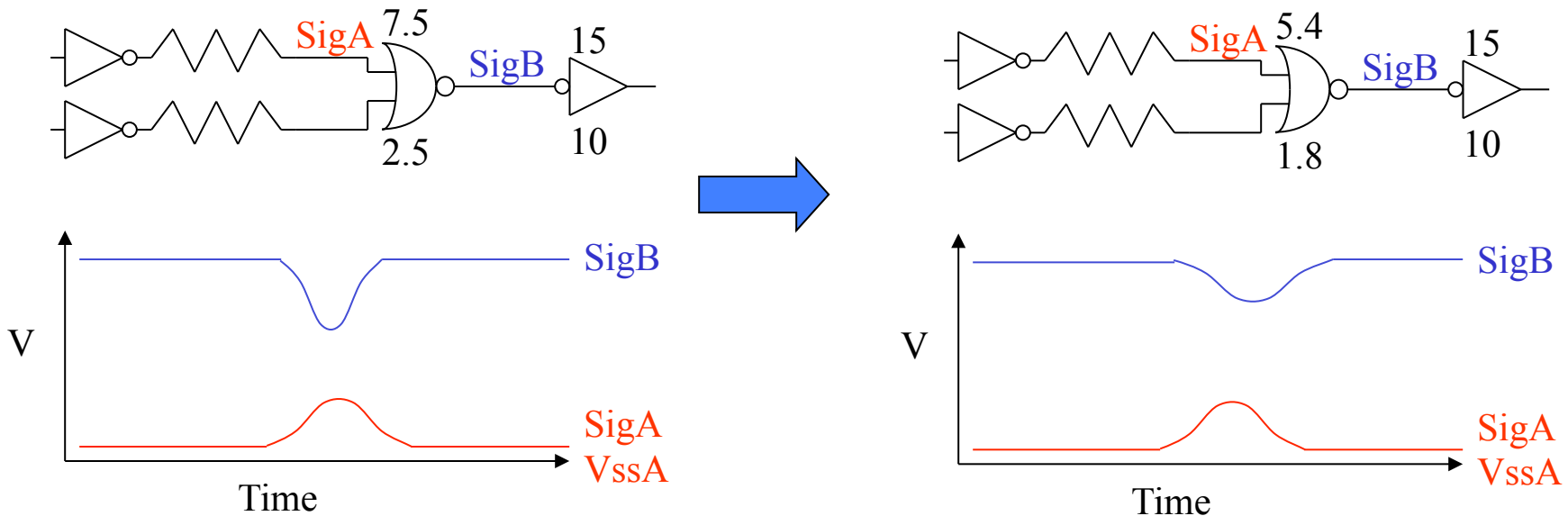
Lower Fan-In of Receiver



Low fan-in gates after noisy nodes will attenuate noise before sensitive receivers are reached.

Con: Can increase delay

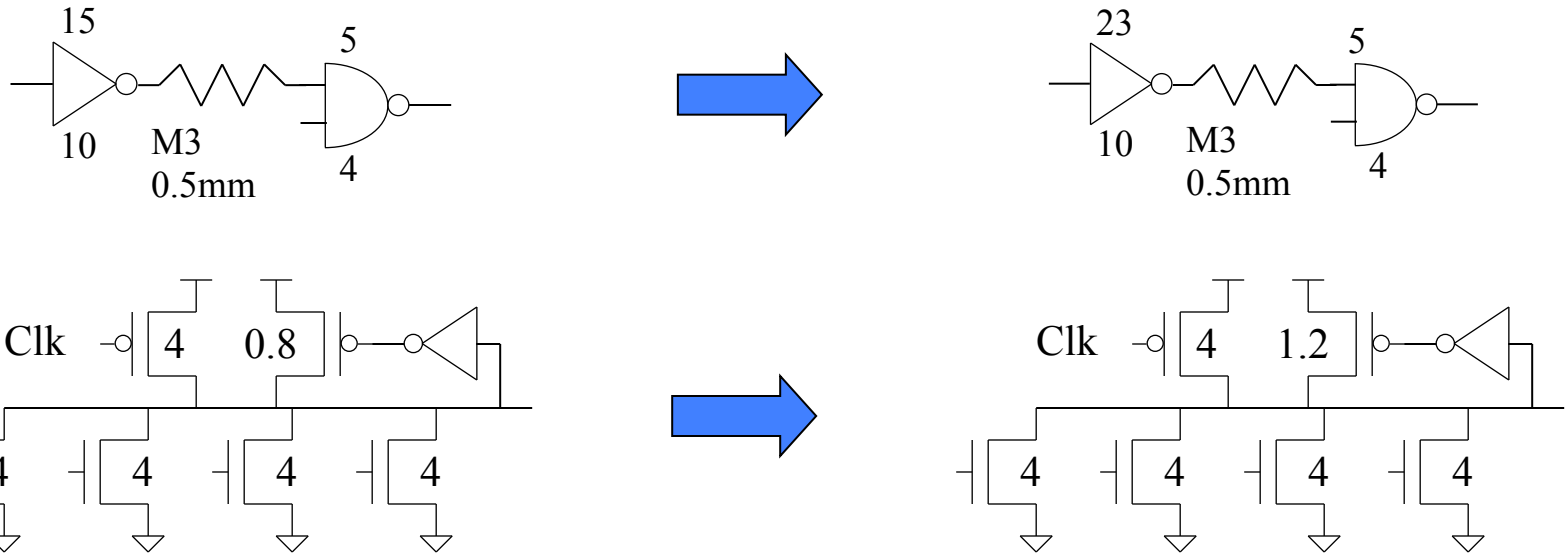
Reduce Size of Receiver



Smaller sized receiver will respond more slowly to transient noise; as a result, propagated noise will be less.

Con: Increases delay

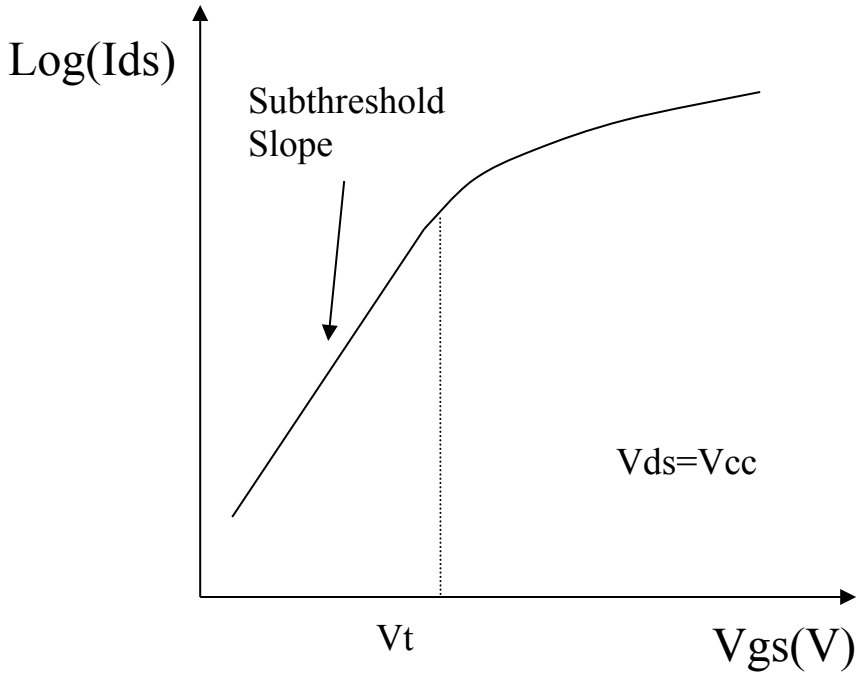
Size Up Driver or Keeper



A larger driver or keeper will provide more current to hold a node at its proper value.

Con: Increases area
Increases power

Subthreshold Leakage



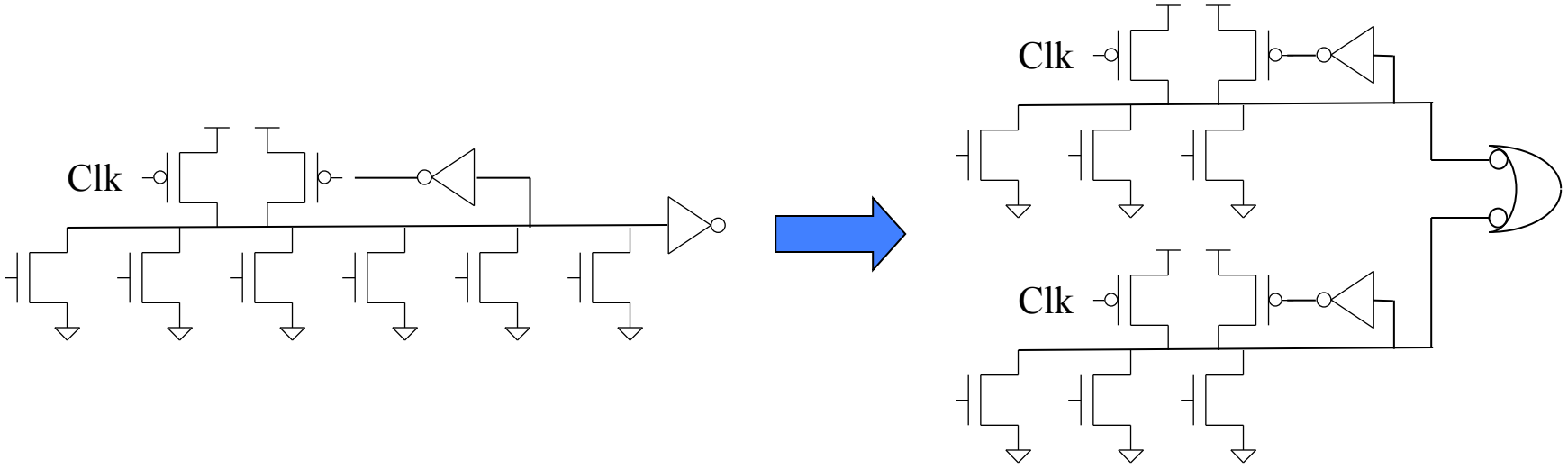
For Vgs<Vt, drain to source current is not actually zero.

Subthreshold Slope ≈ 80-100mV/decade

Leakage currents prevent gates from making full rail swings

Subthreshold leakage is particularly bad in gates with many parallel devices.

Avoid Gates with Many Parallel Paths



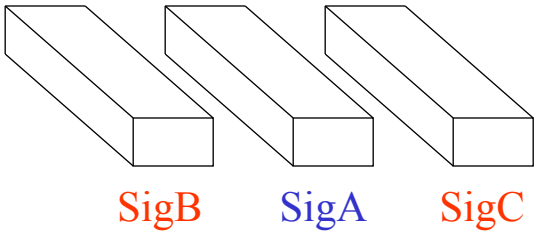
Wide fan-in gates are susceptible to all forms of noise including subthreshold leakage

Con: May limit logic in next gate

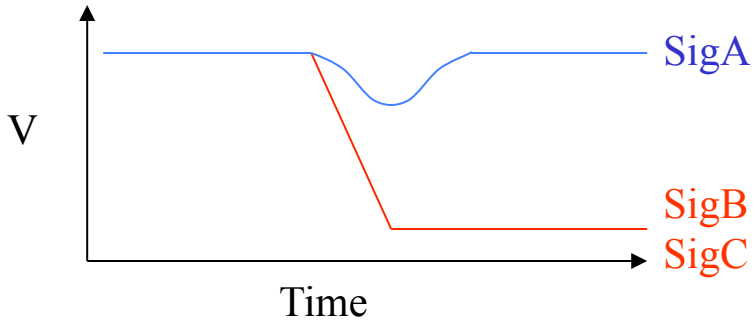
Using Low Vt devices increases subthreshold current dramatically.

Cross-Talk

CrossTalk (Coupling) Noise



A changing voltage on any wire affects the voltage of surrounding wires.



C_{tot} = total capacitance of victim node

C_{ll} = capacitance to aggressors

Worst case noise bump = $Vcc*(C_{ll}/C_{tot})$

General CrossTalk Solutions:

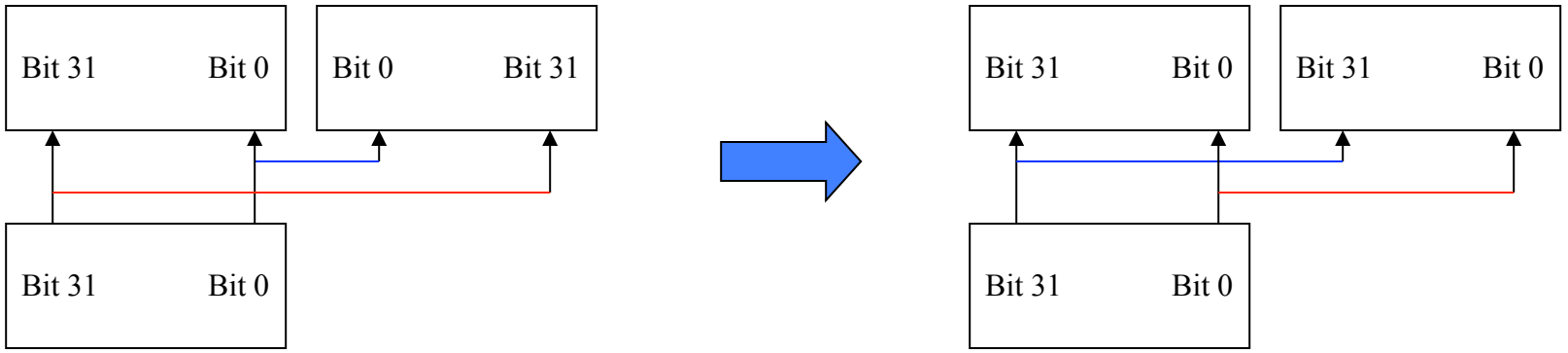
Decrease capacitance to aggressors

Increase capacitance to non-aggressors

Increase driver strength or reduce wire resistance

Change Floorplan to Reduce Wire Length

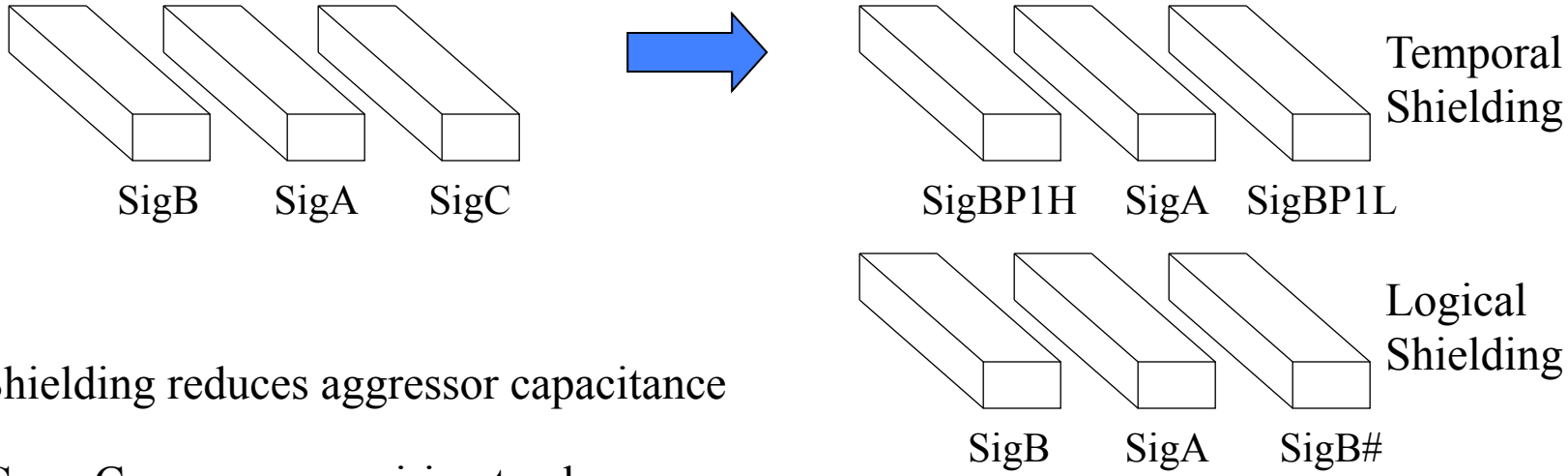
Shorter wire length decreases aggressor capacitance.



Good floorplan can greatly reduce the distance traveled by noisy signals.

Con: May make other wires longer

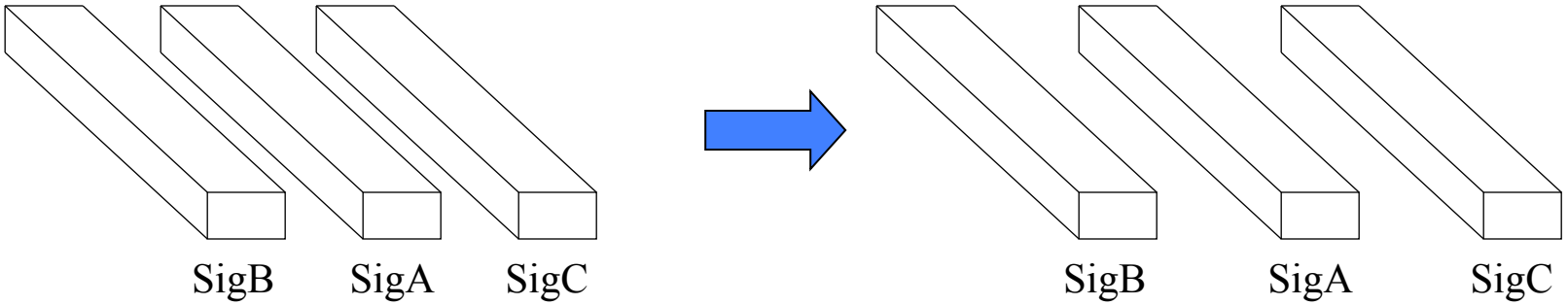
Shield Victim Signals



Shielding reduces aggressor capacitance

Con: Can use more wiring tracks

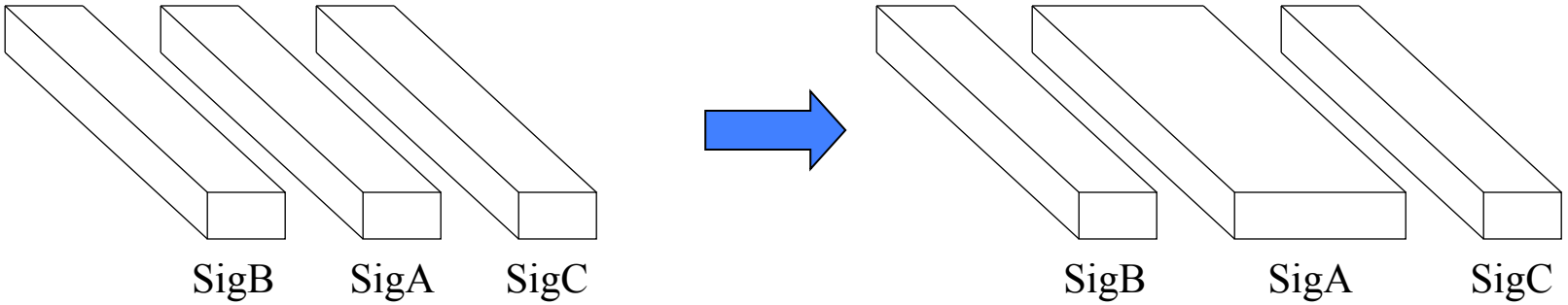
Increase Wire Spacing



Increased wire spacing reduces aggressor capacitance.

Con: Uses more wiring tracks

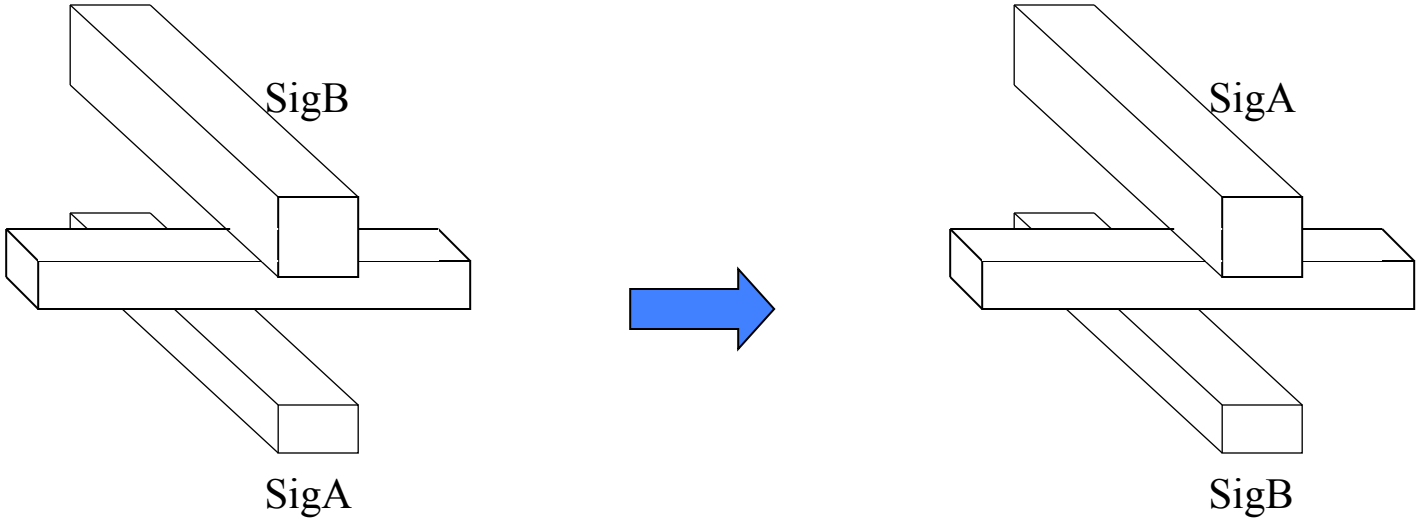
Increase Wire Width



Wider wire reduces resistance and increases non-aggressor capacitance.

Con: Uses more wiring tracks

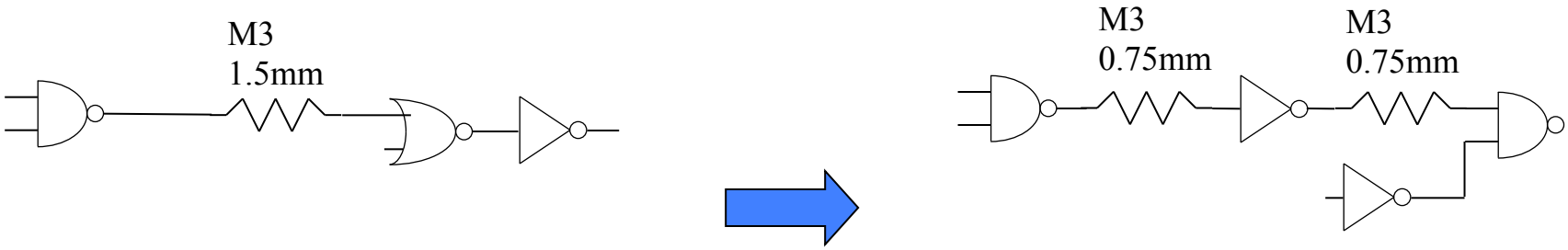
Use Higher Metal Layer



Higher level metals are thicker and therefore have less resistance.

Con: Takes tracks from global routes
Total and aggressor capacitance are about the same.

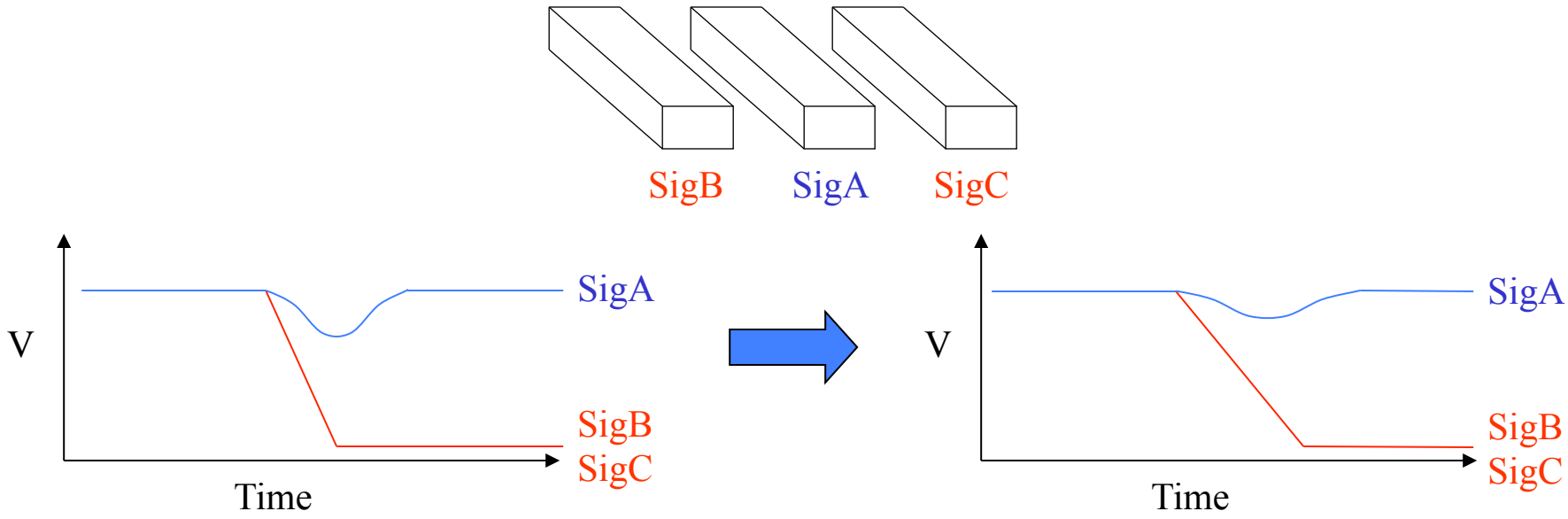
Add Repeaters



Inverters are very effective at filtering out noise.

Con: Increases area
Can increase delay

Slow Down Attacking Signals



Slower slew rate on aggressors allows more time for victim's driver to supply current.

Con: Can cause maxdelay failures

Aggressor signals become noise sensitive

Twisted Differential Buses

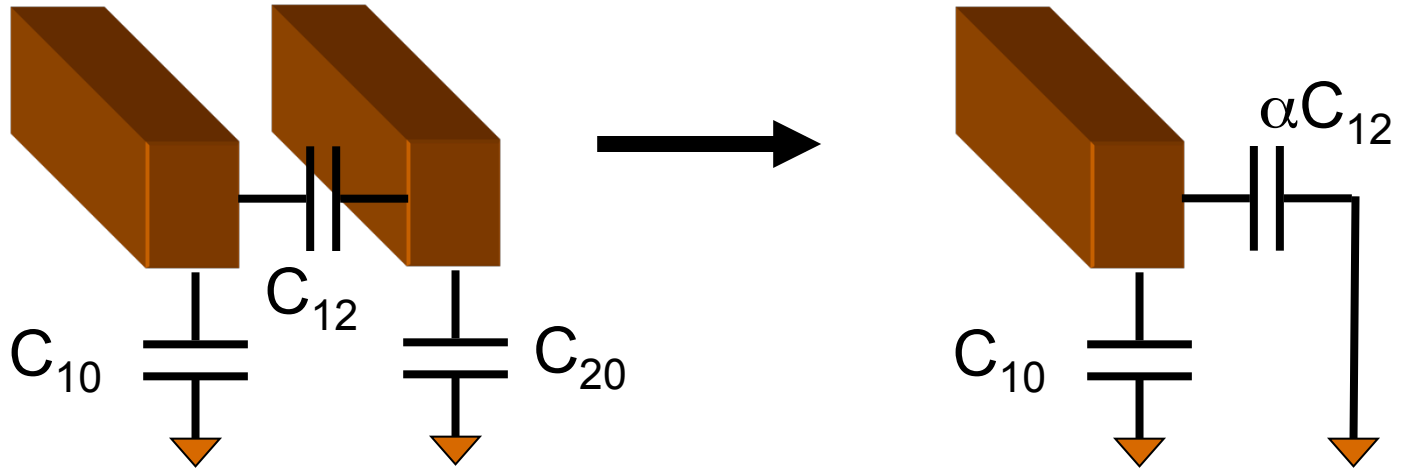
Aggressors which are complements of each other cancel out.

Con: Uses extra metal layers
Complicates layout

Modeling Cross-talk for Static Timing Analysis

Capacitive Cross Talk in Static Timing Analysis

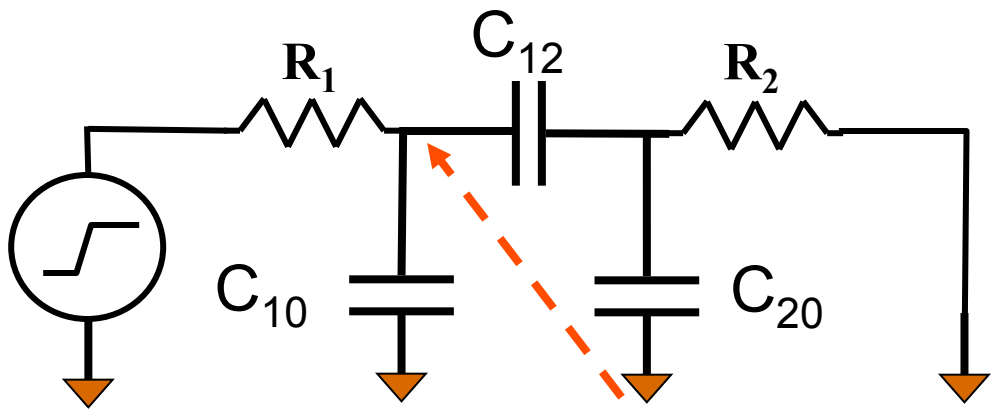
- Static timing analysis reduces coupled circuit models into uncoupled models



- What's the worst case α? Early mode & late mode.

Capacitive Cross Talk in Static Timing Analysis

- **Adjacent line is quiet in the nominal case**

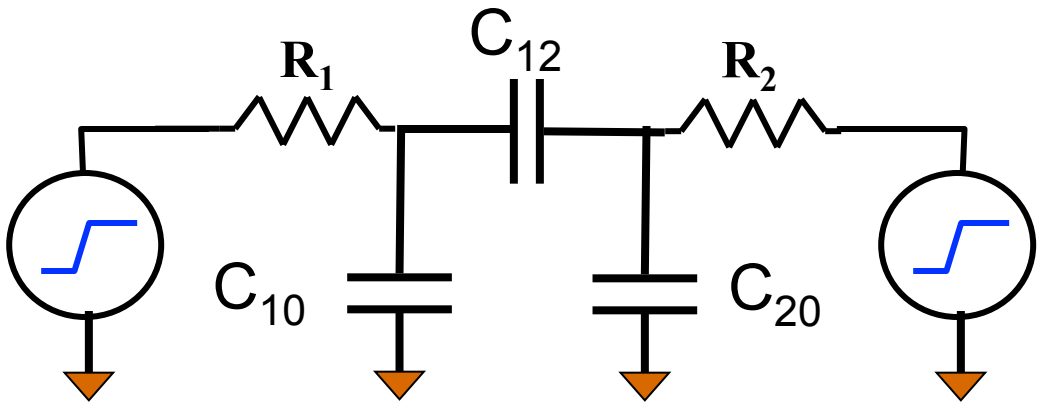


Calculate dQ across C_{12} when switching node reaches ½ Vdd

$\alpha = dQ / (1/2*C_{12}*Vdd)$

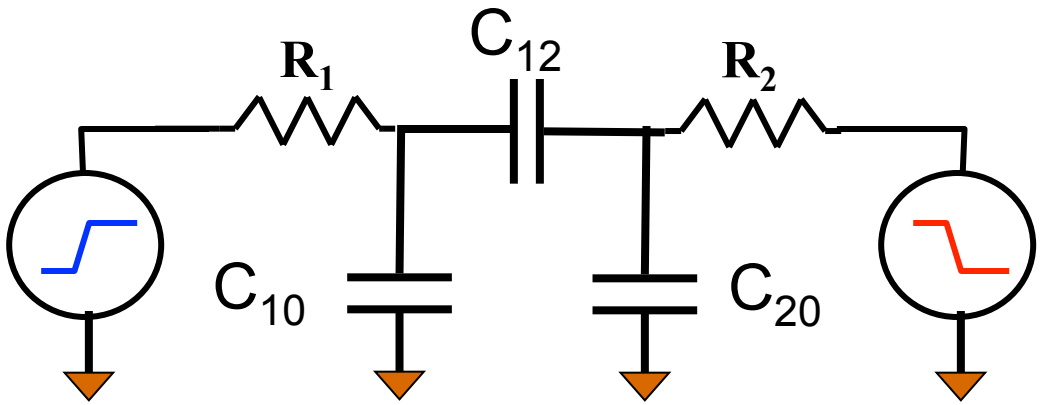
Capacitive Cross Talk in Static Timing Analysis

- Adjacent line switches in same direction in early mode case



Capacitive Cross Talk in Static Timing Analysis

- Adjacent line switches in opposite direction in late mode case



Capacitive Cross Talk in Static Timing Analysis

- Switching on a balanced receiver occurs at ½ Vdd
- To find α find dQ across C_{12} when switching occurs

	Earliest	Early	Nominal	Late	Latest
Line 1 activity			0 - Vdd $\tau_r = t_1$		
Line 2 activity			quiet		
dV on C_{12}			½ Vdd		
α			1		

Capacitive Cross Talk in Static Timing Analysis

- Switching on a balanced receiver occurs at ½ Vdd
- To find α solve dQ = C*dV for C_{12}

	Earliest	Early	Nominal	Late	Latest
Line 1 activity		0 - Vdd $\tau_r = t_1$	0 - Vdd $\tau_r = t_1$	0 - Vdd $\tau_r = t_1$	
Line 2 activity		0 - Vdd $\tau_r = t_1$	quiet	Vdd - 0 $\tau_r = t_1$	
dV on C_{12}		0	½ Vdd	Vdd	
α		0	1	2	

Capacitive Cross Talk in Static Timing Analysis

- Switching on a balanced receiver occurs at ½ Vdd
- To find α solve dQ = C*dV for C_{12}

	Earliest	Early	Nominal	Late	Latest
Line 1 activity	0 - Vdd $\tau_r = t_1$	0 - Vdd $\tau_r = t_1$	0 - Vdd $\tau_r = t_1$	0 - Vdd $\tau_r = t_1$	0 - Vdd $\tau_r = t_1$
Line 2 activity	0 - Vdd $\tau_r = ½ t_1$	0 - Vdd $\tau_r = t_1$	quiet	Vdd - 0 $\tau_r = t_1$	Vdd - 0 $\tau_r = ½ t_1$
dV on C_{12}	-½ Vdd	0	½ Vdd	Vdd	3/2 Vdd
α	-1	0	1	2	3

Power Supply Noise

Power Supply Noise

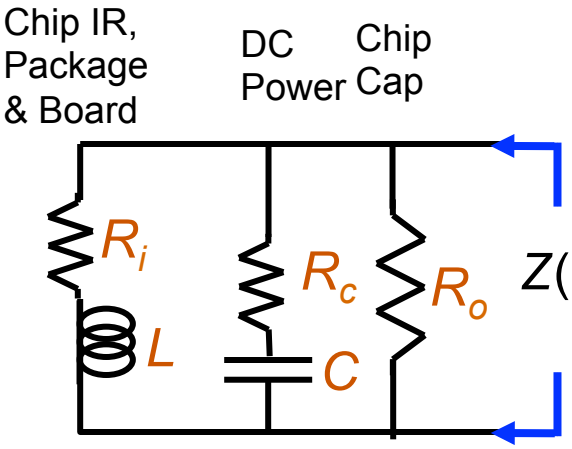
- **Power Supply Noise: Vnoise = Z * I**
  - Global noise
    - Function of total chip switching, chip power grid, chip decoupling capacitance & chip packaging
    - Δt > couple of clock cycles
  - Local noise
    - Function of local circuit switching, local power grid & local decoupling capacitance
    - Δt < clock cycle

- **Ratio of Noise to Supply Voltage Is Increasing**
  - $V_{noise} = Z * I = Z * P / V_{supply}$
  - Consider fixed power density (P) and impedance (Z)
  - Scaling yields a worsening $V_{noise}/V_{supply} = Z * P / (V_{supply})^2$

Chip/Package Resonance

- Chip/package forms an LRC tank circuit
- Driving point has a resonant impedance
  - $2\pi f_{res} \approx (LC)^{-1/2}$ where
    - L = Lpackage + Lboard + Lcap
    - C = Chip capacitance
  - $Z(f_{res})$ is a function of Q

Two Pole Model Perspective



$$Z(s) = \frac{R_c\left(s + \frac{1}{R_cC}\right)\left(s + \frac{R_i}{L}\right)}{s^2(1+\alpha) + s\left(\frac{(R_c + (1+\alpha)R_i)}{L} + \frac{1}{R_oC}\right) + \frac{(1+\beta)}{LC}}$$

$$\text{where } \alpha = \frac{R_c}{R_o} << 1,\ \beta = \frac{R_i}{R_o} << 1$$

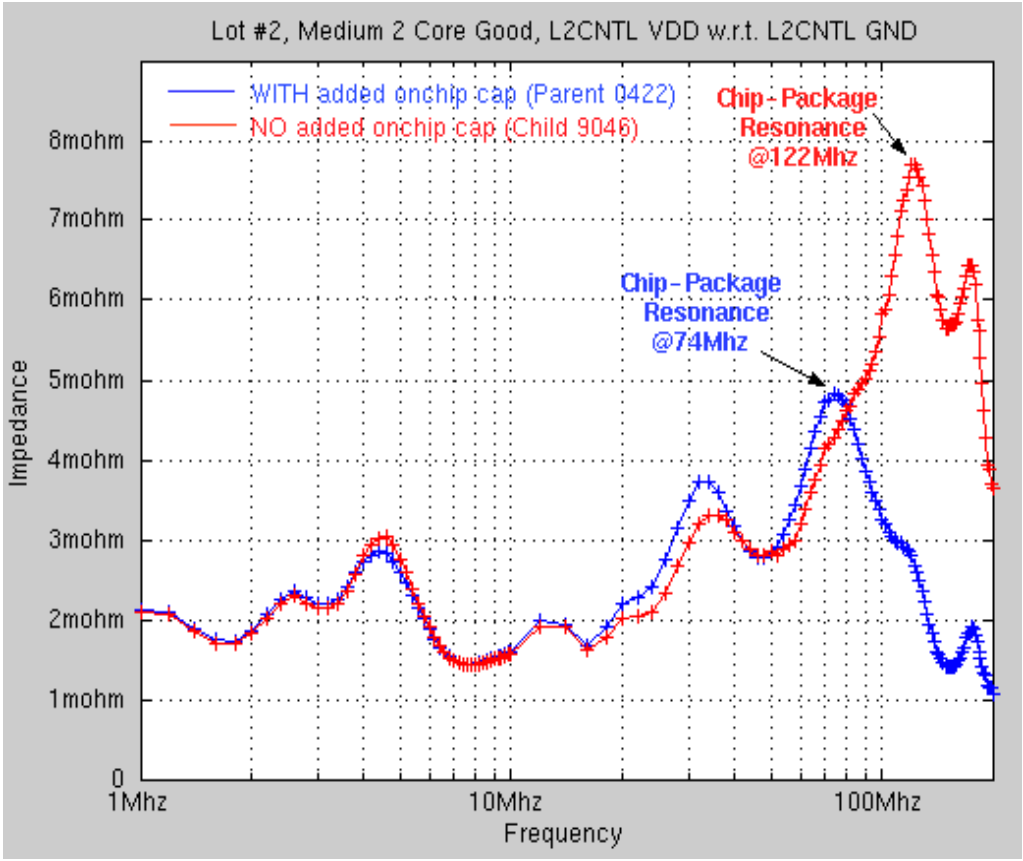
Approximate Behavior

$$2\pi f_{res} \approx (LC)^{-1/2}$$

$$Z(f_{res}) \approx \frac{L}{\left((R_i + R_c)C + \frac{L}{R_o}\right)} \quad \text{for} \quad \left(\frac{R_i}{L} << (LC)^{-1/2} << \frac{1}{R_cC}\right)$$

Power 5 Chip/Package Measurements

With & Without On-chip Capacitance @L2CNTL



* R. Weekly, S. Chun, A. Haridass, C. O'Reilly, J. Jordan, and F. O'Connel, "Optimum Design of Power Distribution System via Clock Modulation," IEEE 12th EPEP Topical Meeting, 2003

Power 5 Chip/Package Measurements

Correlation with Chip-Package Resonance Frequency

Parent 0422: **WITH on chip cap** 1/(2*6.5nsec) = ~77Mhz

* R. Weekly, S. Chun, A. Haridass, C. O'Reilly, J. Jordan, and F. O'Connel, "Optimum Design of Power Distribution System via Clock Modulation," IEEE 12th EPEP Topical Meeting, 2003

Power 5 Chip/Package Measurements

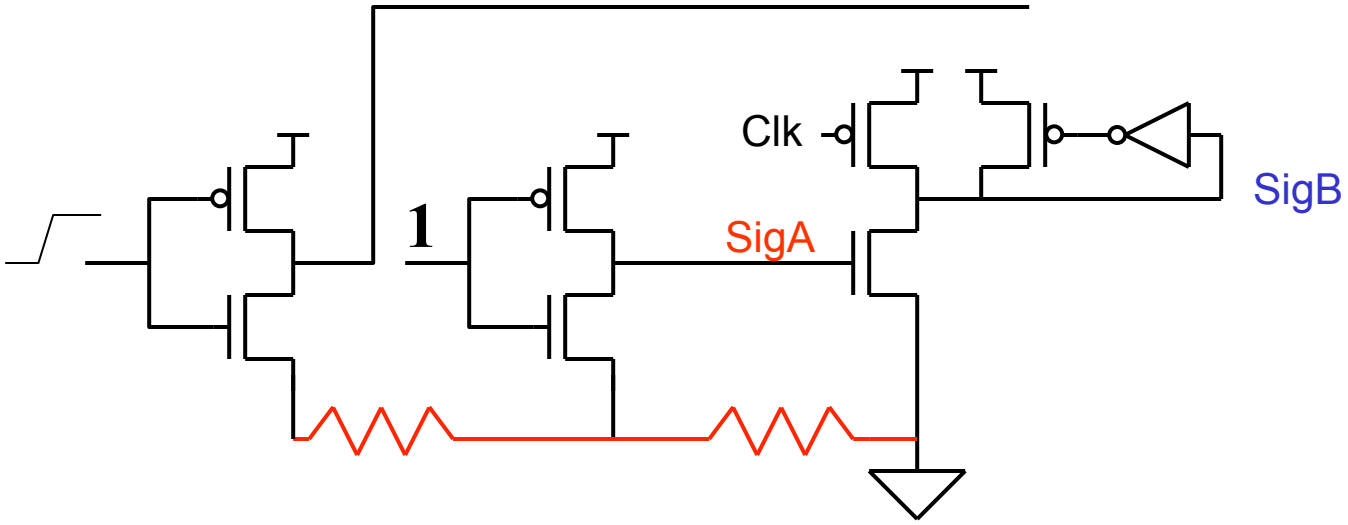
Correlation with Chip-Package Resonance Frequency

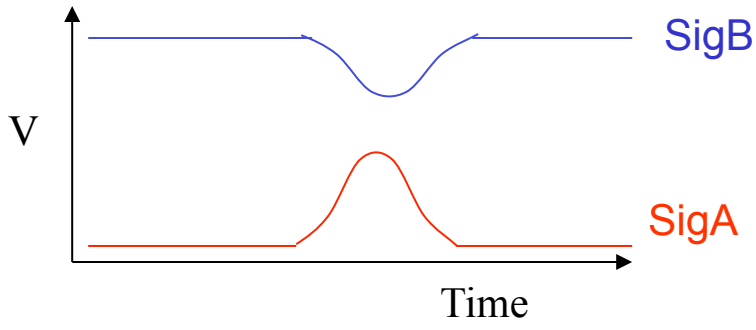
Child 9046: **NO on chip cap** f = 1/(2*4nsec) = ~125Mhz

* R. Weekly, S. Chun, A. Haridass, C. O'Reilly, J. Jordan, and F. O'Connel, "Optimum Design of Power Distribution System via Clock Modulation," IEEE 12th EPEP Topical Meeting, 2003

Local IR Noise

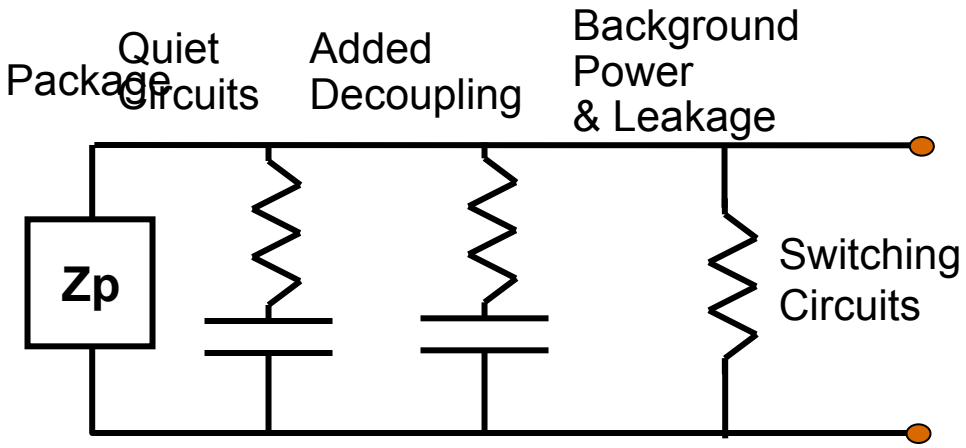
Local *i*R drops occur when power mesh is neglected

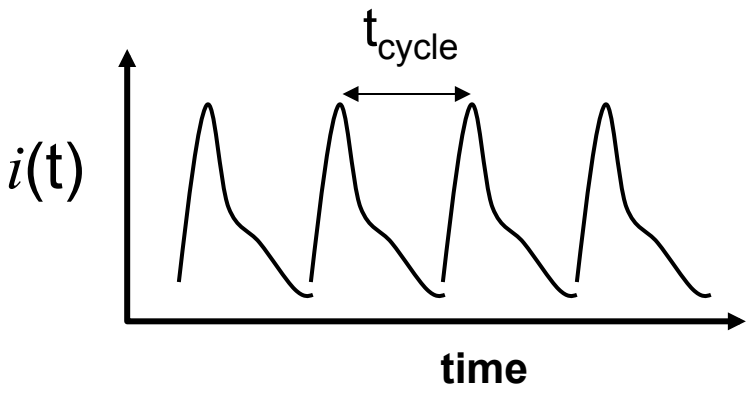


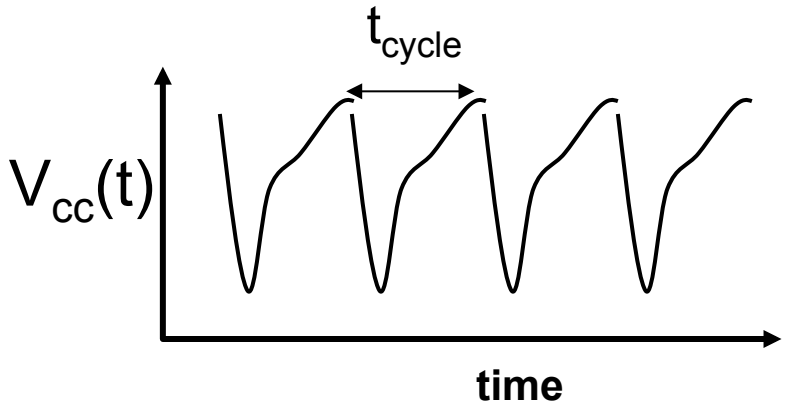


Local AC Noise

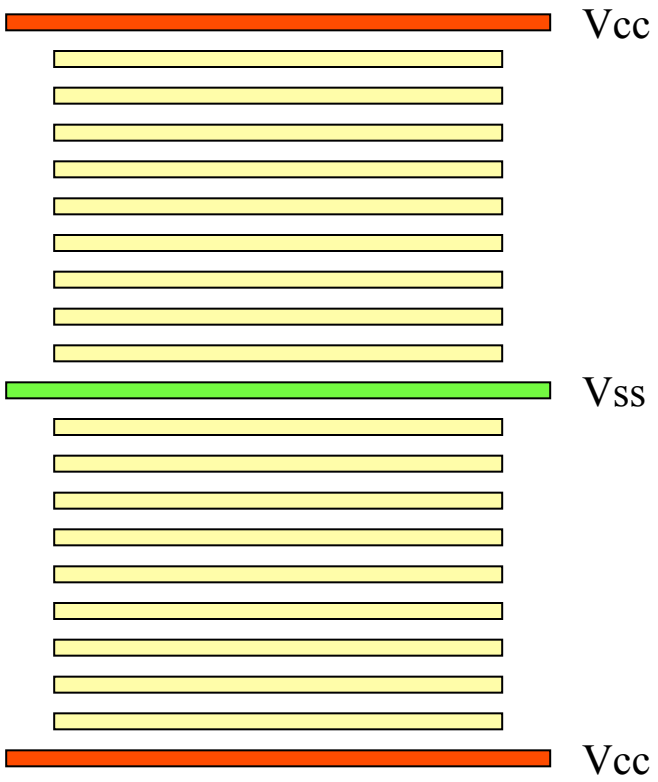
Local supply variations within a cycle reduce dynamic circuit margins & half cycle paths

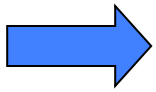


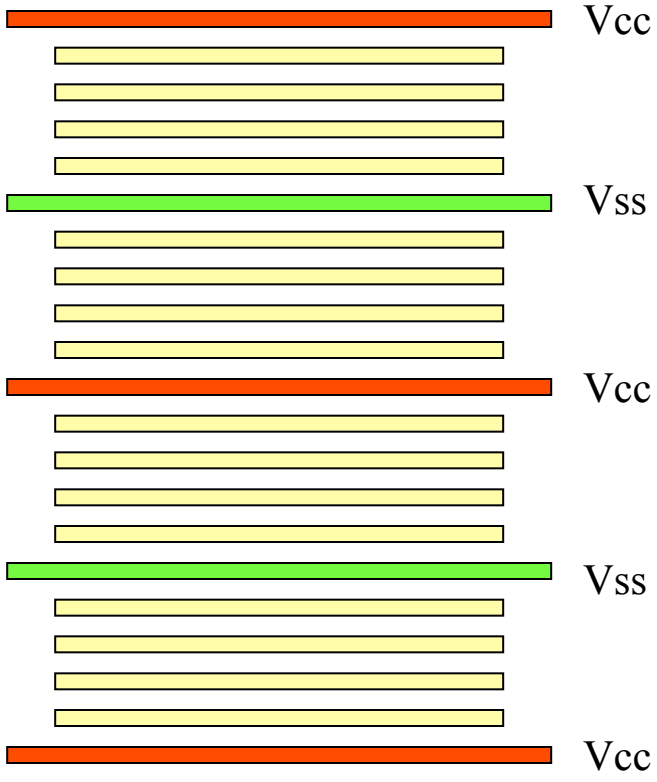




Increase Number of Power Lines



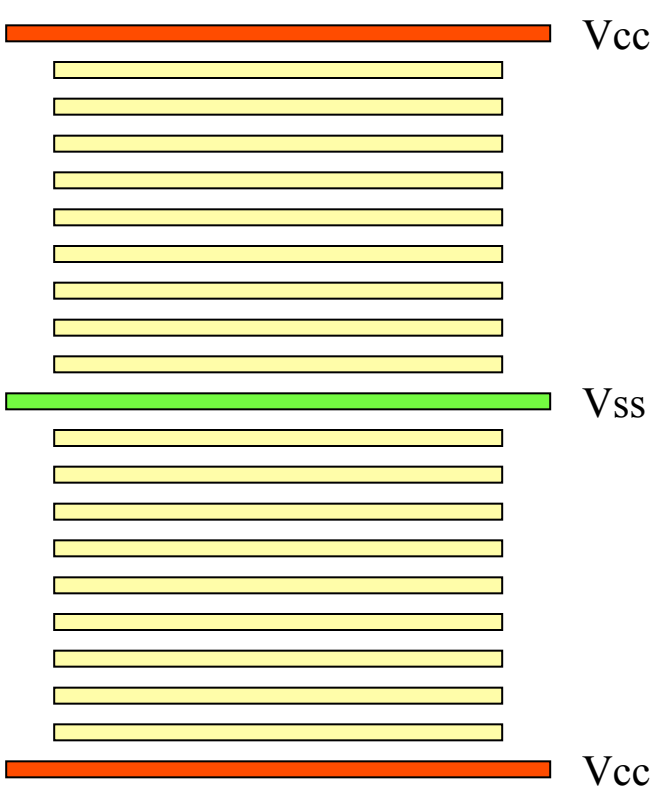


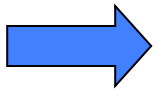


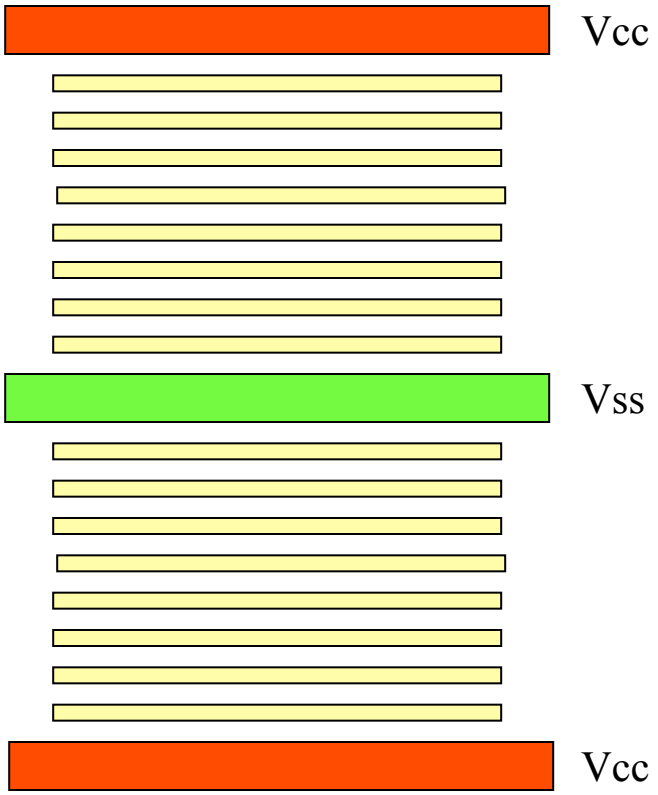
Reduces both resistance and inductance of power grid.

Con: Reduces tracks available for signals

Increase Width of Power Lines



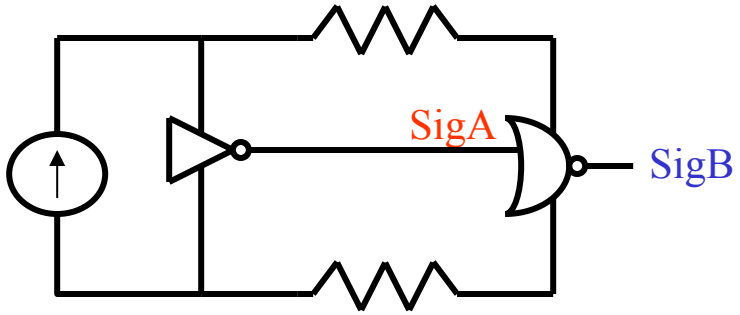


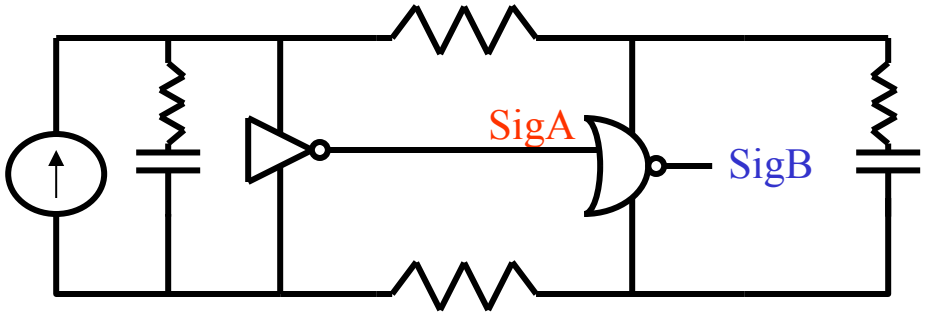


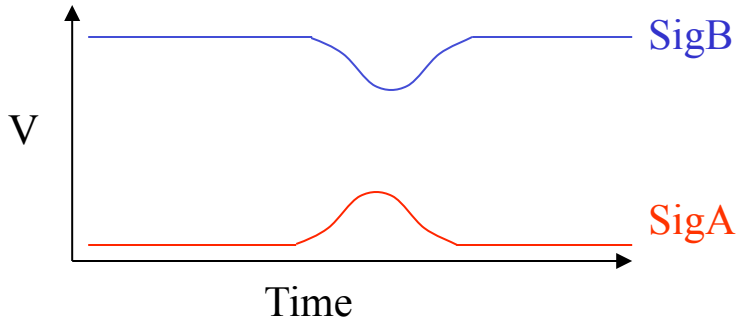
Reduces resistance of power grid.

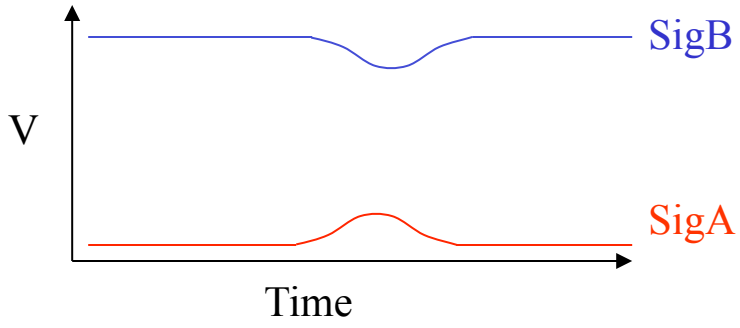
Con: Reduces tracks available for signals

Add Decoupling Capacitors





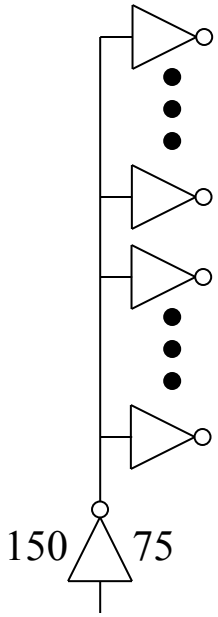


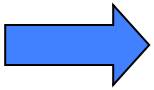


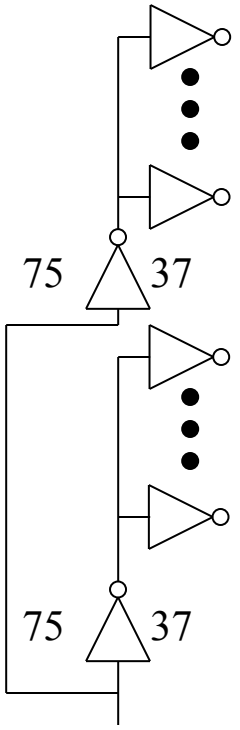
Capacitors added to power grid can provide charge for current transients.

Con: Layout effort
Total benefit uncertain

Reduce Size of Huge Drivers



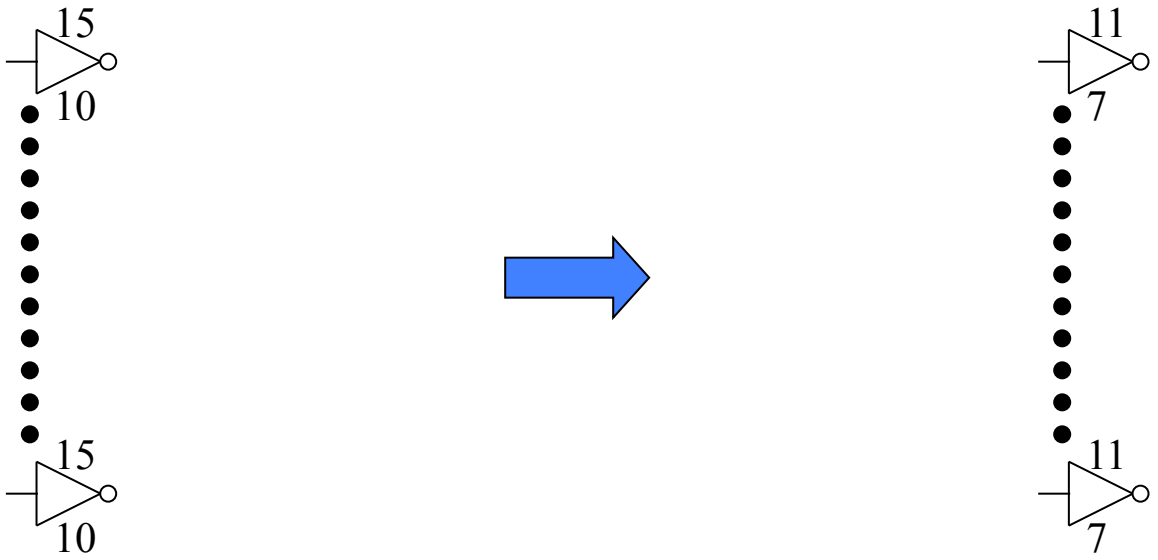




Distributing huge drivers allows current to be drawn from larger area of power grid.

Con: Adds wire load

Reduce Size of Wide Bus Drivers

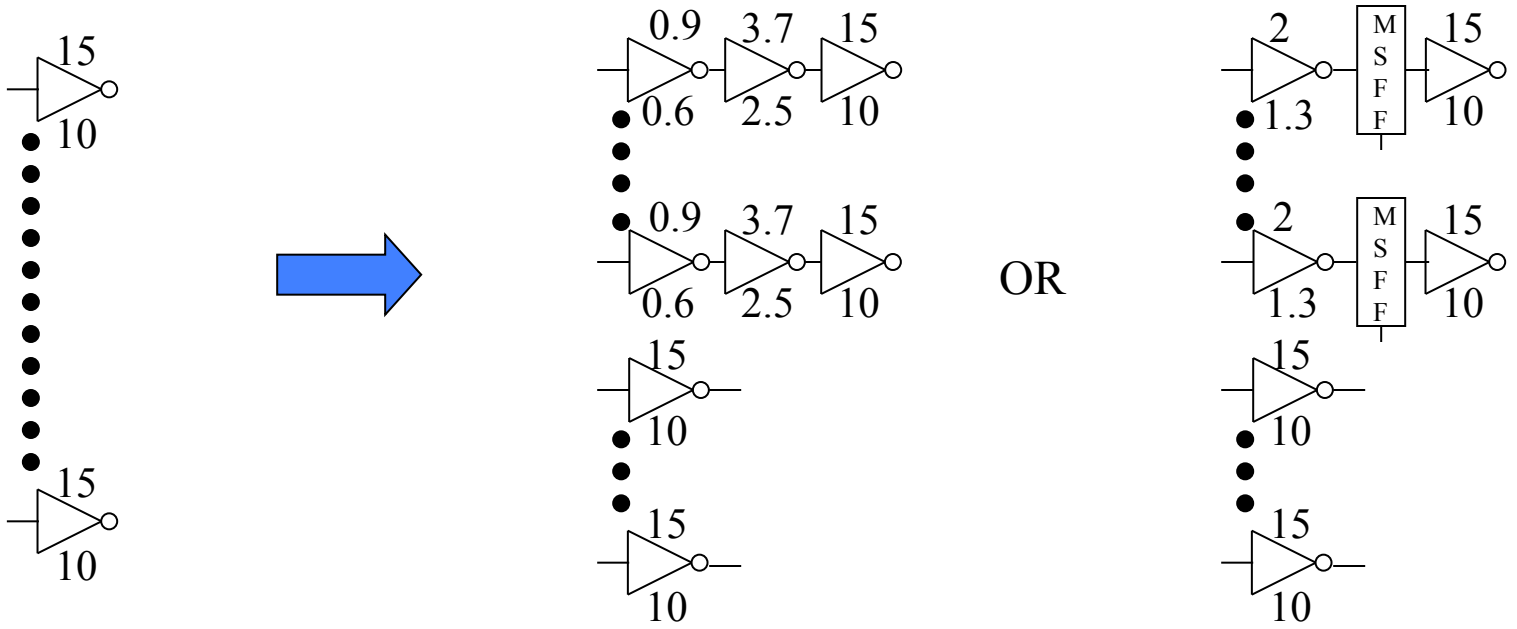


Small drivers on very wide buses can cause large transient currents.

Con: Adds delay
Weak driver can lead to failure at receiver

Adding repeaters can reduce size of needed driver without increasing delay.

Split Timing of Wide Bus Drivers



For extremely large buses (>128 bits) driving at slightly different times can greatly reduce the induced supply noise.

Con: Bits of bus do not all arrive at the same time

SUMMARY

- Noise can impact functionality; increasing cycle time does not always help.
- Presented various methods to increase noise immunity.
- Cross-talk modeling for static timing analysis uses a Miller Coefficient Factor (MCF) in order to simplify the RC network from a coupled circuit model to an uncoupled one.
- Do not forget about global and local power-supply noise; need to consider platform/package RLC to properly model global power supply droop; local power supply noise can be mitigated with robust power grids + decoupling capacitors.

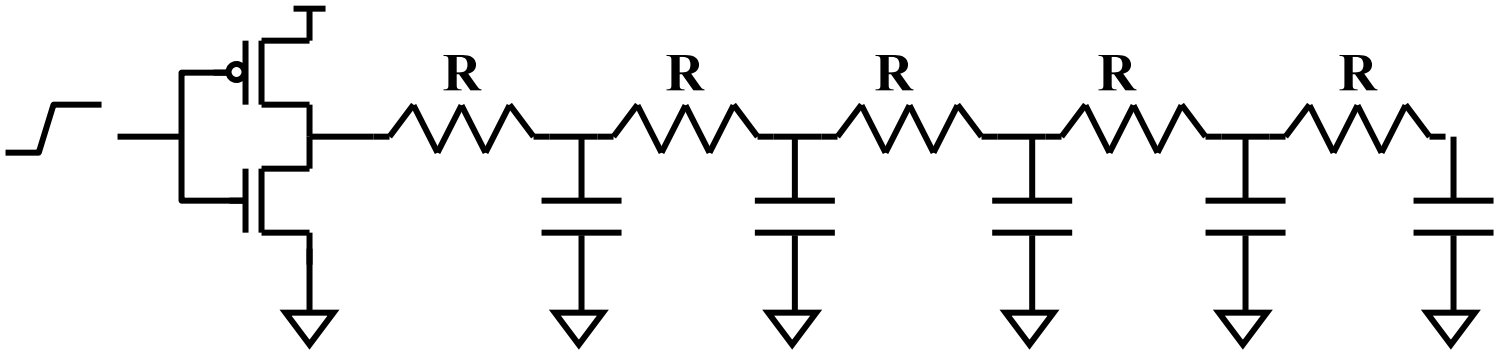
BACKUP

Common Mode Noise

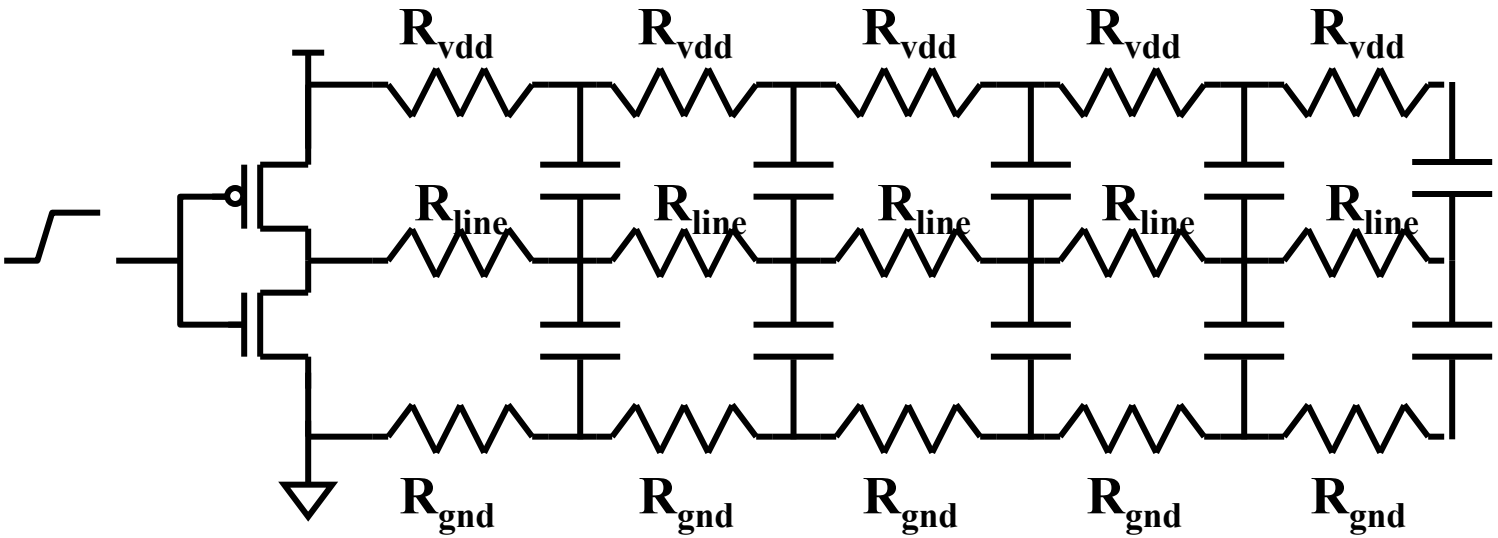
Common Mode Noise

- Interconnect return currents closely follow signal lines at high frequencies
  - Minimizes the loop inductance and total loop impedance
- Simultaneous switching of wide busses creates common mode noise on signals parallel to bus
  - Low impedance signals carry some of the return current
- Common mode noise has both inductive and resistive components
- Can add or subtract from capacitive crosstalk
  - Same transition adds to capacitive crosstalk at near end
  - Same transition subtracts from capacitive crosstalk at far end

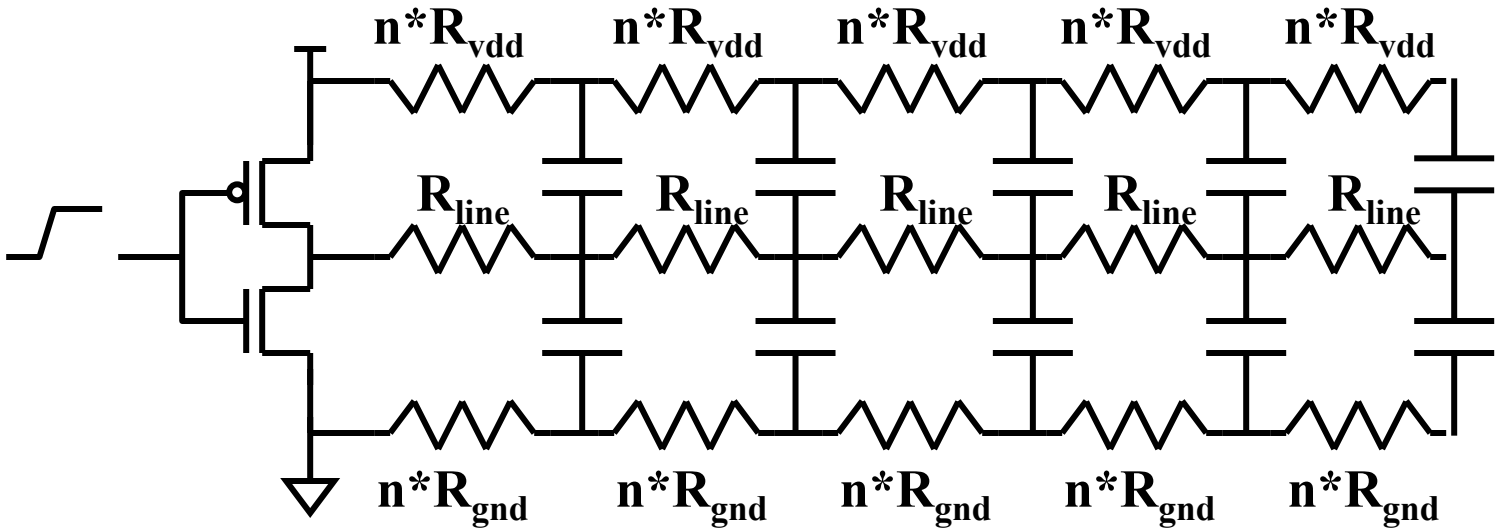
Common Ground RC Interconnect Model



RC Interconnect Model with Return Paths

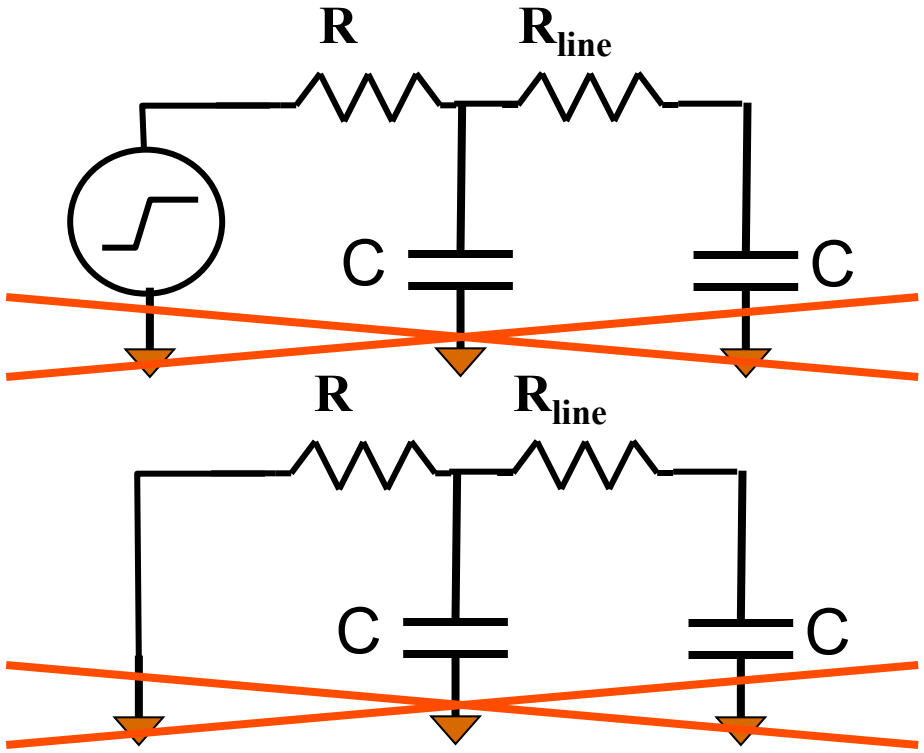


Effect of N Circuits Switching Simultaneous



Common Mode Near & Far End Noise Polarity

- Capacitively uncoupled lines are still inductively and resistively coupled
  - Resistive coupling is a consequence of shared return path
- Common mode near end & far end noises are opposite in polarity



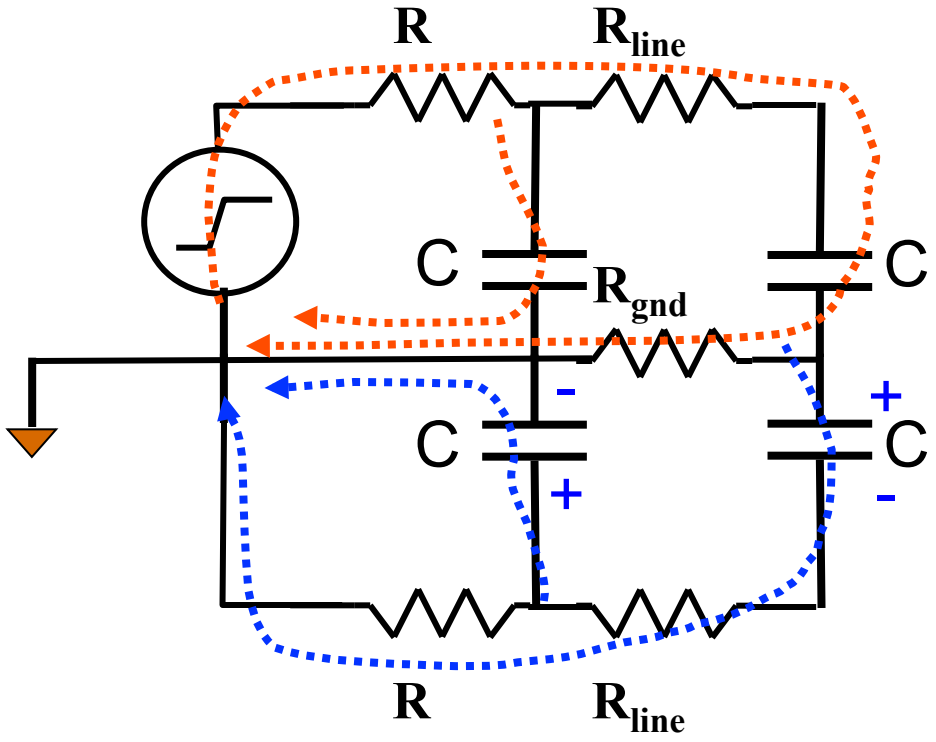
Active Line

Common ground is mythical

Quiet Line

Common Mode Near & Far End Noise Polarity

- **Return current flows oppositely through near & far end impedances**



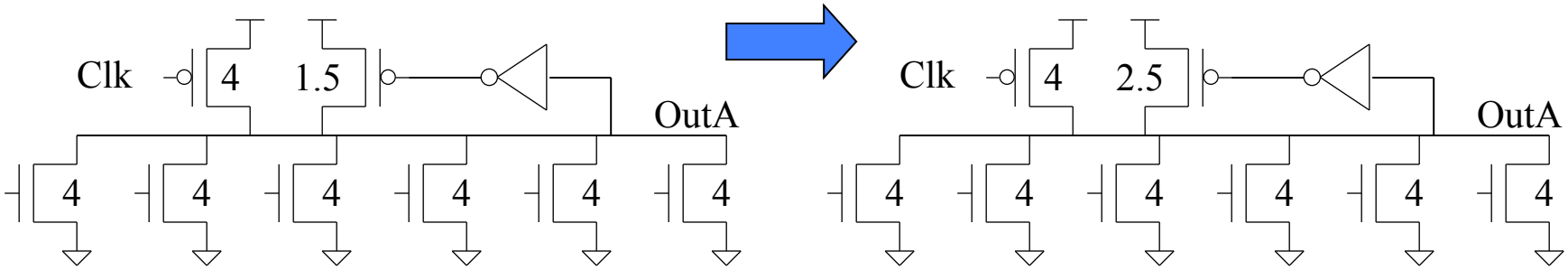
Active Line

Shared Return Path

Quiet Line

Domino Noise Solutions

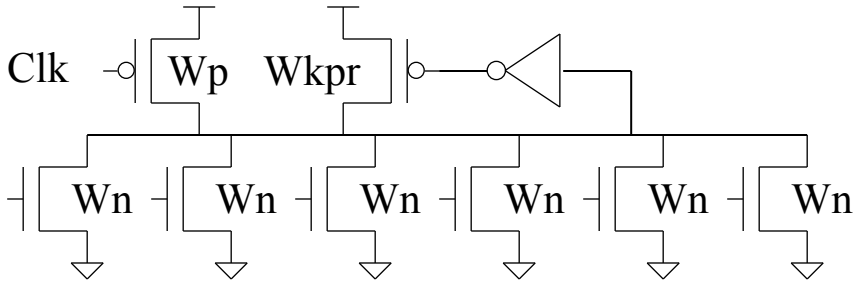
Increase Keeper Size



Up to a point noise margin in any domino gate can be improved by increasing the keeper size.

Con: Increases delay and power

Sizing Keepers



NumN = 6

NumN*Wn/20 < Wkpr

Min keeper size set by noise requirements

Wkpr < Wn/2

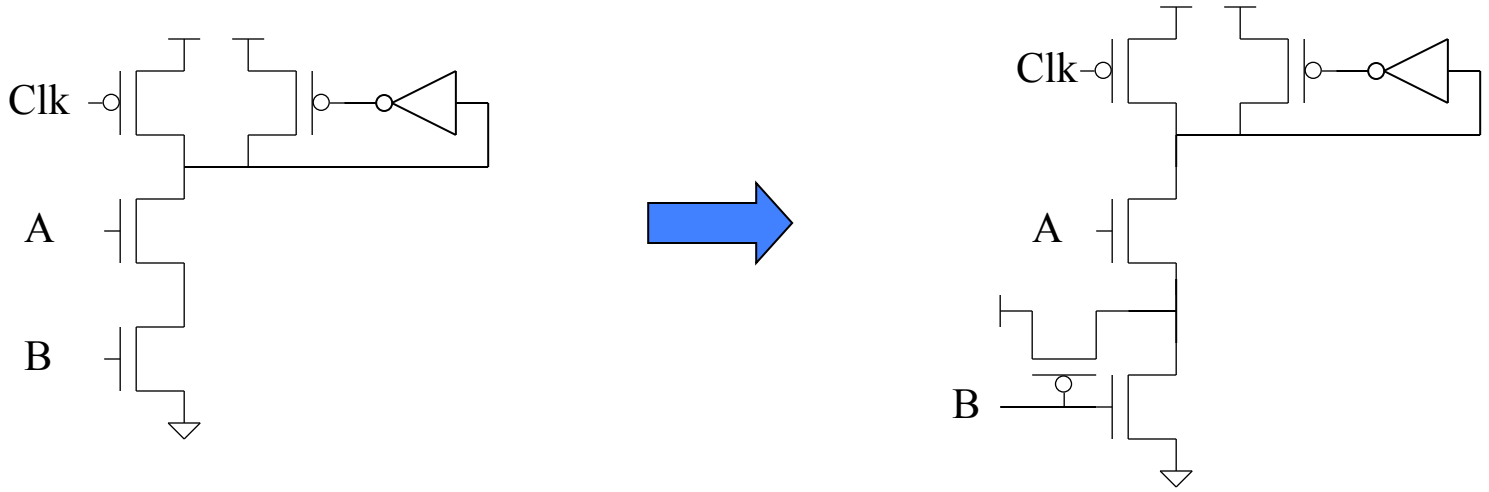
Max keeper size set by delay degradation

NumN*Wn/20 < Wkpr < Wn/2

NumN < 10

Maximum noise sensitivity and delay limit number of parallel stacks.

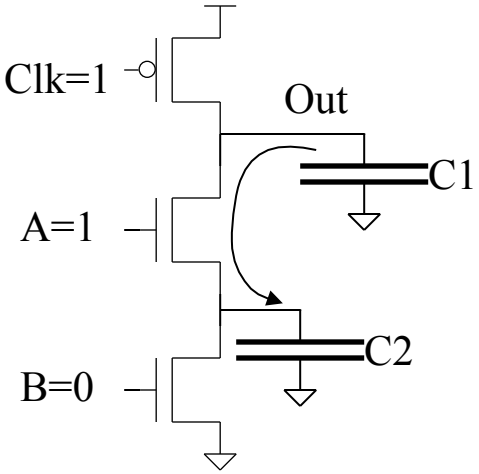
Pseudo CMOS Input Protection



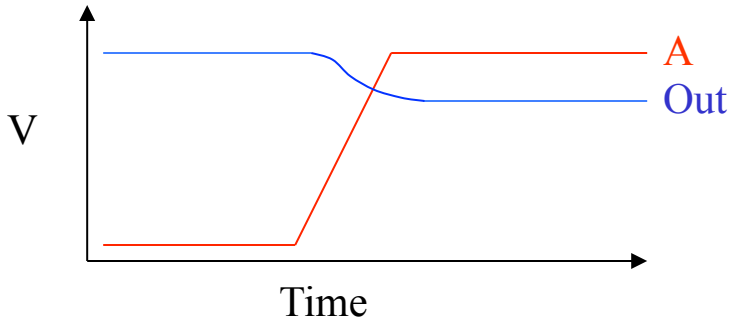
PMOS devices added to domino inputs precharge intermediate nodes and provides current in case of noise bump up on input.

Con: Increased load on inputs
Can't be used for parallel paths

Charge Sharing



During evaluate A goes high while B stays low causing charge sharing between C1 and C2.

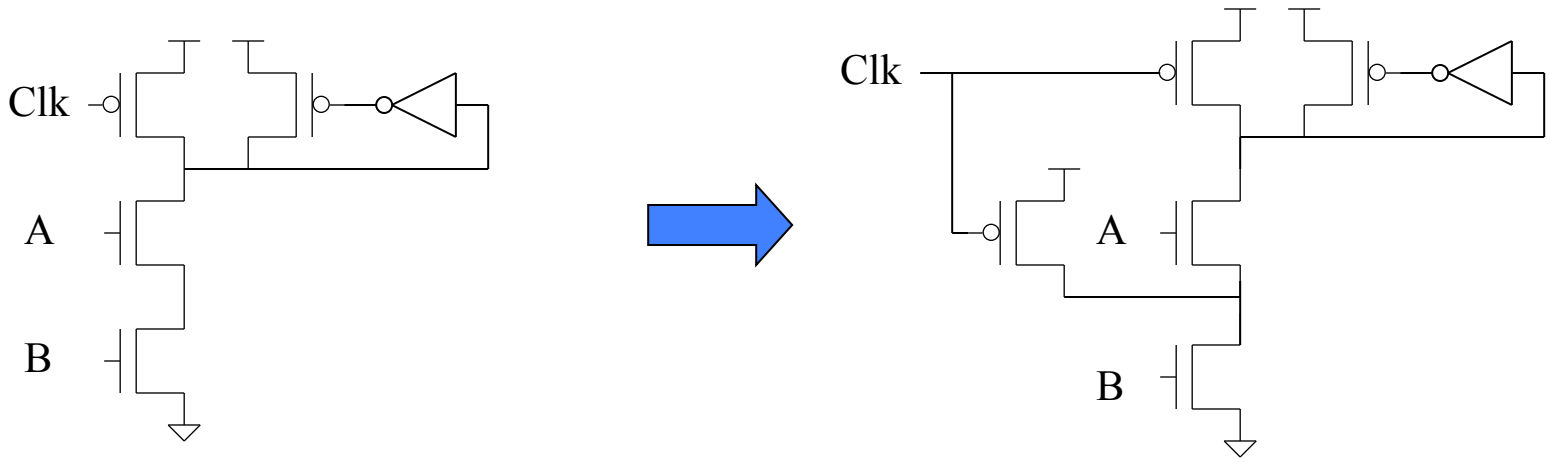


General Charge Sharing Solutions:

- Precharge intermediate node
- Decrease C2
- Increase C1

Out = Vcc*C1/(C1+C2)

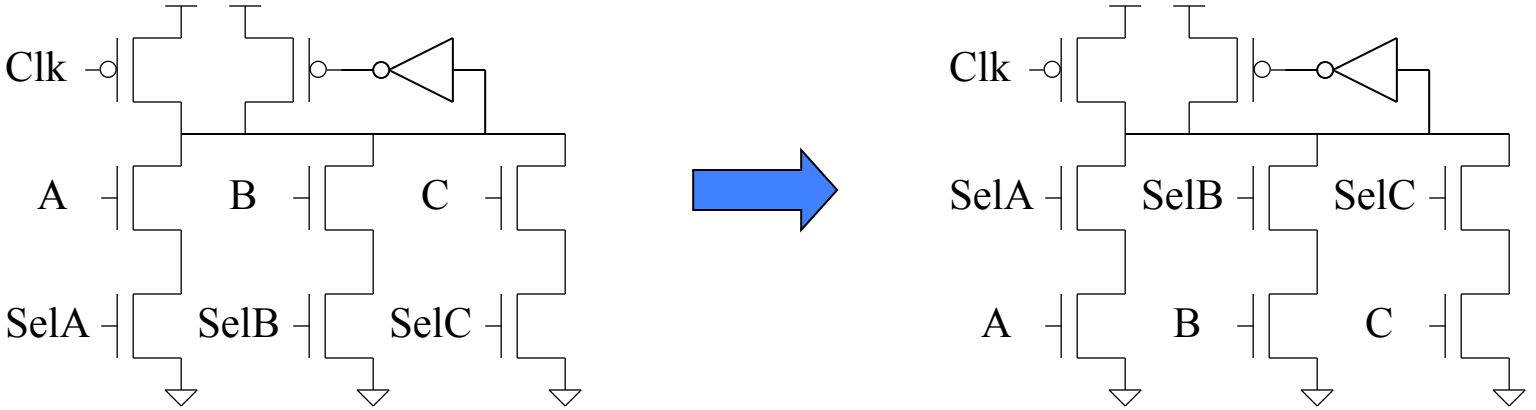
Intermediate Precharge Device



Extra PMOS device makes sure intermediate node is always precharged.

Con: Increased clock load

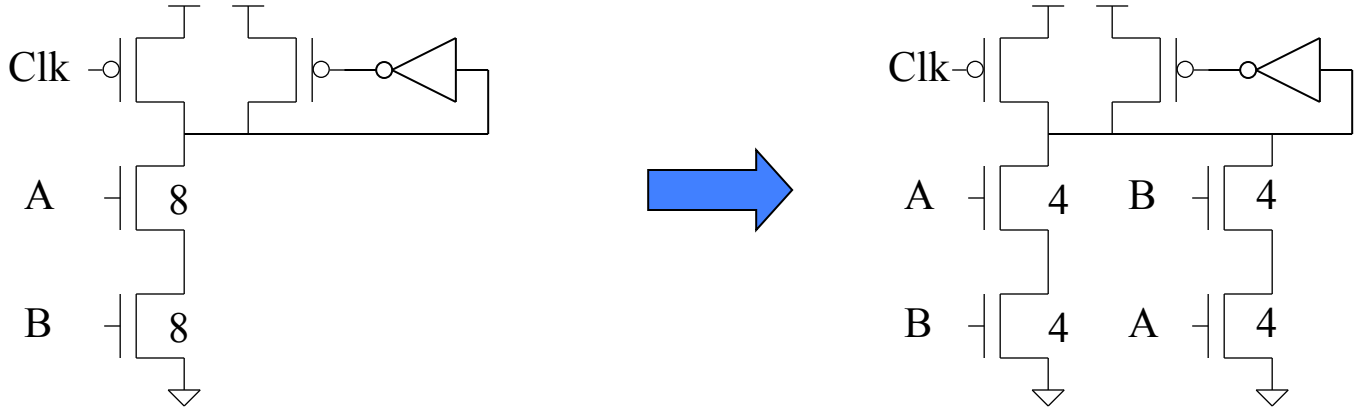
Select Signals on Top of Stack



With select signals at top of stack there can only be charge sharing to a single intermediate node.

Less diffusion load connected to output also leads to faster switching.

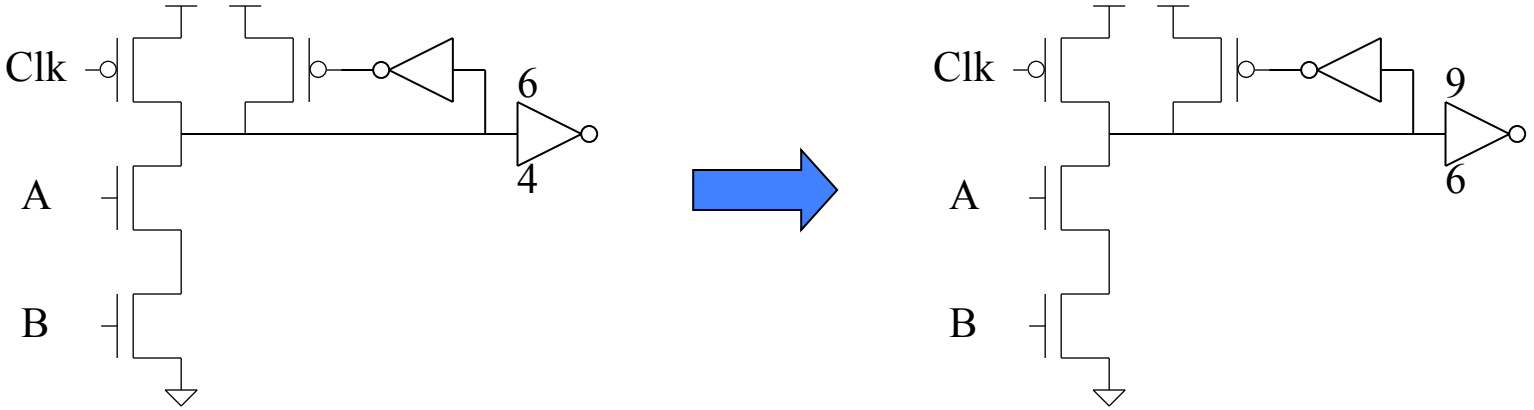
Symmetric Pulldown Stacks



Splitting stacks and reordering inputs cuts charge sharing in half.

Con: More complex layout

Increase Size of CMOS Receiver



Increased capacitance on dynamic node reduces impact of intermediate capacitance.

Con: Increase dynamic gate delay

Smaller delay through CMOS gate may offset increased delay at this gate.