VLSI-2: Off-chip Driver/Receiver Design
Spring 2017

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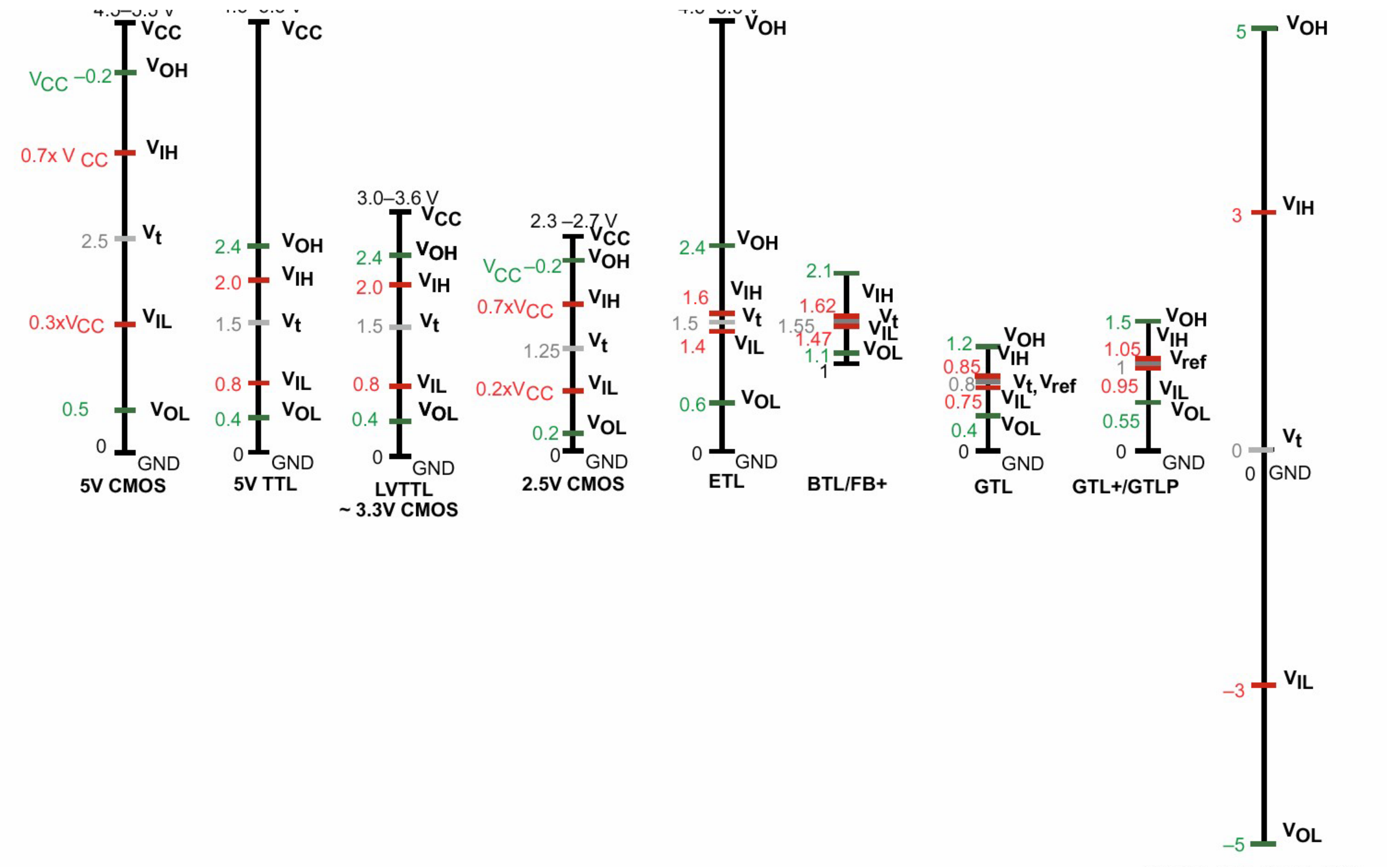
OUTLINE

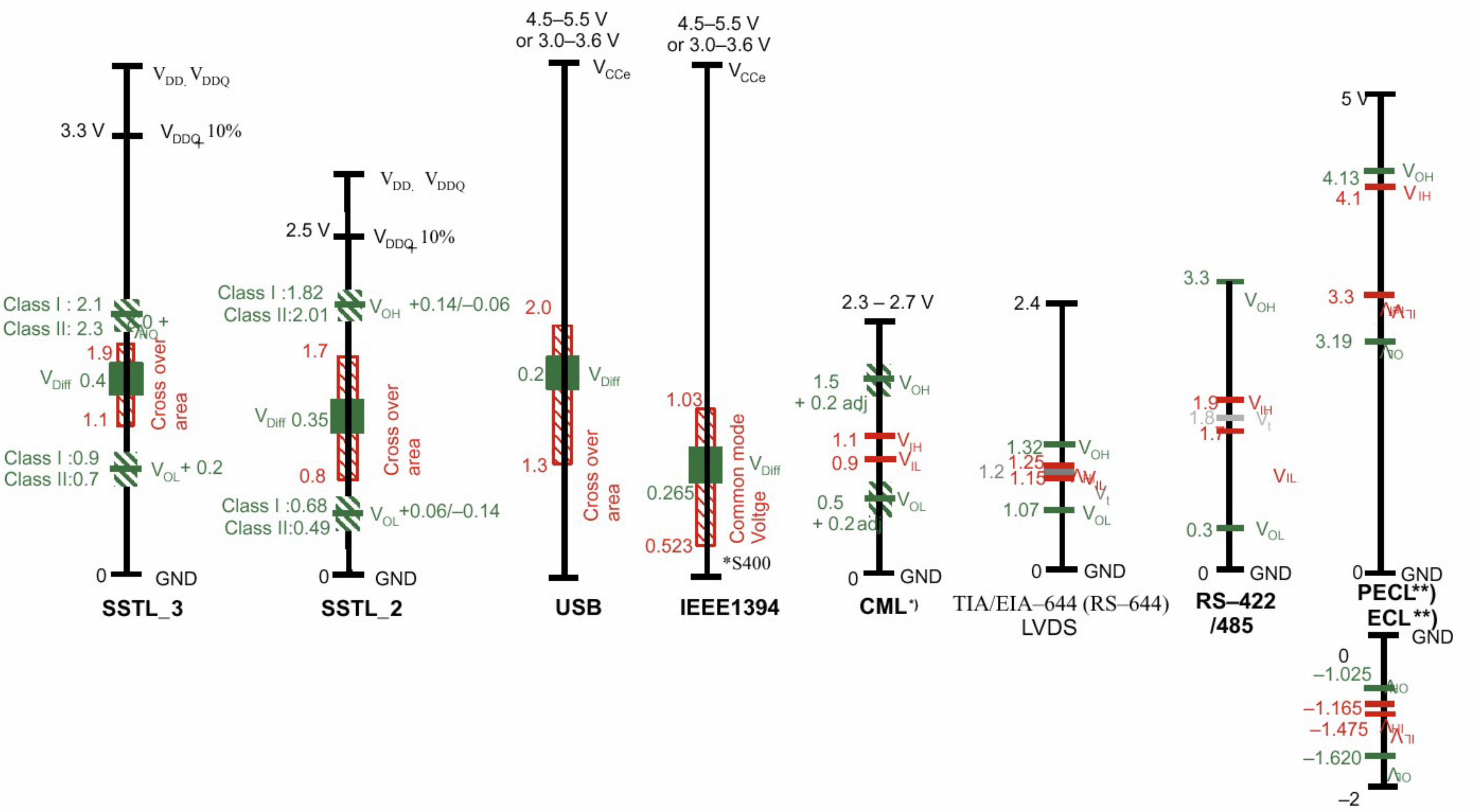
- COMMON and SOURCE-SYNCHRONOUS IO
- Transmission Line Refresher
- IO Signaling
- IO Driver & Receiver Circuit Topologies
  - Resistance Compensation
  - Slew Rate Control
- Mixed Voltage Designs
- Differential Designs
  - HDMI
  - MIPI-DSI
  - MIPI-CSI

Single-ended Bus Signaling Standards



Courtesy Mike Morrow, UW

Differential Bus Signaling Standards



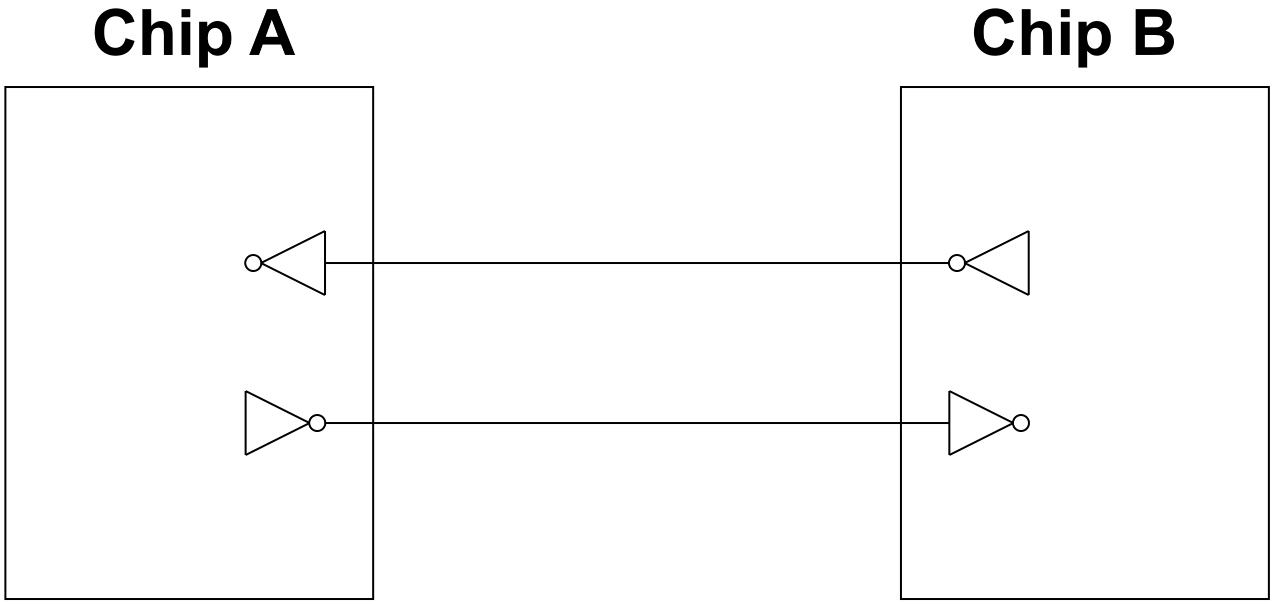
*) The DC offset (transmit Common Mode Voltage Range) for V /V_{OH} and V_{IL}/V_{IH} levels is adjustable in the full supply range

**) levels vary with family an among vendors

Courtesy Mike Morrow, UW

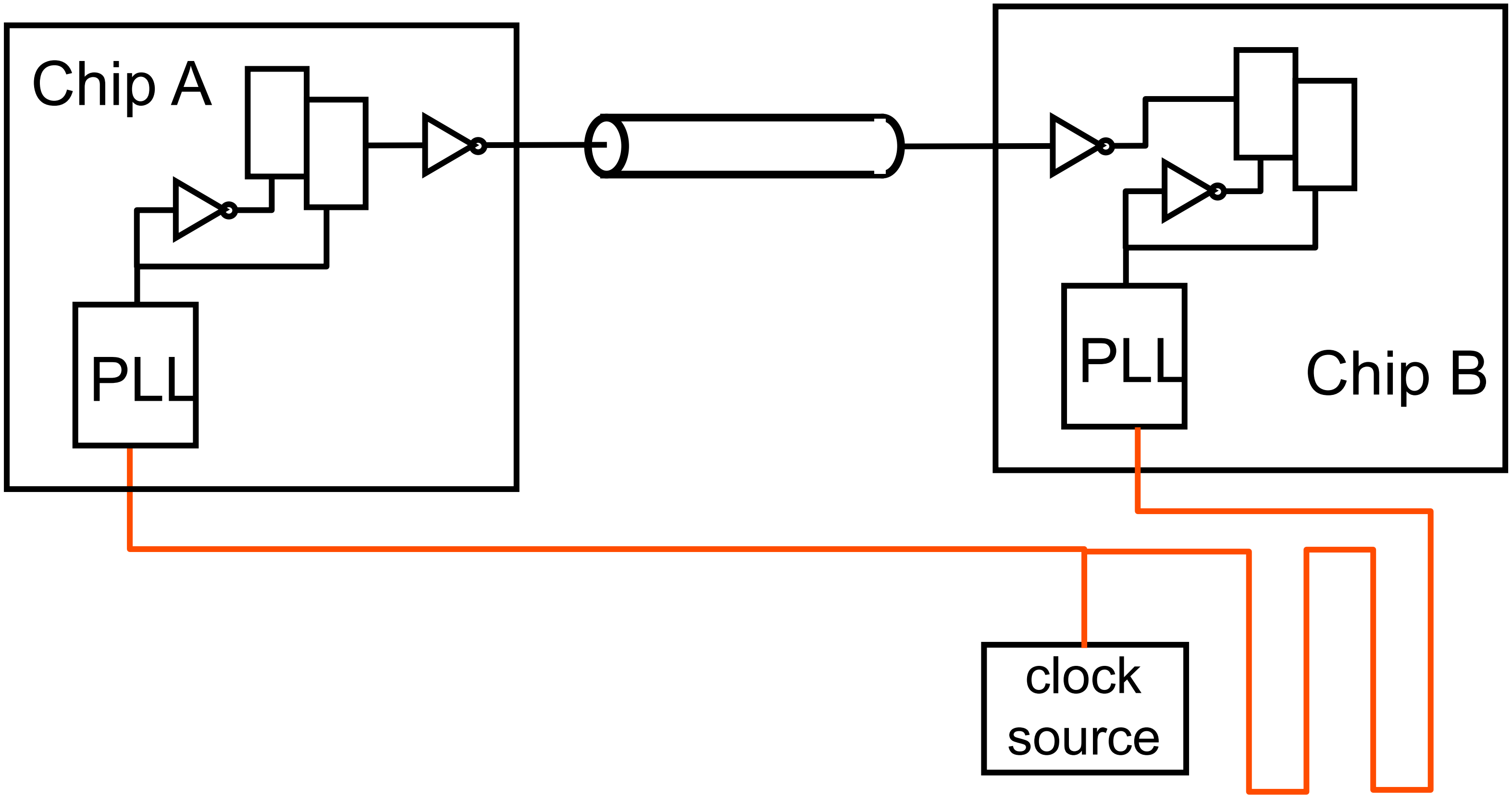
What is the Goal of I/O Design ?

- Send 1’s and 0’s chip to chip
  - Can it be accomplished with simple inverters?
  - Transmit data at the highest frequency with minimal errors.



COMMON CLOCK TRANSFERS

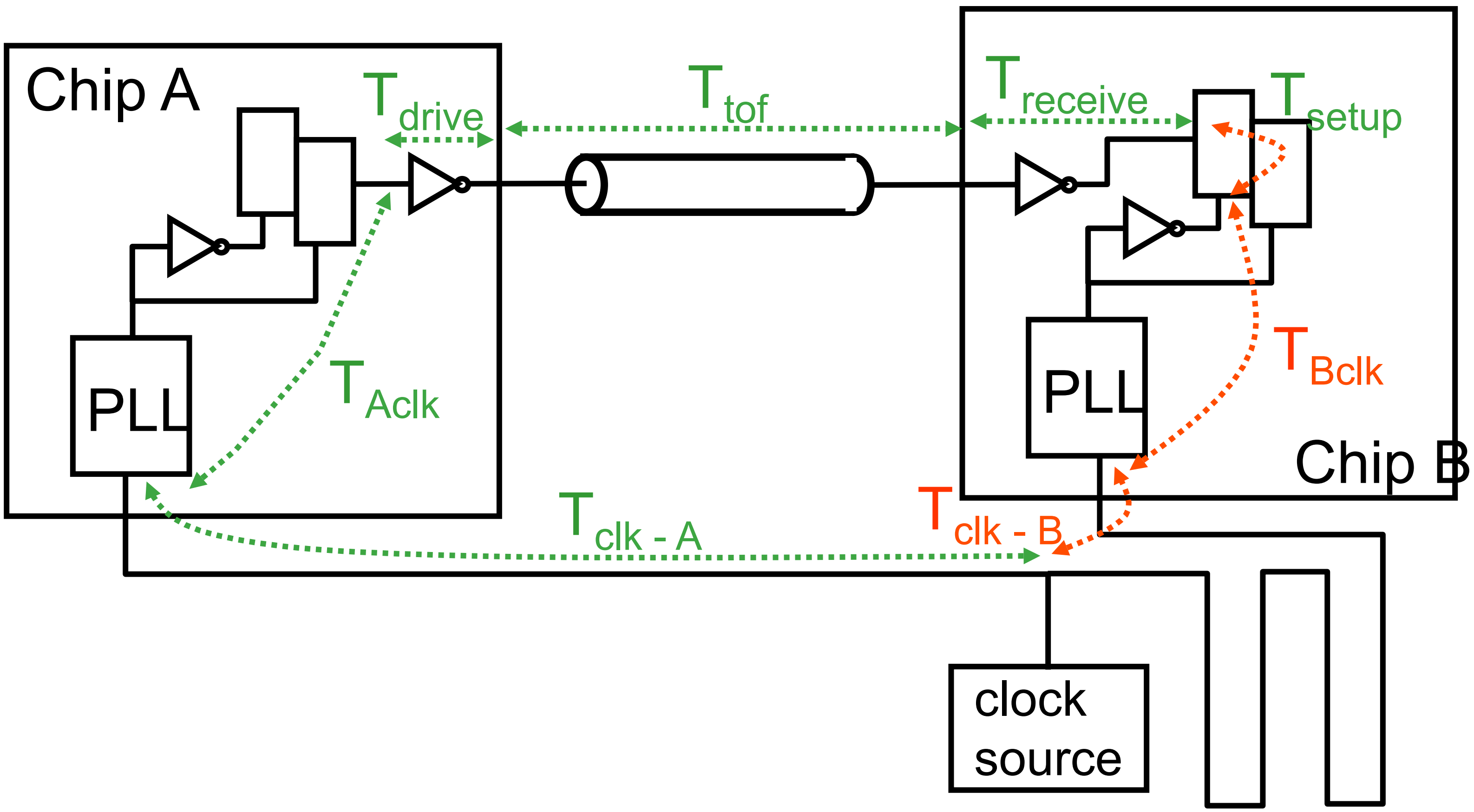
- Chip to chip transfers controlled by common bus clock
- Equal length card routes to each chip & on-chip PLL’s minimize clock skew



COMMON CLOCK TRANSFERS

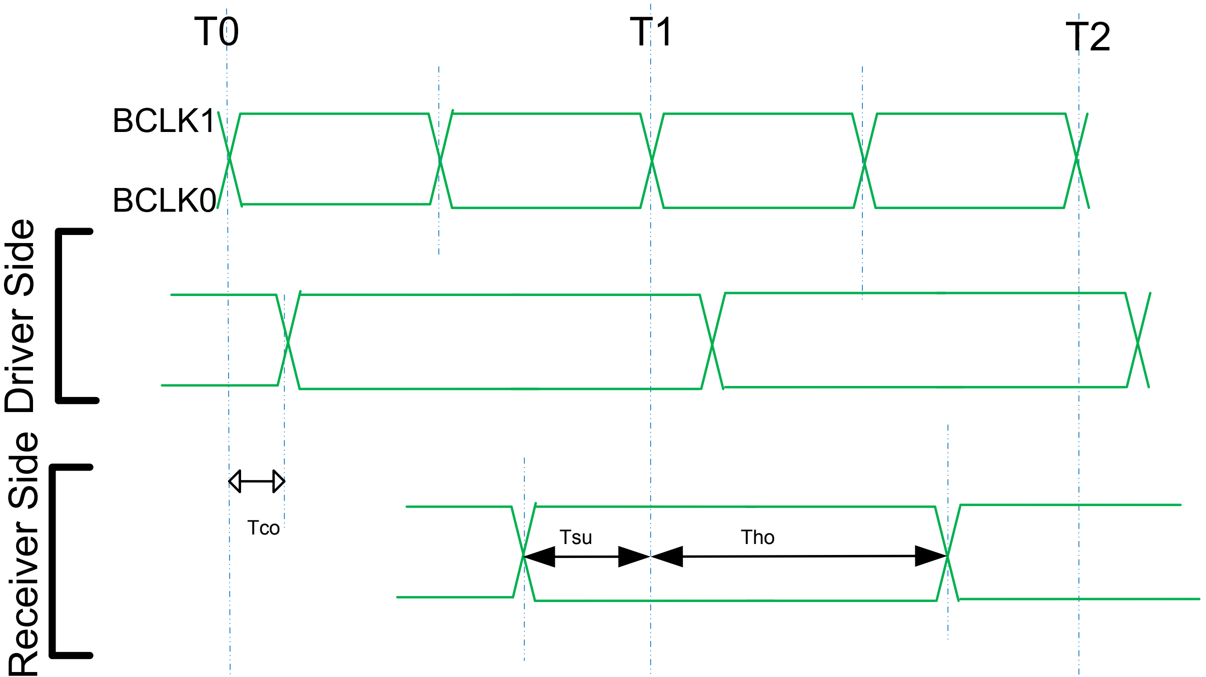
Cycle time to meet setup time

$\max(T_{clk-A}+T_{Aclk}+T_{drive}+T_{tof}+T_{receive}+T_{setup}) - \min(T_{Bclk}-T_{clk-B}) < T_{cycle}$



COMMON CLOCK IO TIMING

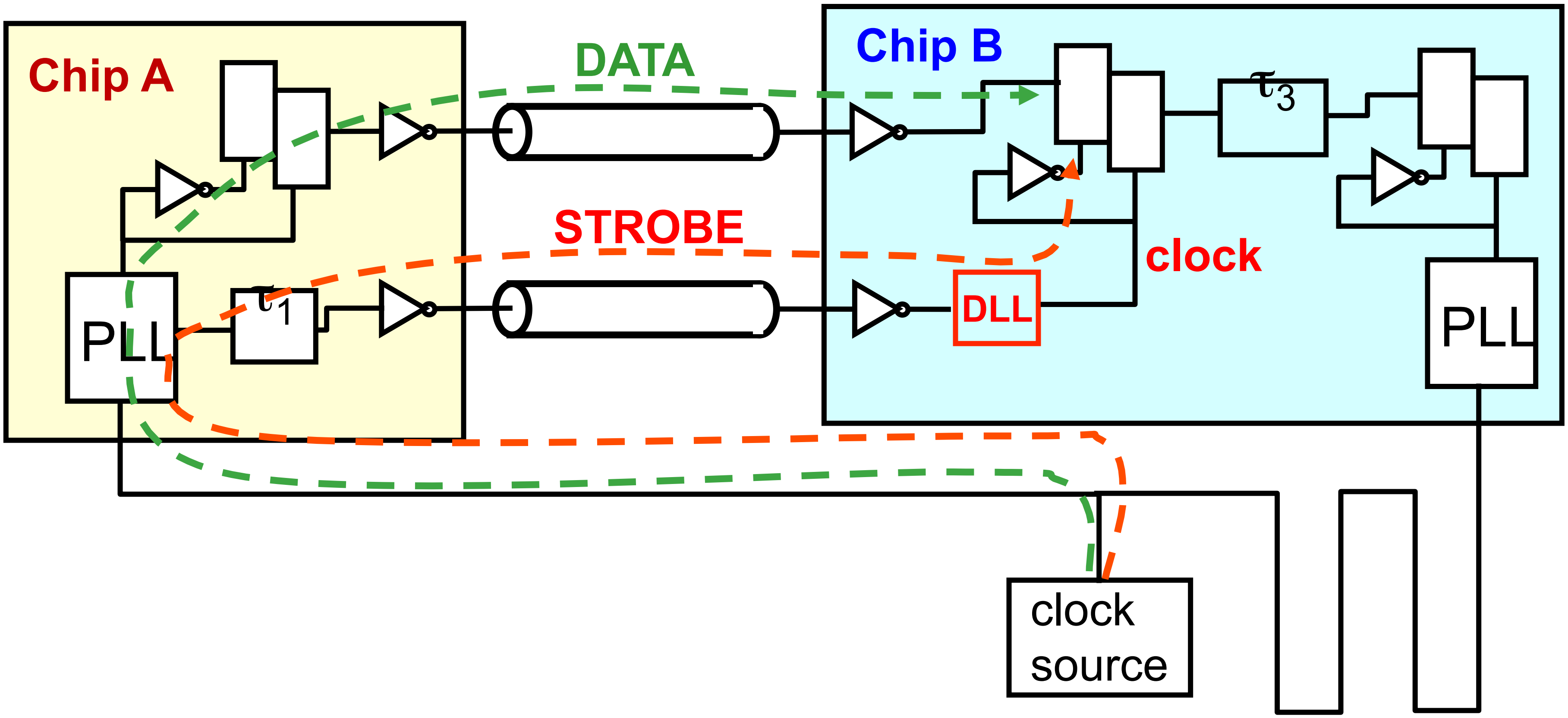
83/100Mhz Common Clock signal



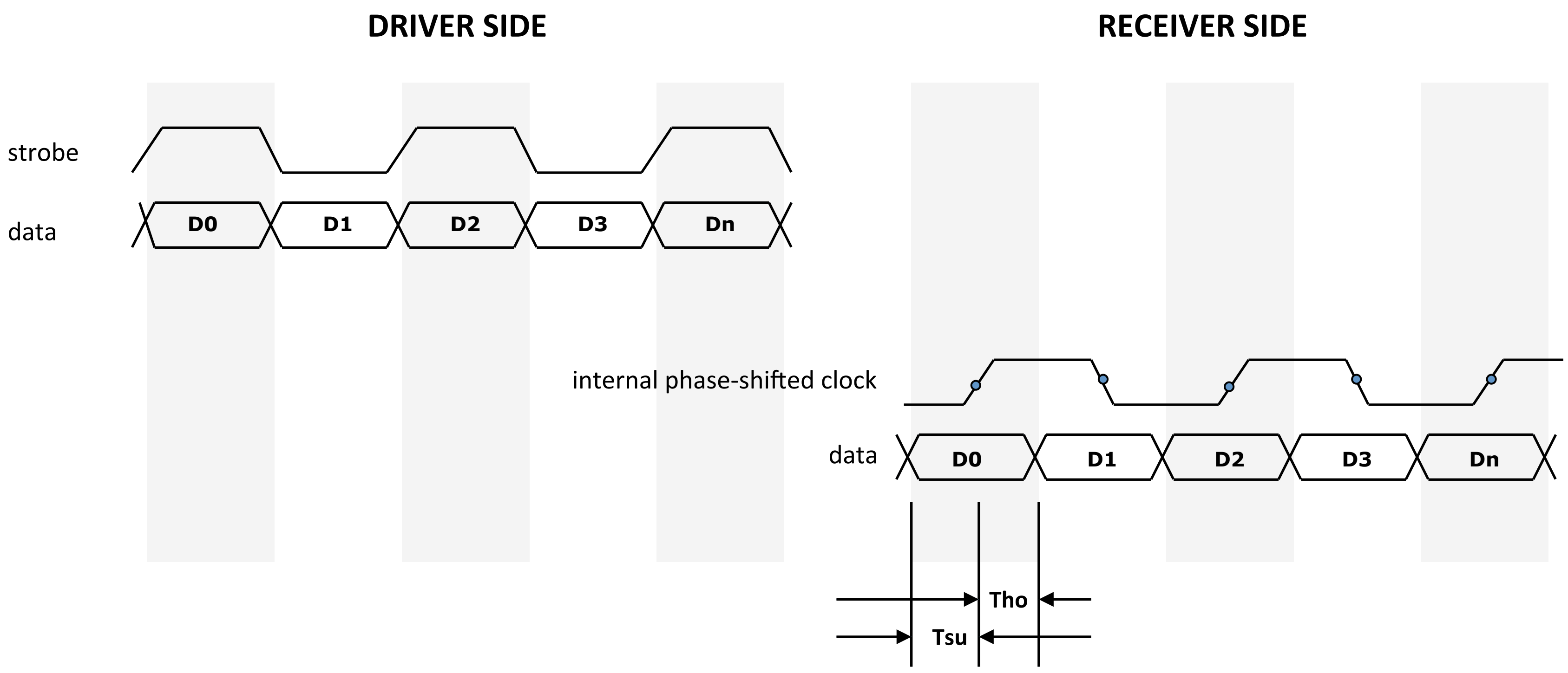
Common Clock	T10	TcoC	CC output valid delay
	T11	TsuC	CC input setup time
	T12	ThoC	CC input hold time

SOURCE SYNCHRONOUS I/O

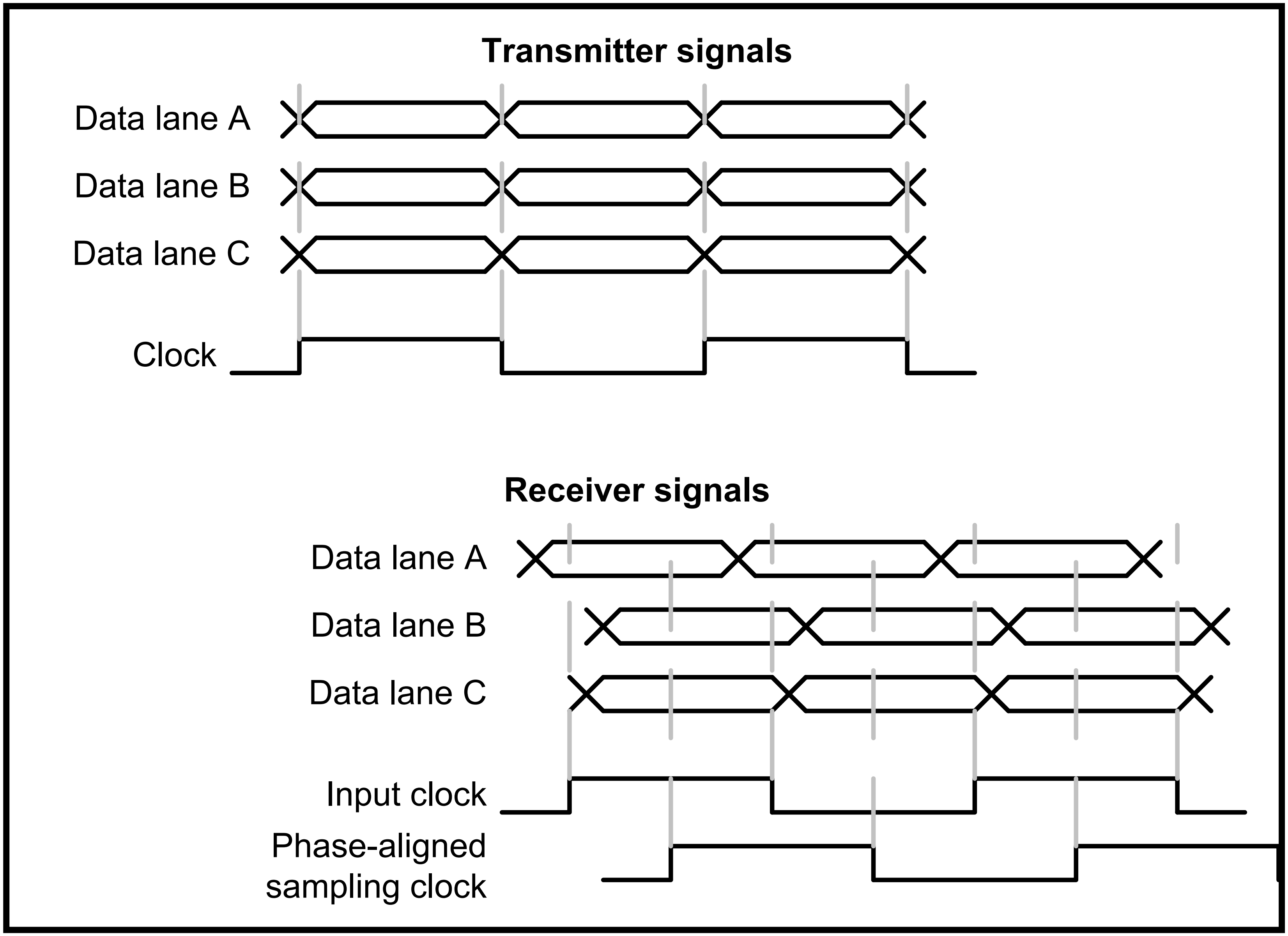
- Send source clock with source data
- Resolve clock phase differences with t_1, t_2, & t_3



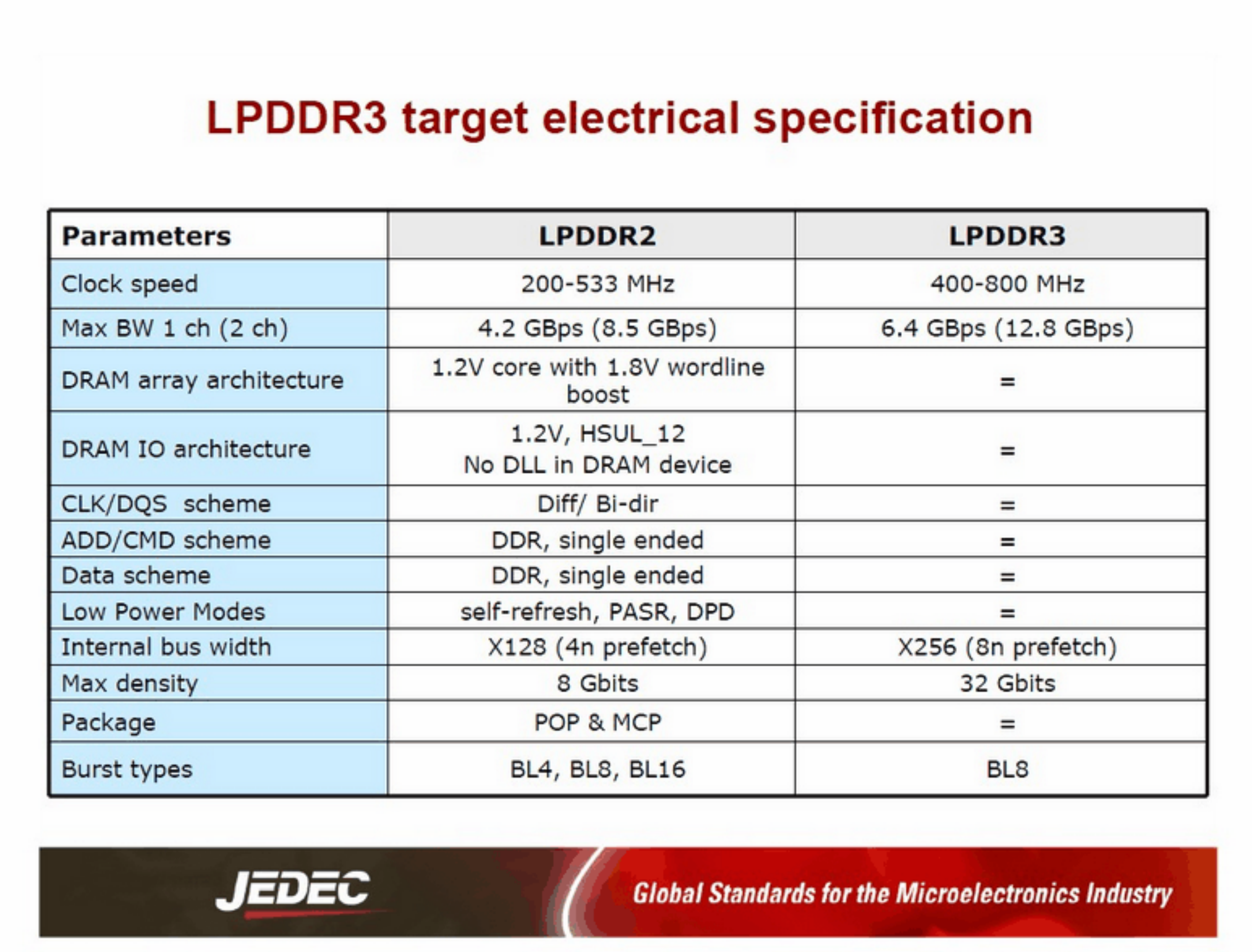
DDR SOURCE SYNCHRONOUS



SKEW in IO SIGNALING



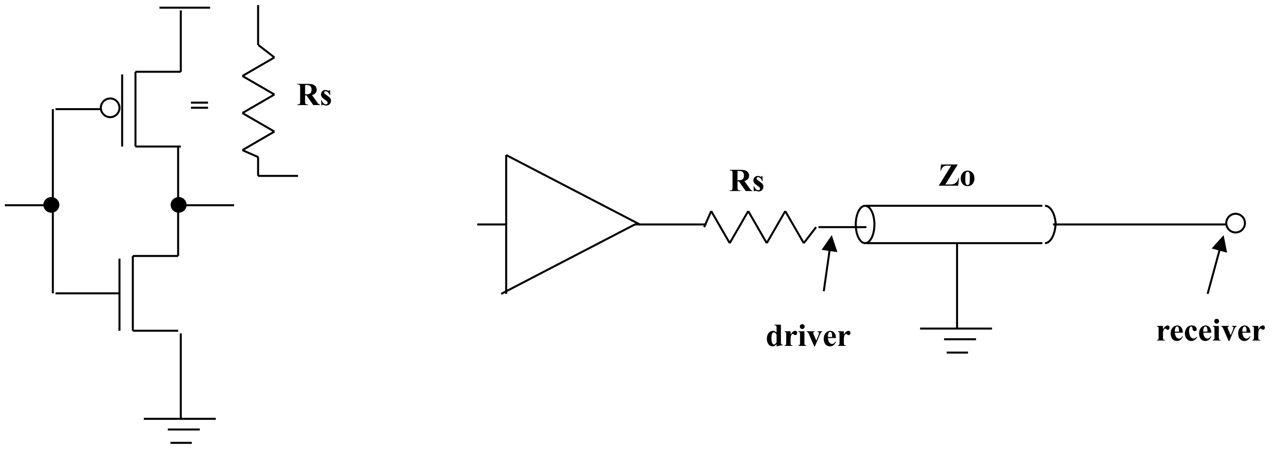
LPDDR SPECS

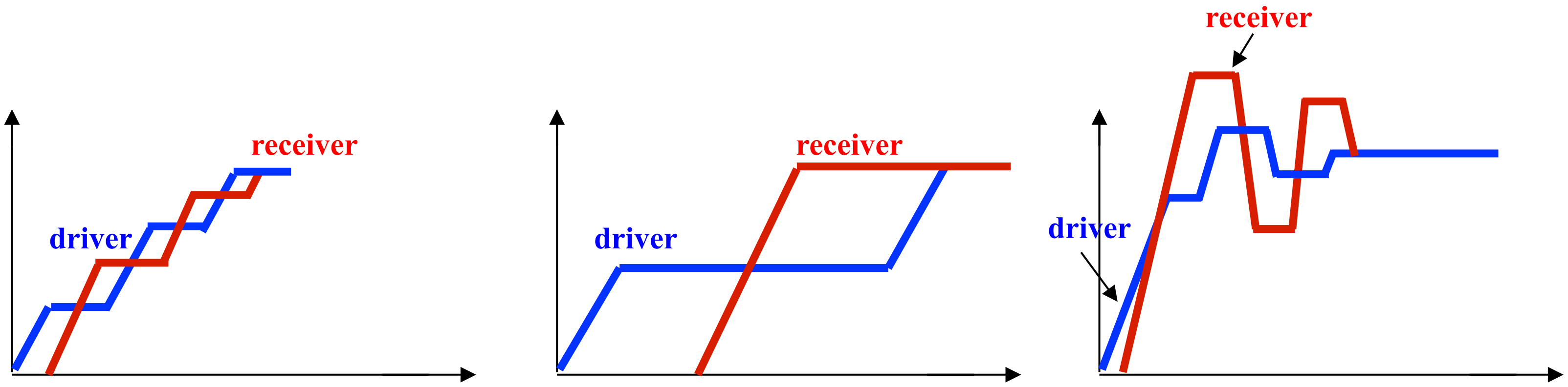


LPDDR3 target electrical specification

Parameters	LPDDR2	LPDDR3
Clock speed	200-533 MHz	400-800 MHz
Max BW 1 ch (2 ch)	4.2 GBps (8.5 GBps)	6.4 GBps (12.8 GBps)
DRAM array architecture	1.2V core with 1.8V wordline boost	=
DRAM IO architecture	1.2V, HSUL_12 No DLL in DRAM device	=
CLK/DQS scheme	Diff/ Bi-dir	=
ADD/CMD scheme	DDR, single ended	=
Data scheme	DDR, single ended	=
Low Power Modes	self-refresh, PASR, DPD	=
Internal bus width	X128 (4n prefetch)	X256 (8n prefetch)
Max density	8 Gbits	32 Gbits
Package	POP & MCP	=
Burst types	BL4, BL8, BL16	BL8

CMOS signaling (series termination)



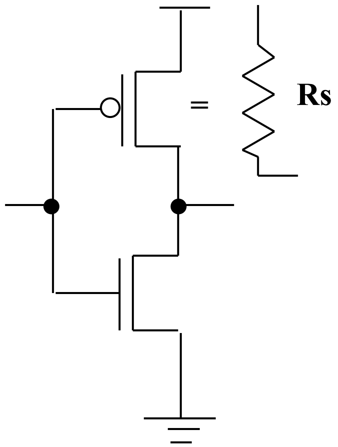


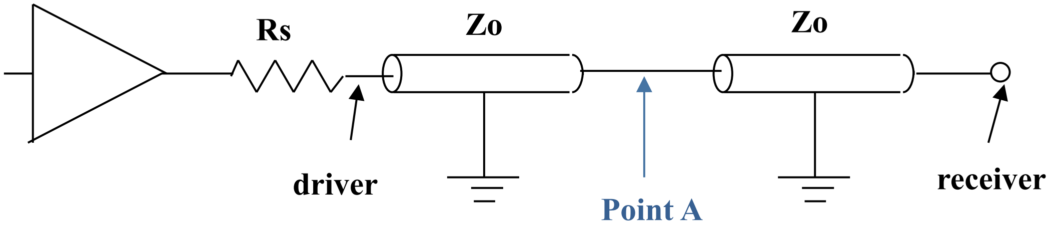
Underdriven :
Rs > Zo

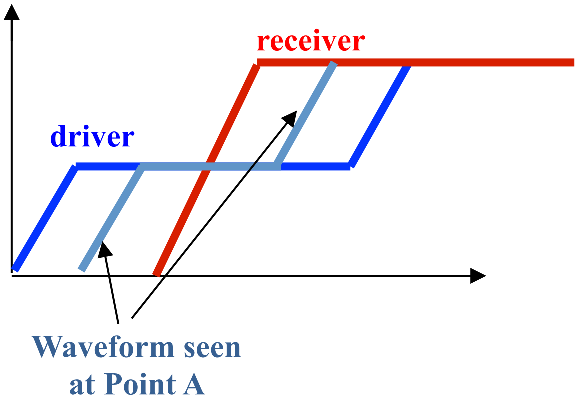
Matched :
Rs = Zo

Overdriven :
Rs < Zo

CMOS signaling (series termination)

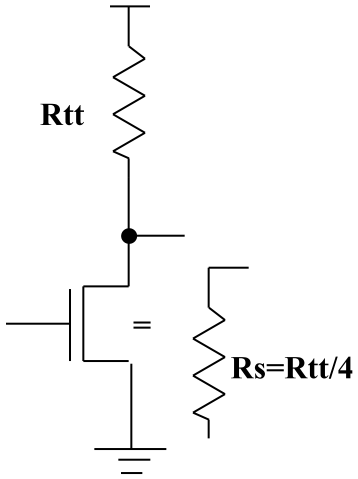


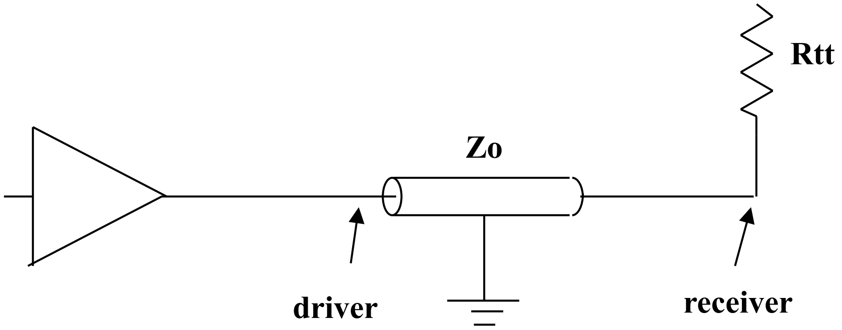


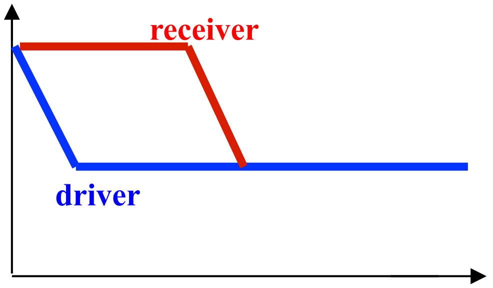


Agents along the bus (Point A) would have to wait for reflected signal to return from the end before seeing full transition, requiring a larger timing budget

GTL signaling (parallel termination)



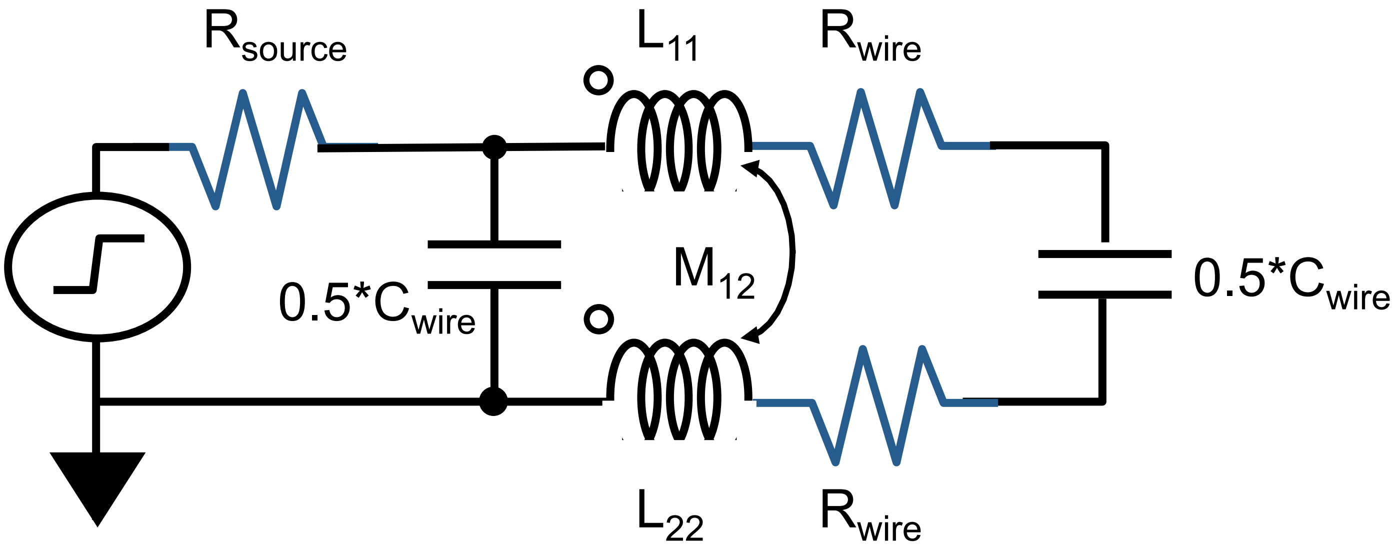




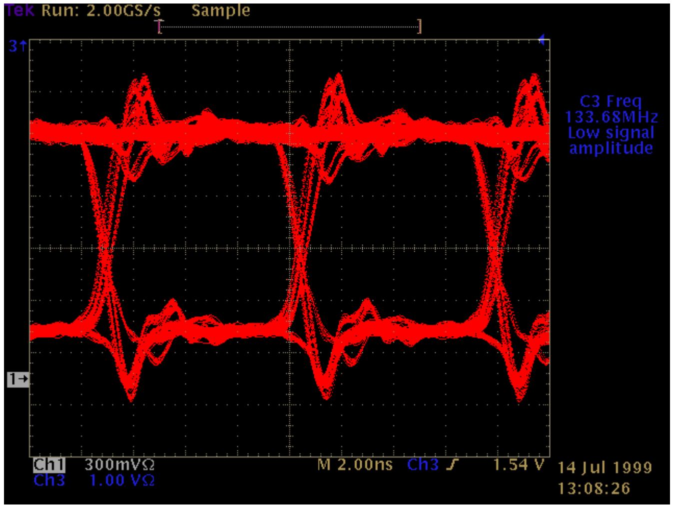
- Signal typically switches from 1/3 Vcc to Vcc
- Wave is absorbed at Receiver (no reflection) if Rtt = Zo

TRANSMISSION LINES

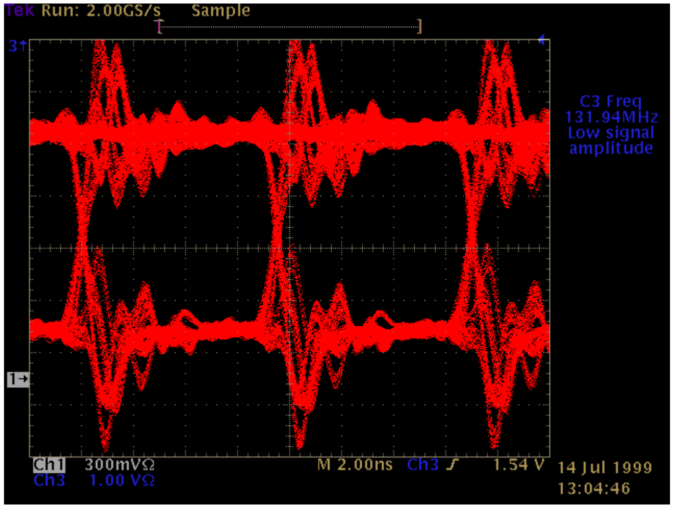
Twin lead transmission line modeled as a single section and driven by a THEVENIN source.



Effects of edge rate on Signal quality

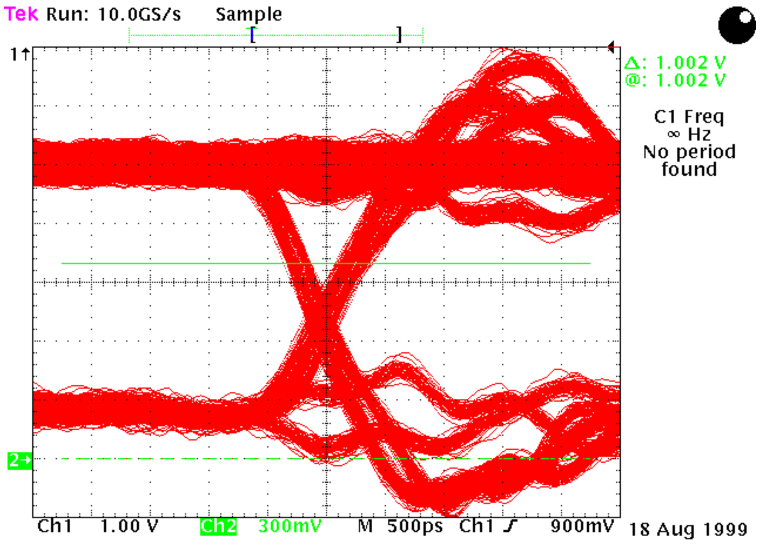


Slower edge rates reduce Overshoot and Ringback



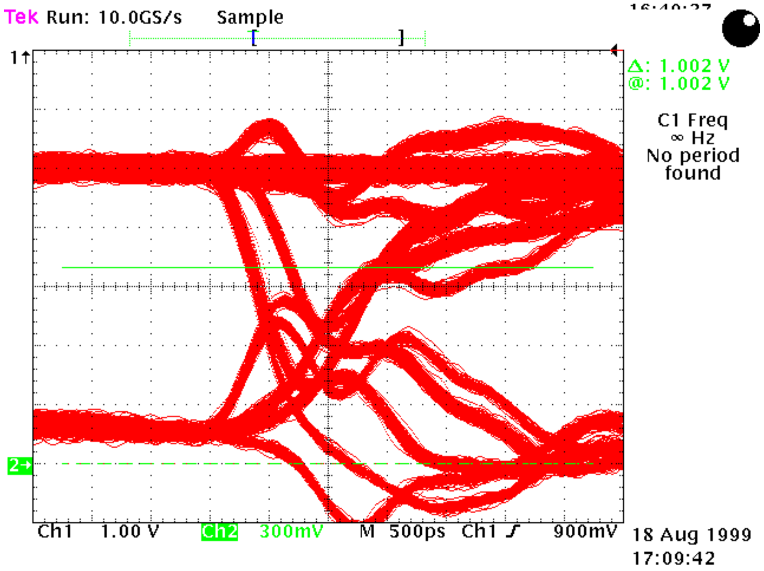
Faster edge rates increase Overshoot and Ringback

SIGNAL INTEGRITY



Acceptable Signal Quality

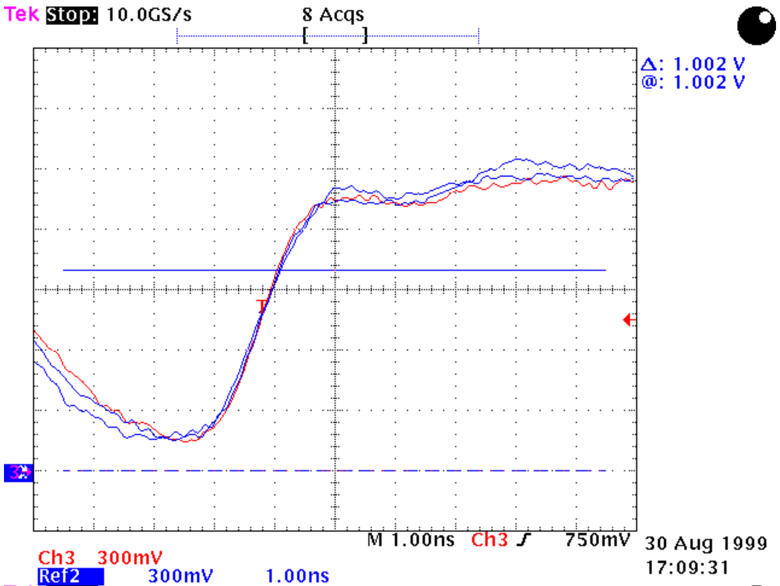
Fairly open “EYE”



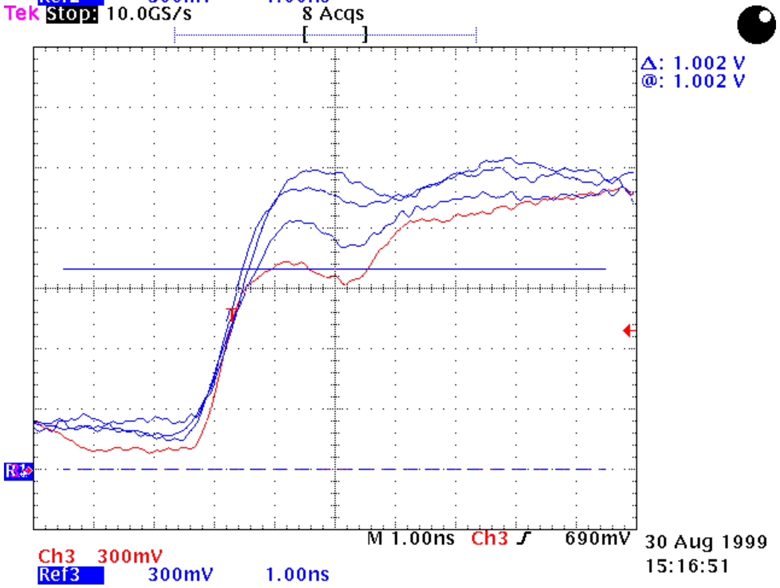
POOR Signal Quality

Closed “EYE”

IMPEDANCE MATCHING



Rs and Zo Matched



Rs > Zo

QUESTION

- **Assuming transmission like propagation delay is 150ps per inch and a transmission line is 2 inch long, how fast does the edge rate needs to be to have transmission line effects on the wire?**

Driver source impedance $\boldsymbol{R_s}$ is considered to be low when $\boldsymbol{R_s < Z_o}$ (line impedance).

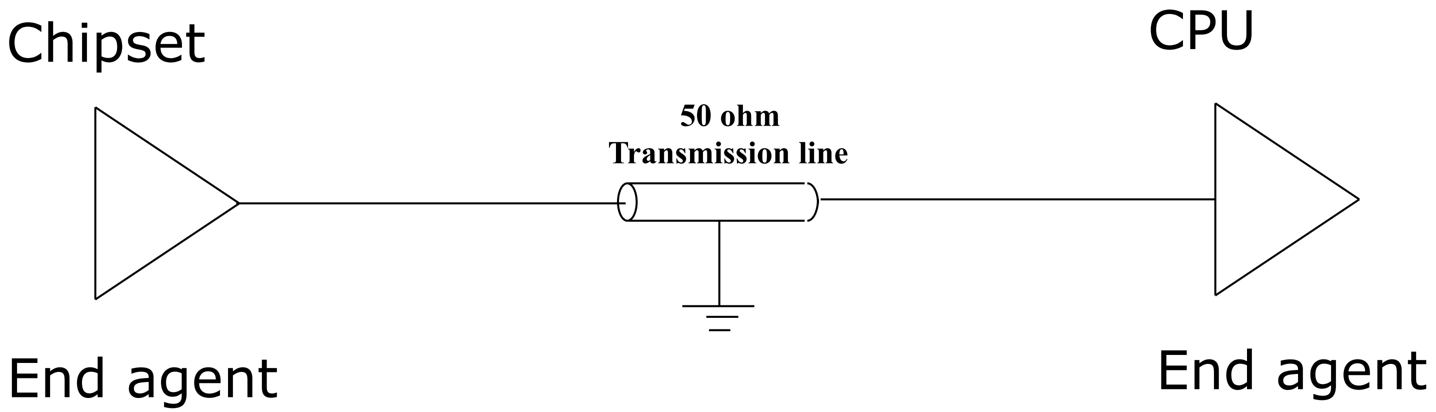
Driver rise time $\boldsymbol{t_r}$ is considered fast if $\boldsymbol{t_r < 2.5\, t_f}$ where $\boldsymbol{t_f}$ is trace time of flight.

FACTORS AFFECTING IO PERFORMANCE

- **Impedance matching**
- **Edge rate**
- **Signal coupling**
- **Power supply noise**
- **ISI (Inter-Symbol Interference)**

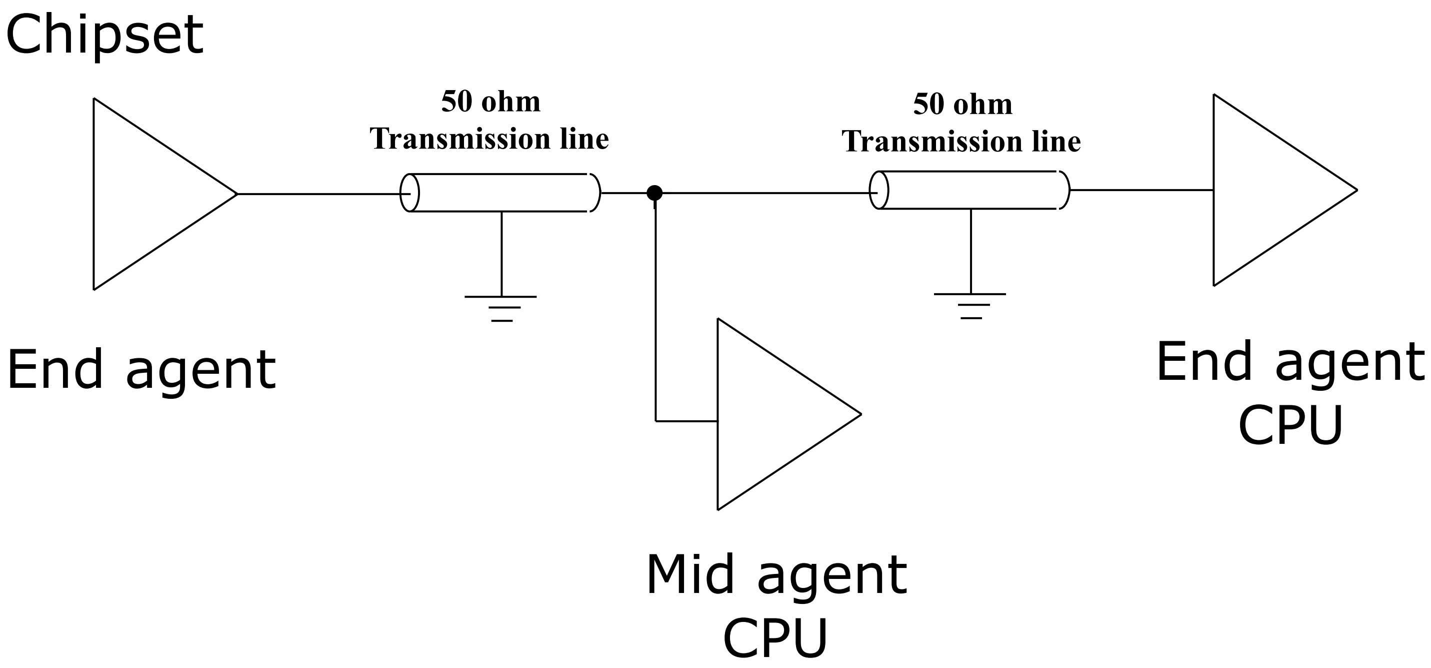
IO DRIVER & RECEIVER CIRCUIT TOPOLOGIES

POINT to POINT BUS



Only two agents reside on the bus and are located at the extreme ends of the bus

Multi-drop Bus



Chipset

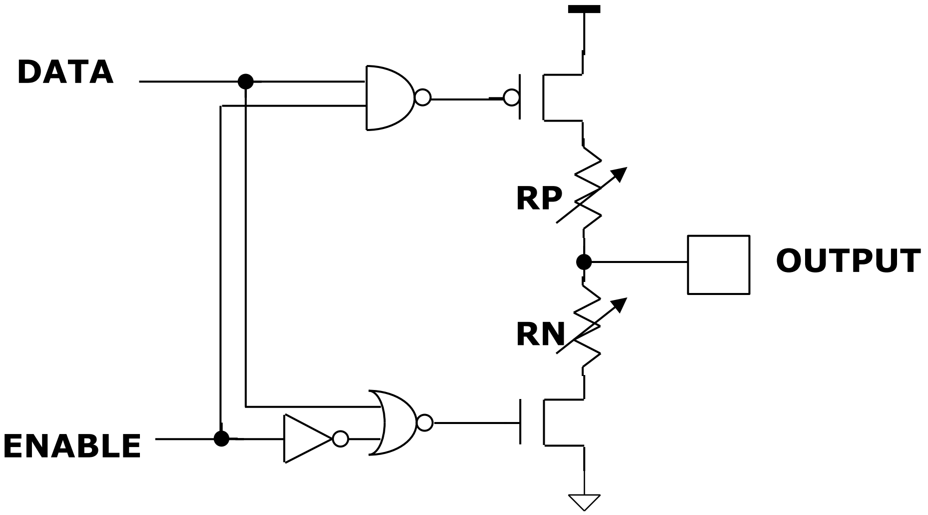
End agent

End agent
CPU

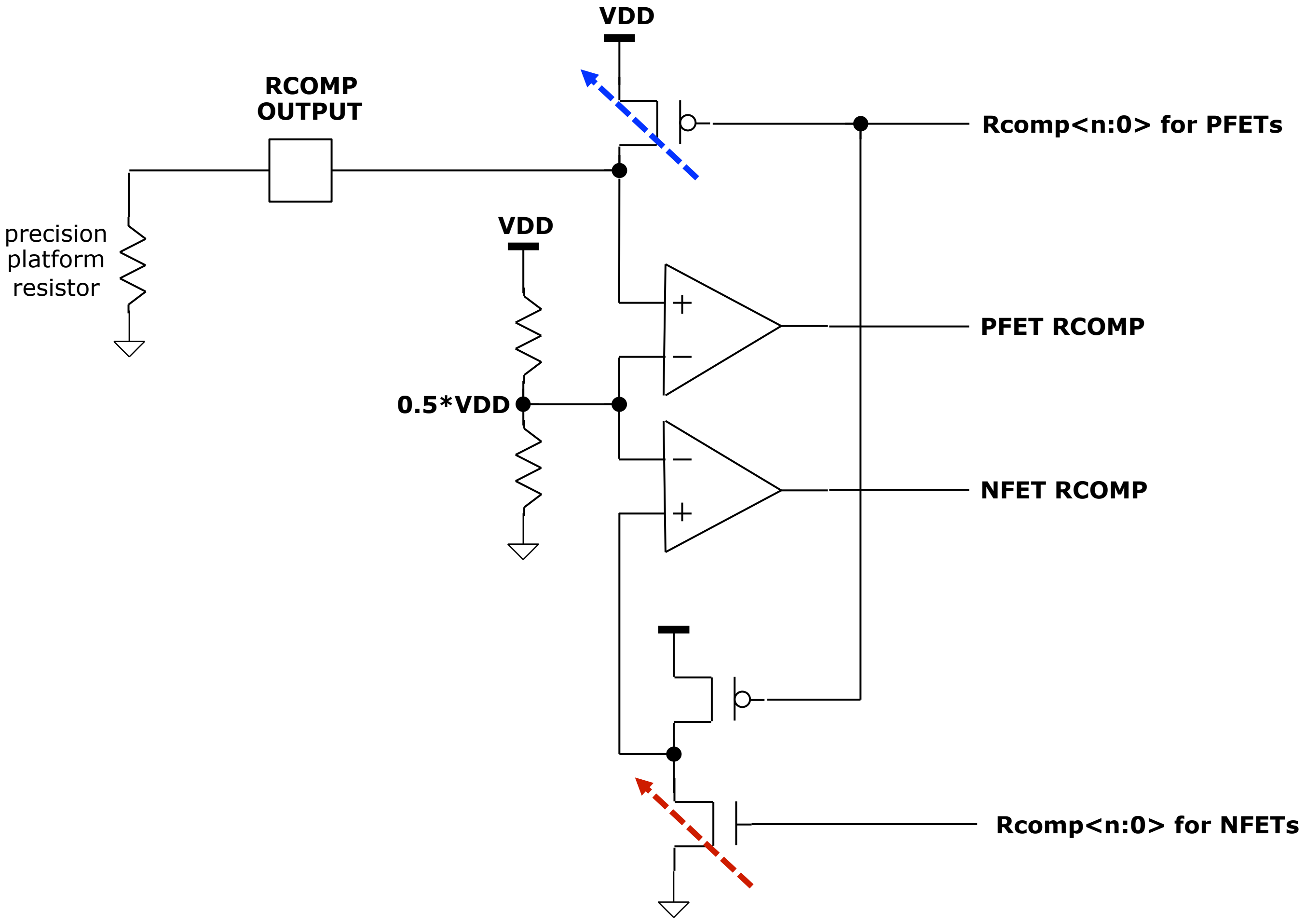
Mid agent
CPU

IMPEDANCE CONTROL

- Given a precise on-chip resistor, this design provides the best impedance control
- R varies with PVT variability.
- Slew rate changes per PVT.
- Need:
  - Dynamic constant Compensation for Temp change
  - Static Compensation for Process and voltage.
  - R and SLEW compensation topologies

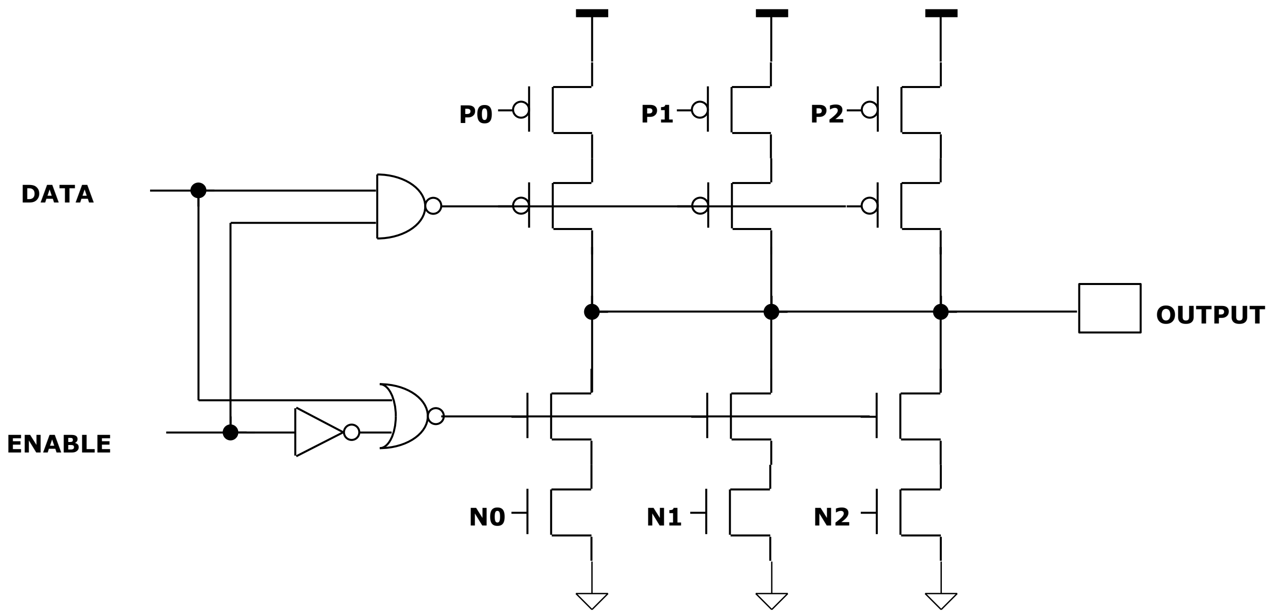


Buffer Resistance Compensation



Tunable Impedance Control

Stacked device settings can be preset or dynamically controlled



Slew Rate Control

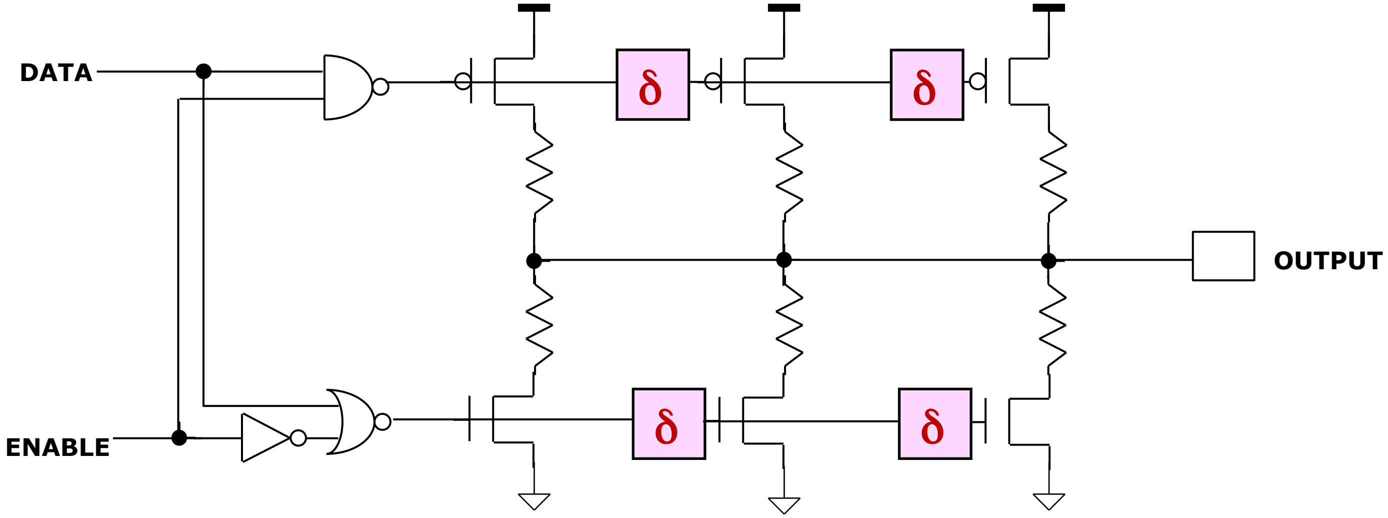
- Output stage slew rate is controlled to reduce noise
  - Cross talk noise
  - Simultaneous switching noise
  - Reflections at discontinuities

- Slew rate control is accomplished by controlling the pre-driver delay and/or pre-driver strength

- Can also be controlled with the addition of Miller capacitance

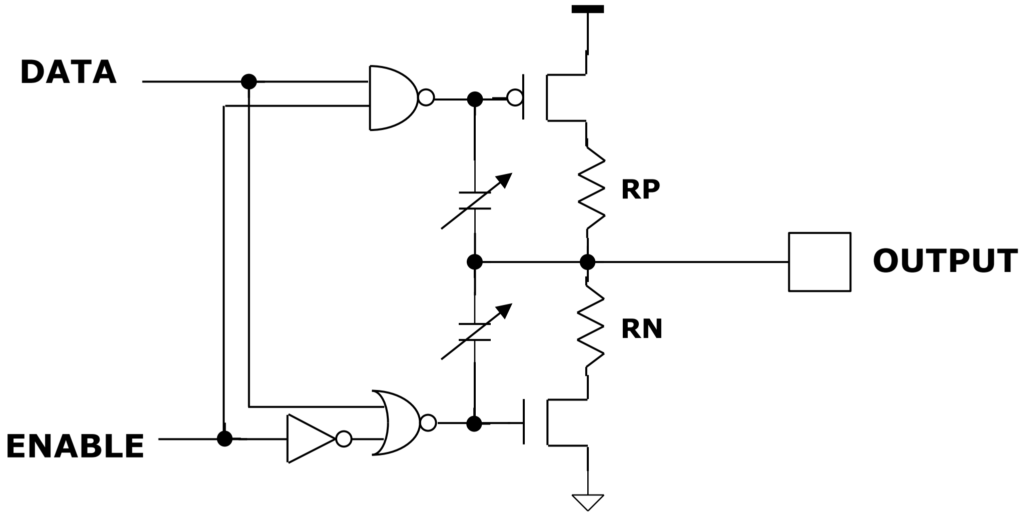
Output Slew Rate Control (1)

- Output stage is divided and pre-drive signal is designed to sequentially arrive at the different sections
- Pre-driver design might even permit crossover currents to guarantee impedance even during switching

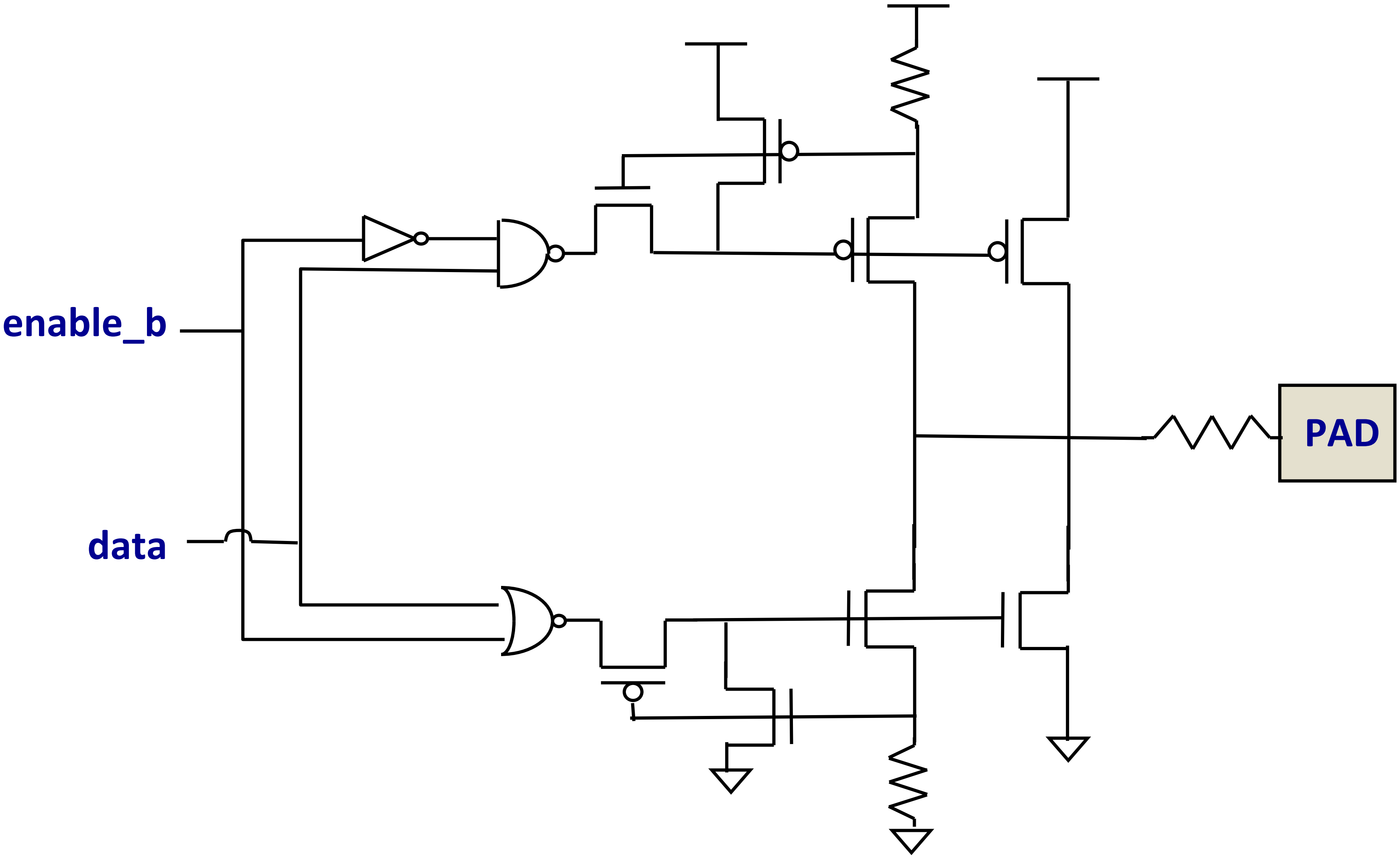


Output Slew Rate Control (2)

- **Adds a tunable Miller capacitance between output and inputs of last stage to control output slew rates.**

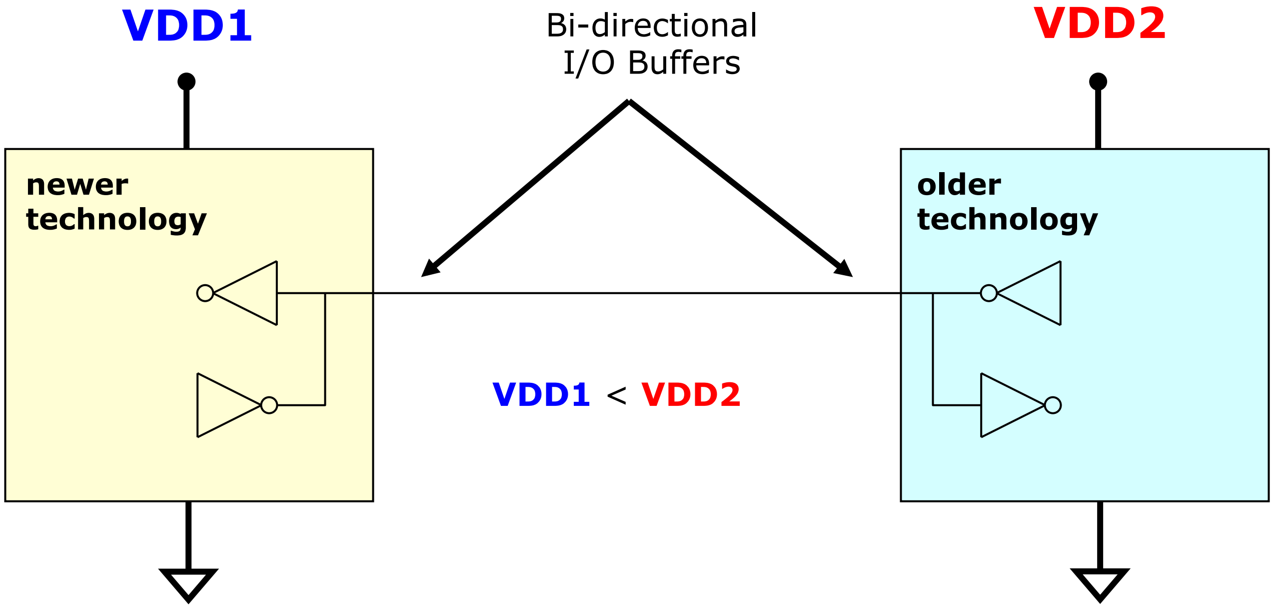


Output Slew Rate Control (3)



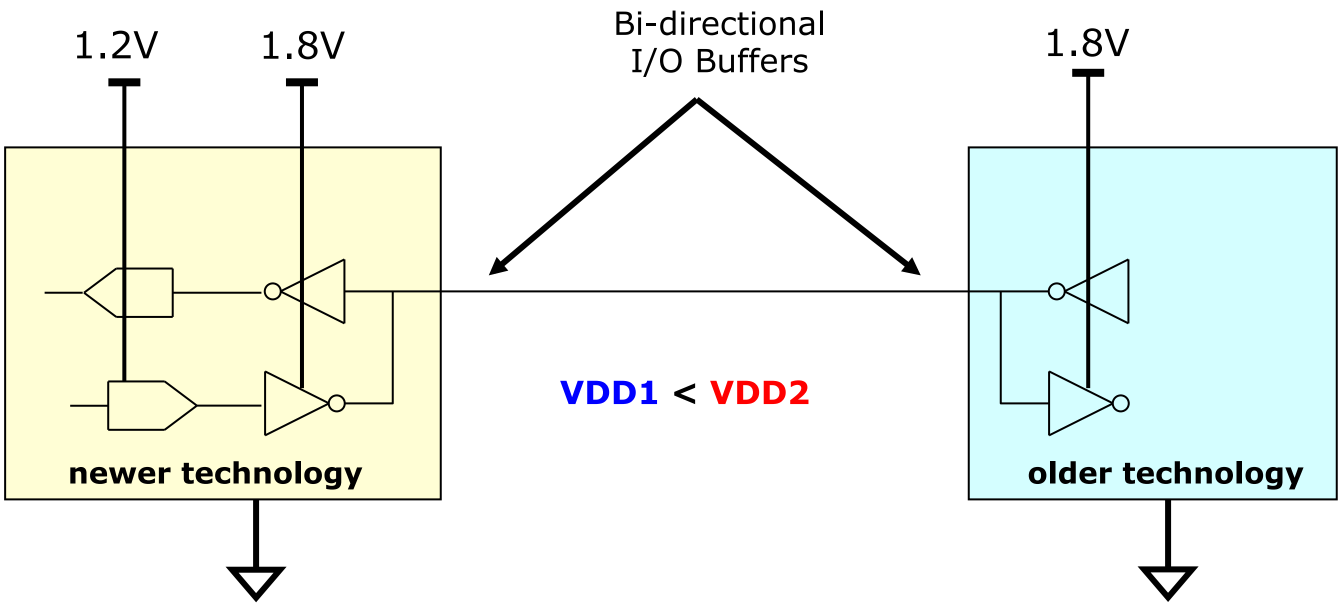
Mixed Voltage Designs

- Needed when chips have different supply voltages
- Low voltage circuits can be damaged by high voltage inputs
- High voltage circuits suffer delay & noise problems when receiving low voltage signals



Dual Supply Designs

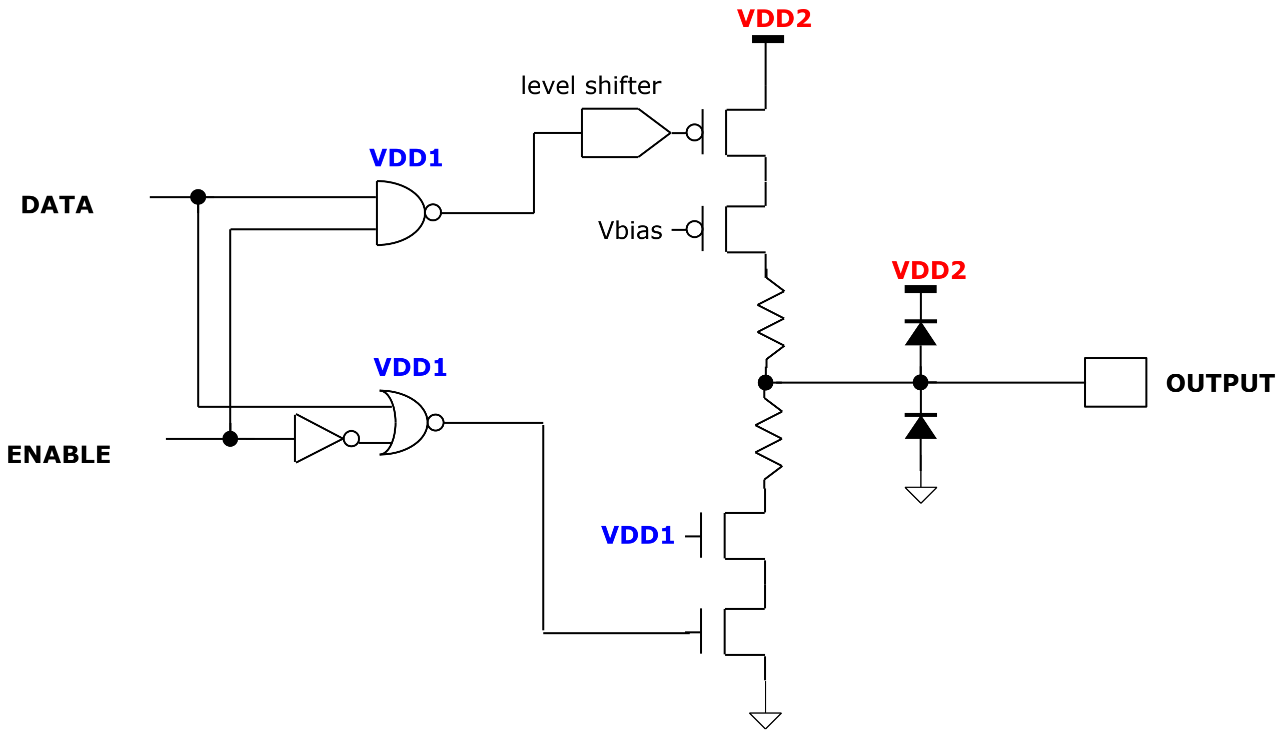
- **Separately power the I/O circuits at a higher voltage**
  - Use level shifters



DUAL SUPPLY DESIGNS

- **Cascode output transistors to support/drive higher voltages.**

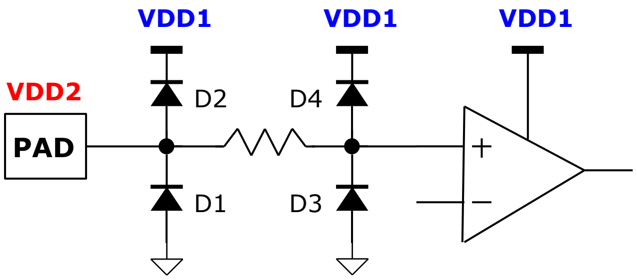
VDD1 < VDD2



INPUT DESIGN for HIGHER VOLTAGES

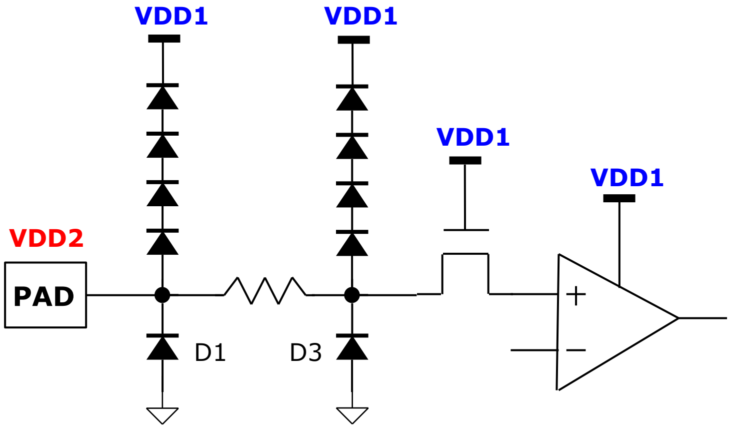
- **Modifications for gate oxide & ESD protection**

Receiving Same Level



VDD2 = **VDD1**

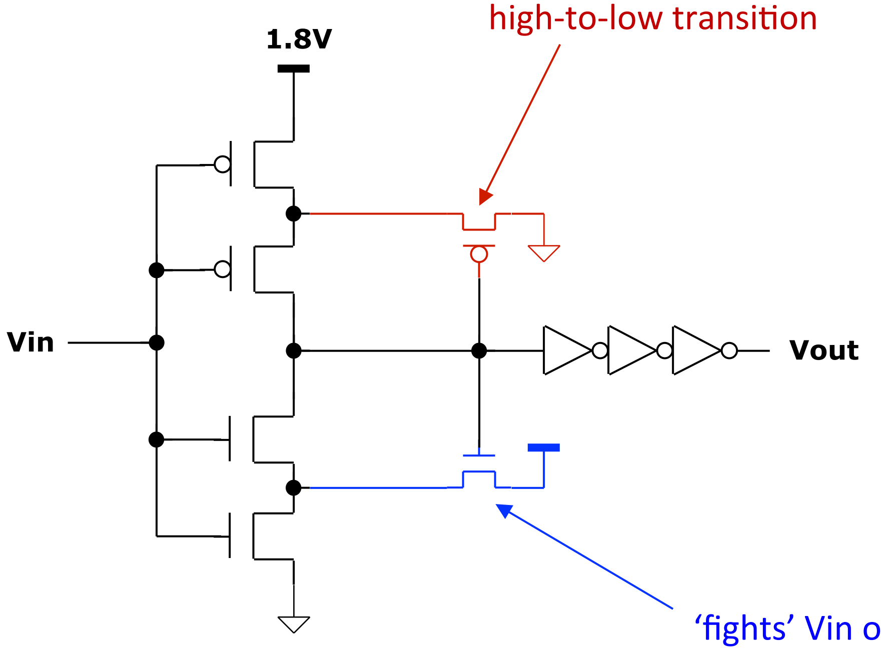
Receiving Higher Level



VDD2 > **VDD1**

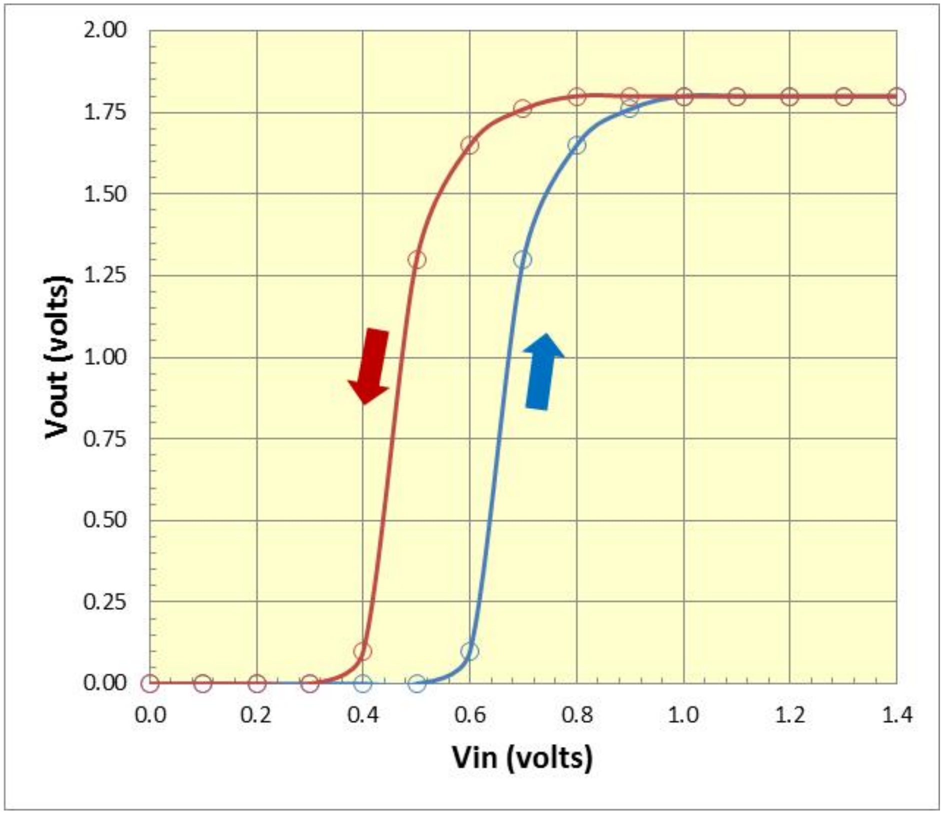
Input Receiver SCHMITT Trigger

adds hysteresis



‘fights’ Vin on the
high-to-low transition

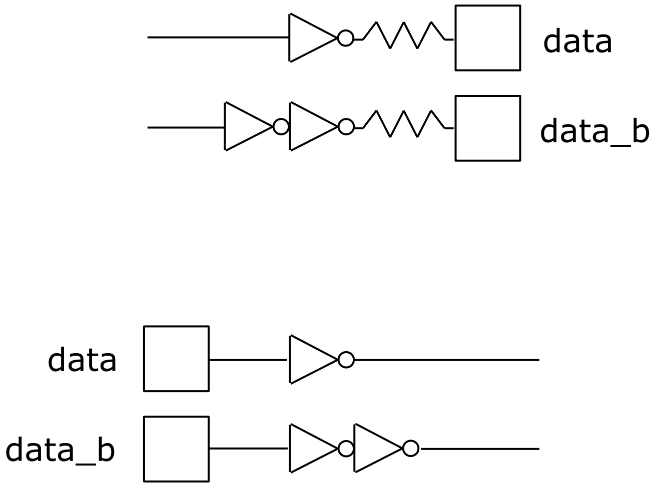
‘fights’ Vin on the
low-to-high transition



Single Ended vs. Differential

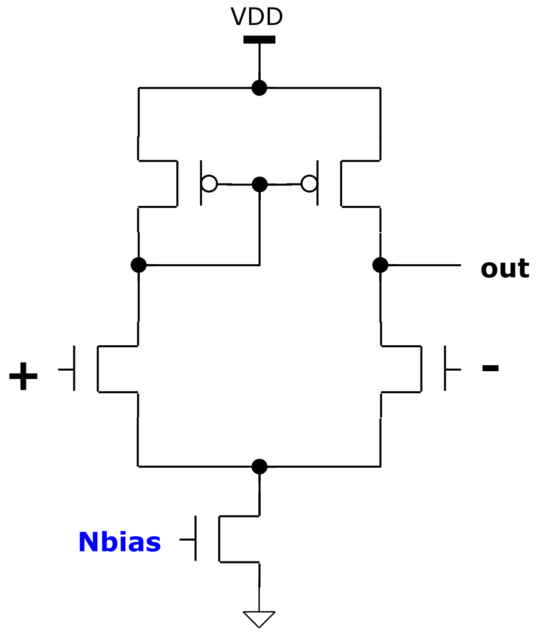
- Differential
  - Reduces simultaneous switching noise
  - Has better common mode noise immunity
  - Receives smaller signal levels
  - Less EMI radiation
  - Must run twice as fast to make sense
    - Consumes twice the number of pins & wiring per bit
  - Layout constraints
    - Symmetrical side-by-side routing & length matching

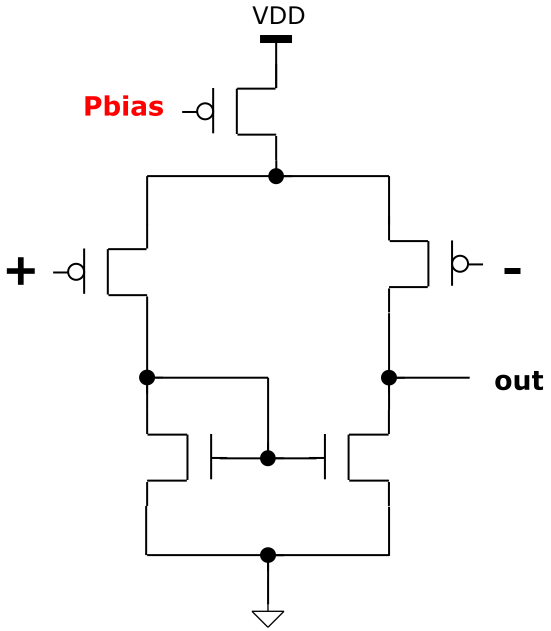
Pseudo Differential using CMOS drivers/receivers



Traditional Biased Differential Receiver

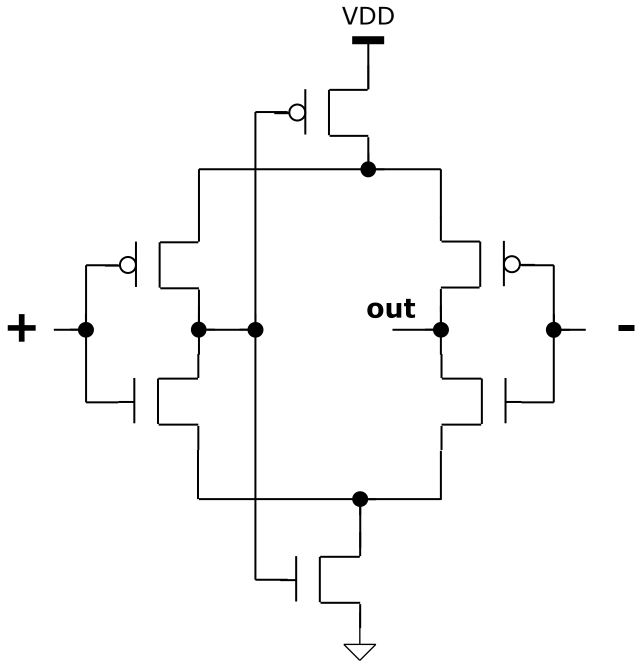
- Traditional differential to single-ended receivers require bias circuits.





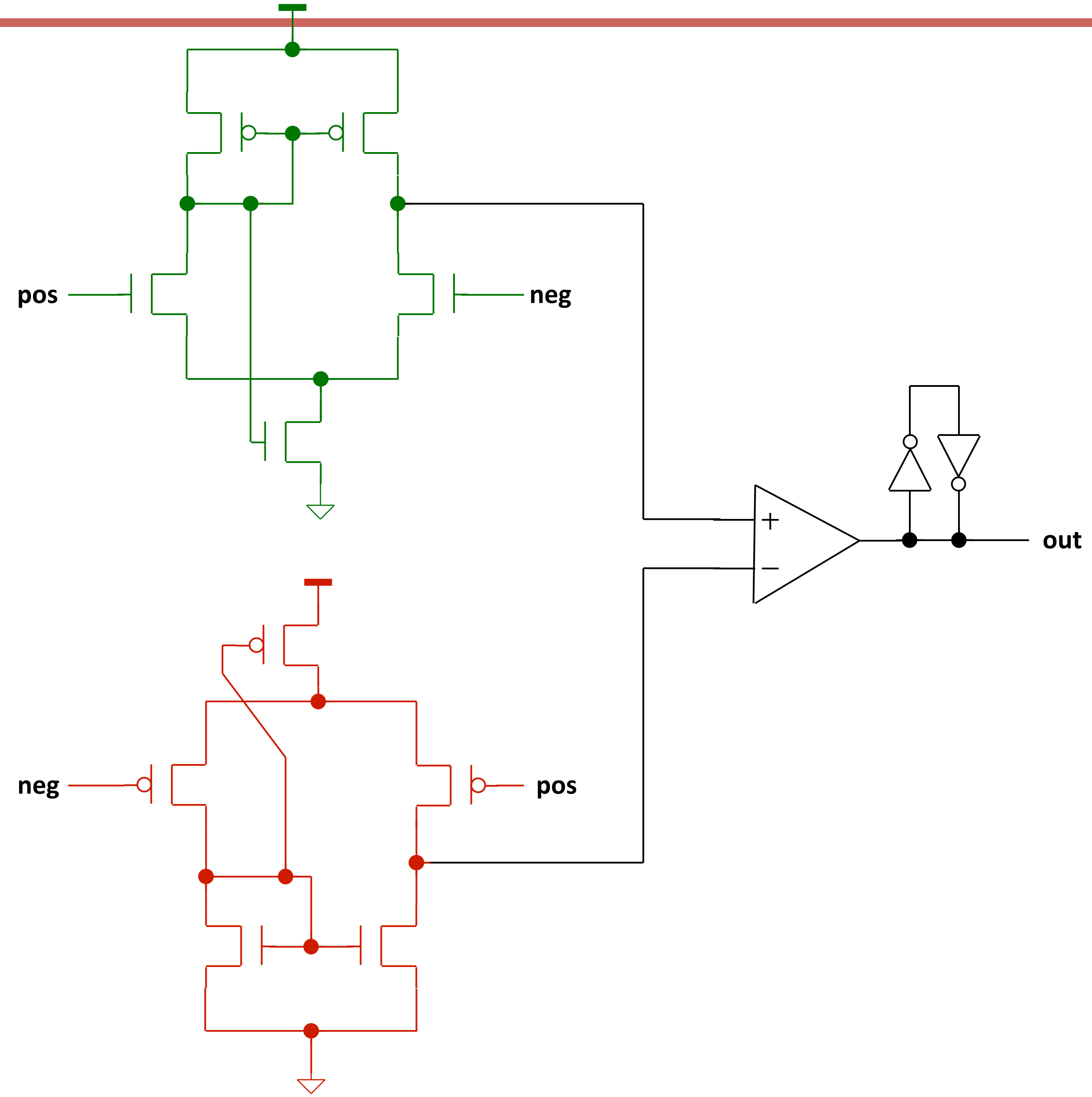
Self-biased Differential Receiver

- **Combines best of NFET and PFET differential receivers**
  - Rail to rail output swing
  - Excellent common mode noise rejection

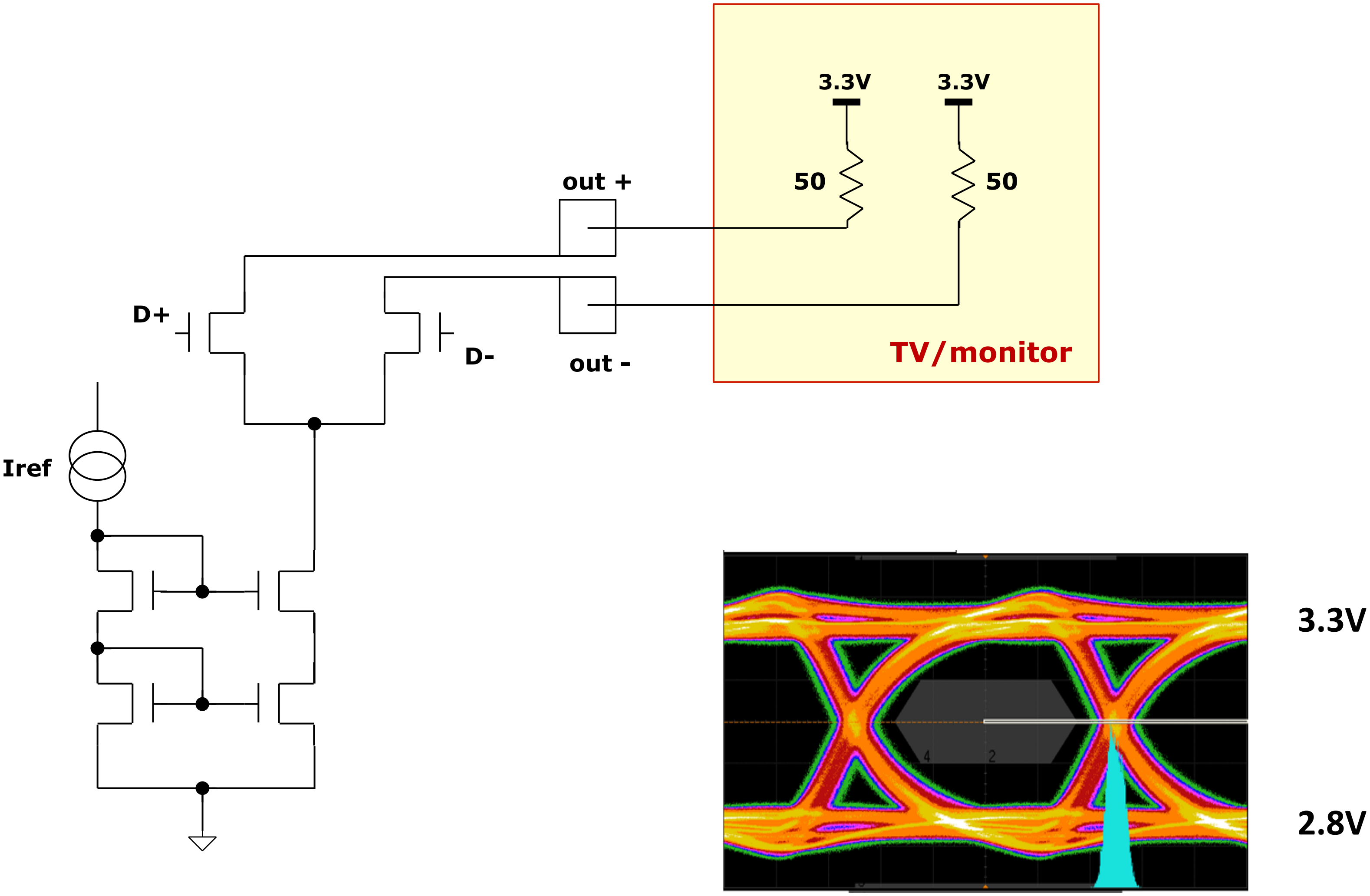


(Bazes, JSSC 91)

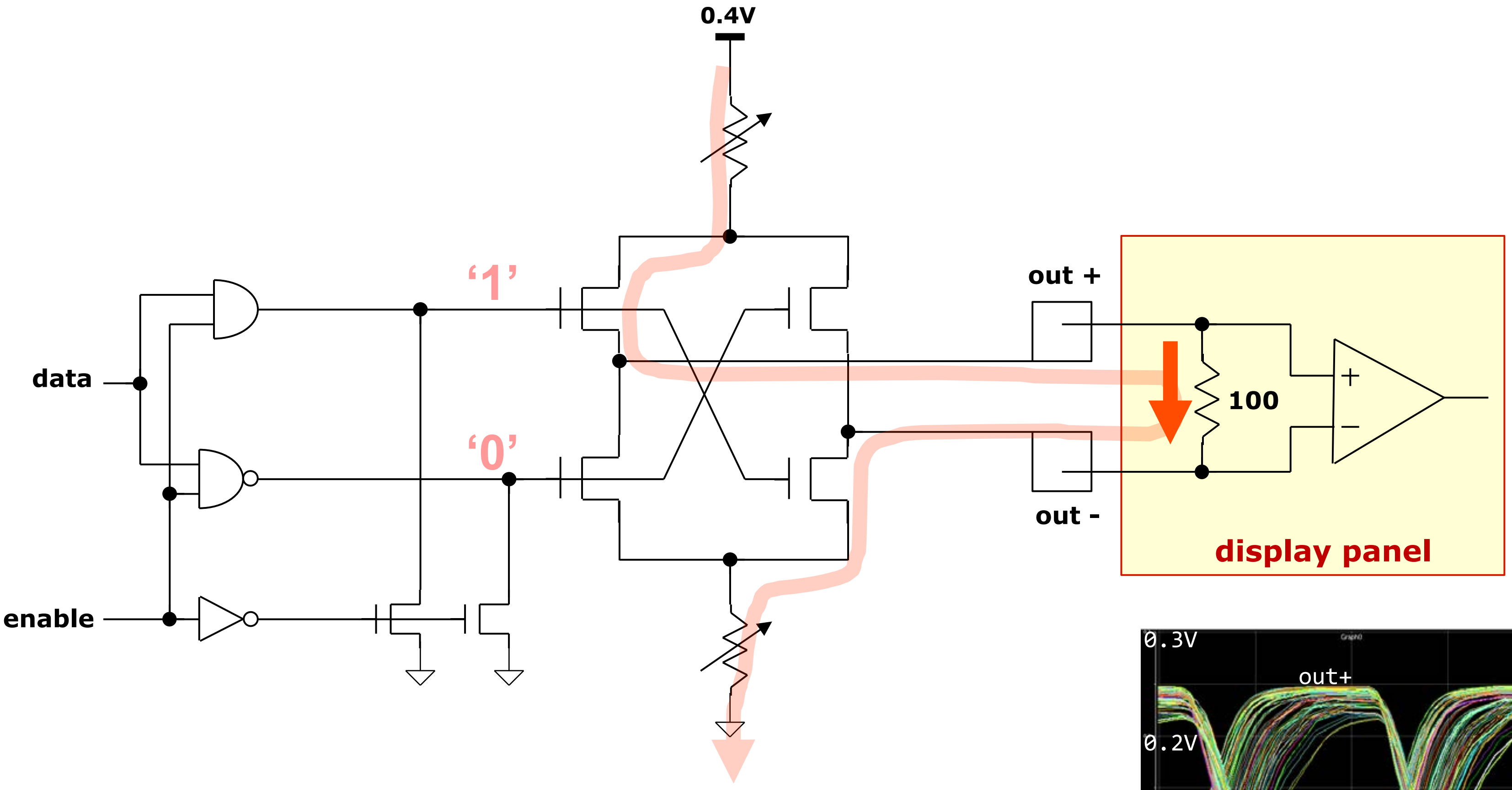
Input Differential Receiver

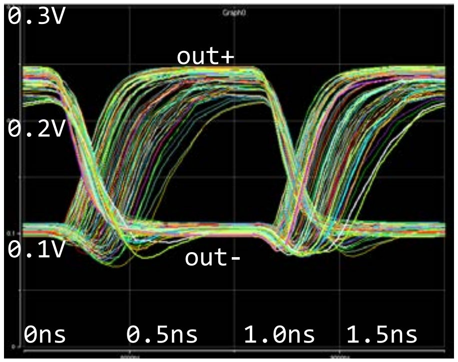


HDMI Differential Output Stage



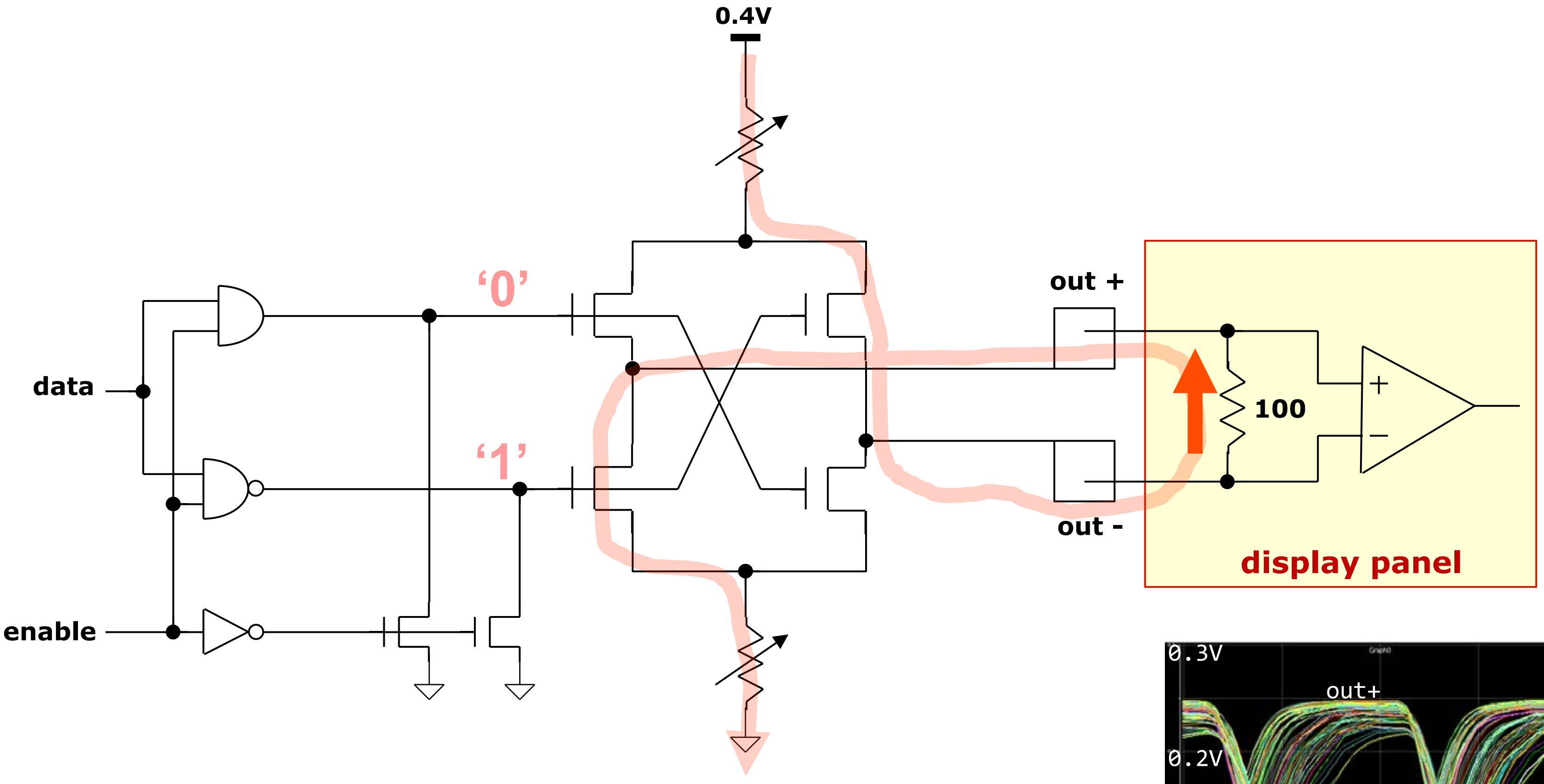
MIPI-DSI Differential Output Stage

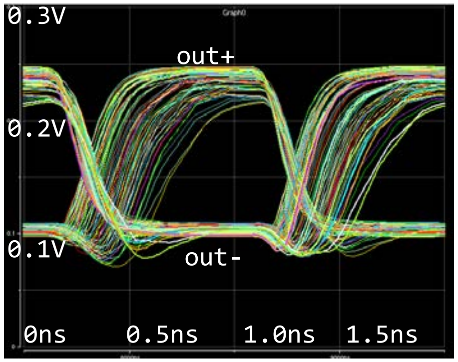




Simulations across process, temperature and +/- 10% voltage tolerance for a 1Gbps interface.

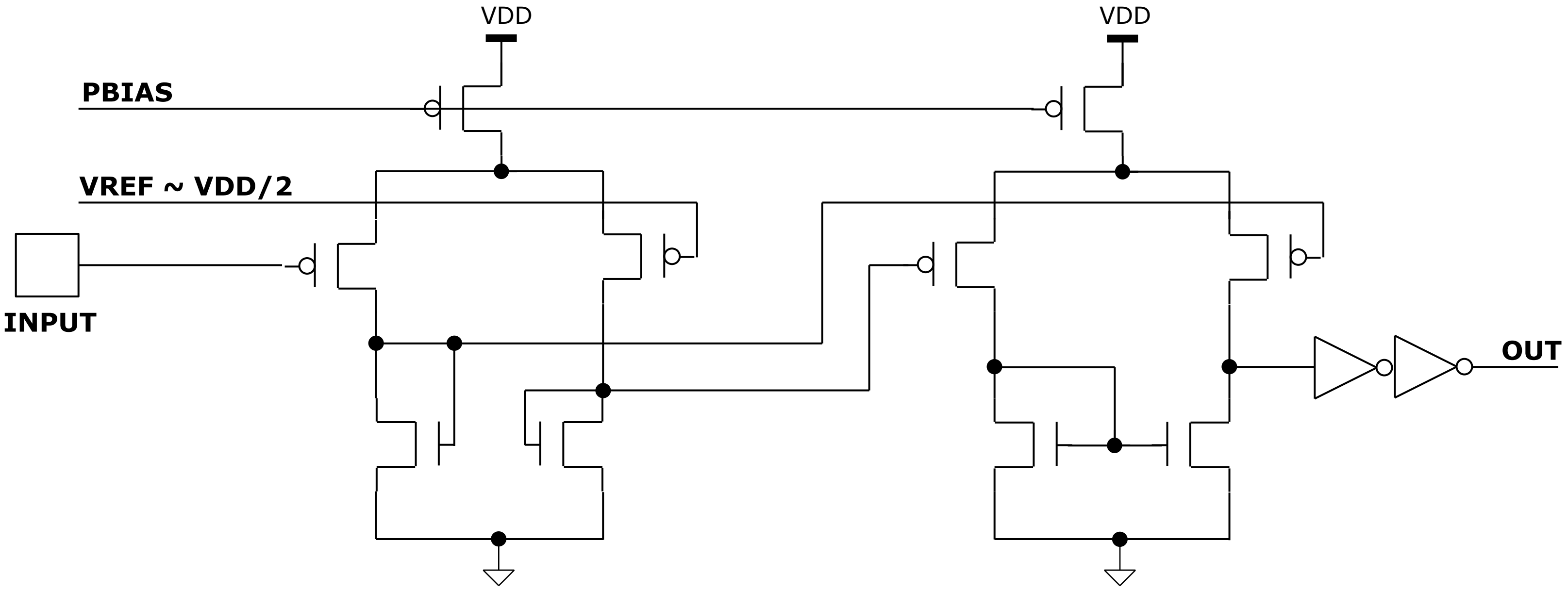
MIPI-DSI Differential Output Stage



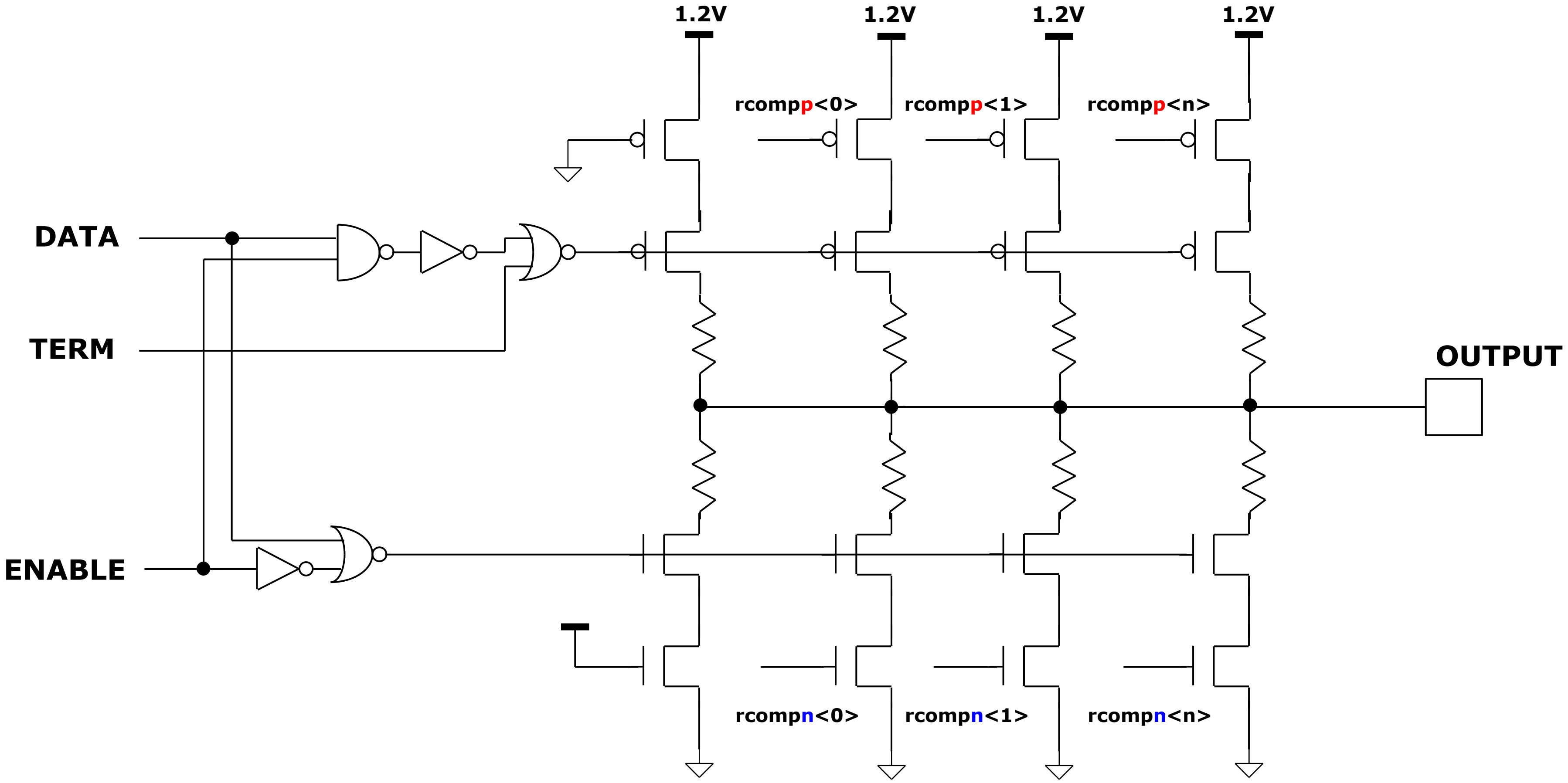


Simulations across process, temperature and +/- 10% voltage tolerance for a 1Gbps interface.

LPDDR Input Receivers



LPDDR Output Drivers



SUMMARY

- OFF-CHIP drivers/receiver clocking come in two ‘flavors’:
  - Common clock
  - Source synchronous
- Transmission-line behavior is observed due to fast edge rates/fast flight times.
  - Edge rate control and resistance compensation are 2 of the most important design techniques to achieve good signal quality at high transfer rates.
- Modern SoC designs need to ‘accommodate’ several IO voltage levels; level shifters and ESD protection for multiple power supplies are required.
- Low swing differential drivers/receivers are used for very high speed rates (HDMI, MIPI-DSI, MIPI-CSI are examples).

References

- Rumi Zahir, 'Medfield Smartphone SoC Intel Atom Z2460 Processor', HOT CHIPS #24, August 2012.

- F. Garcia, et. al., 'Design of a Slew Rate Controlled Output Buffer' IEEE, 1998, pp. 147-150.

- Chandrakasan, Bowhill, Fox, 'Design of High Performance Microprocessor Circuits', IEEE Press, pp. 377-395.